Semiconductor Optical Amplifier Integrated on Silicon Photonic Chip using Photonic Wire Bonds

by

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The following individuals certify that they have read, and recommend to the Faculty of Graduate and Postdoctoral Studies for acceptance, the thesis entitled:

Semiconductor Optical Amplifier Integrated on Silicon Photonic Chip using Photonic Wire Bonds

submitted by **Tianye Wang** in partial fulfillment of the requirements for the degree of **Master of Applied Science** in **Electrical and Computer Engineering**.

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Abstract

Photonic Integrated Circuits (PICs) have made remarkable strides, enabling the realization of complex optical functions within a compact and highly reliable framework. However, high-performance PICs often suffer from significant insertion losses due to numerous optical components. Semiconductor Optical Amplifiers (SOAs) are essential for offsetting these losses, providing amplification of optical signals via stimulated emission. SOAs operate over wide wavelength bands (e.g., 1480nm to 1560nm) and are relatively inexpensive, offering substantial gains. While there are several approaches to integrating SOAs onto silicon photonic chips, including monolithic and hybrid integration, the former presents challenges in manufacturability and cost. In this work, we propose a flexible hybrid integration of SOAs onto silicon photonic chips using Photonic Wire Bonds (PWBs). PWBs are three-dimensional, nano-printed, freeform polymer waveguides that facilitate efficient coupling between optical components with high alignment tolerances and comparatively low insertion losses. The proposed integration method effectively compensates for the significant insertion losses in high-performance PICs, demonstrating its potential for enhancing the performance and reliability of these advanced photonic systems.

Measurements on a connectorized SOA are presented, showing a peak on-chip gain of 10.6dB at 1510nm when applying a 150mA bias current to it. The PWB-connectorized SOA has a wavelength-dependent gain which was measured from 1480nm to 1555nm, the peak gain being obtained at 1510nm. In addition, the gain depends on the bias current applied, increasing with higher bias currents but saturating when the bias current exceeds 150mA. The PWB-connectorized SOA is also sensitive to the power of the input signal, the gain was larger for lower input powers. Varying the polarization state of the input to our PWB-connectorized SOA changed the measured gain by 5.85dB. Additionally, a comparative study of a second SOA sample was conducted to validate the results and ensure measurement reliability.

Lay Summary

Photonic Integrated Circuits (PICs) have achieved significant advancements, enabling complex optical functions within a compact and highly reliable framework. However, high-performance PICs often suffer from considerable insertion losses due to numerous optical components. To address this, we demonstrate the integration of near-C-band semiconductor optical amplifiers (SOAs) onto silicon photonic chips using photonic wire bonds (PWBs). This integration significantly enhances optical communication systems by improving data transmission rates, reducing latency, and increasing bandwidth. This technology contributes to energy efficiency and cost reduction in photonic integrated circuits, while enabling miniaturization and integration for more compact and efficient devices. Overall, this integration represents a step forward in addressing the growing demands of our digital society.

Preface

This thesis is based on the publication "Semiconductor Optical Amplifier (SOA) Integrated on a Silicon Photonic Chip Using Photonic Wire Bonds (PWBs)" [1], for which Becky Lin proposed the initial idea and conducted the preliminary tests on photonic wire bonding with SOA. I then led the sample fabrication and measurements. Additionally, I took the lead in writing the manuscript, with co-authorship and editing contributions from Becky Lin, Professor Nicolas Jaeger, and Professor Lukas Chrostowski.

Chapter 2 is based on work conducted by Becky Lin, Matthew Mitchell, Sheri Jahan Chowdhury, and me in UBC's Photonics and Nanostructures Laboratory. Becky Lin contributed to the design of the layout structure, Sheri Jahan Chowdhury was responsible for the in-house SiP chip fabrication, and I led the die bonding process and fiber assembly. Matthew Mitchell and I collaborated on the photonic wire bonding.

Chapter 3 is based on a paper published in Photonics West [1]. I conducted all the work presented in Chapter 3, which includes designing a set of experiments, setting up the experimental apparatus, conducting measurements, and performing data analysis. I also developed a Python script to automate the measurements. For sample 2, I led the post-fabrication process, including die bonding, fiber assembly, and photonic wire bonding. I then repeated the experimental setup, measurements, and data analysis for Sample 2.

Chapter 4 is based on simulations conducted by me. I led the simulation of a traveling wave laser using ANSYS Lumerical FDE MODE and Lumerical INTERCONNECT.

Table of Contents

List of Figures

List of Abbreviations

2PP	Two Photon Polymerization
ASE	Amplified Spontaneous Emission
CMOS	Complementary Metal-Oxide Semiconductor
DRIE	Deep Reactive Ion Etching
EDFA	Erbium Doped Fiber Amplifier
FDE	Finite-Difference Eigenmode
FPA	Fabry-Perot Amplifier
MQW	Multi-Quantum Well
OFA	Optical Fiber Amplifiers
PIC	Photonic Integrated Circuit
PWB	Photonic Wire Bond
RIE	Reactive Ion Etching
SiP	Silicon Photonic
SOA	Semiconductor Optical Amplifier
SOI	Silicon-On-Insulator
SMF	Single Mode Fiber
SMSR	Side Mode Suspension Ratio
TWA	Traveling-Wave Amplifier

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I would like to express my deepest gratitude to my supervisor, Professor Nicolas Jaeger, for his unwavering support and guidance over the years. He provides me with the opportunity to pursue graduate studies and introduce me to the world of silicon photonics. I am also very thankful to Professor Lukas Chrostowski for his insightful discussions, feedback, and suggestions for my research. My thanks extend to Professor Sudip Shekhar for serving on my supervisory committee.

Special thanks to Matthew Mitchell for his mentorship in nanofabrication and for our many discussions on research questions. His experience and knowledge have been incredibly beneficial. I am grateful to Malcolm Haynes from the Advanced Nanofabrication Facility for his mentorship, discussions, and feedback. I also want to thank Iman Taghavi for guiding me through experiments and generously sharing his insights and skills. Their assistance has been invaluable during my graduate studies.

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Chapter 1

Introduction

1.1 Silicon Photonics

The advancement of electronics miniaturization has brought substantial benefits to our modern information society. Beginning in 1965, scientists pioneered the integration of transistors onto a single chip, marking the inception of Moore's Law. This principle, articulated by Dr. Moore, predicted that the number of transistors on a silicon chip would double approximately every two years. Over time, silicon has become the material of choice for the complementary metal-oxide semiconductor (CMOS) industry [2]. Today, the minimum feature size achieved in CMOS is less than 10nm, resulting in not only a seven orders of magnitude reduction in the cost of transistors but also an increase in transistor density by at least 10 orders of magnitude [3].

Silicon photonic chips serve as versatile platforms for integrating photonic systems. They leverage silicon-on-insulator (SOI) wafers, which facilitate low loss and highly efficient optical confinement on the chip. This confinement is achieved through the high refractive index contrast between silicon and silicon dioxide, and it enables the dense on-chip integration of optical components [4]. Silicon photonics primarily involves the study and application of photonic systems that utilize silicon as an optical medium. Scientists such as Soref and Petermann played a leading role in advancing silicon photonics in the late 1980s and early 1990s. The early work predominantly focused on the development of passive devices in 1990s, including optical directional couplers, optical waveguide switches, and Mach-Zehnder interferometers [2][5][6][7][8][9].

The development of silicon photonics has experienced a significant acceleration since 2004, driven by substantial investments from both government and industry. Notably, the Defense Advanced Research Project Agency (DARPA) initiated two laser projects as part of the Terahertz Technology Program, making a major investment in 1.55μm wavelength silicon photon-

ics [10].

1.2 Photonic integrated circuits

Photonic integrated circuits (PICs) comprise two or more photonic components on a single chip, collectively forming a functional circuit. Unlike electronic integrated circuits that employ electrons, PICs use photons for their operation. Contrary to metallic electronic circuits, PICs are composed of various devices on various optically clear materials.

Silicon's optical properties, including its transparency in key infrared wavelength bands, make it an excellent material platform for large-scale PICs. Silicon photonics capitalize on the extensive investment and research dedicated to silicon semiconductor device processing, resulting in high yield, robust manufacturing, and low-cost production [11]. Silicon photonics has relied on Silicon-on-Insulator (SOI) as the primary integration platform, enabling the implementation of various passive and active devices. However, silicon platform lacks a crucial component for achieving a fully functional photonic integrated circuit: an integrated laser.

Indium phosphide (InP) serves as a prominent material platform for PICs. Advances in InP components have not only led to the introduction of the first InP-based PICs with a few integrated functions but have also significantly improved the performance and commercial availability of discrete devices. InP-based PICs offer the capability to deliver the sufficient functionality, performance, and cost reductions similar to the inherent advantages provided by Si-based integrated electronics [12].

1.3 Semiconductor Optical Amplifiers (SOAs)

In today's contemporary landscape of optical communication networks, communication across metropolitan areas as well as long distance international networks has become widespread. However, the propagation of light through optical fibers introduces attenuation, resulting in signal power loss that limits the transmission distance. Optical amplifiers serve as crucial power boosters, not only compensating for the signal loss, but also enhancing receiver sensitivity within the optical network [13].

1.3.1 Optical amplifiers

There are basically two types of optical amplifier: Optical Fiber Amplifiers (OFAs) and Semiconductor Optical Amplifiers (SOAs). The most common type of OFA is the Erbium Doped Fiber Amplifier (EDFA). EDFAs use a fiber as the gain medium. The gain is achieved by the stimulated emission of photons. In the EDFA, erbium ions and pumped light from an external laser diode are added to the core of the optical fiber to process the stimulated emission, enabling an amplification of incident light. EDFAs offer high gain, low noise, and polarization independence, but they require an external pump laser. As such, EDFAs are not compatible with integration on PICs. On the other hand, SOAs use a semiconductor as the gain medium and also operate by amplifying light through stimulated emission (further details on the operating principles are described in Chapter 3.2). While SOAs may have poorer gain and noise compared to EDFAs, they have rapidly improved their performance in the last decade. SOAs are not only compatible with integration on PICs, but also work as functional devices, such as for wavelength conversion and optical demultiplexing, making them suitable for wide range of applications. The Semiconductor Optical Amplifier is a key device for next-generation, all-optical networks [14].

1.3.2 Types of SOA

The initial investigations into semiconductor optical amplifiers were conducted in the 1960's, coinciding with research on semiconductor lasers. Early work on SOAs, primarily based on GaAs, was carried out by Zeidler and Personick. This early research targeted optical communication systems operating at low temperatures [15].

There exist two primary types of semiconductor optical amplifier: Fabry-Perot Amplifiers (FPAs) and Traveling-Wave Amplifiers (TWAs). The operating principles of FPAs resemble those of Fabry-Perot lasers. In an FPA, as shown in Fig.1.1 (a), input light undergoes amplification as it reflects back and forth within the active region before being emitted at higher intensity. FPAs exhibit high gains and narrow bandwidths, but they are sensitive to variations of the operating temperature and the input optical frequency. In contrast, TWAs, shown in Fig.1.1 (b), the input light propagates through the active regions, getting amplified through stimulated emission, only once. Several approaches have been employed to eliminate reflection including applying the antireflection coatings and/or tilting the active region with respect to facets [14]. The gains of TWAs can be enhanced by increasing

the length of the active regions. Additionally, TWAs exhibit wide optical bandwidths and low polarization sensitivities.

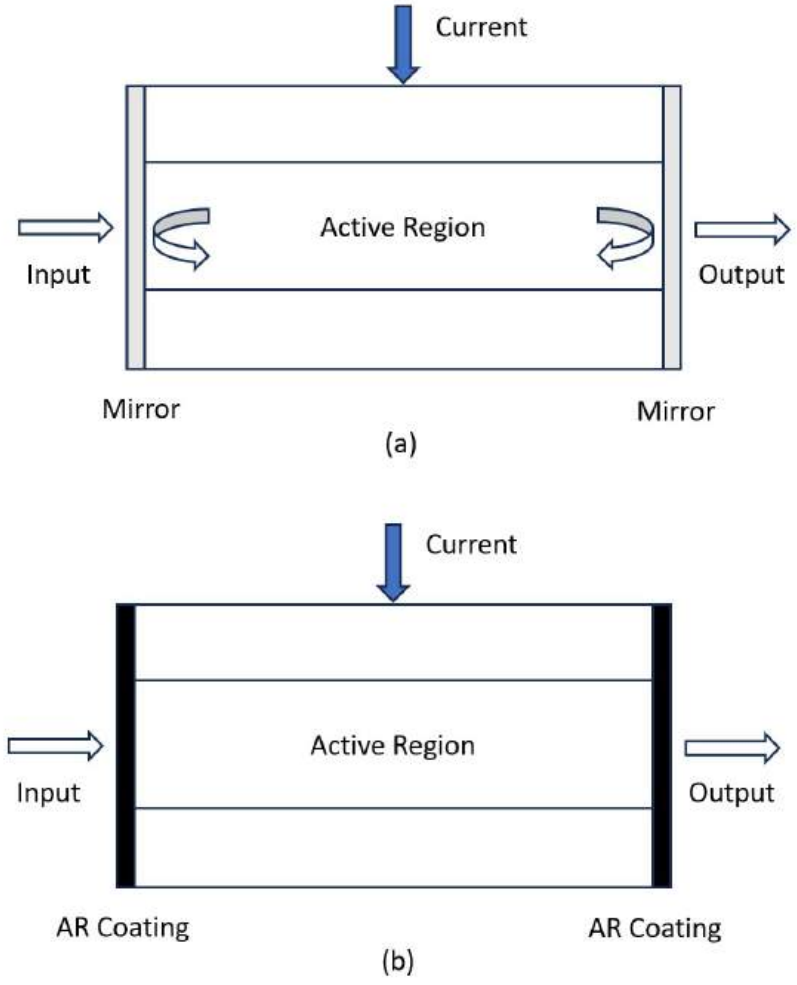

Figure 1.1: Structure of two different types of semiconductor optical amplifier: (a) Fabry-Perot Amplifiers (FPAs), (b) Traveling-Wave Amplifiers (TWAs).

1.3.3 SOA functionality

In the context of sub-micron systems, high performance PICs often contain many functional optical components with significant insertion losses. SOAs are devices that can provide amplification of optical signals to compensate these insertion losses. There are numerous applications of SOAs in telecommunication systems.

SOAs also serve various other functions. For example, SOAs can be used as optical switches due to their fast-switching speed and ability to achieve a high extinction ratio [16]. Additionally, SOAs can function as wavelength converters, translating optical signals from one wavelength to another [17]. Furthermore, SOAs can serve as gain media in wavelength-tunable and multiwavelength lasers. In order to achieve the wavelength tunability, external cavities, like Fabry-Perot cavities and fiber Bragg gratings based cavities, are used [18].

1.4 Photonic Wire Bond (PWB))

In the field of microelectronics, the evolution of electrical wire bonding has not only improved the electrical interfaces between integrated circuits, but also brought about economic enhancements. Photonic wire bonds (PWBs) extend the concept of electrical wire bonds to create 3D, freeform, polymer waveguides connecting photonic components such as fiber arrays, lasers, SOAs, and integrated photonic chips. They also facilitate connections for fiber/chip to free-space optics and cryogenic interconnects.

Photonic wire bonding is a fast optical connection method that usually takes 30 to 120 seconds to write a connection between two components. PWBs allow for flexible interconnects between various material platforms and components to be formed. Additionally, PWBs offer low insertion losses; for example, a typical chip-to-chip insertion loss is 0.7dB $\pm$ 0.15dB [19], and a typical chip-to-fiber insertion loss is 1.6dB $\pm$ 0.13dB [20]. PWBs are easy to use due to their high alignment tolerances. The shape of a PWB is adapted to the positions of the connected components' facets. Furthermore, it is easy to design the structures as well as the mode field sizes of PWBs. PWBs are also compact and mechanically stable.

There are two methods commonly used by PWBs for light coupling into and out of optical components: surface coupling and edge coupling. Surface coupling methods, as illustrated in Fig.1.2 (a), rely on evanescent field cou-

pling, which requires physical contact between the polymer waveguide and the on-chip waveguide (i.e., the silicon waveguide on a silicon photonic chip, from now on I will assume that we are working on silicon photonic chips). In this approach, the silicon waveguide undergoes a tapering process to extract the mode from the silicon layer and expand the mode size. A polymer taper is overlaid onto the silicon waveguide taper to capture the expanded mode. In order to achieving physical contact, an "oxide-open" process is required to expose the silicon waveguide. On the other hand, edge coupling methods, depicted in Fig.1.2 (b), involve directly attaching the polymer waveguide to a facet of the silicon waveguide. In comparison to surface coupling, edge coupling is simpler, as it eliminates the need for the oxide opening process which many foundries don't offer [21].

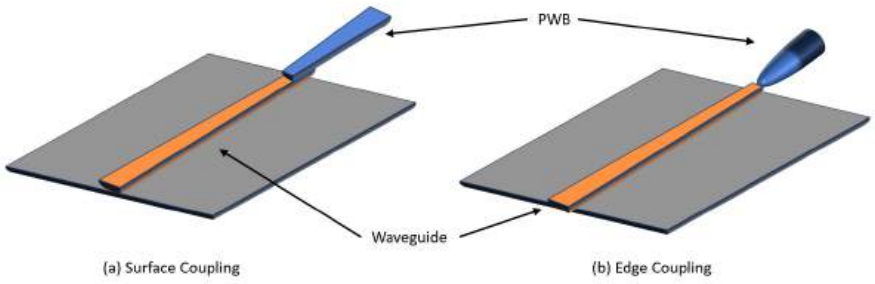

Figure 1.2: Coupling method of PWB: (a) Surface Coupling, (b) Edge Coupling.

Fig.1.3 shows a 3D model of a PWB. The PWB illustrated is comprised of three parts, a mode coupler, a constant cross-section waveguide, and a mode size convertor. For example, the mode coupler couples the light from the silicon chip/SOA into the PWB. Then, a constant cross-section waveguide guides the lights to compensate for the spatial mismatch between two facets in the x, y, and z directions. Lastly, at the end of the PWB, a mode size convertor functions like a taper, changing the mode size of the constant cross-section waveguide to match the mode size of single mode fiber (SMF) [21]. The mode size convertor can also be used to change the mode size of constant cross-section of waveguide to match a surface taper(shown as ST in Fig.2.2). An anchor, made using same material with PWB, is used to

secure the PWB to the facet of the chip for enhancing mechanical stability.

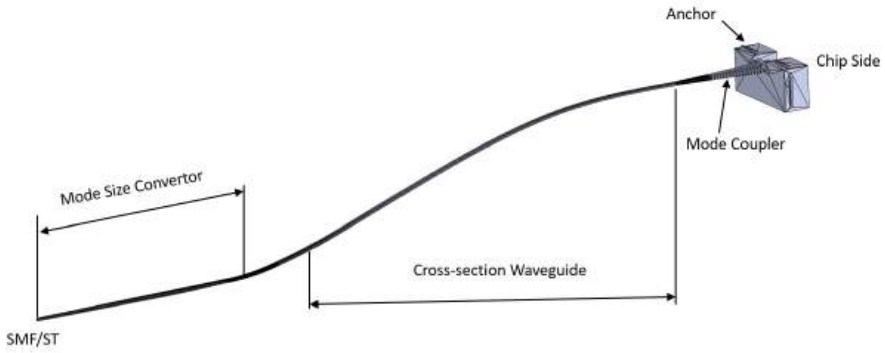

Figure 1.3: 3D structure of PWB coupling between SOA and PIC.

1.5 Thesis Overview

This thesis explores the performance of a semiconductor optical amplifier that is integrated onto a silicon photonics chip using photonic wire bonds. The remaining sections of the thesis are organized into three main chapters:

Chapter 2 details the design and fabrication process of SOA integration onto a SiP chip. This includes the layout structure design, the SiP chip fabrication process, the die bonding process for placing the SOA onto the SiP chip, the fiber array assembly, and the photonic wire bonding.

Chapter 3 introduces the motivation for integrating the SOA onto the SiP chip and the fundamental principles of SOA operation. It describes the design, setup, and execution of experiments to analyze and characterize the performance of the on-chip SOA under various operating conditions. Additionally, another sample is fabricated and compared with differences and improvements analyzed.

Chapter 4 demonstrates the simulation of a traveling wave laser. The simulation is performed using ANSYS Lumerical FDE MODE and Lumerical INTERCONNECT. It analyzes the effects of variations in cavity length, facet reflectivity, and temperature on the lasing threshold point.

Chapter 2

Fabrication

2.1 On-chip SOA Layout Structure

This section presents the designed layout structure for the on-chip integration of the SOA. The layout was created using KLayout, a CAD software specifically developed for layout designing, viewing, and editing. The overall layout structure is shown in the Fig.2.1. It is 3000 μm long and 1600 μm wide, and it features a cavity that is 1080 μm long, 480 μm wide, and 100 μm in depth. The figure on the right shows the gold-plated cavity, silicon photonic waveguides, and surface tapers used for the integration. Meanwhile, the figure on the left provides a detailed "zoom-in" view of the SOA mounted within the gold-plated cavity. Fig.2.2 shows the layout structure of the surface taper. It consists of two diagonal squares and a taper. The two diagonal squares are used for automated image detection by the PWB machine. They also help in alignment. The taper is used for terminating waveguides for adiabatic coupling to the PWBs.

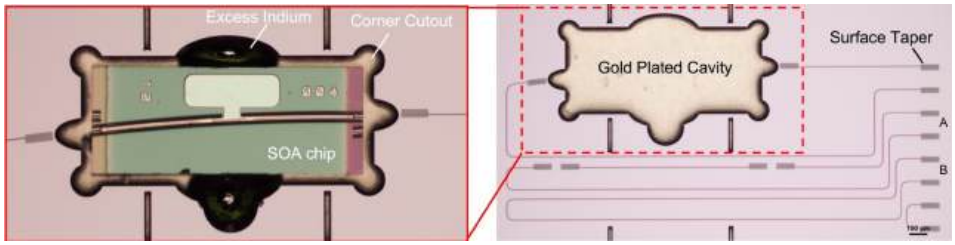

Figure 2.1: Layout of the in-house fabricated silicon photonic chip with a gold-plated cavity for on-chip SOA integration. Surface tapers, indicated by gray rectangles, terminating the on-chip silicon waveguides allow for adiabatic coupling to and from PWBs.

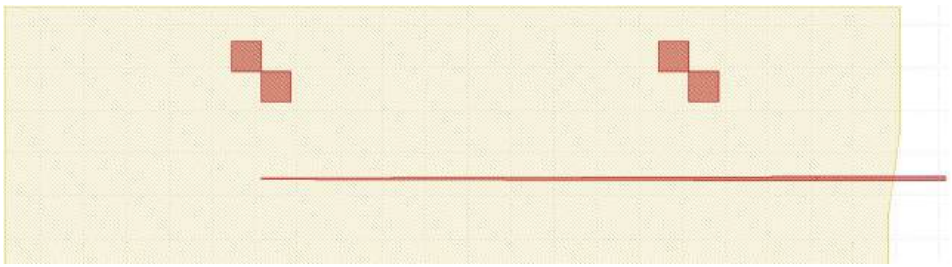

Figure 2.2: The Layout Structure of a surface taper that used for coupling of PWB.

The SOA used in this research is 1000 μm long, 400 μm wide, and 100 μmm in depth. To facilitate the integration of the SOA onto a silicon chip, a cavity was patterned and etched into the silicon substrate with a depth of 100 μmm. The reason for designing the cavity depth to be the same as the SOA height is to ensure that the SOA facet is slightly higher than the chip surface. As illustrated in Fig.2.3, due to the surface coupling method used, the PWB should physically contact the on-chip waveguide. If the SOA facet is lower than the surface of the chip, it will decrease the bending radius of the PWB and cause higher insertion loss. Subsequently, metallization was done inside the cavity. Following the metallization, a die bonder was used to deposit indium solder into the cavity to establish a permanent electrical contact with the bottom of the SOA chip. The width and length of the cavity are designed to be slightly larger than the size of the SOA to allow sufficient clearance from the fillet of the cavity corners. Also, the slightly larger size of the cavity provides enough space for writing a PWB. Insufficient space may decrease the bending radius of the PWB and increase the insertion loss [21]. Corner reliefs, in the form of extra circular cutouts, are added to the corners to ensure a fully flattened cavity base. Additional cutouts on the longitudinal sides of the cavity provide reservoirs for excess indium solder. Lastly, cutouts at the SOA input/output provide space for freeform PWBs to connect the SOA to the silicon waveguides [1].

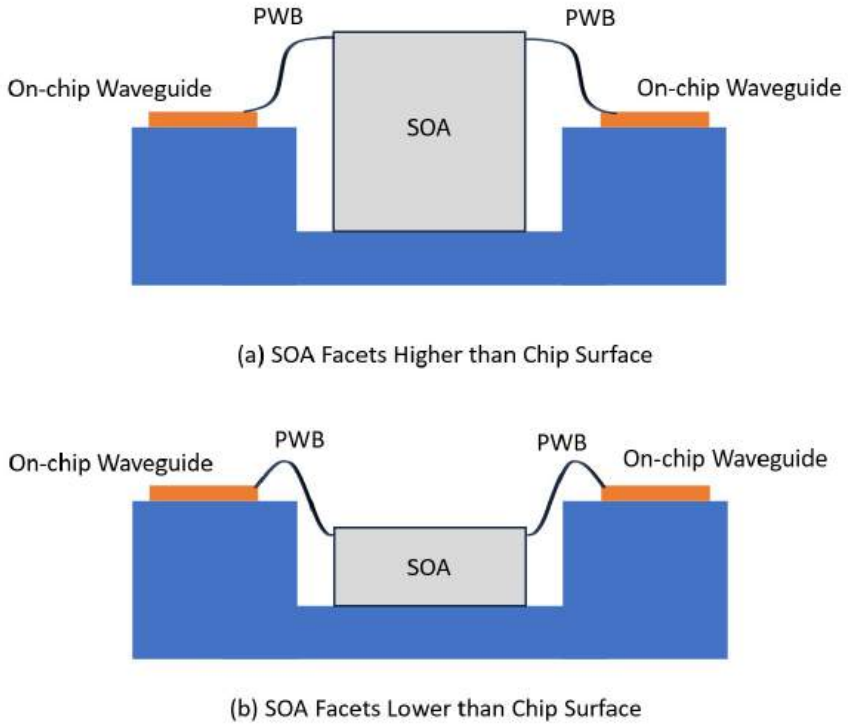

Figure 2.3: Cross section of SOA integration onto SiP chip: (a) SOA facets higher than chip surface, (b) SOA facets lower than chip surface

As shown in Fig.2.4, an array of eight surface tapers is placed at the edge of the chip for connection to an 8-channel, single mode, fiber array via photonic wire bonding, six of which are used for three different loopback structures that allow us to calibrate the gain through the SOA. A short loopback device is used to estimate the loss through the fiber-to-surface taper PWB interface. A longer loopback device, device B, shown in Fig. 2.1 with relatively the same optical path length as the SOA device is used to characterize waveguide loss in addition to the fiber-to-surface PWB loss. Lastly, long loopback device, device A, shown in Fig.2.1 with two surface taper-to-surface taper bonds is used to help characterize loss through the full optical path of the SOA device.

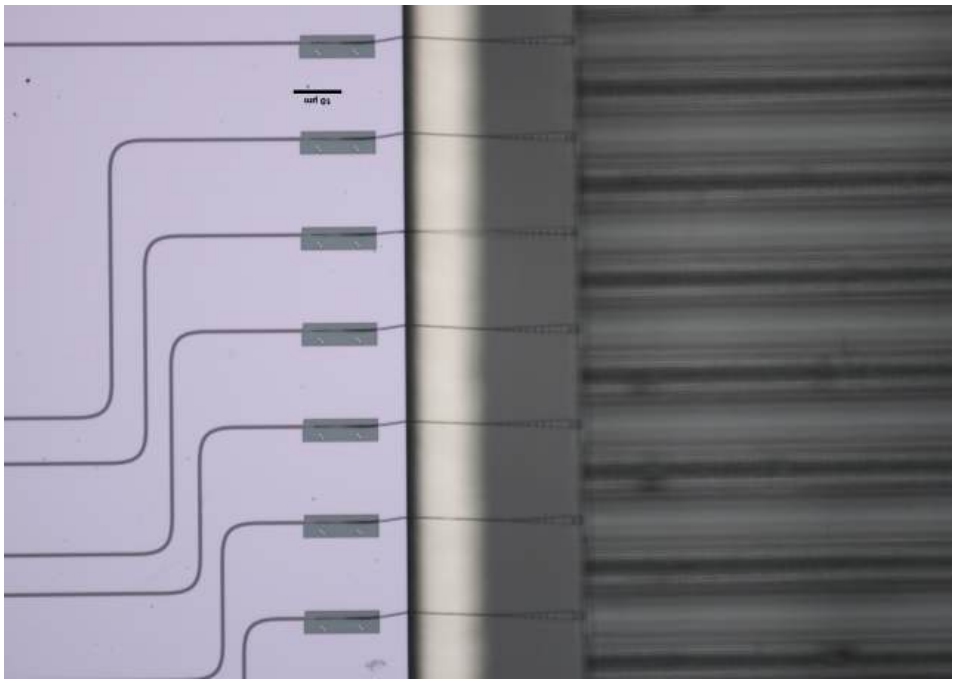

Figure 2.4: Micrograph of PWB coupling between Fiber array and SiP chip

2.2 Detail Fabrication Process

2.2.1 Fabrication of the Silicon Photonic Chip

Fig.2.5 shows the main cross-section of the SiP chip as described in Section 2.1 (please note that the figure is not drawn to scale). The designed chip was fabricated using the same fabrication as for on-chip laser integration [22] where the SiP waveguides were patterned and etched using EBeam lithography (JEOL JBX-8100FS) and ICP-RIE etching (Oxford PlasmaPro 100 Cobra) while the cavity was patterned and etched using maskless lithography (Heidelberg MLA-150) and Bosch etching (SPTS Rapier DRIE). Following the deep trench etching, metallization was done through the deposition of a thin layer of gold at the bottom of the cavity. Note that the oxide open process is demonstrated on top of silicon waveguide for light coupling in/out the waveguide through PWB surface taper (See Section 2.1).

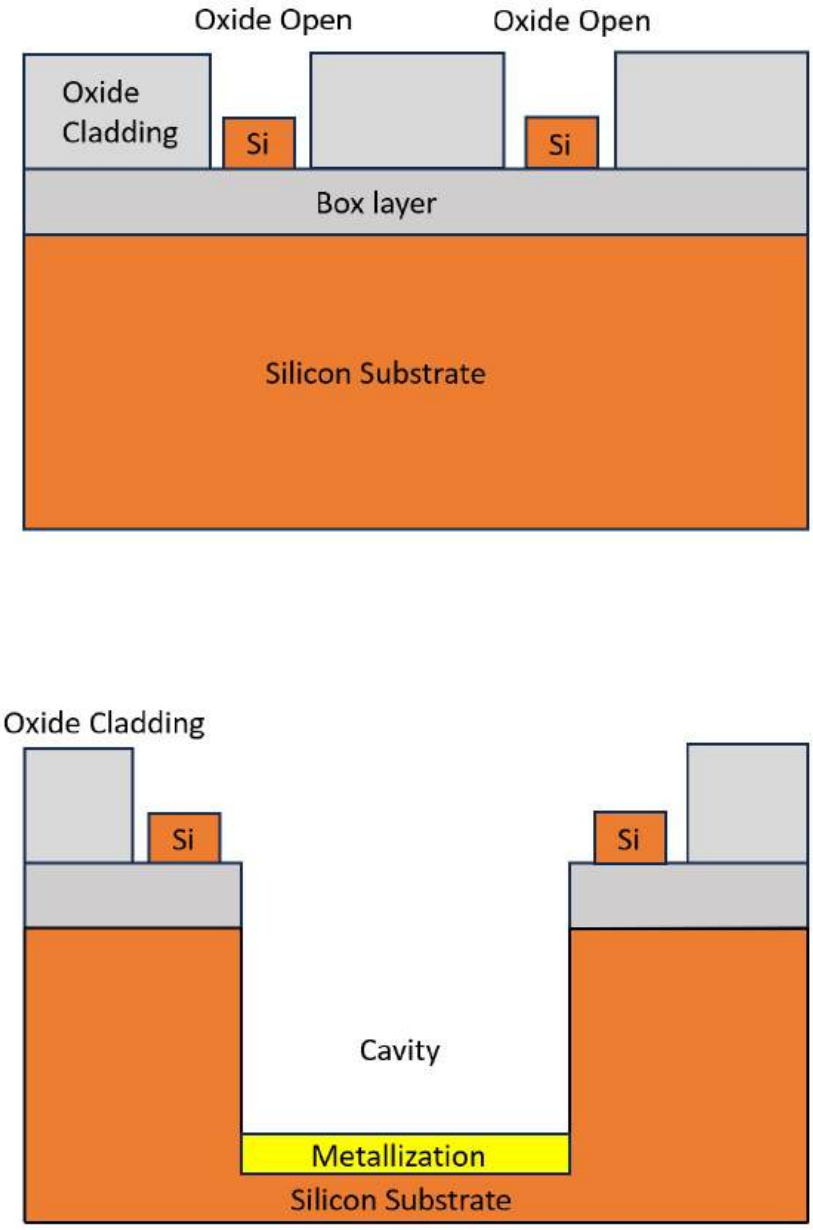

Figure 2.5: Cross section of a SiP chip based on SOI wafer (In-house fabrication). Oxide openings above the silicon waveguide are for PWB surface taper to coupler light in/out the waveguide. Recessed cavity is etched for placing SOA.

2.2.2 Die Bonding process

Following the fabrication of the SiP chip, the initial post fabrication step involves integrating the SOA into the cavity using a flip-chip die bonder (Tresky T-3000 Pro). Fig.2.6 shows the indium solder and the SOA placed in the cavity. The pickup tool is meticulously cleaned to ensure precision and accuracy. However, excessive cleaning force can tilt the angle of the pickup tool, leading to unsuccessful pickups. Subsequently, a package used for Indium die-pack and SOA is positioned on the workholder (Fig.2.7), and the vacuum is activated to ensure its stability on the workholder. The machine can be controlled either automatically or manually, allowing for the pickup and placement of the Indium solder into the cavity. Next, the SOA is picked up and placed on top of the Indium solder while heating is initiated. The heating is applied to both the pickup tool and the substrate. A software program is utilized to control the temperatures and heating times of the pickup tool and substrates. Typically, the temperature of the pickup tool is set to 0 °C to prevent damage to the SOA. Higher temperatures and pressures can harm the top cladding layer and potentially damage the cavity, which may affect the performance and stability of the SOA. While the substrate temperature is set to 310 °C, which is above the melting point of indium, to melt the indium solder. The heating time is set to 30 seconds to ensure it reaches the target temperature of 310 °C, extended heating time can lead to increased intermetallic growth between the indium solder and the chip's bottom metallization layer.

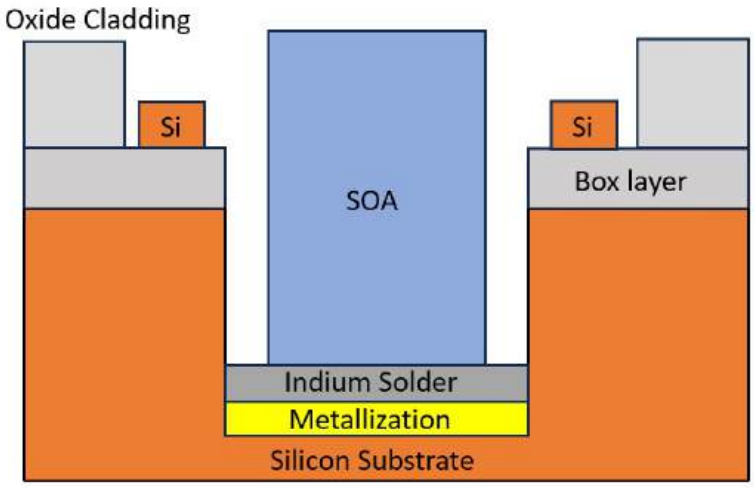

Figure 2.6: Cross section of SOA integration onto SiP chip, including oxide opened process, cavity etched, metallization, solder performed, and SOA placed in the cavity.

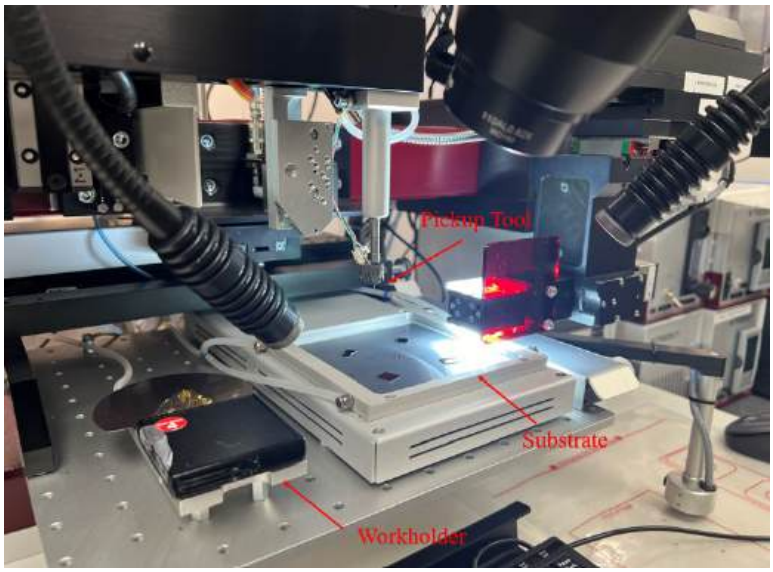

Figure 2.7: Actual Diebonder Setup

2.2.3 Fiber assembly

After affixing the SOA to the cavity, an 8-channel fiber array and the SiP chip were assembled onto a common silicon sub-mount. The fiber array is positioned in close proximity to the chip, the distance between the chip and fiber array is measured under a microscope. Utilizing a micro-positioner and a probe needle to we adjust and align the fiber array's facets to the tips of the surface tapers. Here, precise alignment is not required as the PWB accommodates a relaxation in alignment accuracy of more than 30 μm, but good alignment allows for increased bent radii of the PWBs, which in turn allows for lower insertion losses. Additionally, maintaining a gap of approximately 250 μm between the chip and the fiber array is preferable in order to minimize the insertion losses of the PWBs. After x and y plane alignment, the height offset becomes another important consideration. The core of the fiber array should be slightly elevated above the chip surface (about 30 μm) to increase the bend radii of the PWBs. Lastly, UV-cured glue is applied to secure the position of both the SiP chip and fiber array.

2.2.4 Fabrication of PWB

The PWB fabrication process is described in this section. In the first step, the SOA and silicon photonic chip, including the sub-mount, is cleaned using isopropyl alcohol (IPA) to eliminate any organic residues and dust. Following the cleaning, the sub-mount with the SiP chip is positioned within a 3D direct laser writing lithography system. A droplet of photoresist is then applied to the gaps between the SOA and SiP chip, as well as between the SiP chip and the fiber array. A focal lens is immersed in the photoresist droplet to facilitate the confocal scan and pattern recognition, enabling the measurement of the facets' positions on both the SOA and SiP chip. Confocal scan works by focusing a laser beam onto a specific point on a sample and using a pinhole to block out-of-focus light. The sample is scanned point by point, and the emitted light from each point is detected and processed to create a two-dimensional image. By moving the focal plane through the sample, multiple images at different depths are captured. These images can be compiled into a three-dimensional reconstruction, allowing detailed visualization of the sample's internal structures [23]. The shape of the PWB is subsequently calculated based on the measured coordinates of the facets, and the PWB is automatically generated and exposed by using two-photon polymerization. The sample is then developed in PGMEA (1-methoxy-2-propanol acetate) for 15 minutes to remove the unexposed photoresist. Next,

the sample is placed in IPA for 10 minutes to remove the PGMEA. Finally, a cladding is applied to ensure long-term reliability and protection of the PWBs. Fig.2.8 shows the final cross-section of the sample.

Fig.2.9 shows the fabricated PWB. It is clearly visible that the PWB has an elliptical shape. Similar to a polarization-maintaining (PM) fiber, the PWB uses birefringence to maintain the polarization state of light over long distances. The PWB achieves this by having a contrast between the vertical and horizontal refractive indices, enabling it to maintain polarization.

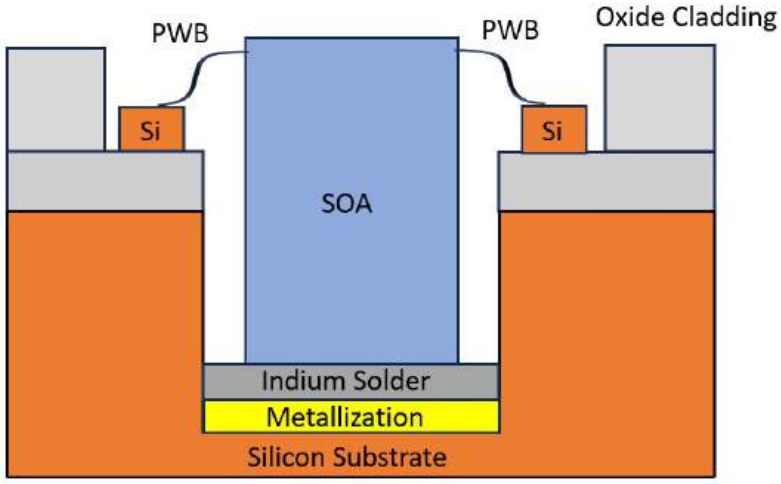

Figure 2.8: Overall Cross section of SOA integration onto SiP chip using PWB

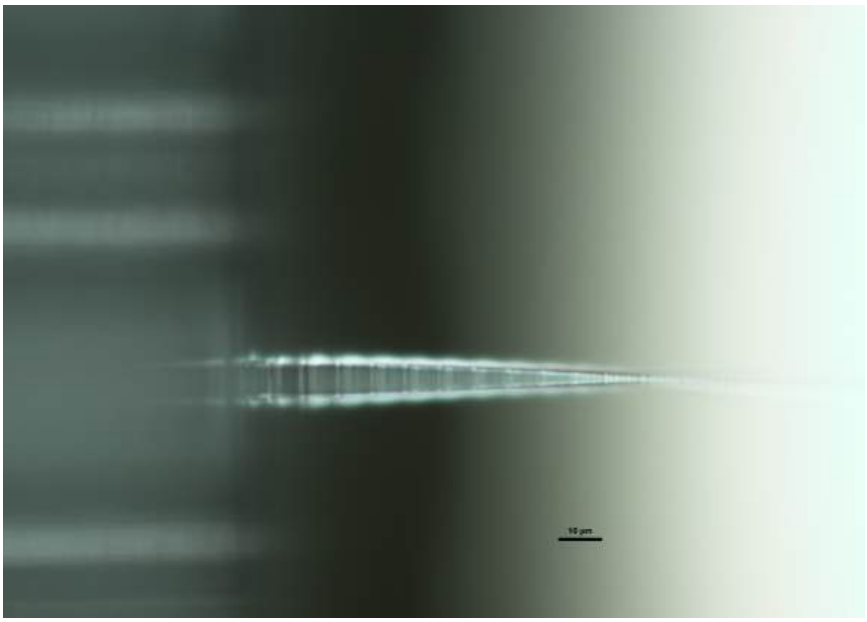

Figure 2.9: Micrograph of structure of PWB

The fabrication of 3D freeform polymer waveguides follows a layer-by-layer process, utilizing a model generated by Computer-Aided Design (CAD) tools. The manufacturing process leverages Three-Dimensional Direct Laser Writing (3D DLW) based on Two-Photon Polymerization (2PP). 2PP enables the fabrication of 3D structures directly from CAD models. A femtosecond laser plays an important role in 2PP, providing laser pulses. This non-linear process relies on the absorption of two photons in a photosensitive material (photoresist). Fundamentally, two-photon polymerization requires high intensity, where the resist is polymerized by focusing laser pulses onto the photosensitive material, activating the photo-initiator in the photosensitive resin through energy absorption. The polymerized 3D structure is generated when the energy absorption exceeds the polymerization threshold of the resin [15][16]. Vanguard Photonics manufactures the Sonata 1000 series for in-situ printing of PWBs. This machine works with a 780nm femtosecond laser which has a 140mW output power and a 100fs pulse duration, enabling PWB generation at a 50nm resolution within a field of 350um x 350um [21].

2.3 fabricated device

This section describes the fabricated chip dimension and microscope images of its PWBs. Fig.2.10 and Fig.2.11 display the overall chip structure. A total of 12 PWBs were used: two were used for connecting both facets of the SOA to the chip, two for the calibration loop backs, and finally, 8 for connecting the chip to the fiber array. Fig.2.12 and Fig.2.13 provides a 'zoomed-in' view of the PWBs between the surface taper on chip and the fiber array. The PWB tapers the 9μm fiber core down to a 2μm cross section waveguide, which is further reduced to 0.5 μm via a mode size converter to connect to the surface taper. The figure clearly indicates that the alignment between the fiber core and the surface taper tip is not perfect. While PWBs are flexible and have high alignment tolerances, However, better alignment may affect the shape of the PWB (i.e., a larger bend radius), potentially resulting in decreased insertion loss. Fig.2.14, Fig.2.15, Fig.2.16 and Fig.2.17 present a 'zoomed-in' view of the PWBs between the SOA and chip on both side. The PWB tapers the 2.4μm SOA facets to a 2μm cross section waveguide, which is then reduced to 0.5 μm by a mode size converter to connect to the surface taper. The figures reveal that the PWB is not well-focused due to the offset between the SOA facets and the chip surface, which shows PWBs can address the vertical offset alignment issue even on angle facets side.

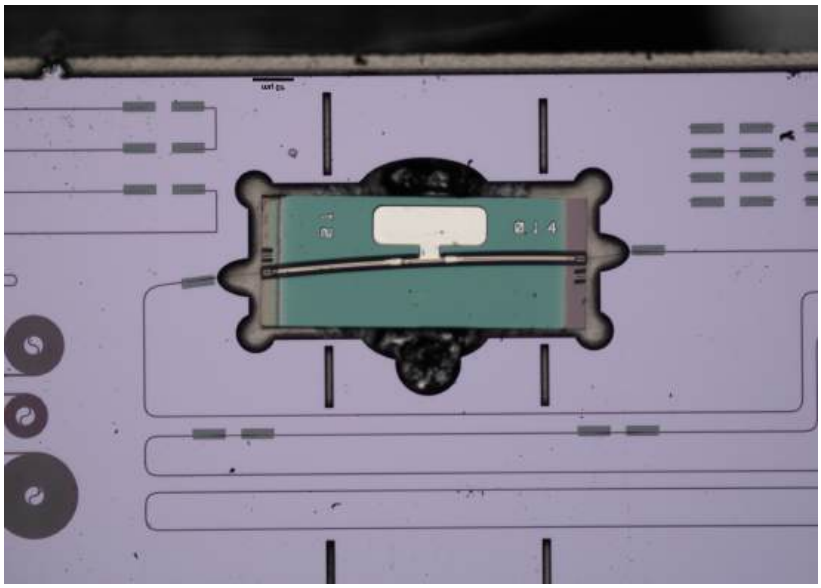

Figure 2.10: Micrograph of fabricated device – SOA integration onto SiP chip on left side

Figure 2.11: Micrograph of fabricated device – fiber array assembly on right side

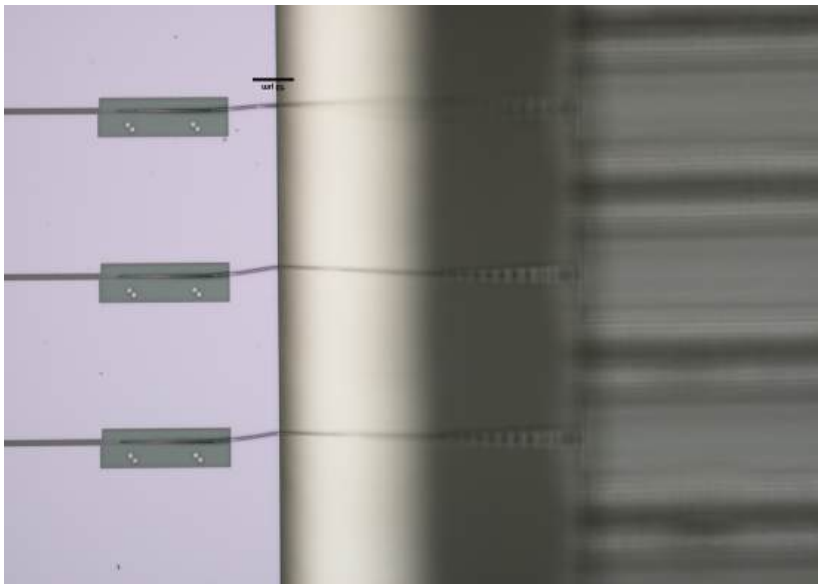

Figure 2.12: Micrograph of PWB connect SiP chip to fiber array - focus on Surface taper

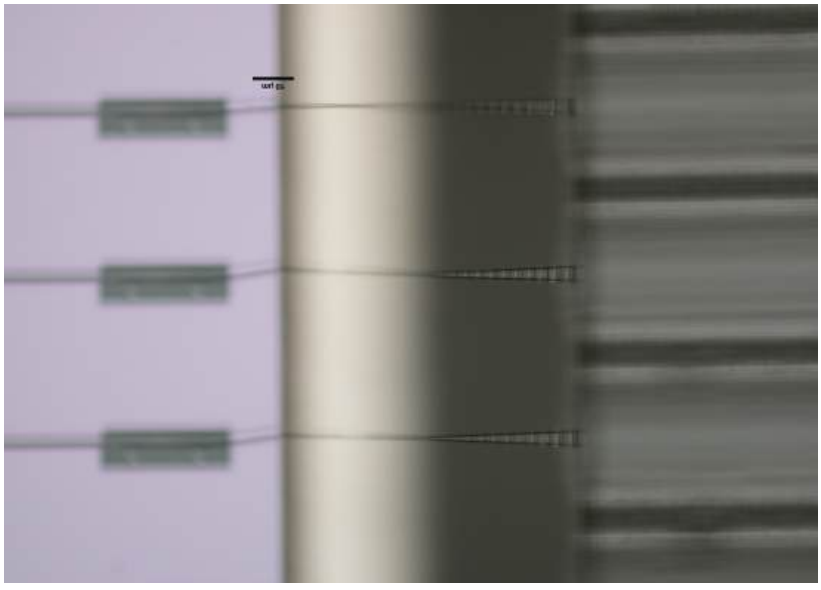

Figure 2.13: Micrograph of PWB connect SiP chip to fiber array - focus on fiber array

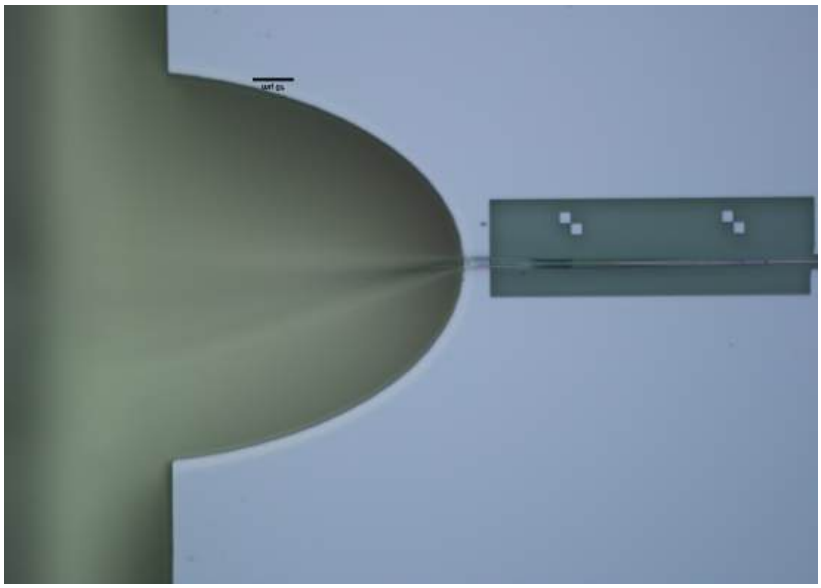

Figure 2.14: Micrograph of PWB connect SOA to SiP chip - focus on surface taper on non-angle side

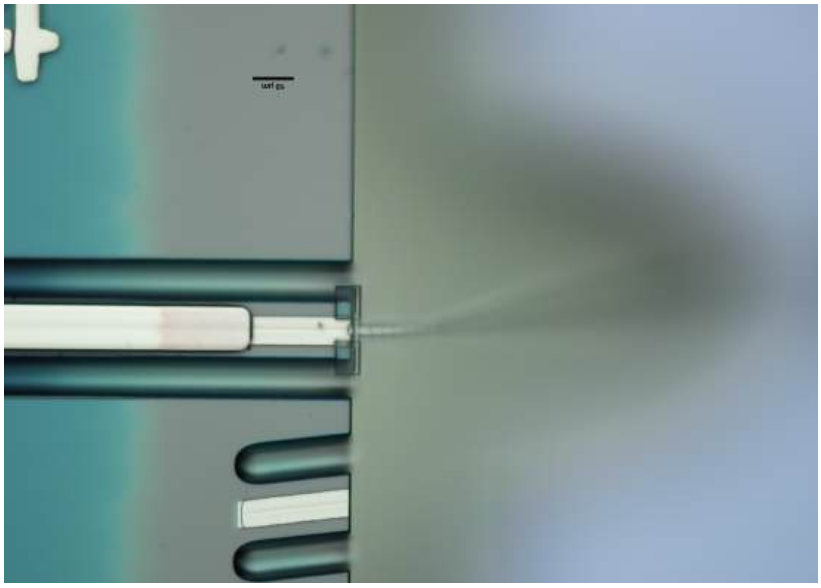

Figure 2.15: Micrograph of PWB connect SOA to SiP chip - focus on SOA on non-angle side

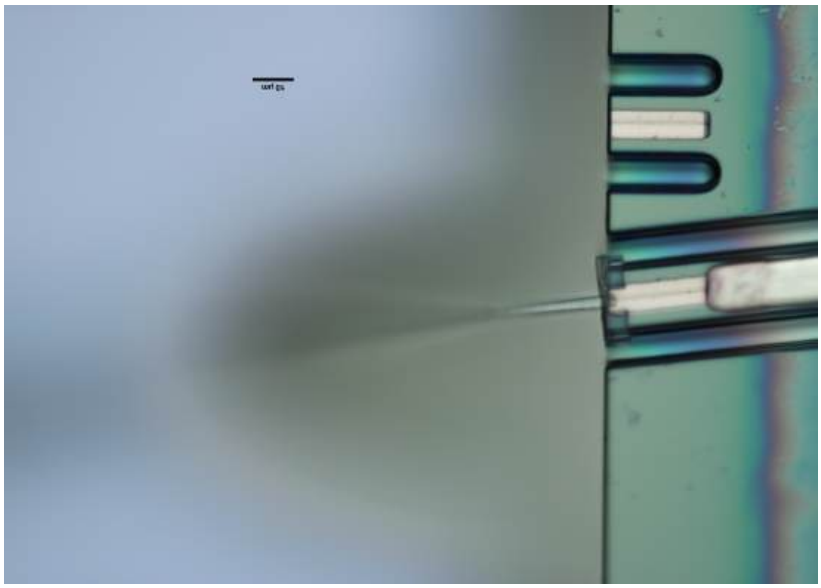

Figure 2.16: Micrograph of PWB connect SOA to Chip - focus on SOA on angle side

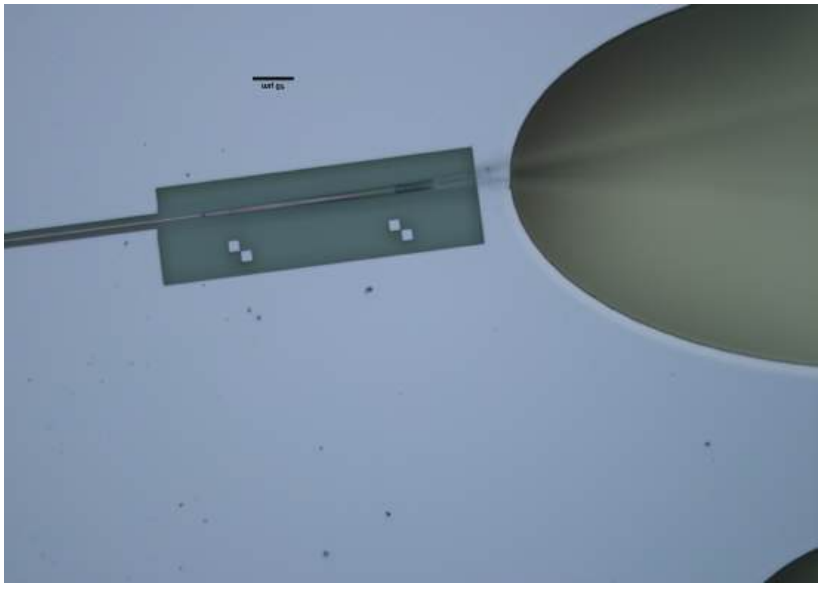

Figure 2.17: Micrograph of PWB connect SOA to Chip - focus on surface taper on angle side

2.4 Summary

This chapter details the design and fabrication process for integrating a SOA onto a SiP chip. The initial step involves designing the layout structure using KLayout, which also features a cavity for placing the SOA on the chip, along with three distinct loopback structures for calibration. The SiP chip is then fabricated in-house by using EBeam lithography (JEOL JBX-8100FS) and ICP-RIE etching (Oxford PlasmaPro 100 Cobra) to pattern and etch the SiP waveguides. Maskless lithography (Heidelberg MLA-150) and Bosch etching (SPTS Rapier DRIE) are employed to pattern and etch the cavity, then metallization was done inside the cavity. Following the metallization, a die bonder is utilized to place the SOA onto the SiP chip, and indium solder is deposited into the cavity to establish a permanent electrical contact with the bottom of the SOA chip. The fiber array assembly is then completed to connect the setup to the laser and optical spectrum analyzer. Finally, photonic wire bonding is performed to interconnect the SOA, SiP chip, and fiber array. Detailed dimensions of the fabricated chip and microscope images of its PWBs are illustrated at the end of this chapter.

Chapter 3

SOA Integrated on SiP Chip using PWB

3.1 Motivation

PICs have made remarkable strides, enabling the realization of complex functions within a compact and highly reliable framework [24]. High-performance PICs often contain many optical components with significant insertion losses. Semiconductor optical amplifiers (SOAs) are devices that can provide amplification of optical signals, via stimulated emission, and, hence, are key components for offsetting these insertion losses. SOAs also operate over wide wavelength bands (e.g., 1480nm to 1560nm) within a wavelength range between about 400nm to about 2000nm [25]. They are also relatively inexpensive and offer large gains. In addition, SOAs can be used for many applications, such as optical switching [26], demultiplexing and wavelength conversion [27]. Therefore, integration of SOAs onto silicon photonic chips serves not only to maintain signal levels on PICs with many lossy optical components, but also to function in optical signal processing.

There are many approaches to integrate an SOA onto a silicon photonic chip. The most common ways are monolithic integration and hybrid integration. Typically, monolithic integrated circuits comprise a group of components and circuits manufactured in a single piece of silicon. This method not only conserves space, but also enhances reliability by minimizing connections between optical components. In the case of integrating an SOA onto a silicon chip using monolithic integration, the active region is directly epitaxially grown on the substrate [28]. However, the manufacturability and the performance of the PIC need validation. The monolithic integration of an SOA requires a complex fabrication process. This results in additional cost. Here, we implement a flexible hybrid integration of SOAs onto silicon photonic chips using PWBs. Photonic wire bonding is a technique that builds three-

dimensional, freeform, polymer waveguides between photonic components (introduced in Section 1.3). PWBs are easy to use due to their high alignment tolerances which lead to their providing comparatively low insertion losses between different material platforms [29]. In addition, PWBs are polarization maintain that maintain a consistent polarization state of the light traveling through so they can be used in high sensitivity circuits. Therefore, SOA integration on silicon photonic chips using PWBs is proposed in the following sections.

3.2 SOA fundamentals

Semiconductor optical amplifier operates as a very similar way to a laser expect that it has anti-reflection facets, or any other technologies that prevent reflections. (The effects of the reflections will be discussed in the Section 3.42). An amplifier chip typically has a size around 0.6mm to 2mm long, with a p-cladding layer, an n-cladding layer, and a gain region shown in the Fig.3.1. The electrons from the n-cladding layer and the holes from the p-cladding layer are injected into the gain region to produce a lower band gap semiconductor.

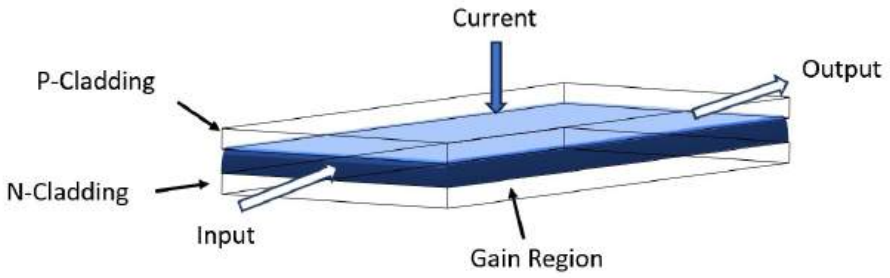

Figure 3.1: Schematic of a Semiconductor optical amplifier

In the fabrication of SOAs, there are two important factors. First, in order to have enough gain at low currents, the materials chosen should have sufficiently high probabilities of radiative recombination. Radiative recombination happens when electrons from the conduction band (N-cladding) combine with holes in the valence band (P-Cladding) and release energy in form of photons in the gain region. Second, the heterostructure formed

by the semiconductor materials chosen, should be lattice matched. Lattice matching heterostructure structures formed between semiconductor materials can lower the band gap region without changing its crystal structure shown in Fig.3.2. Except for lower the band gap, heterostructures formed between semiconductor materials also introduce transverse confinement. This confinement leads to slight changes in the transverse dimension, which can affect the refractive index of the material. Those lower band gap semiconductors have typical higher refractive index than semiconductors with higher band gap [30]. For semiconductor laser or amplifier fabrication, crystalline thin films are produced along the interface of the two semiconductor materials to eliminate defects at the interface and improve the performance of the device. For binary substrates materials like Indium Phosphide (InP), crystalline growth occurs through the Czochralski method. The process involves placing the feed material in a crucible and melting it. Then, a seed crystal is slowly dipped into the melt from the top. The seed is rotated and pulled out gradually from the melt, the crystal will form at the interface. Adjusting the pulling and rotation rates allows for control over the crystal's shape. For ternary or quaternary materials such as mercury indium telluride ($HgIn_2Te_4$), the crystalline layers are epitaxially grown on top of the substrates.

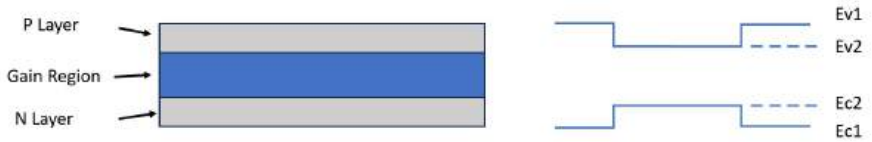

Figure 3.2: Schematic illustration of heterostructure bandgap structures.

Fig. 3.3(a) shows that the co-located electrons and holes recombine. During the process of radiative recombination, the excess energy from recombination is emitted in the form of photons which results in spontaneous emission of light and optical gain for light propagating through the gain region. Spontaneous emission occurs when the excited electrons decay into a lower energy level and the excess energy is released in the form of photons with random direction and frequency. When the current is injected, shown in Fig.3.3(b), large numbers of electrons from the conduction band and holes from the

valence band recombine in the gain region to produce photons through both spontaneous and stimulated emission. Stimulated emission occurs when the excited electrons interact with incident photons and drop to a lower energy level, therefore releasing additional photons. These new photons are emitted in the same direction and with the same frequency as the incident photons. In an SOA, when current is injected, photons are generated through both spontaneous and stimulated emission within the gain region, thereby providing the amplification to the incident light. However, spontaneous emission contributes only a small percentage to the gain, with the rest being noise [30]. (Explain in Section 3.34).

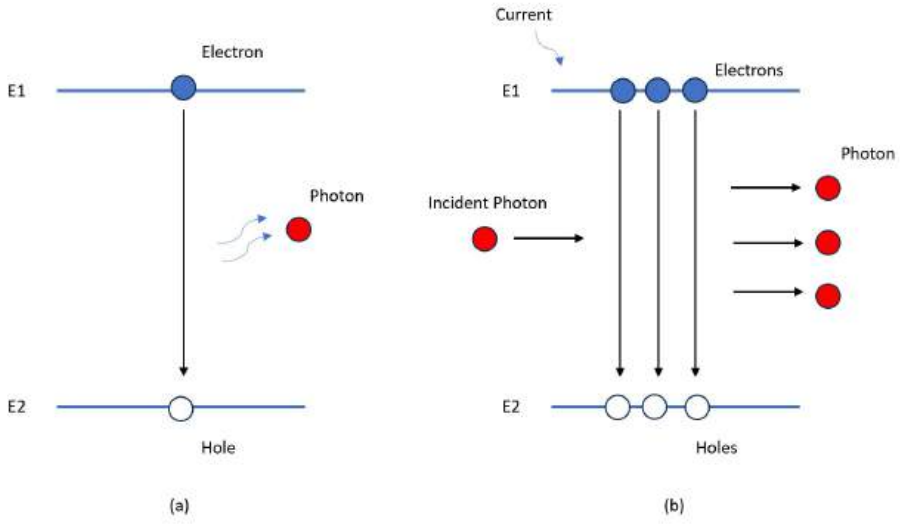

Figure 3.3: Schematic of radiative recombination: a) spontaneous emission, b) stimulated emission.

Additionally, there is another type of recombination that can affect the SOA's performance, which is non-radiative recombination. Unlike radiative recombination, non-radiative recombination doesn't emit photons during the recombination process. This type of recombination is more likely to occur at defects in the material or on the surface of the material that have dangling bonds. Non-radiative recombination can increase the current required for a certain optical gain, thereby affecting the performance of the SOA. [30].

Fig.3.4 shows the SOA utilized in this research, featuring dimensions of 1000μm in length and 400μm in width. The active region is 1.54μm wide and 1.9μm thick, mainly fabricated by InP and various alloys based on III-V elements. It is configured as traveling-wave amplifier (detailed in Section 1.22), the design incorporates a bent cavity to significantly reduce reflections.Despite the limited information provided by the manufacturer, we believe that the SOA employs a gain guiding mechanism.

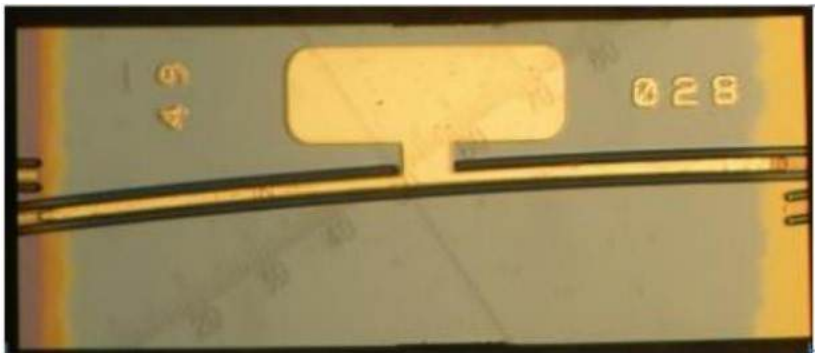

Figure 3.4: Micrograph of the SOA used in this research

3.3 Experimental Setup

The experimental setup is shown in the Fig.3.5. The device is placed on a temperature-controlled stage at 25°C. The measurement setup consists of a tunable laser's output being passed through a polarization controller (Agilent 11896A) and then fed into the SOA mounted on our silicon chip. The light is fed into the SOA via an input optical fiber, an on-chip waveguide, and two PWBs and the output signal from the SOA is routed to an OSA (optical spectrum analyzer, Ando AQ6317B) via an on-chip waveguide, two PWBs, and an output fiber. Two of the PWBs are used to establish the interfaces between the SOA and the on-chip waveguides and two of the PWBs are used to connect the on-chip waveguides to the optical fibers. Here, the cross section of all the PWBs is designed as ellipses with polarization-maintaining characteristics. A laser diode controller (LDC501) is used to control the bias current to the SOA, a micro-positioner and probe needles are used to electrically contact the SOA. Fig.3.7 shows the real experimental setup.

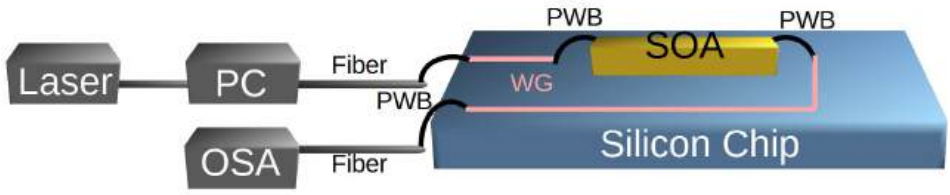

Figure 3.5: Experimental Setup

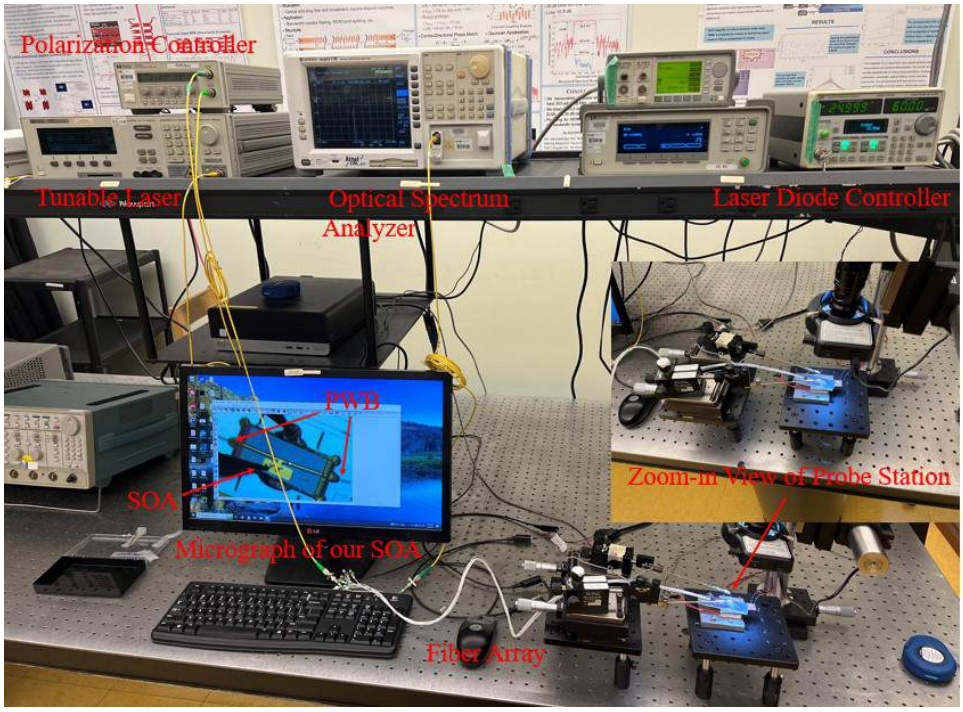

Figure 3.6: Actual Experimental Setup

3.4 Measurement Results

In this section, the results of a set of measurements made on the SOA, mounted on our silicon chip, are presented. These measurements allow us to analyze and characterize the performance of the on-chip SOA under various

operating conditions.

3.4.1 Polarization control Measurements

Light, as an electromagnetic wave, is classified as polarized when the direction of its electric field is specified. There are three primary types of polarization: linear polarization, where the electric field of the light wave oscillates in a single plane along the direction of propagation; circular polarization, characterized by two perpendicular components of equal amplitude and a phase difference of $\pi/2$, resulting in a constant rotation of the electric field vector; and elliptical polarization, where the electric field defined as an ellipse in any given plane perpendicular to the direction of propagation, with two components of differing magnitudes and phases. Polarization of light is important in various optical applications due to its capability to control and manipulate light waves. In telecommunications, polarization ensures precise signal transmission and reception. Moreover, it enhances the performance of optical devices such as lasers and detectors by reducing interference and optimizing signal clarity.

There are different ways to describe the polarization. Firstly, polarized light can be represented by Jones vector shown in Equation 3.1, where the ω describes angular frequency and k is the wave vector. The Jones vector defines the amplitude and phase of the electric field in the x and y direction [31]. (Mention plane wave.)

$$\begin{pmatrix} E_x(t) \\ E_y(t) \end{pmatrix} = \begin{pmatrix} E_{0_x} e^{i(kz-wt+\varphi_x)} \\ E_{0_y} e^{i(kz-wt+\varphi_y)} \end{pmatrix} = \begin{pmatrix} E_{0_x} e^{i\varphi_x} \\ E_{0_y} e^{i\varphi_y} \end{pmatrix} e^{i(kz-wt)} \tag{3.1}$$

Another approach involves Stokes vector, which define the polarization state through a set of values characterizing electromagnetic radiation. This method defines polarized radiation in terms of total intensity (I), degree of the polarization (p) and shape parameters (ψ and χ) shown in Equation 3.2 [31]. The vector S_1, S_2 and S_3 correspond to the coordinates on Poincare sphere shown in figureX. The Poincare sphere serves as a valuable way for representing polarization state. It not only provides a visual representation of polarization but also simplifies the calculation of the effects of polarizing components. Basically, the sphere's coordinates are specified using two angular values, azimuth (ψ) and ellipticity (χ), and a radius (Ip) [31].

$$\begin{pmatrix} S_0 \\ S_1 \\ S_2 \\ S_3 \end{pmatrix} = \begin{pmatrix} I \\ Ip\cos 2\psi cos2\chi \\ Ip\sin 2\psi cos2\chi \\ Ip\sin 2\chi \end{pmatrix} \tag{3.2}$$

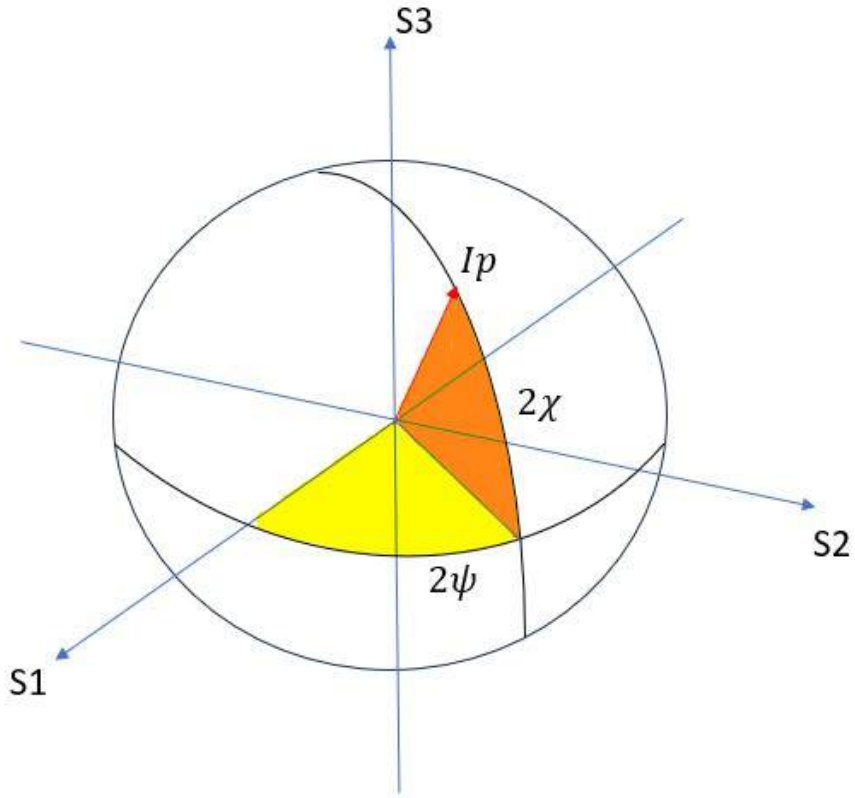

Figure 3.7: Stokes vector and Poincare sphere

Compared to the Jones vector, the Stokes vector employs real numbers to describe a broader range of polarization properties. Also, it provides comprehensive information about the polarization state, including intensity, ellipticity, and orientation, while the Jones vector only provides basic information about polarization components' amplitudes and phases. Therefore, the Stokes vector was chosen to accurately characterize the polarization state of

light input into our SOA, enabling us to assess the polarization dependency of the device. In addition, the polarization of light is crucial as it determines the coupling and injection of light into the SOA, ensuring precise alignment for optimal performance.

The experiment is aimed at investigating the polarization dependency of the SOA. To manipulate the polarization state of the SOA, a polarization controller (Agilent 11896A) was used at the input of the SOA. This controller displays the polarization state using Stokes parameters and PDL markers on the Poincare sphere. The polarization controller consists of four fiber loop assemblies, each optimized as a quarter-wave plate over specified wavelength range from 1250nm to 1640nm. Manipulating the polarization state of the transmitted signal is achieved by independently adjusting each fiber loop over an angular range of 180 degrees.

The system was automated (using Python) to sweep through various polarization states while monitoring the output power level. This process allowed us to identify both the maximum and the minimum output powers as functions of the input polarization. The maximum and minimum measured power were -17.73dB and -23.58dB, respectively shown in Fig. 3.8. These results demonstrate the polarization dependency exhibited by the SOA. Altering the polarization of the input to our PWB-connectorized SOA resulted in a significant, 5.85dB, change in the output power. We attribute the 5.85dB change to the SOA, because of the measurements on calibration loopback showed minimal polarization dependency. Note, due to the SOA noise, that even without intentional changes of input polarization, the output power fluctuated by approximately $\pm$0.25dB (Explain in Section 3.42).

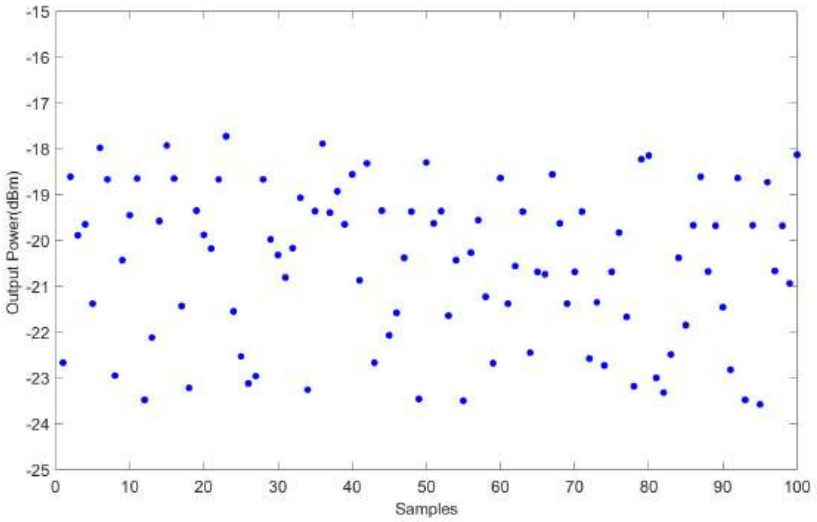

Figure 3.8: Output power for various input polarizations with the external laser ON (-20dBm, 1525nm).

3.4.2 Amplified Spontaneous Emission (ASE) Measurements

Amplified Spontaneous Emission (ASE) comprises both spontaneous and stimulated emission processes. In the gain region, stimulated emission amplifies the photons that are generated by spontaneous emission. During these processes, the interaction between electrons and photons within the gain medium leads to random fluctuations in light intensity and frequency, resulting in ASE noise. Since spontaneous emission occurs continuously, ASE noise is always present and unavoidable. In an SOA, photons are generated and amplified through the ASE process, thereby providing gain to the SOA. ASE plays a crucial role in SOAs; it not only contributes to the gain of the SOA's output but also introduces noise that can affect SOA's performance. This is the reason why the output power was fluctuated by approximately $\pm$0.25dB without changing the input polarization.

An experiment was performed using the setup configuration detailed in Section 3.3, without the laser. The angle side of the SOA was connected to an Optical Spectrum Analyzer (OSA), while the non-angle side of the SOA remained open. The bias current applied to the SOA was slowly increased,

and the spectrum was simultaneously recorded using the OSA. Fig. 3.9 shows the measurement of the ASE of the SOA. As the current applied to the SOA increases, both the power level and the ripples also increase. It became apparent that the on-chip SOA demonstrates parasitic lasing when the bias current exceeds 160mA. This observed lasing phenomenon is attributed to reflections at the interface between the two PWBs that connect the SiP chip to the SOA. The PWB on either side of the SOA acts as a mirror, causing light to reflect back and forth within the active region, thereby creating a cavity conductive to lasing. Furthermore, compared to other integration methods such as monolithic integration, these reflections reduce the amount of light coupling into and out of the SOA, thereby reducing the amplification of the propagating signal. Consequently, all subsequent measurements are conducted using a 150mA bias current to mitigate the parasitic lasing effect.

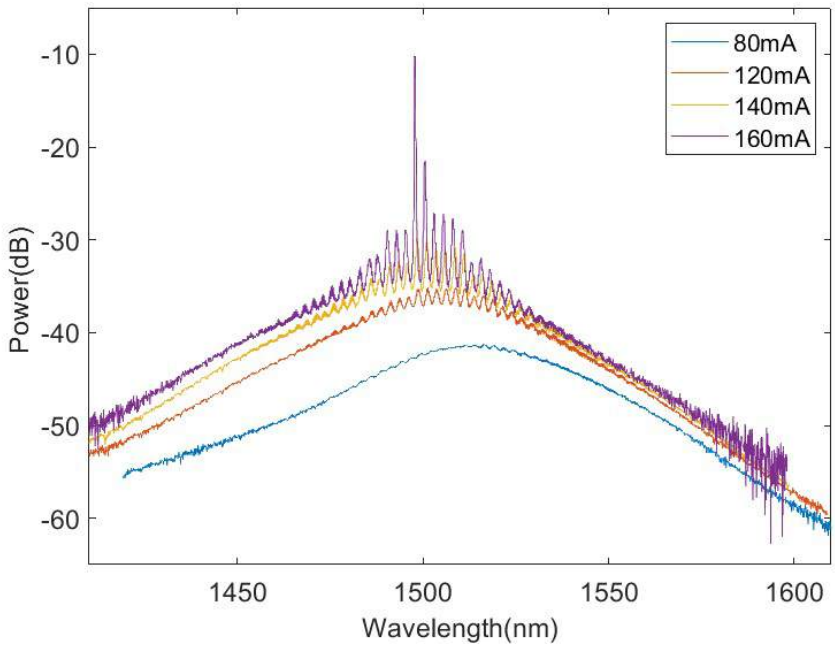

Figure 3.9: ASE power spectrum of our on-chip SOA (the current at the onset of lasing is 160mA)

The Side Mode Suppression Ratio (SMSR) was measured to determine the

lasing threshold point. The experimental setup used the same configuration as described in Section 3.3. The bias current applied to the SOA was increased, while simultaneously recording the spectrum using the OSA. The laser operated at -20dBm input power and 1525nm central wavelength. Fig. 3.10 shows the SMSR as the bias current increased from 70mA to 180mA. It is evident that the side mode begins to emerge at 150mA and becomes stronger than the laser when bias current is higher than 170mA.

Fig. 3.11 depicts the spectrum of the laser passing through the on-chip SOA with a 160mA bias current applied. Two distinct peaks are observed: the peak at 1525nm corresponds to the laser extinction, while the other peak represents parasitic lasing with a central wavelength of 1497nm, due to the reflection at the interfaces between the PWBs and the SOA on both sides.

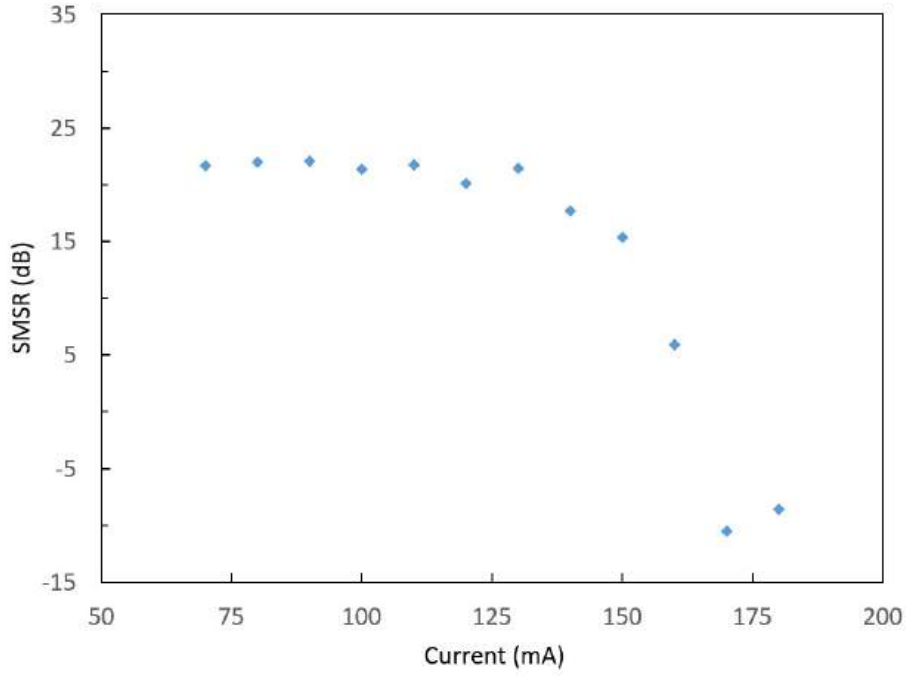

Figure 3.10: Side Mode Suppression Ratio with the external laser ON (-20dBm, 1525nm)

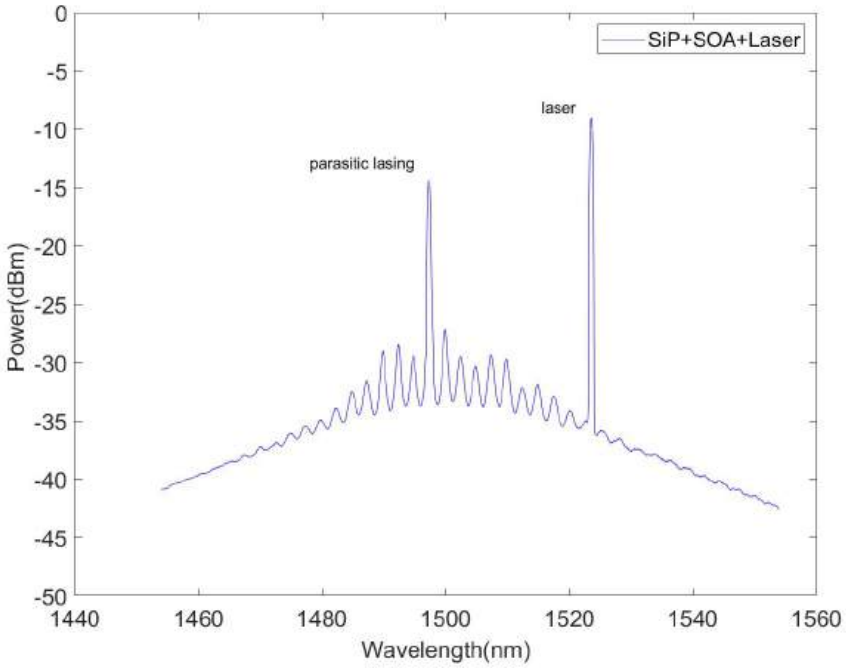

Figure 3.11: Spectrum of on-chip SOA with external Laser on (-20dBm, 1525nm) and a 160mA bias current applied.

3.4.3 SOA gain under various conditions

SOAs are sensitive, and various conditions can affect their performance. In this section, we implement a set of measurements to investigate the SOA gain under various conditions. The gain coefficient can be written as Equation 3.3 [30]:

$$g(\omega) = \frac{g_0}{1 + (\omega - \omega_0)^2 T_2^2 + P/P_s} \tag{3.3}$$

Where the g_0 is the maximum value of gain. ω is the frequency of the incident light and ω_0 is defined as the atomic transition frequency. T_2 is known as dipole relaxation time. P is the power of the incident light that has been amplified and P_s is the saturation power of the gain medium. From

the above equation, we know the optical gain is related to the frequency (wavelength) and power of the incident light.

In addition, the amplifier gain can be written as Equation 3.4 [30]:

$$G(\omega) = exp[g(\omega)L] \tag{3.4}$$

Where L is the length of amplifier medium.

The first experiment is aimed at finding the relationship between the bias current and SOA gain. It makes use of an external, tunable laser, with the output power set to -20dBm. Using this laser, the output power at various SOA bias currents was measured, then the obtained data was normalized for losses attributed to the PWBs between the silicon chip and the optical fibers, and, finally, the on-chip gain of the SOA was calculated [32]. As depicted in Fig. 3.12, positive on-chip gain was observed above 60mA and found to increase with higher applied bias currents up to 150mA. In other words, there was no further improvement in the gain beyond a bias current of 150mA. This suggests that the SOA output saturates beyond this point. As more bias current was applied, the carrier density increased, and a greater number of electrons interacted with incident photons. These electrons then transitioned to lower energy levels, releasing excess energy in the form of new photons. This process led to amplification and optical gain for the propagating light. From Equation 3.3, we can observe that g(ω) decreased as the power of the incident light being amplified (P) increased. As the bias current increased, the gain of the signal also increased, however, its gain started to reduce as the power of the signal increased. During transmission, a higher applied bias current will provide a greater number of excited electrons, leading to a higher non-radiative recombination loss. This process ultimately cause saturation.

Fig. 3.13 presents a comparison between the laser power spectrum at a central wavelength of 1525nm and the SOA output power spectrum with an applied bias current of 110mA, showing a peak gain of approximately 10dB. However, the ripples increased by around 1dB. The noise level was boosted by 15dB due to the contribution of ASE.

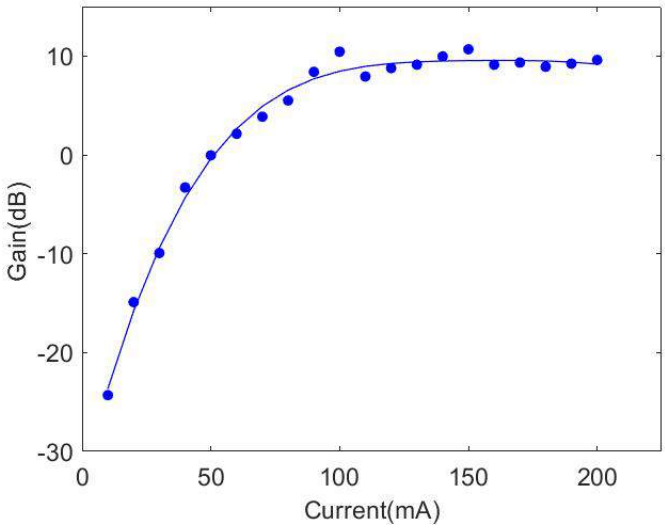

Figure 3.12: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various SOA bias currents.

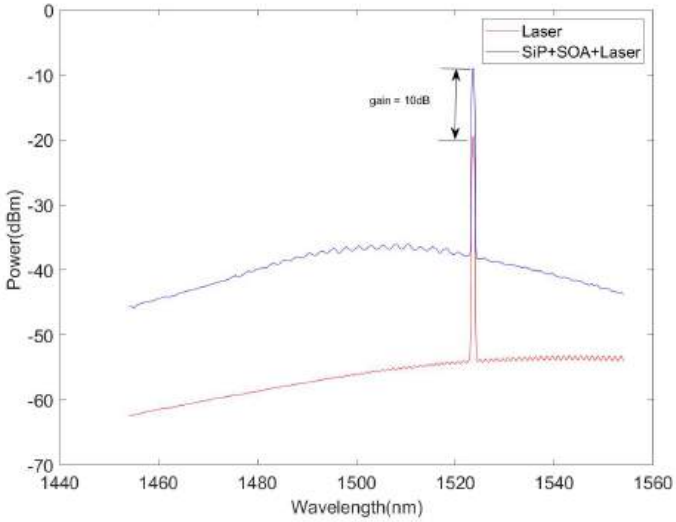

Figure 3.13: SOA power spectrum (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) with the external laser ON (-20dBm, 1525nm), showing a gain of 10dB

Next, according to Equation 3.3, the amplifier gain is related to the power of the incident light. Specifically, the gain increases as the value of "P/P_s " decreases, where P is defined to be the power of the incident light that has been amplified and P_s is defined to be the saturation power of the gain medium. As the power of the incident light changes from low to high, the value of "P/P_s " increases as "P" increases, indicating a decrease in gain.

To examine the influence of the laser input power on the SOA gain, an experiment was performed using the same setup described in Section 3.3 for various input powers. The output powers were normalized, and SOA gain was calculated. Fig. 3.14 illustrates that the SOA gain decreases when the laser input power increases. Conversely, the SOA has higher on-chip gain when exposed to lower input powers, which aligns with our prediction. The measurement was repeated for two different bias currents, 100mA and 150mA.

This phenomenon is attributed to gain saturation and the depletion of carrier density. As input power increases, the carrier density in the gain medium depletes, causing the peak of the material's gain spectrum to shift towards longer wavelengths. Consequently, the signal gain decreases. An amplifier, such as a laser gain medium, cannot provide a constant gain at arbitrarily high input powers because doing so would require an unsustainable amount of energy to maintain the amplification process [33].

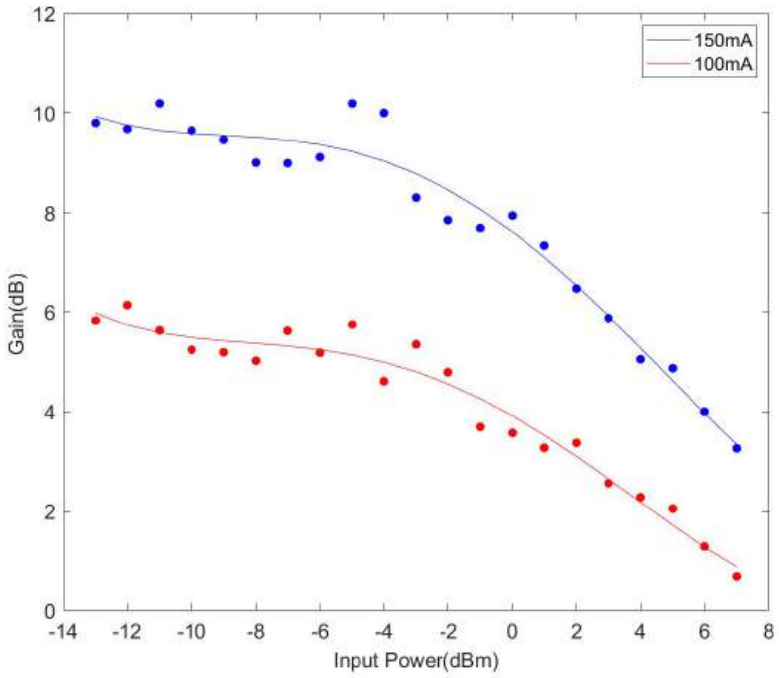

Figure 3.14: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various laser input powers at the central wavelength of 1525nm.

In addition, according to Equation 3.3, the amplifier gain is influenced by the frequency (wavelength) of the incident light. Specifically, the gain increases as the value of "$(\omega - \omega_0)^2$" decreases, where ω is defined to be the frequency of the incident light and ω_0 is defined to be the atomic transition frequency. When we sweep through a broad wavelength range, the value of "$(\omega - \omega_0)^2$" initially decreases as ω approaches ω_0, leading to an increase in gain. However, as ω moves beyond ω_0, the value of "$(\omega - \omega_0)^2$" starts to increase, resulting in a decrease in gain. To measure the variation of the SOA on-chip gain for various central wavelengths, an experiment was performed using the same setup described in Section 3.3. The central wavelength was varied using the external, tunable laser, and the SOA output power was measured using an OSA. The output powers were normalized, and the on-chip gain was subsequently calculated. The measurement was repeated for two different bias currents, 100mA and 150mA. Fig. 3.15 shows that the on-chip SOA

exhibits non-linear gain within a broad bandwidth ranging from 1480nm to 1555nm. The gain increases from 1480nm to 1510nm and then decreases. This behavior aligns with our prediction. The SOA achieves a peak on-chip gain of 10.6dB at 1510nm when a 150mA bias current is applied.

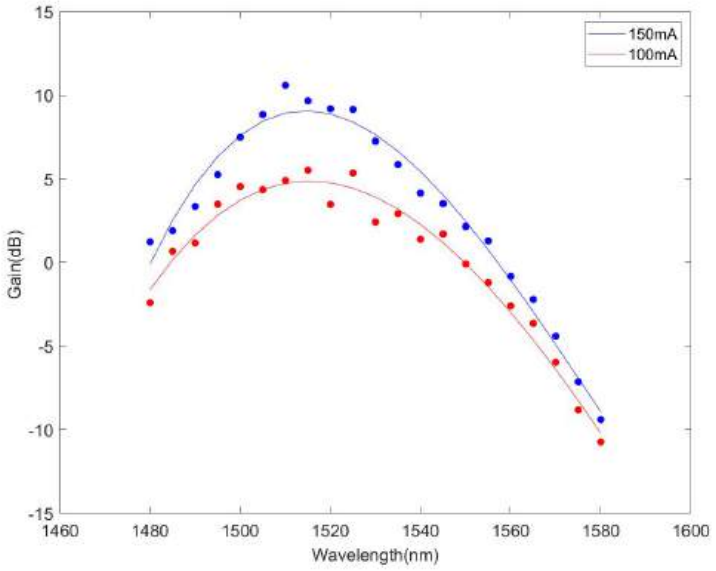

Figure 3.15: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various wavelengths at input powers of -20dBm.

3.5 Analysis of a second on-chip SOA, Sample 2

To obtain more precise data and prevent unnecessary errors, a new sample was assembled using the same process as for the initial one. This involved following the chip fabrication process, SOA die bonding, fiber array assembly, and photonic wire bonding. The same set of measurements was conducted on the new sample to assess its performance.

Polarization Dependency

To determine the polarization dependency of the SOA, polarization measurements were performed using the same setup described in Section 3.3. The system was automated to sweep through various polarization states

while monitoring the output power level. Both the maximum and minimum output powers were recorded. Subsequently, the output powers were normalized, and the SOA gain was calculated. The maximum and minimum calculated gains were 11.72 dB and 5.47 dB, respectively, as shown in Fig. 3.16. These results demonstrate the polarization dependency exhibited by the SOA. Altering the input polarization to our PWB-connectorized SOA resulted in a 6.25 dB change in the on-chip gain. Similarly, the results from the first SOA on-chip sample showed a polarization dependency, with a 5.85 dB change in on-chip gain due to varying the input polarization.

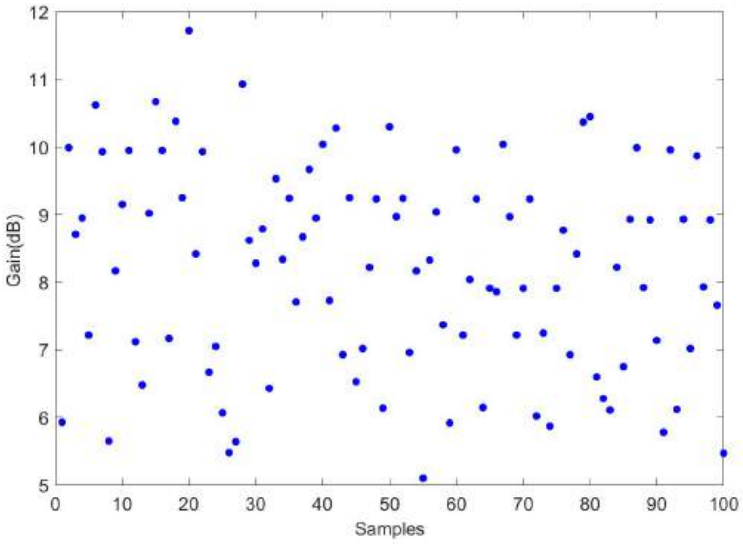

Figure 3.16: On-chip gain for various input polarizations (Sample 2)

ASE (Amplified Spontaneous Emission)

An ASE experiment was performed using the setup configuration detailed in Section 3.3, excluding the laser. The angled side of the SOA was connected to an OSA, while the non-angled side remained open. The bias current applied to the SOA was slowly increased and the spectrum was simultaneously recorded using the OSA. Fig. 3.17 shows the ASE measurement of the second on-chip SOA sample. As the current applied to the SOA increased, both the power level and the ripples also increased. It became apparent that the on-chip SOA exhibits parasitic lasing when the bias current exceeds 80 mA; consequently, all subsequent measurements were conducted using a bias

current below 80 mA. For the first on-chip SOA sample, the lasing threshold was 150 mA (explanation and simulation are described in Section 4.1).

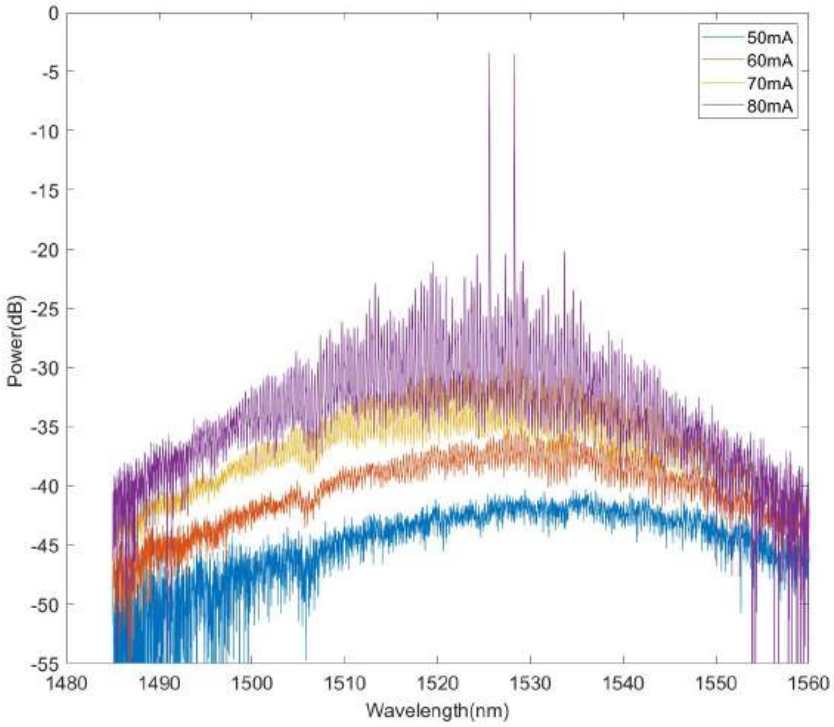

Figure 3.17: ASE power spectrum of our on-chip SOA sample 2 (the current at the onset of lasing is 75mA) for Sample 2

Bias Current Dependency

An experiment was conducted to determine the relationship between the bias current and the SOA gain using the same configuration described in Section 3.3. The output power at various SOA bias currents was measured, normalized for losses attributed to the PWBs between the silicon chip and the optical fibers, and the on-chip gain of the SOA was calculated. As depicted in Fig. 3.18, positive on-chip gain was observed above 40 mA and increased with higher applied bias currents up to 80 mA. There was no further improvement in gain beyond a bias current of 80 mA, indicating

that the SOA output saturates beyond this point. For the first on-chip SOA sample, the saturation point was 150 mA.

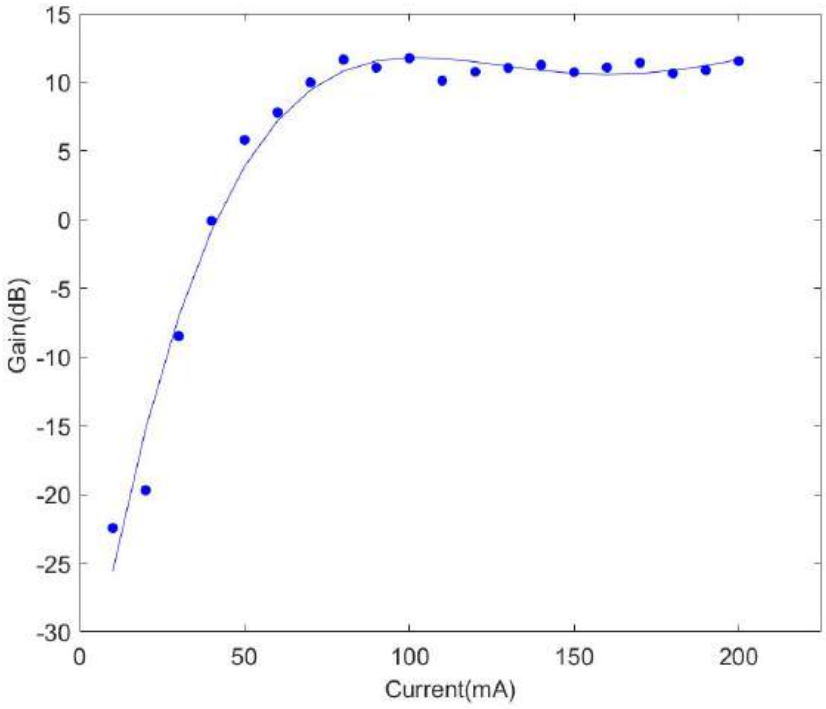

Figure 3.18: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various SOA bias currents (Sample 2).

Input Power Dependency

To examine the influence of laser input power on SOA gain, an experiment was performed using the same setup described in Section 3.3 for various input powers. The output powers were normalized, and SOA gain was calculated. Fig. 3.19 illustrates that the SOA gain decreases as the laser input power increases. Conversely, the SOA exhibits higher on-chip gain when exposed to lower input powers, which is consistent with the results of the first on-chip SOA sample. The measurement was repeated for two different bias currents, 50 mA and 75 mA.

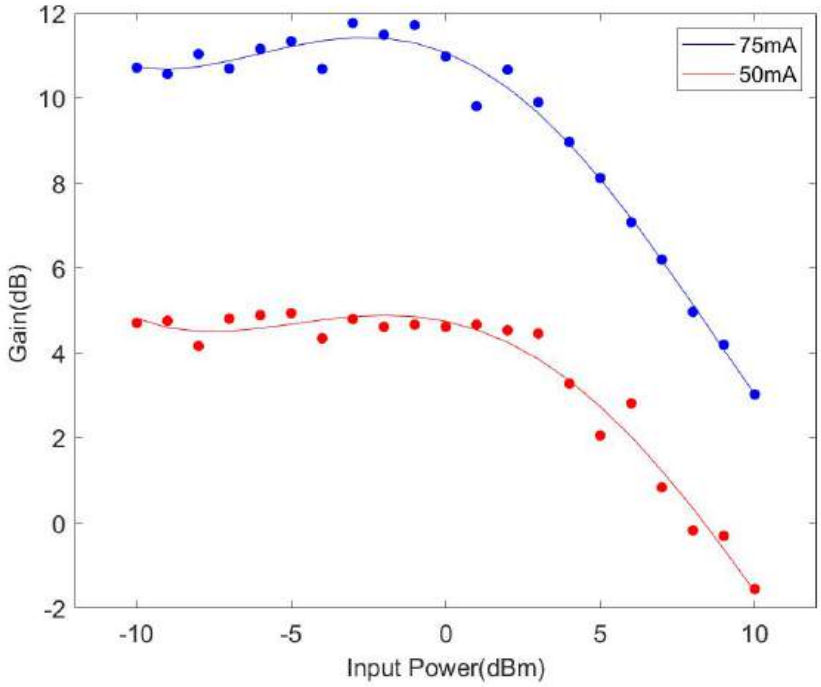

Figure 3.19: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various laser input powers (Sample 2)

Wavelength Dependency

To measure the variation of SOA on-chip gain across different central wavelengths, an experiment was performed using the same setup described in Section 3.3. The central wavelength was varied using an external tunable laser, and the SOA output power was measured using an OSA. The output powers were normalized, and the on-chip gain was calculated. The measurement was repeated for two different bias currents, 50 mA and 75 mA. Fig. 3.20 shows that the on-chip SOA exhibits non-linear gain within a broad bandwidth ranging from 1490 nm to 1560 nm. The gain increases from 1490 nm to 1525 nm and then decreases. This behavior aligns with the results of the first on-chip SOA sample. The SOA achieved a peak on-chip gain of 11.88 dB at 1525 nm when a 75mA bias current was applied. For the first

on-chip SOA sample, the peak on-chip gain was 10.6 dB at 1510 nm.

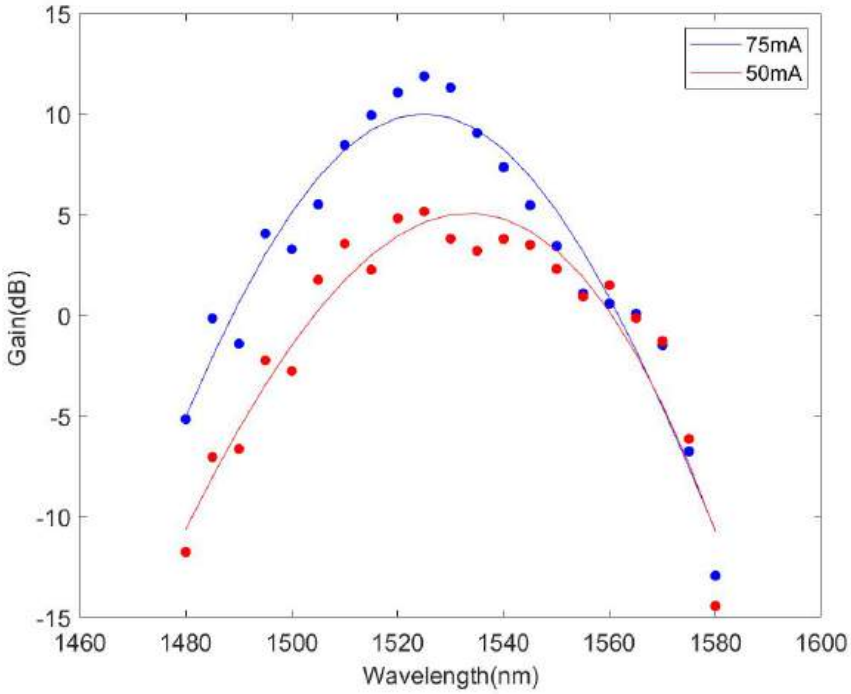

Figure 3.20: SOA on-chip gain (uncalibrated for the loss of the 2 PWBs between the silicon chip and the SOA) for various wavelengths (Sample 2).

3.6 Comparison of two different samples

The performance of the first and second on-chip SOA samples, analyzed in Sections 3.4 and 3.5, respectively, are compared in this section. A comprehensive comparison of the results from the two samples highlights several key differences and similarities.

Both samples exhibited polarization dependency, though the new sample demonstrated a slightly higher change in gain (6.25 dB) compared to the first sample (5.85 dB) when varying the input polarization. This indicates a marginally stronger polarization sensitivity in the new sample, which is likely due to fabrication bias. Regarding ASE, the second sample displayed

parasitic lasing at a significantly lower bias current of 75 mA, compared to 150 mA in the first sample. This suggests that the new sample is more prone to lasing at lower currents. The reason will be further explained in Section 4.1. When examining the relationship between bias current and SOA gain, the new sample showed saturation beyond 80 mA, while the first sample did not saturate until 150 mA, further indicating differences in their lasing thresholds. Next, both samples exhibited a decrease in SOA gain with increasing laser input power, a trend consistent across varying input powers and bias currents. Finally, the wavelength dependency of the SOA gain was similar for both samples. The new sample achieved a peak gain of 11.88 dB at 1525 nm, while the first sample reached a peak gain of 10.6 dB at 1510 nm. These results indicate that while both SOA samples follow similar performance trends in polarization dependency, wavelength dependency, applied bias current, and laser input power, the new sample exhibits a higher peak gain. This could be attributed to more precise assembly and alignment during the PWB fabrication, as well as potential variations in fabrication or material properties that influence performance.

In summary, although both samples exhibit similar overall performance trends, the new sample demonstrates higher peak gain and increased sensitivity to polarization and lasing current, likely due to improvements in fabrication and assembly processes (detailed explanation on lasing threshold point will be described in Section 4.1).

3.7 Summary

This chapter delves into the integration of SOAs onto SiP chips using PWB technology. It covers the motivation, fundamental principles, experimental setup, results, and analysis of two different SOA samples. The primary goal of this integration is to mitigate significant insertion losses in high-performance photonic integrated circuits (PICs) by utilizing SOAs for amplification. This chapter provides a thorough discussion on the fundamentals of SOAs, including their operation and fabrication processes. The experimental setup for measuring SOA performance is elaborated, with a focus on polarization dependency and amplified spontaneous emission (ASE). A series of experiments are conducted to investigate the influence of SOA gain under various operating conditions, including wavelength dependency, applied bias current, and laser input power. Finally, a comparative study of a second SOA sample is also included to validate the results and ensure measurement reliability.

Chapter 4

Simulation of a Traveling Wave Laser

4.1 Simulation on lasing threshold

The results presented in Section 3.6 demonstrate significant variability in the lasing threshold of parasitic lasing across different SOA samples. This parasitic lasing, attributed to reflections between the two PWBs that interface the SOA with the on-chip waveguide, significantly impairs the SOA's performance by disrupting the transmission of signals. To maintain optimal device functionality, it is crucial to mitigate parasitic lasing, either by increasing the lasing threshold or by preventing it altogether. Achieving this requires a comprehensive understanding of the factors influencing the lasing threshold. Consequently, a detailed investigation into the threshold behavior of parasitic lasing, through simulations of a traveling wave laser, is essential for the development of more robust and efficient on-chip SOAs.

This chapter focuses on simulations to determine the effects of cavity length, facet reflectivity, and temperature variations on the lasing threshold point. The simulation was conducted using a Finite-Difference Eigenmode (FDE) solver and a Multi-Quantum Well (MQW) gain solver, see below. The FDE solver explores spatial profiles and data such as mode field profiles, effective index, and loss by solving Maxwell's equations on a waveguide cross-sectional mesh. It also calculates group delay and dispersion through an integrated frequency sweep [33]. The MQW solver calculates the optical and electronic properties of multi-quantum well stacks, providing gain and spontaneous emission coefficients, electronic band diagrams, band structures, and wavefunctions of the semiconductor laser.

The simulation was performed through three steps. Firstly, An InGaAsP-InP multiple-quantum well laser structure was built in Lumerical MODE. MODE's FDE solver was used to calculate the optical mode profile, effec-

tive index, group index of the fundamental (TE) mode, and its confinement factor relative to the gain medium. Secondly, A k-dot-p calculation of the electronic band structure in the MQW gain medium was performed using MODE's MQW solver. This provided data on the electronic bandgap and the stimulated and spontaneous emission spectra. Lastly, all data were imported into a Traveling Wave Laser Model (TWLM) in Lumerical INTERCONNECT. Simulations were performed by varying drive currents, and the L-I curve was plotted based on the optical power emitted as a function of drive current.

Effect of Cavity Length Variation

The lasing threshold point is influenced by the laser cavity length. Due to the complexity of the simulation model, the solver consistently crashes when attempting to simulate results for a laser cavity length of 1 mm, which matches our SOA. To save simulation time, we chose to use laser cavity lengths between 200 and 400 µm. We believe that the effect of cavity length variation in the simulation model should be similar to the effect on the actual SOA cavity length variation. Fig.4.1 shows the simulated L-I curves for cavity lengths of 200 μm, 300 μm, and 400 μm, with the cavity width, thickness, reflectivity, and temperature kept constant. As shown in Fig. 4.1, the lasing threshold point is 100mA, 120mA and 145mA when the cavity length is set to 200μm, 300μm, and 400μm, respectively. As the cavity length increases, the lasing threshold point also increases, indicating that more driving current is required for lasing in longer cavities. This is due to increased material loss with longer cavity lengths. However, mirror loss decreases when laser cavity length increases. Material loss is the dominant factor in this case, leading to an overall increase in total loss. Conversely, in shorter cavities with small reflectivity, mirror loss becomes the dominant factor.

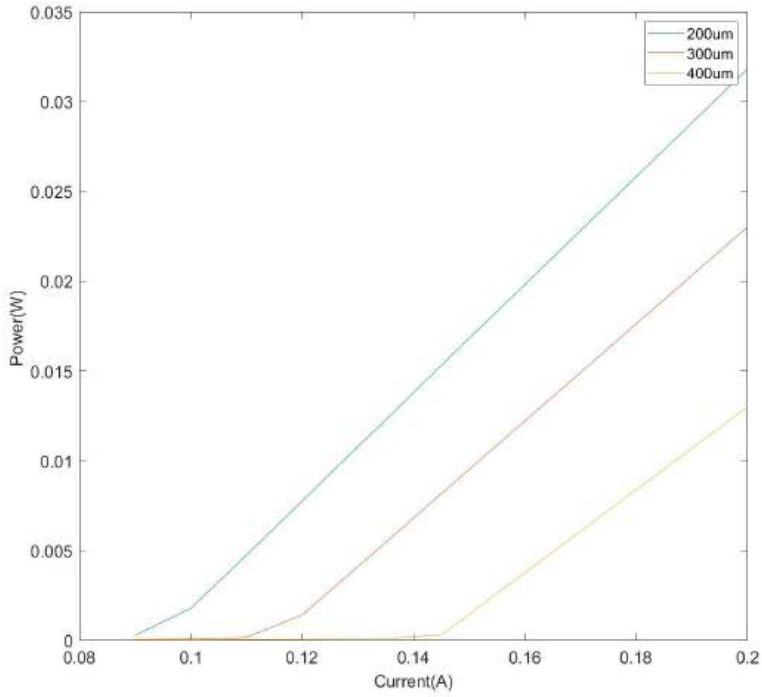

Figure 4.1: Plot showing lasing threshold point for different cavity length.

Effect of Facet Reflectivity Variation

Facet reflectivity also impacts the lasing threshold point. Fig. 4.2 shows the simulated L-I curves for reflectivities of 0.1, 0.2, and 0.3, with the cavity length, width, thickness, and temperature held constant. As shown in the Fig. 4.2, the lasing threshold point is 145mA, 135mA, 125mA, and 120mA when the reflectivity is set to 0.12, 0.15, 0.20, and 0.3, respectively. It clearly shows that the lasing threshold point decreases as the reflectivity increases. This means that the laser needs less driving current when the reflectivity is higher. This is because higher reflectivity enhances the stimulated emission process, which causes lasing at lower driving current. However, this is not true under two conditions: when the reflectivity approaches 1 and when the reflectivity approaches 0. When the reflectivity approaches 1, most of the photons are reflected back to the cavity and hard to emit. Therefore, a higher driving current (high power) is required to facilitate emission. Conversely,

when the reflectivity approaches 0, most photons escape the cavity which requires a higher driving current to enhance the stimulated emission process and achieve lasing.

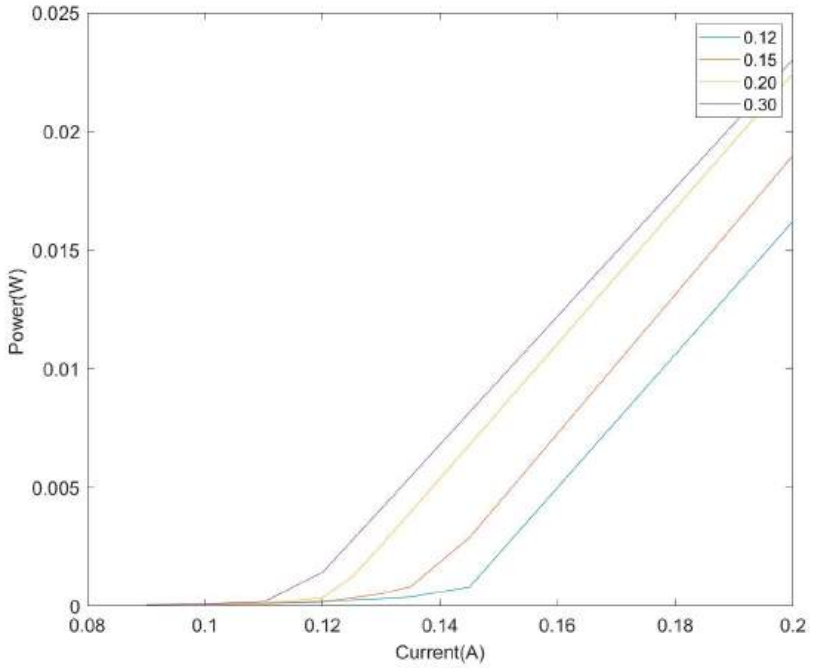

Figure 4.2: Plot showing lasing threshold point for different reflectivities.

Effect of Temperature Variation

The lasing threshold point can also be affected by varying the temperature. Fig. 4.3 shows the simulated L-I curve for temperatures of 273K, 293K, and 333K, with the cavity length, width, thickness, and reflectivity constant. As shown in Fig. 4.3, the lasing threshold point is 110mA, 210mA, and 240mA when temperature is set to 273K, 293K, and 333K, respectively. It shows that the lasing threshold point increases as the temperature increases. This means that the laser needs more driving current to achieve lasing when temperature is higher. This is because increased temperatures lead to a rise in the number of free carriers (electrons and holes) in semiconductor materials, resulting in greater scattering and absorption losses. As the temperature increases, the thermal vibrations of the lattice structure within the

laser material intensify, causing fluctuations in the refractive index. These fluctuations lead to light scattering by inhomogeneities in the material, resulting in higher scattering loss. Additionally, at higher temperatures, the interaction between particles increases and photons are absorbed by the material, leading to a higher probability of non-radiative recombination that converts optical energy into heat. Consequently, more driving current is required to counteract these losses and achieve lasing.

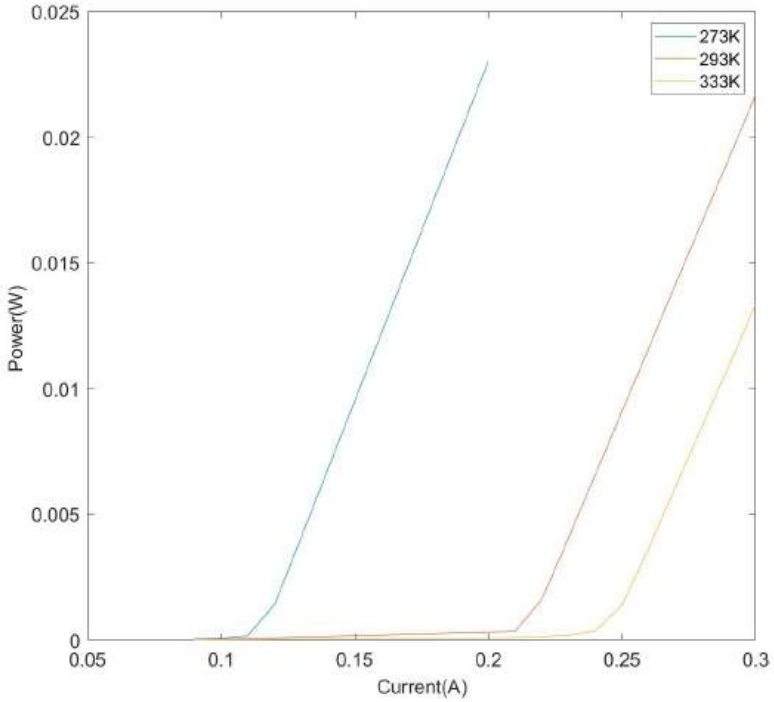

Figure 4.3: Plot showing lasing threshold point for different temperatures.

From Section 3.6, we know that the second sample displayed parasitic lasing at a significantly lower bias current of 80mA, compared to 150mA in the first sample, i.e., the new sample is lasing at lower currents. From the simulation in this section, the lasing threshold point can be affected by cavity length, reflectivity, and temperature. The cavity length for Sample 2 is 25μm less than the first sample. Also, the PWB has fabrication bias, has fabrication biases, with the actual position of PWB writing potentially

varying by ±100 nm. This variation can alter the effective cavity length by the same margin, impacting the overall performance of the system. From the simulation results, a laser that has a shorter cavity length will achieve lasing at lower driving current, which means Sample 2 has a lower lasing threshold point.

The fabrication bias of the PWB could also affect the reflection amplitude. From the measurements on the calibration loopback structure, the PWB loss for Sample 1 is higher than that of second sample. In the setup described in Section 3.3, we have two sources of reflection: a first PWB that connects the chip to the SOA and a second PWB that connects the chip to the fiber array. As the light propagates, it is reflected by the second PWB back to the SOA through the first PWB. The reflected photons attenuate less due to the lower loss of the PWB for Sample 2. Therefore, compared to Sample 1, having less attenuated photons will enhance the stimulated emission process so that Sample 2 achieves lasing at lower driving current.

4.2 Summary

This chapter presents simulations on the effects of cavity length variation, facet reflectivity variation, and temperature variation on the lasing threshold point. The simulation was performed using ANSYS Lumerical FDE MODE and Lumerical INTERCONNECT. It was investigated using MODE's Finite-Difference Eigenmode (FDE) solver and Multi-Quantum Well (MQW) gain solver. The simulation process involved constructing the InGaAsP-InP multiple quantum well laser structure, calculating optical mode profiles and electronic band structures, and integrating these into a Traveling Wave Laser Model (TWLM) to generate L-I curves. The results indicate that longer cavity lengths increase the lasing threshold due to higher material losses, while higher facet reflectivity decreases the lasing threshold when the reflectivity is not close to 0 or 1. Additionally, higher temperatures were found to increase the lasing threshold owing to increased scattering and absorption loses. These results helped in optimizing on-chip SOA design for improved performance with regard to the effects of PWBs.

In addition to these results, other factors such as quantum efficiency and confinement factor can also affect the lasing threshold, which are not considered here. For further improvement, a more complex simulation model, incorporating these factors, can be developed.

Chapter 5

Summary, Conclusions, and Suggestions for future work

5.1 Thesis Summary

In conclusion, we have successfully demonstrated the integration of SOAs onto SiP chips using PWB. The primary objective of this integration is to reduce significant insertion losses in high-performance PICs by utilizing SOAs for amplification. The major components of this thesis include:

- Explanation of the basic concepts of optical amplifiers, including various types of optical amplifiers, the specific types of semiconductor optical amplifiers, and their functionality. Additionally, the fundamental concepts of photonic wire bonding, including coupling methods and 3D structures, were elucidated.
- Detailed demonstration of the design and fabrication process for integrating SOAs onto SiP chips. This encompasses the design of the on-chip SOA layout structure, in-house SiP chip fabrication including cavity etching, the die bonding process for placing the SOA onto the SiP chip, the assembly of the fiber array for measurement setup, and the photonic wire bonding to interconnect the SOA, SiP chip, and fiber array. Detailed dimensions of the fabricated chip and microscope images of its PWBs were also provided.
- Comprehensive description of the experimental setup. The performance of the SOA was measured, focusing on polarization dependency and ASE. A series of experiments were conducted to investigate the influence of SOA gain under various operating conditions, including wavelength dependency, applied bias current, and laser input power. A comparative study of a second SOA sample was included to validate the results and ensure measurement reliability.

- Simulation of the effects on the lasing threshold point of a traveling wave laser. Factors such as cavity length variation, facet reflectivity variation, and temperature variation were discussed. These simulations enhanced our understanding of the lasing principles of a traveling wave laser and helped optimize the on-chip SOA design for improved performance concerning the effects of PWBs.

5.2 Conclusion

In conclusion, we demonstrated the integration of SOAs onto SiP chips using PWBs to compensate for significant insertion losses in high-performance PICs. Our study encompassed a series of experiments aimed at investigating the performance characteristics of the on-chip SOA. The on-chip SOA exhibited dependencies on various input parameters, including polarization, wavelength, applied bias current, and laser input power. Varying the polarization of the input to our PWB-connectorized SOA changed the measured gain by 5.85 dB for sample 1 and 6.25 dB for sample 2. The gain increased with higher applied bias currents and lower laser input powers. Additionally, our on-chip SOA exhibited non-linear gain within a broad bandwidth ranging from 1480 nm to 1555 nm. The connectorized SOA demonstrated a peak gain of 10.6 dB for sample 1 (uncalibrated for the loss of the two PWBs between the silicon chip and the SOA) at 1510 nm with a 150mA bias current. For sample 2, the peak gain was 11.88 dB at 1525 nm with a 75mA bias current. These differences could be attributed to more precise assembly and alignment during the PWB fabrication, as well as potential variations in fabrication or material properties that influence performance. Furthermore, simulations were performed to study the effects of cavity length variation, facet reflectivity variation, and temperature variation on the lasing threshold point. The results indicated that longer cavity lengths increased the lasing threshold due to higher material losses, while higher facet reflectivity decreased the lasing threshold when the reflectivity was not close to 0 or 1. Additionally, higher temperatures were found to increase the lasing threshold due to increased scattering and absorption losses. These findings are instrumental in optimizing on-chip SOA design for improved performance with regard to the effects of PWBs.

5.3 Future Work

Despite the progress made, there is still room for improvement. Optimizing the performance of PWBs by refining the design of layout structures and the geometry of PWBs is a potential area for further research. Additionally, exploring other applications of on-chip SOAs can yield valuable insights and advancements.

5.3.1 Optimizing Photonic wire Bonding

In practice, the insertion loss of PWBs can be influenced by fabrication bias. In Section 3, the first fabricated sample exhibited a PWB loss of 7.5 dB, higher than the second sample's 4.7 dB. This discrepancy could be attributed to more precise assembly and alignment during the fabrication of the second sample. While controlling fabrication bias remains challenging, we can manage the transmission loss of PWBs by modifying their geometric parameters. For instance, from recent simulation, a larger bending radius in PWBs results in lower insertion loss. Similarly, the length of the mode size converter impacts transmission loss; a longer mode size converter correlates with reduced insertion loss. Additionally, mode couplers can be designed to minimize mode mismatch loss [21]. Therefore, optimizing the layout design is crucial for enhancing the performance of PWBs. Based on the two samples we fabricated, there remains room for improvement. Recent experience suggests that the optimal distance between two components is 250 µm with a 30 µm vertical offset, a configuration that results in low insertion loss [34]. Currently, the samples have PWBs with a 150 µm spacing and a 45 µm vertical offset. Performance improvements could be achieved by increasing the cavity length to extend the PWB mode size converter and reducing the vertical offset between the SOA and the surface taper, thereby increasing the bending radius.

5.3.2 Application of Integrating SOA onto SiP Chip

Based on the principles of the SOA, there are numerous applications for this technology. This thesis primarily focuses on its amplification ability to compensate for significant insertion losses in high-performance PICs. Additionally, SOAs can function as optical switches and wavelength converters, making them versatile for a wide range of applications. They can also serve as laser sources. The SOA is a key device for next-generation, all-optical networks [14].

Optical switch

SOAs can function as optical switches by leveraging their ability to control light propagation through the amplification or attenuation of optical signals. When a signal is present, the SOA is biased with a high injection current to allow the SOA to amplify the incoming optical signal. Conversely, when the injection current is reduced or switched off, the SOA stops amplifying the signal, effectively halting light transmission. SOAs can operate over a wide range of wavelengths and switch optical signals rapidly, which has numerous applications. This functionality can be explored further in future research to integrate SOAs on-chip as optical switches.

Wavelength Conversion

SOA can perform wavelength conversion through several nonlinear optical effects. The most common methods for wavelength conversion using an SOA are Cross-Gain Modulation (XGM). In XGM, two signals are input into the SOA: one high-power signal ($\lambda 1$) and a weaker signal ($\lambda 2$). The high-power signal ($\lambda 1$) modulates the carrier density in the SOA, affecting its gain. (Discussed in Section 3.43, the gain decreases as the input signal power increases). As the gain of the SOA varies with the high-power signal's intensity, this change is transferred to the weaker signal ($\lambda 2$). Consequently, the weaker signal at wavelength $\lambda 2$ exits the SOA with its intensity modulated according to the high-power signal's variations at wavelength $\lambda 1$. This process effectively converts the modulation pattern of the high-power signal to the weaker signal at a different wavelength. However, there are a few limitations. The converted signal is an inverted version of the input, necessitating additional steps to correct the inversion. Furthermore, the wavelength range for conversion is limited. Future research can focus on integrating SOAs onto chips to achieve efficient wavelength conversion in high-performance PICs, addressing these challenges and expanding their applicability.

RSOAs Work as Laser Sources

Reflective Semiconductor Optical Amplifiers (RSOAs) serve as laser sources by leveraging their ability to amplify and reflect light. An RSOA features a high-reflectivity mirror at one end and an anti-reflection coating or low reflectivity at the other. This configuration allows the RSOA to act as a reflective amplifier, reflecting and amplifying incoming light. While not always necessary, a seed light can be injected to initiate the lasing process in a RSOA. Even without a seed light, spontaneous emission can generate

the initial photons. When used, the seed light is injected through the anti-reflective coated at the end of the RSOA, and as it passes through the active region, it is amplified via stimulated emission. The amplified light reaches the high-reflectivity end, where it is reflected back into the active region for further amplification.

The design of the cavity is crucial for creating the feedback necessary for lasing. This typically involves external components, such as a fiber Bragg grating (FBG) or a loop mirror, to reflect the amplified light back into the RSOA, thereby forming a feedback loop [35]. When the gain provided by the RSOA exceeds the losses within the cavity, the device reaches the lasing threshold and begins to emit coherent laser light.

However, RSOAs have some limitations. They may exhibit sensitivity to polarization, so polarization management techniques are needed for optimal performance. Additionally, RSOAs generate heat during operation, which can lead to thermal effects that impact performance. Future research can focus on integrating RSOAs onto SiP chips using PWBs to connect with designed cavities to produce functional lasers. This approach would address existing challenges while expanding the practical applications of these integrated systems.

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