TIMING AND COINCIDENCE CIRCUITRY FOR A
TIME-SHARING ANALOG FUNCTION GENERATOR

by

Joseph Samuel Fiorentino
B.A.Sc., University of British Columbia, 1954

A thesis submitted in partial fulfilment of
the requirements for the degree of

Master of Applied Science
in the department of
Electrical Engineering

We accept this thesis as conforming to
the standard required from candidates for
the degree of Master of Applied Science.

Members of the Department
of Electrical Engineering

The University of British Columbia
April, 1956
Abstract

This thesis is concerned with the timing and coincidence circuitry which controls the operation of a time-sharing function generator and four-quadrant analog multiplier. The functions to be generated are fed into the computer in time sequence as voltage waveforms of short duration. A waveform is sampled at a particular value of the independent variable \( x \) and the resulting ordinate \( E_f \) is normalized with respect to the maximum function ordinate \( E_M \) and multiplied by a reference voltage \( E_r \). The output of the multiplier is then a voltage which represents the expression \( E_f E_r / E_M \) and this voltage is channeled through the computer. Multiplication is performed by the following method. Two voltages \( E_1 \) and \( E_2 \) are simultaneously applied to two identical linear networks whose response to unit voltage is \( N(t) \). The outputs are then \( E_1 N(t) \) and \( E_2 N(t) \). If, on comparing \( E_1 N(t) \) with a reference voltage \( E_3 \), the second sweep \( E_2 N(t) \) is clamped at the instant of equality, then \( N(t) = E_3 / E_1 \) and the output is \( E = E_2 N(t) = E_2 E_3 / E_1 \).

The present proposal is to generate the functions optically. A function is graphed, photographed on 35 millimeter film, and mounted on the rim of a rotating disc. The optical system projects a narrow segment of the function onto a phototube and its output, biased for the zero level, follows the function ordinate in a strict voltage analog sense. The full abscissa scale is represented by a constant voltage and the input specifying the sampling point is some fraction of this full-scale voltage. In order that the sampling point \( x \) be independent of the velocity of the scanning disc the coincidence circuitry eliminates velocity as a variable in the selection of \( x \).
Illustrations

<table>
<thead>
<tr>
<th>Fig.</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Calibration and function frames on scanning disc.</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Symbols for computer units.</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Operational Amplifier with negative feedback</td>
<td>9</td>
</tr>
<tr>
<td>4</td>
<td>Negative feedback obtained by an adding network in the grid circuit</td>
<td>10</td>
</tr>
<tr>
<td>5</td>
<td>Principle of the Holding Circuit</td>
<td>13</td>
</tr>
<tr>
<td>6</td>
<td>Bidirectional Holding Circuit</td>
<td>14</td>
</tr>
<tr>
<td>7</td>
<td>Block diagram of the Holding Circuit</td>
<td>15</td>
</tr>
<tr>
<td>8</td>
<td>Timing Circuits.</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Schematic of the Multiplier</td>
<td>20</td>
</tr>
<tr>
<td>10</td>
<td>Sweep and Coincidence Circuits</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Method for obtaining two identical sweeps</td>
<td>25</td>
</tr>
<tr>
<td>12</td>
<td>Function Generator and Multiplier Assembly</td>
<td>26</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Counter and Function Storage</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Diode Gate</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Discharge of a condenser through a diode gate</td>
<td>33</td>
</tr>
<tr>
<td>16</td>
<td>Flip-Flop</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Delay Flip-Flop DFF1</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Delay Flip-Flops DFF2a and DFF2b</td>
<td>37</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Holding Circuit</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>To follow</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Schematic Holding Circuit for stability analysis</td>
<td>40</td>
</tr>
<tr>
<td>21</td>
<td>Inverter for determining G</td>
<td>41</td>
</tr>
<tr>
<td>22</td>
<td>Measured frequency response and calculated open-loop gain of the Philbrick and Storage Amplifiers.</td>
<td>41</td>
</tr>
<tr>
<td>Illustrations (cont'd.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Fig.</strong></td>
<td><strong>Page</strong></td>
<td></td>
</tr>
<tr>
<td>23. Pulse Amplifier.</td>
<td>43</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24. Comparator</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25. Basic Phantastron and its waveforms</td>
<td>47</td>
<td></td>
</tr>
<tr>
<td>26. Blanking Phantastron.</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27. Precision test of the Phantastron. $E_1$ vs. $5t$.</td>
<td>49</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28. Test waveforms occurring in the timing and coincidence circuitry.</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Models K2-W and K2-X Operational Amplifiers.</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>To follow</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Abstract</td>
<td>ii</td>
</tr>
<tr>
<td>Introduction</td>
<td>1</td>
</tr>
<tr>
<td>Description of the Function Generator and Multiplier</td>
<td>5</td>
</tr>
<tr>
<td>Requirements of the Timing and Coincidence Circuitry</td>
<td>7</td>
</tr>
<tr>
<td>General Description of the Components</td>
<td>9</td>
</tr>
<tr>
<td>Operational Amplifier</td>
<td>9</td>
</tr>
<tr>
<td>Diode Gate</td>
<td>11</td>
</tr>
<tr>
<td>Flip-Flop and Delay Flip-Flop</td>
<td>12</td>
</tr>
<tr>
<td>Comparator</td>
<td>12</td>
</tr>
<tr>
<td>Holding Circuit</td>
<td>13</td>
</tr>
<tr>
<td>Pulse Amplifier</td>
<td>15</td>
</tr>
<tr>
<td>Blanking Phantastron</td>
<td>16</td>
</tr>
<tr>
<td>Timing Circuitry</td>
<td>17</td>
</tr>
<tr>
<td>Coincidence Circuitry</td>
<td>20</td>
</tr>
<tr>
<td>Timing of the Function Generator</td>
<td>26</td>
</tr>
<tr>
<td>Storage Circuits and Counter</td>
<td>30</td>
</tr>
<tr>
<td>Circuit Details</td>
<td>32</td>
</tr>
<tr>
<td>Diode Gate</td>
<td>32</td>
</tr>
<tr>
<td>Flip-Flop</td>
<td>34</td>
</tr>
<tr>
<td>Delay Flip-Flop</td>
<td>36</td>
</tr>
<tr>
<td>Holding Circuit</td>
<td>38</td>
</tr>
<tr>
<td>Pulse Amplifier</td>
<td>43</td>
</tr>
<tr>
<td>Comparator</td>
<td>46</td>
</tr>
<tr>
<td>Blanking Phantastron</td>
<td>47</td>
</tr>
<tr>
<td>Testing the Timing and Coincidence Circuitry</td>
<td>51</td>
</tr>
<tr>
<td>Remarks</td>
<td>52</td>
</tr>
<tr>
<td>References</td>
<td>54</td>
</tr>
<tr>
<td>Appendix</td>
<td>55</td>
</tr>
<tr>
<td>Specifications for the Philbrick Operational Amplifiers</td>
<td>55</td>
</tr>
</tbody>
</table>

iii
Acknowledgement

The work described in this thesis is part of a larger project sponsored by the Defence Research Board, Department of National Defence, Canada, under Grant Number DRB C-9931-02(550-GC).

Acknowledgement is gratefully given to Dr. E. V. Bohn, under whose guidance this work was performed, and to Dr. F. Noakes, grantee of the project.

The author is indebted to the National Research Council of Canada for the assistance received through a post-graduate bursary granted in 1954.
T I M I N G  A N D  C O I N C I D E N C E  C I R C U I T R Y  F O R  A  

Introduction

There is an increasing trend in research establishments and industry to solve problems using analog computers. As the name implies such a machine is a model of the physical system in question (11). Each building block of an analog contains electrical or electro-mechanical devices designed to perform a certain mathematical operation or to generate a functional relationship between two computer variables. The inputs and outputs of these blocks are measurable voltages, shaft rotations or distances. These quantities correspond to the parameters in the problem as a consequence of the mathematical analogy which exists between the system performance and the computer performance. The solution, or any parameter, becomes directly observable if its corresponding computer variable is displayed on an oscilloscope or graphed by a recorder.

Existing analog computers completely formulate a problem with a set of continuously operating blocks which are interconnected by feedback loops. Thus, all measurable quantities are available at any time. With such an arrangement identical but independent operations must be performed simultaneously by the duplication of computing blocks. In
comparison, digital computers are time-sequential systems which compute all parameters for a discrete value of the independent variable. The necessary operations are performed in time sequence through one operational unit. One is ultimately led to conceive a computer incorporating desireable properties of both systems (12); namely, the time-sequential operation of digital computers which when applied to analogs minimizes the circuitry, and the analog approach to a problem which facilitates its interpretation.

The advantage of time-sequential operation or time-sharing is apparent when the computer is solving a set of simultaneous differential equations. Such a set might be the flight equations of an aircraft (7, p. 81). Here the computer must generate the coefficients of the derivative terms where these coefficients, in general, are functions of the independent computer variable. Existing analogs generate each function by a costly device such as the cathode-ray photoformer (7, p. 248) or the servo-driven function potentiometer (7, p. 251). Another method approximates a waveform by a series of straight-line or curved-line segments using a network of resistances and diodes (1, p. 315). On the other hand, a computer designed on a time-sequential principle can generate all the required functions with the same basic circuit.

Time-sharing is further appreciated when an analog is used for training men in specialized fields such as instrument flying and aerial gunnery. In this capacity the inputs to the computer are manual deflections of dials and
controls. The resulting computer variables (usually voltages) vary as the corresponding system parameters would in actual operation. Such simulation under manual command requires "real-time" computing speeds and prolonged operation. Because the voltage outputs of d-c. integrators tend to drift over long periods of time these components are not used in standard analogs intended for real-time simulation. Instead integration is performed electro-mechanically (5). However, the relative accuracy, low cost and flexibility of d-c. components make these preferable to the electro-mechanical devices. Fortunately, the affects of voltage drift can be eliminated in time-sharing computers by automatic calibration; hence, d-c. integrators can be used for real-time computation.

The analog computer now being developed in the electrical engineering department of the University of British Columbia has been designed on a time-sharing principle. When completed it will have two desirable features:

1. The function generator and multiplier will accommodate a large number of functions. The function sampling and multiplication processes occur in one operation and the functions need be represented only by a voltage waveform of short duration.

2. A long integration time will be realized using d-c. integrators and a magnetic drum memory.

This thesis is concerned with the timing and coincidence circuitry of the function generator and multiplier. Details apart from the timing circuitry appear in a separate thesis by B. P. Hildebrand (6); however, the author will
borrow from this work in the interest of completeness. The integrator will be the subject of succeeding M. A. Sc. theses.

To simplify initial design the prototype computer will be relatively "slow", hence the response time of various electronic components will not be critical. It is hoped that this machine will solve complex problems with a precision of one or two per cent.
Description of the Function Generator and Multiplier

A function to be generated is graphed on black paper which is cut along the function outline and superimposed on plain white paper. Thus, the area above the function is black and that below is white. The function is then photographed on 35 mm. film and mounted on a slide. Care is taken to guarantee that the absolute maxima of all functions—within the ranges of interest of the independent variables—have equal height on the films. Also, the zero level of all functions must be equidistant from the lower film boundary. Figure 1 illustrates a typical function as it appears on the film together with the calibration frame which will be referred to later. A transition region b precedes each function to permit transient decay in the circuitry.

Each slide representing a function is mounted in a frame which in turn is fastened to a rotating disc. The number of functions which the computer can handle thus depends in part upon the circumference of this disc. The prototype computer accommodates 18. As the disc rotates, a fixed optical system projects a narrow segment of the film on to a phototube and scans each function successively. Consequently, the output of the phototube is a continuously varying positive voltage representing the "ordinate" of all functions in a time-sequential manner. This output is fed into a d-c. amplifier which is biased by a voltage $E_m$ equal to the zero level defined by the calibration frame. Thus, the positive and negative excursions of the amplifier output represent the
Fig. 1. Calibration and function frames on scanning disc.

- marker pulse
- trigger pulses from function frames
- delayed pulse derived from P1
- comparator pulse from coincidence circuitry
- sampling pulse from coincidence circuitry
- comparator pulse from multiplier
- delayed pulse derived from P8

Light → Lens → Scanning Disc → Photo-tube → E_f + E_m

P0, P1, P3, P5
graphed functions in a true voltage analog sense.

By means of the timing and coincidence circuitry (the subject of this paper) each function is successively sampled at a particular value of the abscissa \( x \). In practice, the full abscissa scale is represented by 50 volts and the input voltage specifying the sampling point is some fraction of the full-scale voltage. This input voltage varies slowly relative to the scanning rate; hence, is considered constant over one revolution of the disc.

Immediately after sampling, the voltage \( E_f \) representing a function ordinate is normalized with respect to the maximum ordinate voltage \( E_M \), then multiplied by a reference voltage \( E_r \) whose value is dictated by the computer programme and the limitations of the circuitry. Thus, the output of the multiplier is a voltage \( E_fE_r/E_M \) whose sign is that of the product \( E_fE_r \) (\( E_M \) is always positive). If there are \( N \) functions on the disc there will be \( N \) such voltages during each revolution, and each voltage is channeled to a storage unit where it is available for further operations. All voltages corresponding to the same function frame go to one storage unit.

It should be emphasized that if the optical system described does not provide sufficient resolution for engineering accuracy then the multiplier circuitry is not obsolete. The only requirement of the multiplier is that the function be represented by a voltage waveform. The optical method of generation is certainly the simplest but not the most precise.
Requirements of the Timing and Coincidence Circuitry

The operations of the timing and coincidence circuitry divide into two main categories: the triggering of the sampling circuits at the desired abscissa value, and the timing of the following multiplier operations; biasing, normalization, multiplication and sign determination.

Basic to these operations is the calibration frame illustrated in Fig. 1. When this frame is scanned trigger pulses P1 and P3 occur respectively at the beginning of the frame and at the discontinuity. Also, a pulse P5 marks the beginning of each function frame. The remaining pulses P2, P4, P6, P7, P8 and P9 are derived within the timing and multiplier circuitry. Pulse P6 is significant in that it triggers the sampling circuits at the abscissa \((b + x)\) where \(b\) is the transition region preceding the function. The voltage \(E_m\) fixes the zero level and \(E_M\) is the normalization voltage.

The problem of sampling each function at a discrete abscissa value requires special treatment. As already pointed out the abscissa is represented by a voltage which is proportional to \((b + x)\); but, how can a given voltage represent the same abscissa for different scanning rates? If one could guarantee a constant disc speed the problem would become trivial, but even a slight variation in line voltage would change the speed of the disc sufficiently to destroy any attempt to obtain the required precision. The distance \(a\), fixed in time by the interval between the pulses
Fig. 2. Symbols for computer units.
PI and P3, is used by the coincidence circuitry to eliminate disc velocity \( v \) as a variable in the selection of the sampling point \( b + x \).

The pulse circuitry is designed on the basis of an average scanning time of two milliseconds per function frame and roughly the same time interval between succeeding frames. This circuitry comprises a number of gates, flip-flops, operational amplifiers, etc., whose assigned symbols are illustrated in Fig. 2. The circuit diagrams and specifications of the Philbrick operational amplifiers are included in the appendix. In keeping with their plug-in design most circuits represented in Fig. 2 are constructed on small chassis which are plugged into their assigned positions on a master chassis. Since the linear operating range of the Philbrick amplifiers (model K2-W) is from -50 to +50 volts this working range has been adopted as standard wherever applicable.
General Description of the Components

To facilitate understanding of the overall circuit operations and the design problems encountered, a general description of the components is presented prior to elaboration on the circuit details.

Operational Amplifier

High gain d-c. amplifiers with negative feedback are extensively employed in operational blocks to provide good linearity and to match impedances (a waveform from a high impedance source is frequently required to supply a load). The salient properties which warrant their use are noted here.

In Fig. 3 the open-loop gain of the operational amplifier is $A$ and the fraction of the output voltage which is subtracted from the input voltage is $\beta$. The closed-loop gain is

$$ G = \frac{E_0}{E_i} = \frac{A}{1 - A\beta} $$

and if $A$ is sufficiently large and $A\beta$ much greater than unity

$$ G = \frac{-1}{\beta} $$

Consequently, the gain is essentially independent of the amplifier properties and is determined by the passive elements which determine $\beta$. 
It is easily shown that the output impedance of this amplifier can be made very small. Let \( Z \) be the output impedance of the open-loop amplifier, then the amplifier will deliver \( \frac{A}{Z} \) amp. per input volt into a short circuit across the output. If unit voltage is now applied to the output of the closed-loop circuit by an external source, the current \( I \) drawn from this source is equal to the current through \( Z \) plus the current supplied by the amplifier on being driven by the feedback voltage \( \beta \). That is,

\[
I = \frac{1}{Z} - \frac{A\beta}{Z} = \frac{1 - A\beta}{Z}
\]

Thus, the effective output impedance is \( \frac{Z}{1 - A\beta} \) and this can be made small if \( A\beta \) is large. With a small output impedance the amplifier acts as a constant voltage source.

Frequently negative feedback is obtained by an adding network in the grid circuit (Fig. 4). When the operational amplifier is utilized this way it is convenient to consider its gain and input impedance infinite. Because of feedback the grid voltage \( e_g \) of the amplifier is held virtually at zero and the current through the input impedance \( Z_i \) is equal to the current through the loop impedance \( Z \). That is,

\[
\frac{E_i}{Z_i} = \frac{-E_o}{Z}
\]
and

\[ E_o = -\frac{Z}{Z_1} E_i \]

If \( Z = R \) and \( Z_i = R_i \) a phase inversion is obtained and the output is a low impedance source satisfying

\[ E_o = -\frac{R}{R_i} E_i \]

On the other hand, if \( Z = 1/pC \) and \( Z_i = R_i \)

\[ E_o = -\frac{1}{RC} \int_0^t E_i dt \]

and the circuit acts as an integrator.

Two inputs are available with the operational amplifiers employed in this computer. If phase inversion is required (for negative feedback) one input is used, if no inversion is required the other is used. The remaining input is biased to provide zero output for zero input.

**Diode Gate**

A voltage signal is either passed or blocked by the diode gate depending upon the polarity of two controlling voltages. In the conducting state one control voltage is +60 volts and the other is -60 volts, and in the non-conducting state the polarities are reversed. The gate is a bridge type containing three double diodes and is capable of accurately passing a maximum of +50 or -50 volts. This range is determined by the magnitude of the controlling voltages.
Flip-Flop and Delay Flip-Flop

A bistable multivibrator (denoted as a flip-flop in this text) is used to generate a step function. In this application it has two inputs which accept only negative triggering voltages and two outputs delivering +60 and -60 volts in one state and -60 and +60 volts respectively in the other state. These output voltages control the diode gates. A negative triggering voltage applied to a particular input will always force the circuit into the same state. If the circuit is already in this state, this and succeeding triggers have no effect. Of course, the other input is associated with the opposite state.

The monostable multivibrator (delay flip-flop) has only one stable state and one trigger input. In response to a negative trigger pulse the voltage levels are flipped over into an unstable state whose duration is fixed by the time constant of the circuit. Here, also, two outputs are provided, delivering +60 or -60 volts as described in the preceding paragraph.

Comparator

The two inputs to the comparator are a sweep voltage waveform and a constant reference voltage. At the instant the sweep voltage attains equality with the reference voltage the comparator generates a large negative pulse of very short duration. This pulse is used to start certain operations. In this circuit the reference voltage is negative, hence the sweep must also be negative.
Holding Circuit

In order to store voltages during one revolution of the scanning disc a circuit was developed whose principle of operation is illustrated in Fig. 5. When a step voltage $-E$

![Diagram](image)

Fig. 5. Principle of the Holding Circuit.

is applied to the input the grid of the first amplifier $A_1$ goes negative. Since there is no phase inversion through this amplifier its output is also negative; consequently, the diode conducts and a current $i$ flows in the indicated direction. Because of the high gain of the second amplifier $A_2$ and the negative feedback through $C$, the input grid of this amplifier is held at zero. To offset the tendency for this input to go negative as current is drawn out of $C$, the second amplifier feeds an identical current $i$ into the opposite side of the condenser to build up a balancing positive charge. This operation continues until the output of $A_2$ reaches $+E$. At this point the input to $A_1$ becomes zero due to the equal voltage drops across the two identical grid resistors $R$. Any tendency for the output to exceed $+E$ imposes a positive driving voltage on this input. However, the diode blocks for a positive output from $A_1$ and no current can flow to increase the positive charge on $C$.

The holding action of this circuit is automatic.
As soon as the input voltage is removed the output of $A_1$ is driven positive by feedback from the output of $A_2$; consequently, the diode blocks and the storage circuit is isolated. A small current leak from C through the grid resistor $r$ maintains the grid voltage required to hold the output at $+E$; but, because of this leak the output decays with a time constant $GrC$. A reasonable value for this time constant is about ten minutes.

If the circuit is required to accept a positive input the diode must be inverted so that $A_1$ feeds the plate rather than the cathode.

When the circuit is used for storing a function ordinate $E_f$ it must be capable of accepting both positive and negative voltages. For this reason the circuit features bidirectional control. This requirement was achieved without sacrificing the holding properties of the circuit by inserting a double triode gate in the position occupied by the diode as indicated in Fig. 6. When a positive control voltage $E_c$ is applied to both grids of the double triode conduction is possible in either direction and when a negative voltage $-E_c$ is applied, both triodes are cut off and the holding action is effected. Obviously, the automatic clamping action of the

![Fig. 6. Bidirectional Holding Circuit.](image)
diode has been sacrificed and external control is now required.

If the control voltages are applied only to one triode and the second triode is connected as a diode (grid connected to plate) a unidirectional circuit is achieved with the option of bidirectional control.

Figure 7 represents the holding circuit as it is illustrated in the circuit diagrams which follow. If the circuit is unidirectional one input to the triode gate is connected to the corresponding plate and if bidirectional, both inputs are connected together.

![Fig. 7. Block diagram of the Holding Circuit.]

Pulse Amplifier

As already stated pulses P1, P3 and P5 are required at the discontinuities of the calibration frame and at the beginning (rising edge) of each function frame. Since the scanning beam has a finite width the rising edges appear at the output of the photo-tube amplifier as voltage ramps. The pulse amplifier was designed to guarantee that a pulse occurs within a few microseconds after a ramp is initiated. This circuit consists of an amplifier which amplifies the ramp and whose output triggers a blocking oscillator within the required time interval. When triggered the blocking oscillator emits a large negative pulse whose duration is a few microseconds.
Blanking Phantastron

If the function being scanned varies rapidly it is capable of triggering the pulse amplifier and undesirable pulses are emitted; consequently, a circuit is required to blank the input of the pulse amplifier, after P5 has occurred, for the duration of the function frame. Since the scanning speed is not constant this blanking interval must be inversely proportional to the velocity of the disc. The phantastron has the property that on being triggered it generates a square pulse whose duration is inversely proportional to an input reference voltage. If this reference voltage is proportional to the disc velocity then the resulting pulse can be used to blank the pulse amplifier.
Timing Circuitry

The operation of the coincidence circuits and function generator is timed by an ordered sequence of "pulse-pairs" which trigger a number of flip-flops. For example, if P1 triggers a flip-flop and P3 returns it to its original state then (P1, P3) is a pulse-pair corresponding to the flip-flop which they actuate, and the two output states of this flip-flop are denoted P1 and P3.

The timing circuitry is illustrated in Fig. 8. In describing its operation no attempt will be made to justify the choice of pulse-pairs for this will become obvious when the coincidence circuitry and multiplier are discussed.

The timing is initiated by a pulse PO derived from a reference marker on the disc which precedes the calibration frame. This pulse sets flip-flop FF1 into its PO state and the positive output is fed to the gate of pulse amplifier PA2 which now will accept any rapidly rising waveform arriving from D, where D is connected to the output of the photo-tube amplifier.

The first rising edge of the calibration frame triggers pulse amplifier PA2 which generates P1. This pulse is accepted by flip-flops FF1, FF2, FF3 and delay flip-flop DFF1, and all are forced into their P1 state. Since PA2 is now blocked by the negative output of FF1 no further pulses occur in this branch until PO, marking the start of the next revolution of the disc, initiates the next cycle. Delay flip-flop DFF1 remains in its P1 state for approximately
Fig. 8. Timing Circuits
1/2 millisecond then returns to its stable P2 state. The derived pulse P2 is indicated in Fig. 1.

Since the positive output of flip-flop FF3 is applied to the gate of pulse amplifier PA3, this circuit responds to the second rising edge of the calibration frame. The resulting pulse P3 triggers flip-flop FF8 and resets FF3. PA3 is now blocked until P1 occurs in the next revolution of the disc. Both flip-flops FF2 and FF8 are reset by pulse P4 originating in the coincidence circuitry.

The situation is slightly different for the branch fed by PA1. This pulse amplifier responds to the initial rising edge of each function frame, for the generated pulse triggers the blanking phantastron BPH which blocks PA1 for the duration of the function frame. Thus PA1 generates P1 and successive P5's which all trigger flip-flops FF4 and FF5. These flip-flops are returned to their original states by pulses P6 and P8 before the next pulse from PA1 arrives. P6 is derived in the coincidence circuitry and P8 in the multiplier. The pulse pairs (P1, P6) and (P1, P8) have not been indicated in Fig. 8 since they are not essential to the operation of the function generator. A possible use for them will be discussed later.

The remaining pulse pairs are derived from pulses P6 and P8. P6 triggers delay flip-flop DFF2a into its unstable state and when it returns to its normal state about 200 microseconds later the derived pulse P7 triggers flip-flop FF6. On arriving from the multiplier, P8 triggers flip-flop FF7 and delay flip-flop DFF2b. About 200 microseconds later DFF2b
returns to its stable state and the derived pulse P9 resets both flip-flops FF6 and FF7.

It should be stressed that the pulses generated by pulse amplifiers PA2 and PA3 occur only when the calibration frame is being scanned. All other pulses reoccur for each function frame.
The Coincidence Circuitry

The operation of the coincidence circuitry is based on a multiplication system tested successfully by Freeman and Parsons (3). Its principle is illustrated in Fig. 9. Two voltages $E_1$ and $E_2$ are simultaneously applied to two identical linear networks whose response to unit voltage is $N(t)$. The outputs are then $E_1 N(t)$ and $E_2 N(t)$. If on comparing $E_1 N(t)$ with a reference voltage $E_3$, the second sweep $E_2 N(t)$ is clamped at the instant of equality, then, $N(t) = E_3 / E_1$ and the output is

$$E = E_2 N(t) = E_2 \frac{E_3}{E_1}$$

The absence of settling time makes this multiplier useful for time-sharing applications. A product is available at the instant the comparator notes equality between one of the sweeps and the reference voltage. Immediately after this product has been stored the input voltages can be changed, the sweeps regenerated, and a second product is available. In comparison, multipliers which generate a product proportional to the average value of a cyclic waveform require low pass filtering over several cycles (4, 8, 10). The output of these multipliers is not available until their transient response has decayed, hence they are not suitable for applications requiring sudden changes of the input data.
As already mentioned the coincidence circuitry eliminates the disc velocity \( v \) as a parameter in the selection of the sampling point \((b + x)\). In the description to follow it is assumed that \( v \) is constant for at least one revolution of the disc.

Suppose \( E_1 \) in Fig. 9 is a voltage proportional to \( 1/v \) and both \( E_2 \) and \( E_3 \) are constant reference voltages; then, \( E = E_2E_3/E_1 \) is directly proportional to \( v \). If now \( E \) is stored it can be used to drive an integrator whose output \((-Et/RC)\) is compared to a reference voltage \(-K(b + x)\), where \( K \) is a constant. When equality is reached the comparator triggers the sampling circuit and resets the coincidence circuitry for the next function.

The problem is now solved, for in the time \( t \) required for the integrator output to reach equality with \(-K(b + x)\) the function frame has travelled a distance \( d = vt \).

Substituting \( t = d/v \) in the expression \(-Et/RC\) the velocity terms cancel (a velocity term is implicit in \( E \)), and by a proper choice of time constants and coefficients it can be arranged that \( d = (b + x) \).

In the block diagram of the coincidence circuitry (Fig. 10) the diode gates DG1, DG3 and DG5 are controlled by flip-flop FF8, DG2 and DG4 by FF2 and DG6 by FF4. The letters N and C imply non-conduction and conduction, respectively. \( E_{r1}, -E_{r2} \) and \(-E_{r3} \) are constant reference voltages which have the indicated sign.

A voltage \( E_1 \) proportional to \( 1/v \) is obtained by the integrator in the upper half of Fig. 10. This integrator
v = velocity of function frame
a = distance between P1 and P3 on calibration frame

\[ N(t) = \frac{vR_2C_2 E_{r3}}{a E_{r1}} \]

Fig. 10. Sweep and Coincidence Circuits.
is operative only when DG1 is conducting and DG2 non-conducting; consequently, a consideration of the states of these gates will show that integration is initiated by P1 and stopped by P3. But P1 and P3 define the time interval \( t_1 \) required to scan the distance, \( a \), on the calibration frame when the disc velocity is \( v \). Thus, \( t_1 = \frac{a}{v} \) and the output of the integrator at the end of this time is a voltage

\[
E_1 = -E_{rl} \frac{t_1}{R_2C_2} = -E_{rl} \frac{a}{vR_2C_2}
\]

The counterpart of the two identical sweeps \( N(t) \) of Fig. 9 are the two exponential sweeps with time constant \( R_1C_1 \) in Fig. 10. Thus,

\[
N(t) = (1 - e^{-\frac{t}{R_1C_1}})
\]

Furthermore, in the notation of Fig. 10

\[
E_2 = -E_{r2} \quad E_3 = -E_{r3}
\]

The two sweeps are simultaneously initiated by P3 (diode gates DG3 and DG5 are rendered non-conducting) and when the first sweep \(-E_1N(t)\) reaches equality with \(-E_{r3}\) the comparator M1 emits pulse P4 which triggers FF8 and stops both sweeps. Meanwhile, the holding circuit has accepted the peak value of the second sweep and its output \( E \) is clamped at this value when DG5 discharges \( C_1 \). The magnitude of \( E \) is fixed by the magnitude attained by \( N(t) \). That is,

\[
-E_{rl} \frac{a}{vR_2C_2} N(t) = -E_{r3}
\]

or

\[
N(t) = \frac{vR_2C_2}{a} \frac{E_{r3}}{E_{rl}}
\]
Hence,

\[ E = E_{r2} N(t) = \frac{v R_2 C_2 E_{r2} E_{r3}}{a E_{r1}} \]

This voltage is held for the full revolution of the disc and is used to drive the adjacent integrator.

Each pulse P5, which designates the beginning of a function frame, starts the integrator by throwing DG6 into its non-conducting state. The output of this integrator is fed into a second comparator M2 where it is compared with a voltage \(-K(b + x)\). After a time \(t_2 = (b + x)/v\) equality is reached and the resulting pulse P6 triggers the sampling circuitry.

The holding circuit, storing voltages of one sign only, is unidirectional. In order that its output be proportional to \(v\), the circuit must always accept the peak value of the sweep \(-E_{r2} N(t)\). If this peak decreases faster than the output of the holding circuit, it is not accepted and control is lost. Consequently, the output decay rate must be adjusted to accommodate any anticipated rate of decrease in \(v\).

In selecting time constants and voltage levels, the properties of individual circuits were considered. The reference voltage \(E_{r1}\) was arbitrarily chosen as 50 volts. On the other hand, since the output amplifier of the holding circuit is linear in the range \(-50\) to \(+50\) volts, \(-E_{r2}\) was fixed at \(-100\) volts to permit a well-defined peak sweep voltage of the order of \(-50\) volts. For the same reason \(-E_{r3}\) was fixed at \(-25\) volts. If it is larger the sweep waveform would
start to level off before equality with $-E_{r3}$ is reached, thus the trigger point for M1 would be poorly defined. The abscissa range is 0 to -50 volts.

With this information the ratio of the integration time constants can be determined. Recall that P6 occurs when

$$-E \frac{(b + x)}{vR_3C_3} = -K(b + x)$$

or

$$\frac{E_{r2}E_{r3}}{E_{r1}} \frac{vR_2C_2}{a} \frac{(b + x)}{vR_3C_3} = K(b + x)$$

When $(B + x)$ is equal to the full-scale abscissa value $s$ where $s = 2a$, the abscissa input is 50 volts. On substituting this information and the values of the reference voltages into the above expression it becomes

$$\frac{(-100)(-25)}{50} \frac{R_2C_2}{R_3C_3} \frac{2a}{a} = 50$$

or

$$\frac{R_2C_2}{R_3C_3} = \frac{1}{2}$$

Furthermore, since $Ks = 50$, $K = 50/s$.

In fixing the values of the components the following limitations of the circuitry have to be considered. Diode gate DG6 must discharge $C_3$ within two milliseconds, the approximate time interval between function frames (the discharge action of the diode gates will be discussed later). In the one millisecond interval between P1 and P3 the output of the first integrator should reach about 40 volts; this permits a 20% decrease in the disc speed without exceeding the linear operating limit of the operational amplifier. The size of
the sweep resistor $R_1$ must limit the output current of the first integrator to one milliampere. The sweep time constant $R_1C_1$ should be roughly 1/2 millisecond if the pulse $P_4$ is to occur in the second half of the calibration frame. With these considerations the component values selected are:

$$
R_1 = 68 \text{ K}, \quad C_1 = 0.01 \mu\text{f}, \\
R_2 = 500 \text{ K}, \quad C_2 = 0.002 \mu\text{f}, \\
R_3 = 1 \text{ Meg}, \quad C_3 = 0.002 \mu\text{f}.
$$

It is interesting to note that precision is required only in fixing the values of the time constants; the values of the component $R$'s and $C$'s need not be precise.

![Diagram](image)

**Fig. 11.** Method for obtaining two identical sweeps.

The method used to obtain two identical $R_1C_1$ sweeps is illustrated in Fig. 11. An a-c. signal was applied to both integrators and the two outputs were connected across an oscilloscope. Since the gain of a K2-W is high slight differences between amplifiers will not affect the output of either integrator. Because the outputs are low impedance sources pickup is not troublesome and a ground connection is not required on the oscilloscope. The three components $R_1$, $C_1$ and $C_1'$ were selected without regard to precision and the resistor $R_1'$ was varied until the a-c. signal on the oscilloscope was negligible, indicating equality of the time constants.
Timing of the Function Generator

The details of the function generator and multiplier can be found in P. Hildebrand's thesis (6). Its operation is described here to justify the circuitry of Fig. 8.

The three channels of the assembly are illustrated in Fig. 12. All three channels and the timing circuits are fed by the photo-tube amplifier which consists of two inverters in cascade providing a gain of 100. Since the output of the photo-tube varies from 0 to approximately 1 volt, the output of the amplifier varies from -50 to +50 volts after biasing.

Biasing, or the establishment of the zero level, is provided by the holding circuit in channel 3. Pulse P1, which introduces the calibration frame, triggers the delay flip-flop DFF1 which in turn renders the triode gate TG2 conducting; thus, the holding circuit charges up to a voltage \(-E_m\). When DFF1 returns to its stable state 1/2 millisecond later, TG2 is cut off and the stored voltage is held for the whole revolution of the disc. At the same time DG15 becomes conductive and \(-E_m\) is fed back to the input of the photo-tube amplifier. Suitable scaling is provided by the input grid resistors and the net effect is that the amplifier delivers zero volts when the photo-tube output is \(E_m\). Besides establishing a zero level, feedback also eliminates the affect of d-c. drift, for this affect is slow relative to the scanning rate and biasing, hence self-correction, occurs once every revolution.
E (Fig. 13)

Fig. 12. Function Generator and Multiplier Assembly.
Channels 1 and 2 perform a multiplicative operation similar to that performed by the coincidence circuitry. The output of this multiplier is a voltage \( \frac{E_f E_r}{E_M} \) where \( \frac{E_f}{E_M} \) is the normalized function ordinate and \( E_r \) is a reference voltage which sets the voltage level of \( \frac{E_f E_r}{E_M} \) in storage. The reason for normalizing is to provide a product which is independent of the gain of the system, for there is no assurance that this gain will remain constant.

The unidirectional holding circuit in channel 1 charges up to the peak ordinate \( E_M \) of the calibration frame and automatically holds this voltage. If the succeeding function frames have positive maxima the holding circuit accepts these peaks and the charge lost by the slow discharge of the storage circuit is replaced. Initially, however, this circuit charges up to the zero level \( E_m \). Since the gain of the photo-tube amplifier is likely changed by biasing, \( E_M \) will differ slightly from \( E_m \). Consequently, to guarantee that the holding circuit will accept the maximum ordinate \( E_M \) the triode gate TG1 provides bidirectional control during the charging interval from P3 to P4.

In channel 2 the diode gates DG8, DG9, DG10 and DG11 are conducting on the arrival of a function frame; thus the voltage across the condenser \( C_2 \) follows the function ordinate (with inversion). This voltage is clamped at the ordinate \( E_f \) corresponding to P6 when DG10 reverts to its non-conducting state.

The voltages \( E_M \) and \( E_f \) required to drive two identical sweeps are now available. One sweep is the \( R_1 C_1 \) circuit.
in channel 1; the other is more difficult to obtain since a constant voltage source of $E_f$ is not present. However, a simple analysis of the integrator in channel 2 shows that when this integrator is fed by a charge on $C_2$ its output is

$$E_f \frac{C_2}{C_3} (1 - e^{-\frac{t}{R_2C_2}}).$$

If $C_2 = C_3 = C_1$ and $R_2 = R_1$, two identical sweeps are realized. These sweeps are initiated by $F7$ which makes both DG7 and DG12 non-conducting.

The system employed to establish the correct sign of the product $E_fE_r/E_M$ requires the generation of two sweeps in channel 2; $+E_rN(t)$ and $-E_rN(t)$, where $E_f$ may be positive or negative. The integrator just considered generates $E_rN(t)$ at B. Since DG8, DG9 and DG10 are now non-conducting the output of this integrator is fed to the inverter following DG8. Its output, $-E_rN(t)$, appears at C. At this point three sweeps are in progress; $-E_mN(t)$ at A, $E_rN(t)$ at B and $-E_rN(t)$ at C. When $-E_mN(t)$ reaches equality with $-E_r$ the comparator M3 generates pulse P8 which blocks DG11 and clamps both sweeps in channel 2. The sweep in channel 1 is terminated by P9. Thus, a voltage $E_fE_r/E_M$ is held at B and a voltage $-E_fE_r/E_M$ at C. Which voltage is directed into storage depends upon the sign of $E_f$ and $E_r$.

The sign of the product is fixed by the state of flip-flop FF9. This state determines which of the gates DG13 or DG14 is conducting. Diode gates DG16 and DG17 also are controlled by this flip-flop. Normally DG16 is conducting and DG17 non-conducting; hence, if $E_r$ is negative the
comparator M4 is not triggered since $E_r$ is less than ground potential. Flip-flop FF9 then remains in its initial state. In this state diode gate DG14 is conducting and the sign of the product is determined by the sign of $-E_f$. Furthermore, the voltage fed to M3 is of correct sign for comparison with $-E_{MN}(t)$. Alternatively, if $E_r$ is positive comparator M4 triggers flip-flop FF9; diode gate DG13 conducts and the sign of the product is that of $E_f$. Again the reference voltage fed to M3 is of correct sign, for diode gate DG17 is now conducting. Pulse P9 derived from P8 resets flip-flop FF9 for the next function.
Storage Circuits and Counter

The storage circuits are identical to the holding circuit except that the Philbrick amplifier and the triode gate are common to all. The counter illustrated in Fig. 13 determines which storage circuit $S_n$ is accessible. If there are $N$ functions being generated this counter contains $N$ flip-flops. Each flip-flop controls the access gates corresponding to a particular storage circuit.

The counting operation is initiated by the marker pulse $P_0$ which forces all flip-flops into the same state except $FFS_1$, which takes on the opposite state. In this orientation all storage circuits are inaccessible except the first. When $P_9$ occurs at the end of the first function frame the only flip-flop which is in a state that will accept it is $FFS_1$. Its output triggers $FFS_2$ and the storage circuit $S_2$ is now accessible. At the end of the second function frame $P_9$ triggers $FFS_2$ which in turn flips over $FFS_3$. This process continues until $P_9$ occurring at the end of the $N$th function frame returns $FFS_N$ to its original state. It completes the cycle by resetting $FFS_1$.

Suppose the storage circuit $S_n$ is accessible; then the three gates in this circuit are conducting. Diode gate $DG_{1n}$ permits $S_n$ to charge up to $-E_F E_T/E_M$ where $E_F$ is the ordinate corresponding to the $n$th function. $DG_{2n}$ completes the feedback loop through $R$ to the input grid of the Philbrick amplifier and $DG_{3n}$ permits the channeling of $-E_F E_T/E_M$ to other parts of the computer. It was mentioned previously that the
Fig. 13. Counter and Function Storage.
circumference of the scanning disc was one factor which limited the function capacity of the computer. Obviously, the remaining factor is the number of storage elements provided. However, since the cost of a storage circuit is small this is not a serious limitation.
Diode Gate

The bidirectional gates used in this project (Fig. 14) were developed by J. Millman and T. H. Puckett (12). They are capable of accurately passing any voltage lying in a range defined by the control voltages. Since the working voltages in the computer vary between +50 and -50 volts the control voltages for the gates were chosen as +60 and -60 volts to accommodate variations in the flip-flop outputs arising from the use of non-precision resistors. The gates feature several advantages, among which the following have been exploited: during conduction the gain through the gate is very close to unity, in fact, only for small voltages does the deviation from unity exceed 0.5% (7, p. 24); the gain during conduction is insensitive to unbalance in the control voltages; leakage through the gate is negligible during non-conduction; and the gate rapidly becomes non-conducting if the control voltages have ideal step waveforms.

Figure 14 shows that both V1a and V1b are conducting when the gate is non-conducting. Since there is very little voltage drop across these tubes the plate of V3a is at -60 volts and the cathode of V3b at +60 volts. Consequently, both V3a and V3b are blocked and the output is completely isolated from the input. In the conducting state both V1a and V1b are blocked and current flows from +E to -E through both halves of V3. Depending upon the sign of the input, either V2a or V2b starts to conduct and the bridge properties of the network come into play and force a balance between input and output.
Fig. 14. Diode Gate.

R₁ - 1 K. Pot., Mallory
R₂ - 1 Meg., 10%, 1/2 watt
E - 300 volts
C - 60 volts
N - 60 volts

V₁, V₂, V₃ - 6AL5
It is interesting to note that at balance a load on the output is fed by the +E and -E supplies and not by the input; thus even during conduction the output is isolated from the input. This isolation is apparent when a charged condenser C is being discharged through the gate to ground. Suppose the output is grounded, then both the plate of V1a and the cathode of V3b try to attain ground potential. If the input voltage is positive V2a blocks and the condenser can only discharge through V2b. This, however, raises the potential of the cathode of V3b to that of the input and this tube also blocks. Consequently, the condenser discharges through R2 to the -E supply and control is obtained as soon as the input reaches ground potential. The effective time constant of this discharge to ground is not \( R_2 C \) but something considerably smaller as implied by Fig. 15.

Fast discharges can be obtained by decreasing the value of \( R_2 \); however, this results in an increased current drain from the regulated power supplies which is not desirable. Operations requiring gates with high back impedance and fast discharge action could be adequately performed by a discharge triode rather than the diode gate.
Flip-Flop

The operation of the flip-flop (Fig. 16) depends upon the fact that a stable voltage configuration exists with Vla on and Vlb off, or vice versa. Suppose Vla is on and Vlb off; then, the plate voltage level of Vlb is fixed entirely by the current passing through the resistors $R_1$ and $R_2$, while the plate level of Vla is lower since its plate resistor $R_1$ is carrying the additional tube current. The operating point of either Vla or Vlb and the values of the resistors $R_1$, $R_2$ and $R_3$ are so chosen that the plate of the conducting tube is at -60 volts and that of the non-conducting tube at +60 volts. It is apparent in the circuit diagram that the cathode follower outputs follow the plate voltages. The grid levels of Vla and Vlb are fixed by the voltage divider in either cathode circuit of the output triodes. A grid may be at -160 or -210 volts depending upon the state of the circuit.

Returning to the initial supposition, if Vla is conducting then a negative trigger applied at the input (pin 4) passes through the diode V3a and cuts Vla off. The rapid rise of the plate of Vla is transmitted by $C_2$ to the grid of Vlb which starts to conduct, and in turn, augments the action of the trigger by feeding a negative rising edge from its plate to the grid of Vla through the second coupling condenser, also labeled $C_2$.

Since the cathodes of V3a and V3b are at -150 volts and their plates at -160 or -210 volts these diodes conduct only when a negative pulse is applied to the inputs. Thus,
Fig. 16. Flip-Flop (Bistable Multivibrator).
a diode clips the trailing edge of the input pulse and prevents this positive portion from triggering the flip-flop back into its original state. Furthermore, a diode isolates the flip-flop from the external circuitry; a change of state initiated at one input cannot be transmitted through a diode to the opposite input.

This flip-flop differs somewhat from conventional designs (13, p. 164) in that the discharge resistors normally in parallel with the coupling condensers are now in the cathode circuits of the output tubes. Thus, the plate of one flip-flop triode is isolated from the grid of the other as far as d-c. voltage levels are concerned. The advantage is that an additional degree of freedom is obtained to fix the two output levels at the desired +60 and -60 volts.

Full load occurs for the flip-flop output which is negative when a maximum number of diode gates are non-conducting. Each gate then draws 0.36 ma. from this output; hence, the resistors $R_4$ and $R_5$ must carry sufficient current to supply both the full load and the tube requirement to maintain the cathode follower action.

As mentioned, the voltages controlling the diode gates must exceed 50 volts in absolute value. In some cases 10% variation in the values of the resistors used in the flip-flop could yield outputs which do not satisfy this requirement. For this reason the following precautions are necessary:

1. The ratio $R_1/R_2 = 240/360$ must be satisfied closely if the positive output is to be +60 volts.
2. The ratio $R_4/R_5 = 220/140$ (though not as critical as $R_1/R_2$) must be approximated to ensure the correct operating point for the flip-flop.

3. The resistors $R_1$ and $R_3$ should be close to design value to guarantee an acceptable negative output.

**Delay Flip-Flop**

The basic operation of the delay flip-flop (Fig. 17) is embodied in both the top and bottom half of the circuit diagram. Consider the top half. Initially $V_{1a}$ is conducting and $V_{2a}$ non-conducting (the grid level of $V_{2a}$ is about 25 volts more negative than that of $V_{1a}$). A negative trigger voltage applied to the grid of $V_{1a}$ cuts this tube off and the resulting positive plate rise is fed through $C_1$ to the grid of $V_{2a}$. This tube starts to conduct and continues to conduct as long as its cathode voltage level (which follows the grid level) is sufficiently high to cut off $V_{1a}$. Since there is no d-c. coupling between the plate of $V_{1a}$ and the grid of $V_{2a}$ a positive rise on the plate of $V_{1a}$ appears on the grid of $V_{2a}$ as a positive rise followed by an exponential decay. As soon as the grid level of $V_{2a}$ approaches that of $V_{1a}$, $V_{1a}$ conducts and the plate-grid coupling through $C_1$ rapidly forces $V_{2a}$ into its normal non-conducting state.

The output of the cathode follower $V_{3a}$ follows the plate of $V_{2a}$. This output is +60 volts in the stable state and -60 volts while $V_{2a}$ is conducting.

The plate of $V_{1a}$ cannot provide an output of opposite polarity because the waveform on this plate is not square
Fig. 17. Delay Flip-Flop (Monostable Multivibrator).

DFF1 - 500 microseconds delay.
but similar to the inverted cathode waveform. For this reason the second output is obtained from the independent lower circuit. Alternatively, the output of V3a could have been inverted using a d-c. amplifier. In either case the number of additional tubes required is equal; however, the use of two independent circuits eliminates time delay between the leading edges of both outputs. This delay is unavoidable when using an inverter.

The operation of the lower circuit is similar to that already discussed except that V1b is normally conducting and V2b non-conducting. The negative triggering voltage must now be applied to the plate of V2b rather than the grid since no inversion is required.

The duration of the quasi-stable state is determined by the time constant of the voltage exponential on the grid of either V2a or V1b (the charge on C1 decays through R5 to ground and that on C2 through R4 to ground). Of course, the amplitude of this exponential must also be considered. In the upper circuit the trigger pulse is amplified hence this circuit is more easily triggered than the lower one; in fact, to decrease its sensitivity to pick-up the resistors R8 and R9 were selected so that only pulses exceeding -20 volts can trigger the circuit. A 1/2 millisecond quasi-stable state for delay flip-flop DFF1 was achieved with $C_1 = 470 \mu\text{uf}$.

The delay flip-flops DFF2a and DFF2b do not control any gates, hence there is no need to provide them with two outputs. The only requirement is that the trailing edge of the output pulse be capable of triggering a flip-flop. Since
Fig. 18. Delay Flip-Flops DFF2a and DFF2b.  
200 microseconds delay.
this pulse is only about 200 microseconds wide, it will not trigger a flip-flop when applied directly to the circuit. The reason is that the flip-flop input tends to differentiate this pulse; but, because of the time constant of the input network, the initial rise has insufficient time to decay before the trailing edge of the pulse arrives. Consequently, the full negative edge is not passed by the input diode and the circuit does not trigger.

The difficulty was overcome by differentiating the output pulse of the delay flip-flop, amplifying the derivative, and applying the resulting waveform to the flip-flop. The time constant of the input circuit of the flip-flop now is not so critical since the incoming pulses are larger and have sharp triggering edges.

Both delay flip-flops DFF2a and DFF2b are identical and are contained in the same chassis. Their circuit diagram is illustrated in Fig. 18.

Holding Circuit

The operation of this circuit has been discussed already so the important details of Fig. 19 are now considered. Note that the first amplifier is a Philbrick K2-W. Its high gain and rapid response are required here to accurately control the value of the stored voltage. This amplifier responds to the error between the input and output voltages; hence, the smaller this error need be to ensure control, the more precise is the output. The second amplifier is an adaptation of the K2-W. Very high gain and high frequency response is not a
R₁ - 1 Meg., 0.1%
R₂ - 10 K. Pot., Mallory
R₃ - 1 Meg., 10%
R₄ - 220 K., 10%
R₅ - 2.2 Meg., 10%
R₆ - 470 K., 10%
R₇ - 68 K., 10%
R₈ - 120 K., 10%, 1 watt
R₉ - 2.7 Meg., 10%
R₁₀ - 4.7 Meg., 10%
R₁₁ - 1.5 K., 10%
R₁₂ - 33 K., 10%
R₁₃ - 15 K., 10%
C₁ - 0.5 μf. Polystyrene
C₂ - 50 μf.
C₃ - 10 μf.
C₄ - 470 μf.
C₅ - 0.01 μf.

For bidirectional control (positive and negative voltage storage) both grids of TG are connected in series.

Fig. 19. Holding Circuit.
requirement for this amplifier since its sole purpose is to store a voltage. The value of this voltage is fixed entirely by the adding network at the input of the K2-W and by the response of the K2-W. Since several storage circuits are required in the computer an inexpensive holding amplifier is desireable.

One input of both amplifiers is biased by a resistive network between ground and either power supply. If the signal is applied to the (+) input the (-) input is biased negatively. Alternatively, if the signal is applied to the (-) input the (+) input is biased positively. Both methods are illustrated in Fig. 19. Assuming that the two resistors $R_I$ in the adding network are equal, the bias on the K2-W establishes equality between the absolute values of the input and stored voltages. The 10 K. potentiometer in this bias circuit permits a 1.5 volt variation in the output. The bias on the second amplifier fixes the holding time constant of the storage circuit. The value of this bias determines the voltage differential which must be maintained between the two input grids to hold the output (stored voltage) at its initial level. This differential is obtained by a current leak from the storage capacitor $C_I$ through the grid resistor $R_3$. It is possible to adjust this bias so that no current leak is required. However, the amplifier in this case tends to drift (slight variations in ground level are integrated and the output voltage wanders) and the required differential is not constant for all values of the stored voltage. It is important then that the bias be set to guarantee an output decay
for any stored voltage.

In order that the holding amplifier never be driven beyond its linear operating range a resistor $R_{12}$ limits the current into the storage condenser $C_1$ to one milliampere at maximum output voltage of the K2-W. If the linear range is exceeded the output overshoots before control is established. Thus, when a diode is used for automatic control this diode blocks and considerable time is required for the output to decay to its desired level.

A disadvantage of this circuit is its tendency to oscillate during the charging process due to coupling through the power supplies. This oscillation was reduced to a tolerable minimum by the insertion of a small resistor $R_{11}$ in the feedback loop of the holding amplifier. With $R_{12} = 33 \text{ K}$, $R_{11} = 1500 \text{ ohms}$ and an input of 45 volts the total fluctuation in output due to both overshoot and oscillation was 0.025 volt (0.05% variation). A stable, low impedance power supply should improve this precision.

It can be shown that the holding circuit is basically stable. In Fig. 20 the current through $R$ is equal to the sum of the currents through $r$ and $C$. Thus

\[ \frac{1}{2}(e_i + e_o) \]

Fig. 20. Schematic Holding Circuit for stability analysis
\[ \frac{e_1 - e_g}{R} = \frac{e_g}{r} + (e_g - e_o)PC. \]

Also

\[ e_o = -\Delta e_g \]

and

\[ e_1 = \frac{1}{2} (e_i + e_o)G. \]

Combining equations

\[ \frac{e_1}{R} = e_g\left(\frac{1}{r} + \frac{1}{R} + PC\right) - e_oPC. \]

\[ \frac{1}{2} (e_i + e_o)G = -e_o\left[pRC + \frac{1}{A} (1 + \frac{R}{r} + pRC)\right]. \]

\[ e_i = -e_o\left[1 + \frac{2}{G} \left[pRC + \frac{1}{A} (1 + \frac{R}{r} + pRC)\right]\right]. \]

For the system to oscillate

\[ \frac{2}{G}\left[pRC + \frac{1}{A} (1 + \frac{R}{r} + pRC)\right] = -1 \]

where both \( G \) and \( A \) are functions of \( p \). Rewriting this expression and substituting \( p = j\omega \)

\[ j\omega(2RC + \frac{2RC}{A}) + \frac{2}{A} (1 + \frac{R}{r}) = -G \]

To determine if a solution to this equation exists the function \( G(p) \) and \( A(p) \) should be known. These were approximated from the response curves of both amplifiers used as inverters. Each amplifier in turn was set up as in Fig. 21 and a 15 volt (peak-to-peak) a-c. signal was applied at the input. The input was compared to the output on an oscilloscope screen and the gain and

Fig. 21. Inverter for determining \( G \).
Fig. 22. Measured frequency response and calculated open-loop gain of the Philbrick and Storage Amplifiers.
phase relations were measured over a frequency range from 20 to 300,000 c.p.s. The db. gain and phase lag over this range are graphed for both amplifiers in Fig. 22. The curves for open-loop gain were obtained from the expression

\[ e_0 = - \frac{e_1}{1 + \frac{e_0}{G}}. \]

Hence,

\[ G = -2 \frac{e_0/e_1}{e_0/e_1 + 1}. \]

Substituting the component values \( R = 33 \, \text{K} \), \( r = 1 \, \text{Meg} \) and \( C = 0.5 \, \mu\text{f.} \) into equation (1),

\[ j\omega(0.033 + \frac{0.033}{A}) + \frac{1}{A}(2.066) = -G. \]

At frequencies below 1000 c.p.s. \( A \) is large and this expression can be simplified to

\[ G = -j\omega(0.033) \]

or

\[ |G| = 0.033\omega \quad \angle G = -90^\circ \]

But \( G \) has a phase lag of \(-90^\circ\) at some frequency beyond 200 Kc., which implies

\[ |G| = 0.033(200,000)(2\pi) = 41,500. \]

Since \( |G| \) does not exceed 15,000 there is no solution at low frequencies.

At frequencies above \( 10^5 \) c.p.s. both \( G \) and \( A \) are small. Rewriting equation (1),

\[ GA = -(0.033j\omega + 0.033A\omega + 2.066). \]

This expression cannot be satisfied at high frequencies since the product \( GA \) is small and \( \omega \) is very large.
At an intermediate frequency of roughly 4000 c.p.s. \((\ln 4000 = 8.3)\) the magnitude of both sides of the preceding expression do correspond. However, the phase of \(G_A\) is about \(-12^\circ\) (sum of the angles of \(G\) and \(A\)) and that of the left side is close to \(-90^\circ\). Thus it can be safely concluded that the circuit is basically stable.

Coupling through the power supply was definitely confirmed by using both amplifiers as inverters and connecting both to the same power supply. When an a-c. signal was applied to the Philbrick amplifier a voltage of comparable magnitude and same frequency was detected at the output of the storage amplifier even though there was no direct inter-connection.

A final consideration in this circuit is the holding condenser \(C_1\). A long time constant and accurate voltage storage can be achieved only if this condenser is of good quality. It must have negligible current leakage and small charge absorption. These properties are obtainable in polystyrene condensers.

**Pulse Amplifier**

It is assumed that the output of the photo-tube amplifier corresponding to the rising edges of the calibration frame and function frames is a ramp rising to 50 volts in 1/10 millisecond. Hence, the pulse amplifier must respond rapidly to a wave-form with a positive slope of 0.5 volts per microsecond. Two amplifying stages are provided in Fig. 23 to increase the slope of the incoming waveform. The
Input for PA2 and PA3 (gate controlled by flip-flop).

R₁ - 220 K., 10%  C₁ - 470 μf.
R₂ - 100 K., 10%  C₂ = 0.02 μf.
R₃ - 22 K., 10%  C₃ - 0.01 μf.
R₄ = 1 Meg., 10%  C₄ = 0.001 μf.
R₅ - 270 K., 5%  V₁ - 12AX7
R₆ = 2.2 Meg., 5%  V₂ - 6AK5
R₇ - 150 K., 5%  V₃ - 6AQ5
R₈ - 680 K., 5%  

PA₁ (gate controlled by phantastron).

Fig. 23. Pulse Amplifier.
first stage is the cathode-coupled amplifier V1 and the second a pentode amplifier V2.

The cathode-coupled amplifier has two inputs, one of which is normally held at the fixed zero signal level. If a sufficiently large negative voltage is applied to this reference input (pin 3) the circuit will not respond to a triggering waveform. Thus a convenient means is available for blocking the circuit. This type of amplifier offers a further advantage. Its inherent low impedances reduce the effects of shunting capacitance and thus increase its frequency response. This is desirable if the delay through the pulse amplifier is to be a minimum.

The pentode V2 triggers the adjacent blocking oscillator by a current pulse through the plate circuit of V3. Since this triggering operation is ideally carried out by a constant current generator, the large $r_p$ (in the neighbourhood of zero bias) of a pentode makes this tube preferable to a triode. In the quiescent state the grid of V2 is at ground level and the bias is fixed by the voltage drop across the cathode resistor $R_3$ resulting from a small d-c. current drawn through one of the transformer windings.

The operation of the circuit may be described as follows. Initially V3 is cut off by a -50 volt bias on its control grid. A positive trigger applied to the input is amplified by V1 then applied to the control grid of V2. V2 conducts rapidly and a current surge results in the plate winding of the transformer. This surge induces a positive voltage in the grid winding which is added to the grid bias.
When the grid cut-off voltage is reached $V_3$ starts to conduct and the plate current and grid voltage increase more and more rapidly. This continues until the gain around the plate-grid loop equals unity. Regeneration then occurs and the trigger is no longer needed to sustain the operation. As soon as the control grid becomes slightly positive with respect to the cathode (which is at ground potential) grid current starts to flow and the condenser $C_3$ between the cathode and grid-bias network is charged negatively. The voltage across $C_3$ must be subtracted from the voltage across the grid winding to give the actual grid driving voltage.

A temporary equilibrium is reached when the power dissipated in the grid circuit becomes equal to that supplied by the plate circuit. However, this state is terminated when the grid current becomes so large that the voltage across $C_3$ is changing more rapidly than the voltage supplied by the transformer. The grid then drops, plate current decreases, a further decrease in grid potential results and regeneration again occurs until the grid is driven beyond cutoff. When the tube cuts off, the plate voltage rises above the positive supply voltage as the transformer core remagnetizes. This gives rise to a positive overshoot of the output pulse. Before the blocking oscillator can be reactuated the charge on $C_3$ must be dissipated through the grid leak.

A Westinghouse $1/1/1$ transformer is used (Rad. Lab. No.—132AW2F). This transformer emits a very narrow pulse but requires a fast triggering waveform; consequently, the load to this circuit should offer low shunting capacitance.
between the plate output and ground. Notice that the plate winding consists of a series connection of two transformer windings. This arrangement steps down the voltage going to the grid thus providing a larger plate pulse.

The circuit was tested with a sawtooth waveform with a rising edge of 0.5 volts per microsecond and an amplitude of five volts. The output pulses had a 200 volt negative excursion and a 70 volt positive overshoot. The width of the negative portion was one microsecond. This pulse has a large peak power since a heavy plate current flows in V3 during this interval, thus a low resistive load can be driven without appreciably attenuating the pulse. The total delay through the circuit is about 3.5 microseconds, of which one microsecond occurs across the double triode V1.

A more complete description of blocking oscillators is given in Waveforms (13, p. 205).

Comparator

This circuit developed by P. Hildebrand for the multiplier (7, p. 27) is used in the coincidence circuitry. In Fig. 24 the pentode V2 is normally conducting (control bias is established by grid current through R2) and the diode V1 is non-conducting. When a negative sweep voltage applied at the input reaches equality with the reference voltage \(-E_r\) the diode conducts and a negative pulse is applied to the control grid of V2. The cathode current through this tube decreases and a negative voltage is induced in the input winding of the transformer. The diode then conducts more strongly,
Fig. 24. Multiar Comparator.

- $E_r$ in
- M Symbol
- out

- $V_1$ - 6AL5
- $V_2, V_3$ - 6AK5
- $C_1$ - 0.001 µf.
- $C_2$ - 0.1 µf.
- $C_3$ - 0.01 µf.
- $R_1$ - 100 K., 10%
- $R_2$ - 4.7 Meg., 10%
- $R_3$ - 33 K., 10%, 1 watt
- $R_4$ - 56 K., 10%, 1 watt
- $R_5$ - 33 K., 10%
- $R_6$ - 1 Meg., 10%
- Westinghouse 176AW2F or 134BW2F
regeneration occurs and V2 is rapidly cut off. When the charge on $C_1$ discharges through $R_2$, V2 conducts, the regenerative loop is again closed and another cycle occurs. Thus, a train of positive pulses are generated at the plate of V2. This train continues until the input sweep returns to a voltage level less negative than $E_r$. The second pentode V3 is used to invert the pulses appearing on the plate of V2.

The rise time of a pulse is approximately one microsecond, its width, two microseconds and its height, 230 volts.

**Blanking Phantastron**

Figure 25 illustrates the basic phantastron (14). Initially grid current from V3 is flowing through R and the grid is held at ground. Also, the suppressor of V2 is at -30 volts—a sufficiently negative bias on a 6AS6 to cut off plate current. Thus, the plate level of V2 is held at $E_2'$

![Figure 25: Basic Phantastron and its waveforms.](image-url)
and all cathode current except that passing through $R$ is going to the screen, which is at about 65 volts. Since both the plate and grid of $V_2$ are coupled through $C$, a negative trigger applied to the plate also reaches the grid. Immediately the screen current is sharply reduced and the resulting rise in screen potential is resistively coupled to the suppressor. The suppressor rises to six volts and is held at this level by the diode $V_3$. Plate current now flows; plate voltage drops about seven volts; and the diode $V_1$ is blocked. Meanwhile, the grid has settled to -10 volts, the bias required for the small current permitted by the plate resistor.

This initial step is followed by a Miller sweep generation (13, p. 195). A current $(E_1' + 10)/R$ flows through $C$ to the plate. Since the grid side of $C$ is held at -10 volts the plate side drops at a rate $(E_1' + 10)/RC$ volts per second. This process continues, the grid rising slightly to permit the plate to take the slightly increasing current needed by the plate resistor, until the plate voltage runs against the "knee" in the plate curve (bottoms). At about 15 volts a transfer of space current from the plate to the screen begins. This effect coupled with bottoming prevents any further drop in plate voltage; hence, the grid side of $C$ rises exponentially towards $E_1'$ until grid current flows. At this point screen current increases, the suppressor goes negative, and the circuit returns to its original state. The rate at which the plate returns to $E_2'$ is determined by the time constant $R_1C$ where $R_1$ is the plate resistor. The
Fig. 26. Blanking Phantastron.
diode V4 is not essential but it does prevent the suppressor from being carried so far positively that it may "stick" because of secondary electron emission.

For all practical purposes the plate rundown during the Miller sweep generation can be considered linear. Hence, the time $\delta t$ required for the plate to reach 15 volts is

$$
\delta t = \frac{(E_2' - 15)RC}{E_1' + 10} \text{ sec.}
$$

If $E_2 = E_2' - 15$ and $E_1 = E_1' + 10$ then

$$
\delta t = RC \frac{E_2}{E_1} \text{ sec.}
$$

Furthermore, if $E_2$ is a constant and $E_1$ is proportional to the velocity of the scanning disc then $\delta t$ is inversely proportional to $v$, as required.

In the detailed circuit (Fig. 26) $E_2$ is fixed at approximately 150 volts by the voltage divider circuit feeding the cathode follower V2a. The voltage $E_1$, proportional to $v$, is obtained from the holding circuit in Fig. 10 and applied to the grid of the cathode follower V1a. The arrangement of V1a and V1b increases the linearity of the output $E_1'$; for a change in the level of $E_1$ raises the plate of V1b by an equal amount with a negligible change in the current passing through both tubes. The operating points of V1a and V1b were chosen so that this current is one milliampere. The 12 K. resistor $R_{12}$ provides a ten volt variation between $E_1$ and $E_1'$, thus satisfying the requirement that $E_1 = E_1' + 10$. The cathode follower V2b is used to provide a low resistance recharging path for C. This results in a shorter recovery
Fig. 27. Precision Test of the Phantastron. Control voltage $E_1$ vs. blanking interval $\delta t$—calculated and measured.
time for the circuit.

The only square waveforms which can be used for blanking the pulse amplifier are those of the screen and suppressor; however, either waveform must be inverted before it is useful. The sharpest waveform—that of the suppressor—is inverted and amplified by \( V_5 \). The resistors associated with this tube provide a zero output (pin 3) during the quiescent state.

The resistance \( R \) is variable so that the blanking interval can be set for normal operation of the scanning disc. Any departure from normality is then compensated for by changes in \( E_1 \).

This circuit was tested by applying \( E_1 \), triggering the circuit repetetively, and measuring the duration of the suppressor waveform on an oscilloscope. This time was compared to the calculated time using equation (2). To avoid measuring \( R \) and \( E_2 \) it was assumed that the calculated and measured values of \( \delta t \) correspond when \( E_1 = 40 \) volts. Re-expressing equation (2),

\[
\delta t = \frac{\text{Constant}}{E_1}
\]

and on evaluating the constant using the data corresponding to \( E_1 = 40 \) volts

\[
\delta t = \frac{56}{E_1}.
\]

The measured and calculated values of \( \delta t \) for various values of \( E_1 \) are graphed in Fig. 27.
Testing the Timing and Coincidence Circuitry

The timing and coincidence circuitry assembly was tested independently of the function generator and multiplier. The pulse sequence P1, P3, P5, P1, etc., was supplied by a pulse generator at point D in Fig. 8. The period between pulses was one millisecond.

For reasons which become apparent after examining the waveforms in Fig. 28 pulse amplifier PA1 was permitted to generate only P5. This was accomplished by adjusting the variable resistor R in the blanking phantastron (Fig. 26) until the blanking pulse was somewhat greater than two milliseconds wide. Also, so that pulse P6 could be used as the marker pulse P0 it was necessary to adjust the resistor R3 in Fig. 10 to guarantee that P6 occurred roughly midway between P5 and P1. If the interval between pulses P6 and P1 is too small, flip-flop FF1 will have insufficient time to respond to both pulses. With these minor adjustments the whole operation was possible. The important waveforms are illustrated in Fig. 27 with emphasis on their orientation with respect to the input pulses.
Fig. 28. Test waveforms occurring in the timing and coincidence circuitry.
Remarks

The object of this thesis was to design and construct a number of elementary circuits which can be standardized for the whole computer. Their application in this paper has been limited to the timing and coincidence circuitry controlling the function generator and multiplier. No attempt has been made to conduct tests which would indicate the accuracy of the overall operation since such tests will have more meaning and will be more easily carried out when the calibration and function waveforms are available.

There will be a constant delay arising in the selection of the sampling point which is independent of the abscissa $x$. However, the resulting error can be compensated easily by biasing the input voltage $-K(b + x)$. The required bias can be determined by using the calibration frame as a function. The pulse pairs $(P_1, P_6)$ and $(P_1, P_8)$, which normally do not contribute to the overall operation, now are useful (refer to P. 18).

If the abscissa input voltage $-K(b + x)$ varies sinusoidally with small amplitude about a -25 volt mean, the output of the multiplier $E_F E_T/E_M$ will have a square waveform. Assuming $E_T$ is constant $E_F$ oscillates between 0 and $E_M$ as $(b + x)$ oscillates about the point $a$. Ideally, no time delays occur through the system and the amplitude of the positive and negative excursions about the point $a$ are equal. Consequently, the output waveform is 0 or $E_T$ for equal time intervals. The presence of a constant time delay through the system results in an average value of $(b + x)$ which is greater than the de-
sired value \( a \), and the output waveform has an amplitude \( E_r \) for an interval greater than half the period. If the time delay is sufficiently large the sampling point may never occur in a region where \( E_r = 0 \), and the output is constant.

It follows, then, that the effect of constant time delay can be eliminated by varying a voltage bias on the abscissa input until the output waveform, oscillating between 0 and \( E_r \), assumes either value for half the period.
References


Appendix

The Philbrick operational amplifiers are compact plug-in units primarily intended for feedback operations. They feature balanced differential inputs for versatility and minimum drift. Model K2-W embodies both high performance and economy of operation, whereas K2-X offers higher performance at the expense of greater power consumption. The latter amplifier is not intended to replace the K2-W, but serves for more demanding applications. Following are the general specifications for both models and their circuit diagrams.

Model K2-W Operational Amplifier

GAIN
15,000 DC, open-loop

POWER REQUIREMENTS
4.5 ma. at +300 VDC
4.5 ma. at -300 VDC
0.6 amp. at 6.3 V

INPUT IMPEDANCE
Above 100 Megohms

OUTPUT IMPEDANCE
Less than 1K open-loop, below 1 ohm
fully fed back

DRIFT RATE
5 millivolts per day, referred to the input

VOLTAGE RANGE
-50 to +50 VDC, at output and inputs

INPUT CURRENT
Less than 0.1 micro-amp for either input

OUTPUT CURRENT
-1 ma. to +1 ma., driving 50K load over full voltage range

INPUT BIAS
Positive input should operate 1.5 V high at balance—adjustable external bias required

RESPONSE
2 μsec. rise time with band width over 100 KC when used as an inverter

Model K2-X Operational Amplifier

GAIN
30,000 DC, open-loop

POWER REQUIREMENTS
7.5 ma. at +300 VDC
5.2 ma. at -300 VDC
0.75 amp. at 6.3 V

INPUT IMPEDANCE
Above 100 Megohms

OUTPUT IMPEDANCE
Below 300 ohms open-loop; less than 0.2 ohms fully fed back

DRIFT RATE
5 millivolts per day, referred to the input

VOLTAGE RANGE
-50 to +50 VDC for inputs (together)
-100 to +100 VDC for output (maximum)

INPUT CURRENT
Less than 0.1 micro-amp. for either input

OUTPUT CURRENT
-2 ma. to +2 ma., driving 25K load from -50 to +50 VDC

INPUT BIAS
Positive input should operate 0.6 V high at balance (external bias)

RESPONSE
1 μsec. rise time with band width over 250 KC when used as an inverter

AUGMENTED POWER
50K 1W resistor connected between output and -300 VDC supply. Drives 33K load over full voltage range.
Model K2-W Operational Amplifier.

George A. Philbrick Researches, Inc.
Model K2-X Operational Amplifier.

George A. Philbrick Researches, Inc.