CODING FOR SIGNALS WITH OCCASIONAL TRANSIENTS

by

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ABSTRACT

This investigation is concerned with improvements that can be made in communication systems to enable them to transmit efficiently signals containing occasional transients.

A method of improving delta modulation by the use of variable step size is discussed in detail and the design and construction of a suitable coder and step size control unit are described.

The results of tests made on the equipment constructed are given. From these results it is concluded that considerably better response to sudden large changes in input signal can be obtained with only slight deterioration in the performance under normal conditions of input signal. The method used to effect this improvement is applicable to more complex modulation schemes.

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1. INTRODUCTION

In the past few decades there has been a phenomenal increase in communication. Recently this growth has been particularly rapid in the digital field where messages are represented by discrete electrical impulses, as in data transmission and pulse code modulation.

To keep pace with the expansion in communication, new and better methods of sending information must be found. Much of the work now being done is concerned with increasing the number of messages that can be sent over existing systems. This includes such projects as speech bandwidth reduction and talk-spurt interpolation.

This thesis investigates a more efficient method of transmitting a particular type of signal; one which normally varies at modest rates but which occasionally has transients involving much higher rates of change. Such signals are found in many fields.

The following sections describe a method of using reduced accuracy for transients so that the information rate of the signal does not increase during sudden large changes. The desired characteristics of an efficient system are then listed. Delta modulation is examined as an example of a communication system where greater efficiency in transmission

of signals with occasional transients is desirable and possible.

The latter sections of the thesis describe the design and instrumentation of the modification to delta modulation, discuss the results of tests made on the new system, and present specific and general conclusions regarding an efficient method of transmission of this class of signal.

2. THEORETICAL CONSIDERATIONS

2.1 Information Rate and System Capacity

The capacity required in a communication system depends on the information rate of the message to be transmitted. The information rate of a continuous amplitude- and band-limited signal, in turn, depends on the bandwidth, W, since at least 2W samples per second are required to specify it. The rate also depends on the required accuracy in amplitude of the sample, on the probability of occurrence of each quantized amplitude, and on the amount of correlation in the signal.

If the signal is quantized into 2^n distinct amplitude levels, each level is equally likely, and there is no correlation, then n bits are required to specify each sample. The information rate, and hence the minimum system capacity for such a signal, is 2nW bits per second. This is the capacity of a standard PCM system sampling at the Nyquist rate.

Signals with this information rate are extremely rare. Either the probability of occurrence of some amplitude levels is lower than others or there is correlation among various parts of the signal. It is thus possible in most cases to reduce the capacity required in the communication system. To this end various schemes have been used and many others proposed.

Some of the most effective and practical of these schemes take advantage of the correlation among samples of the signal. In this method a prediction of the next sample value is made at both the transmitter and receiver. The prediction is based on past behaviour of the signal, the simplest type being a prediction that the next value will be the same as the previous value. One such system is differential PCM. This system quantizes, encodes and transmits the difference between the sample and a summation of previous quantized differences. The receiver then adds the quantized difference to the previous value to obtain the correct output.

2.2 "Generally Correlated" Signals

We have available then systems such as PCM which are efficient in transmitting uncorrelated signals, and systems such as differential PCM which are efficient in transmitting correlated signals.

There is a class of signals, however, which fits in neither category. These are signals which are correlated most of the time but in which occasional "surprises" or transients occur. An example is a video signal which normally changes slowly during a scan except at boundaries between light and dark objects where there are sudden large changes in light intensity. Examples can also be found in telemetering, where the measured quantity is normally

steady, or changes gradually, except during abnormal conditions such as switching or breakdowns.

If a "generally correlated" signal is applied to a system which is capable of transmitting an uncorrelated signal, the system will be operating inefficiently most of the time. If, on the other hand, it is applied to a system which is capable of transmitting only correlated signals, the information contained in the transient will be lost.

2.3 Reduction in Accuracy for Transients

The problem of providing a system which will allow transmission of the transients and which operates with a high average efficiency is a difficult one, particularly if the same amplitude accuracy is required for transients as for normal changes. Although methods can be devised to do this they are not too practical since complicated variable-delay networks are required at the transmitter and receiver. Fortunately there are many applications where a reduction in accuracy is tolerable during transients.

For example, in video transmission, advantage may be taken of the inability of the eye to detect the exact size of any discontinuity[1]. Or, as another example, in telemetering the transient signal will often be distorted in any case due to inertia in pick-up or read-out transducers or to other factors.

On this basis, more or less practical schemes for the efficient transmission of "generally correlated" signals are feasible. One such system proposed by R.E. Graham[2] is a modified differential PCM system. In this scheme the error in a predicted value is quantized using a non-linear quantizing staircase. This permits small errors to be transmitted more accurately than large errors. Other methods such as quantizing high frequencies more coarsely than low frequencies[1], and "slope companding"[3], are based on the same principle of reduced accuracy for portions of the signal containing high rates of change.

2.4 Desired System Characteristics

We will now consider a system which operated efficiently for correlated signals and assume that it has been modified for transmission of "generally correlated" signals.

If its capacity is not increased, the modification enabling it to transmit transients will result in reduced accuracy of transmission for some signals which would previously have been transmitted accurately. This is because a portion of its capacity to transmit correlated signals must be assigned to the transmission of transients.

The desired characteristics of the system are as follows:

1. The accuracy of transmission of correlated signals should be retained as closely as possible.
2. The response to transients should be as rapid as possible, preferably in the order of that imposed by bandwidth limitation (rise time about $0.35/W$).
3. The accuracy during transients should be sufficient to show the major features of the transient signal.
4. Normal accuracy should be restored as soon as possible after a transient.

2.5 "Generally Correlated" Signals in Delta Modulation

This project investigates the problem of providing efficient transmission of "generally correlated" signals. Because of the difficulty of evolving practical system designs from a general theoretical examination, a method of improving the efficiency of one particular system was devised. The system selected was delta modulation.

The development of this method, as well as providing a more efficient delta modulation scheme for signals of this type, permitted some general conclusions to be made regarding efficiency improvements in other systems for signals

with occasional transients.

The following sections contain a short description of the standard delta modulation system and its limitations. This is followed by a detailed examination of methods of increasing its efficiency for transmission of "generally correlated" signals.

3. DELTA MODULATION

3.1 Description

Delta modulation (DM) is a method of information transmission employing binary pulses. It differs from the well known pulse code modulation system in that a one-unit code is used instead of a multi-unit code group. This means that the transmitted pulse rate equals the sampling rate.

A simple DM system[4] is shown in Figure 3.1, and operates as follows.

The pulse generator in the coder produces a positive pulse if the error signal, $v_e(t)$, is positive, and an equal negative pulse if $v_e(t)$ is negative. The integrated value of these pulses, $v_o(t)$, is compared with the input signal, $v_i(t)$, to obtain $v_e(t)$. Pulses are produced in synchronism with the clock, with one positive or one negative pulse in every "time slot".

The integrator network in the decoder is identical to the integrator network in the feedback loop of the coder. Thus the decoder output signal is also $v_o(t)$, and is a stepwise reproduction of the input signal. An examination of typical waveforms (Figure 3.2) shows that the input signal has been quantized in both time and amplitude. The integrating network in the decoder is usually followed by a low-pass filter to remove high-frequency components of $v_o(t)$ introduced by the quantizing process.

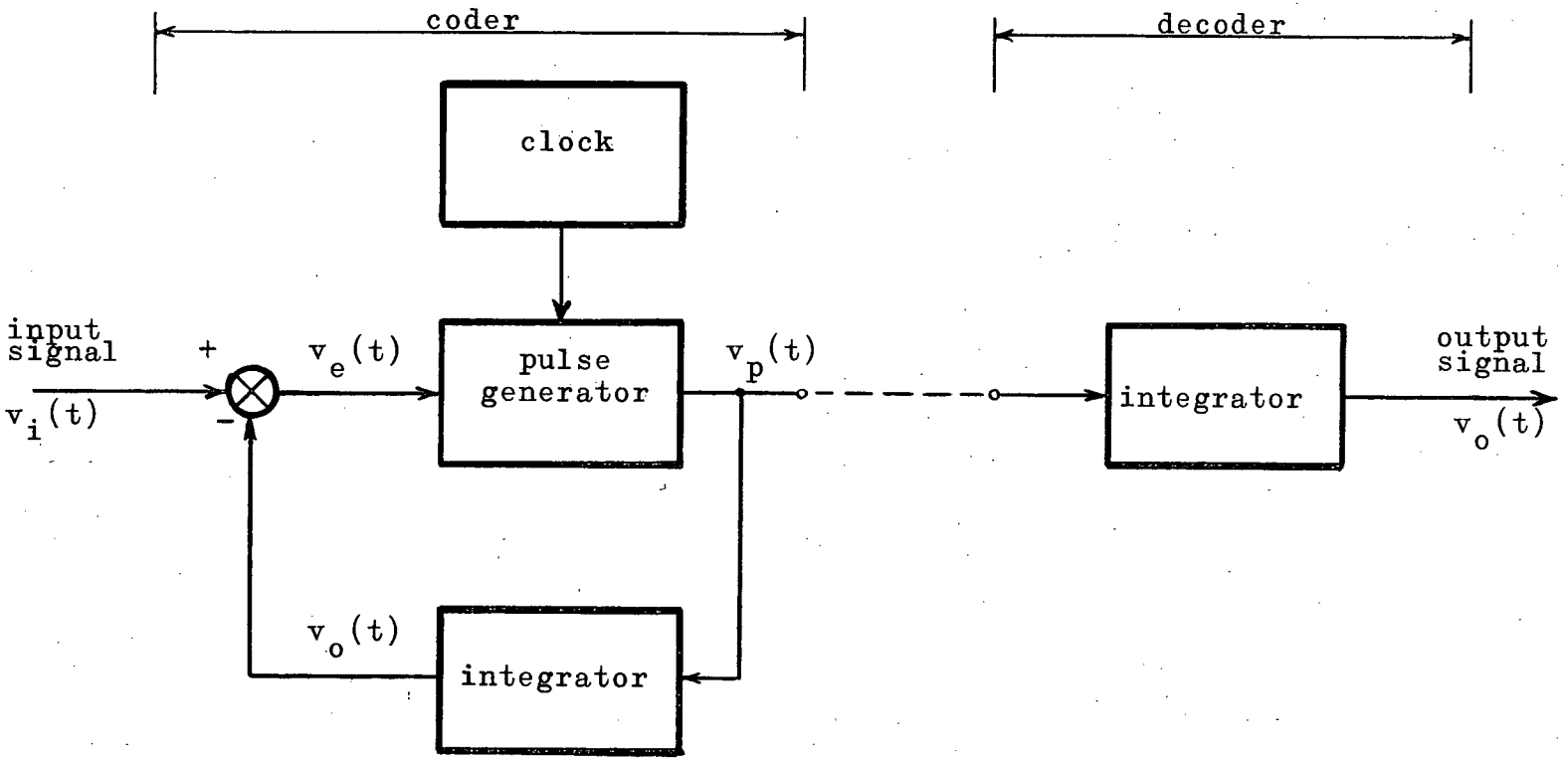


Figure 3.1 Simple Delta Modulation System

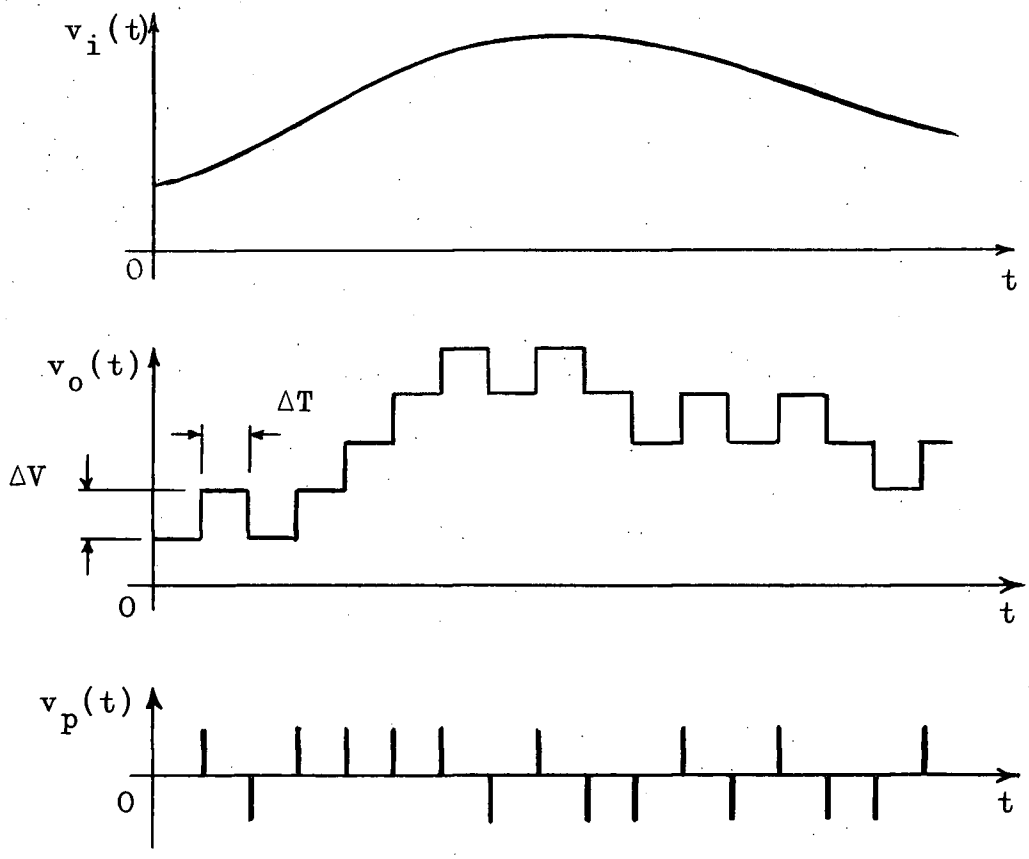


Figure 3.2 Typical Waveforms - Simple DM System

3.2 Overload Characteristics

Overloading occurs in delta modulation when the rate of change of input signal with respect to time exceeds a certain limit. When this happens the integrator voltage is not able to follow, causing the output to be distorted.

The maximum slope (slope-limit) is given by

$$\alpha = \frac{\Delta V}{\Delta T}$$

where ΔV is the height of each step,

$\Delta T = \frac{1}{f_s}$ is the sampling interval,

f_s is the pulse rate.

3.3. Quantizing Noise

In all binary pulse systems, the signal is distorted by being allowed to vary only in discrete steps. This distortion is called quantizing noise.

A special case of quantizing noise is called the threshold effect. This occurs when the amplitude of the input signal is less than one-half step. The coder then transmits a regular pulse pattern (+ - + - + -) and no output is obtained from the decoder.

3.4 Integrator Waveform

In the DM system of Figure 3.1 the integrator employed may be a long-time-constant RC circuit which gives a close approximation of a step output for an input pulse of large amplitude and short duration. Thus positive steps are produced by a positive pulse and negative steps by a negative pulse.

In most communication channels, however, it is simpler to transmit binary pulses as either pulse or no-pulse corresponding to a 1 or a 0, instead of a positive pulse and a negative pulse. In the coder and decoder the

1 and 0 pulses are then converted into short positive and negative pulses to give a step waveform at the integrator. Alternatively, a positive step at the integrator can be produced by using a double-size pulse followed by a linear decay and a negative step by using the decay only[3,5,6].

Yet another possibility is to use positive and negative pulses whose duration is equal to the sampling interval, which results in a ramp waveform at the integrator. This latter method was used in the system constructed.

3.5 Transmission of DC Signals

In many applications the transmission of dc input signals is a requirement, and so a brief review of the method of dc transmission in DM follows.

Delta modulation in its simplest form can transmit dc levels but the transmitted pulse pattern is the same for any level, that is, a pattern consisting of alternate 1 and 0 pulses. A change in dc level is transmitted by altering this ratio of 1 and 0 pulses, but when the new dc level is reached, the pattern again becomes regular. A difficulty is encountered in this method however, since, in the case of an error in transmission the effect of the error is present in the output indefinitely, that is, errors are cumulative.

A method of overcoming this difficulty, called "exponential delta modulation," was investigated by J. Holzer [5]. It consists of the use of a finite-time-constant integrator in the coder feedback loop and in the decoder, instead of a perfect (infinite-time-constant) integrator. The result is a different pulse pattern for every separate dc level of input signal and thus an error in transmission will have a measurable effect on the decoder output for a finite time only.

The use of a finite-time-constant integrator, as well as being more practical, places a definite limit on the amplitude of input signal that can be handled. In a typical arrangement with the capacitor-shunting resistor connected to the mid-point of the integrator voltage range, this limit is reached when a signal of such level as to cause transmission of all pulses or all spaces is applied to the input.

Furthermore, the slope limit of an exponential DM system now depends on the dc voltage level at the integrator and on the direction of change of the input signal. Because of this it is desirable to limit the integrator amplitude range over which the system normally operates so that the slope limit remains finite. For example, if the ratio of slope limit at zero level to that at maximum amplitude, V_m, is taken as 2, then

the corresponding pulse pattern for a dc signal of maximum amplitude is

1 1 1 0 1 1 1 0 1 1 1 0

For, if the pattern becomes

1 1 1 1 1 1 1 1 1 1 1 1

then, at the integrator, a negative step is replacedby a positive step at every fourth pulse, and the voltage will increase at a rate of 2 steps in 4 pulses, which is a slope of $\frac{\alpha}{2}$.

The integrator time constant, λ, corresponding to this condition is found as follows:

$$i_R = \frac{V_m}{R} = \frac{\frac{n}{2}\Delta V}{R}$$

$$= C \frac{dv_o}{dt}$$

where C is the integrator capacitance,

R is the integrator shunting resistance,

n is the total number of steps in the integrator amplitude range

i_R is the current in R

Hence

$$\frac{dv_o}{dt} = \frac{n\Delta V}{2RC} = \frac{n\Delta V}{2\lambda}$$

But for a ratio of 2:1 in slope

$$\left(\frac{dv_o}{dt}\right)_{V_m} = \frac{\alpha}{2}$$

$$\therefore \frac{\alpha}{2} = \frac{n\Delta V}{2\lambda}$$

$$\lambda = \frac{n\Delta V}{\alpha}$$

and since $\alpha = \frac{\Delta V}{\Delta T}$

$$\lambda = n\Delta T$$

The standard DM system, because of its inherent slope limitation is unsuitable for transmission of signals with occasional transients. In the following sections a method of overcoming this limitation is developed. This method, because it uses a change in slope, has been called "accelerated delta modulation."

In developing the fundamental aspects of this method the use of a perfect integrator in the coder feedback loop is assumed. The effect of using a finite-time-constant RC circuit as integrator to allow transmission of dc signals is then considered.

4. ACCELERATED DELTA MODULATION

4.1 Basic Requirements

As indicated in Section 3.2 the maximum rate of change of a DM system is dependent on the size of each step and on the pulse rate. One way of improving the response is to increase the pulse rate, but this of course, means a greater transmission bandwidth is required. Another way is to increase the size of each step, that is, use coarser quantization, but this has the disadvantage of increasing the quantizing noise for all input signals.

It should be possible, however, to use a larger step size only when sudden large changes occur in the input signal and the normal step size at all other times[6]. By this means the original accuracy would be retained for small changes in input signal but a closer representation of transients would be obtained. Because of the increased step size it is likely that an overshoot will occur. The time required for the accuracy to be restored after a transient will depend on the amount of this overshoot.

A basic system of accelerated delta modulation (ADM) for obtaining the required characteristics is shown in Figure 4.1.

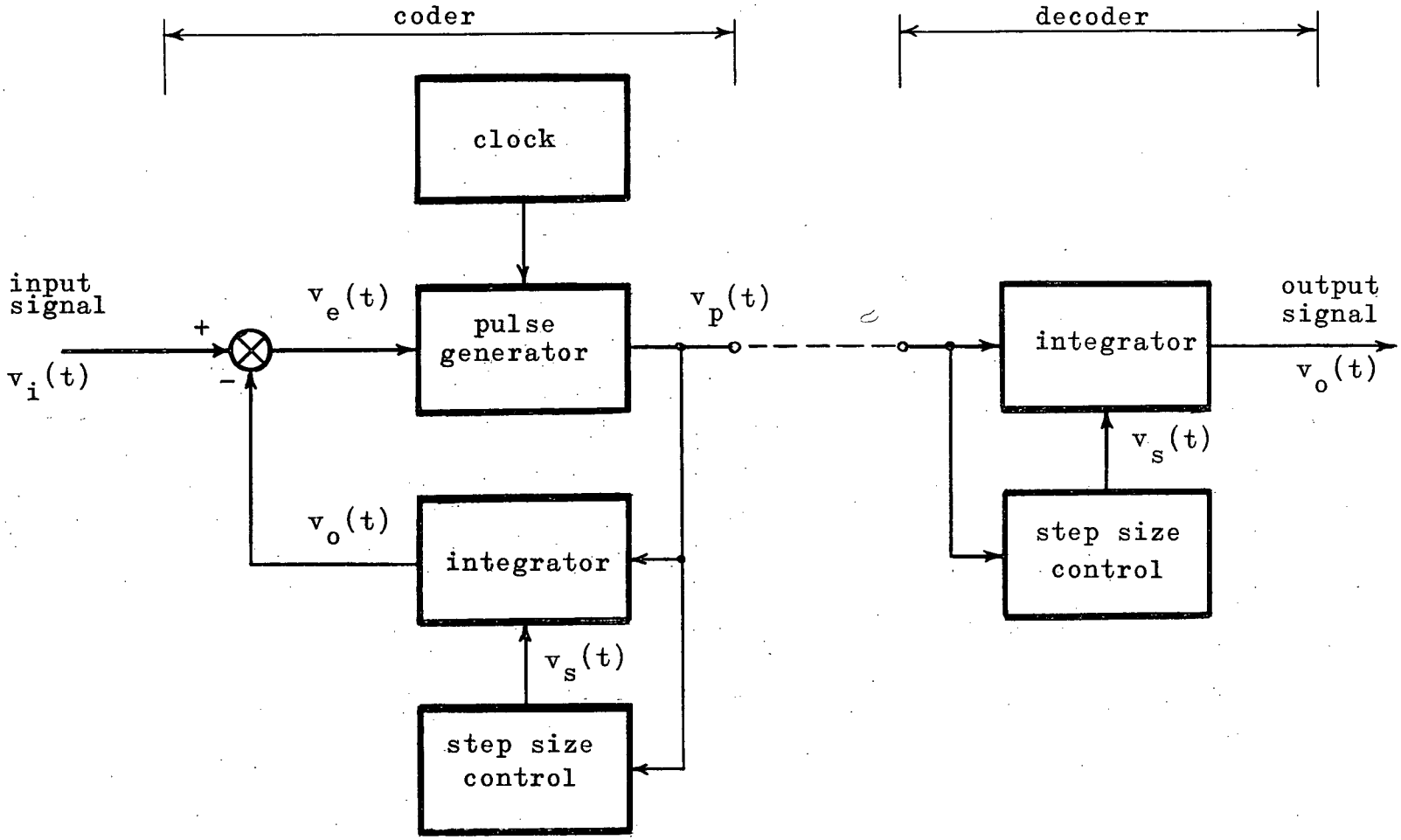


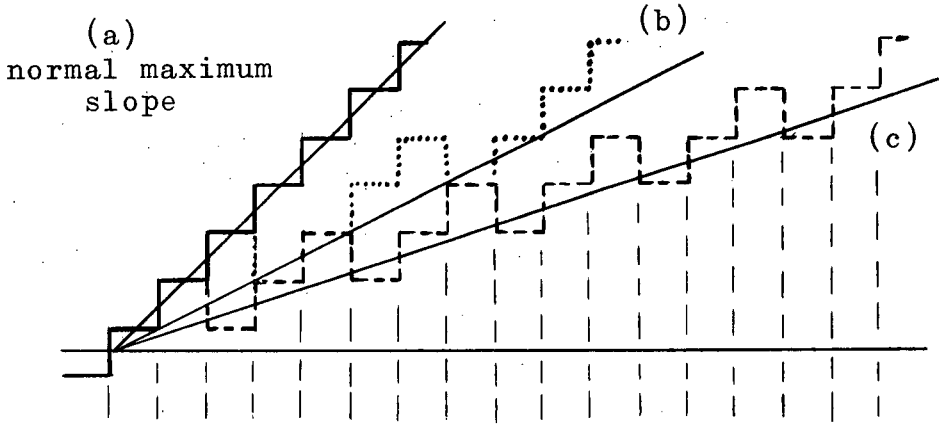
Figure 4.1 Accelerated Delta Modulation System

4.2 Coding for Step Size Increase

The decision to change step size must be derived from either the integrator voltage, $v_o(t)$ or, as shown in Figure 4.1, from the transmitted pulses, $v_p(t)$. That is, assuming no other communication path between transmitter and receiver, this information must be contained within the transmitted pulse train and derived from it by the receiver.

Since in DM only two different signals are transmitted, a 1 or a 0, the information regarding step size must be a certain sequence of pulses which will be called the "acceleration signal." The pulses constituting this acceleration signal will, however, still retain their DM significance, a 1 producing a positive step and a 0 producing a negative step. In delta modulation when slope overload occurs, the coder transmits either all 1's or all 0's. Therefore, the acceleration signal will be made up of a certain number of pulses, all of the same type.

If a large number of pulses are used as the accelerating signal, there will be a long delay before the output overtakes the input. On the other hand, if the acceleration takes place after only a few steps in the same direction, quantizing noise will be increased for relatively small rates of change of input signal.



(a) slope = α 1 1 1 1 1 1 1

(b) slope = $\frac{\alpha}{2}$ 1 1 1 0 1 1 1 0 1 1 1

(c) slope = $\frac{\alpha}{3}$ 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1

Figure 4.2 Slope of $v_o(t)$ for Various Pulse Patterns

This is illustrated in Figure 4.2 where the output signal slope corresponding to various pulse patterns is shown. These slopes are expressed in terms of α, the maximum slope in a normal DM system.

From pattern 4.2(c) it can be seen that if the decision to accelerate were based on two succeeding pulses being the same, acceleration would occur for any change in input signal (of sufficient duration) with a slope exceeding $\frac{\alpha}{3}$. As a consequence the quantizing

noise would increase for input signals with slopes between $\frac{\alpha}{3}$ and α.

If, however, instead of two successive pulses, three were chosen, acceleration would occur for any input signal having slopes exceeding $\frac{\alpha}{2}$ (curve (b), Figure 4.2). Quantizing noise in this case would be increased for input signals with slopes between $\frac{\alpha}{2}$ and α.

As the best compromise between delay and quantizing noise, this latter sequence was chosen as the accelerating signal. That is, whenever three pulses of the same type occur in sequence, the fourth step will be larger if the fourth pulse is also of the same type.

Unless $v_o(t)$ has reached $v_i(t)$ after the fourth pulse, the fifth and succeeding steps should also be larger than normal until a pulse of the opposite type appears when the steps will, in some fashion, return to normal size.

The time delay occurring after a sudden jump of $v_i(t)$ before the first step of increased size, will depend on the particular condition of the coder at the time of the jump. If the jump occurs almost ΔT seconds after a step in the same direction, the delay will be $2\Delta T$ seconds. If the jump occurs just after a step in the opposite direction the delay will be $4\Delta T$ seconds. Discussions in the following sections are based on a mean delay of $3\Delta T$ seconds.

4.3 Rate of Step Size Increase

Having now established a method of initiating the step size increase, the next step is to investigate the various possible rules governing the amount of increase. It is now necessary to compromise between (1), a small increase in step size and consequently further delay in response if the change in $v_i(t)$ is large, and (2), a large increase in step size and hence potentially greater quantizing noise. By using a variable size increase, however, it is possible to minimize both disadvantages. Thus for the fourth pulse a small increase in size would be made, for the fifth a larger increase, and so on. In this way the decrease in accuracy is a function of the change in $v_i(t)$.

This variable increase can be made in a number of ways, two of which are shown in Figure 4.3, where step size and resulting output voltage are plotted against time for a step input occurring at $t = 0$.

For normal DM (no acceleration) the step size is constant, and $v_o(t)$ increases with slope α.

In Figure 4.3(b) the size of step increases as a linear function of time after the acceleration signal. Here, the condition that the step size increase be small at first is met, but there would still be considerable delay in matching $v_o(t)$ to $v_i(t)$ if the jump in $v_i(t)$ were large.

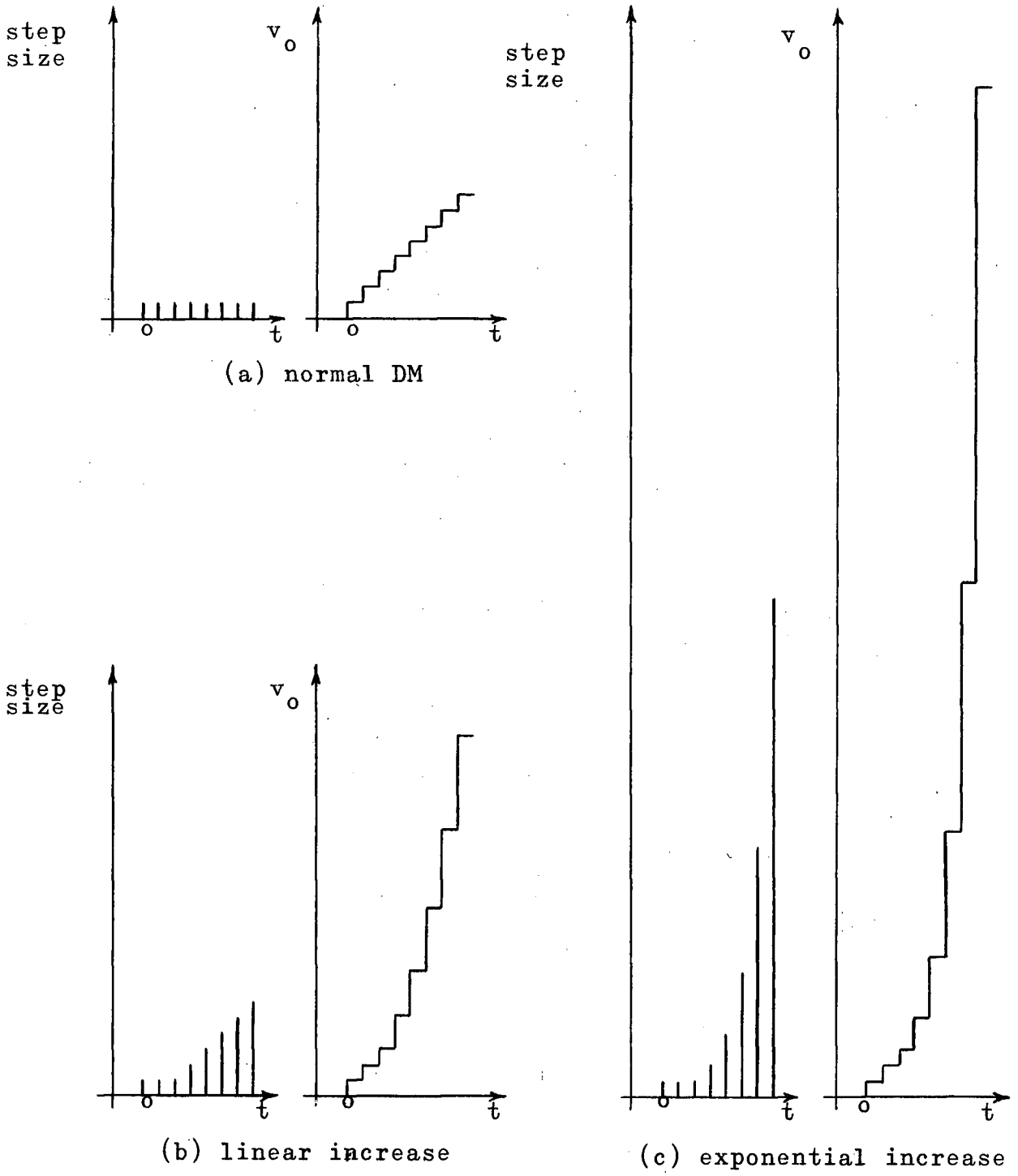


Figure 4.3 Various Acceleration Methods

Figure 4.3 (c) shows a method whereby the step size increases at an exponential rate, doubling for each successive pulse after the accelerating signal.

There is no firm criterion which permits the selection of one method of step size increase over another in a general system. In a particular application the speed of response of input and output devices could be used as the basis for the choice. For the present study the very fast action of the exponential increase in step size outweighs the disadvantages of the rather large overshoot. For this reason the exponential increase will be used as illustration in the following sections.

4.4 Maximum Step Size

The maximum desirable step size is related to the number of steps covering the amplitude range of the system. For example, in an exponentially accelerated system where the range of amplitude is covered in 100 normal size steps, the maximum size step that could be used is $64\Delta V$. That is, if a jump in input from minimum to maximum amplitude occurred, the steps would have the following sizes in terms of ΔV

1, 1, 1, 2, 4, 8, 16, 32, 64

giving a total change in output of $129\Delta V$ of which $29\Delta V$ is overshoot.

The amount of overshoot could be reduced appreciably though, for changes in input ranging from 66ΔV to 97ΔV by making the maximum step size 32ΔV. This would mean of course that for a full scale jump, one more pulse period would be required than previously. The step sizes would be, again in terms of ΔV

1, 1, 1, 2, 4, 8, 16, 32, 32, 32

The likelihood of jumps in input of 97ΔV to 100ΔV in an operating system is quite remote and so, for the 100 step system, a maximum step size of 32ΔV is better than 64ΔV.

Since a maximum of 9 steps is required after a jump in input the time for any single jump would never exceed 9ΔT. This figure includes 3ΔT for the acceleration signal and 6ΔT for the accelerating time.

By similar reasoning it can be shown that the maximum step size for a linearly-accelerated system should not exceed 13ΔV and that the time required for a full-scale jump is 15ΔT.

4.5 Coding for Step Size Decrease

The sequence of pulses used to indicate that $v_i(t)$ has been exceeded can be extremely simple. In fact, the first pulse of opposite sense will indicate that the integrator voltage has exceeded the input voltage and that the next step, which will be in the opposite direction, should

be reduced in size.

The various rates at which the size of the step can be reduced are as numerous as for acceleration. The requirement is, of course, that the correct value of output signal be approached as quickly as possible, but because of the large quantizing interval corresponding to the increased step size it is necessary to hunt for this correct value.

The procedure is complicated by the admission of other sudden changes in $v_i(t)$ occurring a short time after the initial jump. Indeed the possibility of such behaviour is to be expected in many telemetering applications where a disturbance may contain many transients.

Thus if a jump in $v_i(t)$ is followed a few pulse periods later by another jump in either the same or opposite direction, the system must accelerate to follow the second jump with a minimum delay. To accomplish this the same accelerating signal can be used as before, that is, three steps occurring in the same direction during deceleration will indicate that $v_i(t)$ has again changed and that step size should again be increased.

4.6 Rate of Step Size Decrease

One extreme of step size reduction would be to revert immediately to a normal interpretation of the code, which would mean a small recovery time if the overshoot

were small, but a large recovery time and quite possibly instability if the overshoot were large. The other extreme would be to decrease step size by a small amount each period, but this would again result in a large recovery time.

The optimum rate, assuming equal probability for the correct value to lie within any quantum ΔV in the final step before deceleration, is an exponential decrease in which the size of step is halved for each succeeding pulse.

Deceleration at this rate means that for a maximum step size of $32\Delta V$ the integrator voltage arrives to within $\frac{1}{2}\Delta V$ of the correct value of $v_o(t)$ after 5 steps unless 4 of these steps are successively in the same direction, in which case it will take 6 steps. This gives a stable system since any oscillations about the correct value of $v_o(t)$ are quickly damped out.

Figure 4.4 shows some examples of the response of the ADM system to a step-input signal. These examples illustrate the three-step acceleration signal and exponential step size increase and decrease characteristics.

4.7 Transmission of DC Signals in ADM

Use of a finite-time-constant integrator as described in Section 3.5 will permit the system to transmit dc signals. For such a system the slope limit depends upon the dc level, and hence there is no unique slope beyond which acceleration is desirable. It is possible,

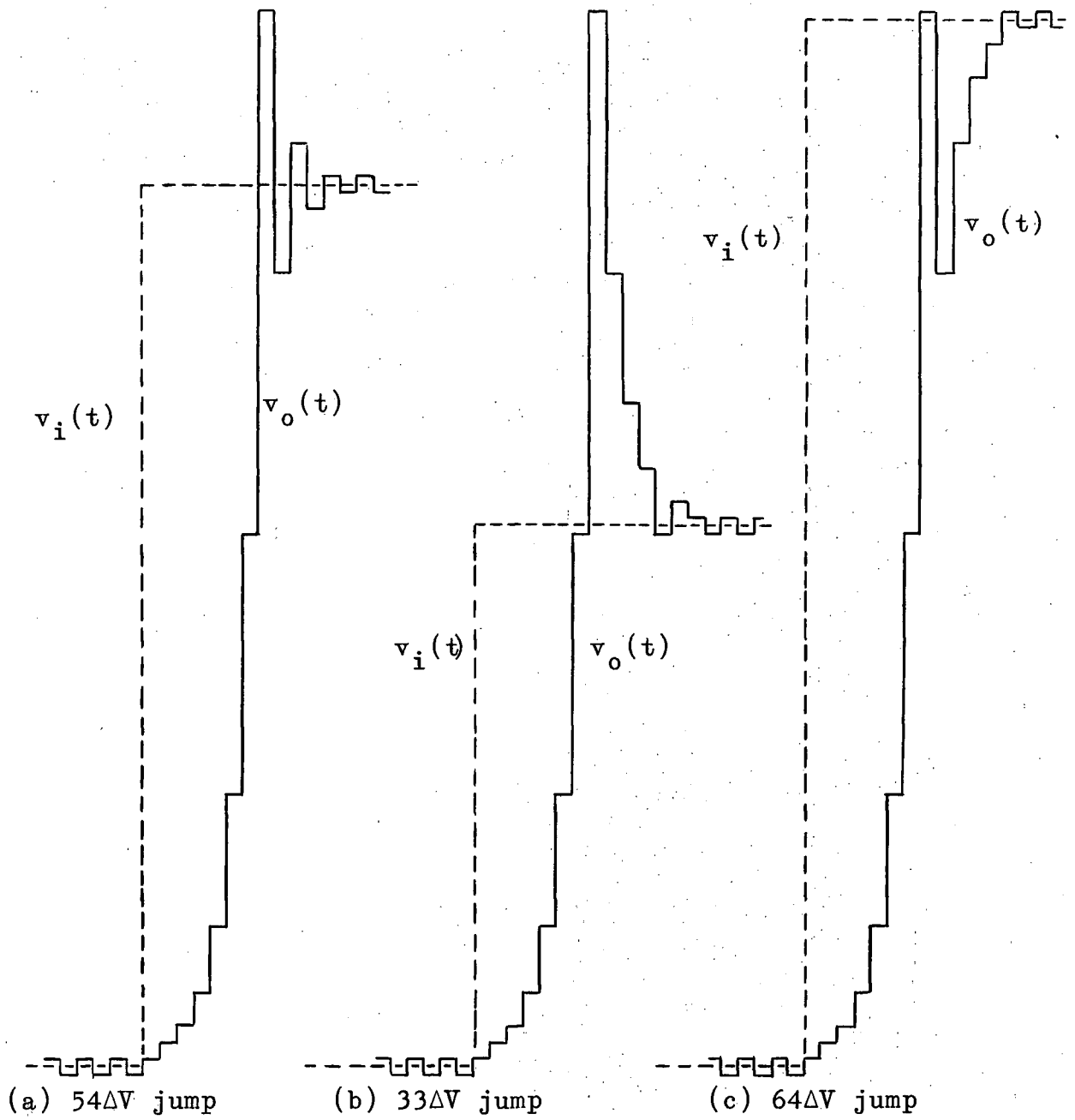


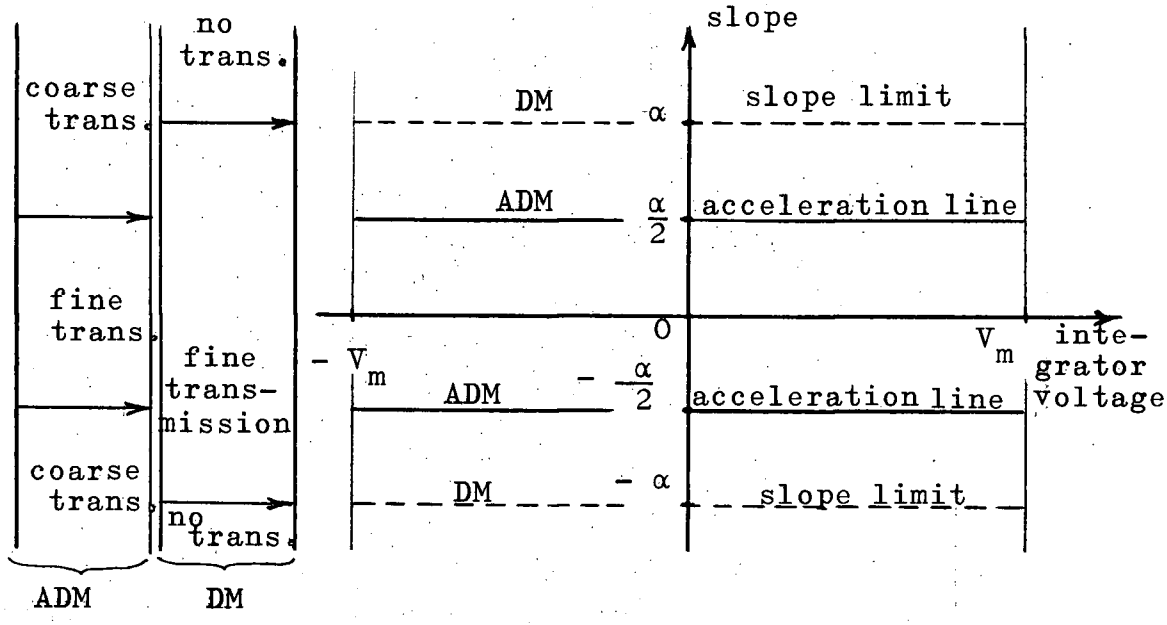
Figure 4.4 Typical Response -ADM

however, to define two "acceleration lines", as shown in Figure 4.5. Below the upper acceleration line, input signals with prolonged positive slopes will not cause acceleration, and above it they will cause acceleration.

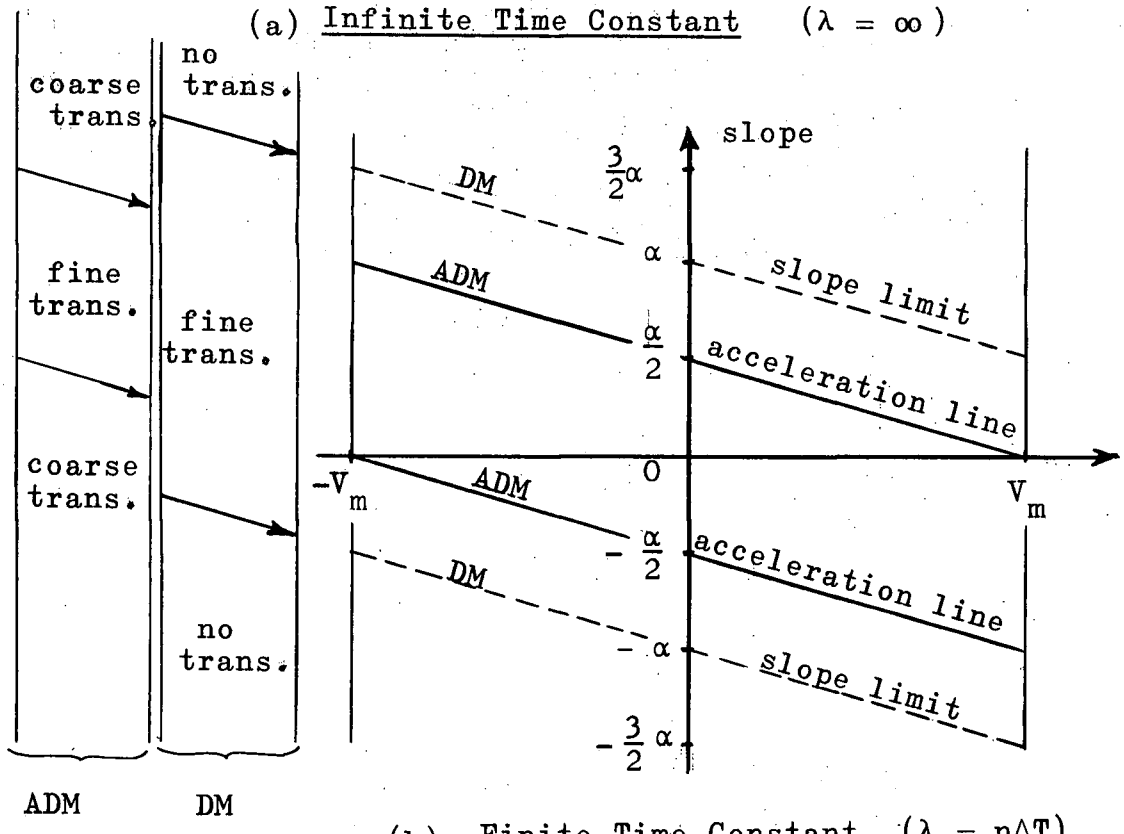
In Figure 4.5(a) the DM slope limit and ADM acceleration line are plotted as functions of integrator voltage for an infinite-time-constant integrator. In this case the acceleration line is horizontal at $\frac{\alpha}{2}$. For a finite-time-constant integrator using the same acceleration signal, the acceleration line can be found by subtracting $\frac{\alpha}{2}$ from the DM slope limit for a particular integrator time constant. Figure 4.5 (b) shows the characteristic for an integrator with a time constant $n\Delta T$.

A time constant of $n\Delta T$ as derived in Section 3.5, corresponds to the DM slope limit at zero dc level being twice the DM slope limit at maximum dc level. As shown, the acceleration line approaches zero as V_m is reached. This also follows from an examination of the pulse pattern for a dc signal of V_m. For this voltage, the code 1 1 1 0 1 1 1 0 is continuously transmitted, and thus for any increase in $v_i(t)$ when it is close to V_m an increase in step size will occur. If all dc levels are to be transmitted without acceleration, then the integrator time constant ,λ, cannot be less than $n\Delta T$.

On the other hand, a value of λ of more than $n\Delta T$



(a) Infinite Time Constant ($\lambda = \infty$)



(b) Finite Time Constant ($\lambda = n\Delta T$)

Figure 4.5 Integrator Characteristics

would mean that dc accuracy would be more difficult to maintain in the case of both errors in transmission and drifts in the coder and decoder circuitry. Therefore a value of λ of $n\Delta T$ was chosen.

5. SYSTEM DESIGN

5.1 Design Method and Requirements

In deciding the desirable characteristics of the ADM system, its properties in response to a large step-voltage input were considered. It was also required (Section 4.2) that for input signals with slopes less than the acceleration line, the system act in an identical manner to a normal delta modulation system. Between these two extremes lies an area in which the properties of ADM had to be investigated.

Of special interest is the region between the acceleration line and the DM slope limit, where an increase in noise was expected in ADM when compared with delta modulation. A study was also required of the behaviour of ADM in response to many types of input signals, including those with continually changing slopes such as sine waves, and signals which might cause instability or large amounts of distortion such as pulses of short duration.

There are two methods of ascertaining the performance of a complex modulation process; by instrumentation and by computer simulation. In the former method great care must be taken lest spurious noise and distortion in the apparatus lead to misinterpretation of the results. However, instrumentation yields some valuable knowledge of the problems involved in construction of an operating system

and of the complexity of the apparatus required. This is an important consideration in the present case, since the chief merit of delta modulation as compared to pulse code modulation is simplicity in coder and decoder construction.

Computer simulation has the advantage of yielding the required performance characteristics free from the vagaries of a particular instrumentation method and often more quickly, but for the above reasons it was decided to use the instrumentation method.

Equipment was constructed with a particular application in mind; that of a low-speed telemetering channel, with the following characteristics:

pulse rate: $f_s = 20$ pps

total amplitude range: 4 volts

amplitude quantizing accuracy: $\pm$ 0.5%

From these requirements the system parameters are found as follows:

total number of steps in amplitude range:

$$n = \tfrac{1}{2}\left(\frac{1}{0.5\%}\right) = 100$$

normal step size: $\Delta V = \dfrac{4 \text{ volts}}{100} = 40$ mv

sampling interval: $\Delta T = \dfrac{1}{20 \text{ pps}} = 50$ msec

DM slope limit at mid-range dc input signal:

$$\alpha = \frac{40 \text{ mv}}{50 \text{ msec}} = 0.8 \text{ volts/sec}$$

ADM acceleration line at mid-range dc input signal:

$$\frac{\alpha}{2} = 0.4 \text{ volts/sec}$$

integrator time constant: $\lambda = n\Delta T$

$= 100 \times 50 \text{ msec} = 5 \text{ sec}$

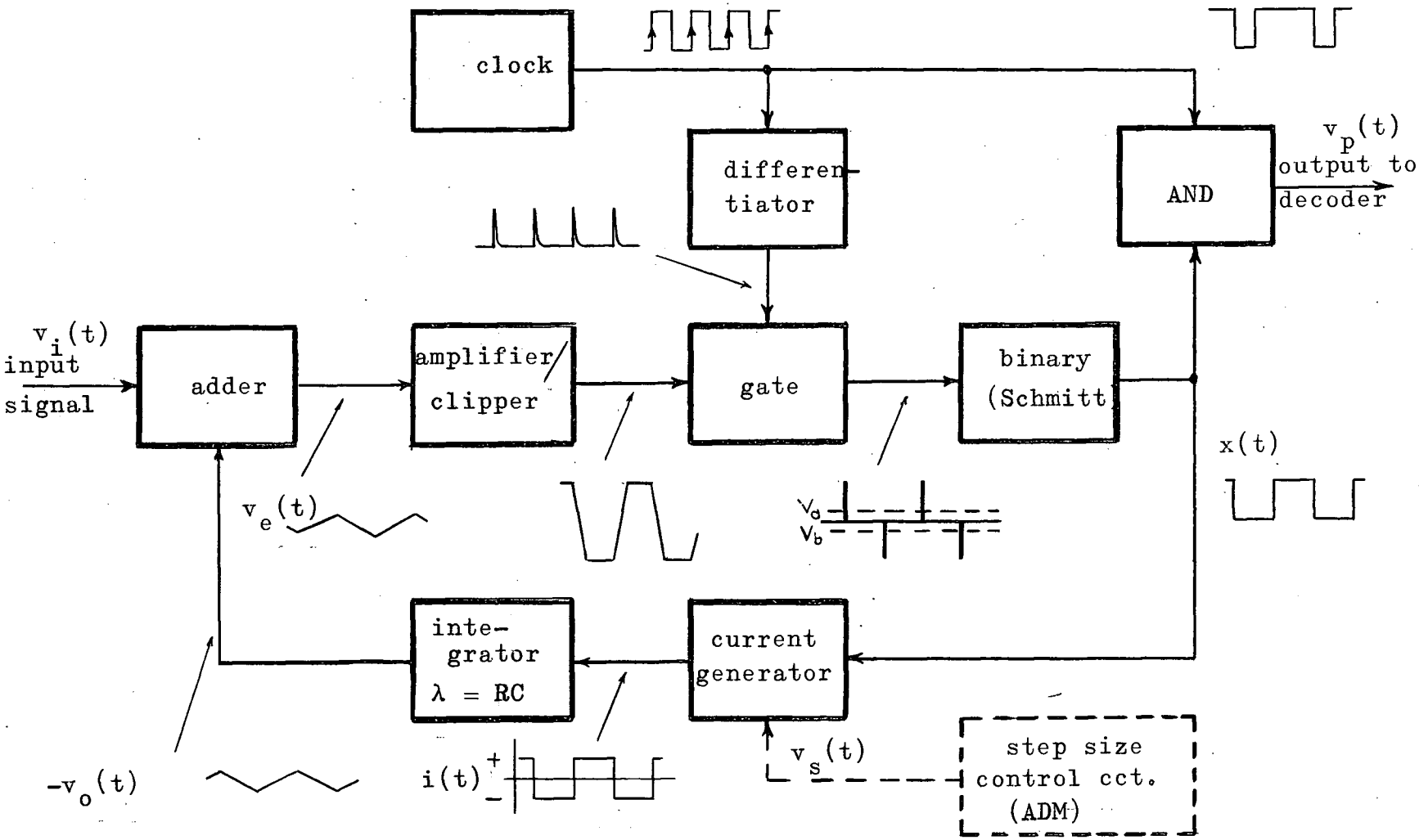
max. step size: $32\Delta V = 32 \times 40 \text{ mv} = 1.28 \text{ volts}$

5.2 DM Coder

In order to compare the various characteristics of DM and ADM, a coder and a separate step size control unit were built. By disabling the step size control unit the equipment could be operated as a normal DM system. Since the feedback voltage, $-v_o(t)$ is the same as the decoder output voltage it was not necessary to construct a decoder for tests of system response.

A block diagram of the coder is shown in Figure 5.1 along with the waveforms at various points in the circuit corresponding to a mid-range dc input signal. The operation is quite straightforward, however a few explanatory notes are given below. A complete circuit diagram and a detailed description of the important parts of the circuit are given in the Appendix.

Referring to Figure 5.1 an input signal, $v_i(t)$, is added to the feedback voltage, $-v_o(t)$. Since the latter is an inverted and quantized reproduction of the input signal the sum of the two voltages tends to be a constant value. A deviation from this constant value



Note: Waveforms shown correspond to mid-range dc input signal.

Figure 5.1 Delta Modulation Coder — Block Diagram.

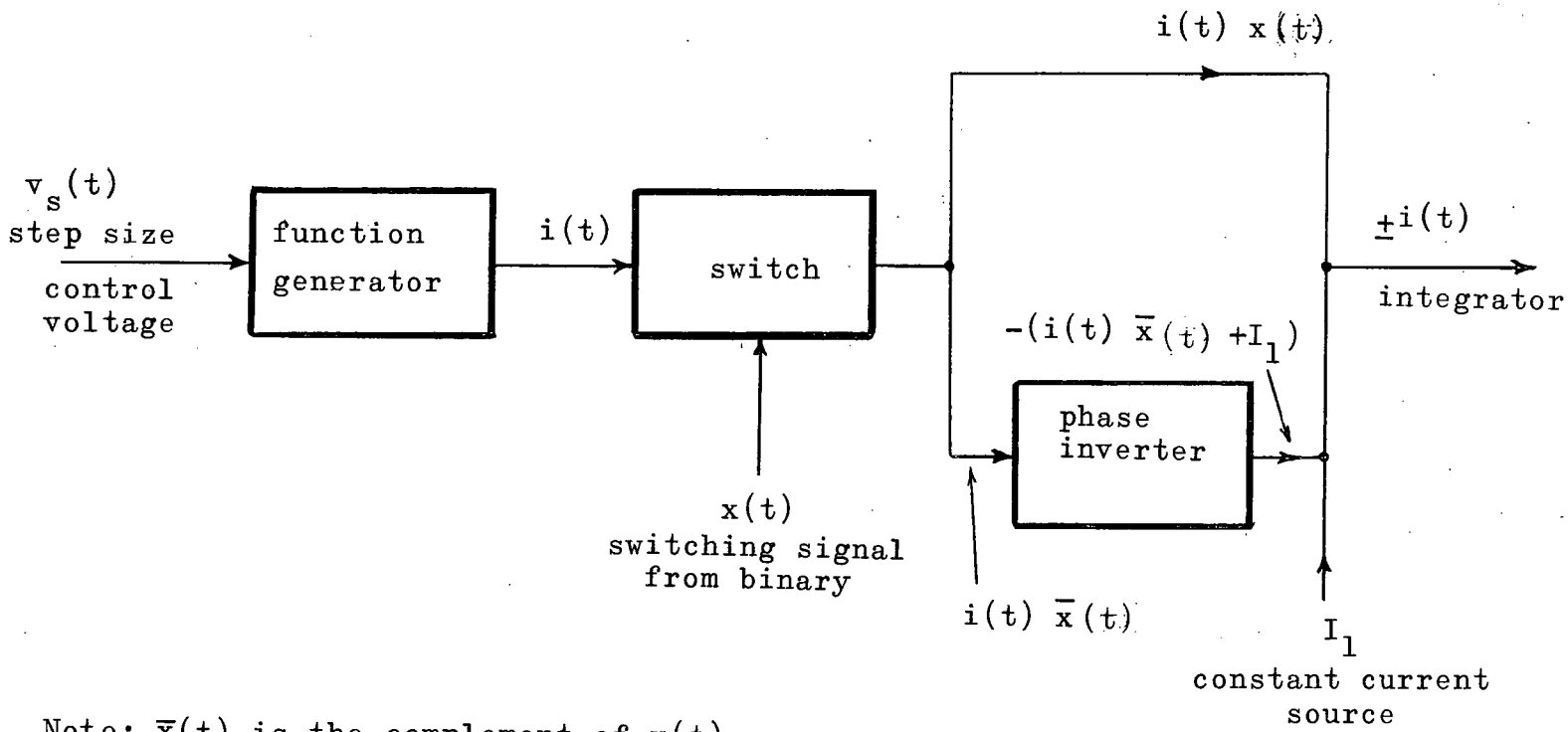
yields an error signal which is amplified and clipped and then sampled by the gate at regular intervals. These short samples switch the binary to state 2 if they are above V_a or to state 1 if they are below V_b.

The coder output pulses from the AND circuit are produced by coincidence of the clock and binary signals. Thus no pulses are transmitted while the binary is in state 1 and pulses are transmitted while it is in state 2.

The integrator is a storage circuit with time constant λ, whose voltage, $-v_o(t)$, is varied by the current generator which supplies positive current for binary state 1 and negative current for binary state 2. The feedback voltage, $-v_o(t)$, is thus always either increasing or decreasing.

5.2.1 Current Generator

A more detailed diagram of the portion of the circuit shown simply as current generator in Figure 5.1 is shown in Figure 5.2. The voltage, $v_s(t)$, from the step size control circuit varies linearly with respect to time during periods of step size increase and periods of step size decrease. The function generator, included as part of the current generator, produces a current which is an exponential function of $v_s(t)$.



Note: $\bar{x}(t)$ is the complement of x(t)

Figure 5.2 Coder Current Generator

The signal x(t) from the binary circuit switches i(t) either directly to the integrator or through a phase inverter which produces -i(t). The inverter is operated with a constant output current of $-I_1$ so that changes in its output are directly proportional to changes in its input. This current is balanced by a current of $+I_1$ from a separate source.

5.3 Step Size Control Circuit

Two different schemes were investigated for obtaining the step size control signal, $v_s(t)$. These were: a digital control circuit and an analogue control circuit. Since the digital control circuit was found to be the better of the two, it is described in detail in Section 5.3.1. A brief description of the other scheme is given in Section 5.3.2.

5.3.1 Digital Control Circuit

The step size control circuit is required to produce an output voltage, $v_s(t)$ as shown in Figure 5.3. For normal step size at the integrator, $v_s(t)$ is a dc voltage, V_o. If three steps in sequence are in the same direction, $v_s(t)$ must increase linearly with respect to time with a slope of

$$\frac{dv_s}{dt} = \frac{V_s}{4\Delta T}$$

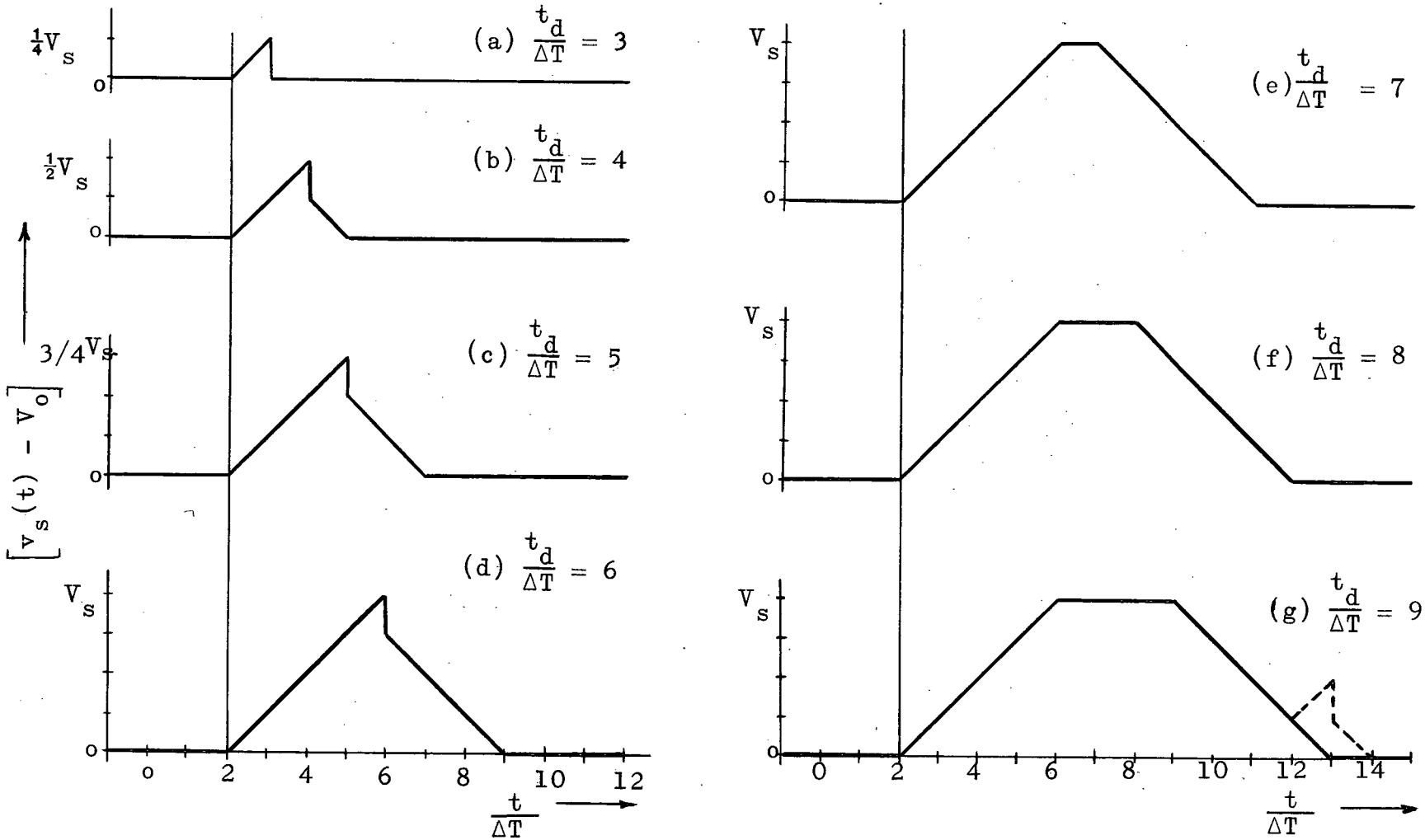


Figure 5.3 Step Size Control Voltage

(for acceleration signal at $t = 2\Delta T$ and deceleration signal at $t = t_d$)

The increase must continue until either the maximum voltage ($V_o + V_s$) corresponding to a step size of $32\Delta V$ is reached, or the deceleration signal is given, in which case $v_s(t)$ must immediately drop by an amount

$$\frac{V_s}{4\Delta T} \cdot \Delta T = \tfrac{1}{4}V_s$$

so that the first step in the opposite direction will be one half of the size of the previous step. The voltage must then continue to decrease with a slope of

$$-\frac{V_s}{4\Delta T}$$

until the minimum value, V_o, is reached.

Should the overloading signal be of such amplitude that a step size of $32\Delta V$ is used, the first step size in the opposite direction should be $16\Delta V$ so that no sudden decrease in $v_s(t)$ is necessary. As discussed in Section 4.5, if, during the deceleration period, three successive steps are in the same direction, the step size decrease must be halted as illustrated by the dotted portion of the waveform of Figure 5.3(g).

The block diagram of this control circuit is shown in Figure 5.4. It operates on a digital basis, that is, it counts the 1 and 0 pulses and if the correct sequence occurs, it switches ramp and step generators

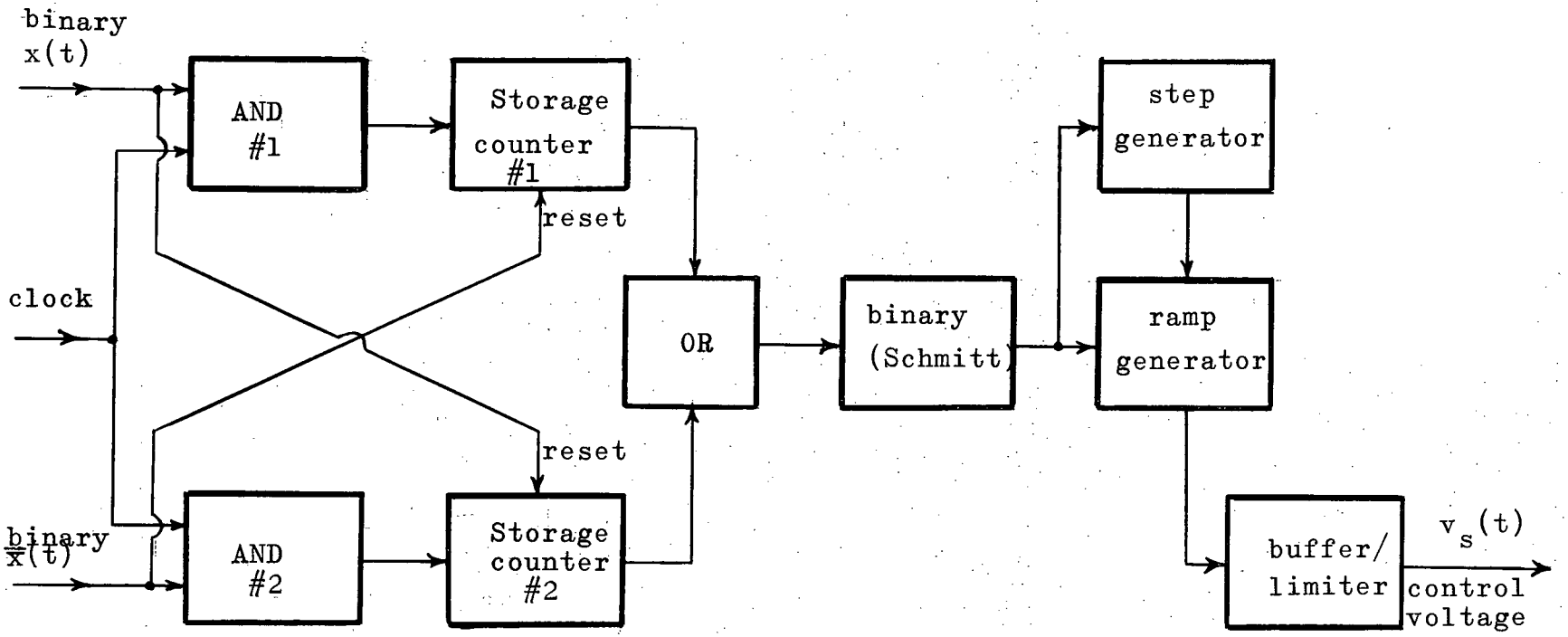


Figure 5.4 Digital Step Size Control Unit — Block Diagram

to produce the required voltage, $v_s(t)$. The actual circuit is not as formidable as would appear from the block diagram since much of it can be built using simple diode circuits. A complete circuit diagram and description are again given in the Appendix, however an abbreviated description of the method of operation follows.

AND circuits #1 and #2 produce pulses corresponding to the coincidence of clock pulses and binary pulses, $x(t)$, and clock pulses and complementary binary pulses, $\bar{x}(t)$. Figure 5.5 shows representative waveforms for a typical input signal.

The storage counters are required to count by three and must be reset to begin counting again if a pulse of the opposite type occurs. This type of counter acts on the trailing edge of the pulse; so there is no output when an input pulse is followed immediately by a reset pulse. In the absence of reset pulses the counter steps to a higher level with each succeeding input pulse. These storage counters, while simple in operation, provided a flexible and reliable counting device which was easily adapted to the resetting requirements.

The binary, acting as a voltage level detector, is switched through the OR circuit by a voltage between the second and third level corresponding to a sequence of three 1 or 0 pulses. Until a reset pulse produced

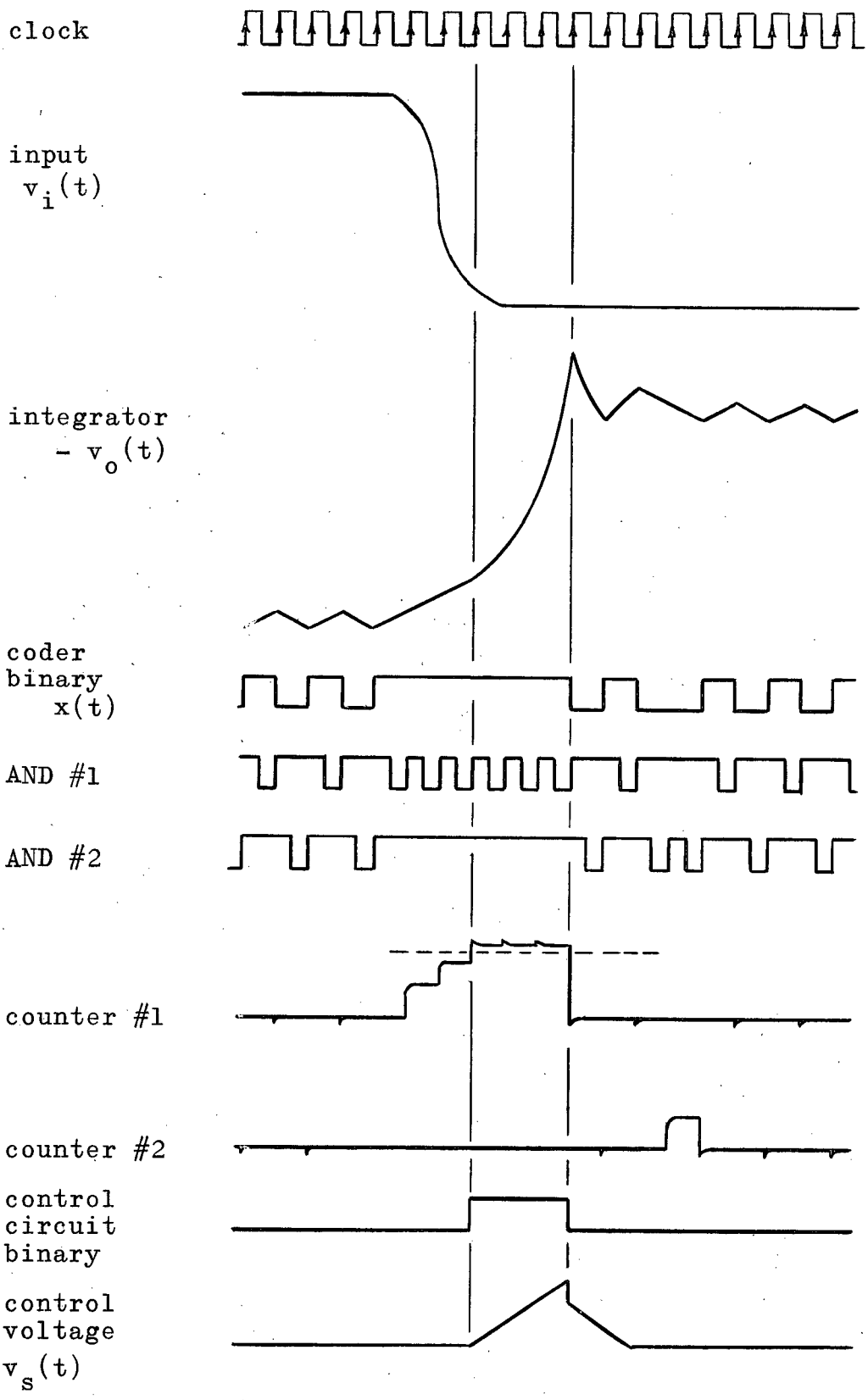


Figure 5.5 Typical Waveforms —— ADM System

by switching of the binary in the coder causes the counter voltage to drop to its normal value, it remains above the triggering level, holding the binary on.

The leading edge of the binary pulse starts the generator which produces the fixed-slope ramp voltage, while the trailing edge causes the step generator to add a negative step of fixed amplitude and reverses the slope of the ramp. The buffer/limiter stage sets the correct values of V_o and $(V_o + V_s)$ and removes the step voltage when it is not required, (as shown in Figure 5.3 (e), (f) and (g)).

5.3.2 Analogue Control Circuit

The second of the two methods of obtaining a step size control signal consists of taking the input to the control circuit from the integrator rather than from the pulse train of Figure 4.1. The decision to change step size is then based on the slope of the integrator signal averaged over a suitable period. In an exponential system this means that the acceleration line will have a constant value independent of the voltage level, instead of varying across the integrator range as in the digital control scheme.

There is an essential disadvantage in the analogue method, however, since the control circuit acts on past pulses thereby causing a delay in step size

change which is especially troublesome in response to the deceleration signal. Also, although the analogue scheme appeared to be relatively simple, in the actual construction a number of problems were encountered such as threshold level stability and dc restoration.

Because of these disadvantages the analogue control circuit was discarded in favour of the digital control circuit described in Section 5.3.1 and the latter was used for system tests and measurements.

6. RESULTS OF TESTS

Two methods were used to compare the performance of the accelerated delta modulation system with that of ordinary delta modulation. The first of these consisted of observing on an oscilloscope and on a chart recorder the response of the two systems to many types of input signals, but especially to"generally correlated" signals.

The second method was a quantitative measurement of overload distortion and quantizing noise, made by taking the mean square of the difference between $v_i(t)$ and $v_o(t)$. From this, an expression of signal-to-noise ratio for a sine wave input signal of varying amplitude was obtained. The main purpose of these measurements was to determine the cost of the improvement in transient response in terms of deterioration of signal-to-noise ratio for signals with slopes near the slope limit.

It should be noted that these tests were made without the use of an output filter and so all components of the noise were present, including high-frequency components that would in most applications be filtered out.

6.1 Waveform Comparisons

Figures 6.1 to 6.5 are oscillograms of output signals ($v_o(t)$). In all cases the upper trace is

the DM response and the lower trace is the ADM response except in Figure 6.1 where both traces are for ADM.

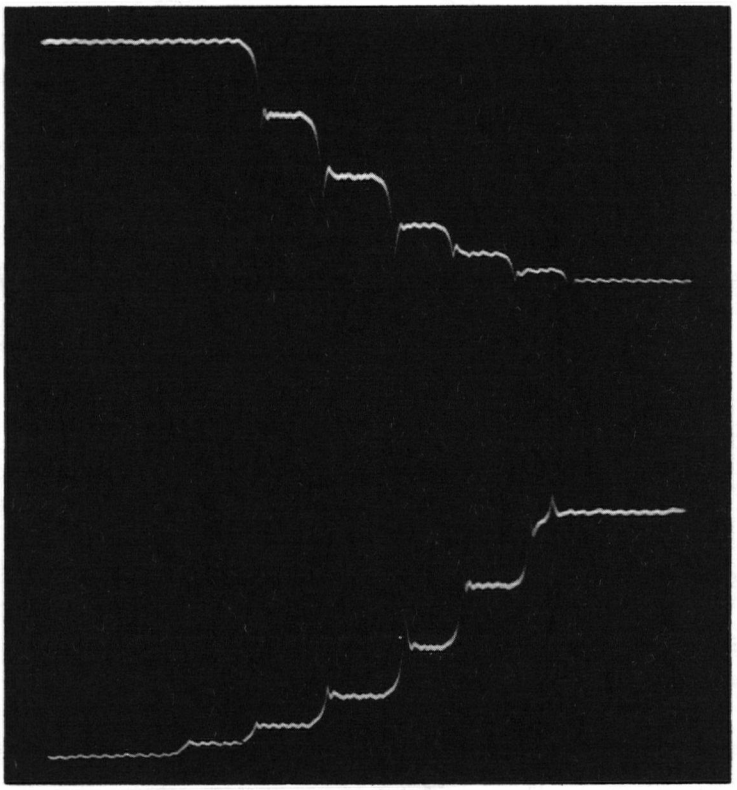


Figure 6.1

This oscillogram shows the ADM output for a series of step input voltages and illustrates the various amounts of overshoot for different size steps. In the upper trace the output is initially at V_m and is reduced by steps of the following sizes until $-V_m$ is reached: 1.2, 1.0, 0.8, 0.5, 0.3 and 0.2 volts.

In the lower trace the output is initially at $-V_m$ and is increased by steps of the same size as before but in the reverse order. The effect of the exponential integrator characteristic is shown by the difference in the amount of overshoot for equal but opposite steps occurring at different integrator voltages. The total trace time in both cases is approximately 10 seconds.

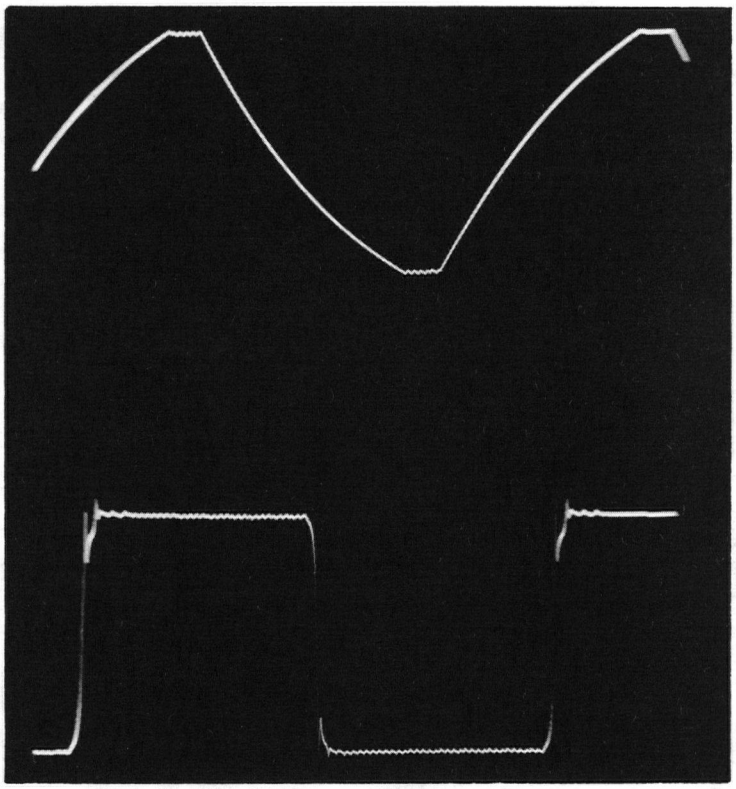


Figure 6.2

In this example the input signal was a 0.07 pps square wave with an amplitude of approximately 4 volts peak-to-peak. The relative ability of DM and ADM to follow a sudden change in input is clearly shown, for while the DM response follows with its maximum possible slope and reaches the correct output only after a long delay, the ADM output very quickly reaches the correct value, and after a short interval of large quantizing noise, again follows the input signal with the desired accuracy.

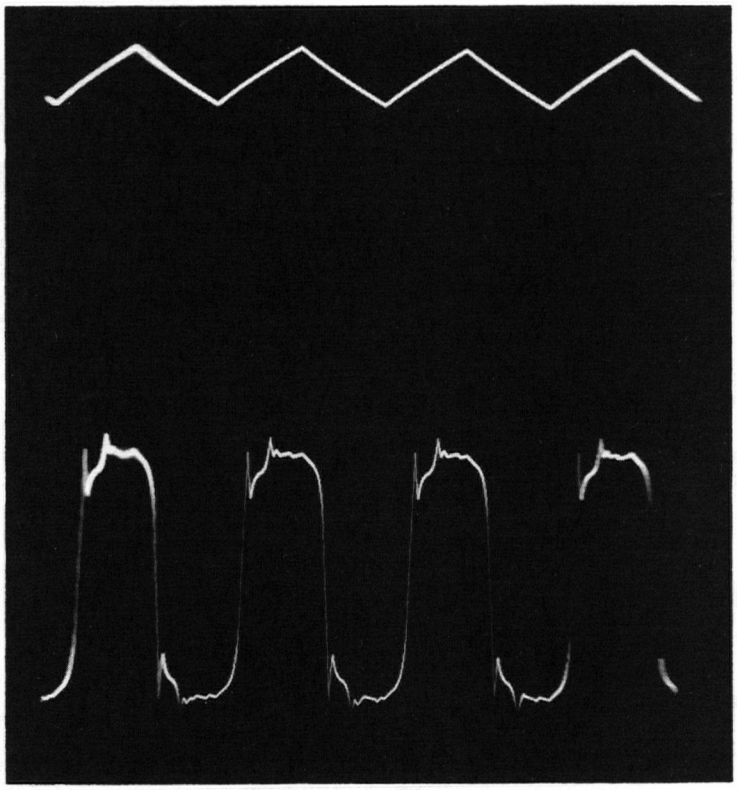


Figure 6.3

These traces show the response to a square-wave input signal of 0.4 pps and approximately 4 volts peak-to-peak. At this frequency the DM output has become a triangular waveform of much smaller amplitude than the input signal while the ADM output still shows the general form of the input signal and reaches the correct amplitude.

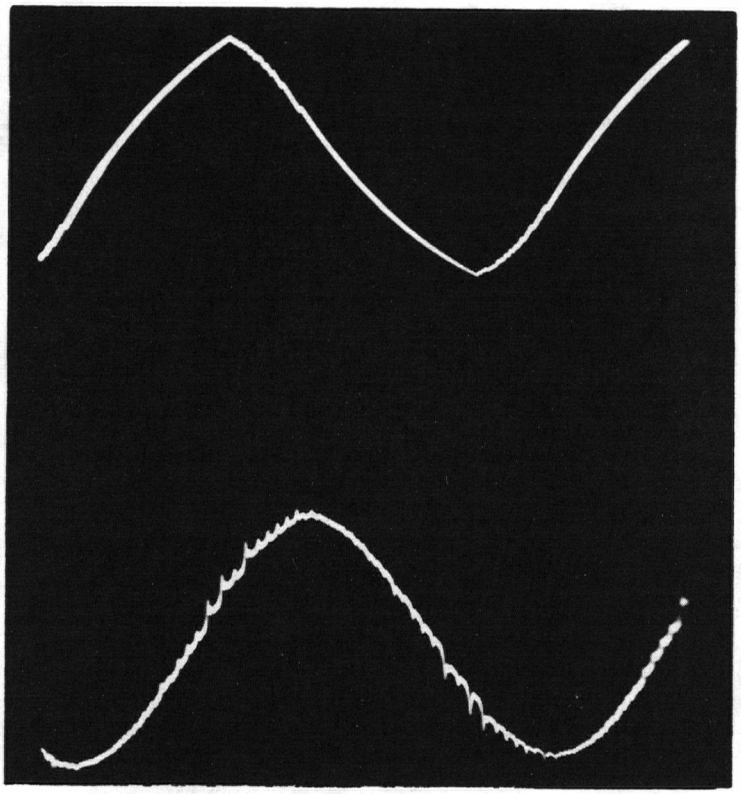


Figure 6.4

This shows the response to a 4 volt peak-to-peak sine-wave input signal of frequency 0.07 cps which causes a small amount of overload distortion for DM, and illustrates the reaction of ADM to a signal with a continually varying slope. It can be seen that the ADM response gives a better gross approximation to the sine wave but has, over most of the curve, considerably greater high-frequency quantizing noise.

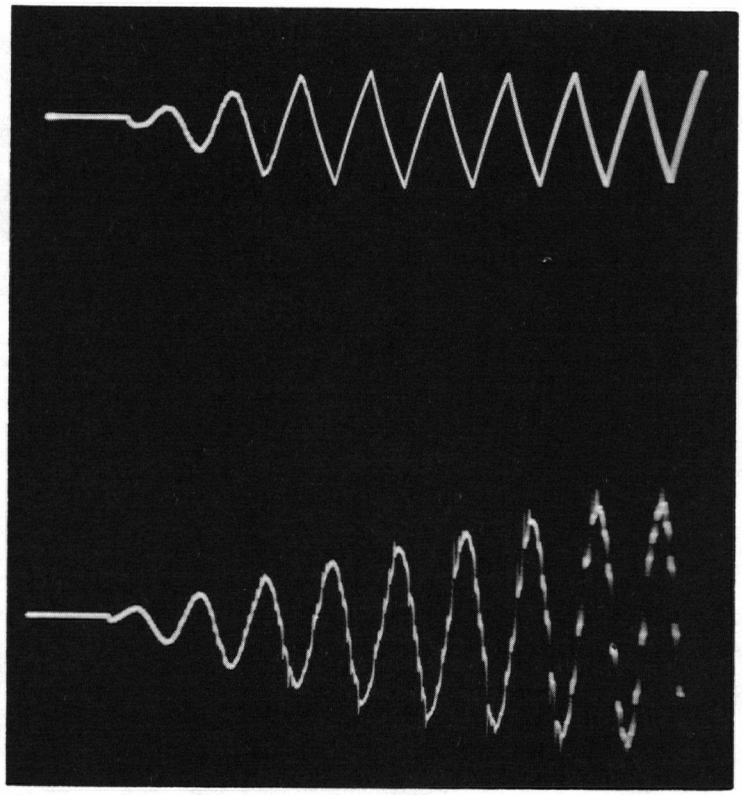


Figure 6.5

This oscillogram was taken for a period of 50 seconds with a sine-wave input signal of frequency 0.2 cps and varying in amplitude from 0 to 4 volts peak-to-peak in 40 seconds. It shows the limiting in output which occurs in the DM system which is able to follow only about the first two cycles of the input signal. The ADM system gives a good representation of the input for all amplitudes from zero to the maximum.

6.2 Discussion of Waveforms

In addition to the system parameters for which the waveforms shown were observed, various other values of the parameters were used in order to check that the best values had been selected. Although some of these different values showed better results for certain types of input signals, it was found that the parameters selected proved most advantageous for a variety of inputs. For example, a delay in reducing step size after the deceleration signal gave better ability to follow very short input pulses but caused excessive recovery time for step inputs.

A lengthening of the acceleration signal from three to four pulses gave less quantizing noise for certain signals with small slopes, but increased the quantizing noise for signals with larger slopes and also increased the delay in responding to steps.

The advantage of varying the step size in correspondence with the amplitude of the overloading signal is demonstrated in Figures 6.1 and 6.4 where, for small overloading signals, the overshoot is small.

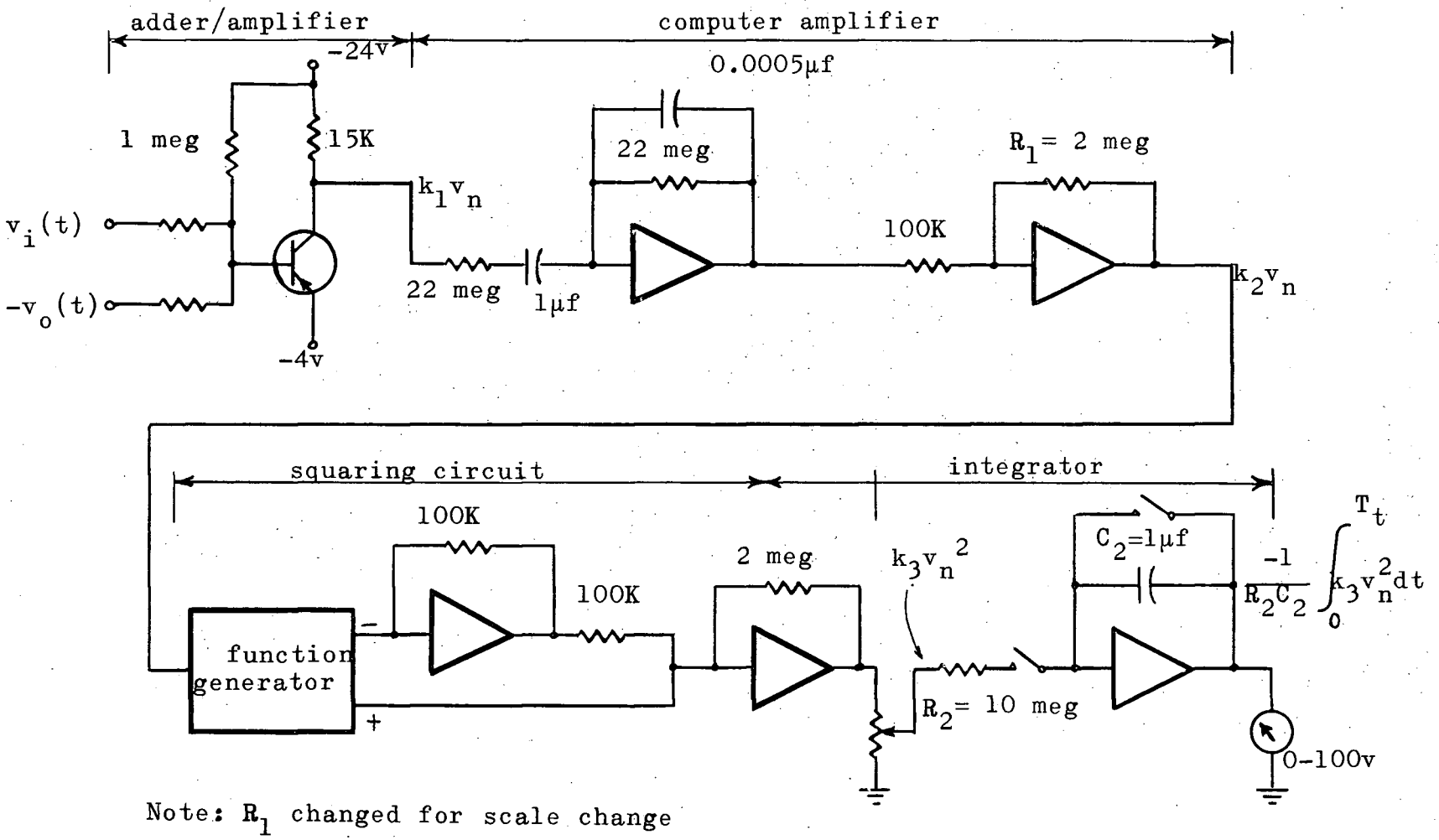
The recovery time after acceleration for various amounts of overshoot can be seen from the oscillograms. This time is quite short in all cases, the longest period being that associated with re-acceleration which occurs mainly at the extremes of

the amplitude range. An example is in the last step of the lower trace of Figure 6.1. Even in such cases as this, the total of delay time plus acceleration time plus recovery time is still only a fraction of the time required for the output of the DM system to arrive at the correct value.

Besides those inputs for which the response is shown in the oscillograms many more input signals were used, including random variations such as could be expected in some telemetering or other applications. For even the most erratic of these, no instability was detected, any oscillations being quickly damped out. At the extreme ends of the amplitude range slight oscillations occur after the deceleration period because, as was shown in Section 4.7, the acceleration line approaches zero. Examples of these may be seen in Figure 6.2.

6.3 Method Used to Measure Noise

Because the speed of operation selected for the constructed system was so low, an analogue computer, as shown in Figure 6.6, was used to obtain accurate noise measurements. The quantity measured was the error signal, which in this case, was the sum of the input signal, $v_i(t)$ and the integrator voltage, $-v_o(t)$. Although this error was composed of quantizing noise plus overload distortion, for simplicity it will be referred to as simply noise. The testing circuit was



Note: R_1 changed for scale change

Figure 6.6 Noise Measuring Circuit

calibrated by replacing $-v_o(t)$ with a fixed voltage.

The signal-to-noise ratio (SNR) was obtained as follows:

$$v_n(t) = v_i(t) - v_o(t)$$

where $v_n(t)$ = instantaneous noise voltage.

The mean-square value of noise is

$$\overline{v_n^2} = \frac{1}{T_t}\left[\frac{1}{R_2 C_2}\int_o^{T_t} k_3 v_n^2 \, dt\right]$$

and similarly for $\overline{v_i^2}$

where T_t is the testing time

k_3 is a constant determined by the computer arrangement

R_2, C_2 are values of resistance and capacitance in the computer integrator.

Then the signal-to-noise ratio is given by

$$SNR = 10 \log \left(\frac{\overline{v_i^2}}{\overline{v_n^2}}\right)$$

$$= 10 \log \frac{\int_o^{T_t} v_i^2 \, dt}{\int_o^{T_t} v_n^2 \, dt} \quad \text{db}$$

The noise sample is not a random function but contains components of the input signal frequency, as well as of the sampling frequency. For this reason the length of the measured sample was made a multiple of the period of the input signal, and of sufficient duration to average the variations from period to period. For example, in the tests using an input signal of 0.2 cps, the noise was integrated over 10 cycles or 50 seconds.

6.4 Results of Noise Measurements

Typical results of noise measurements for the DM and ADM systems are shown on the graph of signal-to-noise ratio versus amplitude of input signal for a 0.2 cps sine-wave input (Figure 6.7). Measurements were also made for other frequencies of input signal with similar results, the overall signal-to-noise ratio being greater at lower frequencies and less at higher frequencies.

The delta modulation characteristic exhibits the usual behaviour; a signal-to-noise ratio increasing with amplitude until slope overload occurs after which it drops off sharply and then approaches asymptotically to zero db.

The accelerated delta modulation signal-to-noise ratio is identical to that of DM for amplitudes giving slopes below the acceleration line. Just above this line a slight improvement in SNR over DM occurs, caused

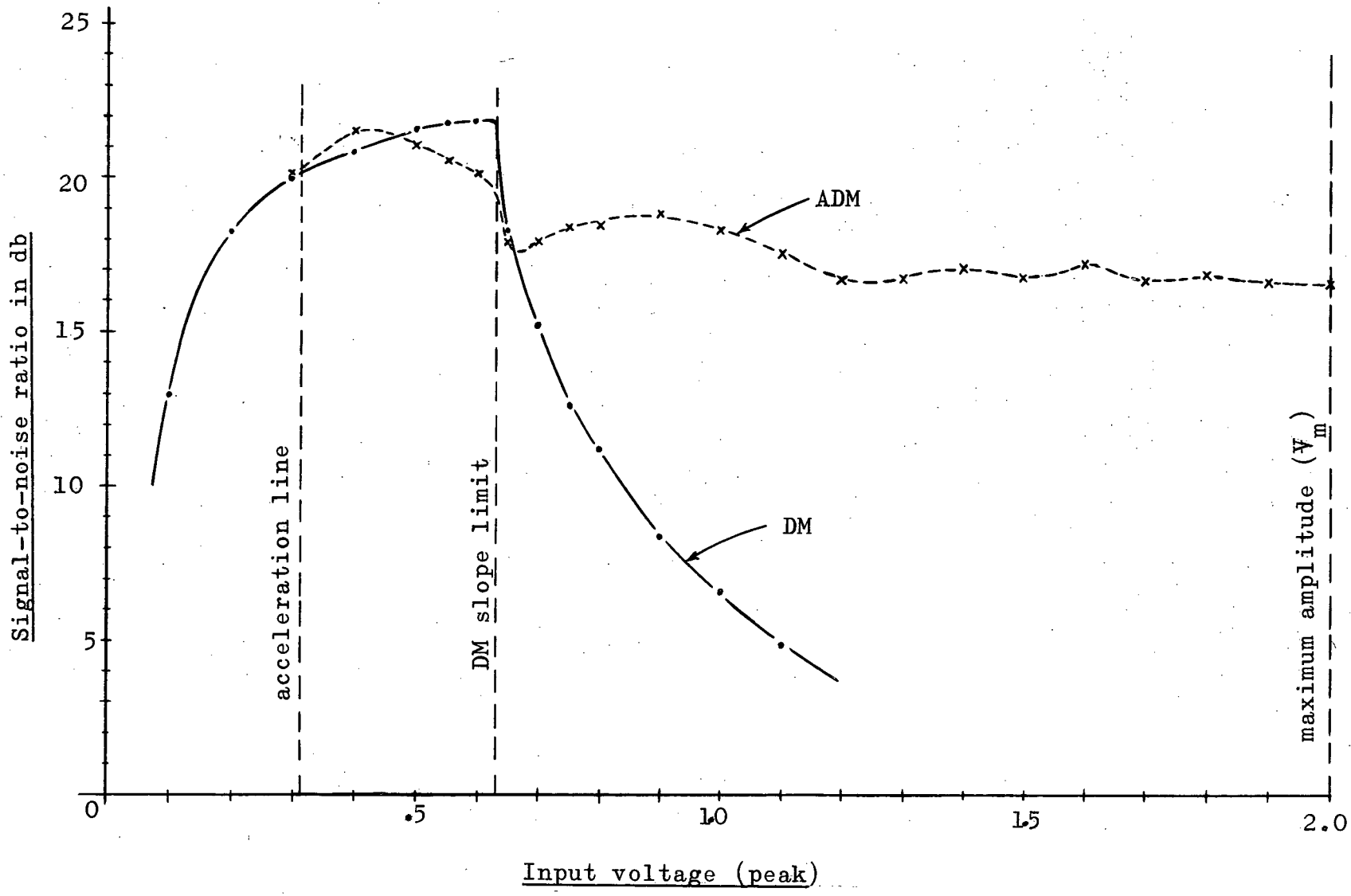


Figure 6.7 Graph of Signal-to-noise Ratio Versus Amplitude for 0.2 cps Sine-Wave Input

by a slight acceleration with little or no overshoot. This slight improvement is less noticeable at other frequencies of input signal.

The expected deterioration in SNR as compared to DM occurs for amplitudes slightly below that causing DM overload distortion. This deterioration is less than was anticipated, being as shown, only about 2 db. Thus for sine-wave input signals the penalty paid for the improvement in response to sudden jumps is indeed quite small.

Although for larger amplitudes the SNR of ADM drops off somewhat from its maximum value, it then remains almost constant for increasing input voltage, showing that the noise voltage increases in direct proportion to the input signal voltage. This means that for a specified minimum signal-to-noise ratio the range of input signals that can be handled by ADM is much greater than can be handled by DM. For example, in Figure 6.7 for a minimum SNR of 15 db the amplitude range of ADM is over 4 times as great as that of DM, indicating an increase in dynamic range of over 12 db. Since the ADM noise contains a larger percentage of high-frequency components than the DM noise, use of a low-pass filter in the output would show an even greater advantage for ADM.

7. CONCLUSIONS

7.1 Conclusions Regarding the ADM System

The object of this work was to investigate a method of increasing the efficiency of systems transmitting signals containing occasional transients. Because of the difficulty of a general theoretical investigation, a method was developed pertaining specifically to delta modulation.

Selection of optimum parameters for transmission of this type of signal produced the ADM system. Results of tests on this system show that a very significant improvement in transient response has been obtained with no increase in transmitted pulse rate. The expected increase in quantizing noise for signals near the DM slope limit was small. Although more circuitry is required for ADM than for DM the equipment is still relatively simple compared to other binary pulse systems.

7.2 Application to Other Systems

The ADM system can be summarized as follows.

Following an acceleration signal derived from the pulse train, both the transmitter and receiver interpret the succeeding pulses in a different manner, and consequently increase the size of steps at the integrator. After the transient condition has passed, normal interpretation of the pulses is resumed. This concept of changing the meaning of the code to accommodate occasional transients in the signal will now be examined in a more general sense.

The idea of changing the meaning of a code is not a new one. Various systems have been developed which operate on this basis. However, informing the receiver of code changes is usually accomplished by using a separate supervisory channel. For instance additional pulses can be time-multiplexed with the message transmission. Such a supervisory channel must be capable of fast action, however, and because of this, a considerable fraction of the total channel capacity would be needed if even only one code change is used. Although an improvement in efficiency can be obtained by this method the equipment required is quite complex. An example of such a system applied to video transmission is described in Reference 7.

In the present case the information for code change is derived from the transmitted message itself. If the signal behaves in a certain manner (indicating impending or incipient overload) both the transmitter and receiver know that the next code pulses are to be interpreted in a different way. This process may be described as a "self-adjusting" code.

A fixed capacity system using a "self-adjusting" code to allow transmission of transients will inevitably cause degradation for some other signals which otherwise would be transmitted accurately. However, the overall quality of transmission will be better than for a system with a non-adjusting code.

From the experience gained with ADM we can conclude that "self-adjusting" codes show promise as a general method of improving the efficiency of systems transmitting "generally correlated" signals. Their application might also be extended to signals containing occasional disturbances of other kinds than transients; for instance, to signals containing occasional large amplitudes.

APPENDIX

Instrumentation

The various stages of the coder and step size control unit are, for the most part, standard circuits and require no explanation other than the circuit diagrams. There are, however, a few sections where some explanation is necessary.

The descriptions refer to the block diagrams, Figures 5.1, 5.2 and 5.4 and to the typical waveforms, Figure 5.5, as well as to the circuit diagrams of the coder and control circuit, Figures A-1 and A-2 respectively.

A. Coder (cf. Figure A-1)

Binary

The binary is a Schmitt trigger with a hysteresis voltage of 1.6 volts. Its input is normally clamped by the gate to -10.1 volts which is in the centre of the hysteresis range. Opening of the gate applies a 0.15 msec sample of the amplified and clipped error signal to its input. This sample switches the binary to state 2 if it is above -9.3 volts or to state 1 if it is below -10.9 volts.

Integrator

The integrator consists of a 300 μf capacitor shunted by an 18K resistor. This resistor is connected to the -4 volt supply in order to establish the mid-point

of the integrator voltage range. This range is from -2 to -6 volts corresponding to an input voltage range of -6 to -2 volts.

This large value of capacitance was chosen so that the currents feeding the integrator are of sufficient magnitude to swamp variations due to temperature.

Since $\lambda = RC = 5$ sec

$C = 300\ \mu f$

$$R = \frac{5}{300 \times 10^{-6}} = 16.7K$$

The value of 16.7K is the total resistance shunting C, including the 18K resistor and the input resistance of T11. The current for normal step size is

$$I_o = C \frac{\Delta V}{\Delta T}$$

$$= 300 \times 10^{-6} \times 0.8$$

$$= 0.24 \text{ ma}$$

and the current for maximum step size is

$$I_{max} = 0.24 \times 32$$

$$= 7.68 \text{ ma}$$

The stability of this portion of the circuit presents the most critical design problem in the coder. In order to obtain a dc voltage accuracy of $\pm 0.5\%$ the deviation of the sum of fixed currents plus average value of switched

current from zero, must not exceed

$$\frac{\frac{1}{2}\Delta V}{R} = \frac{20 \text{ mv}}{16.7\text{K}} = 1.2 \ \mu\text{a}$$

The drift can be held to a small value by using matched complementary transistors for T9 and T10 and a common heat sink. This problem, of course, is not peculiar to ADM but exists in any exponential DM system.

Current Generator

As explained previously, the steps at the integrator are obtained by feeding a closely controlled current into or out of the storage capacitor for a definite time interval.

The amount of current flow into the capacitor is determined by the voltage at the base of transistor T8. For a normal step size of 40 mv this voltage is +10.5 volts, and a corresponding current of 0.24 ma flows through diode D2 to charge the storage capacitor. During this interval transistor T7 is held cut-off by the voltage from the binary through T6.

When a step in the other direction is required, T7 is turned on by applying about -10 volts to its base. This raises the emitter of T7 to -10 volts and cuts off diode D2. The collector current of T8 now flows through the collector resistance of T7 which causes an increase in current in transistor T9 and consequently discharges the

storage capacitor. The value of this discharge current is the same (0.24 ma) as the former charging current.

There is a continuous current, $-I_1$ flowing in T9 whether T7 is open or closed. This is balanced by a constant current, $+I_1$ fed into the capacitor by current generator T10 so that the net current is zero.

The diode and resistor circuit connected to the emitter of T8 makes up the exponential function generator. Design of this function generator was simplified and the approximation improved by including the integrator characteristics. For this purpose the integrator was considered as having an infinite time constant in accordance with the required system characteristics.

In this way, by matching the integrator voltage at the sampling points with the ideal exponential curve, a piece-wise-linear current could be used. The only error then, was that small amount introduced by the effect of the finite time constant of the integrator. It should be pointed out that any such errors would not result in system errors since an identical arrangement would be used in the decoder.

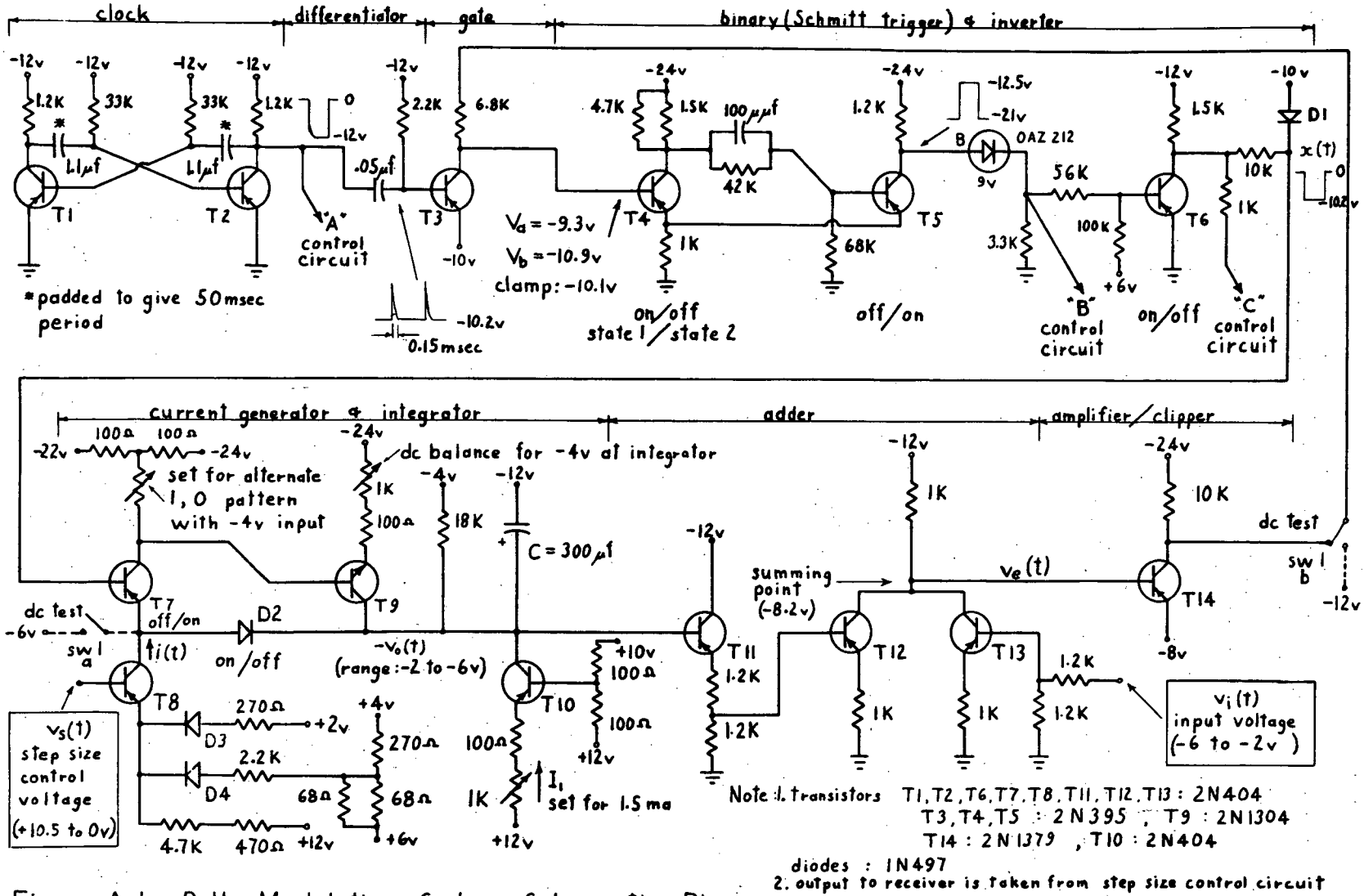


Figure A-1 Delta Modulation Coder — Schematic Diagram

B. Step Size Control Circuit (cf. Figure A-2)

Storage Counters

The counters are standard two-diode storage type, with the added feature of reset control. This reset occurs when the coder binary switches, causing a negative pulse to appear on the reset line. This may occur at any stage in the counting sequence, and after a reset pulse counting starts again from zero.

The output of the counters actually lags the coder binary by one full sampling interval. A one-half period delay is introduced because the AND circuits operate on the negative-going portion of the clock waveform instead of on the positive-going portion. In addition, the counters in themselves have an inherent one-half period delay.

As pointed out in Section 5.3, this total delay enables the reset pulse, acting without delay on the next coder binary decision, to cancel a pulse before it is counted.

Ramp and Step Generator

In the ramp and step generator, transistor T4 is normally held off by a negative voltage from the binary. Transistor T5 is conducting, its collector current, I_{c5}, flowing through diode D18 which clamps the 20 μf capacitor voltage to approximately +10 volts. Diodes D16, D17 and D19 are reverse biased.

When the binary switches, T4 is turned on. The collector current I_{c4} of T4 is twice that of T5. A current equal to $(I_{c4} - I_{c5}) = I_{c5}$ discharges the 20 μf capacitor at a constant rate, dropping the voltage at the base of T6 and cutting off D18. This negative-going ramp voltage continues until either it is clamped to - 2.5 volts by D19 or the binary again switches.

When the binary switches back to its normal condition a negative step turns T4 off and through the 0.6 μf capacitor and diode D16 drops the base voltage of T5 and opens D17. The collector current of T5 is thus greatly increased for a short interval. The time constant of the circuit is such that a positive 2.5 volt step appears on the 20 μf capacitor.

With T4 off, the capacitor, after the initial step is charged at a constant rate by current I_{c5}, diodes D16 and D17 again being reverse-biased. This produces a positive-going ramp which continues until clamping by D18 occurs or the binary again changes its state.

Thus the voltage at the base of T6 varies between $^{+}10$ volts and -2.5 volts.

Buffer/Limiter

Diode D20 performs the final clamping of the control voltage, reducing its limits to $^{+}10.5$ and 0 volts.

Figure 5.3 shows the waveforms produced by the circuit, except that in the constructed unit a negative going control voltage was used instead of a positive going voltage as shown.

The slope of $v_s(t)$, from Section 5.3.1 is

$$\left|\frac{dv_s}{dt}\right| = \frac{V_s}{4\Delta T}$$

$$= \frac{10}{4 \times 50 \times 10^{-3}} = 50 \text{ volts/sec}$$

or 2.5 volts per sampling interval.

From which

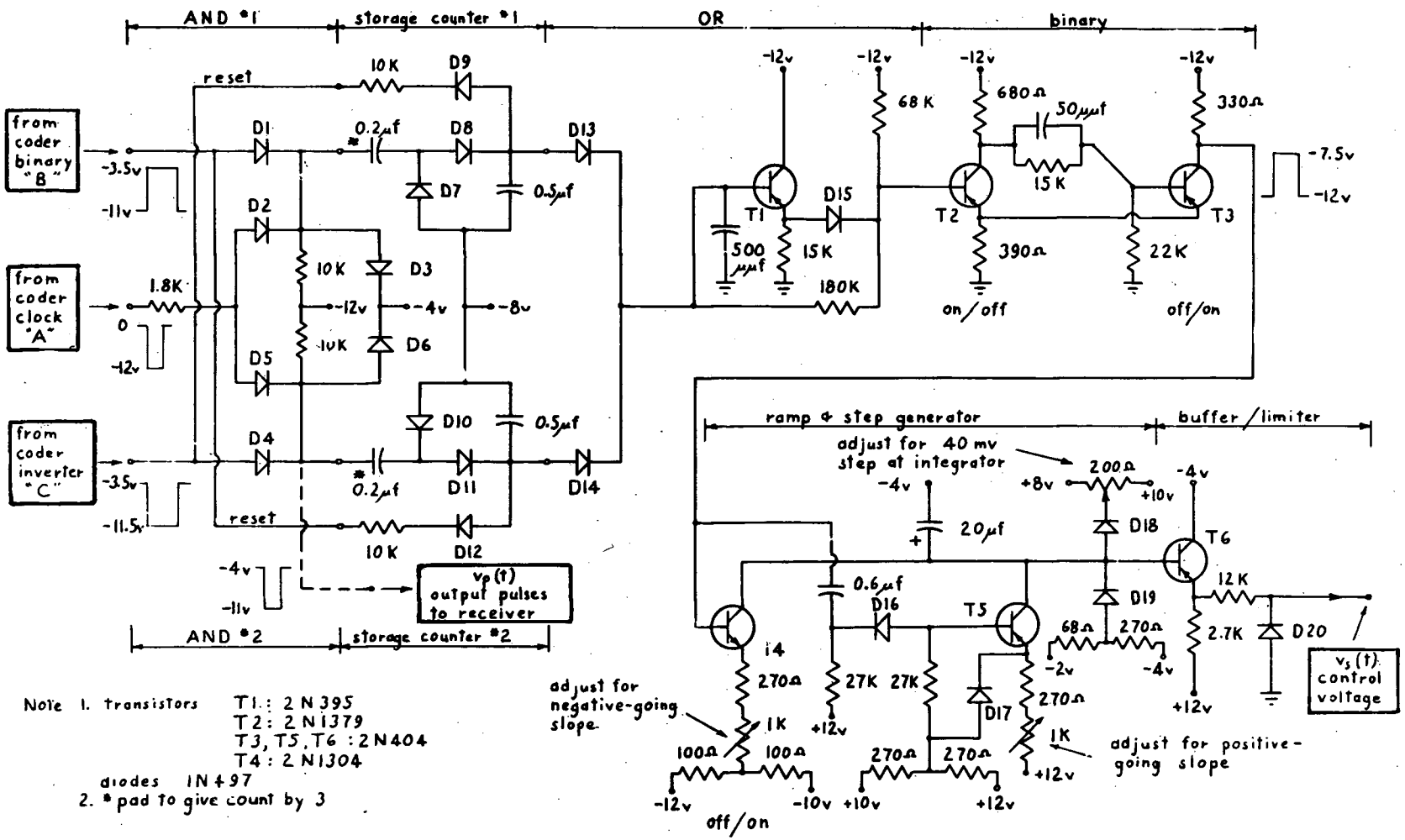
$$I_{c5} = C \frac{dv_s}{dt}$$

$$= 20 \times 10^{-6} \times 50 = 1 \text{ ma}$$

and

$$I_{c4} = 2 I_{c5}$$

$$= 2 \text{ ma}$$



Note 1. transistors T1: 2N395
T2: 2N1379
T3, T5, T6 : 2N404
T4 : 2N1304
diodes IN497
2. * pad to give count by 3

Figure A-2 Step Size Control Circuit — Schematic Diagram

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