RELIABILITY STUDY OF BIPOLAR TRANSISTORS WITH METAL-INSULATOR-SEMICONDUCTOR HETEROJUNCTION EMITTERS.

by

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We accept this thesis as conforming
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Abstract

Bipolar transistors employing an MIS junction for the emitter exhibit the very desirable properties of high operating frequency and/or high common emitter gains. The topic of this thesis is to investigate the usefulness of the MIS bipolar transistor in real applications. The experimental results show two possible limitations of the devices. The principal limitation is the inability of these devices to withstand moderate temperature stressing. The second limitation is the relatively high emitter series resistance. The principal degradation mode of these devices under temperature stressing is suggested to be the reduction of the thin insulating oxide.

Acknowledgement

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Chapter 1

Introduction

Silicon bipolar junction transistors (BJTs) have been used extensively for the last thirty years or so. Although new technologies have evolved, the need for bipolar devices has never stopped. In fact, the fastest silicon digital logic nowadays is still emitter coupled logic (ECL), which is based on bipolar technology. However, as the need for faster computers and higher frequency communication devices grows, bipolar technology is continually being developed in order to further improve the operating speed. Presently the fastest devices have cut-off frequencies (f_T) around 15-20 GHz.

The techniques under development to increase the performance of BJTs, including the use of metal-insulator-semiconductor (MIS) and polysilicon emitter devices, are briefly reviewed in this chapter.

The current components of a typical NPN BJT operating in the active mode are shown in Fig. 1.1. J_{INJ} and J_{BINJ} are the current components that make up the emitter current J_E. J_{REE}, J_{REC} and J_{REB} are the recombination current components that correspond to recombination of holes in the neutral emitter, base-emitter space-charge region, and the neutral

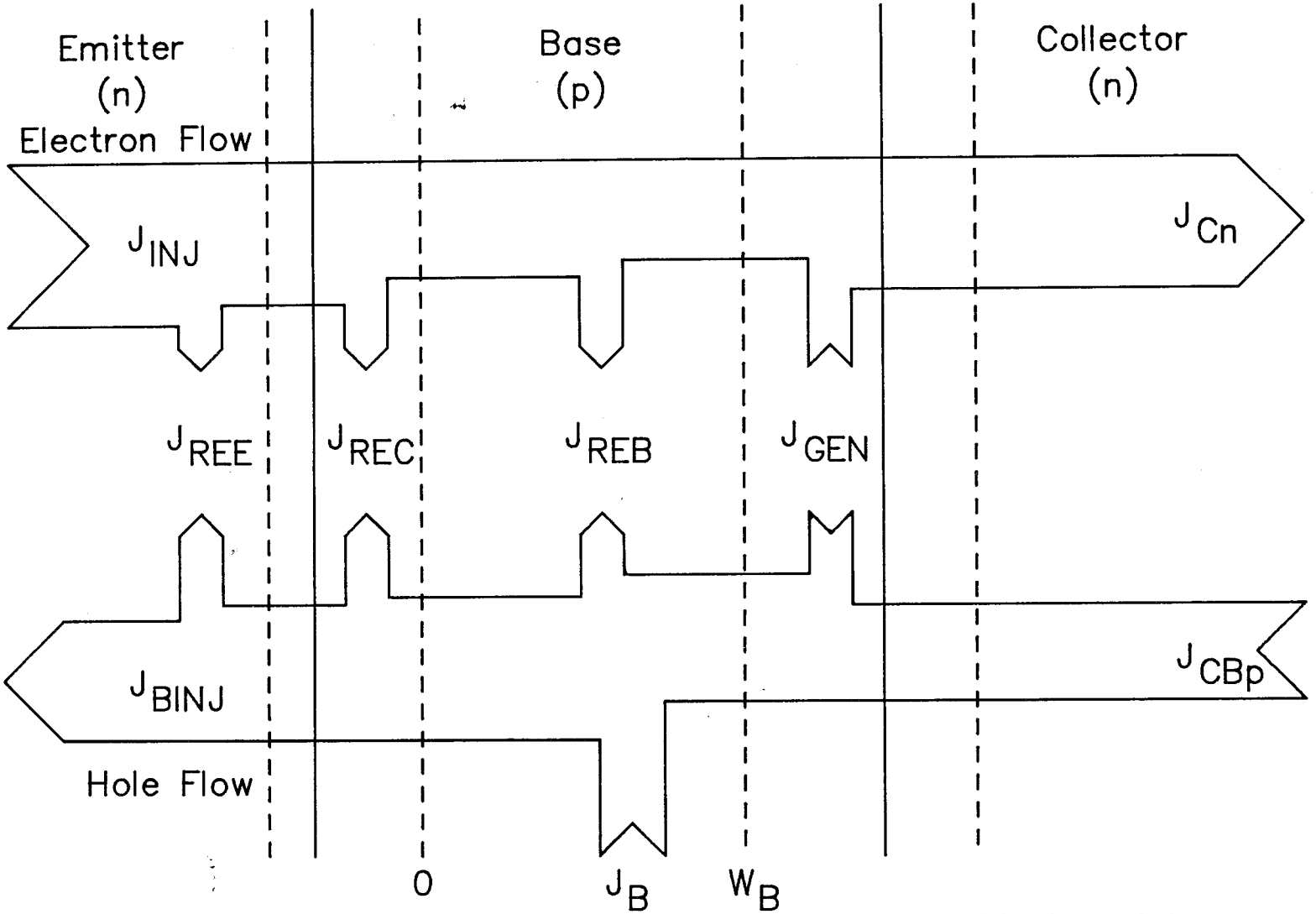


Fig. 1.1. Current components in a typical NPN transistor

base respectively. J_{GEN} is the generation current in the base-collector space-charge region, and J_{CBp} is the hole saturation current due to transport across the base-collector junction. The current components at the three terminals of the BJT are then:

$$J_E = J_{INJ} + J_{BINJ} \tag{1.1}$$

$$J_B = J_B \tag{1.2}$$

$$J_C = J_{Cn} + J_{CBp} \tag{1.3}$$

One approach to obtaining a higher cutoff frequency in a BJT is to first increase the common-emitter current gain and then trade off some of this gain for a higher operating frequency. To achieve high common-emitter current gain, the collector current J_C should be maximized while minimizing the base current J_B. Several techniques are available and can be used together to achieve the goal.

The traditional approach to achieve higher performance BJTs is to increase the emitter injection efficiency by using a lightly doped base and a heavily doped emitter. This arrangement allows the base minority carrier diffusion current to dominate the base-emitter current carrier transport process, since the minority carrier concentration in the emitter is much less than that of the minority carrier concentration in the base region. Furthermore, the base-emitter depletion region appears mainly in the base

region, causing a narrower effective base width, and so reduces the neutral base recombination current.

The dopants can be introduced by either diffusion or ion implantation techniques. The latter is preferred as it can provide better control for doping in the base and emitter regions of the transistor. The tight process control that is possible with ion implantation also allows the width of the base region to be made very narrow, further reducing the neutral-base recombination current. A typical base width in state-of-the art silicon BJTs is 0.15μm [1].

Ion-implanted high/low emitter/base junctions and narrow bandwidths are employed in modern silicon bipolar transistors to achieve better performance and better process control. However, as the doping density of the emitter region increases, bandgap narrowing occurs and Auger recombination takes place. Both these effects cause a reduction in emitter injection efficiency, thereby reducing the transistor performance.

It is known that metal in close vicinity to semiconductor material will cause band bending in the semiconductor. With the right choice of metal, the surface of the semiconductor can be inverted and the band bending in the semiconductor will resemble that of an ideal p-n

junction. Theoretically, if the separation between the metal and the semiconductor is infinitesimally small so that both electrons and holes can tunnel through the separating material, the structure will behave like an ideal p-n junction, with minority carriers within the semiconductor dominating the current transport process [2]. However, when the metal comes in direct contact with the semiconductor, the metal-semiconductor interface will have a large surface state concentration, due to dangling bonds that result from the incompatible bonding structures of the two materials. The large amount of surface states will accommodate the major portion of surface charges that result from the work function difference between the metal and the semiconductor, leading to less band bending in the semiconductor. As a result, the barrier height of a metal-semiconductor interface is usually determined by the property of the semiconductor surface and the barrier height for minority carriers is larger than that for majority carriers.

Low temperature silicon oxide grown on top of silicon bonds nearly perfectly to the semiconductor surface without causing a large surface state concentration at the silicon surface, while the thickness of the oxide can be controlled to such a degree that charge can tunnel through the oxide. With this technology, one can produce a MIS junction that behaves like an ideal p-n junction with the minority

carriers dominating the current transport process, while minimizing the majority carrier flow. Furthermore, the MIS junction will not suffer from the heavy doping effects which can degrade the performance of conventional homojunction bipolar transistors.

Bipolar transistors employing the MIS junction as a replacement for the heavily doped emitter, are presently the subject of much research. The structure for these MIS BJTs is shown in Fig. 1.2. Extremely high common emitter gains, of the order of 30,000 have recently been reported for such devices [3,4]. Gains of this magnitude are not of great practical importance. However, the extremely high gain offers an opportunity for trading-off the gain to achieve a higher operating frequency. This can be most obviously done by increasing the base doping density. This reduces the emitter / base injection efficiency and the base transport factor, so lowering the current gain. However it also reduces the base resistance, and it is this factor which leads to an improvement in frequency response.

This approach has been adopted by several large semiconductor companies. Silicon BJTs fabricated at Plessey research can be operated up to 11 GHz [5], while NTT and Tektronix have fabricated similar devices that have cutoff frequencies of 16 GHz and 15 GHz respectively [6,7]. These

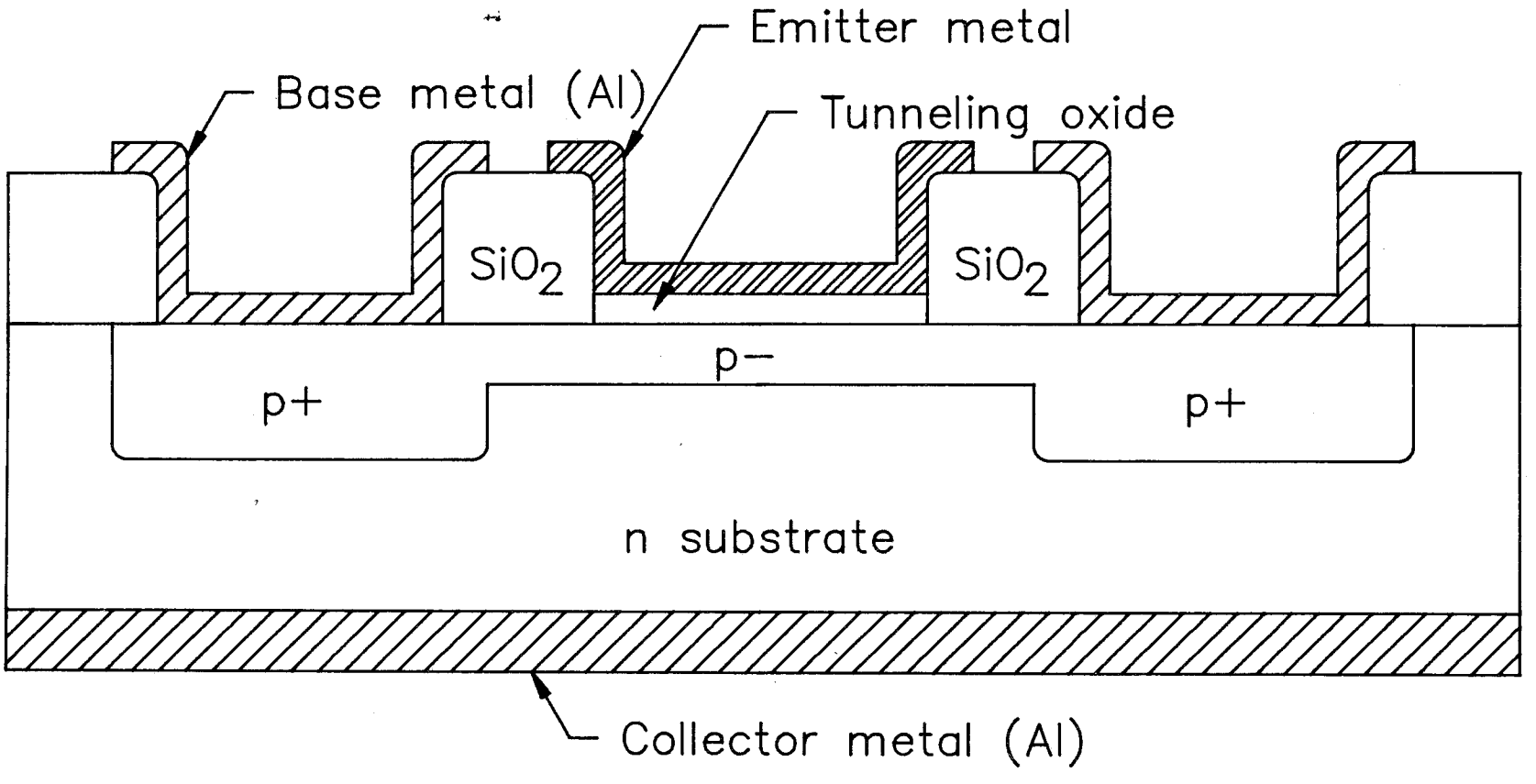


Fig. 1.2. Structure of MIS BJT

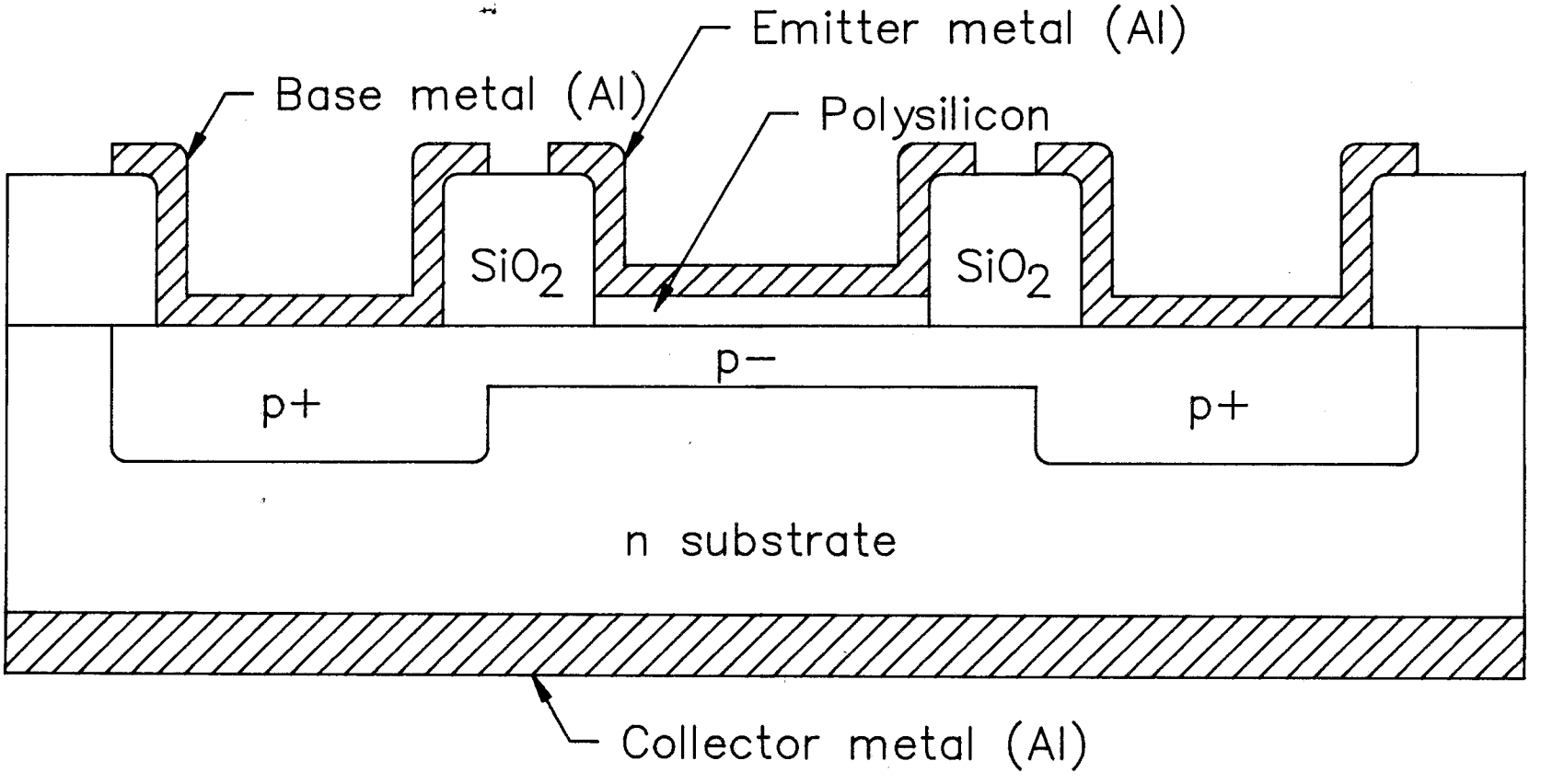


Fig. 1.3. Structure of polysilicon transistor

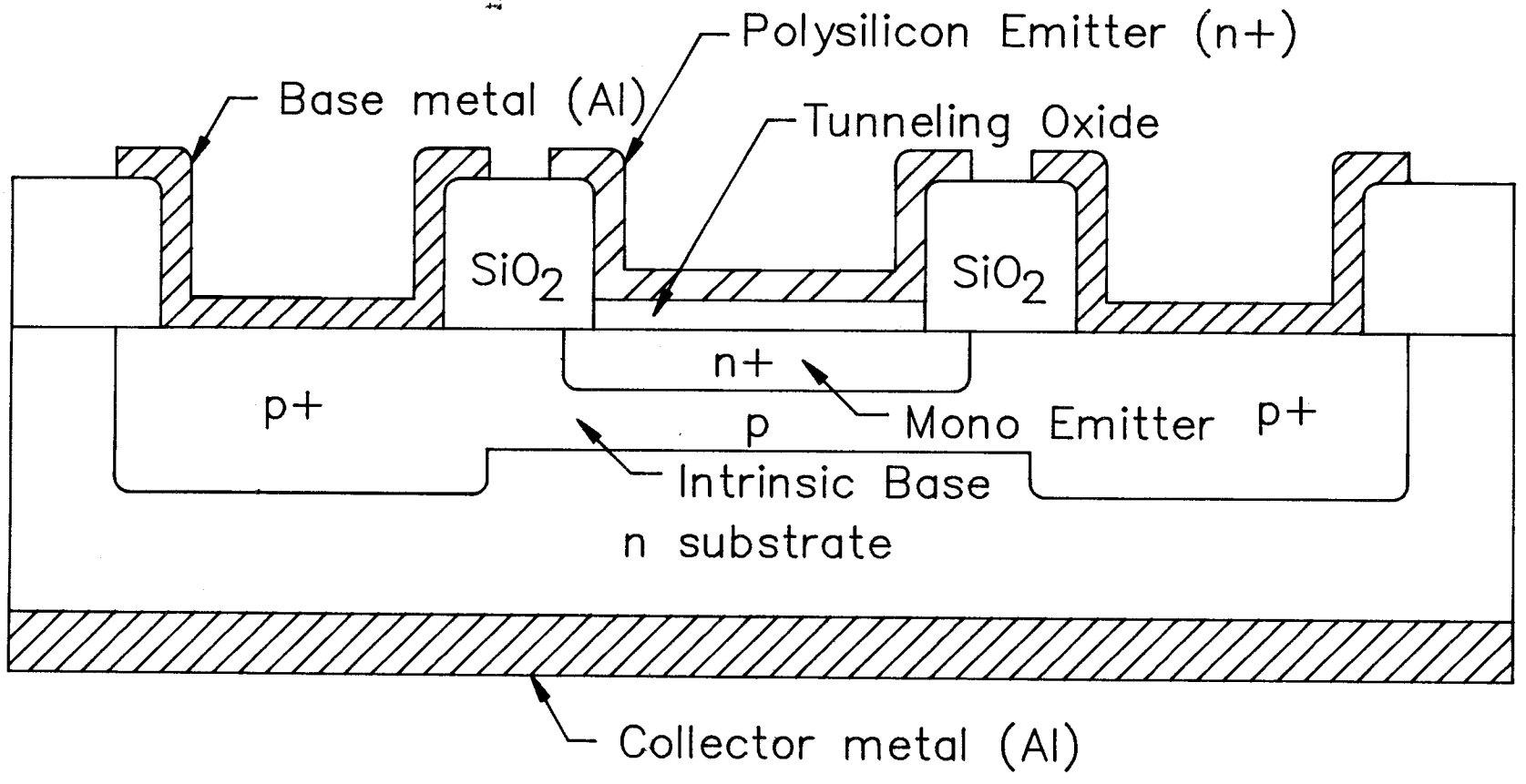


Fig. 1.4. Alternative Structure for Polysilicon Emitter Transistor

cutoff frequencies are a great improvement for silicon devices, and they are just high enough to be used in modern day microwave communication equipment. These excellent results have been achieved using transistors with polysilicon emitters, rather than MIS tunnel junction emitters. The polysilicon may act like the metal in a MIS BJT in the structure shown in Fig. 1.3. [8]. Alternatively the polysilicon tunnel junction may replace the metal layer in a conventional BJT structure, see Fig. 1.4. [9]. The reasons why these polysilicon emitter structures give high gains is still under discussion [9,10,11]. The highest gains so far reported are around 10000 [8].

Both of these new developments in improving the performance of bipolar transistor seem to be very attractive. However, to date there have been no stability and feasibility studies to indicate whether these high performance devices can be implemented in any real applications. A major concern with all the devices lies in the ability to grow the ultra thin oxide layer to an acceptable degree of uniformity in thickness, composition and quality. An additional concern for the MIS junction is the stability and durability of the ultra thin layer of oxide. Aluminum is known to reduce silicon dioxide, both during the deposition of the metal [12] and on subsequent temperature stressing [13]. It is the main purpose of this

thesis to investigate the stability of these MIS-emitter transistor (MIS BJT) devices and to draw a conclusion as to whether the current stage of development of these devices is such that they can be used in any real application.

Another factor that determines the feasibility of implementing these devices is the series emitter resistance. It has been shown that the emitter current of a bipolar transistor of any size, should remain roughly unchanged in order to maintain optimal circuit performance [14]. In VLSI applications, the size of the emitter area is so small that any emitter series resistance would become an important factor in limiting the circuit performance. The interfacial oxide layer in the MIS BJT is a major threat to the successful implementation of the device in VLSI applications. The emitter series resistances of both the MIS BJT and polysilicon emitter transistors were measured to further ascertain the feasibility of implementing these devices in VLSI applications.

Chapter 2

Theory

It is well known that the MIS tunnel junction can behave almost like an ideal pn junction diode [2]. Moreover, the MIS junction is far easier to fabricate than a conventional diffused or ion-implanted pn junction. To formulate the junction characteristics with respect to metal work function, oxide thickness, doping density, carrier lifetime and insulator bandgap is not an easy task. However, with the help of a computer, one can set up numerical model for the MIS junction.

In this chapter a model for the MIS junction diode [2] is reviewed and then used as the basis for a model of a three terminal device, a BJT transistor with MIS emitter.

2.1. The MIS junction model

The band diagram of a typical M-I-p/Si junction is shown in Figure 2.1. There are two tunneling current components J_{CM} and J_{VM} in the model which represent the electron and hole tunneling currents respectively:

$$J_{CM} = \sum_i \theta_{CM}^i A_e^{*i} T^2 (F_1[(E_{Fn}(X_S) - E_C(X_S))/kT] - F_1[(E_{FM}(X_S) - E_C(X_S))/kT]) \qquad (2.1)$$

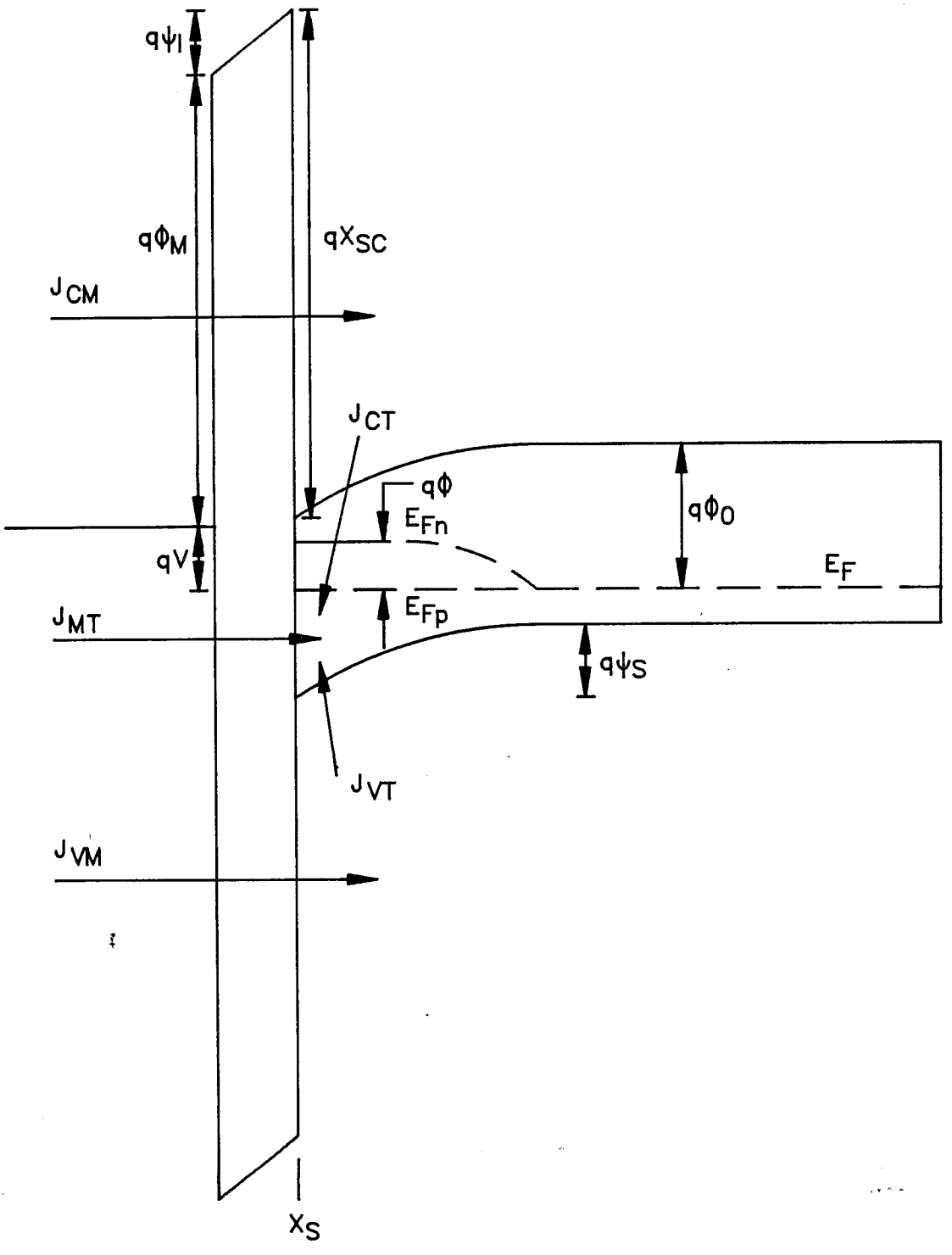


Fig. 2.1. Band diagram for a MIS junction under forward bias

$$J_{VM} = -\sum_i \theta^i_{VM} A^{*i}_h T^2 (F_1[(E_V(X_S) - E_{Fp}(X_S))/kT] - F_1[(E_V(X_S) - E_{FM}(X_S))/kT]) \quad (2.2)$$

where θ_{CM} and θ_{VM} are the tunneling probabilities for electrons and holes respectively, A^*_e and A^*_h are the effective Richardson constants for electrons and holes respectively, F_1 is the Fermi-Dirac integral of order one and the summations run over all the conduction band peaks and valence band valleys.

There are also three surface state current components, J_{MT}, J_{CT}, and J_{VT} which represent the metal to trap, semiconductor conduction band to trap and valence band to trap currents, respectively:

$$J_{MT} = q \sum \frac{N_{Ti}(f_{Ti} - f_{Mi})}{\tau_{Mi}} \quad (2.3)$$

$$J_{CT} = -q \sum N_{Ti} C_{ni} [n(X_S)(1-f_{Ti}) - n_{1i} f_{Ti}] \quad (2.4)$$

$$J_{VT} = q \sum N_{Ti} C_{Pi} [p(X_S) f_{Ti} - p_{1i}(1 - f_{Ti})] \quad (2.5)$$

where N_{Ti} is the trap density at the i^{th} level and f_{Ti} is the occupancy probability at that level, τ_{Mi} is the characteristic time for the metal-to-trap tunneling process and f_{Mi} is the probability that the i^{th} level will be occupied when in equilibrium with the metal, C_p and C_n are the capture cross sections for holes and electrons multiplied by the average carrier thermal velocity. The charge stored in the surface states Q_{SS} is given by

$$Q_{SS} = -q \sum_{\substack{i \\ \text{acceptors}}} f_{Ti} N_{Ti} + q \sum_{\substack{i \\ \text{donors}}} (1 - f_{Ti}) N_{Ti} \tag{2.6}$$

Finally, there are two semiconductor current components, $J_p(X_S^+)$ and $J_n(X_S^+)$, which represent, respectively, the hole current and the electron current just inside the semiconductor.

These currents are linked together by the need for current continuity at the interface. For instance,

$$J_{CM} - J_{CT} = J_n(X_S^+) \tag{2.7}$$

and

$$J_{VM} - J_{VT} = J_p(X_S^+) \tag{2.8}$$

Another boundary condition comes from the summation of the potential drops across the entire diode.

$$-V - \phi_M - \psi_I + \chi_{SC} - \psi_S + \phi_0 = 0 \tag{2.9}$$

These three boundary conditions must be satisfied for the model to produce accurate solutions. By making the assumptions that the majority-carrier quasi-Fermi level is constant throughout the semiconductor and the quasi-Fermi levels for both carriers are constant throughout the space-charge region, the boundary condition that is concerned with the majority carrier (2.8) is overridden. The net minority current component $J_n(X_S^+)$ is given by

$$J_n(X_S^+) = J_d(\phi) + J_{rg}(\phi, \psi_S) - J_{UPC} \tag{2.10}$$

where $J_d(\phi)$ is the minority carrier diffusion current, $J_{rg}(\phi,\psi_S)$ is the recombination current in the space charge region and J_{upc} is the uncompensated photocurrent. The expressions for J_d and J_{rg} from the standard pn junction theory are used here [15]. The uncompensated photocurrent term J_{upc} in the above expression allows for the modelling of photovoltaic effects. It is included for the sake of completeness, but will always be equal to zero for the purpose of this thesis.

$$J_d(\phi) = J_{od} [\exp(q\phi/kT) - 1] \tag{2.11}$$

and

$$J_{rg}(\phi,\psi_S) = J_{org} (\psi_S/2\psi_B)^{1/2} [\exp(q\phi/2kT)-1] \tag{2.12}$$

J_{od} and J_{org} are user input parameters through which the carrier lifetime and semiconductor doping density are included in the model,

$$J_{od} = \frac{qn_i}{N_A} [D_n/\tau_n]^{1/2} \tag{2.13}$$

and

$$J_{org} = \frac{qn_i}{2\tau_n} [2\epsilon_S(2\psi_B)qN_A]^{1/2} \tag{2.14}$$

where $2\psi_B$ is the built-in potential at the onset of strong inversion .

Last of all, the potential across the insulator ψ_I must be calculated in order to evaluate expression (2.9). ψ_I is related to the total charge stored on both sides of the

insulator, by Gauss' law. The charge stored is comprised of Q_S, the charge stored in the semiconductor space charge region, and Q_{SS} the charge stored in the surface states. The expression of ψ_I is then

$$\psi_I = \frac{d}{\epsilon_I} (Q_S + Q_{SS}) \tag{2.15}$$

where d is the insulator thickness. Q_S can be found by assuming that both E_{Fp} and E_{Fn} are constant across the space charge region within the semiconductor [2], then

$$Q_S = \mathrm{sgn}(\psi_S)\ (2kT\epsilon_S)^{1/2} \{ N_C F_{3/2}[(E_{Fn}(X_S) - E_C(X_S))/kT] - n(X_n) + N_V F_{3/2}[(E_V(X_S) - E_{Fp}(X_S))/kT] - p(X_n) + N_D \frac{q\psi_S}{kT} \}^{1/2} \tag{2.16}$$

where $p(X_n)$ and $n(X_n)$ are the hole and electron concentrations at the boundary of the space charge region and the quasi-neutral base.

All the terms in expressions (2.7) and (2.9) can be evaluated by knowing both ψ_S and ϕ. After postulating initial values, one can iterate on ψ_S and ϕ until the two boundary conditions (2.7) and (2.9) are met, In this way the currents J_{VM} and J_{CM} for a given applied voltage V can be computed.

2.2 The MIS BJT model

The model to be discussed assumes a M-I-p/Si-n/Si

structure. The band diagram for such a device operating in the active mode, is shown in Fig. 2.2. The model for the MIS BJT is very similar to the MIS junction diode model. In fact, the MIS BJT model is merely an extension of the MIS junction diode model, with a few additional current components.

A few assumptions were made, in order to keep the model simple and to make it easy to study the device sensitivity to various parameter changes. The assumptions are that the base region is uniformly doped and contains a quasi-neutral region during operation, and that both high level injection and series resistance effects can be ignored.

The current components for the model (shown in Fig. 2.3) include those used in the MIS junction diode model, and the new currents J_{REC}, $J_n(0)$, $J_n(W_b)$, J_{RE}, J_{GEN}, and J_{CBP}.

J_{REC} is the recombination current in the base-emitter space charge region, such that

$$J_{REC} = \frac{q\, W_{BE}\, n_i}{2\, \tau_n} \left[\exp\left(q\phi / 2kT\right) - 1\right] \qquad (2.17)$$

where W_{BE} is the depletion width of the base-emitter junction, and τ_n is the electron life time.

$$W_{BE} = \left(2\epsilon_S \psi_S / qN_A\right)^{1/2} \qquad (2.18)$$

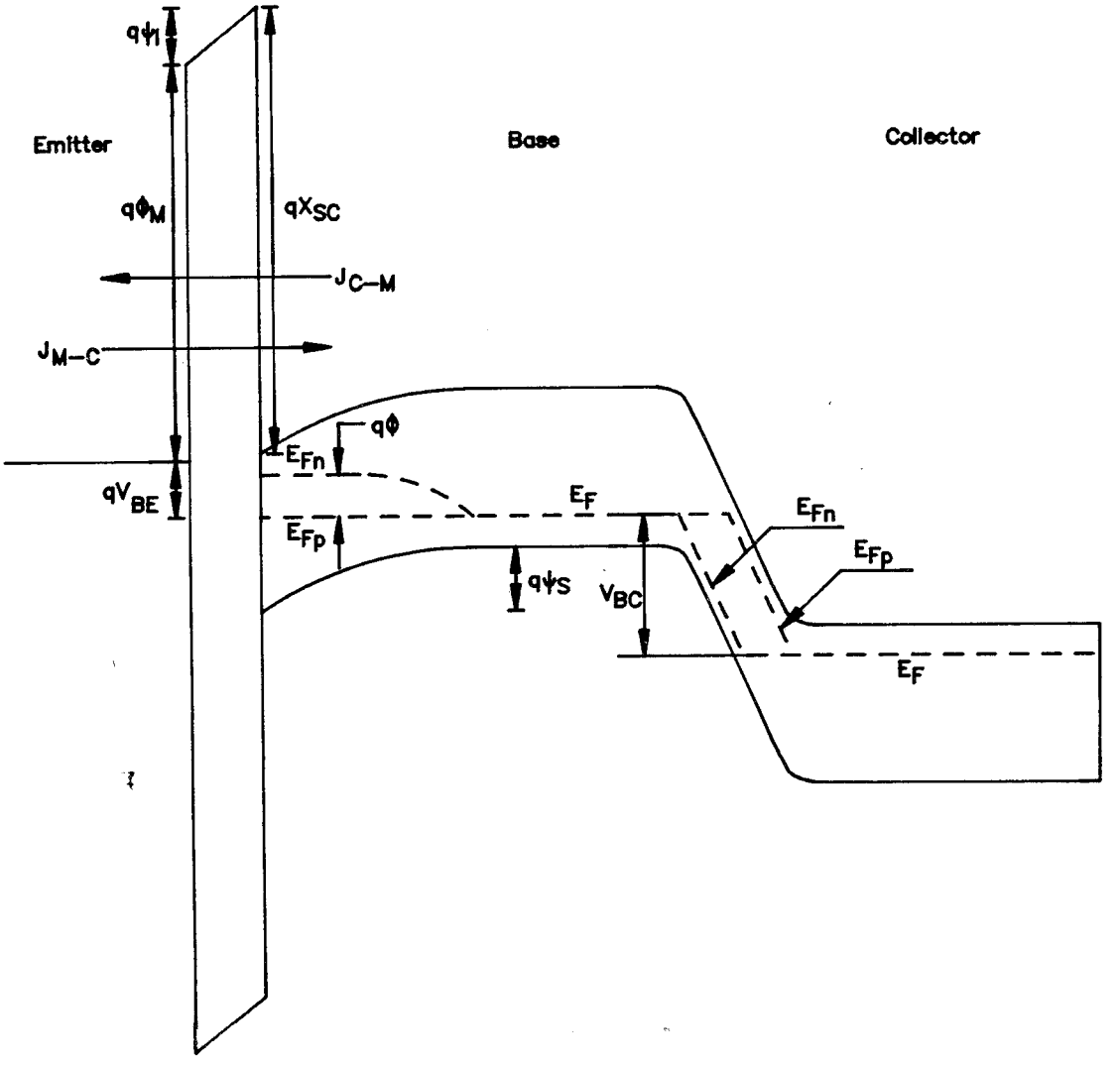


Fig. 2.2. Band diagram of MIS BJT

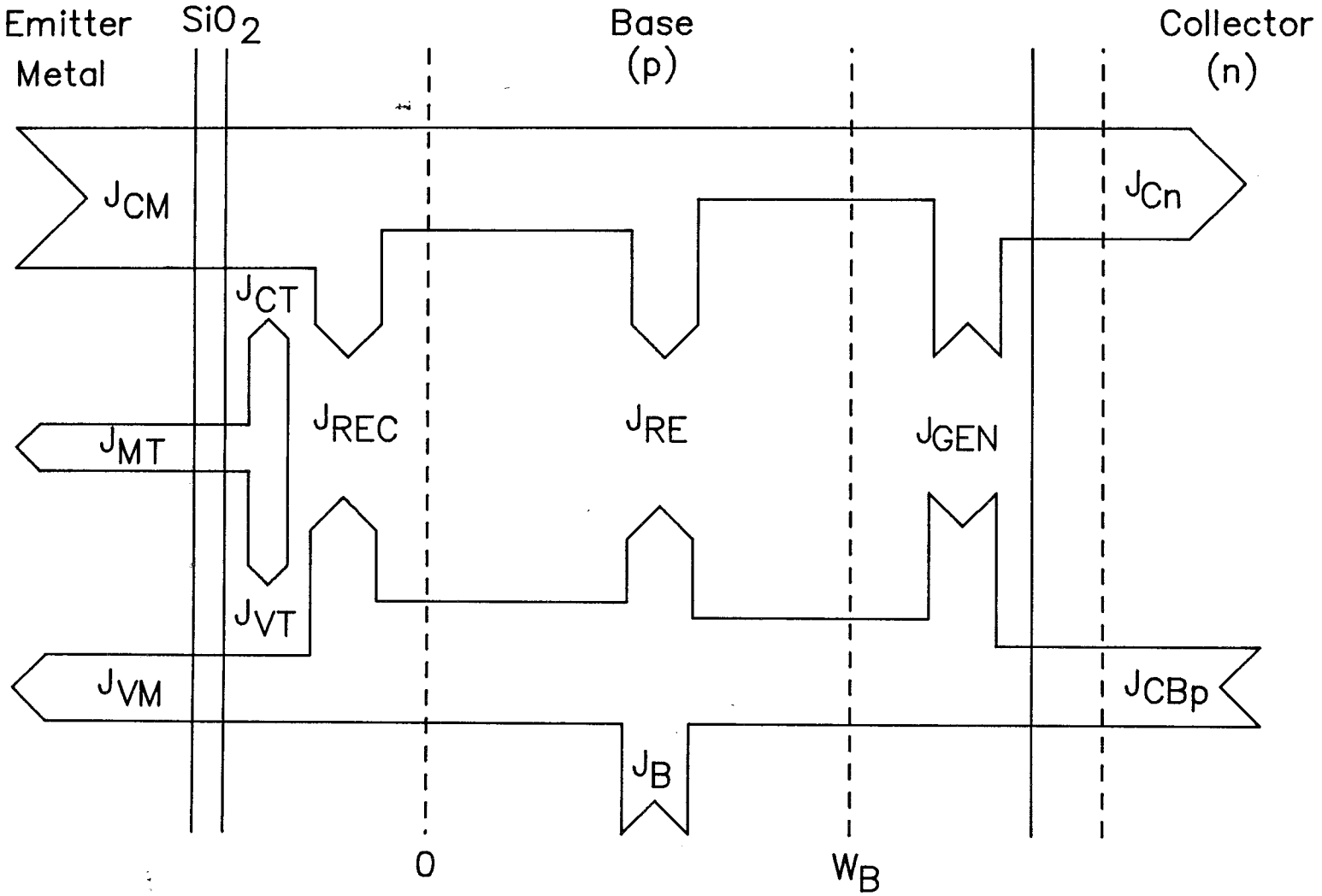


Fig. 2.3. Current components of the MIS BJT

The currents, at both boundaries of the neutral base are represented by $J_n(0)$, the current at the emitter boundary, and $J_n(W_B)$, the current at the collector boundary. The expressions for $J_n(0)$ and $J_n(W_B)$, can be found by solving the continuity equation with no drift current component for a uniformly doped base.

$$\frac{dn}{dt} = - \frac{\delta n_B(x)}{\tau_n} + D_n \frac{\partial^2 n_B(x)}{\partial x^2} = 0 \qquad (2.19)$$

where n is equal to the minority carrier concentration in the base region, δn_B is the excess minority carrier concentration, and D_n is the minority carrier diffusion constant in the base region. The solutions for the continuity equation are as follows:

$$J_n(0) = \frac{q\, D_n\, [\delta n_B(0)\, \cosh(W_{Beff}/L_n) - \delta n_B(W_B)]}{L_n\, \sinh(W_{Beff}/L_n)} \qquad (2.20)$$

and

$$J_n(W_B) = \frac{q\, D_n\, [\delta n_B(0) - \delta n_B(W_B)\, \cosh(W_{Beff}/L_n)]}{L_n\, \sinh(W_{Beff}/L_n)} \qquad (2.21)$$

where the expressions for the excess carrier concentrations at the boundaries of the base region, and the effective base width are as follows:

$$\delta n_B(0) = n_{B0}\, (\exp(q\phi\ /\ kT) - 1) \qquad (2.22)$$

$$\delta n_B(W_B) = n_{B0}\, (\exp(qV_{BC}\ /\ kT) - 1) \qquad (2.23)$$

$$W_{Beff} = W_B - W_{BC} - W_{BE} \qquad (2.24)$$

where W_{BC} is the base-collector depletion width in the base

region, and is expressed by

$$W_{BC} = (2\epsilon_S (V_{bi} - V_{BC}) / q N_A)^{1/2} \quad (2.25)$$

The difference between $J_n(0)$ and $J_n(W_B)$ is equal to the recombination current within the neutral base J_{RE}, hence:

$$J_{RE} = J_n(0) - J_n(W_B) \quad (2.26)$$

The current components contributed by the reverse biassed base-collector junction are J_{GEN} and J_{CBP}, where J_{GEN} is the generation current within the base-collector space charge region and J_{CBp} is the reverse bias saturation current of the junction.

$$J_{GEN} = \frac{q\, n_i\, W_{CB}}{(\tau_n\, \tau_p)^{1/2}} \quad (2.27)$$

and

$$J_{CBp} = \frac{q\, D_p\, n_i^2}{(D_p \tau_p)^{1/2} N_D} \quad (2.28)$$

where D_p, τ_p and τ_n are model parameters that represent the diffusion constant for holes, and the effective lifetimes for holes and electrons respectively. W_{CB} is the total width of the base-collector depletion region, expressed by:

$$W_{CB} = \left[\frac{2\epsilon_S}{q} \left(\frac{N_A + N_D}{N_A\, N_D}\right) (V_{bi} + V_{CB})\right]^{1/2} \quad (2.29)$$

The minority carrier current component at the boundary of the semiconductor and insulator, $J_n(X_S^+)$ is now given by:

$$J_n(X_S^+) = J_{REC} + J_n(0) \tag{2.30}$$

The two boundary conditions for the MIS BJT model are then:

$$- V_{BE} - \phi_M - \psi_I + \chi_{SC} - \psi_S + \phi_0 = 0 \tag{2.31}$$

and

$$J_{CM} - J_{CT} = J_n(0) + J_{REC} \tag{2.32}$$

Once again, the model can be solved by iterating both ψ_S and ϕ, until the two boundary conditions are met. The emitter, base, and collector currents are then:

$$J_E = J_{CM} + J_{VM} + J_{MT} \tag{2.33}$$

$$J_B = J_{VM} - J_{VT} + J_{RE} + J_{REC} - J_{CBp} - J_{GEN} \tag{2.34}$$

$$J_C = J_N(W_B) + J_{GEN} + J_{CBp} \tag{2.35}$$

2.3. Model Calculation

The theoretical MIS BJT model was tested, using parameters listed in Table 2.1. The values for N_A and N_D were obtained by approximating the simulated doping profile of the experimental device MR-20 (refer to section 4.3.) using SUPREM II by uniformly doped regions. The electron affinity and the metal work functions for Al and Mg were obtained from the literature, together with the diffusion constants D_n and D_p, and the effective Richardson constants A_e and A_h [16]. The effective lifetimes τ_n and τ_p were approximated from previous life time measurements of similar

Parameter		Value
Substrate Doping Density	(cm^{-3})	4.0×10^{16}
Neutral Base Doping Density	(cm^{-3})	1.5×10^{15}
Silicon Valence Band Energy	(eV)	3.73*
Metal–Insulator Barrier Height	(eV)	
Aluminum		4.80*
Magnesium		5.55*
Electron Effective Mass in Insulator		0.65 m_e
Insulator Band Gap	(eV)	8.0
Insulator Thickness	($\mathring{A}$)	10
Density of States Ratio	(N_C / N_V)	0.372
Effective Richardson Constant		
Electrons	($A-cm^{-2}{}^{o}K^{-1}$)	45
Holes	($A-cm^{-2}{}^{o}K^{-1}$)	78
Carrier Lifetime		
Electron	(uS)	6
Holes	(uS)	6

*: These energies are measured with respect to the insulator valence band.

Table 2.1. Nominal Parameters used for MIS BJT Model Calculations.

devices [17], and the oxide thickness was also approximated from previous observations [2].

However, neglecting the series resistance, and high injection level effects does raise some problems regarding the usefulness of the device sensitivity studies. The emitter current will increase without bound as the oxide thickness or the metal work function is decreased. This problem was solved by using an external series resistance model in conjunction with the MIS BJT model. The series resistance model simply makes the approximation that I_E is equal to I_C and then calculates the effective V_{BE} by subtracting the voltage drop across the series resistance from the applied V_{BE}.

2.3.1. Effect of oxide thickness

The ultra thin layer of tunneling oxide is the key factor in achieving high gain in a MIS BJT device. Any change in oxide characteristics is likely to have a direct influence on the device behavior. One of the most important parameters of the oxide, is the oxide thickness. It is so thin that it is very sensitive to processing conditions and oxide reduction by the overlaying metal.

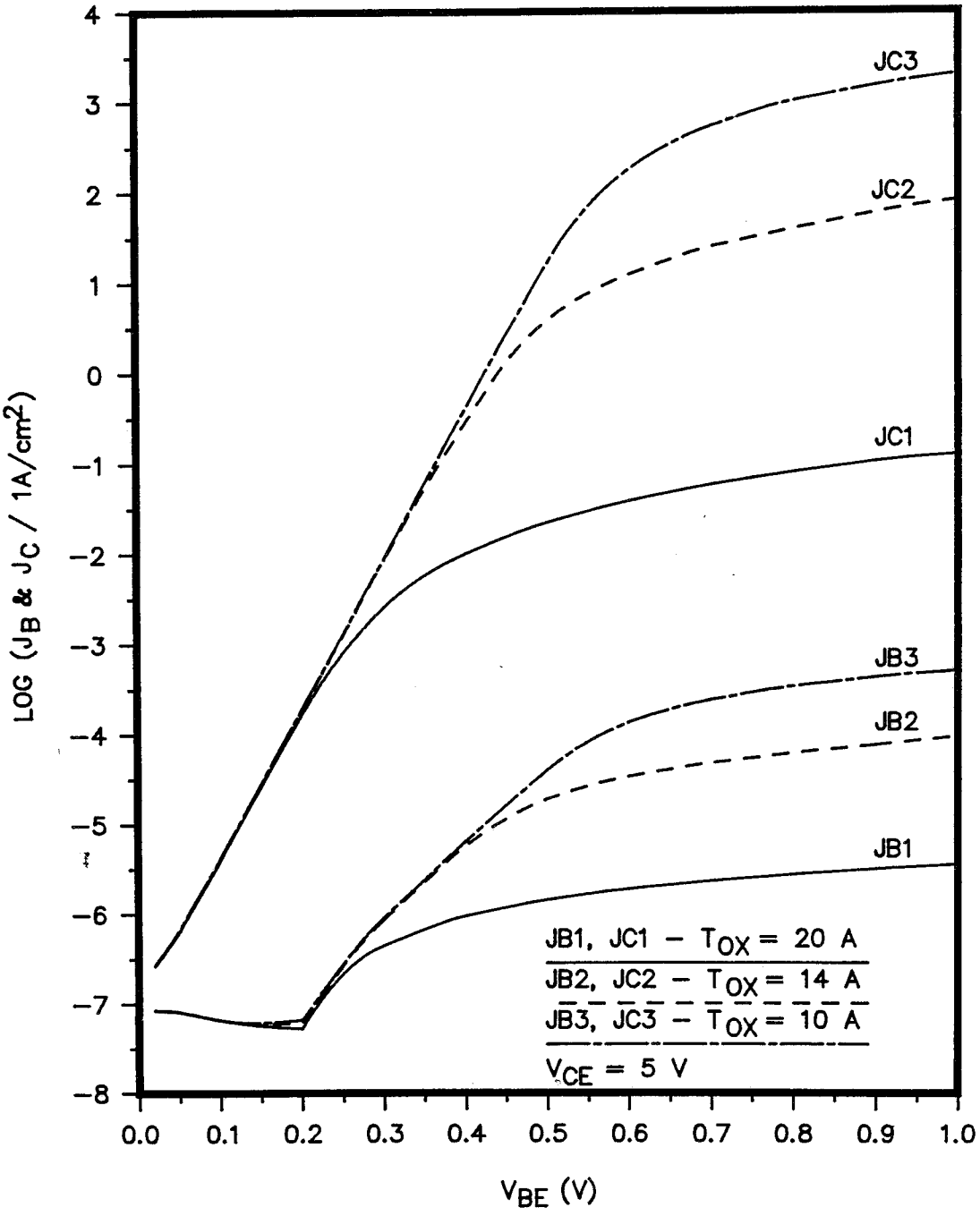
The effect of change in oxide thickness was investigated using the MIS BJT model. The model shows that

the gain of the device would increase without bound as the oxide thickness is reduced. This is due to the fact that the model assumes a perfect layer of oxide and both the high level injection and series resistance effects are ignored. A thinner layer of oxide would enhance the tunneling probabilities for both carriers leading to higher limiting currents, but as long as the oxide continues to passivate the semiconductor surface, the back injected hole current will still be orders of magnitude below that of the electron injection current.

In reality, the gain of the device cannot be increasing without bound, as the current density will be limited by series resistance and high level injection effects. An external series resistance model was used to get more realistic results for the MIS BJT model. The simulated results with series resistance (shown in Fig. 2.4 & 2.5) show that the gain of the device is still increasing but at a much slower rate and is not going to be unbounded.

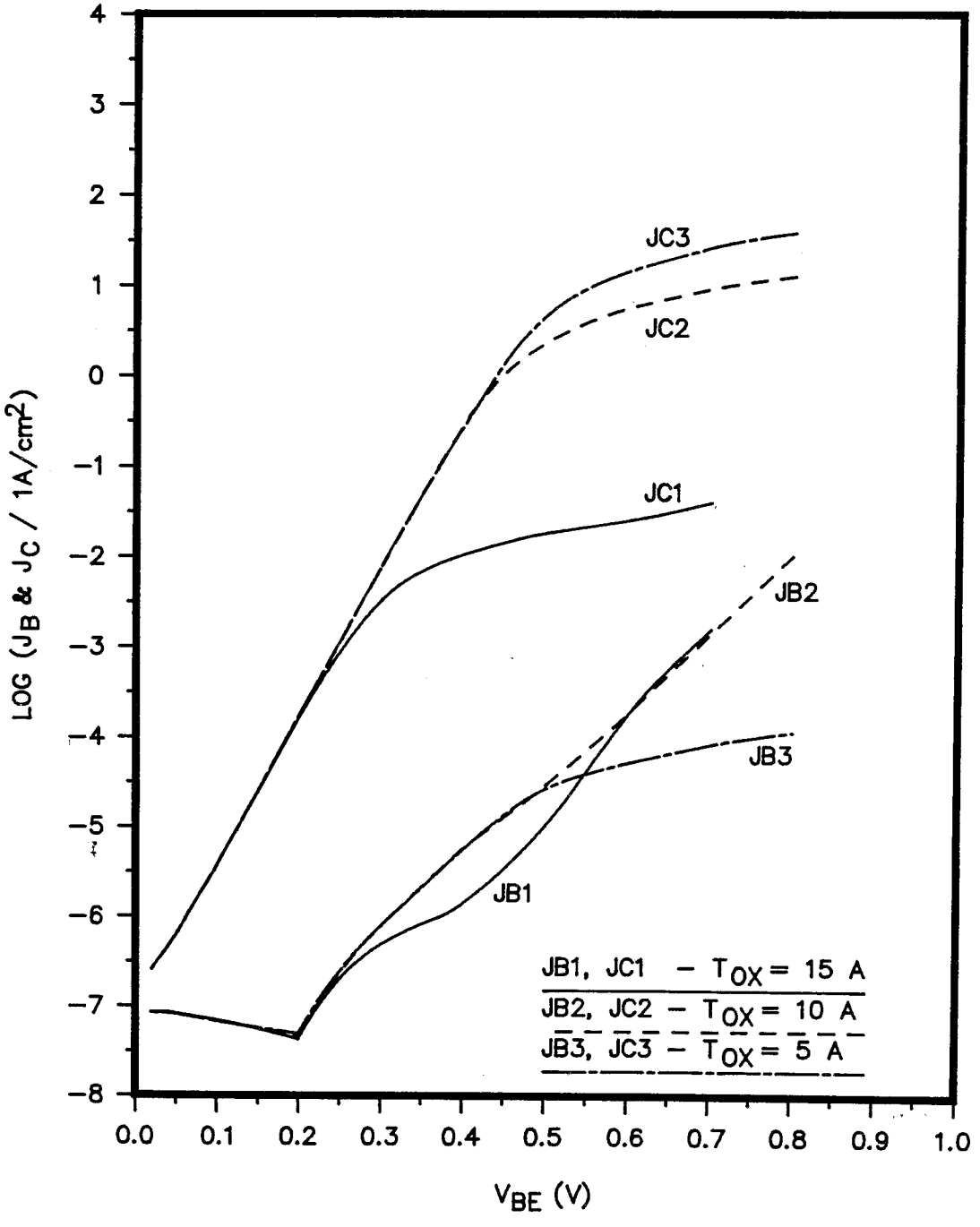
From the simulated results, one can see that the device is not going to suffer from reduction of oxide thickness, as long as the oxide keeps its property of passivating the semiconductor surface.

2.3.2 Effect of carrier lifetime



Simulated with series resistance of 500 Micro Ohm–cm^2

Fig. 2.4. Effects of Oxide thickness on Mg–I–Si transistor



Simulated with series resistance of 500 Micro Ohm−cm^2

Fig. 2.5. Effects of oxide thickness on Al−I−Si transistor

The carrier lifetime in the base region is another important factor in high performance MIS BJTs. A short carrier lifetime would increase both the recombination currents in the base-emitter space-charge region and neutral base region. This would in turn increase the base current and decrease the gain of the device.

The MIS BJT model was used to investigate the effect of change in carrier lifetime. The model result (shown in Fig. 2.6) clearly shows an increase in base current in the low bias region as the minority carrier lifetime decreases. This is consistent with the argument of increasing base recombination current, since the recombination dominated region for a BJT is at the low bias region. However, the base currents at the higher bias region are virtually the same for the range of carrier lifetimes investigated. This is because the base current at high bias regions is dominated by the holes back-injected into the emitter rather than the holes participating in the recombination process in the base.

2.3.3 Effect of metal work function

For low and moderate values of forward bias, the total electron current is small compared to its two components (i.e. J_{MC} from metal to semiconductor and J_{CM} from semiconductor to metal). This state of quasi-equilibrium

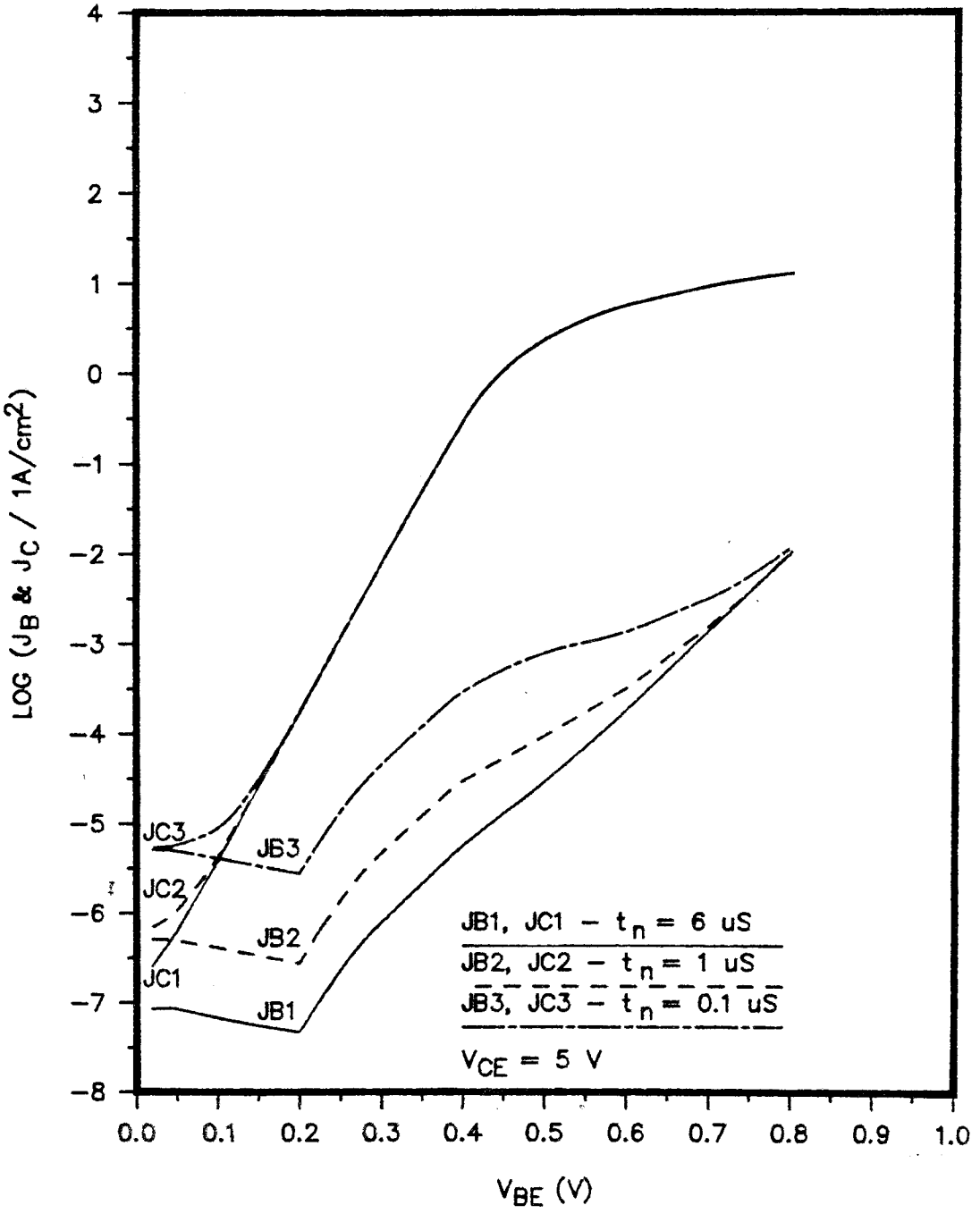


Fig. 2.6. Effects of carrier lifetime on Al–I–Si transistor

keeps E_{Fn} pinned close to E_{Fm}. However, for large currents there is an appreciable energy difference between these two Fermi levels, therefore the total applied base-emitter bias voltage will appear partially across the interfacial oxide. This would cause the device characteristics to deviate from an exponential dependency on the applied bias. Metals with different work functions will produce different surface carrier concentrations on the same semiconductor substrate and so will cause the device to enter the tunneling limited regime at different current densities [17].

The simulated result (shown in Fig. 2.7) shows that metals with higher work function would produce less surface inversion and would in turn lead to entry into the tunnel limited regime at a lower emitter current density. Note that this effect is similar to that resulting when series resistance is present. No series resistance was included in this simulation. The precise values of ϕ_M chosen, represent the ϕ_M of metals that have extremely low work function (2.3 eV), Mg (3.35 eV) and Al (4.4 eV).

2.4. Chapter Summary

The predicted results appear to be reasonable in as much as they give realistic Gummel plots. As expected, high gain devices with p-type bases must have thin oxides, long electron lifetimes and employ metals with low work

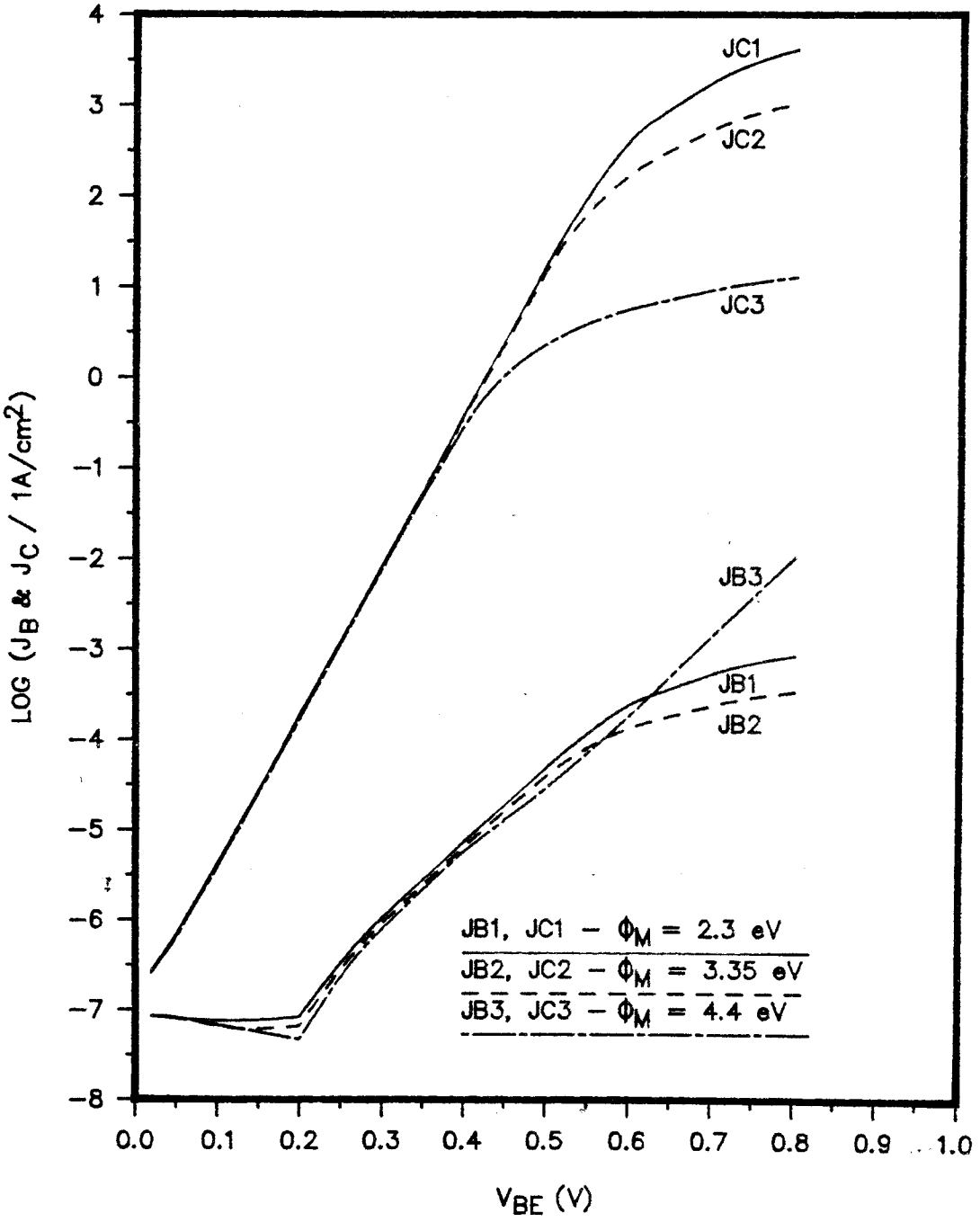


Fig. 2.7. Effects of metal work function on M–I–Si transistor

functions.

Chapter 3

Preliminary Experiments

3.1 Choice of metal

The dominating current transport carriers in a MIS junction can be determined by the combination of doping density of the semiconductor and the work function of the metal. The band diagram of a MIS junction with a n-type semiconductor and a low work function metal that causes accumulation at equilibrium is shown in Fig. 3.1a. Fig. 3.1b shows a MIS junction with a low work function metal and p-type semiconductor. This combination causes inversion of the semiconductor surface at equilibrium. It can be seen that any junction that is accumulated will have a large barrier height for its minority carriers (ϕ_{Bp} in this case) causing the majority carrier to dominate the current transport process. However, the MIS junctions that cause inversion of the semiconductor surfaces will have a small barrier height for minority carriers and a large barrier height for the majority carriers (ϕ_{Bn} and ϕ_{Bp} respectively in this case), allowing minority carriers to dominate the current transport process.

In order to optimize the performance of a silicon MIS BJT, electrons should be chosen as the dominating carrier

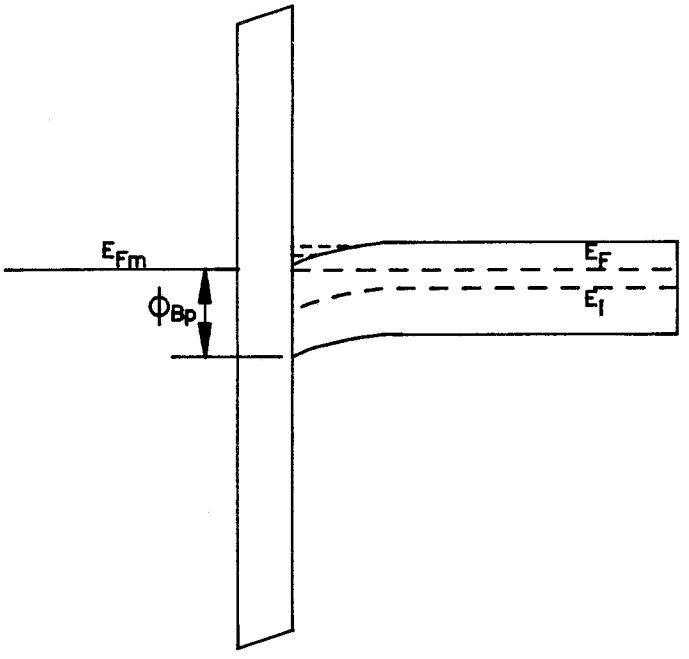


Fig. 3.1a. Band diagram of a MIS junction that causes accumulation

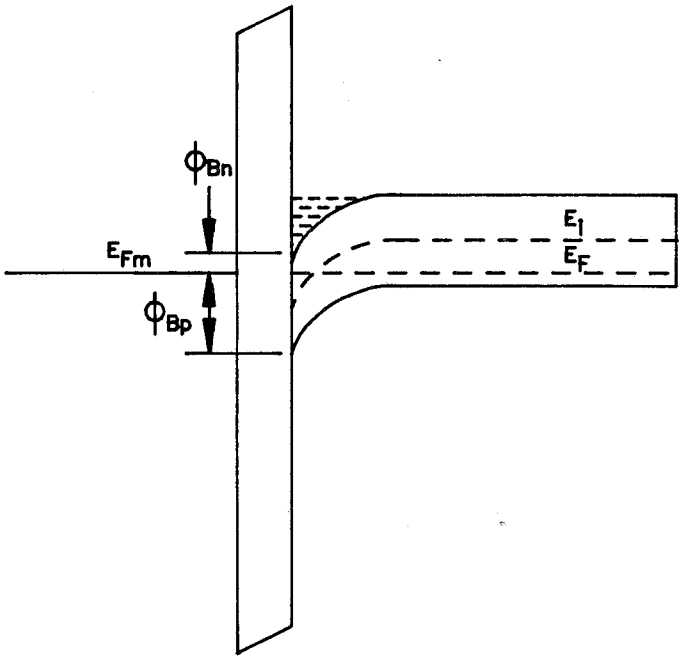


Fig. 3.1b. Band diagram of a MIS junction that causes inversion

because of their higher diffusivty as compared to holes. This will call for a M-I-p/Si-n/Si structure. Furthermore, the metal must have a low work function to invert the p-type base region, so that the relatively low barrier height for electrons will allow electrons to be easily injected into the base while blocking the back-injected holes through the high majority carrier barrier. The work function of the metal must be smaller than the effective work function of the intrinsic base, therefore the work function must be less than the intrinsic Fermi level.

$$\phi_M < \phi_{Si} \simeq \chi_{Si} + E_g/2 = 4.61\text{eV} \qquad (3.1)$$

Several good choices of emitter metal from the point of view of work function would be Al, Ti, and Mg, since their work functions are all less than 4.61eV. However, the practical usefulness of devices made from these materials needs to be investigated. There have been several reports of degradation of tunnel junction diodes made with Al [13]. Mg is well-known to be very reactive and unstable [18]. While the Al metalization process is well established, Ti is a more stable metal leading to potentially more reliable devices.

MIS diodes with the three selected metalizations were fabricated to verify whether the combinations of metal work functions and semiconductor doping densities were inverting

the semiconductor surface, and performing properly like pn junction diodes.

3.1.1 Fabrication of Al-I-S and Ti-I-S diodes

Four boron doped, <100> orientated wafers with nominal resistivity of 0.1 Ω-cm, 1 Ω-cm, 2 Ω-cm and 10 Ω-cm were cut into quarter wafers. Dot diodes were then fabricated simultaneously with quarters from each of the four different resistivity wafers, in order to investigate the effect of different doping densities. The structure of the dot diodes is shown in Fig 3.2.

Groups of four quarter wafers were cleaned by following the standard RCA cleaning procedure [19]. Once the quarter wafers were cleaned, back contacts of aluminum were formed by evaporation of Al in a CHA vacuum chamber at a pressure of around 4×10^{-6} Torr. The back contacts were sintered at the same time as the growth of the ultra thin tunneling oxide in a quartz tube furnace. The oxide growth step required 5 minute warm-up and cool-down periods at 500°C with a nitrogen flow of 1L/min. The actual oxide growth period was between the warm-up and cool-down periods at 500°C with an oxygen flow of 1L/min for 20 minutes [20]. The oxide thickness for such a procedure was estimated to be around 15 Å. The barrier metals were formed by evaporating the desired metal onto the front of the wafers, with a

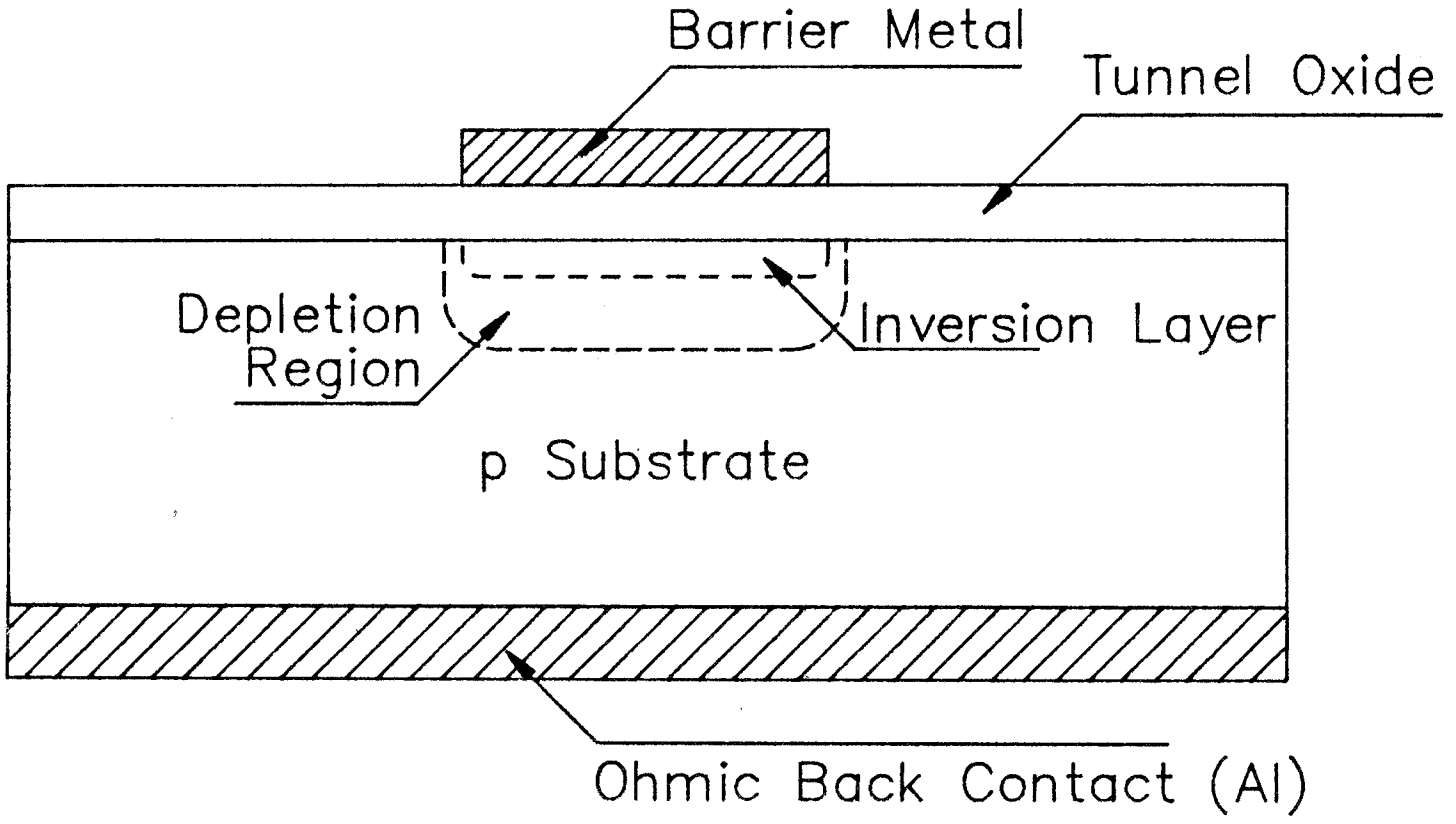


Fig. 3.2. Structure of the MIS dot diodes

shadow mask placed in between the wafers and the evaporation source. The nominal area of the dot diodes was 0.01 cm^2.

Problems were encountered during the evaporation of Ti. The CHA evaporation power supply can only supply filament current in the order of 100 A maximum, which is not enough to evaporate the Ti at an acceptable rate of deposition. The prolonged period of evaporation at an extremely high temperature caused the Ti contact to be oxidized, producing a deposit of dark black color. The resulting film was 1500 Å thick and was found to have a very high resistivity. A Veeco vacuum system, which was capable of supplying a higher current (150A), was also used to produce a second set of Ti diodes. However, this approach did not seem to help reducing the oxidation of Ti and hence did not reduce the metal resistivity.

The Al metalization was performed in the CHA chamber, and did not lead to any oxidation problem, due to its relatively high vapor pressure. The rate of deposition can be easily adjusted to give an acceptable deposition time without overheating the substrate. The thickness of the Al film was chosen to be 3000 Å in order to reduce the metal resistance [20].

3.2 Emitter metal patterning

The shadow mask method is perhaps the best method to pattern the barrier metals for large MIS junctions. The method patterns the metal at the same time as the deposition of the metal, hence eliminating the possibility of damage to the underlying tunneling oxide by any further processing steps. However, the shadow mask method runs into a lot of problems when a fine metal pattern is required and alignment of the metal pattern to previous structures is critical. Photolithography provides a second means of patterning the emitter metal. Currently there are two photolithrography schemes available, namely the lift-off technique and the direct patterning technique. The lift-off technique can eliminate the over etching effects, which can occur with direct etching, and will work on any metal without having to worry about the choice of etchants. However, lift-off has a major drawback in producing MIS junctions. The lift-off method requires the photoresist to be patterned before metal deposition. This extra processing step could lead to possible damage and contamination of the underlying tunneling oxide. Therefore, the direct patterning method is preferable in MIS junction fabrication.

Direct patterning of Al is well-established. The commonly used phosphoric acid is a safe etchant, since it

will etch off the Al without causing any damage to silicon and silicon oxides. Acceptable etch rates can be achieved by using diluted (1:1) H_3PO_4 with DI water when heated to 60°C. The etch rate for such an etchant is approximately 300 Å/Min.

Patterning Mg, however, is a much more difficult task than patterning Al. The highly reactive Mg reacts violently with many common etchants, leading to complete removal of the Mg contact. The right choice of etchant and the optimal concentrations must be determined, in order to fabricate high performance Mg-I-S devices. Despite the fact that the lift-off technique of patterning could lead to possible damage and contamination of the tunneling oxide, publications [3,4] have recorded working MIS BJT fabricated with the lift-off technique of patterning the emitter metal.

Two silicon wafers were used to study and optimize the Mg patterning procedure. The p-type 10 Ω-cm <100> oriented wafers were cleaned using the RCA cleaning procedure. 3600 Å of Mg were deposited on the front of the wafers, using a "Drummel" type tantalum boat as the evaporation source in the CHA vacuum chamber with a pressure of $2x10^{-6}$ Torr and deposition rate of around 10 Å/Sec. Positive photoresist (Shipley HR316) was spun onto the wafers followed by a soft bake to dry out the photoresist. The emitter mask (Fig. 3.3)

for the MIS BJT experiment was used to pattern the photoresist using a Karl Seuss model 505 maskaligner. Once the wafers were developed and hard baked, they were scribed into quarters for studying the Mg etching process.

Nitric acid was chosen to be the etchant for Mg, because it is commonly used in commercial Mg etching for producing press dyes [21]. A number of different concentration HNO_3 solutions was used to try to optimize the Mg etching process. It was found that a 0.1 % solution gave a satisfactory etch time of 3 minutes with minimal amount of overetching. Any solution with a higher concentration was found to lead to significant overetching. With extreme care device structures with dimensions in the order of 1 μm can be patterned by using the 0.1 % etchant solution.

Ti patterning can be done by using low concentration HF solution. The Ti etching process was not studied until the actual Ti-I-S emitter transistor fabrication, where a 1 % HF solution was used. Although the Ti emitter was underetched, the devices seemed to suffer from some loss of the ultra thin layer of tunneling oxide. This is most likely due to the fact that the etch rate of silicon oxides in HF solution is much faster than that for Ti. Further study must be made concerning Ti patterning, if improvements in the performance of Ti-I-S devices are to be made.

3.2.1. Fabrication of Mg-I-S diodes

A set of Mg-I-S diodes was fabricated using the direct patterning scheme, in order to study the feasibility of producing such junctions with the proposed patterning procedure. Both the structure and the processing steps of the Mg-I-S diodes were similar to that of the Al-I-S and Ti-I-S diodes. The only difference was that the emitter mask (Fig. 3.3) for patterning the emitter metal in the MIS BJT, was used together with the proposed method for patterning the Mg instead of using the shadow mask technique. The 300 μm * 300 μm metal pattern was used as the diode contact.

The wafer used in this experiment was boron doped, p-type with nominal resistivity of 2 Ω-cm and <100> orientation. The processing steps prior to barrier metal deposition were identical to those of the Al-I-S and Ti-I-S dot diodes fabrication. After the thin oxide growth, 3500 Å of Mg was deposited on top of the oxide covering the entire wafer. Then, the Mg was patterned using the technique discussed in the previous section. The resultant Mg contact showed minimal amount of over etching. No noticeable damage to the thin tunneling oxide was found on examining the electrical properties of the diodes.

3.3 Experimental results and discussion

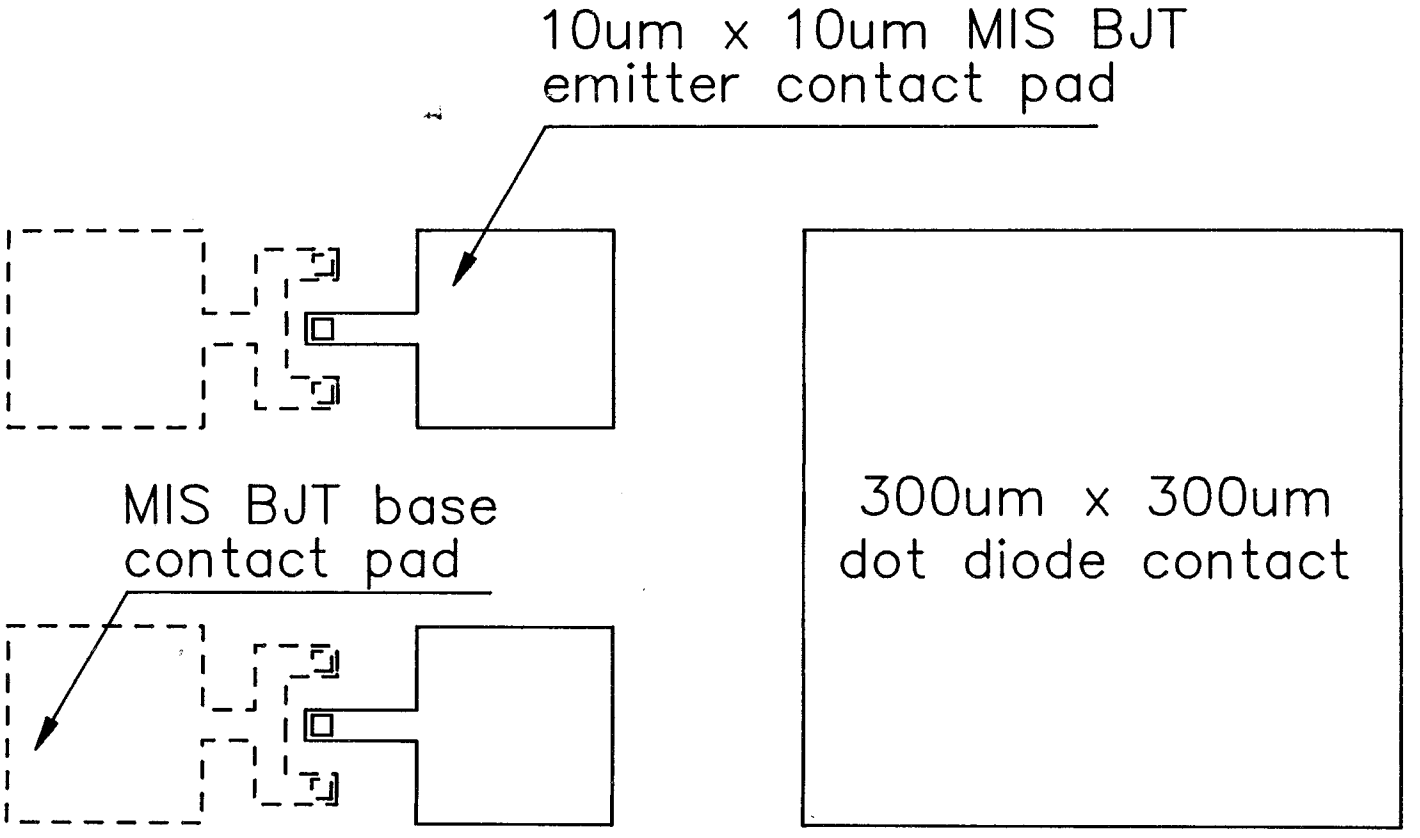


Fig. 3.3. The emitter mask for the MIS BJT experiment

The current-voltage characteristics of the dot diodes made with the three different barrier metals were examined. Observation of an ideal p-n junction characteristic would confirm that these metals were properly inverting the semiconductor surface. Both the Al and Mg diodes were tested using the HP4145 semiconductor parameter analyzer, while the Ti diodes were tested manually with a platinum ball-shaped probe in an attempt to reduce the contact resistance.

In all three cases, the log(J) versus V curves (shown in Fig 3.4 to Fig 3.6) showed typical p-n junction characteristics with a recombination - regeneration dominant region at low bias, a minority carrier injection-diffusion dominant region with ideality factor nearly 1 at the medium biasing range, and finally a tunnel limiting region at high bias. The Al and Ti diodes characteristics were almost identical at both the low and medium biasing range for a given substrate resistivity. This similarity is to be expected because the work functions for the two metals are almost the same. The change in tunnel limiting characteristics for wafers with different substrate resistivities at medium bias was also observed for the Al and Ti diodes. The tunnel limiting current decreases as the substrate doping density increases. The less inverted surface would have less minority carriers available for the

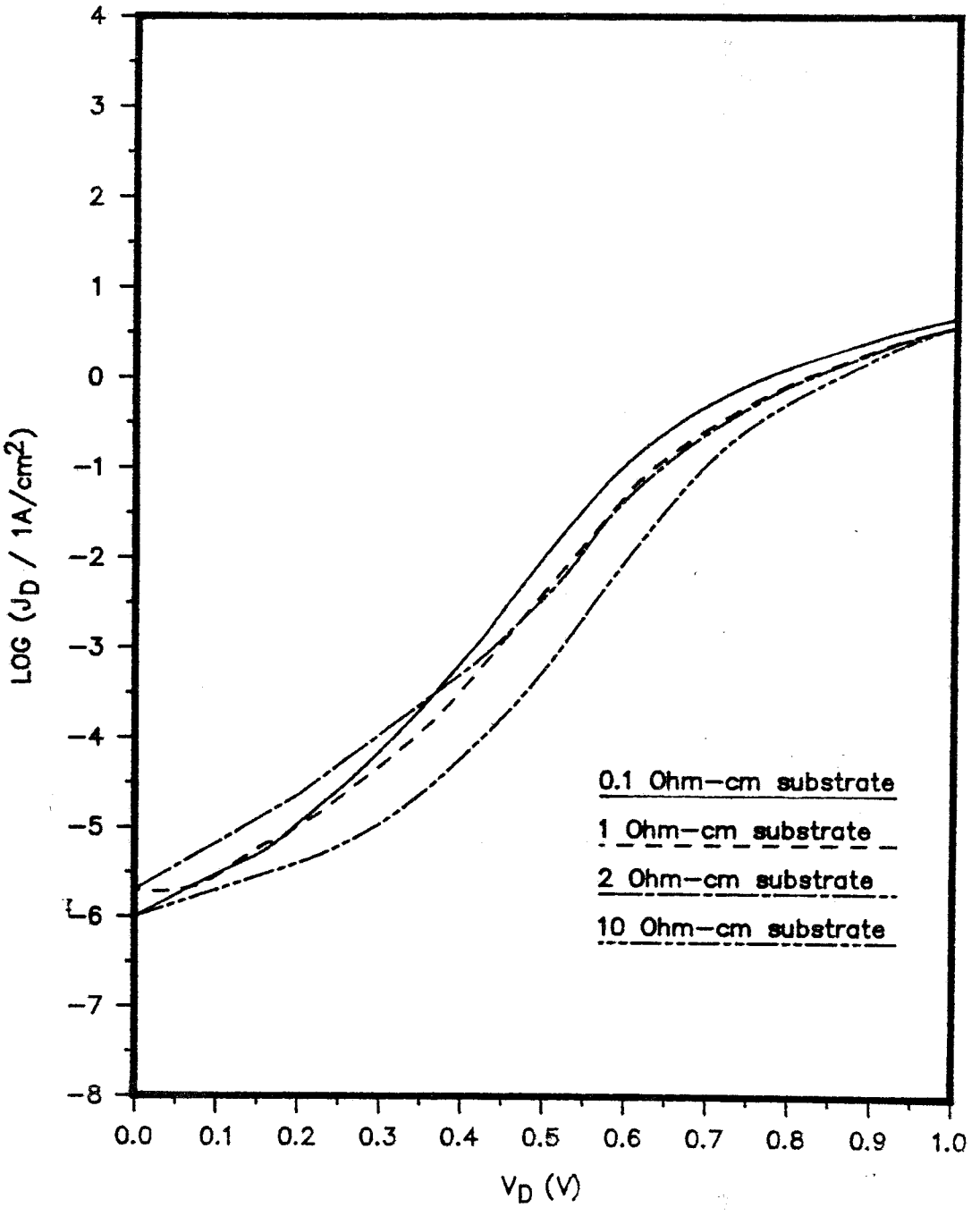


Fig. 3.4. Log(J) vs V curves for the Al−I−Si dot diodes

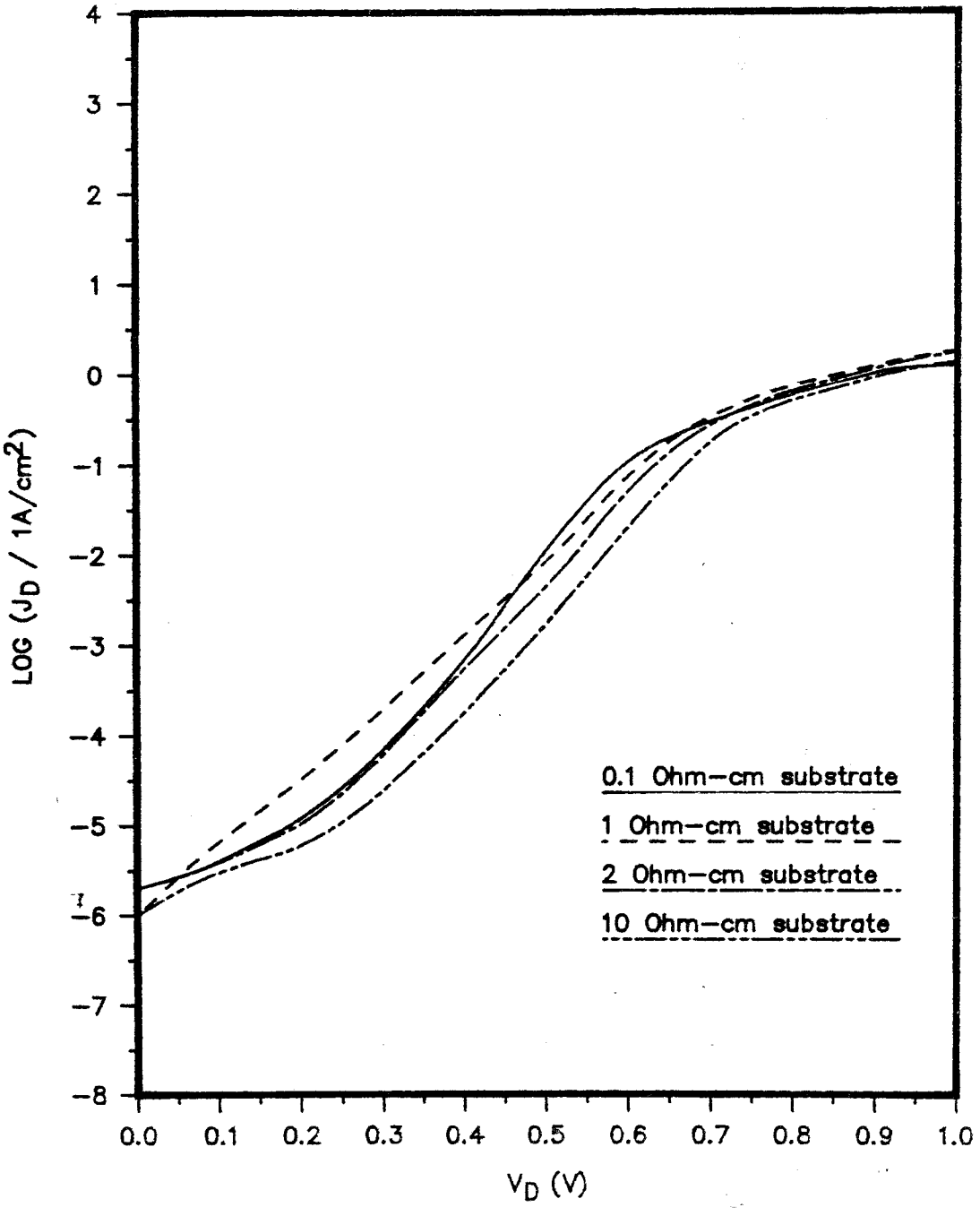


Fig. 3.5. Log(J) vs V curves for the Ti−I−Si dot diodes

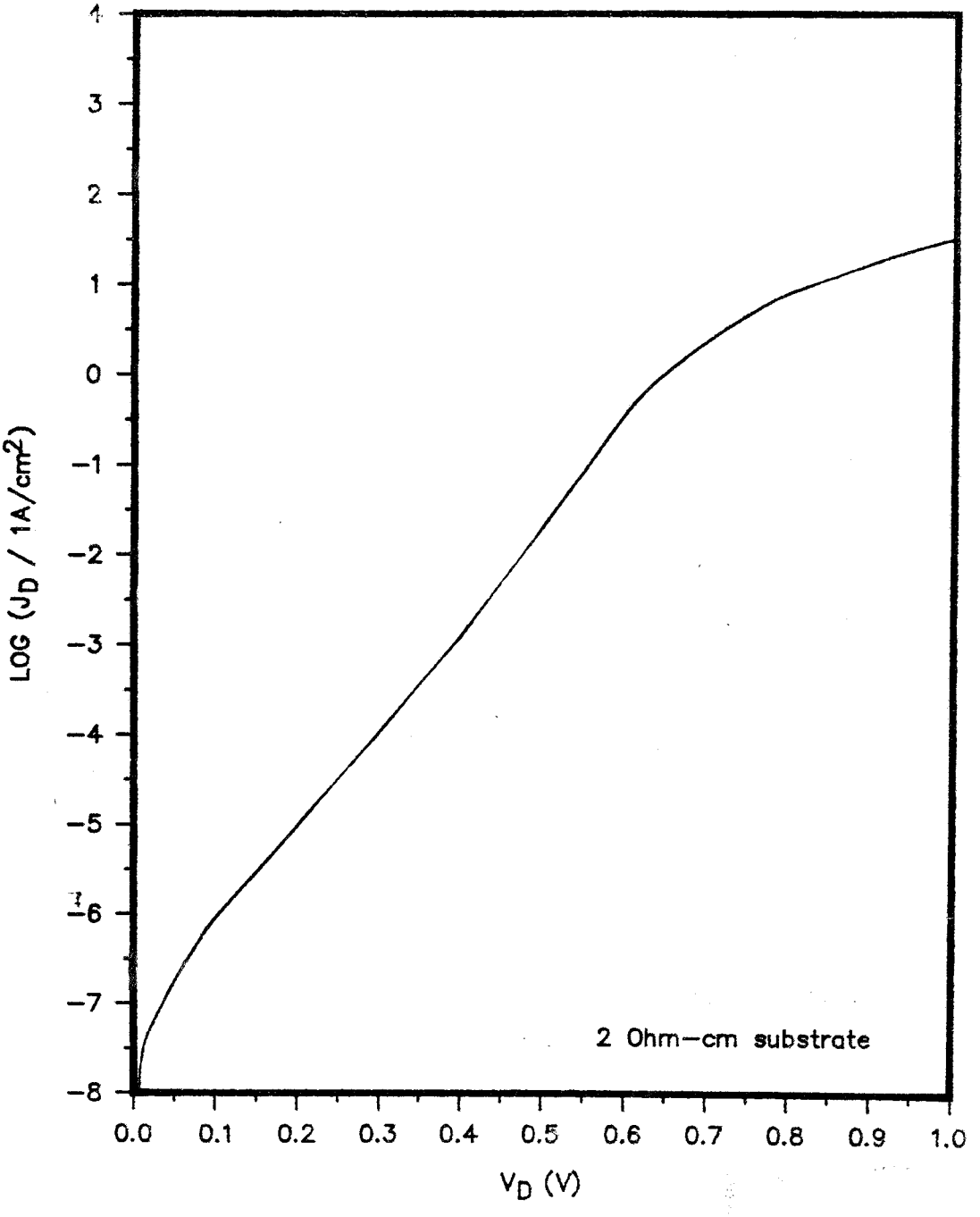


Fig. 3.6. Log(J) vs V curve for the Mg−I−Si diode

bulk diffusion current carrying process, hence the overall current would be decreased. However, this change in characteristics was not observed at high bias, presumably because of high level injection and series resistance effects.

The above results show that the three chosen barrier metals are inverting the p-type silicon properly, thus causing the electron minority carrier current to be the dominant current component. Fabrication of MIS BJTs with direct patterning of both Al and Mg metalization can be achieved with no noticeable damage or contamination to the underlying tunneling oxide. Therefore, no reduction in the performance of MIS BJTs due to surface state effects at the metal and the thin oxide interface should occur. In the case of Ti, the etchant used in the experiment seemed to have damaged the underlying tunneling oxide and caused poor stabilities.

Chapter 4

MIS BJT fabrication

The MIS BJTs used for the MIS BJT experiments, were prepared partly at Carleton University and partly at UBC. The processing steps carried out at Carleton and UBC will be discussed separately in the following sections.

4.1 Overview of processing

N-type, <100> orientated wafers with substrate resistivity of 3-5 Ω-cm were used as the foundation for the M-I-p/Si-n/Si structure transistors (shown in Fig. 4.1). The extrinsic base region was formed by performing a boron diffusion at Carleton University, then the wafers were shipped to UBC for the intrinsic base implantation of boron. The intrinsic base was formed by ion implantation with an implantation energy of 50 keV for the first batch of MIS BJTs and 30 keV for the second with dosage of either $10^{12}cm^{-2}$ or $5x10^{12}cm^{-2}$, then the implanted bases were annealed at 950°C for 30 minutes. The reasons for having two batches of devices was because the first batch of devices exhibited relatively low gains. The doping profile was modified on the second batch to try to improve the device performance. Also, this batch of wafers contained some ready-made polysilicon devices which could be used to compare MIS BJT and polysilicon emitter transistors. The

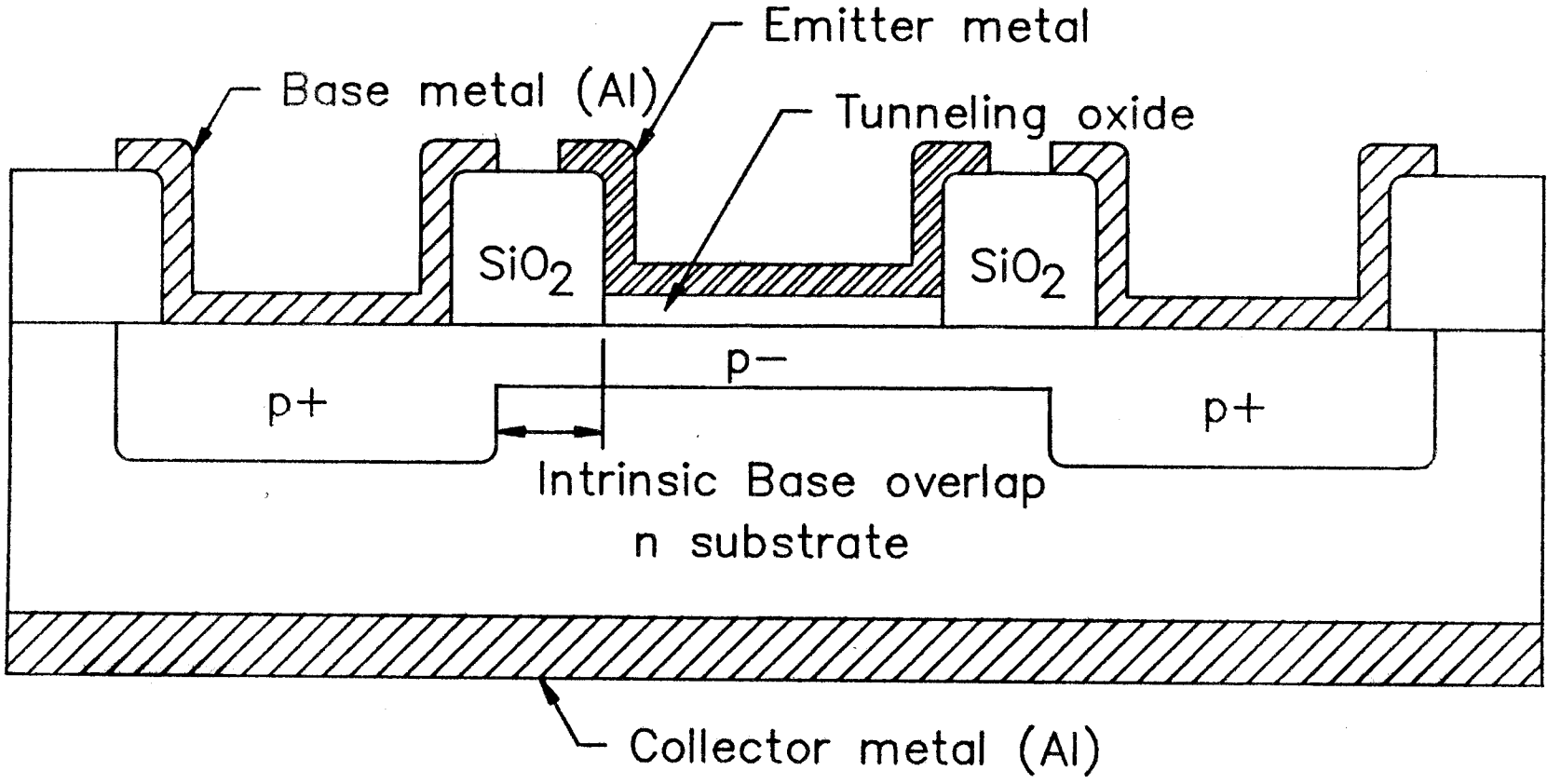


Fig. 4.1. Structure of the MIS BJT showing intrinsic base overlap

doping profiles for the $10^{12}cm^{-2}$ implantations, as computed from SUPREM II simulations are shown in Fig. 4.2. The first batch was labelled GT-G, and the second GT-J.

Once the intrinsic base region was formed, the wafers were shipped back to Carleton. The implantation oxide mask over the base contact window and the emitter contact window region was removed, a layer of Lotox was deposited, and was patterned on the wafer to protect the surface of the emitter contact. The base contact was patterned using the direct patterning scheme as in the emitter contact patterning, after 1 μm of Al was deposited by e-beam evaporation. The patterned contacts were sintered in a hydrogen environment at 450°C for 10 minutes. A second layer of protective Lotox was deposited on top of the entire wafer except for the emitter contact windows. This Lotox layer was intended to protect the structures formed on top of the wafer from any proceeding cleaning steps, while allowing the emitter contact window to be cleaned. The finished wafers were then shipped to UBC for completion of the fabrication of the MIS BJTs.

The remaining processes to complete the MIS BJTs were: deposition of the back collector contact, growth of the thin tunneling oxide and lastly, emitter metal deposition and definition. Before performing any of the above steps, the

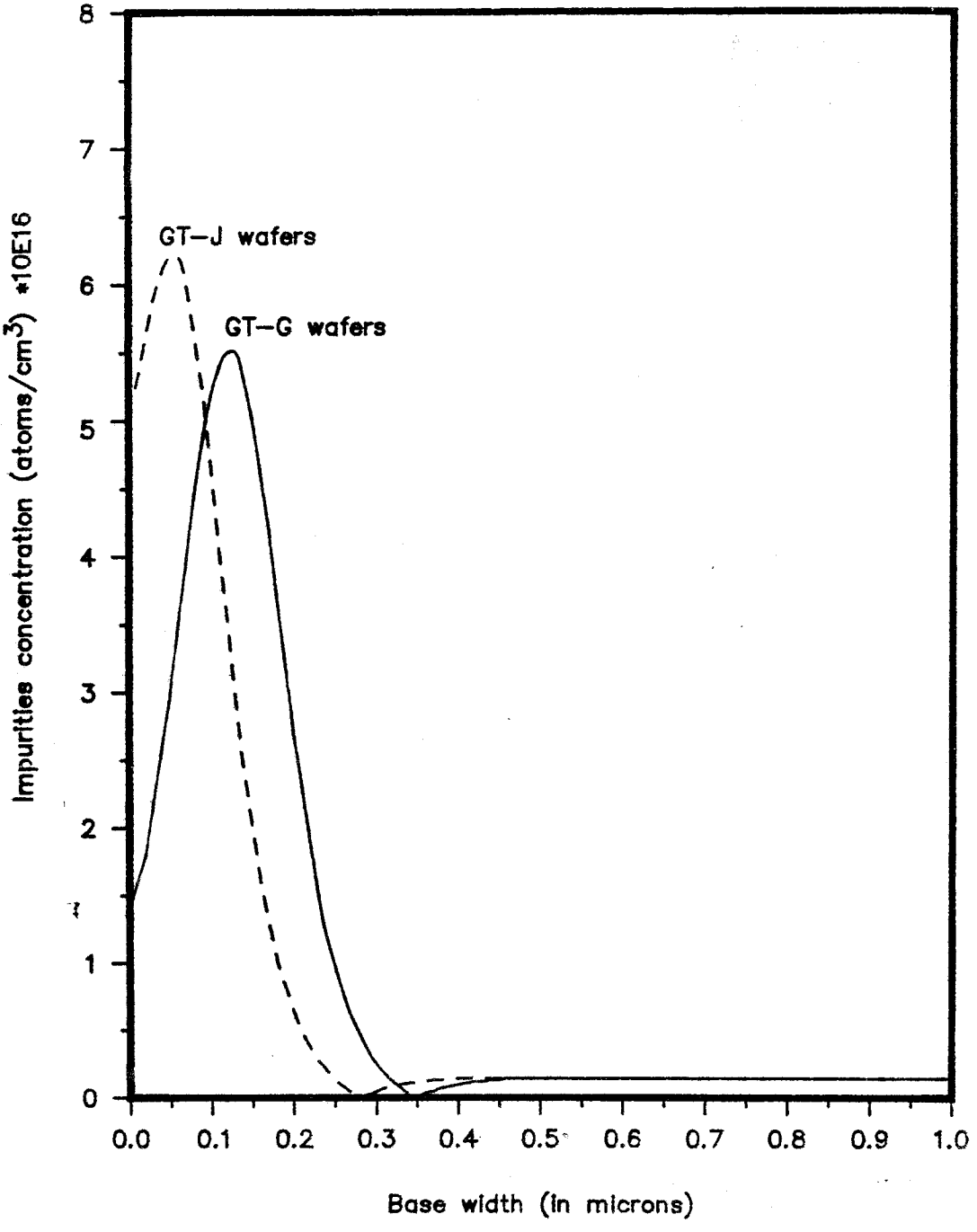


Fig. 4.2. Doping profile of the intrinsic base region

exposed intrinsic base surface had to be cleaned in order to keep the level of contamination low. This is thought to be necessary for reducing the number of surface states and ensuring the growth of a good quality oxide.

4.1.1 Pre-treatment

The pre-treatment step is designed to ensure the cleanliness of the silicon surface of the MIS junction, and remove any native oxide on the silicon surface. The RCA cleaning procedure was used on the first batch of MIS BJTs to perform the pre-treatment step. However, the protective Lotox layer failed to protect the underlying structures during the RCA clean. The base contact metalization was completely removed. A modified RCA cleaning procedure with 1/10 of the cleaning time and leaving the HF cleaning step to the last, was also tried; significant loss of base contact was still observed. In view of these difficulties, the pre-treatment step was reduced to a single 10 second dip in 10% HF.

4.1.2 Collector metal deposition

The MIS BJTs on each wafer shared a common collector which was the substrate itself. Instead of patterning a set of collector contacts on the front of the wafer, a large back contact was used to establish connection to the common collector. 5000Å of Al was deposited on the back of each

wafer using the CHA vacuum chamber. The sintering of the back contact was performed at the same time as the tunneling oxide growth.

4.1.3 Oxidation

The oxidation process for the MIS BJTs was the same as that previously described for the MIS diodes, except that varying the time and temperature of oxidation was investigated. The change in thickness of the tunneling oxide can be observed by its effect on the MIS diode I-V characteristics. A thicker tunneling oxide would lead to higher series resistance, principally due to the decrease in tunnel probabilities.

Three sets of MIS dot diodes with different oxide growth conditions were fabricated and tested to study the effects of oxidation temperature and duration. The oxide growth conditions for these diodes were 500°C for 20 minutes, 500°C for 50 minutes, and 600°C for 20 minutes. The log(J) vs V curves for these diodes (shown in Fig 4.3) showed that the effective series resistance for diodes with lower oxidation temperature was less than that of devices fabricated at higher oxidation temperature. For diodes with the same oxidation temperature but different growth durations, the effective series resistance seemed to have increased as the duration was increased.

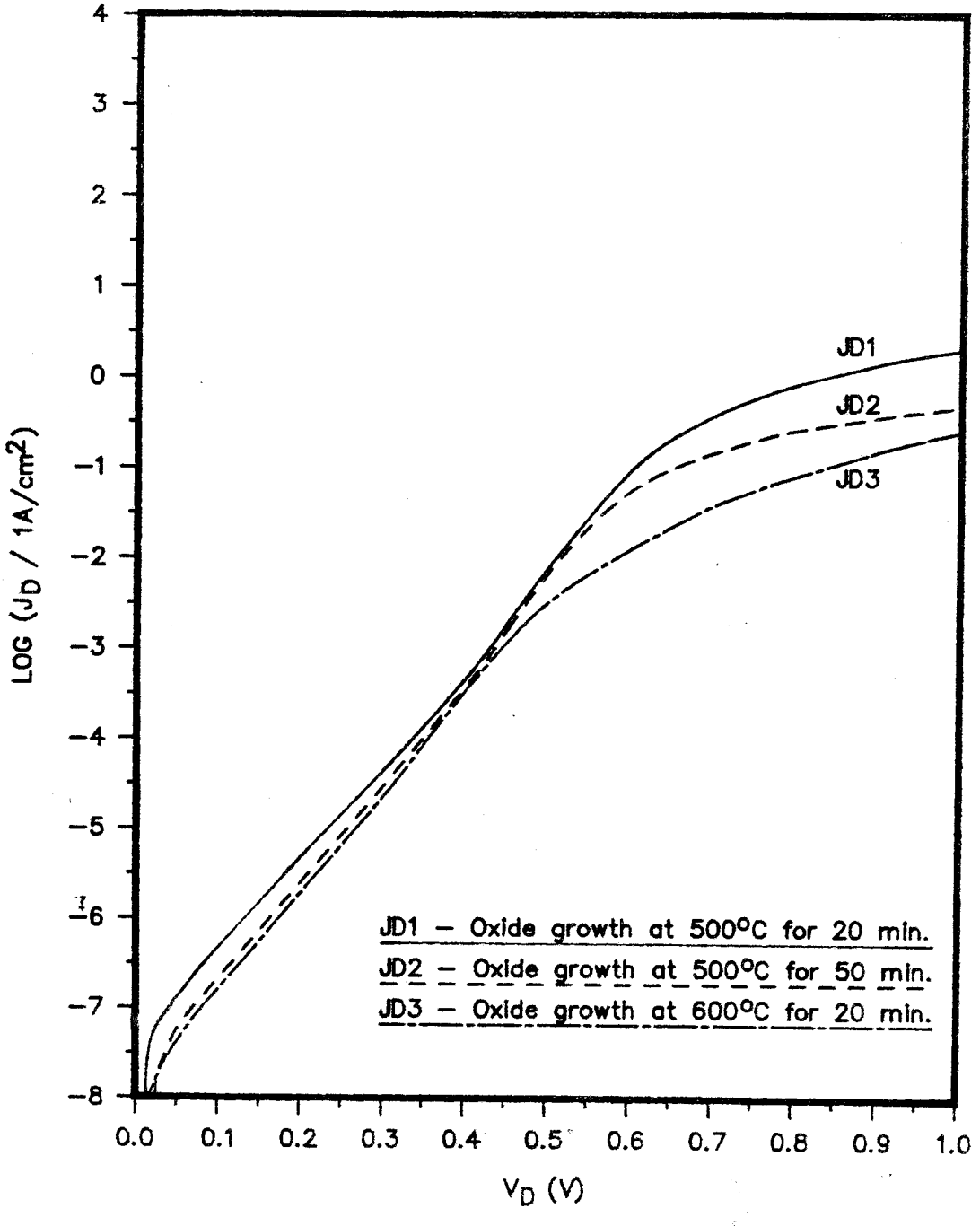


Fig. 4.3. Electrical properties of Al–I–Si dot diodes with different oxide growth

The change in effective series resistances showed, as expected, that the tunneling oxide thickness increases as the growth temperature or the growth duration increase. However, for the low temperature oxide growth process, the oxide thickness is considered to be self limiting for a given temperature [3]. This result contradicts the result of the above experiment. There are two ways to explain the discrepancy. First, the oxide may not have reached its self-limiting thickness for the conditions investigated. Secondly, the oxide growth may not be uniform over the entire wafer, leading to pin holes or small regions with thinner oxide than elsewhere. As the oxidation duration was increased, these thinner regions would continue to oxidize, while the rest of the oxide would be self-limited from any further growth. The second case was likely to be the cause for the discrepancy, since a much decreased reverse bias saturation current and recombination-generation current at low bias were observed in the case of diodes with growth conditions of 500°C for 50 minutes.

In the MIS BJT experiments, the 500°C, 20 minutes growth process was chosen on account of its lower series resistance, and its use in previous studies [3,4]. It may be better to choose a different oxidation process for better device stability.

4.1.4 Emitter deposition and definition

The emitter metal was deposited on the front of the wafer after the oxidation process. A brief discussion of the choice of metals, and patterning of the metals was presented in the previous chapter. The actual emitter metalization procedures were as follows.

The emitter metal thickness was chosen to be 3000 Å. This should give acceptable sheet resistivity, without having to use unsatisfactorily long etch times for any of the three metals. Both Al and Ti were evaporated using a tungsten coil as the heating element in the CHA chamber. Whereas Mg was evaporated using a "Drummel" type tantalum boat as the evaporation source, in the CHA chamber. The acceptable deposition rates for both Al and Mg were about 5 to 10 Å per second, whereas the deposition rate of Ti was limited by the evaporation power supply to about 2 Å per second.

The direct patterning photolithographic method as described in the previous chapter was used to pattern the emitter metal. The etchant for the patterning of Al was 50% phosphoric acid heated to 60°C, and the etch rate was about 300 Å/min. For patterning Mg, 0.4 ml of HNO_3 was diluted with 400 ml of DI water to make a 0.1% HNO_3 etchant.

The etch time for patterning 3000 Å of Mg on a full wafer was about 5 minutes, giving an average etch rate of 600 Å/min. However, if the above-mentioned etchant were used to pattern quarter wafers or half wafers, then a significant increase in overetching was observed. Ti patterning was performed by using 1 % HF acid at room temperature with an etch rate of about 600 Å/min. Because HF attacks silicon dioxide, a portion of the underlying oxide was damaged by the etchant, resulting in less stable devices.

4.2 The transistor structure and test patterns

Two batches of MIS BJTs were fabricated for studying the possibilities of implementing MIS BJTs in VLSI applications. The performance and relative stability of the different emitter metals and polysilicon emitter devices can also be compared. The first batch of devices was fabricated on MR-20 and GT-G series wafers. They were used solely to study the effect of different metalizations and their relative stability. The second batch of devices was fabricated on GT-J series wafers, and they were used to compare metal emitters and polysilicon emitters. The transistor structures (see Fig. 1.2. and 1.3.) were identical in both batches of wafers.

In the first batch of MIS BJTs, the transistor with the largest emitter contact area was the one chosen to be

studied, from a number of different sized transistors on the wafers. This was because the direct patterning scheme had shown some damage to the emitter metal for the smaller devices.

The 10 μm x 10 μm devices with different intrinsic base region overlapping(refer to Fig. 4.1) were studied and compared with polysilicon devices of the same configurations on the same wafers, for the second batch of MIS BJTs. The smaller sized transistors were studied as they were of a more reasonable size for VLSI applications.

A Van der Pauw cloverleaf for measuring the intrinsic base resistivity was also available for checking the base implantation. The structure for such a test pattern is shown in Fig 4.4.

Two separate voltage vs current measurements were required to determine the base spreading resistance using the Van der Pauw method. First of all, the resistance in the ab direction was measured by injecting a charge flow through node b, a and measuring the potential drop across node c,d. The resistance in the ab direction is given by:

$$R_{ab} = \frac{V_{dc}}{I_{ab}} \qquad (4.1)$$

Secondly, the resistance in the orthrogonal direction was

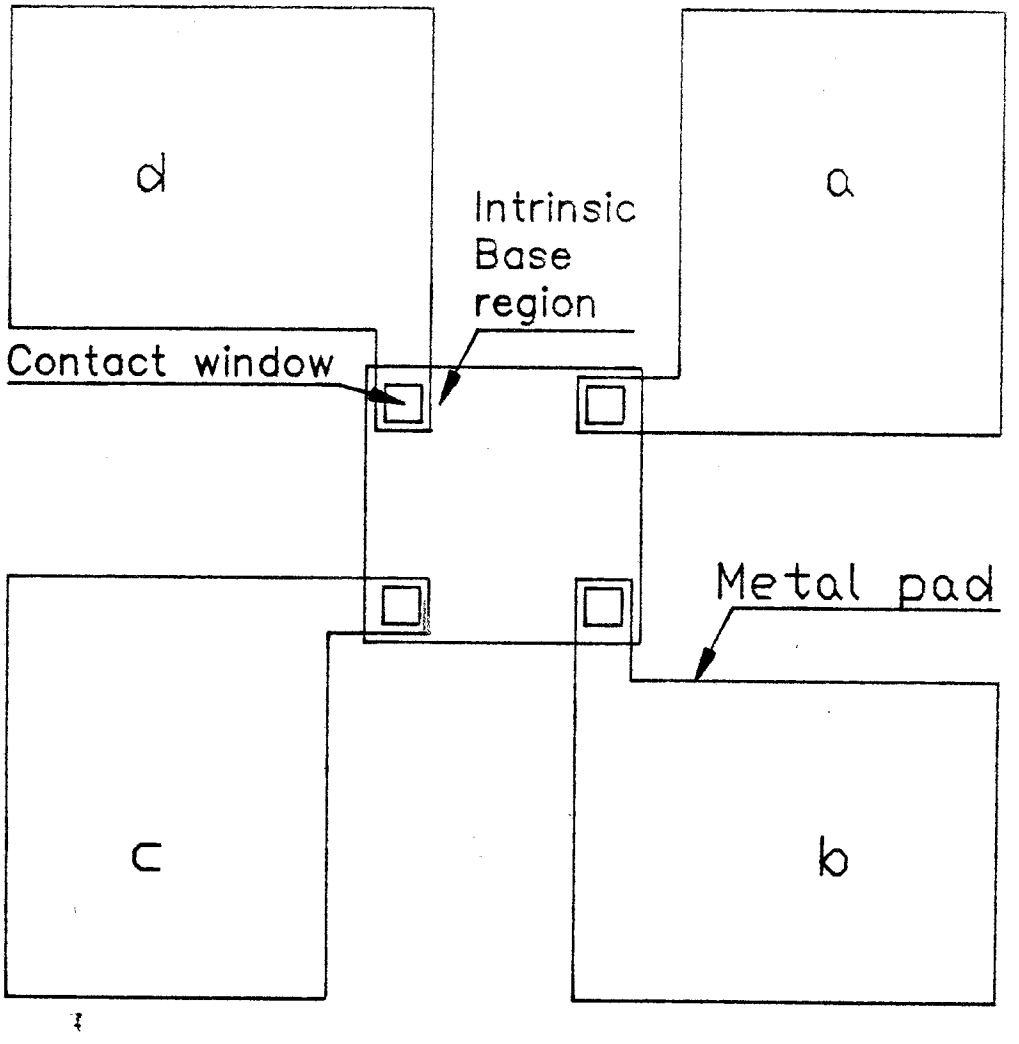


Fig. 4.4. Structure of the Van der Pauw test pattern

measured similarly by injecting the current through node b,c and measuring the potential drop across node a,d. The resistance in the bc direction is then:

$$R_{bc} = \frac{V_{ad}}{I_{bc}} \tag{4.2}$$

Once the two orthrogonal resistances were known then the spreading resistance could be computed from:

$$\rho_s = \frac{\pi}{2 \ln 2} (R_{ab} + R_{bc}) \, f(\frac{R_{ab}}{R_{bc}}) \tag{4.3}$$

where $f(\frac{R_{ab}}{R_{bc}})$ is known as the Van der Pauw function, and it is equal to 1, if R_{ab} is the same as R_{bc} for a symmetrical test pattern.

The spreading resistance for the first batch of transistors was measured and checked against the SUPREM II simulations for the implantation process. The two resistances were of the same order of magnitude. The measured value was 25 KΩ/square, while the simulated value of 17 KΩ/square was in close agreement.

Chapter 5

Temperature stress tests

As discussed in chapter 1, the major concern with MIS BJTs is the stability of the thin oxide layer. To study this phenomenon we subjected MIS BJTs to temperatures which the devices would likely be exposed to in commercial processing, e.g. temperatures of up to 400°C as may be encountered in wirebonding and packaging. The tests reported in this chapter are referred to as temperature stress tests. The devices were heated to a certain temperature for a specified time and then returned to room temperature for measurement of J-V characteristics.

5.1 The experimental setup

An HP4145 semiconductor parameter analyzer was used to perform all the measurements of the transistor characteristics at room temperature. The $\log(J_C$ & $J_B)$ vs V_{BE} curves with a small collector-base bias voltage were recorded after each stress, in order to observe the change in device characteristics. The base-collector characteristics were measured from time to time to ensure that there was no degradation in the base-collector junction.

A Statham convection oven was used to heat-treat the

MIS BJTs for temperatures up to 265°C. A 1 L/min. flow of nitrogen into the oven was used to ensure an inert environment while stressing the devices. The device under test was placed in the oven at room temperature, then the temperature was ramped up to the desired stressing temperature in the nitrogen ambient. The stress durations were measured from the instant that the desired stress temperature was reached to the instant of turning off the oven's heating element. The devices were allowed to cool to room temperature with the nitrogen flow maintained. Therefore, the effective stress times were longer than the recorded values, but by performing the test this way the chance of reoxidation by exposure of the heated devices to atmosphere was minimized. However, some recovery process was observed when leaving the devices at room temperature and atmospheric environment for around 20 Hours.

A Minibrute quartz furnace was used to stress devices at temperatures of 400°C and higher, since the maximum temperature setting for the Statham oven was only 265°C. The quartz furnace was pre-heated to the desired stressing temperature before placing the wafers into the furnace. A nitrogen flow of 1 L/min. was also used to ensure an inert environment for the wafers. The stress duration in this case was measured from the instant of placing the wafers in the furnace to the instant of removing them. The heated wafers

were sprayed with Freon gas for a faster cooling while preventing the heated wafers from being exposed to the atmosphere, at the moment of their removal from the furnace.

5.2 Comparison of Mg, Al, and Ti devices

The GT-G series wafer with an implant dosage of $1x10^{12}cm^{-2}$ was used to compare the relative performance of Mg, Al and Ti MIS BJTs. The GT-G-4 wafer was scribed into quarters, which were then processed simultaneously. However, during the emitter metal deposition step, the three emitter metals were deposited separately. By so doing, the properties of these devices should be identical, except for the emitter metals, allowing a fair comparison between them.

The initial current gain of all the MIS BJTs (refer to Fig. 5.1) was very similar, with the Mg devices giving the highest gain of about 650 and both the Al and Ti devices exhibiting gains of about 550. The percentage yield was quite good for the Al and Mg devices, but was poor for the Ti devices. About 70% of the Mg and Al devices on the quarter wafers gave similar gains to the stated values, whereas the yield was only 20% in the case of Ti devices. The relatively low yield for the Ti devices was due to the major loss of interfacial oxide during the Ti metal patterning step. Therefore the temperature stress test on the Ti devices reflects not only the Ti-I-S junction

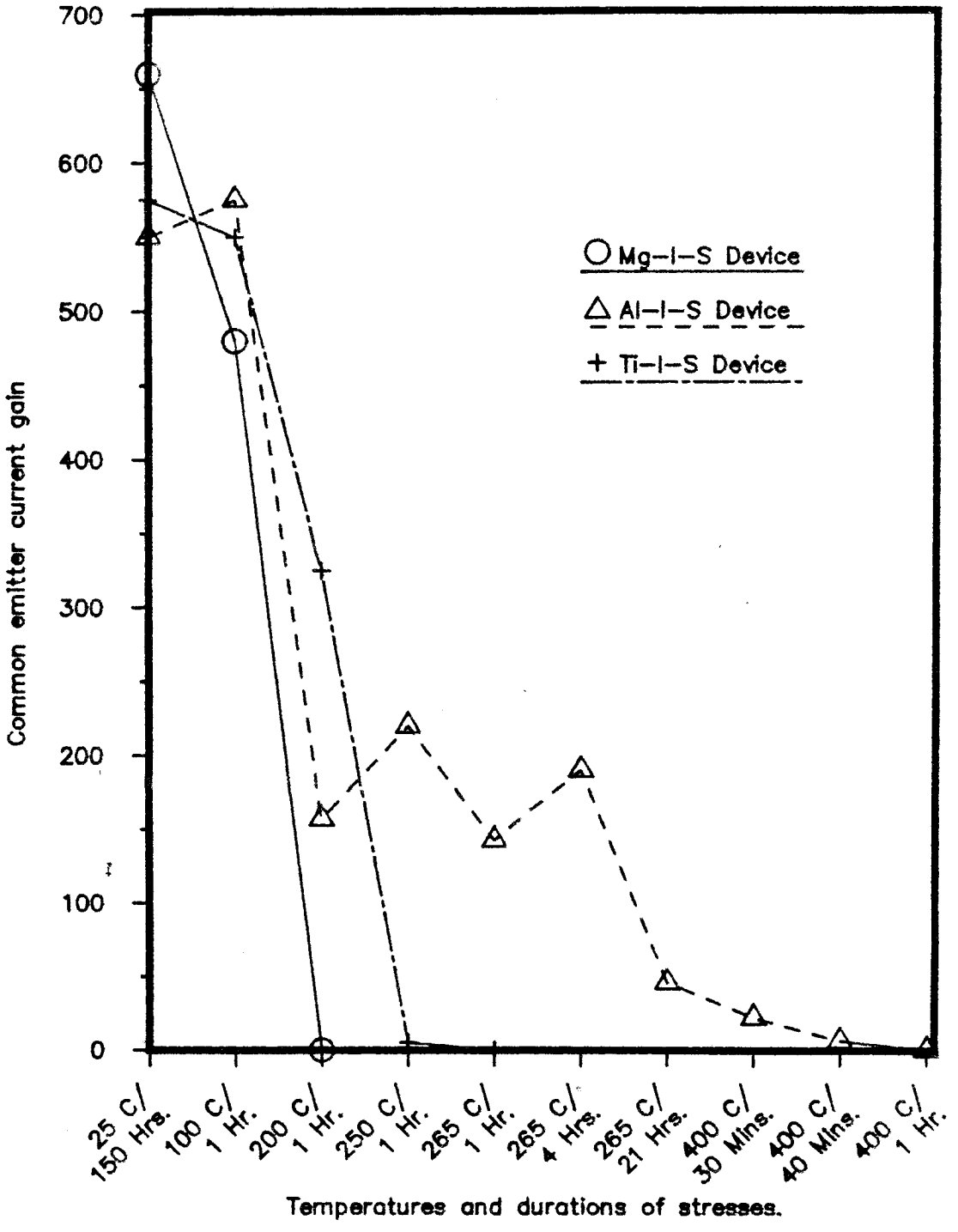


Fig. 5.1. Degradation of current gains for the GT–G series devices

stability but also the suitability of the fabrication process.

The Gummel plots for GT-G series MIS BJTs with the three different metals after various stages of temperature stressing, are shown in Fig. 5.2 to 5.4. The large base current at low bias, with ideality factor being close to 2 for this batch of devices suggested that the relatively low gains could be due to large emitter / base space-charge region recombination. Two mechanisms which might be responsible for this large recombination current are: insufficient annealing of the base implantation leading to short carrier lifetime, and emitter metal penetration through the thin oxide leading to an increase in surface states. These two mechanisms would also account for the relatively low current gains for these devices.

Three devices from each quarter wafer were monitored throughout the stress sequence, while other devices were randomly checked in order to ensure that the degradation of the devices was not local. The measured current gains of the three devices with the highest initial gain for the three different metallizations are shown in Fig 5.1. The current gains of the rest of the devices on the same quarter wafer also degraded with the same trend.

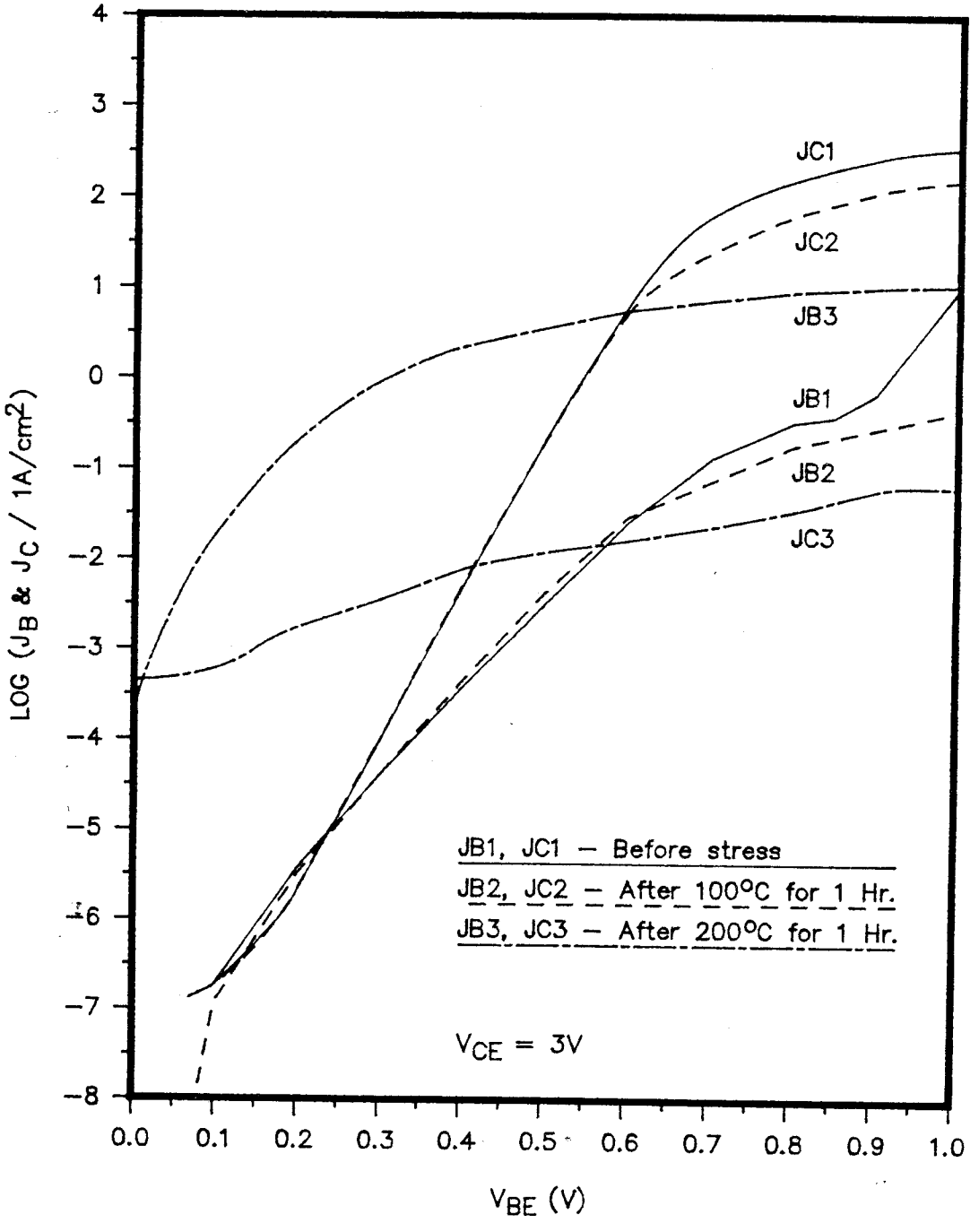


Fig. 5.2. Gummel plots for Mg–I–Si transistor

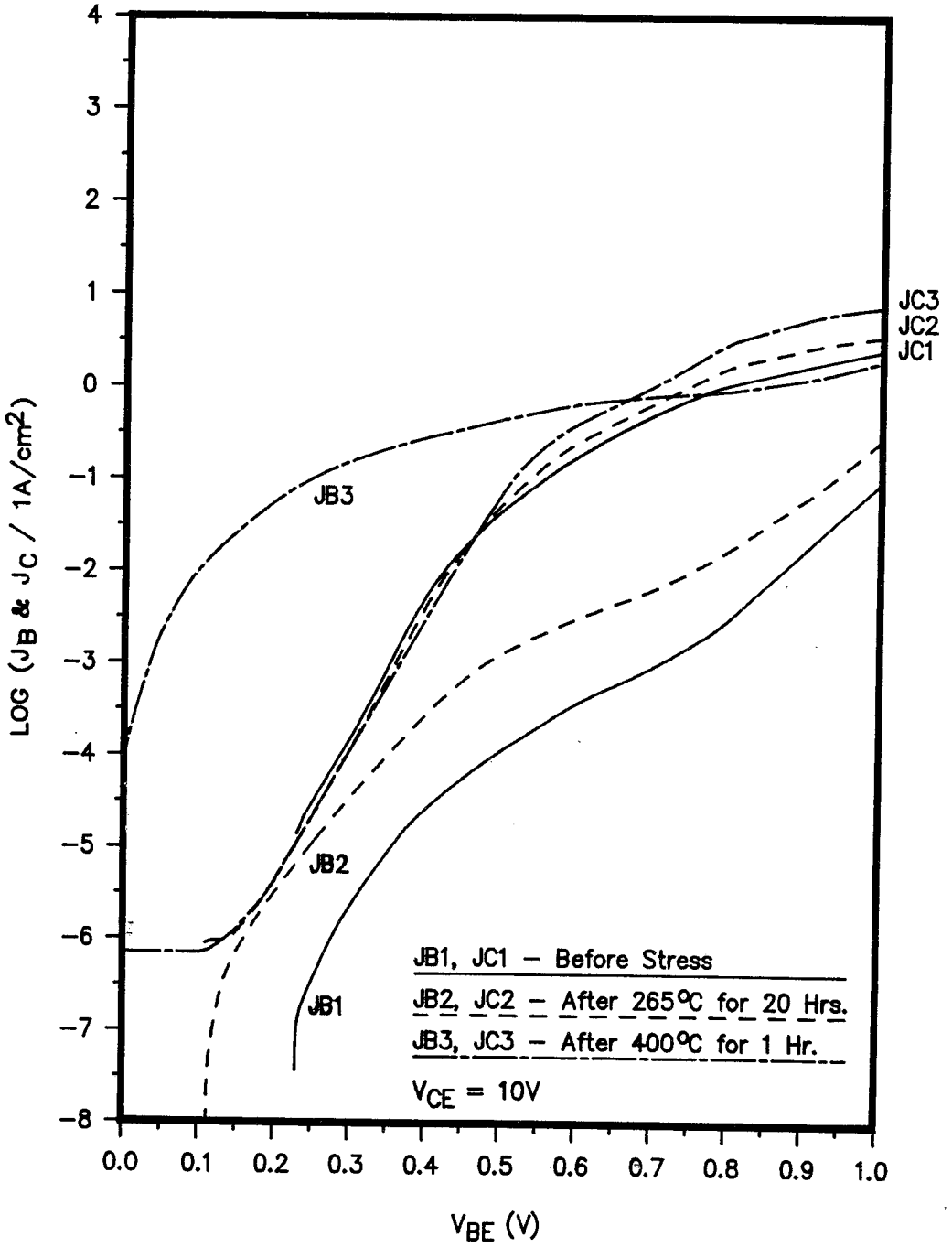


Fig. 5.3. Gummel plots for Al–I–Si transistor

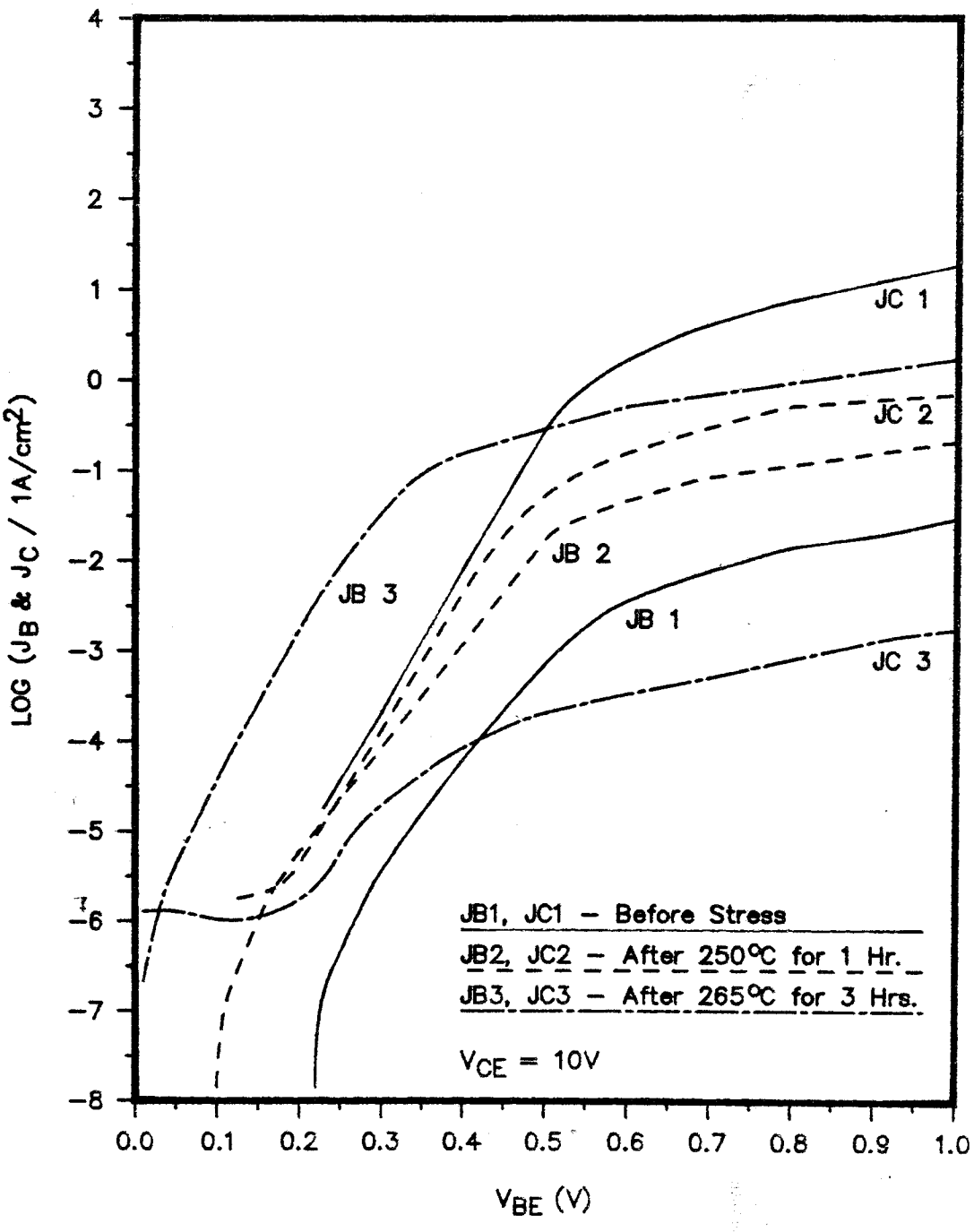


Fig. 5.4. Gummel plots for Ti–I–Si transistor

Physical degradation of the Mg-I-S and Ti-I-S devices was also observed. The Mg emitter changed from a light greyish colour to dark brown and the texture of the metal changed from small uniform grains to large non-uniform grains, when the stress temperature was increased to around 200°C. The Ti emitter metal changed from black to a reddish colour when the stress temperature was around 200°C.

The principal manifestation of degradation in all three MIS BJTs was an increase in base current with increasing temperature stress. However, the collector currents were virtually unchanged during moderate stress until the base currents were comparable to the collector currents. Further stressing on the devices, showed gradual loss of transistor action, as the base currents continued to rise and the collector currents began to decrease.

5.3. Comparison of Mg and Polysilicon devices

A number of the GT-J series wafers, with implant dosage of either $1x10^{12}cm^{-2}$ or $5x10^{12}cm^{-2}$ with both Mg and Al metalizations were fabricated to try to optimize the MIS BJT performance. It was found that the better MIS BJTs were those that had the lower implant dosage and Mg metalization, as expected. The GT-J series wafers also had a set of polysilicon emitter transistors available adjacent to the

MIS BJTs on the same wafers. This enabled the study of the effect of different emitters on otherwise identical devices.

The highest gain devices for this set of wafers were the Mg devices; they showed gains of the order of 3,500. The polysilicon devices gave gains of 3,000 and the best gainfor the Al devices was 1500. The percentage yield for this batch of devices were very good. The yield of the devices on the wafers having gains in the same order of magnitude for all three different emitter devices was close to 90%. The log(J) vs V_{BE} curves (shown in Fig.5.5 & 5.6) for both the Mg devices and polysilicon devices were almost identical initially, with the Mg devices having a slightly larger base recombination current at low bias. However, Mg devices seemed to have higher maximum gain at optimal bias, while polysilicon devices had a more consistent gain throughout the operational bias range.

The devices were left at room temperature in an atmospheric environment for 1 week, and then the device characteristics were measured again. No change in device characteristics was observed, showing that the MIS BJTs were quite stable in room temperature. However, after the devices were heat treated at 200°C for 1 hour, the Mg devices showed the same degradation mode as the previous batch of MIS BJTs. The Mg metalization changed from a light greyish color to

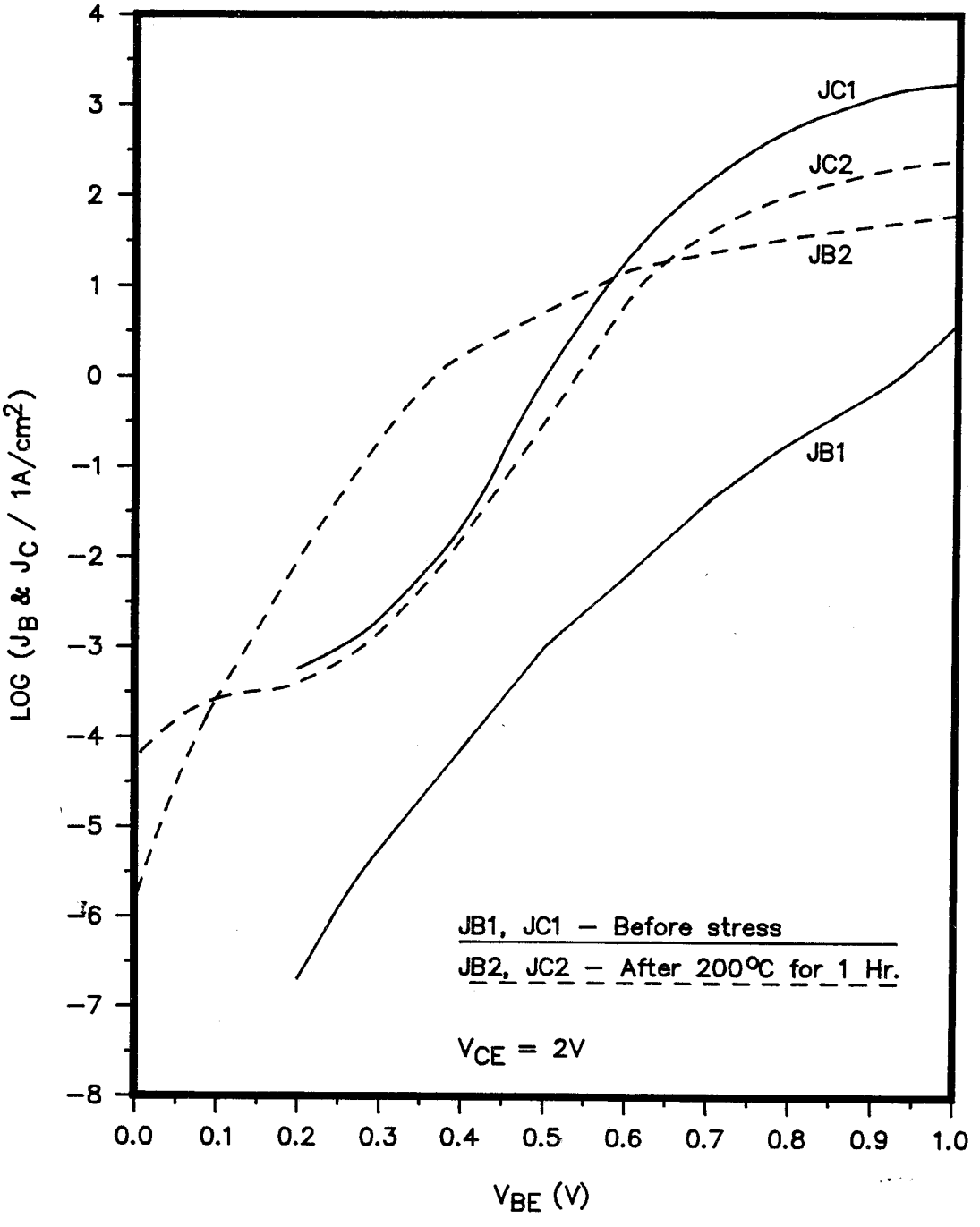


Fig. 5.5. Gummel plots for GT–J series Mg–I–Si transistor

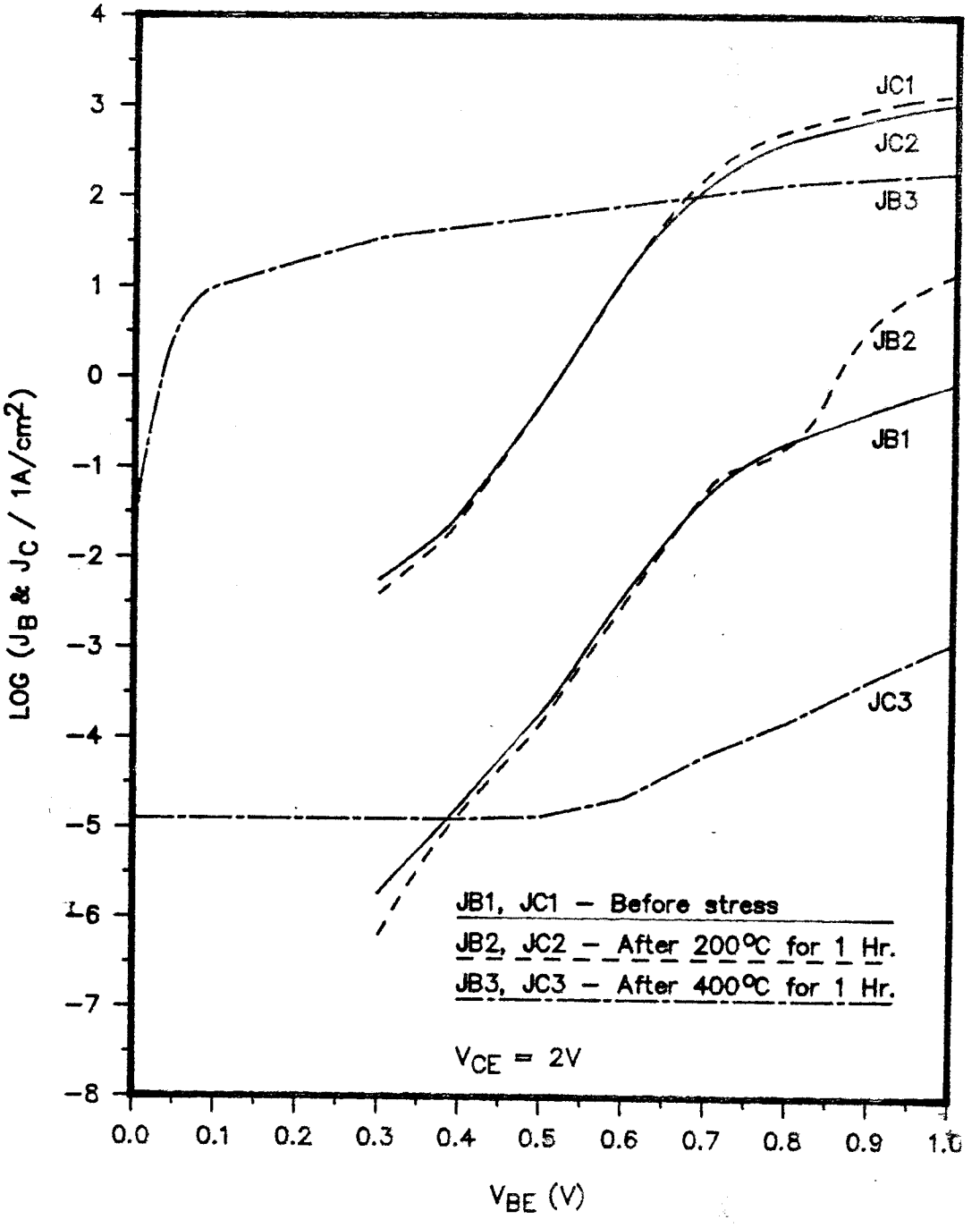


Fig. 5.6. Gummel plots for GT–J series polysilicon emitter transistor

dark brown with large non-uniform grains. The current gain of the Mg devices degraded to essentially zero due to a large increase in the base current at low bias. Whereas the polysilicon device characteristics were virtually unchanged by the temperature stress, except for a slight increase in base current at large base-emitter bias. After the polysilicon devices were stressed at 400°C for 1 hour, the polysilicon devices were all dead. The log(J) vs V_{BE} curve (Fig 5.6.) showed a short-circuit in base-emitter junction, and the collector current was essential zero.

The base-collector junctions for both Mg-I-S and polysilicon devices were checked to ensure that the degradation mode of the devices was entirely due to effects at the base-emitter junctions. The $\log(J_C)$ vs V_{CB} curves (Fig 5.7 & 5.8) before and after stress showed good diode characteristics in both devices, while a small increase in J_C at low bias was observed in the case of Mg-I-S devices.

5.4. Discussion

In the case of Mg and Al devices, the base current curves depart from a logarithmic dependency on base-emitter bias in the low bias region after temperature stressing of 200°C for 1 hour and 400°C for $1\frac{1}{2}$ hours respectively. Attempts were made to simulate the form of these base current-voltage curves with the MIS BJT model. The model

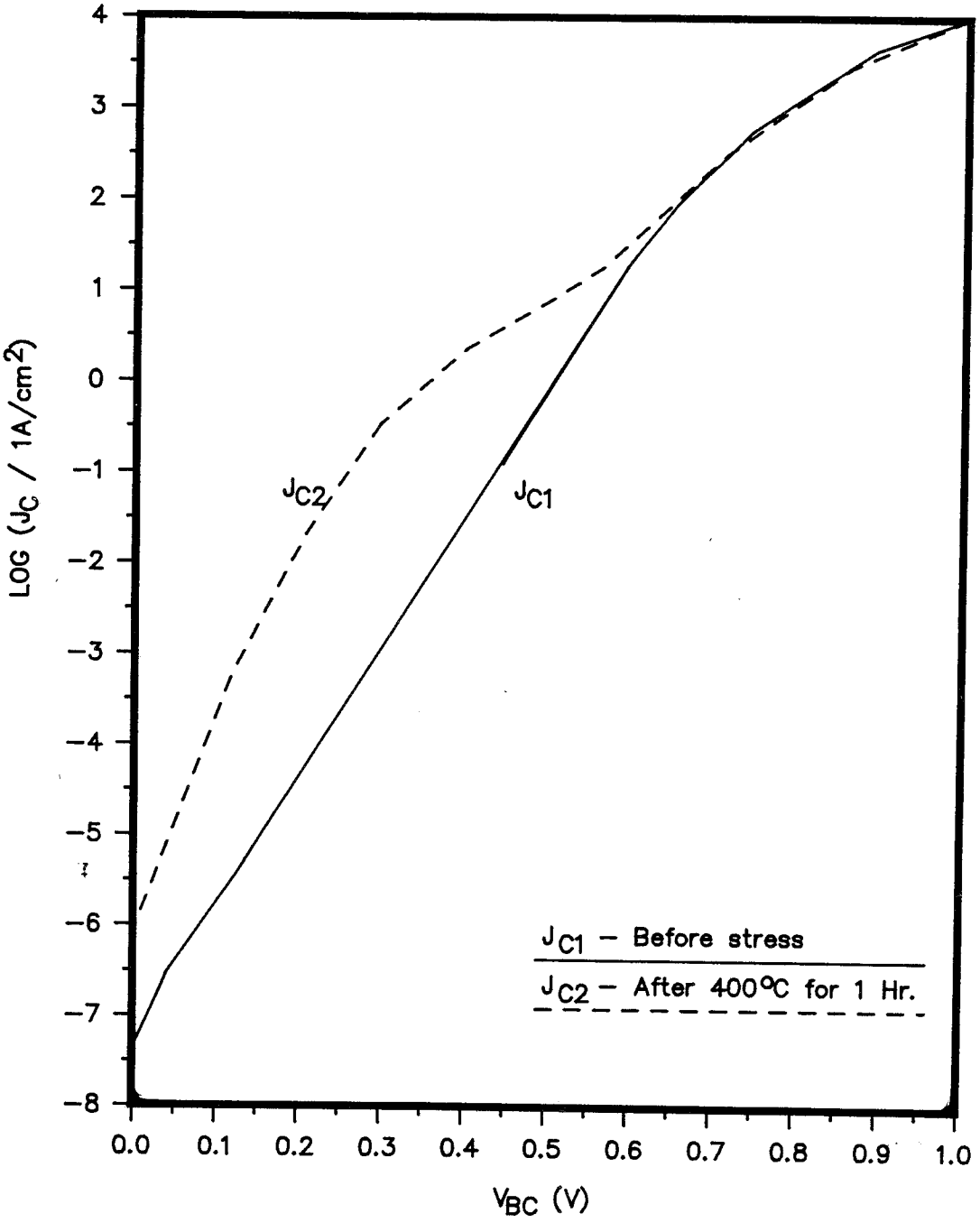


Fig. 5.7. Log(J_C) vs V_{BC} curves for Mg–I–Si transistor

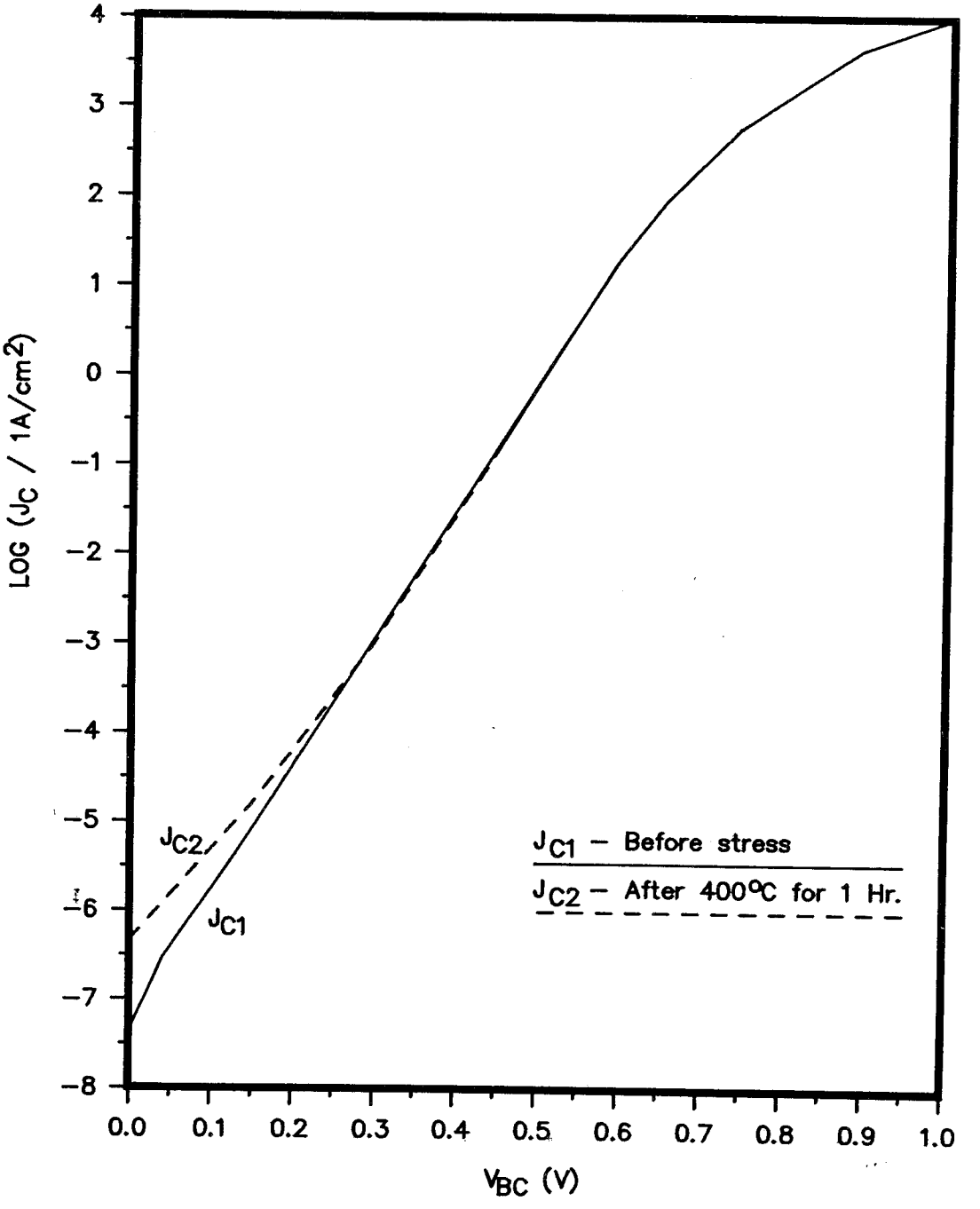


Fig. 5.8. Log(J_C) vs V_{BC} curves for polysilicon emitter transistor

parameters such as oxide thickness, metal work function, and carrier lifetime in the base region were varied over a set of physically realistic ranges (refer to Fig. 2.3 through Fig. 2.6). Yet, none of the changes in these parameters resulted in the experimentally observed form of the base current. However, the actual results were well described by adding a resistive shunt current component to the base current exhibited by the device prior to any temperature stress. This suggested that temperature stressing of Mg and Al devices leads to gradual replacement of the MIS junction by an ohmic contact. In the case of Al devices, for example, a $\log(J_B)$ vs V_{BE} curve resulting from the parallel combination of the unstressed junction and a resistance of 3.5 Ω-cm^2 (shown in Fig. 5.9) gave an excellent fit to the data obtained after stressing at 400°C for 1 Hour. The high contact resistance as compared to 5×10^{-4} Ω-cm^2 for typical Al/pSi contacts to silicon with the intrinsic base resistivity used here [22], could be interpreted as indicating that only small areas of the interfacial oxide were penetrated by the metalization. This would suggest that only selected regions, most probably "weak spots" or pinholes were present on the thin interfacial oxide leading to potentially unstable devices. Metal penetration through the insulating oxide and partially into the base region is further suggested by the observation of increasing collector-base recombination current at low bias in the

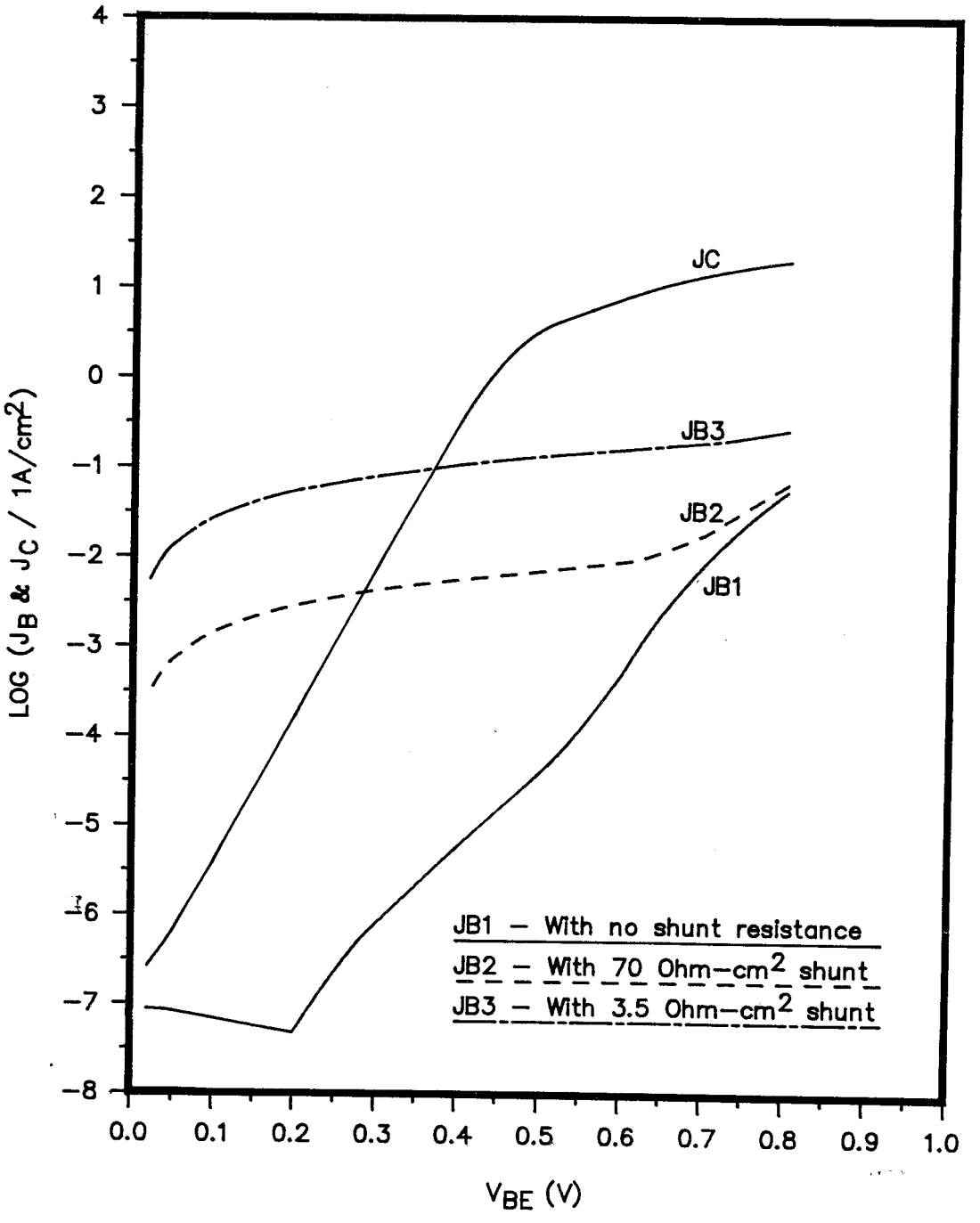


Fig. 5.9. The effect of shunt resistance on Al–I–Si transistor

$\log(J_C)$ vs V_{CB} curve as the temperature stressing increased. Metal penetrated into the base region would cause an increase in majority carrier concentration, leading to higher recombination current at low bias.

In the case of Ti devices, the $\log(J_B \& J_C)$ vs V_{BE} curves did not show a gradual replacement of the MIS junction by an ohmic contact. The base current curves did not depart from the logarithmic dependency on base-emitter bias at low values, but the extrapolated saturated current density at zero V_{BE} increased with increasing stress. The ideality factors for these set of base currents were all very close to unity, showing that the MIS junction was gradually shifting from a minority carrier dominated junction to one that was dominated by majority carriers without becoming an ohmic contact. A major decrease in collector current after stress complemented the above observation, since the collector current is determined by the minority carrier injection current. This degradation mode can be well described by penetration of Ti through the interfacial oxide. The combination of the work function of Ti and the intrinsic base doping density will cause a Schottky barrier when the metal is in contact with the base, whereas in the case of Mg and Al, although having similar work functions, these metals are good doping materials which would result in formation of an ohmic contact when in contact with the

p-type base at high temperature. The extrapolated saturation current density was 5.7×10^{-7} A/cm^2 after a stress of 265°C for 3 hours, whereas the Ti/pSi Schottky barrier junction would have a saturation current density of 1.7×10^{-4} A/cm^2 with barrier height of 0.61eV [23], showing that, either the junction did not completely reduce to a Ti/pSi Schottky barrier or only small areas of the oxide were penetrated by Ti to form Schottky barriers. The degradation mode cannot be easily determined, but the latter one mentioned would seem to be more likely, since it is consistent with the interpretation of the results for the Mg and Al devices.

The rapid degradation of the polysilicon devices is due to the overlaying metal that was used to reduce contact resistance to the polysilicon emitter. It is not indicative of an intrinsic device failure mode since the devices were treated to temperatures of 500°C during processing before metal deposition, but no loss in performance was observed. The metal used for this experiment were either Mg or Al, both of which are acceptor impurities in doping Si. Penetration of these metals at high temperature stressing will cause the n^+ doped polysilicon emitter to gradually become p-type, hence shorting the base-emitter junction. Since the diffusion constants for these dopants are quite high for polysilicon [24], the device tends to degrade rapidly at high temperature stress, while remaining stable

at lower temperature stress.

Chapter 6

Series resistances measurement

As discussed in Chapter 1, a potential drawback to the use of MIS BJTs in high speed applications is the presence of a thin insulating layer in the emitter current path. Because high gains are possible with MIS BJTs, some of this gain can be traded-off against the base series resistance. Reduction of this resistance means that the emitter series resistance can become the dominant resistance limiting the high-speed performance of the transistor. It is not easy to obtain an accurate measure of the emitter resistance. However some attempts to measure R_E in MIS BJTs were made and are reported in this chapter.

6.1. Methods of measurement

There are two commonly used methods of determining the series resistances of bipolar transistors. They are the open collector method [25] and the method proposed by Ning and Tang [14]. Both of these methods were used to try to determine the effective series resistance of the thin tunneling oxide. However, the first method will only yield the emitter series resistance, whereas the Ning and Tang method will yield both the emitter and base series resistances.

6.1.1. Open collector method

This method is based on measuring the voltage across the emitter and collector contacts as a function of base current injected from a current source. The HP4145 parameter analyzer was setup to perform such a measurement, and the resulting V_{CE} vs I_B curves for both Mg and Polysilicon devices are shown in Figs. 6.1 and 6.2 respectively.

It was found that neither of the V_{CE} vs I_B curves was perfectly linear. The slope at low current is slightly greater than that at high current. This is partially due to the nature of the method of measurement, since it has neglected the base conductivity modulation effect, and partially due to the non-linear nature of conduction in the thin insulator. The estimated emitter series resistance for the $10x10\mu m^2$ Mg and Polysilicon devices ranged from 90 to 120 Ω and 75 to 95 Ω respectively.

6.1.2: Ning and Tang method

The Ning and Tang method [14] relies on the fact that I_B & I_C vs V_{BE} curves for an ideal bipolar transistor without any series resistance and high injection effects are strictly proportional to $\exp(qV_{BE}/kT)$. Any deviation from the ideal I_{B0} and I_{C0} curves at high bias is assumed to be caused by either the emitter or base series resistances. The deviation in I_B can be expressed by:

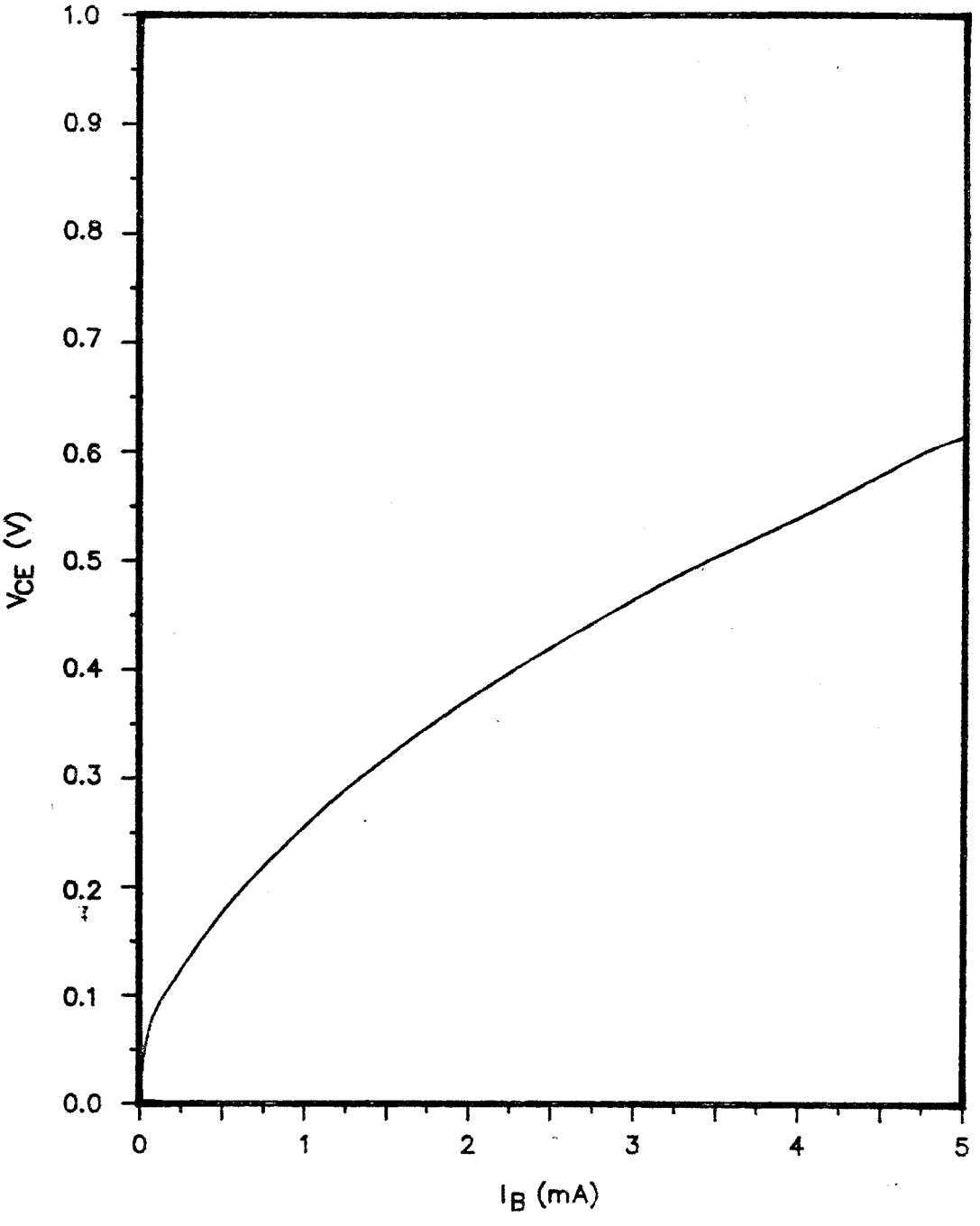


Fig. 6.1. V_{CE} vs I_B curves for Mg–I–Si transistor

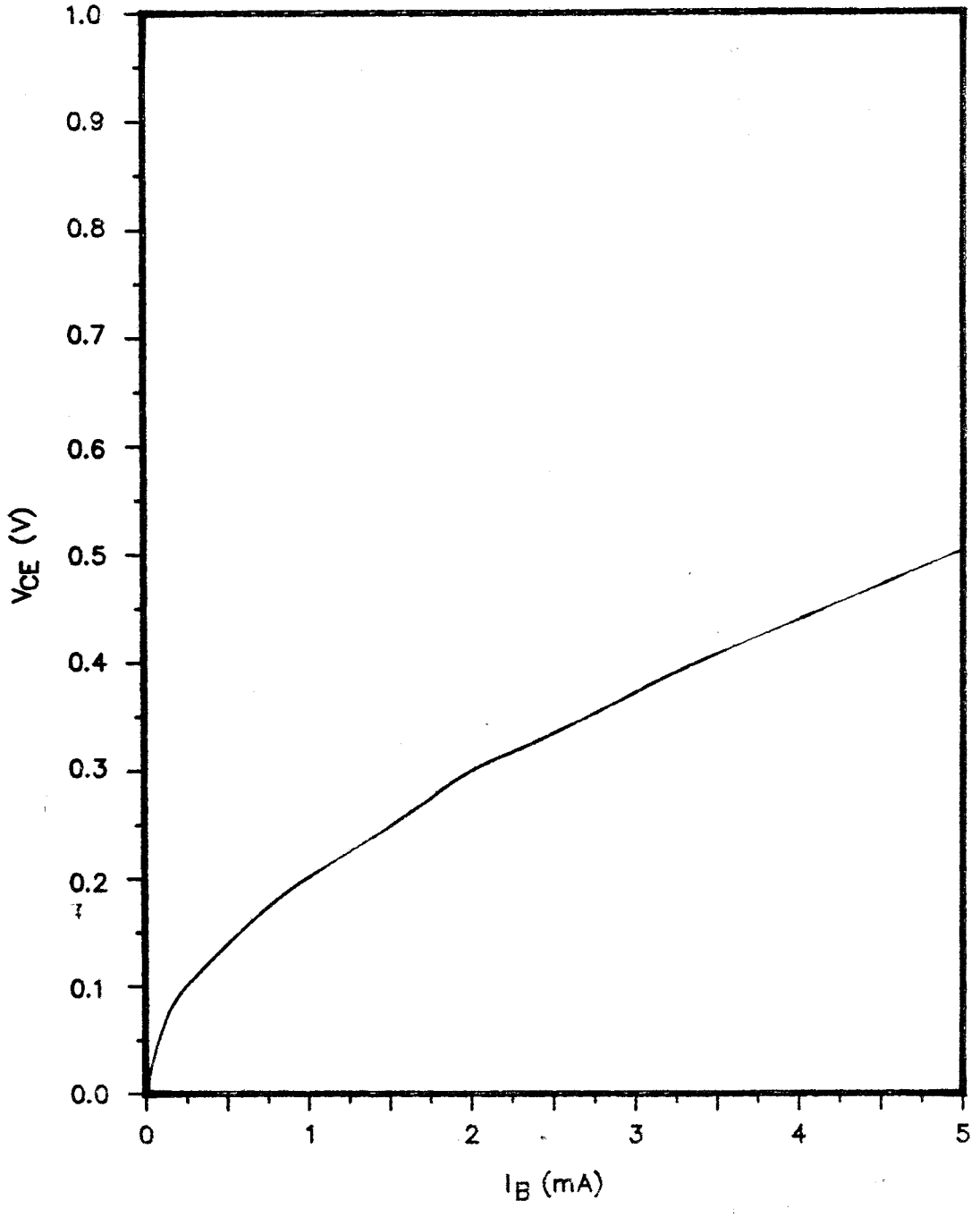


Fig. 6.2. V_{CE} vs I_B curves for polysilicon transistor

$$I_{Bo}/I_B = \exp(q(I_E R_E + I_B R_{bi} + I_B R_{bx})/kT) \qquad (6.1)$$

Where R_E is the emitter series resistance, R_{bx} is the extrinsic base series resistance, and R_{bi} is the intrinsic base resistance. These series resistance components are shown in Fig 6.3.

Since $\beta = I_C/I_B$, the expression (6.1) can be rewritten as

$$(kT/qI_C)\ \ln\ (I_{B0}/I_B) = (R_E + R_{bi}/\beta) + (R_E + R_{bx})/\beta \qquad (6.2)$$

The term R_{bi}/β can be treated as a constant, since R_{bi} can be shown to be proportional to β at all current levels [26]. When $(kT/qI_C)\ \ln(I_{B0}/I_B)$ is plotted against $1/\beta$, the slope of the curve will then be $(R_E + R_{bx})$ and the Y intercept will be $(R_E + R_{bi}/\beta)$. However, R_{bi}/β is generally small and can be neglected in the expression (6.2). Therefore R_E can be evaluated directly from the intercept, while R_{bx} can be readily evaluated from the slope of the curve.

In the actual determination of the series resistance using the Ning and Tang method, values of I_B and I_C were extracted from the log (I_B & I_C) vs V_{BE} curves for both the Mg and Polysilicon devices. The I_{B0} values were extrapolated from the values of I_B at V_{BE} = 0.7 V back to V_{BE} = 0V with the assumption of the ideality factor being unity. The $(kT/qI_C)\ \ln\ (I_{B0}/I_B)$ vs $1/\beta$ curves for both types of devices are shown in Fig 6.4 and 6.5. However, these curves show a

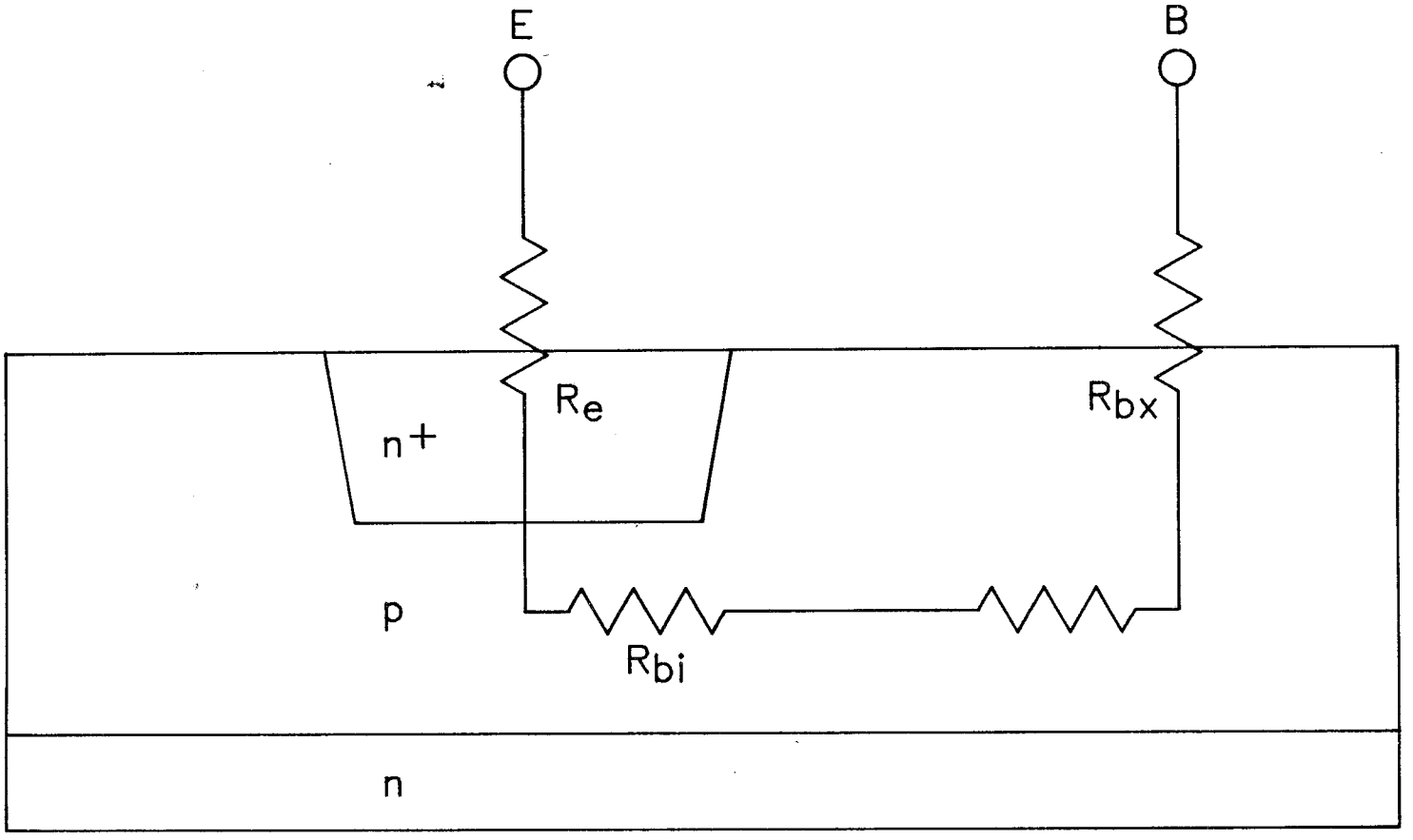


Fig. 6.3. Series resistance components

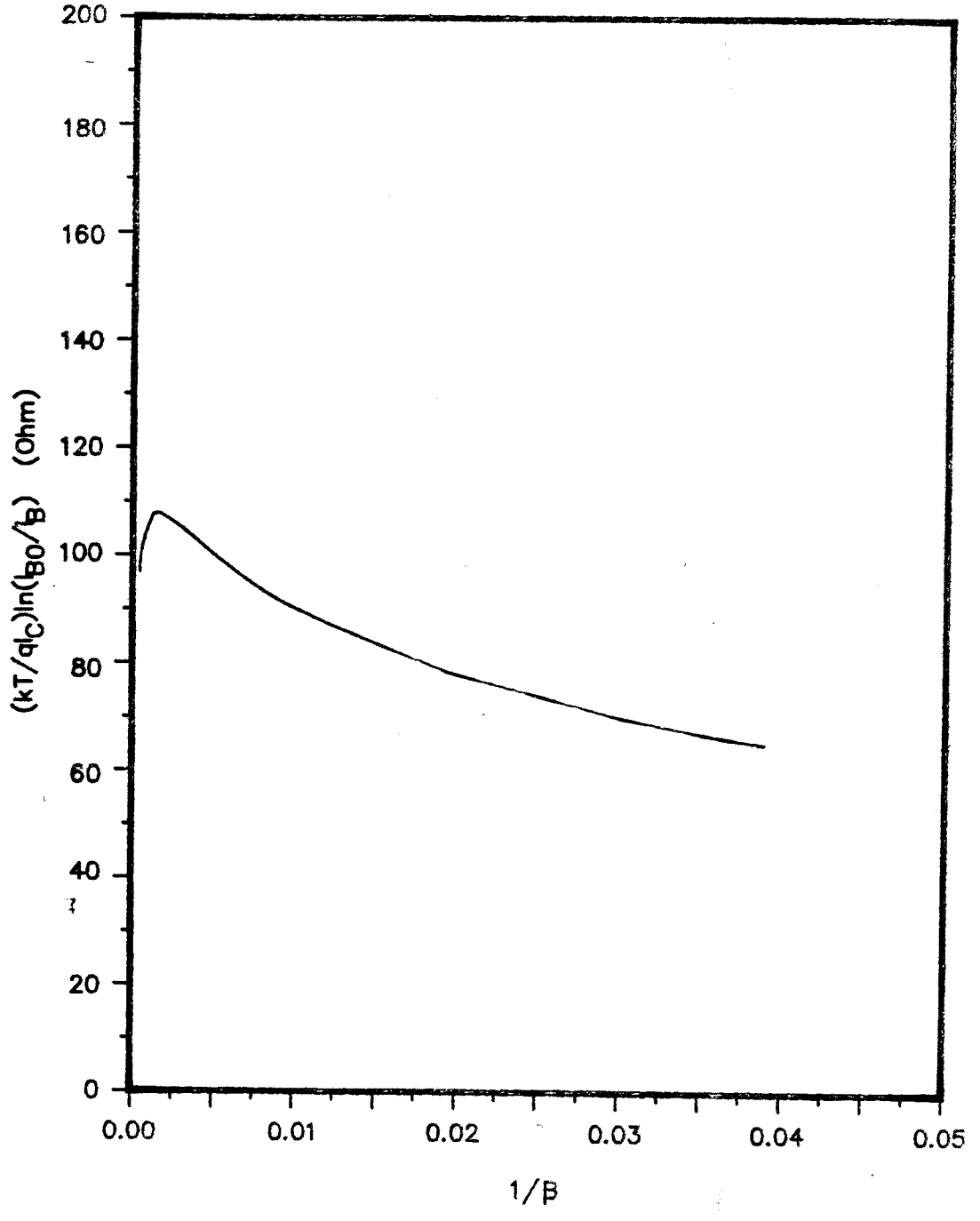


Fig. 6.4. $(kT/qI_C)\ln(I_{BO}/I_B)$ vs $1/\beta$ curve for Mg–I–Si transistor

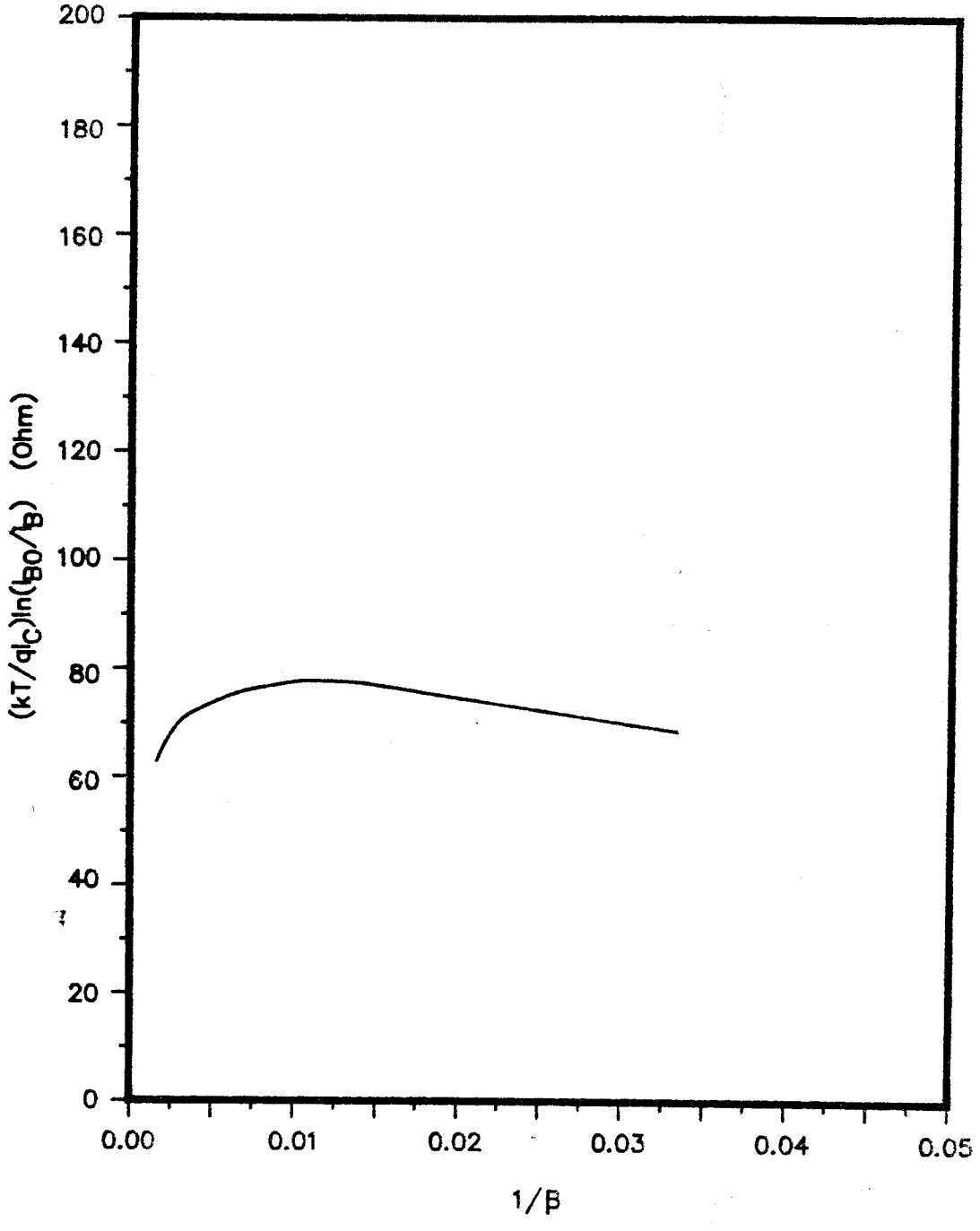


Fig. 6.5. $(kT/qI_C)\ln(I_{B0}/I_B)$ vs $1/\beta$ curves for polysilicon transistor

negative slope while the intercepts were at around 115 Ω for the Mg devices and around 75 Ω for the Polysilicon devices. The intercept values representing the series emitter resistances R_E agree well with the results of the open collector method, but the negative slope would mean that the extrinsic base series resistances was negative! The effective negative base series resistances were due to the fact that dependence of I_B on V_{BE}, at high bias for the devices under test, was exponential instead of the ideal linear dependence.

6.2. Discussion

The absence of a linear I_B, V_{BE} at high bias means that the Ning and Tang method is not helpful in estimating the series resistance of the BJTs used in this work. However, the open collector results appear to be reasonable. The specific contact resistivities for the Mg and Polysilicon devices were around 110 $\mu\Omega$-cm^2 and 85 $\mu\Omega$-cm^2 respectively. These values are high compared to conventional bipolar transistors, which have corresponding resistivities of the order of 1 $\mu\Omega$-cm^2. The relatively high series resistances for the MISETs and Polysilicon devices would be a major drawback in implementing these device structures in VLSI applications.

Chapter 7

Conclusion

The main conclusion to be drawn from the work reported in this thesis is that MIS BJT devices have some severe limitations which may prevent their successful implementation in a commercial IC processing technology.

The principal drawback to the devices is the degradation of common-emitter current gain at moderate temperatures. Magnesium devices with initial gains in excess of 3000 have been shown to fail completely at temperatures as low as 265°C. Devices with aluminum and titanium metallization continue to act as transistors, but with steadily decreasing current gain, until slightly higher temperatures (around 400°C). For all cases the degradation in gain appears to be due to changing conditions at the emitter/base junction. Shunting of this junction by metal from the emitter penetrating the oxide at thin spots in the oxide is suggested as being a likely cause of the results observed.

Another disadvantage of MIS BJTs is the series resistance associated with the thin insulating layer in the emitter tunnel junction. Our measurements of emitter

specific resistivity indicate that a reduction by nearly two orders of magnitude is needed for values of this parameter to reach acceptable levels for VLSI applications.

It is proposed that the degradtion of MIS BJTs be further investigated. Chemical methods, such as angle-resolved photoelectron spectroscopy, would be very helpful in complementing the electrical measurements reported here. Information on the changing oxide composition with temperature stressing, coupled perhaps with the results of high resolution cross-section transmission electron microscopy, would help confirm or deny whether metal penetration into the oxide is, as suggested in this thesis, responsible for device degradation.

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Appendix A.

Fabrication Procedures for the MIS BJTs

A.1. Fabrication procedure for MR-20 and GT-G devices

1. Mask oxide growth

   a) RCA clean

   b) Oxidation: 1100°C
   5 Min. preheat in O_2
   5 Min. push in O_2
   10 Min. dry oxidation in O_2
   20 Min. wet oxidation in $O_2 + H_2O$
   10 Min. dry oxidation in O_2+ 2% HCl
   10 Min. anneal in N_2
   5 Min. pull in N_2
   10 Min. cool in N_2

   Mask oxide thickness $\simeq$ 0.3 μm

2. Open windows for extrinsic base diffusion

   a) Use mask CU-063-01 with negative photoresist to pattern the windows. negative photoresist was also used to protect the back of the wafers.

   b) Etched in buffered HF for approximately 4 Min. until bare silicon exposed.

3. Extrinsic base boron diffusion

   a) RCA clean

   b) Predep: 1000°C
   5 Min. preheat in $O_2 + N_2$
   5 Min. push in $O_2 + N_2$
   5 Min. warm-up in $O_2 + N_2$

10 Min. dope in O_2 + N_2 + dopant

10 Min. hold in O_2 + N_2

5 Min. pull in O_2 + N_2

10 Min. cool in O_2 + N_2

c) Boron deglaze: 30 Sec. in 10% HF

d) drive-in: 1100°C 5 Min. preheat in O_2

5 Min. push in O_2

10 Min. dry oxidation in O_2

15 Min. wet oxidation in O_2 + H_2O

5 Min. dry oxidation in O_2+2.5% HCl

5 Min. pull in O_2

10 Min. cool in O_2

4. Phosphorous backside getter

a) Protect wafer fronts with PR, and strip oxide from wafer backs.

b) RCA clean

c) Predep: 1000°C 5 Min. preheat in O_2 + N_2

5 Min. push in O_2 + N_2

5 Min. warm-up in O_2 + N_2

10 Min. dope in O_2 + N_2 + dopant

5 Min. hold in O_2 + N_2

5 Min. pull in O_2 + N_2

10 Min. cool in O_2 + N_2

d) Phosphorous deglaze: 10 Sec. in 10% HF

e) drive-in: 950°C 5 Min. preheat in O_2

5 Min. push in O_2

5 Min. dry oxidation in O_2

20 Min. wet oxidation in O_2 + H_2O

5 Min. dry oxidation in O_2

5 Min. pull in O_2

10 Min. cool in O_2

5. Open windows for intrinsic base implant

   a) Use mask CU-063-02 with negative photoresist to pattern the windows. negative photoresist was also used to protect the back of the wafers.

   b) Etched in buffered HF for approximately 4 Min. until bare silicon exposed.

6. Implant mask oxide growth

   a) RCA clean

   b) drive-in: 1000°C

5 Min. preheat in O_2

5 Min. push in O_2

30 Min. dry oxidation in O_2+2.5% HCl

5 Min. dry oxidation in O_2

10 Min. hold in N_2

5 Min. pull in O_2

10 Min. cool in O_2

7. Intrinsic base boron implant

   Implant dosage : $1x10^{12}$ cm^{-2}

   Implant energy : 50 KeV

8. Base implant Anneal

a) RCA clean

b) Anneal: 950°C
5 Min. preheat in N_2
2"/6 Sec. push in N_2
30 Min. anneal in N_2
2"/15 Sec. pull in N_2
10 Min. cool in N_2

9. Open emitter contact windows
   a) Use mask CU-063-03 with negative photoresist to pattern window.
   b) Etch in buffered HF for approximatly 40 Sec. until silicon exposed.
10. Open base contact windows
   a) Use mask CU-063-05 with negative photoresist to pattern window.
   b) Etch in buffered HF until silicon exposed.
11. Lotox deposition
   Deposit 0.1 μm undoped Lotox, using 25% SiH_4 and 27.5% O_2 at temperature of 405°C for 6 Minutes.
12. Re-open base contact windows
   a) Use mask CU-063-05 with negative photoresist to pattern window.
   b) Etch in buffered HF for approximatly 50 Sec. until silicon exposed.
13. Deposit base contact metal
   a) Flash dip in 10% HF to remove native oxide from

windows

b) Deposit 1.0 μm Al on wafer fronts by e-beam

14. Pattern base contacts

a) Use Mask CU-063-06 with Positive photoresist.

b) Etch in H_3PO_4 at 60°C for approximately 2 Minutes.

15. Base contact anneal

Anneal in H_2 at 450°C for 10 Minutes.

16. Deposit protective Lotox layer

Deposit 0.2 μm Lotox using 25% SiH_4 and 27.5% O_2 at 405°C for 12 Minutes.

17. Partial RCA clean

The HF clean step was moved to the end and the duration was shortened to approximatly 3 Seconds.

18. Deposit back contact Al

Deposit 4000 Å of Al on wafer front by evaporation in the CHA chamber with filament current of 35 to 40 amps and deposition rate of 10 to 20 Å/Sec.

19. Grow ultra-thin tunnel oxide

Anneal and grow oxide : 500°C 5 Min. warm up in N_2
20 Min. dry grow in O_2
5 Min. hold in N_2

20. Deposit emitter metal

a) Deposit 3000 Å of Al on wafer front by evaporation in the CHA chamber with filament current of 35 to 40 amps and deposition rate of 10 to 20 Å/Sec. for Al-I-S devices.

b) Deposit 3000 Å of Mg on wafer front by evaporation in the CHA chamber using a "Drummel" type boat with filament current of 60 to 70 amps and deposition rate of 10 to 20 Å/Sec. for Mg-I-S devices.

c) Deposit 3000 Å of Ti on wafer front by evaporation in the CHA chamber with filament current of 90 to 100 amps and deposition rate of 2 to 5 Å/Sec. for Ti-I-S devices.

21. Pattern emitter metal

a) Use Mask CU-063-08 with Positive photoresist.

b) Etch in 50% H_3PO_4 at 60°C for approximately 2 Minutes for Al emitter.

c) Etch in 0.1% HNO_3 at 25°C for about 5 Minutes for Mg emitter.

d) Etch in 1% HF at 25°C for about 5 Minutes for Ti emitter.

A.2. Fabrication procedure for GT-J series devices

1. Mask oxide growth

a) RCA clean

b) Oxidation: 1100°C 5 Min. preheat in O_2
2"/6 Sec. push in O_2
10 Min. dry oxidation in O_2
20 Min. wet oxidation in $O_2 + H_2O$
10 Min. dry oxidation in O_2+ 2% HCl
10 Min. anneal in N_2
2"/15 Sec. pull in N_2

10 Min. cool in N_2

Mask oxide thickness ≃ 0.3 μm

2. Open windows for extrinsic base diffusion

   a) Use mask CU-078-01 with negative photoresist to pattern the windows. negative photoresist was also used to protect the back of the wafers.

   b) Etched in buffered HF for approximately 4 Min. until bare silicon exposed.

3. Extrinsic base boron diffusion

   a) RCA clean

   b) Predep: 1000°C
   5 Min. preheat in $O_2 + N_2$
   2"/6 Sec. push in $O_2 + N_2$
   5 Min. warm-up in $O_2 + N_2$
   10 Min. dope in $O_2 + N_2$ + dopant
   10 Min. hold in $O_2 + N_2$
   2"/15 Sec. pull in $O_2 + N_2$
   10 Min. cool in $O_2 + N_2$

   c) Boron deglaze: 30 Sec. in 10% HF

   d) drive-in: 1100°C
   5 Min. preheat in O_2
   2"/6 Sec. push in O_2
   15 Min. dry oxidation in O_2
   2"/15 Sec. pull in O_2
   10 Min. cool in O_2

4. Mask oxide growth

   a) 10 Sec. dip in 10% HF to remove any contamination from Boron drive-in tube.

b) Oxidation: 1100°C 5 Min. preheat in O_2
2"/6 Sec. push in O_2
15 Min. wet oxidation in $O_2 + H_2O$
5 Min. dry oxidation in O_2+2.5% HCl
5 Min. anneal in N_2
2"/15 Sec. pull in N_2
10 Min. cool in N_2

5. Phosphorous backside getter
   a) Protect wafer fronts with PR, and strip oxide from wafer backs.
   b) RCA clean
   c) Predep: 1000°C 5 Min. preheat in $O_2 + N_2$
   2"/6 Sec. push in $O_2 + N_2$
   5 Min. warm-up in $O_2 + N_2$
   10 Min. dope in $O_2 + N_2$ + dopant
   5 Min. hold in $O_2 + N_2$
   2"/15 Sec. pull in $O_2 + N_2$
   10 Min. cool in $O_2 + N_2$
   d) Phosphorous deglaze: 30 Sec. in 10% HF
   e) drive-in: 950°C 5 Min. preheat in O_2
   2"/6 Sec. push in O_2
   30 Min. dry oxidation in O_2
   2"/15 Sec. pull in O_2
   10 Min. cool in O_2
6. Open windows for intrinsic base implant

a) Use mask CU-078-02 with negative photoresist to pattern the windows. negative photoresist was also used to protect the back of the wafers.

b) Etched in buffered HF for approximately 3 Min. until bare silicon exposed.

7. Implant mask oxide growth

a) RCA clean

b) drive-in: 1000°C 5 Min. preheat in O_2
2"/6 Sec. push in O_2
5 Min. dry oxidation in O_2
30 Min. dry oxidation in O_2+2.5% HCl
10 Min. anneal in N_2
2"/15 Sec. pull in O_2
10 Min. cool in O_2

8. Intrinsic base boron implant

Implant dosage : $1x10^{12}$ cm^{-2}

Implant energy : 30 KeV

9. PSG deposition

Deposit PSG using 8.2% SiH_4, 20.2% SiH_4/PH_3 and 27.5% O_2 for 10 Minutes, and the thickness was approximatly 0.25 μm.

10. Base implant Anneal

a) RCA clean

b) Anneal: 627°C 5 Min. preheat in N_2
2"/6 Sec. push in N_2

60 Min. anneal in N_2

2"/15 Sec. pull in N_2

10 Min. cool in N_2

c) Anneal: 950°C 5 Min. preheat in N_2

2"/6 Sec. push in N_2

30 Min. anneal in N_2

2"/15 Sec. pull in N_2

10 Min. cool in N_2

11. Open emitter contact windows

a) Use mask CU-087-03 with negative photoresist to pattern window.

b) Etch in buffered HF for approximatly 1.5 Min. until silicon exposed.

12. Deposit first emitter polysilicon

a) RCA clean without HF etch.

b) Perform HF dip etch immediately before deposition.

c) Deposit polysilicon using 19.4% SiH_4 and 15% SiH_4/PH_3 for 55 minutes and the resulting thickness was approximatly 1000Å.

13. Pattern first polysilicon

a) Using mask CU-078-04 with positive photoresist.

b) Etch in wet poly etch.

14. Open base contact windows

a) Use mask CU-078-07 with negative photoresist to pattern window.

b) Etch in buffered HF for approximatly 4 Min. until silicon exposed.

15. Deposit base contact metal

a) Flash dip in 10% HF to remove native oxide from windows

b) Deposit 1.0 μm Al on wafer fronts by e-beam

16. Pattern base contacts

a) Use Mask CU-078-08 with Positive photoresist.

b) Etch in H_3PO_4 at 60°C for approximately 2 Minutes.

17. Base contact anneal

Anneal in H_2 at 450°C for 10 Minutes.

18. Deposit protective Lotox layer

Deposit 0.2 μm Lotox using 25% SiH_4 and 27.5% O_2 at 405°C for 12 Minutes.

19. Re-open first emitter window

a) Use mask CU-078-03 with negative photoresist.

b) Etch in siloxide etchant until polysilicon exposed.

20. Open second emitter window

a) Use mask CU-078-05 with negative photoresist.

b) Etch in siloxide etchant until bare silicon exposed.

21. Partial RCA clean

10 Second dip in 10% HF to remove any native oxide on the emitter window.

22. Deposit back contact Al

Deposit 4000 Å of Al on wafer front by evaporation in the CHA chamber with filament current of 35 to 40 amps and

deposition rate of 10 to 20 Å/Sec.

23. Grow ultra-thin tunnel oxide

Anneal and grow oxide : 500°C 5 Min. warm up in N_2
20 Min. dry grow in O_2
5 Min. hold in N_2

24. Deposit emitter metal

a) Deposit 3000 Å of Al on wafer front by evaporation in the CHA chamber with filament current of 35 to 40 amps and deposition rate of 10 to 20 Å/Sec. for Al-I-S devices.

b) Deposit 3000 Å of Mg on wafer front by evaporation in the CHA chamber using a "Drummel" type boat with filament current of 60 to 70 amps and deposition rate of 10 to 20 Å/Sec. for Mg-I-S devices.

24. Pattern emitter metal

a) Use Mask CU-078-09 with Positive photoresist.

b) Etch in 50% H_3PO_4 at 60°C for approximately 2 Minutes for Al emitter.

c) Etch in 0.1% HNO_3 at 25°C for about 5 Minutes for Mg emitter.

Appendix B.

Software listing for the MIS BJT Model

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
      C  PROGRAM MIS
      C  WRITTEN BY GARRY TARR SPRING 1982
      C  LAST REVISION JUNE 7 1982
      C
      C  MODIFLIED BY NGAM SZETO FALL 1986
      C  LAST REVISION NOV 3 1986
      C
      C
            IMPLICIT REAL*8 (A-Z)
            INTEGER CNTRL1,DATFL,FDFL,FREE,I,IADNR,IFAIL,ITMAX1,ITMAX2,KR,
           #        LABEL,LP,MINO,NTIMES,NTRAP
            LOGICAL NEWY,NEWA,NEWB
            EXTERNAL COMPF
      C
            DIMENSION NT(100),RHO(100),N1(100),P1(100),SIGMAN(100),
           #          SIGMAP(100),CN(100),CP(100),IADNR(100),TAUM(100)
            DIMENSION ACCEST(2),X(2),F(2)
            DIMENSION FREE(1),LABEL(15)
            DIMENSION FDFLA(81),FDFLC(81),FDFLE(81),FDFLF(81),FDFLG(81)
      C
            COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
           #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
           #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
           #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
            COMMON /AREA2/ NT,RHO,N1,P1,CN,CP,TAUM,IADNR,NTRAP
            COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
           #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
            COMMON /AREA4/ CNTRL1,ITMAX1,LP,NTIMES
            COMMON /AREA5/ CFD1,FDFLA,FDFLC,FDFLE,FDFLF,FDFLG
            COMMON /SE$$OM/ A(20,22),B(20),Y(22,21)
      C
            DATA EPSIO/8.85D-12/,HBAR/1.054D-34/,KBOLTZ/1.38054D-23/,
           #     KS/11.7D0/,ME/9.11D-31/,PI/3.14592654D0/,
           #     T/300.0D0/,VELTH/1.0D5/
            DATA FDFL/2/,DATFL/3/,KR/5/,FREE/'*'/
            DATA NEWY/.TRUE./,NEWA/.FALSE./,NEWB/.FALSE./
      C
      C
      C  READ IN DATA DESCRIBING DEVICE
      C
            READ(KR,5) (LABEL(I),I=1,15)
          5 FORMAT(15A4)
            READ(KR,FREE) ITMAX1,ITMAX2,ERR1,ERR2,DELY
            READ(KR,FREE) CNTRL1
      C
            READ(DATFL,FREE) NA,ND,CHISC,PHIM,MISTAR,D,KI,NCONV,AE,AH
            READ(DATFL,FREE) WB,TP,TN
            DO 100 I=1,100
            READ(DATFL,FREE) RHO(I),NT(I),SIGMAN(I),SIGMAP(I),TAUM(I),IADNR(I)
            IF(NT(I) .LE. 0.0D0) GOTO 200
      100   CONTINUE
      200   NTRAP=I-1
      C
            READ(FDFL,FREE) (FDFLF(I),FDFLA(I),FDFLC(I),FDFLE(I),
           #                 FDFLG(I),I=1,81)
      C
      C  ECHO PRINT
      C
```

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
      WRITE(LP,10) (LABEL(I),I=1,15)
   10 FORMAT('1',20X,15A4///)
      WRITE(LP,15) NA,ND,CHISC,PHIM,MISTAR,D,KI,NCONV
   15 FORMAT(1X,'NA=',D10.3,2X,'ND=',D10.3,2X,'CHIS=',F5.3,2X,'PHIM=',
     #F5.3,2X,'MISTAR=',F5.3,2X,'D=',D10.3,2X,'KI=',F5.2,2X,
     #'NCONV=',F7.5/)
      WRITE(LP,20) WB,TP,TN,AE,AH
   20 FORMAT(1X,'WB=',D10.3,2X,'TP=',D10.3,2X,'TN=',D10.3,2X,
     #'AE=',D10.3,2X,'AH=',D10.3,2X//)
      IF(NTRAP .EQ. 0) GOTO 400
      WRITE(LP,25)
   25 FORMAT(2X,'I:',3X,'ETA:',5X,'NT:',7X,'SIGMAN:',5X,'SIGMAP:',
     #5X,'TAUM:',5X,'IADNR:'/)
      DO 300 I=1,NTRAP
  300 WRITE(LP,30) I,RHO(I),NT(I),SIGMAN(I),SIGMAP(I),TAUM(I),IADNR(I)
   30 FORMAT(1X,I3,2X,F5.3,2X,D10.3,2X,3(D10.3,2X),I2)
      WRITE(LP,35)
   35 FORMAT(///)
C
C
C  NORMALIZE POTENTIALS TO KBOLTZ*T/Q AND COMPUTE CONSTANTS
C
  400 VTHERM=KBOLTZ*T/Q
      CTUNL=2.0D0*DSQRT(2.0D0*ME)/HBAR*DSQRT(Q)
      CFD1=PI*PI/6.0D0
      EPSIS=KS*EPSIO
      EPSII=KI*EPSIO
      NC=NI*DEXPL(EGAP/(2.0D0*VTHERM))*DSQRT(NCONV)
      NV=NI*DEXPL(EGAP/(2.0D0*VTHERM))/DSQRT(NCONV)
      EGAPI=EGAPI/VTHERM
      EGAP=EGAP/VTHERM
      CHISC=CHISC/VTHERM
      CHISV=EGAPI-CHISC-EGAP
      PHIM=PHIM/VTHERM
C
      CBCM=EGAPI-2.0D0*CHISC
      CCM=CHISC*(EGAPI-CHISC)
      CTNLCM=-CTUNL*D*DSQRT(CCM*MISTAR/EGAPI*VTHERM)
C
      CBVM=2.0D0*CHISV-EGAPI
      CVM=CHISV*(EGAPI-CHISV)
      CTNLVM=-CTUNL*D*DSQRT(CVM*MISTAR/EGAPI*VTHERM)
C
      NNO=NA
      PNO=NI*NI/NA
      PHIO=DLOG(NC/NA)
      PSISIO=DLOG(NA/PNO)
      CJVM=AH*T*T
      CJCM=AE*T*T
      CBAR=PHIO+CHISC-PHIM
      CPSII=D/EPSII/VTHERM
      CQS=DSQRT(2.0D0*KBOLTZ*T*EPSIS)
      IF(NTRAP .EQ. 0) GOTO 600
      DO 500 I=1,NTRAP
      RHO(I)=RHO(I)/VTHERM
      CN(I)=SIGMAN(I)*VELTH
      CP(I)=SIGMAP(I)*VELTH
      N1(I)=NC*DEXPL(RHO(I)-EGAP)
```

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
  500   P1(I)=NV*DEXPL(-RHO(I))
C
C
C  READ IN VOLTAGE V AND A STARTING ESTIMATE FOR PHI
C
600   READ(KR,FREE,END=1400) VBE,VCE,PHI
      VBE=VBE/VTHERM
      VCE=VCE/VTHERM
      PHI=PHI/VTHERM
C
      U=VBE-PHI
C  GIVEN PHI, COMPUTE A STARTING ESTIMATE FOR PSIS
      CALL FPSIS
C
C  CALL SSM TO FIND A SOLUTION FOR THE COUPLED POTENTIAL
C  AND HOLE CURRENT CONTINUITY EQUATIONS
C
      NTIMES=0
      X(1)=U
      X(2)=PSIS
      DO 700 I=1,3
      Y(1,I)=U
      Y(2,I)=PSIS
700   Y(I,I)=Y(I,I)+DELY
      NEWY=.TRUE.
      CALL SSM(X,F,2,0,ERR1,ITMAX2,COMPF,NEWY,NEWA,NEWB,IFAIL,&800)
800   U1=X(1)
      PSIS1=X(2)
      NEWY=.FALSE.
C  CALL SSM AGAIN TO OBTAIN AN ESTIMATE OF THE ERROR IN THE SOLUTION
      CALL SSM(X,F,2,0,ERR2,ITMAX2,COMPF,NEWY,NEWA,NEWB,IFAIL,&900)
C
C  PREPARE FOR OUTPUT OF RESULTS
C
900   U=X(1)
      PSIS=X(2)
      PHIER=DABS(U-U1)*VTHERM
      PSISER=DABS(PSIS-PSIS1)*VTHERM
      PHI=VBE-U
      UO=U*VTHERM
C
      CALL FQS
C
      JVT=0.0D0
      JCT=0.0D0
      JMT=0.0D0
      QSS=0.0D0
      IF(NTRAP .EQ. 0) GOTO 1300
      CVALEN=PHIO-EGAP+PSIS
      DO 1200 I=1,NTRAP
      ZETA=CVALEN+RHO(I)+V
      FM=1.0D0/(1.0D0+DEXPL(ZETA))
      FTNUM=NSURF*CN(I)+P1(I)*CP(I)+FM/TAUM(I)
      FTDNM=(NSURF+N1(I))*CN(I)+(PSURF+P1(I))*CP(I)+1.0D0/TAUM(I)
      FT=FTNUM/FTDNM
      IF(IADNR(I) .EQ. 1) GOTO 1000
      QSS=QSS-FT*Q*NT(I)
      GOTO 1100
```

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
 1000  QSS=QSS+(1.0D0-FT)*Q*NT(I)
 1100  JVT=JVT+Q*NT(I)*CP(I)*(PSURF*FT-P1(I)*(1.0D0-FT))
       JCT=JCT+Q*NT(I)*CN(I)*(NSURF*(1.0D0-FT)-N1(I)*FT)
 1200  JMT=JMT+Q*NT(I)*(FT-FM)/TAUM(I)
 1300  PSII=CPSII*(QS+QSS)
C
       ETAMC=-(PHIO+PSIS+VBE)
       ACM=-PSII*PSII
       BCM=PSII*CBCM
       CORFCT=1.0D0+(BCM/4.0D0+ACM/6.0D0-BCM*BCM/24.0D0/CCM)/CCM
       THCM=DEXPL(CTNLCM*CORFCT)
       JCM=CJCM*THCM*(FD1(ETAC)-FD1(ETAMC))
C
       CALL FJVM
C
       CALL FJBASE
C
C EXCHANGE THE TWO TUNNELING CURRENT COMPONENTS
C
       TEMP=JCM
       JCM=JVM
       JVM=TEMP
       TEMP=JCT
       JCT=JVT
       JVT=TEMP
C
       JRE=JNO-JNWB
       VCB=VBE-VCE
       WCB=DSQRT(2*EPSIS/Q*(ND+NA)/(ND*NA)*(0.7-VCB*VTHERM))
       JGEN=Q*NI*WCB/DSQRT(TN*TP)
       JCBP=Q*DP*NI*NI/DSQRT(DP*TP)/ND
       JE=JCM+JVM+JMT
       JC=JNWB+JGEN+JCBP
       JB=JE-JC
       HFE=(JC-JCBP)/JB
C
       UO=U*VTHERM
       VBEO=VBE*VTHERM
       VCEO=VCE*VTHERM
       PHIO=PHI*VTHERM
       PSISO=PSIS*VTHERM
       PSIIO=PSII*VTHERM
       WRITE(LP,40) VBEO,VCEO,IFAIL
  40 FORMAT(1X,'VBE=',F8.5,3X,'VCE=',F8.5,3X,'IFAIL=',I4/)
       WRITE(LP,45) UO,PHIO,PHIER,PSISO,PSISER,PSIIO
  45 FORMAT(1X,'U=',D14.7,2X,'PHI=',D14.7,2X,'(PHIER=',D10.3,')',2X,
     #'PSIS=',D14.7,2X,'(PSISER=',D10.3,')',2X,'PSII=',D14.7/)
       WRITE(LP,50) PSURF,NSURF,ETAC,ETAV,ETAMC,ETAMV
  50 FORMAT(1X,'PSURF=',D14.7,2X,'NSURF=',D14.7,2X,'ETAC=',F8.4,2X,
     #'ETAV=',F8.4,2X,'ETAMC=',F8.4,2X,'ETAMV=',F8.4/)
       WRITE(LP,55) JCM,JVM,JCT,JVT,JMT
  55 FORMAT(1X,'JCM=',D11.4,2X,'JVM=',D11.4,2X,'JCT=',D11.4,2X,
     #'JVT=',D11.4,2X,'JMT=',D11.4,2X/)
       WRITE(LP,60) THCM,THVM
  60 FORMAT(1X,'THCM=',D11.4,2X,'THVM=',D11.4/)
       WRITE(LP,70) JE,JB,JC,HFE
  70 FORMAT(1X,'JE=',D11.4,2X,'JB=',D11.4,2X,'JC=',D11.4,2X,'HFE=',D11.4/)
       WRITE(LP,71) JNO,JNWB,JRE,JGEN,JCBP,JREC
```

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
  233        71 FORMAT(1X,'JNO=',D11.4,2X,'JNWB=',D11.4,2X,'JRE=',D11.4,2X,
  234          #       'JGEN=',D11.4/,1X,'JCBP=',D11.4,2X,'JREC=',D11.4////)
  235      C
  236           GOTO 600
  237      C
  238      C
  239      1400  STOP
  240           END
  241           BLOCK DATA
  242      C
  243           IMPLICIT REAL*8 (A-Z)
  244           INTEGER CNTRL1,ITMAX1,LP,NTIMES
  245      C
  246           COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
  247          #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
  248          #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
  249          #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
  250           COMMON /AREA4/ CNTRL1,ITMAX1,LP,NTIMES
  251      C
  252           DATA EGAP/1.079862456D0/,EGAPI/8.0D0/,Q/1.6021D-19/,LP/6/
  253          #,DN/3.878D-1/,DP/1.184D-1/,NI/1.45D16/
  254      C
  255           END
  256           SUBROUTINE COMPF(X,F)
  257      C
  258      C  THIS ROUTINE COMPUTES THE RESIDUE OF THE POTENTIAL AND
  259      C  HOLE CURRENT CONTINUITY EQUATIONS
  260      C
  261           IMPLICIT REAL*8 (A-Z)
  262           INTEGER CNTRL1,I,IADNR,ITMAX1,LP,NTIMES,NTRAP
  263      C
  264           DIMENSION X(2),F(2),TAUM(100),RHO(100),
  265          #          NT(100),CN(100),CP(100),N1(100),P1(100),IADNR(100)
  266      C
  267           COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
  268          #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
  269          #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
  270          #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
  271           COMMON /AREA2/ NT,RHO,N1,P1,CN,CP,TAUM,IADNR,NTRAP
  272           COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
  273          #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
  274           COMMON /AREA4/ CNTRL1,ITMAX1,LP,NTIMES
  275      C
  276           NTIMES=NTIMES+1
  277           U=X(1)
  278           PHI=VBE-U
  279           PSIS=X(2)
  280      C
  281           CALL FQS
  282      C
  283           QSS=0.0D0
  284           JVT=0.0D0
  285           IF(NTRAP .EQ. 0) GOTO 300
  286           CVALEN=PHIO-EGAP+PSIS
  287           DO 200 I=1,NTRAP
  288           ZETA=CVALEN+RHO(I)+V
  289           FM=1.0D0/(1.0D0+DEXPL(ZETA))
  290           FTNUM=NSURF*CN(I)+P1(I)*CP(I)+FM/TAUM(I)
```

```
      FTDNM=(NSURF+N1(I))*CN(I)+(PSURF+P1(I))*CP(I)+1.0D0/TAUM(I)
      FT=FTNUM/FTDNM
      IF(IADNR(I) .EQ. 1) GOTO 100
      QSS=QSS-FT*Q*NT(I)
      GOTO 200
100   QSS=QSS+(1.0D0-FT)*Q*NT(I)
200   JVT=JVT+Q*NT(I)*CP(I)*(PSURF*FT-P1(I)*(1.0D0-FT))
C
300   PSII=CPSII*(QS+QSS)
      F(1)=CBAR+VBE+PSIS+PSII
C
      CALL FJVM
      CALL FJBASE
      F(2)=JVM-JNO-JREC-JVT
C
      IF(CNTRL1 .EQ. 0) GOTO 400
      UO=U*VTHERM
      PSISO=PSIS*VTHERM
      WRITE(LP,5) NTIMES,UO,PSISO,F(1),F(2)
    5 FORMAT(1X,I3,2X,D23.16,2X,D14.7,2X,2(D14.7,2X))
C
400   RETURN
      END
      SUBROUTINE FQS
C
C  THIS ROUTINE COMPUTES THE CHARGE QS STORED ON THE SEMICONDUCTOR
C
      IMPLICIT REAL*8 (A-Z)
      INTEGER CNTRL1,ITMAX1,LP,NTIMES
C
      COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
     #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
     #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
     #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
      COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
     #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
      COMMON /AREA4/ CNTRL1,ITMAX1,LP,NTIMES
C
      PXN=PNO*DEXPL(PHI)
      NXN=NNO+PXN-PNO
      ETAC=-(PSIS+PHIO)
      NSURF=NC*FD102(ETAC)
      NNSURF=NC*FD302(ETAC)
      ETAV=-(EGAP-PHIO-PSIS-PHI)
      PSURF=NV*FD102(ETAV)
      PPSURF=NV*FD302(ETAV)
      ARGMNT=NNSURF-NXN+PPSURF-PXN+NA*PSIS
      IF(ARGMNT .GE. 0.0D0) GOTO 100
C
      WRITE(LP,5) ARGMNT
    5 FORMAT(1X,'WARNING: SQUARE OF SURFACE FIELD IS NEGATIVE',5X,D11.4)
      ARGMNT=0.0D0
C
100   QS=CQS*DSQRT(ARGMNT)
      IF(PSIS .LT. 0.0D0) QS=-QS
      RETURN
      END
      SUBROUTINE FJVM
```

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```
      C
      C  THIS ROUTINE COMPUTES THE CURRENT FLOW JVM BETWEEN THE
      C  VALENCE BAND AND THE METAL
      C
            IMPLICIT REAL*8 (A-Z)
      C
            COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
           #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
           #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
           #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
            COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
           #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
      C
            ETAMV=-(EGAP-PHIO-VBE-PSIS)
      C
            AVM=-PSII*PSII
            BVM=PSII*CBVM
            CORFCT=1.0D0+(BVM/4.0D0+AVM/6.0D0-BVM*BVM/24.0D0/CVM)/CVM
            THVM=DEXPL(CTNLVM*CORFCT)
      C
            IF (DABS(U) .GT. 1.0D-6) GOTO 200
            IF( (ETAV .GT. -4.0D0) .OR. (ETAMV .GT. -4.0D0) ) GOTO 100
            JVM=CJVM*THVM*DEXPL(ETAV)*U
            RETURN
      C
      100   JVM=CJVM*THVM*DLOG(1.0D0+DEXPL(ETAV))*U
            RETURN
      C
      200   JVM=CJVM*THVM*(FD1(ETAMV)-FD1(ETAV))
            RETURN
            END
            SUBROUTINE FJBASE
      C
      C  THIS ROUTINE COMPUTES THE MINORITY CARRIER HOLE CURRENT FLOWING
      C  INTO THE SEMICONDUCTOR
      C
            IMPLICIT REAL*8 (A-Z)
      C
            COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
           #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
           #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
           #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
            COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
           #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
      C
            PSISI=PSISIO-PHI
            IF(PSIS .GT. PSISI) PSISCR=PSISI
            IF(PSIS .LT. PSISI) PSISCR=PSIS
            IF(PSISCR .LT. 0.0D0) PSISCR=0.0D0
            VBC=VBE-VCE
            NBO=NI*NI/NA
            DNBO=NBO*(DEXPL(PHI)-1.0)
            DNBWB=NBO*(DEXPL(VBC)-1.0)
            LN=DSQRT(DN*TN)
            WBE=DSQRT(2*EPSIS/Q/NA*PSIS*VTHERM)
            WBEFF=WB-DSQRT(2*EPSIS/Q/NA*(0.7-VBC*VTHERM))-WBE
            IF (WBEFF .LE. 0.0) WRITE(6,9999)
      9999 FORMAT (1X,'WARNING THE BASE IS PUNCHED THROUGH !!!'/)
```

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```
      DENOM=2*LN*DSINH(WBEFF/LN)
      A=DNBWB-DNBO*DEXPL(-WBEFF/LN)
      B=DNBWB-DNBO*DEXPL(WBEFF/LN)
      JNO=-Q*DN*(A+B)/DENOM
      JNWB=-Q*DN*(A*DEXPL(WBEFF/LN)+B*DEXPL(-WBEFF/LN))/DENOM
      JREC=Q*WBE*NI*(DEXPL(PHI/2.0)-1)/2/TN
      RETURN
      END
      SUBROUTINE FPSIS
C
C  THIS ROUTINE COMPUTES PSIS GIVEN PHI, ASSUMING NO SURFACE STATES
C
      IMPLICIT REAL*8 (A-Z)
      INTEGER CNTRL1,I,ITMAX1,LP,NTIMES
C
      COMMON /AREA1/ CBAR,CBCM,CBVM,CCM,CVM,CHISC,CHISV,CJCM,
     #               CJVM,CPSII,CQS,CTNLCM,CTNLVM,EGAP,EGAPI,
     #               NC,NA,ND,NI,NNO,NV,Q,PHIO,PNO,
     #               PSISIO,VTHERM,WB,TP,TN,DN,DP,EPSIS
      COMMON /AREA3/ ETAC,ETAMC,ETAMV,ETAV,JVM,NSURF,PHI,PSII,PSIS,
     #               PSURF,QS,THVM,THCM,U,VBE,VCE,JNO,JNWB,JREC
      COMMON /AREA4/ CNTRL1,ITMAX1,LP,NTIMES
C
      CBARV=-(CBAR+VBE)
      IF(CBARV .GT. 0.0D0 ) GOTO 100
      IF(CBARV .LT. 0.0D0) GOTO 200
      PSIS=0.0D0
      RETURN
100   PSISLO=0.0D0
      PSISHI=CBARV
      GOTO 300
200   PSISLO=CBARV
      PSISHI=0.0D0
C
300   DO 500 I=1,ITMAX1
      PSIS=(PSISLO+PSISHI)/2.0D0
      CALL FQS
      PSII=CPSII*QS
      F1=PSIS+PSII-CBARV
      IF(F1 .EQ. 0.0D0) RETURN
      IF(F1 .GT. 0.0D0) GOTO 400
      PSISLO=PSIS
      GOTO 500
400   PSISHI=PSIS
500   CONTINUE
C
      RETURN
      END
      DOUBLE PRECISION FUNCTION FD1(ETA)
C
C  FERMI-DIRAC INTEGRAL OF ORDER ONE
C
      IMPLICIT REAL*8 (A-Z)
      INTEGER INDEX
C
      DIMENSION FDFLA(81),FDFLC(81),FDFLE(81),FDFLF(81),FDFLG(81)
C
      COMMON /AREA5/ CFD1,FDFLA,FDFLC,FDFLE,FDFLF,FDFLG
```

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```
      C
            IF(ETA .LT. -4.0D0) GOTO 100
            IF(ETA .GT. 4.0D0) GOTO 200
            X=(ETA+4.0D0)/0.1D0+0.5D0
            INDEX=X+1
            ETA0=DFLOAT(INDEX-41)*0.1D0
            DELETA=ETA-ETA0
            DXPETA=DEXPL(ETA0)
            FD1=FDFLF(INDEX)+DELETA*(DLOG(1.0D0+DXPETA)+
           #     DELETA/2.0D0/(1.0D0+1.0D0/DXPETA))
            RETURN
      C
      100   FD1=DEXPL(ETA)
            RETURN
      C
      200   FD1=-DEXPL(-ETA)+ETA*ETA/2.0D0+CFD1
            RETURN
            END
            DOUBLE PRECISION FUNCTION FD102(ETA)
      C
      C  FERMI-DIRAC INTEGRAL OF ORDER ONE-HALF
      C
            IMPLICIT REAL*8 (A-Z)
            INTEGER INDEX
      C
            DIMENSION FDFLA(81),FDFLC(81),FDFLE(81),FDFLF(81),FDFLG(81)
      C
            COMMON /AREA5/ CFD1,FDFLA,FDFLC,FDFLE,FDFLF,FDFLG
      C
            IF(ETA .LT. -4.0D0) GOTO 100
            IF(ETA .GT. 4.0D0) GOTO 200
            X=(ETA+4.0D0)/0.1D0+0.5D0
            INDEX=X+1
            ETA0=DFLOAT(INDEX-41)*0.1D0
            DELETA=ETA-ETA0
            FD102=FDFLE(INDEX)+DELETA*(FDFLC(INDEX)+DELETA/2.0D0*FDFLA(INDEX))
            RETURN
      C
      100   FD102=DEXPL(ETA)
            RETURN
      C
      200   FD102=-DEXPL(-ETA)+ETA*ETA/2.0D0+CFD1
            RETURN
            END
            DOUBLE PRECISION FUNCTION FD302(ETA)
      C
      C  FERMI-DIRAC INTEGRAL OF ORDER THREE-HALVES
      C
            IMPLICIT REAL*8 (A-Z)
            INTEGER INDEX
      C
            DIMENSION FDFLA(81),FDFLC(81),FDFLE(81),FDFLF(81),FDFLG(81)
      C
            COMMON /AREA5/ CFD1,FDFLA,FDFLC,FDFLE,FDFLF,FDFLG
      C
            IF(ETA .LT. -4.0D0) GOTO 100
            IF(ETA .GT. 4.0D0) GOTO 200
            X=(ETA+4.0D0)/0.1D0+0.5D0
```

Listing of MISBJT.S at 11:24:09 on MAY 15, 1988 for CCid=NSZE on G

```
      INDEX=X+1
      ETAO=DFLOAT(INDEX-41)*0.1D0
      DELETA=ETA-ETAO
      FD302=FDFLG(INDEX)+DELETA*(FDFLE(INDEX)+DELETA/2.0D0*FDFLC(INDEX))
      RETURN
C
100   FD302=DEXPL(ETA)
      RETURN
C
200   FD302=-DEXPL(-ETA)+ETA*ETA/2.0D0+CFD1
      RETURN
      END
      DOUBLE PRECISION FUNCTION DEXPL(X)
C
      IMPLICIT REAL*8 (A-Z)
C
      IF(X .LT. -150.0D0) GOTO 100
      DEXPL=DEXP(X)
      RETURN
100   DEXPL=0.0D0
      RETURN
      END
```