A SAMPLING-TYPE FUNCTION GENERATOR AND FOUR-QUADRANT ANALOG MULTIPLIER

by

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ABSTRACT

This thesis describes the design and development of a sampling-type function generator and a four-quadrant analog multiplier. The project is divided into two parts, the general arrangement and circuitry of the function generator and multiplier, and the timing circuits which actuate them. This thesis is concerned with the general circuitry.

The functions to be generated are photographed on 35 mm. film and mounted in standard frames which are then fastened to the rim of a rotating disk. An optical system is used to scan the functions in a time-sequential manner. A timing system selects the required abscissa and actuates a combination of electronic gates and clamping circuits which stores the voltage, E_f, representing the ordinate, and the voltage, E_M, representing the maximum of the function. These two stored voltages, E_f and E_M, are applied to separate sweep circuits which produce sweep outputs of $E_fN(t)$ and $E_MN(t)$ respectively. A system of comparator circuits and gates samples the $E_fN(t)$ at the instant a reference voltage, E, equals the sweep $E_MN(t)$. Since the sweeps, N(t) are identical, the value of $E_fN(t)$ at the instant of sampling is $\frac{EE_f}{E_M}$. This sequence of operations occurs for each function as it is scanned. Each successive multiplication is stored in its own storage unit.

All the circuits are designed to be self-calibrating to minimize error due to drift.

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I. Introduction

There is a definite need for an economical electronic computer of sufficient accuracy for solving complex engineering problems. Usually the greatest expense of such a computer lies in the function generator and in the precision components required for reasonable accuracy.

This thesis covers the basic design of a sampling type function generator and the complete design of a four-quadrant analog multiplier with the exception of the timing circuits. The design of the timing circuits was undertaken under a separate thesis by J.S. Fiorentino.

The electronic circuitry contains a number of gates, flip-flops, comparators, d.c. amplifiers, etc. The amplifiers are Philbrick operation plug-in units. * It was decided that all other standard circuits such as gates, flip-flops and comparators would also be built as plug-in units. The general circuitry is shown in block form for convenience and is built up of the standard plug-in units. Figure 1 shows the symbols assigned to these units.

* See appendix.

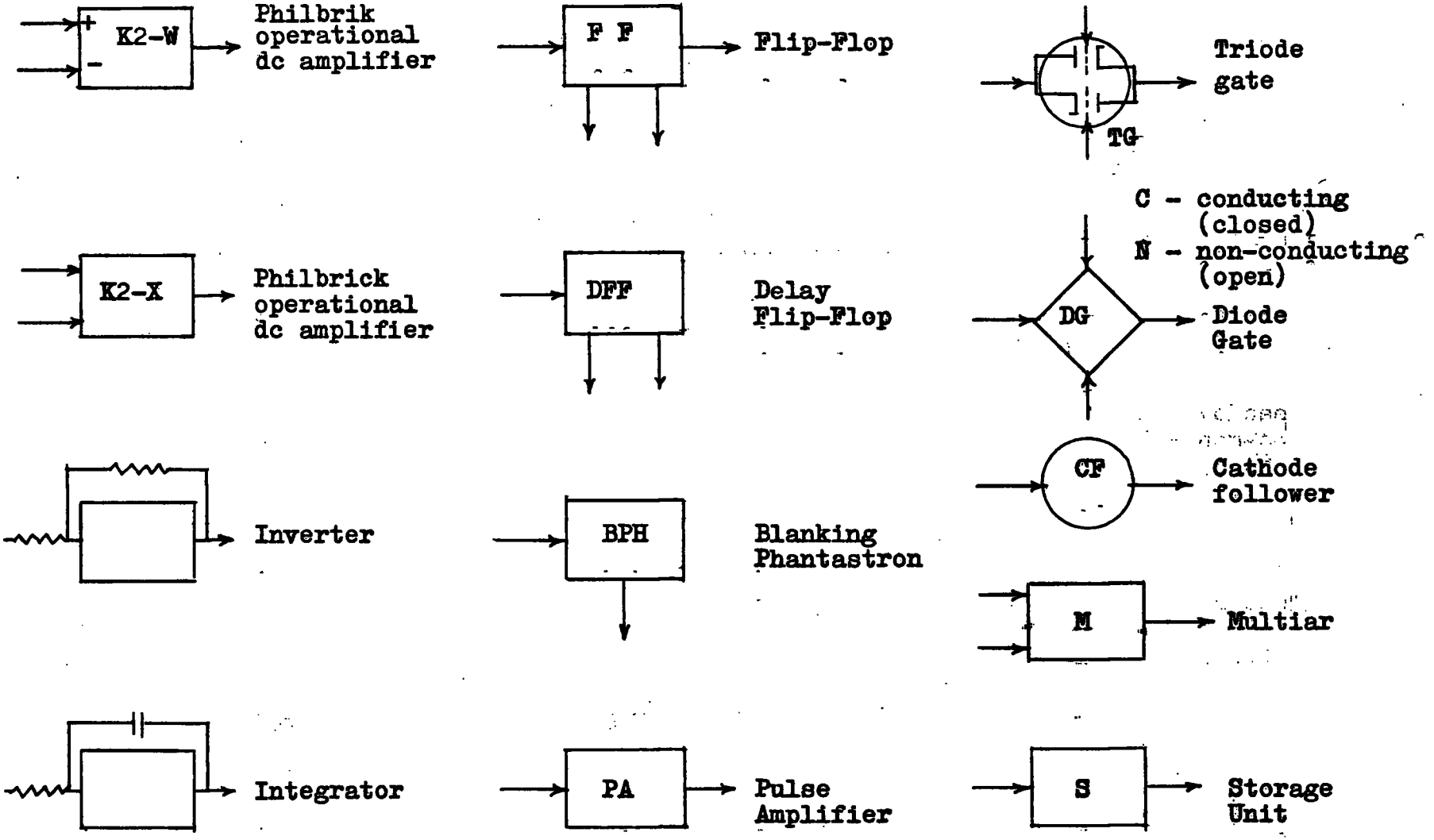


Fig. 1 Symbols for computer units.

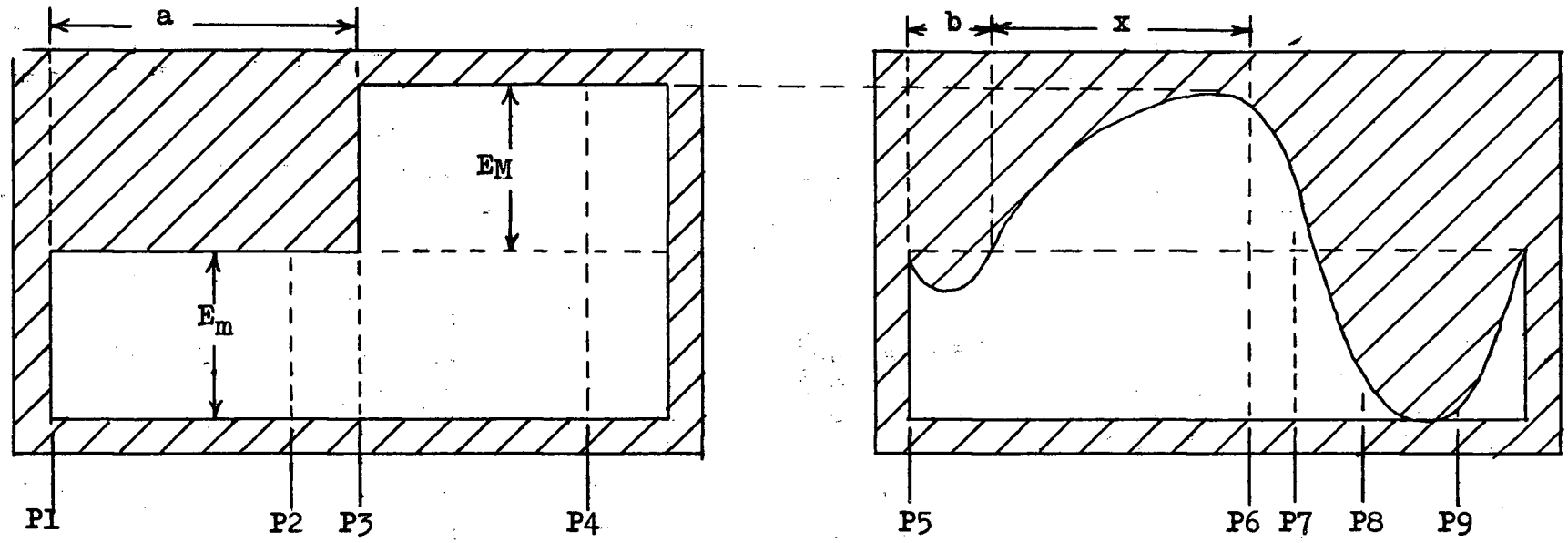
II Principle of Operation

The basic operation of the function generator is to generate a repetitive waveform representing all functions to be generated and then obtain the required ordinate values by sampling the waveform.

The simplest method of generating the required waveform is by means of film and an optical scanning system. This is the method used in the present investigation. Each function to be generated is photographed on 35 mm. film and mounted in a standard 35 mm. frame which is fastened to the rim of a rotating disk. The functions are drawn so that they all have the same maximum. The first frame on the disk is used for automatic calibration and contains the zero level and the maximum level of the following functions. Figure 2 shows the calibration frame and the first function frame together with the pulse sequence which operates the following circuitry.

A narrow beam of light from an optical system is passed through the negatives onto a photo-tube. The output of the photo-tube then represents the ordinate of all the functions in a time-sequential manner.

The linearity of this method depends on the uniformity of the photo-electric effect over the surface of the photo-tube. Tests made on a commercial type 917 photo-tube show that the departure from linearity is about 3%. This could be reduced by placing a mask in the light path. By careful shaping of the mask the error could be made very small.



Po - marker pulse
P1,P3,P5 - trigger pulses obtained from function frames
P2 - delayed pulse derived from P1
P4 - multiar pulse from timing circuits
P6 - sampling pulse from timing circuits
P7 - delayed pulse derived from P6
P8 - multiar pulse from multiplier
P9 - delayed pulse derived from P8

Fig. 2. Calibration and function frames on scanning disk

However, the non-linear characteristic of the photo-tube is the one big disadvantage of the optical system. The input is essentially an open loop and must be calibrated for each photo-tube. It should be possible to connect the input into a closed loop by using a servo to position the mask automatically, since the internal circuitry is arranged to be self-calibrating and capable of precision operation.

The output of the photo-tube is amplified by a d.c. amplifier. The zero level voltage (E_m) is held and fed back to the input of the amplifier by a system of gates and holding circuits. This sets the zero level and automatically corrects for amplifier drift. If the output of the photo-tube rises above E_m, the ouput of the amplifier is positive, and if it falls below E_m, the output is negative.

The block diagram for the function generator unit is shown in Figure 3.

The signal coming from the photo-tube amplifier is directed into three channels 1, 2, 3, and the timing circuit channel D. Channel 3 is the automatic bias circuit and operates as described below. When the calibration frame is scanned, pulse P1 occurs at the beginning of the frame. This pulse makes triode gate TG2 conducting and diode gate DG 15 non-conducting. When TG2 conducts, the feedback loop of the holding circuit closes. The storage unit is then able to charge up to the voltage $-E_m$. A second pulse, P2, makes TG 2 non-conducting, thus breaking the feed-back loop and leaving the storage unit charged to $-E_m$. The same pulse opens

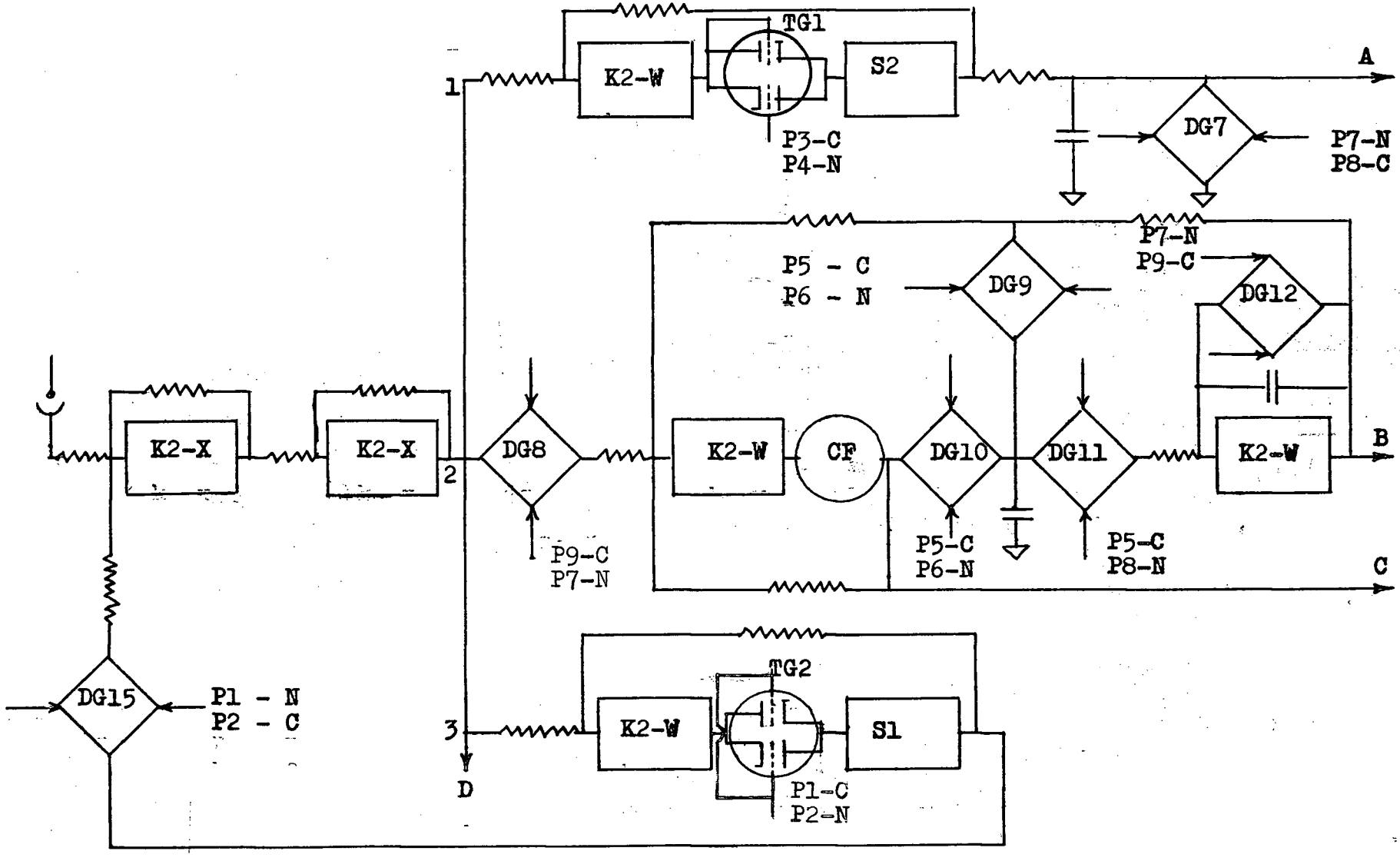


Fig. 3. Function generator assembly

DG 15 and feeds $-E_m$ back to the photo-tube amplifier. The amplifier now has an output of zero volts for an input of E_m volts. The calibration occurs once in every revolution of the function disk. This simple method solves the problem of drift and zero-level calibration.

The purpose of channel 1 will become more apparent when the multiplier is discussed. Its task is to store the maximum positive value of the functions and to generate a sweep which is needed for the multiplier.

As the calibrating frame is scanned by the photo-tube, the storage unit becomes charged to $-E_m$. The pulse P3 opens the second half of the triode gate TG 1 allowing the storage unit to discharge to $-E_M$ in the case when its former charge of $-E_m$ was larger than $-E_M$. The pulse P4 closes the gate leaving the storage unit charged to $-E_M$. The R_1C_1 combination produces the sweep required by the multiplier. The pulse P7 makes the gate DG 7 non-conducting, thus initiating the sweep, and P8 returns it to the ground. The ouput of channel 1 then goes to the multiplier circuit and its value is $-E_MN(t)$.

Channel 2 is the function circuit. Gates DG 8, 9, and 10 become conducting when the function frame begins, that is at P5. At the desired abscissa, determined by the timing circuit, P6 is generated. This pulse makes the above mentioned gates non-conducting, thus leaving the condenser C_2 charged to the inverted ordinate voltage $-E_f$. The pulse P7 makes DG 11 and 12 conducting, thus starting a sweep at B with value $+E_fN(t)$. This sweep is identical to

the one in channel 1, as will be shown later. Since DG 10, 9, and 8 are still non-conducting the sweep at C is inverted, i.e. $-E_f N(t)$.

The circuit diagram of the multiplier is shown in Figure 4. The multiar comparators (M) operate only if the reference voltage, E, is more positive than the sweep input. The original state of DG 16 is non-conducting and DG 17 conducting. If E is negative the inverted positive voltage, -E, is applied to M4. Since the second input of M4 is at ground potential, M4 generates a pulse. The pulse from M4 operates flip-flop FF8 which closes DG 16 and opens DG 17, thus applying the negative voltage, E, to M3. The pulse from M4 also opens DG 14 and closes DG 13. These gates lead to the storage circuits shown in Figure 5. The sweep $-E_M N(t)$ from channel 1 starts at P7 and is applied to M3. At the instant $E = E_M N(t)$ a pulse P8 is generated. This pulse opens DG 11 shown in Figure 3, thus stopping the sweep $-E_f N(t)$, leaving the storage circuit charged tc $-E_f N(t)$. Since the sweep is stopped at the instant $E = E_M N(t)$, and since the N(t) of channel 1 is identical with the N(t) of channel 2, it is obvious that the value stored is $-\frac{EE_f}{E_M}$.

If E is positive, diode gate DG 13 is open and DG 14 is closed. The voltage stored will then be $\frac{EE_f}{E_M}$.

From the above it can be seen that four-quadrant multiplication has been achieved. The pulse P9 resets the gates DG 12, 13, 14, 16, 17 as shown in the diagram.

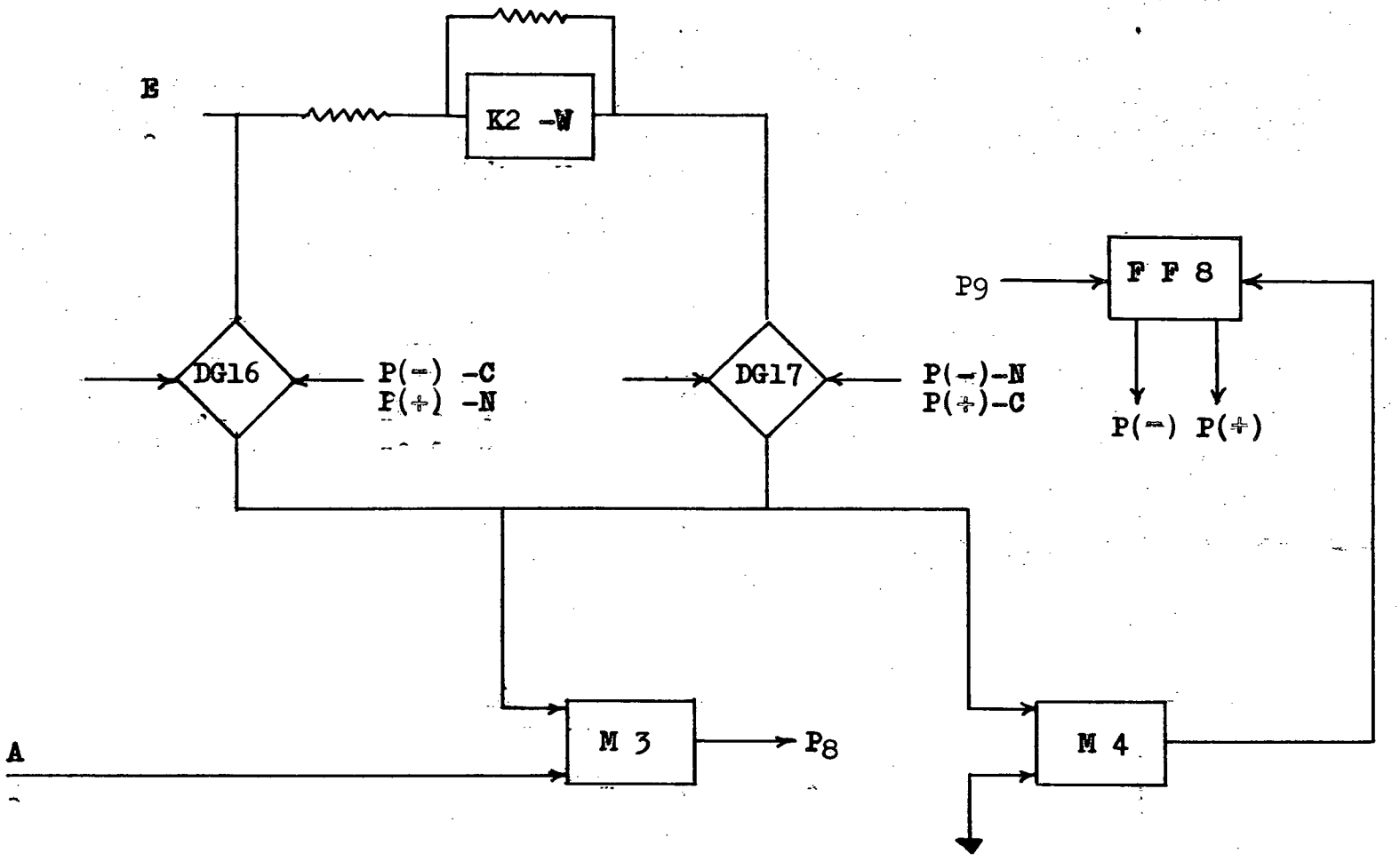


Fig. 4. Four Quadrant Multiplier.

The storage system which is shown in Figure 5 consists of a bank of storage units operated by a counter. A pulse P0 sets the first flip-flop to make the first storage channel open and sets all the other flip-flops so that the remaining channels are closed. The pulse P0 comes from a reference marker on the disk. The function generated from the first frame is stored in the first storage unit. The pulse P9 at the end of the multiplication sets the first storage channel in the closed position and opens the second. The operation repeats until all the functions have been processed and stored.

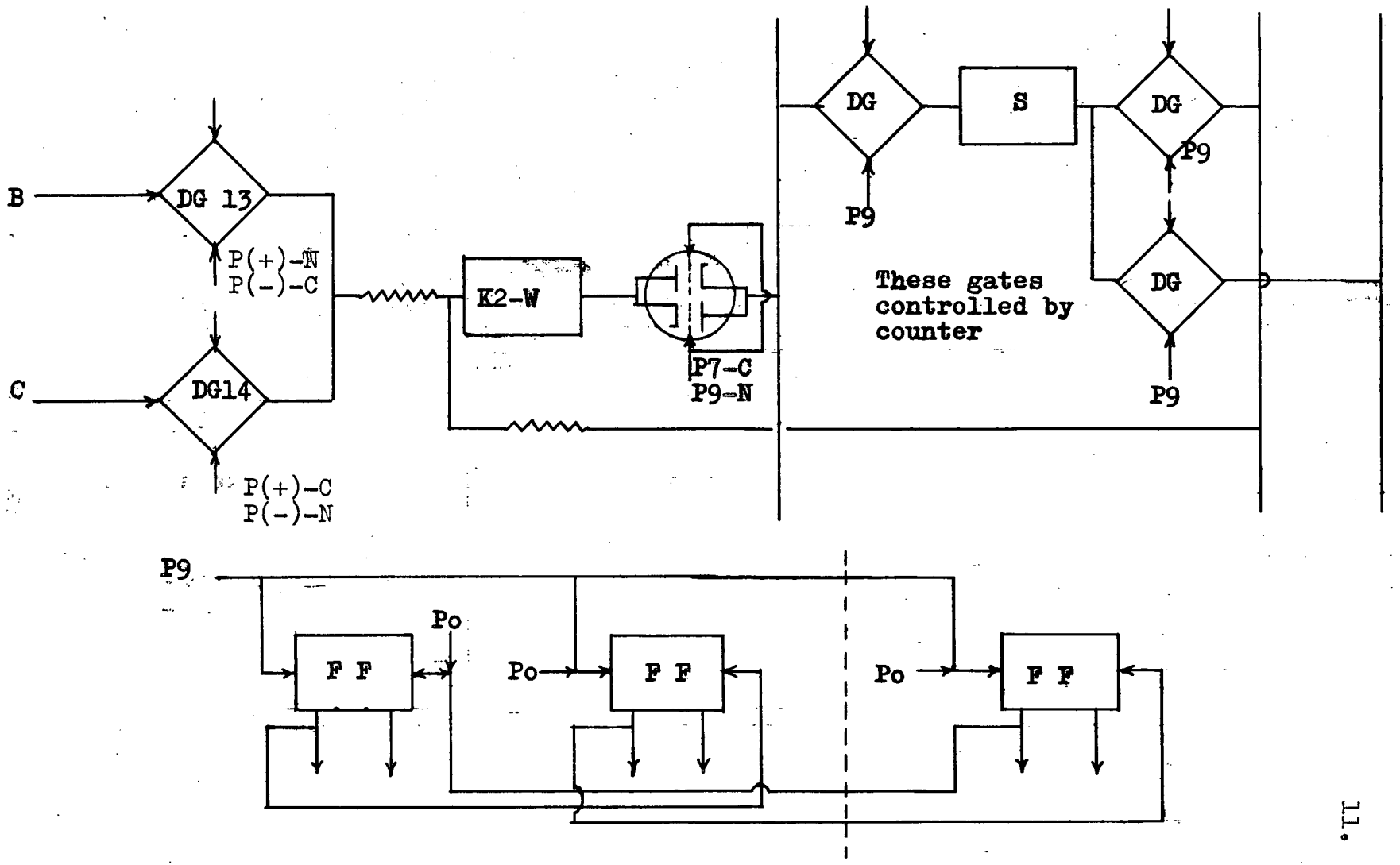


Fig. 5. Function Storage

III Detailed Circuit Design.

The circuits are designed to make use of standard components. The d.c. amplifiers used are Philbrick model K2-X and K2-W operational amplifiers. These amplifiers have a gain of 30,000 and 15,000 respectively. The K2-W output is ± 50 volts at ± 1 ma. and the K2-X maximum output is ± 100 volts at ± 2 ma. The amplifiers are used with 100% feed back in practically all cases. This provides maximum stability.

(1) Scanning Unit

The scanning unit consists of two parts; a rotating frame holder or disk and an optical system. The disk consists of a sixteen-inch diameter, one-quarter inch thick, steel disk, with an outer rim of aluminum three inches wide. The heavy centre of the disk acts as a fly-wheel, smoothing out any variations in the speed of the driving motor. The aluminum rim contains the clips to hold eighteen function frames. Figure 6 shows the construction.

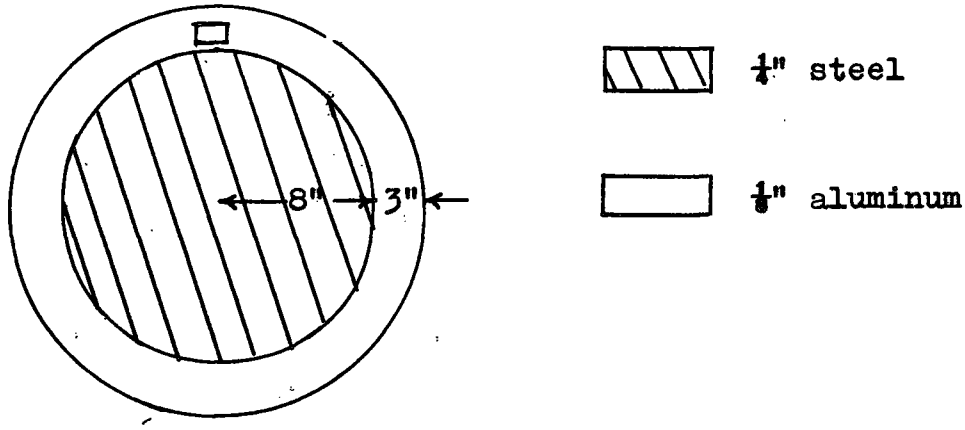


Figure 6. Rotating function disk.

The disk is driven by a one-tenth horsepower, 700 rpm, 110-volt direct-current shunt motor. The drive is transmitted through a rubber belt which also helps to smooth out any variations in the speed of the motor.

The light source is a 6-volt, direct current, straight, vertical filament lamp, which gives an intense vertically uniform light. The light is focused by cylindrical lenses so that the focal point of the narrow beam is at the film. The type 917 photo-tube is situated on the opposite side of the disk to the light source. Figure 7 shows the complete mechanical assembly.

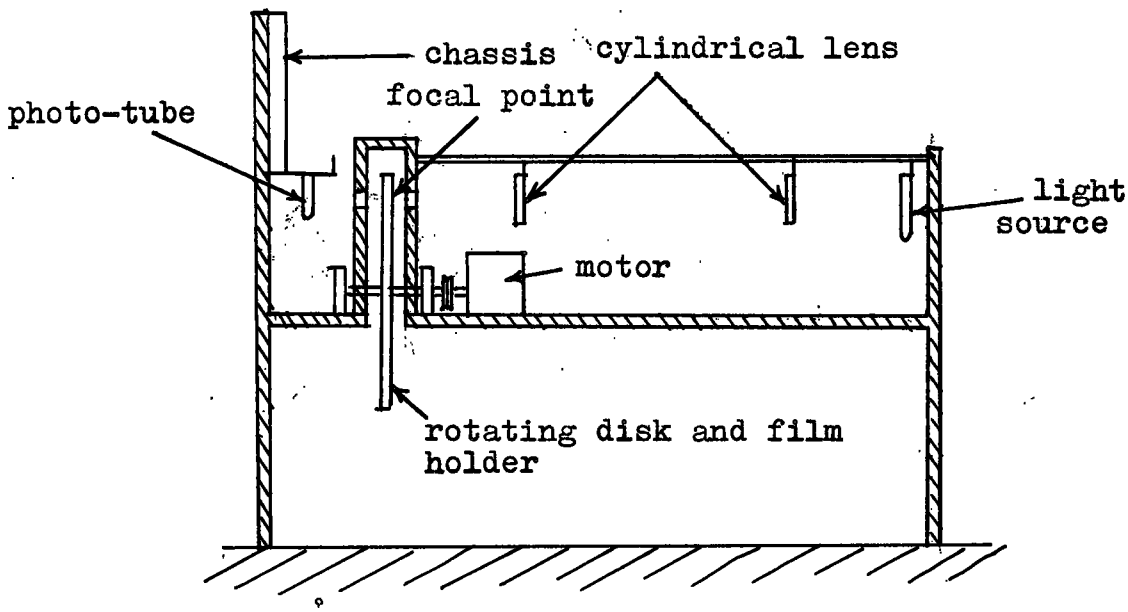


Figure 7. Scanning Unit Assembly.

The output of the photo-tube varies with the amount of light it receives and therefore represents the ordinate of

the functions passing through the beam of light. That is the output of the tube is amplitude modulated by the light beam.

(2) Photo-tube Amplifier.

The amplifier consists of the two Philbrick K2-X d.c. amplifiers in series. These have two inputs. The positive input, 1, is used when inversion is required and the negative input, 2, when inversion is not required. In the present application, inversion is normally required because negative feed-back is used. The positive input is then used for balance control.

The circuit diagram of the photo-tube amplifier appears in Figure 8.

R1, R2, R5, R6 - 1 Megohm

R3, R7 - 470 Kilohms

R4, R8 - 47 Kilohms

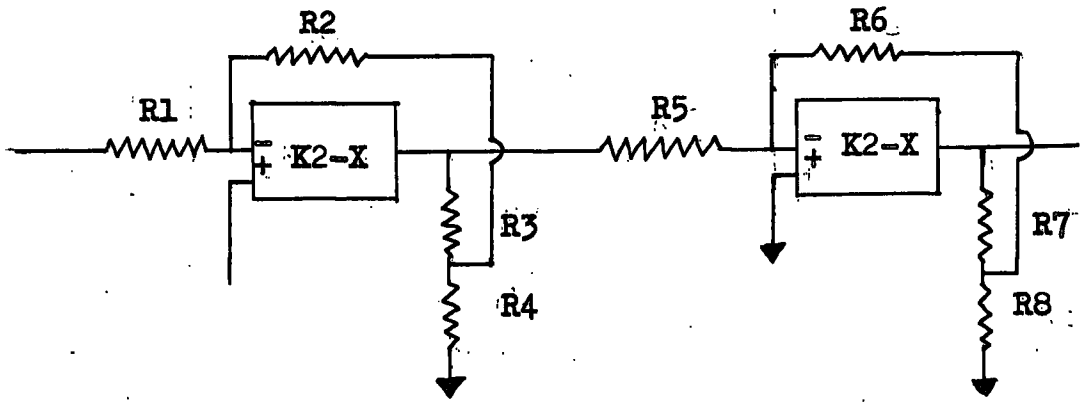


Figure 8. Photo-tube Amplifier.

The ouput of the photo-tube varies from zero to approximately 1 volt as the function varies between its negative and positive extremes. The output of the amplifier should represent the function, therefore a feedback system was designed to give zero output for zero input level, E_m.

The output of each amplifier is fed back to the input to give a gain of 10. The two in series then produce a gain of 100. The gain of 100 was chosen so that the maximum photo-tube signal, approximately 1 volt, would not overload the amplifiers which have a maximum output range of -50 to + 50 volts.

(3) Holding System of Channels 1 and 3.

Channels 1 and 3 operate principally as voltage-clamping circuits. The block diagram of the holding system is shown in Figure 9.

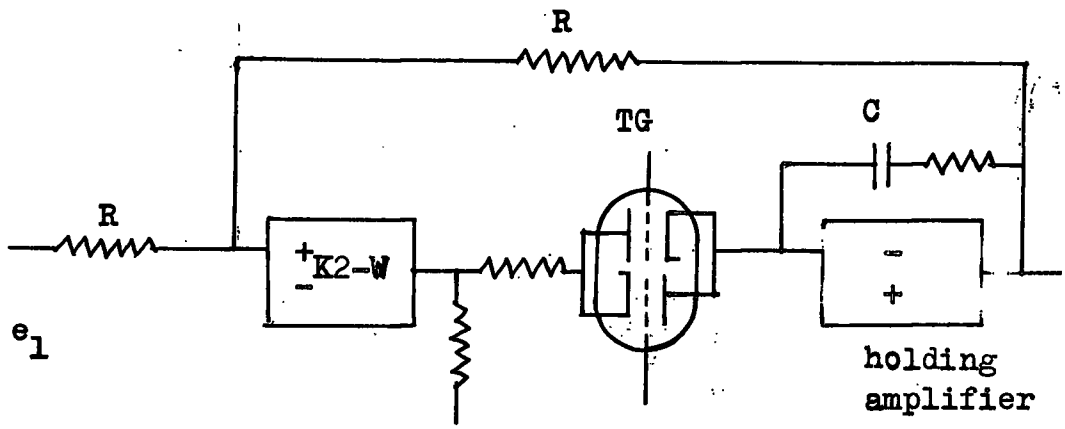


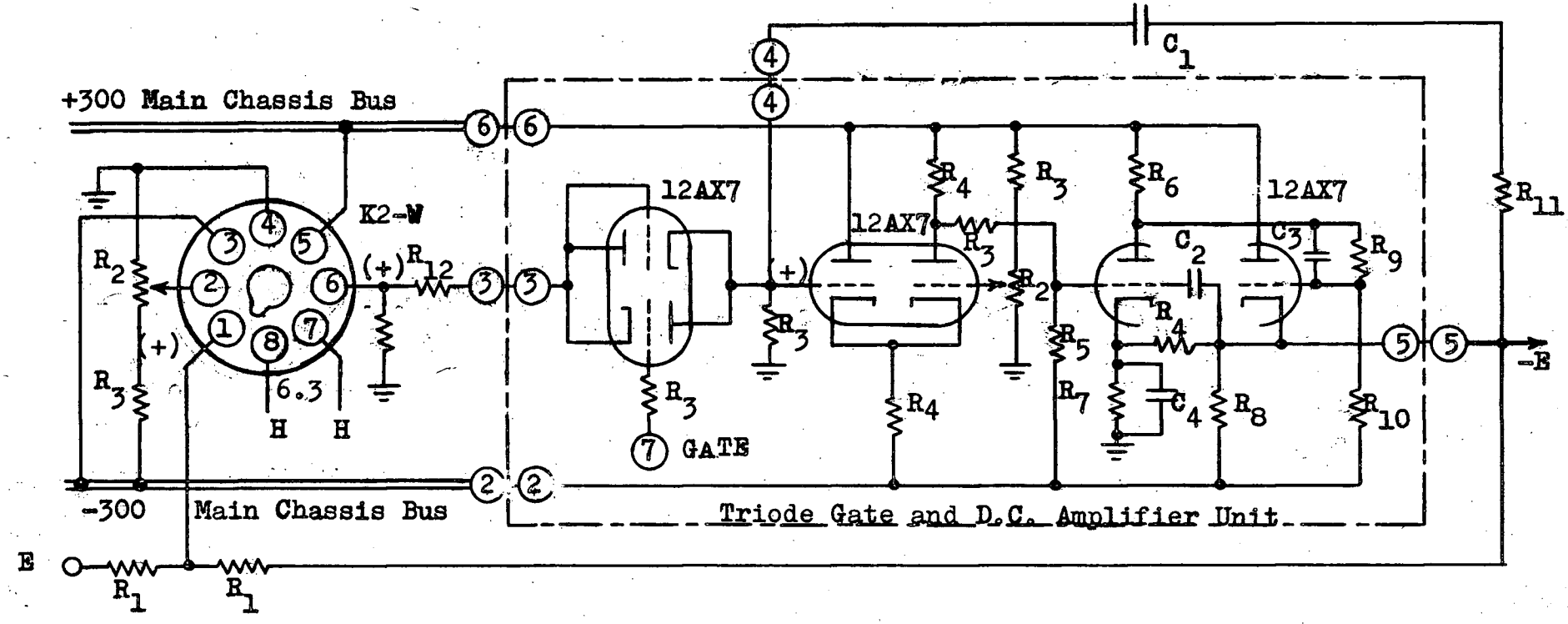
Figure 9. Holding system of Channel 1 and 3.

When a voltage e_1 is applied as shown, and the triode gate is made conducting, the condenser C charges up to this voltage. The amplifiers are connected so as to provide inversion at the output of the holding amplifier. That is, to obtain negative feed-back between the input of K2-W and the output of the holding amplifier, the positive (+) input of K2-W and the negative (-) input of the holding amplifier must be used. If the gate is made non-conducting, the feed-back loop is broken and the condenser C is left charged to $-e_1$. Any variation in the input no longer affects the output. If the charge begins to leak from the condenser, the change in potential is fed back to the input of the holding amplifier. This tends to make the ouput return to its original state.

The detailed circuit diagram of the holding system [1] appears in Figure 10.

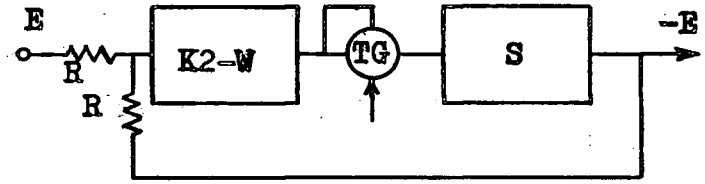
(4) Holding system of Channel 2.

The holding circuit used in channel 2 must be one which follows the varying function very rapidly. It need not hold the function for as long as the holding circuits in channels 1 and 3. Essentially, a condesner is charged through a d.c. amplifier. However, the condenser must be small in order to charge rapidly. At first a Philbrick K2-W amplifier was used to charge the condenser, but this proved to be too slow because of its low current output which is limited to one ma.



R_1: 1.0M 0.1%
R_2: 10K Pot, Mallory
R_3: 1.0 10%
R_4: 220K 10%
R_5: 2.2M 10%
R_6: 470K 10%
R_7: 68K 10%
R_8: 120K 10% 1 watt
R_9: 2.7M 10%
R_{10}: 4.7M 10%
R_{11}: 1500Ω 10%
R_{12}: 33K 10%
R_{13}: 15K 10%

All resistors are ½ watt unless otherwise noted.



REPRESENTATION

C_1 : 0.5 MFD Polystyrene (Low Leakage)
C_2 : 50 MMFD 600 VDC
C_3 : 10 MMFD 600 VDC
C_4 : 470 MMFD 600 VDC

For bidirectional control (positive and negative voltage storage) both control grids of TG are connected in series.

Figure 10: VOLTAGE STORAGE AND HOLDING CIRCUIT.

Suppose the value of the storage condenser is .001 microfarads. If the condenser is charged by the K2-W amplifier, the time of charging is as follows:

$$C = q/v = \frac{i \times t}{v}$$

Therefore $t = Cv/i$

If $V = 50$ volts and $i = 1$ ma.

$t = .001 \times 50 \times 10^{-3} = 50$ micro-seconds.

Since this time is too long the circuit in Figure 11 was developed. In this circuit a cathode follower is used inside the feed-back loop. Since the 12AU7 tube is capable of carrying 10 ma. average current and supplying up to 50 ma. current pulses, it was found to be satisfactory as a cathode follower. The bias to the K2-W amplifier is adjusted so that zero input gives zero output of the cathode follower.

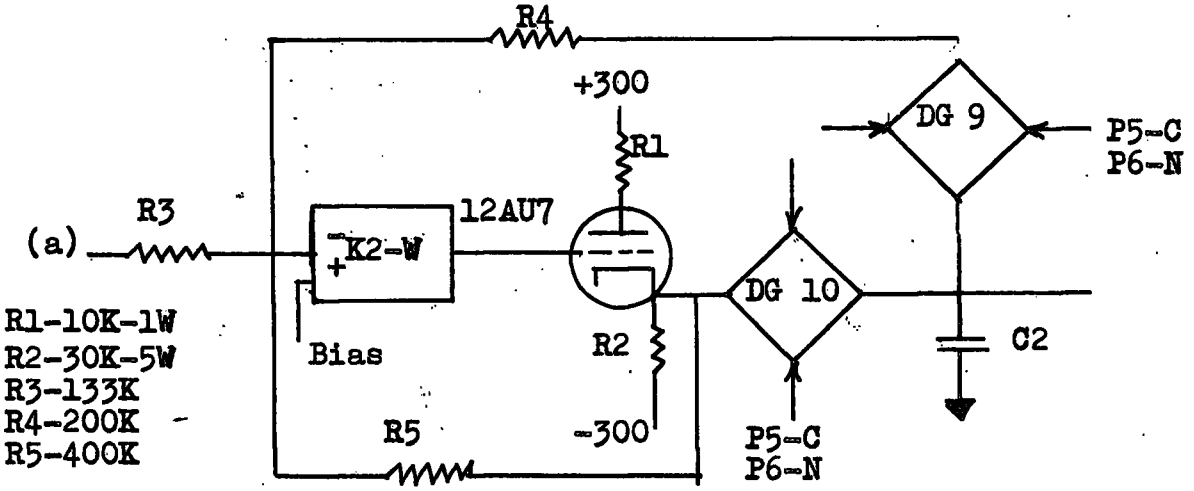


Figure 11. Holding circuit of Channel 2.

Suppose a negative step of 50 volts is applied at (a). The cathode follower is then made to conduct very strongly, say about 50 ma.

Then $t = \frac{CV}{i} = .001 \times 10^{-3} = 1$ micro-second.

If a positive step is applied to (a), the cathode follower is cut off and the condenser is charged from the -300 volt source through the 30K resistor. The time constant, R_2C_2, of the circuit is 30 microseconds. Let the voltage across C_2 be e_2 and the -300 volt supply voltage be e_1. The charging time of the condenser may be found as follows:-

$$\frac{e_2(p)}{e_1(p)} = \frac{R_2}{1 + pR_2C_2}$$

$e_2 =$ 50 volts maximum

$e_1 = -300$ volts

$$e_2(t) = e_1(t)\ (1 - e^{-t/R_2C_2})$$

$$e^{-t/R_2C_2} = \frac{-e_2}{e_1} + 1$$

$$t = R_2C_2 \ln 5/6$$

Therefore $t = 5.088 \times 10^{-6}$

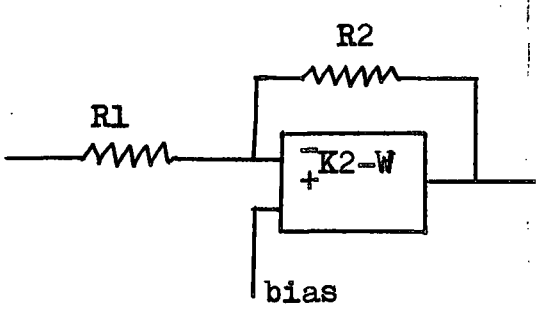
$= 5$ micro-seconds.

Since the function involved will probably never be a step type, the charging time will be less than 5 micro-seconds and may be considered to be negligible.

The diode gates in the circuit are used to isolate the condenser and leave it charged to the voltage representing the ordinate at the instant of sampling. The purpose of the parallel feed-back is to allow the amplifier to be used as the inverter in Channel 2 when charging has been completed.

(6) Inverters.

The inverters consist of a K2-W amplifier with 100% feed-back giving a gain of one. The inverter in Channel 1 is shown in Figure 12.



R1, R2 - 133K

Figure 12. Inverter of Channel 1.

As mentioned earlier, the inverter in Channel 2 employs the same amplifier that is used to charge the holding condenser. This can be done because the holding amplifier is inoperative during the time that the inverter is needed. The circuit diagram for the Channel 2 inverter is shown in Figure 13. The gates are non-conducting and therefore the K2-W amplifier and the cathode follower act as an inverter.

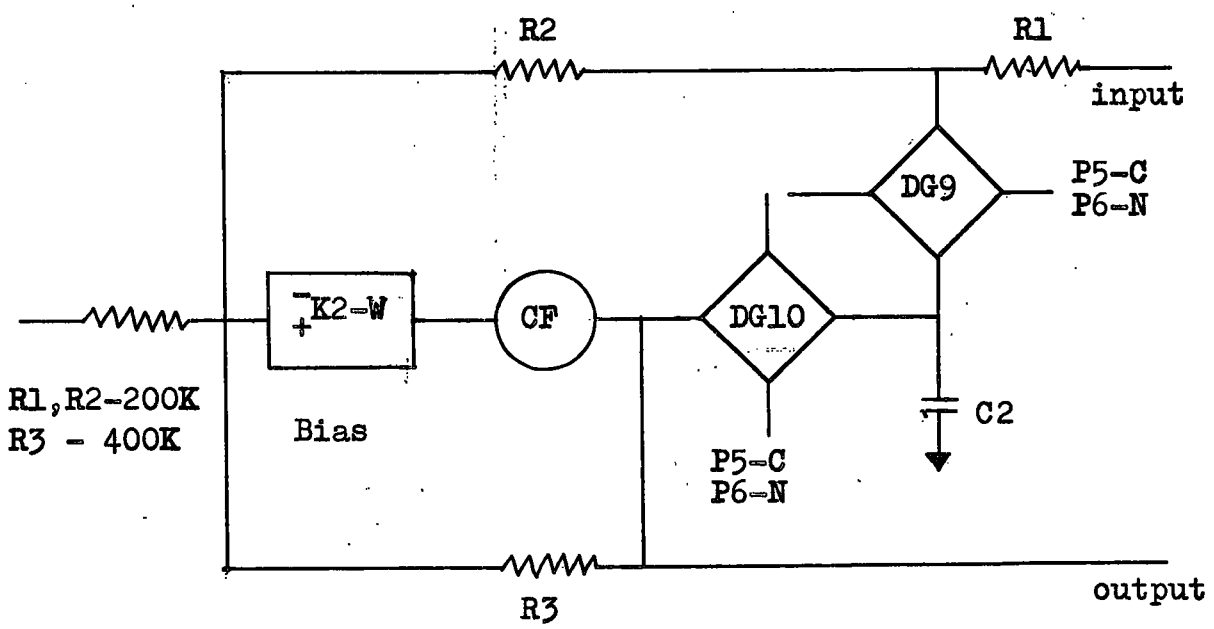


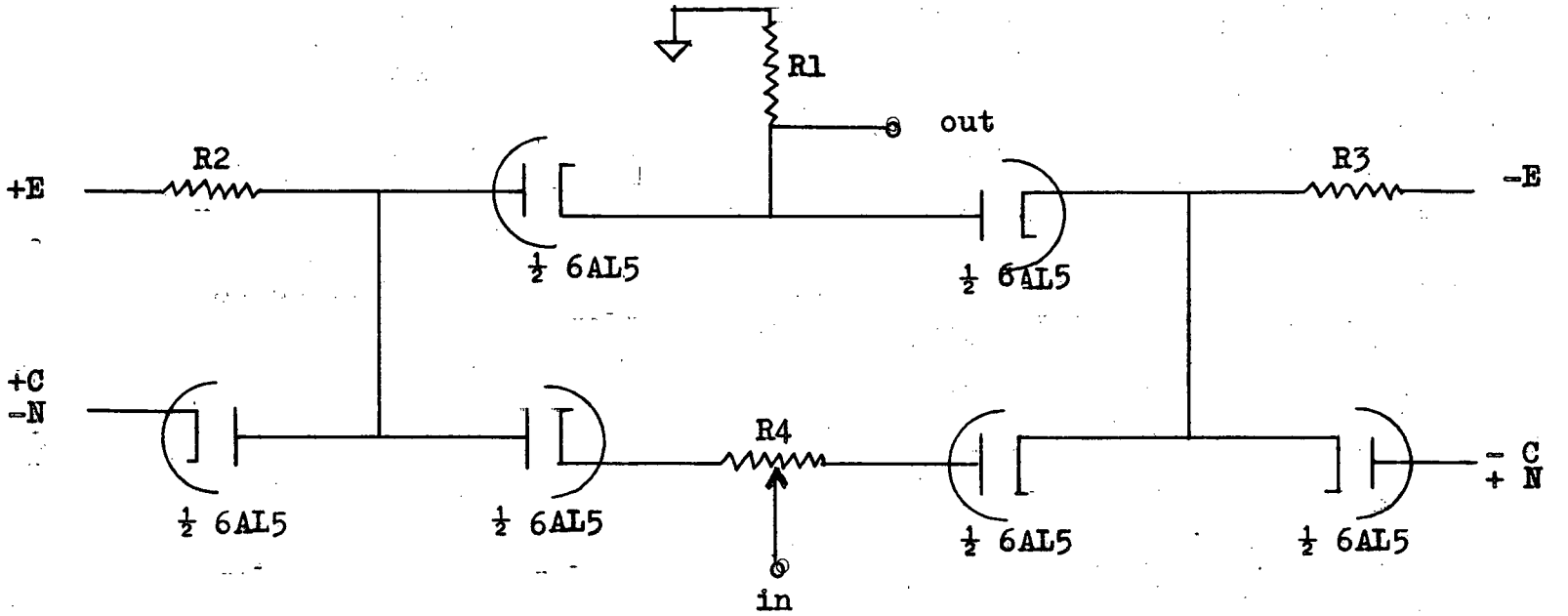
Figure 13. Inverter of Channel 2.

(7) Gates.

Two types of gates were investigated; the triode gate and the six-diode bridge-type gate.[2] The gates must be bi-directional and in most cases be capable of passing voltages with great accuracy. That is, the gain through the gate should be as close as possible to unity.

A double-triode can be used as a bi-directional gate, but it is extremely difficult, if not impossible, to obtain a consistently accurate gain level through the gate. The only circumstances under which triode gates can be used are inside a feed-back loop, where accuracy is not necessary. These were used in the holding systems of Channels 1 and 2 as mentioned previously.

In most cases diode gates are a necessity because a voltage must be passed accurately. The circuit diagram of



R1, R2, R3 - 1M
R4 - 1K

E - 300 volts
C - 60 volts
N - 60 volts

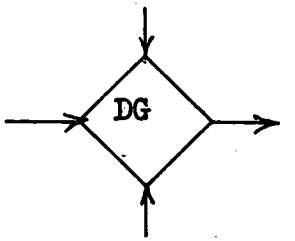


Fig. 14. Diode gate

the diode gate appears in Figure 14. The gate is designed to pass ± 50 volts maximum, since this is the highest voltage passed by the d.c. amplifiers. The control voltages are ± 60 volts. The tubes used are three 6AL5's. The accuracy of the gate was tested as shown in Figure 15. The results are given in Table 1.

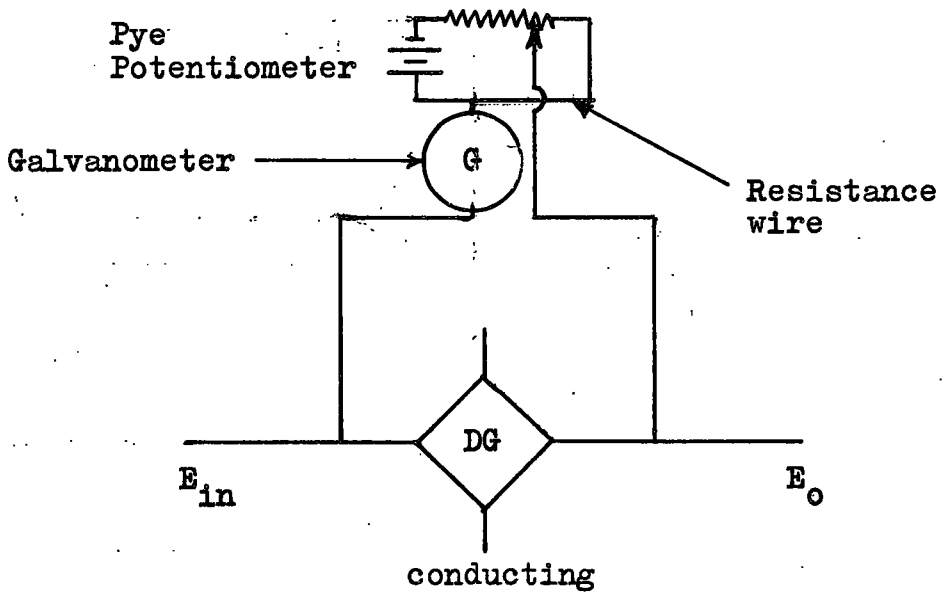


Figure 15. Test Setup for the Diode Gates.

Table 1.

Ein (volts)	Ein-Eo (volts)	% relative error
3.00	.01774	.59%
5.00	.03898	.78%
10.0	.05255	.53%
20.0	.07909	.39%
30.0	.10720	.35%
40.0	.13425	.33%
50.0	.16320	.33%
60.0	.19157	.32%
-60.0	.1608	.27%
-50.0	.12615	.25%
-40.0	.09119	.23%
-30.0	.05690	.19%
-20.0	.02824	.14%
-10.0	.00079	.008%

The greatest relative error occurs at an input of 5 volts. The gain at this point is:

$$G = \frac{E_o}{Ein} = \frac{5.00 - .03898}{5.00} = .992$$

(8) Sweep Circuits.

The sweep circuits of Channel 1 and 2 are different, but the sweeps are identical.

The sweep circuit of Channel 1 is an RC network with a diode gate from the output to ground. Figure 16 shows the circuit. The holding circuit prevents the input to the sweep from changing as the sweep progresses. The equation of the sweep is $e_o(t) = E_M(1 - e^{-t/R_1C_1})$.

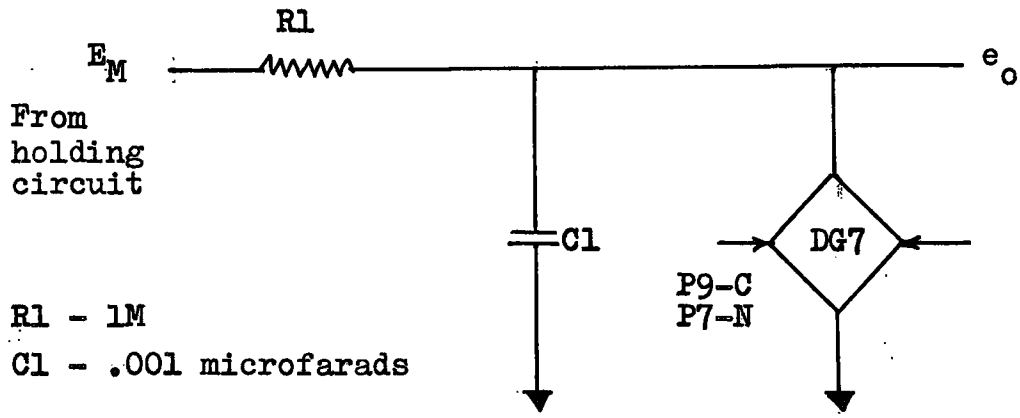


Figure 16. Sweep circuit of Channel 1.

The time constant, R_1C_1, is chosen as one milli-second because of the speed of scanning. The frames are eight inches from the centre of the disk so that at 700 rpm the linear speed of the frame is approximately 560 inches per second. The frame is about $1\frac{1}{2}$ inches wide, therefore the time required for one function to be scanned is 2.5 milli-seconds. The time between frames is 1.5 milli-seconds. If the function is sampled near the end of the frame, there is 1.5 milli-seconds for the sweep and comparators to act before the next function begins. Therefore, the sweep time-constant was chosen to be one milli-second. The gate starts the sweep when it is made non-conducting and stops the sweep when it is made conducting.

The sweep circuit of Channel 2 cannot be a simple RC network. The reason is that ordinate voltage E_f is held on a relatively small condenser. When the sweep starts, the charge

on the condenser is drained off, thereby reducing E_f. Hence some means of correcting for the voltage drop must be found. The solution is to use a direct-current amplifier with capacitative feed-back. The ciruit appears in Figure 17.

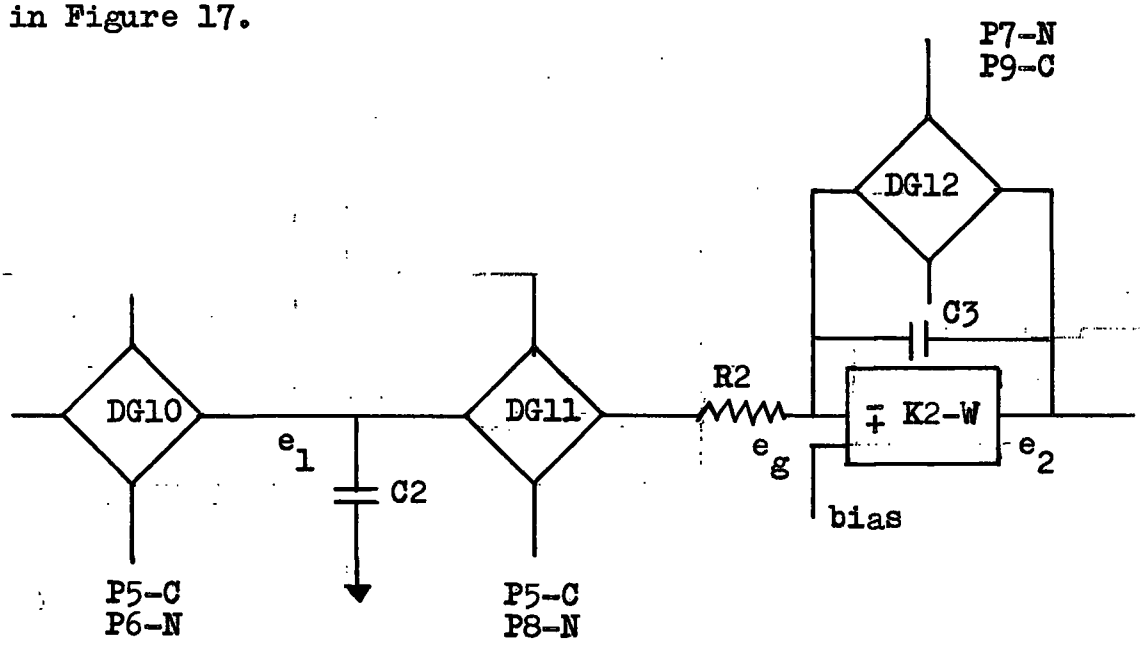


Figure 17. Sweep Circuit of Channel 2.

An analysis of the circuit with gate DG 11 conducting and DG 10 and DG 12 non-conducting, gives the following:

$$\frac{e_1 - e_g}{R_2} = \frac{e_g - e_2}{1/pC_3}$$

Since E_g is essentially zero because of the large gain

$$\frac{e_1}{R_2} = -e_2 pC_3 .$$

The capacitor C_1 discharges through R_2. Hence, if E is the original voltage on C_1,

$$e_{1(t)} = E\, e^{-t/R_2C_2}$$

and $$e_1(p) = \frac{E}{p + \frac{1}{R_2C_2}}$$

Therefore $$e_2(p) = -\frac{e_1(p)}{pR_2C_3} = -\frac{E}{R_2C_3}\left(\frac{1}{p(p + \frac{1}{R_2C_2})}\right)$$

Taking the inverse Laplace Transform:

$$C_2(t) = -E\frac{C_2}{C_3}\left(1 - e^{-t/R_2C_2}\right)$$

If $C_2 = C_3$,

$$e_2(t) = -E\left(1 - e^{-\frac{t}{R_2C_2}}\right)$$

which is the same as the sweep used in Channel 1 except for the sign. C_2 was determined by the requirements of the holding circuit and was set at .001 microfarad. In a preceding paragraph it was found that the sweep time-constant was one milli-second. This requires that R2 must be 1 megohm in both sweeps.

(8) Comparator.

Comparators of the multiar type were chosen because of their inherent simplicity and accuracy. The circuit diagram appears in Figure 18. The negative reference voltage on the plates of V1 keeps the diode from conducting. The tube V2 is normally conducting strongly and V3 is close to cutoff. When the

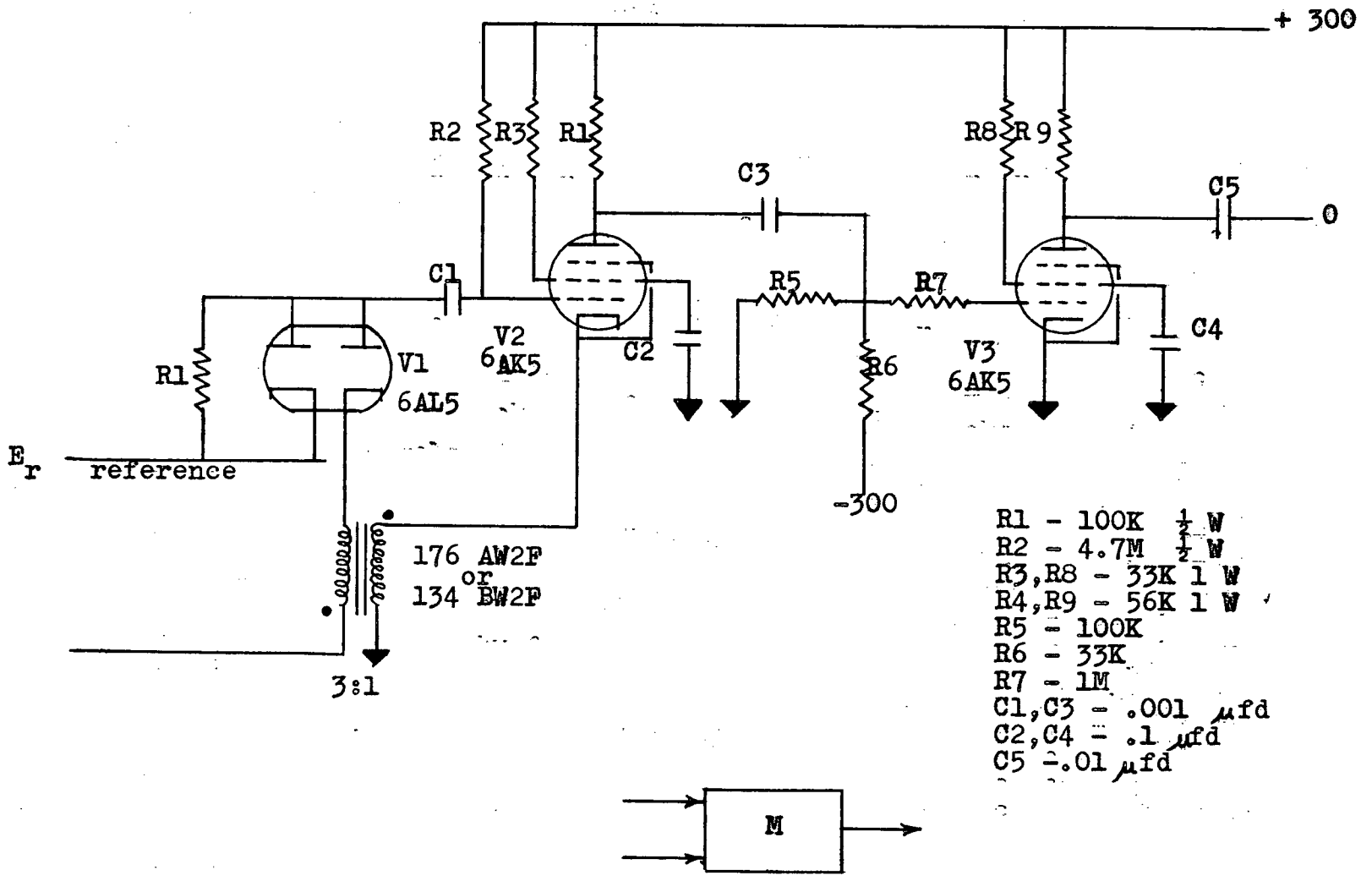


Fig. 18. Circuit diagram of multiar comparator

falling sweep reaches equality with the reference voltage, V1 conducts, thus completing the regerative loop. The regeneration drives the grid of V2 to cut-off very rapidly and as a result we get a large positive pulse at the plate of V2. The tube V3 is used to invert the pulse, although a pulse transformer could also be used for pulse inversion.

The charge on C1 discharges through R2 and makes V2 conducting again. This again closes the regenerative loop and causes another pulse. A train of pulses occurs until the sweep returns to a less negative value than the reference voltage. In actual practice the pulse is applied to a flip-flop which turns on the gate DG 7, thus stopping the sweep and returning it to ground. Therefore only the initial pulse is generated since V1 cuts off as soon as DG 7 conducts.

The rise time of the pulse is of the order of 1 to 2 microseconds and occurs again as soon as the sweep voltage is equal to the reference voltage. The pulse height is 230 volts.

IV Accuracy Test of Multiplier.

The circuit as a whole was not tested because no precision components or power supplies were available. However, a test procedure is desirable for future testing. The test set-up is shown in Figure 20.

As was shown earlier the equation of the sweep in channel 1 is

$$e_1(t) = E\,(1 - e^{-t/R_1C_1})$$

The equation of the sweep in channel 2 is

$$e_2(t) = E\,\frac{C_2}{C_3}\,(1 - e^{-t/R_2C_2})$$

If the sweeps are to be equal, R_2C_2 must equal R_1C_1 and C_2 equal C_3 .

R_2C_2 was matched to R_1C_1 as is shown in Figure 19.

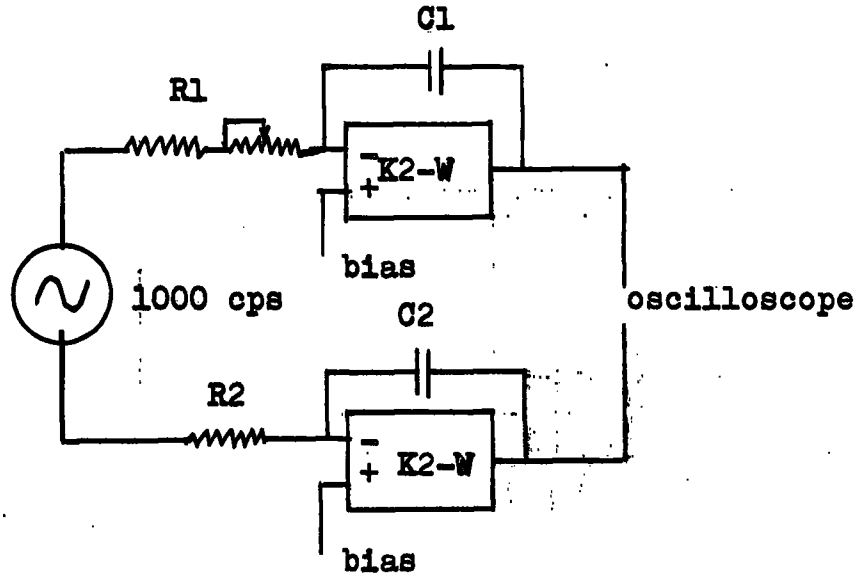


Figure 19. Circuit used to match Time Constants.

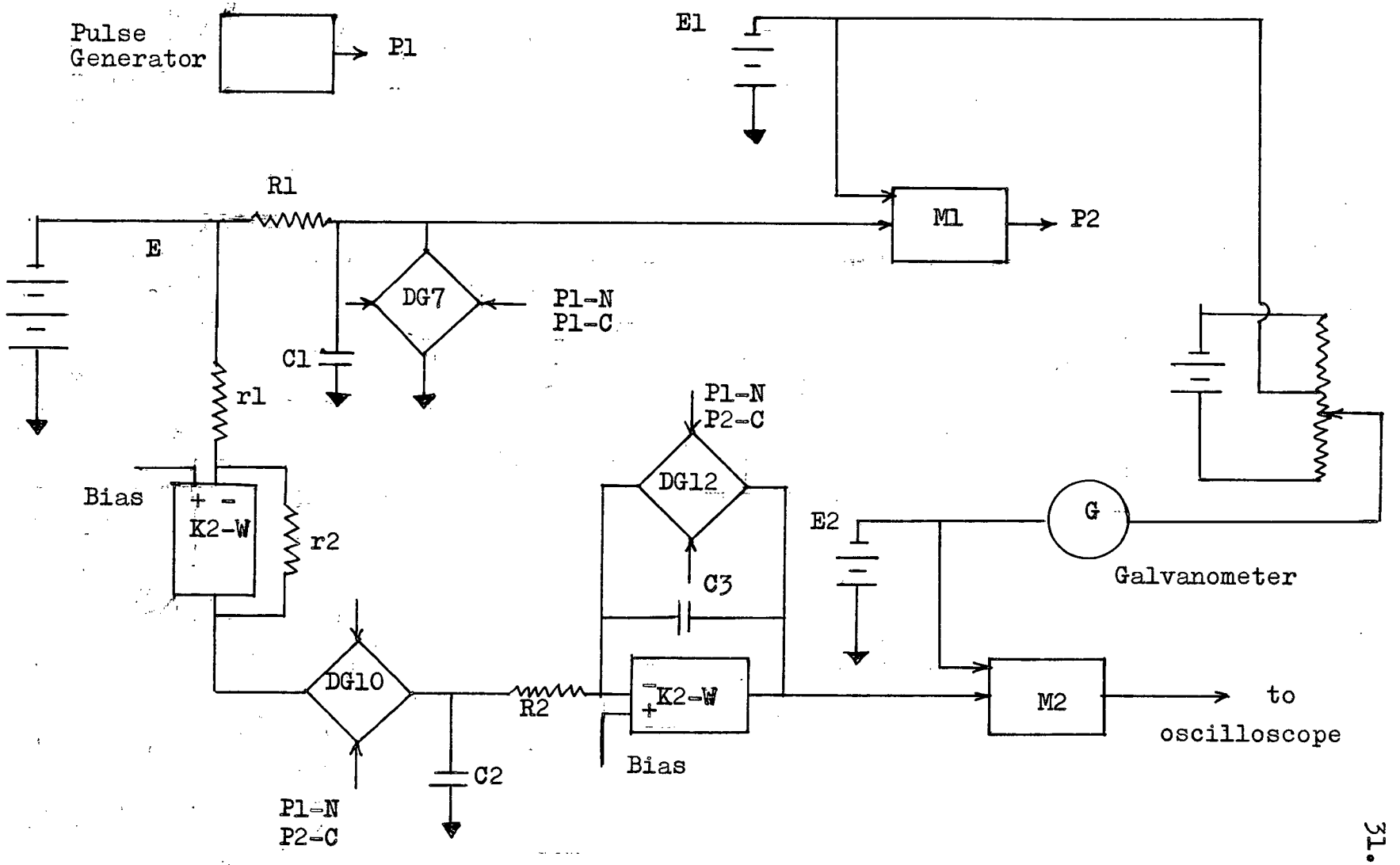


Figure 20. Test setup for the multiplier.

R_1 was adjusted until the oscilloscope showed no 1000 cycle output. Therefore $R_1C_1 = R_2C_2$. The K2-W amplifiers introduce little error since their gains are so large.

It would be extremely difficult to match C_2 to C_3. Therefore a method to overcome this was devised. The input to the R_2C_2 network must be positive in order to produce a negative sweep. Therefore, an inverter is introduced as shown in Figure 20. The input to the R_2C_2 sweep is then $E \frac{r_2}{r_1}$. Hence the output of the sweep is

$$-E \frac{r_2}{r_1} \frac{C_2}{C_3} (1 - e^{-t/R_2C_2}).$$

If $r_2C_2 = r_1C_3$ the sweep will be $-E(1 - e^{-t/R_2C_2})$ which is the same as the R_1C_1 sweep. The r_2C_2, r_1C_3 time constants were matched in the same way as is shown in Figure 19.

The multiplication multiar is M1 and M2 is the peak detecting multiar. The pulse generator produces a pulse P1 which operates the gates as shown in Figure 20, thereby initiating both sweeps. The negative reference voltage of M1 is set at the desired level of multiplication, E_1. When the R_1C_1 sweep reaches equality with E_1, M1 produces a pulse which stops the sweeps.

Some way of measuring the value of the R_2C_2 sweep had to be found, since no storage circuit was available. A second multiar, M2, is introduced and its reference voltage

is raised from a large negative value until it generates a pulse which is seen on the scope. At this point E_2 is equal to the peak of the sweep. The voltages E_2 and E_1 are then compared on a simple bridge as shown in Figure 20 and the voltage difference is measured. If the multiplier is absolutely accurate $E_1 = E_2$. The results of a typical set of readings are shown below.

Table 2.

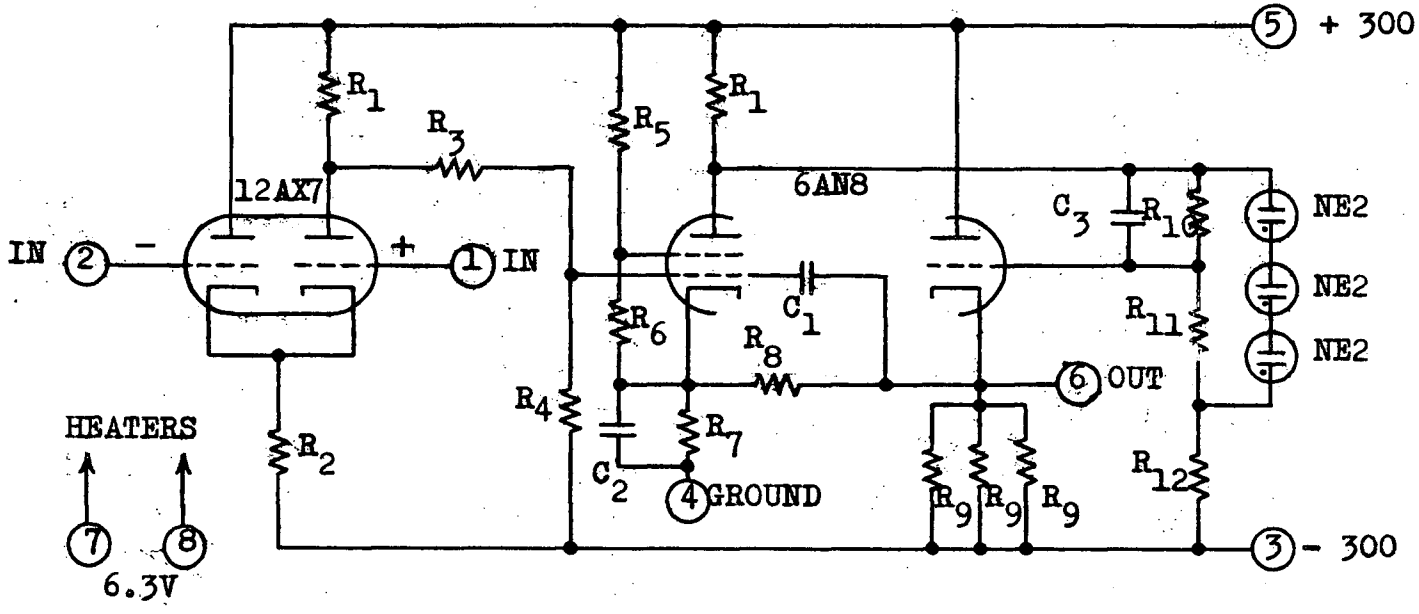
E_1	E_2-E_1 (Approaching from below the peak)	E_2-E_1 (Approaching from above the peak)
5	5.06	5.07
10	10.25	10.26
15	15.25	15.29
20	20.35	20.40
25	25.47	25.53

The above test is designed to measure the accuracy of the multiplier. The way in which the mutliplier has been set up in this case introduces more error than would the actual multiplier. In the example given above the flip-flop is loaded by three gates instead of one and, in addition, the R_2C_2 sweep is stopped by making DG 12 conducting instead of stopping it by making DG 11 non-conducting. The diode gates have a delay of 10 micro-seconds when made conducting, but only 1 to 2 micro-seconds when made non-conducting. Therefore the readings above do not indicate the accuracy which is obtainable, but they do show that the testing method is satisfactory.

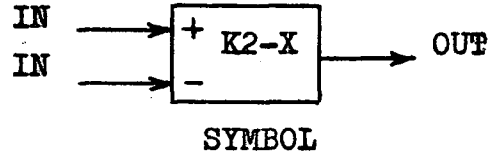
V Conclusion.

The prototype scanning system that was built has indicated that the idea is practicable. Further refinements will be made as work progresses on the analog computer.

The multiplier and function generator could not be fully tested because the timing circuitry was not completed, and precision resistors and condensers were not available for the sweep and inversion circuits. Another factor was the unavailability of well regulated power supplies. The tests on the multiplier did indicate that good accuracy can be obtained.

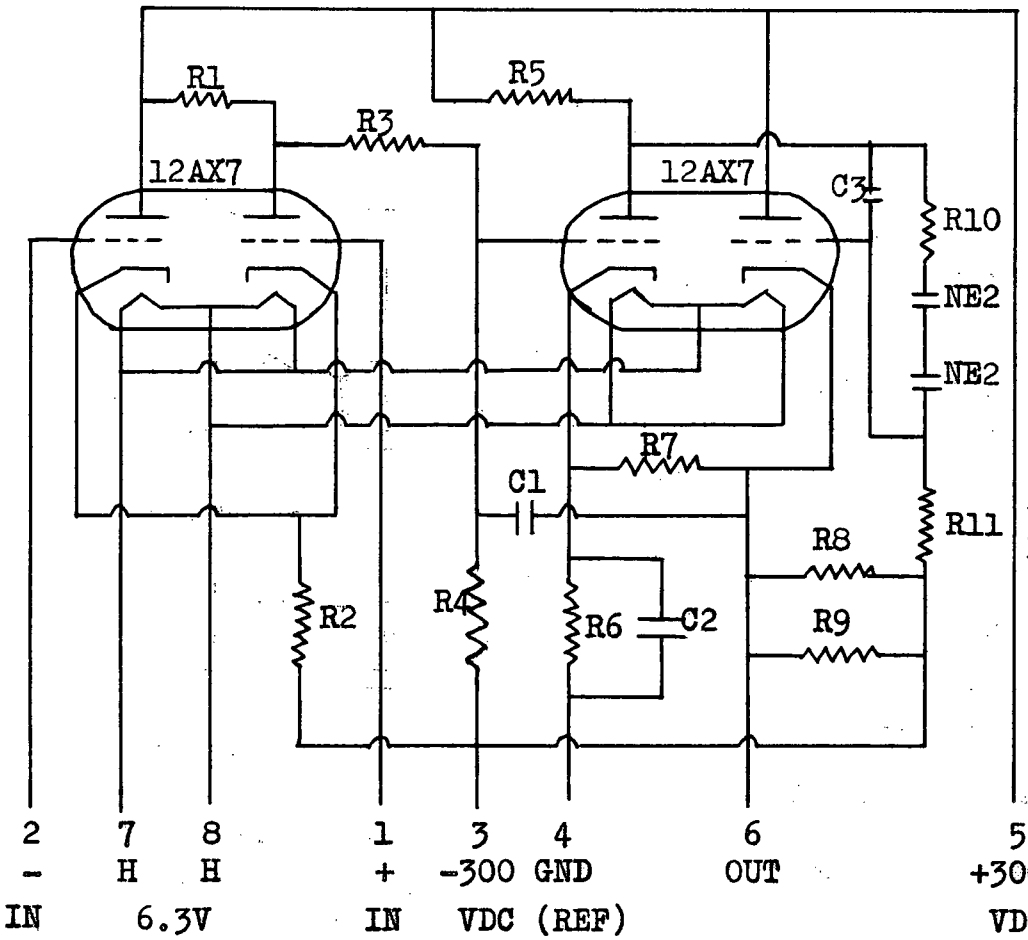


R_1	: 150K	10%	½ watt	R_9	: 220K	10%	½ watt
R_2	: 150K	10%	1 watt	R_{10}	: 10.0M	10%	½ watt
R_3	: 470K	10%	½ watt	R_{11}	: 1.5 M	10%	½ watt
R_4	: 1.0M	10%	½ watt	R_{12}	: 4.7M	10%	½ watt
R_5	: 180K	10%	½ watt				
R_6	: 68K	10%	½ watt	C_1	: 15 MMFD		
R_7	: 2.2K	10%	½ watt	C_2	: 0.005 MFD		
R_8	: 82K	10%	½ watt	C_3	: 7.5 MMFD		



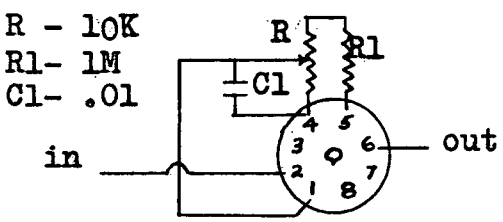
APPENDIX C : MODEL K2-X OPERATIONAL AMPLIFIER

George A. Philbrick Researches, Inc. (GAP/R)

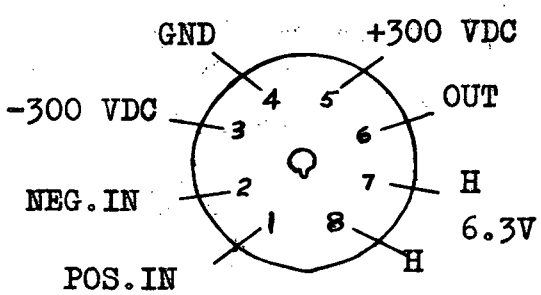


R1 - .22M 5%
R2 - .22M 5%
R3 - 1M
R4 - 2.2M
R5 - .47M 5%
R6 - 10K
R7 - .22M 5%
R8 - .22M 5%
R9 - .27M 5%
R10 - .68M
R11 - 4.7M
C1 - 7.5
C2 - 500
C3 - 7.5

Philbrick Model K2-W Operational Amplifier



Resistive method of bias



Base Connections

General Specifications

GAIN:
15,000 DC, open-loop

POWER REQUIREMENTS:
4.5 ma at +300 VDC
4.5 ma at -300 VDC
0.6 Amperes at 6.3V

TUBE COMPLEMENT
2 12AX7

INPUT IMPEDANCE:
Above 100 Megohms

OUTPUT IMPEDANCE:
Less than 1 K open-loop
below 1 ohm fully fed back

DRIFT RATE:
5 mv per day, referred to the input

VOLTAGE RANGE:
-50 VDC to +50 VDC, at ouput & both inputs

INPUT CURRENT:
Less than 0.1 Microamp for either input

OUTPUT CURRENT: -1 ma to +1 ma over full voltage range.

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