A REAL-TIME ANALOGUE COMPUTER FOR THE ESTIMATION OF SYSTEM DYNAMICS

by

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ABSTRACT

It is possible to obtain the best (in the minimum mean-square error sense) linear model of a control system by solving a convolution-type integral for the impulse response of the system. This thesis presents a method for obtaining an approximate solution for the impulse response by solving a system of linear equations which is statistically equivalent to the convolution integral. An analogue computer which can solve the system of equations is described.

The computer samples the sign of the input signal at an adjustable rate and stores this information in a shift register. The output signals from the shift register are then used to compute functions statistically related to the correlation functions of the system signals. A set of linear equations relating these functions is solved using an arrangement similar to the Gauss-Seidel Iteration method. The computer utilizes a time-sharing technique and the step response of the system can be generated as a repetitive waveform.

The overall operation of the computer is described in block diagram form. The individual circuits are described and the results of a computational test are given.

ACKNOWLEDGEMENT

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure Page

A REAL-TIME ANALOGUE COMPUTER FOR THE ESTIMATION OF SYSTEM DYNAMICS

1. INTRODUCTION

In the study of complex control systems it is often extremely difficult, or even impossible, to determine system dynamics analytically. An estimate of system dynamics must then be made experimentally. In certain cases it is possible to record the system's response to various types of input test signals. In this way a complete set of system characteristics can be obtained. Lendaris[1] has described a method for identifying the transfer function of a system from the response to an impulse or step input. An evident disadvantage of this class of methods is that the operation controlled by the system is usually disturbed by the test signal.* An additional objection is that the output may be influenced by external disturbances which are uncorrelated with the input. A practical method for determining system dynamics should therefore have the following properties:

1. It should not disturb the normal operation of the system.

2. It should discriminate between the effects produced by input signals and external disturbances.

For a linear system with a single input $x(t)$, an output $y(t)$, and unit impulse response $h(t)$, the following

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* An exception is the application of Lendaris' method to sampled-data systems, where the input is converted to a sequence of impulses.

relation is valid:

$$y(t) = \int_0^\infty x(t-u)\ h(u)\ du \qquad \ldots(1\text{-}1)$$

If Equation (1-1) is multiplied by $x(t-\tau)$ and a time average is taken, the result is

$$\phi_{yx}(\tau) = \int_0^\infty \phi_{xx}(\tau-u)\ h(u)\ du \qquad \ldots(1\text{-}2)$$

where $\phi_{yx}(\tau) = \overline{y(t)\ x(t-\tau)}$

and $\phi_{xx}(\tau-u) = \overline{x(t-u)\ x\ (t-\tau)} \qquad \ldots(1\text{-}3)$

are the cross-correlation and auto-correlation functions of the input-output and input signals respectively. Use of Equation (1-2) rather than Equation (1-1) for the solution of $h(t)$ eliminates the effect of any noise disturbances not correlated with the input signal. In the case of non-linear systems Woodrow[2] has shown that the solution of Equation (1-2) results in the best (in the minimum mean-square error sense) linear model of the system.

Reswick[3] has described a method for determining the impulse response, $h(t)$, from Equation (1-2). The auto-correlation and cross-correlation functions are determined using a digital computer by analysis of recorded input and output data, and the impulse response is approximated by a sequence of impulses of the form

$$h(t) = \sum_{k=1}^{n} h_k \, \delta(t-\tau_k) \qquad \ldots(1\text{-}4)$$

If Equation (1-4) is substituted into Equation (1-2), algebraic equations for the unknowns, h_k, can be obtained, and these can be determined experimentally using Reswick's Delay Line Synthesizer. Gabor[4] has described a large scale analogue computer which operates on recorded data and could be used to generate a polynomial approximation to h(t). Both methods require processing the recorded input-output data before analysis and therefore would be satisfactory for use only with a time-invariant system. This may not be adequate. The use of a digital computer to determine system response in real-time has been described by Conn[5]. From the point of view of cost, however, a simple on-line analogue computer would be more suitable. This thesis describes such a computer, in which the determination of system response is based on a method suggested by Bohn[6].

2. THEORY OF COMPUTER SOLUTION FOR IMPULSE RESPONSE

Consider again Equation (1-1). If it is multiplied by $v(t-\tau)$ and a time average is taken, the result is

$$\phi_{yv}(\tau) = \int_0^\infty \phi_{xv}(\tau-u)\, h(u)\, du \qquad \ldots(2\text{-}1)$$

If $\phi_{yv}(\tau)$ is not to vanish, $v(t)$ must be related to $x(t)$ by a functional operation. Watts[7] has shown that if $v(t)$ represents a general amplitude quantization of $x(t)$ and $x(t)$ is a Gaussian random process, then

$$\phi_{yv}(\tau) = C\, \phi_{yx}(\tau) \qquad \ldots(2\text{-}2)$$

where C is some constant. In the computer to be described

$$v(t) = \operatorname{sgn} x(t) \qquad \ldots(2\text{-}3)$$

where

$$\operatorname{sgn} x(t) = \begin{cases} +1, & x(t) \geqq 0 \\ -1, & x(t) < 0 \end{cases} \qquad \ldots(2\text{-}4)$$

$\phi_{yv}(\tau)$ and $\phi_{xv}(\tau)$ are then defined as the switched cross-correlation and auto-correlation functions respectively.

Consider now the integral

$$I = \int_{T}^{\infty} \phi_{xv}(\tau-u)\ h(u)\ du \qquad (\tau \leqq T) \qquad \ldots(2\text{-}5)$$

For a stable linear system I is finite and $\lim_{T\to\infty} I = 0$. However, it is not known a priori how large T should be to make I negligible. It is expected that the maximum value of $|I|$ will occur when $\tau \approx T$ because $\phi_{xx}(\tau)$, and correspondingly $\phi_{xv}(\tau)$, are usually small for large values of τ. Note that for $\tau \approx T$,

$$I \approx \phi_{xv}(\tau-T)\ g_n \qquad \ldots(2\text{-}6)$$

where

$$g_n = \int_{T}^{\infty} \frac{\phi_{xv}(T-u)\ h(u)\ du}{\phi_{xv}(0)} \qquad \ldots(2\text{-}7)$$

The integral I will now be approximated by Equation (2-6) in which form it can be handled by the computer. Equation (2-1) can then be written

$$\phi_{yv}(\tau) = \int_{0}^{T} \phi_{xv}(\tau-u)\ h(u)\ du + \phi_{xv}(\tau-T)\ g_n \qquad \ldots(2\text{-}8)$$

The time interval 0...T is now divided into n equal subintervals as shown in Figure 2-1, in which it is assumed that x(t) varies slowly over each subinterval.

Equation (2-8) can then be written

$$\phi_{yv}(\tau_k) = \phi_{xv}(0)\ g_k + \sum_{m=0}^{n}{}' \phi_{xv}(\tau_k - u_m)\ g_m \qquad \ldots(2\text{-}9)$$

where

$$g_m = \int_{u_m}^{u_{m+1}} h(u)\ du\ ,\ 0 \leqq m \leqq n-1 \qquad \ldots(2\text{-}10)$$

and the prime after the summation sign indicates that the term $m = k$ is not to be included.

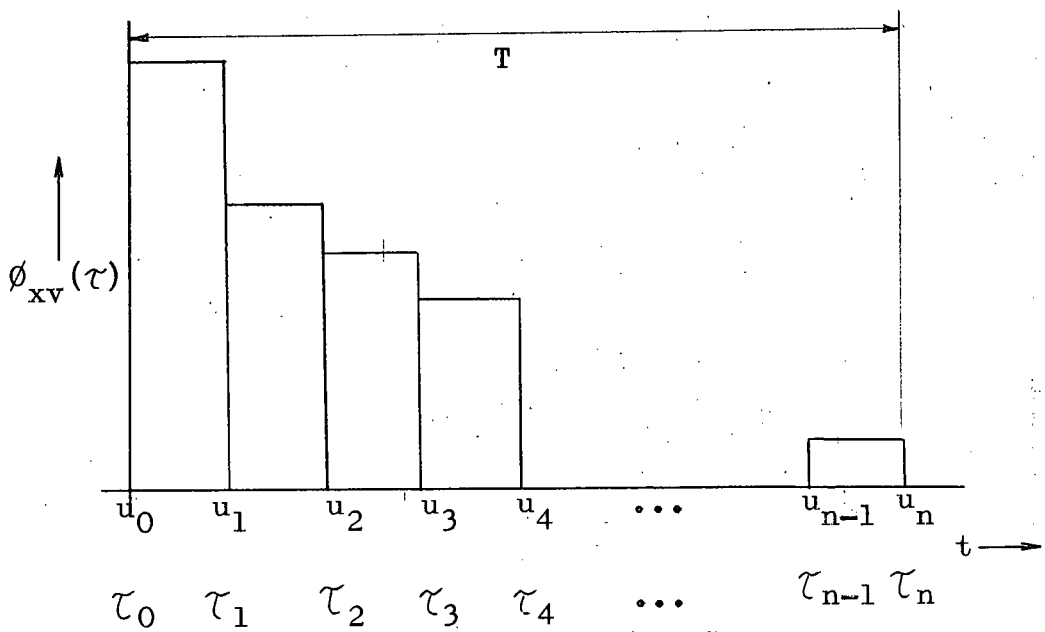

Figure 2-1. Subdivision of Time Scale.

Equation (2-9) is now rearranged into the form

$$\phi_{xv}(0)\ g_k = \phi_{yv}(\tau_k) - \sum_{m=0}^{n}{}' \phi_{xv}(|\tau_k - u_m|)\ g_m \qquad \ldots(2\text{-}11)$$

Note that $\phi_{xv}(\tau_k - u_m)$ has been replaced by $\phi_{xv}(|\tau_k - u_m|)$. This is justified by Watts[7] who has shown that

$$\phi_{xv}(\tau) = \phi_{xv}(-\tau) \qquad \ldots(2\text{-}12)$$

holds for Gaussian-type signals [Equation (2-12) actually follows from Equation (2-2)] and is a good approximation for many other types of signals.

The quantity $\phi_{xv}(0)$ is simply the time average of the magnitude of the system input signal x(t). It is assumed that the signals x(t) and y(t) are normalized* so that

$$\phi_{xv}(0) = 1 \qquad \ldots(2\text{-}13)$$

Combining Equations (2-11) and (2-13) yields

$$g_k = \phi_{yv}(\tau_k) - \sum_{m=0}^{n}{}' \phi_{xv}(|\tau_k - u_m|)\, g_m \qquad \ldots(2\text{-}14)$$

A simplified block diagram of a computer which solves Equation (2-14) for g_k is shown in Figure 2-2. Switch S_2 is swept through positions 0, 1,...,m, m + 1,..., n for each position of S_1. For each m, g_m is sampled and then weighted by $v(t-|\tau_k-u_m|)$ in block 1. The quantity $v(t-|\tau_k-u_m|)\, g_m$ is

---

* This normalization procedure involves a division, which is relatively difficult to realize electronically and would accomplish only a time-variable adjustment of the x and y scale factors. For these reasons it has been omitted from the computer. Instead, a control has been included for manual adjustment of these scale factors for the purpose of testing the computer.

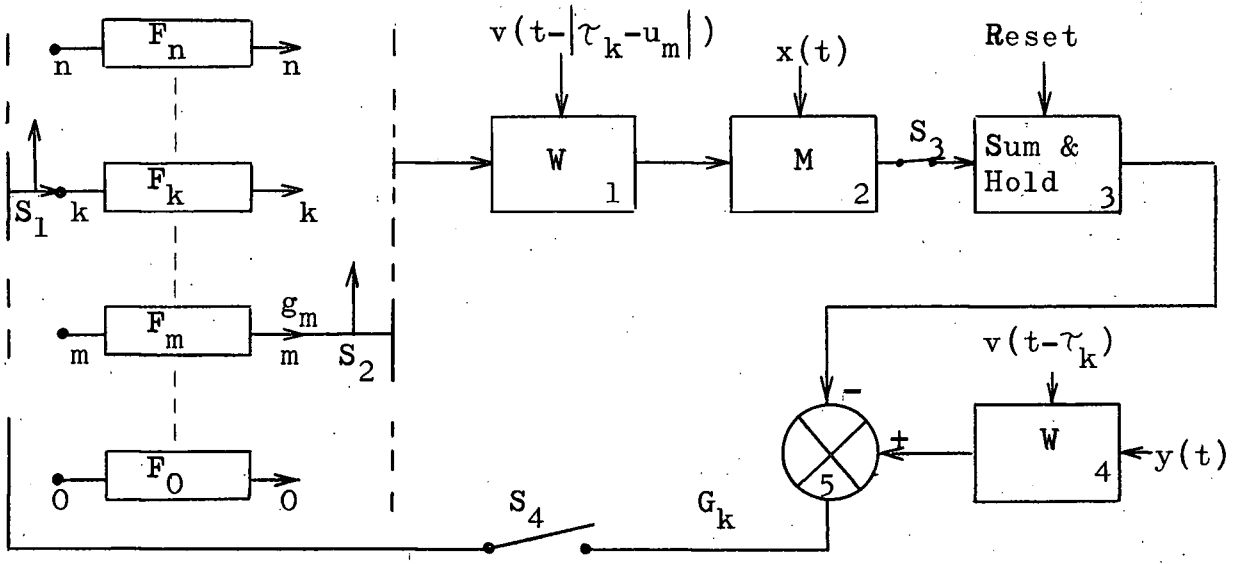

Figure 2-2. Simplified Computer Block Diagram.

multiplied by x(t) in block 2, and the result is added to the contents of block 3. Switch S_3 is opened for the interval $m = k$, so that the term including g_k is not included in the sum. The output of block 3 is therefore $x(t)\sum_{m=0}^{n}{}' v(t-|\tau_k-u_m|)\ g_m$. The quantity y(t) is weighted by $v(t-\tau_k)$ in block 4. The outputs of blocks 3 and 4 are passed to block 5 which yields

$$G_k = y(t)\ v(t-\tau_k) - x(t)\sum_{m=0}^{n}{}' v(t-|\tau_k-u_m|)\ g_m \quad \ldots(2\text{-}15)$$

At the end of a complete cycle by S_2, G_k is sampled by S_4 and the result is applied to F_k. The sum held by block 3 is reset to zero, and k is stepped by one. F represents a time-averaging operation. The output of F_k is therefore

$$\overline{G_k} = y(t)\ v(t-\tau_k) - x(t) \sum_{m=0}^{n}{}' v(t-|\tau_k-u_m|)\ g_m \qquad \ldots(2\text{-}16)$$

Since $\phi_{xv}(\tau-u) = \overline{x(t-u)\ v(t-\tau)} = \overline{x(t)\ v(t-\tau+u)}$,

it follows that

$$\overline{G_k} = g_k \qquad \ldots(2\text{-}17)$$

The entire process described above is repeated for successive values of k. In this way the computer solves the n + 1 equations for $g_0, g_1, \ldots, g_n$ in a fashion similar to that of the Gauss-Seidel Iteration[8] method. The important difference is that an averaging procedure is used here.

The following chapters describe the computer circuits and operations in detail.

3. BLOCK DIAGRAM REPRESENTATION OF THE COMPUTER

This chapter describes in block diagram form the organization and fundamental concepts of the computer and its operation. The description is in two parts. First the timing arrangement is discussed and waveforms are shown. Then the overall operation of the computer is described.

3-1. Timing Arrangement.

The number of subdivisions of the time scale, n, is chosen to be 9. A complete iteration cycle therefore includes 10 k cycles (k = 0, 1, ...,9). (A k cycle is defined as the time required to compute, sample, and store each G_k). Each k cycle includes 11 clock periods [10 m periods (m = 0, 1, ...,9) and one sample-store and clear period]. A typical k cycle is shown in Figure 3-1.

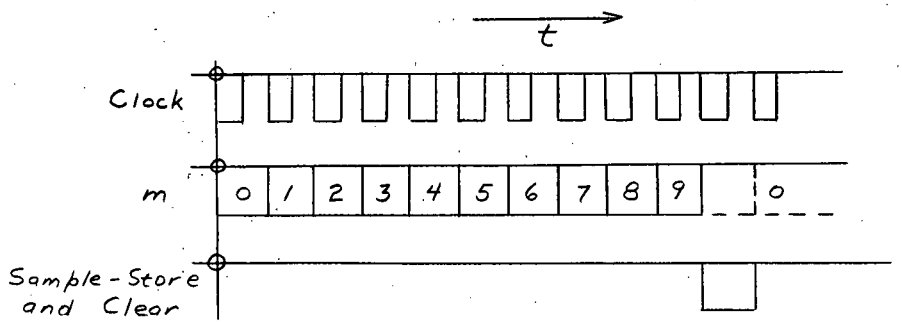

Figure 3-1. Typical k Cycle.

The overall timing control circuit is shown in block diagram form in Figure 3-2. The four waveforms at the output of the clock pulse generator are shown in Figure 3-3.

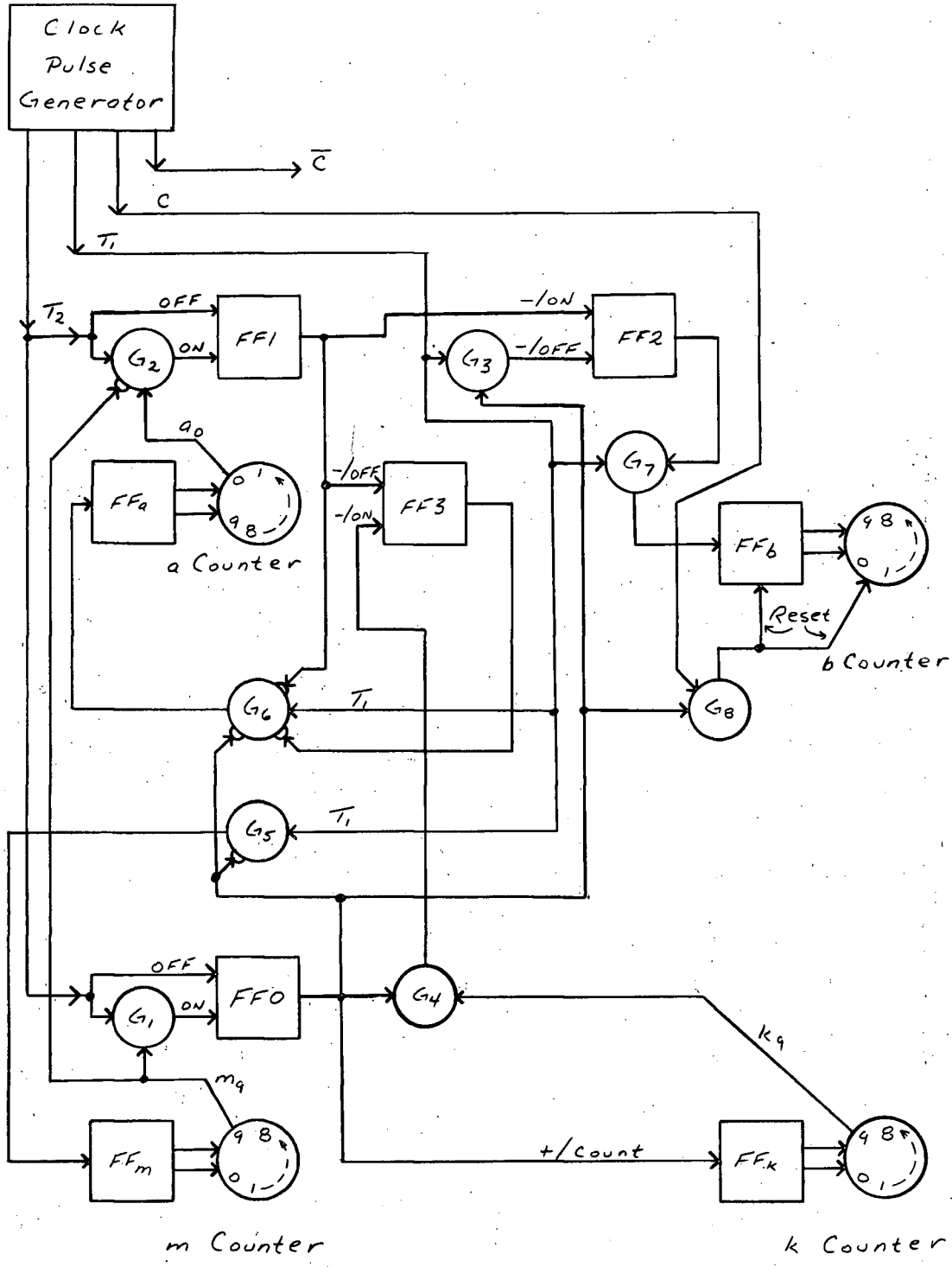

Figure 3-2. Block Diagram of Timing Circuit.

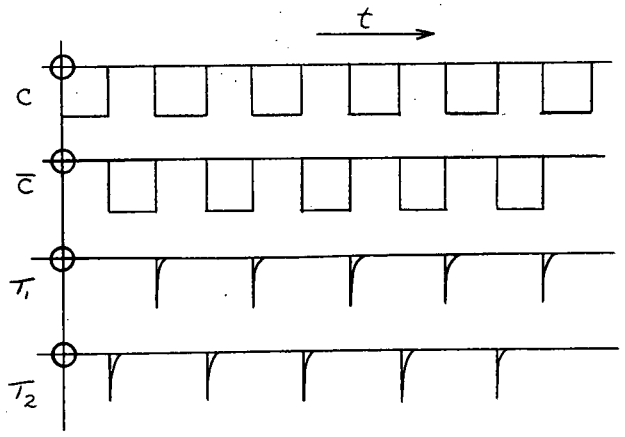

Figure 3-3. Master Timing Pulses.*

Consider first the operation of the m counter. Assume FFO is OFF and the m counter is in position 0. T_1 pulses are passed by G_5 and trigger FF_m, which drives the m counter. T_2 pulses are applied to FFO keeping it OFF. Each T_1 pulse therefore increases m by one until m = 9. The next T_2 pulse is passed by G_1 and turns FFO ON. This inhibits the subsequent T_1 pulse in G_5 and FF_m is not triggered. The following T_2 pulse turns FFO OFF again, and the next T_1 pulse triggers m to position 0. The cycle is thus complete. Note that m = 9 for two clock periods. The second of these is used as the sample-store and clear period. (See Figure 3-1).

At the conclusion of each k cycle, as described above, the positive-going edge of the pulse from FFO triggers FF_k, increasing k by one. Ten such k cycles constitute an iteration cycle.

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* Note that $\overline{C}$ is the logical complement of C. This nomenclature is used throughout the thesis.

Recall Equation (2-15). Note that for each k, the sequence k, k-1,...,2, 1, 0, 1, ...,9-k must be generated to control the selection of $v(t - |\tau_k - u_m|)$. This sequence is generated by the a counter and b counter.

Refer again to Figure 3-2. Assume that all counters are set to position 0, all flip-flops are OFF, and the first T_2 pulse arrives before the first T_1 pulse.* Since a = 0 and $m \neq 9$, G_2 passes this first T_2 pulse which turns FF1 ON. The negative-going (leading) edge of the signal from FF1 turns FF2 ON, enabling G_7 to pass the following T_1 pulses to FF_b. The b counter is therefore stepped by these T_1 pulses. Also, FF1 blocks the first T_1 pulse in G_6 so that the a counter is not stepped. The next T_2 pulse turns FF1 OFF. This opens G_6 and successive T_1 pulses step the a counter,** except for the T_1 pulse which appears while FF0 is on. (FF0 blocks T_1 pulses in G_6). This T_1 pulse is passed by G_3 and turns FF2 OFF. The C pulse which appears while FF0 is ON is passed by G_8 and resets FF_b and the b counter. The b counter is held in position 0 until FF2 is once again turned ON by FF1. The waveforms for the first two k cycles (k = 0, k = 1) are shown in Figure 3-4. The sequence k, k-1, ..., 1, 0, 1, ..., 9-k is obtained from the b counter when FF2 is ON, and from the a counter when FF2 is OFF. This can be expressed in logical form as follows:

$$Q_i = b_i \cdot FF2 + A_i \cdot \overline{FF2} \qquad \ldots(3\text{-}1)$$

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* For description of the Reset Circuit, see Chapter 5.
** Note that the a counter counts down, while the b, m, and k counters count up.

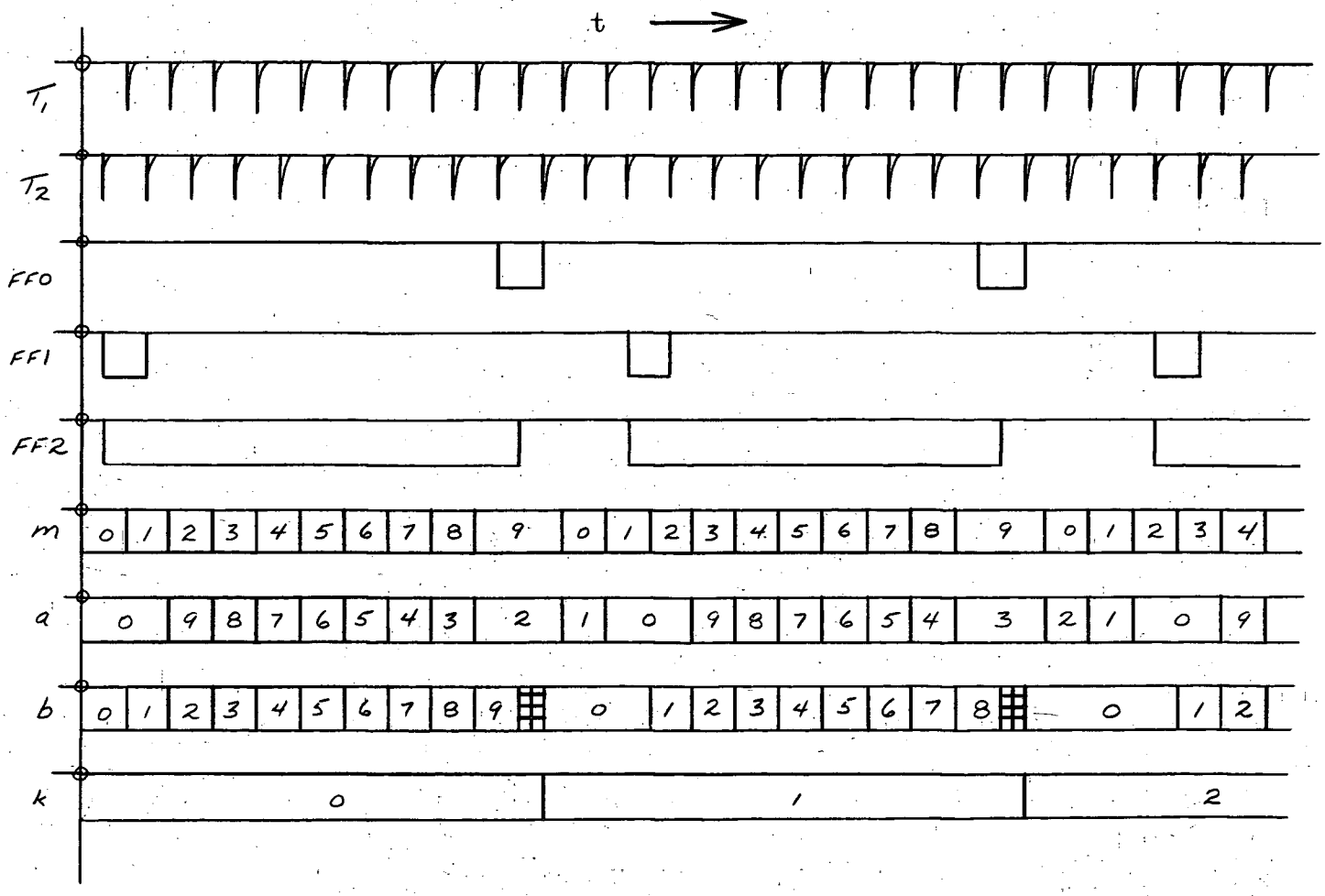


Figure 3-4. Timing Waveforms (k = 0, 1).

where

Q_i represents the binary state (1 $\triangleq$ ON, 0 $\triangleq$ OFF) of the sequence term i,

a_i and b_i represent the binary states of the i-th outputs from the a counter and b counter respectively,

FF2 represents the binary state of FF2 (if FF2 is ON, FF2 = 1, $\overline{FF2}$ = 0; if FF2 is OFF, FF2 = 0, $\overline{FF2}$ = 1),

+ represents the logical OR operation,

· represents the logical AND operation.

The sequences thus obtained can be seen in Figure 3-4 to be

for k = 0, 0, 1, 2, ..., 8, 9

and,

for k = 1, 1, 0, 1, ..., 7, 8.

The waveforms as shown in Figure 3-4 can be continued for the remainder of the iteration cycle. The result for k = 9 is shown in Figure 3-5. The T_2 pulses coincident with the switching of the k count from 8 to 9 and 9 to 0 are inhibited from turning FF1 ON by the action of the m_9 pulses in G_2. Also, the T_1 pulse immediately following the switching of the k count from 9 to 0 is inhibited from stepping the a counter by the action of the FF3 pulse in G_6.

It is evident from Figure 3-5 that at the conclusion of the k_9 cycle the computer begins another iteration cycle.

3-2. Block Diagram Representation of Computing Circuits.

The overall computer is shown in block diagram form in Figure 3-6, exclusive of circuits which control the four counters.

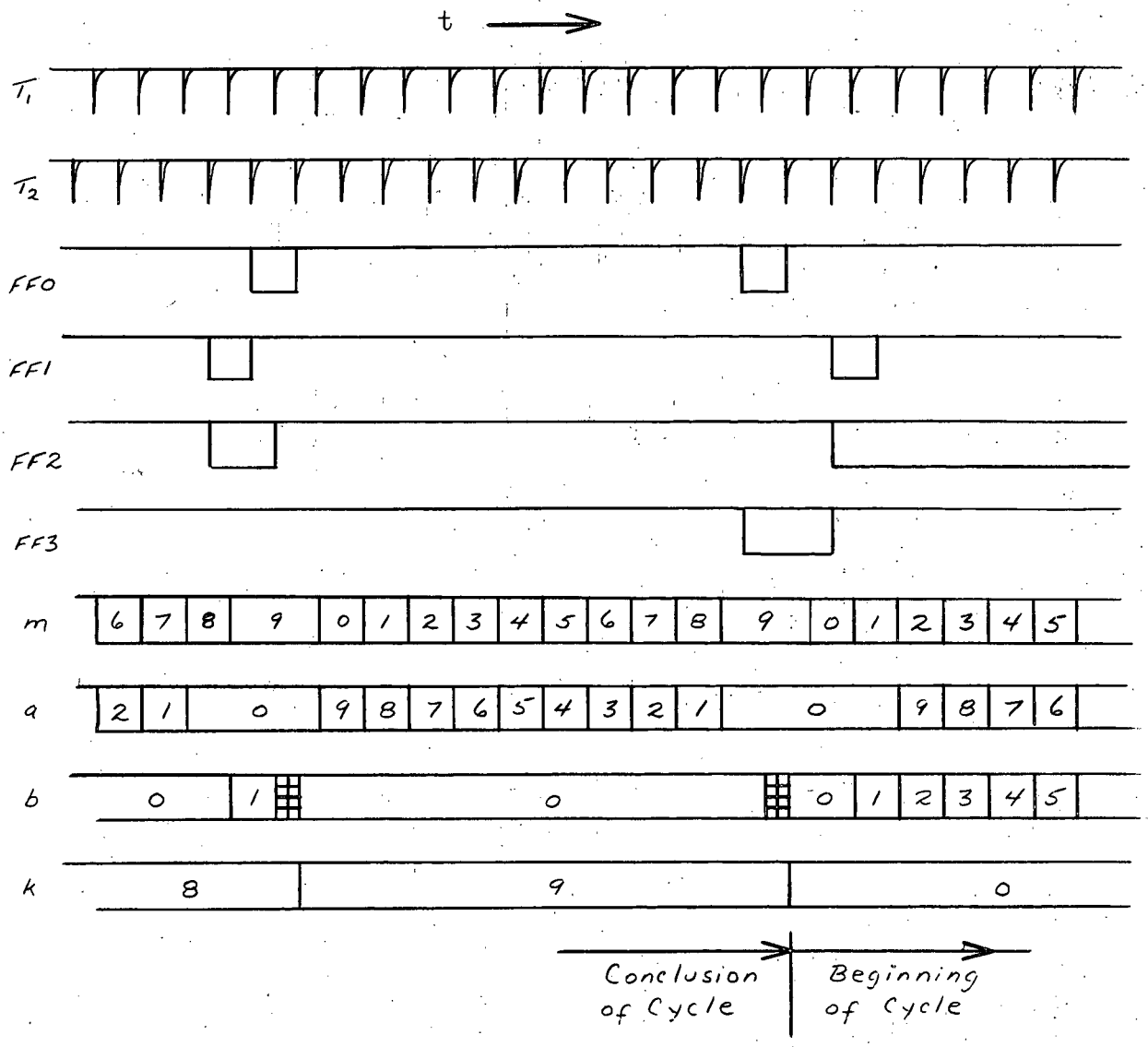


Figure 3-5. Timing Waveforms (k = 9).

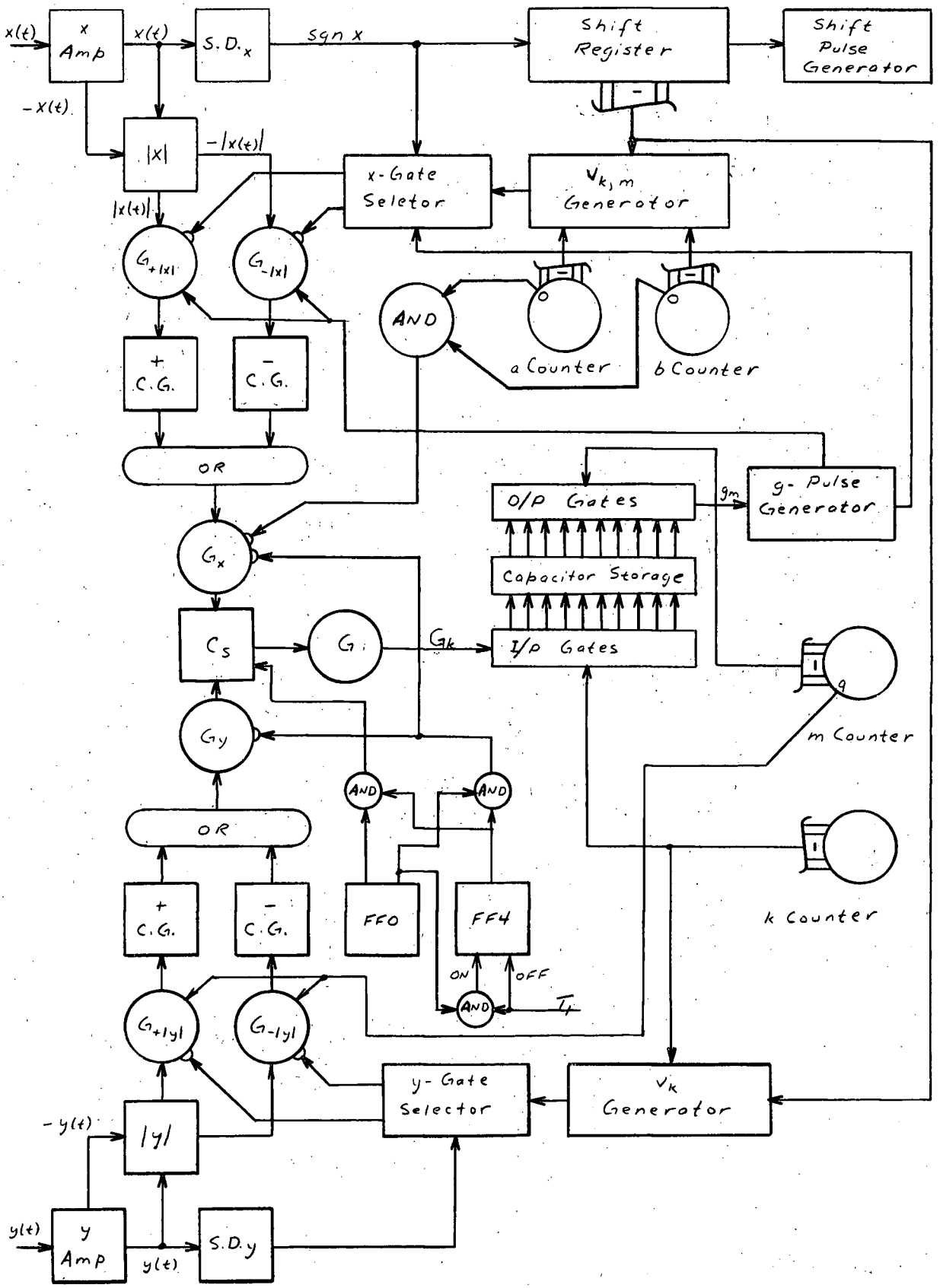


Figure 3-6. Block Diagram of Computer.

The input signal to the control system under test, $x(t)$, is fed into the x-amplifier to produce the two signals $x(t)$ and $-x(t)$. These signals are then fed to the $|x|$ circuit to generate $|x(t)|$ and $-|x(t)|$ which in turn are passed to the $+|x|$ and $-|x|$ gates respectively. ($G_{+|x|}$ and $G_{-|x|}$) The voltage $x(t)$ is also passed to a sign detector ($S.D._x$), the binary output of which represents the sign of $x(t)$. This output, sgn x, is passed to the Shift Register, which samples, stores, and shifts the quantity at a rate determined by the Shift Pulse Generator. (The time between successive shift pulses is equal to $T/9$. See Figure 2-1). The outputs from the Shift Register are sampled according to the sequence $k, k-1, \ldots, 1, 0, 1, \ldots, 9-k$, and the signal $v_{k,m} \triangleq v(t-|\tau_k-u_m|)$ is passed to the x-Gate Selector. Also feeding into the x-Gate Selector are sgn x and a control signal from the g-Pulse Generator. This latter signal is dependent upon the sign of g_m. The combined action of the three control signals causes the x-Gate Selector to remove the inhibit signal from either $G_{+|x|}$ or $G_{-|x|}$. The selected gate is then opened by a pulse from the g-Pulse Generator for a time interval proportional to $|g_m|$. A voltage proportional to $|x(t)|$ is thus applied to either of the current generators +C.G. or -C.G. for a time proportional to $|g_m|$. The result is that the voltage on the summing capacitor, V_{C_s}, changes by

$$(\Delta V_{C_s})_{m,x} = -\beta\, x(t)\, g_m\, v(t-|\tau_k-u_m|) \qquad \ldots(3\text{-}2)$$

where β is a scale factor. The process is executed for $m = 0, 1, \ldots, 9$, except that G_x is blocked for the interval $m = k$.*

The output signal from the control system under test, $y(t)$, is operated upon in a very similar manner. The circuits and operations of blocks y-Amp., $|y|$, and S.D.$_y$ are identical to those of blocks x-Amp., $|x|$, and S.D.$_x$ respectively. The outputs from the Shift Register are sampled in the v_k Generator by the k counter, and the signal $v_k \triangleq v(t-\tau_k)$ is passed to the y-Gate Selector. The signals sgn y and v_k cause the y-Gate Selector to remove the inhibit signal from either $G_{+|y|}$ or $G_{-|y|}$. The selected gate is then opened by the m_9 pulse. The result of this action is that V_{C_s} changes by

$$(\Delta V_{C_s})_y = \alpha\, y(t)\, v(t-\tau_k) \qquad \ldots(3\text{-}3)$$

where α is a scale factor. The total voltage change on C_s over a complete k cycle is therefore

$$(\Delta V)_{C_s} = \alpha\, y(t)\, v(t-\tau_k) - \beta\, x(t) \sum_{m=0}^{n}{}' g_m\, v(t-|\tau_k - u_m|) \qquad \ldots(3\text{-}4)$$

When the scale factors are properly selected so that $\alpha = \beta$,

$$(\Delta V)_{C_s} = \alpha G_k \qquad \ldots(3\text{-}5)$$

---

* This is accomplished by inhibiting G_x by the signal $(a_0)\cdot(b_0)$. Figures 3-4 and 3-5 demonstrate that a_0 and b_0 are both ON only when $m = k$.

At the conclusion of a k cycle the sample pulse S blocks G_x and G_y, thereby holding V_{C_s} constant, and opens the gate G, allowing αG_k to be stored in the storage capacitor selected by the k counter. The clear pulse CL restores V_{C_s} to its initial value in preparation for the next k cycle. Figure 3-7 shows the waveforms for a typical k cycle.

The organization and overall operation of the computer have now been described. The individual circuits will be discussed in the following chapters.

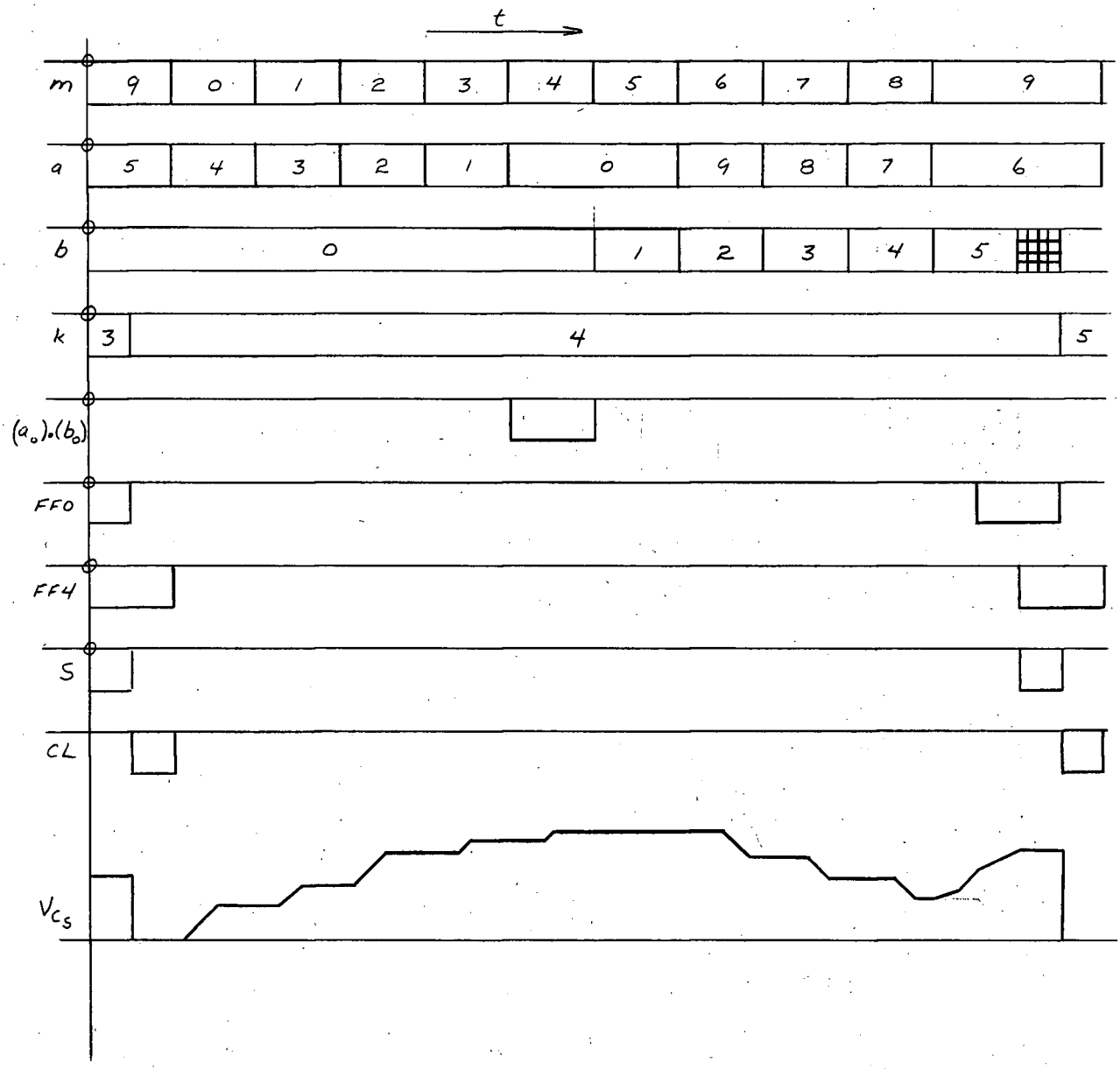


Figure 3-7. Computing Waveforms for a Typical k Cycle.

4. TIMING CIRCUITRY

In this chapter the various sections of the Timing Circuit are described. They are the following:

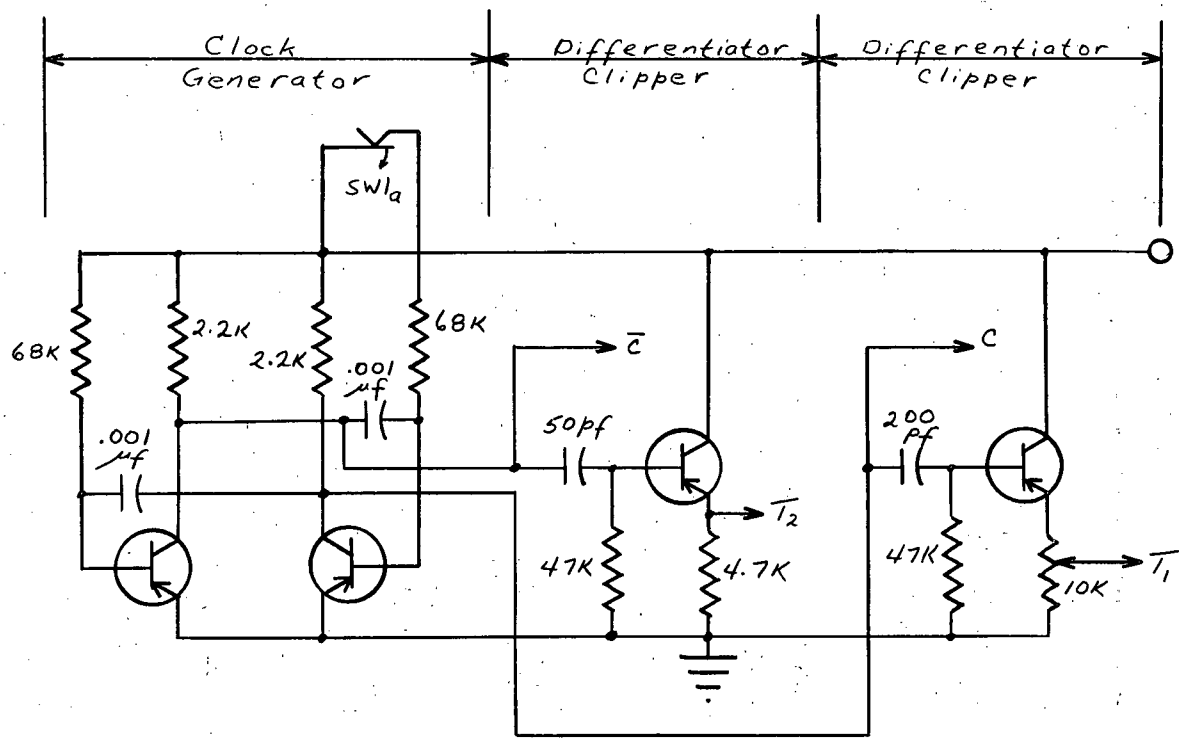
1. Clock Pulse Generator
2. Counters and Flip-Flop Drivers
3. Control Flip-Flops
4. Control Gates.

4-1. Clock Pulse Generator.

The Clock Pulse Generator circuit is shown in Figure 4-1. The clock generator is a standard astable multivibrator producing symmetrical square wave signals C and $\overline{C}$. These signals are differentiated and clipped to produce the trigger pulses T_1 and T_2 respectively. The waveforms are shown in Figure 4-2. $SW1_a$ is part of a double-pole switch used for starting and resetting the computer. (The Reset Circuit is described in Chapter 5).

4-2. Counting Circuit.

There are four identical counting circuits in the computer, the a, b, k, and m counters. Each counter utilizes a BX-1000[9] decade counting tube, which indicates its state by a -15 volt signal at one of ten output pins. The count is advanced by alternately applying negative trigger pulses of at least 50 volts magnitude to two inputs. These trigger pulses are generated by the associated driver flip-flop. Applying a



Resistors: ½W, 10% Transistors: 2N404

Capacitors: 75V, 10%

Figure 4-1. Clock Pulse Generator.

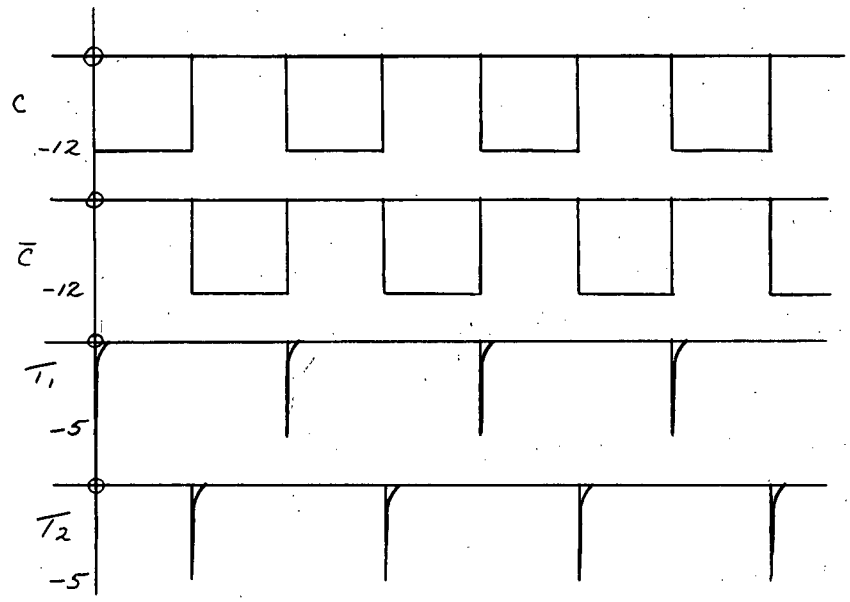


Figure 4-2. Clock Pulse Generator Waveforms.

-5 volt pulse to a third input resets the counter to a predefined 0-state.

The counter circuit is shown in Figure 4-3. The output signals are taken from the points marked 0, 1,..., 8, 9. The driver flip-flop circuit is shown in Figure 4-4. The signals at the transistor collectors, square waves of approximately 75 volts amplitude, are differentiated by the coupling networks (200 pf capacitors and 100 K resistors) of the counter. This provides the negative trigger pulses required for stepping the counter. The positive trigger pulses formed by the differentiators have no effect on the circuit.

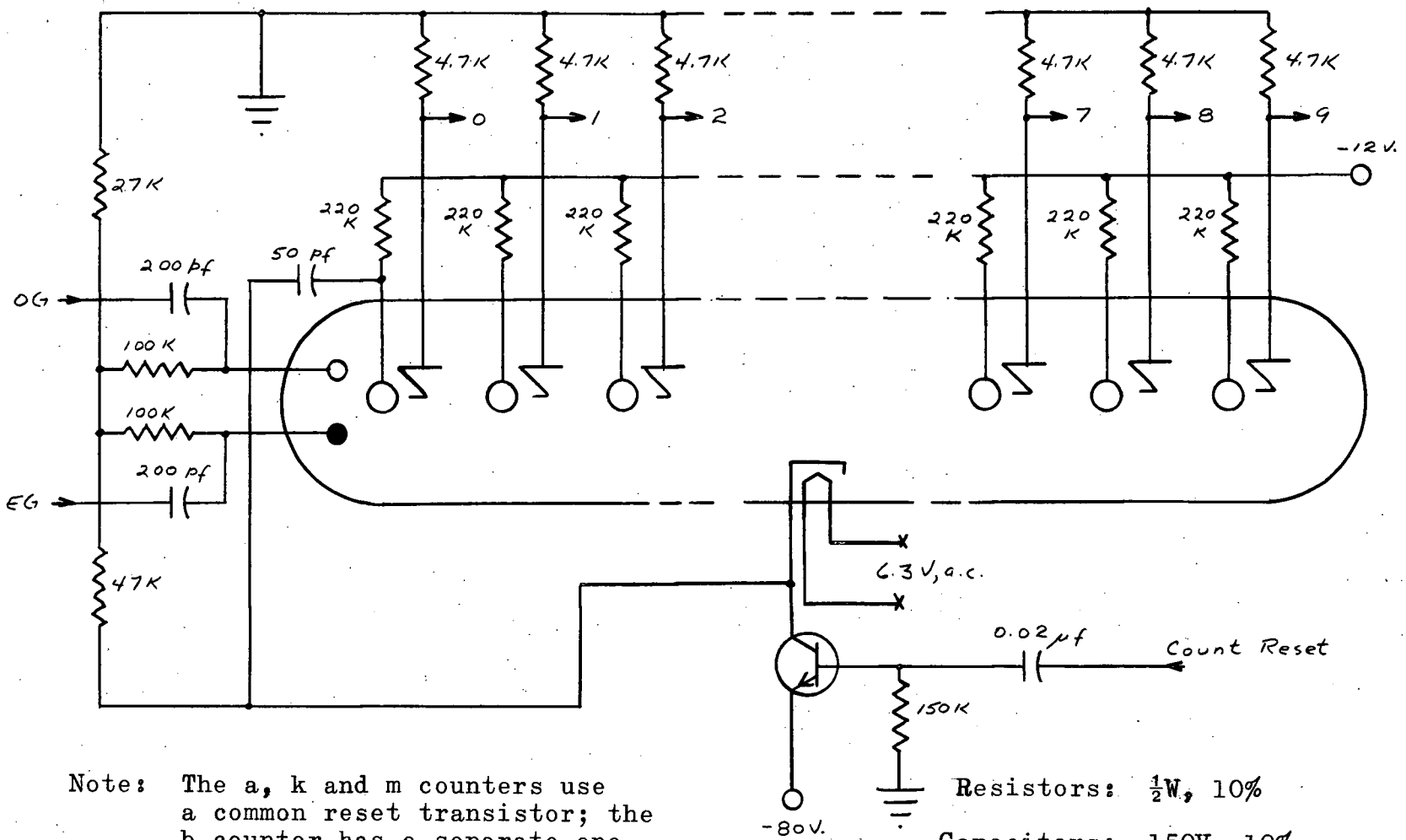
Whenever the counter is reset, it is necessary that the driver flip-flop be in the state such that the next count pulse to the flip-flop results in a negative trigger pulse being applied to the correct counter input. If this is not done, the counter may lose the first count. A FF Reset pulse is applied as shown in Figure 4-4 for this purpose.

4-3. Control Flip-Flops.

The four flip-flops FF0, FF1, FF2, and FF3 are identical. Figure 4-5 shows the circuit diagram. Negative trigger pulses applied to either of two inputs turn the flip-flop ON or OFF as shown. If a Reset pulse is applied to the third input the flip-flop is turned OFF by the negative-going edge. The output levels of the flip-flop are nominally 0 volts and -12 volts.

4-4. Control Gates.

The Timing Circuit includes eight control gates, G_1, G_2,..., G_8. The operation of these gates is indicated by



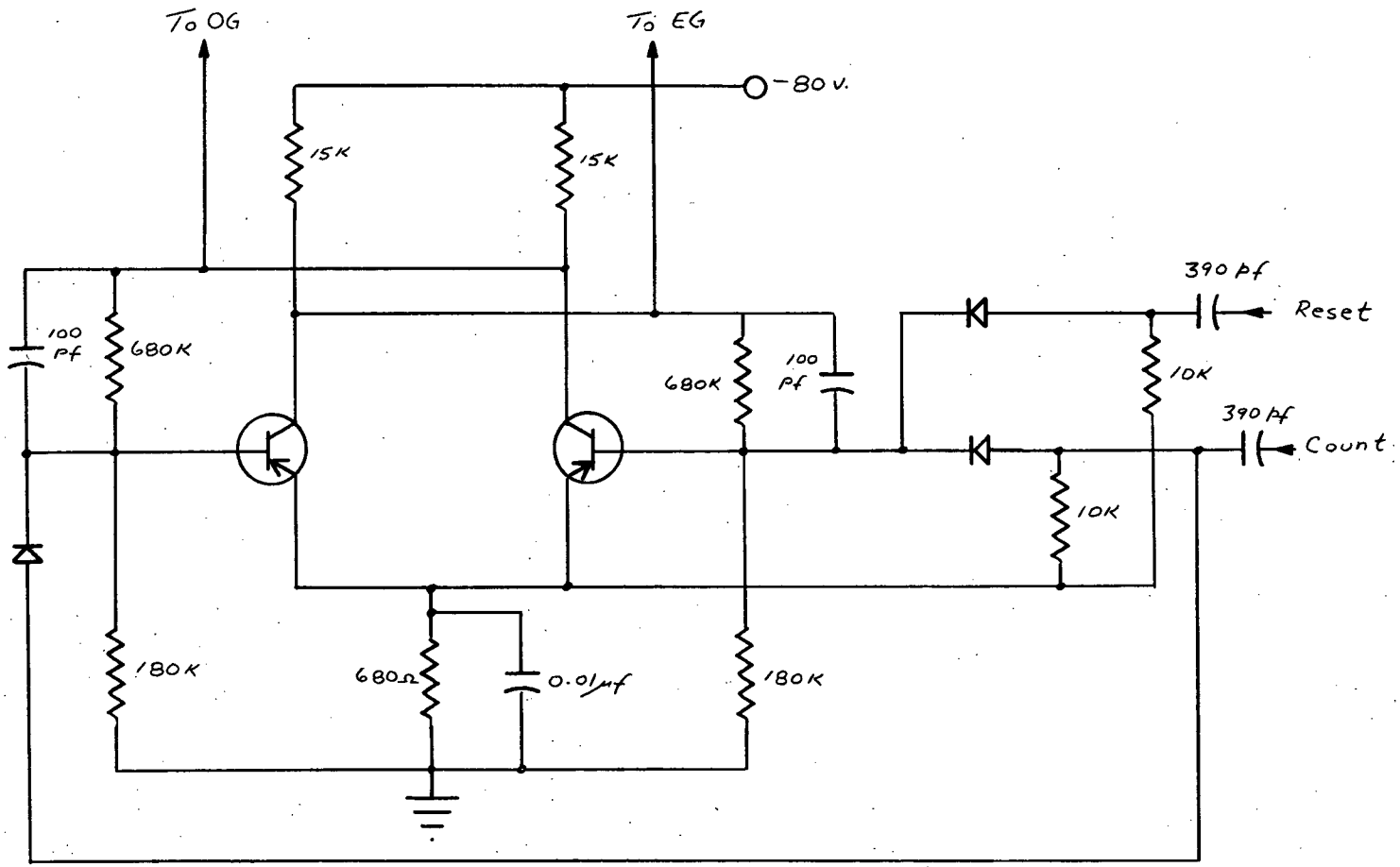
Note: The a, k and m counters use a common reset transistor; the b counter has a separate one.

Resistors: ½W, 10%

Capacitors: 150V, 10%

Transistors: 2N657

Figure 4-3. BX-1000 Counter Circuit.



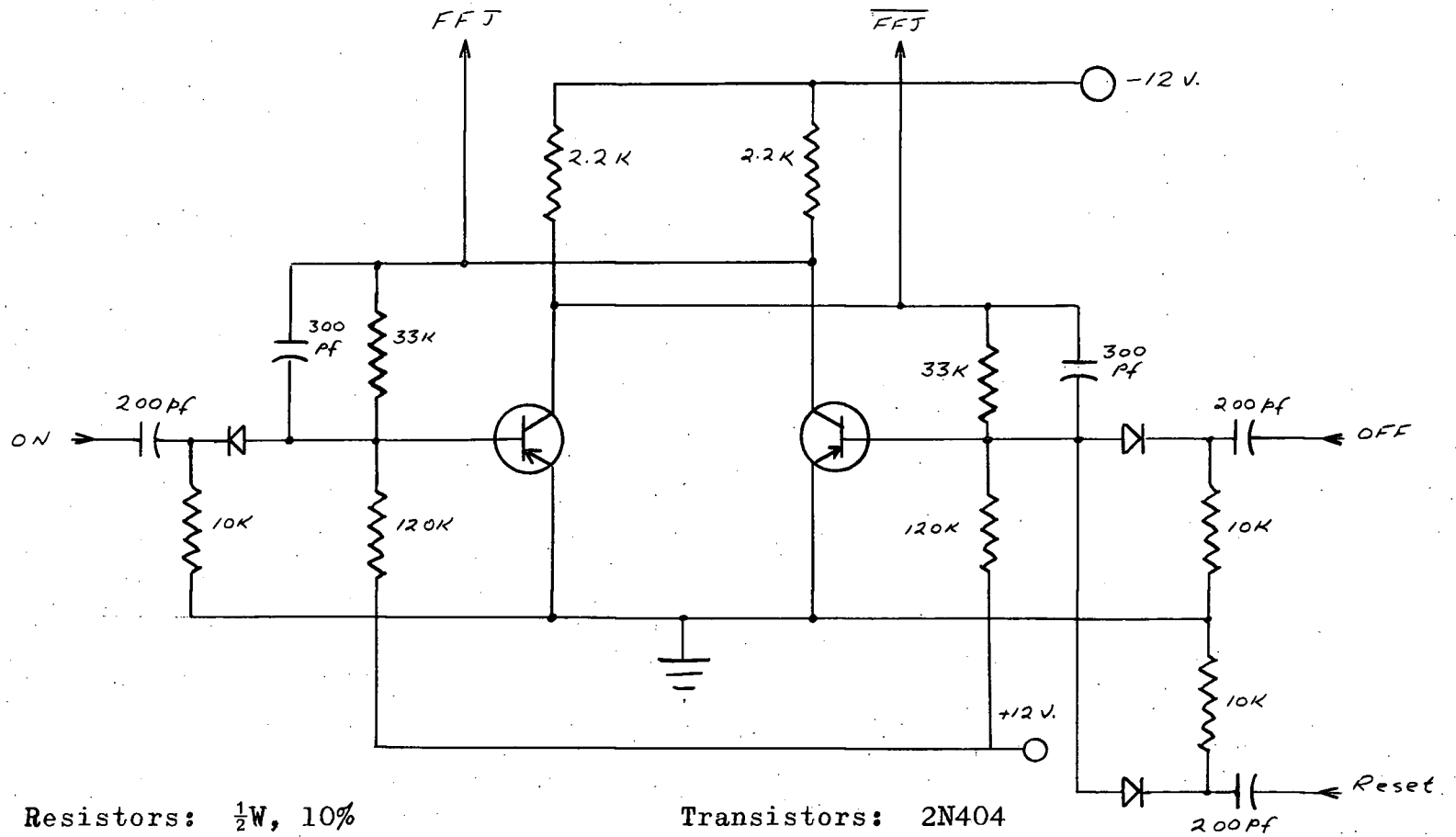
Resistors: ½W, 10%

Capacitors: 75V, 10%

Transistors: 2N398

Diodes: 1N34A

Figure 4-4. Circuit Diagram of Counter Driver Flip-Flop.



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Diodes: 1N34A

Figure 4-5. Circuit Diagram of Control Flip-Flop.

the circuit diagrams and waveforms shown in Figures 4-6 to 4-13. Gates G_1, G_3 and G_4 are standard diode AND gates and require no further explanation. Gate G_2 includes a transistor used to invert the m_9 pulse to achieve an inhibit action. The remainder of the circuit is a standard diode AND gate. Gates G_5, G_6, and G_7 use single transistors to gate the trigger pulses and also to invert and amplify them, providing sharp positive-going leading edges to trigger the counters. G_6 uses an additional transistor in a NOR* configuration to provide the required inhibit action. G_8 is a similar NOR gate.

This completes the description of the timing circuits. The next chapter describes the circuits of the remainder of the computer.

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* The output D of a NOR gate which has two inputs A and B is expressed logically as follows:

$$D = \overline{A + B} = \overline{A}.\overline{B}$$

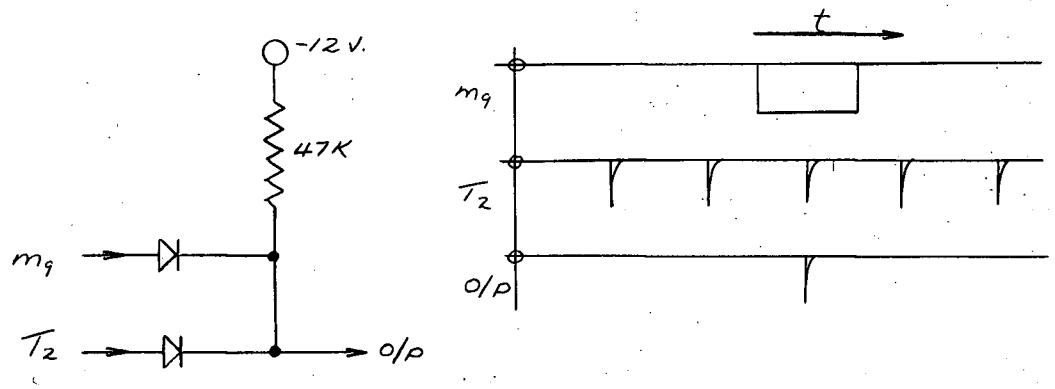


Figure 4-6. Circuit Diagram and Waveforms For G_1.

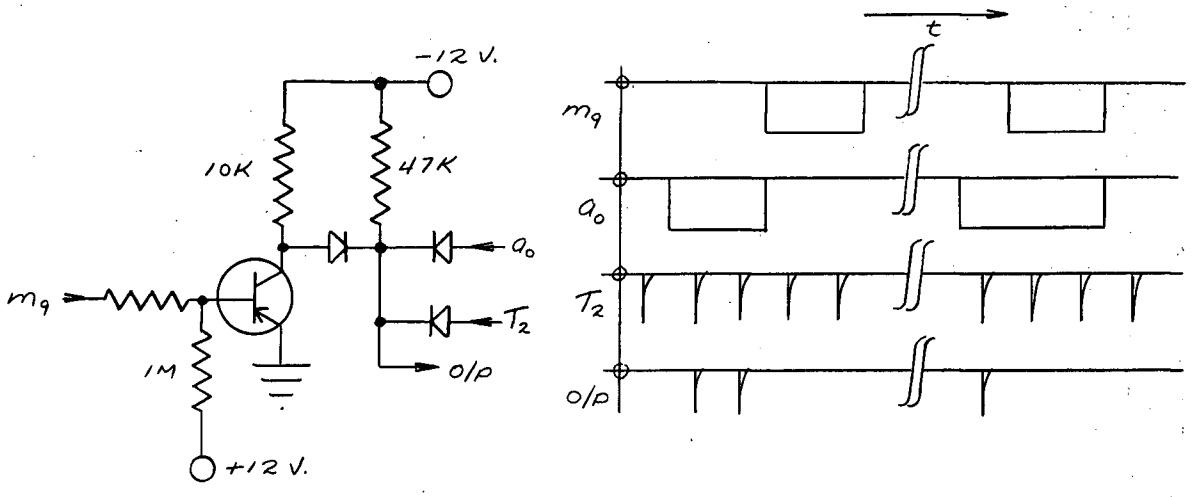


Figure 4-7. Circuit Diagram and Waveforms For G_2.

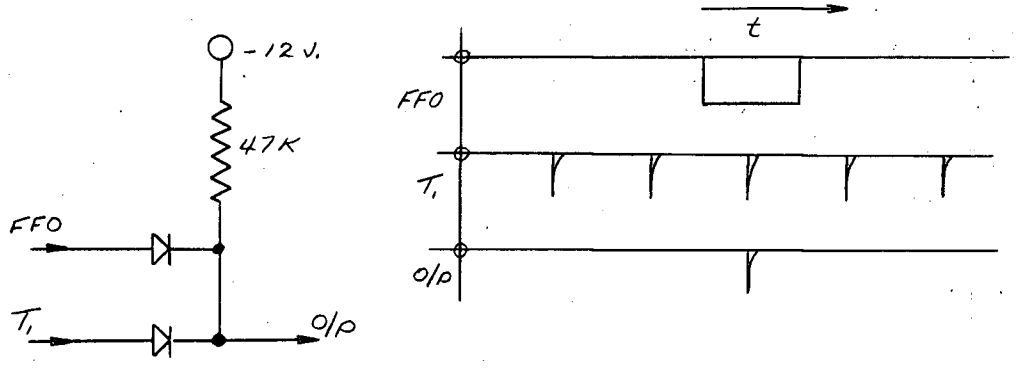


Figure 4-8. Circuit Diagram and Waveforms For G_3.

Resistors: $\frac{1}{2}$W, 10% Transistors: 2N404

Capacitors: 75V, 10% Diodes: 1N34A

(Figures 4-6 to 4-13 inclusive)

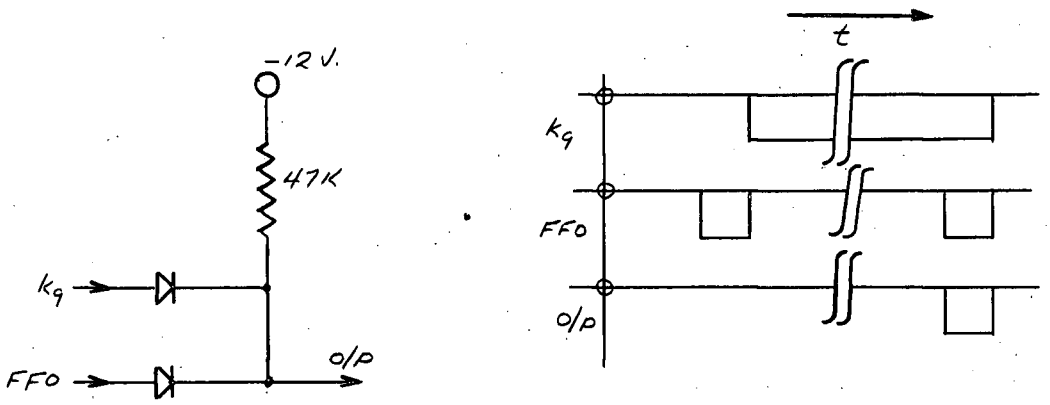


Figure 4-9. Circuit Diagram and Waveforms For G_4.

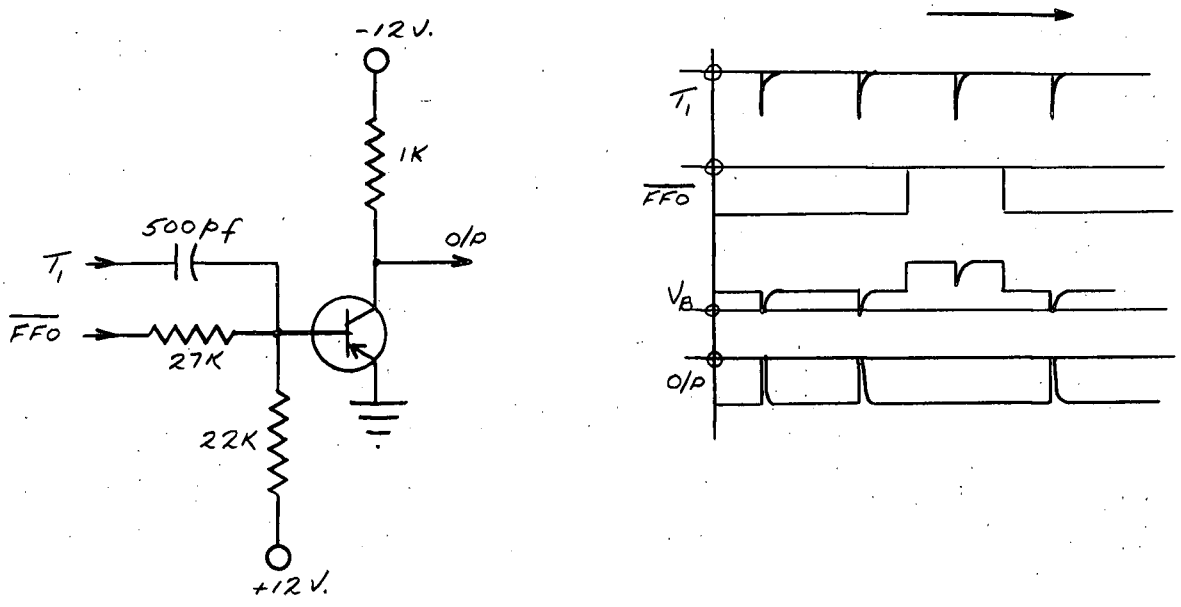


Figure 4-10. Circuit Diagram and Waveforms For G_5.

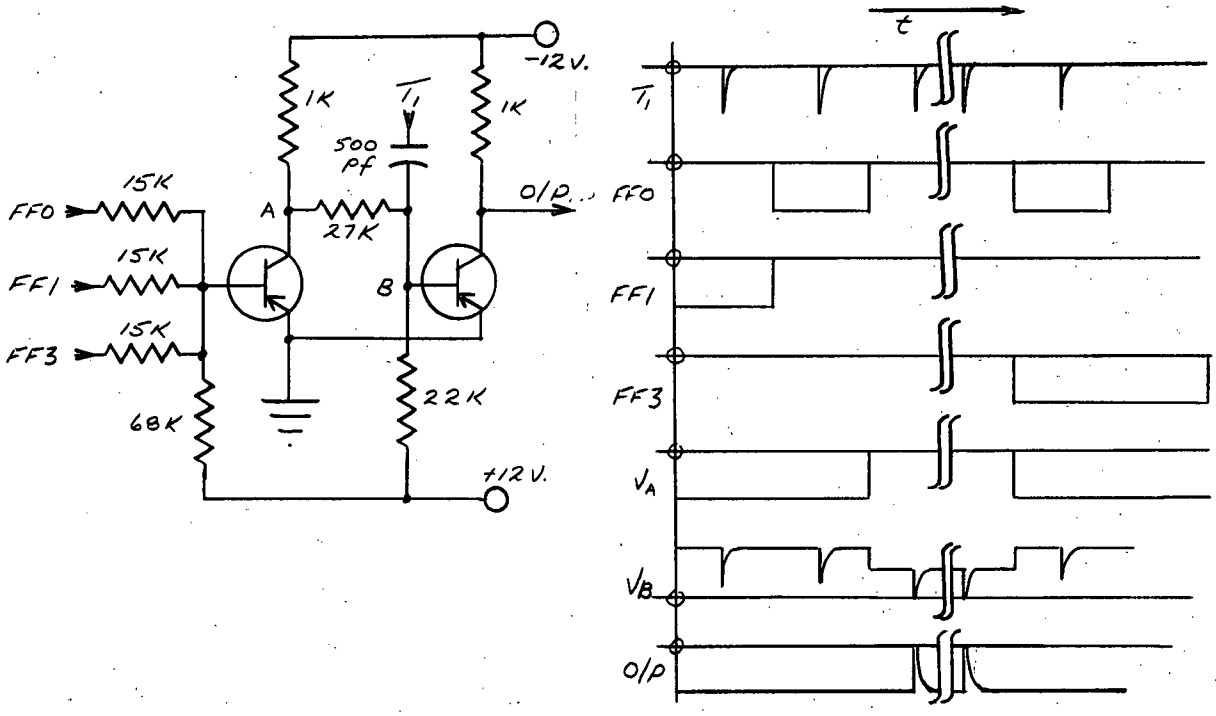


Figure 4-11. Circuit Diagram and Waveforms For G_6.

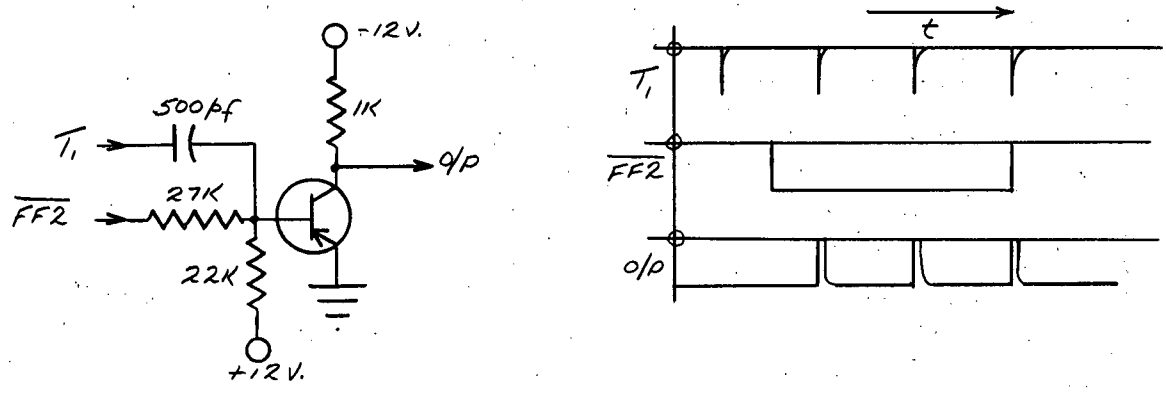


Figure 4-12. Circuit Diagram and Waveforms For G_7.

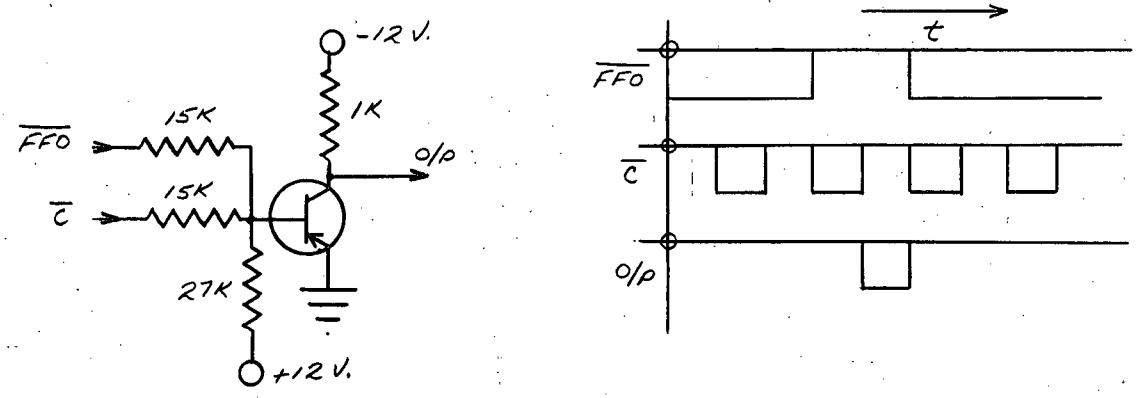


Figure 4-13. Circuit Diagram and Waveforms For G_8.

5. COMPUTING CIRCUITRY

In this chapter the circuits of the computer not included in the Timing Circuit are discussed. For ease of reference, the block diagram of the computer, Figure 3-6, is reproduced as Figure 5-1. The following major subdivisions, which comprise this part of the computer, are described as units:

1. Input Circuit
2. Shift Register
3. Weighting Factor Generators
4. g-Pulse Generator
5. x-Term Circuit
6. y-Term Circuit
7. Capacitor Summing Circuit
8. Sample and Clear Pulse Generator
9. Storage and Averaging Circuit
10. Reset Circuit

5-1. The Input Circuit.

The system signals x(t) and y(t) are fed into identical input circuits. Figure 5-2 shows the circuit diagram of the x Input Circuit. It includes the x-AMP, $|x|$, and $S.D._x$ circuits indicated in Figure 5-1. The potentiometer R_1 is ganged to the corresponding potentiometer in the y Input Circuit to provide a manual adjustment of the system signal levels. R_2 is a gain control which is adjusted to provide unity gain in the inverting amplifier. R_3 is a d-c adjustment to remove the

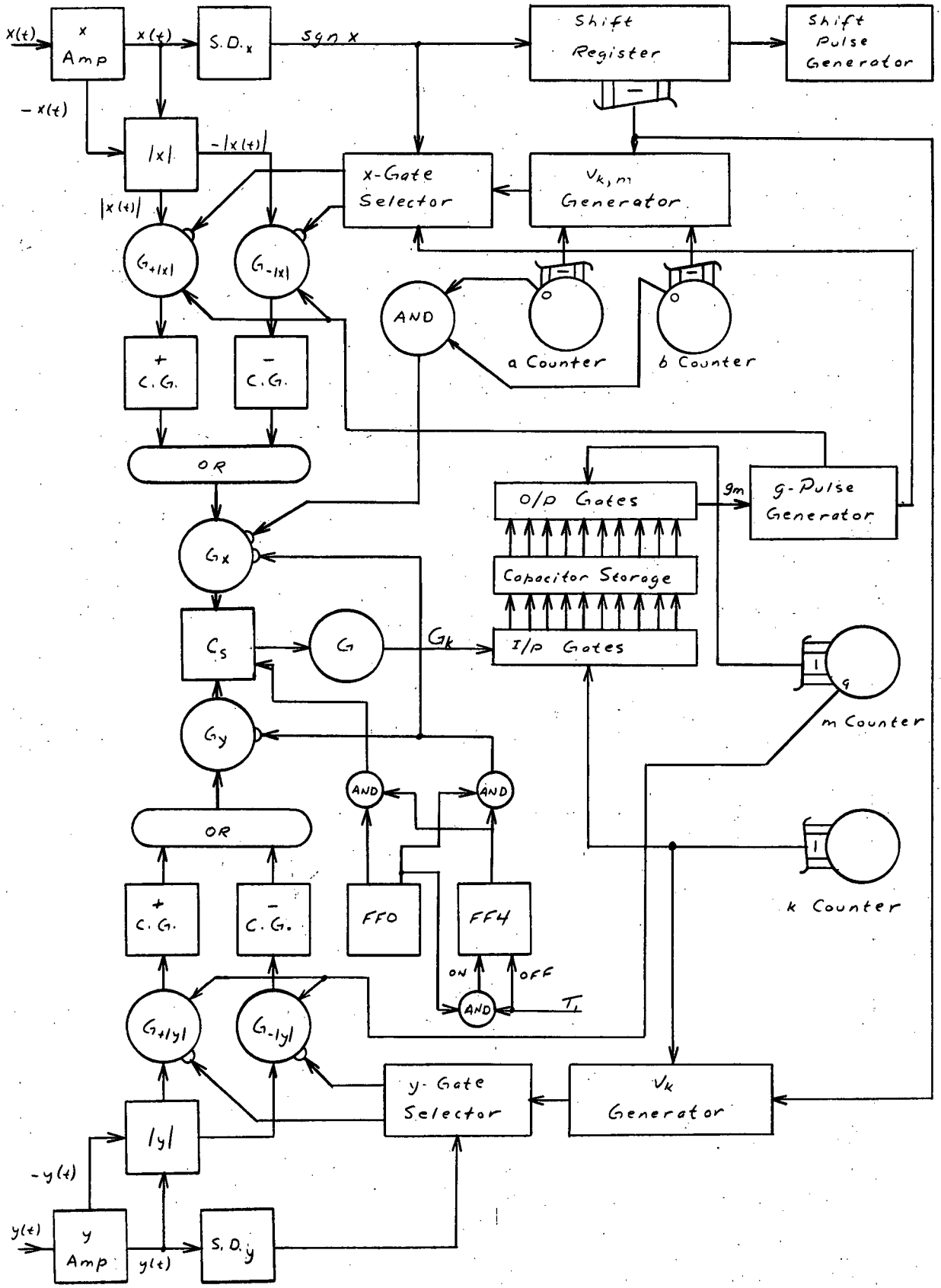
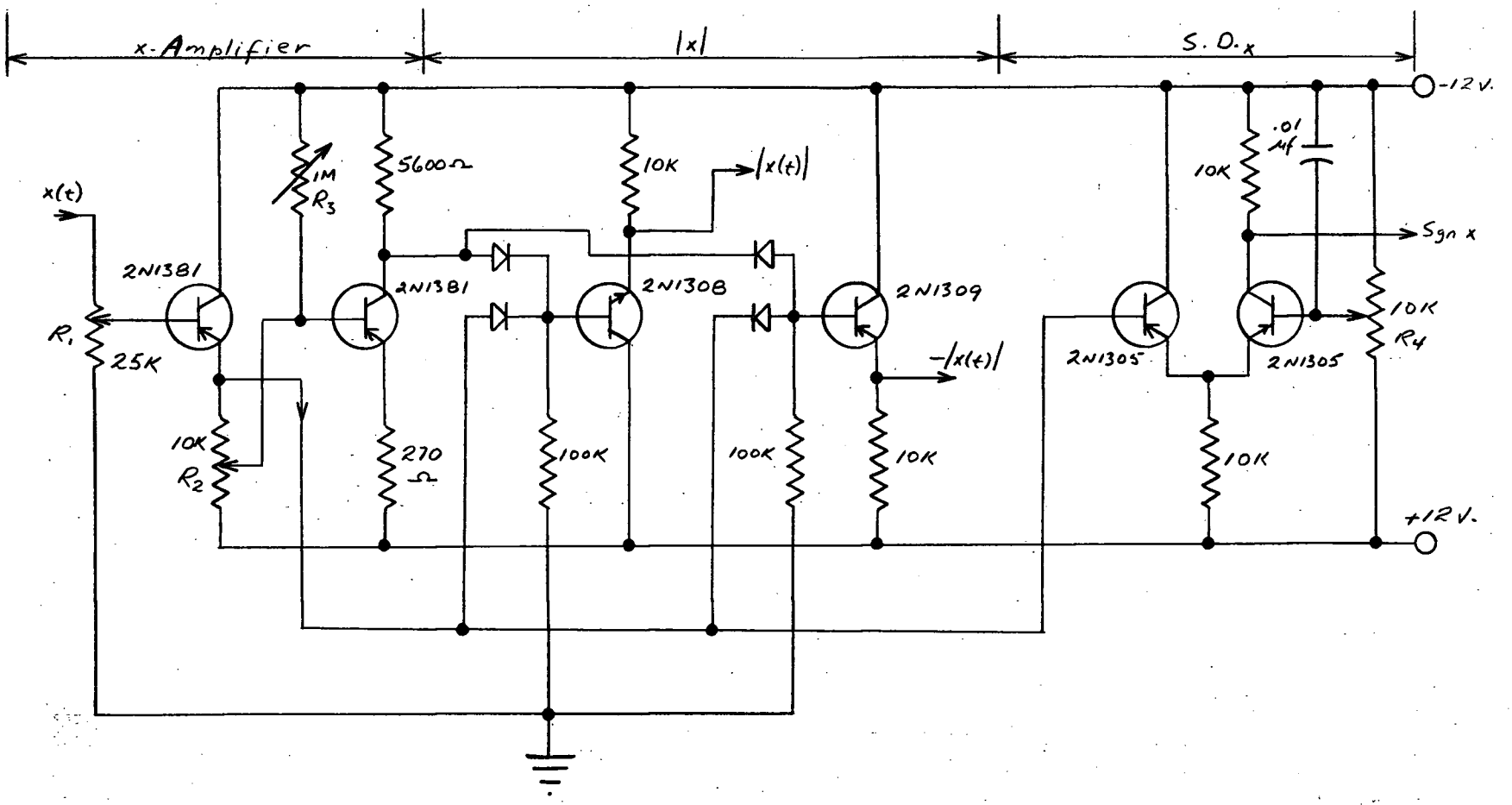


Figure 5-1. Block Diagram of Computer.



Resistors: $\frac{1}{2}$W, 10% Diodes: 1N497

Capacitors: 75V, 10%

Figure 5-2. x Input Circuit.

effect of small voltage drops in the inverting transistor. The output signals + $|x(t)|$ and - $|x(t)|$ are available as shown. Potentiometer R_4 is adjusted so that the output signal sgn x switches precisely when x(t) changes sign. Sgn x assumes the level -12 volts (representing the binary state 1) when x(t) is negative and 0 volts (representing the binary state 0) when x(t) is positive. The output represents sgn x only for levels of $|x(t)|$ exceeding a few tenths of a volt. This is sufficiently accurate for the application.

5-2. The Shift Register.

It is necessary to store the ten most recent values of sgn x = v(t) for use as the weighting factors $v(t-\tau_k)$ and $v(t-|\tau_k-u_m|)$. This is the purpose of the Shift Register. It consists of ten NOR flip-flops in a cascade arrangement, with each unit separated from the previous one by a shift gate. Figure 5-3 shows the circuit diagram. The quantity sgn x is inverted by the first transistor to produce $\overline{\text{sgn x}}$. Each signal is then applied through a 150K resistor to a .01μf capacitor. The signals on the capacitors are gated by the shift pulse and passed on to the input resistors of the first NOR flip-flop. The outputs from this flip-flop are in turn passed to identical RC networks where they are gated by the shift pulse and fed to the following flip-flop. The RC time constant of the coupling network is 1.5 msecs, much longer than the 20 μsec width of the shift pulse. The purpose of the RC combination is to hold each output of the previous flip-flop for the duration of the shift pulse so that the value of sgn x passed on to $(\text{flip-flop})_j$ is independent

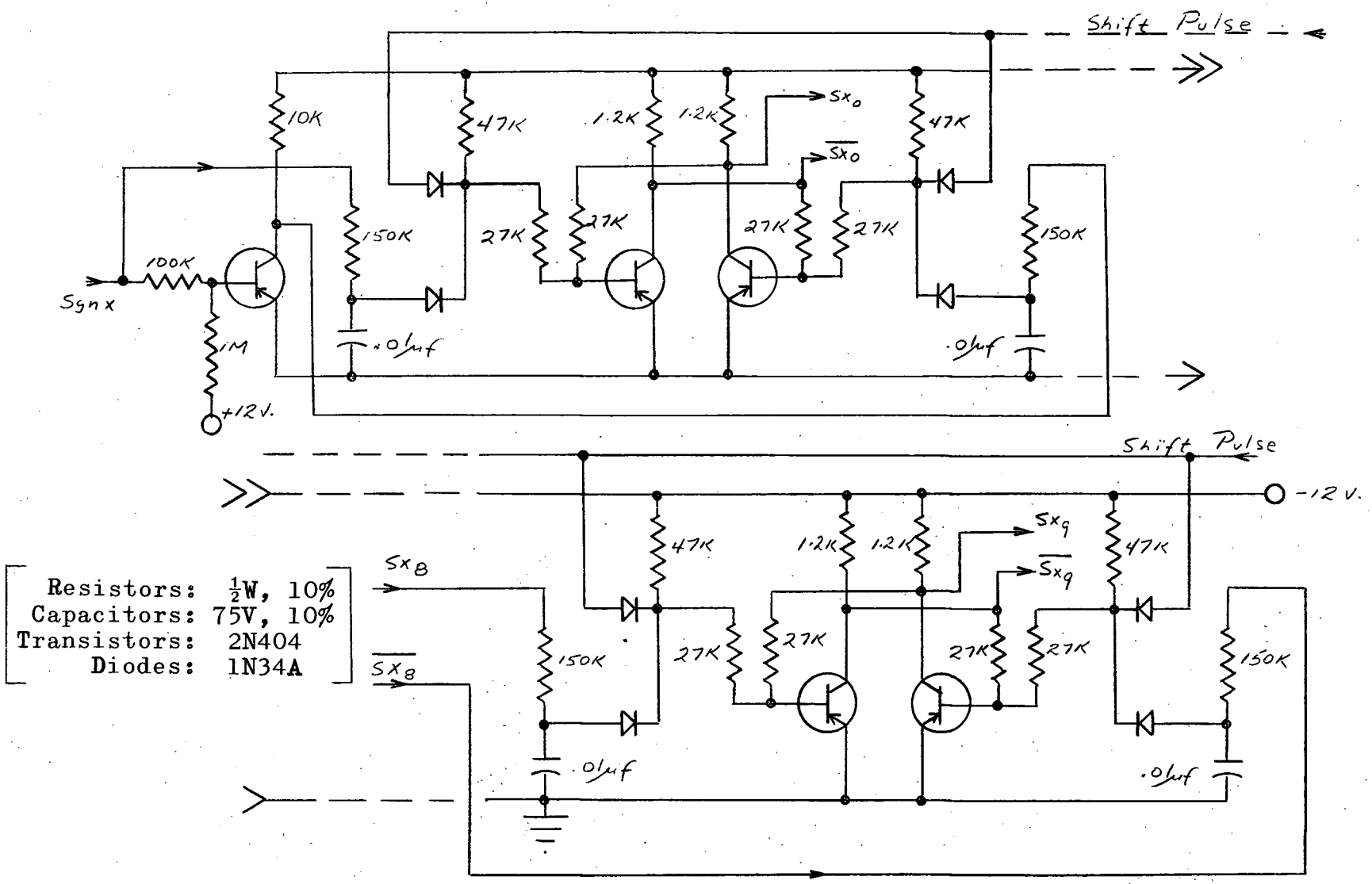


Figure 5-3. Circuit Diagram of Shift Register.

of the new value being stored in $(\text{flip-flop})_{j-1}$.

The circuit diagram of the shift pulse generator is shown in Figure 5-4. AM2 is a standard astable multivibrator with a period adjustable from 0.06 sec to 1.5 sec. Its output is used to trigger MM2, a monostable multivibrator which provides the 20 μsec shift pulse for the shift register.

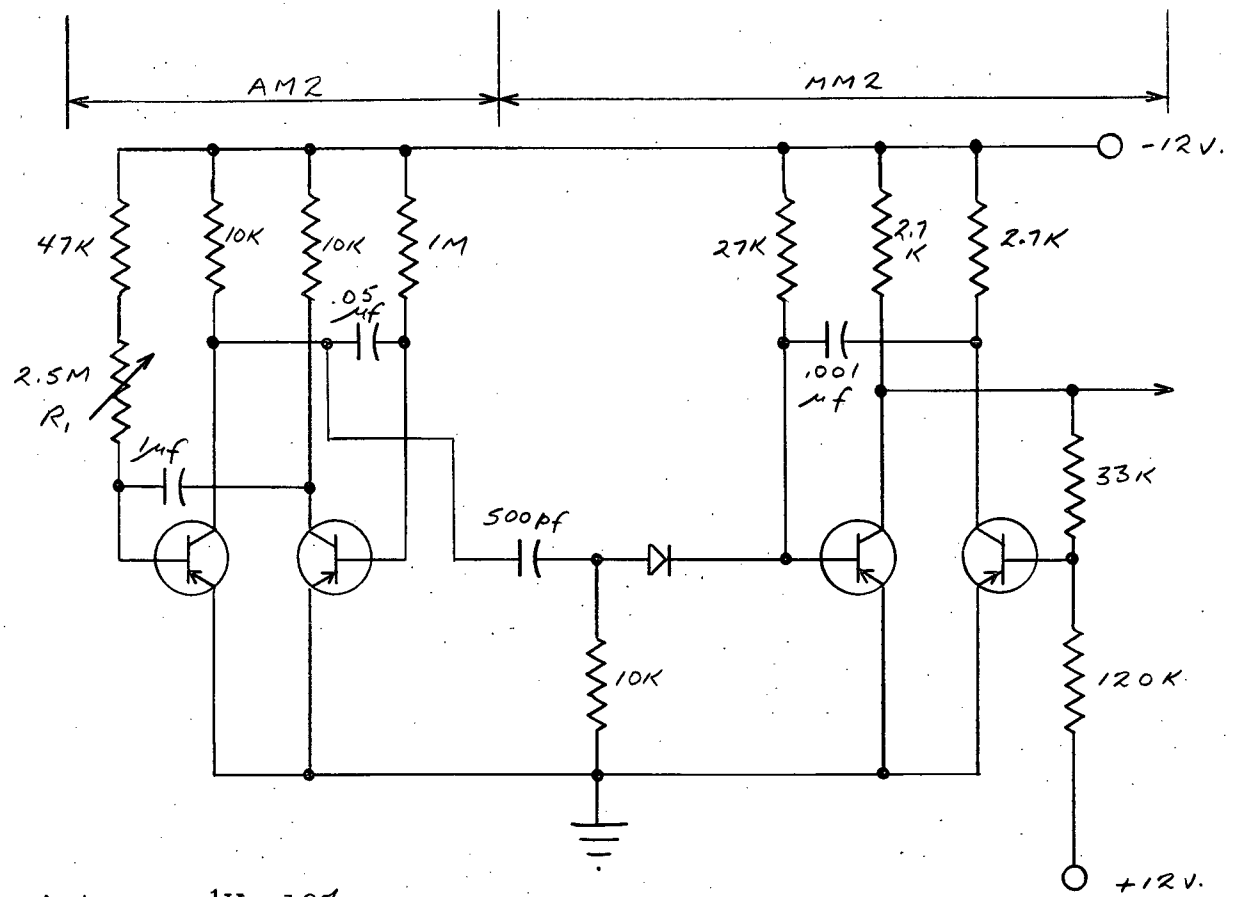
With the above range of adjustment of the shifting period, it is possible to vary the time interval T (see Figure 2-1) over the range 0.5 sec to 14 sec. An adjustment of this type is necessary in order to expand or compress the time scale to cover the significant part of the impulse response of the system under test.

5-3. Weighting Factor Generators.

These circuits, represented in Figure 5-1 by the v_k Generator and $v_{k,m}$ Generator blocks, are shown in Figures 5-5 and 5-6. The v_k Generator is a simple gating circuit in which the outputs of the Shift Register are sampled by the k counter. The diode gate outputs are fed to a NOR gate which is followed by an inverter to produce the signals v_k and $\bar{v}_k$, where v_k is given by the logical equation

$$v_k = k_0 \cdot (\text{sgn } x)_0 + \ldots + k_9 \cdot (\text{sgn } x)_9 \quad \ldots(5\text{-}1)$$

In the $v_{k,m}$ Generator the b counter samples the outputs of the Shift Register in one set of AND gates and the results are combined in an OR gate, producing the signal H. H is thus



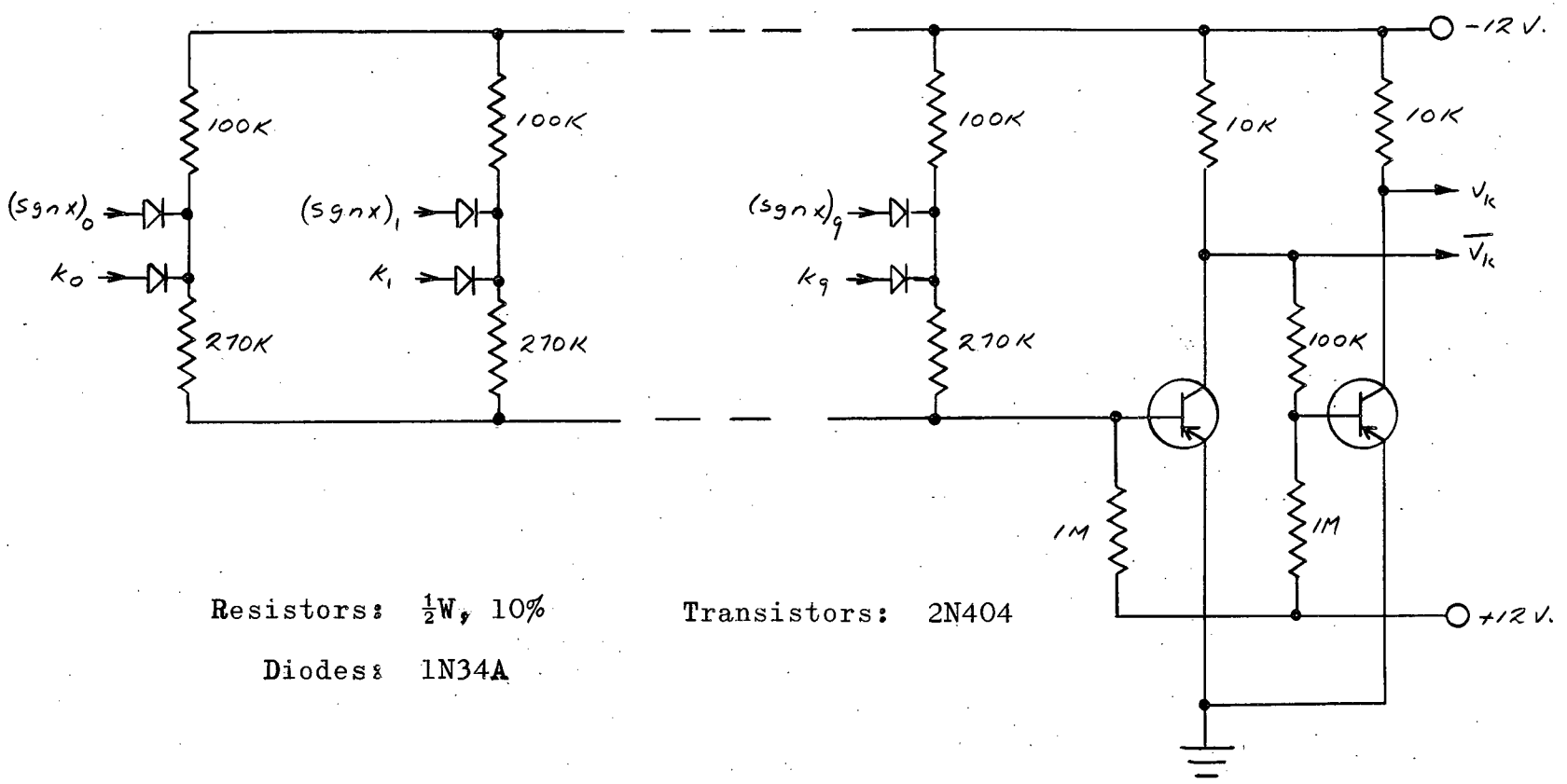
Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Diodes: 1N34A

Figure 5-4. Shift Pulse Generator.



Resistors: $\frac{1}{2}$W, 10%

Diodes: 1N34A

Transistors: 2N404

Figure 5-5. v_k Generator.

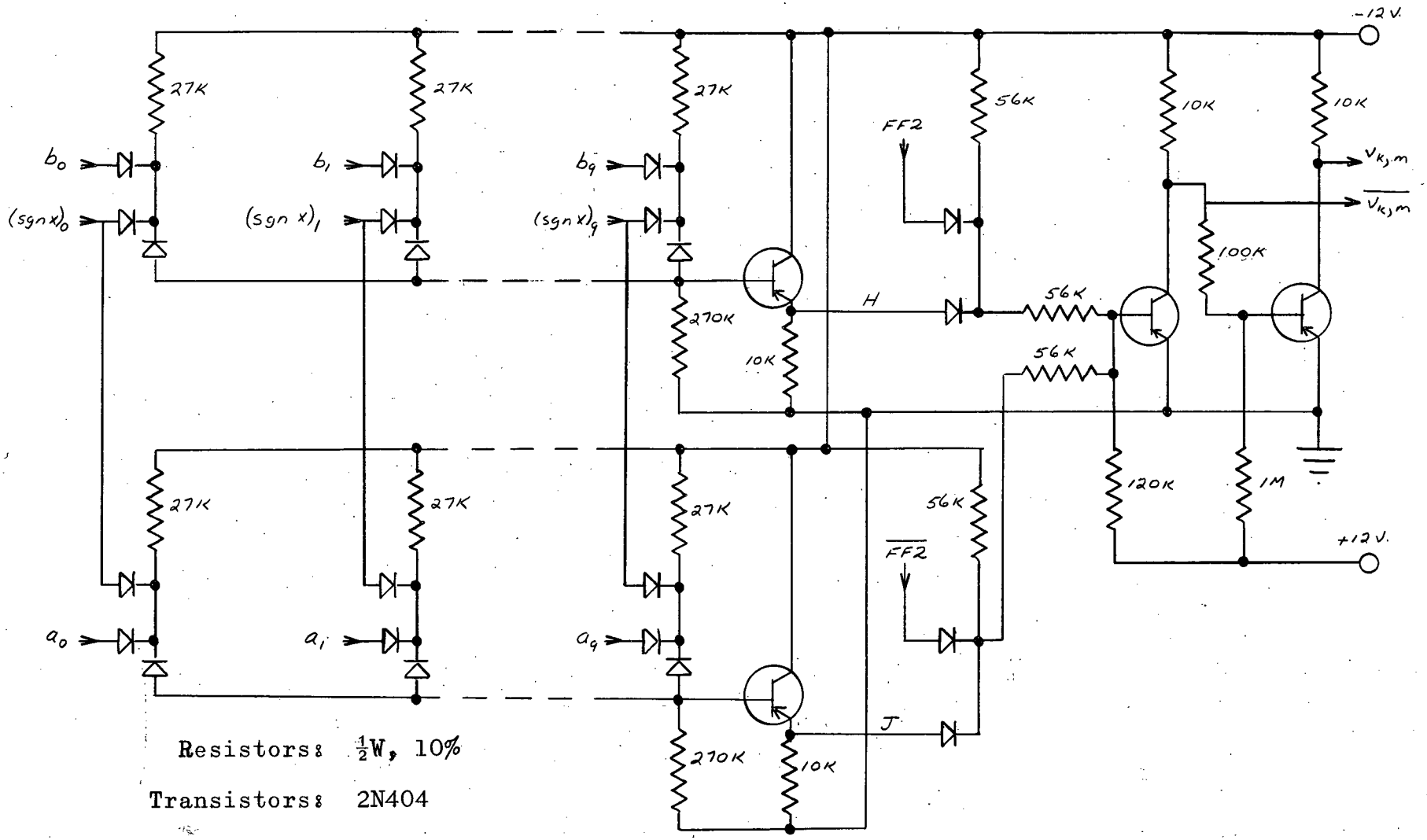


Figure 5-6. $v_{k,m}$ Generator.

given by the logical equation

$$H = b_0 \cdot (\text{sgn } x)_0 + \cdots + b_9 \cdot (\text{sgn } x)_9 \qquad \cdots(5\text{-}2)$$

The a counter also samples the outputs of the Shift Register in an identical manner to produce the signal J. Therefore,

$$J = a_0 \cdot (\text{sgn } x)_0 + \cdots + a_9 \cdot (\text{sgn } x)_9 \qquad \cdots(5\text{-}3)$$

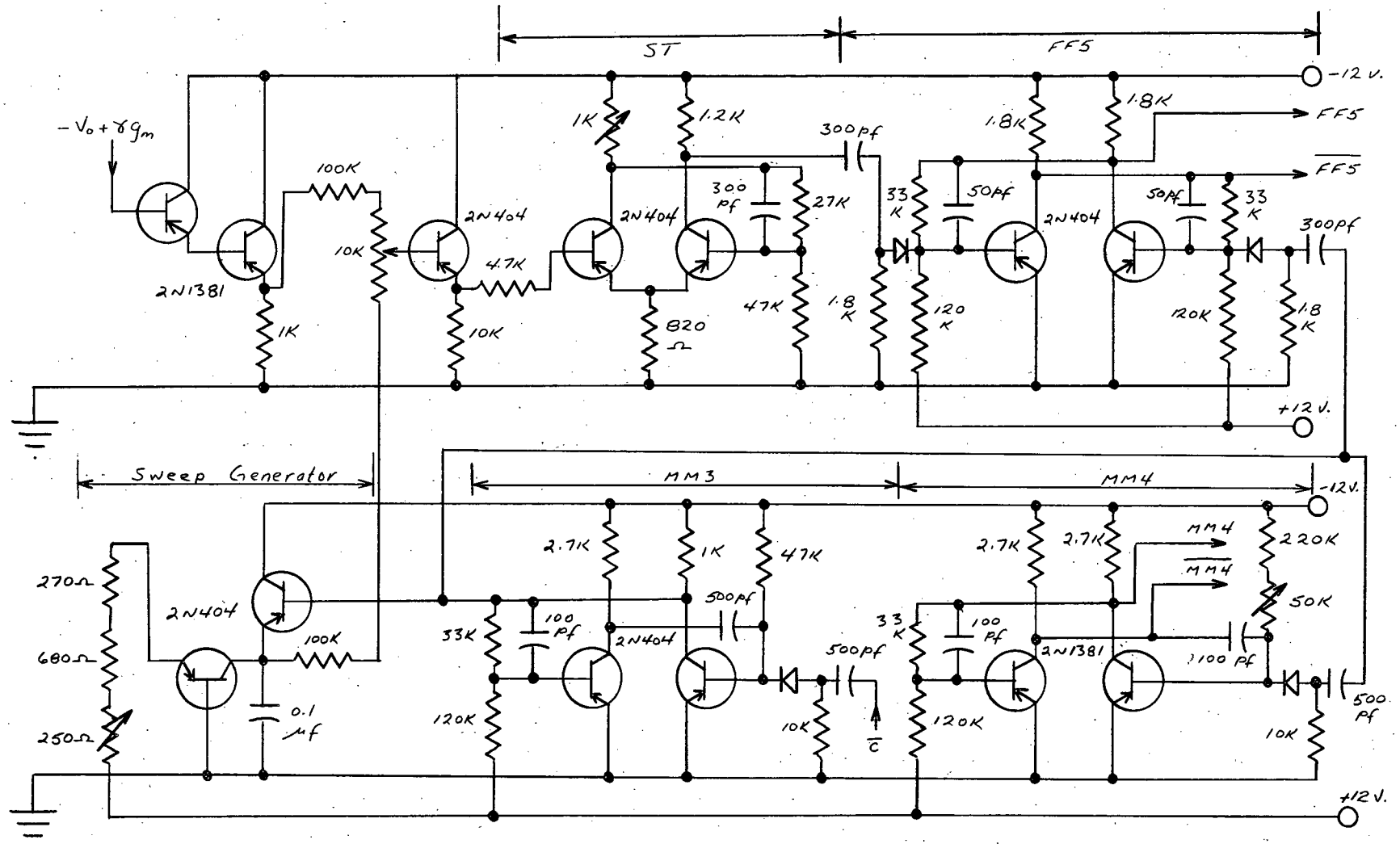
H and J are fed into separate AND gates with FF2 and $\overline{FF2}$ respectively, and the results are combined in a NOR gate and an inverter to produce $v_{k,m}$ and $\overline{v_{k,m}}$, where

$$v_{k,m} = FF2 \cdot \left[b_0 \cdot (\text{sgn } x)_0 + \cdots + b_9 \cdot (\text{sgn } x)_9 \right] + \overline{FF2} \cdot \left[a_0 \cdot (\text{sgn } x)_0 + \cdots + a_9 \cdot (\text{sgn } x)_9 \right] \qquad \cdots(5\text{-}4)$$

5-4. The g-Pulse Generator.

The purpose of this circuit is to generate, during each m period, a pulse proportional in width to the quantity $|g_m|$. The circuit diagram is shown in Figures 5-7 and 5-8. The circuit waveforms for two typical m periods are shown in Figure 5-9.

The output from the capacitor storage is equal to $-V_0 + \gamma g_m$ volts where $-V_0$ is a constant such that $-V_0 + \gamma g_m < 0$, and γ is a scale factor. (Addition of $-V_0$ permits the use of

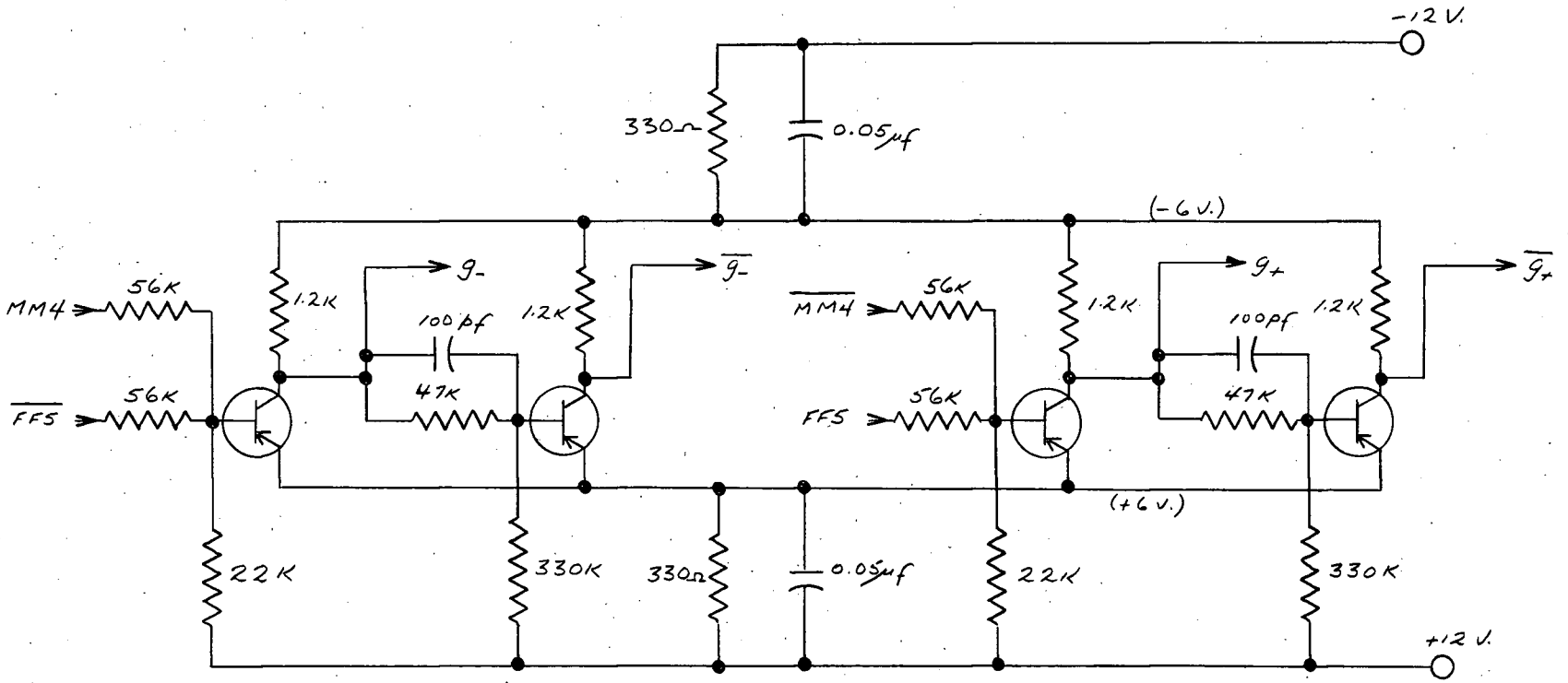


Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Diodes: 1N34A

Figure 5-7. g-Pulse Switching Circuit.



Resistors: $\frac{1}{2}$W, 10% Capacitors: 75V, 10%

Transistors: 2N404

Figure 5-8. g-Pulse Generator Logic.

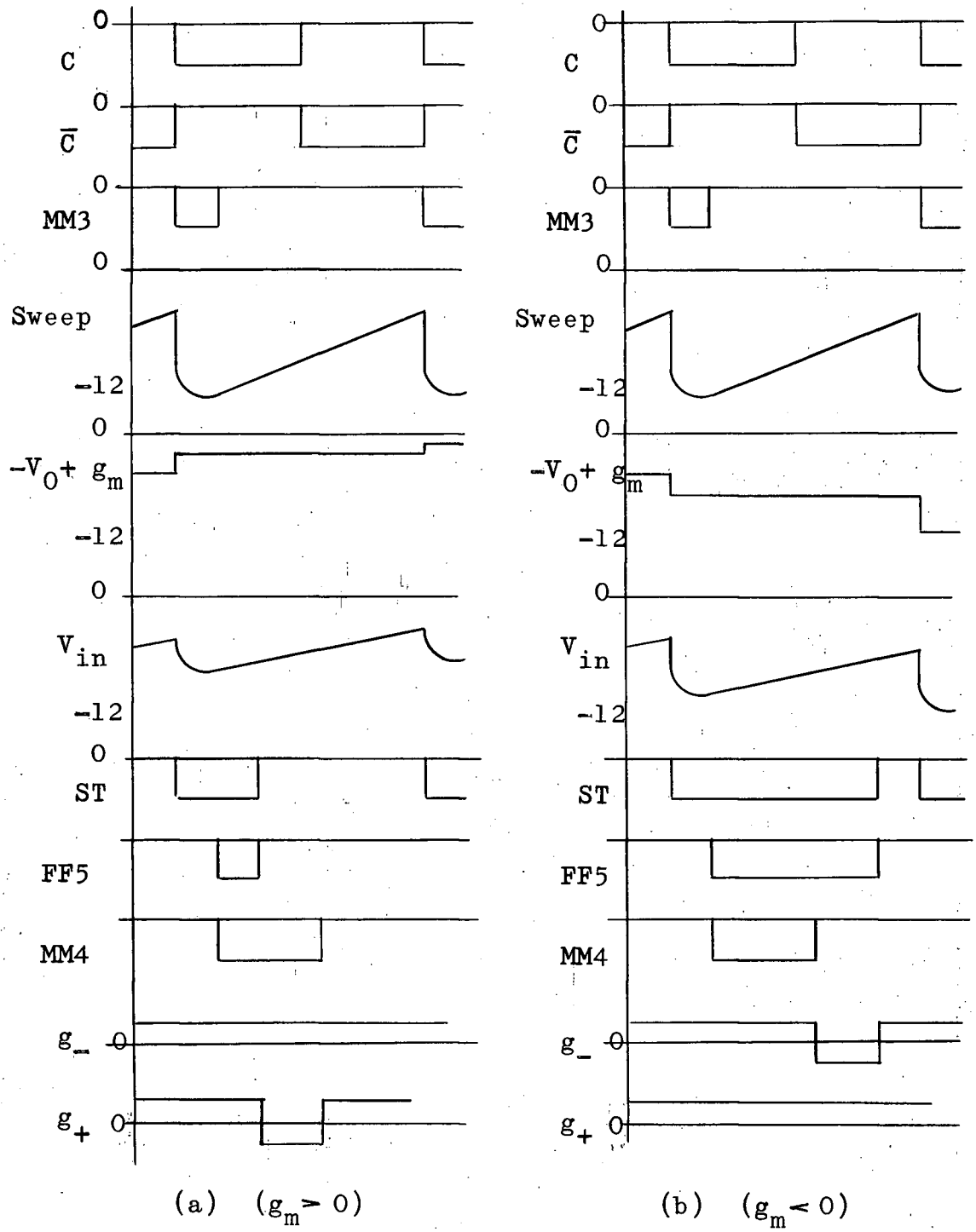


Figure 5-9. g-Pulse Generator Waveforms.

simpler storage and gating circuits). The voltage $-V_0 + \gamma g_m$ is the input to the g-Pulse Generator. A double emitter follower arrangement at the input provides a very high impedance to the capacitor storage output. At the beginning of each m period, the clock signal $\overline{C}$ triggers the monostable multivibrator MM3. This applies a -12 volt reset pulse of approximately 10 μsec duration to the sweep circuit. The output signal of the sweep generator is shown in Figure 5-9. This signal and the signal $-V_0 + \gamma g_m$ are summed by the 100K resistors and the result is applied through an emitter follower to the Schmidt Trigger (ST).

The sweep signal can be expressed in the form

$$V_s = -12 + c\ t \qquad (t \leqq 12/c) \qquad \ldots(5\text{-}5)$$

where c is the sweep slope and t is the time from the beginning of the sweep. The input to ST is therefore

$$V_{in} = \frac{\left[-V_o + \gamma g_m\right] - 12 + c\ t}{2} \qquad \ldots(5\text{-}6)$$

ST is set to switch when V_{in} reaches -6 volts. Suppose it switches at time t_1 after the beginning of the sweep. Equation (5-6) can then be written as

$$-6 = \frac{\left[-V_0 + \gamma g_m\right] - 12 + c\ t_1}{2} \qquad \ldots(5\text{-}7)$$

It follows that

$$t_1 = \frac{V_0 - \gamma g_m}{c} \qquad \ldots(5\text{-}8)$$

FF5 is turned ON at the beginning of the sweep and is turned OFF when ST switches. It is therefore ON for the time interval t_1. The monostable multivibrator MM4 also is turned ON at the beginning of the sweep. It is adjusted to turn OFF after a time interval

$$t_2 = \frac{V_0}{c} \qquad \ldots(5\text{-}9)$$

It follows that a pulse defined as

$$g_- \triangleq FF5 \cdot \overline{MM4} \qquad \ldots(5\text{-}10)$$

has a width equal to

$$\begin{aligned}(\Delta t)_- &= t_1 - t_2 \\ &= -(\gamma/c)\, g_m \qquad (g_m \leqq 0)\end{aligned} \qquad \ldots(5\text{-}11)$$

and also that a pulse defined as

$$g_+ \triangleq \overline{FF5} \cdot MM4 \qquad \ldots(5\text{-}12)$$

has a width equal to

$$(\Delta t)_+ = t_2 - t_1$$

$$= (\gamma/c)\ g_m \quad (g_m \geqq 0) \qquad \ldots(5\text{-}13)$$

The pulses g_- and g_+ and their logical complements are generated by the circuitry shown in Figure 5-8 which consists of two NOR gates and two inverters. The output levels have been shifted from 0 and -12 volts to +6 and -6 volts for use in the x-Term Circuit, which is described in the following section.

5-5. The x-Term Circuit.

This circuit generates a current, proportional to $\left| x(t)\ v_{k,m} \right|$, which is directed into or out of the summing capacitor C_s for a time proportional to $|g_m|$. The gating arrangement is such that the resulting voltage change on C_s is equal to

$$(\Delta V_{C_s})_x = -\beta x(t)\ v_{k,m}\ g_m \qquad \ldots(5\text{-}14)$$

where β is a positive scale factor.

Consider the function

$$z_{k,m} \triangleq \operatorname{sgn}\left[v_{k,m} x(t) \right] \qquad \ldots(5\text{-}15)$$

Equation (5-15) can be expressed in logical form as follows:

$$z_{k,m} = v_{k,m} \cdot \overline{\operatorname{sgn} x(t)} + \overline{v_{k,m}} \cdot \operatorname{sgn} x(t) \qquad \ldots(5\text{-}16)$$

Figure 5-10 shows the circuitry which generates $z_{k,m}$ and $\overline{z_{k,m}}$. Three NOR gates and two inverters are used and the output levels are shifted from 0 and -12 volts to +6 and -6 volts.

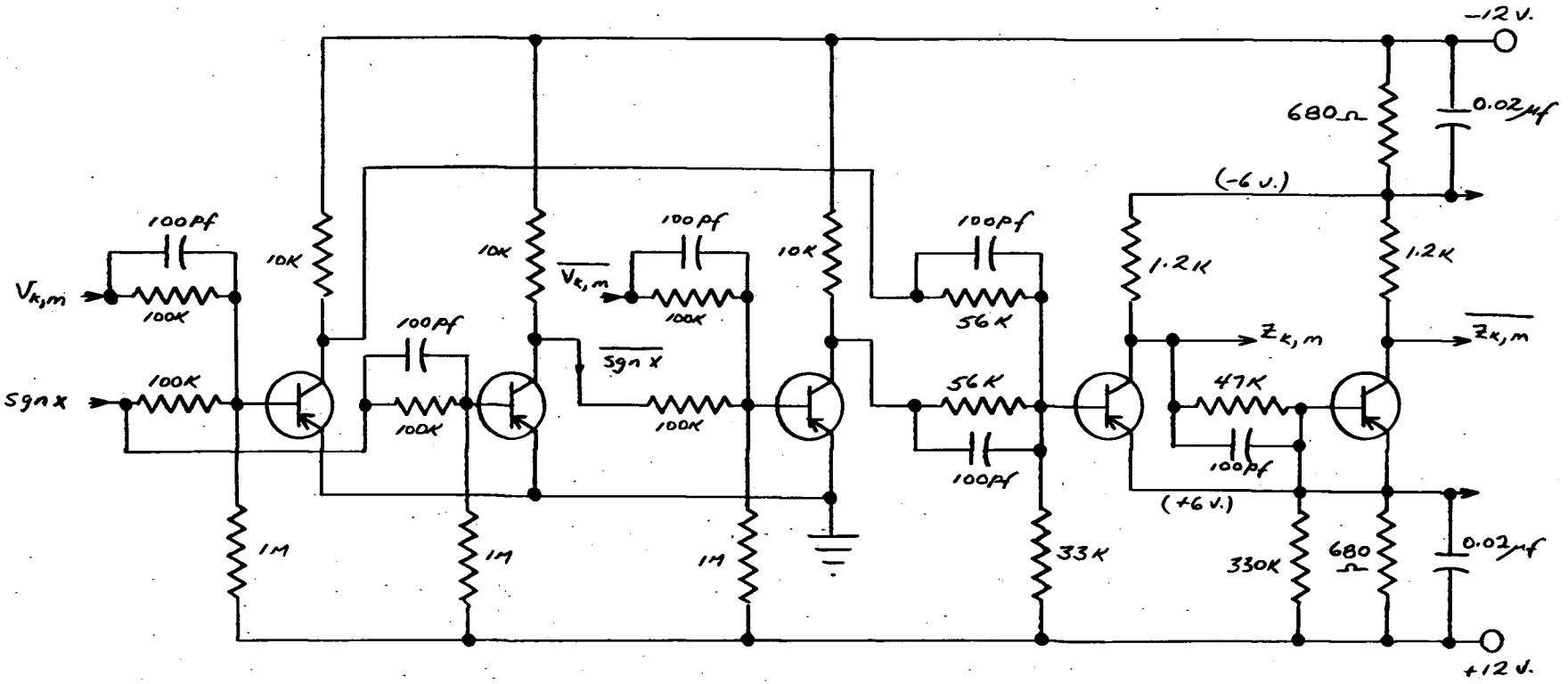
Consider now the circuit shown in Figure 5-11. Transistor T_6 is in the grounded base configuration with the collector connected to C_s. The voltage on C_s is always negative. Thus the emitter of T_6 is held very close to ground potential, provided that the associated circuitry can supply the emitter current as shown. This latter requirement is satisfied by the resistor network R6, through which a constant current, I_{cx}, is provided by the +12 volt supply. The resistor networks R_4 and R_5 are adjusted so that

$$R_4 = R_5 \triangleq R_x \qquad \ldots(5\text{-}17)$$

The combined action of the gating signals, $z_{k,m}$, $\overline{z_{k,m}}$, g_-, $\overline{g_-}$, g_+, and $\overline{g_+}$, causes saturation of one of the transistors T_1, T_2, T_3, or T_4 for a time proportional to $|g_m|$, reducing the collector-emitter voltage of this transistor to almost zero. The current through the transistor is therefore approximately equal to

$$I_x = \frac{|x(t)|}{R_x} \qquad \ldots(5\text{-}18)$$

This current is added to the current I_{cx}, and the sum is passed through T_6. The resistances are so adjusted that



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Figure 5-10. x-Term Circuit Part A.

$I_{cx} > I_x$, ensuring that there is always current through T_6 in the proper direction. Resistance network R_7 and transistor T_7 provide a constant current, I_{cx}, through T_7 as shown. The result is that the net current $(I_{C_s})_x$ is equal to $\pm I_x$.

This causes a voltage change on C_s equal to

$$(\Delta V_{C_s})_x = \frac{(\pm I_x)\ \Delta t}{C_s} \qquad \ldots(5\text{-}19)$$

Combining Equations (5-11), (5-13), (5-18) and (5-19) yields

$$(\Delta V_{C_s})_x = \pm \left| \frac{\gamma}{c} \frac{1}{R_x C_s}\ x(t)\ g_m \right| \qquad \ldots(5\text{-}20)$$

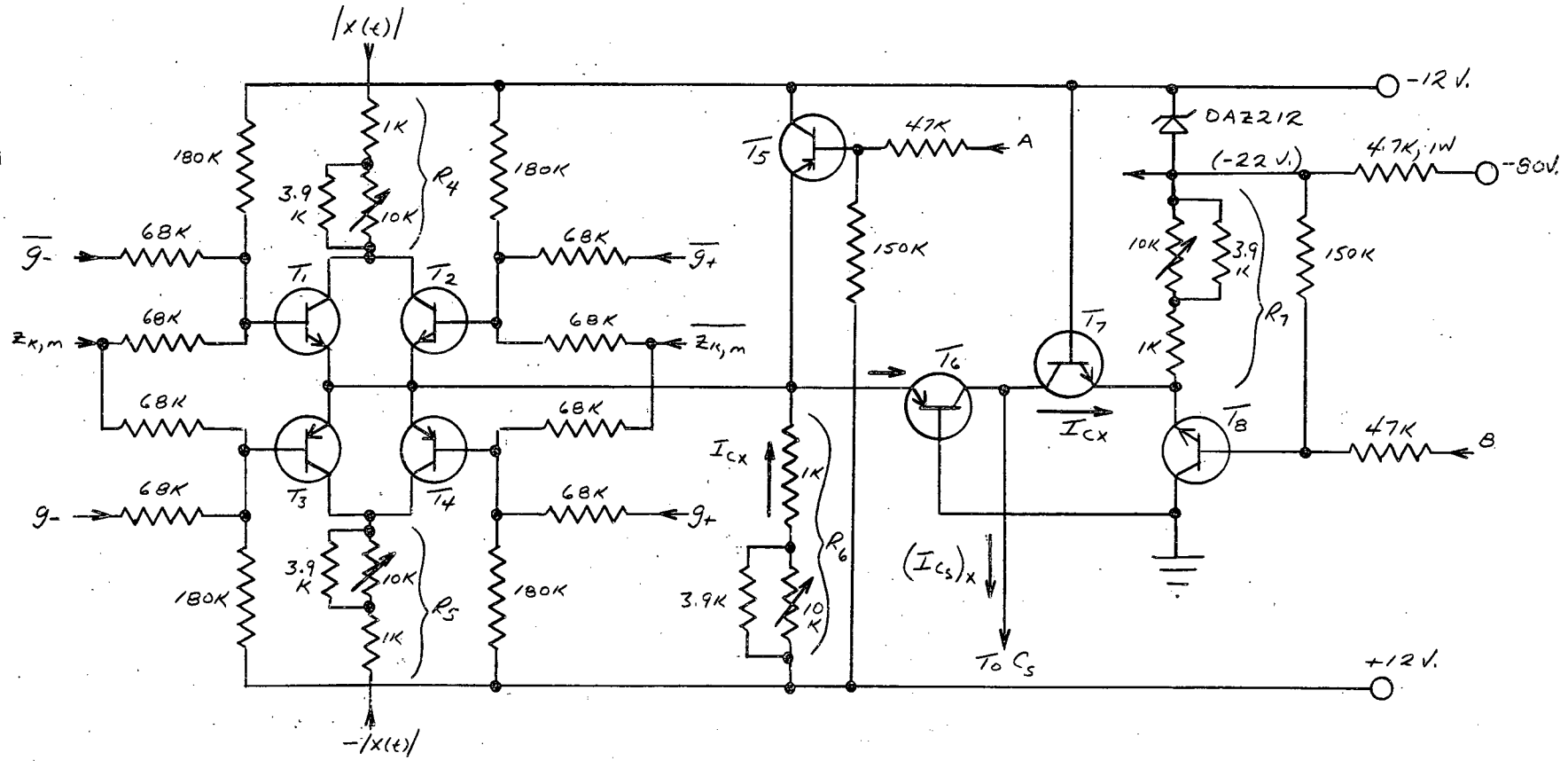
If now the selection of T_1, T_2, T_3, or T_4 by the gating signals is considered, it can be seen that $(\Delta V_{C_s})_x$ is given by the following equation:

$$(\Delta V_{C_s})_x = -\beta\ x(t)\ v_{k,m} \qquad \ldots(5\text{-}21)$$

where

$$\beta = \frac{\gamma}{c}\ \frac{1}{R_x C_s} \qquad \ldots(5\text{-}22)$$

Transistors T_5 and T_8 are employed to block $(I_{C_s})_x$ during the interval for which m = k and also during the Sample interval. (See Chapter 3). This blocking action is controlled by the circuit shown in Figure 5-12. During either of these intervals a -12 volt signal and a 0 volt signal are produced at points A



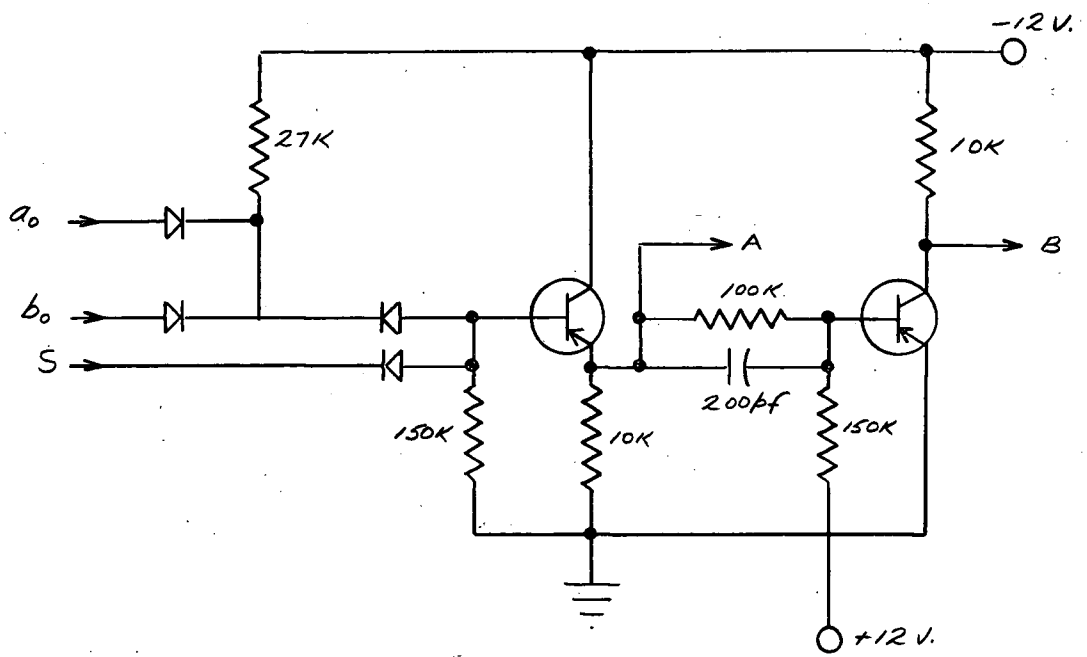
Transistors: T_1, T_2, T_7, T_8 2N1308

T_3, T_4 2N1309

T_5, T_6 2N1381

Resistors: $\frac{1}{2}$W, 10% unless otherwise specified

Figure 5-11. x-Term Circuit Part B.



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Diodes: 1N34A

Figure 5-12. x-Term Circuit Part C.

and B respectively of the circuits shown in Figures 5-12 and 5-11. This has the effect of cutting off transistors T_6 and T_7, and blocks $(I_{C_s})_x$.

5-6. The y-Term Circuit.

The operation of this circuit is very similar to that of the x-Term Circuit. A current proportional to $|y(t)|$ is gated into or out of the summing capacitor for the duration of the m_9 period, causing a voltage change on C_s equal to

$$(\Delta V_{C_s})_y = \alpha\ y(t)\ v_k \qquad \ldots(5\text{-}23)$$

where α is a positive scale factor.

The function w_k is defined as follows:

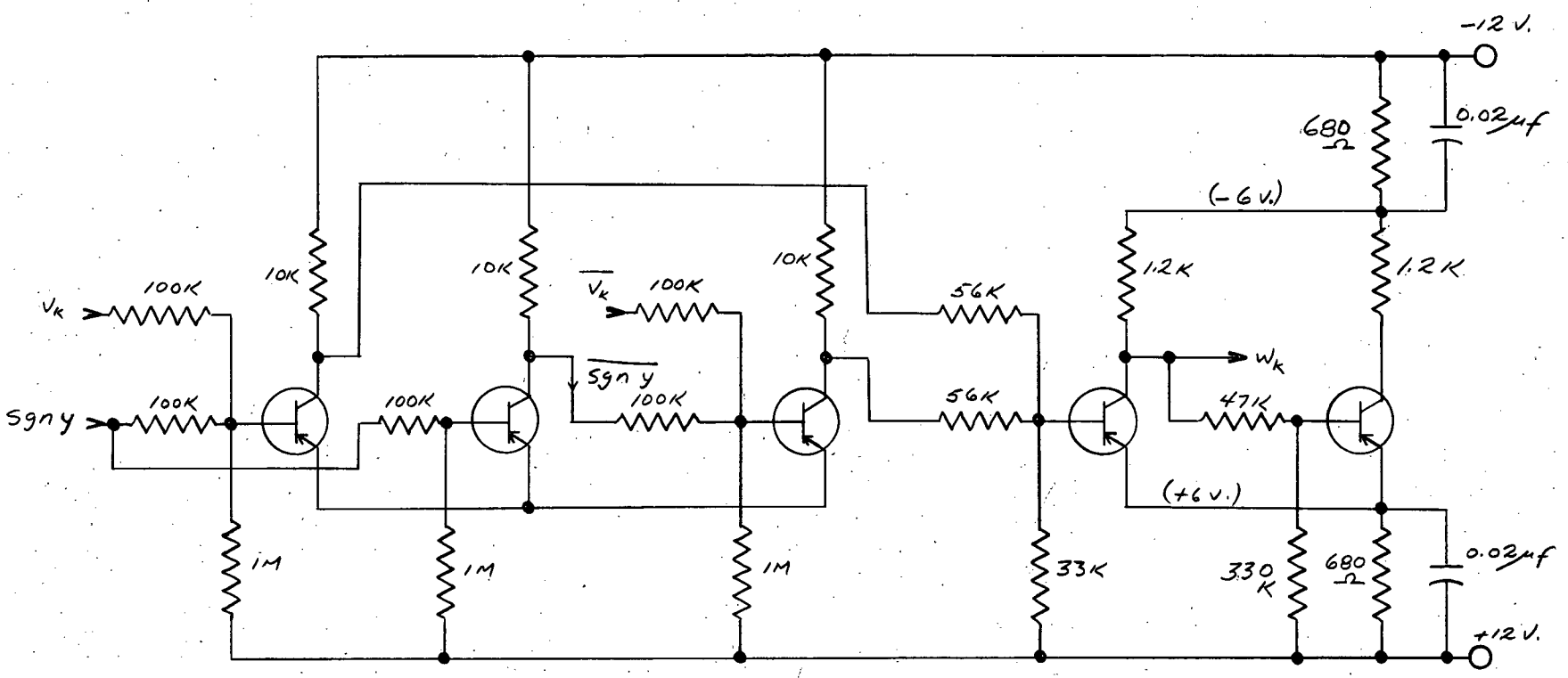
$$w_k \triangleq \text{sgn}\left[v_k\ y(t)\right] \qquad \ldots(5\text{-}24)$$

Equation (5-24) can be expressed in logical form as follows:

$$w_k = v_k \cdot \overline{\text{sgn}\ y(t)} + \overline{v_k} \cdot \text{sgn}\ y(t) \qquad \ldots(5\text{-}25)$$

Figure 5-13 shows the circuit used to produce w_k. The signal $\overline{w_k}$ is also produced but not used. However, the extra part of the circuit serves to provide the +6 and -6 volt sources.

Additional control signals are required for gating the current during the m_9 period. These are derived from the m_9 pulse by the circuit shown in Figure 5-14. The circuit, consisting simply of two inverters, produces the signals M_9 and



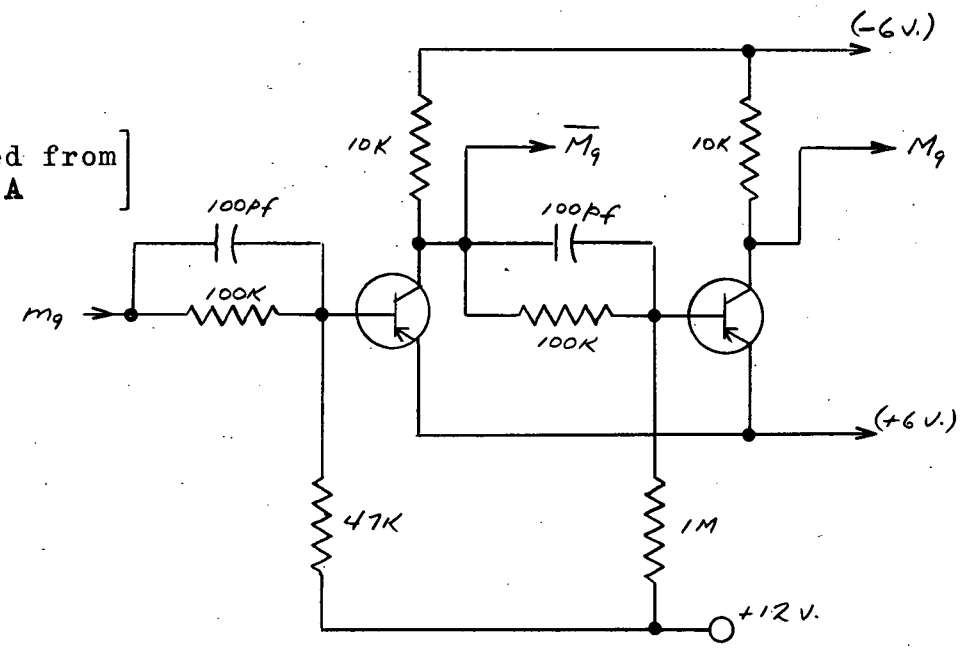
Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Figure 5-13. y-Term Circuit Part A.

[+6, -6 volts obtained from x-Term Circuit Part A]



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Figure 5-14. y-Term Circuit Part B.

$\overline{M_9}$, which are logically equivalent to m_9 and $\overline{m_9}$ respectively. However, the levels have been shifted from 0 and -12 volts to +6 and -6 volts. The signals w_k, M_9 and $\overline{M_9}$ are used as shown in Figure 5-15. The operation of this part of the circuit is very similar to that of the corresponding part of the x-Term Circuit. The resistances R_1 and R_2 are adjusted so that

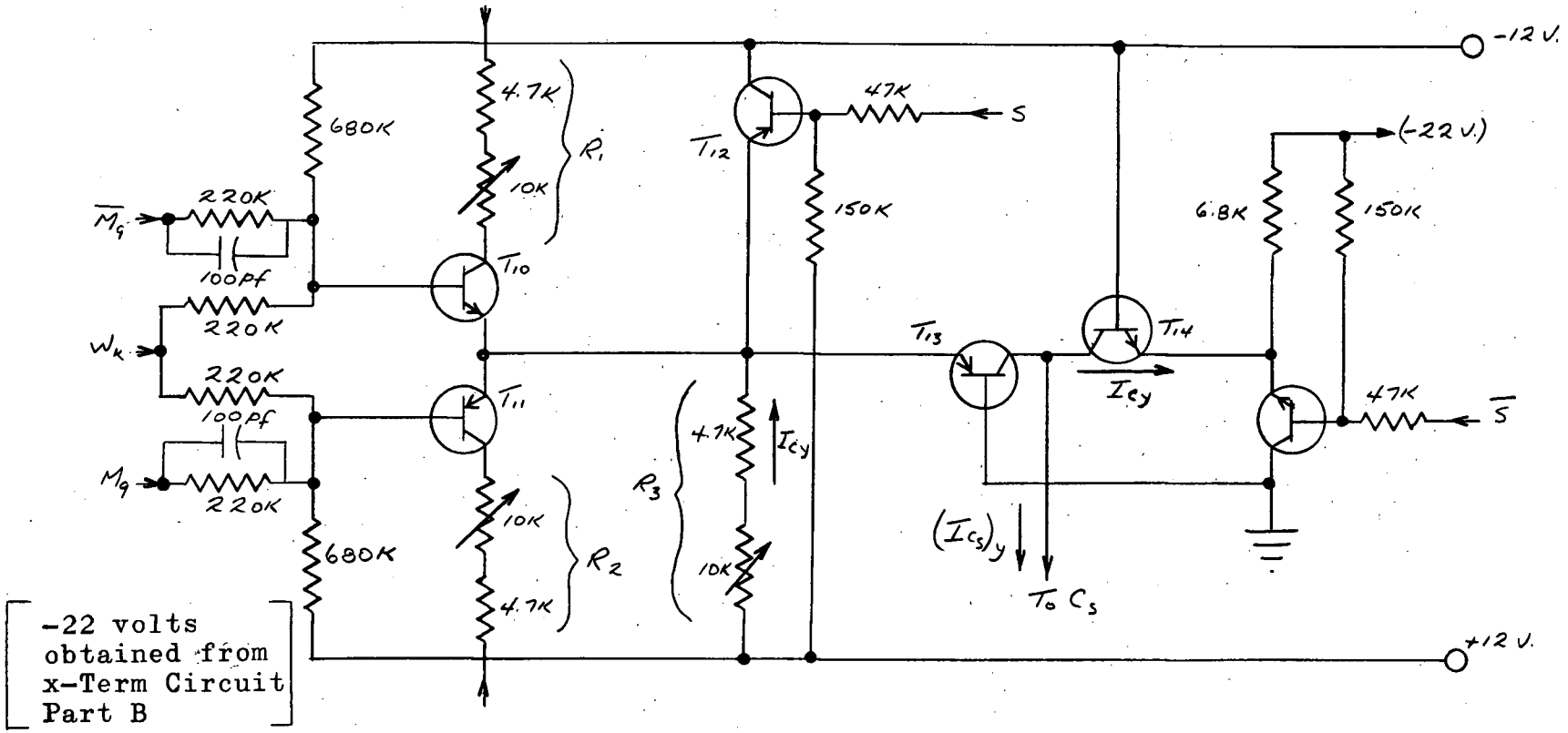
$$R_1 = R_2 \triangleq R_y \qquad \ldots(5\text{-}26)$$

The collectors of transistors T_{13} and T_{14} are connected to C_s, the summing capacitor. The base of T_{13} is grounded, and emitter current is supplied through R_3 from the +12 volt supply. The emitter of T_{13} is therefore very close to ground potential. The combined action of M_9, $\overline{M_9}$, and w_k saturates one of the transistors T_{10} or T_{11} for the duration of the m_9 period, reducing the collector-emitter voltage of this transistor to almost zero. The current through the transistor is therefore approximately

$$I_y = \frac{|y(t)|}{R_y} \qquad \ldots(5\text{-}27)$$

The current through T_{13} is therefore $I_{cy} \pm I_y$. R_3 is adjusted so that I_{cy} is equal to the constant current through T_{14} as shown. The net current $(I_{C_s})_y$ is therefore equal to $\pm I_y$. This causes a voltage change on C_s equal to

$$(\Delta V_{C_s})_y = \frac{\pm I_y \Delta}{C_s} \qquad \ldots(5\text{-}28)$$



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: T_{10}, T_{14}, T_{15} 2N1308

T_{11} 2N1309

T_{12}, T_{13} 2N1381

Figure 5-15. y-Term Circuit Part C.

where Δ is the width of the m_9 period. Combining Equations (5-27) and (5-28) yields

$$(\Delta V_{C_s})_y = \pm \left| \frac{y(t)}{R_y C_s} \right| \qquad \ldots(5\text{-}29)$$

Consideration of the gating actions of M_9, $\overline{M_9}$, and w_k shows that $(\Delta V_{C_s})_y$ is given by the following equation:

$$(\Delta V_{C_s})_y = \alpha\, y(t)\, v_k \qquad \ldots(5\text{-}30)$$

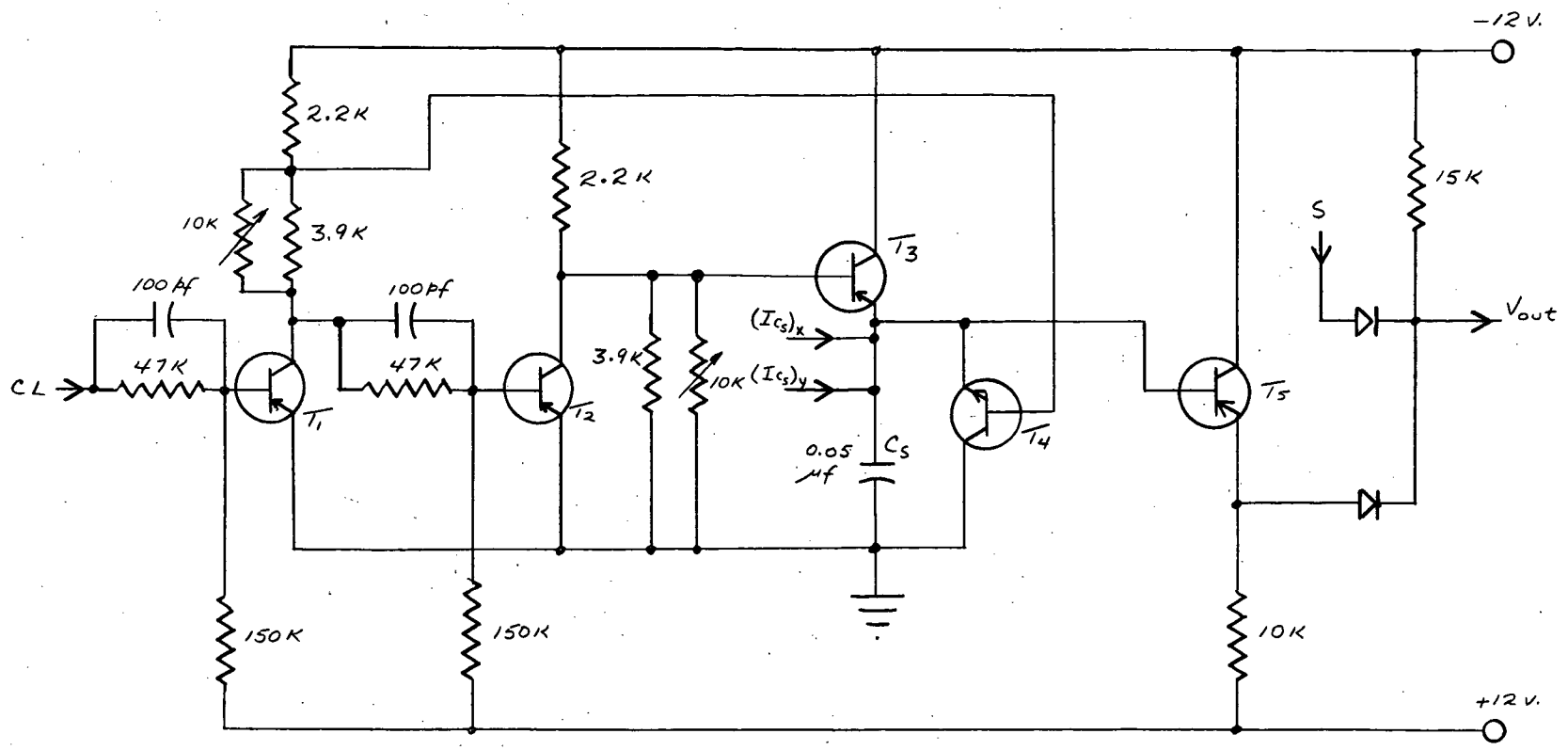
where

$$\alpha = \frac{\Delta}{R_y C_s} \qquad \ldots(5\text{-}31)$$

Transistors T_{12} and T_{15} are used to block $(I_{C_s})_y$ during the sample period S. The signals S and $\overline{S}$ are generated by circuits described in section 5-8. These signals, applied as shown in Figure 5-14, have the effect of cutting off T_{13} and T_{14}. This blocks $(I_{C_s})_y$.

5-7. The Capacitor Summing Circuit.

This circuit is shown in Figure 5-16. At the conclusion of each Sample interval, a clear pulse, CL, is applied as shown. This causes the voltage on the base of transistor T_3 to change from 0 volts to -6 volts and the voltage on the base of T_4 to change from -12 volts to -6 volts. The summing capacitor C_s is thus either charged or discharged, depending upon its previous voltage, to -6 volts. After the CL pulse has been



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: T_1, T_2 2N404

T_s 2N1381

T_3 2N1304

T_4 2N1305

Figure 5-16. Capacitor Summing Circuit.

removed, T_3 and T_4 are cut off. The currents $(I_{C_s})_x$ and $(I_{C_s})_y$ are then directed into or out of C_s, so that at the end of the computing period the voltage on C_s is given by

$$V_{C_s} = -6 + \alpha\, y(t)\, v_k - \sum_{m=0}^{n}{}' \beta\, x(t)\, v_{k,m}\, g_m \qquad \ldots(5\text{-}32)$$

If $\alpha = \beta$, it follows that

$$\begin{aligned} V_{C_s} &= -6 + \alpha\left[y(t)\, v_k - \sum_{m=0}^{n}{}' x(t)\, v_{k,m}\, g_m\right] \\ &= -6 + \alpha\, G_k \end{aligned} \qquad \ldots(5\text{-}33)$$

The Sample pulse blocks $(I_{C_s})_x$ and $(I_{C_s})_y$, and gates the signal V_{C_s} as shown, producing V_{out}.

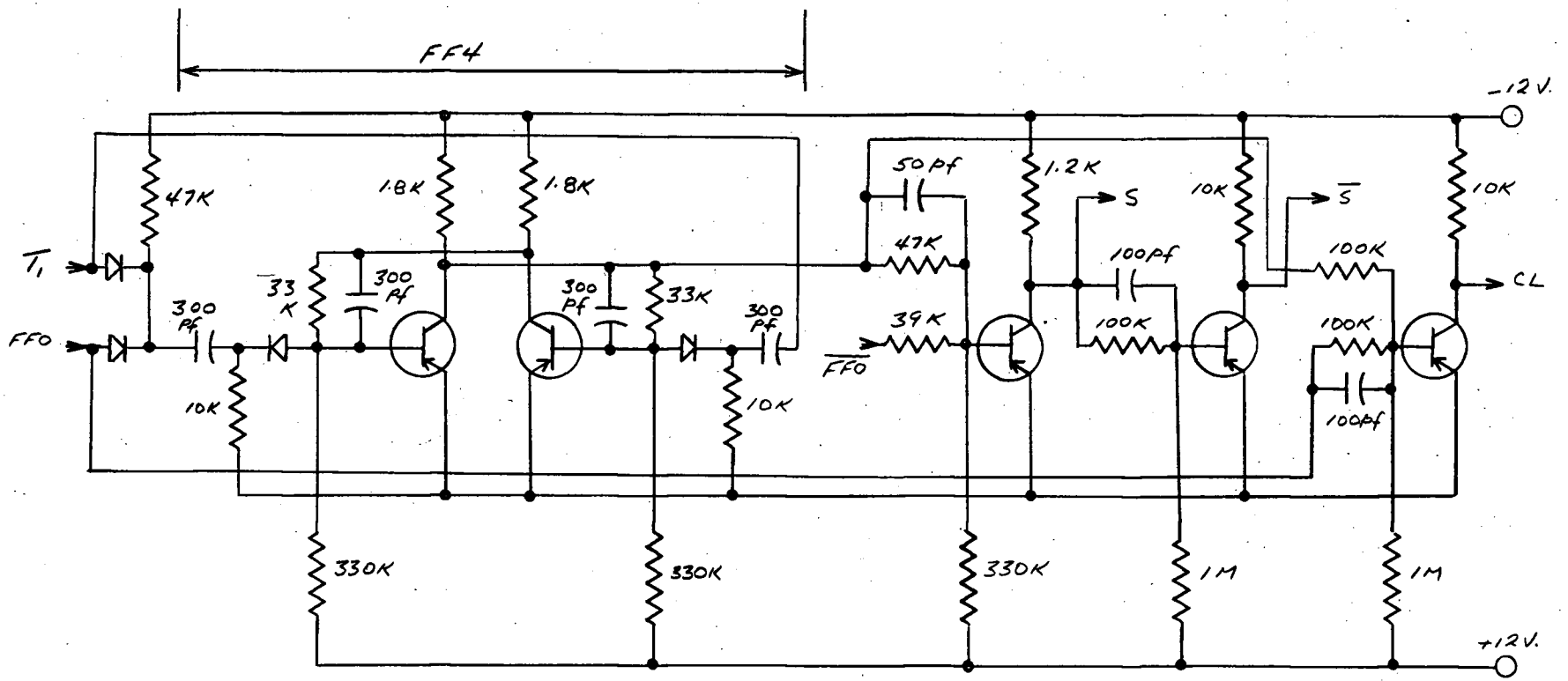
5-8. Sample and Clear Pulse Generator.

This circuit, shown in Figure 5-17, generates the pulses S, $\overline{S}$, and CL which are required in the preceding circuits.

FF4 is normally OFF. It is turned ON during the FFO pulse by the T_1 pulse, and turned OFF again by the next T_1 pulse. The output $\overline{FF4}$ is gated with $\overline{FFO}$ in a NOR gate to produce the Sample pulse S which is given by the logical equation

$$S = FFO.FF4 \qquad \ldots(5\text{-}34)$$

The NOR gate is followed by an inverter which produces $\overline{S}$. The signals FFO and $\overline{FF4}$ are combined in a second NOR gate to



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Transistors: 2N404

Diodes: 1N34A

Figure 5-17. Sample and Clear Pulse Generator.

produce the clear pulse CL, which is given by the logical equation

$$CL = \overline{FF0}.FF4 \qquad \ldots(5\text{-}35)$$

Figure 5-18 shows the waveforms.

5-9. Storage Circuit.

The storage circuit, including input and output gates, is shown in Figure 5-19. The sampled signal, V_{out}, from the Capacitor Summing Circuit is applied to an input bus in the Storage Circuit. This bus signal is then sampled by the k counter and the signal is applied through an emitter follower to the storage capacitor C_1, which has been cleared during the previous k period. The low-pass filter (R_2, C_2, R_3, C_3) smoothes the voltage so that the output (from C_3) is approximately constant over the complete iteration period* and is proportional to the time average of the input. The output signal is sampled by the m counter and is passed through a diode OR gate to the g-Pulse Generator.

5-10. The Reset Circuit.

This circuit provides a means of setting the various counters and flip-flops to their proper states after turning on the computer. It also permits resetting the computer if, for any reason, the proper time relationship between the various units is lost. The circuit is shown in Figure 5-20.

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*This is a sufficiently long period for the tests performed on the computer. For slowly varying system signals, x(t) and y(t), the filter must have a much larger time constant.

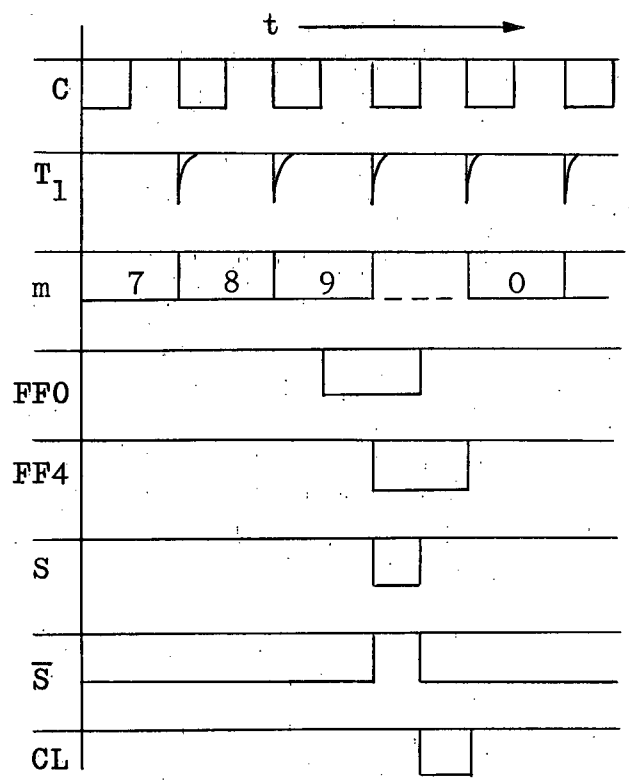
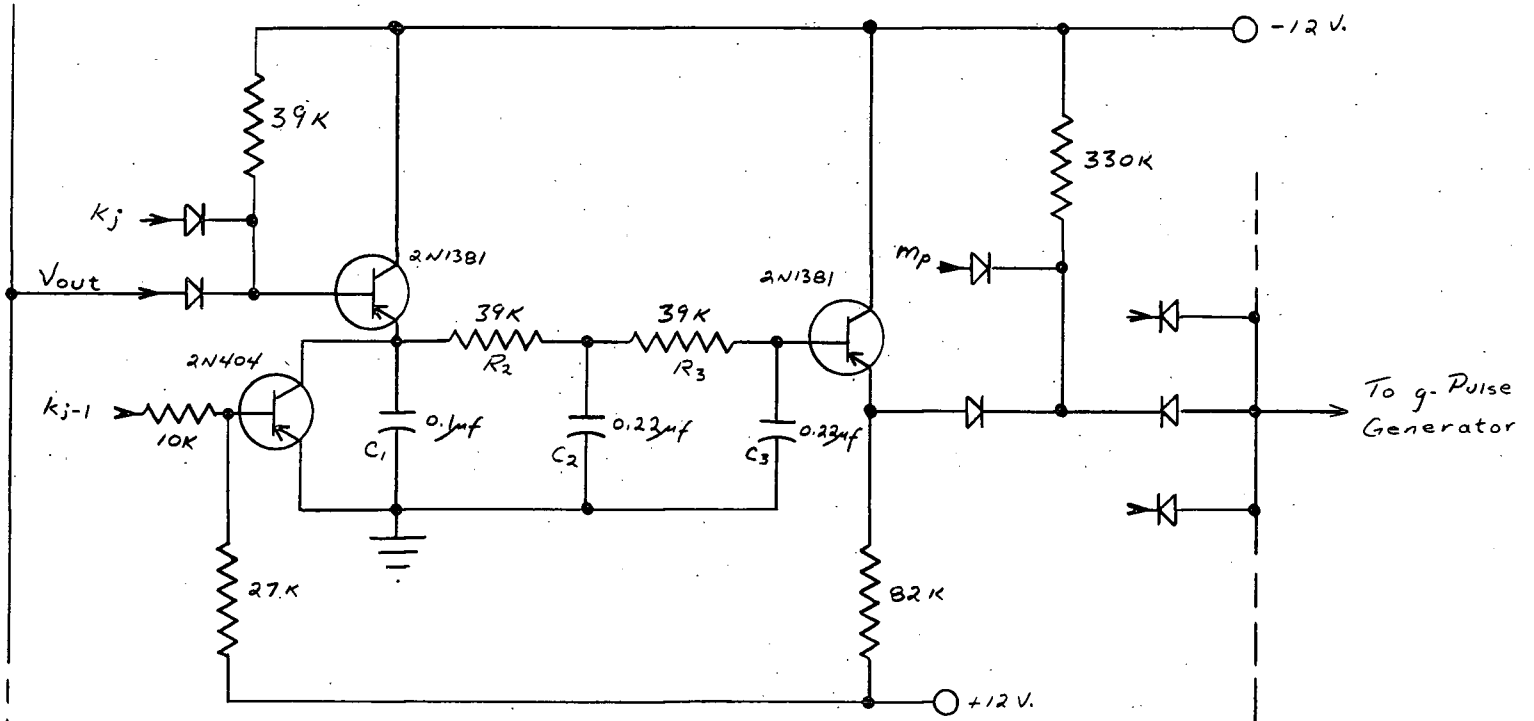


Figure 5-18. Sample and Clear Pulse Generator Waveforms.

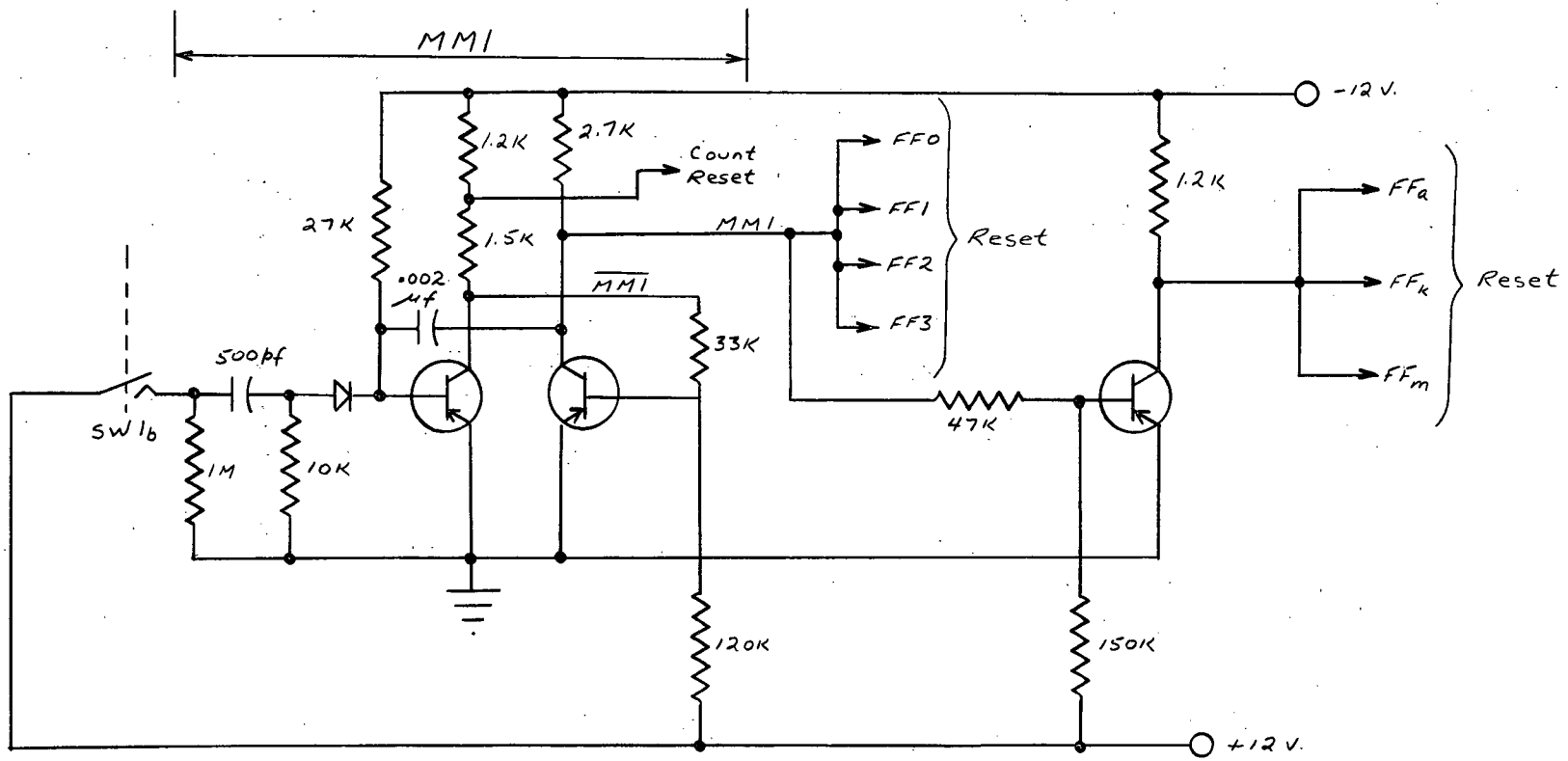


Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

Diodes: 1N497

Figure 5-19. Capacitor Storage and Averaging Circuit.



Resistors: $\frac{1}{2}$W, 10%

Capacitors: 75V, 10%

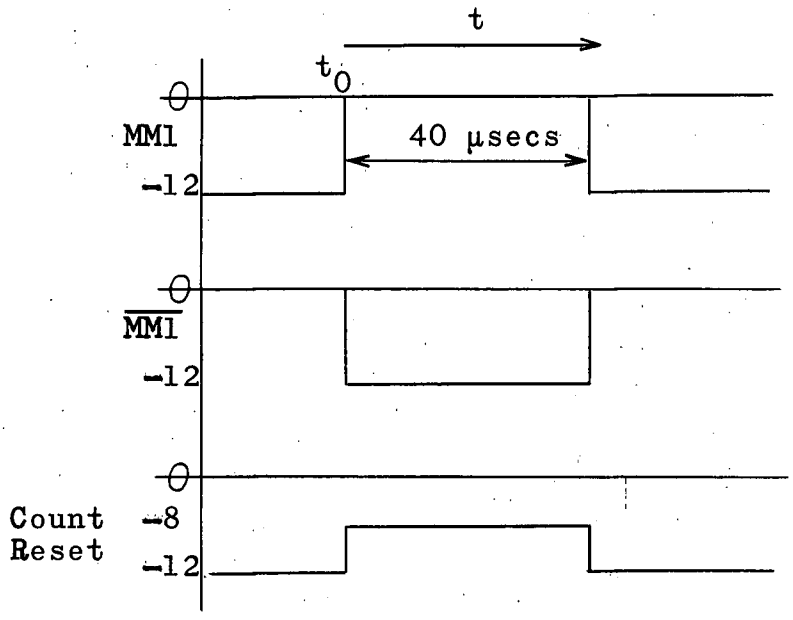
Transistors: 2N404

Diodes: 1N34A

Figure 5-20. Reset Circuit.

Depression of switch SW1 closes $SW1_b$, causing a positive trigger pulse to be applied to the monostable multivibrator MM1, turning it OFF. At the same time, the Clock Pulse Generator is blocked (by the action of $SW1_b$ - See Figure 4-1). The 40 μsec pulse from MM1 is applied to the Reset inputs of FF0, FF1, FF2, and FF3 (see Figure 4-5) and is also inverted and applied to the Reset inputs of FF_a, FF_k, and FF_m. (See Figure 4-4). The Count Reset Pulse is obtained from MM1 as shown, and is applied to the common Count Reset input of the a, k, and m counters. (See Figure 4-3). The waveforms are shown in Figure 5-21. The various circuits are reset by the trailing edges of the respective pulses.

This completes the description of the computer circuits. The performance of the computer in a simple test is described in the following chapter.



SW1 depressed at $t = t_0$

Figure 5-21. Reset Circuit Waveforms.

6. TEST RESULTS

This chapter describes a simple test of the computer's accuracy. A representative set of equations is solved using the computer and the solutions are compared with calculated values.

In Chapter 5 it was shown that the voltage on the summing capacitor at the conclusion of a k cycle should be

$$(V_{C_s})_k = -6 + \alpha\, y(t)\, v_k - \sum_{m=0}^{n}{}' \beta x(t)\, v_{k,m}\, g_m \qquad \ldots(5\text{-}32)$$

When the computer is being used to compute g_k, α must equal β, so that

$$(V_{C_s})_k = -6 + \alpha\, G_k \qquad \ldots(5\text{-}33)$$

For the purpose of the computational test, any scale factors may be chosen.

$$\text{Let } p_k \triangleq (V_{C_s})_k + 6 \qquad \ldots(6\text{-}1)$$

It follows from Equations (5-32) and (6-1) that

$$p_k = \alpha\, y(t)\, v_k - \sum_{m=0}^{n}{}' \lambda\, x(t)\, v_{k,m} P_m \qquad \ldots(6\text{-}2)$$
$$(k = 0, 1, \ldots, 8, 9, 0, 1, \ldots)$$

where P_m is the time average of p_m, and λ is a scale factor

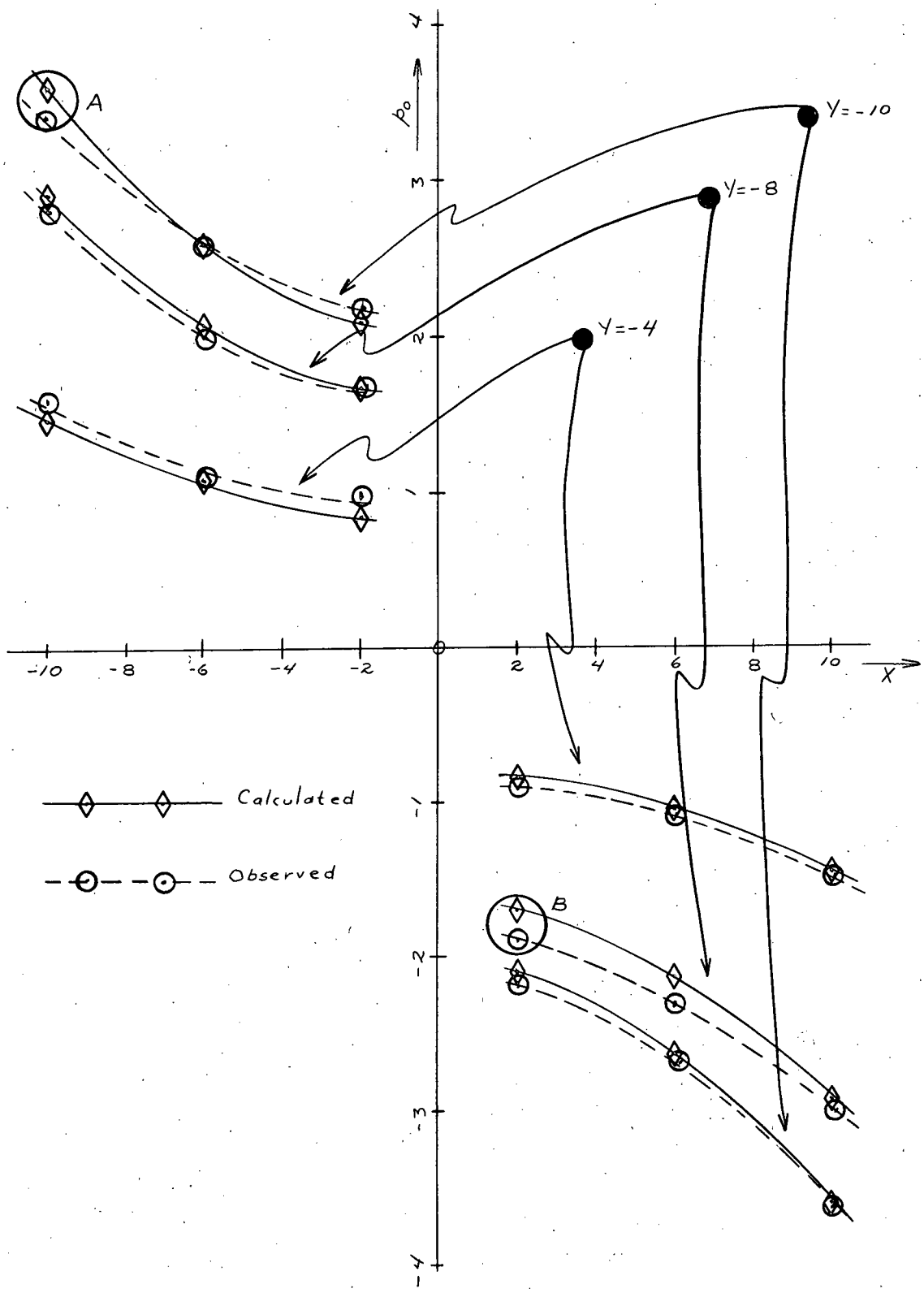


Figure 6-1. Results of Computer Test.

which includes the attenuation in the low-pass filter. The voltages x(t) and y(t) are selected as follows:

$$x(t) = X \text{ volts} \qquad \ldots(6\text{-}3)$$

$$y(t) = \begin{cases} Y \text{ volts}, & k = 0 \\ 0 \text{ volts}, & k \neq 0 \end{cases} \qquad \ldots(6\text{-}4)$$

where X and Y are constants. Note that y(t) can be obtained from pin 0 of the k counter. From Equations (6-2), (6-3), and (6-4), it follows that

$$P_m = p_m \ (m = 0, 1, \ldots 8, 9) \qquad \ldots(6\text{-}5)$$

The computer can therefore solve the following system of equations for $p_0, p_1, \ldots, p_9$:

$$\begin{aligned}
p_0 + \lambda|x|\, p_1 + \lambda|x|\, p_2 + \ldots + \lambda|x|\, p_9 &= \alpha Y \operatorname{sgn} X \\
\lambda|x|\, p_0 + p_1 + \lambda|x|\, p_2 + \ldots + \lambda|x|\, p_9 &= 0 \\
&\vdots \\
\lambda|x|\, p_0 + \lambda|x|\, p_1 + \ldots + p_k + \ldots + \lambda|x|\, p_9 &= 0 \\
&\vdots \\
\lambda|x|\, p_0 + \ldots\ldots\ldots\ldots\ldots\ldots + p_9 &= 0
\end{aligned} \qquad \ldots(6\text{-}6)$$

It can easily be shown that the solution to Equations (6-6) is

$$p_0 = \alpha\, Y\, \text{sgn}\, X \left[1 + \frac{9(\lambda X)^2}{(1+9\lambda|X|)(1-\lambda|X|)} \right] \qquad \ldots(6\text{-}7a)$$

$$p_1 = p_2 = \ldots = p_9 = \frac{-(\alpha\lambda)\, YX}{(1+9\lambda|X|)(1-\lambda|X|)} \qquad \ldots(6\text{-}7b)$$

Computer solutions to Equations (6-6) were obtained for the following conditions:

$$\lambda = 0.2$$
$$\beta = 0.05 \text{ volts}^{-1}$$
$$X = 10, 6, 2, -2, -6, -10 \text{ volts}$$
$$Y = -10, -8, -4 \text{ volts}. \qquad \ldots(6\text{-}8)$$

In Figure 6-1 the solutions for p_0 are compared with the corresponding values of p_0 as calculated from Equation (6-7a).

The maximum discrepancy between observed values and calculated values is approximately 0.2 volts, as found at points A and B in Figure 6-1. This represents an error of less than 6 per cent of full scale.

These results are quite encouraging, and it is felt that the accuracy could be considerably increased by using different storage facilities in place of the capacitor storage units. Recommendations as to such changes are discussed in Chapter 7.

Provision for performing the test described above could easily be built into the computer for the purpose of maintenance and adjustment. The results could be compared with

an acceptable standard to give an indication of the calibration of the computer.

Two additional tests were performed on the computer.

In the first of these tests, the input signals to the computer, $x(t)$ and $y(t)$, were chosen as follows:

$$x(t) = a \sin \omega t$$
$$y(t) = b \sin (\omega t - \beta) \qquad \ldots(6\text{-}9)$$

Bohn[6] has shown that the solution for the impulse response in this case must be

$$h(t) = \frac{b}{a} \delta\left(t - \frac{\beta}{\omega}\right) \qquad \ldots(6\text{-}10)$$

Observations of the computer solution for g_k indicated a peak which changed position as β/ω was varied. This agreed qualitatively with what was expected.

In the second test, a random signal was fed to a simple RC circuit, and the input and output signals were fed to the computer. The computer solution should then have indicated the step response of the test circuit. However, the capacitor storage proved inadequate for proper averaging of the signals, and no meaningful results were obtained.

7. CONCLUSIONS

The design of a relatively simple analogue computer for use in the real-time estimation of system dynamics has been described. Test results have indicated that the obtainable accuracy is sufficient for system design purposes.

However, a more suitable method of time averaging and storage is required before the computer can be used to full advantage. In a satisfactory arrangement the attenuation factors and time constants of the individual storage and time averaging circuits should be uniform. Also, modification of the time constants should not affect the attenuation factors. In the present capacitor-storage and low-pass filter circuits it is very difficult to match the attenuation factors and time constants unless precision components are used. Also, very large filter capacitances would be required for averaging signals over a period of several seconds.

A magnetic drum could be used for the storage and time averaging. Small drums, designed specifically for data processing, are now available at reasonable prices. A method for storing analogue information on a magnetic drum using a pulse position code has been described[10]. The following discussion indicates how a modified computer using this code could solve for g_k (where g_k is as defined in Chapter 2).

Let

$$\varepsilon_k(t) = y(t)\, v(t-\tau_k) - \sum_{m=0}^{n} x(t)\, v(t-|\tau_k-u_m|)\, f_m \qquad \ldots(7\text{-}1)$$

Now let

$$\frac{df_k}{dt} = K\,\varepsilon_k(t) \qquad \ldots(7\text{-}2)$$

If $f_k(t)$ is finite, it follows that

$$\begin{aligned}\overline{\varepsilon_k(t)} &= \lim_{T\to\infty} \frac{1}{T}\int_0^T \varepsilon_k(t)dt \\ &= \lim_{T\to\infty} \frac{1}{Kt}\int_0^T df_k \\ &= 0 \end{aligned} \qquad \ldots(7\text{-}3)$$

Therefore,

$$y(t)\; v(t-\tau_k) - \sum_{m=0}^{n} x(t)\; v(t-|\tau_k-u_m|)\; f_m = 0 \qquad \ldots(7\text{-}4)$$

Equation (7-4) is identical to Equation (2-11) except that g_m has been replaced by f_m.

Therefore,

$$\lim_{T\to\infty} f_m = g_m \qquad \ldots(7\text{-}5)$$

It is evident that the solution of Equations (7-1) and (7-2) results in the generation of g_m $(m= 0,1,\ldots,n)$. The computation of $\varepsilon_k(t)$ as given by Equation (7-1) could be done

using the computer circuits described in this thesis. Note that there is no prime after the summation sign in Equation (7-1). This would permit simplification of the computer circuits in that the diagonal term where k = m need no longer be blocked. The solution of Equation (7-2) can be achieved as shown in Figure 7-1. The quantities Δf_k and f_k are stored on separate tracks of the drum using the pulse position representation mentioned above. The contents of the coarse scale are used for the computation of each $\varepsilon_k(t)$. This quantity is stored in the counter, and is used to change the position of the Δf_k pulse to correspond to the new increment as shown. A carry obtained from the counter is used to shift the f_k pulse forward or backward. It follows that

$$\Delta f_k \approx K \varepsilon_k(t)\ \Delta t \qquad \ldots(7\text{-}6)$$

The following code is the most convenient for storing the information on the drum:

Suppose x is the quantity to be stored. Let z, the computer representation of x, be defined as follows:

$$z = \begin{cases} x, & x \geqq 0 \\ 2+x, & x < 0 \end{cases} \qquad \ldots(7\text{-}7)$$

where x is scaled so that $|x|<1$. If $x<0$, set

$$z = 1 + y \qquad \ldots(7\text{-}8)$$

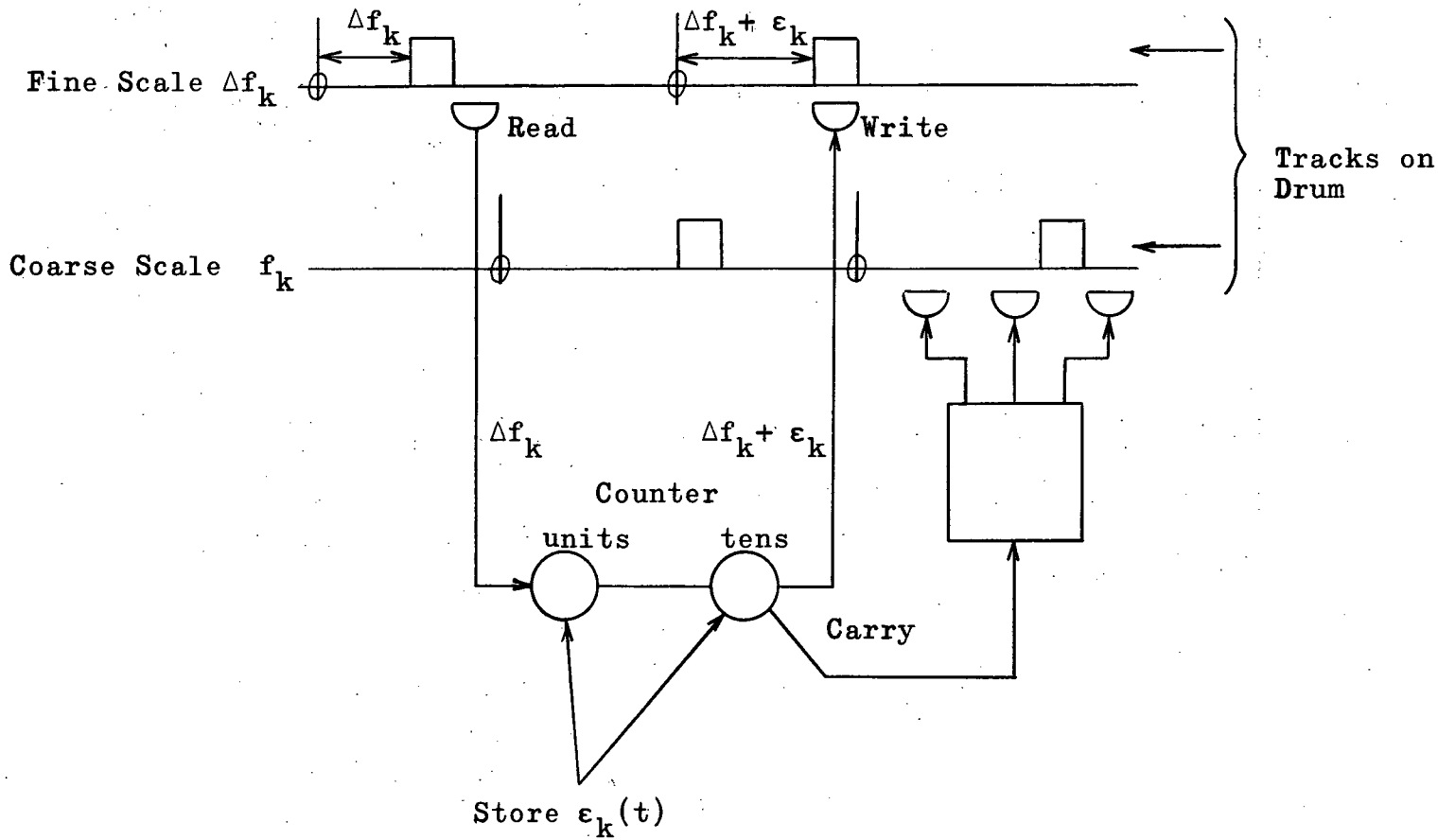


Figure 7-1. Magnetic Drum Storage of ε_k.

where the 1 represents a sign pulse and y represents the quantity which appears in coded form in the various counters and on the drum. Therefore,

$$y = 1 + x \qquad \ldots(7\text{-}9)$$

Since $-1 < x < 0$, it follows that $0 < y < 1$. The contents of the counters and the drum will represent y, where

$$y = \begin{cases} x, & x \geqq 0 \\ 1+x, & x < 0 \end{cases} \qquad \ldots(7\text{-}10)$$

and the sign of x is indicated by a separate sign pulse. This code could easily be used with the circuits suggested in Figure 7-1.

There are several important advantages in the use of a magnetic drum as described:

1. The storage is permanent.
2. The averaging time-constant can be modified simply by changing the scaling factor of the fine scale.
3. The computing circuitry is simplified.

It is believed that modification of the present computer to include a magnetic drum storage as described would greatly enhance the accuracy and flexibility of the computer.

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