A SELF-FRAMING PCM SYSTEM

by

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ABSTRACT

A single channel pulse code modulation (PCM) speech communication system is described using a binary code with seven digits per code group and a sampling rate of 8000 per second.

A unique feature of the system is the pulse group synchronization or framing scheme that is employed to co-ordinate the operations of the coder and the decoder. A method is outlined wherein the system is able to establish correct framing without the use of auxiliary framing digits. The framing information is inherent in the coded signals.

The coder operates on the circulating pulse principle and is a modified version of a coder previously described by Hafer. The decoder is basically one of the pulse count type. The received code pulses produce binary amounts of charge which are stored as voltages on a capacitor. The voltage on the capacitor after one cycle of decoder operation is proportional to the amplitude of the original sample taken at the coder.

Test results indicate that the performance is adequate for good quality reproduction of speech. The group synchronization scheme performed perfectly and correct framing was achieved in times so short that misframing noise was inaudible.

The proposed framing scheme is adaptable to small PCM speech systems where simplicity in the instrumentation and economy in the use of the digits are important.

ACKNOWLEDGEMENT

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1. INTRODUCTION

Communication by pulse code modulation (PCM) methods is well known and is described extensively in the literature[1,2,3]. PCM uses binary pulses, and hence, the system needs to sense only the presence or absence of the pulses and ignores the shape and exact timing of the pulses. The use of binary pulses greatly reduces the system's sensitivity to noise, distortion and crosstalk, the signal power requirements, and simplifies the design of the repeaters. Furthermore, since binary coded signals can be regenerated at each repeater, it is only necessary that a repeater be designed to handle the link from one repeater to the next, whereas in analog systems, since noise and distortion are cumulative, each repeater must be designed to requirements better than the requirements of the entire system. It is this concept of regenerative repeatering that makes PCM so desirable for long-haul communication systems. The penalty that must be paid for this feature is the increased channel bandwidth and increased complexity of the terminal equipment.

A typical PCM system is illustrated in Figure 1. The input signal, after filtering, is sampled at frequent intervals by the sampler. The quantizer reduces the sampled amplitude values to one of many discrete values and each quantized sample is then coded into a binary code, according to its amplitude.

```
  MESSAGE
  SIGNAL
     │
     ▼
┌──────────┐
│ LOW PASS │
│  FILTER  │
└──────────┘
     │
     ▼
┌──────────┐   ┌──────────┐              ┌──────────┐   MESSAGE
│ SAMPLER  │   │  TIMING  │              │ RETIMING │   SIGNAL
└──────────┘   │ CIRCUIT  │              │ CIRCUIT  │      ▲
     │         └──────────┘              └──────────┘      │
     ▼              │                         │      ┌──────────┐
┌──────────┐   ┌──────────┐    ┌──────────┐ ┌──────────┐│ LOW PASS │
│QUANTIZER │──▶│  CODER   │───▶│ DECODER  │ │ FILTER   │
└──────────┘   └──────────┘    └──────────┘ └──────────┘
  ◀── MODULATOR ──▶  TRANSMISSION  ◀── DEMODULATOR ──▶
                      CHANNEL
```
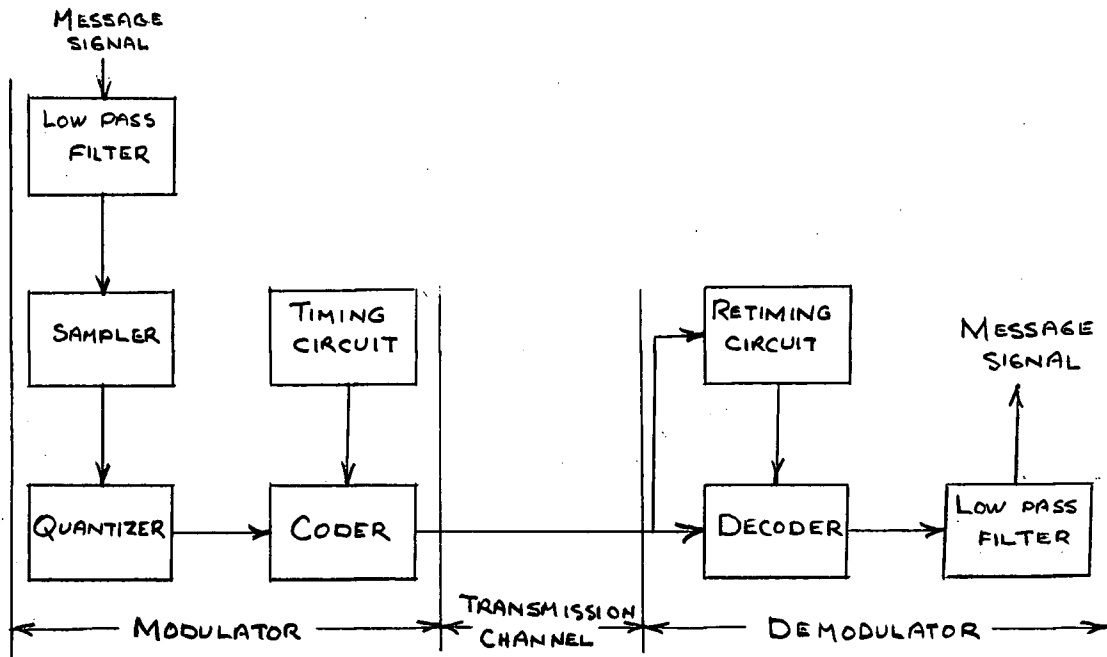
Figure 1.1 A Typical PCM System

The decoder reverses the operation of the coder. Its function
is to reconstruct the amplitude sample presented to the coder
by the quantizer. The reconstructed speech waveform is then
obtained by filtering.

It is apparent that a small error results from the fact
that the sample amplitude that is actually coded by the coder is
not exactly the amplitude of the speech waveform at the instant
of sampling. This is the so-called quantization error. It can
be reduced by increasing the number of discrete values or levels
used by the system.

Many methods have been developed to code analog signals
into PCM signals and, the reverse operation, to decode the coded
signals back into analog signals. Perhaps the most straight-
forward method of coding is the pulse count method as described

by Black and Edson[4] and by Armstrong[5]. This method is of medium speed but is inherently awkward because of the number of operations necessary and because of the fact that the output code is in parallel form and must be converted into serial form to be compatible with standard transmission methods. A second method of coding makes use of electron beam coding tubes. PCM systems embodying coding tubes are described by Sears[6] and by Meacham and Peterson[7]. This method of coding is very fast but the tube requires considerable power, space and maintenance and these drawbacks make it unsuitable with transistorized equipment. A third method involves the use of feedback. Smith[8] describes the principle of the use of feedback in PCM coders and an experimental system using feedback is described by Goodall[2]. A novel approach to coding using feedback methods is described by Fedida[9]. He makes use of the principle of circulating pulses and describes a coder using tubes. A similar coder using transistors is described by Hafer[10]. This method is also of medium speed but, in spite of its apparent simplicity, is probably the most difficult method to instrument. With the exception of the method using beam coding tubes, analogous decoders using the methods described have been constructed. An unsuccessful attempt to construct a decoder using the circulating pulse principle is described by Chang[11].

In PCM, as in other pulse modulation schemes, some means of coordinating the operations of the coder and decoder must be provided. This is the function of the synchronization scheme.

The timing circuit at the coder transmits the synchronizing information which is then detected by the retiming circuit at the decoder.

The synchronization scheme must accomplish two things. First, it must make known to the decoder the phase of the basic pulse repetition frequency. This is the pulse timing problem. Second, it must impart information regarding the pulse group timing. This operation is called "framing", or group synchronization. The framing scheme enables the decoder to select, out of a long train of uniformly spaced pulses and spaces, the correct groups of pulses and spaces that represent the sample amplitudes originally coded at the coder. The framing information must be sent at frequent intervals so that any temporary break in transmission will not adversely affect the operation of the system.

Pulse retiming is easily accomplished since the required information is inherent in the transmitted pulses. The decoder needs only to detect the time of arrival of the pulses. The leading edges of the pulses are then used to pull a local oscillator or ringing circuit into phase.

Perhaps the most obvious way of establishing pulse group synchronization would be to use a separate transmission channel for the framing information. But this method is very wasteful, especially if the overall system utilizes only a few message channels. A better method would be to sacrifice the use of one or more digits in a code group or even an entire code group at frequent intervals to carry the framing information. The use of

parity checks falls into this category. This method, although more ecomonical than the first, is still unsatisfactory for small systems with three message channels or less. The third and most economical means of achieving continuous synchronization involves the use of self-synchronizing codes. These are codes in which the synchronizing information is an inherent feature, and hence, a minimum of information is sacrificed by the transmission channel. Stiffler[12] cites the use of such codes.

Ideally, it would be desirable to transmit the synchronizing information without sacrificing any of the information capacity of the system. Obviously, this is impossible. Therefore, the problem is to determine the most efficient means of transmitting the synchronizing information. If the system is designed to transmit data at a high information rate, with very little redundancy in the messages, synchronization by means of self-synchronizing codes becomes a very serious problem. However, in the case of speech signals, which are highly redundant in the information theory sense, self-synchronization is a less serious problem and may be achieved by relatively simple methods.

This thesis presents a simple solution to some of the problems encountered in the transmission of speech signals by PCM. The first phase of the project was the design and construction of a 7 digit decoder, employing capacitor storage. It is basically one of the pulse count type. The second phase was the development of a group synchronization or framing scheme utilizing the amplitude-frequency characteristic of speech as its basis. The final phase was the modification of the PCM coder built by Hafer[10] so that it was compatible with the

decoder. The entire PCM system, incorporating the modified coder, the decoder, and the group synchronization scheme developed in this thesis, was then tested.

2. SOME THEORETICAL CONSIDERATIONS

This chapter outlines a few of the basic theoretical aspects of PCM and provides background material for subsequent chapters.

2.1 The Sampling Principle

Nyquist[13] has demonstrated that if a signal of bandwidth W_0 is sampled at a rate $2W_0$ or greater, the samples will contain all the information in that signal. This principle is illustrated in all systems that employ sampling methods. PCM is one such system.

2.2 Bandwidth Requirements

Nyquist[13] has also shown that in order to transmit W independent pulses per second, the transmission channel must have a bandwidth of at least $W/2$. This condition establishes the minimum bandwidth for the transmission of pulses with no intersymbol interference. (Intersymbol interference is defined as the interference of one pulse due to the transient energy of previous pulses). However, it is possible to transmit pulses at the same rate over a channel of lesser bandwidth provided that intersymbol interference can be tolerated by the system and that the signal power is increased sufficiently to override the noise, for it is apparent that as the bandwidth

is reduced, there is greater and greater intersymbol inter-
ference and difficulty in recognizing the digits.

However, in the design of pulse systems it is usual to
avoid intersymbol interference and transmit W pulses per second
over a channel of bandwidth W/2 cps or greater.

Hence, a PCM system to transmit messages of maximum
frequency W_0 using n digits to code one sample, would require a
bandwidth of $W = \dfrac{n(2W_0)}{2} = nW_0$. In other words, the bandwidth
required is n times the bandwidth for direct transmission.

2.3 Signal Power Requirements

The signal power for adequate PCM transmission need only
be such that the decoder can distinguish the pulses from spaces
in the presence of channel noise with reasonable accuracy.
Hence, it is only necessary to set the pulse height slightly
higher than twice the height of the peak noise expected over a
reasonable period and to set the decoder pulse distinguishing
level at one-half the pulse height. This requirement then
establishes the threshold signal power. This threshold power is
very low—a signal-to-noise ratio of 20 db is more than adequate—
—whereas for comparable AM transmission a much higher signal-
to-noise ratio is required. Given this signal power, the
quality of the transmitted signal is then limited almost
entirely by noise produced in the encoding process.

2.4 Noise in a PCM System

A PCM system suffers from one type of distortion or

error which can not be reduced merely by increasing the signal power. This is called quantization noise. It results from the fact that there is a difference between the amplitude of the true signal and that actually encoded. This difference appears at the receiver, after decoding, as a random noise very similar to white noise.

The amplitude of this noise varies at random between 0 and 1/2 of a quantizing step. The r.m.s. amplitude, A_n, of the quantization noise of an n-digit system is then given by $A_n = \frac{1}{\sqrt{3}} \cdot \frac{1}{2} \cdot \frac{A_0}{2^n} = \frac{A_0}{\sqrt{3} \cdot 2^{n+1}}$ where A_0 is the maximum range of input signals, in volts.[1] The total quantization noise power, in watts, at any point in the system will be proportional to A_n^2, and may be taken as

$$N_0 = A_n^2 = A_0^2/3 \times 2^{2(n+1)}$$

2.5 Information Capacity

The information capacity of an ideal channel, limited in bandwidth to W, is given by Shannon[14] as

$$C = W \log_2 (1 + S/N) \text{ bits per second,}$$

where S is the average signal power and N the average noise power.

Signals with information content greater than this can not be transmitted through such a channel without error. Thus

for a channel of bandwidth $W = nW_0$ and $S/N = 100$ ($= 20$ db), the upper bound to the information rate that can be transmitted is $C = 6.7 \ nW_0$ bits/sec.

When such a channel is used to send binary pulses, as in PCM, we commonly transmit $2nW_0$ pulses per second, and therefore only $2nW_0$ bits per second. It is thus obvious that there is a great waste in information capacity when a virtually error-free binary channel is fitted into a noisy analog transmission medium. From the point of view of information theory, it would be more efficient to use much smaller S/N ratios, accept a reasonable number of errors in the received binary pulses, and take steps to correct these later. However, the equipment required for this is usually too complicated.

Once it has been decided to use a binary channel in order to transmit information, there arises the secondary problem of how to use its own limited information capacity of $2nW_0$ bits per second to the best advantage. Much work has been done in trying to economize on the number of bits required to transmit speech, music and television signals. This thesis is in part concerned with the same problem.

A few of the basic theorems in information theory and their application to PCM systems have been described. The ideas presented in this chapter are applied in subsequent chapters, - in the evaluation of the proposed framing scheme and in the design of the system.

3. A PROPOSAL FOR GROUP SYNCHRONIZATION FOR A PCM SPEECH SYSTEM

3.1 Requirements of a Synchronization Scheme

As stated previously, the synchronization scheme for PCM must establish and maintain the basic pulse repetition frequency and the pulse group timing in the decoder. The first requirement is easily accomplished by having the incoming pulses to the decoder pull a local clock into synchronism. This local clock may be either a ringing circuit that is shock excited into its proper phase or an oscillator that is pulled into its proper phase. In either case, the frequency of oscillation is closely related to the frequency of the master clock in the coder. The main problem in the design of bit timing synchronization schemes, especially in fast systems with high pulse rates, is that the local clock must be fast starting and yet quite insensitive to interference. Also it must continue to operate in the face of temporary breaks in transmission or relatively long periods of time between digits.

The second requirement, that the synchronization scheme must establish and maintain the proper pulse group timing, is more difficult to attain. If it were possible for the decoder to start up immediately upon receiving the pulses as they were transmitted from the coder, group synchronization would not be a serious problem, but invariably, the decoder circuit is slow in starting or the transmission channel acts upon the pulses in some way to cause errors in the transmitted signal and the

decoder is not able to correctly establish the group timing.

Now, one would like to fulfil the above requirements in the most efficient manner possible. An efficient method would sacrifice a minimum of the information capacity of the system for carrying the synchronization information. It is relatively easy to devise a method that utilizes one digit per code group for group synchronizing purposes. It was thought that a more economical scheme could be found that would require less than one digit per code group for successful operation.

3.2 A Proposal for Group Synchronization

The proposed group synchronization or framing scheme is the following. The input speech voltage waveform is restricted so that it does not vary in amplitude between any two successive sampling instants by more than one-half the maximum amplitude range that can be handled by the system. The resulting input signal is then coded and transmitted to the demodulator where it is decoded. If, after the decoding operation, the difference in amplitude between two successive reconstructed samples is greater than one-half the maximum amplitude range of the system, the decoder detects that it is operating upon the incorrect group of pulses. The decoding operation then shifts to a group one digit removed from the previous group and the process is repeated. Eventually, after a minimum of one or a maximum of n-1 such shifting operations, where n is the number of digits per code group, the decoder will find the correct group sequence

and will continue to operate on this sequence until transmission
is interrupted.

The restriction that is placed on the system, then, is
that the input signal to the sampler shall not vary in
amplitude by more than $A_0/2$ between any two successive sampling
periods, where A_0 is the maximum signal amplitude allowable.
A plot of the allowable input signal amplitude, A_m, versus
frequency can be then derived* and is illustrated in Figure 3.1.

3.3 Evaluation of the Proposal

In order to investigate the effect of the restriction
on the signals to be transmitted it is necessary to consider
the amplitude and frequency characteristics of speech. In the
loudest periods, most of the speech power is normally con-
centrated near a single frequency component, though this
frequency varies with time. The peak sound pressures, and
therefore the peak voltages, depend upon the frequencies in
use. Figure 3.2 shows a typical histogram giving the peak
amplitudes, A_s, in various frequency ranges which are only
rarely exceeded (in 1% of all 1/8-second intervals).

A PCM system designed so that it does not overload at
low frequencies will never experience high-frequency components
anywhere near overload. A comparison of Figures 3.1 and 3.2
shows that even the new restrictions, A_m, imposed on the high
frequencies by the proposed framing system are not normally

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* See Appendix 1 for derivation.
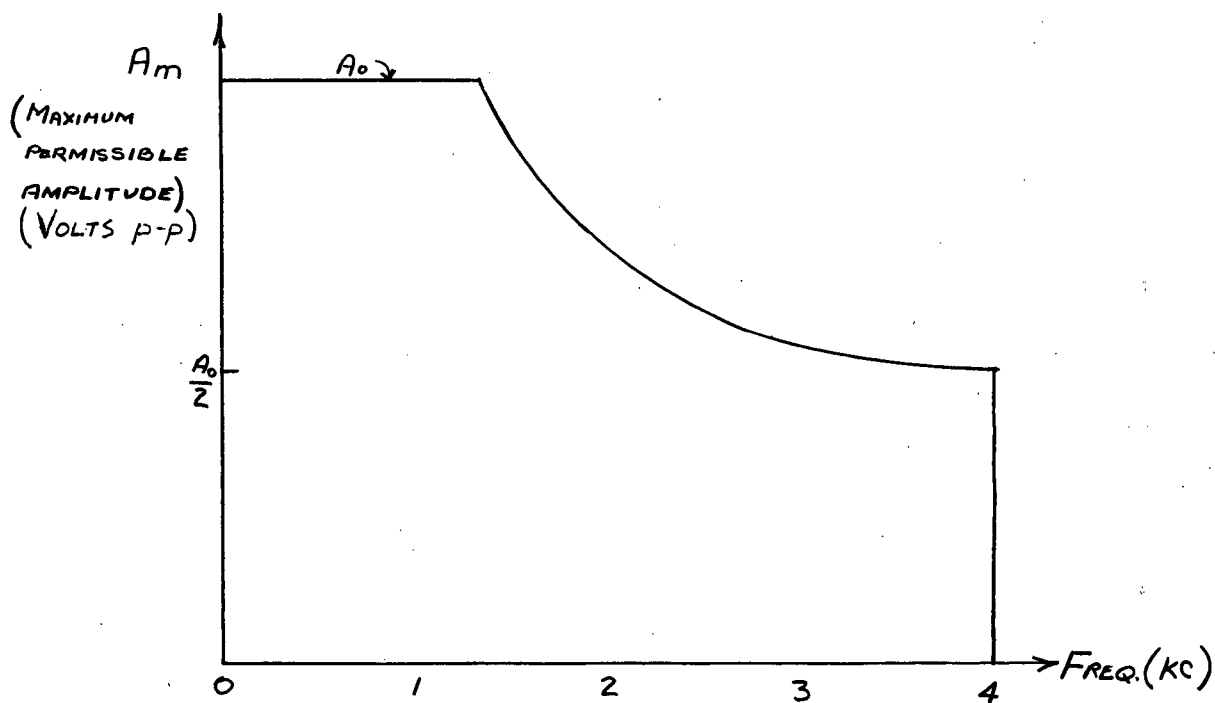
Figure 3.1 Amplitude Versus Frequency Characteristic of
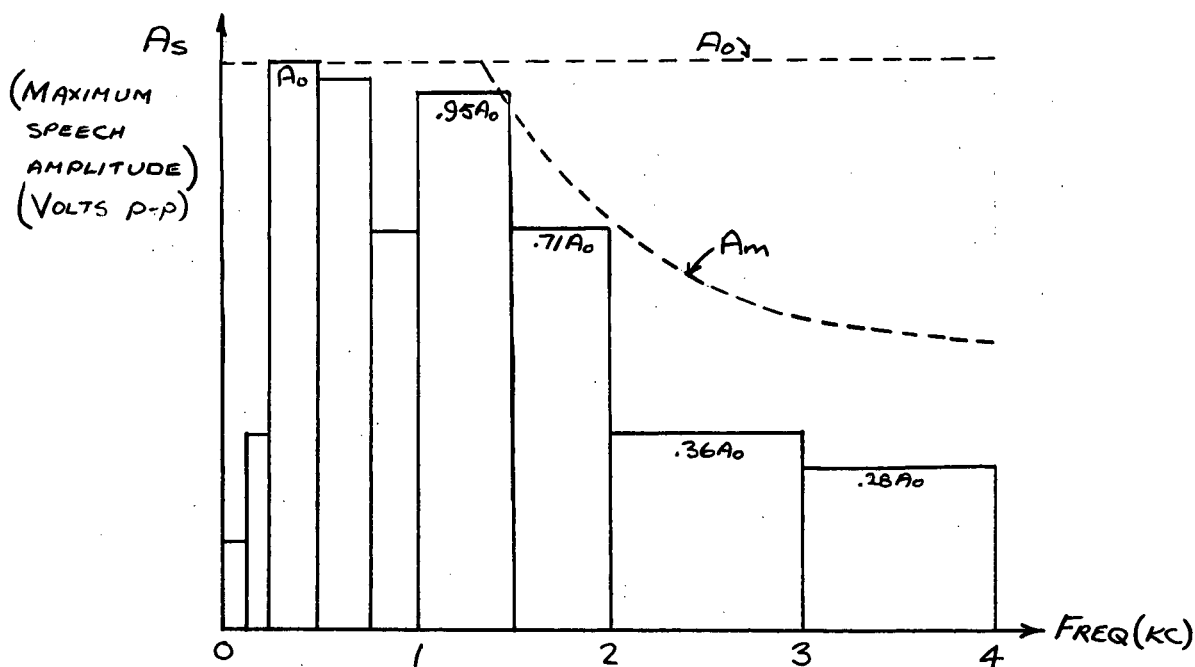Input Signals for Operation of PCM Framing Circuit

Figure 3.2 Maximum Sound Pressures in Various Frequency Bands
for 1/8 Second Intervals of Conversational Speech
(Mean of Composite Voices). Adapted From Reference
15. (Vertical scale adjusted so that low frequen-
cies just overload a PCM system with amplitude
range A_0)

violated by speech signals. Thus it seems that framing has been gained and no information capacity lost.

However, for a true evaluation of the proposal, the following must be considered. Suppose that pre-emphasis is used in the system. This is a method that is often used in speech systems to reduce noise that arises within the system. For example, consider any speech transmission system that uses pre-emphasis. The situation is illustrated in Figure 3.3. Speech normally has an amplitude-frequency characteristic as shown in
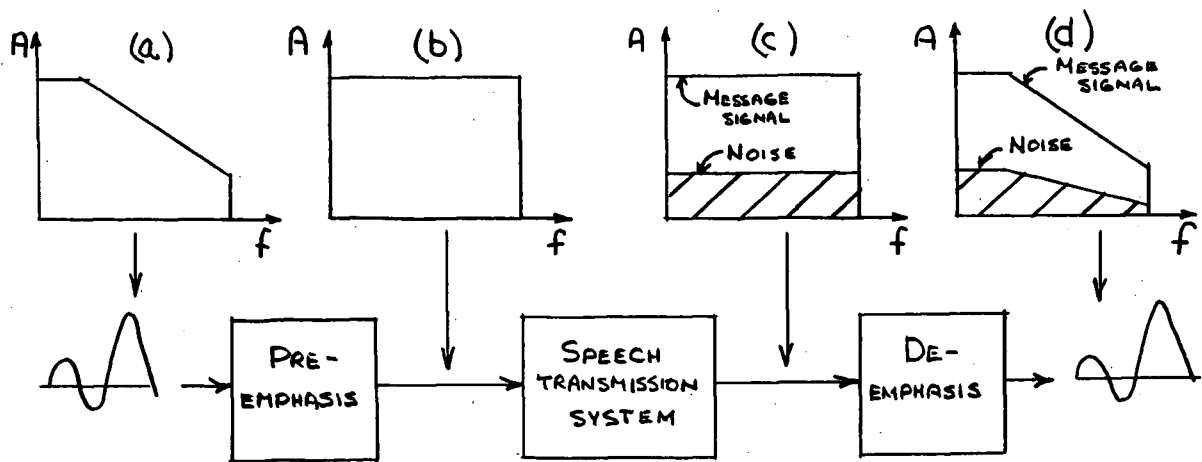
Figure 3.3 Effect of Pre-emphasis on the Amplitude Versus Frequency Characteristic of Speech

(a). The pre-emphasis circuit exaggerates the amplitudes of the higher frequencies in speech so that the resulting amplitude-frequency characteristic is as shown in (b). The speech transmission system acts upon the speech signals in the usual manner. After transmission and demodulation, the speech signals are equalized by the de-emphasis circuit in exactly the inverse manner to the pre-emphasis circuit. The resulting amplitude-

frequency characteristic is shown in (d) and is identical to that originally presented to the pre-emphasis circuit. Thus the speech signals are not altered in any way by the pre-emphasis and de-emphasis processes. But note that any noise that enters the system between the pre-emphasis and de-emphasis circuits and has a more or less continuous spectrum throughout the passband is reduced by the de-emphasis process. For a PCM speech system in particular, the effect of quantization noise[*] can be substantially reduced. Thus, pre-emphasis increases the efficiency of the system by decreasing the noise.

If, in addition to pre-emphasis, the proposed framing scheme is used, it is obvious that the higher frequencies in speech cannot be pre-emphasized to the same extent if none of the information content of the speech is to be sacrificed. Thus, pre-emphasis cannot be as beneficial as in the first case and the system must operate with a greater amount of noise in the received signal.

On the basis of a comparison of the two cases: the system with the maximum pre-emphasis and an entirely separate means of framing, and the system with partial pre-emphasis and the proposed framing scheme, an evaluation of the framing proposal can be carried out.

The evaluation is carried out on the basis of a comparison of the noise that results in the two cases.

The first case yields the following results. Assume that group synchronization is carried out by some other means,

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[*]   The noise in a PCM system may be assumed to be entirely due to quantization, since the signal power can always be increased to reduce all other types of noise to negligible values.

a consideration of which may be ignored. The received signal

is then decoded and a certain amount of quantization noise is

found. After de-emphasis, however, the amplitude of the noise

is greatly reduced. This effect is illustrated in Figure 3.4.

The noise power in the passband is then calculated by a simple

numerical integration method, and then equated to the noise

of an equivalent system whose noise amplitude is constant but

for which the number of digits per code group, n_1 is unknown.

Solving for n_1 yields the number of digits per code group for

an equivalent system with the same noise power.

The second case leads to another value, n_2, smaller

than the first because the amount of noise this time is greater.

The noise frequency characteristic of this case is also

illustrated in Figure 3.4.

The difference in the value of n is then the number of

bits per code group given up by the total information capacity

of the binary channel to the proposed synchronization scheme.

The calculations will now be carried out. Refer to

Figure 3.4.

Let N_0 be the total quantization noise power of an

n-digit PCM system which uses no pre-emphasis. Noise power

is taken to be the square of the r.m.s. noise amplitude, A_n.

It was shown in section 2.4 that A_n is given by

$$A_n = \frac{A_0}{\sqrt{3} \cdot 2^{n+1}} \qquad \text{or} \qquad N_0 = \frac{A_0^{\,2}}{3 \cdot 2^{2(n+1)}}$$

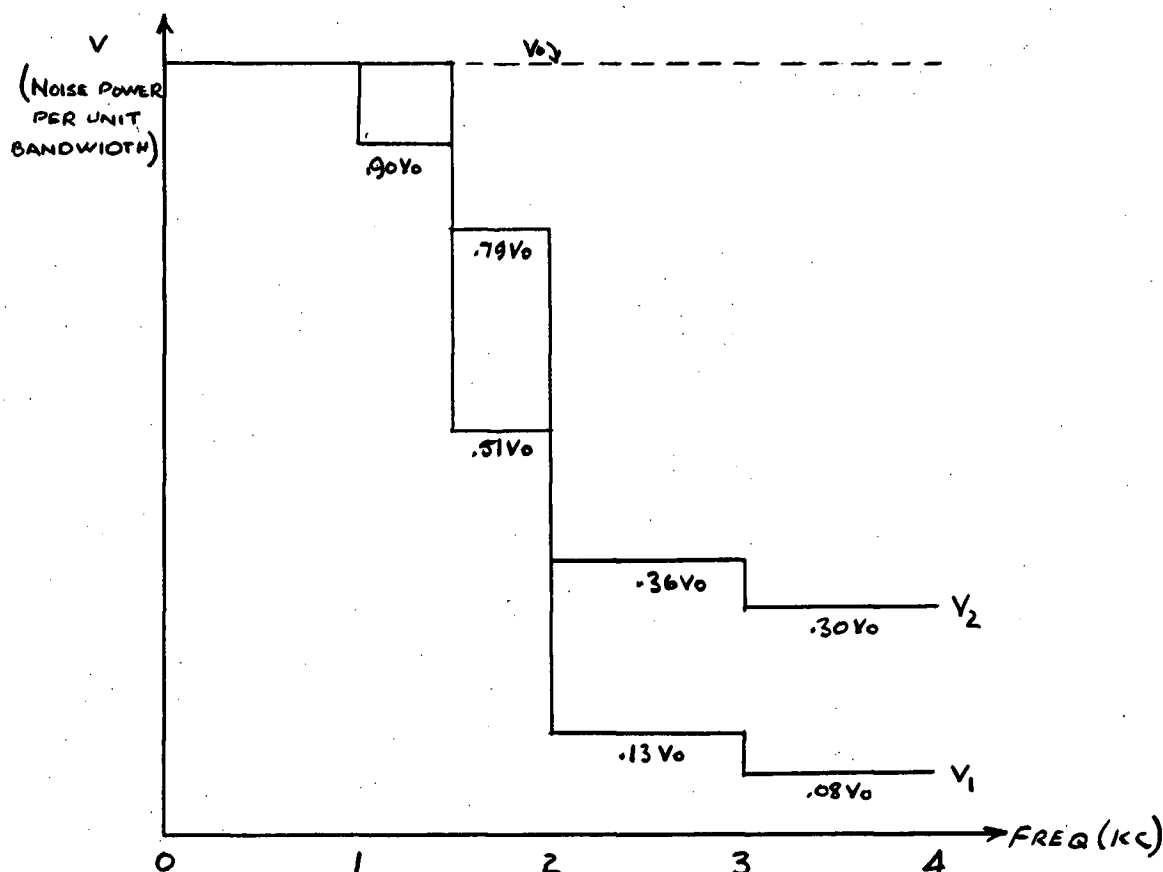This noise is uniformly distributed over the frequency band

Figure 3.4 Power Spectrum of Quantization Noise in Various PCM Systems

v_0 - system without pre-emphasis

v_1 - system with maximum pre-emphasis allowed by speech spectrum

v_2 - system with partial pre-emphasis due to high frequency restriction imposed by the proposed framing scheme

Note that $v_1 = v_0 (A_s/A_0)^2$ and $v_2 = v_0 (A_s/A_m)^2$

where A_s and A_m are given in Figures 3.1 and 3.2.

W_0 (= 4 kc) so that the noise power per unit bandwidth, v_0, is constant throughout. Therefore,

$$v_0 = N_0/W_0$$

Consider now the noise of the same n-digit PCM system, but using the maximum amount of pre-emphasis possible; no restrictions are imposed by framing schemes. Let N_1 be its total noise power and v_1 its noise power per unit bandwidth. v_1 at any frequency is given in terms of v_0 by $v_1 = v_0(A_s/A_0)^2$, and therefore

$$N_1 = \int_0^{W_0} v_1 \cdot df = \frac{N_0}{W_0} \int_0^{W_0} \left(\frac{A_s}{A_0}\right)^2 df = 0.48 \, N_0$$

using numerical integration in Figure 3.4.

The use of pre-emphasis in an n-digit PCM system has therefore more than halved the noise power. The signal to noise ratio is now equal to that of a PCM system using no pre-emphasis but employing n_1 digits per code group. This "effective digit number", n_1, is found as follows:

$$\frac{N_1}{N_0} = \frac{A_0^2/(3 \cdot 2^{2(n_1+1)})}{A_0^2/(3 \cdot 2^{2(n+1)})} = 2^{-2(n_1-n)}$$

Therefore $n_1-n = -\frac{1}{2} \cdot \log_2(0.48) = 0.53$ digits.

When the proposed framing system is used, the high frequency components are restricted to amplitude A_m, and only partial pre-emphasis can be used. Hence the noise power per unit bandwidth, v_2, and the total noise power, N_2, are not reduced as much.

$$v_2 = v_0 \, (A_s/A_m)^2 \text{ and } N_2 = \int_0^{W_0} v_2 \cdot df = \frac{N_0}{W_0} \int_0^{W_0} \left(\frac{A_s}{A_m}\right)^2 df = 0.64 N_0$$

Consequently the new effective digit number, n_2 is not as large as before, and $n_2 - n = 0.32$ digits.

The cost of the proposed framing scheme in loss of quality of the received signal is therefore seen as equivalent to the loss of $0.53 - 0.32 = 0.21$ digits per code group.

Other PCM systems could conceivably achieve correct framing by sacrificing fewer digits per code group on the average, by adding or substituting framing pulses at frequent intervals rather than in every code group. For example, one framing pulse could be added at the end of every tenth code group, or the last pulse in every tenth code group could be sacrificed in favour of framing. But, it is apparent that such schemes are unfavourable because either method, the addition of a framing digit or the substitution of a framing digit for an information digit in a code group at frequent intervals, increases the complexity of the instrumentation considerably.

3.4 Misframing Detection and Correction

If the difference in amplitude between two successive decoded samples exceeds one-half of the range of the system, an error in framing is indicated. The conditions under which error indication occurs will now be investigated.

Assume that the system under consideration is one employing 7 digits per code group, giving rise to 128 possible discrete levels, and a sampling rate of 8kc/s. Figure 3.5 illustrates the time relationship within a code group.
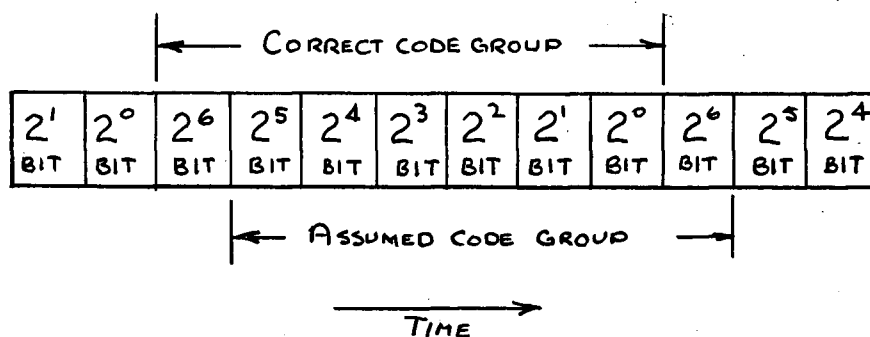

Figure 3.5 Misframing by 1 Digit

Suppose that the decoder is operating on an incorrect frame and in fact is operating on a code group 1 bit later in time than the correct group. That is, the decoder assumes that the true 2^5 bit to be the 2^6 bit and the true 2^6 bit to be the 2^0 bit as illustrated in Figure 3.5. It can be argued that if the actual input signal to the coder has a slope of less than ± 32 levels per sampling period, that is, the sample amplitudes of two consecutive sampling intervals differ by less than 32

levels, an error will be indicated in the decoder if the input signal crosses the 64 level during the sampling period. The situation is illustrated in Figure 3.6.
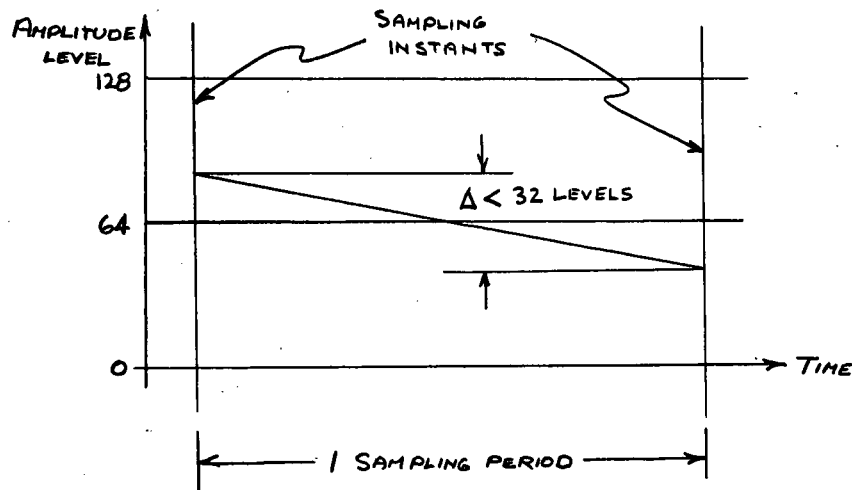

Figure 3.6 Input Signal That Crosses the 64 Level With Slope
            of Less Than 32 Levels/Sampling Period

For example, suppose the amplitudes at the first and second sampling instants in Figure 3.6 are 70 levels and 40 levels respectively. The slope is then 30 levels/sampling period and the signal crosses the 64 level during the sampling period. The binary representations of 70 and 40 are 1000110 and 0101000 respectively, reading from left to right, the most to the least significant digit. If the decoder were operating on the code group 1 digit later from the correct group the numbers would be interpreted by the decoder as 0001100 and 101000_ respectively, where _ indicates the first digit in the following code group. In decimal numbers, the decoded values would then be 12 and either 80 or 81 respectively, depending on whether the first digit in the following code group is 1 or 0.
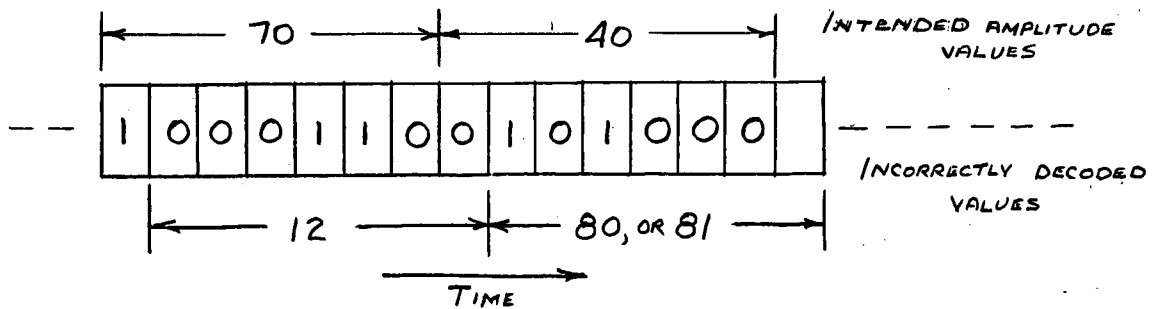
The situation is illustrated in Figure 3.7.

Figure 3.7   Decimal Numbers 70 and 40 Incorrectly Decoded as 12
and 80 or 81

Because the decoded values differ by either 68 or 69, both
of which are greater than 64, the framing circuit detects that the
decoder is operating upon the incorrect pulse group. Hence, the
decoding operation is shifted to a group one digit later in time.

A similar argument can be made for the situation where
the decoder is operating upon a pulse group one digit removed as
in the above case but where the slope of the input signal is
greater than 32 levels and the input signal does not cross the 64
level during the sampling period. Again, the decoder framing
circuit detects the error in framing and shifts the decoding
operation to a group one digit later in time.

There are two cases, when the decoder is operating on
a frame one digit later in time than the correct one, when no
error will be indicated. These cases arise when the input
signal does not cross the 64 level and has a slope of less than
$\pm$ 32 levels per sampling period, and when the input signal crosses
the 64 level and has a slope of between $\pm$ 32 and $\pm$ 64 levels
per sampling period. It is possible to reduce the likelihood of

misframing due to the above causes if the 64 level of the system is established as the zero signal level. The most probable amplitudes in speech waveforms are those less than one-half the maximum or those within $\pm$ 32 levels of the zero signal level. Furthermore, the most probable time between zero axis crossings in speech is about 1 millisecond or 8 sampling periods.[16] The combination of these two factors then ensures that permanent misframing by one digit will be highly unlikely. In fact, the most probable time for indication of misframing by one digit is one-half millisecond, since zero axis crossings are likely to occur every millisecond.

All possible situations for misframing by one digit have been described. Similar arguments can be applied to cases of misframing by more than one digit. Conditions for framing error indication are summarized in Table 3.1.

Misframing by _ Digits	Input signal crosses _ levels and has slope of _ levels/sampling period		Input signal does not cross _ levels and has slope of _ levels/sampling period		Approximate probable time for error indication (msec)
	Levels	Slope	Levels	Slope	
1	64	$0 < |s| \le 32$	64	$32 < |s| < 64$	½
2	32, 64, 96	$0 < |s| \le 16$	32, 64, 96	$16 < |s| < 64$	¼
3	16, 32, 48, 64, 80, 96, 112	$0 < |s| \le 8$	16, 32, 48, 64, 80, 96, 112	$8 < |s| < 64$	⅛
4	8, 16, 24, 32, 40, 48, 56, 64, 72, - - -	$0 < |s| \le 4$	8, 16, 24, 32, 40, 48, 56, 64, 72, - - -	$4 < |s| < 64$	⅛
5	4, 8, 12, 16, 20, - - -	$0 < |s| \le 2$	4, 8, 12, 16, 20, - - -	$2 < |s| < 64$	⅛
6	2, 4, 6, 8, 10, - - -	$0 < |s| \le 1$	2, 4, 6, 8, 10, - - -	$1 < |s| < 64$	⅛

Table 3.1 Conditions and Approximate Probable Times for Misframing Error Indication

It is apparent that the time required for error
detection in the cases of misframing by more than one digit
is somewhat less than that required to detect an error of
misframing by one digit because of the greater number of
possible conditions under which misframing errors are detected.
In fact, for the cases of misframing by more than three digits,
misframing errors are detected as often as not with each
subsequent sampling period. The average time for error
detection is then reduced to one sampling period or 1/8 milli-
second.

The total time for achieving correct group
synchronization is the sum of the times for framing error
indication and error correction. Each shifting operation requires
15 pulse times as shown in Figure 3.8 because in addition to the
single pulse time during which the action of the decoder is
inhibited, the action of the framing error detection circuit must
be inhibited for 1 group time, since a comparison of the
amplitudes of the reconstructed sample from the new assumed code
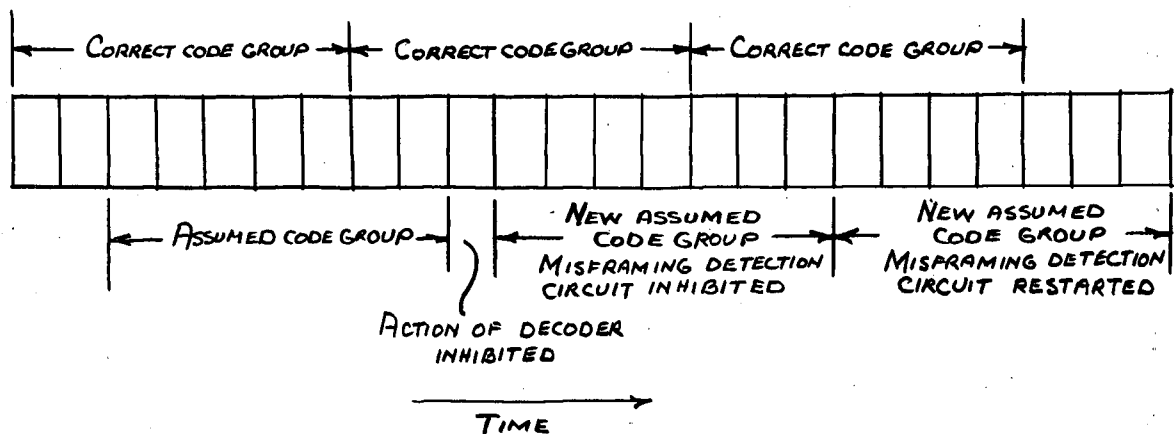group with the previous reconstructed sample is meaningless.

Figure 3.8   Time Required For Misframing Error Indication and
             Shifting

The action of the framing error detection circuit resumes on arrival of the next assumed code group. The total time required to achieve correct framing is, at worst, approximately 3 msecs.

If the decoder is operating upon a code group one digit later in time than the correct group, it is misframing by one digit. When an error is indicated the action of the decoder is such that its operation is inhibited for one pulse time. This action results in the decoder acting upon a group two digits removed from the correct group. Thus, the decoder is misframing by two digits. In general, then, inhibiting the action of the decoder for one pulse time results in further misframing unless, of course, the decoder happens to be misframing by six digits, in which case one shifting action results in correct framing.

It is apparent that correct framing is achieved faster by inhibiting the action of the decoder for one pulse time than by advancing the action of the decoder. This results from the fact that, on the average, indication times for misframing by one or two digits are longer than the indication times for misframing by a greater number of digits.

An outline of the proposed pulse group synchronization or framing scheme for a PCM speech system has now been described. It is economical and relatively simple to instrument. The next chapter describes the instrumentation of the scheme as incorporated in the decoder. Experimental test results of the proposed framing scheme are given in Chapter 5.

4. SYSTEM DESIGN

This chapter describes the design and operation of the constructed PCM system. Since the majority of the design undertaken by the author was on the decoder, the decoder is described first. The operation and the circuits of the decoder are described, followed by a description of the group synchronization circuits. A brief description of the operation of the coder concludes the chapter.

The PCM system constructed was designed to handle signals ranging in frequency from a few cycles per second to 4000 cps. The sampling is carried out at the Nyquist rate or 8000 times per second. A 7 digit code is employed permitting an amplitude range of $2^7 = 128$ levels, more than adequate for voice signal applications. The pulse group frequency is then 8000 cps and the pulse repetition frequency is 7 x 8000 = 56,000 cps. The code pulses are transmitted serially in time where the order of transmission in any pulse group is from the most significant to the least significant digit.

The coder is one of the circulating pulse type and the decoder is essentially one of the pulse count type. Both the coder and decoder are fully transistorized and operate on power supplied by three 12v storage batteries.

4.1 The Decoder

4.1.1 The Basic Decoder Circuit

In order to successfully handle a binary code, the decoder

must be able to produce a series of binary weighted values
and store them either as individual values or as a sum of the
series. In the design of the decoder it was decided that the
binary weighted values in the form of binary weighted currents
would be produced by current generators which were turned "on",
in sequence, for a fixed length of time. The resulting binary
weighted amounts of charge are then summed and stored as a
voltage on a capacitor. A coincidence gating arrangement using
pulses derived from a count-down-by-seven counter and a pulse
regenerator is used to determine the correct current generators
to be turned on. The basic circuit is illustrated in Figure 4.1.
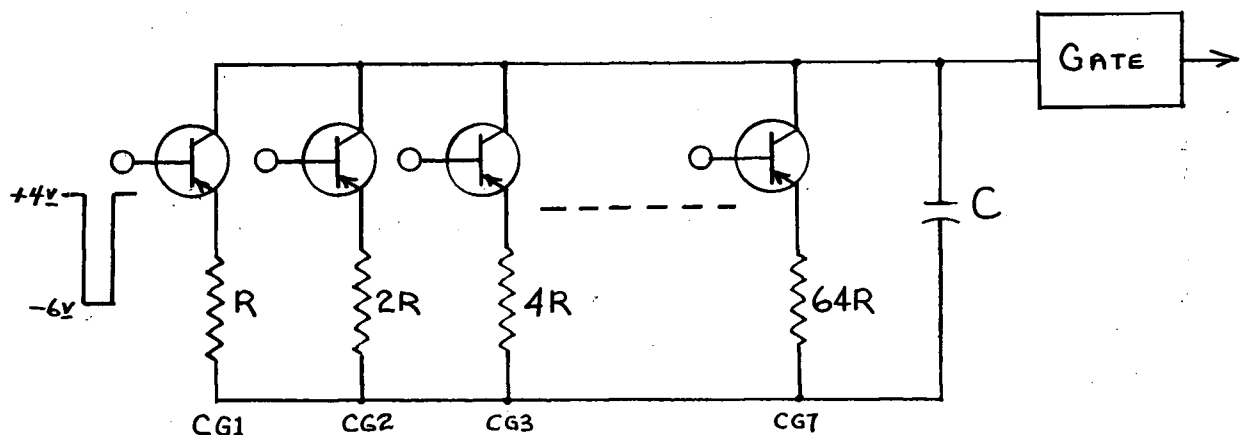
Figure 4.1 Basic Circuit of the Decoder

Assuming that the decoder is operating upon the correct
pulse group or frame, the current generators are turned on in
time sequence from left to right in Figure 4.1 according to
whether or not the particular code pulse in the group is present.
Each current generator, when turned on, allows a pre-determined
current to flow for a fixed time interval, thereby, allowing a

fixed charge to flow into the capacitor. Moreover, with the exception of CG1, each current generator allows one-half of the charge of the previous current generator to flow into the capacitor thereby producing a binary weighted series. The final value of voltage on C after one code group is then proportional to the quantized input sample amplitude presented to the coder.

After one cycle of operation of the current generator, a charge transfer gate which was closed during the cycle opens and allows the charge to flow into subsequent circuits and, at the same time, discharges C to some reference value. The gate then closes, preparing the decoder circuit for another cycle.

The design of the basic decoder circuit was carried out beginning with a consideration of the current and voltage limitations of the transistors used. 2N1309's were chosen primarily for their favourable switching characteristics. The reference voltage to which the capacitor is discharged was chosen to be -12 volts. To permit reasonable size emitter resistors, the turn on pulses were designed to be negative pulses, 10 volts in height, from + 4 to - 6 volts, and 4 microseconds in width. Then, the voltage range available in the capacitor was chosen to be 5 volts, from - 12 volts to - 7 volts, thus ensuring that the current generators transistors were not saturated at any time.

Now, since the entire voltage range of 5 volts was to represent 128 levels, the capacitor voltage was required to be accurate to 1 level or $\frac{5.0}{128} = 39$ millivolts. The minimum possible

value of the capacitor C was fixed by the sum of the I_{co} currents through the current generators. That is, the minimum value of C was such as to ensure that the I_{co} currents would not alter the voltage on the capacitor by more than 18.5 mv during any pulse group period. Hence

$$C > \frac{\sum I_{co}\text{'s (125 }\mu\text{ sec)}}{39 \text{ mv}} = \frac{7(2 \times 10^{-6})(125 \times 10^{-6})}{(39 \times 10^{-3})}$$

$$= 47.7 \times 10^{-9} \approx .048 \text{ }\mu f$$

The maximum possible value of C was determined on the basis of the maximum permissible current in CGl. When CGl was turned on, it was required to supply enough current such that the voltage on C was increased by one-half of the voltage range permitted on C or 2.5 volts. Hence

$$C < \frac{I_c \text{ max (4 }\mu\text{sec)}}{2.5v} = \frac{(300 \times 10^{-3})(4 \times 10^{-6})}{2.5}$$

$$= 480 \times 10^{-9}$$

$$= 0.48 \text{ }\mu f$$

The value of C was chosen to be 0.07 μf to ensure that the maximum power rating of CGl would not be exceeded. The choice of the value C then fixed the value of the required weighting resistors.

For example, the current required when CGl is turned on is

$$I_1 = \frac{\Delta Q_1}{\Delta t} = \frac{C\Delta V_1}{\Delta t} = (0.07 \times 10^{-6}) \frac{(2.5)}{4 \times 10^{-6}} \text{ amps.}$$

The required weighting resistance is

$$R = \frac{V_e}{I_1} = \frac{(6 - 0.2)(4 \times 10^{-6})}{(0.07 \times 10^{-6})(2.5)} = 132.8 \text{ ohms.}$$

The remaining weighting resistors are binary multiples of **R.**

4.1.2 Operation of the Decoder

The operation of the decoder is described briefly as follows. The incoming code pulses are regenerated in the pulse regenerator or repeater. At the same time, they establish and maintain the basic pulse repetition frequency in the decoder by pulling an oscillator into phase. The sine-wave oscillations from the oscillator are converted to square waves which are then differentiated. The resulting pips are then employed to trigger a bistable counter with a count-down-by-seven arrangement which establishes the pulse group frequency.

By suitable connections to various collectors of the bistable counter, a cyclic sequence of seven gating pulses is produced in Gate 1. Turn on pulses for the various current generators are then formed by gating the sequence of seven pulses with the regenerated pulses from the repeater, in Gate 2. The arrangement is such that the height of the resulting turn on pulses for the current generators is independent of the gating pulses but the width is determined by the width of the repeater pulses.

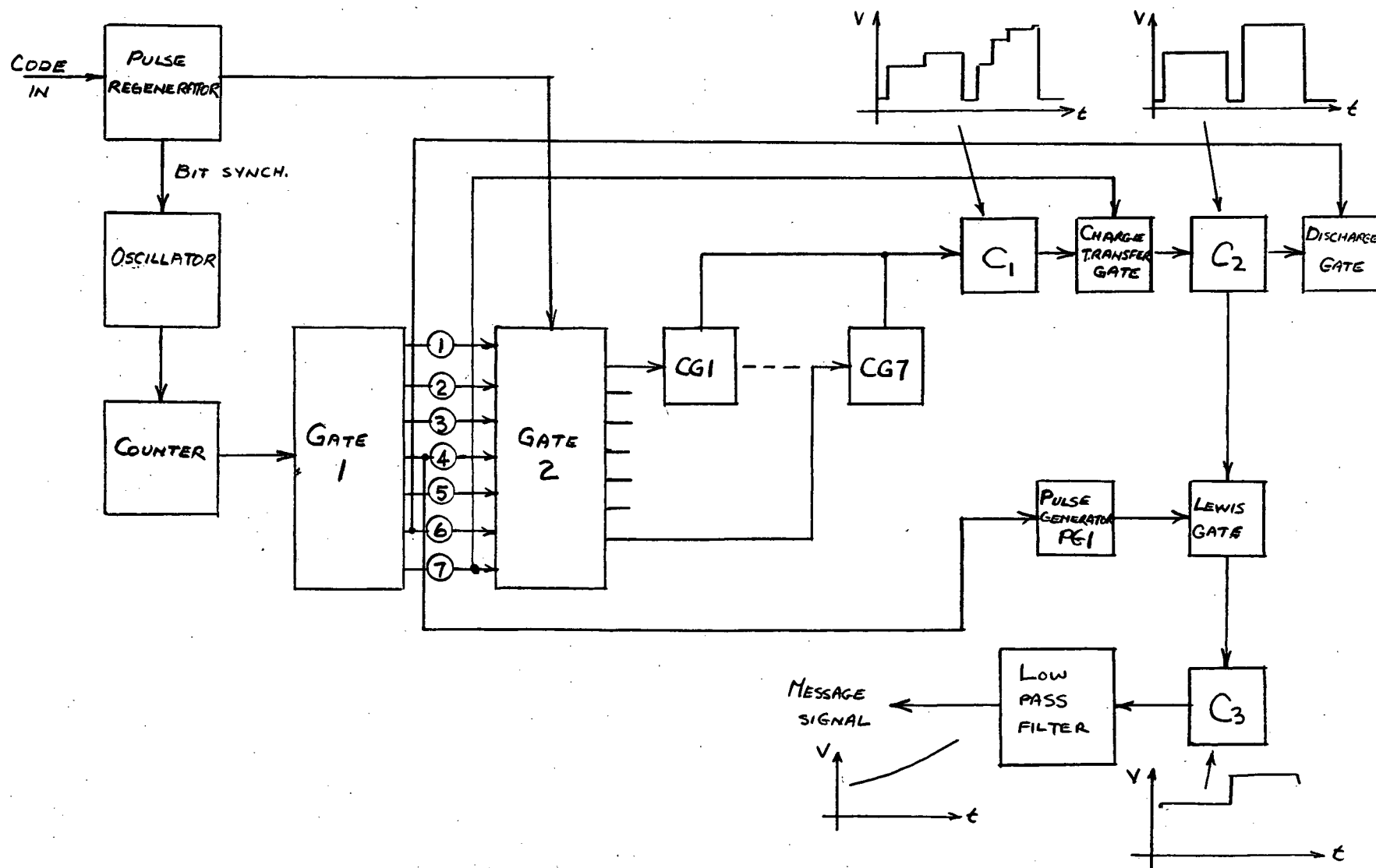Thus, the output from Gate 2 is a sequence of turn on

Figure 4.2   Block Diagram of Decoder

pulses of precise height and width and identical in pulse pattern to the code pulses presented to the repeater. This sequence is used to turn on the appropriate current generators and a sample amplitude is reconstructed on C_1.

During interval 7, as established by the output of Gate 1, the charge stored in C_1 is transferred to C_2. The charge transfer gate is open during the entire interval so that any charge resulting from CG7 during the interval is also transferred. Thus, from interval 7 to interval 6 of the following cycle, the value of the reconstructed sample amplitude as originally coded by the coder is stored in C_2. C_2 is discharged during interval 6 to prepare it for the charge from the following decoding cycle.

During interval 4, the voltage on C_2 is transferrred to C_3 by the Lewis gate. The voltage on C_3, then, is a step function. The waveform on C_3 is filtered and amplified as the desired audio output. Sample waveforms of the decoding operation are given in Figure A-2.11.

In the above description, three details were ignored, in order to facilitate the explanation. In the final decoder circuit Gates 1 and 2 were combined into one gate, one for each current generator, and separate gates were used to produce the pulses for the charge transfer gate and discharge circuits. A delay was introduced between the repeater and the current generator gates to offset the delay in counter circuits. Finally, a monostable pulse generator, PG1, triggered during interval 4, is used to operate the Lewis gate.

4.2 Operation of Framing Circuit

In order for the group synchronization or framing circuit to operate successfully, it is only necessary for the amplitudes of two successive decoding operations to be compared. If the difference in amplitude is less than one-half of the amplitude range of the system, nothing is done. If the difference in amplitude is greater than one-half the amplitude range of the system, one pip from the differentiated square wave is inhibited and thereby prevented from reaching the counter. The result is that the entire decoding operation is shifted by one digit to a new frame one digit later in time.

The block diagram of the required circuitry is illustrated in Figure 4.3. The operation is described as follows. The voltages on C_2 and C_3 are compared during interval 7 by a voltage comparator that produces a negative output regardless of the polarity of the difference. The output of the voltage comparator is then gated to eliminate the undesirable portions of the voltage comparator output and to ensure proper timing in subsequent circuits. The gated output of the voltage comparator is applied to a Schmitt trigger that is set to fire at a voltage corresponding to one-half the amplitude range of the system. If the Schmitt trigger fires, a pulse is produced that inhibits one pip into the counter, thereby shifting the operation of the decoder by one digit. The firing of the Schmitt trigger also inhibits the action of the voltage comparator circuit, while the shifting occurs.
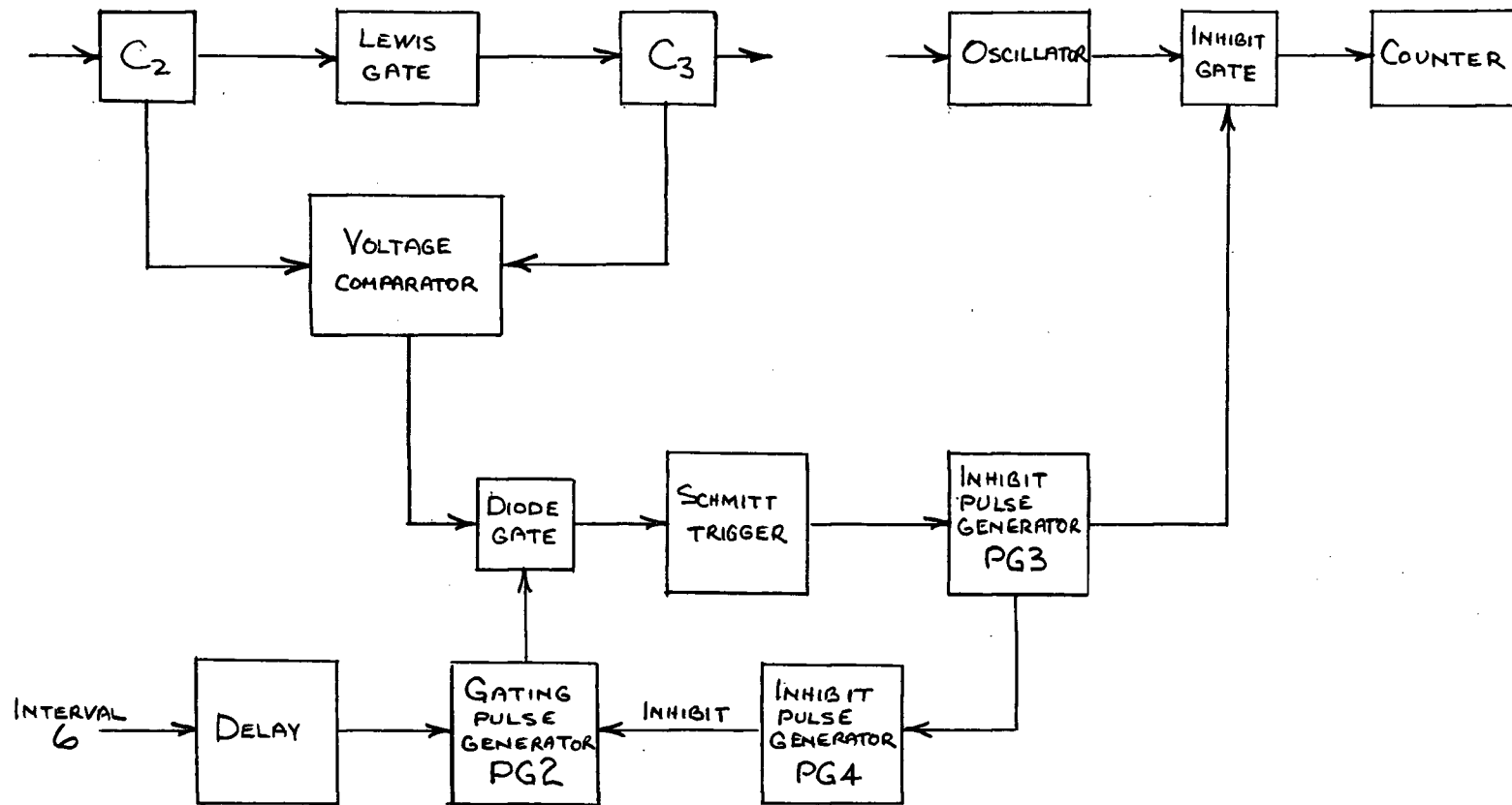
Figure 4.3   Block Diagram of Framing Circuits

Various pulse generators are required to carry out the operation. Because an output from the voltage comparator is undesirable until late in the 7th interval, it was necessary to produce the diode gate gating pulse (PG2) by delaying a trigger pulse derived from interval 6. PG3 is used to produce the pulse that inhibits a pip into the counter. PG4 is triggered by PG3 and is used to inhibit the action of the voltage comparator by inhibiting PG2.

The timing waveforms for the framing circuits are shown in Figure A-2.12.

4.3   Operation of the Coder

A coder to convert analog signals into 7 digits of PCM was built by Hafer and is described in his thesis[10]. Only a brief description is given here.
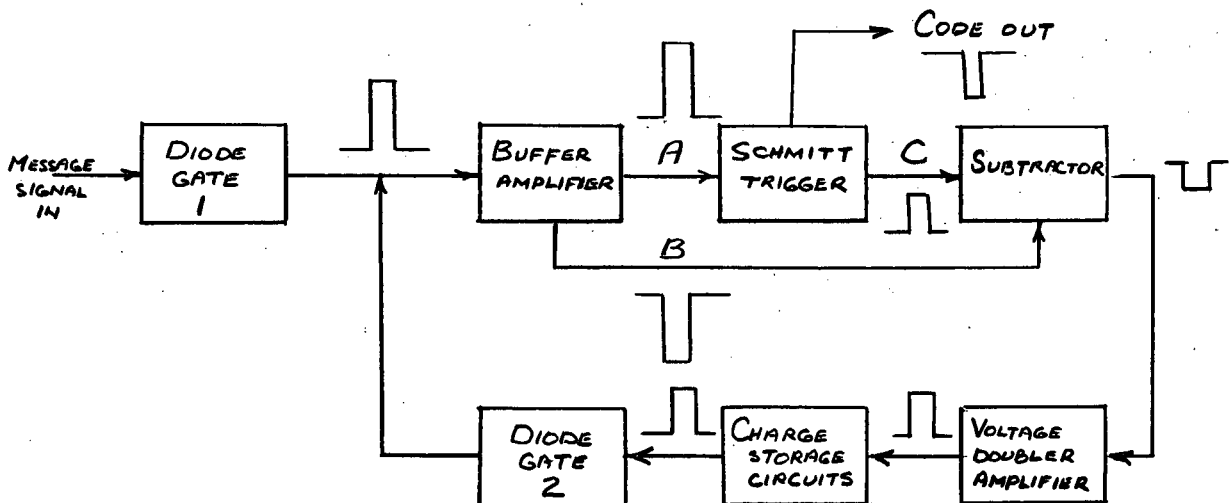
Figure 4.4   Block Diagram of Coder

The block diagram of the coder, excluding the timing circuits, is illustrated in Figure 4.4. When an analog signal is applied to the coder, diode gate 1 samples the amplitude for 6 microseconds. After passing through the buffer amplifier it emerges unaltered at A and inverted at B.

The output from A is applied to a Schmitt trigger which is set to fire at a voltage $A_0/2$, where A_0 is the maximum expected signal level. If the input sample pulse amplitude exceeds $A_0/2$ the Schmitt trigger fires and an output code pulse is produced. At the same time, the Schmitt trigger also produces a positive pulse of fixed height $A_0/2$ at C, which is subtracted from the output at B. If the input sample pulse amplitude does not exceed $A_0/2$, the Schmitt does not fire and neither the code output pulse nor the positive pulse of height $A_0/2$ is produced. The output of the buffer amplifier at B is then passed on, unaffected by the subtractor, to the voltage doubler amplifier.

The output of the subtractor is applied to the voltage doubler amplifier where it is inverted and doubled in amplitude. The pulse is then applied to the charge storage circuit.

The charge storage circuit stores the output pulse of the voltage doubler amplifier for one pulse period as charge on a capacitor. At the end of one pulse period, diode gate 2, which up to this time has been closed, allows the pulse to be applied to the buffer amplifier once more.

Diode gate 1 is closed at this time and remains closed for 7 pulse periods while the original input sample pulse is

allowed to circulate around the loop a total of 7 times.
Each circulation produces an output code pulse or space
depending on whether the Schmitt trigger fires or not. The
first circulation produces the output code corresponding to the
binary weighted value 2^6, the second circulation 2^5, and so on
until the last circulation produces a code output corresponding
to 2^0.

At the conclusion of 7 circulations, the recirculated
pulse is inhibited and a new input sample pulse is taken by
diode gate 1.

It is apparent then, that the coder is able to produce
a binary coded output in serial fashion with the most signif-
icant digit first.

The operation of the PCM system in block diagram form
has now been described. The circuit details including the
modifications made to the coder are given in Appendix 2 and 3.
The next chapter deals with the results of tests on the system.

5. SYSTEM TESTS

5.1 System Performance

The system, as outlined in Chapter 4, performed satisfactorily. Listening test with audio program material indicated that good quality speech transmission was possible, provided that the system was not overloaded.

The power required is approximately 1.4 watts in the coder and 1.3 watts in the decoder (including the framing circuits) for a total power consumption of approximately 2.7 watts.

A delay of 0.35 milliseconds or 2.8 sampling periods between the message signal at the coder and the decoded but unfiltered message signal was observed. The delay is due mainly to the time required for the coding and decoding processes and is of no practical importance.

Instability and drift due to small changes in room temperature did not affect the performance of the system.

The decoder proved to be accurate and reliable. The oscillator in the decoder tolerated changes in the master clock frequency of $\pm$ 3.9% from the centre frequency, thus ensuring that the decoder would follow small changes in frequency caused by effects such as temperature changes.

The framing scheme performed more than adequately and errors due to misframing were few. Framing errors occurred only when the system was overloaded to such an extent that the input

signal restrictions were violated. It was found that the required input signal restriction for operation of the framing scheme was slightly more stringent than the requirements derived from theory. Figure 5.1 illustrates the required input signal restriction for system performance as well as the restrictions as derived in Appendix 1. The time required for proper framing was not measured but observations with an oscilloscpe indicated that correct framing was achieved in times of the order of a few milliseconds. In fact, listening tests during which transmission was interrupted disclosed that correct framing was achieved in a time so short that noise due to misframing was inaudible.
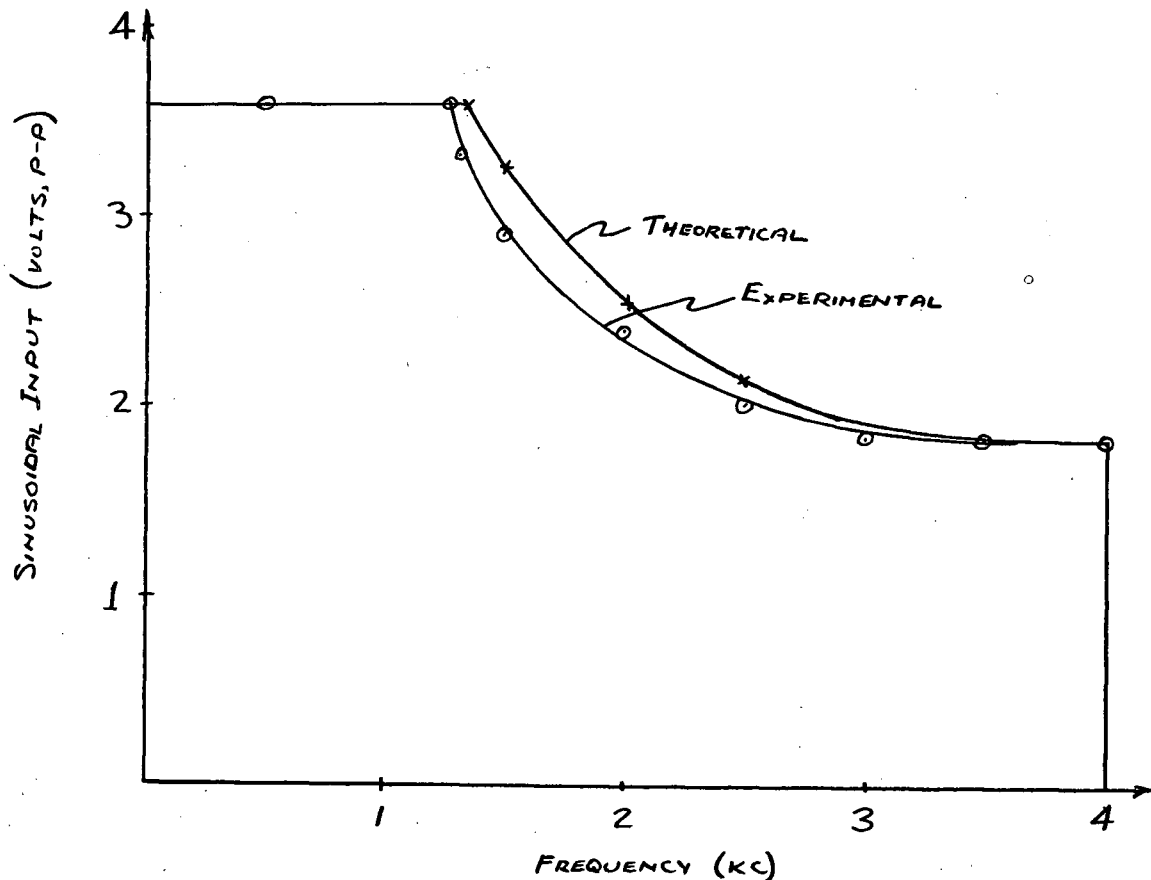
Figure 5.1   Input Signal Frequency-Amplitude Characteristic
             for Successful Operation of the Framing Scheme

The weakest link in the system is the coder which, in spite of the many hours spent in modifying and redesigning, is still lacking in linearity. The imperfections are thought to be due mainly to the non-linearity of the action of the voltage doubler amplifier. (See Figures 4.4 and A-3.3).

5.2 Linearity Tests

Figures 5.2 and 5.3 indicate the results of the linearity tests on the coder and decoder respectively. The test was carried out on the coder by using a series of known d.c. voltages as the input signals and observing the resulting output codes. The test of the decoder was carried out in the same way -- by using coded pulses as the input signals to the decoder and observing the d.c. voltage outputs. In both cases, the coded values in decimal form were plotted versus the measured d.c. voltages.

The non-linearity of the operation of the coder was traced to the voltage doubler amplifier. The gain of the amplifier is less than two at low amplitude levels. As a consequence, when the input signals are of such values that the circulating pulses are small in amplitude, the required input signal voltages are greater than they should be.

5.3 Noise and Distortion

A measure of the distortion and noise produced by the
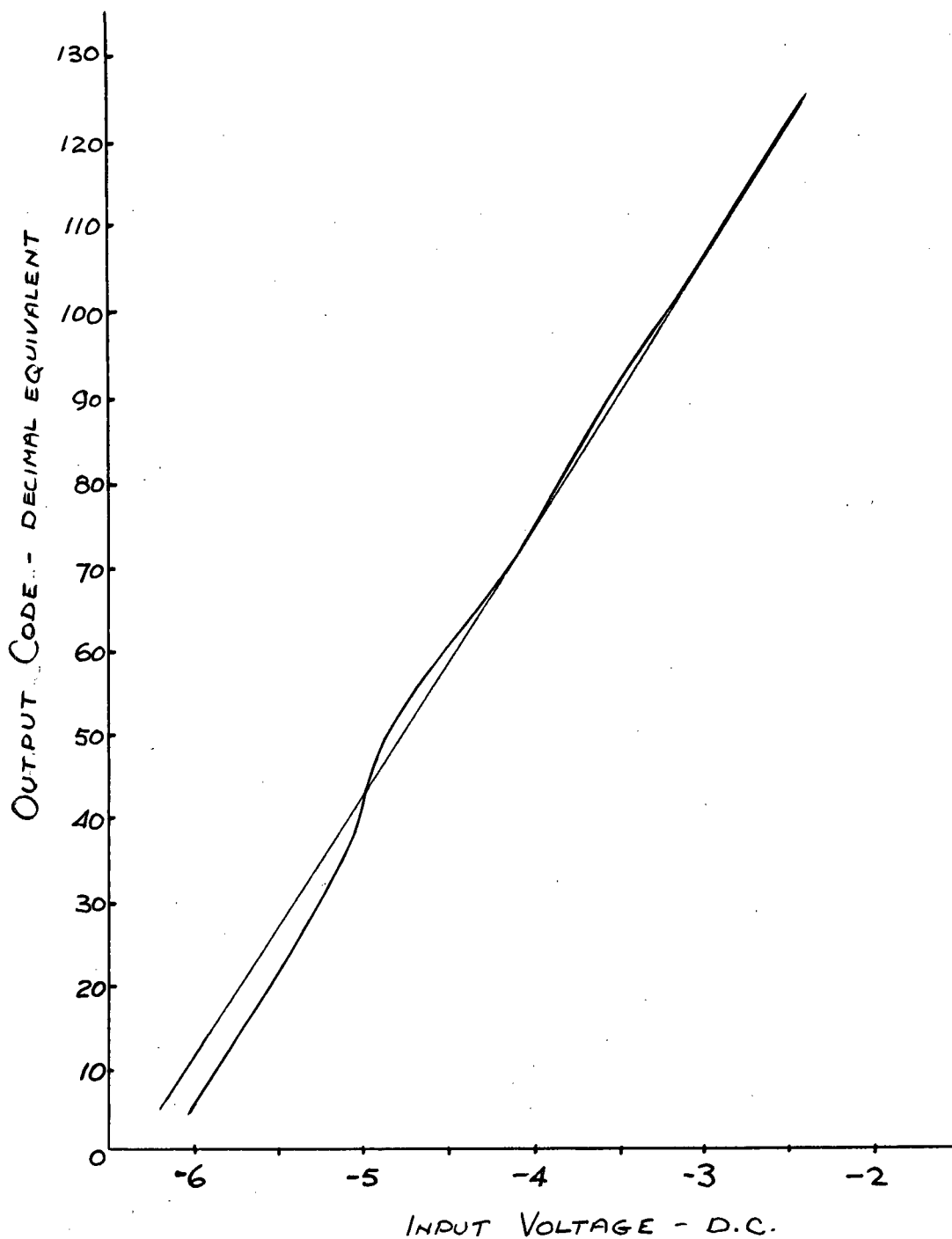
Figure 5.2 Linearity Test of Coder
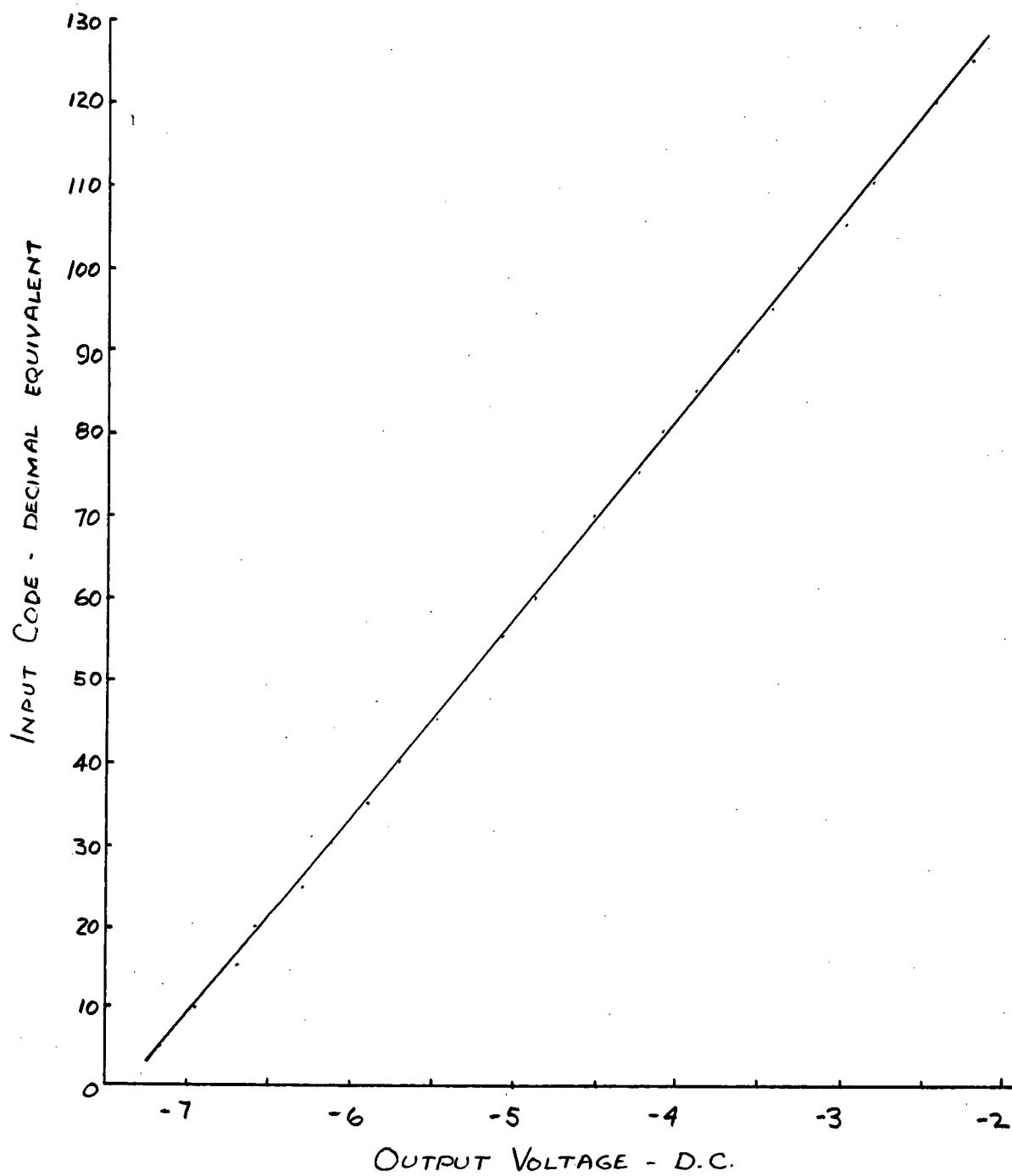
Figure 5.3 Linearity Test of Decoder

system was made by measuring the harmonic distortion of the output message signal using a sine-wave as the input message signal. The method is outlined in Figure 5.4.
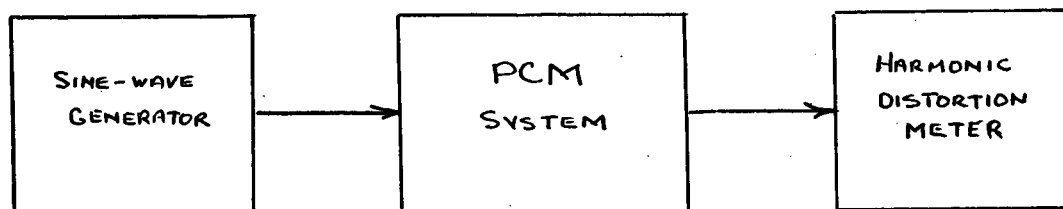

Figure 5.4   Noise and Distortion Measurement

The method served only to indicate that the distortion voltage was much larger than the calculated quantizing noise. This is to be expected in view of the imperfections in the coder linearity as shown in Figure 5.2 and the imperfections in the output low pass filter.

5.4   Waveforms

Figure 5.5 illustrates some example waveforms transmitted by the system. The upper waveform in each oscillogram is the decoded step waveform before filtering, and the lower waveform is the resulting filtered version of the step waveform, which is almost indistinguishable from the input sine-waves.
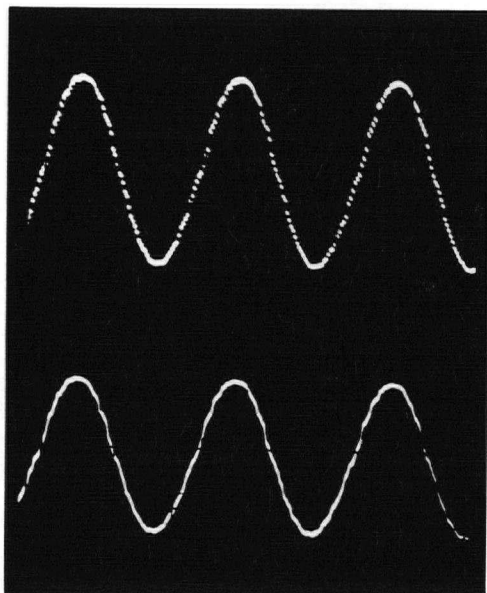
100 cps
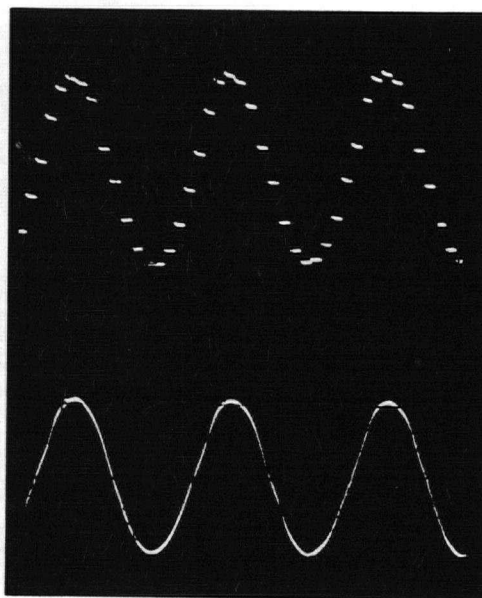
500 cps
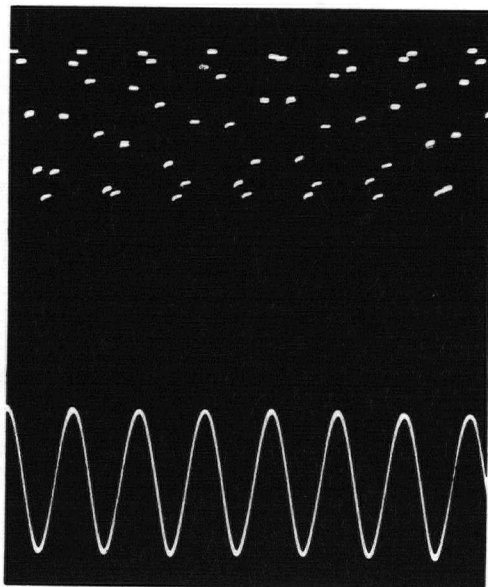
1000 cps
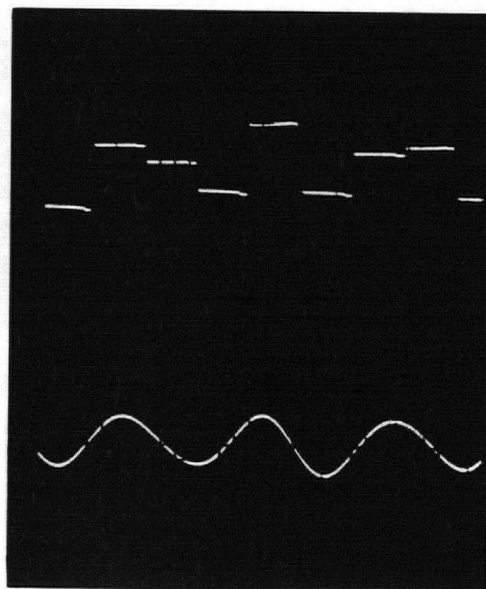
3000 cps

Figure 5.5 Waveforms. Oscillograms of Decoded Signals on C_3 and at Output of Low Pass Filter

6. CONCLUSIONS

A self-framing PCM speech system has now been described. The results of tests on the system indicate that performance is adequate for transmission of good quality speech.

The coder deserves further work. The non-linear input-output characteristic causes distortion at low input signal levels and it is thought that much of the distortion could be eliminated by improving the action of the voltage doubler amplifier.

The decoder and the novel framing circuits performed perfectly and correct group synchronization was achieved quickly and efficiently using simple circuitry.

Although the framing scheme was employed on a single message channel system, the scheme could easily be adapted to larger systems where many message channels are transmitted by time division multiplexing methods. The system would be designed so that once correct framing is achieved in one channel, then, simultaneously, correct framing is achieved in all channels. The maximum pre-emphasis is employed in all message channels except the one that is used for framing purposes. The speech signals in this channel are only partially pre-emphasized and the framing circuits are attached to the decoder for this channel. Framing errors are then detected in the same manner as described in Chapter 3.

But, for a large system, where 24 to 96 or more message channels are transmitted by time division multiplexing methods over one transmission channel, the proposed scheme is not as

advantageous because of considerations such as the time required for achieving proper framing. Such a system can easily afford to sacrifice an entire message channel for a more efficient framing scheme.

The proposed self-framing scheme presented in this thesis is best suited for a PCM speech system that utilizes a small number of message channels. In such a system, economy in the use of the digits is of prime concern in order to conserve bandwidth and to simplify the instrumentation. The simplicity and reliability of the self-framing scheme makes it ideal for use in such an application.

APPENDIX 1

Derivation of Figure 3.1
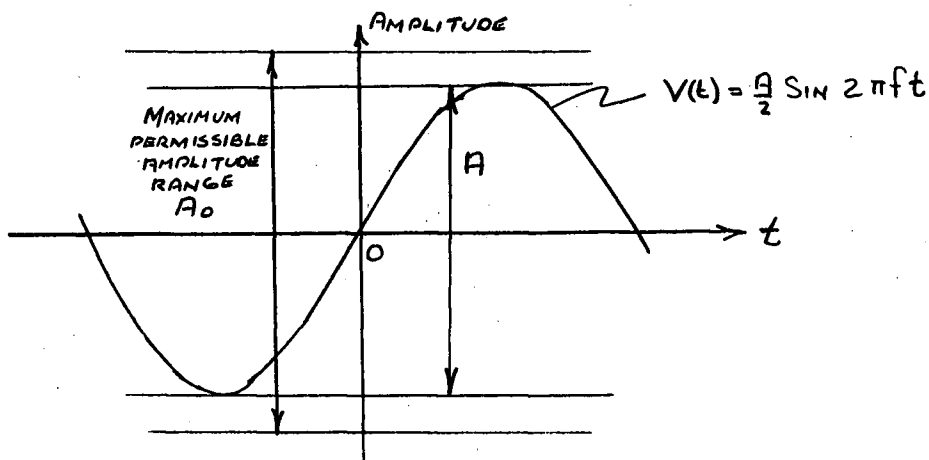
Figure A-1.1   Assumed Form of Input Signals

For the purpose of analysis, assume sine-wave type input signals. The greatest slope of the curve occurs at the zero axis crossings. Therefore, the greatest change in amplitude occurring within one cycle occurs over an interval centering about the zero axis crossing.

Consider the input to the coder to be composed of voice signals ranging from zero to 4000 cps. The input voice signals are sampled at the Nyquist rate of twice the maximum frequency of the input or 8000 times per second. Therefore, the interval between samples is $1/8000$ seconds $= 125 \ (10^{-6})$ seconds $= 125$ microseconds.

The input signals are of the form

$$V(t) = A/2 \ \text{Sin} \ (2\pi f t)$$

as illustrated in Figure A-1.1. The greatest slope in the
waveform occurs at $t = 0, 1/2f, 1/f$, etc. For example, at
$t = 0$, it is necessary to find the amplitude range A such
that the difference in amplitude between $t = -62.5$ and
$t = + 62.5$ microseconds does not exceed $A_0/2$. Hence, the
boundary condition on $V(t)$ is that

$$V(t) = A_0/4 \text{ at } t = 62.5 \text{ microseconds.}$$

That is, the maximum permissible signal amplitude A_m, such
that the difference between two succesive samples 125
microseconds apart does not exceed $A_0/2$ is given by

$$V(t) = A_m/2 \text{ Sin } 2\pi f(62.5 \times 10^{-6}) = A_0/4$$

or

$$A_m = \frac{A_0}{2 \text{ Sin } \pi f/8000}$$

where f = frequency in cps.
For example, at $f = 4000$ cps,

$$A_m = \frac{A_0}{2 \text{ Sin } \pi/2} = A_0/2$$

The results for other frequencies were evaluated and tabulated
in Table A-1.1.

Frequency (cps)	Maximum permissible signal amplitude A_m (p-p)
0 – 1333	A_0
1500	$0.906\ A_0$
2000	$0.707\ A_0$
2500	$0.600\ A_0$
3000	$0.541\ A_0$
3500	$0.510\ A_0$
4000	$0.500\ A_0$

Table A-1.1 Table of Frequencies of Input Signals and Corresponding Signal Amplitudes

APPENDIX 2

Circuit Details of the Decoder.

The decoder is, on the whole, a collection of standard transistor circuits.

The circuit diagrams of the decoder, Figures A-2.1 to A-2.9, are self-explanatory. Figures A-2.10 and A-2.11 illustrate the timing waveforms and waveforms of an example decoding operation. Figure A-2.12 illustrates the waveforms that result from detection of a framing error.

Timing of the circuit operations is important and, because of this, it was necessary to delay various waveforms using monostable multivibrators. Delay lines were out of the question because of the length of delays required.

Note that the decoder can be adjusted to detect the incoming code pulses at the level of one-half the pulse height. This reduces the effect of the interference in the transmission channel, the peaks of which are assumed to be usually considerably less than one-half the pulse height.

Pulse timing is achieved by having the incoming pulses pull an oscillator into phase. But note that the actual synchronization is carried out by the delay monostable in Figure A-2.1. This ensures that interference in the transmission channel does not affect the timing operations of the decoder.

Circuit data for CG1 only are given in Figure A-2.4. Data for the remaining current generators, which are identical in form to CG1 are given in Table A-2.1.

Current Generator	AND Gate Inputs: Pulse regenerator and counter taps (see Fig. A-2.3):	Emitter Resistors (ohms)	
		Fixed	Variable
CG1	2, 3, 6	68	100
CG2	1, 4, 6	168	100
CG3	2, 4, 6	500	100
CG4	1, 3, 5	680	1K
CG5	2, 3, 5	1.5K	1K
CG6	1, 4, 5	3.3K	1K
CG7	2, 4, 5	8.2K	1K

Table A-2.1 Data for Current Generators
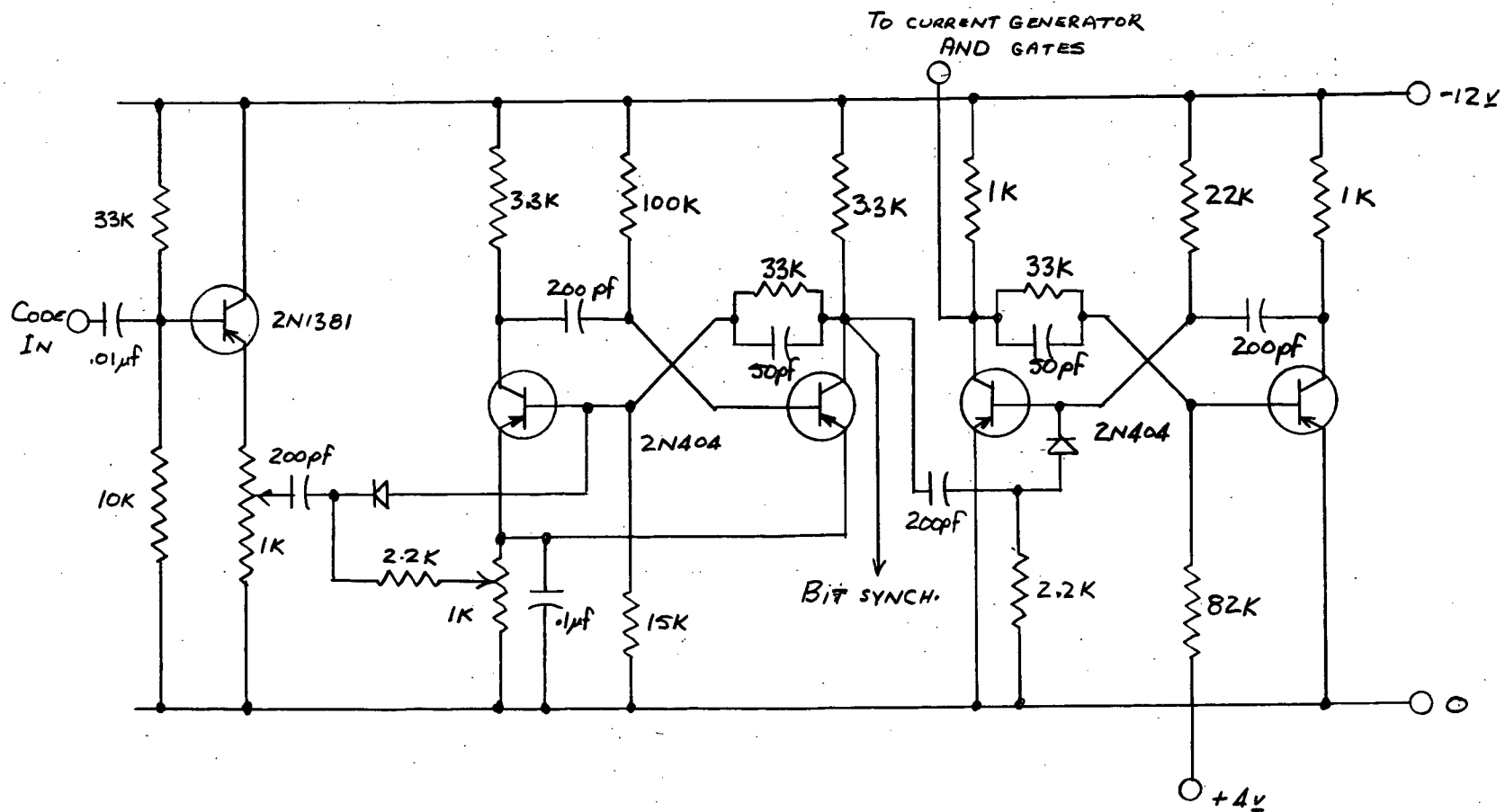
Figure A-2.1   Input Amplifier, Delay Monostable and Pulse Generator

Resistors: ½w, 10%   Capacitors: 75v, 10%   Diodes: 1N497
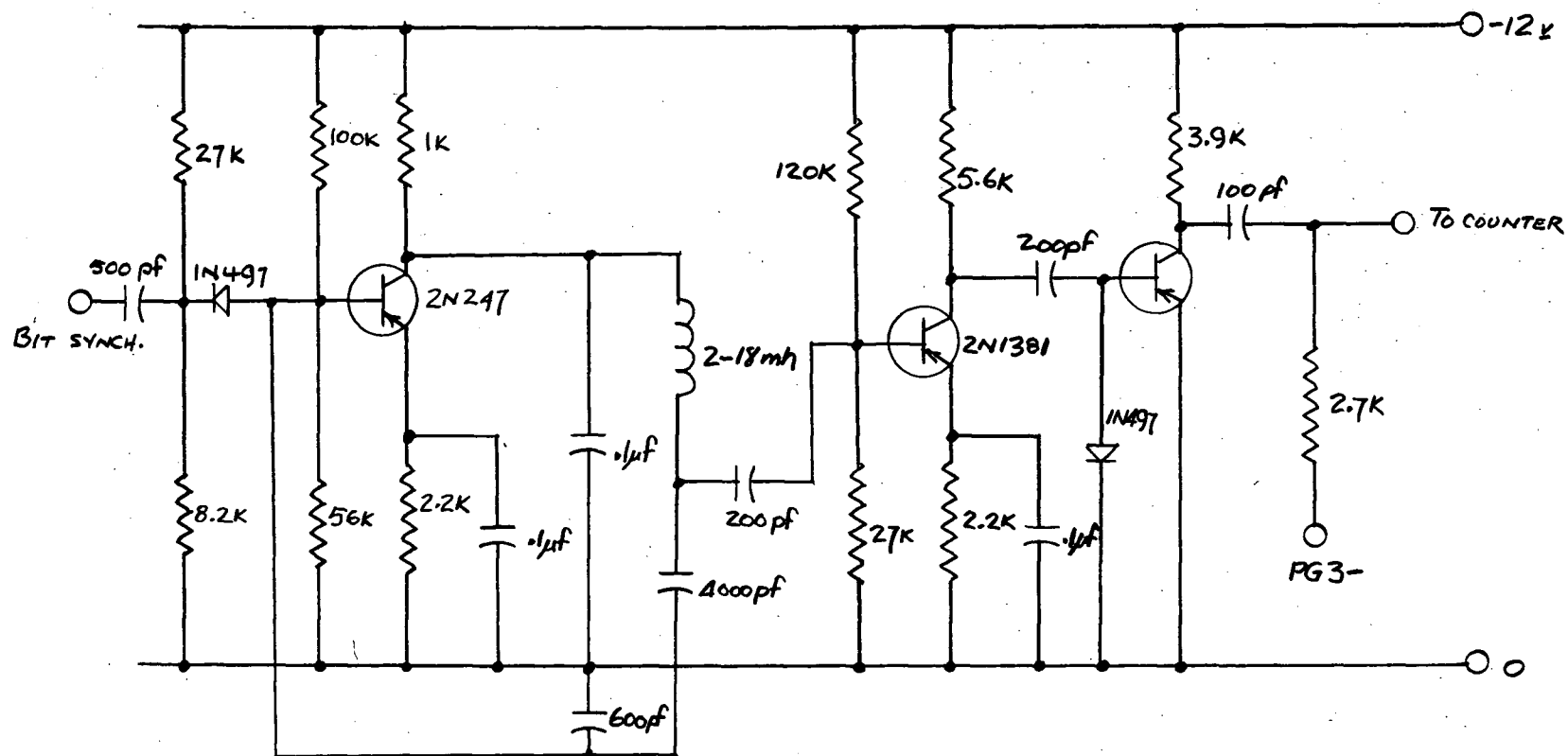
Resistors: ½w, 10%   Capacitors: 75v, 10%

Figure A-2.2 Driven Oscillator, Amplifier and Square Wave
              Generator

Figure A-2.3   Count-Down-By-Seven Counter
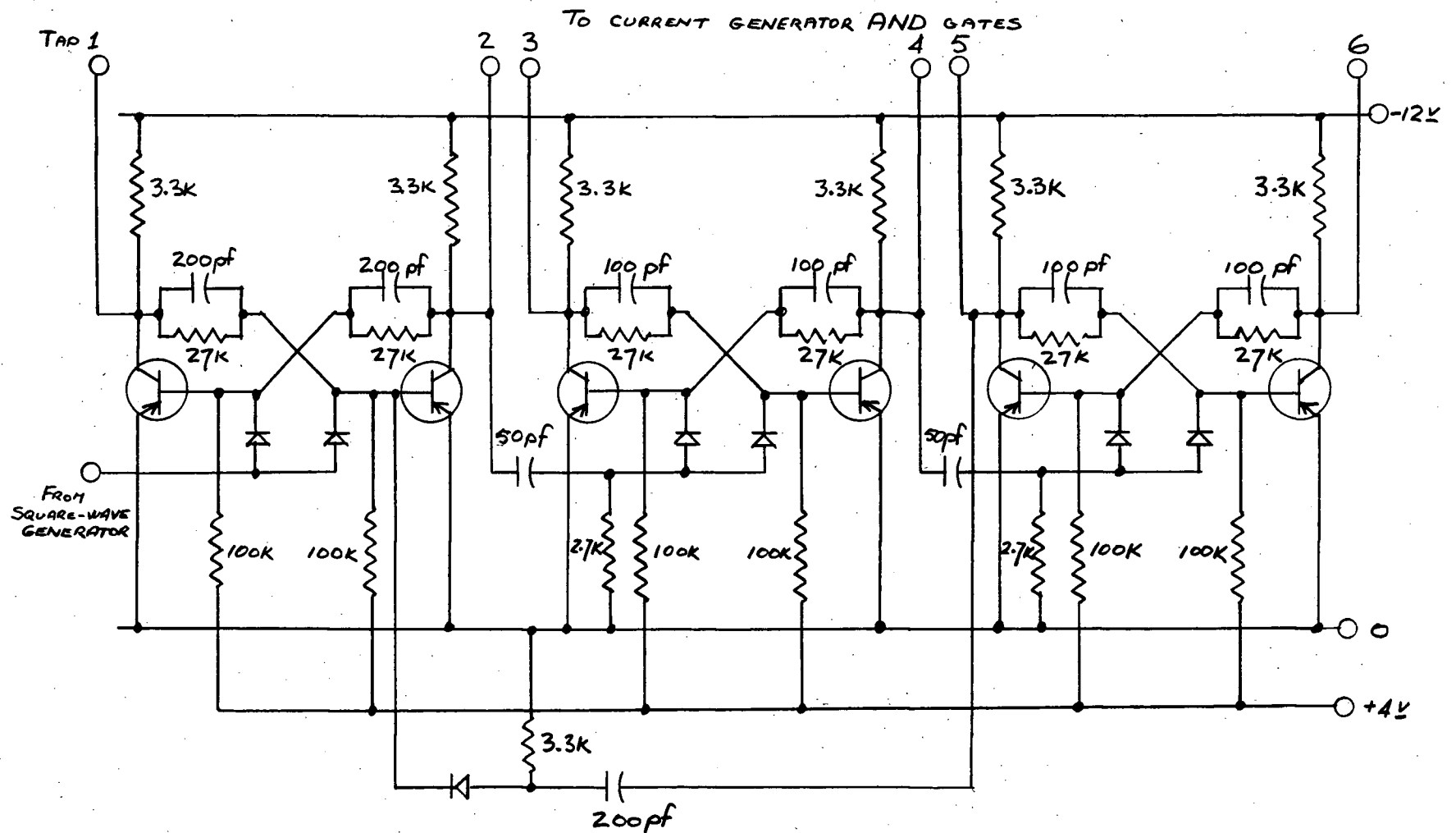
Resistors: ½w, 10%   Capacitors: 75v, 10%   Transistors: 2N404   Diodes: 1N497
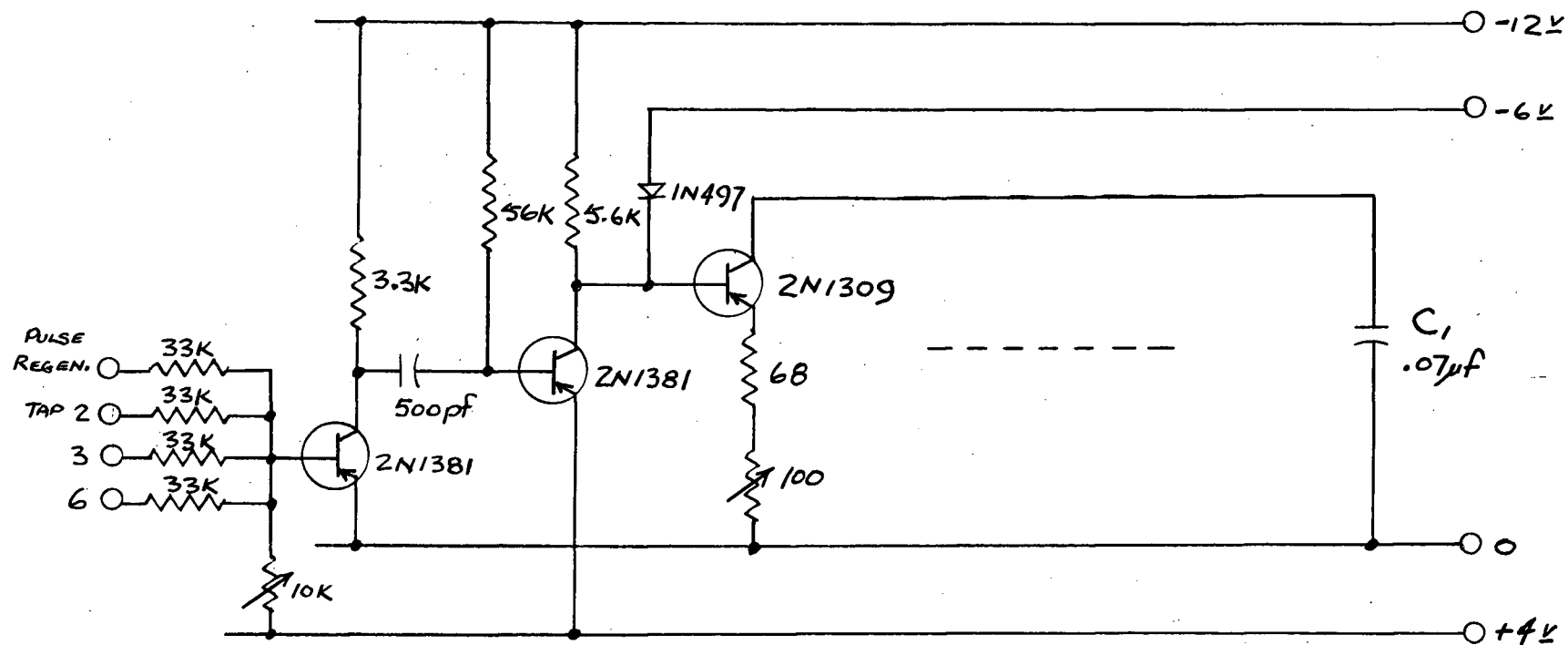
Resistors: ½w, 10%   Capacitors: 75v, 10%

Figure A-2.4   Current Generator CG1 and Storage Capacitor C_1

Resistors: ½w, 10%   Capacitors: 75v, 10%   Resistors: ½w, 10%   Capacitors: 75v, 10%

Figure A-2.5 Charge Transfer Gate   Figure A-2.6 Discharge Gate
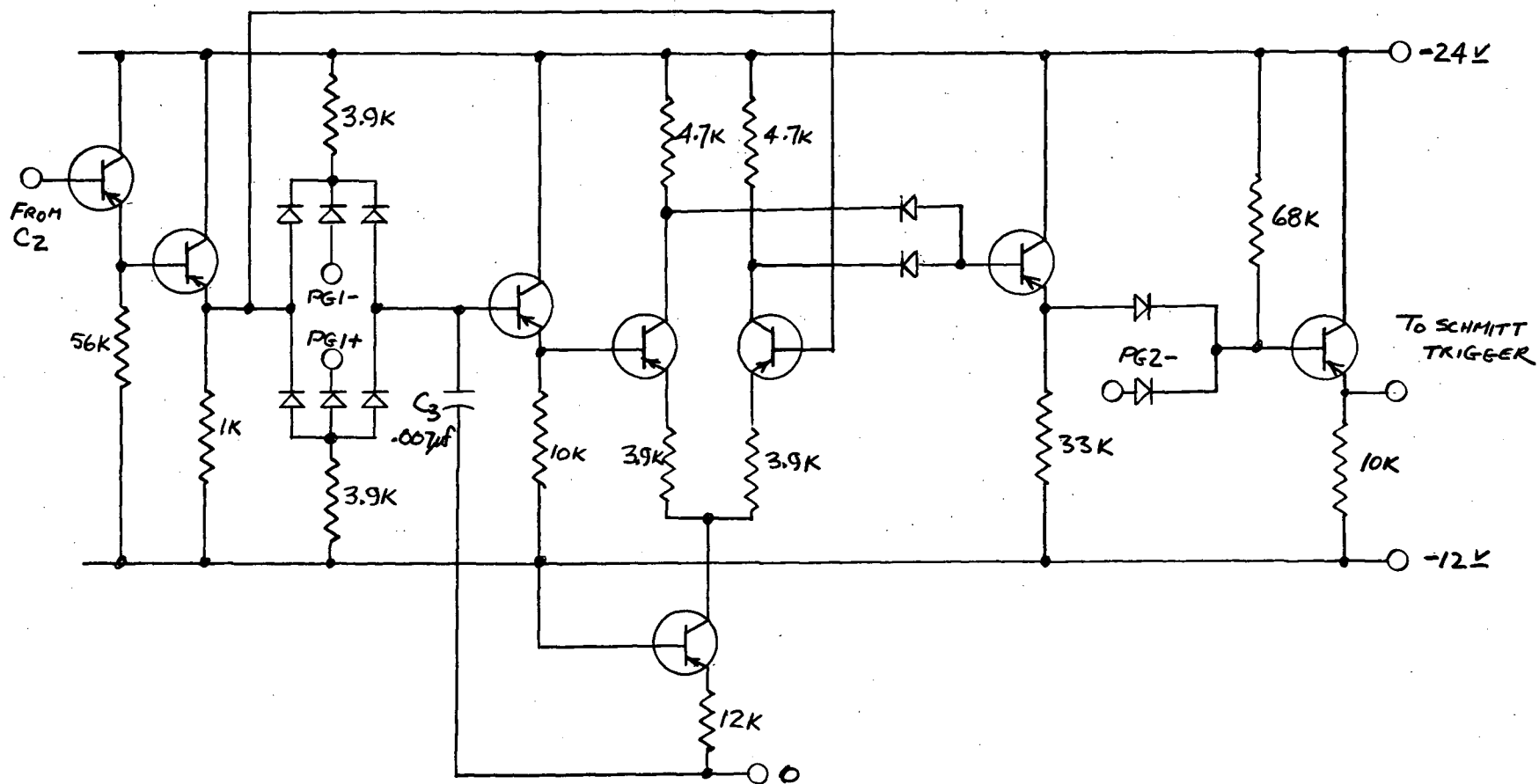
Resistors: $\frac{1}{2}$w, 10%   Capacitors: 75v, 10%   Diodes: 1N497   Transistors: 1N1381

Figure A-2.7   Lewis Gate, Voltage Comparator, and Diode Gate
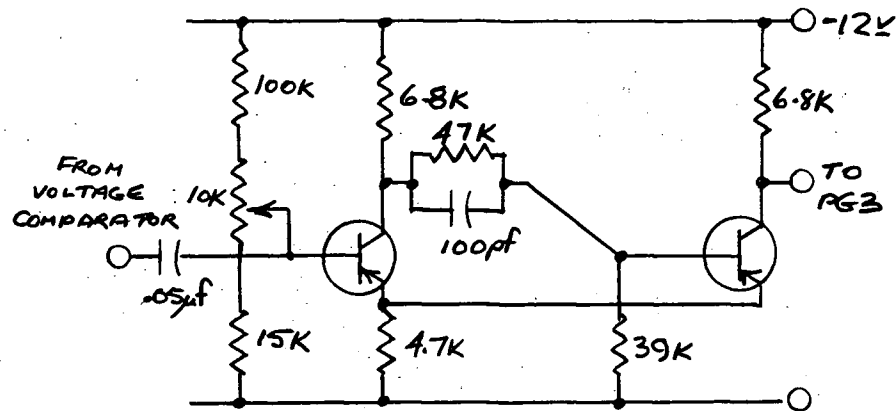
(a.) SCHMITT TRIGGER
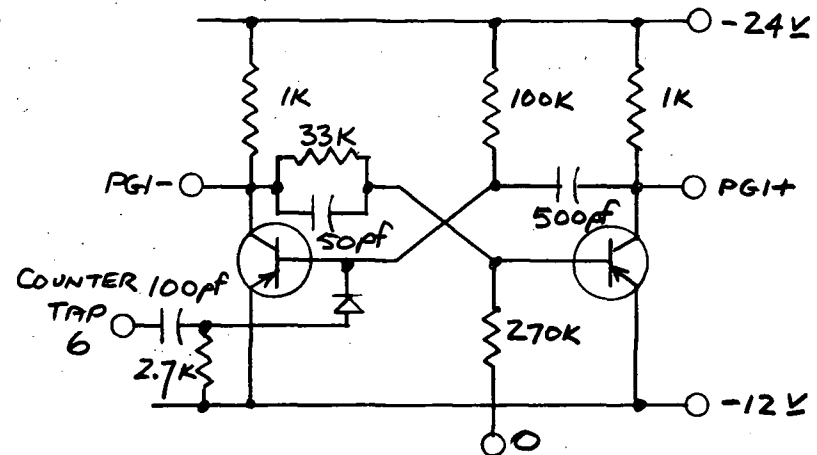
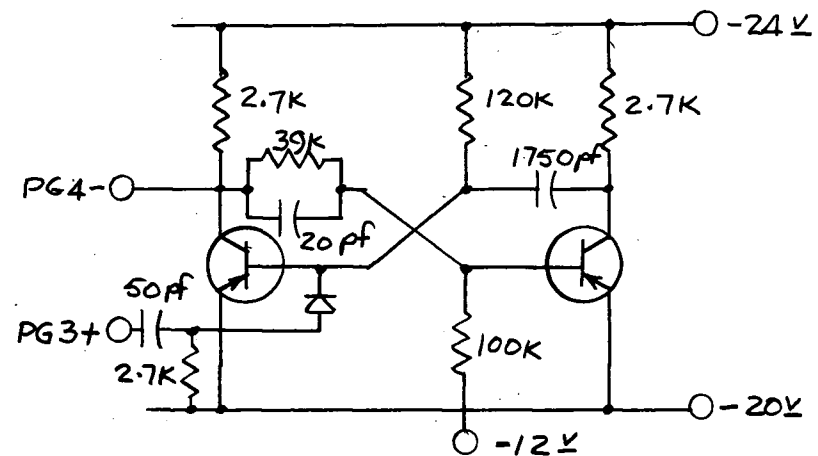(b) LEWIS GATE PULSE GENERATOR (PG1)
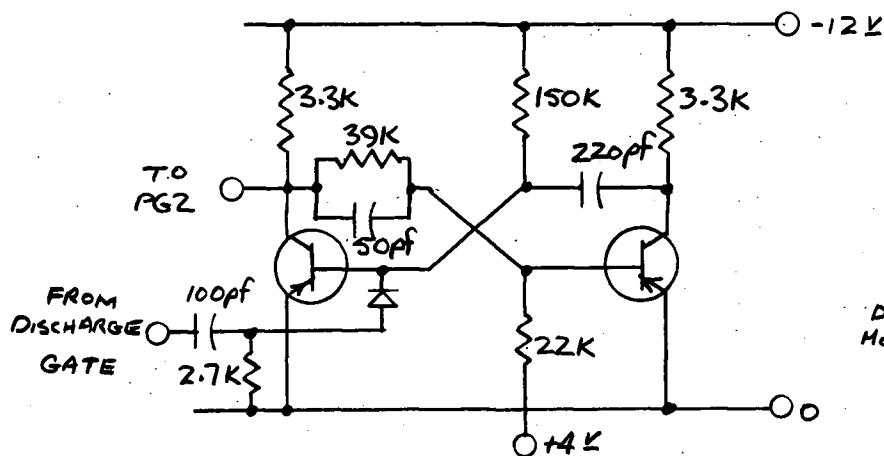
(c) DELAY MONOSTABLE FOR PG2
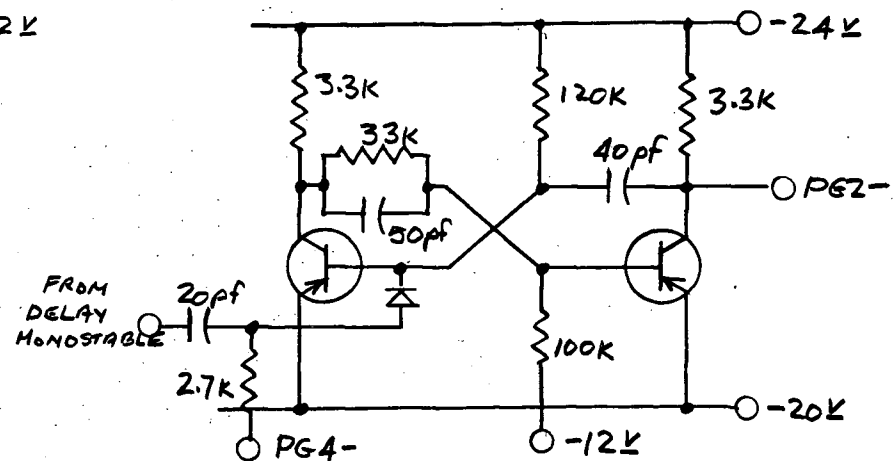
(d) PULSE GENERATOR FOR DIODE GATE (PG2)

Resistors: ½w, 10%   Capacitors: 75v, 10%   Transistors: 2N1381   Diodes: 1N497

Figure A-2.8   (a) Schmitt Trigger (b) PG1 (c) Delay Monostable for PG2 (d) PG2
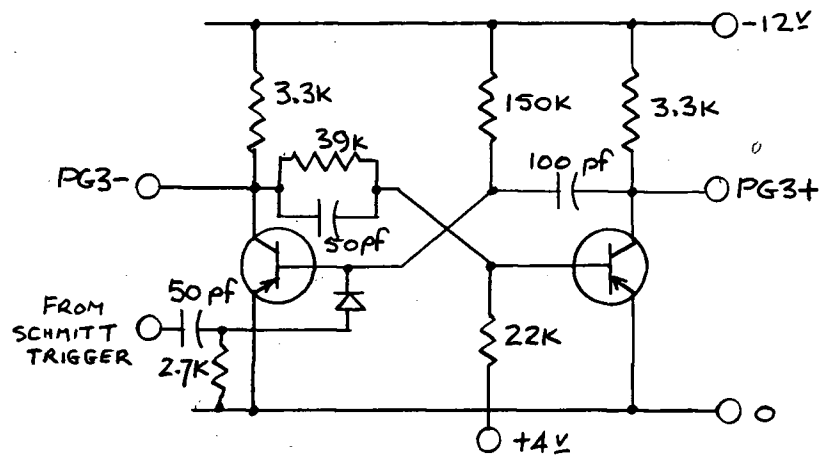
(a) COUNT INHIBIT PULSE GENERATOR (PG3)   (b) DIODE GATE INHIBIT PULSE GENERATOR (PG4)

Resistors: $\frac{1}{2}$w, 10%   Capacitors: 75v, 10%   Transistors: 2N1381   Diodes: 1N497
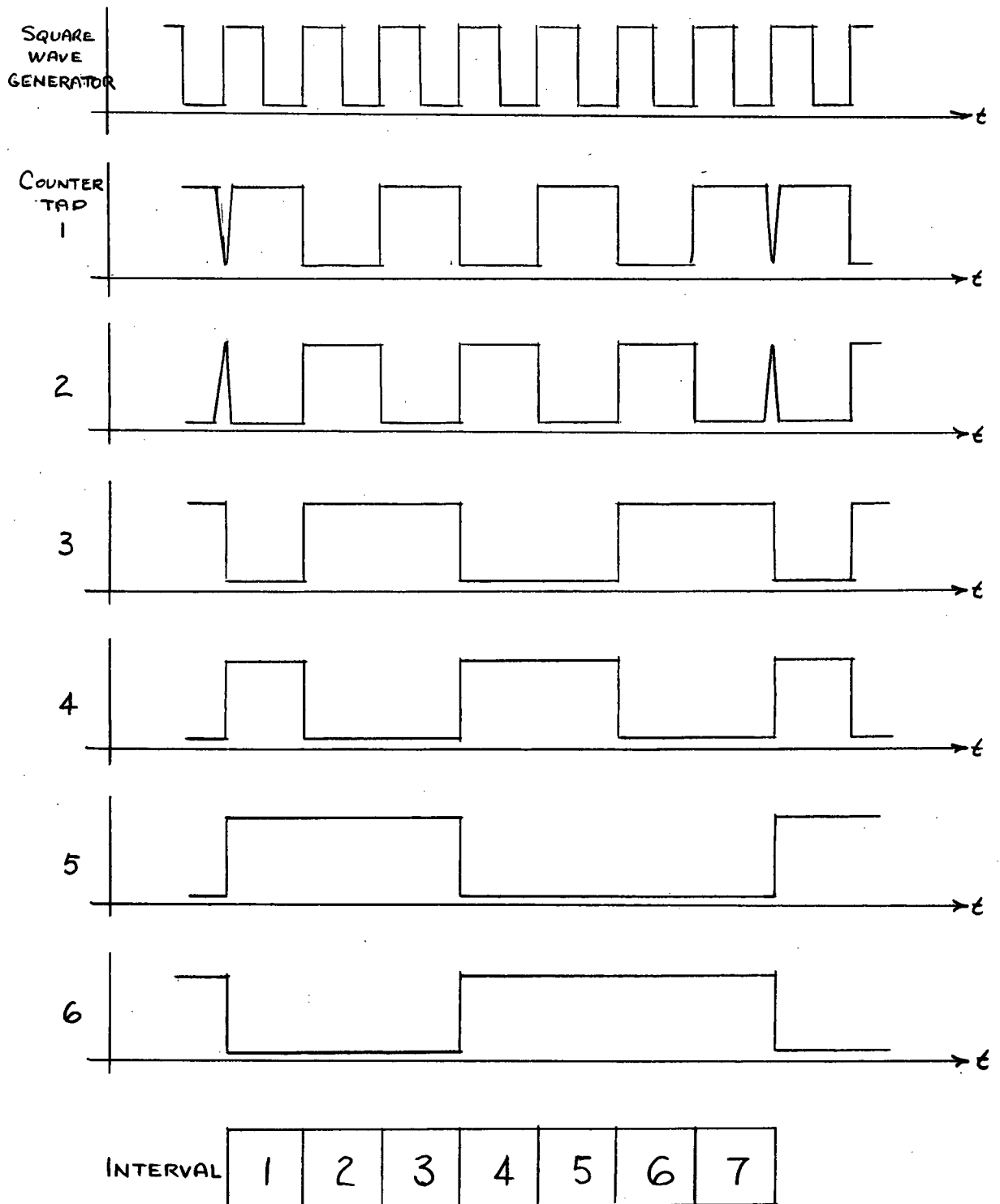
Figure A-2.9   Pulse Generators: (a) PG3 (b) PG4

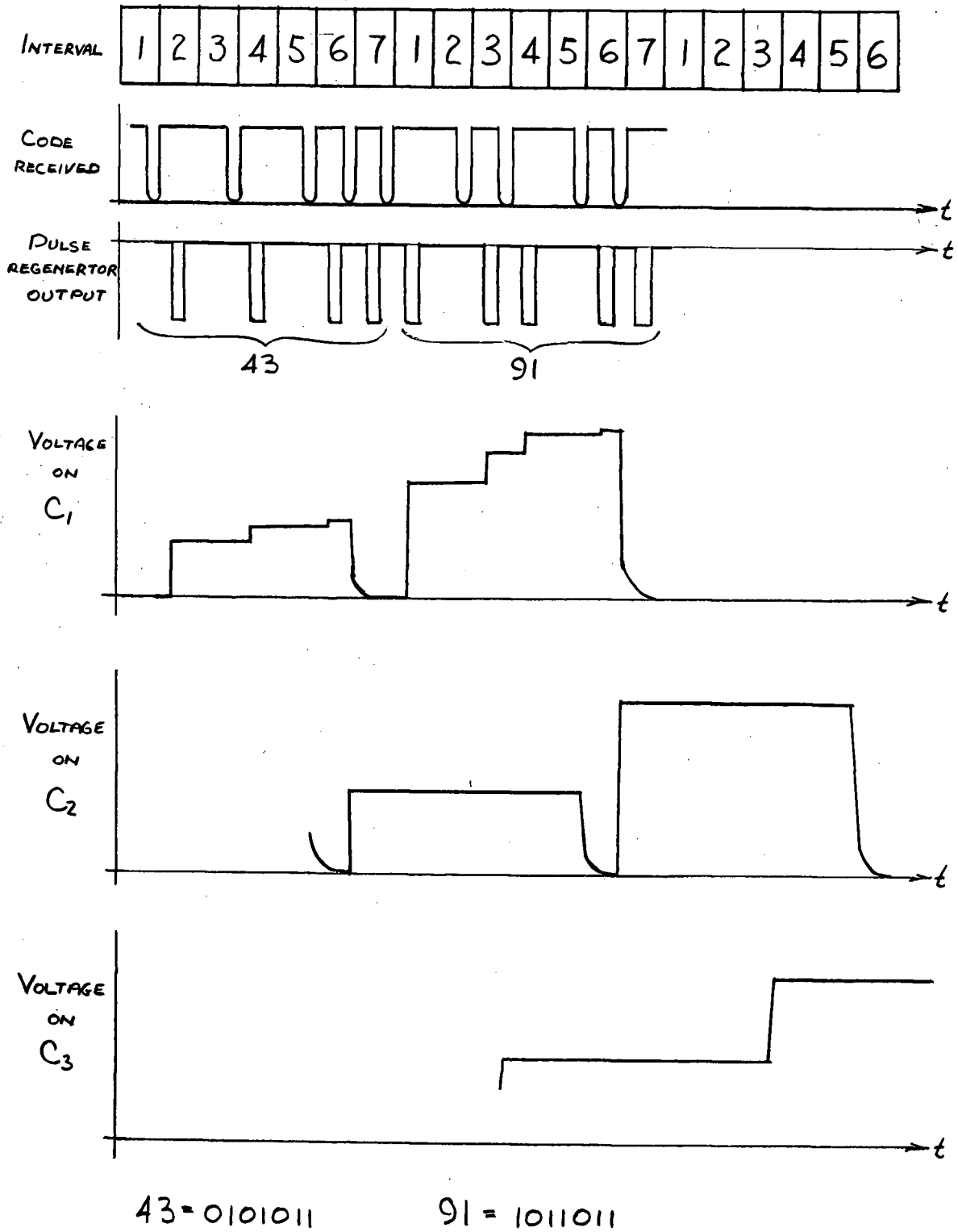Figure A-2.10   Counter Waveforms and Intervals Defined

Figure A-2.11   Waveforms on C_1, C_2, C_3 Due to Received Values of 43 and 91
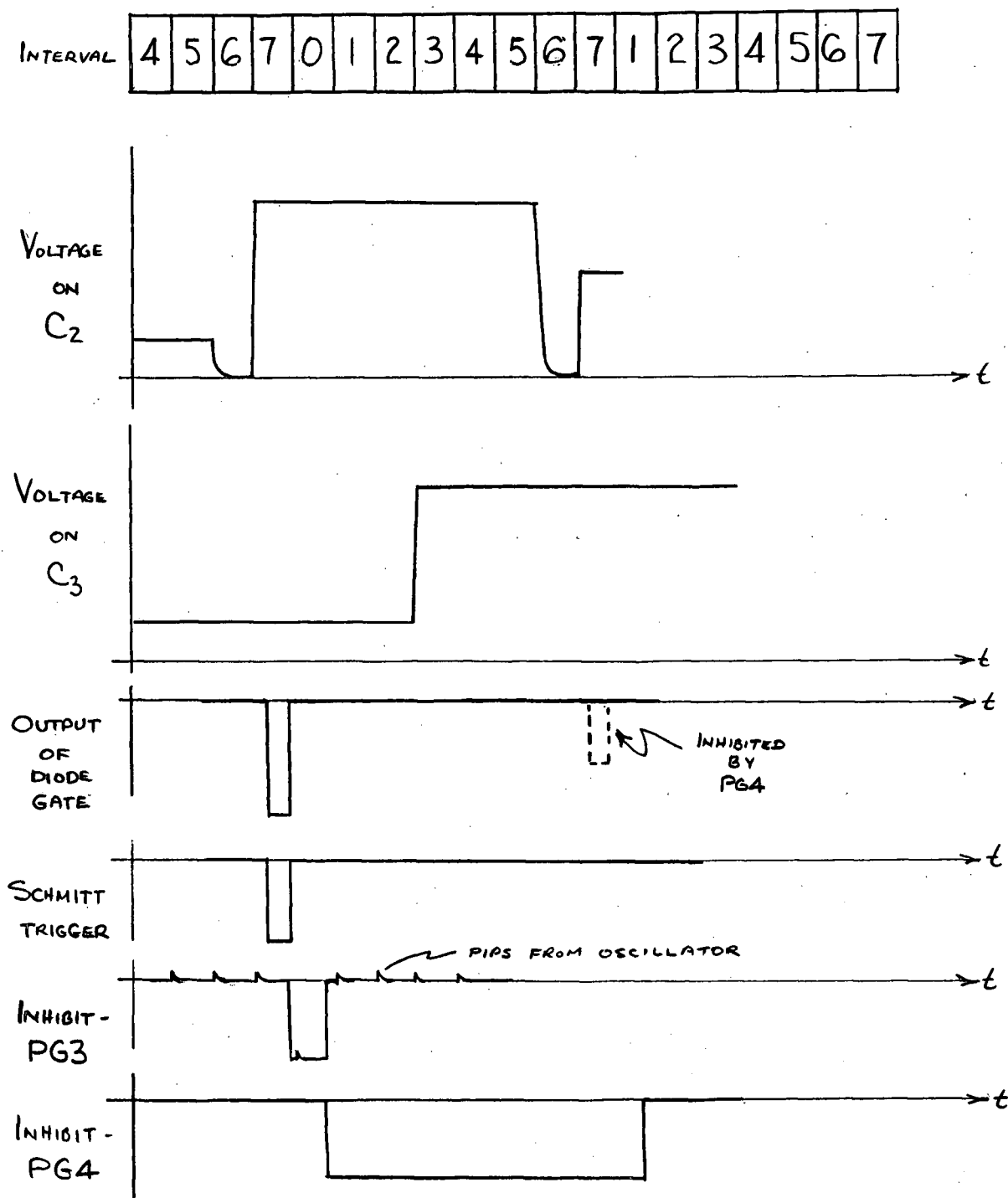
Figure A-2.12 Framing Circuit Waveforms Due to Decoded Values of 20 and 91. Comparison Carried Out During Interval 7; Interval 0 Indicates Shift

APPENDIX 3

Circuit Details of the Coder.

Extensive modifications were carried out on the coder designed and constructed by Hafer[10] to improve and adapt its operation to the operation of the decoder. There were many minor changes but the major changes are the following:

1. The number of digits per code group was changed from six to seven. This change resulted in a twofold increase in the number of levels, from 64 to 128, and required a twofold increase in accuracy of operation.

2. Extensive changes were made in the timing circuits in order to accommodate the increase in the number of digits per code group. The basic clock frequency was increased from 48 kc/s to 56 kc/s and the frequency divider was changed from a 6:1 device to a 7:1 device. Also, most of the delay lines used in Hafer's circuit were replaced by delay monostable multivibrators for greater stability and accuracy.

3. The circuit voltage levels were changed and some were added to adapt the circuit to operation using standard 12 volt storage batteries.

4. A second Schmitt trigger was added in cascade to reduce the effects of the "maybe" pulses that result when a pulse of height near the firing level is applied to the first Schmitt.

5. Transistors in the "on" condition were placed in series with the charge transfer transistors to reduce the effects of

voltage feedback due to a finite reverse impedance ratio. The addition of the second transistor increases the reverse impedance ratio and thus reduces any voltage feedback effects.

6. A change in the charge transfer gating arrangements was made to improve the shape of the recirculated pulses. This change required an additional gating pulse generator (GP2d).

The final circuits are illustrated in Figures A-3.1 to A-3.4 and some timing waveforms are given in Figure A-3.5. Details of the circuit operation are given in Reference 10 and apply to the final circuit as given here except for the additional operational details brought about by the above modifications.

(a) MASTER CLOCK   (b) FREQUENCY DIVIDER

(c) GPl   (d) DELAY MONOSTABLE   (e) GPld
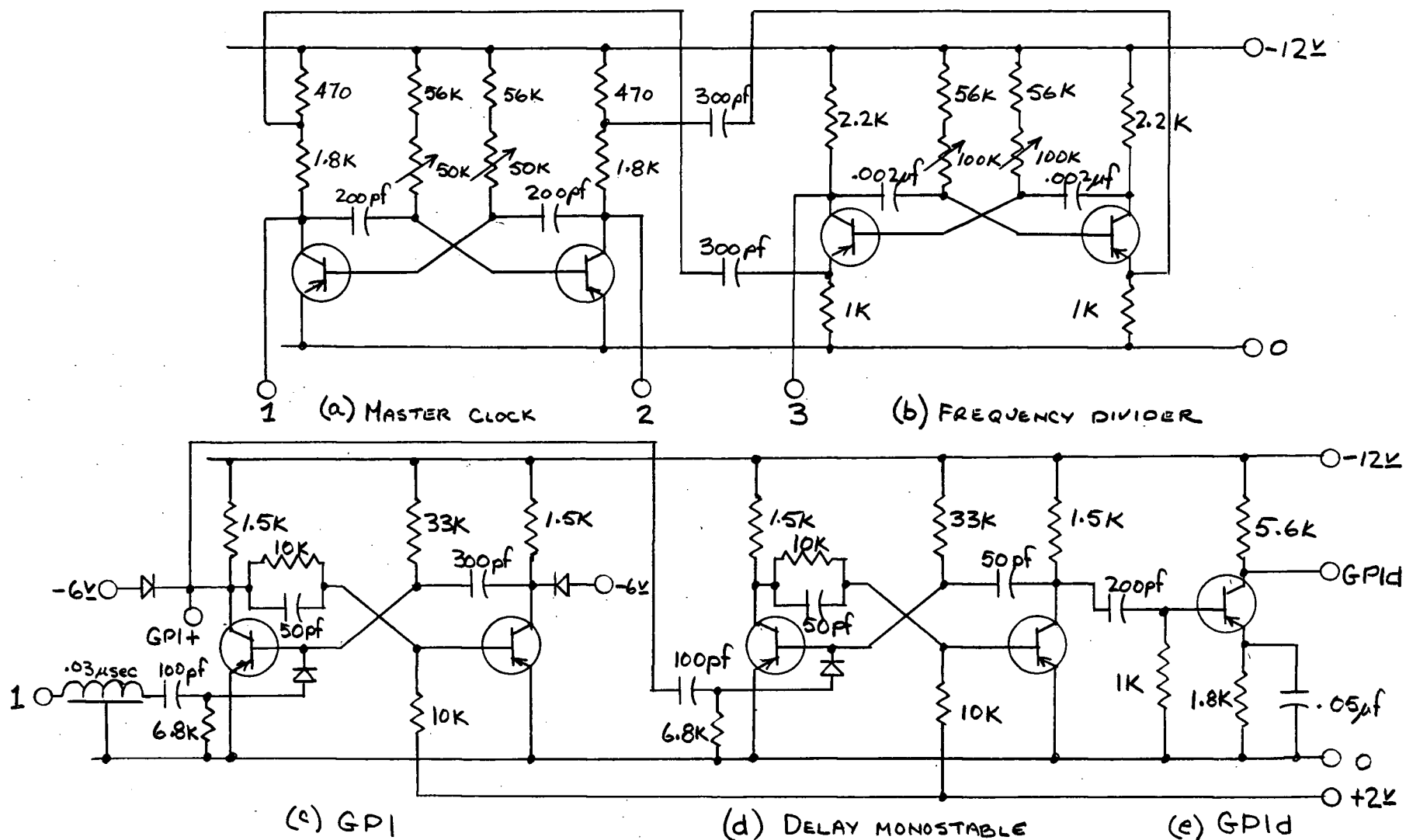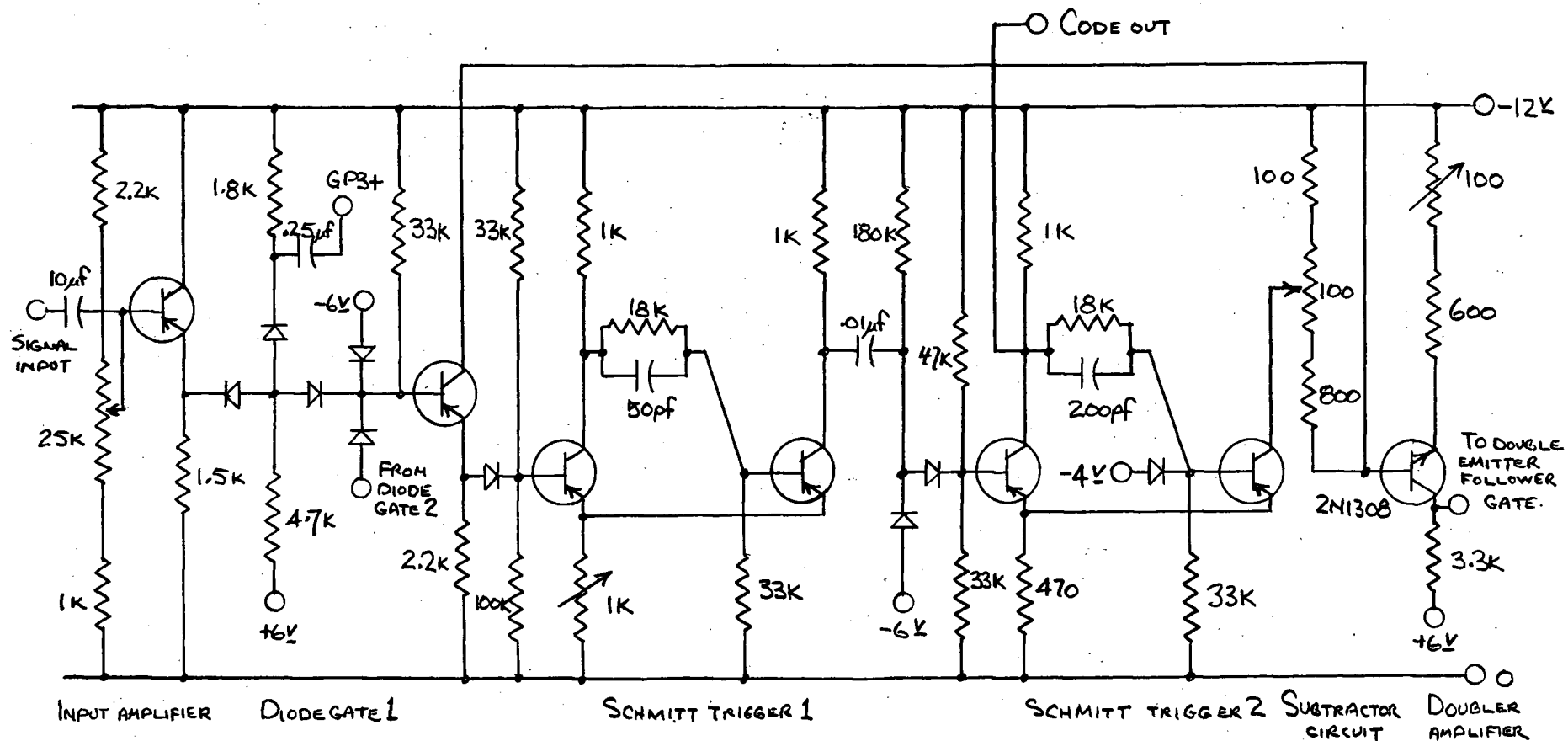
Resistors: ½w, 10%   Capacitors: 75v, 10%   Transistors: 2N1309   Diodes: 1N497

Figure A-3.1   (a)   Master Clock (b)   Frequency Divider (c)   GPl (d)   Delay Monostable
(e)   GPld
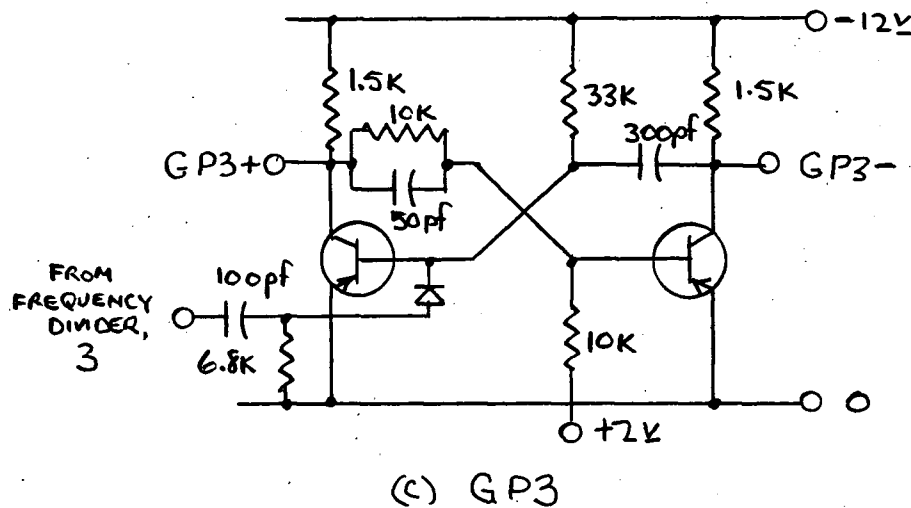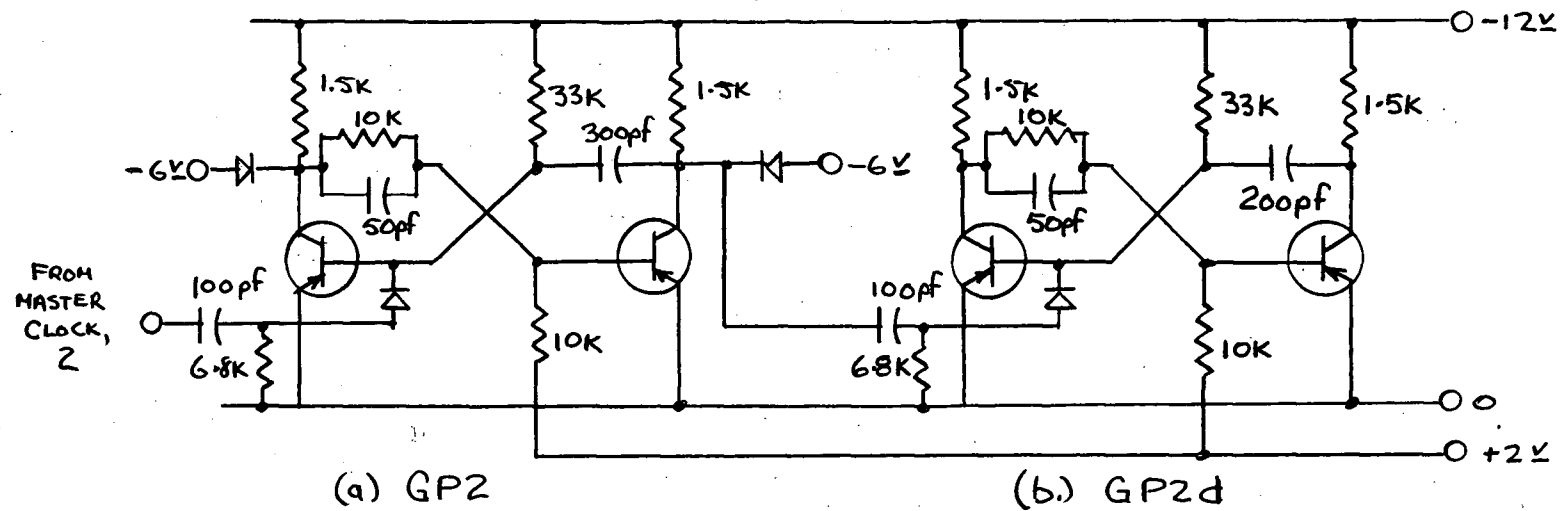
Figure A-3.2 Pulse Generators: (a) GP2; (b) GP2d; (c) GP3

Resistors: $\frac{1}{2}$w, 10%   Capacitors: 75v, 10%   Transistors: 2N1309   Diodes: 1N497

Figure **A-3.3** Input Amplifier, Diode Gate 1, Schmitt Triggers, Subtractor and Voltage Doubler Amplifier

Resistors: $\frac{1}{2}$w, 10% Capacitors: 75v, 10% Diodes: 1N497, 1N34 Transistors: 2N1309 unless otherwise noted

Resistors: $\frac{1}{2}$w, 10%   Capacitors: ..., 10%   Transistors: 2N1309, 2N1381   Diodes: 1N497

Figure A-3.4   Double Emitter Follower Gate, Charge Transfer Circuits, Double Emitter
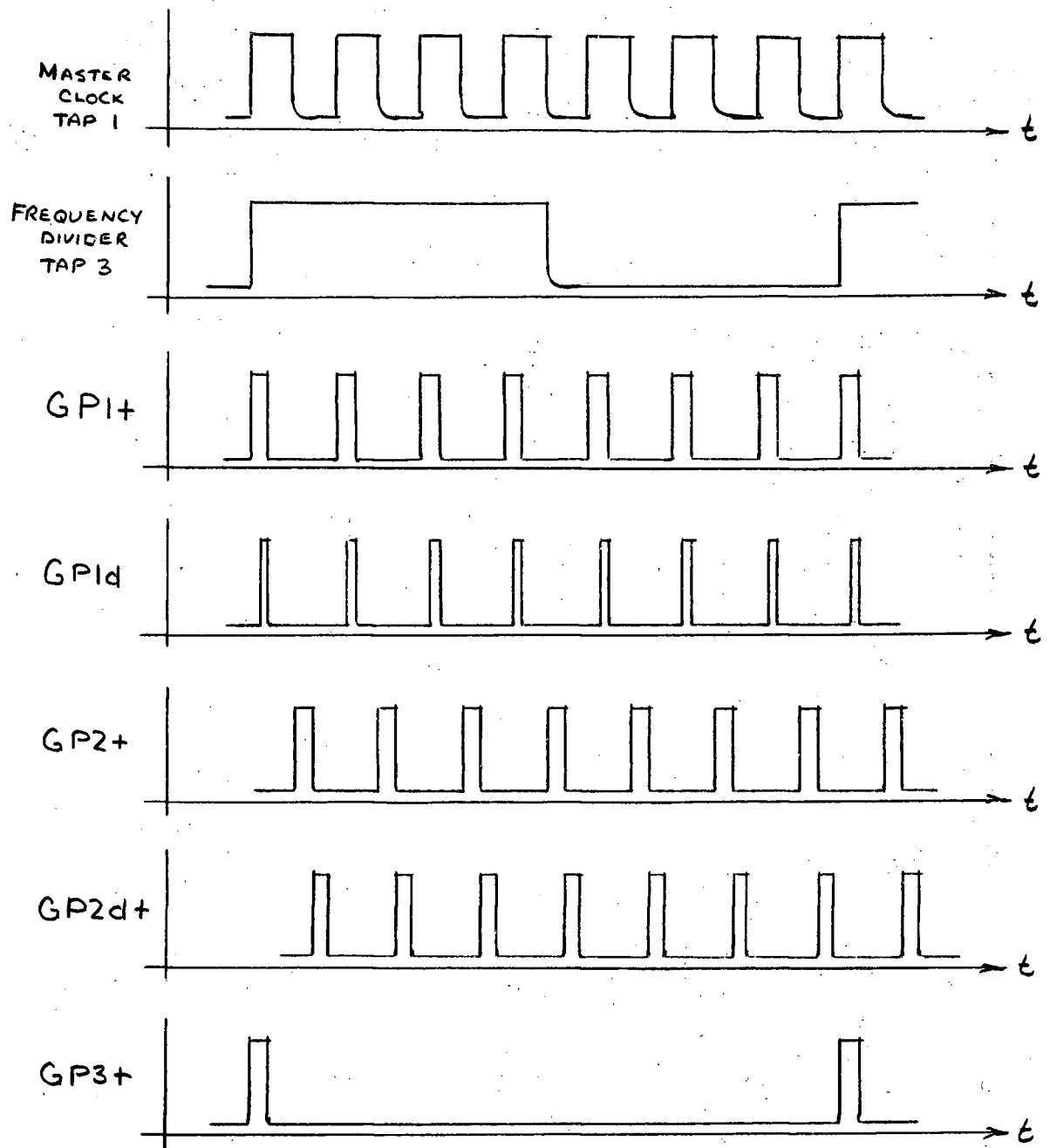Follower, Diode Gate 2

Figure A-3.5 Coder Timing Waveforms

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