AN INTEGRATOR FOR A PULSE-POSITION-MODULATION ANALOGUE COMPUTER

by

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Abstract

This thesis discusses the design of the basic circuits for an integrator for a pulse-position-modulation analogue computer. The computer operates on a time-sequential principle, utilizing a magnetic drum memory. In the integrator, pulse information from the drum is translated into a voltage by a sweep circuit. The information is integrated using pulse techniques and put back into pulse form to be rewritten on the magnetic drum.

In the prototype integrator, the method of integration is a simple straight-line projection of the first derivative according to the equation $y = \frac{dy}{dt} \Delta t$. The integration will therefore have rather poor accuracy, but theoretically any desired accuracy can be achieved by simply extending the circuits developed in this thesis to include higher-order derivatives. Recommendations for the construction of a final prototype integrator are made at the end of the report.

The circuits used are an ac-coupled sweep amplifier, an accurate voltage comparator, and standard flip-flops and gating circuits. Tests were performed which indicate the reliability of these circuits for accurate integration.

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AN INTEGRATOR FOR A PULSE-POSITION-MODULATION ANALOGUE COMPUTER

1. Introduction

The advent of specialized electronic computers has produced several distinct types of integrators. Digital computers are basically pulse-counting systems, capable of high-speed operation and adapted to a repetitive form of calculation. Integration in digital computers requires the application of a converging integrating formula, such as the formula of Simpson or Gauss, to the ordinary arithmetic circuits.[13] Analogue computers, on the other hand, use a number of basic components to form either a direct or an indirect electrical analogy to the physical problem.[6] Integration is performed in a separate integrator unit by electronic, electromechanical or mechanical means, each method having its special advantages. The main difference between analogue and digital computers is that the analogue type uses a number of basic components to simulate the problem in real time, whereas the digital type uses one set of arithmetic circuits and a storage unit to perform all operations in time-sequence.

In recent years the application of digital pulse techniques to analogue systems has given rise to a hybrid-type computer. One such computer, being built at the University of British Columbia, is known as a time-sequential, pulse-position-modulation analogue computer. As the name implies, this design embodies both the time-sequential principle of operation of the

purely digital computer, and the indirect-analogy approach of the electronic analogue computer. Although it is an analogue computer, this unit may be quite easily interconnected with a digital computer because the data is already in pulse form. Circuits are required which will convert the pulse data of the analogue computer to the binary system of representation used in digital computers. This thesis discusses the design of an integrator for the pulse-position modulation analogue computer.

Analogue computers feature several basic types of integrators. The classic example of a mechanical integrator is the Kelvin wheel-and-disk type,[14] which was used in the first electromechanical differential analyzer, built by Bush at the Masschussets Institute of Technology in 1931.[2] This integrator was improved by Berry[1,2] in 1944 by the addition of a polarized-light follow-up servo link which enabled a large output torque to be developed without loading the delicate integrator wheel. Thus the Kelvin integrator became an electromechanical rather than a purely mechanical device. During World War II the electronic operational amplifier became popular as a basic unit of analogue computers. It was pioneered by Philbrick and Lovell, and has since become almost universally accepted in the form of a plug-in unit.[12] Since the operational amplifier is of specific interest here, it will now be considered in more detail.

The electronic operational amplifier is usually a high-gain direct-coupled amplifier. Used as in integrator, it requires only negative capacitive feedback and a precision input resistor for accurate high-speed operation. It can also be used in

conjunction with servo-driven potentiometers as an integrator for an electromechanical analogue computer, which is the modern equivalent of the mechanical differential analyzer. Some of the requirements of operational amplifiers used in conventional systems are listed:[8]

(i) Since variables are represented by voltages, the amplifier must generate voltages of either polarity to simulate either mathematical sign.

(ii) It must invert so that negative feedback can be used.

(iii) It must have high gain and low phase shift within the frequency range of problems to be studied, as well as a good margin of stability when a large amount of negative feedback is used. The useful gain may vary from 50,000 to 500,000 at very low frequencies.

(iv) It must have a high input-impedance so that grid current is neglible compared with signal current.

(v) It must have low zero-drift. That is, with no feedback and in the absence of signal, the output must remain at zero volts. Practical figures for zero-drift range from 10's of millivolts per hour to 100's of microvolts per month.

The following problems arise because of factors other than inaccuracies in the amplifier itself:[5]

(vi) Errors in integration are accentuated by long computer runs. The error in an input signal appears at the output multiplied by the time of integration if the error is a constant, or integrated over the time of integration if the error is a function of time.

(vii) Slowly-varying outputs of integrators are invariably associated with low input voltages and often with low input potentiometer settings in the problem. A low setting leads to a greater percentage error than a setting near full-scale of the potentiometer.

(viii) High frequencies contribute to phase shift in the amplifier and have the same effect as negative damping. Servo devices used for multiplication operate satisfactorily only at quite low frequencies.

(ix) The dynamics of recording devices must be considered so that the recorder response does not affect the recording.

These are a few of the major problems encountered in the design of an operational-amplifier type analogue integrator. The best accuracy obtainable in present computers using these units is in the order of 0.01% error. Because of the physical difficulty of obtaining accurate problem data, this figure is perfectly acceptable for many engineering problems.

The integrator to be discussed uses some of the techniques of both analogue and digital systems. The solution of an ordinary differential equation with variable coefficients is carried out in a digital manner; that is, a recurring calculation is performed using only one basic integrator unit. At the same time, the integrator is built of operational units common to an analogue system, so that some of the versatility, simplicity of operation and ease of programming of an analogue system is preserved. The prototype integrator has been greatly simplified and is expected to have a percentage error of no better than 1%. If required, better accuracy probably can be attained by a simple extension of the principle of operation outlined in this thesis. The present amplifier design meets the following specifications:

(i) Since the output voltage does not directly represent a variable in the time-sequential system to be outlined, the amplifier need generate only positive voltages. Therefore amplifier drift is minimized because ordinary diode clamps can be employed to establish stable quiescent conditions.

(ii) Inversion is accomplished using one inverting stage and one non-inverting stage.

(iii) For 1 percent accuracy, a gain of approximately 3500 suffices. Since the integrating action is repetitive and fairly fast, this gain is required only near the frequency of 1000 cps, and consequently the amplifier can be ac-coupled.

(iv) Zero drift is eliminated so long as the amplifier remains stable with no signal applied. The present design satisfies this requirement.

(v) The time of application of the input signal determines the amplifier output voltage, because the input signal is standardized. The duration of the input signal depends upon the pulse trigger circuits, and these only require a stable power supply for reliable operation. The power supply used[4] is chopper stabilized to within a few millivolts of ±300 volts. The overall accuracy of the integrator can likely be made consistent with that of the other arithmetic circuits.[11]

It is evident that this integrator design is not an improvement on existing designs, but rather a special simplified adaptation of operational amplifiers to the hybrid-type computer. It is hoped that with modifications the basic units discussed herein will perform equally as well as more costly units in existing analogue computers.

2. General Description of the Computer

2-1. Block-Time Solution of the Basic Equation.

The computer design equation is the following ordinary differential equation having variable coefficients:

$$\frac{d^n y}{dt^n} + f_1 \frac{d^{n-1} y}{dt^{n-1}} + \ldots + f_{n-1} \frac{dy}{dt} + f_n y = g(t), \quad \text{or} \qquad (1)$$

$$y^{(n)} + f_1 y^{(n-1)} + \ldots + f_{n-1} y^{(1)} + f_n y = g(t)$$

The computer solves the equation by repeated integration using the same set of basic components for each operation. Assuming that a set of initial conditions is known at time t_o, the procedure will be as follows: first, an integration is performed using the two highest-order derivatives according to the equation:

$$y^{(n-1)}(t_o + dt) = y^{(n-1)}(t_o) + y^{(n)}(t_o)dt \qquad (2)$$

Time dt is the simulated time for one incremental integration in the computer. It is related to real time by the speed at which the computer solves the equation. In the next interval of time dt, the next-lowest derivative is found in a similar operation:

$$y^{(n-2)}(t_o + dt) = y^{(n-2)}(t_o) + y^{(n-1)}(t_o + dt)dt \qquad (3)$$

Notice that these two equations differ slightly in that equation (2) contains the highest-order derivative evaluated at time t_o, whereas equation (3) contains the highest-order derivative evaluated at time $t_o + dt$. The reason for this will become apparent in the following description. As it happens, the difference in the final result caused by the assumption made in equation (2) is slight. It should also be noticed that time dt depends upon the

computer time required to solve one incremental operation, and is therefore the same in each equation of types (2) and (3).

The operation indicated by equation (3) can be repeated to include all derivatives, until finally a complete set of derivatives evaluated at (simulated) time $t_o + dt$ is obtained. The only derivative not so evaluated at this point is the highest-order derivative, $y^n(t_o)$. As they are obtained, the derivatives are stored in the computer storage unit. Now the value of $g(t_o + dt)$ can be obtained from the function generator,[i] since $g(t)$ is a known function. Once $g(t_o + dt)$ is obtained, the computer solves for $y^n(t_o + dt)$ as follows:

$$y^n(t_o + dt) = g(t_o + dt) - \left.\sum_{k=0}^{n-1} f_k \frac{dy^{n-k}}{dt^{n-k}} + f_n y\right\}_{t=t_o + dt}^{f_o=1} \qquad (4)$$

When the computer has found $y\ (t_o + dt)$ and is ready to begin a second incremental integration of the differential equation, the real-time which has elapsed is dT. A second incremental integration will therefore yield a set of values at simulated time $(t_o + 2dt)$, or at real-time 2dT. The operation is repeated in this cyclic manner until a complete solution for $y(t)$ is obtained over the desired range of the independent variable.

This general differential equation was chosen for the design equation of the computer because it introduces features into the design which will be useful in solving a variety of practical

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(i) The function generator will be described in a subsequent thesis from the Dept. of Electrical Engineering, U.B.C.

engineering problems. The modifications in design required for solving more particular problems will be dealt with when the computer becomes operative.

The solution to the basic equation will now be shown in block-time form using the basic units of addition, multiplication, integration, storage, sign change and function generation. This block diagram[11] is designed to show the operations in time-sequence, just as they occur in the computer. The diagram shows the operation in units of time known as cycles, where a cycle is a specified time related to the frequency of the magnetic storage drum, and to the angular displacement of one storage unit on the magnetic drum. Details of the storage drum are given later in this section. The block-time diagram is shown in Figure 1. The explanation of this diagram will be presented in the paragraphs following.

Assume that the derivatives $y^{(n)}$, $y^{(n-1)}$, $y^{(n-2)}$, etc. evaluated at time to, are available as initial conditions on the problem, and are placed in the storage units, represented by the circles. In cycle 1, the computer begins to solve the first incremental equation, $y^{n-1}(t_o + dt) = y^{n-1}(t_o) + y^{n}(t_o)dt$. (2) In cycle 2, the quantity $y^{n-1}(t_o + dt)$ is obtained from this integration and immediately replaces the old value $y^{n-1}(t_o)$ in the storage unit. Simultaneously the integrator starts to solve the next incremental equation, $y^{n-2}(t_o + dt) = y^{n-2}(t_o) + y^{n-1}(t_o + dt)dt$ (3). Also in cycle 2, $f_1(t_o + dt)$ is obtained from the function generator, is multiplied by $y^{n-1}(t_o + dt)$, and the product put in the accumulative register. After n integrations (n = 1, 2, ...13, since there are a maximum of 13 channels

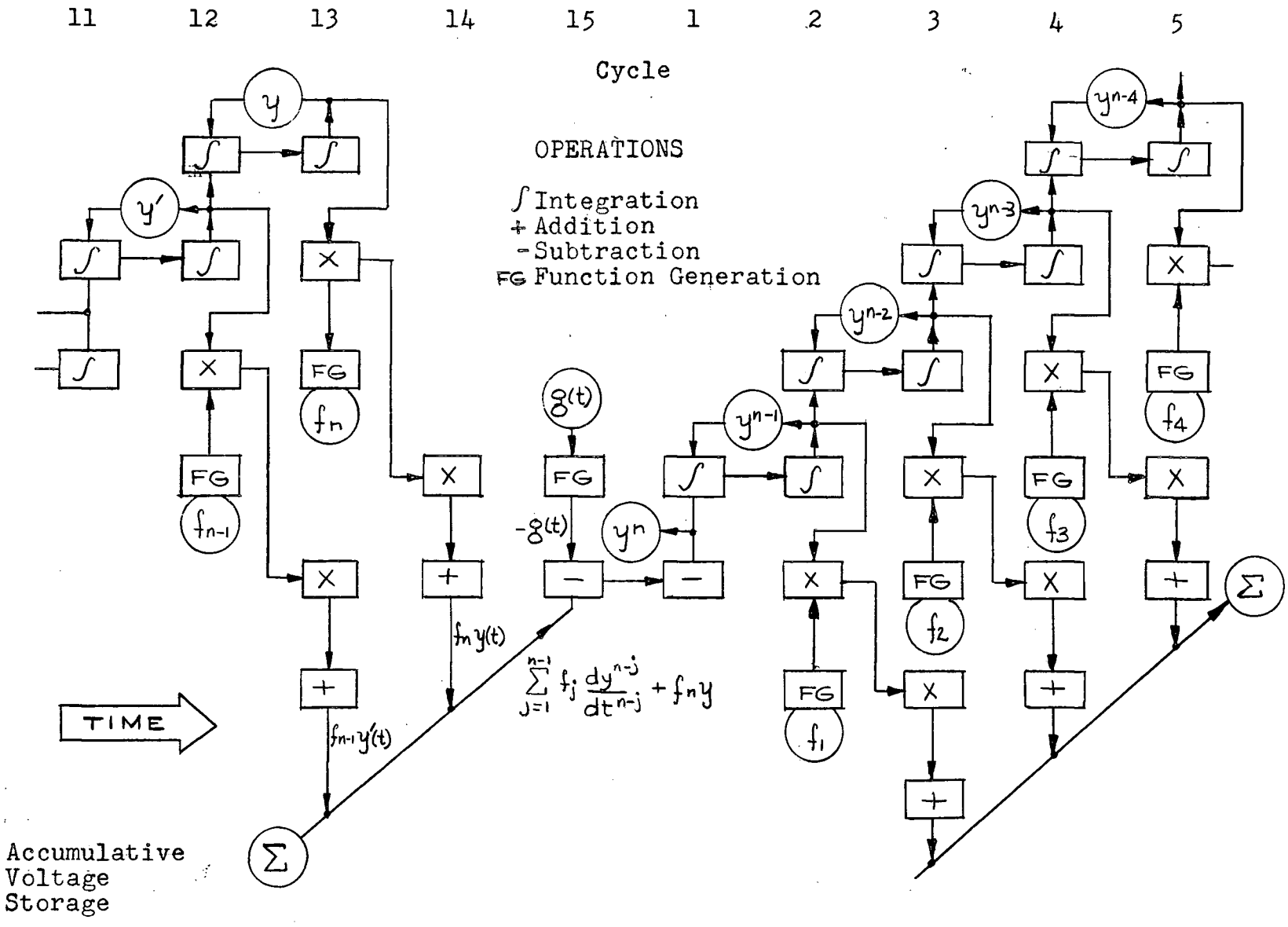


Figure 2-1. Solution of Equation (1) in Block-Time Operations

available for integration in the example chosen) a complete set of new values for the derivatives is available in the storage drum. The 14th cycle completes the storage of $f_n y(t_o + dt)$, and the 15th cycle introduces $g(t_o + dt)$ in order to resume the entire process. At this point, the magnetic storage drum has completed one revolution, and the real-time which has elapsed is dT. The entire process is allowed to continue until the desired range of the independent variable has been obtained. The operation is most accurate when dt is kept small, and the computer run short. The specific errors involved in the integration process will be considered in detail in Section 3. The solution to the equation, or the output of the operation, y(t), is recorded either on an oscillograph or a pen recorder, or by similar means. A short discussion of recorders is given in Appendix A.

2-2. The Magnetic Storage Drum

The magnetic storage drum is the memory of the computer. Information is stored on its surface in the form of position-modulated pulses. These pulses are formed by reversing a narrow band of residual flux on the drum surface. The surface of the drum is coated with an iron-oxide compound which has the property of retaining these reversals over very long periods of time. A pulse is written and/or erased by what are called "read-write head" or "destructive-read heads".[7] A destructive-read head erases the pulse which it reads, whereas the read-write head does not.

The surface of the drum is divided axially into eleven

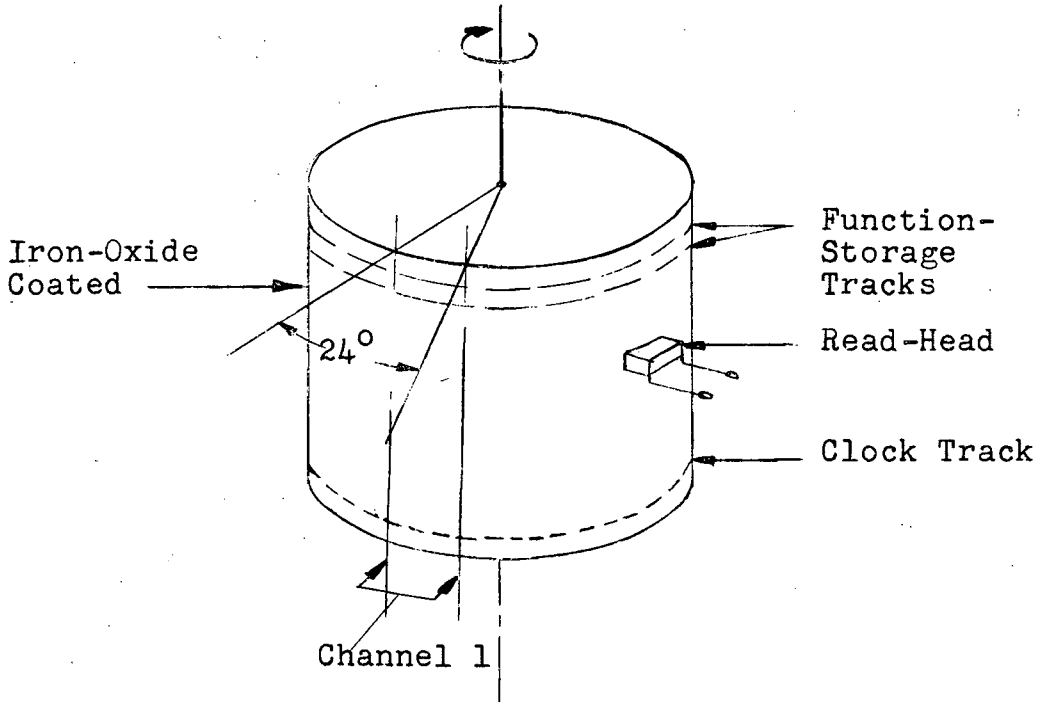


Figure 1-2. The Magnetic Drum

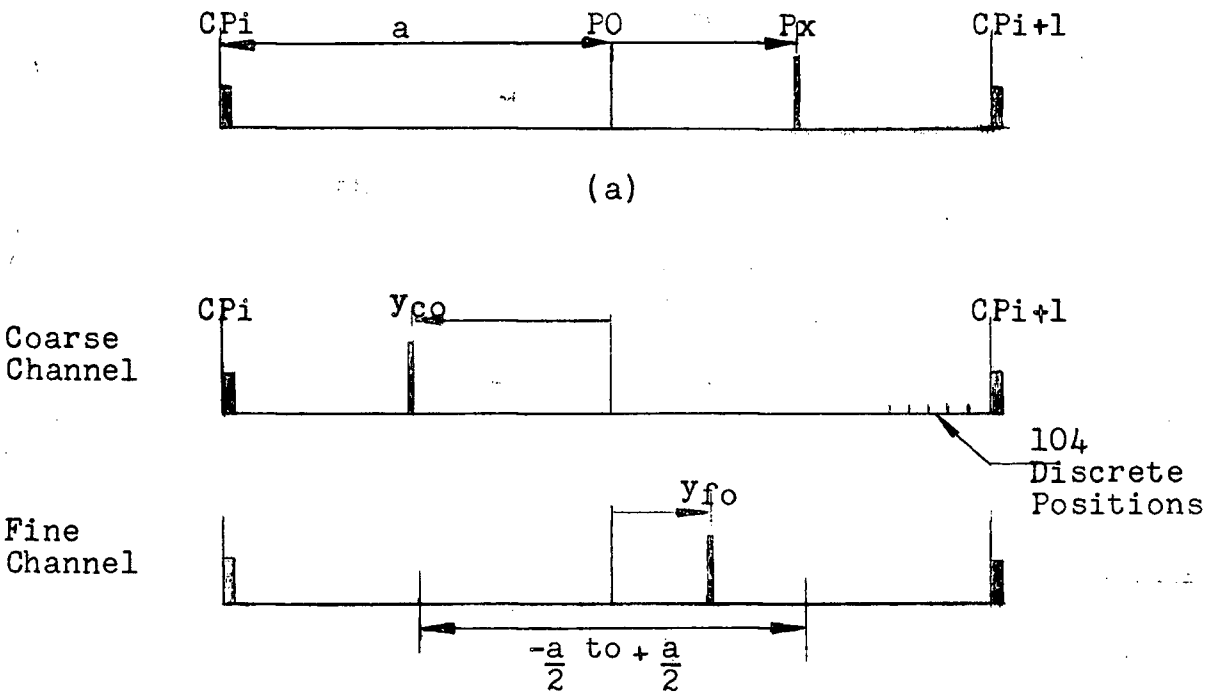


Figure 1-3. Single- and Dual-Channel Function Representation

circumferential tracks, the vertical distance between them being determined by the physical size of their associated heads (see Figure 2). On one of the tracks is permanently stored 1560 equally-spaced flux reversals. The drum is made to rotate at a frequency of precisely 60 cps,[4] so that the permanent signal appears at its read-head as a sinusoidal wave of frequency 93.6 kc/s. This signal, called the clock signal, is used to derive all the important timing pulses.

The remaining ten tracks are used for function storage. Each track has a read-write head and, in the integrator tracks, a destructive-read head. The tracks are marked around the circumference by pulses at 24° intervals; each of the fifteen parts so obtained is called a channel, and the pulses marking the beginning of each channel are called the channel pulses (CP). These pulses are derived from the clock signal and stored onto the drum. The "cycle" mentioned in section 2-1 refers to the time taken for one channel length to pass a fixed reference point as the drum rotates at its prescribed frequency.

In the computer is derived a pulse train containing pulses which correspond to every cycle of the clock signal. Therefore, there are 1560 pulses generated in one drum rotation, or 104 in the duration of a single channel. These pulses are called the "sine clock pulses" (SCP). As will be seen presently, they are used extensively in the timing circuitry and in the integration process.

2-3. Pulse Representation of Functions

A function is represented in the computer by a pulse whose position is variable, stored in a particular channel of the magnetic drum. The position of the pulse about the centre of the channel determines the value of the function (see Figure 3(a)). The length of a channel is arbitrarily taken as 2a, so that the function can assume maximum values of ±a. The practical limit is somewhat less than this amount because of possible interference between channels. Since the drum is frequency-controlled, the quantity 2a is exactly the same for all channels.

The position of the function-pulse in a channel is translated into a voltage for use in the circuitry. After the operation the voltage is changed back into pulse form and the function re-stored in its channel. Circuits which accomplish this action are discussed in detail in subsequent sections.

The above system of function representation is used extensively in the arithmetic circuitry of the computer. For the integrator, however, a different system is employed. It is called, "dual-channel representation".

2-4. Dual-Channel Function Representation.

Since the integrator employs operational amplifiers, it is subject to the effects of voltage drift. There are additional drift effects inherent in the magnetic storage drum. In order to maintain drift at a very low level, a dual-channel function representation is employed (see Figure 3(b)). This representation

uses two tracks of the drum, referred to as the "coarse" and "fine" tracks, which contain "coarse" and "fine" channels, respectively. The function under consideration is stored in two parts in corresponding channels of the two tracks, so that two pulses are required to fully represent a function, P(x).

The coarse channel contains only the discrete part of the function. That is, discrete positions are defined on this track by the possible positions of the sine-clock pulses, of which there are 104 per channel. The part of the function stored in the coarse channel varies by increments of ±1/104 of the total channel length. This is assured by selecting a certain one of the sine-clock pulses to represent the function while it is stored.

The fine channel contains the fractional part of the function. Only half the available length of this channel is used (the part about the centre) and this length represents two (±1) discrete positions in the coarse channel, or 1/52 of the total coarse channel. The function-pulse in the fine channel varies in an analogue fashion; that is, it can exist anywhere within the confines of the channel. The integration process, it will be seen, is carried out entirely in the fine channel, and the coarse channel merely records the number of times that the fine channel overflows in either a positive or a negative direction.

As an example, if the value of a function y(t) (properly scaled) at time t_o were $y(t_o) = +35.85$, then $y_{co} = +35$ is written in the coarse channel, and $y_{to} = +0.85$ is placed in the fine channel. Thus $y_o = y_{co} + y_{fo} = 35 + 0.85 = 35.85$. If now the

function receives an increment of +0.65, a count of +1 is transferred to the coarse scale and +0.50 remains in the fine channel. The new value then is $y_1 = y_{c1} + y_{f1} = 36 + 0.50$. The method by which this transfer is accomplished is left to sections 3 and 5.

3. Theory of Integrator Operation

3-1. Integrator Circuit Action

It has been stated that the integration is performed in the fine channel of the integrator. The basic equation for the fine channel operation is as follows:

$$y_{fl}^{(n-1)} + a = y_{fo}^{(n-1)} + a + \frac{y_{co}^{(n)}dt + a}{2} - \frac{a}{2}$$

In this equation, $y_{fl}^{(n-1)}$ is the integrated value of $y_{fo}^{(n-1)}$ after time dt, and $y_{co}^{(n-1)}$ is the coarse-scale value of the next-highest derivative. This latter term accounts entirely for the incremental change in the term $y_{co}^{(n-1)} + y_{fo}^{(n-1)}$, so that the equation represents integration by straight-line projection of the derivative at a known point. The a's are appropriately placed to represent the variables as the distance from a channel pulse, since it is this distance, or time-length, which is translated into a voltage in the integration process. The various fractions appear because the maximum fine-channel variation is $\pm\frac{a}{2}$, whereas the maximum coarse-channel variation is $\pm a$.

The equation as written indicates the various operations necessary to solve one incremental integration. First the variable $y_{co}^{(n)}dt + a$ is scaled by 1/2 as it is added into the fine channel containing the variable pulse, $y_{fo}^{(n-1)} + a$. The operation terminates when the quantity $y_{fl}^{(n-1)} + a$ is obtained at the completion of the operation. In order that the equation balance, $\frac{a}{2}$ must be subtracted during the operation. Now if the new fine-channel value $y_{fl}^{(n-1)} + a$ exceeds 3a/2 in the positive

direction, or a/2 in the negative direction, then a count of +1 or -1 must be transferred into the coarse channel which contains $y_{c1}^{(n-1)} + a$, and the fine-channel must be reset at the fractional value which remains after the transfer. This process represents one complete incremental integration. The circuits which have been devised to carry out this basic operation will be described in block-schematic form in section 5. Before this, a brief summary of the errors in the integration is given in section 3-2, and a brief resume of the basic circuits in section 4.

3-2. Analysis of the Error

To understand the mathematical errors involved in the integration process, consider the simple differential equation

$$\frac{dy}{dt} = k = k_c + k_f \cdot$$

The solution to this equation is of the form $y = k_c t + k_f t$. The increment in y obtained in one drum revolution is $y = k_c dT$. This increment accumulates in the fine channel until an overflow occurs, causing the coarse-scale count to increase by 1. If n is the number of drum revolutions required for the coarse-scale count to increase by 1, and the total number of revolutions is N, the the count transferred to the coarse scale is $y_c = \frac{N}{n}$. But the total time involved for N revolutions is $T = NdT$, and in n revolutions we have $k_c dTn = 1$. Substituting these expressions in the previous expression for y_c yields

$$y_c = Nk_c dT = k_c T \cdot$$

It is apparent that the only error involved is due to neglecting the fine-scale increment y_f; since the value of y_f can always be kept at 1/2 unit or less, this error is in the order of 1% or less. In a repetitive chain of integrations, truncation errors are introduced (from neglecting higher-order derivatives in the integration), but these are second-order errors. The truncation error is derived in the following paragraph.

For this simple case, the exact increment per drum revolution $\Delta y = y(dT) - y(o)$. The computer increment is $y_c^{(1)}(t_1)dT$, $o < t_1 < dT$. Therefore the error made by the computer is

$$E = y(dT) - y(o) - y_c^{(1)}(t_1)\, dT$$

Expanding $y(o)$ in a Taylor series in terms of its value at time dT yields

$$E = \left\{ y^{(1)}(o) - y_c^{(1)}(t_1) \right\} dT + y^{(2)}(o)\frac{(dT)^2}{2!} + \ldots$$

Substituting $y^{(1)}(o) = y_c^{(1)}(o) + y_f^{(1)}(o)$ gives

$$E = \left\{ y_c^{(1)}(o) - y_c^{(1)}(t_1) \right\} dT + y_f^{(1)}(o)(dT) + y^{(2)}(o)\frac{(dT)}{2!} + \ldots$$

This expression shows that all terms are of the second order, since dT is the time for one drum revolution, and is quite small. Hence the truncation error is of the second order.

The first error considered, that due to the action of the integrator, can theoretically be eliminated by extending the circuitry to take into account the fine-scale portion of the derivative, $y_f^{(1)}(o)$, since this quantity is available in the storage drum. Then the increment in y would become

$$\Delta y = y_f^{(o)} + y_c^{(1)} dT + y_f^{(1)} dT$$

The truncation error can be minimized by decreasing dT (increasing drum speed) and by taking into account higher-order derivatives. For the type of problems which the pulse-position-modulation analogue computer is designed to solve, however, these refinements are not justified. For example, in systems simulation, the system is usually stable and integration errors are not cumulative; therefore a 1% integrator error is perfectly acceptable. On the other hand, the degree of accuracy required in the adders, multipliers and function generators must usually be considerably better than this because of the possibility of appreciable cumulative errors.

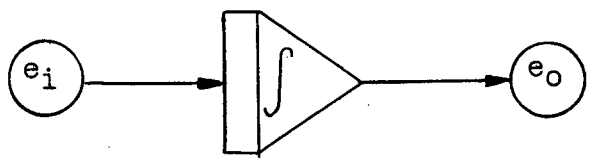
This error analysis has been for a very simple equation. The analysis becomes increasingly difficult for more complicated equations, and a complete analysis is practically impossible. It is felt that for all practical purposes, the foregoing indication of the magnitude of error is sufficient.

4. Review of the Basic Circuits Required

Before embarking on a discussion of the integrator circuits it is first desirable to briefly review the basic circuits which will be encountered. A block-schematic will be given for each circuit.

4-1. Sweep or Integrator Circuit

The sweep circuit (Figure 4-1) consists of a high-gain ac-coupled amplifier having a series resistor input and negative capacitive feed-back. It is shown in subsequent sections that for the gain A very large, the arrangement acts as an integrator and the output is essentially independent of the amplifier characteristics. The output e_o for an input e_i is given by $e_o = -1/RC \int_{t_1}^{t_2} e_i dt$. The integrator or sweep circuit is used



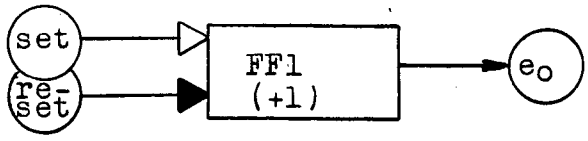
$$e_i = -\frac{1}{RC}\int_{t_1}^{t_2} e_i dt$$

Figure 4-1. Sweep Circuit

to obtain an output ramp from a step input given by a bistable flip-flop. It is interesting to note that the output depends only upon the time-constant RC for A sufficiently large, and not upon R and C individually. Therefore in order to build several identical sweep circuits, it is necessary only to assure that the time-constants are identical. This is accomplished by using a bridge calibrator.

4-2. Bistable Flip-Flop

The bistable flip-flop is a double-tube circuit which has two stable states, either of which may be achieved by applying a trigger pulse to the grid of the conducting tube. The units used in the integrator supply an output voltage, taken from a grid, of ±15 volts. This signal is used to actuate the sweep



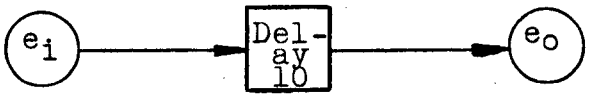
e = ±15 volts

Figure 4-2. Bistable Flip-Flop

circuits and to supply certain gating signals to the pulse control circuits. The two possible states of the flip-flop are referred to as the "set" and "reset" conditions. The set condition refers to the state when a usable signal is being supplied the integrator, and the reset condition to the state when the signal is blocked. The figure in brackets in the schematic is the slope of the normalized sweep caused by these flip-flops being applied to their respective diode gates.

4-3. Monostable or Delay Flip-Flop.

The monostable flip-flop has two possible states, only one of which is stable. It may be triggered into its unstable state by applying a negative pulse to the grid of the conducting tube. The time spent in the unstable state is determined by an



e_i = trigger pulse
e_o = 10 microsecond gating pulse

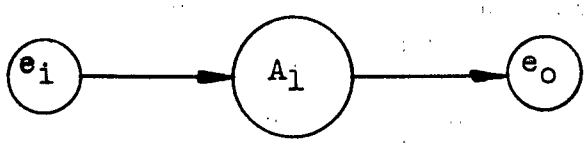
Figure 4-3. Delay Flip-Flop

RC timing network placed in the grid of the normally-conducting tube, and also by the amplitude and shape of the trigger pulse. This time is called the "delay time". The delay time is not always accurately calcuable because of the several factors which influence its length.

The monostable circuit used in the integrator serves chiefly to supply gating waveforms of from 10 to 500 microseconds duration. The same basic circuit with different timing combinations is used over this entire range. The pulse generator reviewed in this section is merely a monostable flip-flop having an extremely short delay time.

4-4. Astable Flip-Flop

The astable flip-flop is another double-tube circuit, and has two unstable states. The time-duration of each state (in the free-running condition) depends upon the timing networks in the grids. However, as is done in the particular application here, the flip-flop can be synchronized by a pulse train of frequency higher than the natural frequency.



e_i = 1000 kc/s synch pulse
e_o = channel-gating pulse

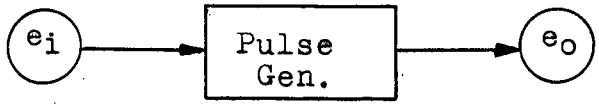
Figure 4-4. Astable Flip-Flop No.1

The astable flip-flop is used in a device separate from the integrator called a ring-counter. This device consists of 15 flip-flops connected in a ring so that the signal from one flip-flop triggers its following neighbour. The device is

synchronized such that a signal obtained from each flip-flop is used to select a particular channel pulse. These pulses, fifteen in all, must be selected individually for use in the general programming of the computer (see Appendix B).

4-5. Pulse Generator.

As mentioned earlier, the pulse generator is a monostable flip-flop having a very short delay time. It is used to generate the sine-clock pulses from the clock signal of the magnetic drum. The sinusoidal clock signal is amplified and



e_i = clock signal
e_o = 3 microsecond clock pulses

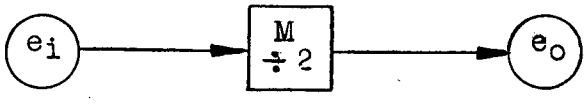
Figure 4-5. Pulse Generator

clipped to supply the signal for the pulse generator. Two pulse generators are employed, one to generate sine-clock pulses and the other to generate cosine-clock pulses, which are displaced in phase by 180° from the sine pulses.

4-6. Divider Circuits.

(a) Monostable Flip-Flop Divider.

The monostable flip-flop is used as a frequency divider for pulse trains by making the delay time last over one or more of the input trigger pulses. After the flip-flop is



e_i = 93.6 kc/s PRF
e_o = 46.8 kc/s PRF

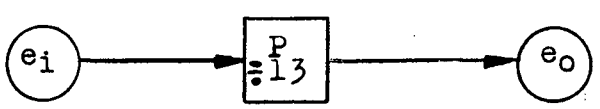
Figure 4-6(a). Monostable Division-by-Two Circuit

triggered into its unstable state, the input is disconnected by a diode, so that only after the flip-flop returns to its stable state, which may be several pulses later, can the trigger be effective. The output is obtained from the plate of the normally-off tube.

The division ratio is a direct function of the timing network, initial voltage levels, and the size and shape of the input trigger. This type of divider is used once as a division-by-two circuit to divide the clock signal from 93.6 kc/sec to 46.8 sec, and then after an intermediate stage as a division by four circuit to divide the PRF (pulse recurrence frequency) of 3.6 kc/sec to 0.9 kc/sec. The dividers are basically the same circuit but with different time constants.

(b) Phantastron Divider

The phantastron divider consists of a pentode with independent grids which has an RC timing circuit connected between its plate and its control grid. This type of divider is more stable over long division times than the monostable type. Normally the tube is not conducting plate current. When a



e_i = 46.8 kc/s PRF
e_o = 3.6 kc/s PRF

Figure 4-6(b). Phantastron Division-by-Thirteen Circuit.

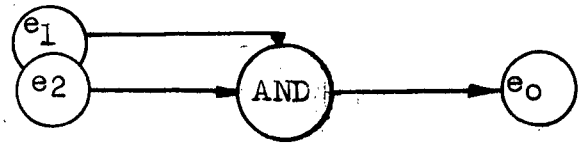
trigger pulse is received from the input, the tube begins to conduct plate current, and the source is disconnected. The timing circuit action causes the plate current to increase linearly until finally the tube bottoms. Shortly thereafter the

condenser of the timing network re-charges very rapidly, causing the tube to return to its non-conducting state. Then the next trigger is accepted and the process repeated. The cathode supplies a low-impedance output for triggering the next divider.

The phantastron divides the clock PRF from 46.8 kc/sec by 13 to give a 3.6 kc/sec output. A potentiometer is used in the timing circuit to adjust the division ratio to the exact value.

4-7. The AND gate

The AND gate is a circuit which selects one waveform if it occurs in conjunction with a certain part of a second waveform. For example, the ring counter mentioned earlier supplies a signal which is used in conjunction with a train of 10-microsecond channel-gate pulses to select a particular channel-gate pulse. Two types of AND gate are used in the integrator.



e_1 = pulse gate
e_2 = pulse train
e_o = selected pulse

Figure 4-7. The AND Gate

(a) Triode AND Gate

In the triode AND gate the grid of the tube is biased to cutoff so that conduction occurs only when the two input waveforms add so as to bring the grid above cutoff. The addition of the two waveforms is accomplished with resistors, resistors and condensers, or with resistors and diodes. The objection to this type of gate is that there is always interaction at the sources

of the waveforms, which in some cases is intolerable. In such cases, the pentode AND gate is used.

(b) Pentode AND Gate

The pentode AND gate is used extensively for gating trigger pulses for the integrator flip-flops. With the positive gating pulse applied to the suppressor, and with the positive trigger pulse train applied to the control grid (both grids are biased to cutoff), the tube selects one pulse from the train and delivers a very large, sharp negative trigger pulse. The tube has a very large gain which makes the circuit ideally suited to this particular application.

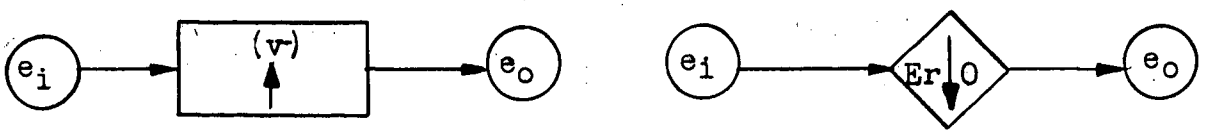
4-8. Voltage Comparators

The voltage comparator is a device which delivers an output pulse when the input signal reaches equality with a certain reference voltage level. Comparators are used in the integrator to deliver a pulse when the output waveform from the sweep circuit reaches, and to perform certain logical-decision operations in pulse selection.

The Schmitt comparator is essentially a dc-coupled multivibrator with the input grid biased to cutoff. In one application, the input is a positive ramp, and the circuit triggers when the grid comes out of clamp far enough to start regeneration. In the integrator logical-decision circuits, two comparators are used in parallel, one having a reference level set to trigger at the 1/4 the maximum normalized sweep, and the other with a level set to trigger at 3/4 the maximum normalized

sweep. The two voltage levels from each comparator are used to bias the grids of pulse-gating tubes. The details of the arrangement will be discussed in the next section.

In the zero comparator, a difference amplifier is used before the actual comparator circuit, so that the flip-over of the circuit will occur on a very small input signal. The



(a) Upgoing, Er = v- - (b) Downgoing, Er = o

Figure 4-8. Comparators

important point is that the comparator turn off when the waveform reaches zero, and not delay unnecessarily, or trigger prematurely. If the comparator does not turn on and off at the proper point of the triggering waveform, the action of the clamp in the sweep circuit, which is controlled by the comparator, will be erratic, and the sweep will be useless. Also, drift errors will occur. Therefore the design values of the comparator are critical.

5. Block-Schematic Description of the Integrator Circuits.

Now that the integration procedure has been outlined and the basic circuits reviewed, it is possible to discuss a circuit which performs the integration. It has already been seen that the coarse-channel of the integrator serves to count the accumulated fine-channel increments, and that the actual integration is performed in the fine channel. It has also been seen, in section 2, that two cycles are required for one incremental integration. Hence if one complete integration of the equation is to be completed in one revolution of the magnetic drum, then two basic integrators will be required for each of the coarse and fine channels. Therefore, Coarse Integrator I shall integrate the information in the ODD channels and Coarse Integrator II shall integrate the information contained in the EVEN channels. Similarly, the fine channel will require an ODD and an EVEN integrator. The four basic integrators must be interconnected so that the derivative from the previous coarse-channel is read into the fine-channel under consideration in order to carry out the integration procedure. The basic block schematics will now be described.

5-1. Coarse Channel Integrators.

Figure 5-1(a) shows a block schematic of Coarse Integrator I. The block labelled I is a sweep circuit which is actuated by flip-flops FFI and FF7. Block C is a zero comparator, and the block G following represents a sine clock pulse (SCP) selector circuit. The three circles together represent cosine

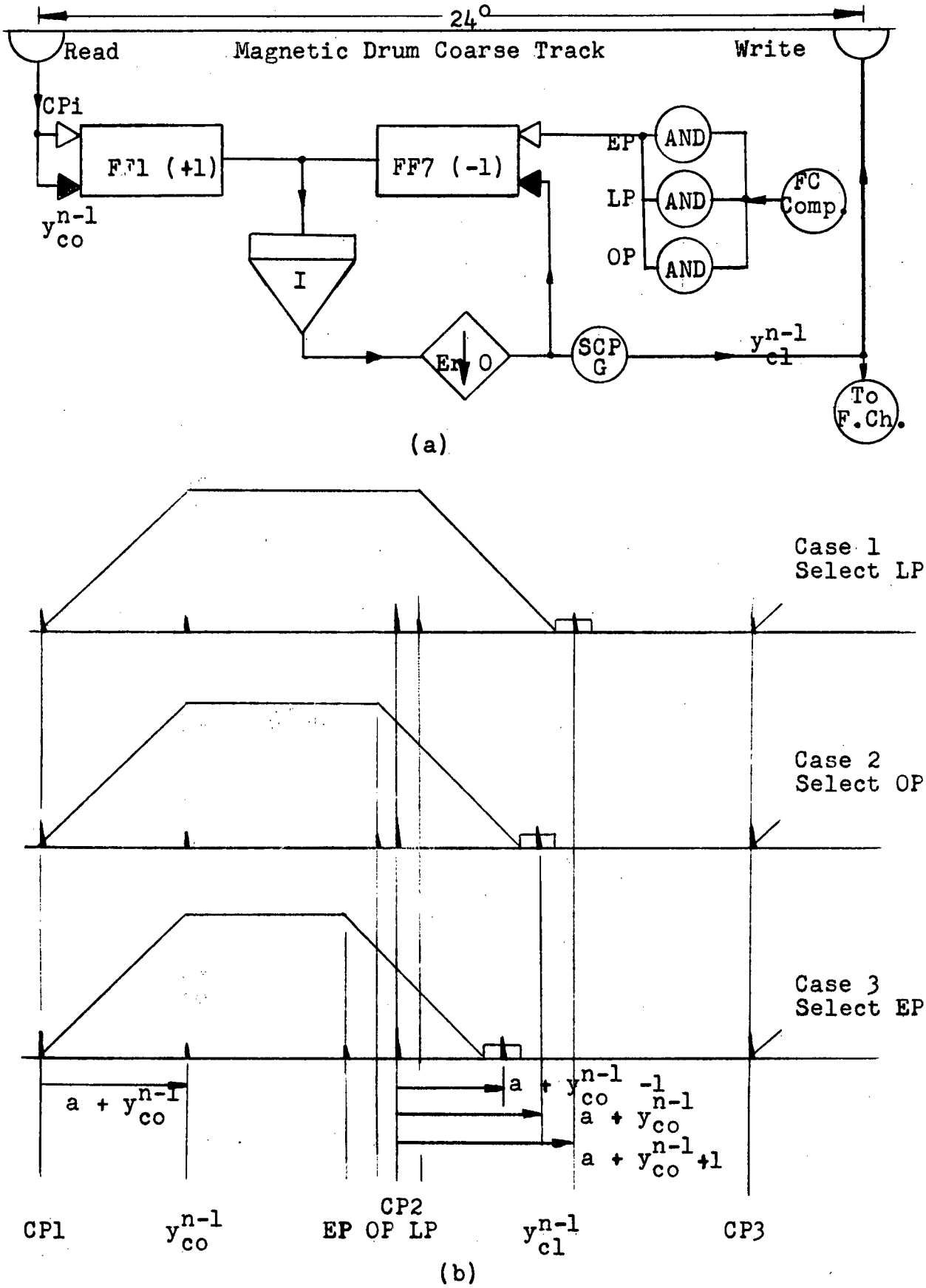


Figure 5-1. The Three Possible Coarse-Sweep Output Voltages

clock pulse (CCP) selector circuits, which are the pentode AND gates reviewed earlier. The outputs of these three gates are EP (early pulse), OP (zero pulse) and LP (late pulse). The circuit action will now be described with reference to Figures 5-1(a) and 5-1(b).

Suppose that $y_{co}^{(n)}$ is stored as a pulse in coarse channel 1, and that it is desired to carry out an integration to find $y_{c1}^{(n)}$, which is the value of $y_c^{(n)}$ at time $t_o + dt$. First CP1 (channel pulse 1) is read from the magnetic drum set to flip-flop FF1. The signal from FF1 causes the output of sweep I to increase positively. The next pulse read is $y_{co}^{(n)}$; this pulse resets FF1 and causes the sweep to terminate at a voltage dependent on the time-length between CP1 and $y_{co}^{(n)}$. Hence the position of the function pulse has been translated into a voltage at the output of the sweep amplifier.

While this action is taking place, the fine-channel comparator associated with Coarse Integrator I decides whether to select EP, OP or LP to set FF7 and initiate the coarse channel downsweep. Once the selection is made, the downsweep begins at a normalized rate of (-1) until the output voltage reaches zero. At this point, the zero comparator generates a pulse which resets FF7 and terminates the sweep. The same pulse generates a 10-microsecond gate which is used in conjunction with the SCP in the selector gate G to obtain the pulse which represents the new variable, $y_{c1}^{(n)}$. This pulse is rewritten on the storage drum and, as will be seen later, it is used in the EVEN fine channel to

perform integration of the next-highest derivative.

It is obvious from Figure 5-1(b) that the selection of EP to initiate the downsweep effects a subtraction of one pulse-position in the value of $y_{c1}^{(n)}$; the selection of OP causes no change in its value; and the selection of LP causes an addition of one pulse position to $y_{co}^{(n)}$. The three cases are illustrated. The interpretation is simply that in the first case, the (n+1)st derivative is negative over the interval under consideration, so that the value of the (n)th derivative is decreasing. In the second case, the (n+1)st derivative is relatively near zero, so that no change in the (n)th derivative is noticed. And in the third case, the (n+1)st derivative is positive and has caused the fine channel containing the nth derivative to overflow in the positive direction, so that a count of +1 is effected in the coarse channel.

After the sweep has terminated, the output holds at zero volts and awaits the next ODD channel pulse, in this case CP3. It is apparent from Figure 5-1(b) that the integration consumes two cycles. Coarse Integrator II, which accepts the information in the EVEN channels, begins integration in channel 2 (or cycle 2), terminates in channel 3, begins again in channel 4, and so on, just the opposite of Coarse Integrator I. Hence all the stored information is accounted for by the two circuits. This action requires that the channel pulses be selected into ODD and EVEN channel pulses. Notice that the terms ODD and EVEN refer to the integrators I and II, and not to the

numbers of the channel pulses. This is because there are an odd number of channels, so that after channel 15 passes through the ODD integrator (I), channel 1 is read into the EVEN integrator (II). Therefore in alternate revolutions of the storage drum, the integrators will handle the opposite channels that they did in the previous revolution.

5-2. Fine Channel Integrators

Integration and the logical decision operation of selecting the downsweep-initiating pulses is performed by the fine-channel integrators. The same basic components that appear in the coarse integrators are used, except for the logical-dicision comparator arrangement. The action is slightly more complicated, since two more input flip-flops are required, and scaling of the sweep must be effected. The schematic of Fine Integrator IV is shown in Figure 5-2(a), and the three possible sweep waveforms in Figure 5-2(b). The input flip-flops are FF5, FF6, FF11 and FF12. The downsweep initiating pulses, P-, PO and P+, selected by the comparator $v^- < v_o < v^+$ together with their coarse-channel counterparts EP, OP and LP, are sine clock pulses which occur at 1/4-channel intervals. The schematic of the comparator block $v^- < v_o < v^+$ will be described later in this section.

To review the operation, refer to Figures 5-2(a) and 5-2(b). Suppose that the operation begins with channel pulse 2, CP2, and that the value of the fine-channel function is $y_{fo}^{(n-1)}$. Consider this to be an extension of the case considered previously, so that while the value of $y_{fo}^{(n-1)}$ is being read into the

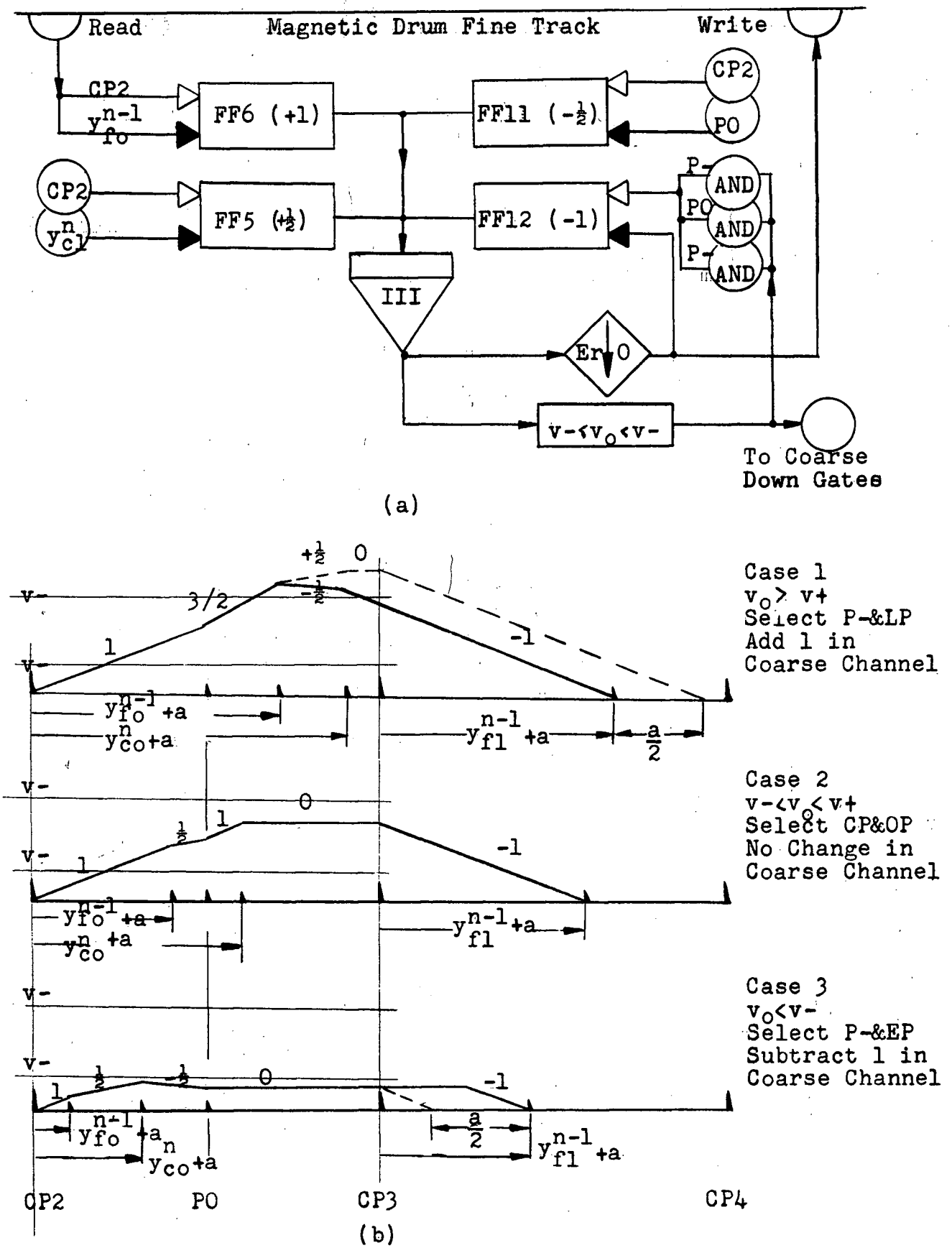


Figure 5-2. The Three Possible Fine-Sweep Output Voltages

fine channel, the value of $y_{c1}^{(n)}$ is being found in the opposite coarse integrator. Pulse CP2 sets FF5 and FF6, both of which cause a positive sweep, and FF11, which causes a negative sweep. The normalized sweep rates caused by each of these flip-flops is indicated in brackets in the respective blocks. The standard sweep rate is approximately 100 volts per 1000 microseconds. As the storage drum rotates, $y_{fo}^{(n-1)}$ is read and resets FF6, $y_{c1}^{(n)}$ is obtained from the ODD coarse integrator and resets FF5, and PO, a "fixed" pulse, resets FF11, the operation assuming no particular sequence. The sweep rates due to each pulse input add as shown in the diagram. It is apparent from a consideration of Figure 5-2(b) that the output voltage of the sweep now represents $y_{f1+a}^{(n-1)} = y_{fo}^{(n-1)} + a + \frac{y_{c1}^{(n)}dt + a}{2} - \frac{a}{2}$. The sweeps which represent $y_{c1}^{(n)} + a$ and PO(- a) have been scaled by 1/2 to represent the last two terms of the equation. In the three cases illustrated, the dotted lines show the path the sweep would take if no count were transferred to the coarse scale via Coarse Integrator II.

At this point in the operation, the sweep output voltage represents the fine-channel derivative, or portion of the derivative, after one incremental integration. Now a decision must be made by the comparator block as to which pulses to select to actuate the Coarse Integrator II and Fine Integrator IV downsweeps in order to transfer a part of this quantity (if necessary) to the coarse channel. Figure 5-3 shows how the comparators are arranged with the pulse AND gates so that the

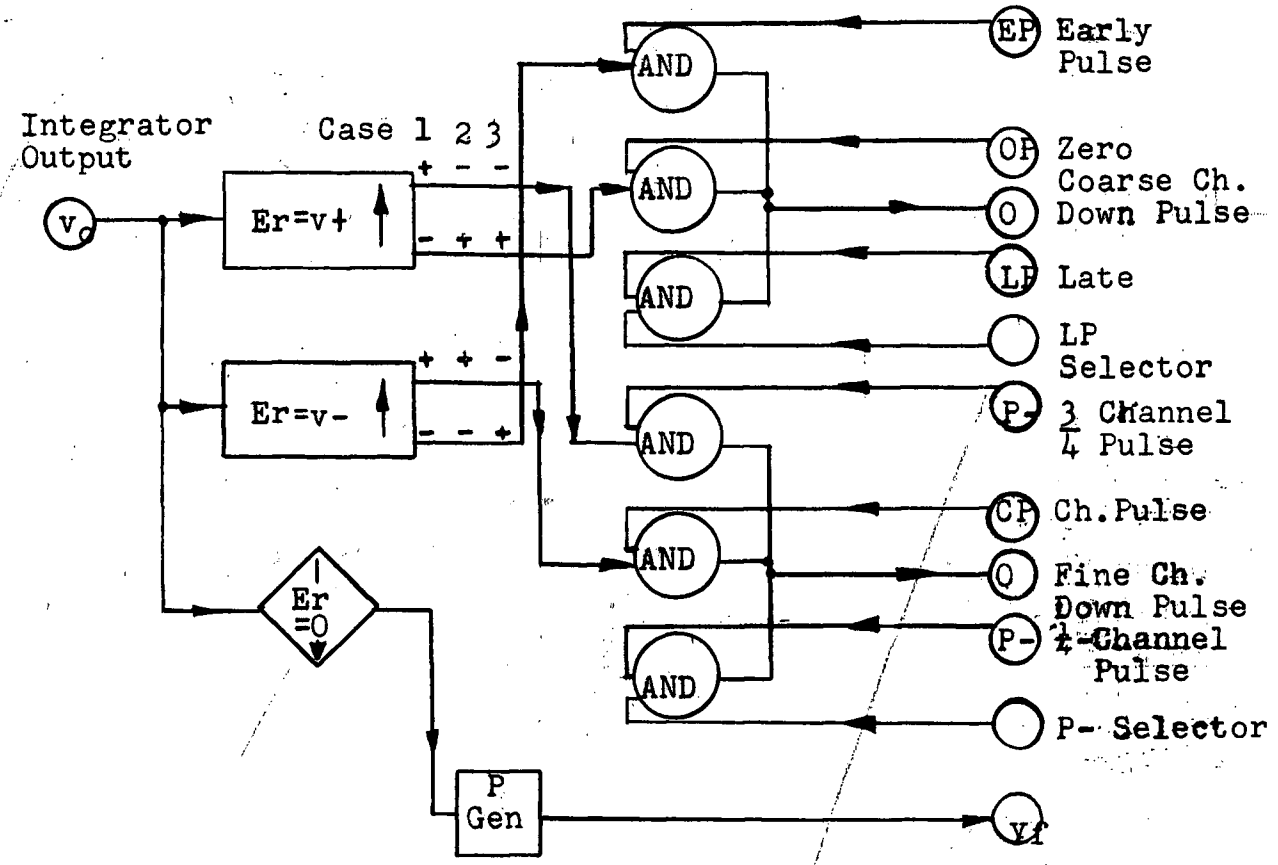


Figure 5-3. Fine Channel Schmitt Comparator Arrangement

proper selection is made. Each of the two comparators comprising the block have two possible states, designated as the (+) or the (-) state. A comparator is in the (+) state if the input voltage has exceeded the reference voltage, and is in the (-) state if the input is less than the reference voltage. When a(+) signal is delivered to one of the gates, that gate is allowed to conduct, and when a(-) signal is delivered, the gate blocks. Figure 5-3 illustrates that the pulses EP and P-, OP and PO, and LP and P+, always occur together, and the comparators effectively choose one of these pairs. Hence in case 1, the input exceeds v+, and LP and P+ are chosen; in case 2 , the input voltage lies between v- and v+, so that OP and PO are chosen; in case 3 , the input is less than v-, so that EP and P- are chosen. The corresponding

action of the coarse scale for the three cases is to add one, do nothing, and subtract one, respectively.

When the proper decision has been made, the coarse-channel downsweep pulse actuates the corresponding flip-flop, as discussed before, and the fine-channel downsweep pulse actuates (in this case) FF12, causing a normalized sweep of -1 to be added to the existing waveform. When the fine-channel sweep zeros, the zero-comparator delivers a pulse which terminates the sweep, and which is written on the drum to represent the integrated fine-channel value of the (n-1)st derivative, $y_{f1}^{(n-1)}$. Thus the circuit has accomplished one incremental integration. The Fine Integrator does not select one of the sine clock pulses to re-write on the drum because the fine scale operates in an analogue fashion, whereas the Coarse Integrator selects a particular SCP, since the coarse channel operates in a digital, or incremental, fashion. Theoretically, no drift will occur in the coarse channel, but the fine channel may feel the cumulative effects of small voltage drifts in the sweep circuit which might have only a minor effect in the coarse channels.

5-3. Combined Coarse and Fine Integrators.

The arrangements of all four integrator units is illustrated in Figure 5-4. The interconnection of the units is self-evident from the foregoing discussion. It may be noticed that since the two integrators in each scale handle the information in alternate channels, certain pulses must be selected as ODD and EVEN in order that the action does not become confused.

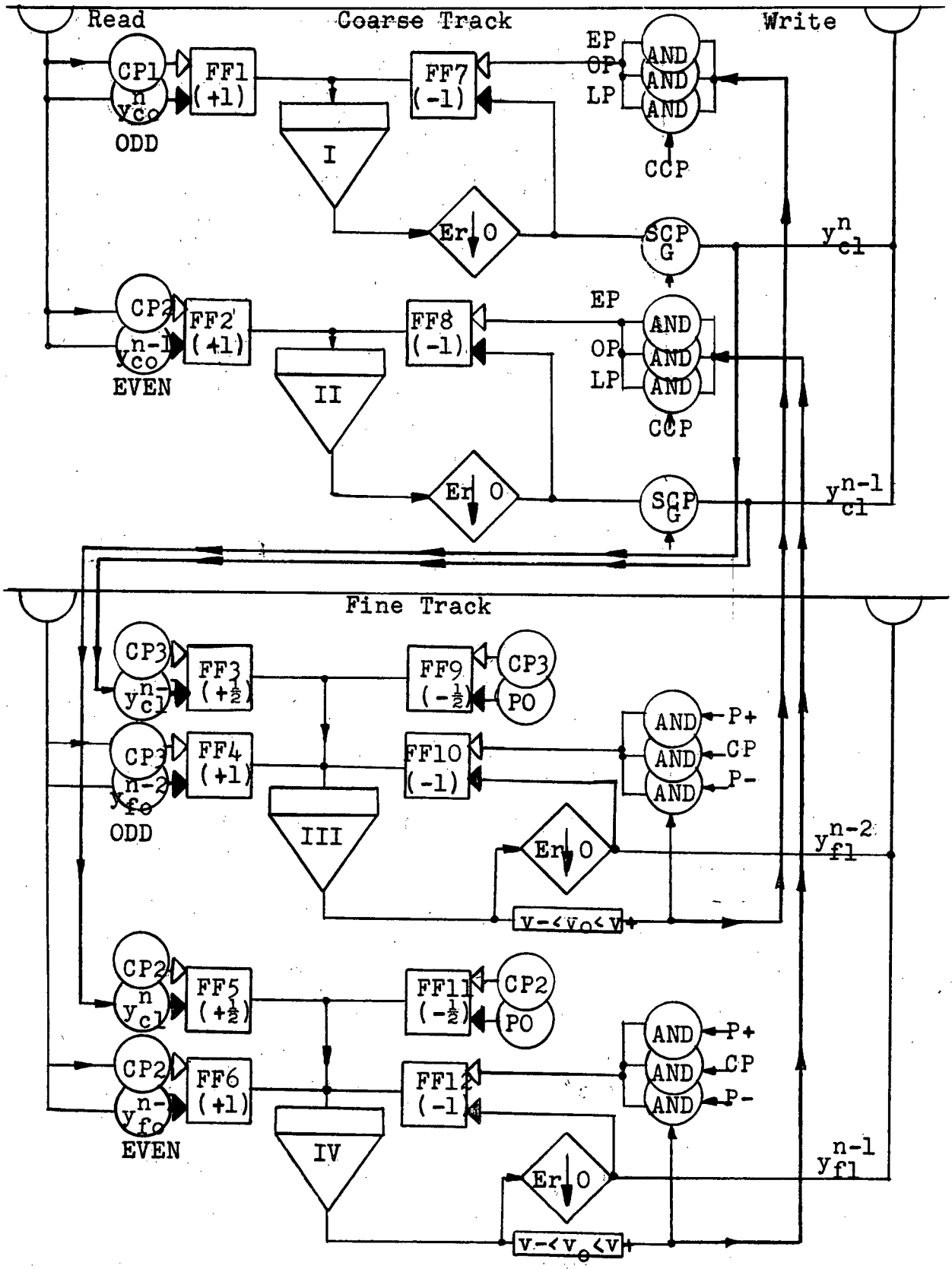


Figure 5-4. Block Schematic of Combined Integrators

It has already been mentioned that the channel pulses, CP, are selected. In addition, P-(1/4-pulse), PO(centre pulse) and OP (zero pulse) must be selected into ODD and EVEN from their respective pulse trains before being applied to the comparator-controlled gates. Selection is accomplished by using a signal from a "control flip-flop" which blankets alternate channels. The signal is taken from one grid of the flip-flop. The signal from the opposite grid is used to gate any required pulse which occurs in any of the remaining channels. Details of the selection are given in section 6.

In Figure 5-4, blocks I and III are the ODD integrators, coarse and fine, and blocks II and IV are the EVEN integrators, coarse and fine. An example of a typical integration is shown. The action begins (for purposes of illustration) when block I begins to sweep on CP1 and terminates on $y_{co}^{(n)}$, both pulses being received from the magnetic drum read-head. Assuming that the fine-channel decision circuits dictate no change for this initial step, the downsweep begins on OP and terminates when the sweep reaches zero volts. The pulse terminating the sweep selects one of the SCP to be rewritten on the drum to represent $y_{co}^{(n)} + a = y_{c1}^{(n)} + a$. While this sweep-down is happening, $y_{co}^{(n-1)}$ is being integrated in the EVEN integrators II and IV. In Fine Integrator IV, the $y_{c1}^{(n)}$ found above is used in the integration process; then the comparators decide which pair of pulses to select to start the downsweep. The EVEN downsweep begins on either EP, OP or LP as channel 3 begins to pass under the read-head. Also while channel 3 is passing, the variable pulse

$y_{c1}^{(n-1)}$ is read into the ODD integrator I to start another incremental integration. One of the inputs to ODD integrator III is the pulse $y_{c1}^{(n-1)}$ obtained above when the EVEN sweep terminates. Again a decision is made by the fine-scale comparators and the ODD sweepdown begins. The recycling action of the two sets of integrators is apparent from the diagram. The basic process just outlined is extended to include all storage channels. At the end of one revolution of the magnetic drum, one incremental integration of the entire equation has been accomplished. With regard to the comparator block $v- < v_o < v+$, note that for simplicity only one lead is shown to the AND gates, whereas in actuality four separate inputs are required.

This concludes the discussion of the integrator schematic circuits. It should be noted here that the object of this thesis is not to obtain the integrator in its final form, as has been outlined, but rather to devise the basic units required and to perform tests indicative of their reliability of operation. The complete operation of this unit as outlined would require parts of the computer, notably the storage drum, which are not yet available. In addition, it will be seen presently, a great deal of redesign of the circuits is necessary to obtain optimum operation. The details of the basic circuit elements are presented in sections 7 and 8.

6. Description of the Control Circuits

The operation of the integrator will be clarified at this time by a discussion of the control circuits. These include all pulse-generation and gating circuits. The logical-decision circuits referred to in the last section may also be considered as part of the control circuits; these will be elaborated in the next section.

All pulses are initially derived from the clock signal. The magnetic drum rotating at a fixed speed of sixty cps delivers from the clock track a sinusoidal signal of 93.6 kc/sec. This clock signal is amplified and differentiated before being applied to the pulse generator. The output of the pulse generator is a pulse train which occurs in time-coincidence with the negative-going sinusoidal signal at its zero voltage level (Figure 6-1). These are the sine clock pulses, or SCP. Simultaneously the clock signal is inverted and passed through another pulse generator to give the cosine clock pulses, or CCP.

Next the SCP are passed through three divider stages which divide the clock PRF (pulse repetition frequency) by 2, 13 and 4. The 13 circuit yields the 1/4 channel marker pulses, or 1/4 CMP, and the 4 circuit yields the channel marker pulses, or CMP. These latter pulses are used to gate the actual channel pulses, CP, used in the integrator. This selection of the original SCP is used to eliminate any possible drifts or phase shift in the divider chain.

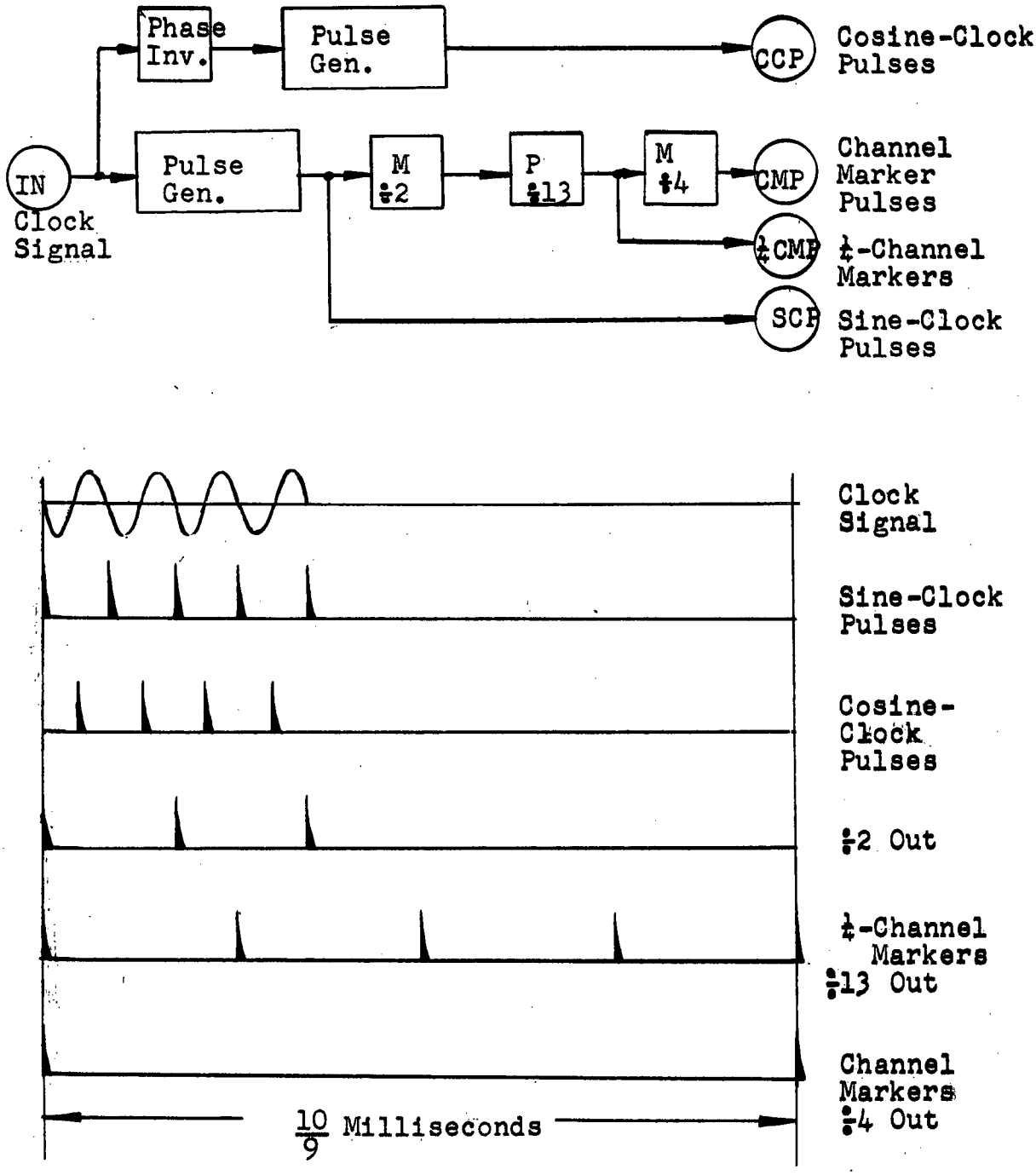


Figure 6-1. Pulse Generator and Dividers

To perform the pulse selection it is first necessary to generate the coarse scale downsweep pulses EP, OP and LP (early pulse, zero pulse, late pulse). This is done as follows (Figure 6-2). First the CMP are used to trigger three 10-microsecond coincident delay flip-flops. The three gating pulses obtained are applied to three AND gates which in conjunction with the CCP train select EP, OP and LP.

Then the OP (zero pulse) triggers another 10-microsecond delay multivibrator to yield the channel-gate pulse, CHG. This pulse blankets the SCP which will eventually be selected as the channel pulses, CP, to be stored permanently on the magnetic drum. Before this is done, further selection of the channel gates (CHG) into ODD and EVEN gates is required.

Another train of 10-microsecond gating pulses is required for the 1/4-channel pulses, P-, OP and P+. To obtain these the 1/4 CMP (channel marker pulses) are used to trigger two coincident delay flip-flops, one with a delay of 15-microseconds and the second with a delay of 10-microseconds (Figure 6-3). The signal from the latter is the 1/4 CHG which occurs in coincidence with the 1/4 channel pulses of the SCP train. To select P- and PO individually, two more coincident delay flip-flops are used, each of delay time 300 microseconds. The LP pulse is used to trigger the first flip-flop, and the signal obtained is used in conjunction with the 1/4 CHG train in an AND gate to select the P-G (P-gate). The signal from the second coincident flip-flop is similarly used to select the POG (PO gate). Selection of the actual pulses P- and PO is now a

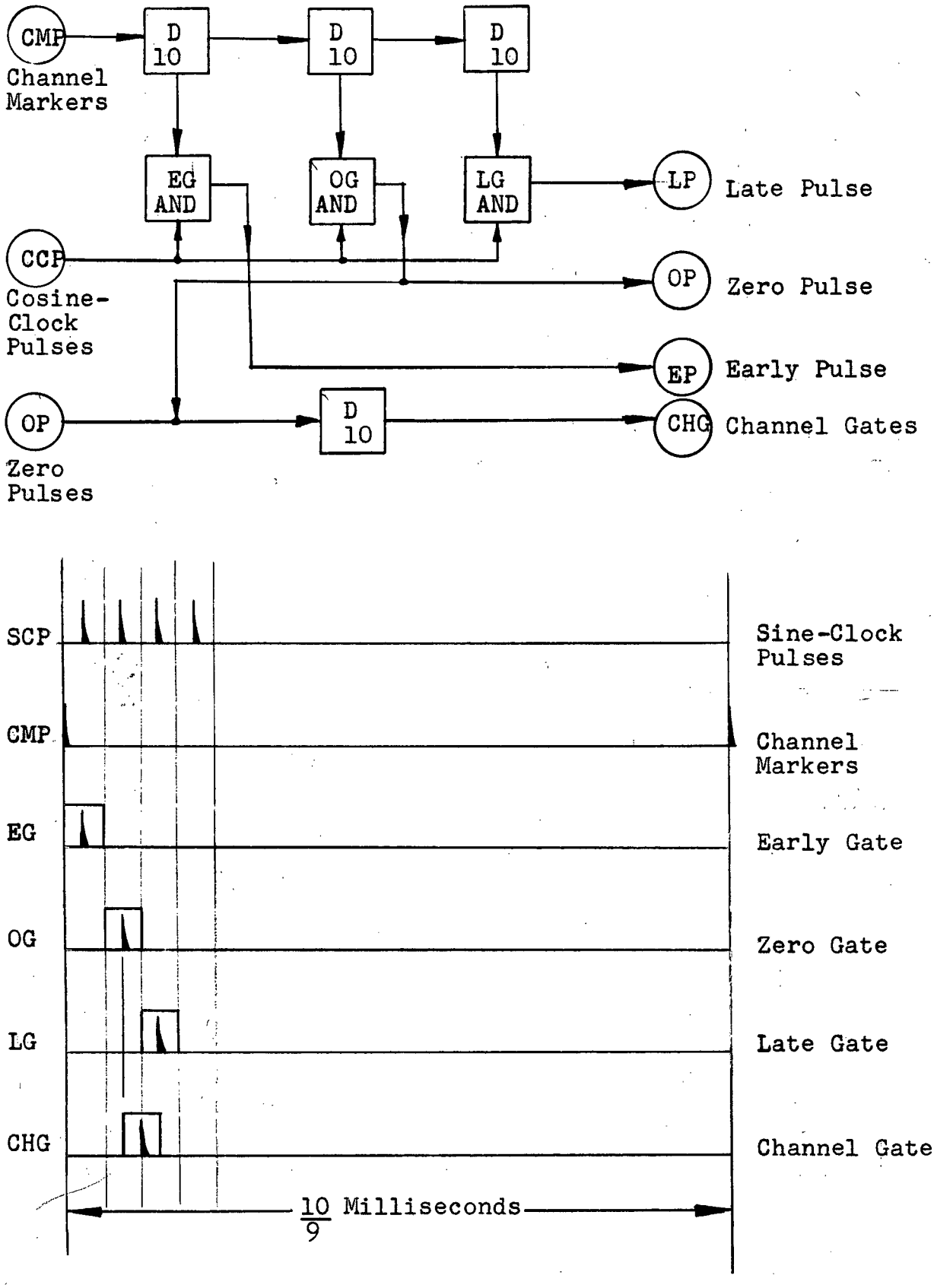


Figure 6-2. Ten-Microsecond Coincident Gates

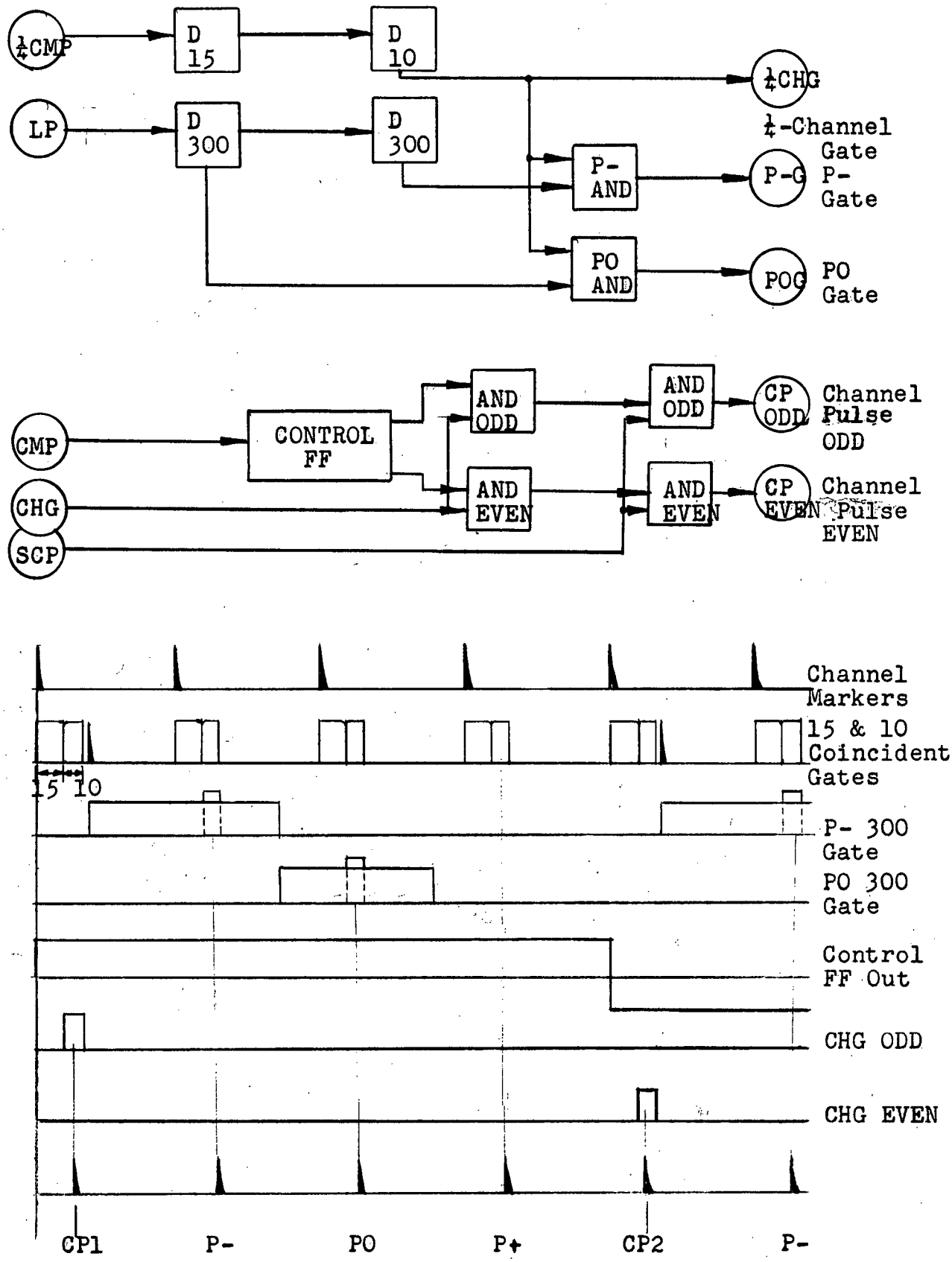


Figure 6-3. Channel Pulse Selection

simple matter, but this is not done until the pulse is required at the flip-flop because the gating waveform is much less sensitive to distortion than is the sharp pulse.

In the pulse trains already discussed, certain of the pulses must be selected further into ODD and EVEN pulses for use in the integrators. The process will be illustrated with the channel pulses, CP (Figure 6-3). The first step is to trigger a "control flip-flop" with the CMP. This flip-flop is designed for an output swing of ±15 volts. The outputs from both grids are taken one to an ODD AND gate and the other to an EVEN AND gate. The output of these gates are the EVEN and ODD channel gates, CHG. These in turn are used to obtain the selected channel pulses, CP, by gating the SCP in two additional AND gates. These pulses are then used to trigger the integrator input flip-flops.

The signal from the control flip-flop is also used to select alternate sets of downsweep pulses, EP, OP and LP in the coarse channels, and P-, OP and P+ in the fine channels. These pulses are then gated by the comparators, as stated previously. With regard to the previous discussion of the comparators, notice that the LP and P- pulses do not have to be blocked at any time by the comparator. This is because they are the last pulses in the group to occur, and if one of the previous pulses has been selected to trigger the downsweep flip-flops, their application can have no further effect.

The only pulses not yet mentioned are the function pulses which must be read from the drum and into the flip-flops.

These are gated by a pentode AND gate placed between the read amplifier and the flip-flop input. The pentode gate amplifies the pulse enough to enable it to trigger the input flip-flops.

This concludes the discussion of the control circuits. The derivation of any further pulses required for the integrator is merely a repetition or extension of the principles and circuits already discussed. With these principles in mind, all phases of the integration may be understood. The details of the control and logical decision circuits are given in section 7, and of the integrators, in section 8.

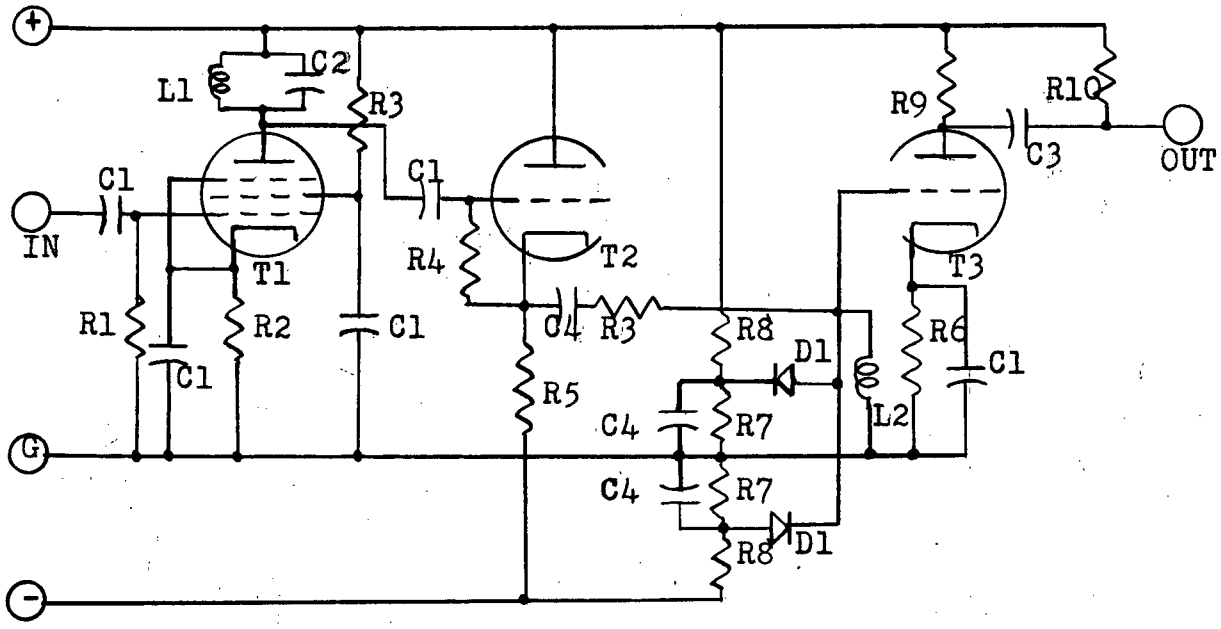
7. Circuit Details of the Control System

The control circuits, discussed in section 6, include the pulse-derivation circuits and the comparator decision circuits. These will now be described in detail. Where a circuit is used in several similar applications, mention is made of its specific uses.

7-1. The Clock Amplifier and Limiter

The clock amplifier is shown in Figure 7-1. This circuit amplifies the 93.6 kc/s, 1 volt peak-to-peak clock signal from the read-head to an amplitude of 550 volts peak-to-peak. A tuned plate load is used, and the output is taken through a cathode follower to a diode clipping circuit. From here the signal is amplified and differentiated to provide the negative clock pulses. The various waveforms accompany the circuit of Figure 7-1. The output PRF (pulse recurrence frequency) is known as the sine-clock PRF (SCP), which has been discussed previously. A PRF displaced in phase by 180° from the sine-clock pulses is obtained by inverting the clock signal and passing it through a similar limiting circuit; this signal is the cosine-clock PRF (CCP), or cosine-clock pulses.

In the circuit, inductor L_2 is used to dc-restore the grid of the amplifier. This inductor offers a high-impedance to the clock signal input, but is a low-resistance path for any charge which tends to accumulate on the grid; hence the grid is effectively clamped at zero volts, and the output pulses correspond accurately to the points where the sinusoidal



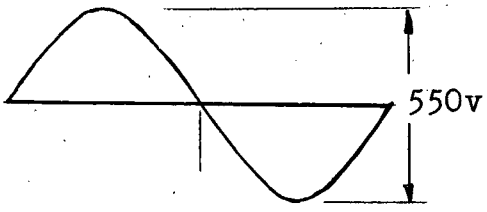
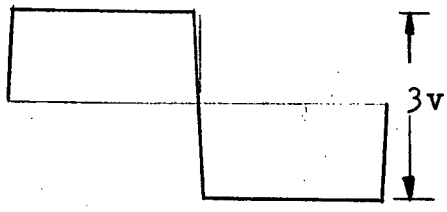
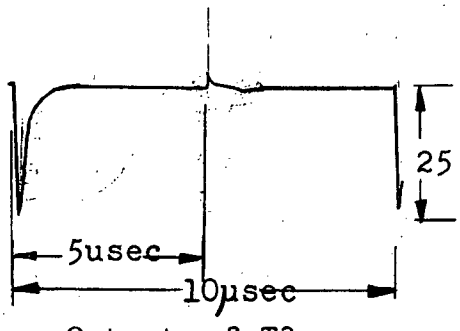


Plate of T1



Grid of T3



Output of T3

R1	560K	½W	10%
R2	1K	"	"
R3	39K	"	"
R4	330K	"	"
R5	68K	2W	"
R6	270ohm	½W	"
R7	910ohm	"	5%
R8	270K	"	"
R9	10K	1W	10%
R10	10K	½W	"
C1	.05 mfd		20%
C2	500 mmfd		"
C3	25 "		"
C4	.01 mfd		"
L1	6 mh		
L2	5-35 "		
T1	6AU6		
T2,T3	12AT7		
D1	1N191		

Figure 7-1. Clock Amplifier and Limiter Circuits

clock signal crosses the zero axis.

The resistor R5 is placed in series with the coupling capacitor C4 in order to prevent excessive current into the diode-clipping arrangement. There is a small phase shift through R5C4, but this is negligible.

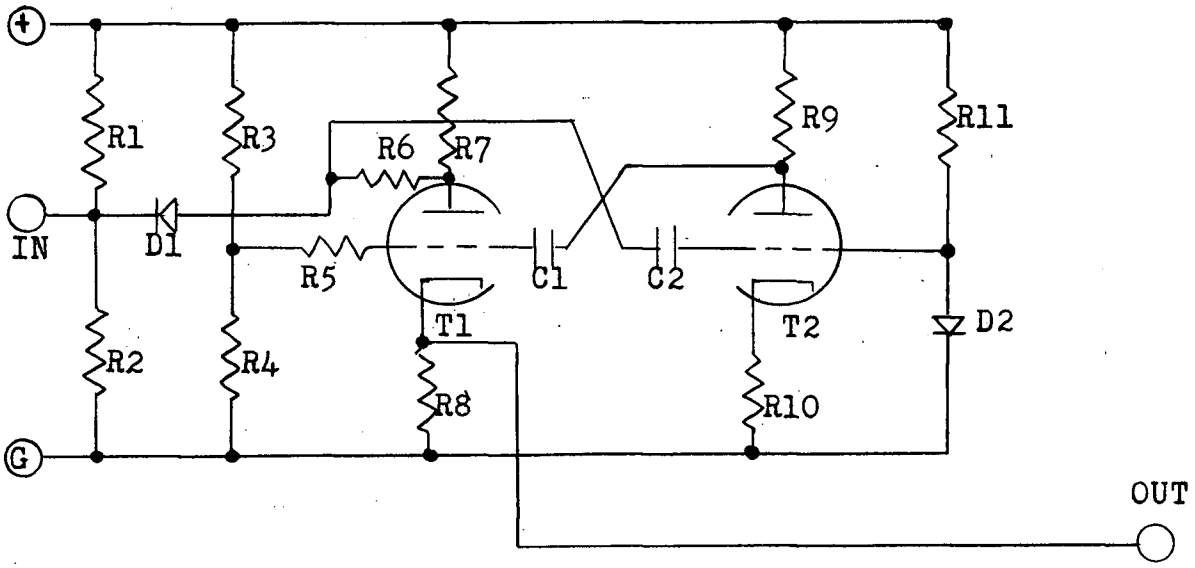
At this point in the operation, the clock pulses are accurate in time, but they are necessarily small. To be useful, they must be amplified in two separate pulse generators, or pulse-shaping circuits. At the output of the limiting circuit the pulses have an amplitude of -20 volts and a rise-time of 1/2 microsecond. In the pulse generators they will be amplified and shaped to +50 volts amplitude and 3 microseconds width.

7-2. The Pulse Generator

The schematic of the delay flip-flop[3] used as a pulse generator is shown in Figure 7-2. This circuit generates low-impedance clock pulses for use in the various gating circuits. The circuit action will now be summarized.

In the quiescent state, T2 is conducting heavily, since it is biased only by a 1K cathode resistor, and T1 is almost at cutoff since it is biased by a 4.7K cathode resistor. Therefore the output from the cathode of T1 is just above zero volts. The plate of T1 is down slightly from the voltage which would be established by the plate current alone because of a small current flowing through R7-R6-D1-R2.

The input signal is the SCP or CCP PRF. As soon as a



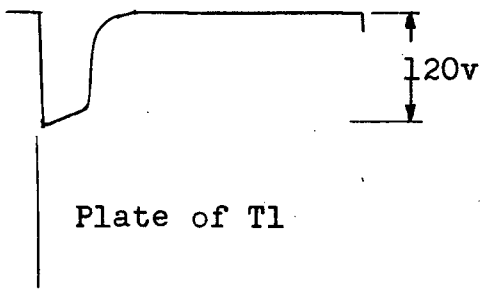
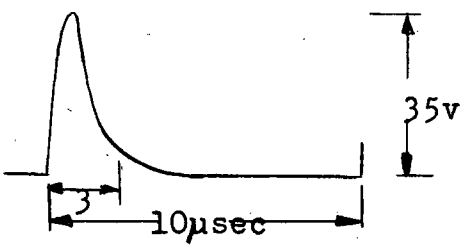


Plate of T1

Grid of T2



Cathode of T1 - OUT

R1	27K	½W	10%
R2	270K	"	"
R3	1M	"	"
R4	22K	"	"
R5	680K	"	"
R6	470K	"	"
R7	15K	1W	"
R8	4.7K	½W	"
R9	22K	1W	"
R10	1K	½W	"
R11	2.2M	"	"

C1	1000 mmfd	20%
C2	50 "	"

T1	½-12AT7
T2	"
D1	1N67A
D2	"

Figure 7-2. Clock Pulse Amplifier

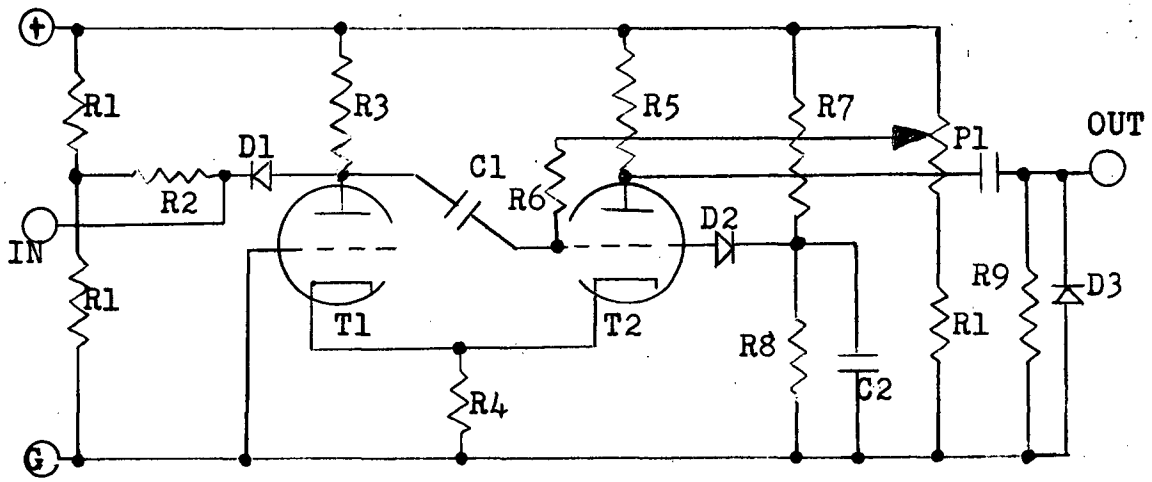
trigger occurs, D1 conducts and the pulse charges C2 negatively. The plate current of T2 diminishes because of this negative-going grid signal, regeneration through C2 and C1 begins, and within a very short time (1/2 microsecond) T2 is cut off and T1 is conducting heavily. At this time, the plate of T1 is down and diode D1 is blocked.

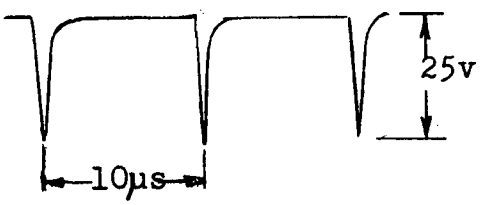
Since C2 is now disconnected from the trigger source, its charge leaks off through R11, causing the grid of T2 to rise exponentially toward zero, where it is normally clamped by diode D2. As soon as the grid rises high enough that T2 begins to come out of clamp, regeneration occurs through C1 and C2, and the tube currents are restored very rapidly to their original states. As this happens, the plate of T1 rises in potential and once more the diode D2 is allowed to conduct current. Now the circuit is ready to accept the next trigger pulse.

For the circuit values shown, the output is a pulse of 50 volts amplitude and 3 microseconds duration (Figure 7-2). The duration of the pulse depends upon the initial voltage levels, the shape of the trigger pulse, and the time-constant R11C1.

7-3. Division-by-Two and Division-by-Four Circuits

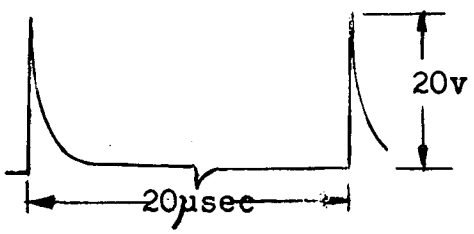
The division-by-two and division-by-four circuits are essentially the same monostable flip-flop with different time-constants and grid-return voltages. The division-by-two circuit, shown in Figure 7-3, is a cathode- and plate-to-grid coupled monostable flip-flop. The input PRF is the sine-clock PRF, and the output is 46.8 kc/s , illustrated in Figure 7-3. The circuit





Clock Pulses - IN

Plate of T2



Divided PRF - OUT

R1	100K	½W	10%
R2	1K	"	"
R3	47K	1W	"
R4	1K	"	"
R5	10K	"	"
R6	1M	½W	"
R7	330K	"	"
R8	15K	"	"
R9	2.7K	"	"
P1	200K	"	"

C1	25 mmfd	20%
C2	.01 mfd	"
C3	100 mmfd	"

T1,T2	½-12AT7
D1,D2,D3	1N191

Figure 7-3. Division-by-Two Circuit and Waveforms

action is as follows:

Initially, T2 is conducting and the voltage drop across R4 biases T1 to cutoff. The plate of T1 is down slightly due to a small current flowing through R3-D1-R2-R1. For division by two with the components shown, the grid-return voltage Er is approximately 200 volts. The grid of T2 is clamped at +15 volts in the quiescent state.

When an input pulse is applied, the grid of T2 is driven negative and released from its clamp. Regeneration occurs through the common cathode resistor R4 and, in a very short time, T1 is conducting and T2 is biased to cutoff. Because the plate of T1 is down, the circuit is isolated from the trigger source through diode D1.

Now the charge on the coupling capacitor C1, which is holding T2 in clamp, begins to leak off exponentially through R6 to the return voltage Er. The time-constant C1R6 and the return voltage are chosen so that while T2 is still in clamp, a second trigger pulse passes at the input and is blocked by D1. In between this pulse and the next trigger pulse, the grid of T2 rises high enough to overcome the bias imposed by the current of T1 through R4. Regeneration then occurs and restores the circuit to its original state, with T2 conducting and T1 cut off. The circuit is then ready to accept another trigger pulse. The output PRF is taken from the plate of T2.

It will be noticed that the circuit action is very similar to that of the pulse generator, but cathode coupling

instead of double plate-to-grid coupling is employed. Also, Er can be changed to alter the delay time of the circuit. The delay time depends upon the trigger shape, initial voltage settings, and the time-constant C1R6, as well as upon Er.

The division-by-four circuit divides a PRF of 3.6 kc/s to 0.9 kc/s. To obtain this divider, the following changes are made in Figure 7-3: C1 = .002mfd

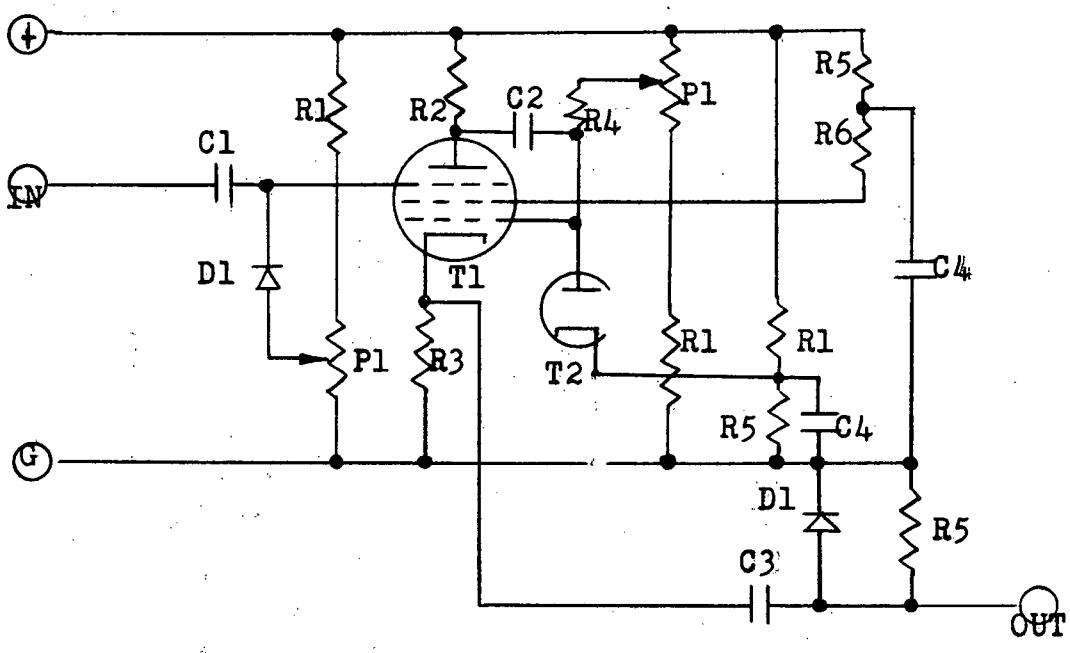
R6 = 2.2 M 1/2W 10%

R9 = 68K 1/2W 10%

7-4. Phantastron Division-by-Thirteen Circuit

The phantastron divider,[3,4] shown in Figure 7-4, divides the output of the first divider stage from 46.8 kc/s to a 3.6 kc/s PRF. The phantastron is essentially a Miller sweep generator which has a linear timing waveform, rather than the exponential waveform of the multivibrator circuits already discussed. The linear waveform gives increased timing stability. A positive trigger of 15 volts is required to obtain a 25-volt negative pulse from the cathode. The circuit action will be described briefly.

In the quiescent state, screen current flows to raise the cathode potential to +40 volts. Since the suppressor is biased at +25 volts, plate current is cut off. When a trigger is received at the suppressor, plate current starts to flow, causing a sharp drop in potential at the plate. This drop, however, is coupled to the control grid, so that the plate current is limited to a small value. At the same time the cathode



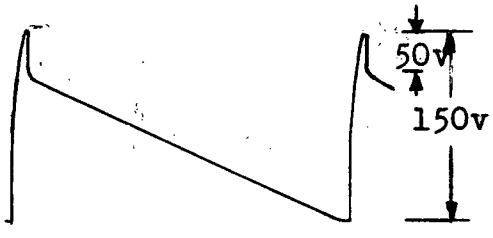
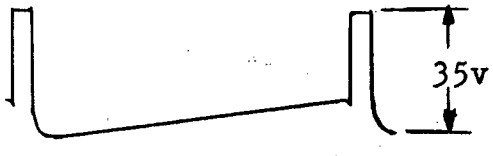
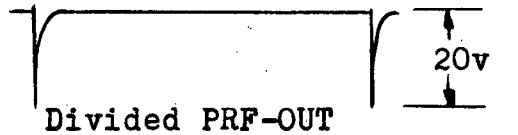


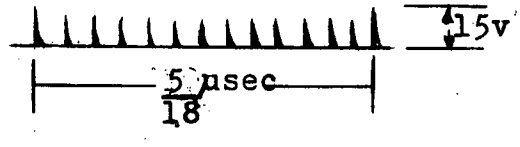
Plate of T1



Cathode of T1



Divided PRF-OUT



Input PRF - IN

R1	100K	½W	10%
R2	68K	"	"
R3	6.8K	"	"
R4	6.9M	"	"
R5	22K	"	"
R6	4.7K	"	"
P1	200K	"	"
C1	100 mmfd		20%
C2	50 "		"
C3	250 "		"
C4	.25 mfd		"
T1	6AS6		
T2	½-6AL5		
D1	1N191		

Figure 7-4. Phantastron Division-by-Thirteen Circuit

current, and hence the screen current, is greatly reduced, so that a large positive step appears at the screen.

After this initial sharp drop, the Miller sweep action begins (Figure 7-4). The control grid is now free and has a large positive bias, and the plate-to-grid coupling condenser C2 forms a negative feedback loop. Electron current flows from the tube into the left side of C2, and through R4 to Er. Therefore the left side of C2 must drop in potential at a rate dependent upon R3C2. This requires a plate current which increases linearly with time until finally the tube "bottoms", or runs against the knee of the plate characteristic. Since further drop in the plate voltage is impossible, and the increasing current cannot be further supplied, the right side of C2 rises exponentially toward Er until the grid supplies the current. Now the screen current again increases, the control grid is in clamp, and the tube returns to its quiescent state and awaits the next trigger pulse.

With the component values shown, a division ratio of 13 is obtained by adjusting Er in the neighbourhood of 220 volts. It has been stated in the literature[3] that with a stable power supply and precision components, reliable division by 30 has been achieved. Therefore a ratio of 13 appears to be well within the stable range of operation of the phantastron.

With the suppressor triggering employed here, the source is not disconnected during the plate rundown, but the waveforms are not adversely affected. The phantastron divider output pulse, as mentioned earlier, is a 3.6 kc/s PRF which triggers

the division-by-four divider.

7-5. The 10-Microsecond Coincident Gates

It has already been seen that the output PRF of the division-by-four circuut triggers three coincident gates which supply the early (EP), zero (OP), and late (LP) 10 microsecond gating pulses. The circuit used is the pulse generator of

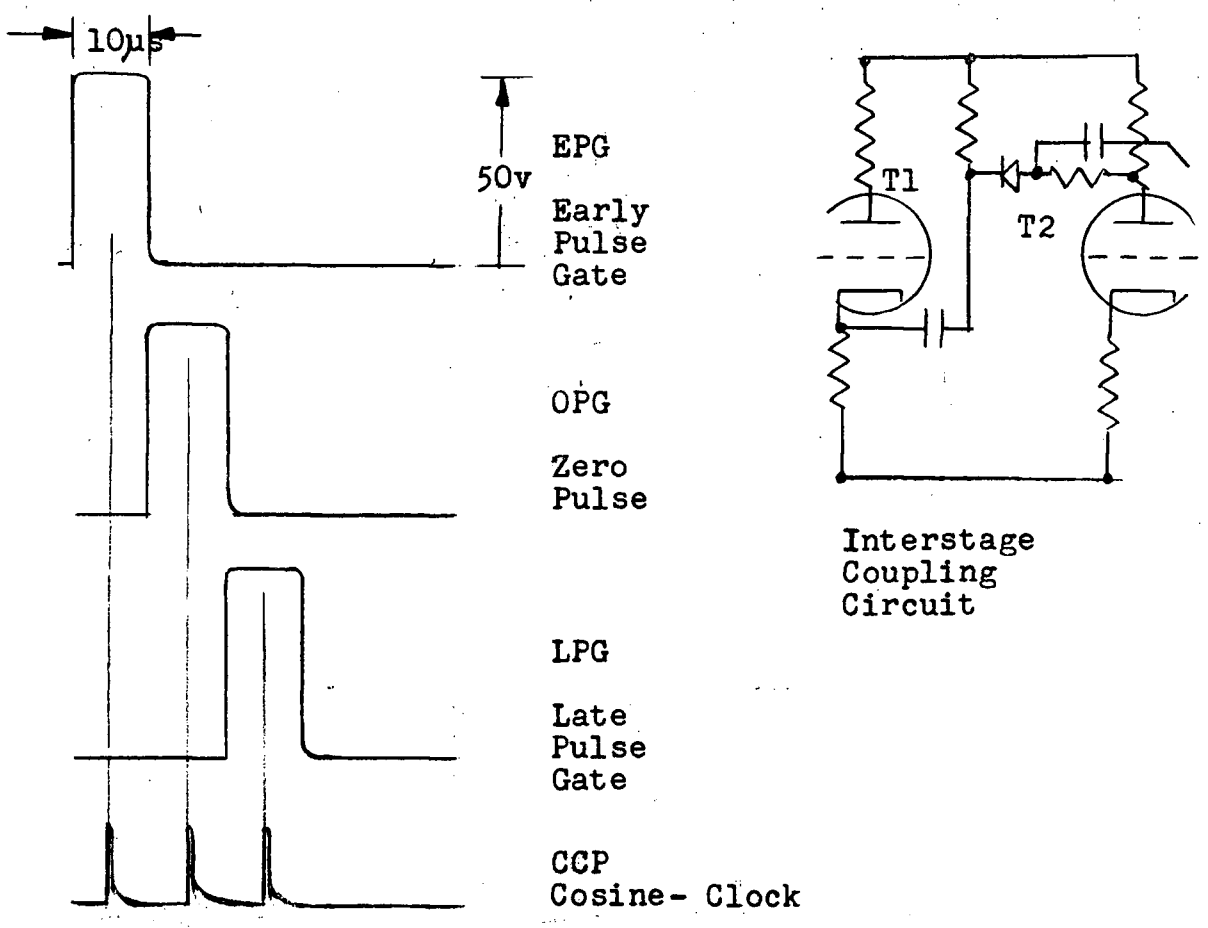


Figure 7-5. Coincident Down-Gate Waveforms

Figure 7-2 with the following change to increase the width of the output pulse from 3 microseconds to 10 microseconds: R11 = 1.5M 1/2W 10%. The waveforms for the coincident gate

circuits are shown in Figure 7-5.

With a stable power supply the circuit is very reliable, but the timing resistor and condenser, R11 and C2, are quite critical. With the 20% capacitors available, it was necessary to make up the exact resistance required with a combination of smaller values. For a design which is critical and which has to be standardized, it is advisable to use components of 5% tolerance throughout.

The cathode waveform of the EP is differentiated to supply the trigger for the OP gate, and that of the OP gate supplies the trigger for LP. Diode-coupling between gates if employed to bias off a small amount of high-frequency leak-through which appears on the output waveform of the final divider stage (the trigger for the EP gate).

A circuit identical to the coincident gates is used to supply the channel-gate pulse. As mentioned earlier in connection with the block schematics, this gate is triggered by zero pulse (OP). The trigger pulse is selected in a pentode AND gate, to be described later in this section.

The 1/4-channel gate is a 10-microsecond gate like those already discussed. To obtain this gate, however, a 15-microsecond coincident gate, triggered on the channel-marker pulses (CMP), must supply the required trigger pulse. For a 15-microsecond delay time, R11 of the previously-described circuit must be increased to 2 megohms. The output of the 1/4-channel gate is used in conjunction with two 300-microsecond selector

pulses to obtain the individual P- and PO gating pulses.

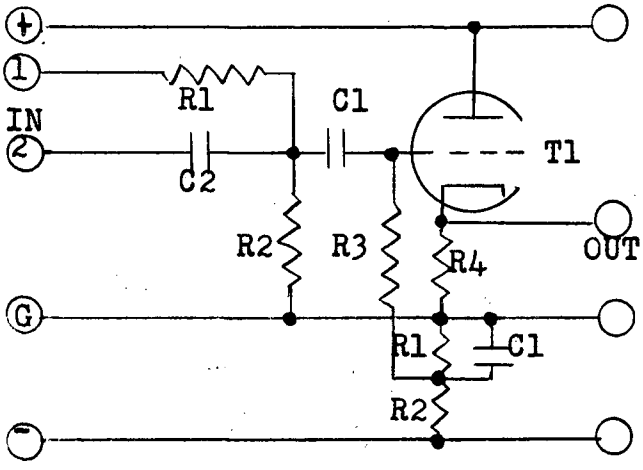
7-6. The 300-Microsecond Coincident Gates and Triode AND Gate

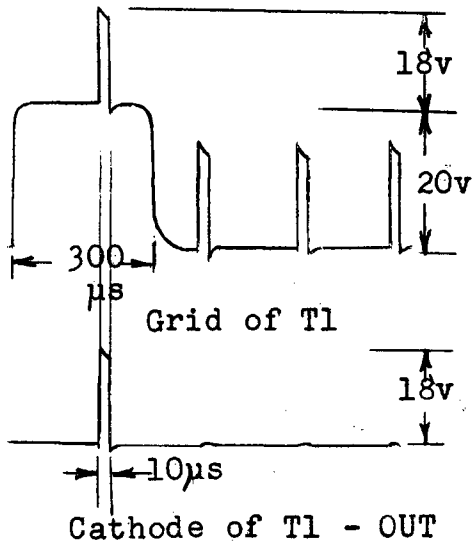
Two 300-microsecond coincident gates are used to supply the selector pulses for the P- and PO gates of the 1/4-channel gate train. The circuit of the coincident gates is the same as that of Figure 7-2 but for the following changes:

C2 =	620 mmfd		20%
R11 =	4.7M	1/2W	10%

The components in these gates are not too critical so long as the waveforms blanket the P- and PO pulses. The first gate is triggered by late pulse (LP), and the second by the trailing edge of the output from the first. The two pulses obtained are added to the P- and PO gates at the grid of a triode AND gate,[10] shown in Figure 7-6. The triode is biased to cutoff except when the selected pulse causes it to come out of clamp. Then the tube conducts, and the selected pulse appears at the output.

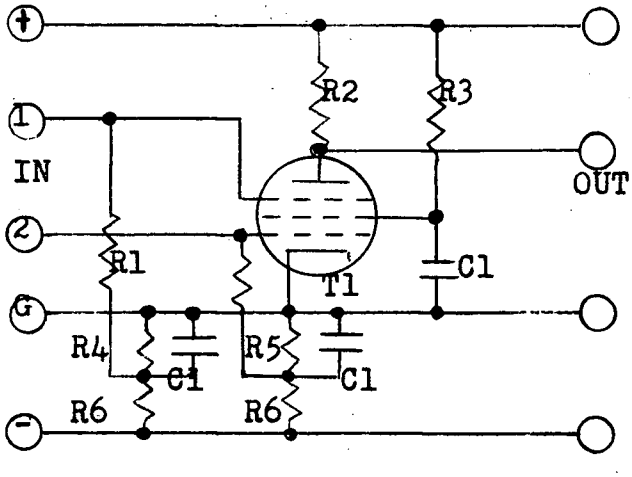
The main objection to this gate is that the selected pulse is attenuated, and there is always some interaction of the pulse sources. If a larger pulse is necessary, a stage of amplification could be used before the triode gate. This would also isolate the sources. As it happens, the 15-volt pulse obtained from the present arrangement is just sufficient to operate a pentode clock-pulse selector gate, since the suppressor of such a gate is biased to cutoff at -20 volts.

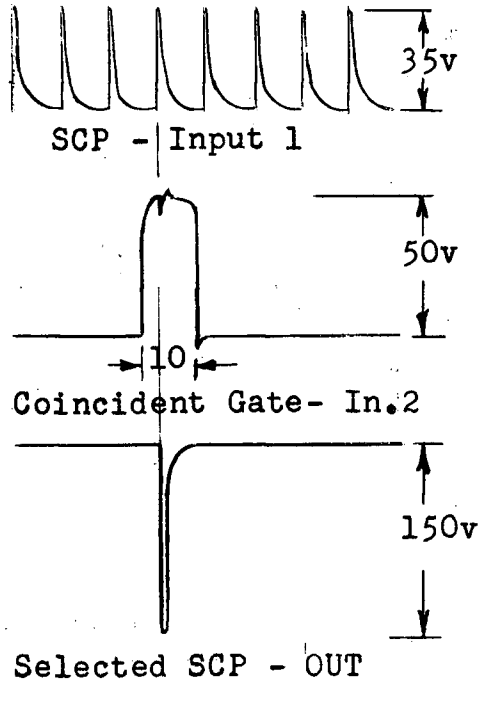




R1	39K	½W	10%	C1	.01 mfd
R2	270K	"	"	C2	.001 "
R3	1M	"	"		
R4	1K	"	"	T1	½-12AT7

Figure 7-6. Triode AND Gate and Waveforms





R1	1M	½W	10%	C1	.01 mfd
R2	68K	"	"		
R3	27K	"	"	T1	6AS6
R4	10K	"	"		
R5	22K	"	"		
R6	270K	"	"		

Figure 7-7. Pentode AND Gate and Waveforms

7-7. The Zero- and Late-Pulse Selector Gates

The zero pulse (OP) and late pulse (LP) must be derived separately for triggering the channel and 1/4-channel coincident gates. This is accomplished using a pentode AND gate,[10] shown schematically in Figure 7-7. This gate is typical of the pulse-selector gates used extensively in the sweep triggering circuits. Its operation will be reviewed briefly.

Normally, both grids are biased to cutoff, so that no plate or screen current flows with no signal applied. The cosine-clock pulses are applied to the control grid, and the OP or LP selector pulses to the suppressor. With the plate current biased to cutoff by the suppressor, a small screen current will flow whenever a cosine-clock pulse brings the control grid out of clamp. However, nothing as yet appears at the plate.

When a gating pulse occurs at the same time as one of the clock pulses, both grids are released and the tube is allowed to act as an amplifier for the duration of the gating pulse. This allows just one of the clock pulses to be amplified, so that a large negative pulse appears at the plate of the tube. The large gain of the tube causes the output pulse to be sharpened considerably.

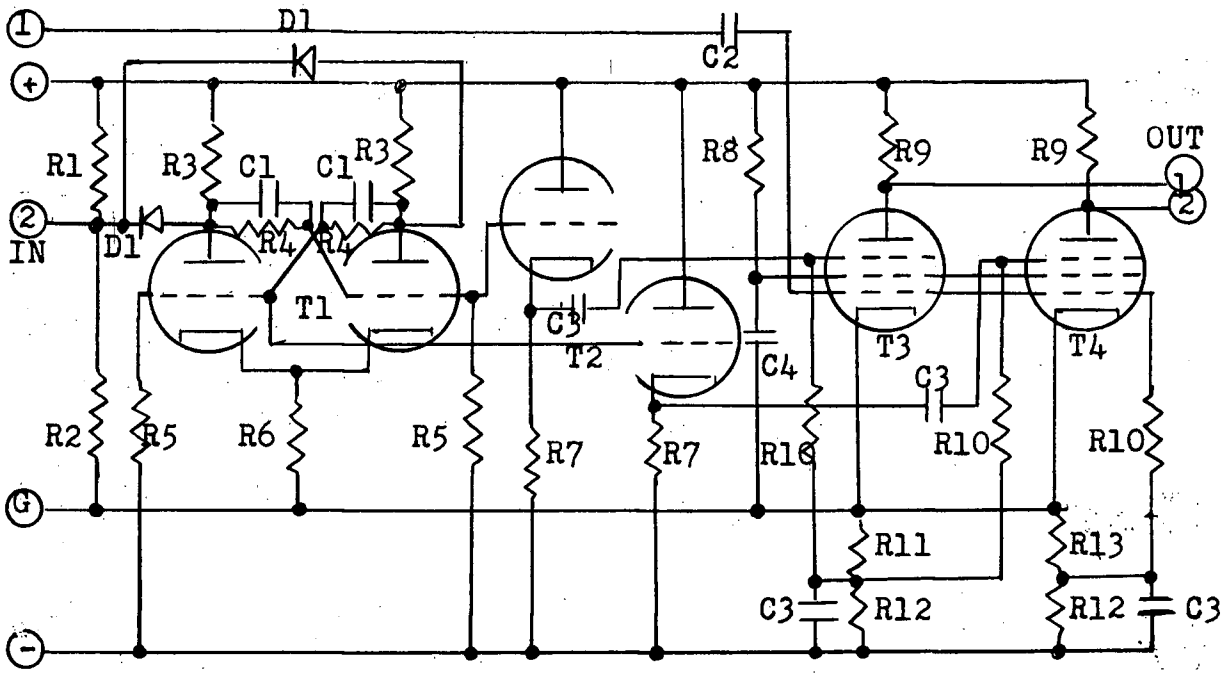
With large input pulses, output pulses of 50-300 volts and of 0.2 microsecond rise-time are easily obtained. The circuit is ideal for triggering sweep input flip-flops because, in addition to supplying a large trigger pulse, it normally

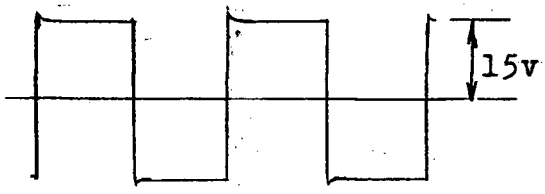
conducts no plate current, thus saving on power supply requirements.

7-8. Control Flip-Flop and Channel Gates

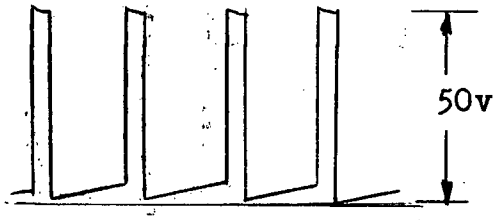
The control flip-flop, bistable multivibrator triggered by the channel-marker pulses (CMP), supplied from each grid a positive output voltage which blankets alternate channels from CMP_i to $CMP_i + 1$. The output from each grid is taken through a cathode follower to a group of gating circuits to select the required ODD and EVEN pulse groups. The pulses which must be so selected are the 1/4-channel (P-), centre-channel (PO), channel (CP), and late (LP) pulses. The schematic circuit of the control flip-flop, cathode followers and channel gate selectors is shown in Figure 7-8. Selection of the P-, PO and LP pulses will be reviewed presently.

The control flip-flop circuit is identical to the sweep input flip-flops previously mentioned. The circuit is designed for a grid swing of ±15 volts. The exact voltage swing is not too important, so long as a suitable amplitude is obtained for gating requirements. In the number of circuits built , the outputs vary between 12 and 20 volts amplitude, which is quite satisfactory. It is important that the plate and grid-biasing resistors be well matched for symmetrical operation. In a general analysis of the flip-flop design problem, which has a unique solution for a particular tube and output voltage, it was found that if the resistor errors were in the same direction (i.e. high or low) then for a resistor tolerance of 5%, and a

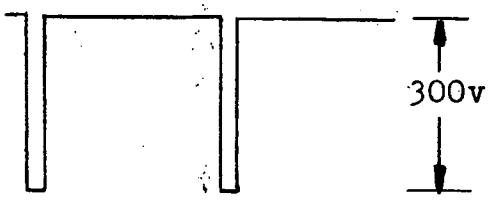




Output of T1



Channel Gates - IN 1



Selected CHG - OUT 1

R1	56K	½W	10%
R2	270K	"	"
R3	56K	"	5%
R4	180K	"	"
R5	270Kww	"	½%
R6	15K	"	5%
R7	180K	"	10%
R8	27K	"	"
R9	68K	"	"
R10	1M	"	"
R11	27K	"	"
R12	220K	"	"
R13	18K	"	"

C1	100 mmfd	20%
C2	50 "	"
C3	.01 mfd	"

T1	5751
T2	12AX7
T3,T4	6AS6
D1	1N191

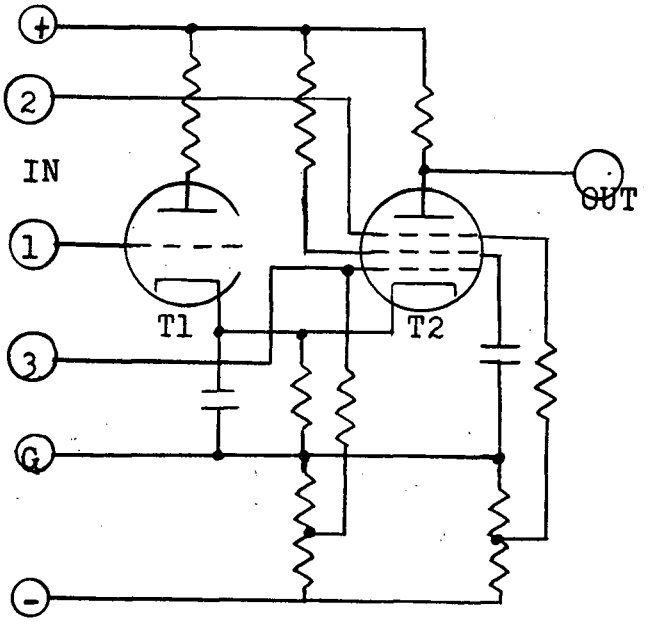
Figure 7-8. Control Flip-Flop and Channel Gates

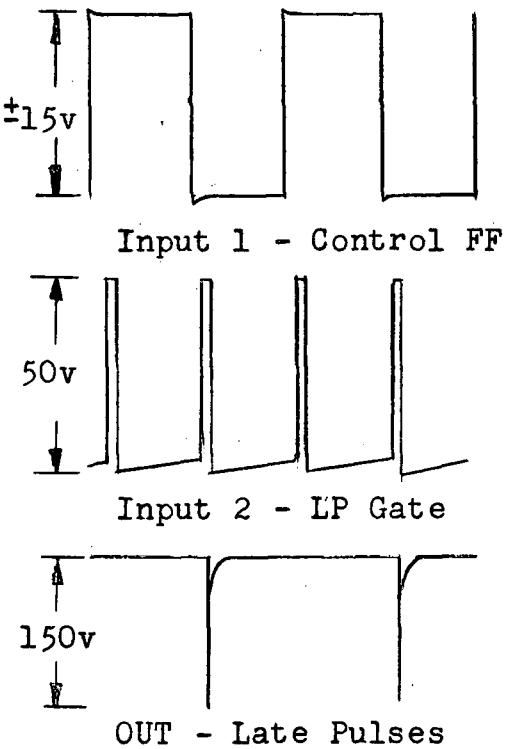
matched tube, the error in the output swing is approximately 10%. Since the operation of the flip-flop is very straightforward, it will not be reviewed here, except to say that a 30-volt trigger pulse is required to effect a change in state. The input and output waveforms are illustrated with the circuit diagram.

In the channel-gate arrangement, the control flip-flop outputs are added at the suppressor grids of two pentode selector gates. The suppressor is normally biased to cutoff, so that only when the positive-going waveform appears does the tube conduct. The channel-gate train is applied to both control grids through a small decoupling condenser, so that alternate channel gates appear inverted at the pentode output. The two outputs are then taken to separate phase inverters which give both polarities of the ODD and EVEN channel gates at their outputs. Now that the gates are selected, the ODD and EVEN channel pulses are selected in another gating circuit and applied to the ODD and EVEN sweep input flip-flop. These circuits will be reviewed in section 8.

7-9. Late Pulse (LP) Triode-Pentode Gates.

The late pulses, ODD and EVEN, are selected for use in the sweep flip-flops in a pentode-triode gate, shown in Figure 7-9. Two similar gates are required, actuated by the two signals from the control flip-flop, for the ODD and EVEN integrators. The control flip-flop signal is applied to the grid of the triode, so that when this signal is positive, the pentode is biased to cutoff by the current through the common cathode resistor. When





R1	15K	1W	10%	C1	.01 mfd
R2	27K	½W	"	C2	.05 "
R3	68K	"	"		
R4	.68K	"	"		
R5	1M	"	"	T1	½-12AT7
R6	10K	"	"	T2	6AS6
R7	22K	"	"		
R8	270K	"	"		

Figure 7-9. Late-Pulse Triode-Pentode Selector Gate

the signal goes negative, the triode is cut off and the circuit acts like the pentode AND gate of section 7-7. The cathode must be by-passed to preserve the high gain of this type of gate.

7-10. The P- and PO Pulse Selector Gates

The P- and PO pulses, ODD and EVEN, are selected in a pentode AND gate which combines two signals at the suppressor to bring the tube into the conducting state. The signals are the control flip-flop output and the P- or PO coincident gates. The sine-clock pulses are applied to the control grid, and both grids are normally biased to cutoff.

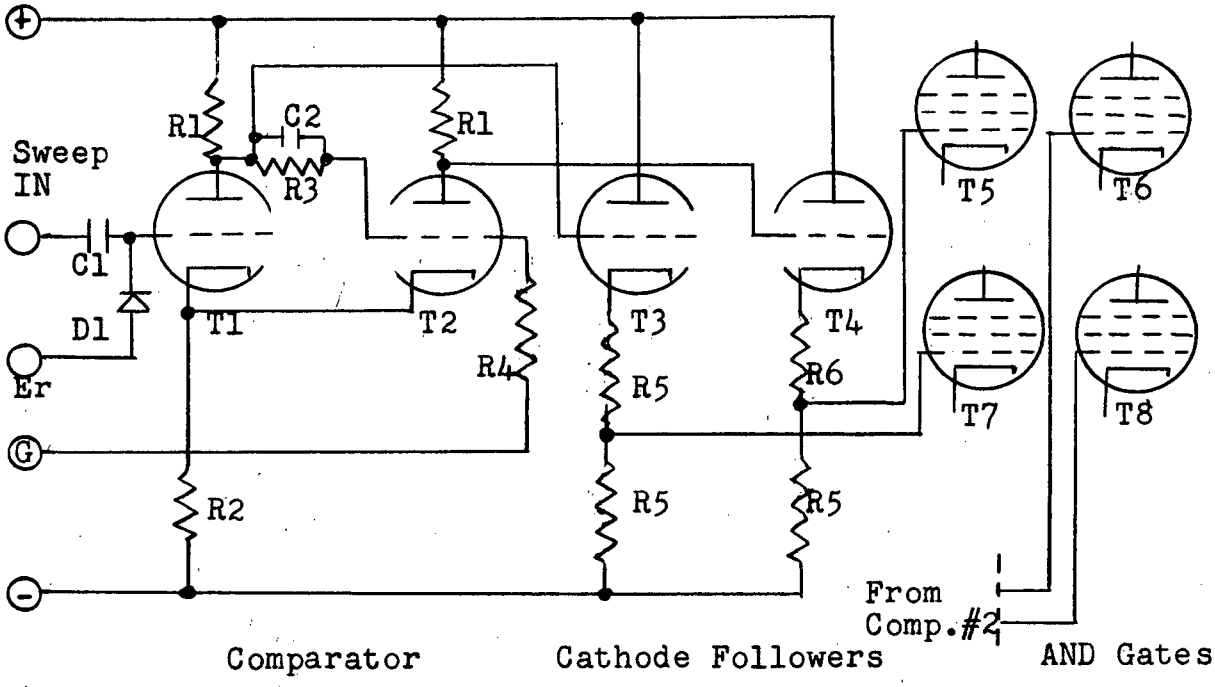
The circuit action is identical to that of the gate of section 7-7 except for the addition of the two signals at the suppressor. Since both signals are derived at low-impedance sources, and the grid draws very little current, the adding circuit is quite efficient. There is virtually no interaction of the sources. The suppressor is biased such that the positive part of the control flip-flop waveform brings the tube to the verge of conduction, and the added coincident pulse brings it into the conducting state. The 15-volt coincident pulse is just sufficient to produce a usable selected SCP trigger-pulse at the plate. Because of the rather critical grid-bias values for this amplitude of input pulse, the power supply must be very stable.

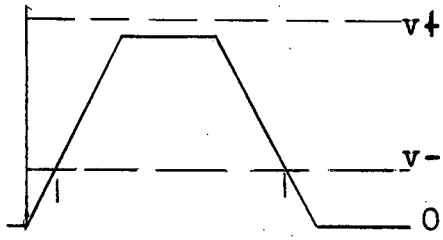
The only pulse circuits which remain to be discussed are the sweep flip-flop triggering circuits. These will be left to section 8, which will also describe the sweep amplifier and zero-comparator circuits.

7-11. The Fine-Channel Schmitt Comparators and Associated Gates

The block schematic arrangement of the fine-scale logical-decision comparators was discussed in section 5. It remains to illustrate the details of the circuit and its interconnection with the pentode selector gates. The circuit of one of the comparators and the associated down-gates is shown in Figure 7-10.

It has already been mentioned that the Schmitt direct-coupled comparator is a bistable circuit which changes state





Sweep Input to T1

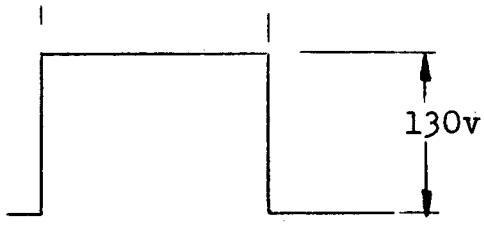
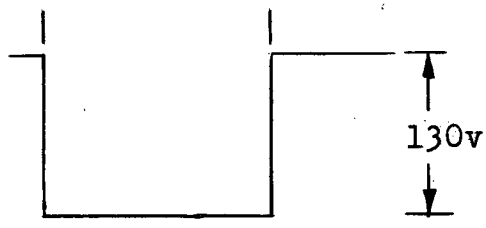


Plate of T2 - OUT



$\frac{10}{9}$ msec

Plate of T1 - OUT

R1	47K	1W	5%
R2	82K	"	"
R3	180K	½W	"
R4	47K	"	"
R5	150K	"	10%
R6	180K	"	"
C1	.05 mfd		20%
C2	.01	"	"
T1,T2	½-12AT7		
T3,T4	½-12AX7		
T5	6AS6		OP Gate
T6	"		P+ Gate
T7	"		EP Gate
T8	"		CP Gate
D1	1N191		

Figure 7-10. Fine-Scale Schmitt Comparators and Down-Gates

whenever the input voltage rises above a particular reference level. The required trigger voltage Er is the difference between the negative bias voltage and the voltage at which tube T1 begins to come out of clamp. The circuit returns to its quiescent state when the input falls below that same level, barring the small hysteresis effect which is always present.[10] For this particular application, a small hysteresis effect, or failure of the circuit to trigger back at the same voltage that it triggered forward, is of no significance.

The cathode follower of the comparator is arranged so that the output when applied to a pentode gate will cause the gate to open when the comparator is in the (+) state, and will cause the gate to block when it is in the (-) state. For the AND gates shown, the comparator must supply a signal which is just below the suppressor cutoff bias in the (+) condition, so that the coincident pulse will turn the tube on the rest of the way. In the (-) state, the comparator must supply a signal which will cause the gate to block the 50-volt coincident pulse. The circuit shown satisfies this requirement with an output signal of -30 volts in the "on" or (+) condition, and a signal of -150 volts in the "off" or (-) condition.

Briefly, the circuit action is as follows: In the quiescent state, both comparators of the block $v- < v_o < v+$ are in the off condition (T1 off, T2 conducting), so that the two output signals cause the gates to block. If the sweep input rises above v-, the first comparator triggers, and if it rises above v+, the second comparator also triggers. The T1 grid bias levels are

such that the first comparator triggers at 1/4 the maximum normalized sweep (approximately 25 volts) and the second comparator triggers at just below 3/4 the maximum normalized sweep (approximately 75 volts). The second unit is set at just below 75 volts to allow time for P+ to be gated should that pulse be chosen to initiate the downsweep. The comparator outputs combine in the arrangement of Figure 5-3 to select the proper pair of pulses for triggering the coarse- and fine-channel downsweeps.

This concludes the discussion of the integrator control circuits. Section 8 describes the circuit details of the sweep input flip-flops, the sweep amplifiers, and the zero comparators.

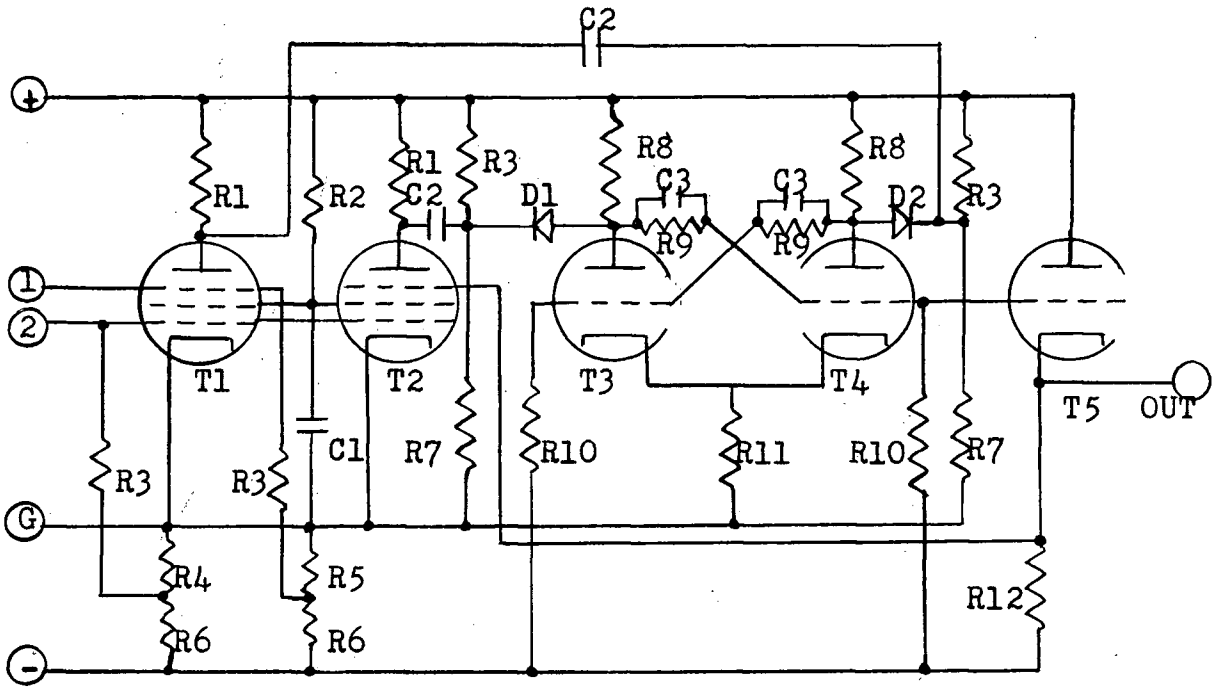
8. Integrator Circuit Details

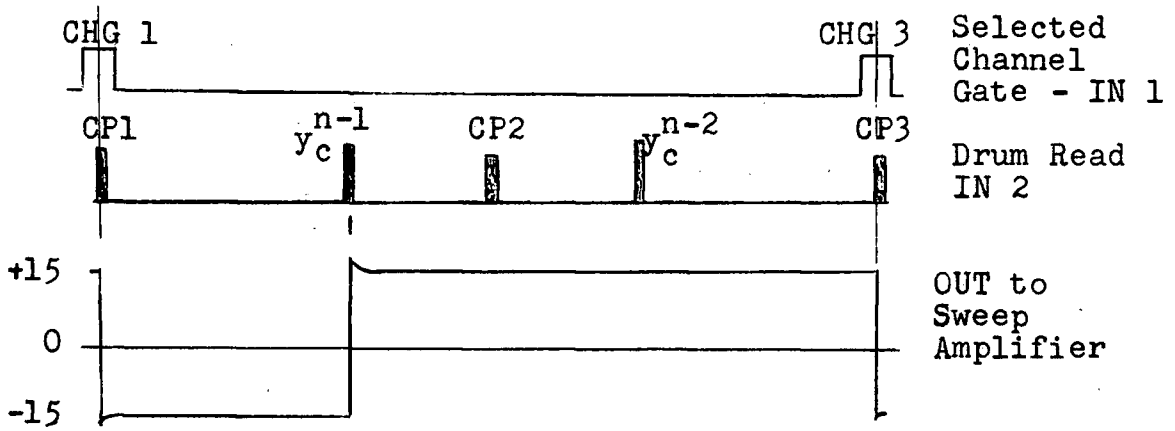
This section is concerned with the details of the input flip-flops and their associated gates, the diode gate sweep inputs, the sweep amplifiers, and the zero comparators. These will be described in order in the following sections.

8-1. Sweep Input Flip-Flops

The sweep amplifier requires a positive or negative step voltage input to produce respectively a negative or a positive ramp output.[10] The input flip-flops, triggered by appropriate pulses, supply this voltage. The flip-flops are standardized to deliver an output of ±15 volts, and are identical to the control flip-flop discussed earlier. A typical input flip-flop and its gates are shown in Figure 8-1.

The circuit action is as follows: The two pentode gates, T1 and T2, receive pulses from the magnetic drum read-head or from some part of the control circuits. In the former case, the magnetic drum is positioned so that, for example, the CP1 gating pulse from the control circuits appears at the same time as CP1 (channel pulse 1) read from the drum. This pulse is amplified in T1 to trigger the flip-flop. The flip-flop is now in the "set" condition, and its output signal turns on T2 to allow it to accept the function pulse from the drum. For the example chosen, the function pulse is y_{co}^{n-1}. This pulse resets the flip-flop through T2, and the sweep input is turned off. Now the input tubes are in their original states, with T1 ready to accept the next channel pulse, and T2 turned off.





R1	68K	½W	10%	C1	.05 mfd	20%
R2	27K	"	"	C2	.01 "	"
R3	1M	"	"	C3	100 mmfd	"
R4	10K	"	"			
R5	18K	"	"			
R6	270K	"	"			
R7	4.7M	"	"	D1,D2	1N191	Germanium
R8	56K	"	5%	T1	6AS6	CP Selector
R9	180K	"	"	T2	"	Py "
R10	270Kww	"	½%	T3,T4	5751	Input Flip-Flop
R11	15K	"	5%	T5	½-12AT7	Cathode Follower
R12	68K	2W	10%			

Figure 8-1. Sweep Input Flip-Flop and Selector Gates

This flip-flop therefore reads the information in the ODD channels into the sweep amplifier. An identical arrangement reads the information in the EVEN channels into the opposite sweep. Obviously a total of four such "read-in" units are required for the four sweep circuits.

In the coarse channels, another flip-flop is required to supply the signal for the down-sweep. As discussed in section 5, this flip-flop turns on with a selected early, zero or late pulse input, and turns off with a pulse from the zero comparator when the sweep reaches zero volts. The output signal is positive, since it must produce a negative-going ramp. The two flip-flops must be in the correct initial state to produce the sweep in the required manner.

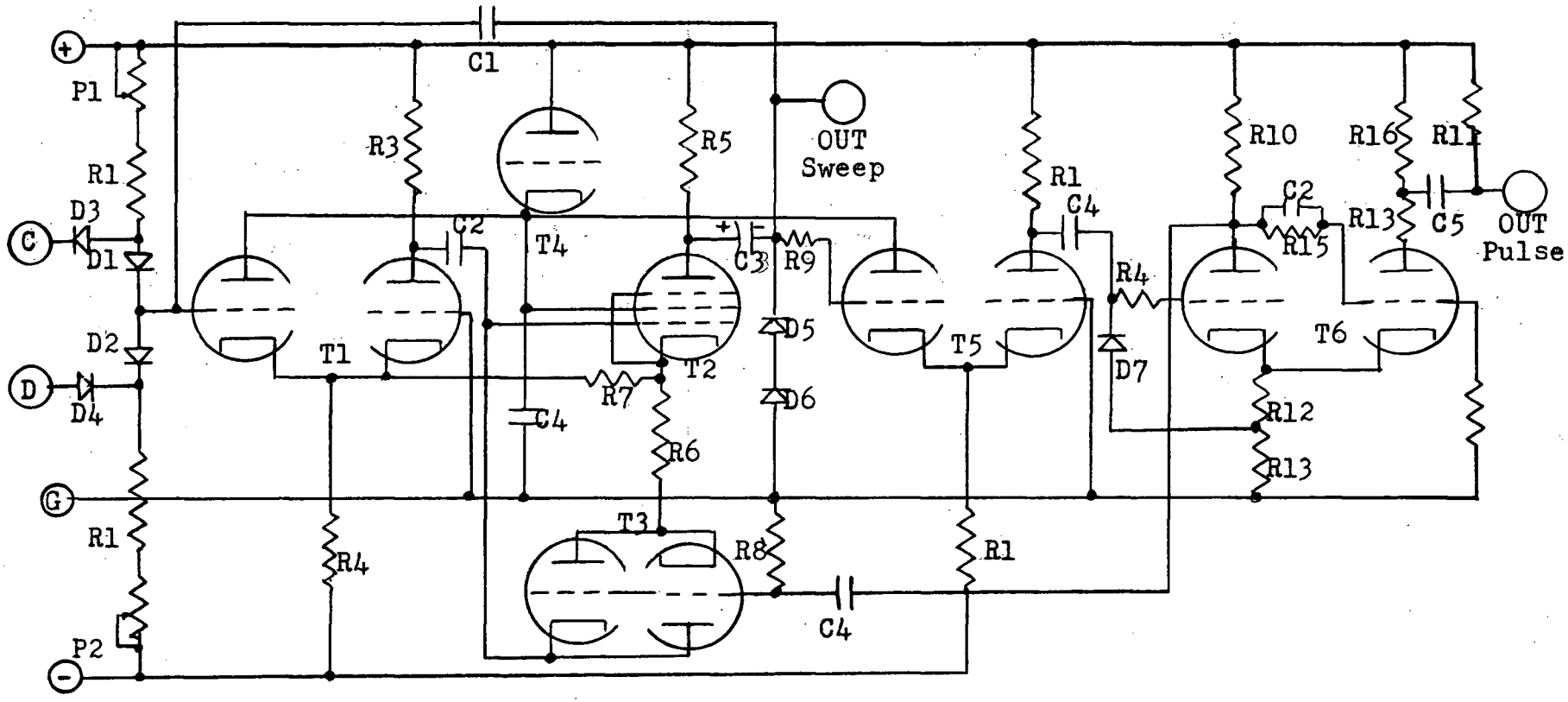
As mentioned in section 5, the fine-scale sweeps require two additional flip-flops. These units are identical to those already discussed, but for a different input arrangement. The first of these flip-flops triggers on the channel pulse and resets on the centre-channel pulse, PO. The signal from this unit causes a negative sweep which when added to the existing sweep, effectively subtracts $\frac{a}{2}$ in the integration operation. The second flip-flop reads the coarse-channel variable, scaled by dt, into the fine scale. Therefore this unit is set by the channel pulse and is reset by the pulse representing the new coarse-channel variable as it is generated by the coarse-scale zero comparator. This flip-flop effectively adds to the sweep the quantity $\frac{y_{co}^{n-1} - a}{2}$. The scaling by $\frac{1}{2}$ of these two inputs is accomplished in the sweep input diode gates (section 8-2).

It is clear that the input flip-flops are elements which translate a pulse position into a signal of accurately-determined time-duration. When this voltage or signal is applied to the sweep amplifier, a corresponding positive or negative ramp of accurately-known amplitude is produced. The sweep circuit which accomplishes this action will now be described.

8-2. The Sweep Amplifier

One of the most critical designs encountered in the integrator circuits is that of the sweep amplifier.[3,10] The four amplifiers must all sweep at precisely the same rate for the same input signal. As mentioned before, it is not important that the gain of the amplifiers is a constant, but the time-constants of the different feedback networks must all be the same. How this is accomplished will be seen later in this section.

The basic function of the sweep circuit has already been described. The circuit details are shown in Figure 8-2. The zero comparator (section 8-3) is also shown. The sweep amplifier has two stages. The first stage T1 is a difference amplifier having a gain of approximately 50. The second stage, a pentode amplifier, has a gain of about -70. The open-loop gain of the amplifier is therefore approximately -3500. This gain is quite sufficient to achieve the accuracy expected in the integration. The mathematical errors inherent in this type of approximate integration will probably exceed any error introduced from the sweep amplifier. The overall gain is negative in order that negative feedback can be used.



R1	270Kww	½W	10%	R9	100K	½W	10%	C1	.01 mfd	1%	T1,T5 5751
R3	180K	"	5%	R10	27K	"	5%	C2	.01 "	20%	T4,T6 12AT7
R4	180K	1W	"	R11	56K	"	"	C3	12 "	electrolytic	T3 12AX7
R5	18K	"	"	R12	1.5K	"	"	C4	.05 "	20%	T2 6AK5
R6	270ohm	½W	"	R13	10K	"	"	C5	50 mmfd	"	
R7	33K	"	10%	R14	330K	"	10%				
R8	1M	"	"	R15	150K	"	5%	D1,2,3,4	1N461		
				R16	15K	"	"	D5,6,7	1N191		

Figure 8-2. Diode Gate, Sweep Amplifier and Zero Comparator

The amplifier has two feedback loops, an inner positive loop and an outer negative loop. The inner loop, from the cathode of T2 to the cathode of T1 through R7, compensates for the loss in gain in T2 caused by not bypassing the cathode, thereby avoiding the use of a bypassing capacitor. The outer loop formed by the capacitor C1 and the input resistor together cause the amplifier to act as an integrator. The time constant R1C1 determines the rate of the sweep. More will be said about this in the discussion of the diode gates later in this section.

One important aspect of the circuit not yet considered is the clamping tube T3. This tube, a back-coupled 12AX7, is biased to cutoff during the entire sweep, so that the grid of T2 is free to receive the negative input signal during this time. The signal for the clamp is obtained from the zero comparator; this will be made clear in the next section. As soon as the sweep returns to zero and tries to go negative, a positive signal of a few millivolts from the comparator drives the clamp tube into conduction, thus dc-restoring the coupling capacitor C2, and effectively holding the grid of T2 at zero volts. The clamp tube acts like a diode except that the action is made very fast through the use of the grid, and the back-resistance is much higher than conventional germanium or silicon junction diodes. Because of this high back-resistance, the capacitor C2 can be made quite small and the time-constant of the coupling circuit still remain very large.

The capacitor C3 is dc-restored by the germanium diodes D5 and D6 in Figure 8-2. A large capacitor is required

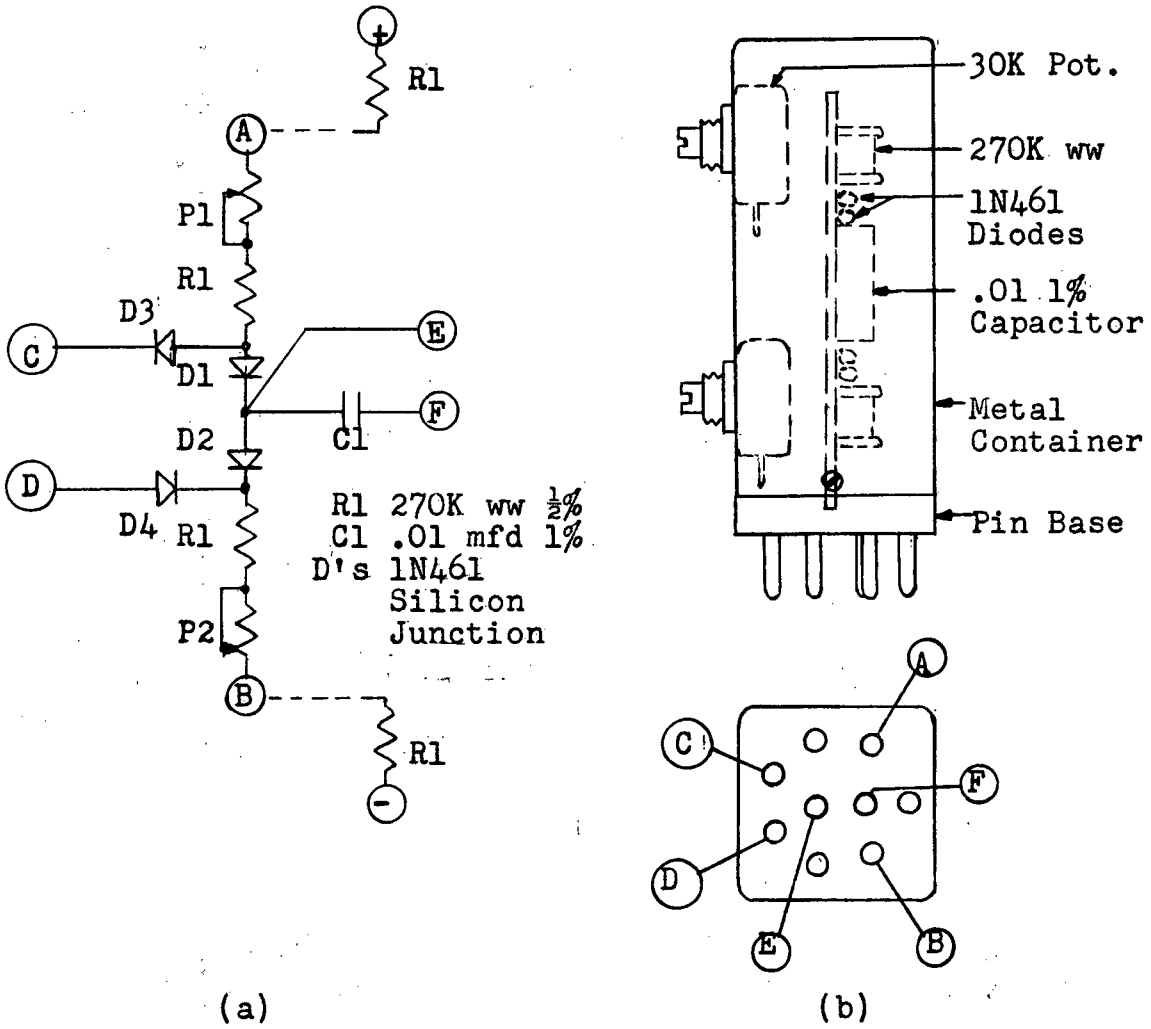


Figure 8-3. Sweep Input Diode Gate

here so that the feedback current is not appreciably impeded. If the impedance presented by this capacitor were large, the sweep would be attenuated and the full linear range of the amplifier would not be used to best advantage.

The action of the diode-gate input will now be reviewed. This type of gate[9] (Figure 8-3) has a positive and a negative input. With no signal applied, a current flows through P1-R1-D1-D2-R1-P2. If a negative voltage is applied to input C from a flip-flop, diode D3 conducts, causing a drop in

potential at the anode of D1. Therefore D1 blocks, and the input grid is connected through D2-R1-P2 to the negative supply. The power supply is stabilized so that the output ramp rises at a fixed rate dependent on the time-constant R1C1 (approximately).

If now a positive signal is applied to input D, the positive supply is connected to the grid through P1-R1-D1, and B- is integrated to give a negative ramp output. The slope of this ramp is the normalized (-1) sweep spoken of earlier, whereas the slope given by the case above is the normalized (-1) sweep. The standard sweep caused by one input is easily calculated from the equation

$$e_o = \int_{t_1}^{t_2} e_i \, dt.$$

If it is assumed that the input resistance is 300K, the input signal is e_i -300v, C1 is .01 mfd, and the integration time is 1000 usec, then it is found from the above formula that $e_o = 100v$.

A sweep rate of approximately half the standard is obtained by simply adding another precision resistor in series with each half of the diode gate (Figure 8-3(a)). The sweep rate obtained is not exactly half the standard because the original input resistance is not exactly R1, but is R1 in series with P1 in series with the forward resistance of diode D1. The error due to this difference is very small indeed, especially since it is taking place in the fine scale. Notice that the two additional resistors are placed external to the plug-in unit in order that the units be interchangeable. Calibration

of the various time-constants is performed in an RC bridge, designed specifically for this purpose. Potentiometers P1 and P2 are required to compensate for variations in the capacitor C1 in the different circuits, since this element is the least exact of the bridge elements.

It is apparent, then, that so long as the amplifier has sufficient gain and is stable, and the input circuit is calibrated, the ramp voltage output will have an accurate and consistent slope. Proper calibration of the time-constants of the input circuits assures repeatability among the four circuits. In addition, the resistance of each half of the individual gates must be the same to assure that the positive and the negative ramps have the same sweep rate.

8-3. The Zero Comparator

The zero comparator delivers an output pulse whenever the down-going sweep reaches zero volts. The circuit is shown in Figure 8-2, tubes T5 and T6. For reliable operation, it is imperative that the comparator pulse coincide very closely with the time that the sweep reaches zero. Any error in the triggering time will be reflected as a cumulative error in the integrator variable undergoing operation.

The comparator consists of a direct-coupled flip-flop, T6, preceded by a difference amplifier, T5. In the quiescent state, the input is at zero volts, and T6(a) is cut off by the cathode current flowing through T6(b). The clamp tube T3 is ac coupled from T6(a); its grid is at zero volts in the quies-

cent state, so that the grid of T2 is clamped at zero.

When the sweep starts to go positive, a large positive signal (amplification 60) appears at the output of T5 and triggers the flip-flop. The flip-flop bias levels are adjusted so that it will trigger on a 3-volt signal; this corresponds to something less than the first 0.1 volt rise of the sweep voltage. When regeneration occurs, T6(a) conducts heavily and its current bieases T6(b) to cutoff. Simultaneously, the grid of T3 is driven negative, so that T3 is biased to cutoff and the grid of T2 is free.

After a decision in the fine-scale, the sweep-down begins. When the sweep falls to approximately 0.1 volts, the grid of T6(a) begins to cut off, regeneration occurs, and the original tube currents are quickly restored. As soon as the flip-over is accomplished, a negative pulse from the differentiated plate waveform of T6(b) turns off the flip-flop which supplies the signal for the downsweep, and the sweep is clamped at zero by the clamp tube, T3.

In the coarse scale, the negative trigger from the comparator is used to generate the 10-microsecond coincident pulse required to gate the sine-clock pulse representing the integrated variable. In the fine scale, a positive pulse is taken from T6(a) to represent the variable directly.

This concludes the discussion of the circuit details of the integrator. The results of the tests of the basic units and a summary are presented in section 9.

9. Testing the Circuits

9-1. Introduction

In testing the apparatus, the main object was to determine whether the sweep circuits could function as a dynamic storage unit. The arrangement is technically described as a pulse-selection analogue dynamic storage unit. The digital computer counterpart of this unit is a dynamic storage register. The basic mechanism of this type of register is the following:[10]

> The word (pulse train) is introduced at one end of a delay line whose delay time is equal to the time-duration of the word, and the output signal is returned to the delay-line input so that the word continues to circulate around a closed path.

The test devised uses the two coarse-scale units, and comprises three basic steps. First the sweeps are made to function from a selected group of pulses. When they are functioning properly, the two circuits are connected in series so that the information injected into the first circuit is read into the second circuit. Next, the output of the second circuit is returned to the input of the first, and the synchronizing source disconnected, so that the injected information is recycled between the two sweeps. The final test is to inject a pulse which effects a small subtraction from the value of the stored function. After subtraction, the sweep recycles the remaining information. Details of the test procedure will now be described.

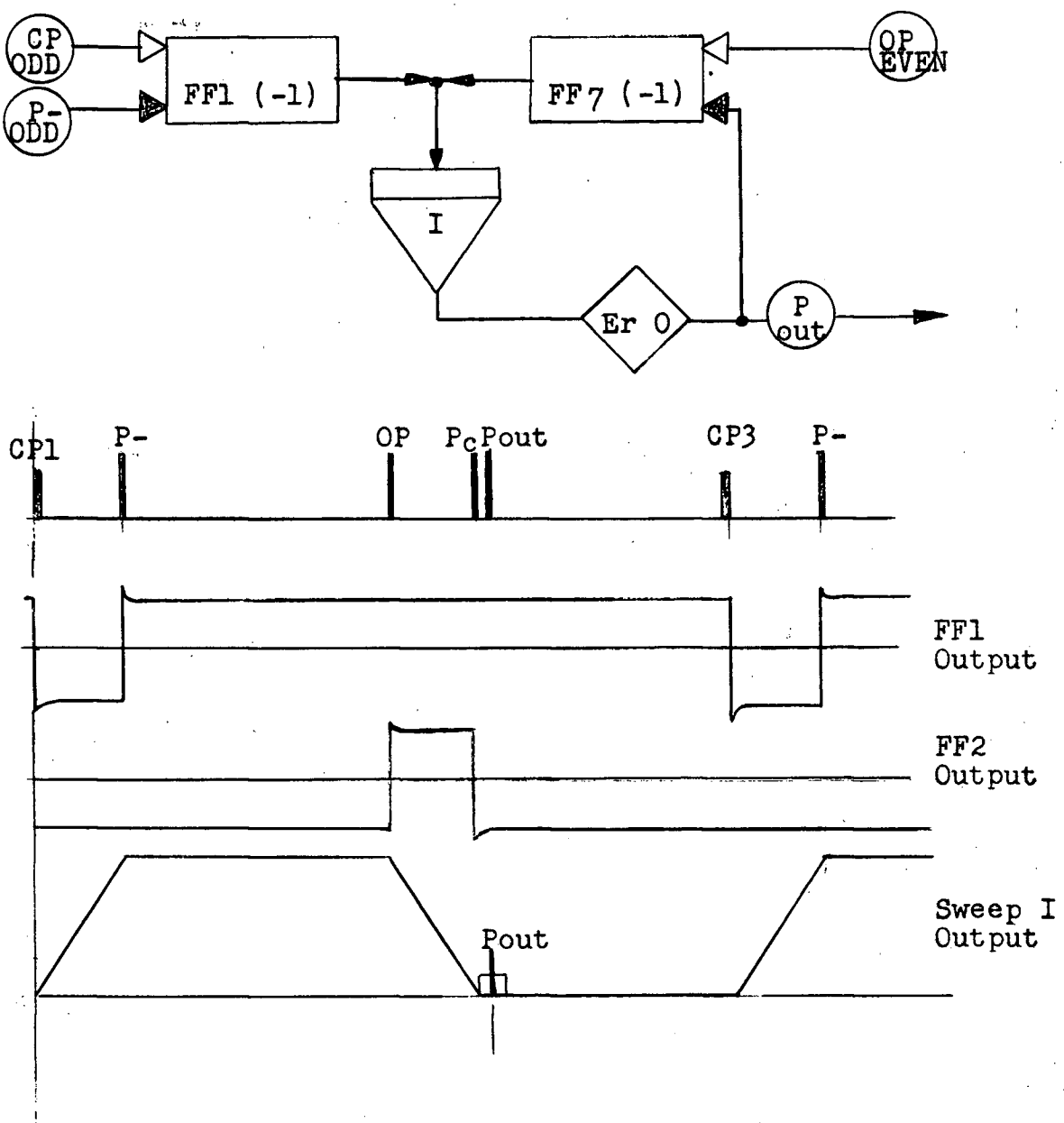


Figure 9-1. Block and Waveforms for Coarse Integrator I

9-2. Basic Operation of the Sweep Circuits

The block-schematic arrangement for the first test of the sweeps is shown in Figure 9-1, where the ODD coarse-channel sweep and its waveform are illustrated. The flip-flop FF1 is triggered by channel pulses CP1, CP3, etc., and is reset by the ODD P-pulses. That is, P- is used to simulate the function

pulse which, in the normal operation of the computer, would be read from the magnetic drum. The downsweep, controlled by FF7, is initiated by the zero pulse, OP, which is selected into ODD and EVEN pulses for purposes of the test. The OP is the downsweep pulse which corresponds to a decision in the fine scale to produce no change in the coarse-scale value of the function. The comparator pulse resets FF7.

For this group of fixed pulses, the selected output pulse should correspond exactly to the P- EVEN pulse if the ODD circuit is functioning properly. As nearly as could be determined by the oscilloscope, the coincidence between the output pulse and the P- EVEN pulse which is generated from the clock signal is within 1 microsecond.

The results of this test indicate the following: First, the input flip-flops, sweep amplifier and zero comparator must all be functioning satisfactorily in order to produce the waveforms shown. The fact that the output pulse coincides within 1 microsecond with the selected P- pulse indicates that the zero comparator is functioning according to design. With the second coarse-channel triggered by the CP2, CP4, etc., P- EVEN, and OP pulses, a similar result was obtained. The amplitudes of the two different sweeps were not quite the same because of a slight unbalance in the time-constants. For purposes of this test, this difference is of no consequence. In the fine-channel circuits, however, the exact calibration of the time-constants is very important, because the sweeps trigger comparators which select the downsweep-initiating pulses for

both the coarse and fine-scale circuits. A mismatch here may seriously affect the action of these comparators and their selector gates.

9-3. Dynamic Storage Test

The block-circuit and waveforms for the test as a dynamic storage are illustrated in Figure 9-2. The circuit action is as follows: Initially, with switch S1 in position 1, the simulated function pulse P- is injected into the EVEN sweep via FF2. The output of this circuit is the selected SCP which should correspond to the P- ODD pulse, and is used to terminate the ODD upsweep as illustrated (point 1 on the waveforms). The output of the ODD sweep should then correspond to the second P- pulse. It appeared upon examination of the open-loop waveforms that the sweeps were functioning properly.

At this time, the switch S1 was thrown to position 2, disconnecting the P- pulse input and injecting the P_{out_I} pulse in its place. If the two pulses corresponded exactly before switching, and if the switch was disconnected somewhere during the level portion of the two sweeps, then the pulse recycled with no noticeable change in the sweep waveforms. Of course, this switching procedure is crude, because there is a time lasting over several cycles that the loop is disconnected. The switching interval is illustrated in Figure 9-2. While the source is disconnected, the sweeps must hold at either 0 volts or at V volts, in order that the operation continue as before (point 2 on the waveforms) once the switching complete.

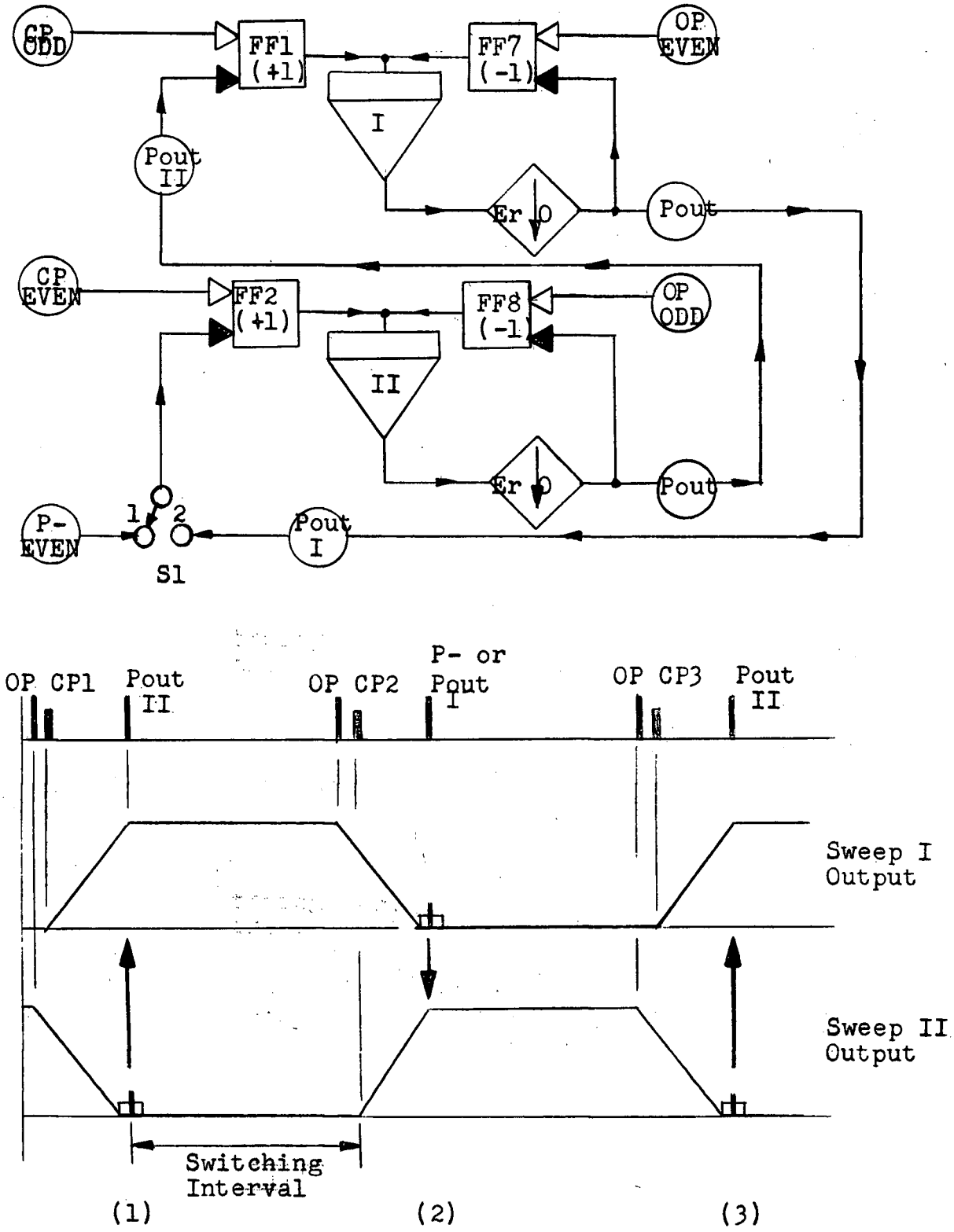


Figure 9-2. Dynamic Storage System and Waveforms

It would not be difficult to devise an electronic switch which would remove this erratic behaviour during switching, but it was found that a successful switchover could be made in about 50 percent of the number of attempts, so that a more elaborate setup is impractical.

Once the switchover was completed successfully, the stored pulse usually recycled for anywhere from several seconds to 10 or 20 minutes. The factors which cause the pulse to be lost are, (1) accumulated drift due to small voltage variations in the sweep which eventually cause the selector gate to choose a pulse on either side of the recycling pulse, and (2) mechanical disturbances of the tubes, which are reflected in the sweep waveforms. In the first case, the selection of a pulse other than the recycled pulse would in effect cause an addition or subtraction on the stored pulse which would throw the sweep off scale in either direction in a matter of a few milliseconds. Therefore it was impossible to detect the exact cause for the loss of the pulse.

Probably the best criteria of how well the circuit is storing information is the Figure 9-3 showing the output pulse from the ODD sweep, triggered on the injected P- pulse, which is now disconnected from the circuit. Since the leading edge of the P- pulse is about 0.2 microseconds long, there will not be more than this amount of deviation in the triggering point. The output shows, then, that the 300-volts drop of the leading edge of the pulse which is being recycled lies within 1 micro-

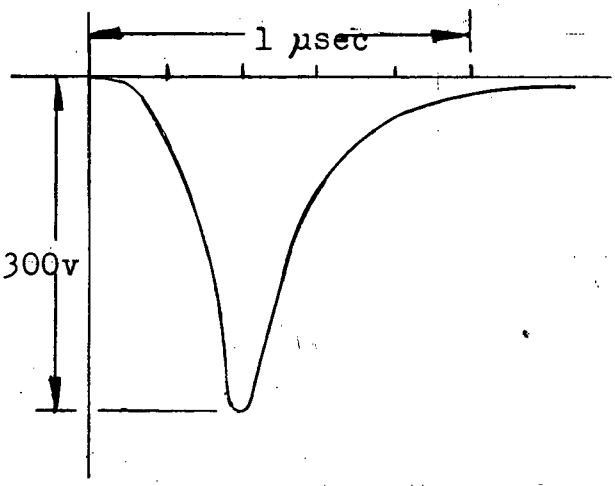


Figure 9-3. Recycled Function Pulse Triggered on P-

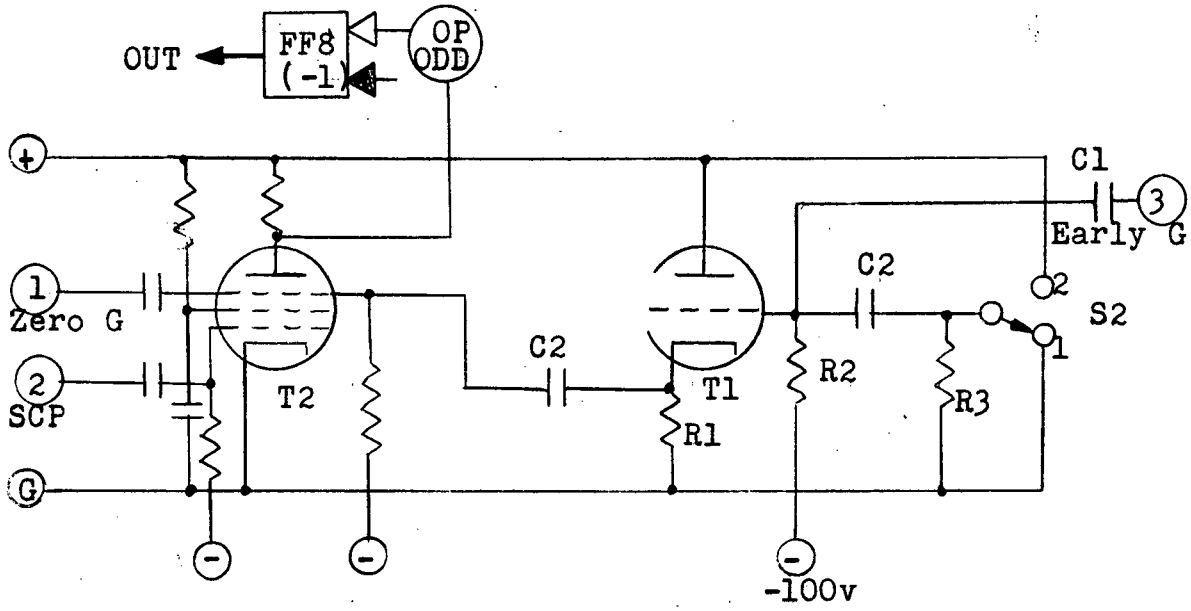
second of the leading edge of the injected pulse. It is felt that with the existing gating methods, this performance is unsurpassable. It is possible that with different gating methods and flip-flops (for example, using very fast-switching, low-impedance transistors) much better results can be achieved.

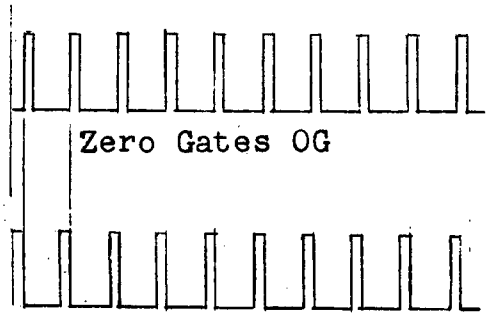
9-4. Incremental Subtraction from the Stored Pulse.

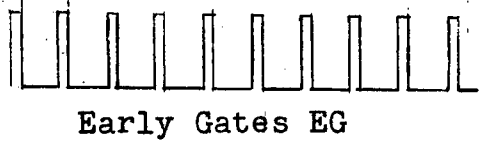
In the operation of the integrator, it is necessary that a small increment be added to or subtracted from the stored pulse without causing the circuit to go unstable. This action was simulated in a test arrangement which makes use of the dynamic storage just described.

The injection tube and its connection for effecting a subtraction in the stored pulse is shown in Figure 9-4. It is more convenient to perform a subtraction rather than an addition because of the arrangement of the existing circuits.

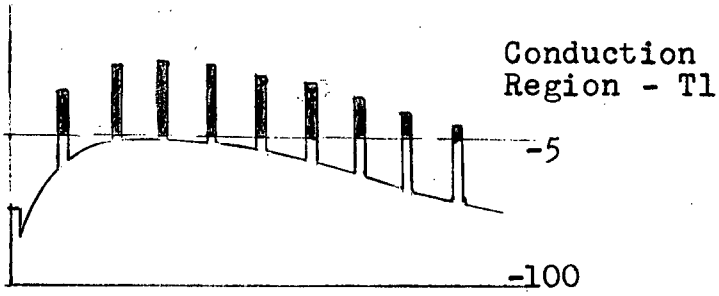
Flip-flop 8 of the previous circuit receives the







R1	15K	1W	10%
R2	56K	½"	"
R3	1M	"	"
C1	100 mmfd		20%
C2	.01 mfd		"
T1	½-12AT7		
T2	6AS6		



Injected Early Gates

Figure 9-4. Incremental Subtraction by Pulse Injection

injected pulse from the tube T2. This tube is already in the circuit of 9-2, but is not shown. The additional circuitry required is the injecting tube T1 which supplies the early gate to the OP gating tube, T2. The action is described briefly: Initially, T1 is biased to cutoff and S2 is in position 1. To perform subtraction, the circuit is first made to function as a dynamic storage. When the sweeps are functioning properly, switch S2 is closed. This introduces a step of B+ volts at input 3; the step is differentiated at the grid of T1 to form a short pulse. This pulse is added to the incoming EG pulses, as shown in Figure 9-4, and the added pulses bring T1 into conduction and thus allow several pulses to be gated. The addition of these pulses at the grid of T2 allows the EP pulse to trigger into FF8 in front of the OP pulse for several cycles of operation.

Suppose for example that two EP pulses are gated. The first pulse will cause an incremental subtraction in the ODD sweep, and the new value will be cycled to the EVEN sweep. Therefore the amplitude of the sweep will drop approximately 1/100 of the maximum sweep voltage, or about 1 volt. If now a second EP pulse is gated, the ODD sweep subtracts another incremental position from the stored pulse, which is again cycled to the EVEN channel. It is evident that if a burst of EP pulses is injected, as is done here, then the sweep waveform will decrease in amplitude several volts with each burst, or each time the switch S2 is closed. After each burst, the OP pulses take over once more, and the amplitude of the sweep holds at whatever value

it has reached. This type of subtraction was achieved successfully with the circuit illustrated. There is no obvious reason why addition could not be carried out with equal ease. It would be necessary to devise a circuit which would block the OP pulse and inject instead the LP pulse for a few cycles of operation.

The ultimate test would involve use of the magnetic storage drum for introducing the variables. Because of the complexities involved, and the improvements which first should be made in the integrator, such a test is not feasible at this time. On the basis of the tests outlined, it may be stated that the design of the basic integrator units has been successful.

9-5. Summary and Recommendations.

From the tests of the basic circuits, it can be concluded that integration based on the method outlined in the thesis is feasible and worthy of further study. The present arrangement of gating tubes and sweep amplifiers will probably give results to an accuracy commensurate with the errors introduced by truncating the Taylor series after the first derivative. As was pointed out in section 3, it should be emphasized that an integrator error of even 5 percent to 10 percent is tolerable in many problems of systems simulation, since the integrator error does not accumulate as do the errors in the other arithmetic circuits. However, assuming that an accuracy of 1 percent is desired over a reasonably long integration, the following recommendations are made:

1. Accurate triggering of the zero comparator is worthy of further study, because the comparator action probably contributes more to drift than any other single element in the circuit. If the comparator has a triggering error of 1 microsecond (this appears to be the approximate error in the existing arrangement), and if this error accumulates, then in 10 incremental integrations the triggering point could drift enough to cause the addition or subtraction of 1 in the coarse scale. This magnitude of error is intolerable for any precise problem solutions.

2. Calibration of the sweep amplifier time-constants in the plug-in units of Figure 8-3 was found to be very critical. It is recommended that the carbon-resistance potentiometers be replaced with 5K or 10K wire-wound trimmers in order to better define the calibration point.

3. With regard to the mathematical errors involved, a definite improvement can be made by simply extending the principle of operation outlined to include higher-order derivatives. For any precise solutions involving a lengthy computer run, this is imperative. This is theoretically possible because the higher derivatives are already present as function pulses stored on the magnetic drum. Before attempting this, however, the long-term drift stability of the circuits

should be investigated. This would include the drift effects inherent in the storage drum, which have not been at all considered in this thesis.

4. The circuits, particularly the flip-flops and selector gates, could be greatly simplified by the application of fast-switching transistors (Pulse and Digital Circuits, 10, pp 598-606). In the prototype integrator, approximately 100 vacuum tubes are used. Some of these tubes are applied to other parts of the computer as well, but about 75 of them are used just for the integrator. This does not include the ring counter (Appendix B), which could also benefit by application of transistor circuits. Of these 75 tubes, about 35 are used for pulse gating requirements, and 13 of them are bistable flip-flops. These 48 tubes could be easily replaced by transistors, as in the literature cited; this would save enormously on space and power requirements, and would greatly simplify the circuitry. The circuit of the sweep amplifier could also be simplified by application of the circuit shown schematically in Figure 9-5. This is a two-stage balanced amplifier with direct-coupling between the stages, but with ac-coupling at the output. If the output stage uses a wide grid-base tube (eg. 12AU7) then the drift in the first stage can be tolerated, so long as the tube is still operating in the linear portion of its

plate characteristics. This arrangement eliminates the interstage ac-coupling network, composed of the condenser C2 and the clamp tube T3 of Figure 9-2.

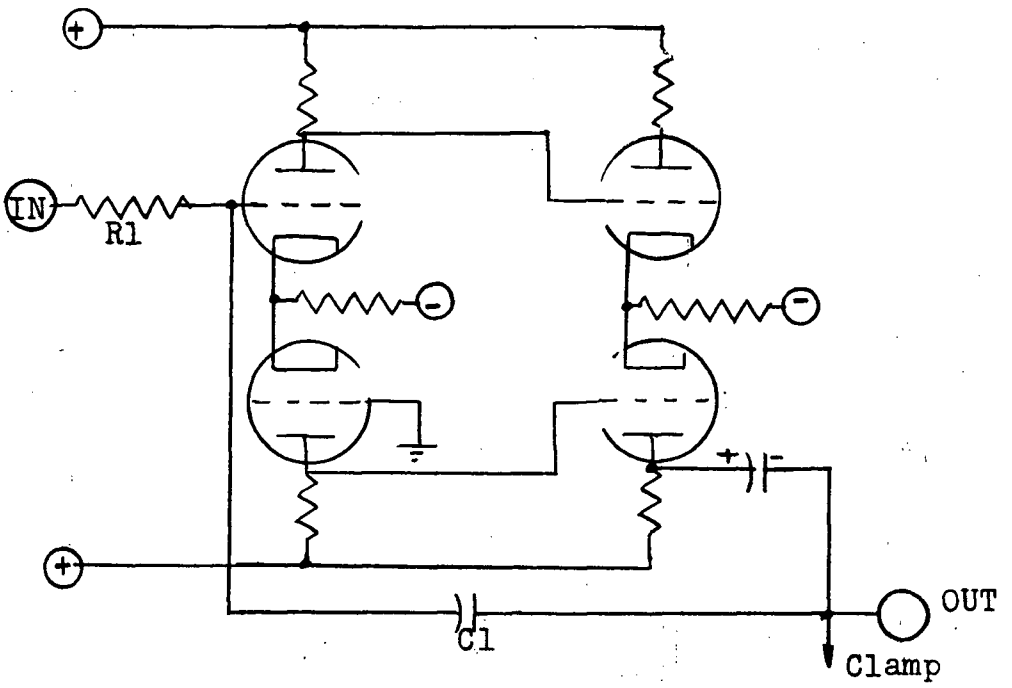


Figure 9-5. Proposed Sweep Circuit

The above are a few of the points which require further study before construction of the final prototype integrator is attempted. From the results of the investigation outlined in this thesis, there appears to be no great obstacle in the way of attaining integration to 1 percent accuracy.

Appendix A. Recording Devices

The integration operation is very fast, and for many applications a continuous recording device is impractical because of the lengthy response time of the recorder. The recorder is therefore usually more of a sampling device, and the integration operation is stopped while the record is being taken. In order to see the high-speed variations taking place during integration, an oscilloscope would be required. Such a device would be useful only as a qualitative measure of the operation, that is, to see whether or not the integrator is working.

One possible system of reading the functions at a particular point in the operation is illustrated in the Figure A-1. In order to use this system, the erase and rewrite operations must be blocked, so that the sweep circuits are continously reading out a fixed value of the function. If sampling at a certain interval is required, an electronic switching device which blocks the operation after a specified number of incremental integrations can be used. Assuming that the operation has been blocked, the circuit of Figure A-1 will function as follows:

Channel pulse 1 sets FF1 and FF2. The outputs of these two flip-flops are of opposite polarity and are added in the circuit represented by block A (or they are of the same polarity if the adder has a negative input). The adder delivers a positive or negative output during the time that

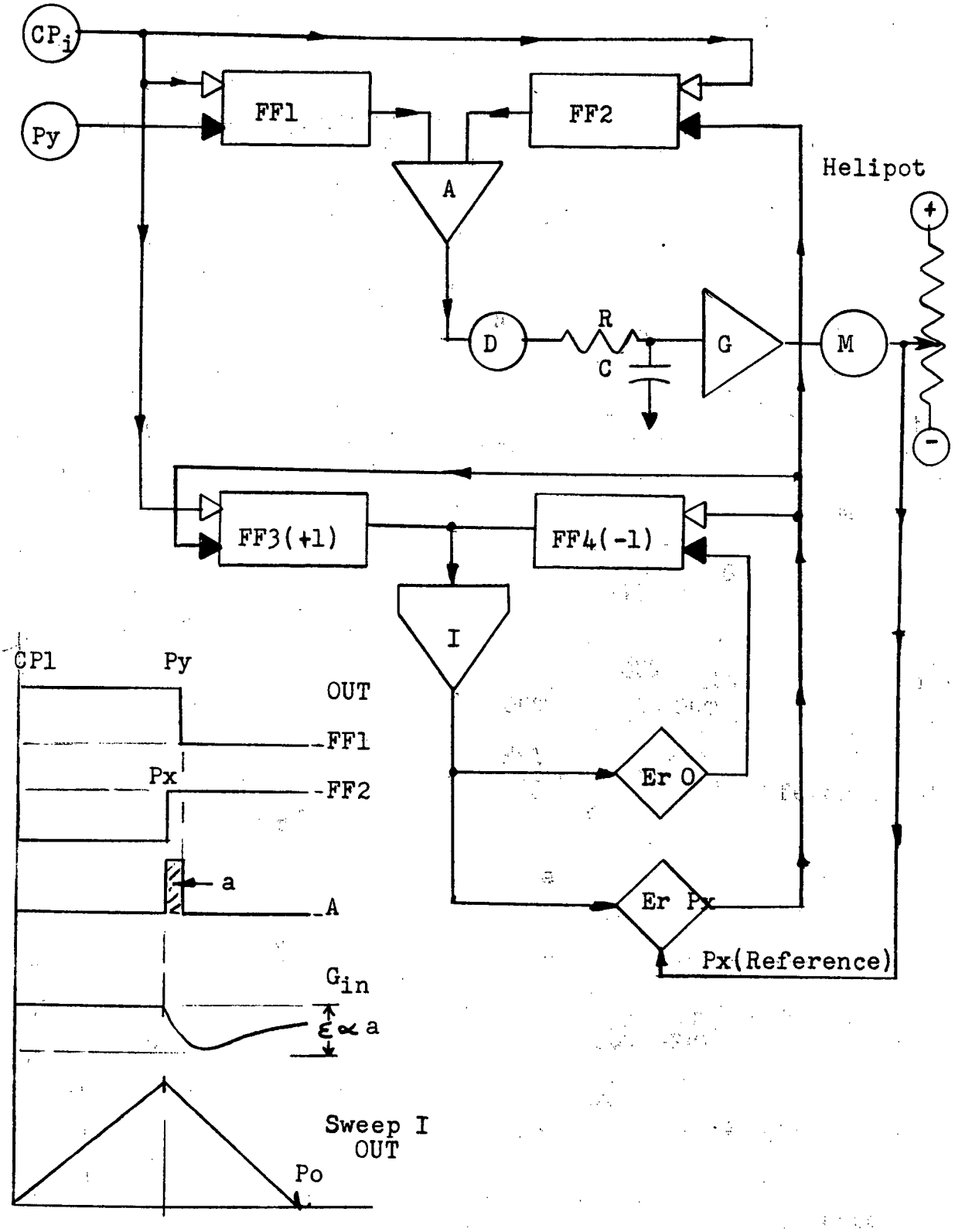


Figure A-1. Servo Read-Out System

the two signals do not cancel one another. The flip-flop FF1 is rest by the function pulse Py. Channel pulse 1 also sets FF3, causing the Sweep I to begin sweeping positive.

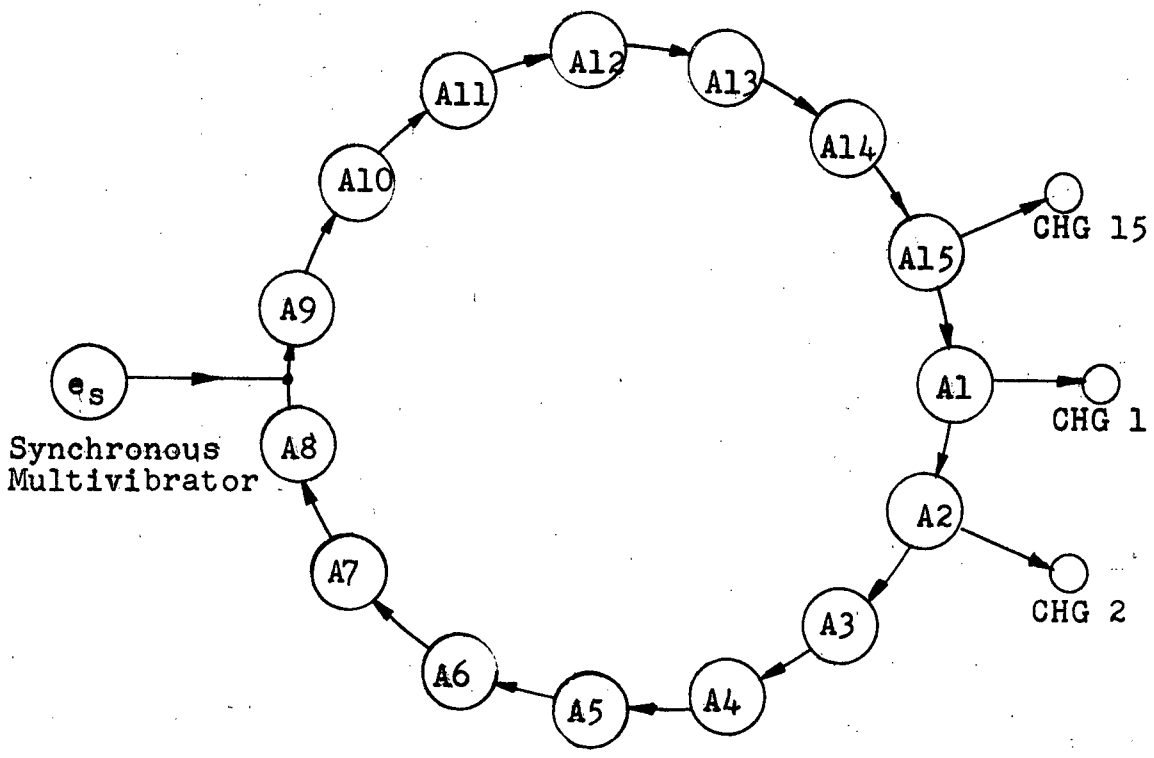
Assume that the potentiometer driven by the servo motor is set near the voltage which (when translated into a pulse position) represents Py. Now Sweep I rises until it reaches the voltage setting of the potentiometer; then the comparator generates a pulse Px, which is an approximation to Py. The pulse Px resets FF3, and sets FF2 and FF4. The Sweep I falls until the zero comparator resets FF4. It may be seen from the waveforms that a positive or negative signal is obtained at the output of the adding circuit. This signal is detected and then integrated in a RC circuit to give at the input to the servo amplifier an error signal proportional to the area of the adder output pulse. The amplifier then applies the signal to the motor, and the servo positions the potentiometer accordingly. Since the function pulse is being read continuously, the servo should position the potentiometer at the correct voltage representation of Py within a very brief time.

An alternate method of recording is to use a similar arrangement, but to set the potentiometer manually. The pulses Px and Py could be observed on an oscilloscope. Either method should give accurate results, but the servo system is simpler to operate. The functions in any channel can be read by this method by selecting the desired channel-pulse input from the ring counter. This could be done very easily with a rotary switch connected to the various ring-counter outputs.

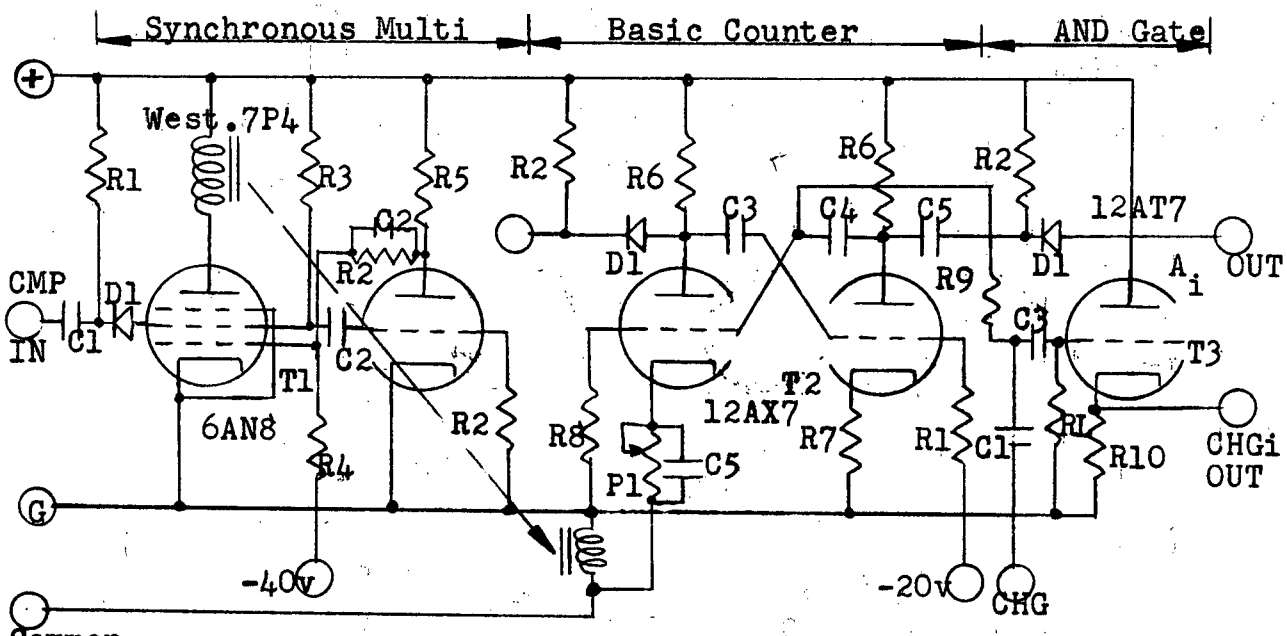
Appendix B. The Ring Counter

The ring counter is used to generate the individual channel gates. The circuit is shown block-schematically in Figure B-1(a). The device consists of 15 astable multivibrators (A1, A2, A3, ..., A15) connected in series and closed in a loop. Each such multivibrator or counter has two unstable states, and the time duration of each state, for a fixed number of counters in the ring, is determined by the frequency of a synchronizing pulse.

The details of a particular counter in the ring are shown in Figure B-1(b). Tube T2 is the counter, T1 is the synchronizing tube, and T3 is the AND gate which uses the signal from this particular counter to select a particular channel-gate pulse. The circuit action is as follows: The synchronizing tube is triggered from the channel-marker pulses, which occur just before the channel pulses. In order to obtain a signal from the ring counter which blankets the channel-gate pulse, the "synchronous multivibrator" (T1) is given a period of about 500 microseconds, so that its output pulses from the pulse transformer is approximately 180° out of phase with the channel pulse PRF. At any instant of time, only one of the counters is in the (1) state (T2(a) conducting, T2(b) cut off), and the remainder are in the (0) state. Say for example that A1 is conducting, and that the current which it draws through the common cathode of T2(a) sets all the other counters into the (0) state.



(a) Ring Counter Block Schematic



(b) Circuit Details

R1	1M	½W	10%	R5	39K	1W	10%	P1	50K pot.
R2	100K	"	"	R6	56K	½W	"	C1	.001 mfd
R3	100K	1W	"	R7	33K	"	"	C2	.0027 "
R4	150K	½W	"	R8	560K	"	"	C3	.02 "
R9	330K	"	"	R10	1K	"	"	C4	.25 "
								C5	250 mmfd

Figure B-1. The Ring Counter

Suppose now that a pulse is injected into the secondary of the pulse transformer from the synchronous multivibrator. This pulse drives the common cathode positive, causing the current in T2(a) of A1 to diminish. Regeneration occurs, and immediately after the pulse has passed, A1 is triggered into the (0) state. Simultaneously, A2 is triggered into the (1) state, because it is the only one of the 15 counters which receives a trigger pulse on both the cathode of T2(a) and the grid of T2(b), the latter from the differentiated plate waveform of T2(b) of A1. Therefore the ring counter has changed by one the position of the conducting multivibrator around the ring. The next trigger pulse causes A2 to return to the (0) state, and triggers A3 into the (1) state. This action is repeated around the loop, so that each of the 15 counters conducts for 1/15 of the total time.

If the synchronizing signal is a PRF of 1000 cps, then each counter unit will be on for 1 millisecond, and off for the next 14 milliseconds. The output from each counter is a 45-volt pulse, lasting about 1 millisecond, from the grid of T2(a). The output from each counter is taken to a triode AND gate, identical to T3 in Figure B-1(b), where it is added to the 10-microsecond channel-gate pulse train. Therefore the output of A1 is CHG1, and of A2 is CHG2, and so on up to CHG15. These output pulses are then applied to pentode AND gates to select the sine-clock pulses which represent the channel pulses, CPi. These pulses are then used in the general programming of the computer, and no t specifically for the integrator.

Appendix C. List of References

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