A VERSATILE DIGITAL-TO-ANALOG FUNCTION GENERATOR AND MULTIPLIER

by

LASZLO TAMAS LOVAS

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Department of ELECTRICAL ENGINEERING

The University of British Columbia,
Vancouver 8, Canada.

Date MARCH 13, 1964

ABSTRACT

This work describes the design, construction, and testing of a digital-to-analog function generator and multiplier for analog computation and non-linear system simulation.

The unit consists of two separate channels each of which is fed by a punched paper tape. Functions (of time) are represented on the tapes in binary code and are read into the machine photoelectrically. In one channel, voltage sources of constant value but of either polarity are switched into the parallel branches of a ladder network in accordance with the incoming digital information. As a result of the particular choice of resistor values in the ladder network the voltage at one end of the resistive network is proportional to the binary number signified by the polarity combination of the voltage sources. In the other channel the function represented on the tape controls the polarities of the voltage sources, and the magnitudes of the source voltages are changed according to a second function, which results in an output voltage proportional to the product of the two functions. This second function may be generated independently in the first channel, or it may be an external computer variable.

One level on each tape is reserved for the generation of control pulses which can be used to de-energize the reset relay in the computer, i.e. to initiate the compute mode. The variable tape speed and gain controls greatly enhance the versatility of the device and render it very useful in analog computer simulation studies.

Error analyses of two resistive decoding networks are

outlined and their results are considered in the final choice of the decoding network. Complete circuit diagrams with short explanations of their operation are presented. Results of tests on accuracy, speed and general performance are summarized and illustrated.

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1. INTRODUCTION

The analysis of complex systems by means of simulation on a large scale analog computer has created an ever increasing demand for better function generators. The large number of different generators available today indicates the great deal of effort put into improving the performance of these devices.

The functions used in analog computation are of two basically different types. Those having a monotone increasing independent variable, such as time, as their argument represent one kind, while the other kind may depend on any arbitrary computer variable. Most function generators lend themselves to generation of both types of functions, but some are limited to the generation of only one type of function, for example, the diode function generator which generates functions of arbitrary computer variables, or the photoelectric function generator which generates time dependent functions by representing them on photographic film.

The line of development of function generators starts back in the days of the mechanical differential analyzer, since even in the age of mechanical computation, people soon realized the need for function generation. As a result, the so-called input table[2], a purely mechanical function generator, was devised. The input table consisted of two perpendicular shafts

placed along adjacent edges of a table. Two pointers, one attached to each shaft, moved along the shafts at a rate proportional to the rate of rotation of the corresponding shaft. A plot of the desired function, say f(t)*, was placed on the table. One of the shafts was driven proportional to the variable t, while the other shaft was driven manually in such a manner that the intersection of the two pointers followed the plot of the function. The position of the manual shaft represented the function f(t). Since quantities in the mechanical differential analyser were represented by shaft positions, it was an easy matter to couple the input table to the mechanical computer.

The next phase of development was marked by the introduction of contour potentiometers and tapped potentiometers (1), both of which are still in use today. The latter kind consists of a linear tapped potentiometer whose wiper is usually servo-set proportional to the variable t. The tap points are connected to voltages proportional to the required function f(t). As the wiper moves along the potentiometer, the potential on the wiper represents a linear-segment approximation of the function f(t). In the case of the contour potentiometer the wiper is specially shaped so that it makes contact with the linear potentiometer at a point where the potential is proportional to the function f(t). Another variation of the contour potentiometer is made by shaping the potentiometer itself

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* Throughout Chapter One the symbol f(t) will mean a function of t, where t is either an independent variable representing time, or an arbitrary computer variable.

according to the desired function (i.e. exponential, logarithmic, sine - cosine, etc.). A major disadvantage of the contour potentiometer is that either a specially shaped potentiometer body or a wiper has to be prepared for each function to be generated. Consequently, the contour potentiometer is satisfactory for function generation only when the same function has to be generated repeatedly as, for example, in flight simulators. A serious disadvantage of the tapped potentiometer is the time required to set up a function. As the voltage at a given tap is adjusted, it affects the setting at every other tap. With experience the excessive set-up time can be reduced considerably. Also, special calibration equipment and procedures are available which help shorten the set-up time, but diminish the simplicity and economy of function generation by potentiometers. Another disadvantage is low speed, since this type of generator is semi-mechanical.

Perhaps the best-known of all are the diode function generators [4]. Containing no mechanical parts they were the first high-speed function generators developed. The diode function generator approximates the desired function by straight-line segments whose slope, and in most models the break points as well, are adjustable. (The intersection of two straight lines is called a break point). In the more expensive models a high-frequency "dither" signal is used to smooth the sharp break points to yield an even better approximation to the desired function.

Another group of electronic function generators makes use of photoelectric principles. The photoformer [2] is probably the

best known among these devices. It consists of a cathode ray tube (CRT), a mask, and a photocell. The horizontal sweep of the tube is made proportional to the variable t. The mask is a plot of the desired function f(t) with the area below the curve made opaque and the upper portion of the mask made transparent. The photocell is placed in the path of the beam and the mask is placed between the tube and the photocell. With the photocell disconnected the bias on the vertical amplifier is adjusted until the beam is deflected to the upper edge of the CRT. The photocell is then connected in the bias circuit of the vertical amplifier in such a way, that its output opposes the bias previously applied, and hence, deflects the beam downwards. As the beam reaches the opaque region on the mask, the photocell is cut off, and ceases to deflect the beam any further. Hence the beam will stay at the boundary between the opaque and transparent regions. Since this boundary is plotted as the function f(t), the voltage across the vertical deflection plates is proportional to the desired function. The photoformer is a very high-speed but low-accuracy device.

In other photoelectric function generators the required function f(t) is represented on photographic film by either variable density or variable area [8]. The film is used to intercept the passage of a beam of light to a photocell. Since the transmitted light is proportional to the function, the output of the photocell represents the desired function f(t), provided the film is moved according to the variable t.

The x-y plotter type of function generator is basically a mixture of the potentiometer generator and the early input

table. Here the plot of the function is traced by a photoelectric pick-up head whose output controls a servomotor which positions the head above the plot. The servomotor also drives a potentiometer wiper which supplies an output voltage proportional to the desired function. In a modified version of the x-y plotter generator the plot is replaced by a current carrying conductor, and the photoelectric curve-follower is replaced by a magnetic pick-up stylus which senses the magnetic field set up by the current in the conductor. The signal from the pick-up stylus controls a servomotor which, in turn, drives a potentiometer as in the photoelectric x-y plotter generator.

The most recently developed function generators incorporate many digital techniques. Most of the devices described in the literature store the desired function f(t) in digital form and use a suitable method to convert the digital information into analog form at the output. In one scheme [5] discrete values of the function f(t) are stored on a rotating magnetic drum. The values are read from the drum in the correct sequence, and are converted to analog form, the intermediate values being produced by linear interpolation. Another method [7] is to store the initial value of the function along with a large number of subsequent increments. The generation, here, is done by adding up the increments, in other words by simple integration. In both methods the argument of the function is represented by the rotation of the drum. The drum is usually driven at a constant rate in which case the operation is limited to the generation of time-dependent functions only.

In the function generator described in this thesis, discrete values of the function are stored in binary code on a punched paper tape, which is read photoelectrically. The digital output of the tape reader is converted to analog form by a resistive decoding network supplied with a constant bias voltage. The analog output is held constant until the next conversion occurs. Hence the output is a step-voltage approximation of the desired function whose degree of accuracy depends on the interval between conversions and the step size. The latter is determined by the number of digits used in the binary code. The device can also be used as a multiplier. If one function, say $f_1(t)$, is generated in the manner described above and the bias voltage on the decoding network is varied according to another function $f_2(t)$, then the output voltage is proportional to $f_1(t)\ f_2(t)$, the product of the two functions. The device consists of two channels. Channel A, which is completely transistorized, is for function generation, and Channel B, containing high-speed magnetic reed switches, serves for multiplication. The possible modes of operation of the device are as follows:

a) both channels generate functions independently according to their tape inputs,

b) channel A generates a function, say $f_A(t)$, channel B generates another function, say $f_B(t)$, and multiplies $f_B(t)$ by $f_A(t)$,

c) channel A generates a function, $f_A(t)$, channel B generates a function, $f_B(t)$, and multiplies $f_B(t)$ by an arbitrary external function.

The ensuing chapters describe the theory, design, construction, and testing of the device.

2. THEORETICAL BACKGROUND

This chapter is intended to form the theoretical groundwork for the design procedure discussed in Chapter 3. Reference will be made to the various sections of this chapter whenever a certain step in the design needs justification. For more details in regard to topics discussed in this chapter the reader is referred to the references[9] listed in the bibliography.

2-1. Digital - Analog Conversion

In today's effort to combine the advantages of analog and digital techniques, an important link between the two domains is the process of digital-to-analog (D/A) and analog-to-digital (A/D) conversion. In analog systems, quantities are represented continuously, while the digital representation involves quantization. Consequently, the converted analog signal can only be an approximation in the digital domain. Consider the analog quantity f(t) in Fig. 1. In the digital representation of this quantity, two kinds of approximation are involved. Instead of continuous observation, the analog quantity is measured at discrete time intervals, a technique which is called sampling. The second kind of approximation occurs when the observed value during each sampling is approximated by the nearest available number. This is called quantization. Analog-to-digital conversion, then, is nothing else than the process of sampling and quantizing of the analog quantity, or, in more familiar terms it is a kind of pulse modulation as shown by the arrows in Fig. 1. Digital-to-analog conversion, as the

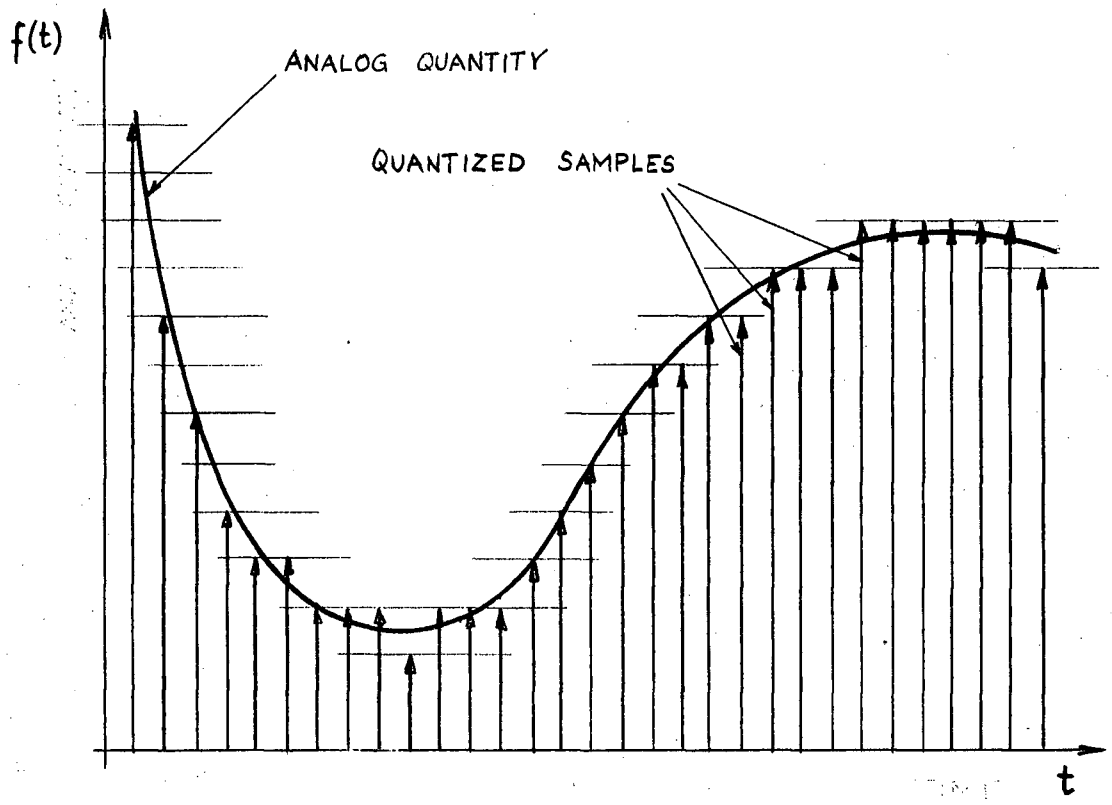

Fig. 1. Digital Representation of an Analog Quantity

name suggests, is the inverse process. Here the digital information is decoded* and the analog output is assumed to have the same value until the next modulated pulse arrives. Hence, holding of some sort is required because the analog world is continuous, and the value of a sample must be maintained until the next sample arrives. Fig. 2 shows the analog signal obtained from a pulse modulated signal.

The question arises: How well can an analog signal be recovered after a complete cycle of digital-analog conversion? The answer to this question is given in the Sampling and

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* Digital-to-analog conversion is often called decoding, while coding refers to analog-to-digital conversion.

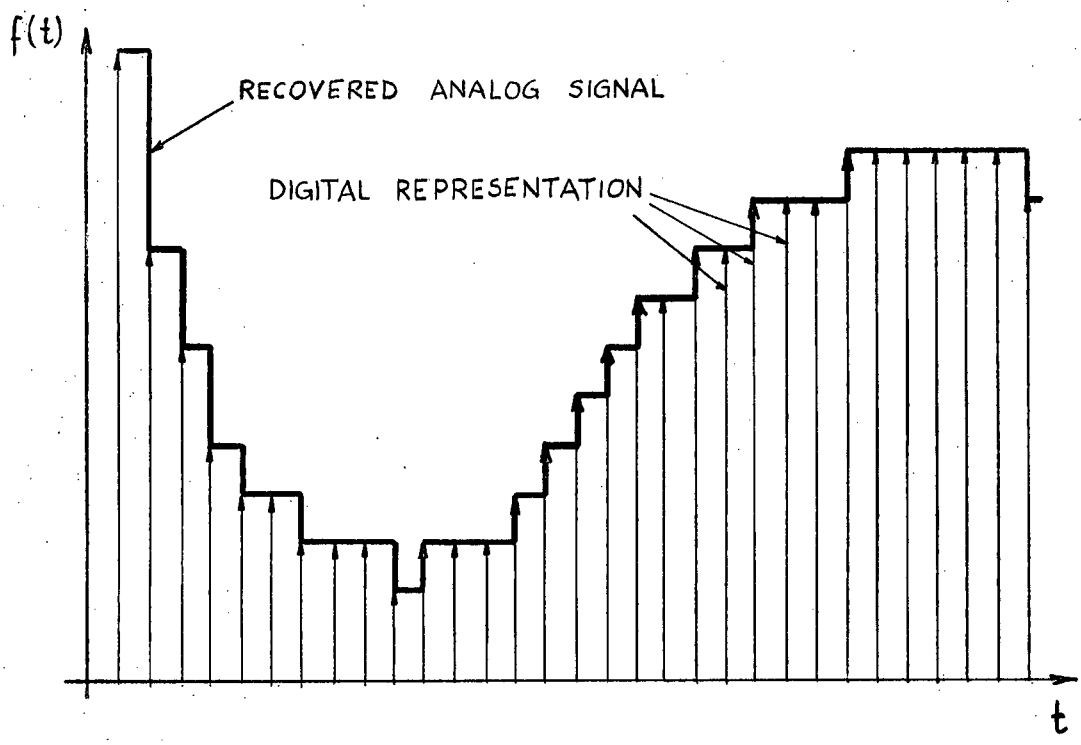


Fig. 2. Analog Signal Recovered from Digital Information

Quantizing Theorems [9] which set out the conditions of complete recovery in terms of the frequency spectrum of the signal, the sampling rate, and the quantization error.

2-2. Decoding Networks

The basic function of a decoder is to produce a voltage proportional to a number. If this number is binary then we talk about a binary decoder. There are two main groups of decoders. The first group consists of decoders in which conversion involves an intermediate step, usually the generation of a pulse of some kind whose duration is proportional to the number being decoded. These devices are relatively slow and complex, but if a number of conversions have to be done simultaneously, most of the equipment can be time shared by the various channels. Storage for holding information between

conversions is usually not needed. The second group, formed by decoders which carry out conversion in a single step, is characterized by short conversion time and extreme simplicity, but time sharing is difficult and storage for holding is in all cases required. Two decoders of the second group will be illustrated in the following sections. For details on the other types of decoders the reader is referred to reference (9).

2-3. Network of Weighted Resistors

Perhaps the simplest method of decoding consists of the switching of current or voltage sources into a resistive network in accordance with the number to be decoded. This method is illustrated in both examples given here. The network of Fig. 3. is a binary decoder. Suppose the numbers to be decoded are (n+1)-digit binary numbers of the form

$$p = b_n\, b_{n-1} \cdots b_1 b_0.$$

Conversion is performed by switching the voltage sources E_k (k=0, 1...n) in such a way that

$$E_k = +E \quad \text{if} \quad b_k = 1, \text{ and}$$

$$E_k = -E \quad \text{if} \quad b_k = 0.$$

To show that by choosing the resistors r_k according to the formula

$$r_k = \frac{R_0}{2^k} \tag{1}$$

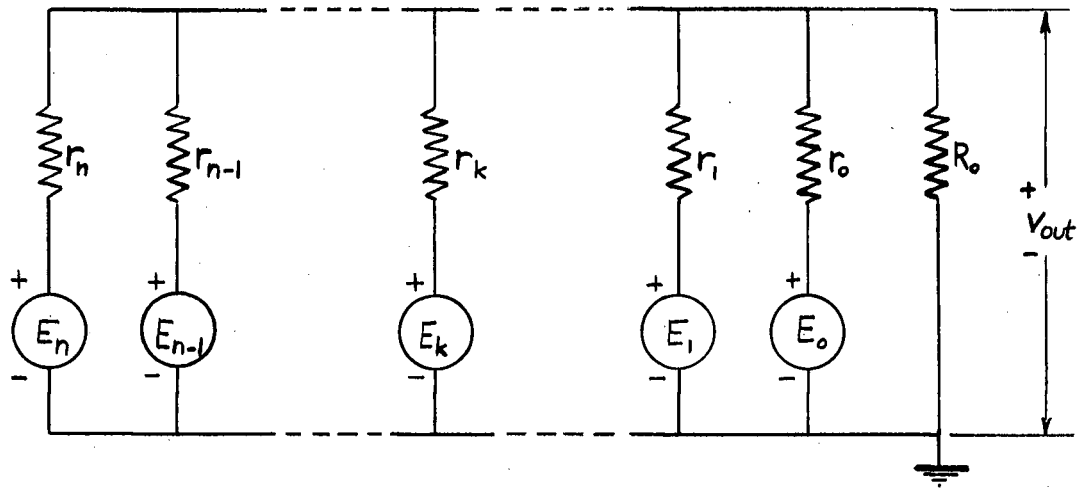


Fig. 3. Network of Weighted Resistors

the network is capable of binary decoding, consider the equivalent circuit shown in Fig. 4, where the voltage sources are assumed ideal. Grounding the -E and +E terminals in turn and applying the superposition theorem we can write:

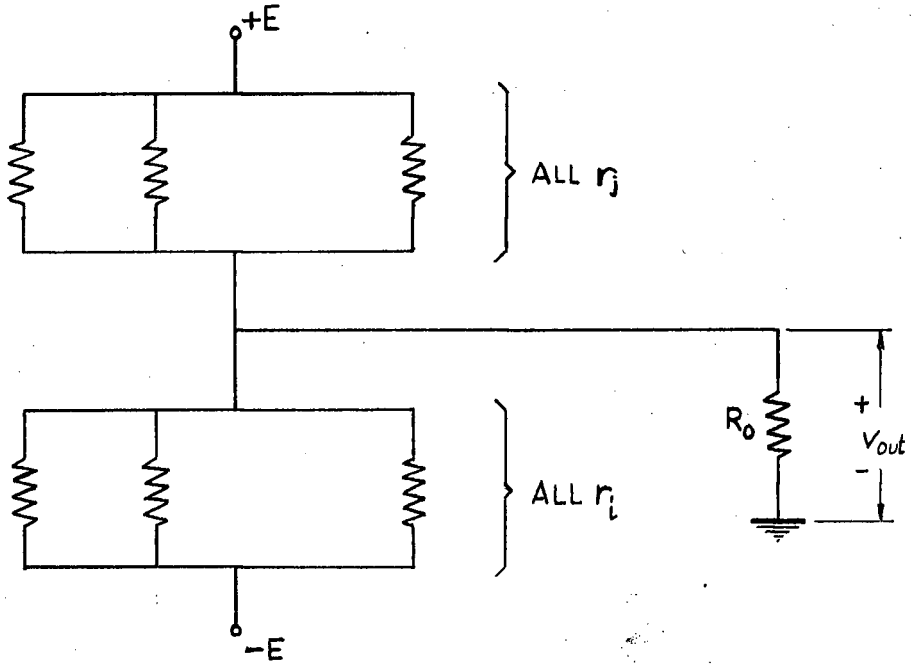


Fig. 4. Equivalent Circuit of the Network of Weighted Resistors

$$v_{out} = \frac{\left(\frac{1}{R_0} + \sum_i \frac{1}{r_i}\right)^{-1} E}{\left(\frac{1}{R_0} + \sum_i \frac{1}{r_i}\right)^{-1} + \left(\sum_j \frac{1}{r_j}\right)^{-1}} + \frac{\left(\frac{1}{R_0} + \sum_j \frac{1}{r_j}\right)^{-1} (-E)}{\left(\frac{1}{R_0} + \sum_j \frac{1}{r_j}\right)^{-1} + \left(\sum_i \frac{1}{r_i}\right)^{-1}} \tag{2}$$

where summations are carried out over all i and j such that $b_i = 0$ and $b_j = 1$. Equation (2) can be simplified to give

$$v_{out} = \frac{E\left(\sum_j \frac{1}{r_j} - \sum_i \frac{1}{r_i}\right)}{\frac{1}{R_0} + \sum_0^n \frac{1}{r_k}}. \tag{3}$$

Combining (1) and (3) we obtain

$$v_{out} = \frac{E\left(\sum_j \frac{1}{r_j} - \sum_i \frac{1}{r_i}\right)}{\frac{1}{R_0}\, 2^{n+1}}. \tag{4}$$

Observe that if p is the binary number corresponding to the state of the voltage sources, then

$$\sum_j \frac{1}{r_j} = \frac{1}{R_0} \sum_j 2^j = \frac{1}{R_0}\, p \tag{5}$$

since r_j stands for each of those resistors whose corresponding

binary digit is 1. Consequently,

$$\sum_i \frac{1}{r_i} = \sum_0^n \frac{1}{r_k} - \sum_j \frac{1}{r_j} = \frac{1}{R_0}\left(2^{n+1} - 1\right) - \frac{1}{R_0} p$$

or

$$\sum_i \frac{1}{r_i} = \frac{1}{R_0}\left(2^{n+1} - p - 1\right). \qquad (6)$$

Using (4), (5) and (6) we obtain

$$v_{out} = E\left(\frac{2p + 1}{2^{n+1}} - 1\right). \qquad (7)$$

Equation (7) which was derived by Susskind[9], is a linear relation between v_{out}, the analog output voltage, and p, the binary number to be decoded. Note that if p is changed by 1, the output voltage v_{out} changes by $\frac{E}{2^n}$, hence the quantization error is given by

$$\Delta v_{out} = \frac{E}{2^n}. \qquad (8)$$

Equation (8) also follows from the fact, that with n + 1 binary digits, a total of 2^{n+1} different binary numbers can be formed. A simple examination of equation (7) will show that no binary integer exists for which $v_{out} = 0$. If $E \neq 0$, for v_{out} to be zero $2p+1 = 2^{n+1}$, i.e. $p = 2^n \div \frac{1}{2}$ must hold. However, since p is an integer the last relation cannot hold, and hence v_{out} cannot be zero. Hence, a special provision must be made for $v_{out} = 0$.

Since the relationship between component tolerances and conversion accuracy for decoders is of considerable interest, we will consider the following error analysis.

2-4. Error Analysis of the Weighted Network

For the network of weighted resistors, the output voltage v_{out} in terms of component values was given by equation (3) which is repeated here for convenience:

$$v_{out} = \frac{E\left(\sum_j \frac{1}{r_j} - \sum_i \frac{1}{r_i}\right)}{\frac{1}{R_0} + \sum_0^n \frac{1}{r_k}} \quad . \tag{9}$$

Differentiation of (9) with respect to r_i, r_j and R_0 in turn will indicate the relation between small changes in resistor values and the resulting changes in the output voltage. Thus,

$$\frac{1}{E}\ \frac{d}{dr_i}\ v_{out} = \frac{\left(\frac{1}{R_0} + \sum_0^n \frac{1}{r_k}\right)\frac{1}{r_i^2} - \left(\sum_j \frac{1}{r_j} - \sum \frac{1}{r_i}\right)\left(-\frac{1}{r_i^2}\right)}{\left(\frac{1}{R_0} + \sum_0^n \frac{1}{r_k}\right)^2}$$

which combined with (1), (5) and (6) reduces to

$$\frac{d\ v_{out}}{E} = K_i(p)\ \ \frac{dr_i}{r_i} \tag{10}$$

where the factor of proportionality $K_i(p)$ is a function of p

and is given by

$$K_i(p) = \frac{2p + 1}{2^{2(n+1)-i}} \cdot \tag{11}$$

Equation (10) relates the percent error in resistor r_i to the corresponding full scale error in the output voltage in terms of the binary number p for the cases when $b_i = 0$.

Differentiation of (9) with respect to r_j yields a similar relation for the cases when $b_j = 1$:

$$\frac{d\, v_{out}}{E} = K_j(p)\, \frac{dr_j}{r_j} \tag{12}$$

where $K_j(p)$ is given by

$$K_j(p) = \frac{2p-2^{n+2} + 1}{2^{2(n+1)-j}} \cdot \tag{13}$$

Finally if (9) is differentiated with respect to R_0 the following result is obtained

$$\frac{d\, v_{out}}{E} = K(p)\, \frac{dR_0}{R_0} \tag{14}$$

where

$$K(p) = \frac{2p - 2^{n+1} + 1}{2^{2(n+1)}} \cdot \tag{15}$$

Equations (10), (12) and (14) can be simplified if the coefficients $K_i(p)$, $K_j(p)$ and $K(p)$ are replaced by their maximum values over

the range defined by $0 \leq p \leq 2^{n+1} - 1$. With the assumption that $2^{n+1} \gg 1$ we may simplify and combine (10) and (12) to obtain

$$\frac{d\, v_{out}}{E} \leq \frac{1}{2^{n-k}} \quad \frac{dr_k}{r_k} \tag{16a}$$

and rewrite (14) as

$$\frac{d\, v_{out}}{E} \leq \frac{1}{2^{n+1}} \quad \frac{dR_0}{R_0} . \tag{16b}$$

The inequalities given by (16) define an upper bound for the full scale relative conversion accuracy in terms of component tolerances.

If equations (10), (12) and (14) are multiplied by E/v_{out}, the following relations are obtained:

$$\frac{d\, v_{out}}{v_{out}} \leq 2^k \quad \frac{dr_k}{r_k} , \tag{17a}$$

$$\frac{d\, v_{out}}{v_{out}} \leq \frac{1}{2^{n+1}} \quad \frac{dR_0}{R_0} . \tag{17b}$$

The inequalities given by (17) indicate an upper bound for the relative conversion accuracy in terms of component tolerances. The weighting factors (powers of two) appearing in (17) are closely related to the place values of the binary digits, and therefore indicate that the resistor associated with the most significant binary digit must be the most accurate.

2-5. Ladder Network

Our second example of binary decoders is shown in Fig. 5. The process of decoding is exactly the same as in the first example, i.e. the voltage sources are switched according to

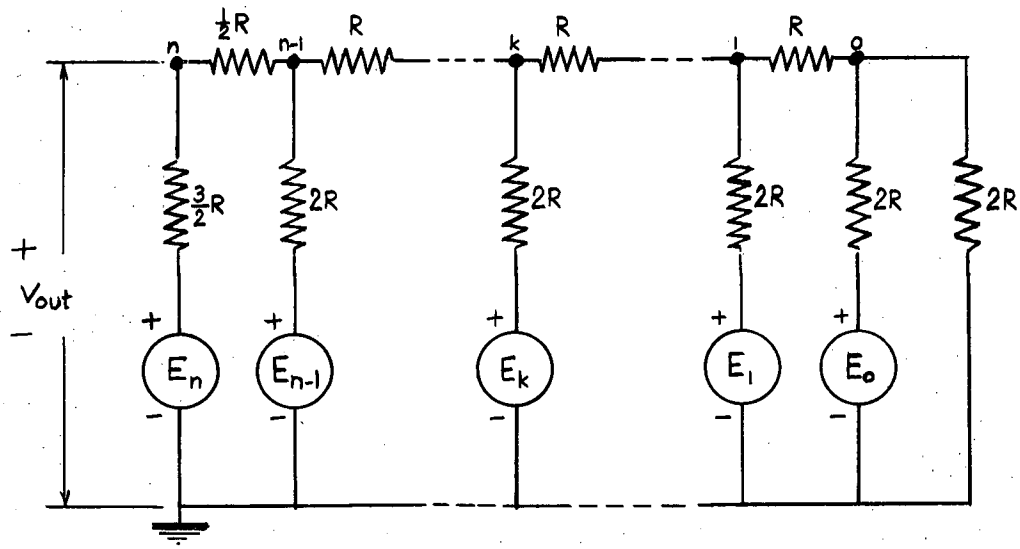


Fig. 5. Ladder Network for Binary Decoding

the binary number to be decoded. To derive the binary conversion formula, use will be made of the equivalent circuits in Fig. 6, and the voltage sources will be assumed ideal. From Fig. 6, the voltage at the k^{th} node due to the k^{th} source is given by

$$v_{k,k} = \frac{E_k}{3} \qquad \text{for } k = 0, 1, 2 \ldots n-1 \qquad (18a)$$

and

$$v_{n,n} = \frac{E_n}{2} \qquad \text{for } k = n. \qquad (18b)$$

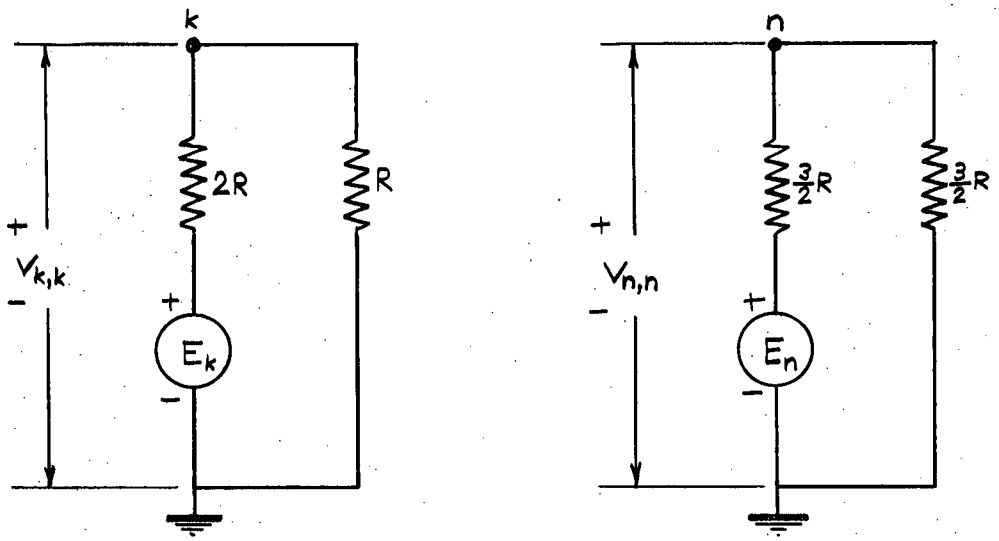
It follows from equation (18a) that

$$v_{k+1,k} = \frac{1}{2} \frac{E_k}{3}$$

$$v_{k+2,k} = \frac{1}{4} \frac{E_k}{3}$$

$$\vdots$$

$$v_{n-1,k} = \frac{1}{2^{n-1-k}} \frac{E_k}{3} .$$



a) k = 0,1....n-1 b) k = n

Fig. 6. Equivalent Circuits of the Ladder Network

Referring to Fig. 6b we may write the output voltage due to the k^{th} source alone as

$$v_{n,k} = \frac{\frac{3}{2} R}{2R} v_{n-1,k} = \frac{3}{4} \frac{1}{2^{n-1-k}} \frac{E_k}{3}$$

or

$$v_{n,k} = \frac{E_k}{2^{n-k+1}} \cdot \qquad (19)$$

Comparing (19) with (18b) we find that (19) holds for all values of k = 0, 1.....n. It remains, then, to find the output voltage due to all sources. This can be found by superimposing the output voltages due to the individual sources, thus

$$v_{out} = \sum_{k=0}^{n} v_{n,k} = \sum_{k=0}^{n} \frac{E_k}{2^{n-k+1}}$$

or

$$v_{out} = \frac{E}{2^{n+1}} \left(\sum_{j} 2^j - \sum_{i} 2^i \right) \qquad (20)$$

where i and j are such that $b_i = 0$ and $b_j = 1$. Since

$$\sum_{j} 2^j = p$$

and

$$\sum_{i} 2^i = \sum_{k=0}^{n} 2^k - \sum_{j} 2^j = 2^{n+1} - 1 - p$$

where p is the binary number to be decoded, we have

$$v_{out} = \frac{E}{2^{n+1}} \left[p - (2^{n+1} - 1 - p) \right]$$

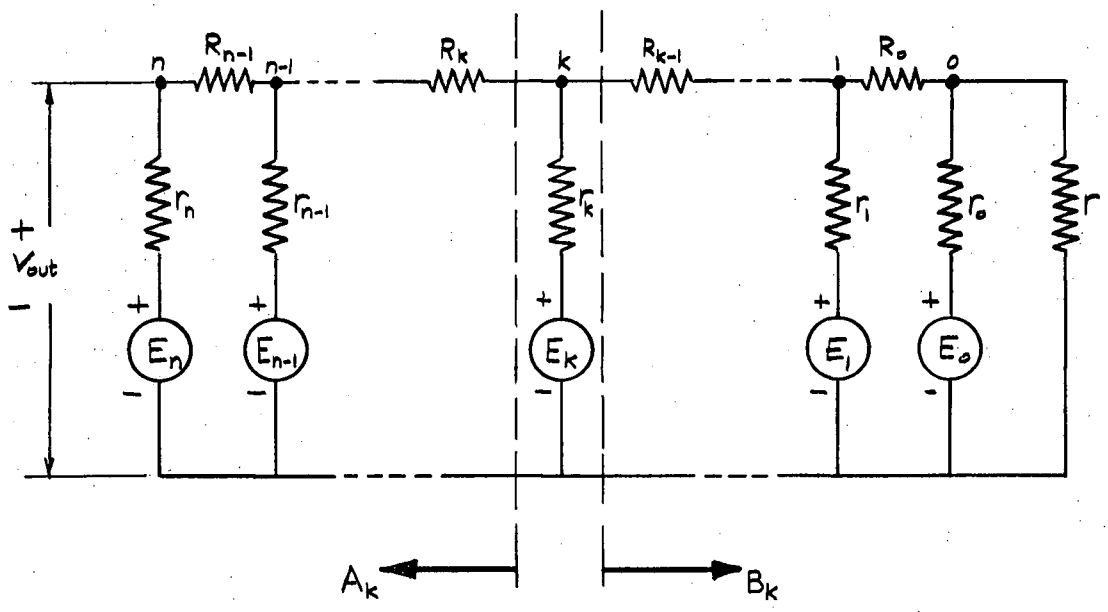
or

$$v_{out} = E\left(\frac{2p+1}{2^{n+1}} - 1\right) \qquad (21)$$

which is the desired relation. Equations (21) and (7) are identical, and hence, the ladder network, too, is capable of binary conversion.

2-6. Error Analysis of the Ladder Network

In order to carry out the error analysis for the ladder network it is again necessary to express the output voltage in terms of the decoding resistors. The network is redrawn in



$$r = r_0 = r_1 = \cdots\cdots = r_{n-1} = 2R, \quad r_n = \frac{3}{2}R$$

$$R_0 = R_1 = \cdots\cdots\cdots = R_{n-2} = R, \quad R_{n-1} = \frac{1}{2}R$$

Fig. 7. Ladder Network for Binary Decoding

Fig. 7 with the resistors identified in a more convenient way for the analysis. A_k and B_k are the equivalent resistances of the two sections of the ladder as indicated, where their values are given by the continued-fraction expansions

$$A_k = R_k + \cfrac{1}{\cfrac{1}{r_{k+1}} + \cfrac{1}{R_{k+1} + \cfrac{1}{\cfrac{1}{r_{k+2}} + \cfrac{1}{R_{k+2} + \cdots + \cfrac{1}{\cfrac{1}{r_{n-1}} + \cfrac{1}{R_{n-1} + r_n}}}}}}} \tag{22}$$

and

$$B_k = R_{k-1} + \cfrac{1}{\cfrac{1}{r_{k-1}} + \cfrac{1}{R_{k-2} + \cfrac{1}{\cfrac{1}{r_{k-2}} + \cfrac{1}{R_{k-3} + \cdots + \cfrac{1}{\cfrac{1}{r_1} + \cfrac{1}{R_0 + \cfrac{1}{\cfrac{1}{r_0} + \cfrac{1}{r}}}}}}}}.$$

The voltage at the k^{th} node due to the k^{th} source, E_k, is given by

$$v_{k,k} = \frac{E_k \left(\frac{1}{B_k} + \frac{1}{A_k} \right)^{-1}}{r_k + \left(\frac{1}{B_k} + \frac{1}{A_k} \right)^{-1}} = \frac{E_k}{1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}},$$

and

$$v_{k+1,k} = v_{k,k} \frac{\left(\frac{1}{r_{k+1}} + \frac{1}{A_{k+1}} \right)^{-1}}{\left(R_k + \frac{1}{r_{k+1}} + \frac{1}{A_{k+1}} \right)^{-1}} = \frac{E_k}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k} \right)\left(1 + \frac{R_k}{r_{k+1}} + \frac{R_k}{A_{k+1}} \right)}$$

$$\vdots$$

$$v_{n,k} = \frac{E_k}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k} \right)\left(1 + \frac{R_k}{r_{k+1}} + \frac{R_k}{A_{k+1}} \right) \cdots \left(1 + \frac{R_{n-1}}{r_n} + \frac{R_{n-1}}{A_n} \right)} . \tag{24}$$

The total output voltage is the sum of the contributions of the individual sources. Hence,

$$v_{out} = \sum_{k=0}^{n} v_{n,k} \tag{25}$$

where the $v_{n,k}$ are given by (24). The error analysis can now be carried out by differentiating equation (25) with respect to r_s, R_s and r in turn. Consider the differentiation of (25) with respect to r_s first. We can write

$$\frac{d}{dr_s} v_{out} = \sum_{k=0}^{n} \frac{d}{dr_s} v_{n,k} . \tag{26}$$

The derivatives on the right hand side of equation (26) are obtained from relation (24). It is convenient to consider the

following three cases:

case a) $s < k$, where $\frac{d}{dr_s} A_k = 0$, (27a)

case b) $s = k$, where $\frac{d}{dr_s} A_k = \frac{d}{dr_s} B_k = 0$, and (27b)

case c) $s > k$, where $\frac{d}{dr_s} B_k = 0$. (27c)

The differentiation of equation (24) is carried out using the general formula

$$\frac{d}{dx} \frac{1}{abc \ldots\ldots\ldots} = \frac{-1}{abc \ldots\ldots\ldots} \left(\frac{1}{a}\frac{da}{dx} + \frac{1}{b}\frac{db}{dx} + \ldots\ldots\right). \tag{28}$$

Case a)

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s<k} = \frac{E_k}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}\right) \prod_{t=k}^{n-1} \left(1 + \frac{R_t}{r_{t+1}} + \frac{R_t}{A_{t+1}}\right)} \frac{\frac{r_k}{B_k^2} \frac{d}{dr_s} B_k}{1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}} \tag{29}$$

where

$$\frac{d}{dr_s} B_k = \frac{\frac{1}{B_{k-1}^2} \frac{d}{dr_s} B_{k-1}}{\left(\frac{1}{r_{k-1}} + \frac{1}{B_{k-1}}\right)^2} = \frac{1}{\left(1 + \frac{B_{k-1}}{r_{k-1}}\right)^2} \frac{d}{dr_s} B_{k-1}$$

$$= \frac{1}{\left(1 + \frac{B_{k-1}}{r_{k-1}}\right)^2 \left(1 + \frac{B_{k-2}}{r_{k-2}}\right)^2} \frac{d}{dr_s} B_{k-2}$$

$$\vdots$$

$$= \frac{1}{\left(1 + \frac{B_{k-1}}{r_{k-1}}\right)^2 \left(1 + \frac{B_{k-2}}{r_{k-2}}\right)^2 \cdots \left(1 + \frac{B_{s+1}}{r_{s+1}}\right)^2 \left(1 + \frac{r_s}{B_s}\right)^2}$$

or

$$\frac{d}{dr_s} B_k = \frac{1}{\left(1 + \frac{r_s}{B_s}\right)^2 \prod_{t=s+1}^{k-1} \left(1 + \frac{B_t}{r_t}\right)^2} . \qquad (30)$$

Equations (30) and (29) can now be combined and simplified to

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s<k=n} = \frac{E_n}{3r_s} \frac{1}{2^{2(n-s)}} \qquad (31a)$$

and

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s<k<n} = \frac{E_k}{3r_s} \frac{1}{2^{n+k} - 2s+1} . \qquad (31b)$$

Case b)

Differentiation of (24) with respect to r_s for the case $s = k$ gives

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s=k} = \frac{\frac{E_k}{r_k}}{\prod_{t=k}^{n-1} \left(1 + \frac{R_t}{r_{t+1}} + \frac{R_t}{A_{t+1}}\right)} \frac{-\left(\frac{r_k}{A_k} + \frac{r_k}{B_k}\right)}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}\right)^2}$$

which after much simplification reduces to

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s=k=n} = -\frac{E_n}{4r_s} \qquad (32a)$$

and

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{s=k<n} = -\frac{E_k}{3r_s} \frac{1}{2^{n-k}} . \qquad (32b)$$

Case c)

For the third case with $s > k$ the differentiation of

equation (24) results in the following:

$$\left.\frac{d}{dr} v_{n,k}\right]_{s \to k} = \frac{E_k}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}\right) \prod_{t=k}^{n-1} \left(1 + \frac{R_t}{r_{t+1}} + \frac{R_t}{A_{t+1}}\right)} \left\{ \frac{\frac{r_k}{A_k^2} \frac{d}{dr_s} A_k}{\left(1 + \frac{r_k}{A_k} + \frac{r_k}{B_k}\right)} + \right.$$

$$\left. + \frac{\frac{R_k}{A_{k+1}^2} \frac{d}{dr_s} A_{k+1}}{\left(1 + \frac{R_k}{r_{k+1}} + \frac{R_k}{A_{k+1}}\right)^2} + \cdots + \frac{\frac{R_{s-2}}{A_{s-1}^2} \frac{d}{dr_s} A_{s-1}}{\left(1 + \frac{R_{s-2}}{r_{s-1}} + \frac{R_{s-2}}{A_{s-1}}\right)^2} + \frac{\frac{R_{s-1}}{r_s^2}}{\left(1 + \frac{R_{s-1}}{r_s} + \frac{R_{s-1}}{A_s}\right)} \right\}$$

(33)

where

$$\frac{d}{dr_s} A_k = \frac{\frac{1}{A_{k+1}^2} \frac{d}{dr_s} A_{k+1}}{\left(\frac{1}{r_{k+1}} + \frac{1}{A_{k+1}}\right)^2} = \frac{1}{\left(1 + \frac{A_{k+1}}{r_{k+1}}\right)^2} \frac{d}{dr_s} A_{k+1}$$

$$= \frac{1}{\left(1 + \frac{A_{k+1}}{r_{k+1}}\right)^2 \left(1 + \frac{A_{k+2}}{r_{k+2}}\right)^2} \frac{d}{dr_s} A_{k+2}$$

$$\vdots$$

$$= \frac{1}{\left(1 + \frac{A_{k+1}}{r_{k+1}}\right)^2 \left(1 + \frac{A_{k+2}}{r_{k+2}}\right)^2 \cdots \left(1 + \frac{A_{s-1}}{r_{s-1}}\right)^2 \left(1 + \frac{r_s}{A_s}\right)^2}$$

or

$$\frac{d}{dr_s} A_k = \frac{1}{\left(1 + \frac{r_s}{A_s}\right)^2 \prod_{t=k+1}^{s-1} \left(1 + \frac{A_t}{r_t}\right)^2} . \qquad (34)$$

After combining and simplifying equations (33) and (34) we obtain

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{\substack{s<k \\ s=n}} = \frac{E_k}{r_s} \frac{1}{2^{n-k+1}} \left\{ \frac{1}{4^{s-k}} + \frac{3}{4} \sum_{\ell=1}^{s-k-1} \left(\frac{1}{4}\right)^{\ell} + \frac{1}{4} \right\} \qquad (35a)$$

and

$$\left.\frac{d}{dr_s} v_{n,k}\right]_{\substack{s>k \\ s<n}} = \frac{E_k}{r_s} \frac{1}{2^{n-k+1}} \left\{ \frac{1}{3} \frac{1}{4^{s-k}} + \sum_{\ell=1}^{s-k} \left(\frac{1}{4}\right)^{\ell} \right\} . \qquad (35b)$$

If substitution of equations (31), (32) and (35) into relation (26) is carried out, after simplification the result is

$$\frac{d\, v_{out}}{E} \leq \frac{1}{2^{n-k+1}} \frac{dr_k}{r_k} . \qquad (36a)$$

Differentiation of equation (26) with respect to R_k and r produces the following results:

$$\frac{d\, v_{out}}{E} \leq \frac{1}{2^{n-k+1}} \frac{dR_k}{r_k} , \qquad (36b)$$

and

$$\frac{d\, v_{out}}{E} \leq \frac{1}{2^{n+2}} \frac{dr}{r} . \tag{36c}$$

The relations given by (36) indicate the dependence of the full scale conversion accuracy on component tolerances for the ladder network. Comparison of relations (36) with relations (16) reveals that the output voltage of the ladder network is less sensitive to changes in component values than that of the network of weighted resistors, and therefore, for the same degree of conversion accuracy the ladder network requires resistors half as accurate as those in the weighted network. Consequently the conversion accuracy for the ladder network can be derived from the relations in (17) by making the appropriate adjustment by a factor of two. Thus,

$$\frac{d\, v_{out}}{v_{out}} \leq 2^{k-1} \frac{dr_k}{r_k} \tag{37a}$$

and then, comparing (36a) with (36b) and (36c) one obtains

$$\frac{d\, v_{out}}{v_{out}} \leq 2^{k-1} \frac{dR_k}{R_k} \tag{37b}$$

and

$$\frac{d\, v_{out}}{v_{out}} \leq \frac{1}{4} \frac{dr}{r} . \tag{37c}$$

2-7. Summary

In summary, then, both networks are capable of binary decoding, the accuracy of which depends on the number of decoding resistors and on the tolerances of their values. Furthermore, these tolerances should be weighted by fractions of two as indicated in (16) and (18) for the weighted network and in (36) and (37) for the ladder network. It was also shown that for the same tolerances the ladder network is twice as accurate as the network of weighted resistors.

3. CIRCUIT DESIGN

3-1. Design Philosophy

The object of this work was

1) to investigate the use of a digital-to-analog conversion device as a combination function generator and multiplier, and
2) to build and test such a device if feasible.

The double-input function generator was to provide arbitrary driving functions for purposes of analog real-time computation and simulation. One of the two channels (one corresponding to each input) was to be capable of multiplication as well as function generation. In order for the device to be compatible with analog computer facilities the standard output range of $\pm$ 100 volts, with overall accuracy of 1% or better, was sought.

The first attempt resulted in the block diagram of the device as shown in Fig. 8. Channels A and B form the generating channel and multiplying channel, respectively. Two twelve-level punched paper tapes provide the digital input for the two channels. The trigger circuits driven by the incoming digital information activate the switching and decoding networks which in turn produce analog voltages corresponding to the hole and no-hole combinations read by the photoelectric readers. The two channels differ from each other in the method of switching and the bias voltage across the decoding network. In Channel A transistor switches are used to connect the proper bias voltages to the decoding network. For

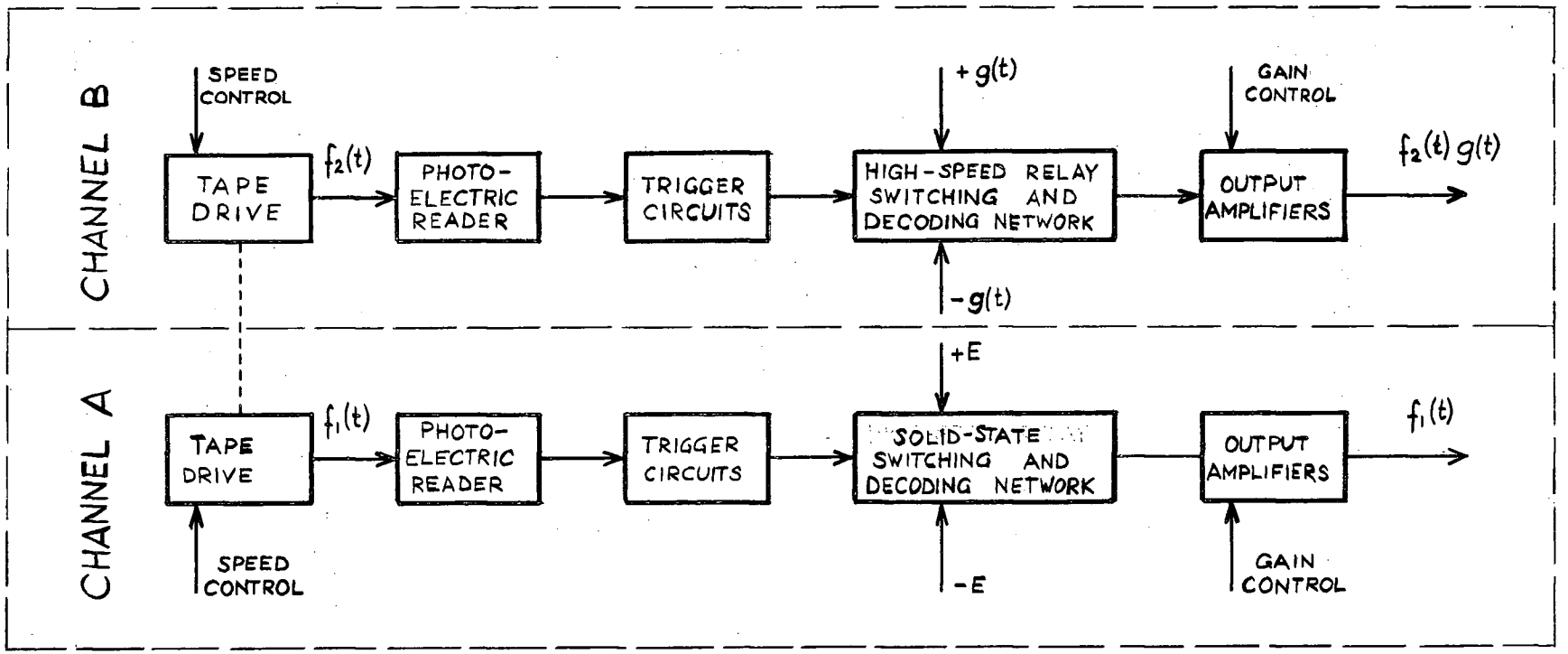


Fig. 8. Block Diagram of the Combination Function Generator and Multiplier

function generation the bias is $\pm$ E volts, where E is a constant. In the case of multiplication the bias across the decoding network has to vary according to the multiplicand which in turn may change sign. In this case high-speed relays, which are insensitive to changes in polarity, have to be used instead of transistor switches. Channel B can also be used to generate functions provided the bias across the decoding network is held constant (i.e. g(t) = constant). The speed and gain controls add a great deal of versatility to the device because they provide means of varying the time scale and magnitude of the generated function. The dotted line connecting the two blocks labelled TAPE DRIVE in Fig. 8 indicates provision for synchronization between the two independent channels.

At this point, with the general outline of the function generator and multiplier in the background, we are ready for the first step towards the realization of our block diagram. Fig. 9 shows the middle block of the channels in Fig. 8 in somewhat more detail. The diagram shows how the twelve available levels of the tape are assigned. One level (No. 12) is used to generate clock pulses for the purpose of synchronization between the various levels. Nine levels (Nos. 1 to 9), each corresponding to a binary digit, are reserved for the point value representation of the desired function. One of the remaining two levels (No. 10) provides zero output, since, as it was shown in Chapter 2, no quantization level coincides with zero, and hence, an extra level is required to ground the output directly whenever zero output is called for. Finally the last level (No. 11) generates control pulses which provide communication between the generator and the

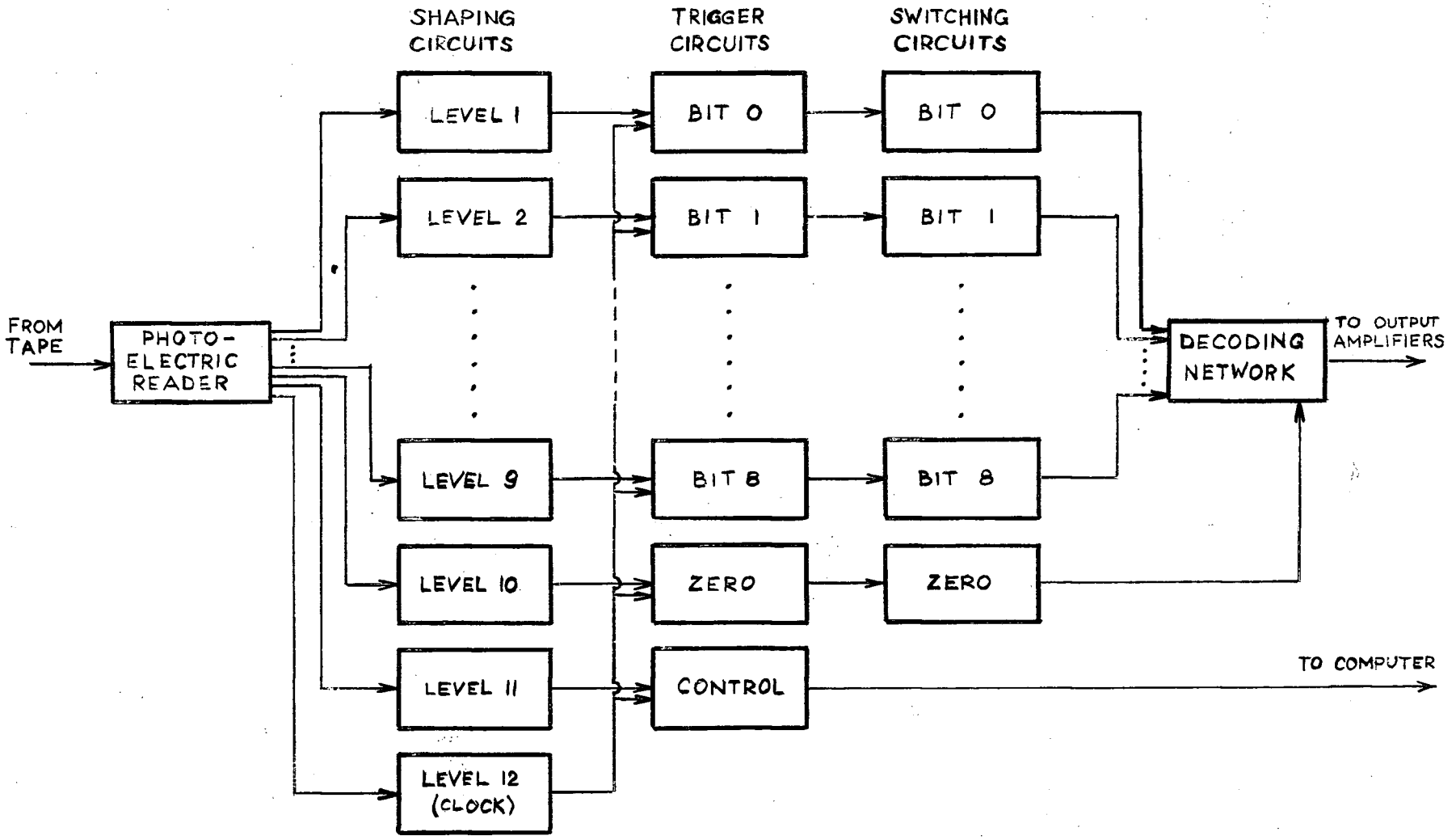


Fig. 9. Details of Tape Level Allocation

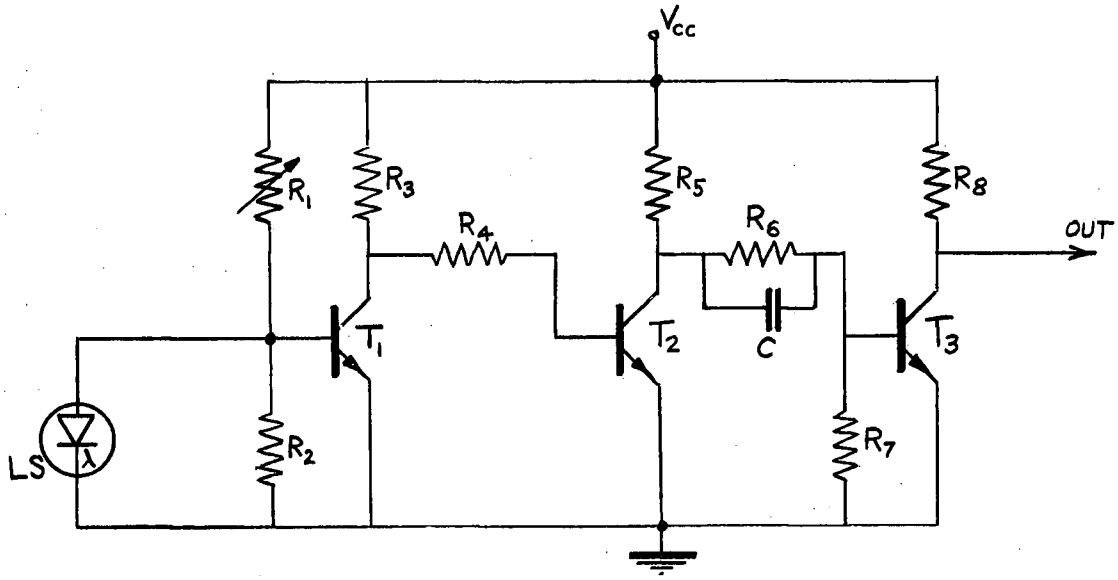
computer. The binary code for representing functions is given in Table 1 in Appendix I where the use of the table is illustrated by an example. The functions of the various blocks in Fig. 9 are as follows. When the reader senses a hole in a particular level on the tape it sends a pulse to the corresponding shaping circuit which produces a square pulse with short rise and fall times. The control pulse de-energizes the hold and reset relays in the computer, and hence initiates the compute mode. The nine bit pulses and the zero-level pulse are combined with the clock pulses in the trigger circuits which produce nine trigger pulse trains of evenly spaced sharp pulses synchronous with the leading edges of the square clock pulses. The polarity of the pulses changes according to the information received from the tape. If a hole is observed in a level the corresponding trigger circuit sends a positive pulse, and in the absence of a hole it generates a negative pulse. Single-sided triggering of the flip-flops in the switching circuits then results in a one-to-one correspondence between the presence or absence of holes and the state of the flip-flops. The final step in obtaining the analog output is to switch the voltage sources in accordance with the state of the flip-flops.

The following sections deal with circuits designed to perform functions called for in the block diagram representation.

3-2. Shaping Circuits

The shape of the pulses generated by the light sensors depends a great deal on the speed of the paper tape. As the hole approaches the light sensor the amount of transmitted light

increases gradually, attains a maximum, and then again falls down to a minimum. Consequently, the photoelectric response has similar rather poor rise and fall time characteristics which have to be improved by pulse shaping. The shaping circuit (see Fig. 10) consists of a Schmidt trigger (formed by T_2 and T_3) and an input transistor (T_1) which is turned on when only the dark current is flowing, and is turned off by the light current due to a hole. The decision level of the Schmidt trigger is set



LS = Type LS222 Light Sensor	R_2 = 4.7K	R_6 = 47K
T_1, T_2, T_3 = Type 2N1304	R_3 = 10K	R_7 = 100K
C = 0.01 μf	R_4 = 47K	R_8 = 4.7K
R_1 = 50K	R_5 = 4.7K	V_{cc} = +6 volts

Fig. 10. Pulse Shaping Circuit

between the two extreme values of the collector voltage of T_1, and hence, the output of the shaping circuit is a fast rising and falling square pulse coincident with, but somewhat narrower than, the input pulse. The pulse width at the output can be adjusted by R_1, since the degree of saturation of T_1, depends on the bias set by R_1 and R_2, which also determines the amount of light required to bring T_1, out of saturation.

3-3. Trigger Circuits

The generation of trigger pulse trains can best be understood from the block diagram in Fig. 11 where the method of combining the clock pulses with the bit pulses from a particular level is shown. By means of the pulse width adjustment described in the previous section the bit pulses are made to overlap the

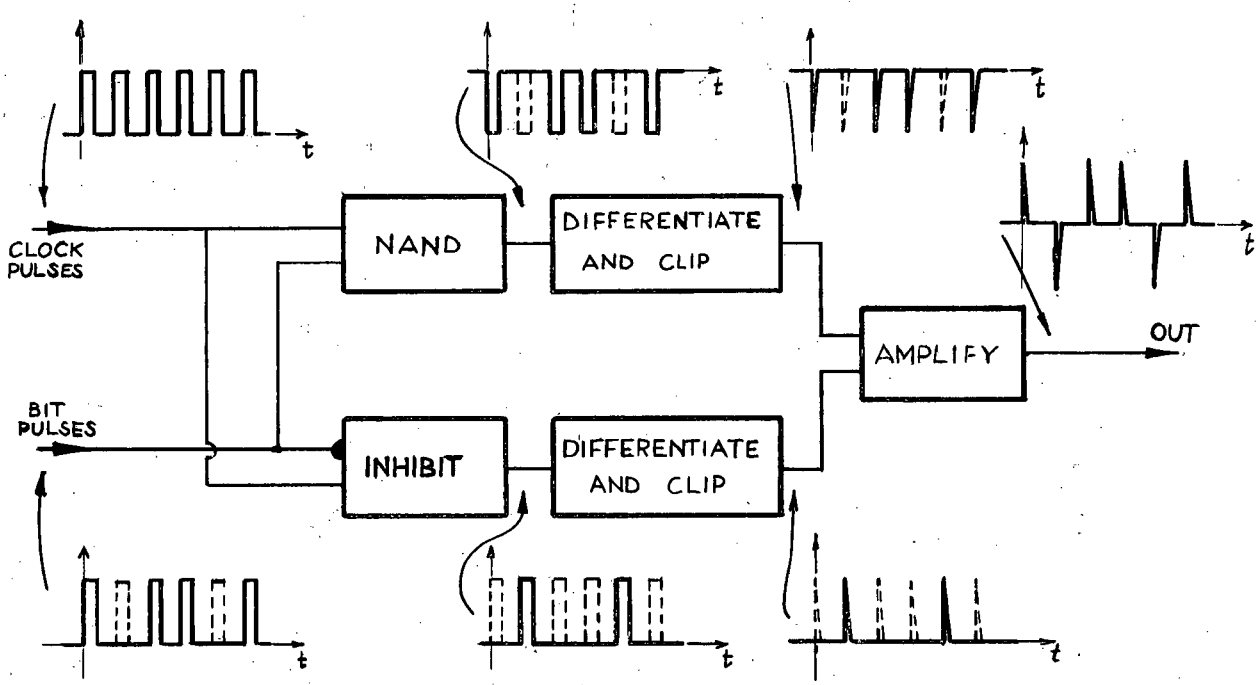


Fig. 11. Generation of Trigger Pulses

clock pulses in duration so that the output pulses of all the NAND and INHIBIT circuits are synchronized to the leading edges of the clock pulses. The waveforms shown at key-points in Fig. 11 make any further explanation unnecessary. In the circuit diagram of the trigger pulse generator (Fig. 12) the diodes D_1 and D_2 along with transistor T_1 perform the NAND function, while T_2, D_5, and D_6 make up the INHIBIT circuit. The pulses are differentiated by C_1R_5 and C_2R_{11}, clipped by D_3D_4 and D_7D_8, then added by R_6 and R_{12}, and finally amplified by T_3.

3-4. Decoding Network

Although the part immediately following the trigger circuit is the switching circuit, it is more convenient to discuss the decoding network first and then fill in the gap between the trigger circuit and the decoding network.

We have already started comparing the two binary decoders introduced in the previous chapter, where it was found that the ladder network was more accurate than the network of weighted resistors. From the circuit designer's point of view the ladder network has additional desirable properties for which it was chosen over the other network. One such advantage is that each of the sources, E_k, sees the same equivalent resistance, which is not true for the weighted network. Another useful property of the ladder network is that its component values are of the same order of magnitude. Precision resistors with a wide range of values as required for the weighted network would be very expensive and troublesome to obtain. The network is redrawn in Fig. 13 with all component and tolerance values shown. The

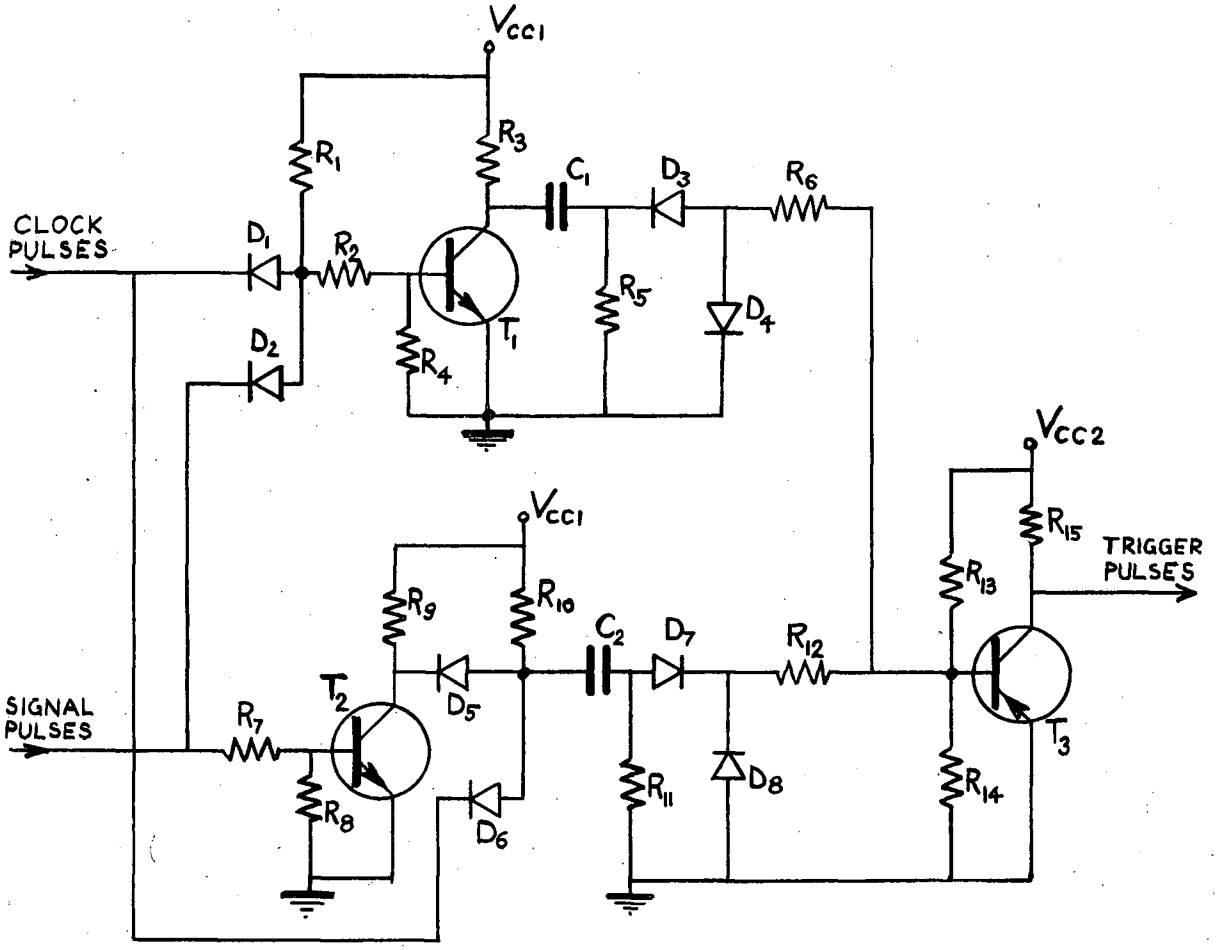
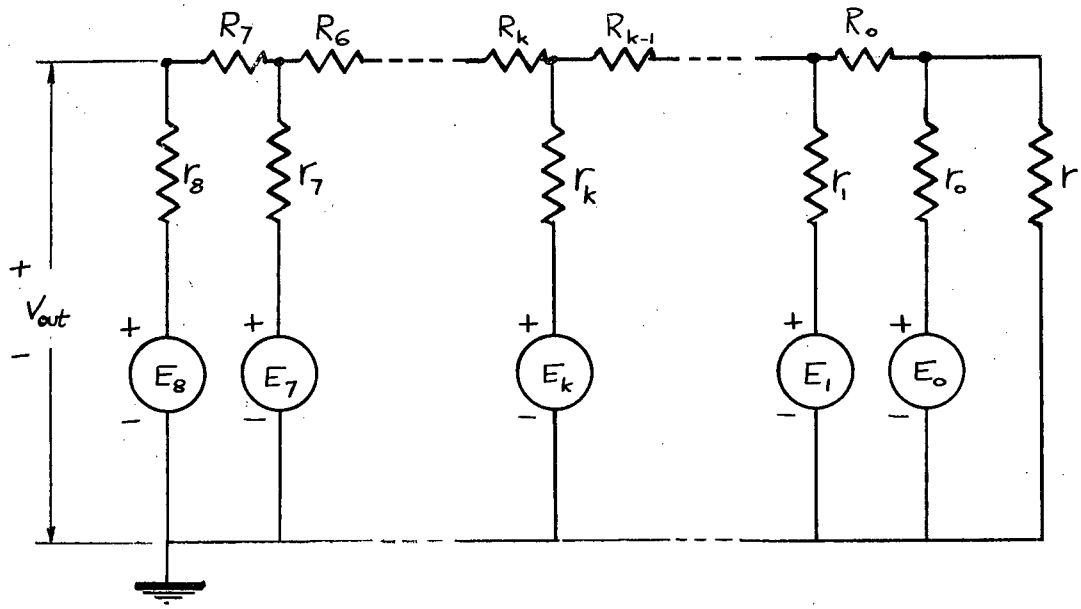


Fig. 12. Trigger Circuit

R_1 = 12K	R_8 = 8.2K	R_{15} = 27K
R_2 = 100K	R_9 = 18K	C_1, C_2 = 0.002 μf
R_3 = 18K	R_{10} = 12K	D_1 to D_8 = Type 1N34A diodes
R_4 = 8.2K	R_{11} = 47K	T_1, T_2 = Type 2N1304 transistors
R_5 = 47K	R_{12} = 22K	T_3 = Type 2N1381 transistor
R_6 = 22K	R_{13} = 470K	V_{cc1} = +6 volts
R_7 = 100K	R_{14} = 1.5K	V_{cc2} = -40 volts

tolerance values are commercially available values nearest to those obtained from inequalities (37) in which a relative accuracy of 0.5% in the output voltage was assumed.



r_0 = 10K, 1%
r_1 = 10K, .5%
r_2 = 10K, .25%
r_3 = 10K, .1%
r_4 = 10K, .05%
r_5 = 10K, .02%
r_6 = 10K, .01%
r_7 = 10K, .005%
r_8 = 7.5K, .005%

r = 10K, 2%
R_0 = 5K, 1%
R_1 = 5K, .5%
R_2 = 5K, .25%
R_3 = 5K, .1%
R_4 = 5K, .05%
R_5 = 5K, .02%
R_6 = 5K, .01%
R_7 = 2.5K, .005%

Fig. 13. Decoding Network

3-5. Switching Circuit for Channel A

To provide the source voltages, E_k, in Fig. 13 we require a circuit activated by the trigger pulses that will give at its

output either +E or -E volts depending on the sign of the trigger pulses. In addition to this, the circuit should hold its output constant until the next change in the sign of the trigger pulses occurs. The circuit of Fig. 14 fulfils both of these requirements. The bistable multivibrator (flip-flop) consisting of T_1 and T_2 is triggered at the base on one side, and hence changes its state only when the sign of the trigger pulses changes. The collector voltage of the opposite side is coupled to the transistor pair T_3, T_4 which provide turn-on and turn-off currents for the switching transistors T_5 and T_6. Depending on the state of the flip-flop, T_5 and T_6 can be either in the ON or OFF states, but not in the same state simultaneously. Ideally, the output voltage is +E volts when T_5 is on, and -E volts when T_6 is on. In practice, however, due to the non-zero saturation voltage of the transistors the output voltage will only approximate the supply voltages $\pm E$. The error can be made relatively small by choosing as large a value for E as the maximum V_{CE}, V_{CB} and V_{BE} ratings of transistors T_5 and T_6 allow. The saturation voltage, or in other words, the error itself can be decreased by driving the transistors well into saturation, and also by operating them in the inverted mode.* In Fig. 15 average saturation characteristics for the type 2N398B transistor (T_5 and T_6) are shown. According to the curves, for the same load and base currents the saturation voltage for small load currents in the inverted mode is considerably less than that in the normal mode. Design values for the base drive currents were obtained from the saturation characteristics as follows. When T_5 is on, the output current flowing into the

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* In the inverted mode the roles of the emitter and collector are interchanged.

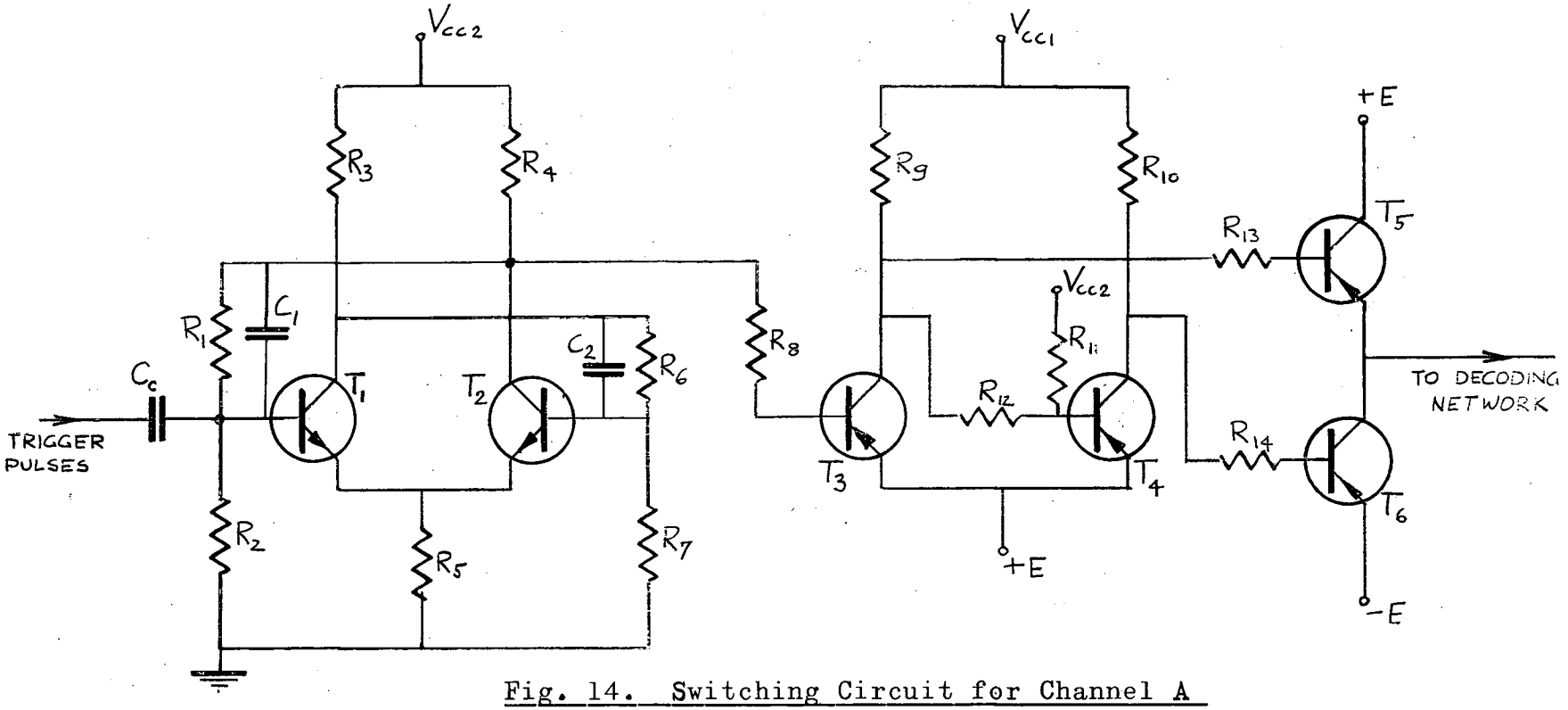


Fig. 14. Switching Circuit for Channel A

R_1 = 150K	R_8 = 82K	C_c = 0.1 μf	
R_2 = 560K	R_9 = 27K	C_1, C_2 = 0.001 μf	
R_3 = 33K	R_{10} = 12K	T_1, T_2 = Type 2N1304 transistors	
R_4 = 22K	R_{11} = 180K	T_3 = Type 2N1381 transistor	
R_5 = 8.2K	R_{12} = 6.8K	T_4, T_5, T_6 = Type 2N398B transistors	
R_6 = 150K	R_{13} = 1K	V_{cc1} = -40 volts	
R_7 = 560K	R_{14} = 1K	V_{cc2} = +40 volts	
		E = 25 volts	

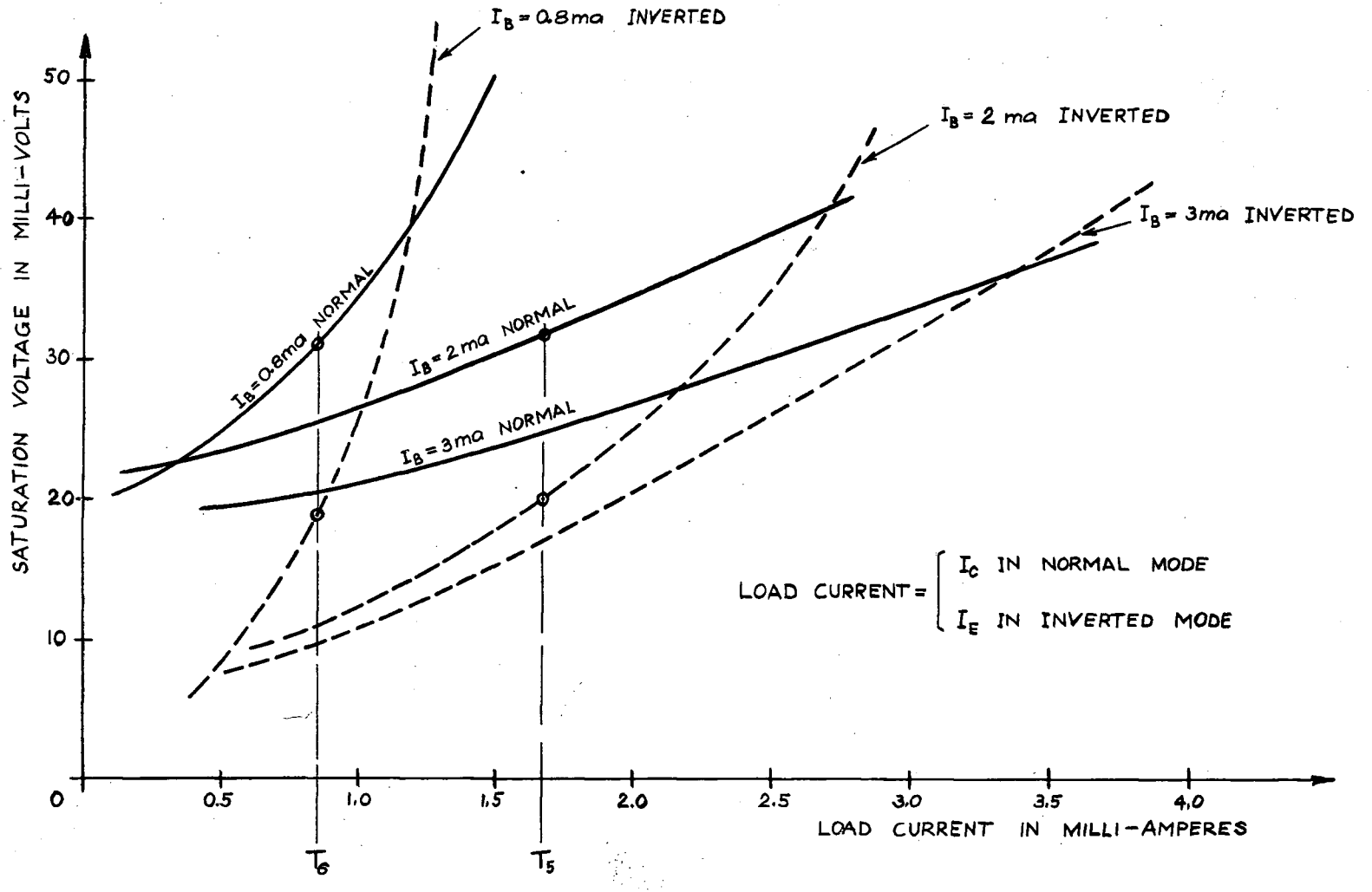


Fig. 15. Saturation Characteristics for the Type 2N398B Transistor

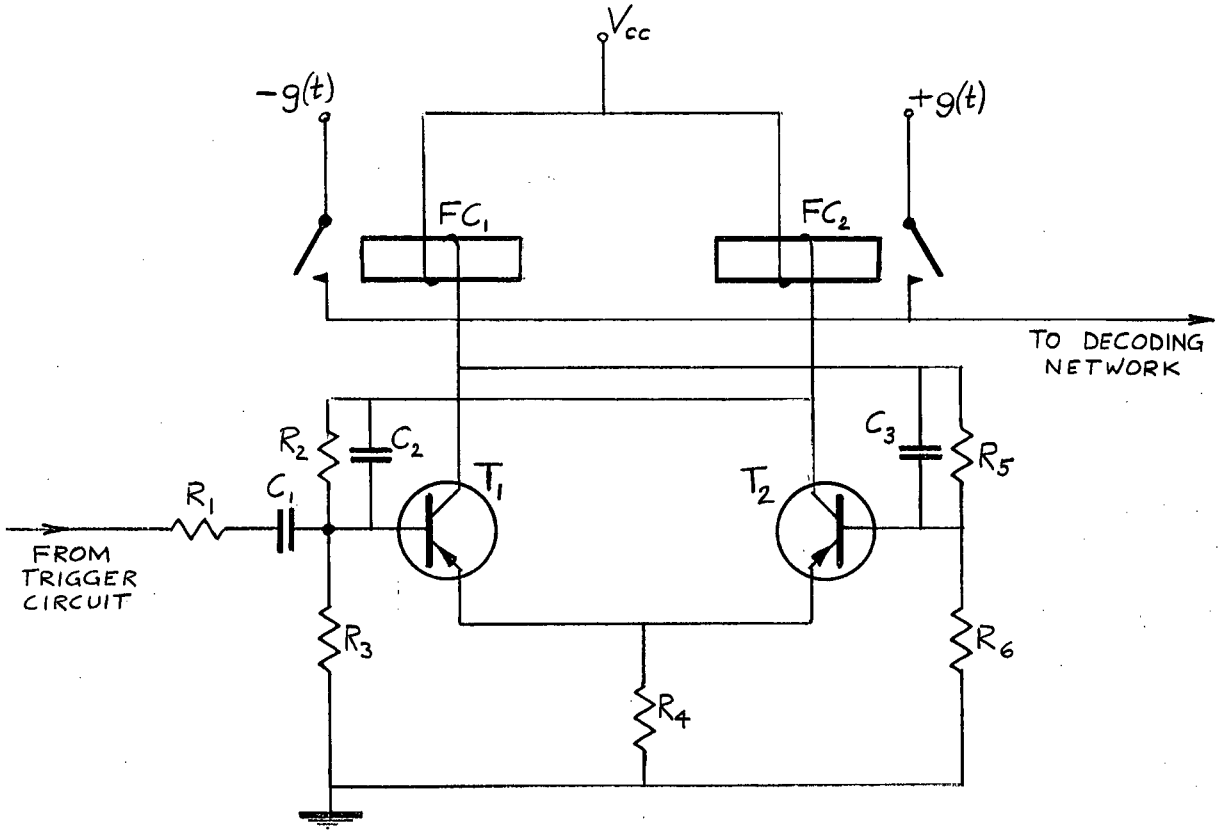
decoding network, which has an equivalent input impedance of 15K, is 25v/15K or 1.67 ma. From the curves in Fig. 15 a base drive of 2 ma with a load current of 1.67 ma results in less than 25mv saturation voltage which represents an error of approximately 0.1% of the output value of 25 volts. When T_6 is on, the output current is again 1.67 ma flowing into the collector of T_6, but the load current is only 1.67 ma less the base drive current. By trial and error one finds that a base drive of 0.8 ma (i.e. a load current of 0.87 ma) yields an error comparable to that introduced across T_5.

3-6. Switching Circuit for Channel B

We already know that in the multiplying channel the role of the constant sources of $\pm$ 25 volts is taken by variable voltages, say $\pm$ g(t). It is immediately apparent that the transistor switch of Fig. 13 cannot work in this case since the collector supply, g(t), changes in both magnitude and sign. In Fig. 16 transistors T_5 and T_6 are replaced by high-speed magnetic reed switches, which eliminate the need for transistors T_3 and T_4 as well. The flip-flop (T_1 and T_2) is still present, and holds the information between conversions, as before. The field coils of the reed switches appear directly in the collector circuits, and hence, the switches are alternatively closed or open according to the state of the flip-flop. Details about the characteristics and preparation of the field coils are given in Appendix II.

3-7. Zero-Level Swtiching

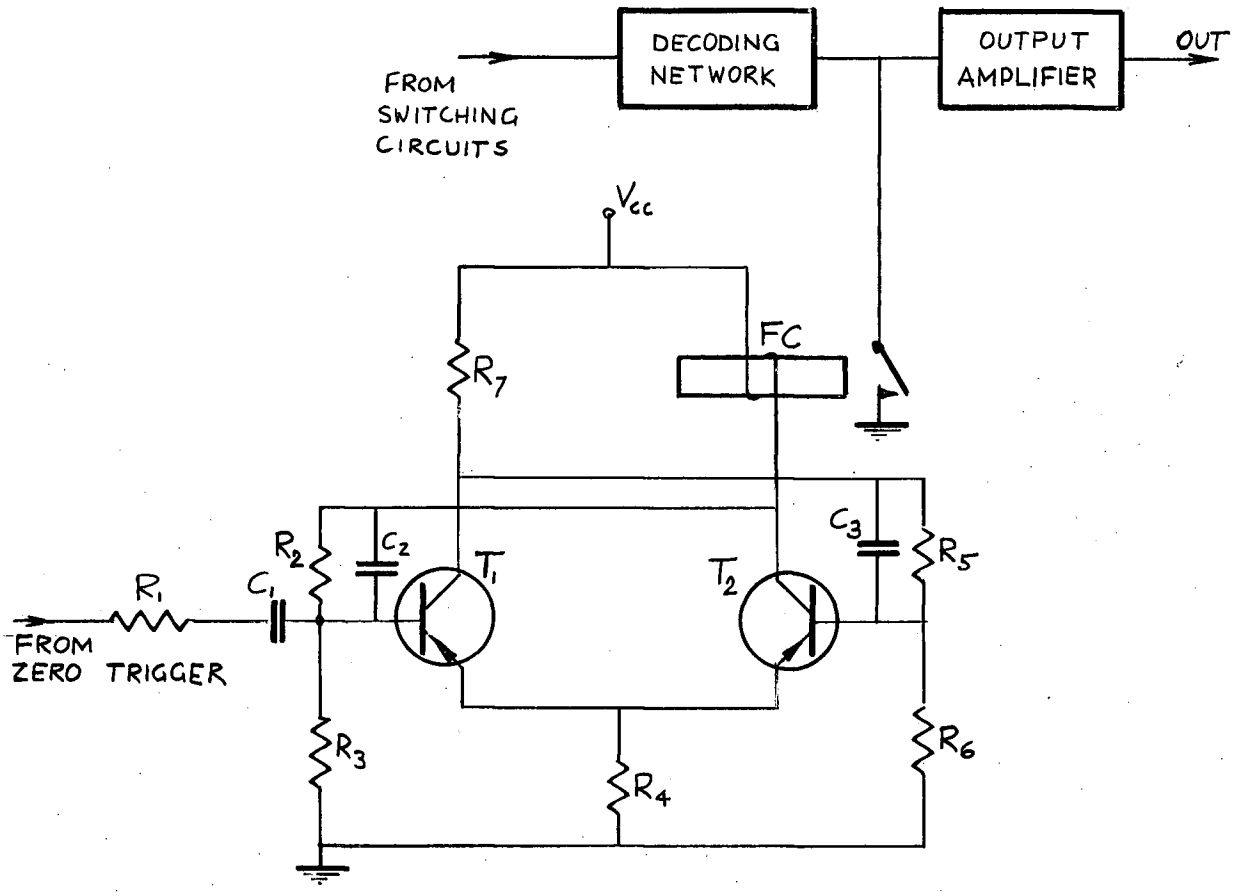
We have seen that a weakness of the resistive decoding



R_1 = 3.3K	R_5 = 820	FC_1, FC_2 = Field coil of reed switch
R_2 = 820	R_6 = 3.9K	T_1, T_2 = Type 2N1381 transistor
R_3 = 3.9K	C_1 = 1 μf	V_{cc} = -6
R_4 = 33	C_2, C_3 = 0.02 μf	

Fig. 16. Switching Circuit for Channel B

networks is the inability to give a zero level output when used as a dual polarity decoder (range of $\pm E$ volts). In cases when the function to be generated only crosses the zero level this is not a disadvantage because the conversion time, in general, will not coincide with the time of crossing. However, when the function takes on the zero value over a number of conversion intervals it may be desirable to have provision for zero level decoding. The use of an extra level on the tape serves this purpose (Fig. 17). Trigger pulses are generated the same way as



R_1 = 3.3K	R_5 = 820	C_2, C_3 = 0.02 μf
R_2 = 820K	R_6 = 3.9K	FC = Field coil of reed switch
R_3 = 3.9K	R_7 = 82	T_1, T_2 = Type 2N1381 transistors
R_4 = 33	C_1 = 1 μf	V_{cc} = -6 volts

Fig. 17. Switching of Zero Level

for the other bit levels. When a hole appears in the zero level on the tape a positive going pulse from the zero trigger turns transistor T_1 off and T_2 on, and hence the reed switch closes and grounds the output amplifier. As soon as the holes in the zero level are absent the trigger pulses change sign, T_2 turns off and the ground is removed from the output amplifier. The circuit of Fig. 17 applies for both channels A and B.

3-8. Output Amplifiers

The requirements imposed on the output amplifiers are three-fold. They should:

(i) convert the relatively high output impedance offered by the decoding networks to a low value,

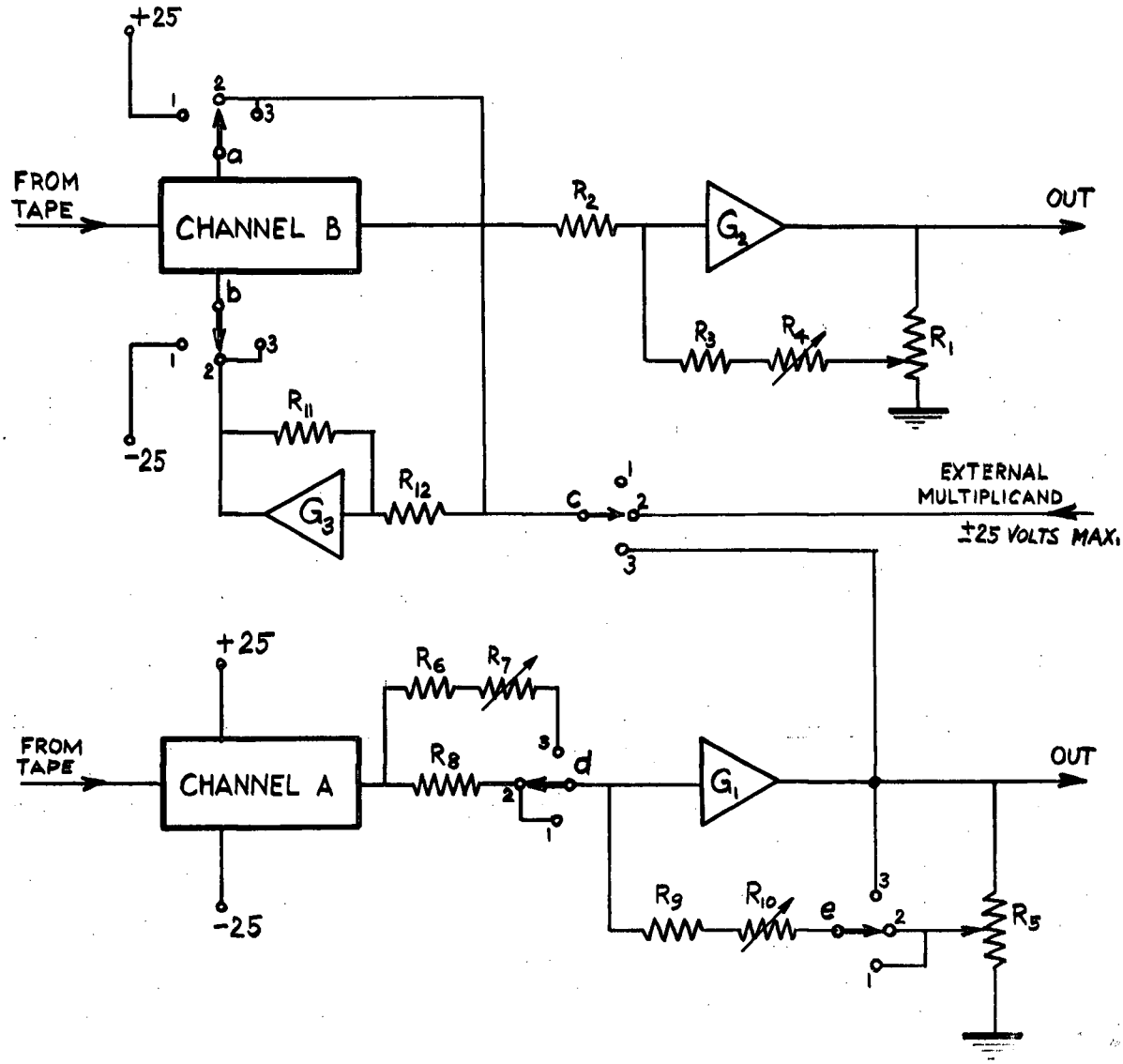
(ii) have a variable gain in order to enhance the versatility of the device,

(iii) have calibrated fixed gains to yield an output range of exactly ± 100 volts.

Fig. 18 illustrates the interconnection of Channels A and B with the three stabilized D.C. amplifiers G_1, G_2, G_3, often known as computing amplifiers. Besides meeting the above requirements, these amplifiers (except G_2) must also be capable of delivering a current of at least 8.5 ma which is the required drive for the decoding network of channel B. Switches a, b, c, d and e are sections of a rotary selector switch (Fig. 22) which selects the mode of operation for the device. The output range of ± 100 volts for both channels A and B is adjusted by R_{10} and R_4, respectively, with the SELECT switch in position 1 and the potentiometers R_1 and R_5 set at 0.25. The SELECT switch is then moved to position 3 and R_7 is adjusted until the output range of channel A is ± 25 volts.

3-9. Power Supplies

Except for the high-voltage sources for the amplifiers which are supplied by an external power source, all voltages are provided by internal power supplies. The first of these (Fig. 19)



R_1, R_5 = 100K, 10-turn potentiometer

R_2, R_3, R_6, R_8, R_9 = 10M, 1% resistor

R_4, R_7, R_{10} = 500K, variable resistor

R_{11}, R_{12} = 10M, $\frac{1}{4}$% resistor

G_1, G_2, G_3 = High gain D.C. amplifiers

a, b, c, d, e = Sections of rotary switch

Fig. 18. Output Circuit

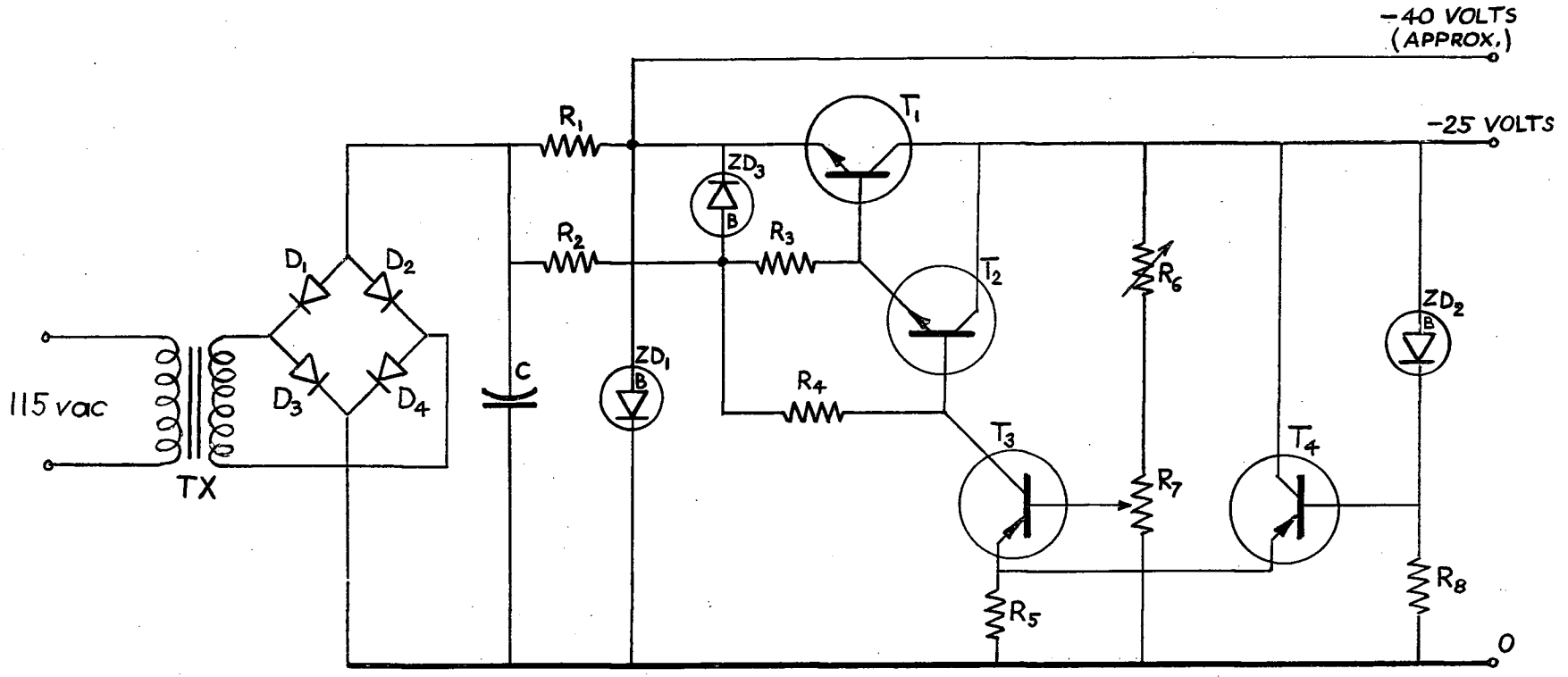


Fig. 19. Short-Circuit Proof Regulated Power Supply

R_1 = 56 , 2 watt
R_2 = 390
R_3, R_4 = 10K
R_5 = 5.6K
R_6 = 1K variable
R_7 = 10K variable
R_8 = 1.8K
C = 1000 µf, 50 WVDC

D_1, D_2, D_3, D_4 = Type 1N2484 rectifier diodes
ZD_1 = Type 1N1366A Zener diode
ZD_2 = Type 1N936 Zener diode
ZD_3 = Type BZY66 Zener diode
T_1 = Type 2N144 transistor
T_2 = Type 2N1304 transistor
T_3, T_4 = Type 2N1381 transistor
TX = Hammond 167U transformer

provides -40 volts and -25 volts. The full-wave rectifier bridge with capacitive output provides approximately -52 volts d.c. which is stepped down to approximately -40 volts by the Zener diode regulator (ZD_1). The rest of the circuit is a feedback regulator providing exactly -25 volts for the decoding network bias. The low temperature coefficient Zener diode ZD_2 is the reference element. The output voltage is compared with the reference by the dividing resistors R_6, R_7, and by the differential amplifier T_3, T_4. Any unbalance is fed back to the series regulator transistors T_2, T_1 which correct the output voltage in the direction to restore the balance. The output voltage is adjustable by resistors R_6 and R_7. For low output currents good regulation is assured by the "keep alive" currents through resistors R_3 and R_4. The value of R_5 determines the current limitation which is an inherent feature of the circuit.* The low output impedance at the -25 volt terminals (less than 0.1 ohm) which appears effectively in series with the decoding resistors is low enough to have negligible effect on the accuracy of conversion.

The circuit of Fig. 20 which provides +40 volts and +25 volts is identical to its counterpart in Fig. 19 except that polarities and diodes are reversed and type PNP transistors are replaced by type NPN. One of the two identical power supplies providing +6 and -6 volts is shown in Fig. 21.

3-10. Control Panel and Driving Mechanism

With the aid of the schematic diagram of the control panel

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* See reference (3), pp. 215-218.

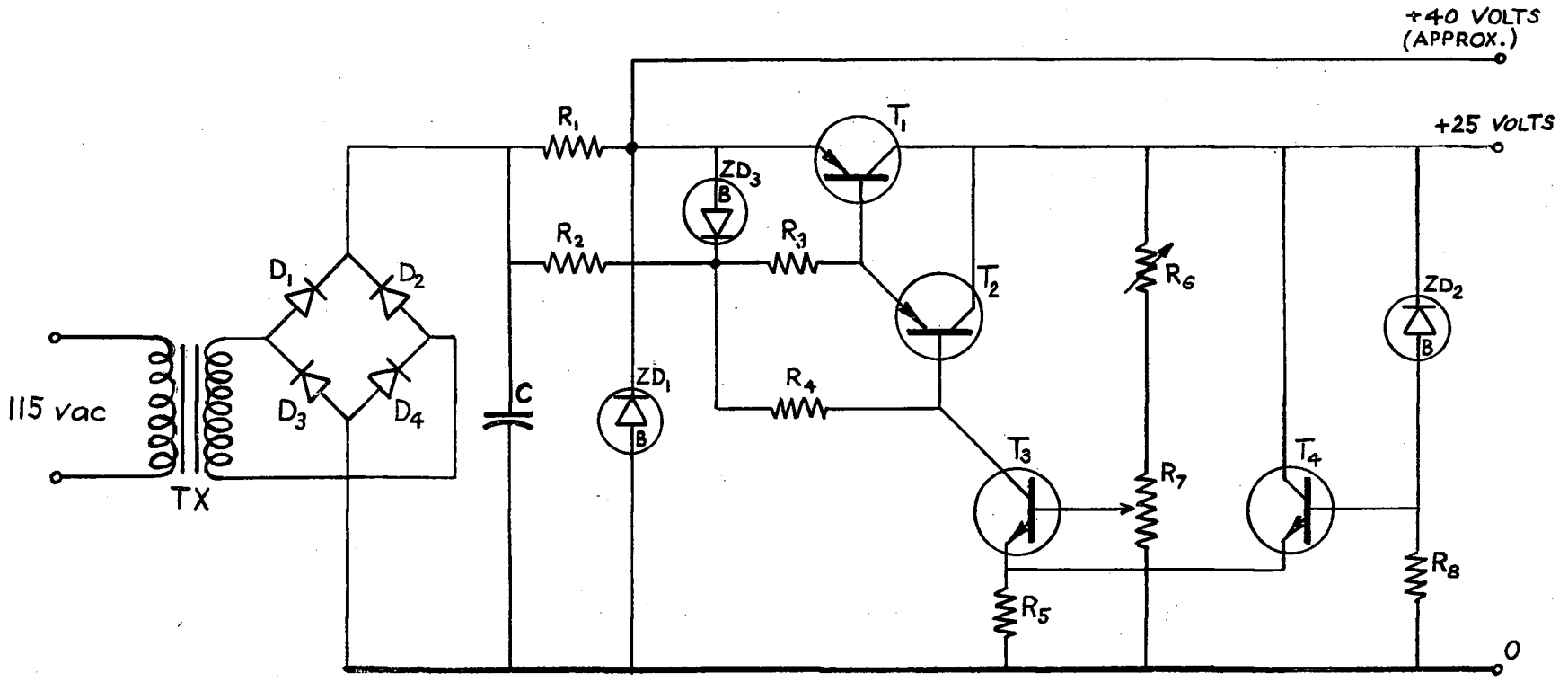
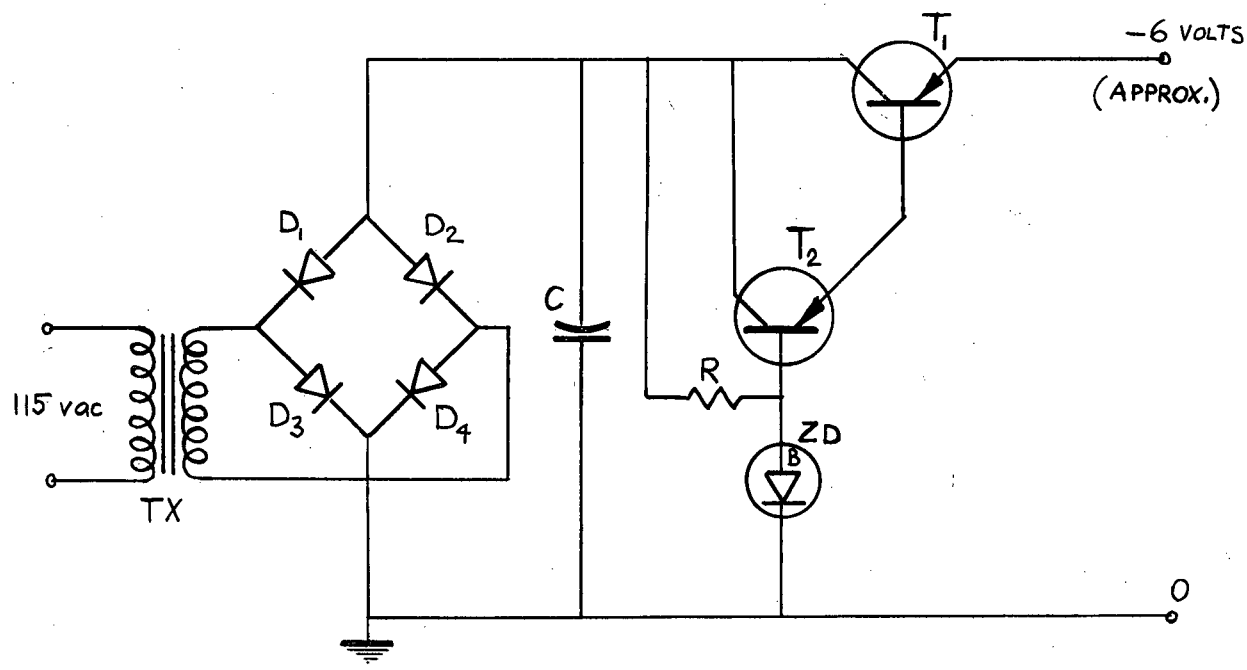


Fig. 20. Short-Circuit Proof Regulated Power Supply

R_1 = 56 , 2 watt
R_2 = 390
R_3, R_4 = 10K
R_5 = 5.6K
R_6 = 1K, variable
R_7 = 10K variable
R_8 = 1.8K
C = 1000 µf, 50 WVDC

D_1, D_2, D_3, D_4 = Type 1N2484 rectifier diodes
ZD_1 = 1N1366AR Zener diode
ZD_2 = Type 1N936 Zener diode
ZD_3 = Type BZY66 Zener diode
T_1 = Type 2N143 transistor
T_2 = Type 2N1381 transistor
T_3, T_4 = Type 2N1304 transistor
TX = Hammond 167U transformer



R = 560
C = 2000 μf, 50 WVDC
T_1 = Type 2N1073 transistor
T_2 = Type 2N600 transistor

D_1, D_2, D_3, D_4 = Type 1N1218 rectifier diodes
ZD = Type BZY66 Zener diode
TX = Hammond Z10E Transformer

Fig. 21. Zener Regulated Power Supply

(Fig. 22) we shall now discuss the various modes of operation of the device.

The two blocks marked A and B are the reading heads for channels A and B, respectively, and contain the light sensors (lower half) and the light source (upper half). The sprocket wheels A_1, A_2 and B_1 are driven by two 2-phase servo motors with tachometer feedback to ensure constant, slip-free motion of the tapes. A_1 and B_1 are mechanically coupled and are driven by one motor (synchronous operation) while the other motor drives A_2.

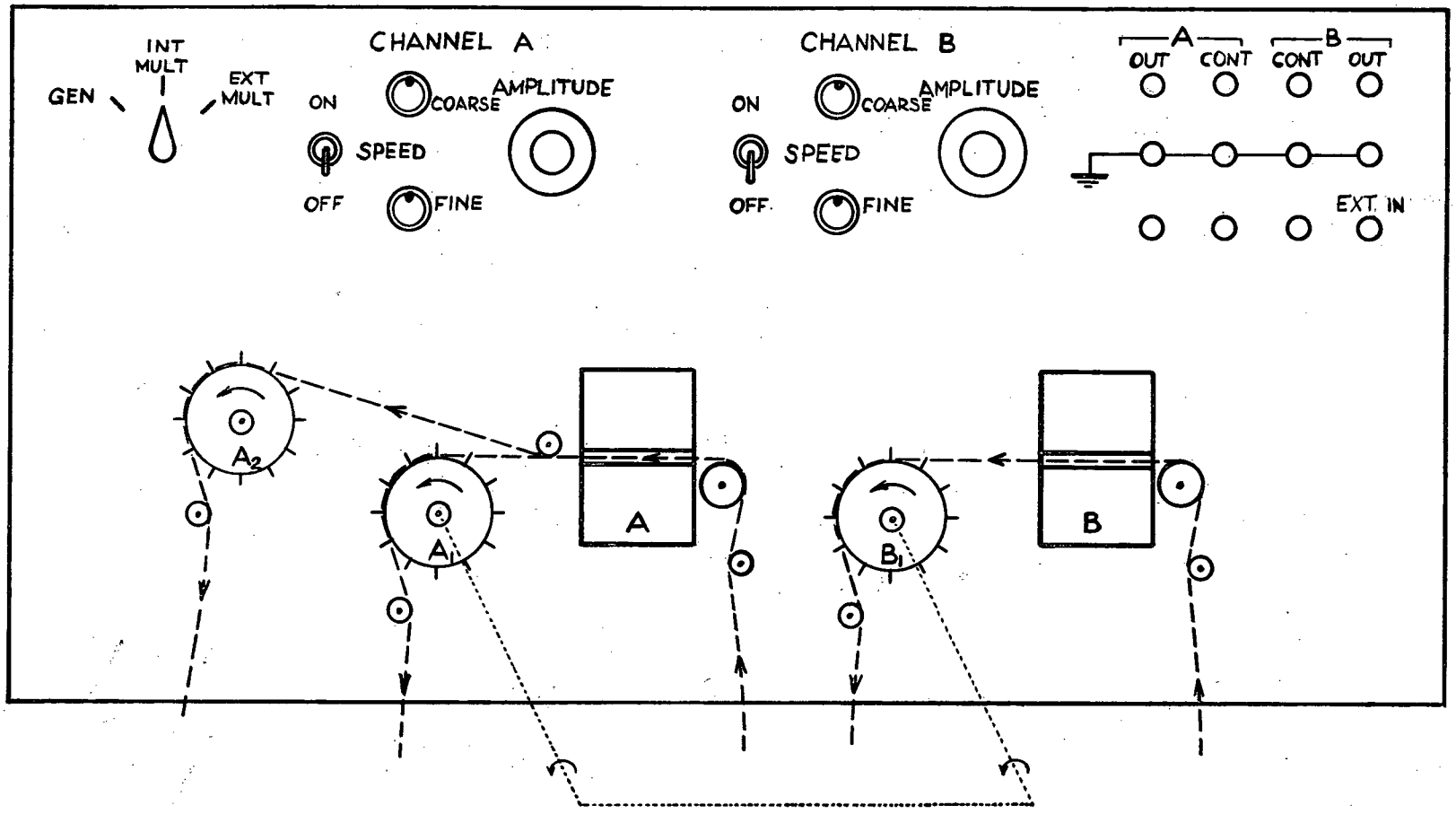


Fig. 22. Control Panel with Tape Drivers

The input tape of channel B is always driven by sprocket B_1, while the other tape may be engaged in either A_1 (for synchronous operation) or in A_2 (if independent speeds are desired).

The modes of operation selected by the three-position **SELECT** switch are the following.

GEN.	Both channels generate functions according to their tape input ($f_A(t)$, $f_B(t)$).
INT. MULT.	Channel A generates $f_A(t)$; Channel B generates $f_B(t)$ and multiplies the two functions together.
EXT. MULT.	Channel A generates $f_A(t)$; Channel B generates $f_B(t)$ and multiplies $f_B(t)$ by the external function introduced at **EXT. IN.**

The output of each channel and the control pulses for de-energizing the reset relay in the computer are brought out at the upper right corner of the panel.

3-11. Summary

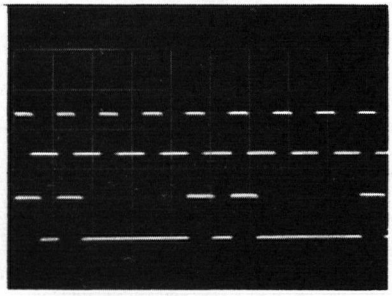
A general outline of the device was presented in the form of a block diagram. Circuits to perform according to initial specifications were designed, and were interconnected according to section 3-1, (Fig. 9).

The results of various tests conducted on the individual levels and on the complete device as a whole are discussed and illustrated in the following chapter.

4. TEST RESULTS

4-1. Testing the Levels Individually

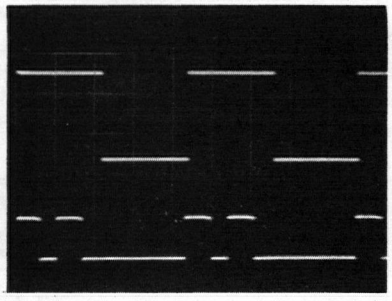
In order to simplify the testing procedure, each level was isolated and tested separately. The first step was to adjust the shaping circuit of each level including the clock pulse level (No. 12), as explained in section 3-2. The purpose of these adjustments was to make the signal pulses slightly wider than the clock pulses. This is required for proper synchronization of the trigger pulses of the various levels. The oscillograms in Fig. 23 show typical waveforms observed during the preliminary tests on the signal levels. In Fig. 23a the reshaped clock pulses (level 12) and signal pulses of level 2 are displayed. In this particular case the hole pattern in level 2 on the tape was periodic: ....1100110011100.... where the numbers 1 and 0 signify the presence and absence of holes, respectively. The signal pulses in Fig. 23a are indeed wider than the clock pulses and they follow the same pattern as the holes on the tape. Fig. 23b shows the signal pulses of level 2 with the output of the associated switching circuit in channel A. This output is the source voltage E_2 (see Fig. 13). It is seen in Fig. 23b that the polarity of the source voltage changes in accordance with the presence or absence of holes. The corresponding waveform for channel B is shown in Fig. 23c. The small dots at the discontinuities manifest the relatively long switching time of the magnetic reed contacts. In reality, at any discontinuity there is only one dot, but, since a single-sweep



Clock pulses (level 12) after shaping (approx. 200 pulses per second)

Signal pulses (level 2) after shaping

a)

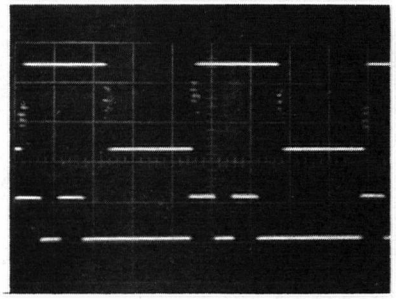


Output of the switching circuit

Associated signal pulses

Channel A (Level 2)

b)



Output of the switching circuit

Associated signal pulses

Channel B (Level 2)

c)

Fig. 23. Oscillograms of Typical Waveforms

trace did not leave an adequate impression on the photographic film, multiple exposure had to be used which resulted in the collection of dots at each of these places on the film.

The waveforms of Fig. 23 were recorded at a tape speed of approximately 200 characters per second (ch/sec) but similar observations were made over the range from 50 ch/sec to 500 ch/sec. Further increase in tape speed was limited by the driving mechanism.

The next step was to make measurements on the speed and accuracy of the individual levels:

a) Channel A

Even at a tape speed of 500 ch/sec, which is the upper limit set by the driving mechanism, the switching time of the transistors (a few μsec) is at least two orders of magnitude smaller than the conversion interval of 2 msec. corresponding to this maximum tape speed. Consequently, the switching time can be assumed negligible. In Channel A it is the saturation voltage across the switching transistors that may limit the quality of the overall performance. Measured values of saturation voltages ranged from 5mv to 20mv in the off state (-25 volt output) and from 15mv to 25mv in the on state (+25 volt output), which agreed very well with design values.

b) Channel B

Again, only one measurement is important, but this time it is the observation of the switching speed. The transition from one state to the other was observed to take place in less than 300 μsec (including bounce) with a maximum time delay of 200 μsec. Both the transition time and the delay time have un-

desirable consequences, namely, they introduce sharp spikes in the generated function. For an ideal reproduction of the function the switches have to change their state instantaneously and with no time delay. If each switch is delayed by the same amount, but acts instantaneously, the function will still be truly reproduced but with a time delay equal to that of the switches. The time delays for the read switches are not necessarily the same for each unit, and therefore, in addition to the slight delay, the reeds will not switch in synchronism, and hence, the function being generated may take on any indeterminate value during the switching interval. This indeterminate value shows up as a sharp spike. The non-zero transition times cause sharp spikes, too, since during the transition intervals the source voltages (E_k) themselves are indeterminate, and hence their weighted sum, i.e. the value of the function being generated is also indeterminate.

It is impossible to establish a criterion for the maximum acceptable switching time. Zero delay and zero transition time are ideal, and delay and transition times comparable to the conversion interval are definitely not acceptable. Hence, the maximum limit is somewhere between the two extremes and its exact place depends on the quality of reproduction sought. It must be emphasized that usually a fair number of spikes can be tolerated, since, having a limited frequency response, most of the analog computing and recording equipment will tend to smooth the spikes out, or may not even "see" them at all. Both the time delays and transition times of 200 μsec and 300 μsec, respectively, are only small fractions of the conversion interval

at low and moderate tape speeds. As the tape approaches the speed of 500 ch/sec, however, they become comparable to the conversion interval, and consequently, for channel B, the conversion speed is not limited by the tape-drive mechanism only, but by the switching time of the reed contacts as well.

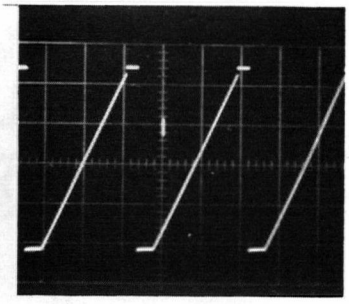
In channel B the switching accuracy is determined by the contact resistance of the reeds which were found to be less than 0.5 ohms. With a current of less than 2 ma flowing through them, the resulting voltage drop of less than 1 mv across the reed switches can be assumed negligible compared to the full scale value of 25 volts.

4-2. Testing the Decoding Network

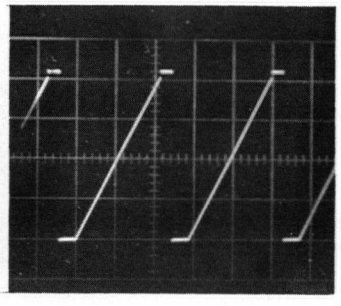
Bias voltages of $\pm$ 25 volts were applied to the nine decoding resistors directly from the power supplies. Output voltages in various regions over the full output range were measured with a high accuracy differential voltmeter, and were found to be very accurate in the vicinity of full scale output. The degree of accuracy decreased with lower output voltages, but remained less than 1% even around the zero level output.

4-3. Testing the Overall Performance

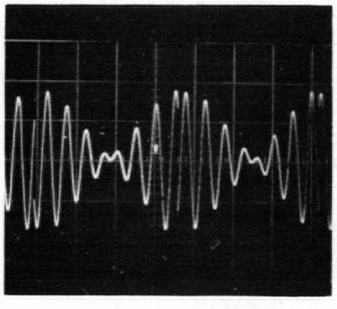
When the individual levels had been checked separately, the device as a whole was tested for function generation and multiplication. Fig. 24a shows the test function as generated by channel A, while the same function generated by channel B appears in Fig. 24b. The two waveforms appear to be the same, however, the spikes discussed in section 4-1 were visible on the



a) Test function as generated by Channel A



b) Test function as generated by Channel B



c) Product of the test function and an external function (sinusoidal)

Fig. 24. Output Waveforms Showing Overall Performance

oscilloscope but did not register in the photographic film in Fig. 24b, for they were very narrow and faint. It is interesting to note that the largest spike occurred at the mid-point of the ramp portion, i.e. when the switch associated with the most significant binary digit changed its state. The next largest spikes (two of approximately equal magnitudes) appeared at points $\frac{1}{4}$ and $\frac{3}{4}$ of the distance along the ramp. These points corresponded to the second most significant binary digit. A few more spikes were observed but their magnitudes were very small.

The next step consisted of the testing of the EXTERNAL MULTIPLY mode of operation. The test function was generated on channel B and an external sine function was applied as the bias on the decoding network of channel B. The product of the two functions is shown in Fig. 24c, as it appeared at the output of channel B. The frequency of the sine wave was a few times larger than that of the test function.

The INTERNAL MULTIPLY mode of operation was not tested, because two of the light sensors in one of the reader heads were accidentally damaged, and replacements did not arrive in time for test results to be included in this publication. Both channels were tested separately and the results indicate that the device can be expected to work satisfactorily in this third mode of operation as well.

4-4. Summary

The various tests on the individual levels and on the integrated device itself, were conducted mainly to establish

speed and accuracy measurements and to check the general performance of the device. The results can be summarized as follows:

Channel A:

Switching speeds are negligible over the speed range determined by the tape-drive mechanism. Switching accuracy is adequate, measured offset voltages being the same as, or less than, the design values.

Channel B:

Offset voltages (across reed contacts) are negligible. Switching speeds are adquate at low and medium speeds but become unacceptable at speeds approaching 500 ch/sec.

The device was tested for multiplication in the EXTERNAL MULTIPLY mode only, and was found to function satisfactorily.

5. CONCLUSION

A double input device consisting of two channels and operated by punched tape was developed. In its three modes of operation the unit can:

a) generate two functions independently,

b) generate two functions and multiply them together, and

c) generate two functions and multiply one of them by an external computer variable.

In both channels the simplest and fastest method of digital-to-analog conversion, namely, the decoding by a resistive network, is used. The precision resistors used in the decoding networks and, in channel A, the transistorized switching circuits ensure high-speed and high-accuracy (better than 1%) function generation. The application of magnetic reed switches in channel B allows for high-accuracy four-quadrant multiplication, but the relatively slow switching speeds of the reed contacts prevent the multiplier channel from being used at tape speeds higher than 400 ch/sec. The speed and gain controls provide convenient time and amplitude scaling of the output of both channels, and hence greatly increase the versatility of the device in analog computer applications, especially where the relation between system performance and changes in driving function amplitude and/or frequency is investigated.

In light of the experimental results the following comments on the possible improvement of the device are in order. In its present form the device is operated by a 12-level tape, which

has to be punched manually prior to the use of the device. A major improvement would be to change the tape to a 7-level tape used in the recently acquired digital computer installation of the Department of Electrical Engineering. This change would make the use of the high-speed punch possible and would greatly shorten the time of tape preparation. The modifications on the device required by the use of this new tape would be:

i) to change the sprocket wheels to fit the dimensions of the new tape, and

ii) to construct new reading heads, which would read two lines at a time (block reader) so that all twelve bits of a character can be read simultaneously.

The proposed modification suggests a new field of application of the device, namely hybrid computation and simulation, where analog functions have to be generated directly from the output of a digital computer.

In view of the experience gained during his association with this project, the author believes that the device developed could be improved by the proposed modification, but is nonetheless a worth-while and versatile addition to the field of analog computation.

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APPENDIX I

Representation of Functions on the Tape

Functions of time to be generated are stored on the tape by point-value representation. The values of the function at equal intervals are coded into binary numbers by means of Table 1, in which the numbers 0 and 1 mean the absence and presence of a hole, respectively. (Level 1 is the one closest to the panel when the tape is in position). Level 12 generates the clock pulses and should have holes punched in every position along it. Level 11 is reserved for the generation of control

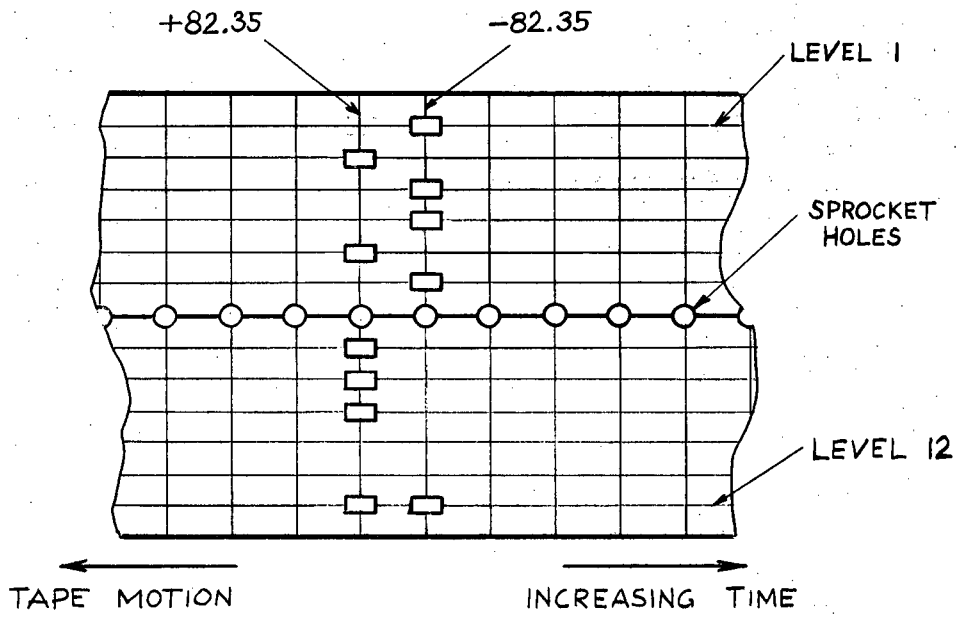


Fig. 25. Example of Coding

pulses and should have one hole to mark the beginning of the

function. The pulse due to this hole de-energizes the reset relay in the computer and initiates the compute mode.

EXAMPLE: Suppose the function to be generated changes from +82.35 volts to -82.35 volts. The two consecutive characters representing this discontinuity are punched as shown in Fig. 25. The first character is found by locating the range in the "MAGNITUDE" column that includes the absolute value of the function, i.e. 82.35, and then by choosing the hole combination in the "POSITIVE" column, since the value of the function is positive. The second character is found in the same line but in the "NEGATIVE" column, since the value of the function is negative.

Table 1. Binary Code for Representing Functions on the Tape

MAGNITUDE	SIGN																			
	+										-									
	LEVEL										LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
0.000	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
0.001- 0.391	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0.392- 0.781	0	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	0
0.782- 1.17	0	1	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0	1
1.18 - 1.56	0	1	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	0	0
1.57 - 1.95	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	1	1
1.96 - 2.34	0	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	1	0
2.35 - 2.73	0	1	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0	1
2.74 - 3.16	0	1	0	0	0	0	0	1	1	1	0	0	1	1	1	1	1	0	0	0
3.17 - 3.52	0	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1	1	1
3.53 - 3.91	0	1	0	0	0	0	1	0	0	1	0	0	1	1	1	1	0	1	1	0
3.92 - 4.30	0	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	1	0	1
4.31 - 4.69	0	1	0	0	0	0	1	0	1	1	0	0	1	1	1	1	0	1	0	0
4.70 - 5.08	0	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1
5.09 - 5.47	0	1	0	0	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1	0
5.48 - 5.86	0	1	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	0	1
5.87 - 6.25	0	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0
6.26 - 6.64	0	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1	1	1
6.65 - 7.03	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	0	1	1	1	0
7.04 - 7.42	0	1	0	0	0	1	0	0	1	0	0	0	1	1	1	0	1	1	0	1
7.43 - 7.81	0	1	0	0	0	1	0	0	1	1	0	0	1	1	1	0	1	1	0	0
7.82 - 8.20	0	1	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	0	1	1
8.21 - 8.59	0	1	0	0	0	1	0	1	0	1	0	0	1	1	1	0	1	0	1	0
8.60 - 8.98	0	1	0	0	0	1	0	1	1	0	0	0	1	1	1	0	1	0	0	1
8.99 - 9.36	0	1	0	0	0	1	0	1	1	1	0	0	1	1	1	0	1	0	0	0
9.37 - 9.77	0	1	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1
9.78 -10.2	0	1	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	1	1	0
10.3 -10.5	0	1	0	0	0	1	1	0	1	0	0	0	1	1	1	0	0	1	0	1
10.6 -10.9	0	1	0	0	0	1	1	0	1	1	0	0	1	1	1	0	0	1	0	0
11.0 -11.3	0	1	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0	1	1
11.4 -11.7	0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	0	0	0	1	0
11.8 -12.1	0	1	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0	1
12.2 -12.5	0	1	0	0	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0	0
12.6 -12.9	0	1	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	1	1
13.0 -13.3	0	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1	1	0
13.4 -13.7	0	1	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	1	0	1
13.8 -14.1	0	1	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	0	0
14.2 -14.5	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1
14.6 -14.8	0	1	0	0	1	0	0	1	0	1	0	0	1	1	0	1	1	0	1	0
14.9 -15.2	0	1	0	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+										-									
	LEVEL										LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
15.3 -15.6	0	1	0	0	1	0	0	1	1	1	0	0	1	1	0	1	1	0	0	0
15.7 -16.0	0	1	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1	1	1
16.1 -16.4	0	1	0	0	1	0	1	0	0	1	0	0	1	1	0	1	0	1	1	0
16.5 -16.8	0	1	0	0	1	0	1	0	1	0	0	0	1	1	0	1	0	1	0	1
16.9 -17.2	0	1	0	0	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0	0
17.3 -17.6	0	1	0	0	1	0	1	1	0	0	0	0	1	1	0	1	0	0	1	1
17.7 -18.0	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1	0	0	1	0
18.1 -18.4	0	1	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	0	0	1
18.5 -18.8	0	1	0	0	1	0	1	1	1	1	0	0	1	1	0	1	0	0	0	0
18.9 -19.1	0	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	1
19.2 -19.5	0	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1	1	0
19.6 -19.9	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0	1
20.0 -20.3	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
20.4 -20.7	0	1	0	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	1
20.8 -21.1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0
21.2 -21.5	0	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1	0	0	1
21.6 -21.9	0	1	0	0	1	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0
22.0 -22.3	0	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1
22.4 -22.7	0	1	0	0	1	1	1	0	0	1	0	0	1	1	0	0	0	1	1	0
22.8 -23.1	0	1	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0	1	0	1
23.2 -23.4	0	1	0	0	1	1	1	0	1	1	0	0	1	1	0	0	0	1	0	0
23.5 -23.8	0	1	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1
23.9 -24.2	0	1	0	0	1	1	1	1	0	1	0	0	1	1	0	0	0	0	1	0
24.3 -24.6	0	1	0	0	1	1	1	1	1	0	0	0	1	1	0	0	0	0	0	1
24.7 -25.0	0	1	0	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	0
25.1 -25.4	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
25.5 -25.8	0	1	0	1	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	0
25.9 -26.2	0	1	0	1	0	0	0	0	1	0	0	0	1	0	1	1	1	1	0	1
26.3 -26.6	0	1	0	1	0	0	0	0	1	1	0	0	1	0	1	1	1	1	0	0
26.7 -27.0	0	1	0	1	0	0	0	1	0	0	0	0	1	0	1	1	1	0	1	1
27.1 -27.3	0	1	0	1	0	0	0	1	0	1	0	0	1	0	1	1	1	0	1	0
27.4 -27.7	0	1	0	1	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	1
27.8 -28.1	0	1	0	1	0	0	0	1	1	1	0	0	1	0	1	1	1	0	0	0
28.2 -28.5	0	1	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1	1
28.6 -28.9	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1	0
29.0 -29.3	0	1	0	1	0	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1
29.4 -29.7	0	1	0	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1	0	0
29.8 -30.1	0	1	0	1	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1	1
30.2 -30.5	0	1	0	1	0	0	1	1	0	1	0	0	1	0	1	1	0	0	1	0
30.6 -30.9	0	1	0	1	0	0	1	1	1	0	0	0	1	0	1	1	0	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+ LEVEL										- LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
31.0 -31.3	0	1	0	1	0	0	1	1	1	1	0	0	1	0	1	1	0	0	0	0
31.4 -31.6	0	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	1	1	1
31.7 -32.0	0	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1	1	1	0
32.1 -32.4	0	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0	1
32.5 -32.8	0	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0
32.9 -33.2	0	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	0	1	1
33.3 -33.6	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0
33.7 -34.0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	1	0	1	0	0	1
34.1 -34.4	0	1	0	1	0	1	0	1	1	1	0	0	1	0	1	0	1	0	0	0
34.5 -34.8	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1
34.9 -35.2	0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	0	0	1	1	0
35.3 -35.5	0	1	0	1	0	1	1	0	1	0	0	0	1	0	1	0	0	1	0	1
35.6 -35.9	0	1	0	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	0	0
36.0 -36.3	0	1	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0	1	1
36.4 -36.7	0	1	0	1	0	1	1	1	0	1	0	0	1	0	1	0	0	0	1	0
36.8 -37.1	0	1	0	1	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0	1
37.2 -37.5	0	1	0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	0	0	0
37.6 -37.9	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1
38.0 -38.3	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1	1	1	0
38.4 -38.7	0	1	0	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1	0	1
38.8 -39.1	0	1	0	1	1	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0
39.2 -39.5	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1
39.6 -39.8	0	1	0	1	1	0	0	1	0	1	0	0	1	0	0	1	1	0	1	0
39.9 -40.2	0	1	0	1	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1
40.3 -40.6	0	1	0	1	1	0	0	1	1	1	0	0	1	0	0	1	1	0	0	0
40.7 -41.0	0	1	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1	1	1
41.1 -41.4	0	1	0	1	1	0	1	0	0	1	0	0	1	0	0	1	0	1	1	0
41.5 -41.8	0	1	0	1	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0	1
41.9 -42.2	0	1	0	1	1	0	1	0	1	1	0	0	1	0	0	1	0	1	0	0
42.3 -42.6	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1
42.7 -43.0	0	1	0	1	1	0	1	1	0	1	0	0	1	0	0	1	0	0	1	0
43.1 -43.4	0	1	0	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	1
43.5 -43.8	0	1	0	1	1	0	1	1	1	1	0	0	1	0	0	1	0	0	0	0
43.9 -44.1	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1	1
44.2 -44.5	0	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1	0
44.6 -44.9	0	1	0	1	1	1	0	0	1	0	0	0	1	0	0	0	1	1	0	1
45.0 -45.3	0	1	0	1	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0
45.4 -45.7	0	1	0	1	1	1	0	1	0	0	0	0	1	0	0	0	1	0	1	1
45.8 -46.1	0	1	0	1	1	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0
46.2 -46.5	0	1	0	1	1	1	0	1	1	0	0	0	1	0	0	0	1	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+ LEVEL										- LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
46.6 -46.9	0	1	0	1	1	1	0	1	1	1	0	0	1	0	0	0	1	0	0	0
47.0 -47.3	0	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1
47.4 -47.7	0	1	0	1	1	1	1	0	0	1	0	0	1	0	0	0	0	1	1	0
47.8 -48.0	0	1	0	1	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0	1
48.1 -48.4	0	1	0	1	1	1	1	0	1	1	0	0	1	0	0	0	0	1	0	0
48.5 -48.8	0	1	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1
48.9 -49.2	0	1	0	1	1	1	1	1	0	1	0	0	1	0	0	0	0	0	1	0
49.3 -49.6	0	1	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	1
49.7 -50.0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0
50.1 -50.4	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
50.5 -50.8	0	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	0
50.9 -51.2	0	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	1
51.3 -51.6	0	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0
51.7 -52.0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1	1
52.1 -52.3	0	1	1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	1	0
52.4 -52.7	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0	1
52.8 -53.1	0	1	1	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	0
53.2 -53.5	0	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1	1
53.6 -53.9	0	1	1	0	0	0	1	0	0	1	0	0	0	1	1	1	0	1	1	0
54.0 -54.3	0	1	1	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	0	1
54.4 -54.7	0	1	1	0	0	0	1	0	1	1	0	0	0	1	1	1	0	1	0	0
54.8 -55.1	0	1	1	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0	1	1
55.2 -55.5	0	1	1	0	0	0	1	1	0	1	0	0	0	1	1	1	0	0	1	0
55.6 -55.9	0	1	1	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0	1
56.0 -56.3	0	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	0	0	0	0
56.4 -56.6	0	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1	1
56.7 -57.0	0	1	1	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	1	0
57.1 -57.4	0	1	1	0	0	1	0	0	1	0	0	0	0	1	1	0	1	1	0	1
57.5 -57.8	0	1	1	0	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0	0
57.9 -58.2	0	1	1	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1	1
58.3 -58.6	0	1	1	0	0	1	0	1	0	1	0	0	0	1	1	0	1	0	1	0
58.7 -59.0	0	1	1	0	0	1	0	1	1	0	0	0	0	1	1	0	1	0	0	1
59.1 -59.4	0	1	1	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	0	0
59.5 -59.8	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1
59.9 -60.2	0	1	1	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	1	0
60.3 -60.5	0	1	1	0	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1
60.6 -60.9	0	1	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1	0	0
61.0 -61.3	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	1	1
61.4 -61.7	0	1	1	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0	1	0
61.8 -62.1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+										-									
	LEVEL										LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
62.2 -62.5	0	1	1	0	0	1	1	1	1	1	0	0	0	1	1	0	0	0	0	0
62.6 -62.9	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1
63.0 -63.3	0	1	1	0	1	0	0	0	0	1	0	0	0	1	0	1	1	1	1	0
63.4 -63.7	0	1	1	0	1	0	0	0	1	0	0	0	0	1	0	1	1	1	0	1
63.8 -64.1	0	1	1	0	1	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0
64.2 -64.5	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	1	1
64.6 -64.8	0	1	1	0	1	0	0	1	0	1	0	0	0	1	0	1	1	0	1	0
64.9 -65.2	0	1	1	0	1	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
65.3 -65.6	0	1	1	0	1	0	0	1	1	1	0	0	0	1	0	1	1	0	0	0
65.7 -66.0	0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	1	1
66.1 -66.4	0	1	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0
66.5 -66.8	0	1	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	0	1
66.9 -67.2	0	1	1	0	1	0	1	0	1	1	0	0	0	1	0	1	0	1	0	0
67.3 -67.6	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	0	1	1
67.7 -68.0	0	1	1	0	1	0	1	1	0	1	0	0	0	1	0	1	0	0	1	0
68.1 -68.4	0	1	1	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0	1
68.5 -68.8	0	1	1	0	1	0	1	1	1	1	0	0	0	1	0	1	0	0	0	0
68.9 -69.1	0	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	1
69.2 -69.5	0	1	1	0	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1	0
69.6 -69.9	0	1	1	0	1	1	0	0	1	0	0	0	0	1	0	0	1	1	0	1
70.0 -70.3	0	1	1	0	1	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0
70.4 -70.7	0	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1	1
70.8 -71.1	0	1	1	0	1	1	0	1	0	1	0	0	0	1	0	0	1	0	1	0
71.2 -71.5	0	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1
71.6 -71.9	0	1	1	0	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	0
72.0 -72.3	0	1	1	0	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1
72.4 -72.7	0	1	1	0	1	1	1	0	0	1	0	0	0	1	0	0	0	1	1	0
72.8 -73.0	0	1	1	0	1	1	1	0	1	0	0	0	0	1	0	0	0	1	0	1
73.1 -73.4	0	1	1	0	1	1	1	0	1	1	0	0	0	1	0	0	0	1	0	0
73.5 -73.8	0	1	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	1	1
73.9 -74.2	0	1	1	0	1	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0
74.3 -74.6	0	1	1	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1
74.7 -75.0	0	1	1	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0
75.1 -75.4	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
75.5 -75.8	0	1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0
75.9 -76.2	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	1
76.3 -76.6	0	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0
76.7 -77.0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	1
77.1 -77.3	0	1	1	1	0	0	0	1	0	1	0	0	0	0	1	1	1	0	1	0
77.4 -77.7	0	1	1	1	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+ LEVEL										- LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
77.8 -78.1	0	1	1	1	0	0	0	1	1	1	0	0	0	0	1	1	1	0	0	0
78.2 -78.5	0	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1	1
78.6 -78.9	0	1	1	1	0	0	1	0	0	1	0	0	0	0	1	1	0	1	1	0
79.0 -79.3	0	1	1	1	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1
79.4 -79.7	0	1	1	1	0	0	1	0	1	1	0	0	0	0	1	1	0	1	0	0
79.8 -80.1	0	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	1
80.2 -80.5	0	1	1	1	0	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0
80.6 -80.9	0	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0	1
81.0 -81.3	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	0
81.4 -81.6	0	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	1
81.7 -82.0	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	0	1	1	1	0
82.1 -82.4	0	1	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	1
82.5 -82.8	0	1	1	1	0	1	0	0	1	1	0	0	0	0	1	0	1	1	0	0
82.9 -83.2	0	1	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1	1
83.3 -83.6	0	1	1	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	0
83.7 -84.0	0	1	1	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	0	1
84.1 -84.4	0	1	1	1	0	1	0	1	1	1	0	0	0	0	1	0	1	0	0	0
84.5 -84.8	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1
84.9 -85.2	0	1	1	1	0	1	1	0	0	1	0	0	0	0	1	0	0	1	1	0
85.3 -85.5	0	1	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0	1
85.6 -85.9	0	1	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0
86.0 -86.3	0	1	1	1	0	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1
86.4 -86.7	0	1	1	1	0	1	1	1	0	1	0	0	0	0	1	0	0	0	1	0
86.8 -87.1	0	1	1	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	1
87.2 -87.5	0	1	1	1	0	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0
87.6 -87.9	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
88.0 -88.3	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0
88.4 -88.7	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1
88.8 -89.1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	0	1	1	1	0	0
89.2 -89.5	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0	1	1
89.6 -89.8	0	1	1	1	1	0	0	1	0	1	0	0	0	0	0	1	1	0	1	0
89.9 -90.2	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0	1
90.3 -90.6	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	0	0
90.7 -91.0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1
91.1 -91.4	0	1	1	1	1	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0
91.5 -91.8	0	1	1	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0	1
91.9 -92.2	0	1	1	1	1	0	1	0	1	1	0	0	0	0	0	1	0	1	0	0
92.3 -92.6	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1
92.7 -93.0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	1	0
93.1 -93.4	0	1	1	1	1	0	1	1	1	0	0	0	0	0	0	1	0	0	0	1

Table 1 (Contd.)

MAGNITUDE	SIGN																			
	+										-									
	LEVEL										LEVEL									
From-To	10	9	8	7	6	5	4	3	2	1	10	9	8	7	6	5	4	3	2	1
93.5 -93.8	0	1	1	1	1	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0
93.9 -94.1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
94.2 -94.5	0	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	1	1	1	0
94.6 -94.9	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0	1
95.0 -95.3	0	1	1	1	1	1	0	0	1	1	0	0	0	0	0	0	1	1	0	0
95.4 -95.7	0	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	1
95.8 -96.1	0	1	1	1	1	1	0	1	0	1	0	0	0	0	0	0	1	0	1	0
96.2 -96.5	0	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1
96.6 -96.9	0	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	1	0	0	0
97.0 -97.3	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1
97.4 -97.7	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	1	1	0
97.8 -98.0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1
88.1 -98.4	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1	0	0
98.5 -98.8	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1
98.9 -99.2	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	1	0
99.3 -99.6	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
99.7 -100	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0

APPENDIX II

Construction Details

The combination function generator and multiplier made up of three parts is mounted on a standard 19 inch rack (Fig. 26). The lower part consists of the sprocket wheels and reader heads in front of the panel and the driving motors and the transformers behind the panel. The middle part is the con-

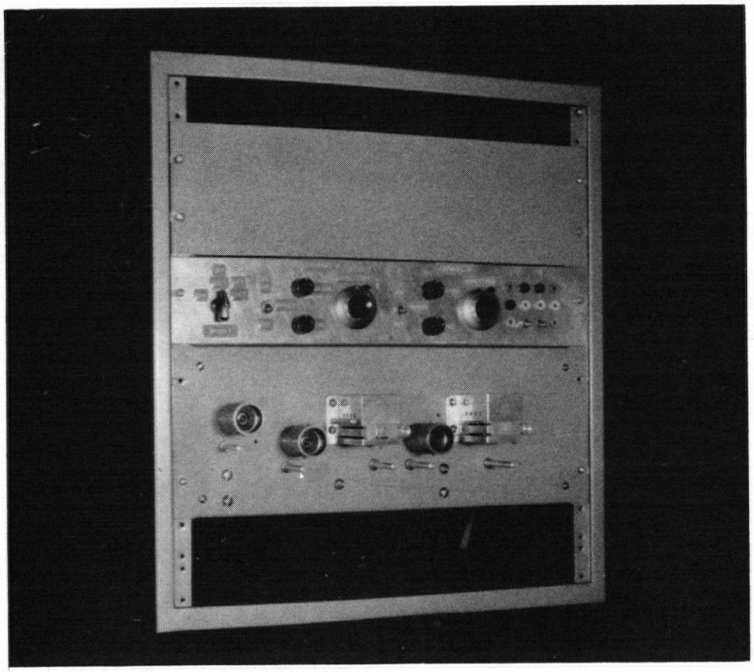


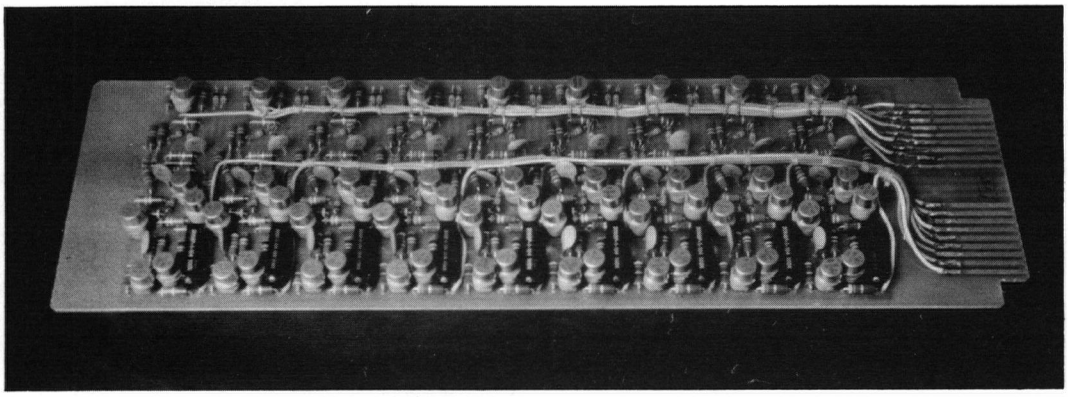
Fig. 26. Control Panel and Tape Drive

trol panel and supports all the switches and knobs used during the operation of the device. The top part covered by an empty panel houses the electronic parts on printed circuit cards. Removal of the empty panel allows the cards to be pulled out

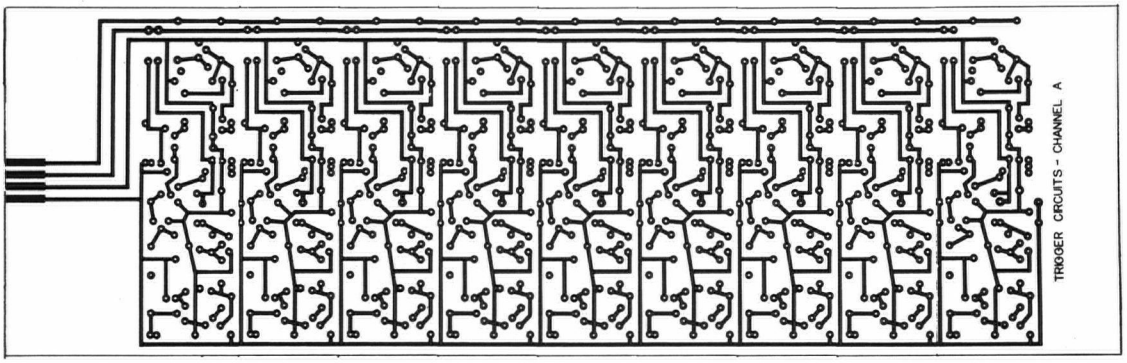
towards the front for easy servicing. Extension cards were specially made in order to keep the cards "in the circuit" while they are in the pulled-out position.

One of the $4\frac{1}{2}$ by $14\frac{1}{2}$ inch cards accommodating nine shaping and trigger circuits is shown in Fig. 27a, and the corresponding sketch for the wiring layout is displayed in Fig. 27b. A total of nine cards were needed to mount the circuitry including power supplies and output amplifiers. Two high-power transistors ($\pm$ 6 volt power supply) and two Zener diodes ($\pm$ 40 volt nominal, $\pm$ 25 volt power supply) are located on heat sinks at the rear of the lower part. The total power dissipated by these components averages approximately 28 watts with a possible maximum of 36 watts.

The preparation of the field coils for the magnetic reed switches was a sizeable project itself. According to the manufacturer's specifications the reed switches have a nominal pull-in sensitivity of 40 ampere-turns (AT) and are able to close and open 500 times a second. A 1500-turn field coil excited by a current of 40 ma provides the required pull-in force, with adequate over-drive to account for variations in pull-in sensitivity of the switches. The relatively low number of turns is chosen to avoid excessive delay in switching due to coil inductance. The diameter of the bobbin (Fig. 28) is also minimized to keep the coil inductance at a low value. The switch and coil terminals are brought out to the heavy wires fixed in the bobbin (see Fig. 28) which after plastic encapsulation serve as sturdy supports for mounting on the printed circuit cards.



a) Typical Printed Circuit Card



b) Wiring Layout for the Card in a) above

Fig. 27.

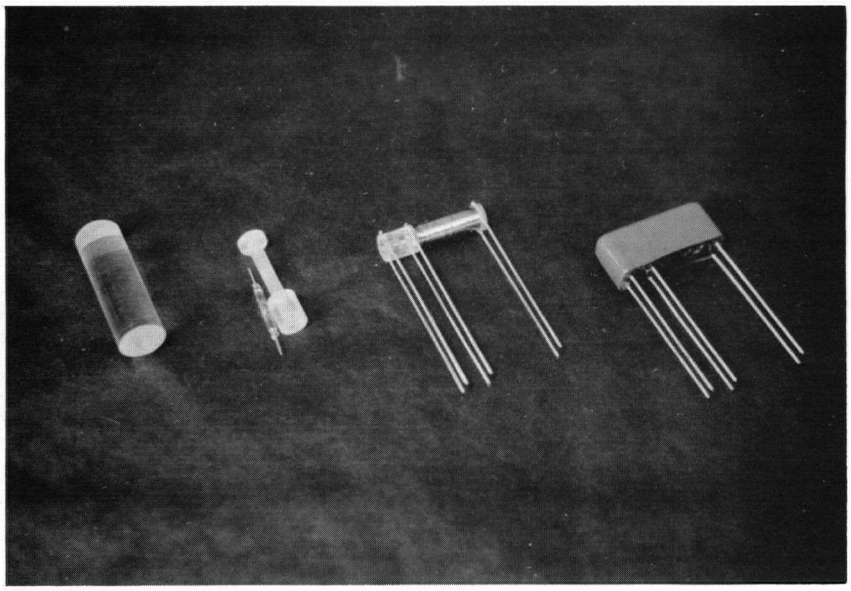


Fig. 28. Construction Phases of the Magnetic Reed Switching Unit

Measurements made after the encapsulation revealed that some of the switches changed their pull-in sensitivities during encapsulation. The changes were very likely caused by stresses due to shrinkage of the plastic. Those switches that demonstrated pull-in sensitivities much different ($\pm$ 5%) from the nominal value were discarded.