EVAPORATED SILICON THIN-FILM TRANSISTORS

by

CLEMENT ANDRE TEWFIK SALAMA

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Research Supervisor

Members of Committee

.....

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THE UNIVERSITY OF BRITISH COLUMBIA

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Department of Electrical Engineering

The University of British Columbia
Vancouver 8, Canada

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C. ANDRE T. SALAMA

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IN ROOM 228, HECTOR MacLEOD BUILDING

COMMITTEE IN CHARGE

Chairman: H. D. Fisher

J. Bichard

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E. Teghtsoonian

F. K. Bowers

L. Young

External Examiner: R. R. Haering

Department of Physics

Simon Fraser University

Burnaby

Research Supervisor: L. Young

EVAPORATED SILICON THIN-FILM TRANSISTORS

ABSTRACT

The method of fabrication, the theory and the properties of evaporated silicon thin-film transistors are discussed. The device consists of a p-type silicon film (0.5 to 2 μ thick) on a sapphire substrate, with aluminum source-drain electrodes evaporated onto the silicon and followed by a silicon oxide, SiO_x , insulating layer and an aluminum gate. The device operates by field-effect conductivity modulation of an n-type inversion layer at the surface of the p-type film.

The silicon films were evaporated by electron beam heating in a typical vacuum of 7×10^{-7} mm Hg at a rate of 200-600 $\text{\AA}/\text{min}$. The films exhibited single crystal diffraction patterns when deposited at a substrate temperature in the range 1050°C to 1100°C . They were found to be high resistivity ($> 400 \Omega\text{-cm}$) p-type and the hole mobility was of the order $20\text{-}30 \text{ cm}^2/\text{volt-sec}$. The minority carrier lifetime was $1\text{-}2 \mu\text{sec}$ and the optical absorption edge of the films was found to be broader than the absorption edge of single crystal silicon at all substrate temperatures. The low carrier mobility and minority carrier lifetime as well as the broadening of the optical absorption edge are attributed to the presence of a large number of crystallographic defects in the films.

The effective surface state density at the Si/evaporated SiO_x interface was estimated by the MOS technique and was found to be of the same order of magnitude ($3 - 4 \times 10^{11} \text{ cm}^{-2}$) as that at the Si/thermally grown SiO_2 interface. The silicon surface potential in the MOS structure was found to be particularly susceptible to

water vapour and contamination by sodium.

The silicon thin-film transistors fabricated have typical effective mobilities of $5\text{-}10\text{ cm}^2/\text{volt-sec}$ with transconductances as high as $100\text{ }\mu\text{mho}$ and gain bandwidth products up to 1 MHz . Surface trapping was found to affect the behavior of the devices at low gate voltages. The characterization of the traps by a method which involves measurements of the source-drain conductance, its temperature dependence and its transient response is discussed. The effect of surface scattering on the mobility at high gate voltages is also considered. The device characteristics were stable in vacuum but drifted when exposed to the atmosphere.

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Solid State Physics I*	E. L. Hahn
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* University of California, Berkeley

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3. M.P. Beddoes, C.A.T. Salama, "Series connected tunnel diode multilevel register," I.E.E.E. Trans. on Elect. Comp., Vol. EC-13, p. 308, 1964.
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The silicon thin-film transistors fabricated have typical effective mobilities of 5-10 $\text{cm}^2/\text{volt-sec}$ with transconductances as high as 100 μmho and gain-bandwidth products up to 1 MHz. Surface trapping was found to affect the behavior of the devices at low gate voltages. The characterization of the traps by a method which involves measurements of the source-drain conductance, its temperature dependence and its transient response is discussed. The effect of surface scattering on the mobility at high gate voltages is also considered. The device characteristics were stable in vacuum but drifted when exposed to the atmosphere.

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LIST OF SYMBOLS

C_g	= the total oxide capacitance over the channel area
C_o	= the oxide capacitance per unit area
C_s	= the silicon space charge capacitance per unit area
C	= the total capacitance per unit area of the MOS structure
d	= the thickness of the silicon film
E_c	= the energy level of the conduction band edge
E_v	= the energy level of the valence band edge
E_F	= the equilibrium Fermi level
E_i	= the intrinsic energy level
E	= the ionization energy of the traps
F_s	= the surface electric field normal to the channel
F_x	= the longitudinal electric field along the channel
f_{to}	= the initial occupancy of the traps at zero gate voltage
g_d	= the source-drain conductance
g_{do}	= the source-drain conductance at zero source-drain voltage
g_{ds}	= the source-drain conductance in the saturation region
g_m	= the transconductance
g_{ms}	= the transconductance in the saturation region
h	= the effective thickness of the inversion layer
I_D	= the dc source-drain current
I_{DS}	= the dc source-drain current in the saturation region
L	= the length of the channel
q	= magnitude of the electronic charge
N_A	= the acceptor impurity concentration
N_c	= the effective volume density of free carriers in the conduction band

N_t = the density of surface traps per unit area
 n = the total electron density per unit area
 n'_c = the volume density of conduction electrons in the inversion layer
 n_c = the surface density of conduction electrons in the inversion layer
 n_{co} = the equilibrium surface density of conduction electrons at zero gate voltage
 $n_s(x)$ = the electron density per unit area in the channel at a distance x from the source
 n_t = the surface density of trapped carriers
 n'_l = the volume density of carriers present in the semiconductor when the Fermi level is at the trap level
 n_l = the effective surface density of carriers present in the semiconductor when the Fermi level is at the trap level
 Q_s = the silicon space charge density per unit area
 Q_{ss} = the surface state charge density per unit area
 Q_T = the total charge per unit area initially present in the source drain region at zero gate voltage
 r = the surface reflectivity
 $\mathcal{R}_t$ = the rate at which electrons are trapped per unit area
 $\mathcal{R}_e$ = the rate at which electrons are emitted from the traps per unit area
 S = the cross sectional area of the traps
 T = the temperature in $^{\circ} K$
 t_{ox} = the thickness of the oxide
 t = the optical transmission through the specimen
 V_c = qn_c/C_o
 V_D = the dc source-drain voltage
 V_{DS} = the dc source-drain voltage in the saturation region
 V_G = the dc gate to source voltage

V_T	= the threshold gate voltage to turn-on or -off a channel
V_t	= qN_t/C_o
V_l	= qn_l/C_o
v	= the thermal velocity of the carriers
W	= the width of the channel
x	= the distance measured parallel to the oxide-semiconductor interface
y	= the distance measured perpendicular to the oxide-semiconductor interface
α	= the optical absorption coefficient of the film
ϵ_{ox}	= the permittivity of the oxide
ϵ_{Si}	= the permittivity of the silicon
ϕ_s	= the silicon surface potential
ϕ_{MS}	= the metal-semiconductor work function
ρ	= the resistivity of the film
σ_n	= the conductivity of the channel
τ_e	= the electron emission time constant from the traps
η_l	= the index of refraction of the film
μ_n	= the effective electron mobility in the channel

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EVAPORATED SILICON THIN-FILM TRANSISTORS

1. INTRODUCTION

1.1 Integrated Circuits

Integrated circuits require the combination of passive and active electronic devices on a single substrate. Active devices offer the best performance when fabricated on a semiconductor single crystal substrate while the best passive elements are fabricated on an insulating substrate.⁽¹⁾ Their combination in integrated circuits has so far meant compromising the performance of each.

In monolithic silicon integrated circuits, the circuit elements have to be electrically isolated from each other. The reverse biased p-n junction is the most common method of isolation.⁽¹⁾ It is inadequate at high frequencies where the coupling capacitances become important and it tends to suffer from dc effects such as junction leakage, inversion layers and unwanted transistor and p-n-p-n effects.

Several methods have been proposed to alleviate the limitations inherent in p-n junction isolation in monolithic integrated circuits. One method is the so called "insulated isolation"⁽²⁾ where an insulating layer of silicon dioxide or high resistivity polycrystalline silicon separates the components from each other and from the silicon substrate. This technique involves a large number of processing steps and is still at the experimental stage. Good electrical isolation can also be achieved by assembling discrete silicon transistor chips and

thin film passive components mounted on insulating substrates. The disadvantage of this method is the high assembly cost associated with the handling of many separate chips and the making of a large number of interconnections. An alternative approach which offers ideal isolation and simplified fabrication procedure consists of depositing all components active and passive upon an insulating substrate in the form of thin films ($< 10 \mu$ thick). The rate of development of this approach has been limited by the properties of the available thin-film active devices on insulating substrates.

1.2 Types of Thin-Film Active Devices on Insulating Substrates

Four types of thin-film active devices have been proposed. The first type is a conventional bipolar transistor fabricated using a technology compatible with thin film techniques. Rasmanis⁽³⁾ attained some success by crystallizing silicon layers evaporated on molten glass substrates and fabricating diffused junction transistors within these layers as shown in Figure 1-1(a). The characteristics of these transistors were adversely affected by the presence in the films of crystallographic defects which acted as additional recombination centers in the base, thus decreasing the current gain.

The second type of device is based on the transport of hot-carriers in thin metal films.⁽⁴⁾ The operation of the two hot-carrier triodes, illustrated in Figure 1-1(b) and 1-1(c), is similar to that of a conventional bipolar transistor except that the base is a metallic film which is thin enough to transmit

(a) CONVENTIONAL BIPOLAR JUNCTION TRANSISTOR

(b) TUNNEL-EMITTER TRIODE

(c) SEMICONDUCTOR
METAL-EMITTER TRIODE

(d) "ANALOG" TRIODE

(e) SPACE CHARGE-LIMITED
TRIODE

Figure 1-1 Thin-Film Triodes Deposited on Insulating Substrates

hot-electrons from the emitter to the collector. These two triodes differ however in the structure of the emitter and the mechanism of hot-carrier injection into the metal base. In the tunnel-emitter triode (Figure 1-1(b)), the carriers are injected into the base by tunneling through the insulator separating the emitter from the base. In the semiconductor-metal emitter triode (Figure 1-1(c)), the carriers are injected into the base by Schottky emission from the semiconductor. These triodes are still at an early experimental stage due to the difficulty encountered in growing thin enough metal films free from pinholes.

The third type of device involves the flow of space-charge-limited currents⁽⁵⁾ in a wide band gap semi-insulating material and is illustrated in Figures 1-1(d) and 1-1(e). This approach has received considerable theoretical attention and has yielded experimental thin-film devices having useful characteristics.⁽⁶⁾

The operation of the fourth type of device is based on the modulation of the conductivity of a semiconductor film by field effect. Since all of the devices mentioned are still being actively investigated, no attempt will be made here to evaluate their ultimate merits. The ensuing work will be concerned with a thin-film version of the insulated-gate field-effect transistor.

1.3 Thin-Film Field-Effect Transistors

The first attempts to realize active solid-state devices operating on the field-effect principle appear to have

been undertaken by Lilienfeld⁽⁷⁾ in 1933, and independently by Heil⁽⁸⁾ in 1935. The most relevant early reference of the device is a note by Shockley and Pearson⁽⁹⁾ on conductivity modulation which appeared in 1948, and in which the conductivity of a thin germanium film was modulated by an electric field perpendicular to the film surface. Considerably smaller conductivity modulation than expected was found, and this discrepancy was interpreted as due to a high concentration of charge trapped in states⁽¹⁰⁾ at the semiconductor surface. The role of surface states in limiting the observed modulation was so convincingly demonstrated that for many years this much-quoted experiment served as warning against any attempt to use the insulated gate structure in a practical transistor. The field effect however became a most useful tool in the study of the electronic properties of semiconductor surfaces. An alternative approach to an active solid-state field-effect device was conceived by Shockley⁽¹¹⁾ who circumvented the problem of surface states by using a reverse biased p-n junction as the field-effect electrode. This transistor was realized by Dacey and Ross⁽¹²⁾ in 1953 and became available commercially in 1959.

The obstacles which delayed the progress towards a practical surface-controlled field-effect transistor were the lack of stability of the surface and the high density of surface states (of the order of $10^{15}/\text{cm}^2$). In 1959, the success of Atalla⁽¹³⁾ and his co-workers in passivating silicon surfaces by means of thermally-grown oxide and reducing the density of states at the silicon/silicon dioxide interface to $10^{11}/\text{cm}^2$, revived the interest in the insulated-gate transistor, and led

to the realization of the first surface field-effect transistor on bulk silicon by Atalla and Kahng^{(14),(15)} in 1960. Since then considerable work has been carried out on this type of transistor and as a result these transistors have been commercially available for the past two years and are commonly known as the metal/oxide/semiconductor (MOS) transistors.

In 1961, the first insulated-gate thin-film transistor (TFT) deposited by evaporation techniques on an insulating substrate was reported by Weimer^{(16),(17)} who used cadmium sulfide thin films as the semiconducting material. Cadmium selenide,⁽¹⁸⁾ tellurium⁽¹⁹⁾ and lead sulfide⁽²⁰⁾ have also been used successfully. The coplanar electrode structure for these devices is shown in Figure 1-2(a). Another version of the insulated-gate field-effect transistor formed in the surface of pyrolytically deposited single crystal films of silicon has been reported^{(21),(22)}. This device, shown in Figure 1-2(b), is fabricated by standard diffusion and photoetching techniques and is identical in structure to the MOS transistor.

The devices described in this thesis are silicon insulated-gate field-effect TFTs⁽²³⁾ fabricated by evaporation on sapphire substrates. These devices are similar in structure to Weimer's TFTs and possess the common advantage of being fabricated by the same techniques used in the production of passive thin film circuits.

Silicon was chosen as the semiconductor film to investigate:

- (1) the possibility of achieving high mobility in the films and therefore high gain in the transistors,

(a) WEIMER'S TFT

(b) MOS TRANSISTOR

Figure 1-2 Two Forms of the Insulated-Gate Field-Effect Transistor on Insulating Substrates

Figure 1-3 Silicon Thin-Film Field-Effect Transistor

- (2) the possibility of developing a method of preparation and integration of good active and passive components on insulating substrates while at the same time utilizing the large amount of technology available for silicon.

This thesis deals with the structure, the operation, the theory and the factors affecting the performance of the silicon TFTs.

1.4 Silicon Thin-Film Transistor: Structure and Operation

The basic device structure is shown in Figure 1-3. The device consists of a thin film of p-type silicon deposited on a sapphire substrate. Aluminum source-drain electrodes are evaporated onto the silicon followed by a silicon oxide insulating layer and an aluminum gate. The structure and the mechanism involved in the operation of the silicon TFT and Weimer's TFT are very similar. Both devices operate by modulation of the conductivity of a surface channel by field effect. The source-drain electrodes must make ohmic contacts to that surface channel. However, in the present silicon TFT the conducting channel is an n-type inversion layer at the surface of the p-type film. The contacts must therefore be minority carrier (electron) injecting contacts with respect to the film. In the case of Weimer's TFT the conducting channel is an accumulation layer of the same conductivity type (n-type for CdS) as the film and the contacts are ohmic with respect to the film.

The TFTs are high input impedance devices having

saturated pentode-like characteristics typical of a field-effect transistor. The insulated gate can be biased either positively or negatively with respect to the source without drawing current and two modes of operation are therefore possible.

- (a) Enhancement mode in which the drain current is substantially zero and increases by many orders of magnitude as the gate voltage is raised from zero to several volts positive with respect to the source.
- (b) Depletion mode in which useful drain current flows at zero gate bias, in this case a negative voltage is required to pinch-off the source-drain current.

1.5 Elementary Physical Theory of the Insulated-Gate Field-Effect Transistor

The purpose of this section is to give a brief review of the elementary theory⁽²⁴⁻²⁸⁾ of the insulated-gate field-effect transistor pointing out the simplifying assumptions which have come into common use in analyzing the characteristics of these devices. The simple physical model used in the analysis is based on the following assumptions.

- (1) The mobility of the carriers is assumed to be constant independent of the gate or source-drain field.
- (2) The gradual channel approximation is assumed to hold. In this approximation the rate of change

of the field along the channel is very small compared to the rate of change of the gate field normal to the channel. This approximation permits the solution of Poisson's equation in one dimension leading to a channel conductivity which is a function of the applied gate field.

- (3) The effective channel depth is very small compared to the thickness of the oxide so that most of the potential drop between the gate and channel appears across the oxide.
- (4) The trapping effects are neglected.
- (5) The metal-semiconductor work function difference is neglected.
- (6) The gate capacitance is assumed to be independent of gate voltage.

The device structure and the coordinate axes used in the analysis are shown in Figure 1-4. The source-drain electrodes make ohmic contacts to the inversion layer which is present at zero gate voltage. The potentials applied to the gate and drain electrodes are V_G and V_D respectively. The potential of the semiconductor at any point x from the source electrode is given by $V(x)$.

The source-drain current I_D is given by:

$$I_D = \sigma_n F_x ,$$

$$= q\mu_n W n_s(x) F_x = q\mu_n W n_s(x) \frac{dV(x)}{dx} , \quad (1-1)$$

(a) CROSS-SECTIONAL VIEW

(b) ELECTRODE STRUCTURE

Figure 1-4 The Idealized Geometry of the Silicon TFT

where σ_n is the channel conductivity,

F_x is the electric field strength between source and drain

q is the magnitude of the electronic charge,

μ_n is the effective electron mobility in the channel,

W is the width of the channel,

and $n_s(x)$ is the electron concentration per unit area in the channel at a distance x from the source.

The relation between the surface charge density $qn_s(x)$ and the total applied gate voltage is given by:

$$qn_s(x) = C_o [V_G - V(x)] + Q_T \quad (1-2)$$

where: C_o is the capacitance per unit area of the gate oxide layer capacitor is given by $C_o = \epsilon_{ox}/t_{ox}$,

ϵ_{ox} is the permittivity of the oxide and t_{ox} is the thickness of the oxide layer,

and Q_T is the total charge per unit area present at zero gate voltage in the source-drain region.

Substituting for $qn_s(x)$ in equation (1-1) and integrating between $x = 0$ and $x = L$ we get:

$$\int_0^L I_D dx = \int_0^{V_D} q\mu_n W n_s(x) dV(x),$$

$$= \int_0^{V_D} \mu_n W [C_o(V_G - V(x)) + Q_T] dV(x), \quad (1-3)$$

$$I_D = \frac{\mu_n C_o W}{L} \left[\left(V_G + \frac{Q_T}{C_o} \right) V_D - \frac{V_D^2}{2} \right], \quad (1-4)$$

$$I_D = \frac{\mu_n C_g}{L^2} \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right], \quad (1-5)$$

where $C_g = C_o WL$ is the oxide capacitance over the channel area,

and $V_T = -Q_T/C_o$ is the threshold voltage required for the onset of drain current. V_T is positive for enhancement mode operation and negative for depletion mode.

In the fabrication of TFTs one should be able to control the threshold voltage V_T to within a specified range. This voltage is determined to a large extent by the surface state charge density and the bulk charge density. Usually the surface states contribution dominates over the bulk charge. (27)

The drain characteristics given by equation (1-5) are valid only for gradual channels, i.e. up to the knee of the I_D vs V_D characteristic. The resulting characteristics are shown by the heavy lines in Figure 1-5. As the drain voltage V_D is increased beyond the knee and the gate voltage is kept constant at some value greater than V_T the channel is pinched off near the drain. The pinch-off condition at which the gradual channel approximation fails and equation (1-5) ceases to be valid corresponds approximately to the condition of maximum drain current and may be obtained by setting

$$\left(\frac{\delta I_D}{\delta V_D} \right)_{V_G} = 0 \text{ from which we get:}$$

Figure 1-5 The Theoretical Drain Characteristics of an n-Channel Thin Film Transistor

$$V_D = V_{DS} = (V_G - V_T). \quad (1-6)$$

The drain current at pinch-off is given by:

$$I_{DS} = \frac{\mu_n C_g}{2L^2} (V_G - V_T)^2 = \frac{\mu_n C_g}{2L^2} V_{DS}^2. \quad (1-7)$$

If the drain voltage is further increased beyond the pinch-off voltage given by equation (1-6), the pinch-off region lengthens into the channel from the drain as illustrated in Figure 1-6 which shows the potential rise along the channel from source to drain for $V_D > (V_G - V_T)$. In region I, near the source, where the channel potential is less than the gate potential, an inversion layer is present. In region II the inversion layer is progressively pinched-off. In region III, near the drain, where the channel potential exceeds $(V_G - V_T)$ the channel is completely pinched-off but current flow is maintained by the high field and the injection of minority carriers into this space from region II. Current flow in regions I and II is ohmic while in region III it is space charge or emission limited. (28)

Most of the additional drain voltage in excess of $(V_G - V_T)$, appears across the length of the pinched-off region and results in very little increase in drain current. An increase in the drain current does occur as predicted from equation (1-7) since the length of the channel is now effectively shorter. An accurate calculation of the length of the pinched-off region is not possible in the gradual channel approximation. In the elementary theory, the drain current in the region $V_D \geq V_{DS}$ is taken as the value given by equation (1-7) and is assumed to be independent of V_D . This is illustrated in Figure 1-5.

Figure 1-6 Cross-Sectional Model of the Transistor Under Saturation Conditions

Several alternative physical mechanisms have been proposed to account for the saturation characteristics. In his surface-channel dielectric triode Wright⁽²⁹⁾ has distinguished a source region where a gradual approximation is legitimate, and a drain region through which a space-charge-limited current flows with a longitudinally directed field. Some arbitrariness was involved, however, in the matching of the solutions for the $V-I$ characteristics in the transition region between the source and drain regions. In the case of silicon insulated-gate field-effect transistors fabricated on high resistivity substrates Hofstein and Heiman⁽²⁵⁾ have related the large but finite output resistance beyond pinch-off to excess charge carriers induced in the channel by the drain electrode at the substrate side of the semiconductor. The output resistance, calculated by these authors, and valid in the saturation region gives rise to a voltage amplification of the same order of magnitude as that measured on experimental transistors. Reddi et al⁽³⁰⁾ and Hofstein et al⁽³¹⁾ have attributed the dependence of the incremental saturation resistance on the drain and gate voltages in silicon MOS devices fabricated on low resistivity substrates to the modulation of the width of the pinched-off region in a similar manner to the modulation of the collector depletion region in a bipolar transistor (Early Effect). Jund⁽³²⁾ has suggested that the physical phenomenon responsible for saturation current in field-effect devices was not complete pinch-off of the channel but the fact that the carriers can reach a limit velocity at high longitudinal fields near the drain. A different explanation of the finite output resistance at saturation has

been put forward by Johnson.⁽³³⁾ This author assumes that the donors present in the semiconductor layer are initially only partially ionized. The saturation of the V-I characteristics would then correspond to the ionizing of the donors in the deeper lying levels. Complete saturation would occur when these donors are completely stripped of their electrons. More recently Guerst⁽³⁴⁾ has related the finite saturation resistance in the insulated-gate field-effect transistor to the geometric configuration of its electrodes and characterized the conditions prevailing in the entire channel by means of a single equation which serves as a non-linear boundary condition for the determination of the electric potential in the insulator region. In his analysis a division of the channel into a conducting part (source region) and a part with space-charge-limited current (drain region) can be made but is not essential for the evaluation of the V-I characteristics.

1.6 Equivalent Circuit of the Insulated-Gate Field-Effect Transistor

The commonly accepted⁽²⁷⁾ low-frequency small-signal intrinsic circuit model for an insulated-gate field-effect transistor is shown in Figure 1-7. The gate, drain and source electrodes are represented as the nodal points marked G, D and S. This intrinsic model does not include the stray capacitances or lead impedances. The impedances between gate and source, and gate and drain are represented by parallel R-C circuits. The values of C_{gs} , C_{gd} , R_{gs} and R_{gd} depend on the dc operating point

and on the frequency. (27, (28), (35)) The output circuit consists of the source-drain conductance g_d driven by a constant current generator $g_m v_g$. Drain-source capacitance is small and has been neglected.

Figure 1-7 Intrinsic Circuit Model for the Insulated-Gate Field-Effect Transistor.

Some of the important parameters of the circuit model can be obtained from equation (1-5). The output conductance below saturation is given by:

$$g_d = \left(\frac{\partial I_D}{\partial V_D} \right)_{V_G} = \frac{\mu_n C_g}{L^2} (V_G - V_T - V_D) = \mu_n C_o \frac{W}{L} (V_G - V_T - V_D), \quad (1-8(a))$$

$$\text{and } g_{do} = \left(\frac{\partial I_D}{\partial V_D} \right)_{V_D \rightarrow 0} = \frac{\mu_n C_g}{L^2} (V_G - V_T), \quad (1-8(b))$$

i.e., the output conductance is linear with V_G . The transconductance below saturation is:

$$g_m = \left(\frac{\delta I_D}{\delta V_G} \right)_{V_D} = \frac{\mu_n C_g V_D}{L^2} = \mu_n C_o \frac{W}{L} V_D, \quad (1-9)$$

and its maximum which occurs at saturation is given by:

$$g_{ms} = \mu_n C_o \frac{W}{L} V_{DS} = \mu_n C_o \frac{W}{L} (V_G - V_T). \quad (1-10)$$

The voltage amplification of the device is:

$$A_V = - \left(\frac{\delta V_D}{\delta V_G} \right)_{I_D} = \frac{V_D}{V_G - V_T - V_D}, \quad (1-11)$$

which is identical to the ratio g_m/g_d . At the point of saturation $V_D = V_{DS} = (V_G - V_T)$, the voltage amplification factor diverges due to $g_d = 0$. In actual devices, due to the channel length shortening-effect beyond the saturation point, the drain conductance is finite in the saturation region and hence the voltage amplification factor is also finite.

The gain-bandwidth product of the device is given by:

$$GBW = \frac{g_m}{2 \pi C_g} = \frac{\mu_n V_D}{2 \pi L^2} \quad \text{below saturation,} \quad (1-12)$$

$$\text{and } GBW = \frac{\mu_n (V_G - V_T)}{2 \pi L^2} \quad \text{at saturation.} \quad (1-13)$$

1.7 Circuit Applications of the TFT

The TFT has a wide range of applications. In many respects it recalls the vacuum tube but with the advantage that its cut-off or threshold voltage can be positive or negative and

the gate does not conduct when it is forward biased. The TFT is unique in that it is made by techniques which are compatible with those used in making thin-film passive components and can therefore be included in the fabrication schedules of these components. It is not envisaged that thin film transistors will be produced as single discrete components since they lose their advantages as soon as they are removed from the context of the thin film circuit.

The circuit applications of the TFT are similar to those of the MOS transistor which are listed below. An obvious application is that as an electrometer amplifier taking advantage of the extremely high input resistance.⁽³⁶⁾ The high on-off resistance ratio and zero dc leakage make these transistors particularly suitable in chopper and analog switching circuits.⁽³⁷⁾ The devices can also be used in high frequency small signal amplifiers where the circuit simplicity is the principle advantage.⁽³⁸⁾

Another application is in micropower integrated circuits which require an active device with a good gain at microamp⁽³⁹⁾ working currents and resistors which approach the megohm range as currents approach the microamp level. The silicon-on-sapphire approach discussed in the following chapters offers a reasonable solution to both of these problems. The TFT can provide fairly good amplification in the microamp range and with the thin silicon films used in this technology, sheet resistances as high as 10^7 ohm/square can easily be obtained making high value resistors possible in very small

sizes. The fact that this approach can give devices which are electrically isolated from each other (thus eliminating leakage currents) is even more significant in micropower circuits than at higher power levels.

These devices can also be useful in large digital arrays where slow speed functional blocks are required, although the general advantages here are not nearly so clear-cut when compared with equivalent, bipolar structures.⁽³⁶⁾ The devices will not, however, be useful in high speed switching circuits⁽³⁶⁾ or where ionizing radiation is an important environmental requirement.⁽³⁶⁾

1.8 Factors Influencing the Design and Performance of the TFT

For good performance, the TFT must have large transconductance and gain-bandwidth product, high input impedance, maximum source-drain breakdown voltage, low noise and high stability. The factors which affect the performance of the TFT are considered below, and are dealt with in more detail in the following chapters.

(1) The properties of the semiconductor film.

The surface mobility in the films must be high and the density of the carriers must not be too large to be effectively modulated by the gate voltage. The high carrier mobility implies single crystal films free from crystallographic defects. Dislocations, stacking faults and accelerated growth regions are the principle defects observed in grown semiconductor films.⁽⁴⁰⁾

These defects can decrease the mobility and minority carrier lifetime and introduce acceptor centers in the semiconductor.⁽⁴⁰⁾ They also reduce the breakdown fields and increase the noise level.

(2) The properties of the insulator.

The insulator must have a high dielectric constant, high breakdown strength, good frequency and temperature behavior and be impervious to the ambient atmosphere.

(3) The properties of the semiconductor/insulator interface.

The insulator must act as a passivating layer on the surface of the semiconductor. The surface state density at the semiconductor/insulator interface must be effectively controlled and is crucial in determining the ultimate usefulness of the device. The surface states determine to a large extent the value of the threshold voltage V_T , in fact too large a surface state density at the interface will so completely shield the space-charge region from the influence of the gate that no control action whatever is observed.⁽²⁸⁾

Surface states are customarily divided into two groups. The "fast" states, which are believed to be located at the semiconductor

surface and the "slow" states, located on the oxide which normally covers the surface of a semiconductor.⁽⁴¹⁾ Since this oxide, in germanium for example, is between 10 and 40 Å^o thick,⁽⁴¹⁾ transfer of charge between the slow states and the free carriers can take place producing long response times. In the case of a semiconductor surface covered by a thick ($> 200 \text{ Å}^o$) oxide layer, there is little charge transfer between the semiconductor and the slow states. The short-term response of the semiconductor/insulator interface will depend on the states at the interface as well as on traps in the oxide and in the semiconductor. However only those traps lying very close to the interface will truly affect the short-term response. The long-term response of the surface will be affected by the deep traps within the oxide as well as the ionic charge contribution on the surface of and in the bulk of the oxide.⁽⁴²⁾

2. PREPARATION AND PROPERTIES OF THIN FILMS OF SILICON

2.1 Introduction

There is considerable interest in growing single crystal epitaxial* silicon films because of their inherent advantages in the fabrication of both improved and new solid state devices. Ideally one would like to control layer thickness and resistivity and to produce layers free from crystallographic defects. The two most commonly used methods of growing epitaxial silicon films are:

(a) Chemical or pyrolytic methods

The chemical methods involve the hydrogen reduction of a suitable halide, for example, silicon tetrachloride⁽⁴³⁾ (SiCl_4) or the pyrolysis of silane⁽⁴⁴⁾ (SiH_4). Most of the early work was concentrated on the chemical deposition of silicon onto silicon substrates and led to the extensive use of epitaxial layers in transistor and integrated circuits fabrication. Recently it became apparent that single crystal silicon films could be grown on insulating single crystal substrates such as sapphire,⁽⁴⁵⁾ quartz,⁽⁴⁶⁾ calcium fluoride,⁽⁴⁷⁾ and magnesium oxide.⁽⁴⁷⁾ The deposition of silicon on

* The term epitaxy meaning "arrangement on" will be used to denote the growth of one material on another in such a way that the deposited material possesses a definite orientation with respect to the substrate.

insulating substrates by pyrolytic methods is presently under intensive investigation by various organizations.^{(48),(49)}

(b) Evaporation in high vacuum

The method of growing epitaxial silicon layers by vacuum evaporation has only received serious attention during the past three years, despite its versatility and its potential application to complicated geometries. It offers a number of advantages over the chemical methods:

- (1) cleanliness and absence of the halogens,
- (2) masking without interference with the process,
- (3) complete fabrication of devices in vacuum,
- (4) lower substrate temperatures for epitaxial growth.

A possible drawback of this method is the high content of crystallographic defects which are usually associated with evaporated films. Recent studies^{(50),(51)} have demonstrated however, that by suitable adjustment of vacuum conditions and evaporation rates it is possible to deposit defect-free silicon films on silicon substrates.

Vacuum evaporated epitaxial silicon layers deposited onto single crystal silicon substrates were first reported by Unvalla⁽⁵²⁾ and further investigated by Unvalla⁽⁵³⁾ and Hale.⁽⁵⁴⁾

They found that epitaxial growth occurs readily on silicon substrates of any orientation provided the substrate temperature is sufficiently "high". Both Hale and Unvalla give the epitaxial temperature as about 1120°C and Unvalla claims that this temperature increases with increasing rates of deposition being 1250°C at a rate of $4\ \mu/\text{min}$. In general, the electrical properties of the films are determined by the dopant present in the source material.⁽⁵⁴⁾ However a consistent tendency towards p-type conductivity in the films has been observed when the sources used are of relatively high resistivity ($> 10\ \Omega\text{-cm}$), independently of whether the source is p or n. The cause of the tendency is still subject to controversy.^{(50), (55)} Three possible explanations have been suggested. First, a p-type contaminant may be introduced into the layers during growth. Possible impurities are boron or aluminum from materials associated with the furnace and/or substrate heater. Second, the source material may be compensated, i.e. may contain both n and p type dopants and the measured resistivity corresponds to the amount of unbalanced dopant. Consequently, although n type material is used, owing to vapour pressure considerations more n-type dopant (antimony or phosphorus) is lost than p-type dopant (boron) during evaporation, and so the resulting layers are p-type. The third possibility is that the bias toward p-type material arises because of the presence of crystallographic defects which act as acceptor centers.

Relatively little work has been reported on the deposition of evaporated silicon on insulating substrates.

Epitaxial single crystal growth has been reported on calcium fluoride single crystal^{(55),(56)} and polycrystalline growth has been reported on sapphire⁽⁵⁷⁾ and quartz.^{(57),(58)}

2.2 Vacuum Evaporation of Silicon

The thermal evaporation of silicon in vacuum involves the heating of the silicon source material to a high temperature above 1600°C ⁽⁵⁵⁾, for reasonable rates of evaporation, and the heating of the substrate to a high temperature, between 900°C and 1200°C , to ensure good epitaxy.

For high quality and high purity films the following requirements must be satisfied.

- (1) The contamination of the films from the vacuum ambient must be reduced by evaporating in high vacuum or as an alternative to improving the vacuum the rate of deposition may be increased provided the crystal perfection of the growing film is not impaired. The most troublesome ambient contaminants are considered to be the residual hydrocarbons which decompose on the surface of hot silicon forming silicon carbide crystallites.
- (2) The contamination from the source crucible must be minimized.
- (3) The source and substrate heaters must provide localized heating to prevent outgassing of the areas surrounding the source and substrate.

Various methods can be used to evaporate silicon. Evaporation from refractory metal heaters causes considerable contamination of the silicon source due to the alloying of silicon with these metals at the very high temperatures which are commonly used.⁽⁵⁹⁾ Refractory oxide boats overcome this problem to some extent but lead to the presence of SiO in the films.⁽⁵⁹⁾ Evaporation of silicon from a boron nitride crucible in a carbon resistance heating filament produces films containing 0.5% boron.⁽⁶⁰⁾ Such contamination is considerably reduced by the use of electron bombardment heating⁽⁵²⁾ or RF heating⁽⁶¹⁾ of the silicon source.

The substrate can be heated by radiation from a filament made of tungsten and situated immediately behind the sample and enclosed in a refractory metal box. Unvalla⁽⁵³⁾ has shown that heavy tungsten contamination occurs from this type of substrate heater. RF heating can also be used. It is a clean and efficient process but requires elaborate water cooling inside the vacuum system. Another alternative, electron bombardment heating provides a method of concentrating power into a small, well defined area thus minimizing outgassing.

In this work electron beam heating of the source and substrate were used and the silicon source acted as its own crucible, i.e. the silicon was evaporated from a molten pool on the surface of the source. The electron beam method is very versatile and can be adapted to the evaporation of materials other than silicon, e.g. metals and insulators involved in the fabrication of thin film circuitry.

2.3 Choice of the Evaporation Parameters

The parameters affecting film properties may be listed in probable order of importance as follows:

- (1) the substrate,
- (2) the substrate temperature,
- (3) the evaporation rate,
- (4) the ambient purity,
- (5) the film thickness,
- and (6) the source doping.

It is apparent that, even if only a few of the parameters are allowed to vary, a large number of combinations are possible. In view of this fact, this investigation has been carried out by fixing some of the parameters and observing how film properties vary as a function of the remaining variables always keeping in mind the ultimate use of these films as active substrates for thin film devices.

2.3.1 Choice of the Substrate

Most theoretical considerations of the occurrence of silicon epitaxy on insulating substrates have been based on the concept of a certain geometrical fitting between the lattice of the overgrowth and that of the substrate.⁽⁴⁷⁾ These considerations imply the necessity of a crystalline substrate with lattice spacings and expansion coefficients similar to those of silicon.

It has been shown that a misfit in the lattice spacing can lead to dislocations, which in turn lead to strains

and possibly localized energy levels.⁽⁴⁷⁾ A comparison between the crystallography of potentially useful single crystal insulators and silicon suggests that calcium fluoride, quartz and sapphire would be the most suitable substrates for epitaxial silicon growth since at least one of the lattice constants is about the same as that of silicon. These materials are listed in Table 2-1 together with their crystallographic constants.

Figure 2-1 shows the temperature variation of the reported linear coefficient of thermal expansion β for these substrates and silicon. A large discrepancy between this coefficient for silicon and the substrate can cause poor film

Material	Crystal System ⁽⁶²⁾	Lattice constants ⁽⁶²⁾ $\overset{\circ}{\text{A}}$	
		a_0	c_0
Si	Cubic	5.41	--
CaF ₂	Cubic	5.46	--
SiO ₂ (Quartz)	Hexagonal	4.90	5.39
Al ₂ O ₃ (Sapphire)	Hexagonal	4.75	12.96

Table 2-1 Crystal Structure and Lattice Constants for Silicon and Some Single Crystal Substrates.

adherence. This has been reported to occur in the case of relatively thick films which flaked off a CaF₂ substrate.⁽⁴⁷⁾ Quartz was not considered usable, in spite of a good lattice match to silicon, because film fracture was reported to occur at the quartz phase transition temperature (573°C), when the films were cooled down from the high deposition temperature to room temperature.⁽⁴⁶⁾ Sapphire offers the closest match to

Figure 2-1 Linear Coefficient of Thermal Expansion for Silicon and Ceramic Substrates as a Function of Temperature

silicon as far as the thermal coefficient of expansion is concerned and offers the further advantages of high melting point (2040°C), low dielectric loss, high resistivity and mechanical strength, freedom from outgassing, no chemical interaction with the deposit, and good thermal conductivity. This last property is important in determining the allowed power dissipation in the thin film. From a practical point of view synthetic sapphire substrates are not much more expensive than single crystal silicon substrates presently used in integrated circuits and are furthermore reusable.

The substrates used in this investigation were single crystal 60° orientation sapphire, $\frac{1}{4}$ inch in diameter, 0.080 inch thick, optically polished on one side*.

2.3.2 The substrate temperature and the evaporation rate

The proper combination of substrate temperature and rate of evaporation determines to a large extent the crystalline perfection of the deposited layers. Substrate temperatures between 880°C and 1220°C and a range of evaporation rates between $200 \frac{\text{\AA}}{\text{min}}$ and $600 \frac{\text{\AA}}{\text{min}}$ were used. The characteristics of the films were found to be relatively independent of the evaporation rate in this range.

2.3.3 The ambient and source purity

The ambient and source purity were discussed in section 2.2 and were the determining factors in the choice of

* Adolf Meller and Company, Providence, Rhode Island.

electron bombardment in the heating of the source and the substrate.

2.3.4 The film thickness

Above a certain minimum thickness ($> 500 \text{ \AA}$), size effects become negligible. Most of this investigation was concerned with films 0.5 to 2 μ thick.

2.3.5 The source doping

Hyper-pure polycrystalline silicon rods* 1 inch in diameter were used as the source material. The resistivity of these rods was larger than 200 Ω -cm with the following impurity concentrations:

Maximum boron content $1.5 \times 10^{13} \text{ atoms cm}^{-3}$

Maximum donor impurity content $10 \times 10^{13} \text{ atoms cm}^{-3}$

The oxygen content was less than $1 \times 10^{17} \text{ atoms cm}^{-3}$.

The choice of a lightly doped source material was not arbitrary and was made bearing in mind the requirement for films of high enough resistivity which would allow effective field-effect modulation in the thin film transistors.

2.4 Apparatus

2.4.1 The vacuum system and the evaporation assembly

The system used in the evaporation of silicon films is shown in Figure 2-2. The vacuum system consists of a 10" NRC oil diffusion pump provided with a liquid nitrogen cooled

* Dow Corning Corporation, Hemlock, Michigan.

Figure 2-2 The Silicon Evaporation System

trap. The evaporation assembly is shown schematically in Figure 2-3. It consists of a water cooled stainless steel shell provided with a pyrex viewing port and fitted with two electron guns, a substrate changer disc and shutter, a source holder, a crystal thickness monitor and an auxiliary liquid nitrogen trap.

The electron guns* are provided with magnetic focusing and x-y deflection and are rated at 30 kV -400 mA (maximum). One of the guns is used to heat the silicon source material and the other to heat the substrate. The substrate heater gun is modified to include oscillators connected in series with each of the x and y deflection coils to sweep the beam in a circular or elliptical pattern on the back of the substrate. The frequency and amplitude of the oscillators signals are adjusted to provide uniform heating of the substrate.

The stainless steel substrate changer disc, which can accommodate six substrate holders, and the stainless steel shutter are inclined at 30° to the horizontal. The substrate changer disc can be driven manually from outside the shell by a gear system with a double O-ring seal. The space between the O-rings is evacuated by a rotary pump.

The substrate holders, shown in Figure 2-4, are stainless steel rings which are inserted in the substrate changer disc. The sapphire substrates are held by means of tantalum clips spot-welded to the ring. The rings act as heat baffles, and the tantalum being a poor heat conductor ensures a uniform

* Brad-Thomson Industries, Indio, California.

Figure 2-3 The Evaporation Assembly

heat distribution over the substrate. In operating position, the substrate to source distance is 10 cm.

The arrangement for holding the silicon block used as the evaporation source is shown in Figure 2-5. The silicon block fits into a water cooled movable copper pedestal. During evaporation, the thermal expansion of the silicon causes it to be in good thermal contact with the tapered rim of the copper pedestal thus improving the effective cooling. The source cooling restricts the molten zone to a small area at the center of the block and thus prevents any contamination from the source holder. For fast evaporation rates, the molten zone tends to spread, and unless the rate of cooling is sufficient, spills over the sides onto the copper pedestal. Figure 2-6 shows the substrate changer and source holder inside the shell.

A quartz crystal oscillator is used to monitor the film thickness during evaporation.^{(66),(67)} The crystal monitor is mounted inside the vacuum system, symmetrically opposite the substrate, on a water cooled copper block. To prevent charge build up on the crystal during evaporation, a low resistance leakage path is provided from the crystal to ground.⁽⁶⁶⁾

An auxiliary liquid nitrogen trap is also fitted inside the system to improve the vacuum during evaporation. The trap consists of a tightly wound copper tube through which the liquid nitrogen is circulated. The external connections of the tube to the nitrogen supply are made through thin stainless steel feedthrough built into the flange supporting the quartz crystal monitor as shown in Figure 2-3.

Figure 2-4 The Substrate Holder

Figure 2-5 The Source Holder

Figure 2-6 The Substrate Changer and the Source Holder

2.4.2 Performance of the system

Under the high vacuum conditions ($<10^{-6}$ mm Hg) encountered in the system, manual control of the power input and therefore the evaporation rate was quite feasible. The source heater beam could be focussed into a spot less than 0.5 cm in diameter and the molten zone at that spot was estimated to be at 1600-1700°C. The power output from the source gun was 800 watts at 18 kV for an evaporation rate of 300 $\text{\AA}^{\circ}/\text{min}$ and the power output from the substrate gun was 75 watts at 5 kV for a substrate temperature of 1100°C.

2.5 Experimental Procedure

2.5.1 Substrate preparation

The substrates were degreased in trichlorethylene, etched in hot phosphoric acid, ultrasonically cleaned in distilled water and finally air dried. During the electron bombardment, the substrates became electrically charged and repelled any further electrons thus preventing good heating. This problem was overcome by precoating the back of the substrates with an electrically conducting film of sputtered platinum or tantalum and platinum thus providing a leakage path from the substrate through the tantalum clips to ground.

2.5.2 The experimental run

The system was evacuated with the source and substrates in position. When the pressure reached 10^{-6} mm Hg. a short outgassing of the source and substrate was carried out. The

system was then left pumping overnight. The typical pressure after such a pump-down was $2 - 4 \times 10^{-7}$ mm Hg which dropped to $3 - 4 \times 10^{-8}$ mm Hg when both traps were filled with liquid nitrogen. During the actual run the substrate heater was first turned on and sufficient time was allowed for the substrate temperature to become uniform before turning the source gun on. The evaporation was carried out in a typical pressure of 7×10^{-7} mm Hg. After deposition, the film was annealed for five minutes at the deposition temperature and then gradually brought down to room temperature. The pressure performance of the system as recorded during a typical run is shown in Figure 2-7.

2.5.3 The substrate temperature

The substrate temperature was measured previous to the silicon deposition by means of an optical pyrometer.* The temperature was assumed to remain constant during deposition, this assumption is valid provided the silicon layer is much thinner than the sapphire substrate. Since the emissivity of sapphire in the temperature range of interest could not be found, the pyrometer was calibrated using a chromel-alumel thermocouple which was in good thermal contact with the platinum film on the back of the substrate. The cold thermocouple junction was kept inside the vacuum system at 18°C by having it in good thermal contact with the water cooled copper block used to hold the quartz crystal (see Figure 2-3).

* Pyropto, Hartmann and Braun, Frankfurt/Main, Germany.

Figure 2-7 The Pressure Performance of the System during a Typical Run

2.6 Determination of the Thickness of Silicon Thin Films

The thickness of the silicon films was determined by an infrared interference method.⁽⁶⁸⁾ The primary requirement for the production of interference fringes by reflection from a film is that the optical constants of the film differ from those of the substrate material. Since this requirement is satisfied in the case of silicon films deposited on sapphire substrates, the infrared interference method commonly used in measuring the thickness of epitaxial silicon films deposited on silicon substrates was adapted to the measurement of the thickness of the evaporated silicon films. This method has the advantage of being accurate, quick, non-destructive, and well adapted for routine measurements.

The thickness of the film d can be expressed in terms of the fringe order m , the wavelength of the fringe maxima λ_m , the refractive index of the film η_1 and the angle of refraction ϕ' :

$$d = \frac{(m + \frac{1}{2}) \lambda_m}{2 \eta_1 \cos \phi'} \quad (2-1)$$

The above equation includes a phase change of π at the air-film interface but no phase change at the film-substrate interface. The lower limit of silicon film thickness, that can be measured by observing fringes, depends on the wavelength of the radiation used to measure it and on the absorption of the silicon films.

The relationship between film thickness and the optical wavelengths of interference fringe maxima given by equation (2-1) is plotted in Figure 2-8 for the case of normal

Figure 2-8 Chart for Determining the Thickness of Silicon Films by Near Infrared Interference

incidence, and results in a family of straight lines of constant fringe order. This chart is useful for rapid and accurate data reduction without calculation. Once the fringe maxima are determined for a specific film, a horizontal line $d = \text{constant}$, can be found to intersect the fringe order lines at wavelength values corresponding to the fringe maxima for that thickness. The accuracy of this method is of the order of $\pm 5\%$.

A Cary spectrophotometer was used for the near infrared interference measurements. A typical fringe pattern obtained on one of the silicon on sapphire specimens is shown in Figure 2-9. The thickness of that particular specimen was determined by means of the chart in Figure 2-8 and was found to be $0.90 \mu^*$ as shown.

2.7 Structural Properties of the Films

The layers were first examined by optical microscopy. Figure 2-10 shows the typical appearance of two layers grown at 990°C and 1100°C respectively. These micrographs indicate that the growth involves the initiation of very small nuclei which coalesce in a chain-like manner to form a continuous film.

The layers were also examined by reflection electron diffraction in order to determine the orientation of the silicon deposit and the approximate epitaxial temperature. Most of the films studied were approximately 1μ thick and were deposited at a constant rate of $300 \frac{\text{\AA}}{\text{min}}$. Figure 2-11 shows the electron diffraction patterns of films deposited at temperatures ranging

* The thickness of the film determined by weighing using a microbalance was 0.92μ .

Figure 2-9 Near Infrared Interference Pattern for a Thin Silicon Film

from 880°C to 1150°C. The patterns were obtained using 100 kV electrons with a Hitachi 11A microscope. From Figure 2-11(a) it can be seen that at 880°C the film obtained is amorphous, at 950°C (Figure 2-11(b)) the film becomes polycrystalline as indicated by the appearance of Debye rings. As the substrate temperature is raised, the degree of orientation increases as indicated by the appearance of dots along the rings (Figure 2-11(c)). At 1050°C a predominantly single crystal* pattern is formed (Figure 2-11(d)). As the temperature of the substrate is raised above 1150°C, the growth process is disturbed and the films revert to polycrystalline (Figure 2-11(e)). Similar results were obtained for evaporation rates between 200 A/min and 600 A/min. From this investigation it can be concluded that, for the specific set of evaporation parameters considered, the epitaxial temperature lies between 1025°C and 1075°C as compared to 1100-1200°C for pyrolytically grown epitaxial silicon. (55)

Figure 2-12(a) shows the indexed diffraction pattern of Figure 2-11(d). The zone axis of this pattern is $[1\bar{1}0]$. Unallowed reflections appearing in the pattern (indexed in parentheses) commonly occur in electron diffraction at grazing incidence and probably arise from multiple diffractions or twinning. (69) Figure 2-12(b) and (c) show indexed diffraction patterns of the same film, taken at different orientations of the film relative to the electron beam. The zone axes of these patterns are respectively $[\bar{3}12]$ and $[\bar{2}11]$. Unallowed reflections

* In this investigation, a film is classified as single crystal provided the diffraction pattern indicates single crystal patterns and the orientation remains identical over the entire area of the film.

Figure 2-10 Micrographs Showing the Surface Structure of Deposited Layers (magnification x 1200)

(a) 880°C

(b) 950°C

(c) 990°C

(d) 1050°C

(e) 1150°C

Figure 2-11 Reflection Electron Diffraction Patterns for Silicon Films Deposited at Various Substrate Temperatures

are also observed in these patterns. The three zone axes determined from the patterns of Figure 2-12 are perpendicular to the (111) plane indicating a (111) orientation of the film. This finding agrees with the experimental results obtained by Nolder and Cadoff⁽⁷⁰⁾ who found that (111) silicon grows on 60° orientation sapphire.

2.8 Electrical Properties of the Films

2.8.1 Conductivity type determination

The conductivity type was determined by means of the thermoelectric method. If two point contacts are made to the sample and the contacts are kept at different temperatures (either cooling one or heating the other) a potential will appear between them. The polarity of the cold probe is positive for p-type and negative for n-type material.⁽⁷¹⁾ In order to avoid ambiguous results an electrometer was used to detect the potential difference and the samples were cooled to ensure that they were extrinsic before application of the probes. The films were consistently found to be p-type. This result was also confirmed by Hall effect measurements.

2.8.2 Resistivity and Hall effect measurements

The resistivity and Hall effect were measured using a van der Pauw geometry.⁽⁷²⁾ The advantage of this geometry is that the shape of the sample is not critical. The circular samples used were formed by masking and sandblasting. Four aluminum contacts were then evaporated along the circumference

Figure 2-12 Indexed Diffraction Patterns for a Silicon Film

- (a) Identification of Pattern in Figure 2-11(d) (magnified);
- (b) and (c) Identification of Patterns Taken at Different Orientation of the Film with Respect to the Electron Beam.

of the sample and alloyed at 570°C in a nitrogen atmosphere to ensure ohmic contacts to the silicon film. The measuring circuit was similar to the one described by Mitchell and Putley.⁽⁷³⁾

The measurements were carried out at constant current. A Keithley 600-A electrometer with an input impedance of 10^{14} ohms was used as a voltmeter or as a null detector in conjunction with a potentiometer to measure small voltage changes. Due to the high resistivity of the samples, large portions of the circuit had to be shielded to prevent stray signals from entering the meter, and the system was set up on a teflon sheet to obtain the best insulation resistance.*

The resistivity was calculated in the usual manner for van der Pauw geometries⁽⁷²⁾ by substituting in the equation:

$$\rho = \frac{\pi d}{2 \ln 2} \left(\frac{V_{12,34} + V_{23,41}}{I} \right) f \quad (2-2)$$

where ρ is the resistivity in Ω -cm,

d is the thickness of the sample in cm,

$V_{12,34}$ is the voltage across contacts 3 and 4 when the current I is through 1 and 2, and the contacts are numbered in order around the circular sample,

and f is a function of $\frac{V_{12,34}}{V_{23,41}}$.⁽⁷²⁾

The mobility was calculated from the equation:

* A circuit similar to the one described by Fisher et al.⁽⁷⁴⁾ for measuring Hall effect in high resistivity semiconductors, is presently being used by T.W. Tucker⁽⁷⁵⁾ of this laboratory for a more detailed investigation of the galvanomagnetic effects in silicon films.

$$\mu = \frac{d}{H} \cdot \frac{\Delta V_{24,13}}{I} \cdot \frac{10^8}{\rho}, \quad (2-3)$$

where μ is the mobility in $\text{cm}^2/\text{volt-sec}$,

H is the magnetic field across the sample in oersteds,

and $\Delta V_{24,13}$ is the change in voltage $V_{24,13}$ due to the magnetic field.

The thickness of the silicon samples was determined by the infrared interference technique described in section 2.6.*

The results of the measurements on films deposited at 300 $\text{\AA}/\text{min}$ are shown in Table 2-2. The accuracy on the resistivity measurements was estimated at $\pm 5\%$ while the accuracy on mobility measurements was $\pm 15\%$. From these measurements, it appears that the hole mobility in the single crystal films is smaller (by a factor of 15) than the mobility in bulk silicon and that the density of carriers is an order of magnitude larger than the acceptor density in the source material. Both the low mobility and the increased carrier density are possibly due to the large density of crystallographic defects (see section 2.1.2) present in the films.

2.8.3 Minority carrier lifetime

The minority carrier lifetime was measured by the photoconductivity method⁽⁷⁶⁾ which involves the measurement of the decay of the photoconductive current response in the semiconductor after excitation by light. The minority carrier

* The thickness of the films was also determined by weighing and was in all cases within 5% of the value determined by optical interference.

Substrate Temperature	Conductivity Type	Structure of Film	Thickness of Film μ	Resistivity Ω -cm	Hole mobility $\text{cm}^2/\text{volt-sec}$	Carrier Concentration cm^{-3}
950 °C	p	polycrystalline	0.90	10^4	--	--
990 °C	p	oriented polycrystalline	0.92	4×10^3	1	1.8×10^{15}
1050 °C	p	single crystal	0.5	0.5×10^3	20	6.3×10^{14}
1050 °C	p	single crystal	0.94	0.4×10^3	32	4.9×10^{14}
1100 °C	p	single crystal	0.90	0.6×10^3	28	3.7×10^{14}

Table 2-2 Resistivity and Mobility for Silicon Films Deposited at Various Substrate Temperatures

lifetime was found to be between 1-2 μsec in the single crystal films.

2.9 Optical Absorption Edge of the Silicon Films

The onset of optical absorption in a semiconductor occurs when the incident photon energy is equal to the forbidden energy gap between the valence and conduction bands. Studies of this absorption edge yield useful information on the band structure and the crystalline perfection of the semiconductor. In particular it has been shown that the internal strain due to dislocations or grain boundaries causes a broadening of the absorption edge of the semiconductor.⁽⁷⁷⁾

In this investigation, the absorption spectrum of the silicon films deposited at various substrate temperatures was compared with that of bulk single crystal silicon. The difference between the spectra of the single crystal and the evaporated films can be attributed to internal strains in the films and is used as a qualitative measure of the crystallographic perfection of the films.

The relation between the absorption coefficient α of a silicon specimen of thickness d and the transmission t of the specimen and mount may be written as:⁽⁷⁷⁾

$$t = f(r_1) \frac{(1 - r_1)(1 - r_2) e^{-\alpha d}}{1 + r_1 r_2 e^{-2\alpha d}}, \quad (2-4)$$

where r_1 and r_2 are the reflectivities of the first and second specimen surfaces and $f(r_1)$ is a function of the reflectivities of all other interfaces traversed by the beam. Interference

fringes due to multiple reflections inside the specimen were obtained, giving an indication of the thickness of the sample (see section 2.6). They were easily averaged so phase factors were neglected in equation 2-4. In the small spectral range under investigation (0.6 to 1.8 μ) the absorption coefficient α of silicon was small and all other materials were transparent. Thus the variation of the refractive indices and hence the variation of the reflectivities of all materials were negligible. Since only the relative shape of the absorption curves was of interest, the transmission data were normalized so that $t_n = 1$ in the spectral range where the specimens were transparent. This avoided the introduction of the effect of substrates and interfaces with only a small error. The expression used to calculate α was $t_n = e^{-\alpha d}$ with an estimated error in α of 10%. (78)

The measurements were carried out at room temperature using a Cary spectrophotometer. The evaporated specimens were all approximately 1 μ thick. The single crystal silicon specimen was prepared from a (111) p-type, 100 Ω -cm, silicon wafer and thinned down to a thickness of 1 μ by jet chemical polishing using an HNO_3/HF mixture. (79) The results are shown in Figure 2-13. As the substrate temperature is raised, the absorption edge becomes sharper, however in all cases, it is broader than the absorption edge of single crystal silicon indicating a large density of dislocations and grain boundaries even in the single crystal films.

SUBSTRATE TEMP.	TYPE OF FILM
880°C	AMORPHOUS
950°C	POLYCRYSTALLINE
990°C	POLYCRYSTALLINE WITH PREFERRED ORIENTATION
1050°C	ORIENTED SINGLE CRYSTAL
1100°C	ORIENTED SINGLE CRYSTAL

Figure 2-13 The Effect of Substrate Temperature on the Absorption Edge of Silicon

2.10 Summary

An electron beam method of evaporating silicon films on sapphire substrates was described in the preceding sections. The evaporation was carried out from a high resistivity ($> 200 \Omega\text{-cm}$) polycrystalline silicon source in a typical vacuum of 7×10^{-7} mm Hg. The evaporation rates used ranged from 200 - 600 $\frac{\text{Å}}{\text{min}}$. The thickness of the films was 0.5 to 2 μ . The films obtained were of (111) orientation and exhibited single crystal diffraction patterns when the substrate temperature was in the range 1050 to 1100°C. The films were high resistivity ($> 400 \Omega\text{-cm}$) p-type. The carrier mobility in the single crystal films was of the order of 20 - 30 $\text{cm}^2/\text{volt sec}$ and the minority carrier lifetime was typically 1 - 2 μsec . The optical absorption edge of the films was found to be broader than the absorption edge of single crystal silicon at all substrate temperatures. The low carrier mobility of the films, the low minority carrier lifetime as well as the broadening of the optical absorption edge seem to indicate the presence of a large number of crystallographic defects in the films.

3. STUDY OF THE CHARACTERISTICS OF THE SILICON/EVAPORATED SiO_x INTERFACE

Evaporated silicon oxide films have been used as the insulating layers in the silicon thin-film transistors described in this work as well as in CdS and CdSe thin-film transistors. The electrical properties of these devices were found to depend to a large extent on the properties of the semiconductor/insulator interface. This chapter contains the results of a study of the gross characteristics of the silicon/evaporated silicon oxide interface interpreted on the basis of a simple physical model.

The method used in the study of the properties of the interface is the MOS (metal/oxide/semiconductor) technique.^{(80),(81)} This involves the study of the capacitance of the semiconductor surface as a function of the applied normal electric field. This technique is particularly easy to use in the study of oxide covered surfaces since the metal/oxide/semiconductor sandwich provides a convenient capacitor. The essence of the MOS technique lies in a comparison between an idealized theory⁽⁸⁰⁾ and experimental observations: conclusions regarding the nature of the interface are based upon interpretation of the deviations between the two.

The MOS technique has been used very successfully in the study of the Si/thermally grown SiO_2 system. It has been shown on the basis of numerous experiments on that system that:

- (1) The charge in the surface states is practically independent of surface potential,⁽⁸⁰⁾

- (2) The charge in the surface states is positive for both n-and p-type silicon and is independent of the oxide thickness or the doping level, (80)
- (3) The surface state charge density is typically $2 - 5 \times 10^{11} \text{ cm}^{-2}$. (80), (81)

The main object of the investigation reported in the next sections is the evaluation of evaporated silicon oxide films as passivating layers on the surface of single crystal silicon and in particular the determination of the effective surface state density at the silicon/evaporated silicon oxide interface.

3.1 Principles of the MOS Method

The MOS structure is illustrated schematically in Figure 3-1. It consists of an evaporated aluminum field plate (referred to as the "gate"), the oxide dielectric, and the silicon substrate. Contact to the back of the silicon substrate is through an evaporated aluminum electrode. Consider a MOS structure based on a p-type semiconductor. If the voltage

Figure 3-1 The MOS Structure

applied to the field plate, V_G , is negative, holes are attracted to the vicinity of the interface so that the semiconductor is much

like a metal and the capacitance of the MOS structure is approximately the same as the capacitance of the oxide layer alone. On the other hand if the applied voltage is made positive, holes are repelled from the vicinity of the interface, leaving behind a space charge region of uncompensated ionized acceptor ions. This region will be referred to as the depletion region. Because the depletion region adds to the thickness of the dielectric, the capacitance decreases. Upon further increase in the positive applied voltage, electrons are attracted to the vicinity of the interface and form an extremely narrow inversion layer. Additional charge induced in the semiconductor by further increase in the applied voltage will almost entirely appear in the inversion region and therefore the depletion region stops increasing in size. Correspondingly the capacitance reaches a minimum value. In the case where the measurement frequency is low enough in comparison with the generation rate of minority carriers, the electrons will be able to follow the variations of the ac measurement signal, and the capacitance will rise again to the value of the oxide capacitance.⁽⁸²⁾ The maximum width of the depletion region, however, is independent of frequency. In the following discussion only the high frequency characteristics will be considered.

In the absence of surface states and work function difference between the metal and the semiconductor, the capacitance of the device can be assumed to be due to two capacitances in series, one due to the oxide and the other due to the space charge at the silicon surface. Thus the total capacitance per

unit area is:

$$C = \frac{C_s C_o}{C_s + C_o} , \quad (3-1)$$

where C_o is the oxide capacitance per unit area and C_s is the space charge capacitance per unit area. The relationship between the gate voltage V_G , the silicon space charge density Q_s per unit area and the surface potential ϕ_s defined in Figure 3-2, is given by:

$$V_G = \phi_s - \frac{Q_s}{C_o} . \quad (3-2)$$

The theoretical relationship between ϕ_s , Q_s and C_s for silicon has been calculated by Whelan.⁽⁸³⁾ From this relationship and equations (3-1) and (3-2), knowing the oxide capacitance, one can calculate a theoretical curve for the capacitance vs gate voltage (C-V) for a given doping in the silicon substrate. The effect of the work function difference ϕ_{MS} between the metal and the semiconductor and of the surface state charge per unit area Q_{ss} at the insulator/semiconductor interface is simply additive to that of the applied gate voltage, and results in a shift of the C-V curve along the voltage axis. If the charge in the surface states is independent of surface potential, this charge can simply be determined from the displacement between the theoretical and experimental C-V characteristics. The experimental gate voltage is given by:

$$V_G = \phi_s - \frac{Q_s}{C_o} + (\phi_{MS} - \frac{Q_{ss}}{C_o}) , \quad (3-3)$$

where the quantity in brackets represents the offset between the experimental and theoretical curves.

3.2 Experimental Procedure

Boron-doped (111) silicon wafers* were used. The resistivity of the silicon was $1.5 \Omega\text{-cm}$. The lapped wafers were cleaned and chemically polished in a mixture of 4 parts HF to 10 parts HNO_3 . Aluminum was evaporated on the back side of the wafers and alloyed in a nitrogen atmosphere for 5 minutes at 570°C , and the wafers were then allowed to cool down to room temperature in the nitrogen atmosphere to prevent formation of oxide on the front side of the wafer. The oxide layers were evaporated from $\frac{1}{4}$ " pellets of silicon monoxide** at a rate of $5 - 10 \frac{\text{Å}}{\text{sec}}$ using a modified Drumheller type source.⁽⁸⁴⁾ The gates consisted of circular aluminum dots 350μ in diameter evaporated onto the oxide through a beryllium-copper photo-etched mask. A total of 36 devices were fabricated in four batches.

The capacitance-voltage characteristics of the resulting MOS devices were usually obtained at room temperature and in the dark. Figure 3-3 shows a simplified diagram of the C-V measuring equipment. An ac signal (10 mV rms) is superimposed on a dc bias and applied to the MOS device. The termination resistor R is a much lower impedance than the capacitor and the voltage appearing across it is thus proportional to the MOS capacitance. This voltage is amplified, converted to dc and applied to the vertical channel of an x-y recorder. The bias

* Texas Instrument Co. Inc., Dallas, Texas.

** "Select Grade", Kemet Co., Cleveland, Ohio.

Figure 3-2 The Energy Bands in an MOS Structure Under Applied Gate Bias

- * GR Type 1232-A
- ** Moseley Type A-1
- *** Moseley Type 135

Figure 3-3 Diagram of C-V Measurement Equipment

voltage is electronically swept about any desired average value such that a C-V curve is traced in about 100 sec. The measurement frequency was 100 kHz. In most cases the curves followed the high frequency characteristics. Some of the samples were selected for more precise measurements using a General Radio 1615-A Capacitance Bridge.

The thickness of the oxide layers and their indices of refraction were determined using an L119 Gaertner ellipsometer.⁽⁸⁵⁾ The dielectric constant of the oxide was measured by applying a bias large enough to produce a strong accumulation layer at the semiconductor surface, such a layer acts as a metal electrode and only the oxide capacitance is measured.

3.3 Experimental Results

Figure 3-4 shows the experimental and theoretical capacitance-voltage characteristics for a typical sample. The two curves are approximately parallel throughout the entire range of variation of the capacitance, lending support to the assumption that the charge in the surface states is independent of surface potential. Thus the horizontal displacement between a pair of points corresponding to the same value of capacitance on the two curves immediately yields the value $(-\phi_{MS} + \frac{Q_{ss}}{C_o})$, in this case 3.6 V.

The metal-semiconductor work function for p-type silicon with about 10^{16} cm^{-3} impurities is approximately -0.7 V .⁽⁸⁰⁾ On this basis $\frac{Q_{ss}}{C_o} = 2.9 \text{ V}$ and therefore $\frac{Q_{ss}}{q} = 3.6 \times 10^{11} \text{ cm}^{-2}$. In all cases the charge in the surface states was found to be

Figure 3-4 Determination of the Surface State Density by Comparison of the Experimental Characteristic with the Theory for p-type Silicon

positive and independent of the oxide thickness. However it was observed that the effective surface charge density was consistently larger for the oxides evaporated in low vacuum. The characteristics of two samples evaporated at 5×10^{-7} mm Hg and 5×10^{-5} mm Hg respectively are listed in Table 3-1.

In some of the samples a hysteresis in the C-V characteristics was observed. The hysteresis can be attributed to limited migration of the space charge in the oxide during tracing of the C-V curve or to electronic trapping effects within the oxide.

The effect of the ambient on the C-V characteristics was also observed. Figure 3-5 shows the C-V curve before and after exposure to water vapour and vapour from a water solution containing NaCl. The shift in the characteristic after exposure to water vapour was found to be reversible under heat treatment at 120°C . In the case of exposure to NaCl vapour the shift is considerably larger and was found to be only partially reversible under heat treatment with applied gate voltage. The adsorbed ionic charge density can be estimated from the shift of the characteristic C-V curve. In the case of water vapour the ionic charge density is approximately 10^{11}cm^{-2} and in the case of sodium contamination it is $3 \times 10^{11}\text{cm}^{-2}$.

3.4 Summary

The effective surface state density at the Si/evaporated SiO_x interface is of the same order of magnitude ($3-4 \times 10^{11}\text{cm}^{-2}$) as that at the Si/thermally grown SiO_2 interface. Furthermore,

Sample #	Pressure During Evaporation mm Hg	Rate of Evaporation ° A/sec	Thickness ° Å	Optical Refractive Index	Relative Permittivity	Effective Surface State Density cm ⁻²
3.1	5×10^{-7}	5	2190	2.03	5	3.6×10^{11}
4.2	5×10^{-5}	5	2260	1.85	4.8	9×10^{11}

Table 3-1 Characteristics of Typical MOS Samples

Figure 3-5 Effect of Ambient on the C-V Characteristics

the surface state density is larger with an oxide evaporated in poor vacuum than with one evaporated in good vacuum. This result is in agreement with the experimental observations made on the threshold voltage of the TFTs (see section 4.2). The larger surface state densities in the oxides evaporated under poor vacuum are probably due to the presence of excess ions within the oxide. Water vapour and in particular high mobility ions like sodium appear to have a considerable effect on the semiconductor surface potential and are probably the cause of the drift and instabilities observed in the threshold voltage of the TFTs (see section 4.5).

4. SILICON THIN-FILM TRANSISTORS

4.1 Device Fabrication

The devices were fabricated by evaporation onto sapphire substrates (60° orientation). The photograph of an actual device is shown in Figure 4-1. The method and the system used in the deposition of the silicon thin films were described in section 2.4 and 2.5. Most of the devices were fabricated on predominantly single crystal films unless otherwise noted. The system used in the deposition of the metal electrodes and the insulator films is an 18" glass bell-jar Veeco evaporator. The system is evacuated by means of a 4" oil diffusion pump and a liquid nitrogen cooled trap. A movable substrate holder and shutter are fitted inside the bell jar and can be operated from outside the vacuum system. A photograph of the evaporation system is shown in Figure 4-2. The thickness of the evaporated films was monitored during evaporation by means of calibrated quartz crystal^{(66), (67)} oscillators fitted inside the vacuum system close to the substrate. A separate vacuum cycle was used for each evaporation.

The electrode and insulator patterns of the experimental TFTs were produced by means of photo-etched beryllium-copper masks mounted close to the substrate in a jig which permitted the adjustment of the substrate relative to the mask. The source-drain gap was defined by means of a $20\ \mu$ tungsten wire stretched across the source-drain mask and the gap width was 0.16 cm.

The most critical dimensions of the insulated-gate transistor are the thickness of the insulator, the lateral spacing of the source-drain gap and the positioning of the gate. The semiconductor thickness is not particularly critical except when the semiconductor resistivity is so low that its thickness must be kept to a minimum. The area of the semiconductor and insulator and the thickness of the metal electrodes need be controlled but are not usually critical.

Figure 4-1 Photograph of a Silicon Thin-Film Transistor

4.1.1 The source-drain contacts

The operation of the silicon TFT requires an ohmic source contact to the inversion (n-type) layer, i.e. a minority carrier (electron) injecting contact with respect to the p-type film (see section 1.4). Aluminum electrodes were found to make injecting contacts to the p-type silicon films.⁽⁸⁶⁾ The experimental V-I characteristics of these contacts are discussed in section 4.2.1.

The aluminum (99.999% purity) clips were evaporated

Figure 4-2 Photograph of the Al, SiO_x Evaporation Setup

from tungsten wires in a vacuum of 10^{-6} mm Hg at a relatively fast rate ($\approx 1000 \text{ Å/min}$). The thickness of the source and drain electrodes was typically 1000 Å . The exposure of the silicon films to the atmosphere prior to the evaporation of the source-drain contacts was kept a minimum in order to reduce the formation of the oxide film which normally covers the silicon surface and which may hinder the transport of carriers especially at low temperatures.

Failure to achieve good injecting contacts at the source can give rise to a low transconductance and to the peculiar "crowded"⁽²⁸⁾ characteristics in which the transconductance, instead of increasing with gate bias, levels off and decreases towards zero as the family of characteristic $V_D - I_D$ curves crowd together at a maximum value of I_D . A poor contact at the drain electrode is less serious but it yields an S-shaped characteristic in the neighborhood of the origin.

4.1.2 The insulating layer

The silicon oxide SiO_x insulating layers were evaporated from $\frac{1}{4}$ " pellets of silicon monoxide*. The source heater was a modified Drumheller⁽⁸⁴⁾ type source consisting of a tantalum canister with a tantalum screen. The source temperature was measured by means of a thermocouple inserted in the center of the canister. The SiO_x layers were typically $1000 - 2000 \text{ Å}$ thick and were evaporated from a source at a temperature of about 1200°C to 1250°C resulting in rates of deposition of 3 to 10 Å/sec . The pressures used during

* "Select Grade", Kemet Co., Cleveland, Ohio.

evaporation ranged from 5×10^{-5} mm Hg to 5×10^{-7} mm Hg. The low frequency relative permittivity of the oxide was found to vary between 4.8 and 5 (see section 3.3). Insulation breakdown fields in excess of 10^6 volt/cm were obtained and the dielectric loss tangent at 1 kHz was typically between 0.01 and 0.03.

4.1.3 The gate electrode

The deposition conditions of the aluminum gate electrode were identical to those of the source-drain electrodes.

4.2 Experimental Results

4.2.1 V - I characteristics of the source-drain contacts

The typical volt-ampere characteristics from source to drain are shown in Figure 4-3. Before application of the oxide the characteristic is essentially the same as that for back to back diodes. After application of the oxide the characteristic indicates a conducting path from source to drain due to the formation of an inversion layer.

4.2.2 Operating characteristics of the silicon TFTs

The measurements reported here were carried out with the devices in vacuum and in the dark. The ambient pressure was maintained in the one to ten micron range by means of a rotary vacuum pump. Accurately positioned platinum wire probes were used to make electrical contacts to the transistors. The $V_D - I_D$ characteristics were obtained using a Tektronix 575 transistor curve tracer. Figure 4-4 shows a set of drain current vs drain

voltage characteristics for one of the transistors fabricated. The unit shown has a maximum transconductance of $60 \mu\text{mho}$. The dynamic output resistance derived from the saturated portion of the curve is $150 \text{ k}\Omega$. The voltage amplification factor calculated from the product of these two quantities is 9. The input capacitance under operating conditions is 40 pf for a gate width of 50μ . The calculated gain-bandwidth product is 0.25 MHz, and the dc input resistance is larger than $10^{10} \Omega$. Some of the devices built with the same geometry exhibited transconductances of up to $100 \mu\text{mho}$, voltage gains of 20 and gain-bandwidth products of 1 MHz.

Most of the devices fabricated were depletion mode devices, i.e. V_T was negative. However, it was found experimentally that the magnitude of V_T could be controlled between 4 and 12 volts by proper choice of the oxide insulator. If the oxide was deposited in good vacuum (5×10^{-7} mm Hg) and at fast rate ($10 \text{ \AA/sec}$), the resulting $|V_T|$ value was small. An example of the characteristics of this type of device is shown in Figure 4-4. If the oxide layer was evaporated in poor vacuum (5×10^{-5} mm Hg) and at slow rate ($3 \text{ \AA/sec}$) the resulting $|V_T|$ value was large. Figure 4-5 shows the $V_D - I_D$ characteristics for a device with $V_T = -10 \text{ V}$. Similar effects were observed on the MOS structure investigated in chapter 3.

The TFT characteristics exhibit good saturation as shown in Figures 4-4, 4-5 and 4-6(a), (b). The finite incremental source-drain resistance in the saturation region is most probably due to space-charge-limited currents in the pinched-off region. (31)

Figure 4-3 $V_D - I_D$ Characteristics of the Source-Drain Contacts

Some of the devices built on high resistivity single crystal or polycrystalline silicon failed to saturate and exhibited characteristics similar to the plate characteristics of a vacuum triode as shown in Figure 4-7. This behavior can be attributed to the fact that a conducting channel is not formed and the device operates as a space-charge-limited triode. (15), (87)

Figure 4-4 Operating $V_D - I_D$ Characteristics for a Silicon TFT (2V/div. horizontal, 50 μ A/div. vertical, gate voltage 0.5V/step); Si thickness $\approx 0.5\mu$, SiO_x thickness $\approx 0.2\mu$, Al Electrodes thickness $\approx 0.1\mu$.

Figure 4-5 Operating $V_D - I_D$ Characteristics for a Silicon TFT (2V/div. horizontal, 20 μ A/div. vertical, gate voltage 1V/step)

Figure 4-8 shows the characteristic curves of a transistor with drain voltage extended into the breakdown region. A "soft" (gradual) breakdown is apparent with a hardening of the knee as the gate voltage decreases. This breakdown is most likely to occur between source and drain and begins in the region of maximum field near the drain. The soft breakdown characteristic is caused by the generation of impact ionized hole-electron pairs in the high field of the drain region. Since these holes and electrons act as a shielding plasma, the onset of severe avalanching is spread out over a wider voltage range.⁽⁸⁸⁾ The average breakdown field observed in the devices tested varied between 1.5×10^4 to 2.5×10^4 volt/cm. These values are of the same order of magnitude as the ones obtained in MOS transistors, but are much smaller than the field required for avalanching in bulk silicon (2×10^5 volt/cm).⁽²⁹⁾ This is probably due to the fact that the breakdown in the TFT is a surface effect, dominated by imperfections affecting the surface channel, rather than a bulk effect.

4.2.3 Comparison of the simplified theory with experiments

In this section, the elementary theory presented in section 1.5 and the characteristics calculated from it (section 1.6) are compared with experimental data taken on some of the fabricated devices.

Experimental data were obtained for the following characteristics: (a) I_D vs V_G with V_D as a parameter (transfer characteristics), (b) g_m vs V_G with V_D as a parameter and

Figure 4-6 Saturation $V_D - I_D$ Characteristics

- (a) 5V/div. horizontal, 50 μ A/div. vertical, gate voltage 1V/step
- (b) 5V/div. horizontal, 100 μ A/div. vertical, gate voltage 2V/step

Figure 4-7 Operating $V_D - I_D$ Characteristics for a TFT Fabricated on a Polycrystalline Silicon Film (1V/div. horizontal, 10 μ A/div. vertical, gate voltage 1V/step).

Figure 4-8 Operating $V_D - I_D$ Characteristics for a TFT Showing the Breakdown Region (5V/div. horizontal, 100 μ A/div. vertical, gate voltage 1V/step).

(c) g_{do} vs V_G with $V_D = 0$. The transfer characteristics were obtained at dc and were recorded directly using an x-y recorder. The channel conductance as a function of dc gate voltage was obtained by graphically differentiating the dc $V_D - I_D$ curves near the origin. In order to check the accuracy of this method the channel conductance was also measured by applying a small ac voltage (100 Hz) in series with the source-drain and determining the ac current. Results obtained from these two methods agreed within 5%. The transconductance was measured by superimposing a small ac signal (1 kHz) on the dc bias between gate and source. The ac signals used in all measurements were smaller than 5 mV rms. The ac channel currents were determined by measuring the voltage across a small resistance R (≤ 10 ohms) in series with the channel. A narrow band detection system was used throughout the measurements. The detected signal was converted to dc and applied to the y channel of an x-y recorder. Figure 4-9 shows a simplified diagram of the transconductance measurement setup.

Figure 4-9 Simplified Diagram of the Setup Used in the Trans-Conductance vs Gate Voltage Measurements.

From the transfer characteristics, a plot of $\sqrt{I_{DS}}$ vs V_G can be obtained and is shown for TFT #2 in Figure 4-10. Linear dependence of $\sqrt{I_{DS}}$ on the gate voltage is observed over a range of gate voltages in agreement with the theory. Departure from linearity is observed at low and high gate voltages. From the slope of the plot, knowing the oxide capacitance and the dimensions of the device one can determine the effective mobility of the carriers in the channel from equation (1-7). The effective mobility is given by:

$$\mu_n = \frac{2L}{C_o W} \left(\frac{\delta \sqrt{I_{DS}}}{\delta V_G} \right)^2 \frac{1}{V_D} \quad (4-1)$$

For the device under consideration, the experimental effective mobility is approximately 5 cm²/volt-sec. The best devices fabricated had effective mobilities as high as 10 cm²/ volt-sec.

The agreement between the ideal theory and the measurements of transconductance is less satisfactory, as can be observed in Figure 4-11. The transconductance has a maximum near the saturation gate voltage and instead of remaining constant in the saturation region it decreases at high gate voltages.

A disagreement is also indicated in the g_{do} vs V_G curve as shown in Figure 4-12. The conductance is virtually zero up to the threshold voltage V_T , then rises gradually and saturates at high gate voltages. Similar departures from the theory have been observed by Sah⁽²⁷⁾ in MOS transistors fabricated on bulk silicon.

Figure 4-11 Experimental Transconductance vs Gate Voltage Characteristics

Figure 4-12 Experimental Channel Conductance vs Gate Voltage

The departure from theory at low gate voltages might be attributed to:

- (1) non-linearities due to contact effects,
- (2) changes in the surface mobility, and
- (3) the presence of surface traps which as they are gradually filled with increasing gate voltage allow more of the charge generated in the semiconductor by the gate voltage to contribute to the conduction mechanism.⁽⁸⁹⁾

Linear $V_D - I_D$ characteristics were observed at small source-drain voltages indicating that non-linearities due to the contacts can be excluded. Changes in the surface mobility in silicon at low surface fields have not been reported.⁽³¹⁾ The filling of surface traps is therefore the most likely mechanism which can account for the observed discrepancies at low gate voltages. Trapping effects imply a transconductance which is frequency dependent, as predicted by Haering,⁽⁹⁰⁾ who showed that for the case of constant mobility the magnitude of the small signal transconductance near zero source-drain voltage is an increasing function of frequency and the output current leads the output voltage (i.e. $\tan \Psi > 0$) regardless of the bias conditions. This behavior arises from the fact that at frequencies which are lower than the characteristic frequencies of the traps, the transconductance is reduced since a fraction of the induced carriers is always trapped. However, at higher frequencies, the traps are unable to follow the gate voltage variations and have no effect.

In order to confirm the presence of traps, measurements of the transconductance as a function of frequency were carried out at zero source-drain voltage. The measurement setup is the same as shown in Figure 4-9 except that a high sensitivity detector (Princeton Applied Research, Lock-in Amplifier Model HR-8) was used to monitor the small signal source-drain current. The results obtained on TFT #16 are shown in Figure 4-13. As observed the transconductance is an increasing function of frequency confirming the presence of traps,* however due to the small signals and the small transconductances involved, the measurements had to be restricted by the sensitivity of the measuring equipment to a range of frequencies below 50 kHz preventing a complete characterization of the traps. In order to characterize the traps a detailed study of the source-drain conductance is carried out in the following sections.

At high gate voltages, under high inversion conditions, most of the surface traps are filled. The observed reduction in conductance and transconductance with increasing gate voltage can be attributed to the increasing reduction of carrier mobility due to surface scattering⁽⁹¹⁾ and is discussed in section 4.4. Sah and Pao⁽⁹²⁾ have also attributed some of the decrease of the transconductance in the saturation region in MOS transistors to effects associated with the bulk charge due to ionized impurities

* The dielectric relaxation effects, which contribute a decrease in g_m due to the decrease of the oxide capacitance with increasing frequency, were estimated from measurements on an Al/SiO_x/Al sandwich. The oxide capacitance was found to decrease by 1% per decade of frequency in the range 10^2 to 10^5 Hz.

Figure 4-13 Normalized Transconductance and Phase as a Function of Frequency

and its variation as a function of surface potential.

4.3 The Source-Drain Conductance

4.3.1 Theoretical model to account for trapping effects on the source-drain conductance

In investigating the surface trapping effects, the assumptions made in section 1.5 will be taken as valid, except for assumption 4 and instead carrier trapping^{(90),(93),(94)} will be used to account for the observed source-drain conductance characteristics. The traps will be assumed to lie at the silicon/insulator interface and will be specified by a single energy level in the forbidden gap and by their effective density and their capture cross-section for electrons.

Assuming that the states communicate with the conduction band then the rate per unit area at which electrons are trapped is proportional to the number of free electrons and the number of empty states and is given by:

$$\mathcal{Q}_t = Sv n'_c (N_t - n_t) \quad (4-2)$$

where S is the effective cross-sectional area of the traps, v is the thermal velocity of free electrons, n'_c is the volume density of free electrons, N_t is the surface density of traps and n_t is the surface density of trapped carriers. The product $S(N_t - n_t)$ is the probability that an electron is captured by a state. Similarly the rate per unit area at which the electrons are emitted from the traps is proportional to the number of traps and the density of carriers n'_l which would be present in

the semiconductor if the Fermi level was at the trap level and is given by:

$$\mathcal{Q}_e = Sv n_1' n_t , \quad (4-3)$$

and

$$n_1' = N_c e^{-\frac{E}{kT}} , \quad (4-4)$$

where N_c is the effective volume density of free carriers in the conduction band and E is the ionization energy of the traps. The net rate of change of trapped carriers is therefore:

$$\frac{\delta n_t}{\delta t} = Sv n_c' (N_t - n_t) - Sv n_1' n_t . \quad (4-5(a))$$

At equilibrium the rate of change of trapped carriers must be zero and therefore:

$$n_c' (N_t - n_t) = n_1' n_t , \quad (4-5(b))$$

or

$$n_c (N_t - n_t) = n_1 n_t , \quad (4-6)$$

where $n_c = \int_0^h n_c' (y) dy$ is the surface density of carriers, h

is the effective thickness of the inversion layer, and

$n_1 = \int_0^h n_1' dy$. At zero applied gate voltage, equation (4-6)

becomes

$$n_{co} (1 - f_{to}) = n_1 f_{to} , \quad (4-7)$$

where $f_{to} = n_{to}/N_t$ is the initial occupancy of the traps, n_{co} is the initial density of free electrons and n_{to} is the initial density of trapped carriers.

The total charge per unit area induced due to an applied gate voltage is given by:

$$q\Delta n = q(\Delta n_c + \Delta n_t) = C_o V_G, \quad (4-8)$$

or

$$q(\Delta n_c + \Delta n_t) = q[(n_c + n_t) - (n_{co} + n_{to})] = C_o V_G. \quad (4-9)$$

If the gate to source voltage is sufficiently negative to deplete the initial charge, the channel will be cut-off. The voltage at which this happens is the gate threshold voltage given by:

$$V_T = - \frac{q}{C_o} (n_{co} + n_{to}), \quad (4-10)$$

and therefore

$$q(n_c + n_t) = C_o (V_G - V_T). \quad (4-11)$$

At equilibrium, with an applied gate voltage, the number of filled traps, given by equation (4-6), is:

$$n_t = \frac{n_c N_t}{n_c + n_l}. \quad (4-12)$$

Substituting for n_t into equation (4-11) we get:

$$q(n_c^2 + n_c n_l + n_c N_t) = C_o (V_G - V_T)(n_c + n_l). \quad (4-13)$$

The charges can be expressed in terms of the following effective voltages:

$$V_c = \frac{qn_c}{C_o}, \quad (4-14)$$

$$V_t = \frac{qN_t}{C_o} , \quad (4-15)$$

$$V_l = \frac{qn_l}{C_o} . \quad (4-16)$$

Substituting into equation (4-13) we get:

$$V_c^2 + V_c [(V_t + V_l) - (V_G - V_T)] - V_l(V_G - V_T) = 0 , \quad (4-17)$$

and

$$V_c = \frac{1}{2} [(V_G - V_T) - (V_t + V_l)] + \frac{1}{2} \sqrt{[(V_G - V_T) - (V_t + V_l)]^2 + 4V_l(V_G - V_T)} \dots \quad (4-18)$$

The source-drain conductance at zero source-drain voltage is given by:

$$g_{do} = q n_c \mu_n \frac{W}{L} = C_o \mu_n \frac{W}{L} V_c . \quad (4-19)$$

This expression reduces to equation (1-8(b)) provided V_l is small and $(V_G - V_T) \gg (V_l + V_t)$, i.e. in the case of small trap densities and large trap ionization energies.

From this model one can also predict that the temperature dependence of the conductance will be determined by the temperature dependence of the mobility and the ionization energy (implicit in n_l) of the surface traps. The temperature dependence of the surface mobility of electrons in silicon has been investigated by Leistiko et al⁽⁹⁵⁾ who found a $T^{-1.5}$ dependence at high temperatures ($> 100^\circ\text{C}$). While surface mobility is highly dependent on surface treatment it can be assumed that a decrease, or at least no increase in mobility, is to be expected with

increasing temperature.⁽⁹⁵⁾ At low dc gate voltage, the temperature dependence of the conductance will be dominated by the ionization of traps which donate charge to the semiconductor surface thus increasing the number of mobile carriers and therefore the conductance with increasing temperature. The slope of the conductance vs $1/T$ curve should give the ionization energy of the traps. At higher gate voltage more traps should be filled, the effective ionization energy should decrease and the temperature dependence of the mobility should become more effective. When all the traps are filled the conductance should reflect only the mobility change as a function of temperature.

By comparing the experimental results with the theory presented above one can determine the effective density of traps, their initial occupancy as well as their ionization energy. However, in order to completely characterize the traps, an estimate of their dynamic response is necessary. A method of determining the electron-emission time constant from the trap is discussed below. It involves measurements of the large signal transient response of the source-drain conductance.

Considering equation 4-5(a), the large signal (step response) solution of this equation remains exponential as long as the following two conditions are fulfilled: $n'_c < n'_l$ and n_t is not too small compared to N_t .⁽⁹⁷⁾ The time constant of the process under these conditions is simply the electron emission time constant τ_e given by:

$$\tau_e = (8vn'_l)^{-1}. \quad (4-20)$$

The above conditions can be maintained over a considerable portion of the amplitude of the relaxation process if a large positive voltage pulse is applied to the gate. At the leading edge of the pulse, electrons drop into the unoccupied surface traps and due to the large value of n'_c established by the positive voltage step the charging of the states is fast and equilibrium is rapidly established between the trapped and mobile electrons. At the termination of the pulse, the excess trapped electrons, initially repel from the surface an equal number of free electrons and the surface conductance drops abruptly. The subsequent emission of the trapped charge can be measured as a relaxation of the surface conductance to its equilibrium value prior to the application of the external field. When only one set of states is involved, the initial portion of the curve (where n'_c is small compared to its final value) is exponential and can be used to determine the emission time constant. The temperature dependence of the relaxation time can also be used to estimate the ionization energy of the traps. Several sets of states may be involved in the charge emission process. Unless the states are very close in energy, however, each will dominate the relaxation process at a different applied gate voltage and can be singled out accordingly.

4.3.2 Comparison of the modified theory of the source-drain conductance with experiments

The experimental measurements were carried out under vacuum and in the dark on five of the devices fabricated. The

source-drain conductance was measured as a function of a dc applied gate voltage (see section 4.2.3). Measurements of the temperature dependence of the conductance were carried out with the sapphire substrate resting on a large copper block provided with a heater and a cooling coil through which liquid nitrogen could be circulated. By means of this setup, the temperature of the substrate could be accurately controlled between -200°C and 200°C . The transient response of the source-drain conductance to a positive voltage pulse applied to the gate was observed using the circuit shown in Figure 4-14.⁽⁹⁸⁾ The measurement procedure was as follows: with the pulse applied to the gate and the dc measuring voltage V_D shorted out, the resistor R_1 is adjusted until the signal on the CRO is a minimum. Under these conditions, the displacement current in the MOS capacitor is evenly distributed across the two input terminals of the differential amplifier. When the dc measuring voltage is switched on, the trace on the oscilloscope represents very nearly the true field-effect signal.⁽⁹⁷⁾ The resistors R_1 and R_2 were kept small to prevent the time constant of the circuit from influencing the relaxation time measurements.⁽⁹⁸⁾ The dc measuring voltage was typically 1-2 volts.

To estimate the constant parameters in equation 4.19, this equation was fitted to the experimental results obtained on the five devices investigated. The fit was fairly good in all five cases. The estimated trap densities were between $4 - 7 \times 10^{11} \text{ cm}^{-2}$ and their initial occupancy varied between 0.7 and 0.85. Figure 4-15 shows the theoretical fitting of the experimental conductance characteristic presented in Figure 4-12

Figure 4-14 Circuit Used in Measuring Transient Response of the Source-Drain Conductance

for TFT #2. For this device the constants and trapping parameters were estimated to be:

$$N_t \approx 6 \times 10^{11} \text{ cm}^{-2} ,$$

$$n_{oo} \approx 2 \times 10^{11} \text{ cm}^{-2} ,$$

$$f_{to} \approx 0.8 ,$$

$$n_1 \approx 6 \times 10^{10} \text{ cm}^{-2} .$$

For all the devices investigated, the conductance was found to increase with temperature at zero gate voltage and became relatively less dependent on temperature at gate voltages ranging from 6 to 10 volts in agreement with the theory.

Figure 4-15 Theoretical and Experimental Channel Conductance vs Gate Voltage Characteristic

Experimental temperature dependence data was obtained for both increasing and decreasing substrate temperatures from -50°C to 150°C . The points for increasing and decreasing temperatures fall on one smooth curve in three of the samples investigated indicating a stable oxide. In two cases, however, a large hysteresis was observed between the results obtained for increasing temperatures and those obtained for decreasing temperatures. This hysteresis is most probably due to ionic charge migration within the oxide.⁽⁹⁹⁾ The trap ionization energies at zero gate voltage ranged from 0.16 to 0.22 eV. The temperature dependence of the conductance for TFT #2 is shown in Figure 4-16.

The electron emission time constant τ_e in the samples investigated was estimated to be between 10 and 20 μsec . The observed transient response for TFT #3 is shown in Figure 4-17(a)* and an expanded view of the relaxation waveform for TFT #2 is shown in Figure 4-17(b) from which the relaxation time is estimated to be $\tau_e \approx 10 \mu\text{sec}$. The temperature dependence of the emission time constant for that device was also measured. The value of the ionization energy (0.18 eV) determined from the slope of the τ_e vs $1/T$ plot agrees fairly well with the value determined from the temperature dependence of the conductance (Figure 4-16) at zero gate voltage.

4.4 Surface Mobility

As mentioned in section 4.2.3, the observed reduction of g_{d0} with increasing gate voltage is due to the reduction of

* Similar waveforms were observed by Miksic et al⁽¹⁰⁰⁾ in their CdS TFT (unit #1).

Figure 4-16 Temperature Dependence of the Channel Conductance

Figure 4-17 (a) Transient Response of the Source-Drain Conductance to a Repetitive Pulse (500 $\mu\text{sec}/\text{div.}$ horizontal)
 (b) Relaxation Waveform at the Termination of the Pulse (5 $\mu\text{sec}/\text{div.}$ horizontal)

Figure 4-18 Temperature Dependence of the Electron Emission Time Constant

carrier mobility caused by surface scattering. The experimentally observed μ_{d0} is used in this section to determine the effective surface mobility at high surface fields.

A reduction of the surface carrier mobility relative to the bulk is to be expected if the transverse field (normal to the surface) is sufficiently high and if in addition the surface is a diffuse scatterer (i.e. the carriers are randomized thermally upon impinging at the surface). The effect of surface scattering in semiconductors was discussed by Schrieffer⁽¹⁰¹⁾ who extended the treatments of Fuchs⁽¹⁰²⁾ and Sondheimer⁽¹⁰³⁾ on metal films by incorporating the effects of the surface potential barrier. (Such effects are insignificant in metals, where the thickness of the space charge layer is of the order of an interatomic spacing.) Assuming a linear potential gradient at the surface and complete diffuse scattering Schrieffer showed that at constant high transverse fields the carrier mobility is inversely proportional to the field strength. In addition, it is generally assumed that as the field near the surface is decreased the mobility approaches the corresponding bulk mobility. Recent experiments on the conductivity of inversion layers in p- and n-type silicon indicate that:

- (a) the effective mobility of the carriers in the inversion layer is in general dominated by a combination of specular and diffuse scattering, (95), (104)
- (b) the effective mobility is constant at low surface fields ($< 1.5 \times 10^5$ volt/cm) (this observation was used as an assumption in deriving

equation (4-19)) and is lower than the bulk mobility,⁽⁹⁵⁾

- (c) the effective mobility at high fields follows a modified Schrieffer formula.⁽¹⁰⁴⁾

The experimental effective mobility at high gate voltages was obtained from equation (4-19) and is given by:

$$\mu_n = \frac{\epsilon_{do}}{C_o \frac{W}{L} V_c}, \quad (4-21)$$

where the constant parameters in V_c were determined at low gate voltages as discussed in section 4.3.2. Figure 4-19 shows the effective mobility for TFT #2, as a function of $1/F_s$, where F_s is the surface field normal to the channel and is approximately given by $F_s \simeq \frac{C_o V_c}{\epsilon_{si}}$ and ϵ_{si} is the permittivity of silicon.

The experimental results can be expressed in the form:

$$\mu_n = \mu_o + \frac{v_s}{F_s} * , \quad (4-22)$$

where μ_o can be interpreted as a specular scattering term and v_s/F_s as a diffuse scattering term, v_s being an effective surface carrier velocity. The values of μ_o and v_s for the sample under consideration are given in Figure 4-19. Using this interpretation,

* The form of this equation is suggested by the work of Fuchs⁽¹⁰²⁾ who assumed that the effective surface mobility can be written as:

$$\mu_{eff} = p \mu_b + (1 - p) \mu_d ,$$

where μ_b is the bulk mobility, μ_d is the diffuse scattering limited mobility and p is the probability that a carrier striking the surface will be specularly scattered.

Figure 4-19 Surface Mobility as a Function of $1/F_s$

which was found valid in the case of MOS transistors,⁽¹⁰⁴⁾ the samples examined indicate that electrons in the inversion layer undergo specular as well as diffuse scattering. The relative percentage of each varying from device to device depending on the surface conditions.

4.5 Stability

Under ideal conditions the drain current of an insulated-gate TFT should be uniquely determined by the voltages applied to the gate and drain independently of duration of application. While such stability is approached in many of the vacuum encapsulated units others exhibit an irreversible deterioration of the transconductance and a gradual shift in the threshold voltage particularly when exposed to a humid atmosphere or to thermal and electrical stresses. Some of the units also exhibit hysteresis loops in the drain characteristics as observed on a conventional curve tracer and illustrated in Figure 4-20.

The slow drift and other instabilities in the characteristics can be attributed to electronic traps⁽⁴¹⁾ and ionic defects⁽¹⁰⁵⁾ within the oxide and to mobile ionic charge in the surface or in the interior of the oxide. It is believed, at least in the case of thermally grown silicon dioxide films, that the ionic defects are oxygen vacancies^{(106), (107)} which give rise to a space charge within the oxide films. This space charge can be altered by thermal and electrical stresses. The mobile portion of the charge is assumed to result from contamination of the oxide by high mobility ions for example sodium⁽¹⁰⁸⁾

or from metal ions⁽¹⁰⁸⁾ originating from the gate electrode. In evaporated silicon oxide films an added source of instability is the hygroscopicity of the oxide. The observed hysteresis loops may also be attributed to internal heating effects or to an insulating layer having a range of dielectric relaxation times.

Some of the drift and instabilities can be overcome by reducing the mobile charge density and by nullifying the effects of the space charge within the silicon oxide films. The first objective can be achieved by careful processing and improved cleanliness and by proper choice of the metal electrodes to prevent metal ion migration. The second objective can be accomplished by high temperature bias^{(106),(107)} treatments which can lock an interface charge that will not decay at device operating temperature, or by heat treatments of the devices in a hydrogen^{(109),(110)} atmosphere: this process effectively reduces density of acceptor surface states by introducing donor states.⁽¹⁰⁹⁾ An alternative solution of the stability problem can also be found in the use of new insulating layers. It has recently been claimed that sputtered or chemically deposited silicon nitride⁽¹¹¹⁾ is more effective as a passivating layer than thermally grown SiO_2 in MOS transistors.

4.6 Summary

The fabrication and operation of the evaporated silicon thin-film transistors were described in the preceding sections. Devices with transconductances up to 100 μmho and

Figure 4-20 Hysteresis Loops in the Drain Characteristics of the TFT (1V/div. horizontal, 10 μ A/div. vertical, gate voltage 1V/step)

gain-bandwidth products up to 1 MHz were obtained. The experimental results were compared with the elementary field-effect theory presented in Chapter 1. Some of the discrepancies between theory and experiment at low gate voltages were explained by taking into account trapping effects. A characterization of the traps by a method which involves measurements of the source-drain conductance, its temperature dependence and its transient response was discussed. The typical trap densities obtained by this method are of the order of $4 - 7 \times 10^{11} \text{ cm}^{-2}$. The ionization energies of the traps ranged from 0.16 to 0.22 eV and the electron emission time constants were between 10 and 20 μ sec at zero gate voltage. At higher gate voltages, the discrepancies between theory and experiment were attributed to the surface scattering effects on the mobility. The effective mobility

was found to be dominated by a combination of specular and diffuse scattering. The instabilities of the TFTs were also discussed.

5. CONCLUSION

Silicon thin-film transistors having useful gain were fabricated by evaporation techniques compatible with those used in making thin film passive components. The silicon TFTs are promising thin-film active elements but suffer, at the present stage of their development, from relatively low transconductance.

In the course of this investigation, the factors affecting the fabrication, the design and the performance of these TFTs; in particular the properties of the evaporated silicon films and of the Si/evaporated SiO_x interface, were discussed.

A method of evaporating silicon by electron beam heating was described. The films obtained were high resistivity ($> 400 \Omega\text{-cm}$) p-type and exhibited single crystal diffraction patterns at substrate temperatures in the range 1050°C to 1100°C . The deposited films were of (111) orientation. The low carrier mobility ($20 - 30 \text{ cm}^2/\text{volt-sec}$) in the films, the low minority carrier lifetime ($1 - 2 \mu\text{sec}$) as well as the broadening of the optical absorption edge were attributed to the large density of crystallographic defects in the films.

The effective surface state density at the Si/evaporated SiO_x interface was found to be of the same order of magnitude ($3 - 4 \times 10^{11} \text{ cm}^{-2}$) as that at the Si/thermally grown SiO_2 interface. The surface potential of the Si/evaporated SiO_x structure was also found to be particularly susceptible to water vapour and contamination by sodium indicating that the evaporated SiO_x layers do not provide good passivation of the silicon surface in spite of the low surface state densities observed.

The silicon TFTs exhibited transconductances in the range of 50 to 100 μmho . These low values were attributed to the low effective surface mobility which is most probably due to the large density of defects in the silicon films. The observed effective mobilities were between 5 - 10 $\text{cm}^2/\text{volt-sec}$ as compared to 100 - 200 $\text{cm}^2/\text{volt-sec}$ for a typical MOS transistor.

Surface traps were found to affect the behavior of the devices at low gate voltages and the carrier mobility was dominated by surface scattering effects at high gate voltages. The characterization of the traps by a method which involves measurements of the source-drain conductance, its temperature dependence and its transient response was discussed.

The instabilities observed in the characteristics when the devices were exposed to the ambient atmosphere are common to insulated-gate field-effect transistors and are attributed to the insulating oxide layer. These instabilities were more pronounced in evaporated SiO_x due to the hygroscopicity of the oxide.

The first objective of any further work on the silicon TFTs should be an investigation of the parameters affecting the quality of the silicon films deposited on sapphire substrates and the determination of the best combination of these parameters to obtain high carrier mobility in the films. Methods of stabilizing the devices and making them insensitive to contamination from the ambient should also be investigated.

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