DEVICES EMPLOYING CONDUCTIVITY MODULATION IN SEMICONDUCTOR FILMS BY FERROELECTRIC POLARIZATION CHARGING

by

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ABSTRACT

Two types of devices employing ferroelectric modulation of a semiconductor thin-film have been realized and studied. The first consists of a cadmium selenide film with electrodes deposited on a barium titanate substrate together with a switching electrode on the other side of the substrate. This gives a two-valued resistor; in effect, a nondestructive read-out of the state of the ferroelectric crystal which is regarded as a storage element. The second device is a thin-film transistor (TFT) deposited on a barium titanate crystal. A fourth counterelectrode on the other side of the crystal allows changing between two opposite polarization directions in the crystal, thus giving a TFT with two sets of characteristics, roughly equivalent to a two-valued built-in gate bias.

The read-in, or switching time, of the device is substantially determined by the barium titanate crystal and can be in the microsecond range for high switching fields. Readout of the devices can be continuous or not, as desired.

Characteristics of the TFT, which is considered equivalent to a two-gate device, are analyzed in terms of the gradual channel approximation. Experimental results of the two devices are presented and discussed in relation to the predicted behaviour.

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LIST OF SYMBOLS

A_d	domain wall area
2a	width of antiparallel domain step
B	magnetic field strength (Kilogaus)
b	lattice constant parallel to the plane of the crystal
C_g	gate capacitance per unit area
c	antiparallel domain step thickness
D_n	normal component of electric displacement (coulombs/cm.^{2})
D_l	trapping energy level (eV)
d	thickness of crystal
E_c	energy level of conduction band (eV)
E_{co}	coercive field strength
E_D	Electric field strength between source and drain (assume constant)
E_F	Fermi level energy (eV)
E_n	normal component of electric field
E_T	energy difference between trapping level and Fermi level (eV)
E_v	energy level of the valence band (eV)
E_x	field strength at any point x between source and drain
e	electronic charge
g_m	transconductance
h	thickness of the semiconductor layer
I_D	source-drain current
i_{max}	maximum current level of switching pulse
$i_s(t)$	switching current at time t
i_∞	experimentally determined constant of the equation

K_v	constant of the domain velocity equation
k	Boltzman constant
L	length of source-drain channel
L'	reduced channel length due to "pinch-off"
L_D	the Debye length
l	height of antiparallel domain step
N_D	electron demarcation level
N_o	the initial charge concentration in the semiconductor (el./cm.^{2})
N_T	concentration of traps
$\Delta N(x)$	electronic charge induced into the S-D channel at any point x (el./cm.^{2})
$\vec{n}$	unit vector normal to the surface of the capacitor
n	electron concentration per unit area of the semiconductor film (assumed constant)
n_b	bulk electron concentration in the semiconductor (el./cm.^{3})
n_c	concentration of conduction band electrons (el./cm.^{2})
n_T	concentration of filled traps
n(x)	electron concentration in the S-D channel at a point x from the source (el./cm.^{2})
$\frac{dn}{dt}$	nucleation rate of new antiparallel domains
P_D	hole demarcation level
P_r	remanent polarization (coul./cm.^{2})
P_{rn}	normal component of remanent polarization (coul./cm.^{2})
$P_r$eff	amount of P_r effective in causing conductivity modulation
R_H	Hall constant
S	capture crosssection of a trapping centre for electrons

t_{ox}	thickness of insulator layer
t_s	length of current pulse caused by polarization reversal
t_∞	experimentally determined constant
ΔU	energy change due to nucleation
U^*	critical activation energy for nucleation
U_1^*	critical activation energy for nucleation of a step 1 unit cell wide
U_d	depolarizing energy
u	thermal velocity of carriers
V_D	source-drain voltage
V_G	applied gate voltage
V_n	volume of nucleus
V_p	"pinch-off" voltage necessary to saturate the I_D-V_D characteristics
V_s	potential difference between the surface and bulk of the semiconductor
V_T	threshold gate voltage needed for the onset of S-D current
$V(x)$	potential at any point x in the S-D channel
v	reduced potential in the semiconductor (eV/kT)
v_d	domain wall velocity
W	width of S-D channel
W_o	activation energy of conductivity
α	activation energy for polarization reversal
γ	fraction of P_r effective in causing conductivity modulation
ε_a	dielectric constant parallel to the plane of the crystal

ε_o	permittivity of free space
ε_{ox}	permittivity of the SiO_x layer
ε_r	dielectric constant of material being considered
μ_n	mobility of electrons ($cm.^2$/volt-sec.)
ρ	charge density in the semiconductor ($el./cm.^3$)
σ	conductivity
σ_n	S-D channel conductivity
σ_o	experimentally determined constant of the equation
σ_p	constant of the equation
σ_ω	wall energy per unit area
τ_T	time constant of trapping level

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1. BASIC PRINCIPLE OF DEVICES

The purpose of the work described in this thesis was the study of nondestructive readout of the polarization state of ferroelectric crystals. Possible methods include optical techniques (Ayers, 1967), (Yan, 1964), pyroelectric effect, (Chynoweth, 1960), and conductivity modulation of a semiconductor thin-film deposited on the ferroelectric crystal. The latter is the method to be investigated here.

A ferroelectric crystal has a remanent polarization $\vec{P_r}$, the direction of which can be altered by the application of an electric field. This implies that, for a parallel plate capacitor with a ferroelectric dielectric, the charge per unit area on the electrodes is non-zero for zero applied voltage, and is instead equal to $\vec{P_r}.\vec{n}$, where $\vec{n}$ is a unit vector normal to the capacitor surface. The direction of $\vec{P_r}$, and thus the amount of surface charge, can be reversed by application of a switching voltage pulse.

If a semiconducting layer with ohmic contacts is used as one of the electrodes of the capacitor, then the amount of charge in the semiconductor will vary as the ferroelectric is switched by an amount equal to $2P_r$ per unit area, if $\vec{P_r}$ is perpendicular to the capacitor surface. Thus the direction of polarization (i.e. the state of the ferroelectric) can be determined by measuring the conductivity of the semiconductor film. It is possible to fabricate semiconductor layers with a concentration of carriers per unit area small with respect

to the ferroelectric remanent polarization of some crystals. This would seem to ensure a large conductivity change. In practice, trapping of charge by surface states and impurities in the semiconductor, mobility changes due to changes in charge concentration, and other effects complicate the behaviour.

If an insulating layer and gate are added to the semiconducting film with electrodes, a thin-film transistor is formed. This device is expected to have two sets of characteristics which differ in zero gate voltage current level, depending on the polarization direction of the ferroelectric crystal.

The devices discussed provide continuous non-destructive readout of the state of the ferroelectric substrate. The read-in or storage time is a function of the switching time of the ferroelectric crystal itself, and for high switching field strengths can be in the microsecond range.

2. THEORY OF DEVICES

2.1 Field Effect

Conductivity modulation of a sample of semiconductor by an electric field perpendicular to its surface is known as field effect. Early references to this effect include those of Lilienfeld, 1933 and Heil, 1935.

Shockley and Pearson, 1948 observed field effect modulation in a germanium film due to a charged field plate parallel to the germanium surface, similar to the case shown in Figure 2-1. In effect, the semiconductor acts as one plate of a capacitor. The electric displacement D_n of the capacitor system can be described by equation 2-1:

$$D_n = \varepsilon_o \varepsilon_r E_n \qquad (2\text{-}1)$$

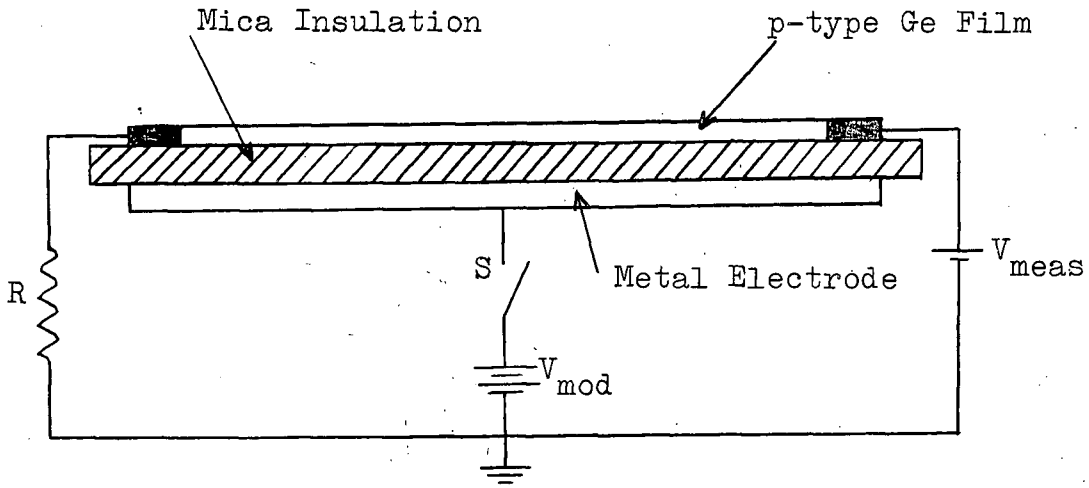


Figure 2-1. Modulation of Conductance by Field Effect

where D_n is the electric displacement normal to the surface,

ε_o is the permitivity of free space,

ε_r is the dielectric constant of mica,

and E_n is the electric field normal to the surface.

Thus for a given applied field E_n, the electric displacement is known in terms of the surface charge on the capacitor plates. This field-induced charge, if mobile, will take part in the conduction process. In the particular case shown in Figure 2-1, closing of the switch S will repel holes from the p-type germanium, thus reducing the current through it.

The current modulation observed by Shockley and Pearson was only a small fraction of that expected. The discrepancy was interpreted as evidence for the existence of surface states capable of trapping the induced charge.

Field effect modulation has also been observed by using a ferroelectric insulator between the capacitor plates. An early reference is that of Godefroy, 1952, who observed measureable field effect modulation in tellurium evaporated onto ceramic barium titanate. For the case of a ferroelectric insulator, equation 2-1 is modified to form equation 2-2:

$$D_n = \varepsilon_r \varepsilon_o E_n + P_{rn} \qquad (2\text{-}2)$$

where ε_r is the relative dielectric constant of the ferroelectric,

and P_{rn} is the remanent polarization of the ferroelectric normal to the surface.

Field effect modulation of conductivity can be observed even with no applied field since the direction of P_r can be changed by a voltage pulse applied across the ferroelectric.

Stadler, 1965, observed a conductance change of 2% in 100A° thick gold films on single crystal barium titanate after reversing the polarization direction. Moll, 1963 and Zuleeg and Wieder, 1966, described an active device with variable gain and remanent memory. This device, shown in Figure 2-2, consisted of a cadmium sulphide insulated gate field effect transistor, similar to that developed by Weimer, 1962, deposited

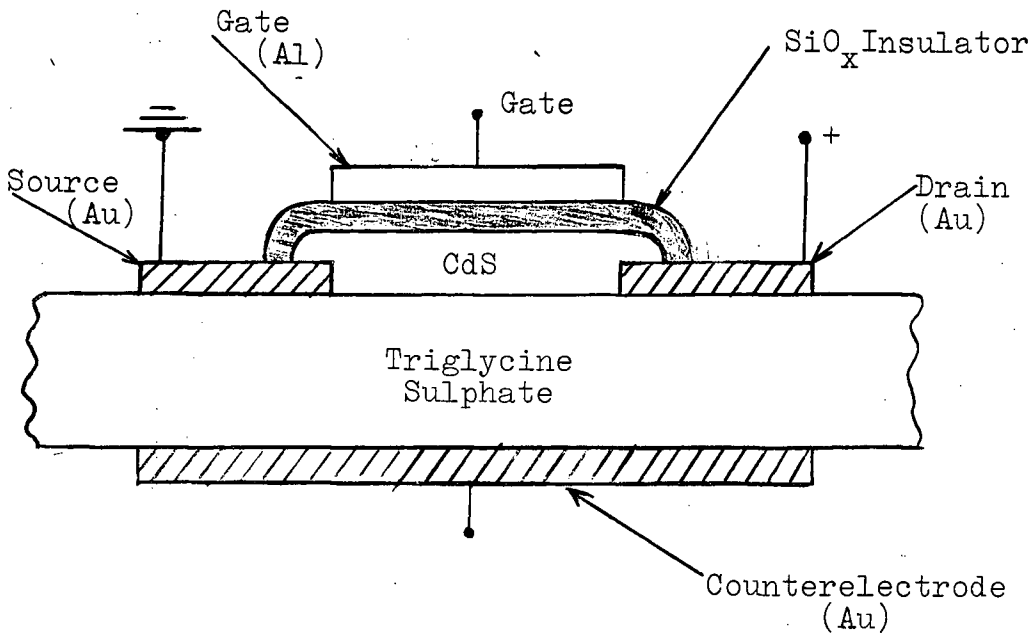


Figure 2-2. Cadmium Sulphide TFT on Triglycine Sulphate (Moll)

on a ferroelectric substrate of triglycine sulphate with a counter electrode on the other side. Moll, 1963 observed a resistance variation of 25%, as the polarization was reversed, for a resistance of 60KΩ between source and drain. Finally, Heyman and Heilmeier, 1966, described a variable resistor using p-type tellurium between ohmic contacts on triglycine sulphate, with a counterelectrode on the other side of the ferroelectric substrate.

In the work to be reported here, cadmium selenide was used as the semiconductor, and barium titanate as the ferroelectric substrate, to form an active device with memory storage. Passive devices with variable resistance are also described using cadmium sulphide and cadmium selenide films deposited on barium titanate.

2.2 Two-State TFT-Structure and Operation

The basic structure of the active device to be considered is shown in Figure 2-3. It consists of a thin film of n-type cadmium selenide deposited onto a barium titanate substrate. Aluminum source-drain electrodes are then evaporated onto the cadmium selenide, followed by an insulating layer of silicon oxide and an aluminum gate electrode. The device operates by modulation of the cadmium selenide film conductivity by both the gate and the ferroelectric substrate. Essentially, therefore, the device can be considered as a two-gate TFT. One of the gates, the barium titanate, has only two possible settings, and the other is continuously variable.

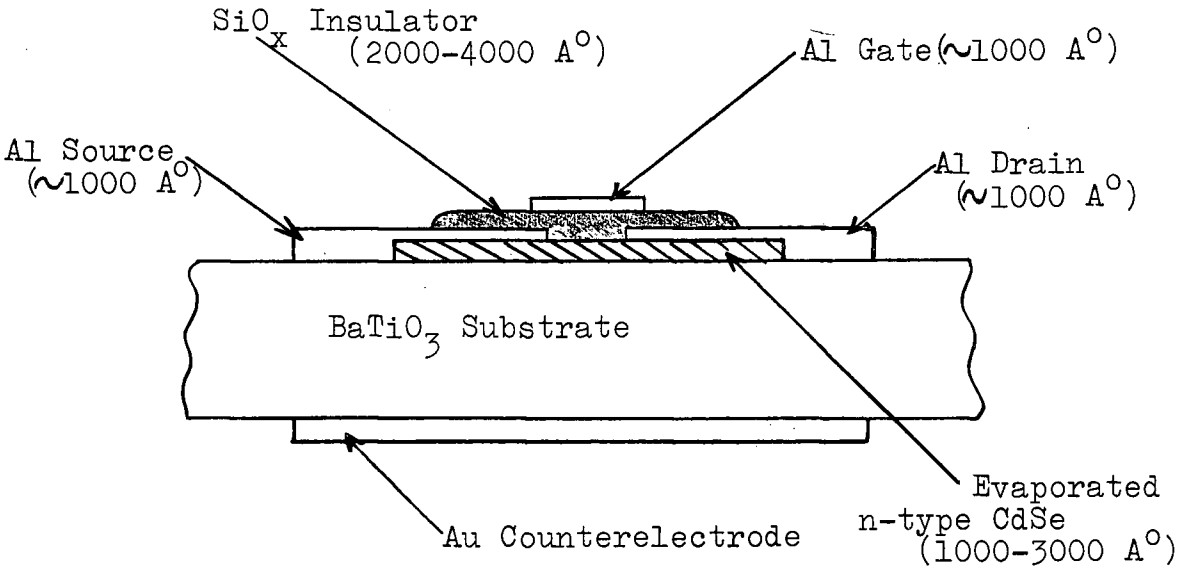


Figure 2-3. Cadmium Selenide Two-State Thin-Film Field Effect Transistor

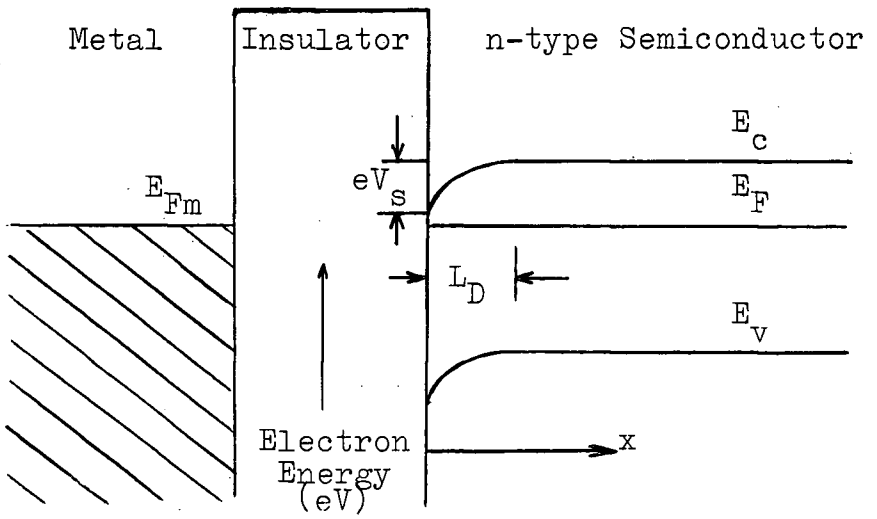


Figure 2-4. Metal-Insulator-Semiconductor Energy Level Diagram

Consider a one-dimensional model of an n-type semiconductor at thermal equilibrium with an insulator-metal contact as shown in Figure 2-4 (Many, 1965). The potential V in the semiconductor is given by Poisson's equation:

$$\nabla^2 V = -\frac{\rho}{\varepsilon_r \varepsilon_o} \qquad (2\text{-}3)$$

where ρ is the charge density in the semiconductor.

For the planar geometry shown and assuming negligible hole concentration in the semiconductor, equation 2-3 reduces to the Poisson-Boltzman equation:

$$\frac{d^2V}{dx^2} = -\frac{e}{\varepsilon_r \varepsilon_o} n_b (1-\exp eV/kT)$$

or further,

$$\frac{d^2v}{dx^2} = \frac{e^2}{\varepsilon_r \varepsilon_o kT} n_b (1-\exp v) \qquad (2\text{-}4)$$

where n_b is the semiconductor bulk electron concentration and $v = \frac{eV}{kT}$. For $v \leq \frac{1}{2}$, equation 2-4 can be approximated by equation 2-5:

$$\frac{d^2v}{dx^2} = \frac{v}{L_D^2} \qquad (2\text{-}5)$$

where

$$L_D = \sqrt{\frac{\varepsilon_r \varepsilon_o kT}{e^2 n_b}}$$

With boundary conditions: $v = v_s$ at $x = 0$, and $v = 0$ at $x = \infty$, equation 2-5 can be integrated directly to yield equation 2-6:

$$v = v_s \exp(-x/L_D) \qquad (2\text{-}6)$$

Thus L_D, the effective Debye length, is the distance into the semiconductor at which the potential v is the 1/e of its value at the surface, for small v.

The model just developed is analogous to the gate-insulator-semiconductor layer of the device to be considered. Thus, for small V, modulation of the conductivity of the semiconductor by the gate is confined to a depth in the order of the Debye length from the surface of the insulator. Similarly, conductivity modulation at the ferroelectric-semiconductor interface ends at a depth in the order of the Debye length into the semiconductor.

Table 1 gives the value of L_D for cadmium selenide with various electron concentrations.

ELECTRON CONCENTRATION	L_D
10^{16} el./cm.^{3}	416 A^o
10^{15}	1320
10^{14}	4160
10^{13}	13200

TABLE 1

Debye Length for Cadmium Selenide at Various Electron Concentrations

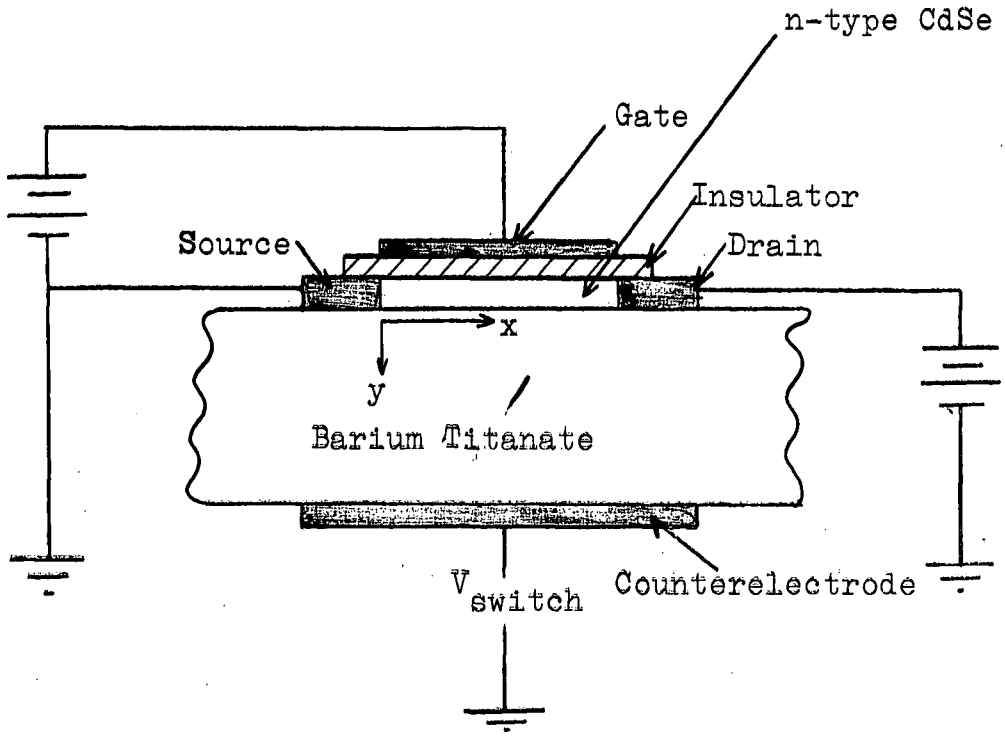
It is also necessary that the carrier concentration be kept small in order to have a large amount of carrier modulation due to the gate and ferroelectric substrate. If the carrier concentrations are too large, then the additional charges injected by the field effect will be negligible in comparison.

The structure of the two-state resistor is similar to that of the active device except the insulating layer and gate are missing. Conductivity modulation is caused only by the ferroelectric polarization change. As for the active device, modulation is greatest when the semiconductor layer has a small carrier concentration and is relatively thin.

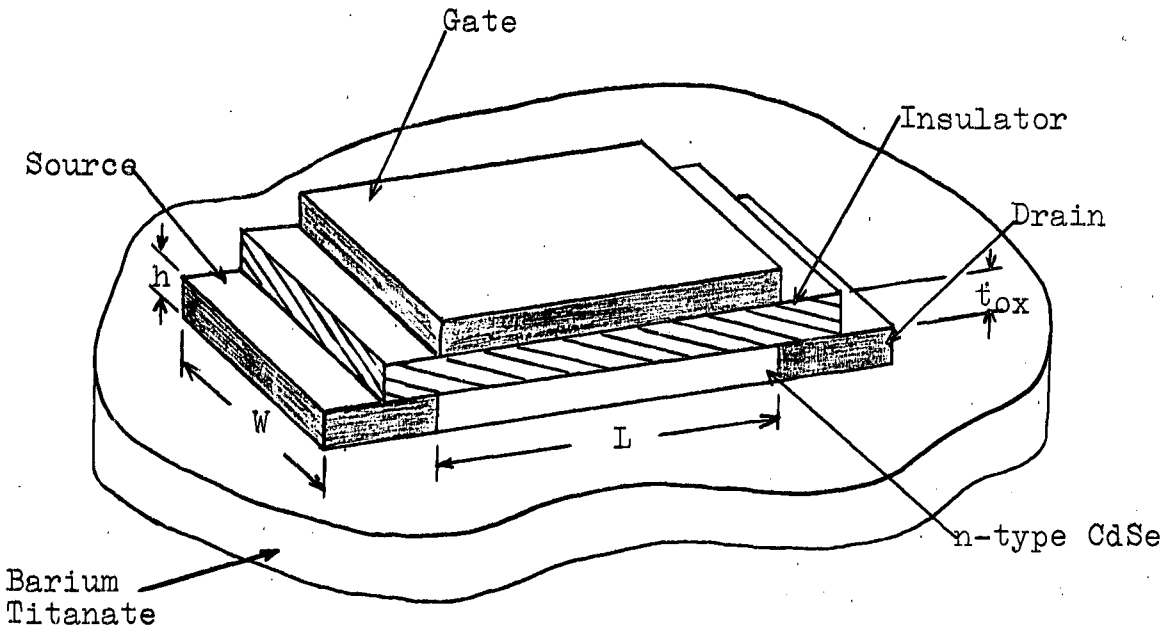
2.3 Elementary Theory of the Insulated Gate Field Effect Transistor Modified to Include the Ferroelectric Substrate

In this section, the elementary theory of the thin-film field effect transistor (Borkan and Weimer, 1966), (Weimer, 1964), is modified to include the effect of the ferroelectric substrate. It is seen that a two-state TFT results from this analysis. The following assumptions are used in this treatment of the model:

1. Carrier mobility is constant, independent of the gate or source-drain field, and of the polarization state of the ferroelectric substrate.
2. The gradual channel approximation holds. That is, the rate of change of the source-drain field is small compared to the rate of change of the gate field normal to the channel. Poisson's equation may then be solved in one dimension.



(a) Crossectional View



(b) Electrode Structure

Figure 2-5. Idealized Geometry of Cadmium Selenide Two-State Transistor

3. Trapping effects are neglected.

4. Gate capacitance is assumed constant.

5. The work function differences between the electrodes and the semiconductor are neglected. Ohmic source and drain contacts are assumed.

6. The carrier modulation at each surface of the semiconductor is assumed independent of the other.

The idealized device structure and the co-ordinate axes used in the analysis are shown in Figure 2-5. V_G and V_D represent the potentials applied to the gate and drain electrodes respectively. V(x) is the potential of the semiconductor at any point with respect to the source.

Source-drain current I_D is given by:

$$I_D = \sigma_n E_x$$

$$= e\ \mu_n\ Wn(x)\ \frac{d\ V(x)}{dx}$$

where

σ_n is the channel conductivity,

E_x is the field strength between source and drain,

μ_n is the effective mobility in the source-drain channel

W is the channel width,

n(x) is the electron concentration per unit area in the semiconductor at a distance x from the source,

and e is the electronic charge.

The charge per unit area induced into the semiconductor layer at any point x by the applied gate voltage is given by equation 2-7:

$$\Delta N(x) = \frac{C_g}{WLe} (V_G - V(x)) \qquad (2\text{-}7)$$

where C_g is the gate capacitance per unit area, $C_g = \varepsilon_{ox}/t_{ox}$.

Consider also the ferroelectric substrate which has a permanent polarization charge per unit area of $\pm P_r$, which will cause a compensating charge of $\mp P_r$ to be induced into the semiconducting layer.

Thus,

$$n(x) = \Delta N(x) + N_o \pm \frac{P_r}{e}$$

$$= \frac{1}{e}\left[\frac{C_g}{WL}(V_G - V(x))\right] + N_o \pm \frac{P_r}{e} \qquad (2\text{-}8)$$

where N_o is the initial charge concentration per unit area in the semiconductor, neglecting the effect of the ferroelectric substrate.

Substituting for n(x) in equation 2-6 and integrating from x = 0 to x = L, yields equation 2-10:

$$\int_0^L I_D \, dx = \int_0^{V_D} e \mu_n W n(x) \, dV(x)$$

$$= \int_0^{V_D} \left[\mu_n W \frac{C_g}{WL}\left[V_G - V(x)\right] + eN_o \pm P_r\right] dV(x) \qquad (2\text{-}9)$$

$$I_D = \frac{\mu_n C_g}{L^2}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \qquad (2\text{-}10)$$

where $$V_T = -\frac{N_o eWL}{C_g} \pm \frac{P_r WL}{C_g} \qquad (2\text{-}11)$$

The threshold voltage V_T is the applied voltage required for the onset of drain current. It is negative for depletion mode and positive for enhancement mode devices.

As V_D is increased, a condition occurs in which the surface concentration of carriers at a distance x from the source is zero:

$$0 = \frac{V_T C_g}{WL} + \left[V_G - V(x)\right] \frac{C_g}{WL} \qquad (2\text{-}12)$$

This condition occurs first at $x = L$ and the pinch-off voltage V_p is given by equation 2-13:

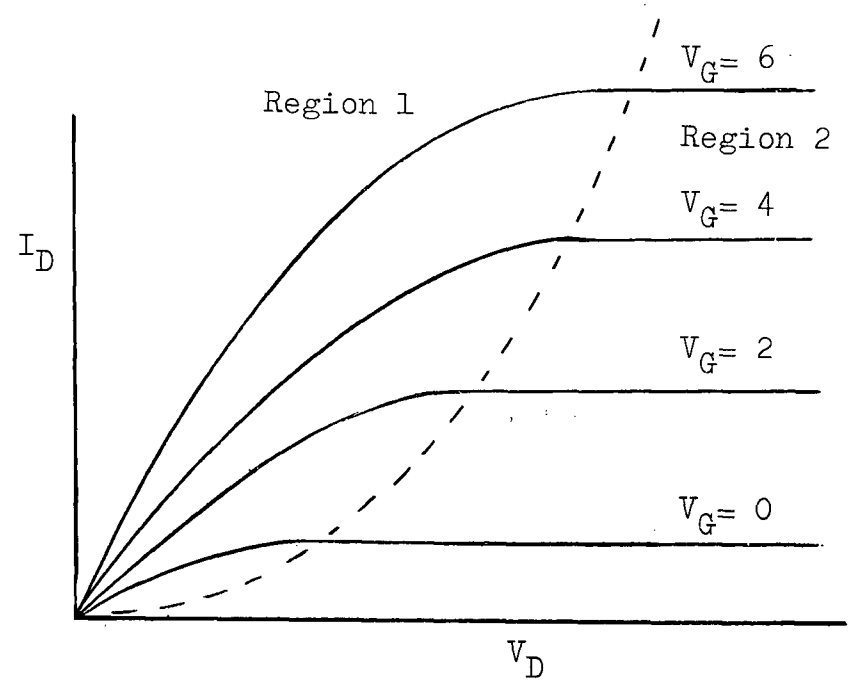
$$V_p = V_G - V_T \qquad (2\text{-}13)$$

For drain voltages greater than V_p, the gradual channel approximation no longer holds, since no channel exists over part of the source-drain region. It is assumed that the gradual channel approximation holds up to the point where $V(x) = V_p$. This occurs at L', where $L' < L$. All charge which arrives at L' is assumed to be swept across the remaining high field region to the drain.

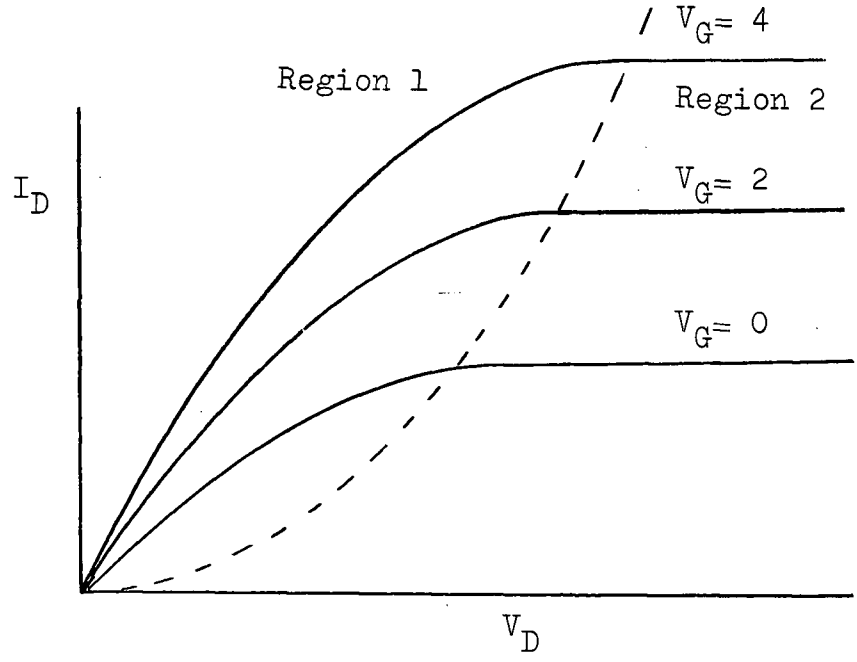
Thus, for $V_D > V_p$, equation 2-10 becomes:

$$I_D = \frac{\mu_n C_g}{2L'^2} (V_G - V_T)^2 \qquad (2\text{-}14)$$

L' is very nearly equal to L. Therefore, the characteristics of the device saturate for $V_D > V_p$.



(a) Low-State Characteristics



(b) High-State Characteristics

Figure 2-5. Representative Drain Characteristics for Two-State TFT

Figures 2-6(a) and (b) show representative I_D-V_D characteristics given by equations 2-10 and 2-13 for the two regions of the device and the two states of the ferroelectric crystal.

Transconductance of the device below saturation is given by equation 2-15:

$$g_m \triangleq \left(\frac{\delta I_D}{\delta V_G}\right)_{V_D} = \mu_n \frac{C_g V_D}{L^2} \qquad (2\text{-}15)$$

In this elementary analysis of the device, the reversal of the ferroelectric polarization charge gives two sets of I_D - V_D characteristics differing only in V_T. All other parameters of the device, including mobility and g_m, are constant.

For this device, with $V_D > V_p$, and constant gate voltage, two current levels may be observed, depending on the polarization state of the ferroelectric substrate. Thus, information about the state of the ferroelectric crystal is given by the current level of the device characteristics.

2.4 Theory of Resistance Modulation Due to Ferroelectric Substrate

The following is an elementary treatment of the theory of the two-state resistor. The device structure as described in Figure 2-4 will be assumed with the insulator and gate neglected. For a given voltage V_D across the source-drain gap, assuming ohmic contacts, the drain current I_D is:

$$I_D = \frac{V_D}{R} = \frac{V_D Wh}{L}$$

$$= ne\mu_n E_D W \qquad (2\text{-}16)$$

where $E_D = V_D/L$ is the electric field strength between electrodes, and n is the electron concentration per unit area of the semiconductor film.

Once again, assume the polarization charge at the surface of the ferroelectric is compensated by an equal and opposite mobile charge in the semiconductor. Then, $n = n_o \pm \frac{P_r}{e}$ where n_o is the electron concentration of the semiconductor assuming no polarization charge. Therefore, the current between the source and drain will be linear with voltage applied, as a resistor, and will have two values which depend on the polarization direction of the ferroelectric substrate as described by equation 2-17:

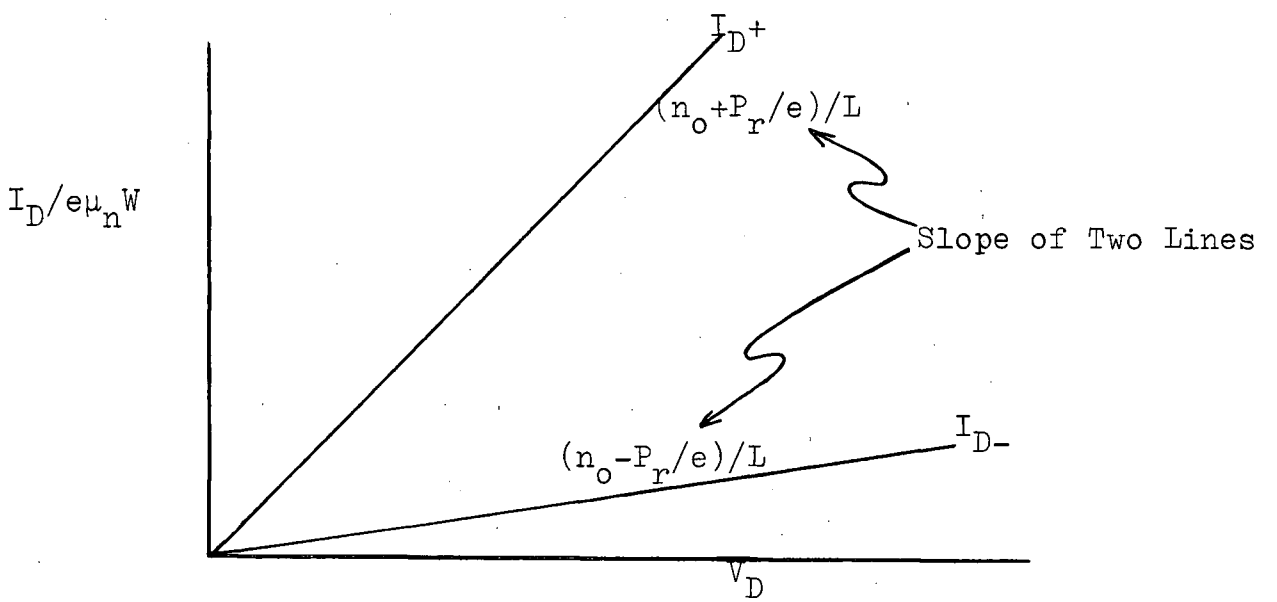


Figure 2-7. Typical Characteristics of Two State Resistor

$$I_D = ne\mu_n WE_D$$
$$= (n_o \pm \frac{P_r}{e})\, e\mu_n WE_D \qquad (2\text{-}17)$$

Note that since P_r is constant, the modulation efficiency of the device, defined by $\frac{I_{D^+}}{I_{D^-}}$, is inversely proportional to n_o. This device may also be used to give non-destructive readout of the state of the ferroelectric crystal. In this case, the state of the crystal is determined by the resistance level of the device.

2.5 Effect of Traps on Proposed Devices

Both within the semiconductor and at its surface there exist centres which can capture one or more electrons from the conduction band. If the captured electron has a high probability of returning to the conduction band rather than recombining with a hole, the centres act as traps (Bube, pg. 273). If there are several levels of centres between the conduction and valence bands, those close to the conduction band act as traps while those further away are recombination centres, since there is a higher probability of combining with a hole than of returning to the conduction band. It is possible to define an electron demarcation level N_D between the two types of centres (Rose, Pg. 28). At this level, the probability of an electron returning to the conduction band and of recombining with a hole is equal. There also exists an equivalent demarcation level for holes, P_D.

The demarcation levels shown in Figure 2-8 hold for only one specific equilibrium condition. As the Fermi level moves, N_D and P_D must change also.

Surface states often act as trapping centres and may be so numerous as to seriously affect the performance of field effect devices such as are considered here (Weimer, 1964). Consider the case where the ferroelectric polarization direction is reversed suddenly to increase the electron concentration in the semiconductor. The charge induced into the semiconductor goes initially into the conduction band. Over a period of time, some of this charge is removed from the conduction band to fill traps. Thus, the carrier concentration decreases until a steady state level is reached where the number of traps being filled equals the number emptying back into the conduction band.

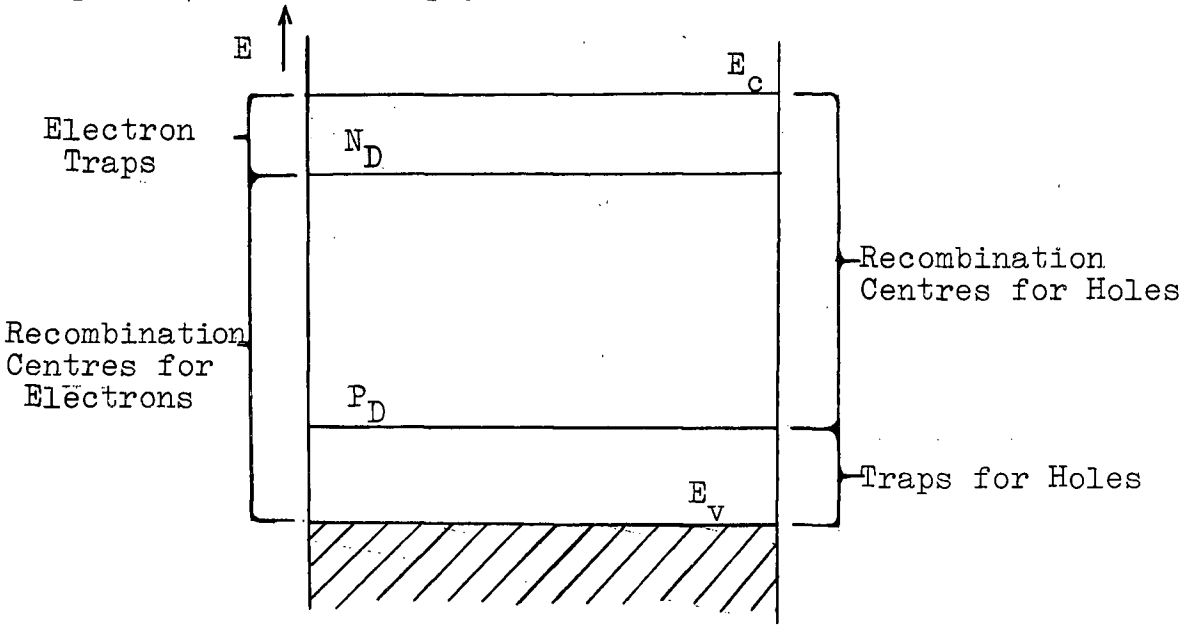


Figure 2-8. Demarcation Levels in Semiconductor

If the number of traps is large, almost all of the induced charge may be trapped.

The kinetics of the trapping process are governed by an equation of the form:

$$\frac{\delta n_T}{\delta t} = uSn_c(N_T - n_T) - Kn_T \exp(-E_T/kT) \qquad (2\text{-}18)$$

where u is the thermal velocity of the carrier ($u = \sqrt{2k\pi n}$),

S is the capture cross section of the centre for electrons,

n_c is the concentration of conduction band electrons,

n_T is the concentration of filled traps,

N_T is the concentration of trapping levels,

E_T is the energy between the trap level and the conduction band,

and K is a constant of proportionality.

A single electron trapping level will give an exponential time variation in carrier concentration, the time constant of which is given by:

$$\tau_T = (uSN_T)^{-1}$$

However, in most materials, several trap levels are present and the change in carrier concentration with respect to time becomes the sum of many exponentials.

For the case of the proposed devices, a large surface state density at the semiconductor-insulator interface is expected for several reasons. Tamm states, (Tamm, 1932),

which are due to a termination of the periodic potential of the crystal lattice at the semiconductor surface, may be present. Also, there may be a large concentration of impurities on the ferroelectric crystal before the semiconductor film is deposited, due to electrostatic attraction between the ferroelectric crystal and impurity atoms present in the atmosphere. These contaminants, being in intimate contact with the ferroelectric surface, would have very fast trapping time constants, similar to the fast states found in germanium (Heiman and Warfield, 1965).

3. FERROELECTRIC AND RELATED PROPERTIES OF BARIUM TITANATE

3.1 Ferroelectricity

A ferroelectric crystal is defined as one which exhibits a spontaneous electric dipole moment or polarization, the direction of which may be altered by application of an electric field (Dekker, Pg. 184). Total polarization P is related to applied electric field E by a hysteresis loop as in Figure 3-1.

In general, the direction of spontaneous polarization, known as the polar axis, is not the same throughout the crystal. A number of individual domains may exist with different polarization directions which depend on the crystal structure of the material. If a macroscopic sample with zero initial net polarization is considered, application of an electric field will cause the net polarization to increase as the various domains tend to line up with the applied field. This process corresponds to the curve OAB in Figure 3-1. When all domains are aligned with the applied field, further increases in P are small and due only to induced polarization effects.

Ferroelectrics are so named because of the analogy between the P-E hysteresis loop of Figure 3-1 and the B-H loop of ferromagnetic materials (Megaw, Pg. 1). The permanent dipole moment of ferroelectric crystals disappears above a certain temperature T_C, which is known as the Curie temperature. Ferroelectrics are characterized by a non-centric crystal structure with a unique

P polarization(coulombs/cm.^{2})
E electric field(volts/cm.)
E_{co} coercive field
P_r remanent polarization

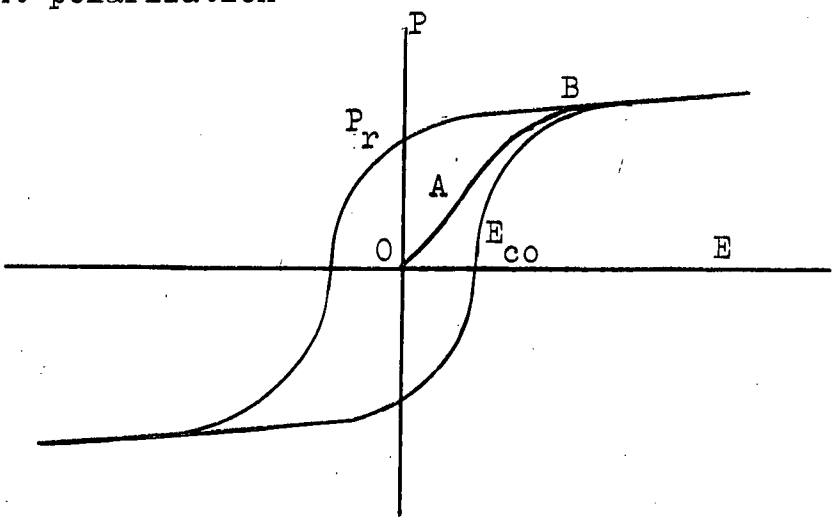


Figure 3-1. Ferroelectric Hysteresis Loop

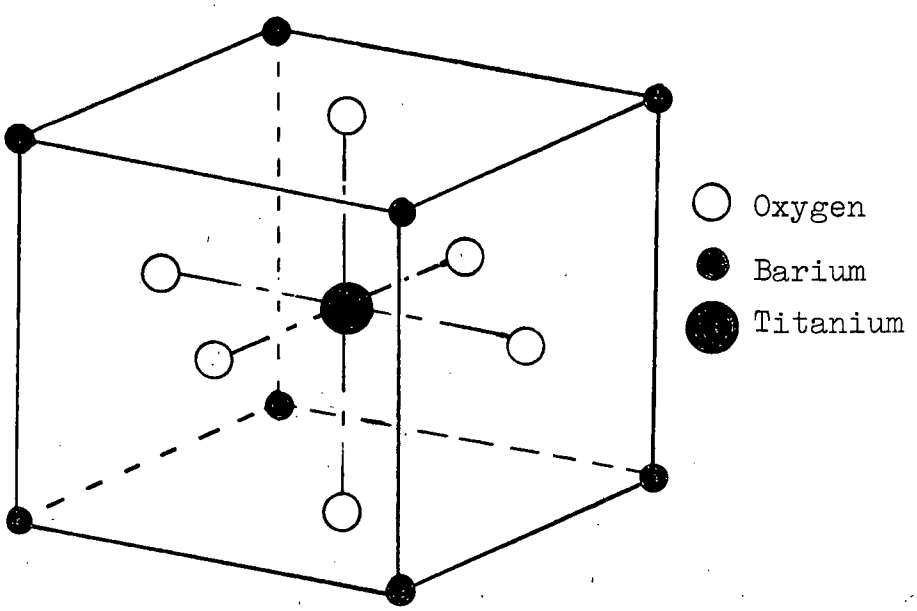


Figure 3-2. Cubic Perovskite Structure of Barium Titanate

polar axis which can be reversed by an electric field. Above the Curie temperature, the crystal class changes to one of higher symmetry.

In their ferroelectric phase, ferroelectric crystals exhibit both pyroelectric and piezoelectric properties.

3.2 Physical Properties of Barium Titanate

Barium titanate, although only discovered to be ferroelectric in 1945-46, (Wul and Goldman, 1945), (Von Hippel, 1946) has since been widely investigated. Its stability, both mechanical and chemical, a large remanent polarization, and a Curie temperature of over 100°C are some of the reasons for the interest shown barium titanate, especially for practical device applications. The atomic structure of the perovskite crystals, of which barium titanate is the best known, is much simpler than that of other ferroelectrics. Thus, research into the basic phenomenon of ferroelectricity has included much work with barium titanate (Devonshire, 1954).

Barium titanate is crystalline, clear to dark brown in colour depending on the amount of iron dopant present, and has a high refractive index. The Curie temperature is near 120°, the exact transition temperature being dependent on the crystal impurities. The non-polar phase of barium titanate is cubic (point group m3m) and has the cubic perovskite type structure, a unit cell of which is shown in Figure 3-2.

Below the Curie temperature, the crystal becomes tetragonal (point group 4mm). The tetragonal axis may have three possible orientations, which are along one of the three

pseudo-cubic axes. Also, the polar axis, which is parallel to the tetragonal c axis, may be in either direction along the axis. The tetragonal c axis is about 1% longer than the other two. This causes mechanical stresses to occur in the crystal between different domains (Megaw, Pg. 65). In an equilibrium condition, the polar axis lies in a direction to minimize stresses, both mechanical and electrical, on the crystal. Small areas within the crystal tend to align themselves together to form domains, since, over a small area of the crystal, stress conditions are the same. Thus, the ferroelectric domain structure of barium titanate can be very complex, with various individual domains aligning themselves in any one of six possible directions.

Further crystallographic phase changes occur in barium titanate at 5°C and -90°C (Jona and Shirane, Pg. 109). The crystal remains ferroelectric but with reduced remanent polarization.

3.3 Polarization Reversal

3.3.1 Introduction

Unlike uniaxial ferroelectrics such as Rochelle salt and triglycine sulphate (TGS), it is possible to change the direction of polarization of a single domain of barium titanate by either 90° or 180°. Of the two, 180° switching or polarization reversal has been studied most, since many practical applications of barium titanate involving information storage make use of the effect of polarization reversal (Anderson, 1952), (Anderson, 1956), (Campbell, 1957).

Most barium titanate single crystals are grown by the Remeika method (Remeika, 1954). The growth habit of the crystals is such that triangular plates with one pseudo-cubic axis perpendicular to the plane of the plate are formed. When the polar axis of a domain is normal to the crystal surface, the domain is said to be c-domain; when parallel to the surface, the domain is a-domain (Hooton and Merz, 1954). One can differentiate between the two polar directions of a c-domain by using the notation c^+ and c^-, depending on the direction of the polar axis with respect to the top of the crystal.

180° switching usually involves reversing the direction of polarization in a c-domain crystal by application of an electric field opposite to the existing polarization direction.

3.3.2 Mechanism of Polarization Reversal in Barium Titanate

The thermodynamic theory of barium titanate switching developed by Devonshire (Devonshire, 1949, 1951) predicted the general shape of the P-E relationship found experimentally. However, the predicted coercive field was several orders of magnitude above that obtained experimentally. It was therefore assumed that polarization reversal took place in a small area of the crystal first, then spread out, rather than the whole crystal reversing its polarization state at once as required by the thermodynamic theory, since the energy requirements are much lower for this process than for a total instantaneous change.

Merz, 1954 and Little, 1955 both reported polarization reversal to occur by the formation of small anti-parallel domains

on the crystal surfaces which then grew through the crystal to form spikes as shown in Figure 3-3.

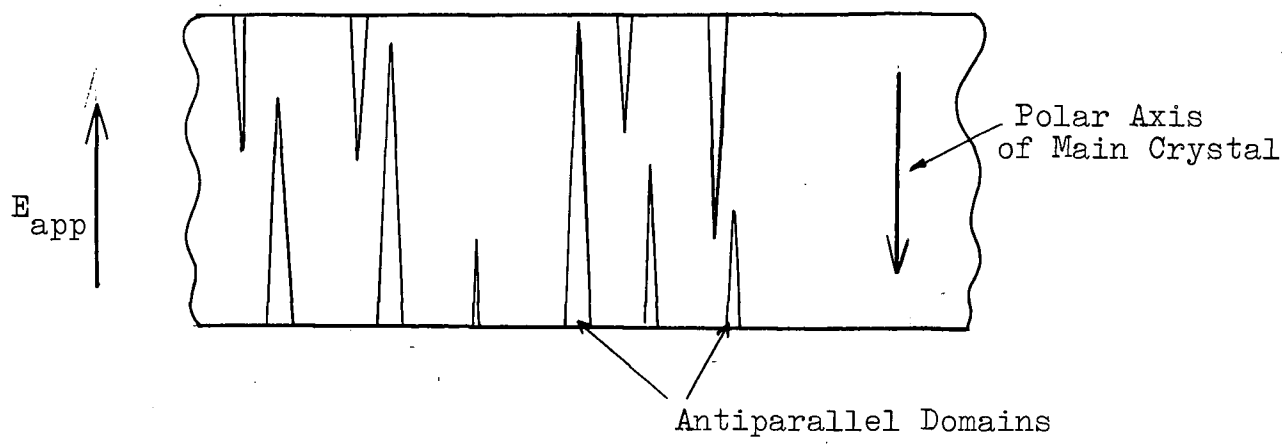


Figure 3-3. Polarization Reversal of Barium Titanate

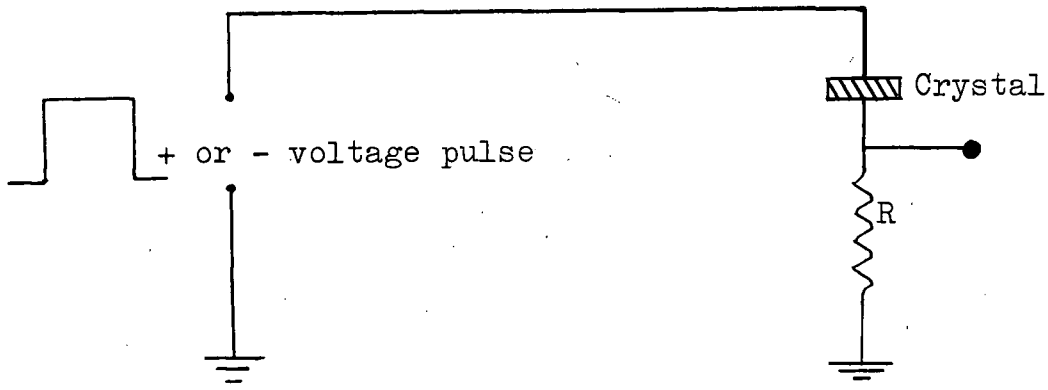
The first published data on the rate of polarization reversal and time of reversal was presented by Merz, 1954. The switching current was recorded as a voltage drop across a resistor in series with the switching voltage source as shown in Figure 3-4(a). Metal electrodes were used on the crystals. Figure 3-4(b) denotes a typical response curve of a crystal in the c^- state to a positive voltage pulse. Figure 3.4(c) represents the response of the crystal to a second positive voltage pulse. At low field strengths, (2 Kv./cm. or less) the experimental results of Merz can be fitted to equations of the form:

$$i_{max} = i_{\infty} \exp(-\alpha/E) \qquad (3\text{-}1)$$

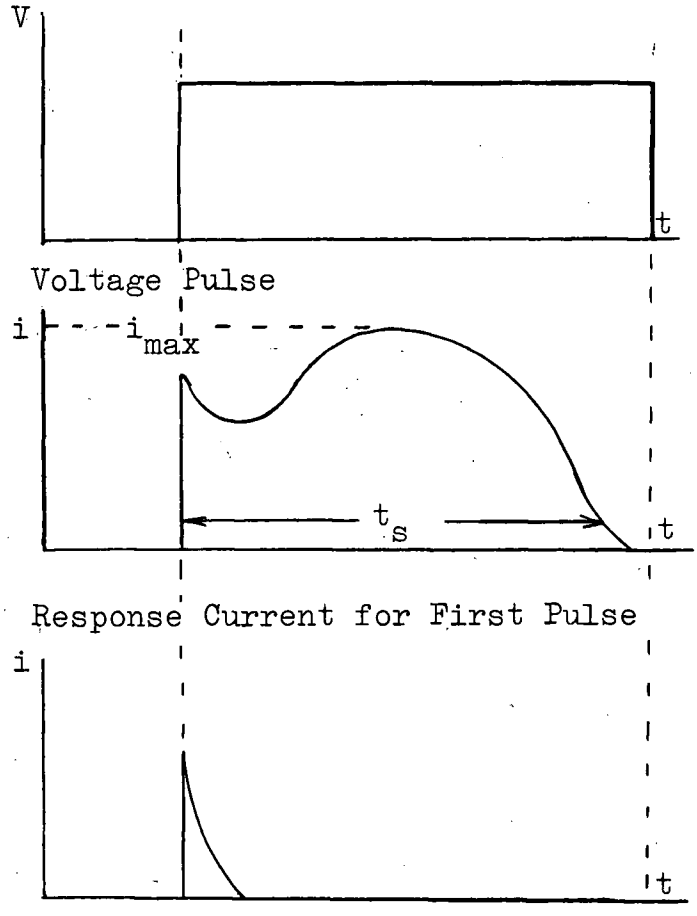
and

$$1/t_s = 1/t_{\infty} \exp(-\alpha/E) \qquad (3\text{-}2)$$

i_{∞} and t_{∞} are the current and switching time respectively for an infinite field strength E,



(a) Switching Circuit of Merz



(b) Voltage Pulse

(c) Response Current for First Pulse

(d) Response to Second Pulse

Figure 3-4. Voltage Pulse Switching (Merz)

and α is termed the switching activation energy and is 1V./cm. for the samples of Merz. Switching times as fast as .2 μseconds were observed for crystals 5 x 10^{-3} cm. thick.

Stadler, 1958, 1962 extended the work of Merz to higher values of field strength and found that for fields up to 100 Kv./cm. equation 3.3 was valid:

$$1/t_s = 1/t_\infty E^{1.4} \qquad (3\text{-}3)$$

A theoretical model of polarization reversal which assumes motion of 180° domain walls, developed by Miller and Weinreich, 1960, gives results which are consistent with much of the published experimental data. The model assumes that nucleation of antiparallel domains controls domain wall motion. That is, nucleation of new antiparallel domains occurs at the wall boundary preferentially and causes domain wall propagation. This theory, which is developed in Appendix I, yields expressions for nucleation rate $\frac{dn}{dt}$, and domain wall velocity v_d, of the form:

$$\frac{dn}{dt} = K_1 \exp - \alpha/E \qquad (3\text{-}4)$$

and

$$v_d = K_2 \exp - \alpha/E \qquad (3\text{-}5)$$

where K_1 and K_2 are independent of E.

These expressions hold for low field strengths (<3Kv./cm.). For higher field strengths, the derivations of Miller and Weinreich were extended by Stadler and Zachmandis, 1964 and yielded expressions of the form:

$$\frac{dn}{dt} = K_3 E^{1.4} \qquad (3\text{-}6)$$

and $$v_d = K_4 E^{1.4} \qquad (3\text{-}7)$$

where K_3 and K_4 are also independent of E.

Stadler and Zachmandis, 1964 also observed experimentally the high field nucleation rate and domain wall velocity and found the same power dependence on E as derived from the Miller-Weinreich theory.

While the theory of polarization reversal is by no means complete, the mechanism of polarization reversal proposed by Miller and Weinreich is promising as a basis for formulating a more complete theory of switching behaviour.

3.4 Experimental Procedure and Results

3.4.1 Crystal Preparation

The barium titanate crystals used were thin triangular plates 0.2 to 0.4 mm thick. They were commercially grown by a modified Remeika process.* The crystals were cleaned by etching for 10-15 minutes in 85% by volume H_3PO_4 at a temperature of 140-160°C, then rinsed in distilled and deionized water. Longer etching periods were used at times to further reduce crystal thickness. The etching was carried out above the Curie temperature in order to prevent preferential etching of the various domains (Hooton and Merz, 1955).

In most cases, no effort was made to obtain single domain crystals before electrode deposition. However, the crystals could be 'poled' to the "c" state by placing the crystals between electrodes in deionized water and applying a

*Semi-Elements Inc. Purity of crystals $>$ 99.95%

large alternating voltage (Campbell, 1957). There was a tendency following this treatment for some of the crystals to revert to a polydomain state because of stresses within the crystal. Circular electrodes of aluminum or gold were deposited on the crystals using standard vacuum deposition techniques in a Veeco vacuum system. Deposition pressures were in the 10^{-5} - 10^{-6} torr. range.

For most measurements, aluminum electrodes were used since they were more durable. However, gold electrodes were used in some instances to ensure good contacts.

3.4.2 Conductivity of Crystals

The conductivity of prepoled samples with circular aluminum electrodes was measured at low field strength. The simple circuit used to determine sample resistance is shown in Figure 3-5. The voltage was applied so as not to reverse the domain polarization direction. Conductivity of the crystals was found to vary between 1.0×10^{-9} and 2.0×10^{-10} Ω-cm. for

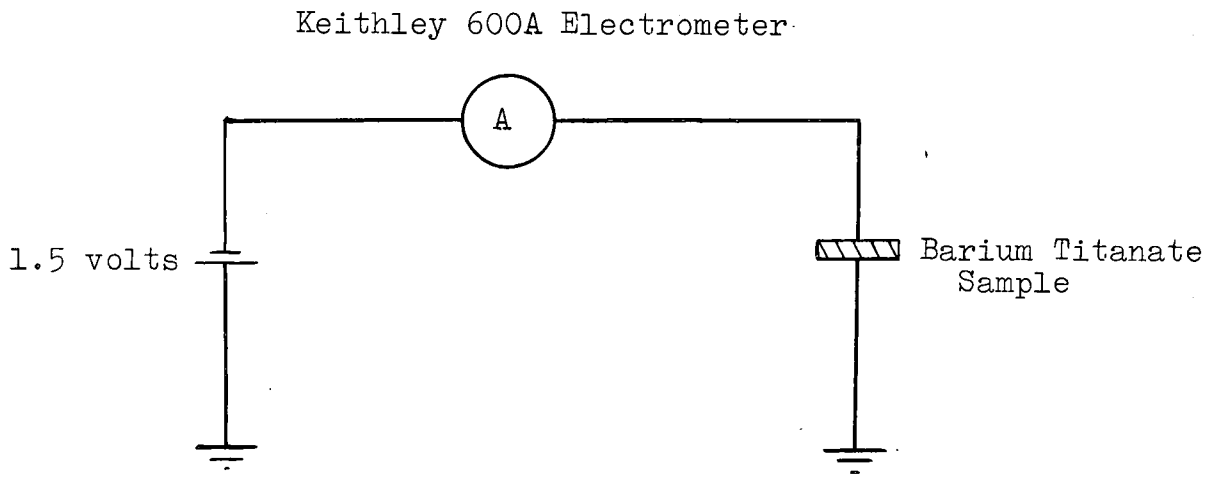


Figure 3-5. Conductivity Measurement of Barium Titanate Crystals

samples .17 to .32 cm. thick. This compares favourably with previously quoted values (Jona and Shirane, pg. 182).

3.4.3 Measurement of Remanent Polarization

In order to observe the P-E hysteresis loop of the crystals, the modified Sawyer-Tower, 1930 circuit of Figure 3-6, was used. The voltage across the crystal was measured directly by the X deflection of the oscilloscope. The polarization of the crystal, proportional to the voltage across the linear capacitor C_o, is measured by the Y deflection of the oscilloscope. The crystal holder was designed to minimize stray capacitance.

The P-E hysteresis loop of crystal #1 is shown in Figure 3-7 at various frequencies. In Table II are given the values of P_r and E_{co}, calculated for crystals #1 and #4 at various frequencies.

X_{TAL} #1 thickness: .21mm. Electrode area: 3.0mm.^{2}

X_{TAL} #4 thickness: .15mm. Electrode area: 3.0mm.^{2}

	Frequency cps.	10	100	250
X_{TAL} #1	P_r μcoul./cm.^{2} ±5%	23.6	22.2	21.0
	E_{co} volts/cm. ±5%	2000	2350	2750
X_{TAL} #4	P_r μcoul./cm.^{2} ±5%		24.8	
	E_{co} volts/cm. ±5%		2400	

TABLE II

Summary of P-E Hysteresis Loop Measurements at Various Frequencies

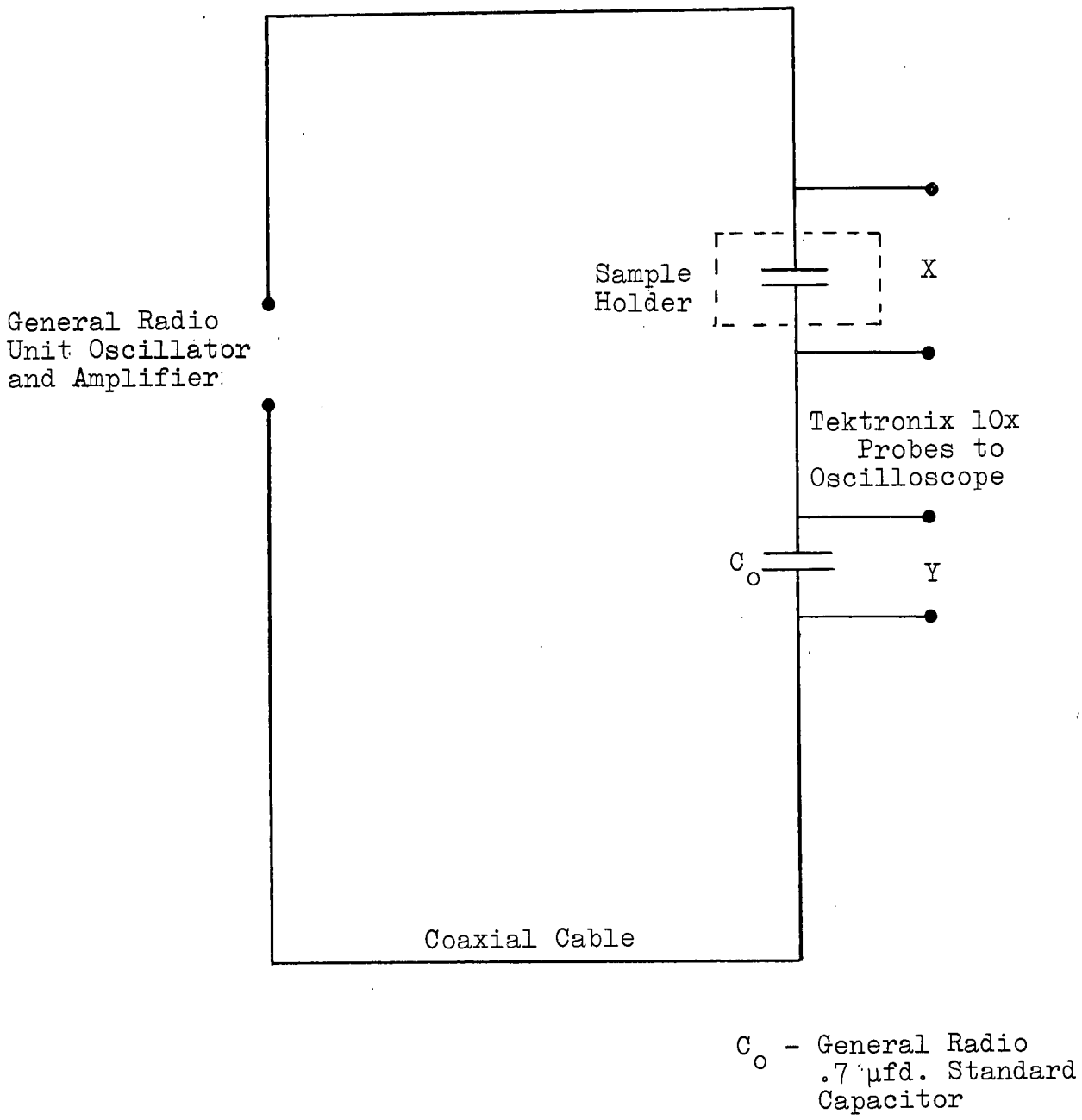
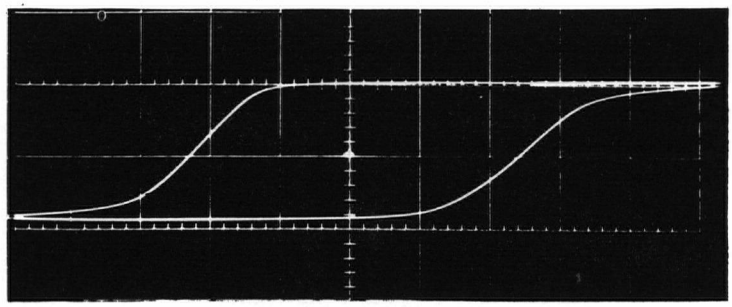
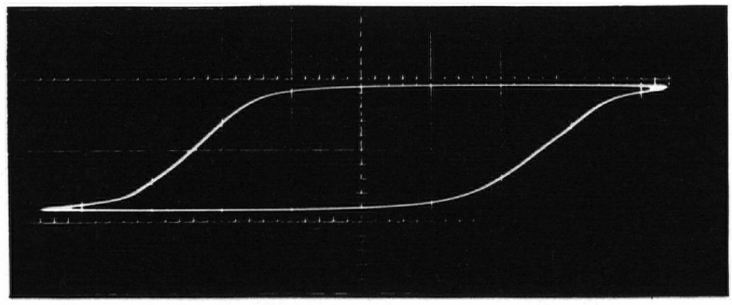


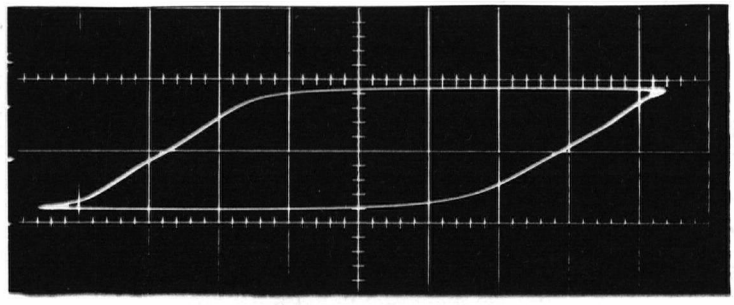
Figure 3-6. Sawyer—Tower Circuit to Determine Remanent Polarization



(a) Measurement Frequency 10 c./s.



(b) Measurement Frequency 100 c./s.



(c) Measurement Frequency 250 c./s.

Figure 3.7 Experimental P-E Hysteresis Curves of Crystal #1 at Various Frequencies

Vertical Scale .7 amp./div.
Horizontal Scale 20 volts/div.

The commonly accepted low frequency value of P_r for single crystal $BaTiO_3$ is 26 μcoul./cm.^{2} (Merz, 1953) at room temperature. The slightly lower values obtained here indicate that the crystals used are not entirely single domain, but rather contain small domains which do not switch, possibly because of crystal imperfections.

As the measurement frequency increased, the value of P_r decreased slowly as shown in Figure 3-7(a), (b) and (c). A possible reason for this effect is that the more highly strained areas of the crystal do not have time to reverse and thus do not contribute to the measured polarization.

The coercive field is also seen to increase in value as the frequency increases. This behaviour is predicted by equation 3-1. At faster switching speeds, the switching current i_s must be larger in order to complete polarization reversal in time, since

$$2P_r = \int_0^{t_s} i_s(t)dt \qquad (3\text{-}8)$$

where $i_s(t)$ is the switching current at time (t). Thus, higher switching voltages are required and E_c increases as t_s decreases.

3.4.4 Slow Speed Switching

Very slow speed switching characteristics of the barium titanate crystals were recorded using the circuit of

Figure 3-8. Switching occurs at a much better defined voltage at low speeds. Figure 3-9(a), (b) and (c), show the I-V switching curves for three different crystals for a slowly increasing ramp voltage (30 V./min.). The crystal of Figure 3-9(a) is relatively well-behaved. Switching occurs at the same voltage in both directions and E_c is well defined. The switching curve is also very symmetrical. This is typical of an unstrained, single domain crystal. Figures 3-9(b) and (c) show deviations from the ideal. In Figure 3-9(b), the coercive field is ill-defined and the crystal appears to be highly strained and polycrystalline. The crystal of Figure 3-9(c) seems to be preferentially oriented. That is, it would rather be one of the c states than the other.

In all cases, the areas under the curve are equal in both directions from zero volts. This is necessary, since the area under the curve is a measure of the amount of charge

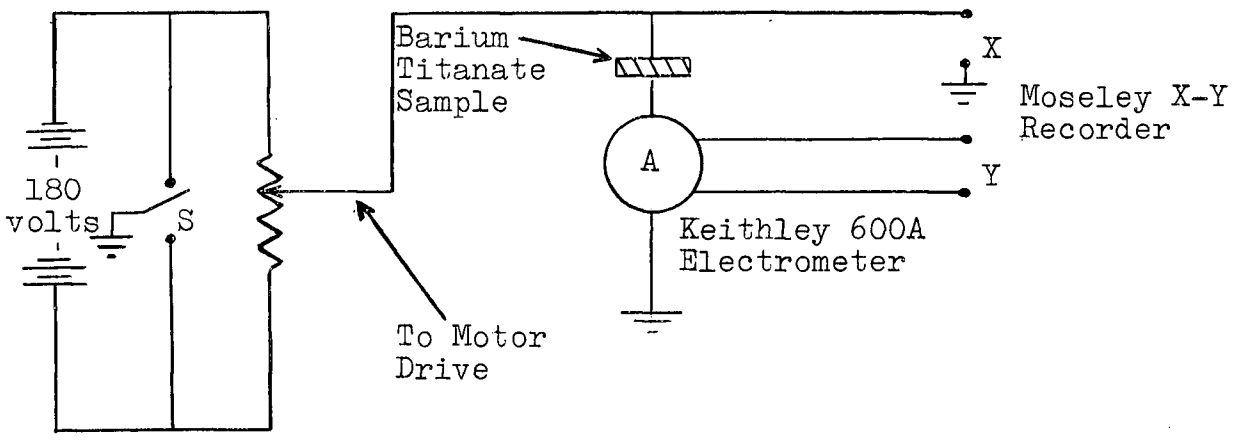


Figure 3-8. Slow-speed Switching Characteristic Measurement Circuit

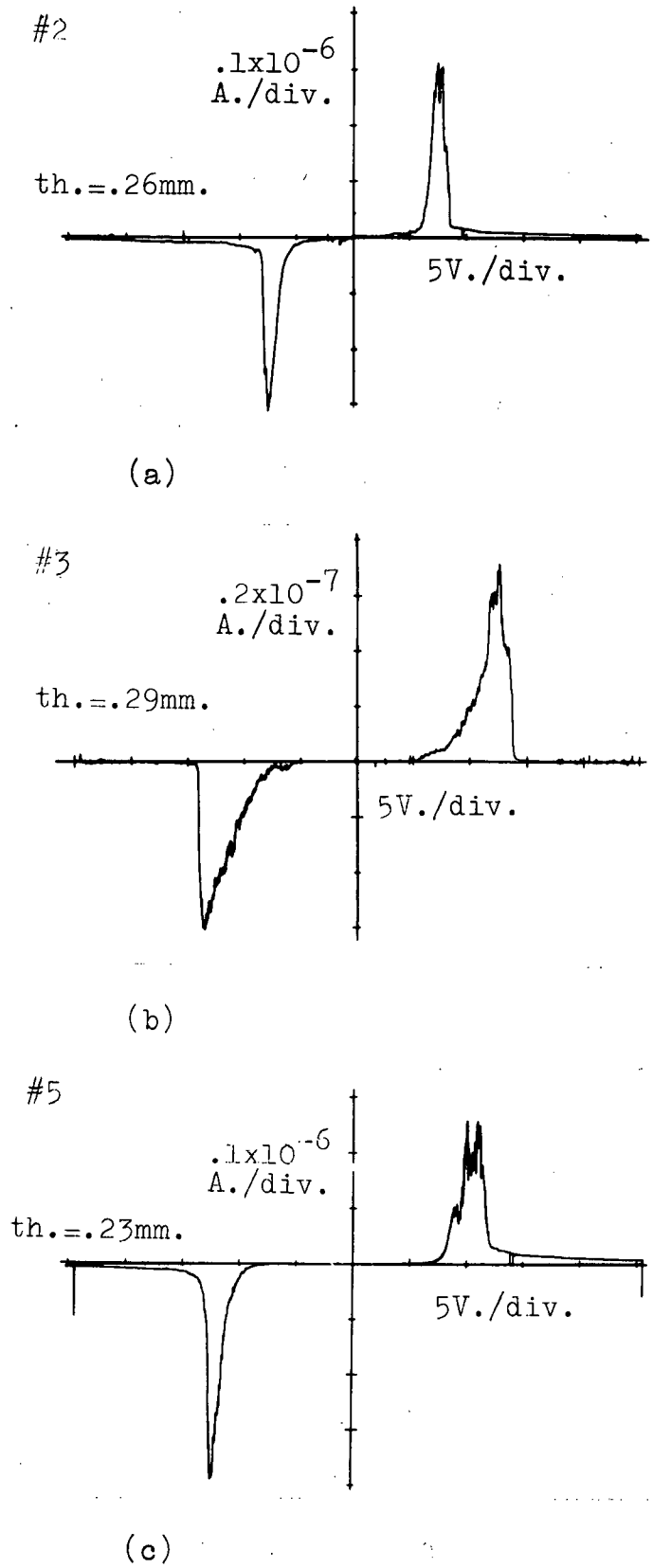


Figure 3-9. Slow Voltage Ramp I-V Switching Characteristics

being reversed by the applied voltage. If a voltage ramp is followed by a second ramp of the same polarity, negligible current will flow during the second ramp, since the polarization charge has already been reversed and the resistance of the sample is very high ($> 10^9 \Omega$).

The spontaneous polarization of the crystals may be calculated from this graph and the total charge flowing has been found to be equal to $2P_r$ within the limits of experimental error ($\sim 20\%$).

The coercive field, defined as the field at which the current is maximum, is between 310-550 V/cm for the samples shown. These values are much below those found at the higher switching speeds used to determine the hysteresis loops of Figure 3-7, as expected.

3.4.5 High Field Polarization Reversal

Polarization reversal of the barium titanate crystals was performed using high voltage pulses. The magnitude of the switching current and the switching time were measured using the circuit shown in Figure 3-10.

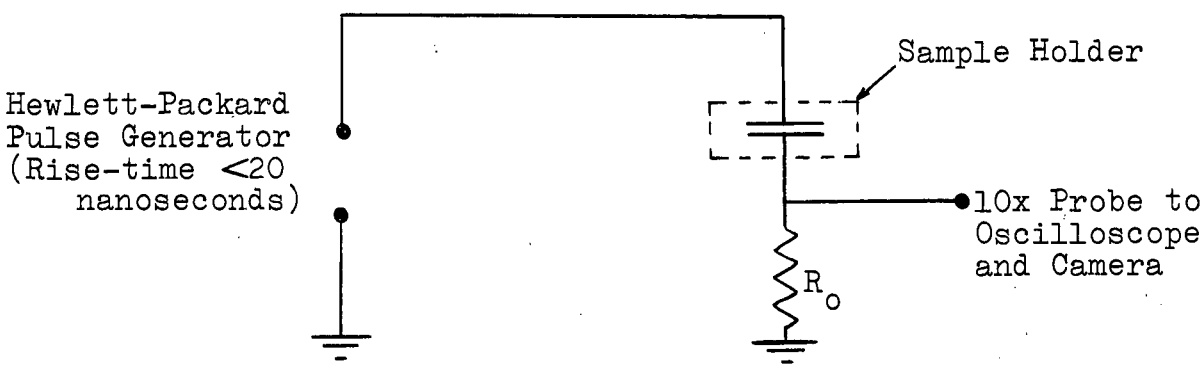


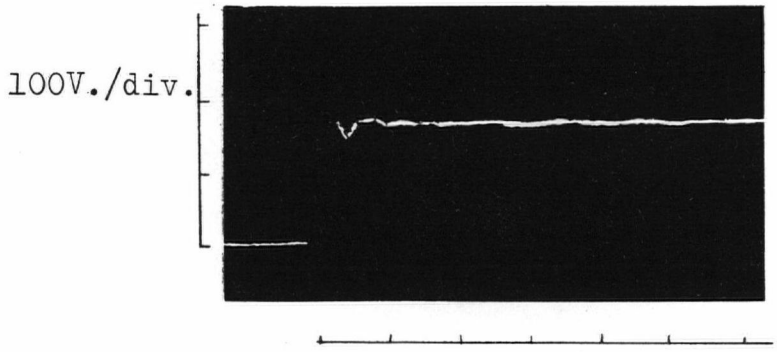
Figure 3-10. High Field Response Measurement Circuit

R_o must be small in order to keep the system time constant as small as possible. A value of 10 Ω gave reasonable output voltages for the crystal electrode area used. The crystals tested were prepoled by the slow speed switching technique to ensure single-domain structure, then switched by a single voltage pulse. Figure 3-11(a) and 3-11(b) show the input voltage pulse and polarization reversal current flow respectively for a well behaved crystal. It is seen that the output current pulse is similar to that obtained by Merz, 1954. Figure 3-11(c) shows the current flow caused by a second input pulse of the same sign and magnitude. The area under the second pulse is less than 10% of that under the first. The crystal has been almost completely switched by the first pulse and the second pulse is caused almost totally by the normal capacitive action of the barium titanate crystal (Anderson, 1952).

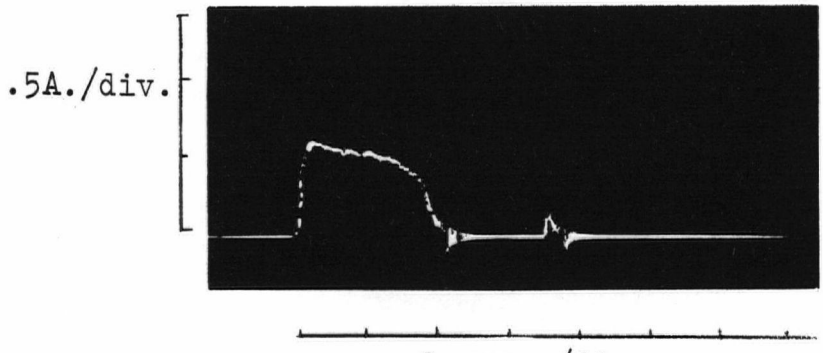
An instantaneous current level of .7 amps is reached across the crystal during switching. Care must be taken not to destroy the electrodes by rapidly repeated switching at high speeds.

It is also possible to determine P_r from the area under the switching curve at these speeds. A rough calculation from Figure 3-11(b) yields a value for P_r of 22 μcoul./cm.^{2}, in good agreement with the expected value of 26 μcoul./cm.^{2}.

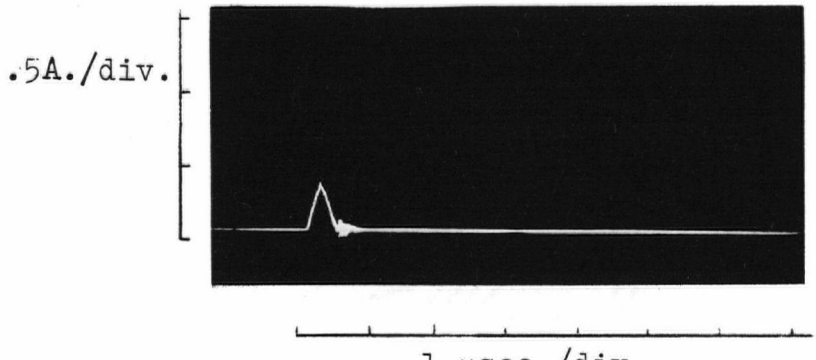
Switching time of 2 μsec. for crystal thickness of .22mm. and switching voltage of 170 volts has been obtained. For thinner crystals, the switching voltage may be reduced proportionately to maintain the same switching time.



(a) Input Voltage Pulse



(b) Crystal Response to First Pulse



(c) Crystal Response to Second Pulse of the Same Polarity

Figure 3-11. High Field Pulse Measurements

4. THE SEMICONDUCTOR FILM

4.1 Introduction

Important requirements on the characteristics of the semiconductor film are high mobility and low carrier concentration (Weimer, 1964). High mobility is needed to give good device gain and frequency response. The carrier concentration must be low enough to allow effective modulation by both the gate and ferroelectric substrate.

Much of the work done with thin-film transistors has employed wide band-gap semiconductors in order to obtain low carrier concentrations. Various semiconductors have this property: silicon of the group IV, gallium arsenide and gallium antimonide of the group III-V, and cadmium sulphide and cadmium selenide of the group II-VI compounds. Of these, cadmium selenide and cadmium sulphide were chosen for the work described here.

The preparation of relatively high mobility, low concentration polycrystalline films of cadmium selenide and sulphide has been reported by many authors. The amount of substrate heating required for deposition of silicon would cause problems, and the techniques of depositing semiconducting gallium arsenide are not well defined. Cadmium selenide was found to be better suited than cadmium sulphide as the semiconductor film for the devices considered since the single crystal mobility of cadmium selenide is higher than that of cadmium sulphide (500 $cm.^2$/volt-sec. vs. 200 $cm.^2$/volt-sec., Bube, Pg. 269).

Another reason for the use of cadmium selenide is that deposition of this material has been found to be much more uniform and reproducible than cadmium sulphide.

4.2 Properties of Cadmium Selenide and Cadmium Sulphide and Effects of Deposition Conditions

Cadmium selenide and cadmium sulphide are group II-VI compounds with an hexagonal crystal lattice structure. The energy band gap for single crystal cadmium selenide has been found to be 1.7 ev. and for cadmium sulphide 2.4 ev. (Bube, Pg. 234).

Preparation of thin films of these compounds is very important in determining their electrical properties. Films deposited onto unheated substrates are highly disordered, of low mobility, and nonstoichiometric because of the nonequilibrium process. The films are usually highly conductive and cadmium-rich. Deposition onto heated substrate reduces these effects but does not remove them. Therefore, post-deposition treatment of the semiconductor films is often desirable (Boer, Esbitt, and Kaufman, 1966) to obtain films with proper characteristics.

Crystal defects are important in determining the properties of the film. Cadmium vacancies act as donors and cation (sulphur, selenium) vacancies act as acceptors. Crystal defects are present in all films and are especially prevalent in polycrystalline films. Impurity atoms affect the electrical properties of the films as well. Group III and VIII impurities act as donors and group I and V atoms as acceptors. Figure

4-1 shows the energy levels of various donors and acceptors of cadmium sulphide and cadmium selenide as shown by Bube, Pg. 159. The acceptor levels are so deep that p-type conductivity is not observed in either cadmium sulphide or cadmium selenide. Also, Oxygen impurity atoms may act as acceptors in both cadmium sulphide and cadmium selenide.

Post-deposition treatment of the films, if necessary to bring the carrier concentration level to the desired value, may take many forms, but heat treating in an air or sulphur atmosphere at 300-500°C has been found to reduce the conductivity of the material by diffusion of oxygen or sulphur acceptor atoms into the semiconductor (Bube, Pg. 175). Heat treating in vacuum or in cadmium vapour produces the opposite effect.

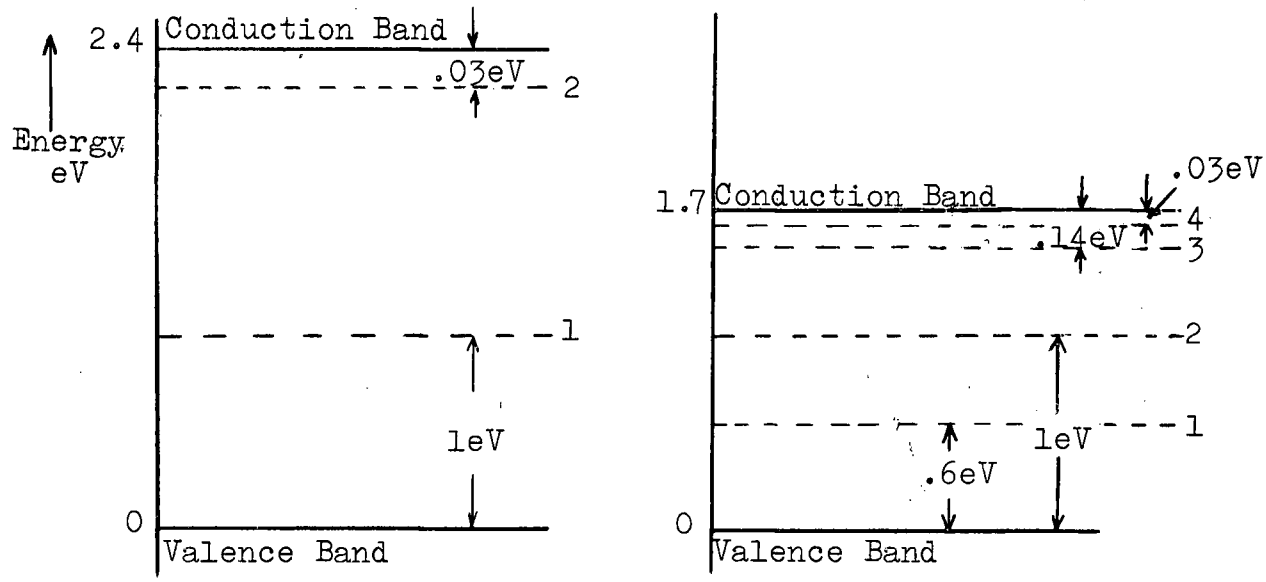


Figure 4-1. Imperfection Energy Levels in Cadmium Sulphide and Cadmium Selenide

Ohmic contacts are formed by evaporating aluminum onto the cadmium sulphide or cadmium selenide film, or by depositing gold electrodes on the substrate before the semiconductor film is deposited.

4.3 Thin Film Evaporation and Measurement

4.3.1 Evaporation Technique

CdS* and CdSe** thin films were prepared by evaporating from a heated quartz crucible in the Veeco vacuum system onto a cold or heated substrate. Figure 4-2 shows the experimental set-up for the deposition. Evaporation pressures were in the 10^{-6} - 10^{-5} torr. range. Film thickness was monitored using quartz crystal oscillators (Chaurasia, 1964) inside the vacuum system close to the substrate. Further discussion of thickness measurement is given in Appendix II.

The various film configurations were obtained by evaporating through photo-etched berylium copper masks held with the substrate in a mechanical jig.

Substrate heating, when required, was accomplished by placing a resistive heating element enclosed in a copper holder in thermal contact with the mechanical jig. Temperature was monitored by a thermocouple held in the centre of the mechanical jig which is in contact with the barium titanate crystal.

The evaporation technique consisted of placing the cleaned mechanical holder mask and substrate, already aligned, in place in the vacuum system, closing it and pumping the

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*Cadmium Sulphide Powder UHP Eagle Picher Co.
**Cadmium Selenide Powder 99.9995% pure A.D. Macay, Inc.

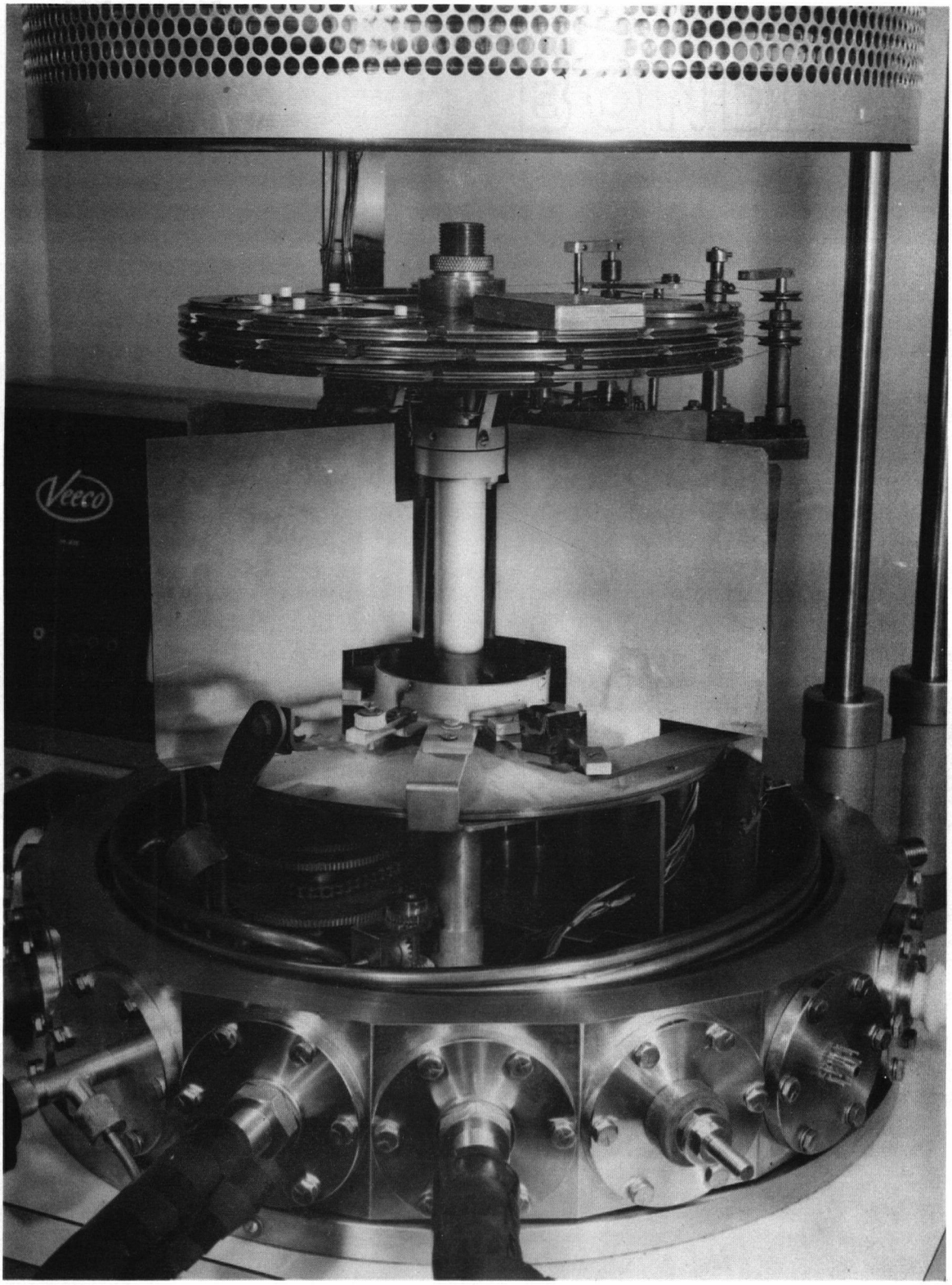


Figure 4-2. Veeco Vacuum Deposition Apparatus

system until the pressure was in the high 10^{-6} torr. range. The resistive heated quartz crucible holding the source material was then heated slowly to outgas the semiconductor evaporant. The source current was then increased until the source material began to evaporate at the proper rate (1-10 A^{o}/sec.), then the shutter closing off the substrate from the source was opened and deposition began. Source current, pressure, elapsed time, and thickness crystal monitor reading were all recorded. After evaporation, the system was allowed to cool before exposing the film to atmosphere.

Ohmic contacts were obtained by evaporating aluminum onto the semiconductor film from a tungsten filament source with a vacuum of 1 x 10^{-5} torr.

4.3.2 Hall Effect Measurements

Hall effect measurements to determine thin-film carrier concentration and mobility were performed using a Van der Pauw, 1958 geometry. The advantage of this geometry is that sample shape is not critical, only sample thickness need be known.

The measuring circuit used was described previously by T. W. Tucker, 1966 of this laboratory. The circuit employs Keithley 600A electrometers and can measure specimen resistances up to $10^{10}\Omega$ with $<5\%$ error.

The resistivity of a sample of arbitrary periphery as shown in Figure 4-3 is calculated by substituting in equation 4-1:

$$\rho = \frac{\pi h}{\ln 2} \left(\frac{R_{ABCD} + R_{BCDA}}{2}\right) f \left(\frac{R_{ABCD}}{R_{BCDA}}\right) \qquad (4\text{-}1)$$

where ρ is resistivity of the sample in Ω-cm.,

h is sample thickness in cm.,

$R_{ABCD} = \frac{V_D - V_C}{I_{AB}}$, and $R_{BCDA} = \frac{V_A - V_D}{I_{BC}}$, where $V_A - V_D$ is the potential difference between A and D while current I_{BC} is flowing between B and C.

When $R_{ABCD} \approx R_{BCDA}$, then $f(\frac{R_{ABCD}}{R_{BCDA}}) \approx 1$.

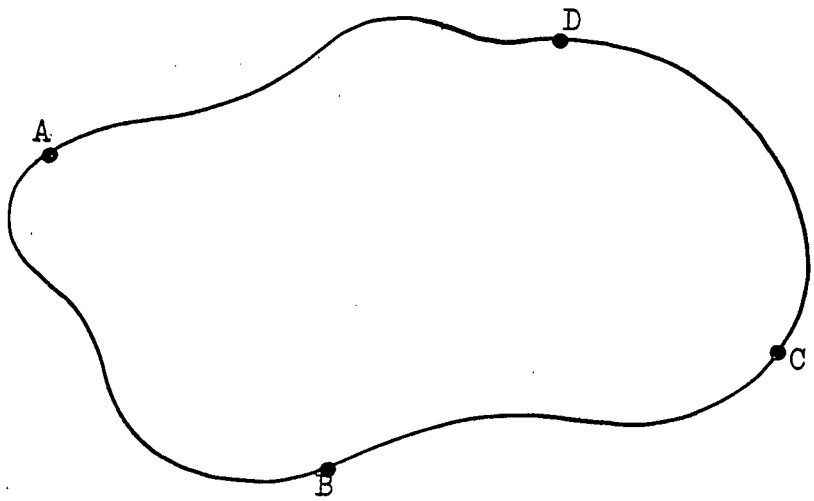


Figure 4-3. Hall Sample with Arbitrary Periphery

The Hall constant R_H is calculated from equation 4-2:

$$R_H = \frac{1}{ne} = \frac{10^8 \, \Delta(V_C - V_A)h}{B \, I_{BD}} \qquad (4\text{-}2)$$

where B is magnetic field across the crystal in Kilogaus,

and $\Delta(V_C - V_A)$ is the change in $V_C - V_A$ caused by the magnetic field, under constant current I_{BD}.

The mobility is calculated from equations (4-1) and

(4-2), since

$$\mu = \frac{R_H}{\rho} \qquad (4\text{-}3)$$

where μ is the mobility in cm.^{2}/volt-sec.

Measurement of ρ is accurate to $\pm 5\%$, if errors in film thickness are neglected, while the accuracy of R_H is variable depending on the amount of noise superimposed on the Hall voltage $(\Delta V_C - V_A)$. The accuracy of R_H is usually better than $\pm 15\%$.

4.3.3 Specimen and Specimen Holder

Specimens were evaporated in a four leaf clover configuration, used by Van Daal, 1964, to reduce contact error due to non-infinitesimal contacts. Aluminum electrodes were deposited under vacuum on top of the semiconductor film to form ohmic contacts. Figure 4-2 is a photograph of an evaporated Hall specimen with contacts.

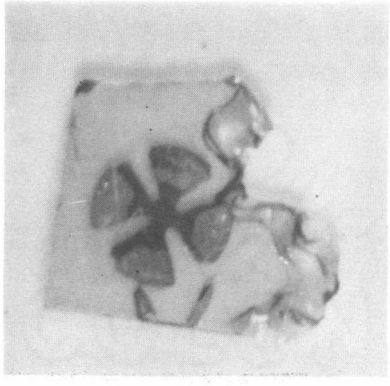


Figure 4-2. Hall Sample of Cadmium Selenide with Aluminum Contacts

The specimen holder used had four pressure contacts of gold-plated berylium copper to contact the specimen. A fifth electrode consisted of the specimen holder base plate and was used to perform switching experiments on Hall samples of cadmium selenide deposited on barium titanate. This will be discussed further in the next chapter. The specimen holder is pictured in Figure 4-4(a) and (b). All measurements were performed with the light-proof casing in place.

4.3.4 Experimental Results

Hall specimens of cadmium sulphide and cadmium selenide, deposited onto unheated glass substrates, were measured immediately after preparation. The results of these measurements are shown in Table III.

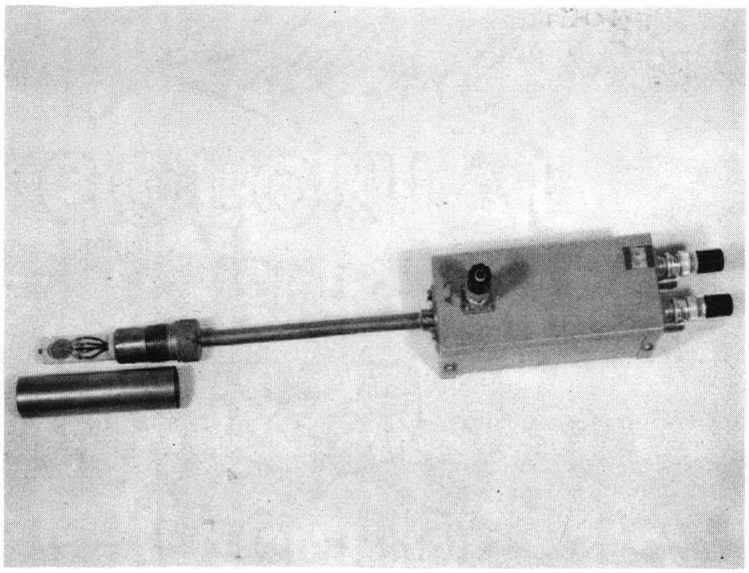
FILM	THICKNESS	RATE OF DEPOSITION	μ_n ($cm.^2$/volt-sec.)	n (el./$cm.^3$)
CdSe	3200 A^o	3.3 A^o/sec.	63±10%	5.3×10^{18} ±10%
CdSe*			55±10%	2.1×10^{16} ±10%
CdS	2600 A^o	3.3 A^o/sec.	40±10%	2.2×10^{16} ±10%

TABLE III

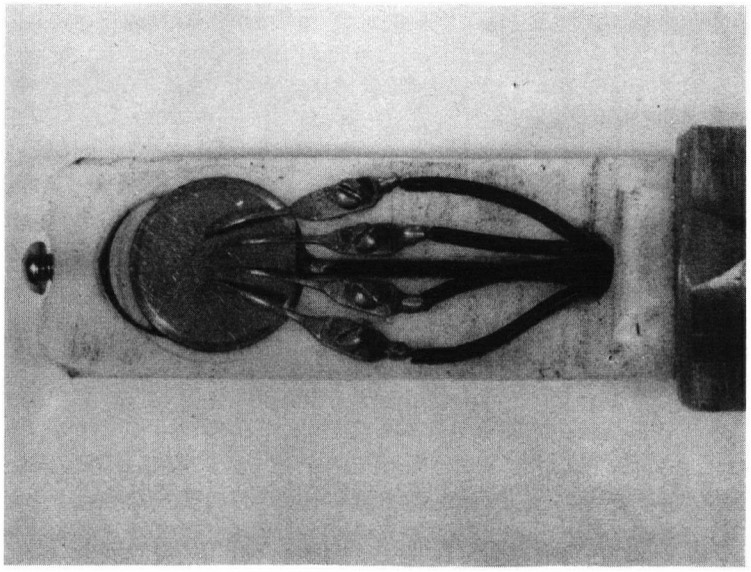
Hall Measurement Results of Cadmium Sulphide and Cadmium Selenide on Glass

These measurements show that the mobility of cadmium selenide is higher than that of cadmium sulphide, even in the

*After standard heat treatment in air at 300°C. for 15 min.



(a) Overall View



(b) Contacts

Figure 4-5. Hall Specimen Holder

polycrystalline form as deposited. Also, the reduction in carrier concentration by heat treatment in air is demonstrated. Cadmium selenide thin films were found to be much easier to deposit and were much more reproducible than those of cadmium sulphide, especially on a barium titanate substrate. Therefore, cadmium selenide was used almost exclusively for the remaining experiments.

5. CADMIUM SULPHIDE AND CADMIUM SELENIDE FILMS ON BARIUM TITANATE

5.1 Introduction

Both conductivity and Hall measurements were performed on cadmium selenide films deposited on barium titanate. Film preparation is discussed. The film conductivity modulation obtained experimentally is related to that which was predicted in Chapter 2. Initial conductivity modulation measurements were made with cadmium sulphide as well.

5.2 Specimen Preparation

The barium titanate substrate was etched as described in Section 3.4.1 and cleaned by agitating in trichlorethylene, in alcohol, and in distilled, deionized water consecutively in the Ultrasonic cleaner. A large round gold or aluminum counter or switching electrode was then deposited onto the underside of the substrate. No attempt was made to align the crystal domain structure. The semiconductor film was then deposited, either as a square for resistance measurements, or in a four leaf clover configuration for Hall measurements. At this stage, the sample was usually subjected to a 15 minute heat treatment in air at 300°C to reduce the film conductivity. The mechanism for this effect is assumed to be oxygen absorption as described in Chapter 4. Aluminum electrodes were then deposited onto the film. Electrical measurements were performed as soon as possible after removal from the vacuum system.

For the narrow electrode gap resistance modulation

samples, a 75μ wire was used to form the source-drain gap, which was 0.6mm. long.

5.3 Electrical Measurements

5.3.1 Hall Measurements

Hall measurements were performed with cadmium selenide films on barium titanate in the same manner as described in Chapter 4. Measurements were taken with the crystal in both the c^+ and c^- states. As described in Section 3.4.4, switching was performed by applying a slow ramp voltage across the crystal, between the counter electrode, contacted to the copper base of the specimen holder, and the four aluminum contacts of the Hall specimen combined. The top switching electrode is formed by the four aluminum contacts and the semiconductor film.

Conductivity modulation in the cadmium selenide films was observed. Values of mobility and electron concentration in the two states for several samples are given in Table IV.

SAMPLE	THICKNESS	STATE	MOBILITY ($cm.^2$/volt-sec.)	ELECTRON CONCENTRATION (el./$cm.^3$)
#6	1850A° ±15%	*	66±10%	3.0×10^{18}±10%
		low	12±15%	7.0×10^{13}±20%
		high	13±15%	6.0×10^{13}±20%
#7	1700A° ±15%	low	33±15%	3.0×10^{13}±15%
		high	36±15%	1.5×10^{14}±15%

TABLE IV

HALL MEASUREMENT RESULTS OF CADMIUM SELENIDE ON BARIUM TITANATE

*Before Heat Treatment

It can be seen that the modulation of the electron concentration is much below that expected from theory. Assuming a one for one compensation of the polarizing charge by the semiconductor film, only 0.03% of the electron concentration change expected occurs for sample #6 and for #7, 6.5×10^{-4}%. Possible reasons for this discrepancy are discussed following the next section.

Mobility changes between the two states are negligible. If the charge concentration changes were larger, mobility changes might occur (Haering, 1964). Decreased mobility due to increased scattering at greater electron concentration levels is possible, or the mobility may increase due to reduced scattering by filled traps. However, no changes were observed during these experiments.

5.3.2 Two-State Resistor

Conductivity measurements were performed on the two-state resistor with the gap formed by a 75μ wire, which gave a gap width of 70μ. Measurements were performed using the simple circuit of Figure 5-1. For sample #9, 1000A° thick, heat

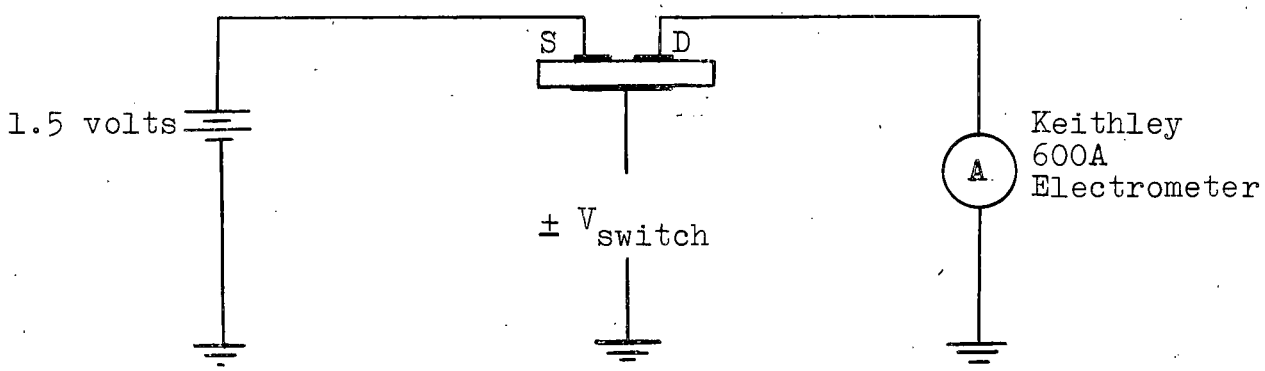


Figure 5-1. Semiconductor Film Conductivity Measurement

treated in air, the resistance change betweeen the electrodes for the two polarization states of the ferroelectric was from $9.5 \times 10^6 \Omega$ to $1 \times 10^9 \Omega$. If a mobility of 20cm.^{2}/volt-sec. is assumed, calculation shows that only 0.01% of the expected charge modulation occurs.

Table V gives changes in resistance for several resistors of varying magnitude. Figure 5-2 shows the two states of sample 5. As predicted, the ratio $\frac{R_H}{R_L}$ in general increases with increasing resistance. If the charge P_r were all compensated by free carriers, then the ratio would increase linearly with increasing resistance. It is thus necessary to modify equation 2-17 to include the effect of uncompensated charges as shown in equation 5-1:

$$I_D = (n_o \pm \gamma \frac{P_r}{e}) e\mu_n WE_D \qquad (5\text{-}1)$$

where γ is the amount of free charge modulated by the barium titanate, as a fraction of the total polarizing charge of the crystal.

There are several possible reasons for the discrepancy in magnitude between the actual and predicted conductivity modulation effect. These will be discussed in turn.

There is a possibility that the barium titanate crystal is not switching fully. However, in every case that the switching charge was measured, it was found to be equal to twice the remanent polarization charge, within the accuracy of measurement. Possibly some small areas do not switch, but the discrepancy is much too large to be caused by this effect.

SAMPLE #	THICKNESS	R_{LOW}	R_{HIGH}	% CHARGE**	R_H/R_L
5	1400*	4.2×10^5	6.0×10^5	.1	1.33
9	1000	9.5×10^6	1×10^9	1.2×10^{-3}	105
14	1700	5×10^8	1.2×10^9	2.3×10^{-5}	24
12	1700	5×10^9	3×10^{11}	2.3×10^{-6}	60

TABLE V

Summary of Data on Two-State Resistor

*Hall Sample, no Heat Treatment
**Assume μ:20cm.^{2}/volt-sec.

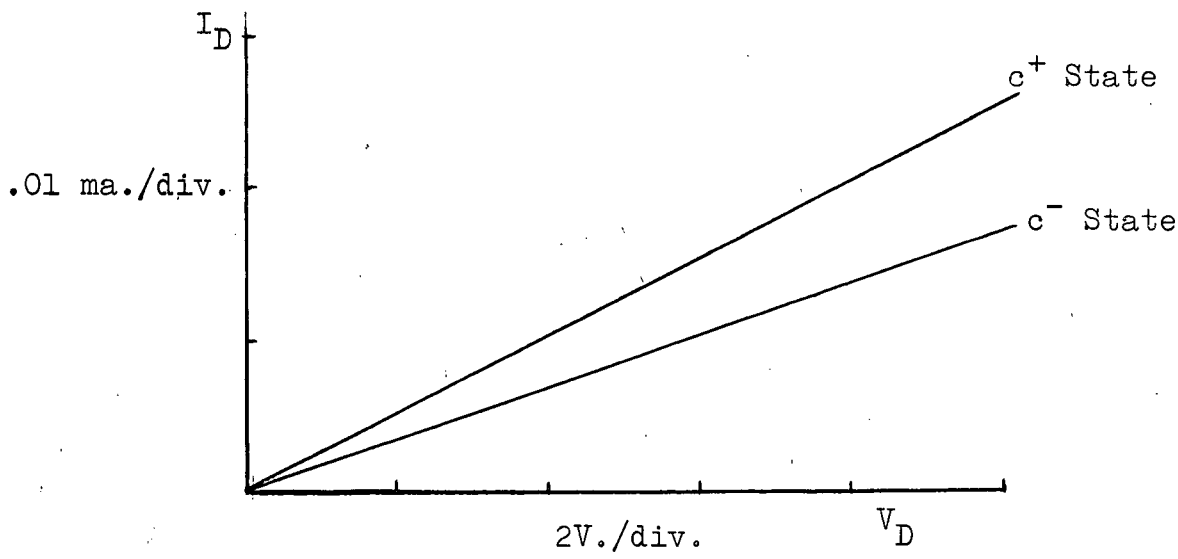


Figure 5-2. Operating Characteristics of Two-State Resistor Sample #5

A high surface state density at the ferroelectric-semiconductor interface would reduce the effect of the remanent polarization reversal. The induced electrons would be trapped at the interface and unable to take part in the conduction process.

Also, the semiconductor itself, because of the method of preparation, contains a large number of traps and these would act to reduce the change in charge concentration (Weimer, 1964) due to polarization reversal.

Of these processes, the last two mentioned are the most likely to cause the reduced effect. The surface state problem especially is applicable. The barium titanate crystal is exposed to the atmosphere before deposition of the semiconductor, and the electrostatic attraction between the ferroelectric domains and the molecules in the atmosphere could increase the surface state density of traps greatly. A surface state trap density in the order of $10^{14}/cm.^2$ would cause the reduction in the effect observed.

5.3.3 Temperature Dependence of Conductivity

It is possible to express the temperature dependence of the conductivity of the semiconductor by an equation of the form:

$$\sigma = \sigma_0 \exp(-W_0/kT) \qquad (5\text{-}2)$$

where W_0 is the thermal activation energy, and σ_0 is a constant of the equation.

This equation is based on the simple harmonic oscillator

with a periodic potential well of energy W_o. This energy W_o is the effective barrier which electrons have to overcome to enter the conduction band. The barrier may be due to inter-crystallite potential variation (Tucker, 1966), the Fermi level, or the lowest energy difference between the conduction band and filled trap levels. It is assumed that the latter is the dominant process for the device being considered here.

Consider the case of an n-type semiconductor, as shown in Figure 5-3, with various trapping levels between the conduction and valence band. At a given temperature, the Fermi level may be as shown. Donor levels 1 and 2 are empty and donor level 3 is partially filled. Any increase in temperature will cause the electrons in Donor levels to enter the conduction

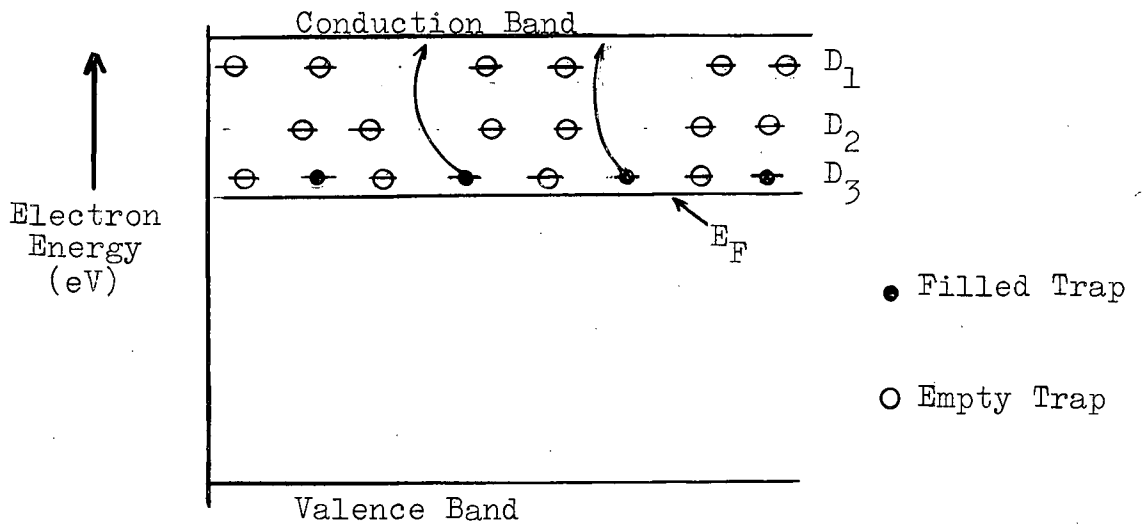


Figure 5-3. N-Type Semiconductor with Trapping Levels

band at a rate proportioned to exp $(E_c - E_{D3})/kT)$. Until this level is exhausted, it will contribute the dominant effect to the conduction band electron density increase. Thus, over a small temperature range, the activation energy W_o of the conductivity of the sample will be $E_c - E_{D3}$.

For low conduction band electron concentration levels the value E_F is less than when the concentration is higher. Thus, the highest energy of filled traps will be lower than when the conduction band electron concentration is high, and the semiconductor will have a larger activation energy.

Cadmium selenide Hall sample #8 was used to test the temperature dependence of conductivity. The circuit used was as shown in Figure 5-4. The temperature range of the test was restricted to $10^{o}C$ - $40^{o}C$ in order to reduce the effect of the change in P_r which occurs with temperature (Jona and Shirane, pg. 116). Over the temperature range given, the value

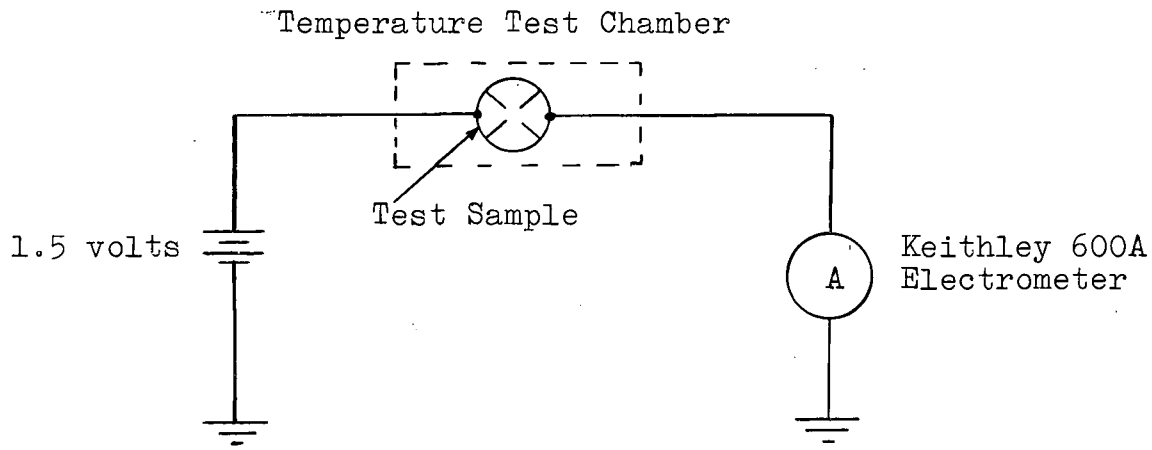


Figure 5-4. Temperature Dependence of Conductivity

of P_r varies from 26 to 24 μcoul./cm.^{2}, which is negligible compared to the exponential conductivity increase due to the thermal activation energy. Also, further heating would affect the properties of the semiconductor due to diffusion of oxygen acceptor atoms into the film. Figure 5-5 gives the $\log_{10} I_D$ vs. $\frac{1}{T}$ plot for the conductivity of sample #8 in both c^+ and c^- polarization states.

The activation energy W_b in electron volts is given by equation 5-3:

$$W_b = 2.303\ k \frac{d \log_{10} I_D}{d \frac{1}{T}} \qquad (5\text{-}3)$$

As predicted, the activation energy of the semiconductor for the low conductance state is greater (0.55ev.) than that for the high conductance state (0.20ev.). In the high conductance state, the traps between 0.55ev. and 0.20ev. of the conductance band have been filled. The electrons induced into the semiconductor by the polarization charge and which have not entered into the conduction process are most likely to be found here. Assuming this to be true, one can state that the number of traps between 0.55 and 0.20ev. is approximately equal to twice the remanent polarization of the ferroelectric substrate.

The experimental plot is a straight line over the temperature range given, and justifies the theory presented. Little more can be said about the results because of the lack of detailed knowledge about the various trapping levels and concentrations in the cadmium selenide film.

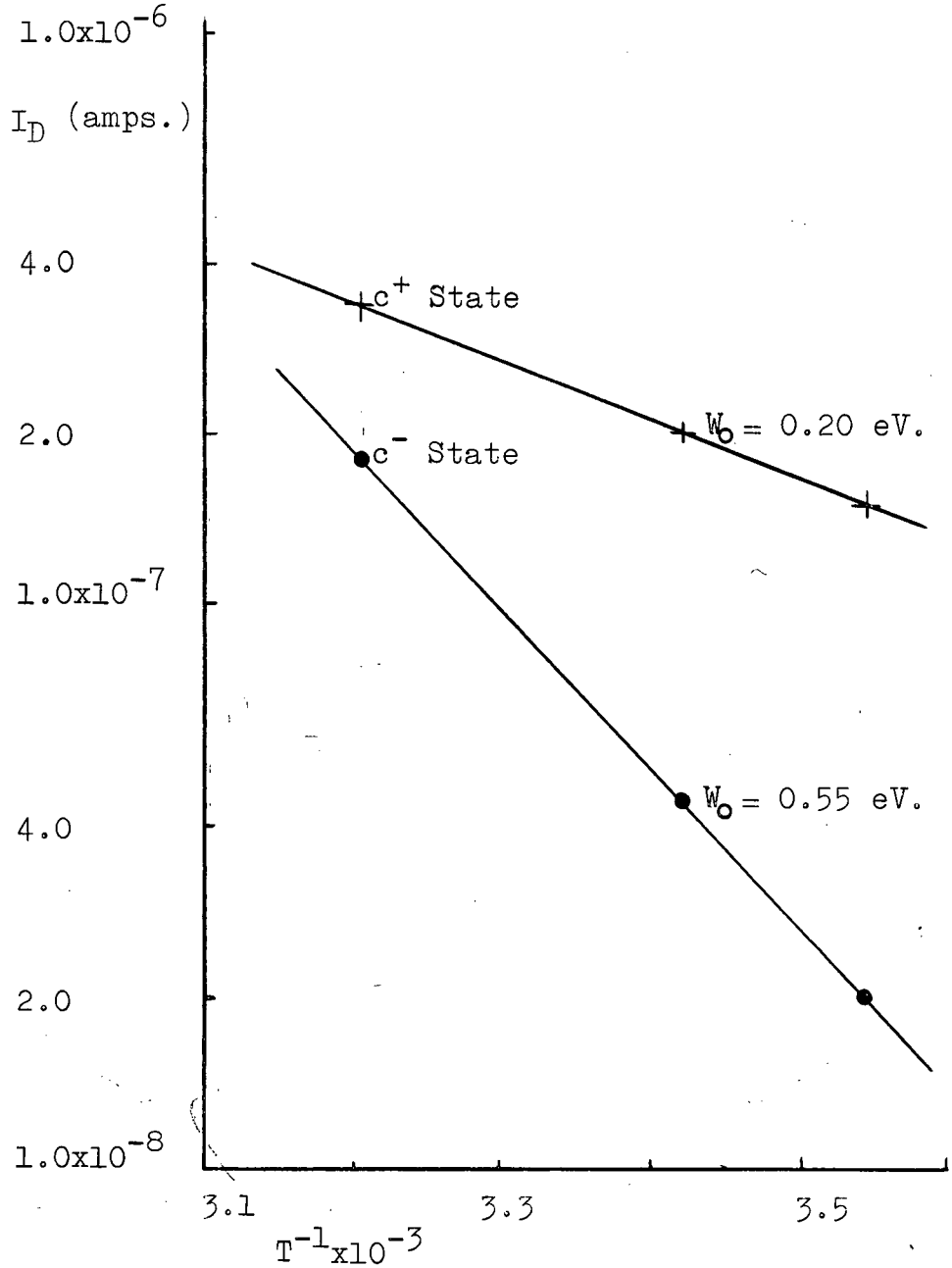


Figure 5-5. $\text{Log}_{10} I_D$ vs. $\frac{1}{T}$ Plot of Sample #8

5.3.4 Stability of Device

Stability of the resistance of the device in either of the two states seems to depend mainly on the switching stability of the ferroelectric substrate. The switching stability in turn is dependent on the stresses within the crystal. If the crystal substrate is well-behaved and single domain, there will be no back-switching of the polarization after removal of the switching pulse, and the resistance will be constant. The current across the source-drain of sample #9 of Table V was recorded for a period of one hour following switching to the highly conducting state. Resistance changes were found to be negligible on the scale used (less than 5%). Sample #10 was also tested and back switching of the crystal to the highly conductive state from the low conducting state was observed as shown in Figure 5-6.

A second effect was also observed over longer periods of time. Resistance of the device in the high state

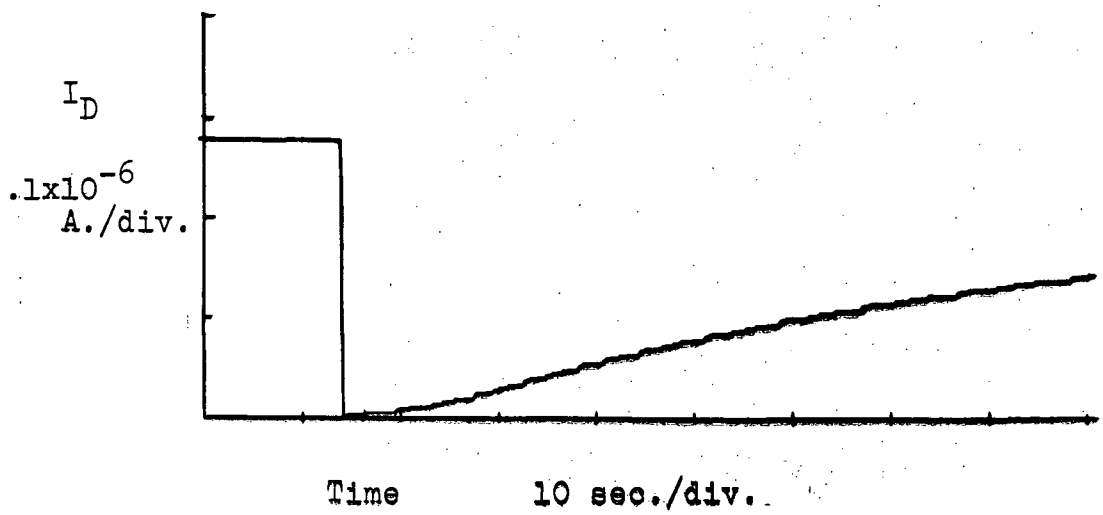


Figure 5-6. Back-Switching of Resistance Sample #10

decreased by a factor of 3 over three days. Also, the R_H/R_L ratio of resistance was somewhat reduced. This can be attributed to the diffusion of further oxygen impurity atoms into the film,which act as acceptors for the n-type cadmium selenide. Encapsulation of the devices in an inert atmosphere would remove this effect.

5.3.5 Photoconductivity Measurements

Photoconductivity of the cadmium selenide films was measured in order to demonstrate trapping effects and to obtain an idea of the range of trap time constants present in the material. Sample #9,described in Table V, was tested for response to white light. The light-to-dark conductivity ratio was approximately 12-1 for the light intensity used. Figure 5-7 shows the conductivity, as measured on the Moseley X-Y recorder, as a result of the switching of the light on and off while the two state resistor is in the high conductance state. The current level is still changing slowly 40 sec.

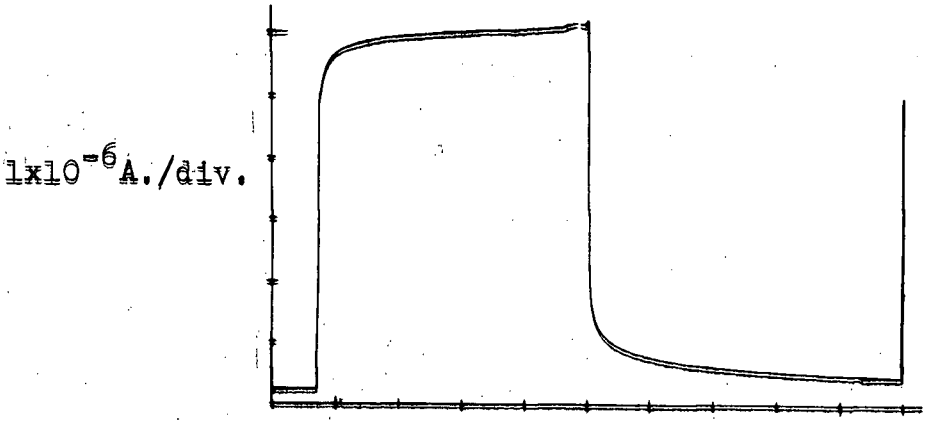


Figure 5-7. Photoconductivity Measurement

after switching the light. Also, the change is not a single exponential. A spectrum of trapping time constants exists for the film, extending from microseconds up to 10 seconds or more. This shows that trapping levels exist between the conduction and valence bands over a large range of energies.

5.4 Cadmium Sulphide Device

A two-state resistor was also constructed using cadmium sulphide as the semiconductor. The film was deposited onto an unheated substrate at a pressure of $1x10^{-5}$ torr. Film thickness was calculated from the crystal thickness monitor to be 3000A°. The film was then air-baked at 300°C for one hour and the aluminum electrodes added. Figure 5-8 shows the resistance of the device for the two states of the ferroelectric substrate.

Further attempts to obtain cadmium sulphide films on barium titanate were plagued by inconsistencies. Difficulties were experienced in getting the cadmium sulphide to stick to the substrate. Also, films which were obtained were non-uniform in colour and in thickness. Therefore, studies of cadmium sulphide on barium titanate were discontinued.

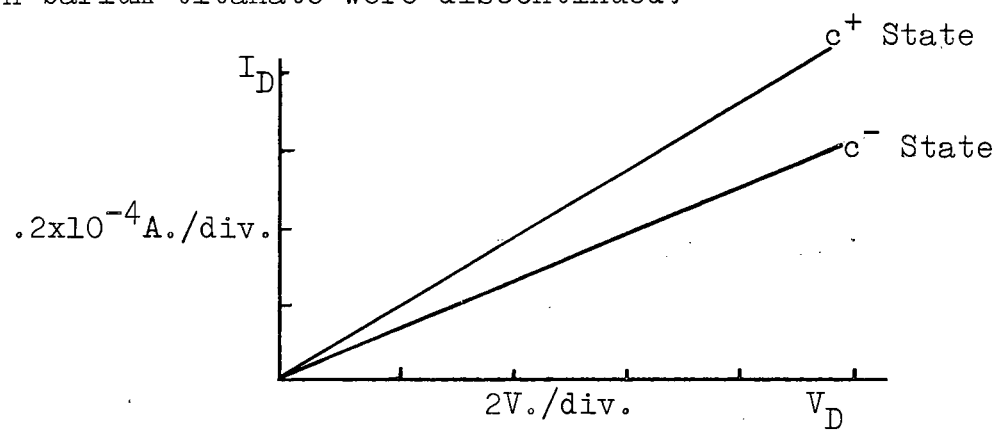


Figure 5-8. Two-State Resistor of CdS

6. THE TWO-STATE THIN-FILM TRANSISTOR

6.1 Fabrication Techniques

A thin-film field effect transistor was fabricated by evaporating an insulating layer of silicon oxide 4000A° thick onto the 75 μ-wide source-drain gap of sample #14 of Table V, followed by an aluminum gate electrode 200 μ-wide over the source-drain gap. The completed device is shown in Figure 6-1. The silicon oxide layer was evaporated from pellets of silicon monoxide* held in a tantalum boat. Evaporation pressure was 1×10^{-5} torr. The insulating film was evaporated in three layers, each 1000 A° thick, at a rate of 8 A°/sec. with 1 minute between evaporations. The aluminum evaporation for the gate electrode was then performed. All evaporations of different materials were made on successive vacuum cycles, since masking techniques necessitated removal of the sample from the vacuum system. A second device, #15, was fabricated in the same manner, except that the semiconductor film was only 900 A° thick, and the air bake of the film was for 30 minutes at 400°C. This was done to obtain a device with lower film conductivity, so that the modulation due to the ferroelectric substrate would be greater.

6.2 Electrical Measurements

All measurements reported here were carried out in the dark. Electrical contacts were made to the devices by using three of the pressure contacts of the Hall specimen holder of Figure 4-3. Switching of the ferroelectric was carried

*"Select Grade" Kemet Company, Cleveland, Ohio.

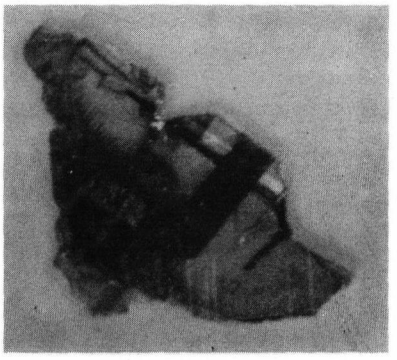
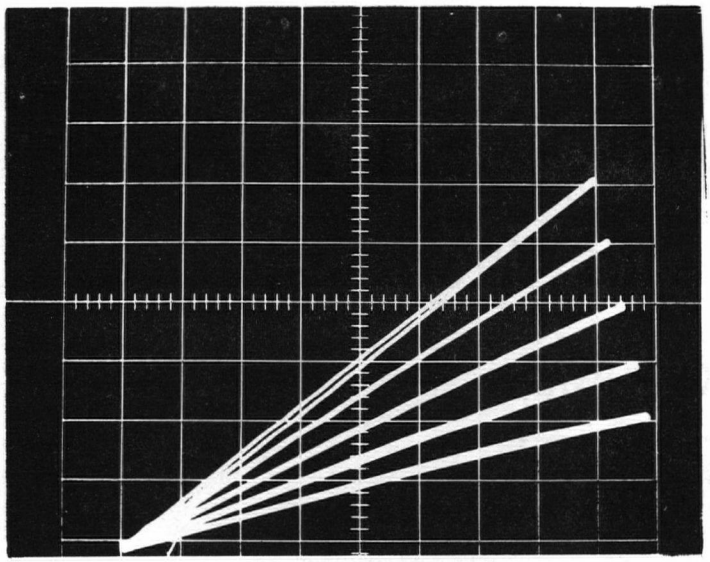


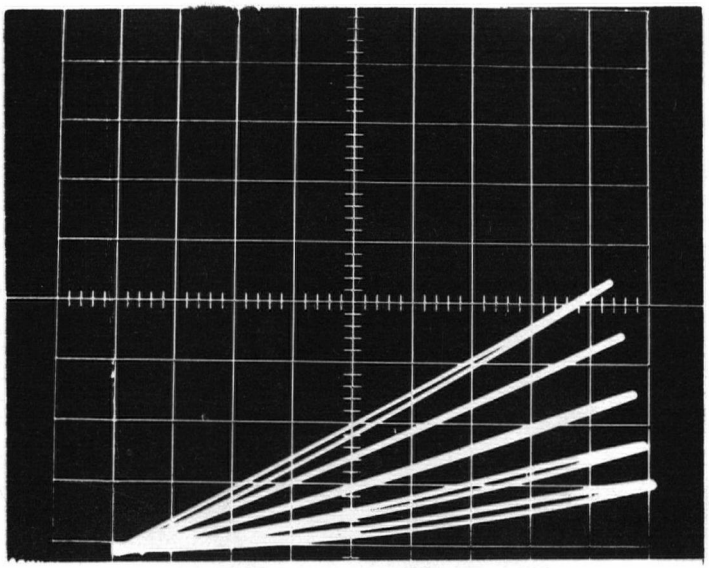
Figure 6-1. Cadmium Selenide Two-State TFT

out by applying a slow voltage ramp between the gold counter-electrode and the source of the device, which was grounded. The V_D- I_D transistor characteristics of sample #14 were displayed on a Tektronix 575 curve tracer with a 1000 Ω resistor between the emitter and base to transform the base current steps of the curve tracer to the required gate voltage steps. The operating characteristics of the device in both positive and negative gate bias conditions and for both states of the ferroelectric, c^+ and c^-, are shown in Figure 6-2(a), (b), and Figure 6-3(a) and (b).

To check the relative effect of each of the gate and the ferroelectric substrate, the amount of gate voltage necessary to change the current level of the device by an amount equal to that caused by the substrate switching was measured for

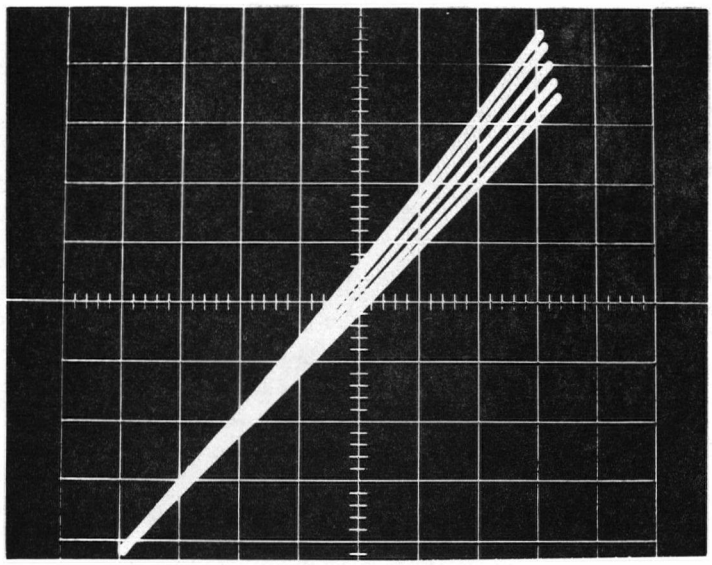


(a) c^+ State

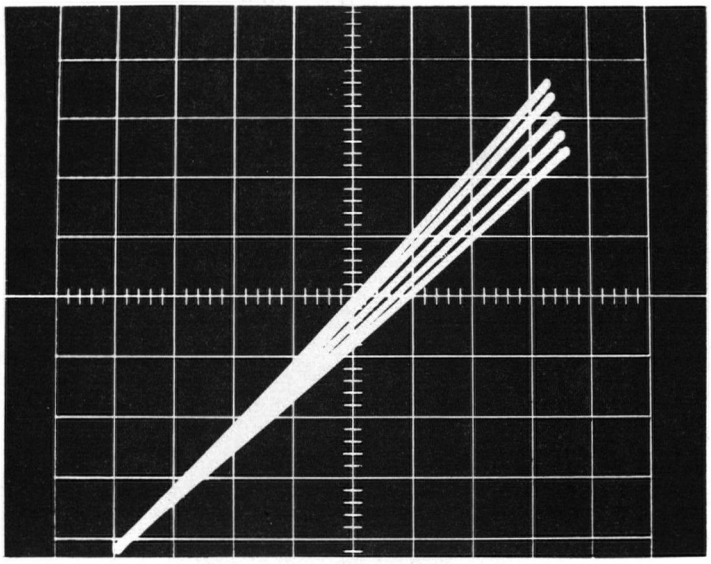


(b) c^- State

Figure 6-2. I_D-V_D Characteristics of Sample #14 in Two States with Negative Gate Bias



(a) c^+ State



(b) c^- State

Figure 6-3. I_D-V_D Characteristics of Sample #14 in Two States with Positive Gate Bias

sample #14.

The device characteristics fail to saturate as the drain voltage increases. Also, the zero gate bias current level changes as the device is operated in the positive or negative gate bias condition. Reasons for this behaviour will be discussed later. The transconductance of the device, calculated from Figure 6-2(a), is 4 μmhos at V_D = 4 volts and varies linearly with V_D since the device does not saturate. Input capacitance, measured at 1Kc./sec. was 38 pf. D.C. input resistance was measured to be greater than $10^{10}\Omega$.

The effective mobility for the TFT below saturation is given by equation 6-1:

$$\mu_n = \frac{g_m L^2}{C_g V_D} \qquad (6\text{-}1)$$

Mobility for the device under consideration was calculated to be approximately 7 $cm.^2$/volt-sec. Also, the gain bandwidth product of the present device given by GBW = $\frac{g_m}{2\pi C_g}$ is 16 Kc. at V_D = 4 volts.

Characteristics of sample 15 were obtained using the measuring circuit shown in Figure 6-4, since the current level

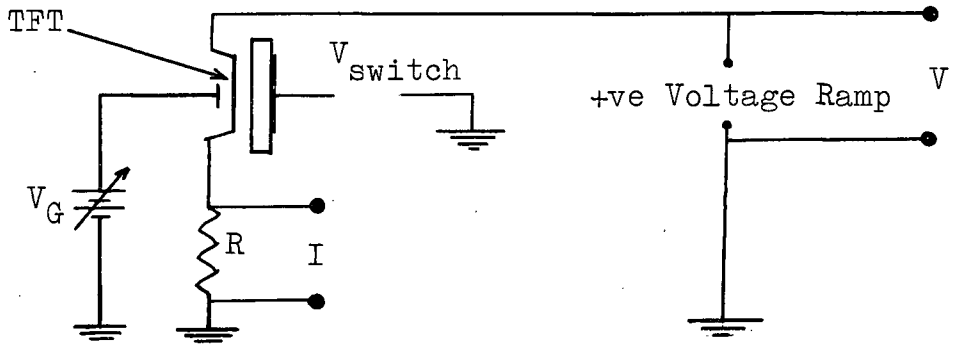


Figure 6-4. V_D-I_D Characteristic Measuring Circuit

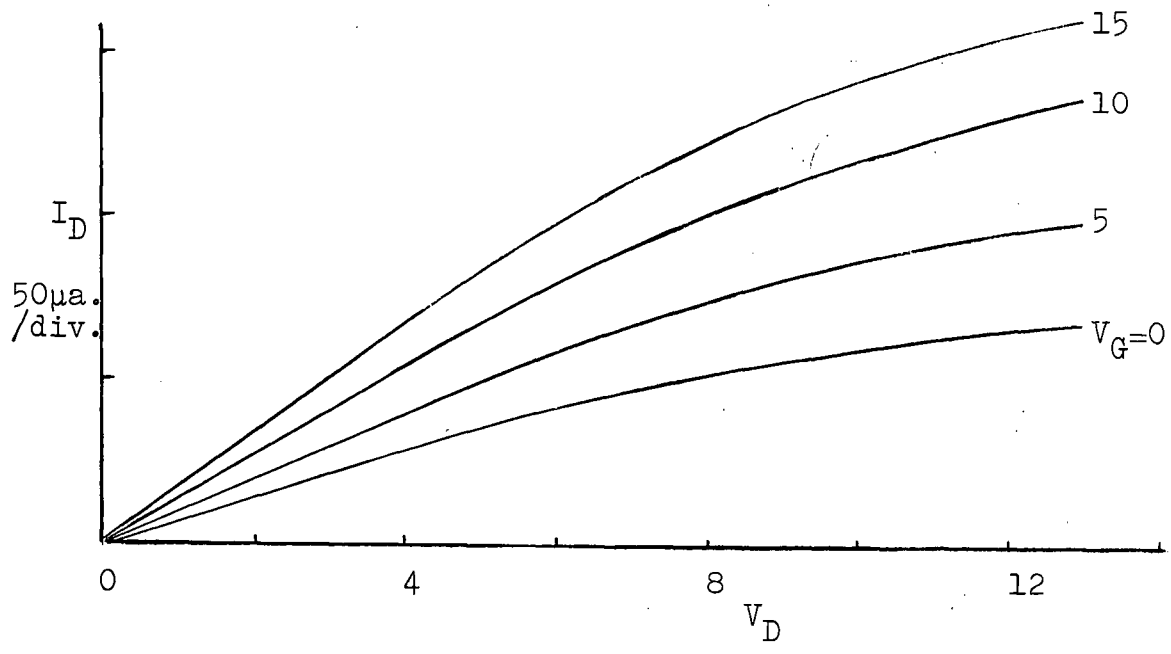
of the device is too low to be detected on the curve tracer. In Figure 6-5(a) are the I_D- V_D characteristics of the device with the ferroelectric substrate in the c^+ state. In the c^- state, the device characteristics are completely cut off. Figure 6-5(b) shows the difference in the zero gate voltage current level of the device in the two states. This device does saturate better than sample #14. The g_m of the device in the c^+ state is 6 μmhos at V_G = 10 volts. D.C. input resistance of sample #15 was measured to be greater than $10^{10}\Omega$ also.

6.3 Effect of Silicon Oxide Layer

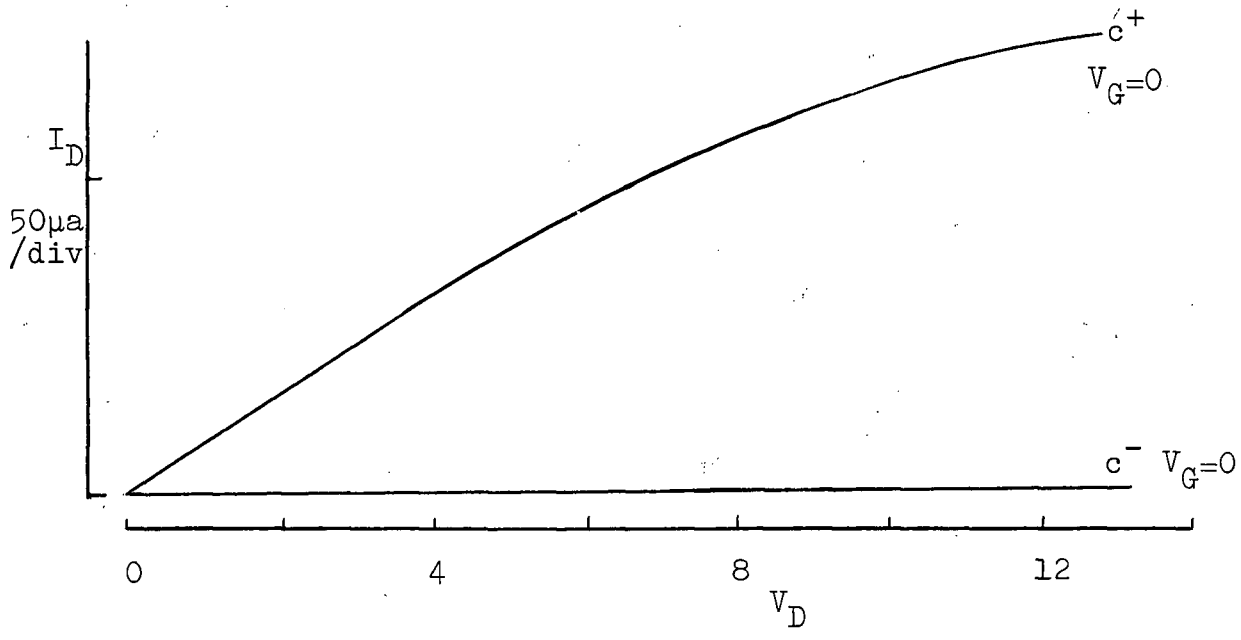
The insulating layer as evaporated has a chemical formula, SiO_x, where $1<x<2$, because of absorption of oxygen into the material from the vacuum system atmosphere. There is a net positive charge in the insulating layer, caused by oxygen vacancies. This charge is compensated by an electron accumulation layer at the semiconductor surface, thus increasing the overall conductance of the film. Resistance between source and drain electrodes for sample #14 decreased to $3\times10^4\Omega$ and $4.5\times10^4\Omega$ for the two states of the ferroelectric after the insulating layer was added. This is a large decrease and must be allowed for in the fabrication of the device. The conductivity before evaporation of the film must be made very small by heat treating or other means so that the final electron concentration will be small enough to make effective gate modulation possible.

6.4 Discussion of Results

The change in gate voltage necessary to change I_D by an amount equal to that caused by the ferroelectric switching was



(a) c^+ I_D-V_D Characteristics



(b) Difference in Zero Gate Bias Current Levels Between c^+ and c^- Polarization States

Figure 6-5. Output Characteristics of Sample #15

used to calculate P_r eff., the amount of polarization charge effective in influencing the device characteristics. At V_D= 10v the required gate voltage was measured at 2.5 volts. P_r eff. was calculated and found to be 1.8 x 10^{11}el./cm.^{2}, approximately 0.1% of P_r actual. This amount of effective change is consistent with that calculated for the two-state resistor and can be explained by the effect of surface states at the barium titanate semiconductor interface and the trap density in the semiconductor as well.

The surface state density at the semiconductor insulator interface was calculated at about 1x10^{11}/cm.^{2}, while that at the barium titanate semiconductor interface is in the order of 10^{14}/cm.^{2}

The change in V_T under positive or negative gate bias conditions may be attributed to charge migration in the insulating layer. Impurity ions caused by adsorption of water vapour and other impurities into the insulating layer may become mobile under application of an electric field across the insulating layer. A positive ion under the effect of a positive gate voltage will, if mobile, migrate to the semiconductor to counteract this increased positive charge at the interface. Increased conductivity will result in the semiconductor film. The hygroscopicity of the SiO_x layer contributes to this effect. It is possible to reduce the amount of drift of V_T by keeping the device in a vacuum or inert atmosphere. A rough calculation, which accounts for the effect of mobile ions in the insulating layer, yields an ionic charge concentration of

$1x10^{18}$ el./cm.^{2}, which is comparable with the found by Salama, 1966, due to water vapour absorption.

The source-drain characteristics of sample #14 failed to saturate, possibly because a parallel conductance path existed in the centre of the semiconductor layer, as well as the modulated surface layers. This unmodulated parallel conductance path, having a relatively large concentration of carriers and being unaffected by the gate, displays a linear I-V characteristic, thus the overall characteristics of the device do not saturate. Reduction of film thickness, and/or longer heat treatment of the film would counteract this effect.

The response of sample #14 to a ± 2V step on the gate electrode is shown in Figure 6-6. The slow rise to the steady state value is similar to that found for photoconductivity measurements in Figure 5-7, and can be explained by the migration of mobile ions in the insulating layer as discussed previously.

In the case of sample #15, the semiconductor film of which was thinner and was subjected to a longer heat treatment than that of sample #14,

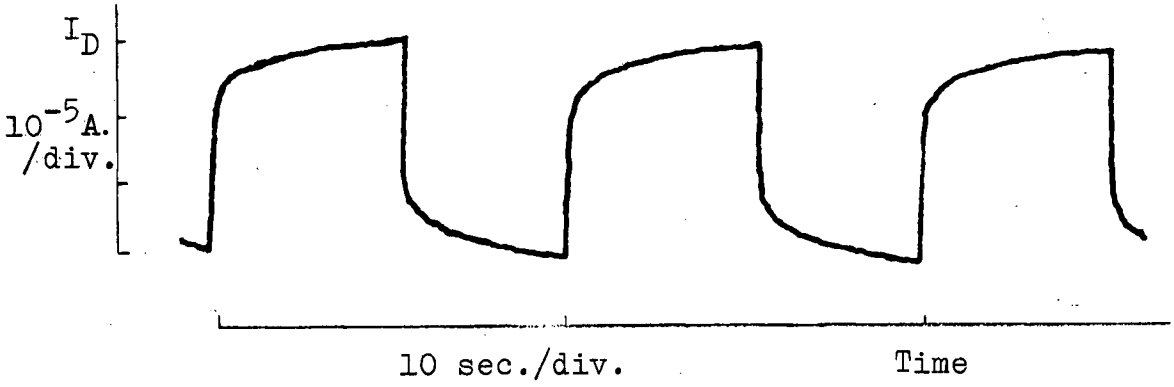


Figure 6-6. Response of Sample #14 to Square-Wave Input on Gate

the device characteristics are completely turned off while the crystal is in the c^- state. No measurable transconductance was obtained. In the c^+ state, the characteristics tended to saturate and a g_m of 5 μmhos was measured in the saturated section of the characteristics. As expected, for thinner films with a lower charge concentration, the effect of the gate and ferroelectric substrate increases.

6.5 Comparison of Two Devices

The two-state resistor operates as a three terminal device with the ferroelectric crystal varying the slope of a linearly increasing I_D- V_D characteristic. In order to obtain a certain current level, the drain voltage must be at a specified level as well.

For the case of the two-state TFT, which operates as a four terminal device, and assuming saturating characteristics, a constant current level will occur over a range of source-drain voltages greater than V_P. The gate electrode can also vary the current level in the saturated region of the characteristics. It would be possible to "gate" a signal applied to the gate of the device, by switching the ferroelectric crystal back and forth between its two states.

The actual current levels obtained in the two states are dependent on the conditions of deposition, thickness and post-depositional treatment of the semiconducting film.

7. CONCLUSIONS

A cadmium selenide thin-film transistor was deposited onto a barium titanate substrate to form an active device with two sets of characteristics dependent on the polarization state of the ferroelectric crystal. Cadmium sulphide and cadmium selenide films deposited on barium titanate were also used to produce two-state resistors, the resistance of which was a function of the ferroelectric substrate polarization state.

The experimental results were found to agree qualitatively with the theory derived for both types of devices. However, the amount of modulation of the electron concentration in the n-type semiconductor layer was found to be very much less than that predicted by theory. A large surface state density at the barium titanate-semiconductor interface was postulated as the reason for the deviation from theory.

The cadmium selenide semiconducting films, as prepared in this work, were found to have a large number of slow trapping centres, as demonstrated by the photoconductivity measurements.

The stability of the resistors was found to be mainly dependent on the ability of the ferroelectric substrate to maintain itself in a single domain configuration without backswitching. An additional slow decrease in overall film conductivity was assumed due to absorption of oxygen atoms from the air.

The stability of the TFT was also dependent on the ferroelectric substrate. Absorption of impurity ions into the

silicon oxide insulating layer from the air, especially water vapour, causes a decay in device characteristics.

Objectives of any further work on these devices should include improvement of the semiconductor film in terms of increase in mobility and decrease in the density of traps, as well as an improvement in the stability of the insulating layer of the transistor. Attempts should also be made to reduce the surface state density at the ferroelectric-semiconductor interface.

APPENDIX I

DEVELOPMENT OF MILLER-WEINREICH MODEL OF 180° DOMAIN WALL MOTION

It is assumed that nucleation of new antiparallel domains occurs only at 180° domain walls, and is the sole cause of domain wall movement. This is the dominant effect in polarization reversal.

Assume nucleation of a triangular, antiparallel step at a 180° domain wall, as shown in Figure A-1, where c is the step width and $l >> d$.

The energy change which occurs following the formation of a nucleus of volume V_n and domain wall area A_d, is given by equation AI-1:

$$\Delta U = -2P_r E V_n + \sigma_w A_d + U_d \qquad \text{(AI-1)}$$

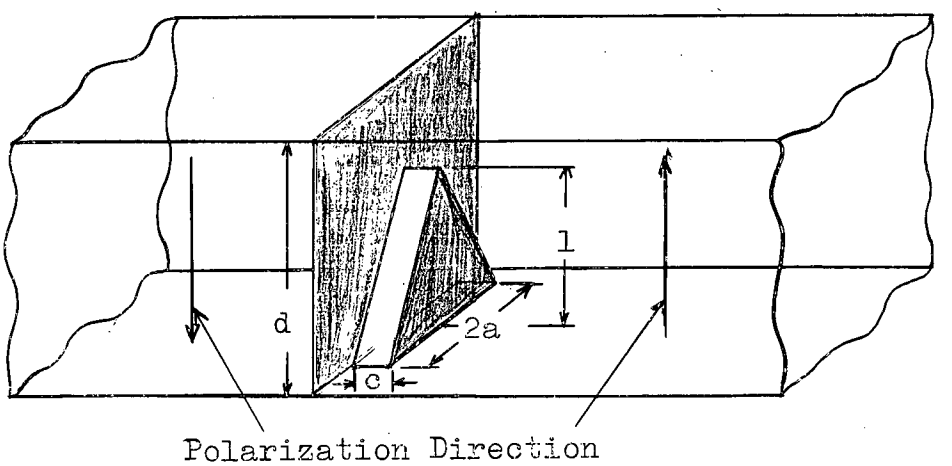


Figure AI-1. Nucleation of Antiparallel Domain

where σ_w is the wall energy per unit area,

P_r is the remanent polarization of barium titanate,

U_d is the depolarizing energy,

and E is the applied field strength.

Calculation of U_d by Miller and Weinreich yielded equation AI-2 after suitable transformations to compensate for dielectric anisotropy in barium titanate were made:

$$U_d = 8 P_r^2 \frac{c^2}{\varepsilon_a} \frac{a^2}{l} \ln \frac{2a}{eb} \qquad \text{(AI-2)}$$

where ε_a is the dielectric constant perpendicular to P_r,

and b is the lattice constant of the crystal in the c direction.

The total energy change following nucleation at the wall is, from equations AI-1 and AI-2:

$$\Delta U = -2 P_r E alc + 2\sigma_w c(a^2 + l^2)^{1/2} + 8 P_r^2 \left(\frac{c^2 a^2}{\varepsilon_a l}\right) \ln \frac{2a}{eb} \qquad \text{(AI-3)}$$

The conditions $\frac{\delta U}{\delta a} = 0$, and $\frac{\delta U}{\delta l} = 0$ determine the critical nucleus dimensions a^* and l^*, as well as the critical activation energy U^* for nucleation to occur.

The expression simplifies to form equation AI-4 if the boundary conditions are applied; higher order terms are neglected and a nucleation step one lattice constant wide

is assumed:

$$U^* = \left(\frac{8b}{3\sqrt{3}}\right) \frac{\sigma_p^{1/2}\,\sigma_w^{3/2}}{P_r E} \qquad \text{(AI-4)}$$

with $a^* = 2/3\frac{\sigma_w}{P_r E}$, and $l^* = \frac{2\,\sigma_w^{1/2}\sigma_p^{1/2}}{\sqrt{3}\,P_r E}$, where

$$\sigma_p = \frac{4P_r^2 b}{\varepsilon_a} \ln \frac{2a}{eb} .$$

The nucleation rate is proportional to $\exp(-\frac{U^*}{kT})$. Thus, assuming that sidewise wall motion is caused only by nucleations at the boundary, the wall velocity may be expressed by equation AI-5:

$$v_d = K_v \exp\left(-\frac{U^*}{kT}\right) = K_v \exp\left(\frac{-8b\,\sigma_p^{1/2}\,\sigma_w^{3/2}}{3\sqrt{3}\,P_r E\,kT}\right) = K_v \exp(-\alpha/E) \qquad \text{(AI-5)}$$

The theoretical activation field α_t is given by equation AI-6:

$$\alpha_t = \frac{-d \ln v}{d\, 1/E} = \frac{1}{kT}\frac{d\,U^*}{d1/E} \qquad \text{(AI-6)}$$

Equation A-5 yields the field dependence of velocity required to fit experimental results for low field strengths (Miller, 1958, 1959), that is, $v \propto \exp -\alpha/E$. Also, substitution of experimentally determined values of the parameters in equation AI-5 yields a 180° wall energy of 0.42 ergs/cm.^{2}, which is in agreement with previously determined

values.

Further Development of the Model

If nucleation steps nb with $n > 1$ are allowed in the model, then for small n, equation AI-7 holds:

$$U^* = n^{3/2} U_1^* \qquad \text{(AI-7)}$$

where U_1^* is the activation energy for a step one unit cell wide. The expression for wall velocity now becomes:

$$v_d = K_v \exp(-U_1^*/kT) + 2\exp(-2^{3/2} U_1^*/kT) + 3\exp(-3^{3/2} U_1^*/kT) + \ldots \qquad \text{(AI-8)}$$

or, in closed form:

$$v_d = v_\infty n \exp(-n^{3/2} \alpha/E) \qquad \text{(AI-9)}$$

Stadler and Zachmandis, 1963 summed this series for various values of E, assuming $\alpha = 4$ Kv./cm., as found by Miller and Weinreich, and showed that for low field strengths, (<2 Kv./cm.) equation AI-5 was valid. At higher field strengths, multiple step widths are more likely, and the series changes. Wall velocity becomes proportional to E^x, with x varying from 1.45 to 1.33 as E varies between 3 Kv./cm. and ∞ .

APPENDIX II

MEASUREMENT OF FILM THICKNESS

The thickness of the semiconductor and other films deposited in the Veeco vacuum system is determined from measurements on a quartz crystal oscillator, the frequency of which varies proportionally to the weight of material deposited on it, which is in turn proportional to the thickness of the material. The thickness is given empirically by the relation:

$$\text{thickness of material} = .61 \frac{D_{Al}}{D_x} \Delta f = \xi_x \Delta f, \qquad \text{(AII-1)}$$

where D_x is the density of the material. For cadmium selenide, $\xi = .284$ and for cadmium sulphide, $\xi = .342$.

The relation has been found to be accurate for aluminum films, (Chaurasia, 1964). Errors do arise in the case of semiconductor films however, especially when the substrate is heated. The sticking coefficient of the semiconductor may be different on cold and heated surfaces, as well as on different types of surfaces, such as the quartz crystal and the barium titanate substrate.

The thickness of several films of cadmium selenide deposited onto an unheated barium titanate crystal was measured using the crystal oscillator, and checked using a Sloan Angsrommeter, which has a resolution of $\pm$ 50 A^o. The thickness measured by the Angstrommeter was found to be within 200 A^o of that determined by the crystal oscillator for films 1000-2500 A^o thick.

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