A PORTABLE PHYSIOLOGICAL RECORDING SYSTEM

by

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ABSTRACT

Equipment was designed and constructed to monitor automatically and unobtrusively up to twelve physiological variables on a human subject engaged in a prolonged field exercise.

Inputs from transducers are sampled in turn, and are encoded into 7-digit PCM. They are then recorded on a small tape-recorder worn by the subject. All equipment is battery-operated, but the recorder and digital circuitry is energized for only 1/2 second every 30 seconds. This permits recording for over 24 hours without interruptions for a change of battery or tape cassette.

A decoder and de-commutator were built so that the tapes can be played back later in the laboratory. Selected parameters can be viewed on an oscilloscope or plotted on a chart-recorder. Overall accuracy of the system is 1%.

Two types of transducers have been developed: one measures the heart rate and the other the skin temperature. Other transducers remain to be developed.

Component circuits were tested at varying environmental temperatures, and a prototype of the whole system was tested on an arctic exercise.

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1. INTRODUCTION

The measurement and monitoring of the physiological variables of active human subjects in the field has been of interest to medical researchers for some time. The advent of modern electronics and microminiaturization techniques has opened up a host of new experimental programs. This thesis resulted from one such program.

For some years the Department of Physiology, University of Hawaii, has been carrying out research into arctic survival. One of their aims is to determine the physiological changes that occur in a typical arctic field situation due to the low-calorie diet, extreme cold and heavy physical exertion. To this end it is required to monitor as many physiological variables (such as heart rate, body temperature, etc.) as possible. The aim of this thesis was the design and implementation of such a monitoring system.

The specifications of the system are as follows: It is to be carried by the subject without excessively limiting his freedom of movement. It should be able to withstand the environmental conditions of vibration due to motion and of extreme cold. A permanent record of the output for each subject is required, and the readings should be virtually continuous, and accurate to 1%. Finally, the system should be completely automatic, requiring no attention for at least 12 hours, in order to minimize its effect on the experiment.

The monitoring system proposed in this work is an extension of a method employed on a previous field experiment. This

method used self-contained transducer packages with the outputs brought out onto dials marked in the proper units. A small portable tape recorder was then used to record the dial readings by voice at fixed intervals, pairs of subjects helping each other with this. It was found that the recorders worked well provided they were kept next to the body, underneath the outer clothing. The system, however, was extremely awkward, and yielded few experimental points since readings could not be taken too often.

The proposed system uses the basic idea of recording the information on a portable cassette tape recorder. High accuracy and reliability are achieved by using a digital recording modulation, since it was found that the digital recording characteristics of the Phillips tape recorder used are excellent. The availability of low cost plastic integrated circuits makes digital recording practical.

Since the variables recorded are averaged or slowly varying functions (sampled every 30 seconds), long term operation is achieved by switching the system off between samples. A duty cycle of 1/60 is thus achieved, making the system operate up to 30 hours without attention (after this only the batteries and tape cassettes have to be changed). The resultant time compression also makes the data easier to interpret.

Up to twelve input transducers may be used, these being time multiplexed onto a single track of tape. The transducers are small, self-contained units that can be interchanged. Two types of transducers were designed; many others can be readily developed.

An experimental prototype of the system was built and extensively tested in the laboratory. This included the decoding

circuits to recover the information from the tape. The system functioned as specified, with a one percent accuracy and output errors of not more than $\pm\frac{1}{2}$ LSB.

Field trials conducted by the author in Alaska during January, 1968, indicated that both the encoder electronics and the tape recorder function satisfactorily down to an ambient temperature of -40°C provided they are kept next to the body, under the outer clothing.

The idea of converting a portable tape recorder into a reliable and small size digital instrumentation recorder at low cost is believed to be a new and important development, particularly when coupled with an intermittent, low duty-cycle operation. Such a system would find many uses in other areas of research where the high cost and large size of commercial instrumentation recorders is prohibitive.

2. CHOICE OF RECORDING STRATEGY

The information obtained from the transducers may be processed in two different ways. It may be telemetered by a small portable transmitter to a "distant" base station where it is received and recorded. This method has been extensively used.[1,2] Alternately the information may be locally recorded on a small portable tape recorder carried by the subject. This method is believed to be new.

Telemetering offers obvious advantages. There is no "hard" wire connection between the transmitter and the recording instrument. The transmitter is simple and can be made very small. Frequency or time multiplexing may be used to accommodate a large number of channels, and the bandwidth per channel may be quite wide. There are disadvantages too, however. The range of small telemetry units is restricted since only a limited amount of power is available. Interference from other sources (such as communications channels, power lines, etc.) may also be a problem. Though the transmitter circuits required may be quite simple, integrated circuits cannot be used and hence the actual saving in size may not be significant if a large number of channels are used. The receiver as well as the decoding and recording circuits, on the other hand, are relatively complex and expensive.

The most obvious advantage of local recording is that each person monitored is completely self-contained and independent, permitting much more versatile field experiments. However, rather elaborate circuits are needed to permit the use of a portable recorder with variable speed and gain, and to shut off the recorder between samples. Only the recent advent of plastic integrated circuits makes portable recording practical both in terms of cost

and size.

Since the system was expected to operate up to 10 miles from the base station, and for over 12 hours at a time, it was decided that telemetry is not suitable. The high cost of the base station equipment, and the need to transport and operate the receiver and recorders in the field were also prohibitive. The local recording method was therefore chosen because it is versatile and self-contained (no base station required), because it can be implemented at a lower cost and because it is expected to be more reliable.

3. CHOICE OF MODULATION

Several modulation methods were considered as a means of recording the twelve signals onto magnetic tape. These methods included both analog and digital types.

3.1 Analog modulation[5,6]

In the simplest analog methods, the signal is conveyed by a voltage, as in direct recording or in modulating the amplitude of one carrier. Several channels can then be transmitted by using several carriers, or the signals can be interleaved in time. Such a record is affected by variations in tape surface, and by dust and oxide particles on the recording heads.

Another analog technique is to convey the information in the time domain, as in frequency-modulating one (or several) carriers, or as in pulse-position modulation or pulse-duration modulation. Here one is disturbed by tape speed variations, both rapid and slow. (For FM with a modulation of up to 20% of the carrier frequency, a 1% tape speed change produces a 5% error.)

In all analog schemes, errors can be minimized by the use of reference tones at frequent intervals, but the complexity of such a system makes it uneconomical by comparison with digital schemes.

3.2 Digital Modulation[3,4,5,6]

In a digital modulation scheme the input is quantized into n discrete levels and transformed into one of n possible output code patterns. This makes the recorder output completely independent of the recording channel (i.e., tape speed and quality) as long as the code can be recognised. This system has two disadvantages.

It requires fairly complex encoding circuitry, and the quantization process introduces small errors of up to 1/2n of the full-scale range (quantization noise). Since the system uses digital circuitry, integrated circuits may be used to reduce its size. The need for precise linear circuits is also eliminated. Therefore digital modulation was chosen for this project, with n = 100 to ensure 1% accuracy.

A variety of codes may be used to represent the 100 levels. The simplest code is a sequence of pulses, from 1 to 100 in number; such a code is wasteful of tape however, since up to 100 pulses are needed to specify one sample. Another code is a set of 100 binary numbers to represent the 100 levels. Since 7-bit binary numbers have to be used ($2^7 = 128$), only seven pulses are needed to specify a sample. In order to conserve tape it was therefore judged preferable to use the binary code, resulting in 7-bit pulse code modulation (PCM), with 128 quantization levels. The additional circuitry necessary to produce the binary code from the sequence of pulses is not large if integrated circuits are used.

4. THE DIGITAL CODE

In order to determine the most efficient and reliable digital code, we have to study the effects of the recording process on the various codes. Thus we have to know the response of the recorder to a step change of magnetization, and to a series of step changes. To this end a few fundamental relationships of the digital magnetic recording process are stated, and the required results are derived.

In this analysis we shall be concerned mainly with the readback process. It has been shown that the magnetization of the tape due to a step change of writing current can be considered as a step function.[3,4] Specifically, the transition region of this magnetization is much smaller than the width corresponding to the characteristic voltage pulse upon readback. Hence the recording density is limited entirely by reading resolution.

The model adopted for analysis is a ring type magnetic head, as shown in Figure 4.1. The permeability of the head magnet is assumed infinite, and the recording process one dimensional and linear.[3] Under these conditions the flux through the read coil due to a horizontal component of magnetization $M_x(x-\bar{x})$ on the tape can be expressed by the convolution integral[3]

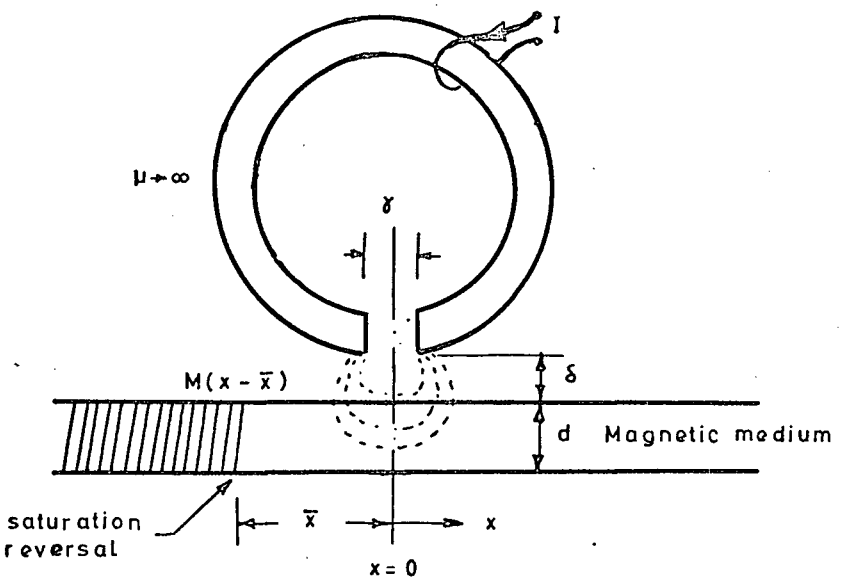
$$\phi_x(\bar{x}) = K \int_{x=-\infty}^{x=+\infty} M_x(x-\bar{x})\, H_x(x)\, dx \qquad 4.1$$

where K is a constant related to the particular recorder

H_x is the horizontal component of the magnetic head gap fringing field

$\bar{x}$ is the distance along the tape and equals tape speed times elapsed time

and the other symbols are defined in Figure 4.1



4.1 Ring Magnetic Head Geometry

Since the electric voltage induced in the read coil is proportional to the derivative of the flux,[3] i.e.,

$$v_x(\bar{x}) \alpha \frac{d\phi_x}{d\bar{x}} \qquad 4.2$$

we have from Equation 4.1

$$v_x(\bar{x}) = K' \int_{x=-\infty}^{x=+\infty} \frac{dM_x}{d\bar{x}} H_x(x)\, dx \qquad 4.3$$

Let us now take M_x to be a step change of magnetization,

normalized to unity, occurring at t=0 ($\bar{x}$=0). Then

$$\frac{dM_x}{d\bar{x}} = \delta(x-\bar{x}) \qquad 4.4$$

Equation 4.3 therefore reduces to

$$v_x(\bar{x}) = K' H_x(\bar{x}) \qquad 4.5$$

It is found that a good approximation to the "near zone" head gap field is given by the Gaussian curve[3]

$$H_x(\bar{x}) \alpha \exp(-u^2) \qquad 4.6$$

Where $u = 2\bar{x}/\Delta$ is a normalized distance along the tape

and 2Δ is the pulse width measured to the 2% points.

The output voltage is therefore

$$\frac{v(u)}{v(0)} = \exp(-u^2) \qquad 4.7$$

where v(0) is the maximum output pulse amplitude and the subscript has been dropped, since the vertical component of magnetization does not contribute to the output appreciably. The ultimate justification of Equation 4.7 is that it does provide an excellent fit for the experimental data.

Since the reading process is assumed linear, the overall output for a series of step changes in magnetization can be computed on the basis of the superposition of characteristic voltage pulses.[3] This process will yield accurate results down to the writing density limit. Since, as previously mentioned, the transition width M_x is

much smaller than the characteristic voltage pulse width 2Δ, this limit is not approached in practice.

The simplest application of the superposition process is for the case of a square wave. For low frequencies it is seen that the recording process performs a "differentiation", in the sense that step changes of input current are reproduced as delta-function-like voltage pulses on output. As the frequency is increased, however, the individual voltage pulses begin to overlap, and since adjacent pulses are of opposite polarity, their amplitude begins to fall off. In a 2-level code, each transition of input current, and hence each output pulse, can be interpreted as one bit of information. Thus, the amplitude falloff is represented on a graph of amplitude vs. bits per inch (bpi) of tape, as in Figure 4.2. This is analogous to the usual amplitude vs. frequency characteristics for amplitude modulated recording. These two amplitude falloff curves thus set the theoretical bit density and frequency limit respectively for the two types of recording.

To compute the rolloff characteristic, consider a voltage pulse centered at $u=0$, and the peaks of the two adjacent pulses at $u=\pm q$. The (normalized) amplitude of the center pulse is thus

$$v(u=0) = 1 - 2v(u=q) \qquad 4.8$$

and

$$bpi = 2/_{q\Delta}$$

Since the measured pulse width was

$$2\Delta = 0.5 \text{ msec} \times 1\ 7/8 \text{ ips} = 0.94 \times 10^{-3} \text{ in.}$$

we have that

$$bpi = 1/_q \times 4.25 \times 10^3 \qquad 4.9$$

This theoretical amplitude characteristic is plotted in Figure 4.2, together with the measured characteristic. Note that the conversion from input frequency in Hz to bpi is

bpi = input frequency in Hz x 2 ÷ 1 7/8

The agreement between the measured and computed characteristics is excellent, thus justifying the choice of the Gaussian field distribution.

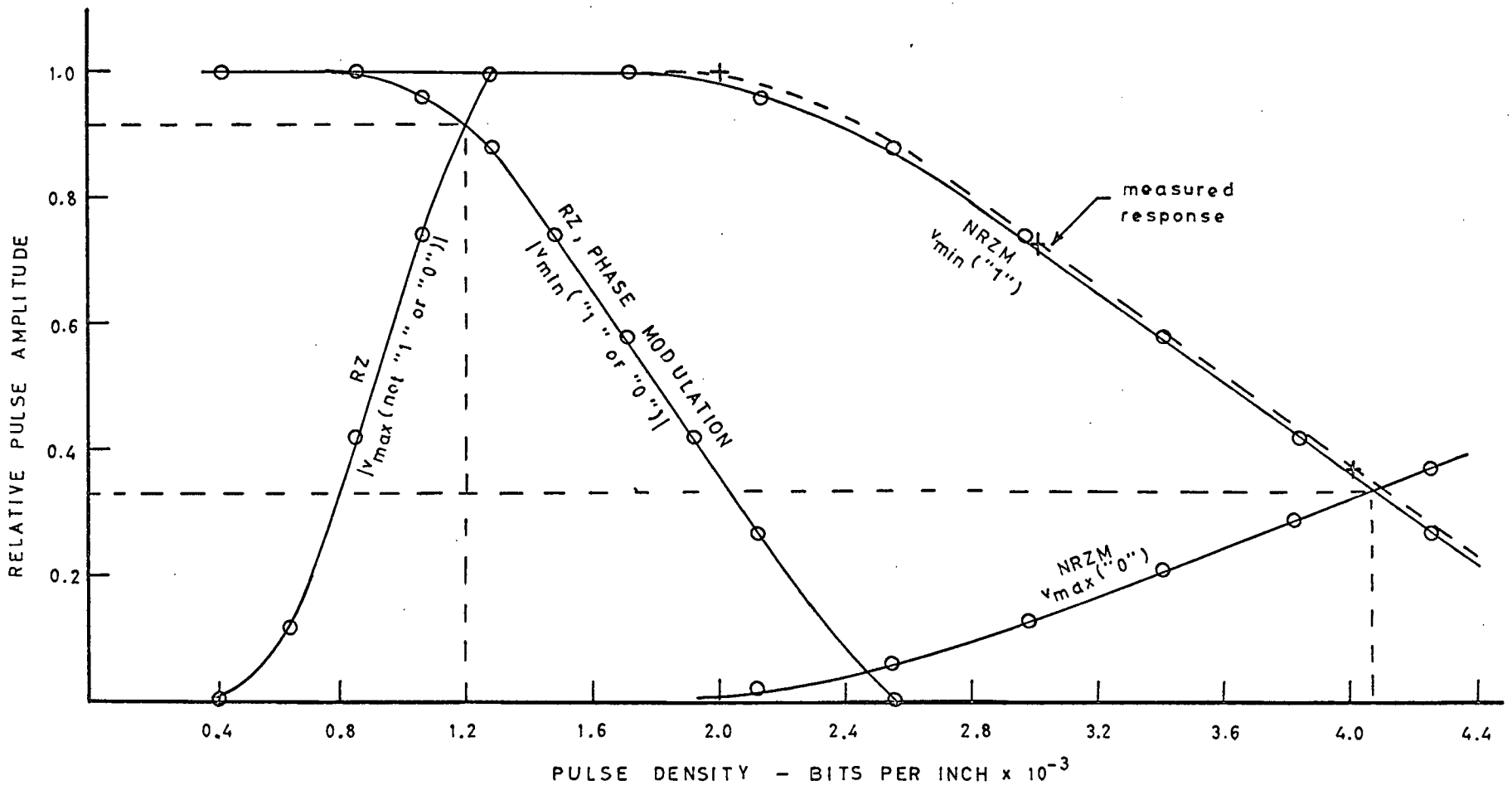
Having developed a method for estimating the response of the recorder to step changes of input current, we can now investigate the theoretical bit density limitations of some of the more commonly used codes. A simple amplitude threshold detection is assumed, as well as an accurate clock source for sampling at the center of each data-bit interval.

4.1 Modified Non-Return-to-Zero Method (NRZM)

This is a commonly used, modified non-return-to-zero code. The writing current is either plus or minus the saturation value. Each transition is interpreted as a logical "1", the absence of a transition as a logical "0". (See Figure 4.3). The output decision circuit thus performs the function

$$\begin{aligned} v > v_T \qquad & \text{output} = \text{"1"} \\ v < v_T \qquad & \text{output} = \text{"0"} \end{aligned} \qquad 4.10$$

The significance of this code is that an error in one bit does not "propagate" to other bits, which would be the case if a positive transition were interpreted as an "1" and a negative transition as



4.2 Theoretical and Experimental Pulse Densities

a "0". Since in the worst case of a code of all "1's" each transition is one bit, the min. "1" level of this code behaves exactly as the square wave previously discussed. Thus

$$v_{min}\ (\text{"1"}) = 1 - 2v(u=q) \qquad 4.11$$

On the other hand the worst case pattern for the interpretation of a zero is ..0010.. In this case the max. "0" level is

$$v_{max}\ (\text{"0"}) = v(u=q) \qquad 4.12$$

Equating the max. "0" and min. "1" levels we can determine the maximum possible theoretical bit density, as well as the (normalized) optimum threshold level v_T. Thus

$$1 - 2v(u=q) = v(u=q)$$

therefore

$$v_T = v(q_{min}) = 0.33$$

$$q_{min} = 1.05 \qquad 4.13$$

$$bpi_{max} = 4.1 \times 10^3$$

It is clear, however, that any amplitude variations due to dropout as well as imperfect clock synchronization will hold any practical system to a bit density well below this theoretical maximum. The results of Equation 4.13 are plotted in Figure 4.2.

4.2 Phase Modulation Method (PM)

This code is also of the non-return-to-zero type. Here positive transitions of writing current are "1"'s, negative transitions "0"'s. If a "1" follows a "1", however, an extra transition is inserted halfway between the normal transition times, and similarly for adjacent zeros. (See Figure 4.3). Thus this code has

the desirable property that there is at least one output pulse per bit, making self-clocking relatively easy. However, this self-clocking property is attained at the expense of lower bit densities, since in the worst case of a code of all "1"'s (or "0"'s) there is now two output pulses per bit.

Since the code alternates in the sense that a positive pulse always follows a negative one, the optimum decision level is

$$v_T = 0 \tag{4.14}$$

Therefore the decision function becomes

$$\begin{aligned} v > 0 \qquad & \text{output} = \text{"1"} \\ v < 0 \qquad & \text{output} = \text{"0"} \end{aligned} \tag{4.15}$$

The worst case amplitude rolloff of this code is given by the relation

$$\left| v_{min} \quad (\text{"1" or "0"}) \right| = 1 - 2v(u=q) \tag{4.16}$$

We see that both the "1" and "0" output pulse amplitudes decay equally. Due to the alternating nature of the output its average value is zero, and therefore the theoretical maximum bit density is approximately given by

$$\begin{aligned} 1 - 2v(q_{min}) &= 0 \\ q_{min} &= 0.83 \\ bpi_{max} &= 2560 \end{aligned} \tag{4.17}$$

This is to be compared with the NRZM code, as shown in Figure 4.2, whose max. bit density is 4100 bpi. Since the clocking information is lost in NRZM coding, requiring either a phase-locked decoder, or a very stable tape speed and external oscillator, the

phase modulated code is often preferred where the smaller bit density is acceptable.

4.3 Return-to-Zero Method (RZ)

This is perhaps the most obvious code. "1"'s are indicated by positive pulses, "0"'s by negative pulses. Between bits the writing current is reduced to zero (see Figure 4.3). Here we have two pulses per bit at the output, and hence the magnitude of the pulses decays in the same way as for the phase modulation method, i.e.,

$$\left|v_{min}\ (\text{"1" or "0"})\right| = 1-2v(u=q) \qquad 4.18$$

On the other hand, now the average value of the code is not zero, since a positive output pulse may follow a positive one as for the code ..01... Hence the level between two such pulses increases as the bit density is increased, until finally the two pulses merge, making identification impossible. The maximum value of this voltage is

$$\left|v_{max}\ (\text{not "1" or "0"})\right| = 2\left[v(u=\tfrac{q}{2}) - v(u=\tfrac{3q}{2})\right] \qquad 4.19$$

This equation is plotted in Figure 4.2, and it is seen that it rises very fast, intersecting the $\left|v_{max.}(\text{"1" or "0"})\right|$ curve at $v/v_{(0)} = 0.9$. Hence the normalized optimum decision level for this code is, from Fig. 4.2

$$v_T = 0.9 \qquad 4.20$$

and

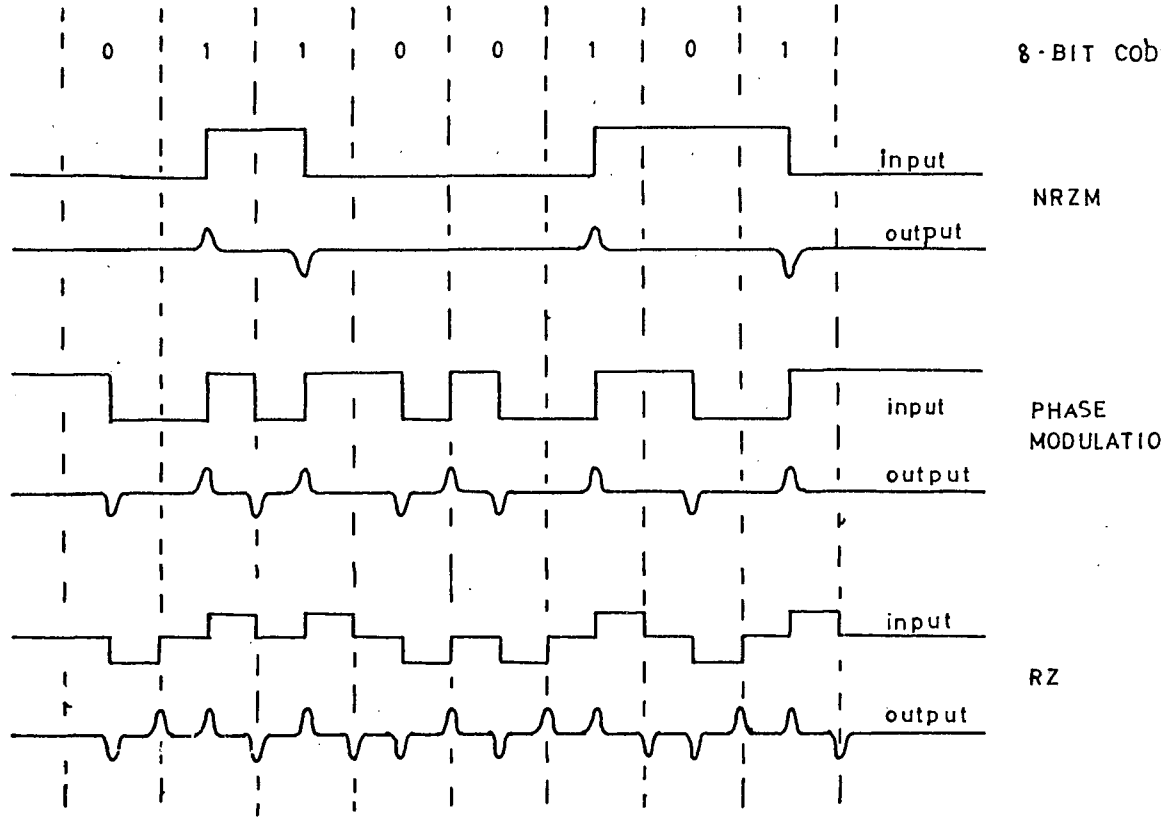
$$bpi_{max} = 1200$$

The decision function becomes

$$v > v_T \qquad \text{output} = 1$$

$$v < -v_T \qquad \text{output} = 0 \qquad 4.21$$

provided the output is sampled at the bit interval centers. (Every second output pulse is thus redundant.)



4.3 Typical Waveforms for the Three Digital Codes

In conclusion we see that the NRZM method of recording offers the highest theoretical bit densities. Since this is accompanied by lack of clock information, however, its application entails complex decoding circuitry, as well as a restriction of the permis-

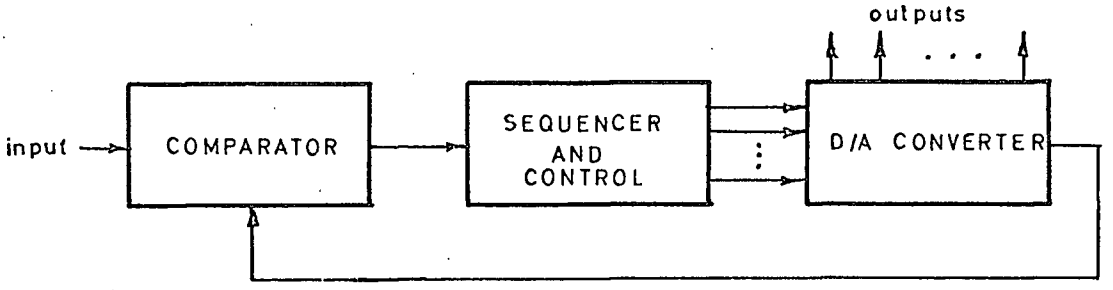
sible input codes. The RZ method is self clocking, but its maximum bit rate is low. Thus for high density as well as reliability, the phase modulated code is used. This code has the advantages of self-clocking, minimum base-line and peak-shift distortion, as well as easy capacitive coupling due to its alternating nature. For these reasons this code was used for the proposed system.

5. ANALOG TO DIGITAL CONVERSION TECHNIQUES

Two basic methods of analog to digital (A/D) conversion are examined. These are representative of the simpler methods usually employed.

5.1 Conversion by Comparison (Potentiometric type)

This class of converters operates on the principle of comparing the input voltage, with a locally generated reference. The reference is generated by a digital sequencer, and transformed to an analog voltage by a digital to analog (D/A) converter. A block diagram of this conversion method is shown in Figure 5-1.



5.1 Block Diagram of Potentiometric Type A/D Converter

There are three basic forms of this method, depending on the way in which the digital reference is generated. The first uses an up-counter, thus producing a staircase reference. The output code is taken in parallel from the counter at the end of the conversion. The conversion time in this case is [7]

$$T_{max} = \frac{2^n - 1}{r_c} + T_R \qquad 5.1$$

where n is the number of bits in the output code

r_c is the clock rate in pulses per sec.

T_R is the time required to read out the contents of the counter

The second method uses an up-down counter, together with a two-level detector, thus forming a servo loop that tracks the input. The contents of the counter are increased or decreased depending on whether the present sample is larger or smaller than the previous one. The conversion time in this case is usually smaller than for the first method, and depends on the rate of change of the input. The output code is obtained in parallel from the counter, as before.

In the third method the output code is generated one bit at a time, starting with the most significant. As each bit is turned on, the D/A output is compared to the input. If at any stage the output exceeds the input, that bit is turned off (i.e. set to "0"), otherwise it is left on. In this case the output is available from the sequencer both in parallel and in series. The conversion time becomes[7]

$$T_{max} = nr_c + T_R \qquad 5.2$$

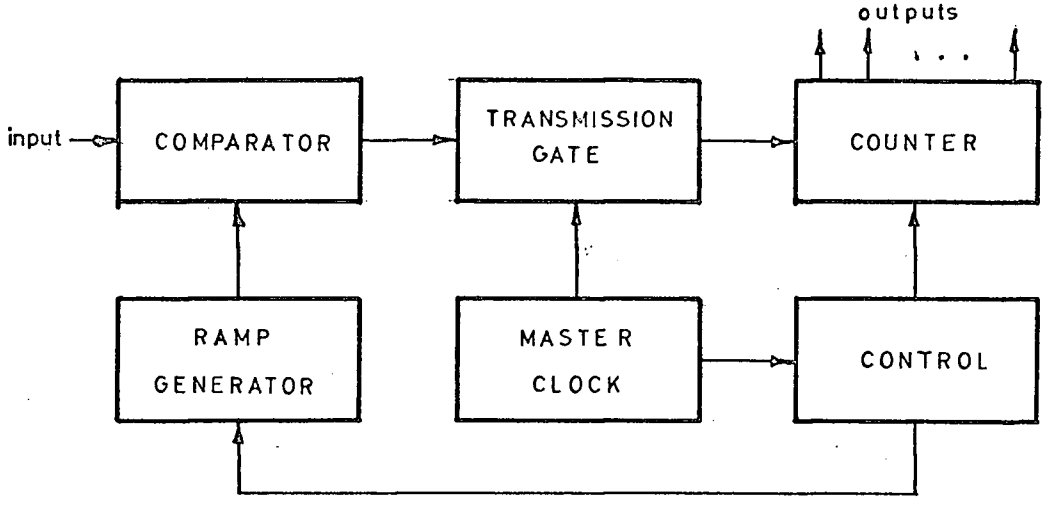
where all the symbols have the same significance as for Equation 5.1.

The accuracy of this class of converters is determined primarily by the comparison circuit and the D/A converter, and can therefore be made very high. High conversion rate is also possible

if the third form of sequencing is used. On the other hand the immunity of the system to noise is poor, since it looks at the input for the entire conversion time, and any noise during this interval will cause errors. Finally the circuitry required is complex, since a D/A converter and a sequencer are required. Since high accuracy and conversion rates are not as important as simplicity, this method is not used in the proposed system.

5.2 Conversion by Time Interval Modulation (Integrating Type)

This class of converters operates on the principle of first transforming the analog voltage to a time interval. During this interval a high frequency clock is gated to drive a counter. The content of the counter at the end of the interval is thus proportional to the analog input. A general block diagram of this conversion method is shown in Figure 5.2.



5.2 Block Diagram of Integrating Type A/D Converter

Two forms of this method are common, the difference being the way in which the time interval is generated. In both cases an integrator (i.e., linear ramp generator) is used. In the first method a single linear ramp is generated and is compared to the input. The transmission gate is opened at the beginning of the ramp, and closed when the ramp equals the input. This method is simple, but its accuracy is limited by ramp linearity. The noise immunity is the same for the potentiometric converters, and is poor. The conversion time is[7]

$$T_{max} = \frac{2^n - 1}{r_c} + T_R \qquad 5.3$$

where all the symbols are the same as for Equation 5.1.

This is seen to be the same as for the first potentiometric type.

In the second method the input is integrated for a fixed time, after which a fixed reference of opposite polarity is integrated until the output returns to zero. The transmission gate is open during the second of these intervals. Since the conversion is effectively performed on an integrated version of the input, the noise immunity of this method is high. The need for an accurate ramp is also eliminated. However, the conversion time is increased to[7]

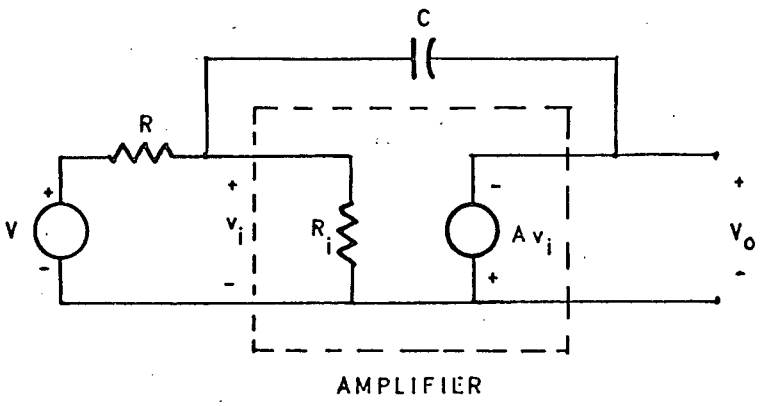
$$T_{max} = 2 \times \frac{2^n - 1}{r_c} + T_R \qquad 5.4$$

where all the sumbols are the same as for Equation 5.1. and the instrumentation for this method is more complicated. For this reason it was decided to adopt the single-ramp technique of an integrating type converter.

5.2.1 Accuracy of the Single-Ramp Integrating Type Converter

Here we shall consider the single-ramp integrating type conversion method in detail. In particular, we shall consider the accuracy of the ramp, of the high frequency clock and of the reference voltage to be integrated.

The ramp is generated by an integrator, i.e., an operational amplifier with capacitive feedback, as shown in Figure 5.3.



5.3 Operational Amplifier Connected as an Integrator

From the figure it can be shown that for a step input of magnitude V the output is given by

$$V_o = -A\left(\frac{V}{1+\Delta}\right)\left[1 - \exp\left(-\frac{t(1+\Delta)}{(1+A)T}\right)\right] \qquad 5.5$$

where A is the open circuit voltage gain

R_i is the input impedance

$\Delta = R/R_i$

$T = RC$

Expanding Equation 5.4 in a power series, and using the definition of slope error[9]

$$e_s = \frac{\text{final slope - initial slope}}{\text{initial slope}}$$

we get

$$e_s = \frac{1 + \Delta}{(1 + A)} \frac{t_s}{T} \qquad 5.6$$

where higher order terms have been neglected,

and t_s is the sweep duration.

For a typical gain of 3000, an input resistance 4 times the amplifier input impedance and a sweep time equal to one time constant, the slope error is 0.17%.

An interesting feature of this method is that the stability of the system against temperature variations can be made better than that of the high frequency clock. Let the clock period be proportional to a single RC time constant T_c. (This is valid since the clock oscillator's frequency is stabilized against junction temperature changes to better than 1% as will be shown in Chapter 6, and the integrator's gain is not significantly altered by temperature.) The count corresponding to an input voltage V_i is therefore

$$p_i = K_1 \frac{V_i}{V} \frac{T_r}{T_c} \qquad 5.7$$

where p_i is the decimal number corresponding to V_i

T_r and T_c are the ramp and clock time constants respectively

V_i is the input voltage

V is the ramp reference voltage

K_1 is a constant

Differentiating Equation 5.6 with respect to temperature and assuming that only the capacitor values change we get

$$\frac{1}{p_i}\frac{dp_i}{dT} = \left(\frac{1}{C_r}\frac{dC_r}{dT} - \frac{1}{C_c}\frac{dC_c}{dT}\right) \qquad 5.8$$

where C_r and C_c are the ramp and clock capacitors respectively.

Thus, by matching the two temperature coefficients and placing the two capacitors close together we can achieve a significant improvement in stability (This improvement is typically about 10%).

Finally, we must consider the integrator input V. Looking at Equation 5.7 we see that a simple way of eliminating its effect is to make

$$V_i = K_2 V \qquad 5.9$$

where K_2 is a constant related to the input transducer and is made independent of temperature.

Therefore p_i becomes independent of V, i.e.,

$$p_i = K_1 K_2 \frac{T_r}{T_c} \qquad 5.10$$

6. IMPLEMENTATION OF THE PROPOSED SYSTEM

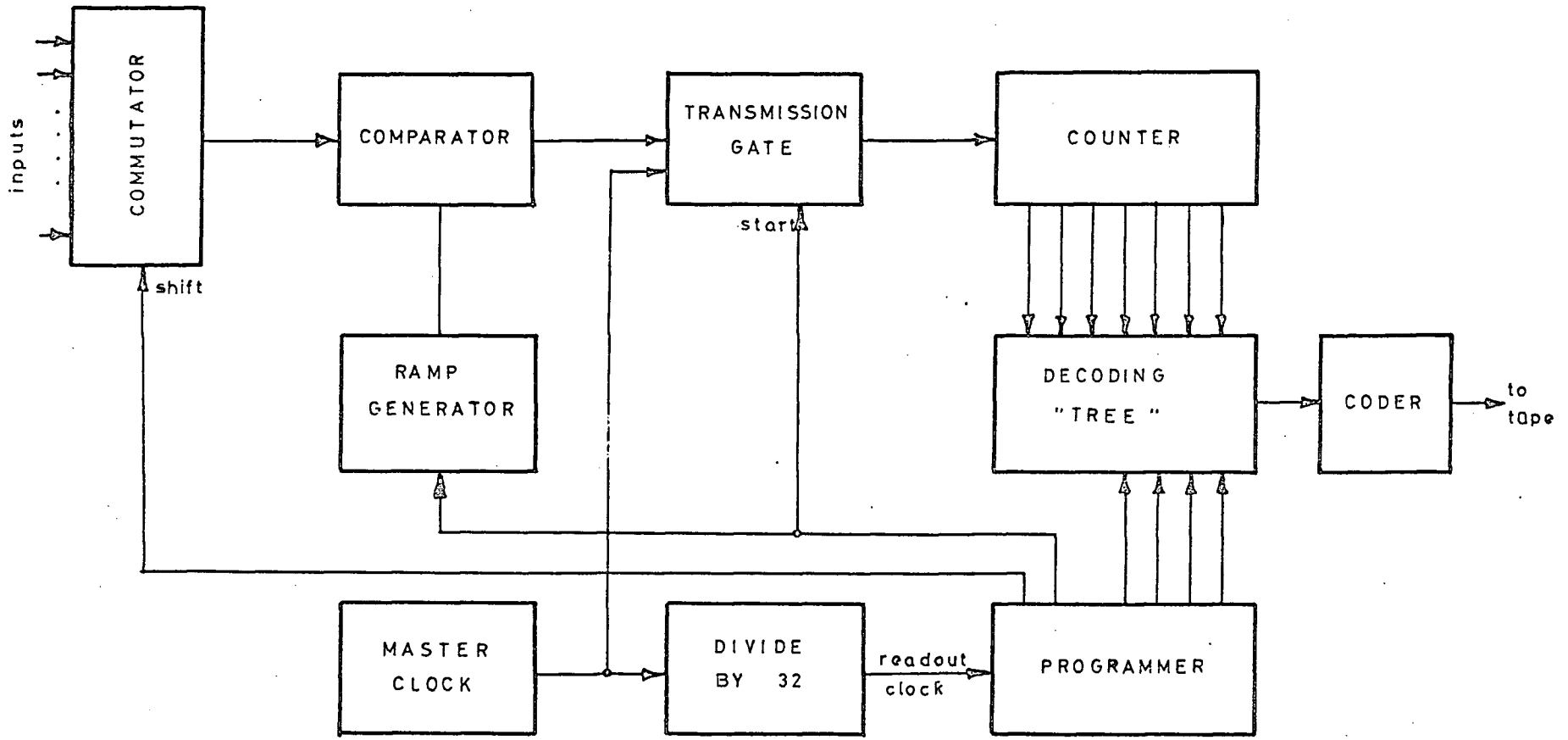
6.1 The Recording System

6.1.1 The Encoder

The encoder performs the conversion of a given analog input voltage (generated by transducers) into a digital code. It consists of an analog to digital converter (A/D), a coder and readout circuits. A block diagram of the encoder is shown in Figure 6.1, where the input commutator is also included.

For the reasons outlined in Chapter 5, a single-ramp integrating type A/D conversion is used. A linear ramp is generated by an operation amplifier connected as an integrator. The output of the integrator and the instantaneous value of the input are fed into a comparator. The comparator output changes state when the ramp exceeds the inputs. Since the conversion rate is much higher than the highest input frequency, the input does not change appreciably during conversion. Therefore a sample-and-hold circuit is not used, simplifying the system.

During the time interval between the start of the ramp and the switching of the comparator the master clock pulses are gated into the binary counter. The count at the end of the conversion interval is thus proportional to the input voltage. After conversion, the parallel outputs of the counter are read out through a decoding circuit controlled by the programmer. The decoding circuit consists of a NOR-gate "tree" that gates the counter outputs onto a single line at the readout frequency. Finally, the output is converted from binary to the phase modulated code. This operation is particularly simple since the two codes are related as follows:

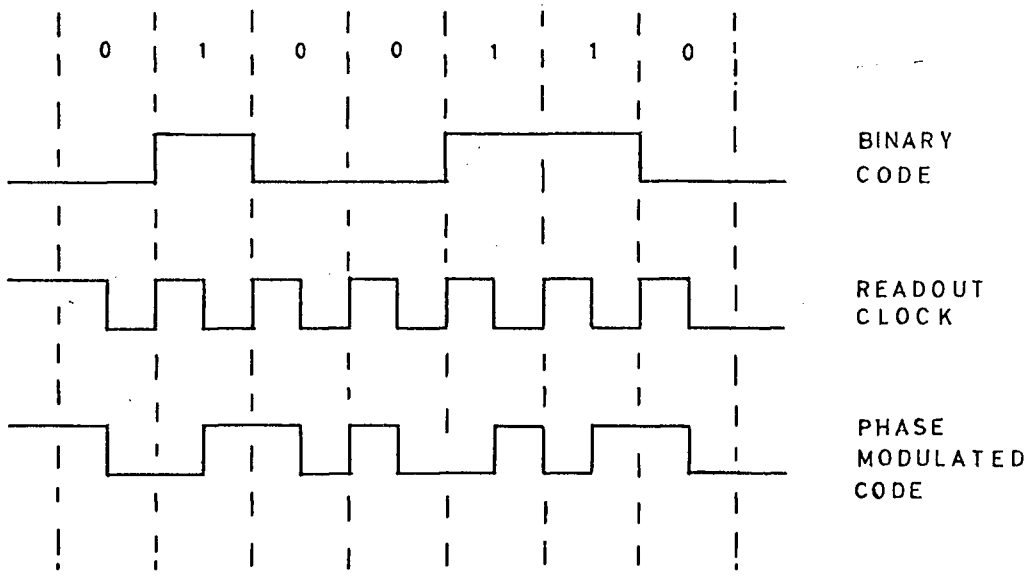


6.1 Block Diagram of Encoder

$$\text{binary code} \oplus \text{readout clock} = \text{phase modulated code} \qquad (6.1)$$

where $\oplus$ is the exclusive OR

This relationship is indicated in the timing chart of Figure 6.2.



6.2 Derivation of the Phase Modulated Code

A scope tracing of the ramp, the comparator output, the binary and the phase modulated code is shown in Figure 6.3.

The various operations in the encoder are controlled by the programmer. This circuit generates two time intervals, one for conversion, and the second for readout. To minimize the uncertainty in the number of pulses passed by the transmission gate during conversion, the beginning of the conversion interval is synchronized to the clock. It is therefore convenient to derive the readout clock frequency by dividing down the master clock frequency, and to use

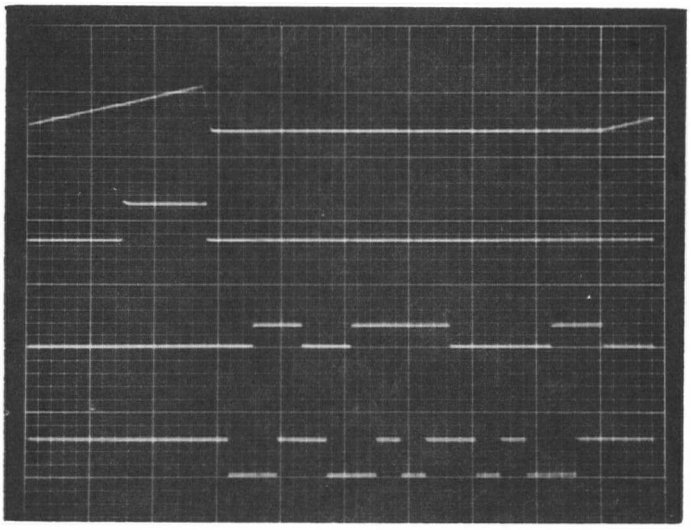
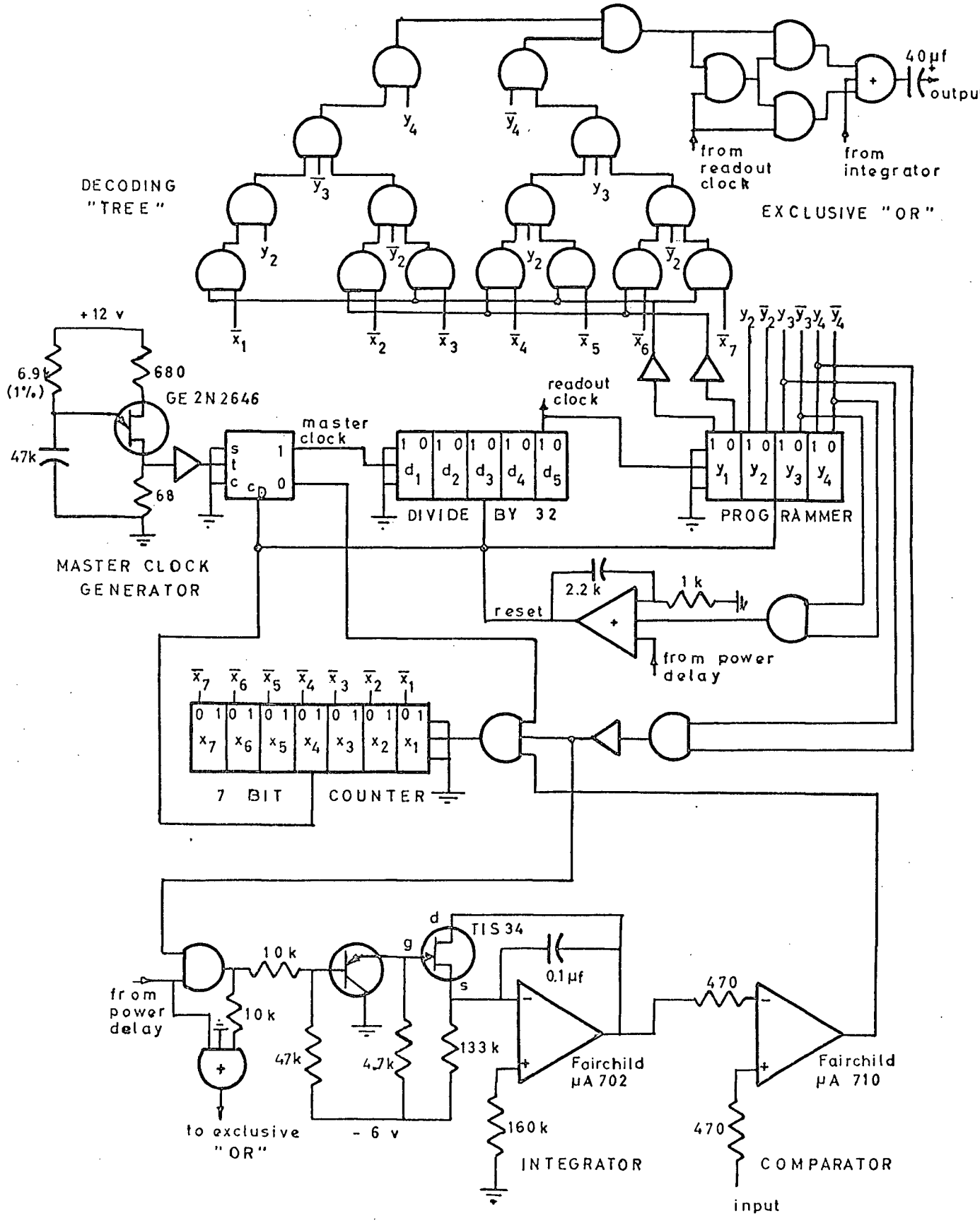


Figure 6.3 Typical Encoding Waveforms
Horizontal scale: 3msec/cm
Vertical scale: 5v/cm

the readout clock to trigger the programmer.

The readout clock frequency was chosen as 500Hz, in view of the tape recorder characteristics discussed in Chapter 4. A reasonable master clock frequency is then 32 x 500Hz = 16 kHz, requiring a conversion time of 8 msec for a 7-bit code. (A higher master clock frequency requires a more elaborate divider; a lower frequency prolongs the operating time of the encoder.)

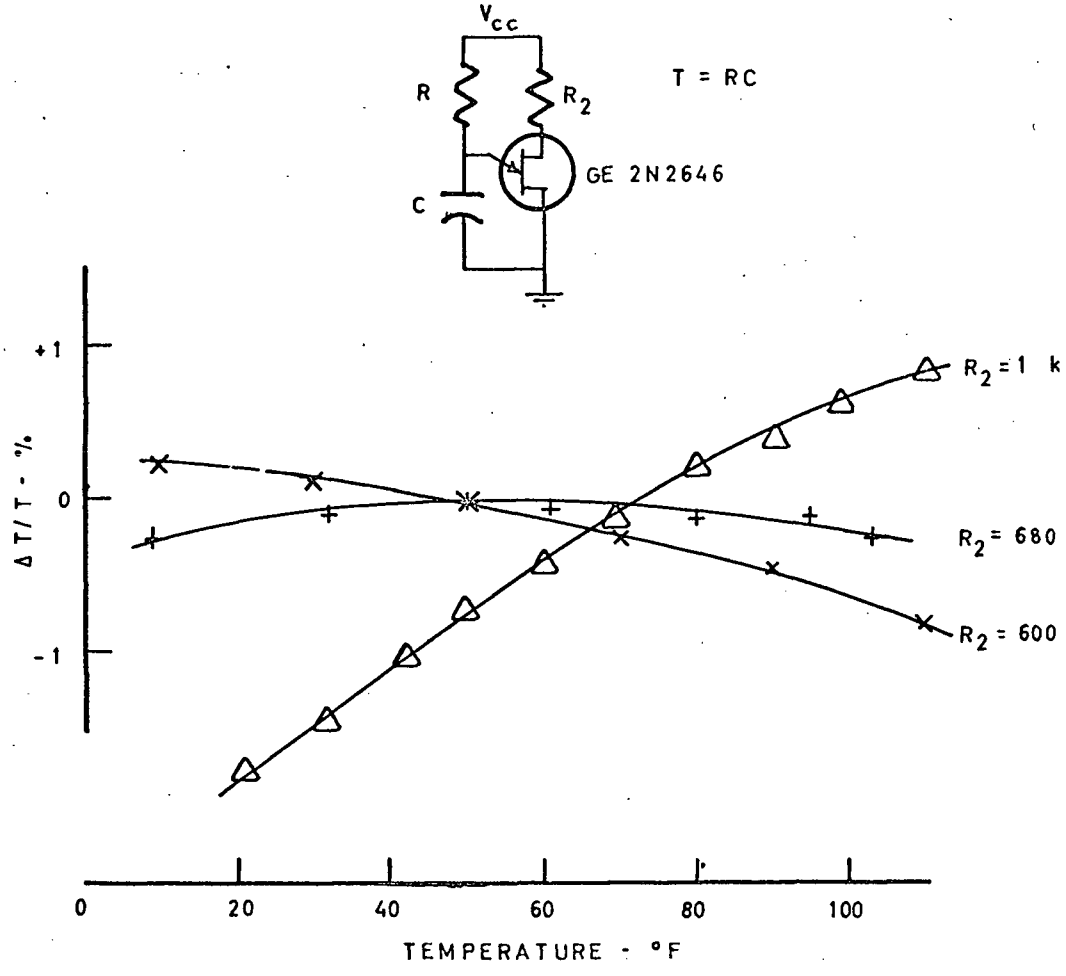
The readout cycle was chosen to occupy 8 clock periods. Thus the output code has 8 bits, where the first bit carries no information and is set to zero. (This extra bit is utilized in the decoder to recover the clock.) The circuit used for the programmer is a binary counter counting to 12 and resetting itself. The first



6.4 Circuit Diagram of Encoder

four states of the counter are used to generate the ramp, and the last eight to read out the code. A detailed circuit diagram of the whole system (i.e. the encoder) is shown in Figure 6.4.

The encoder is implemented using integrated circuits (IC) throughout. Fairchild linear IC's are used for the integrator and comparator, and Motorola plastic IC's are used for the digital logic. The only discrete circuit is the master clock, which is a unijunction oscillator feeding an IC flip-flop. The oscillator's frequency is stabilized against temperature variations by adjusting the base-two resistance as shown in Fig. 6.5.



6.5 Frequency Deviation of UJT Oscillator due to Temperature Variation

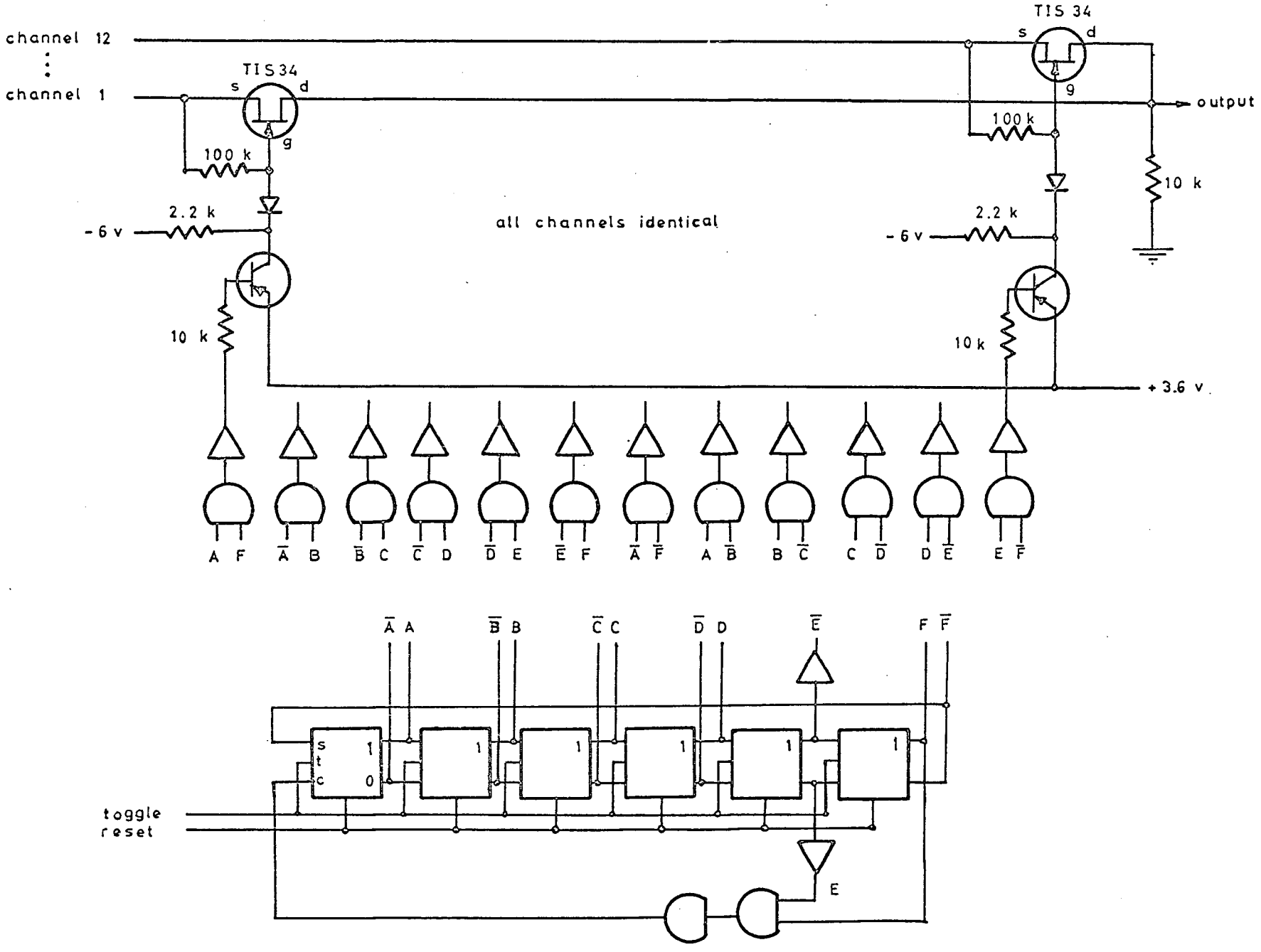
6.1.2 The Commutator

Since several channels of information are to be recorded on a single track of tape, time multiplexing is used. This function is performed by the commutator, which assigns adjacent time slots in sequence for the various channels. The sequencing is synchronized with the encoder programmer, such that the operating channel is switched after each conversion cycle.

The twelve channel commutator used in this system consists of a twelve-state counter, one-out-of-twelve decoding circuits and switches.

A shift counter is used, since it simplifies the decoding and minimizes the number of interconnections between the gates of the decoding circuit. The counter is a shift register with inverse feedback as shown in Figure 6.6. Since the counter uses only 2N out of a possible 2^N states, different modes of counting may appear if it accidentally enters one of the unassigned states. These modes are stable, and hence extra gating is used in the feedback circuit to supress them.[11] The fundamental counting mode is tabulated in Figure 6.7, together with the decoding function, and it is seen there that only one two-input NOR gate is required to decode each state of the counter.

The switches use N channel field effect transistors (FET) with a negative pinch off voltage of less than 6 volts. A switching transistor is used to provide the required +3.6 and -6 volts, operated from an extra inverter after the NOR gate. (See Figure 6.6). A diode isolates the FET from the switching source and the source to



6.6 Circuit Diagram of Commutator

COUNT	A	B	C	D	E	F	DECODING
0	0	0	0	0	0	0	$\overline{A}.\overline{F}$
1	1	0	0	0	0	0	$A.\overline{B}$
2	1	1	0	0	0	0	$B.\overline{C}$
3	1	1	1	0	0	0	$C.\overline{D}$
4	1	1	1	1	0	0	$D.\overline{E}$
5	1	1	1	1	1	0	$E.\overline{F}$
6	1	1	1	1	1	1	A.F
7	0	1	1	1	1	1	$\overline{A}.B$
8	0	0	1	1	1	1	$\overline{B}.C$
9	0	0	0	1	1	1	$\overline{C}.D$
10	0	0	0	0	1	1	$\overline{D}.E$
11	0	0	0	0	0	1	$\overline{E}.F$

6.7 Fundamental Counting Mode for a Six Stage Shift Counter

gate resistor of the FET assures that these are at the same potential when the gate is on.

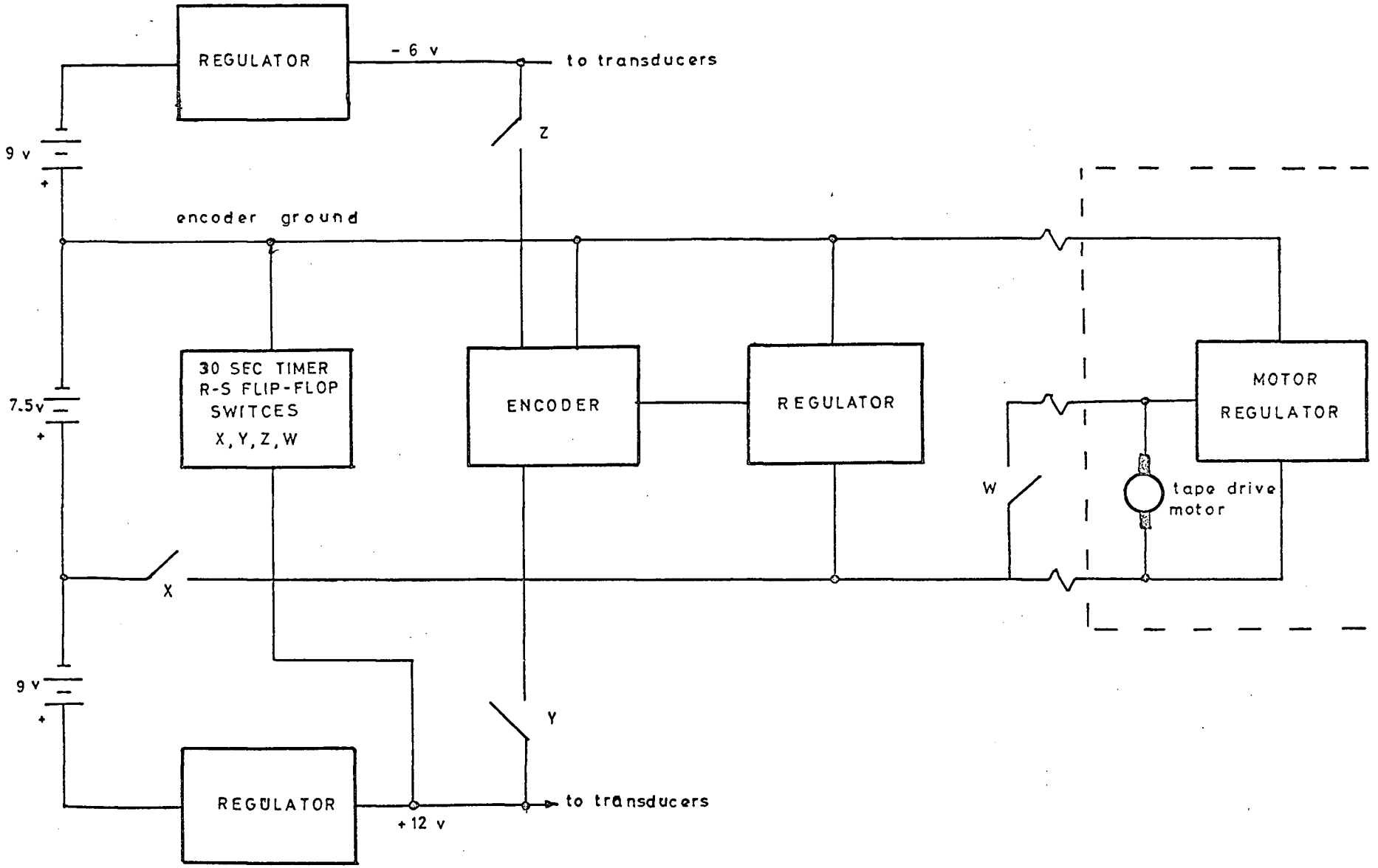
6.1.3 Power supplies and Switching Circuits

The overall system, i.e. the encoder and the recorder, is a portable unit operating from small batteries. To achieve the low power and tape consumption necessary for long term operation, the slowly varying nature of the input is utilized. The input variables are sampled every 30 seconds, and the recorder and encoder are turned off between samples. This is made possible by the fast response of the tape drive motor, which takes approximately

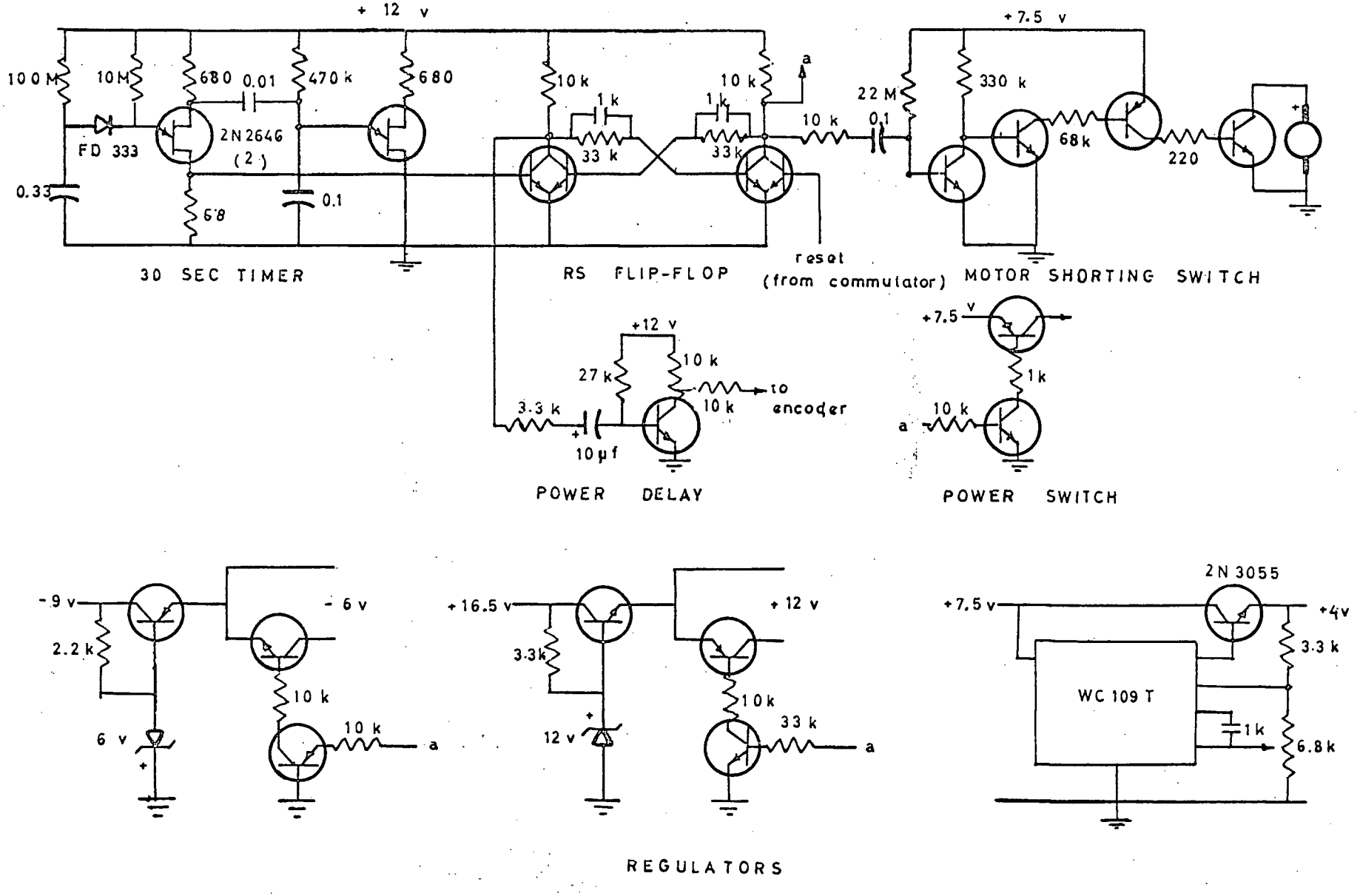
200 milliseconds to come to full speed. After the data is recorded the power is turned off, and the motor is stopped by electronically placing a short circuit across it. (This is used as a dynamic brake). The d-c series motor used can be stopped in about 50 milliseconds in this way. Thus the total time taken to record 12 channels of information is 200 + 12 x 24 + 50 = 538 millisec., and the duty cycle is approximately 1/60. A tape cartridge having 30 minutes of tape will therefore last for about 30 hours, and the batteries' life is correspondingly increased to about 40 hours for alkaline type C cells. This was confirmed by field trials.

The power supplies are derived from 5 C cells (since the recorder operates on 7.5 volts) plus two 9 volt batteries. The tape drive motor has its own regulator, and the encoder uses three regulators to obtain +12, -6, +3.6 volts..

A timing circuit is on all the time. This circuit provides a timing pulse every 30 seconds. At this time the power is turned on, starting the recorder and actuating the encoder. A delay is also initiated during which the encoder output is held at zero. (This time is to allow the motor to come to full speed.) After the delay terminates, the 12 inputs are encoded in turn. The reset pulse of the last channel is then used to turn the power off. A second delay circuit is used to place a short circuit across the motor for a short time after the power is turned off, to stop it quickly. This circuit is connected to the batteries directly, but draws no power except when the delay is on. A block diagram of the various switching circuits and power supplies is shown in Figure 6.8, and a detailed circuit diagram in Figure 6.9.



6.8 Block Diagram of Power Supplies and Switching Functions



6.9 Circuit Diagram of Power Supplies and Switching Functions

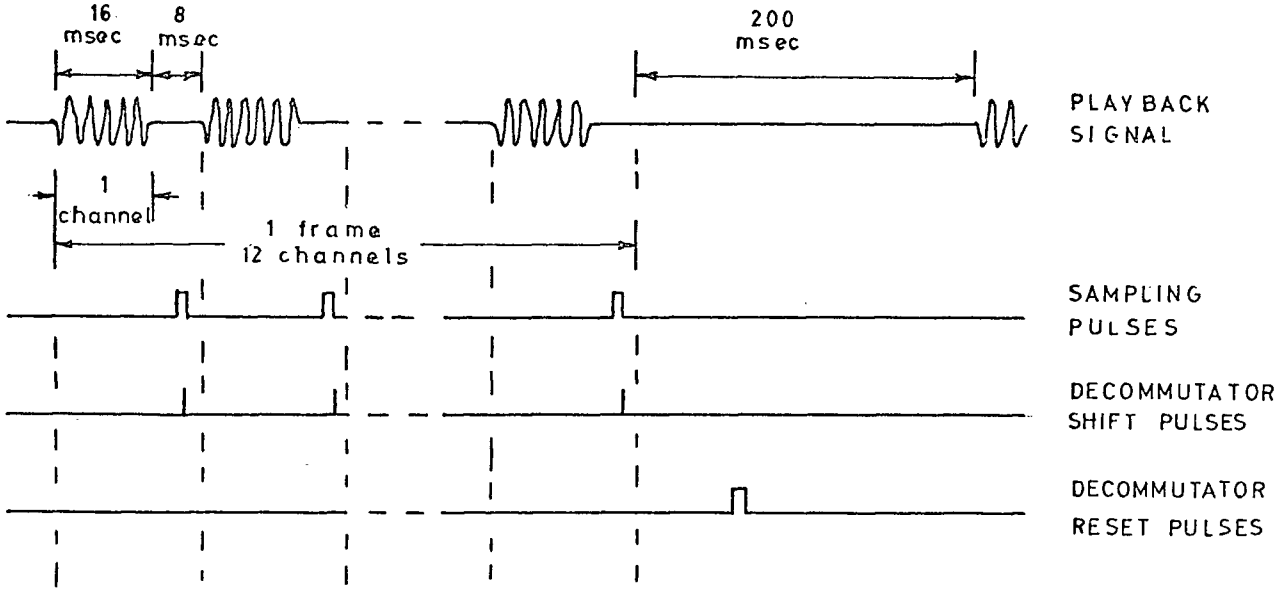
The 30-second timer is a two stage unijunction transistor oscillator.[10] The long time constant is obtained by using a 100 megohm precision resistor to charge a 0.33 μf capacitor. This large resistance presents a serious problem due to reverse leakage currents. The effective voltage to which the capacitor charages is reduced by the leakage current times the charging resistor. Since the leakage current increases 10% for every 1°C increase in temperature, it has to be kept low if precise timing is required. Therefore a very low leakage diode (having a leakage current less than 1 nanoamp at 25°C) is used to isolate the resistor from the emitter. The transistor is biased at its peak point by a second resistor, which also reverse biases the diode. The necessary current to trigger the unijunction is obtained from the capacitor by momentarily lowering the base two voltage, and hence the trigger point. This is achieved by pulsing the base two with a second oscillator that free runs at a much higher frequency than the first. The junction voltage variations with temperature are cancelled by selecting the proper value of base two resistance. In this way 1% accuracy is achieved, making it possible to determine the time base of the recorded data by simply counting the number of sample points. A circuit diagram of the timer is included in Figure 6.9.

6.2 The Playback System

The playback equipment performs the function of transforming, upon playback, the digital data recorded on tape into analog output voltages. Since there is only one playback system and it is operated in the laboratory, there is less need here to be concerned with size, economy, temperature variations and power

consumption.

Before describing the playback system, it will be helpful to consider the nature of the playback signal. Each channel input sample corresponds to a group of pulses lasting 16 milliseconds. These groups are separated by an 8 millisecond conversion interval during which the signal is zero. There are 12 such pulse groups per frame, each group corresponding to one of the twelve input channels. Adjacent frames are separated from each other by a larger interval that occurs while the recorder is being turned on and off between samples. (See Chapter 6.1.4). These features of the playback signal are used to provide both channel and frame synchronization pulses to the decommutator, as shown below. The various time intervals of the playback signal are shown in Figure 6.10 together with the channel and frame sync pulses.



6.10 Typical Playback Signal, Sampling, Shift and Reset Pulses

A block diagram of the playback system is shown in Figure 6.11 and a detailed circuit diagram in Figure 6.12. The overall operation of the system will now be discussed with reference to Figures 6.10 and 6.11. The operation of the individual blocks is discussed in detail later.

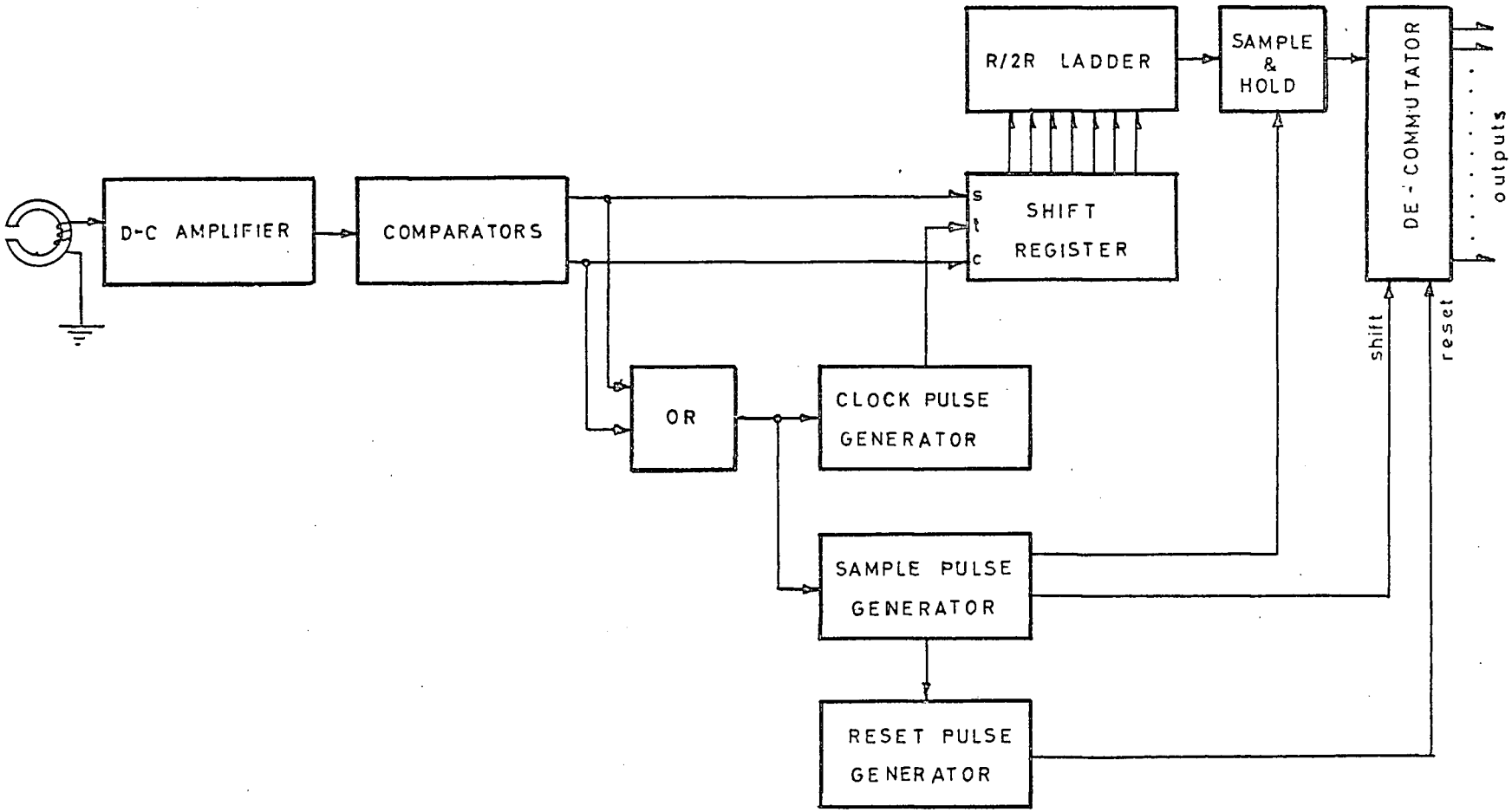
The amplified output pulses are fed to a decision circuit that recognizes positive and negative pulses. These are then fed to the set and reset terminals of a seven bit shift register. The clock is derived from the data by the clock pulse generator and is fed to the toggle input.

The register performs several functions. It effectively "integrates" the playback signal to recover the phase modulated code, transforms it into the binary code and stores the seven bits for readout. The register outputs are decoded by a ladder type digital to analog (D/A) converter. The converter output feeds a sample and hold circuit, which is connected to the decommutator. (The latter is identical to the commutator, connected in reverse.)

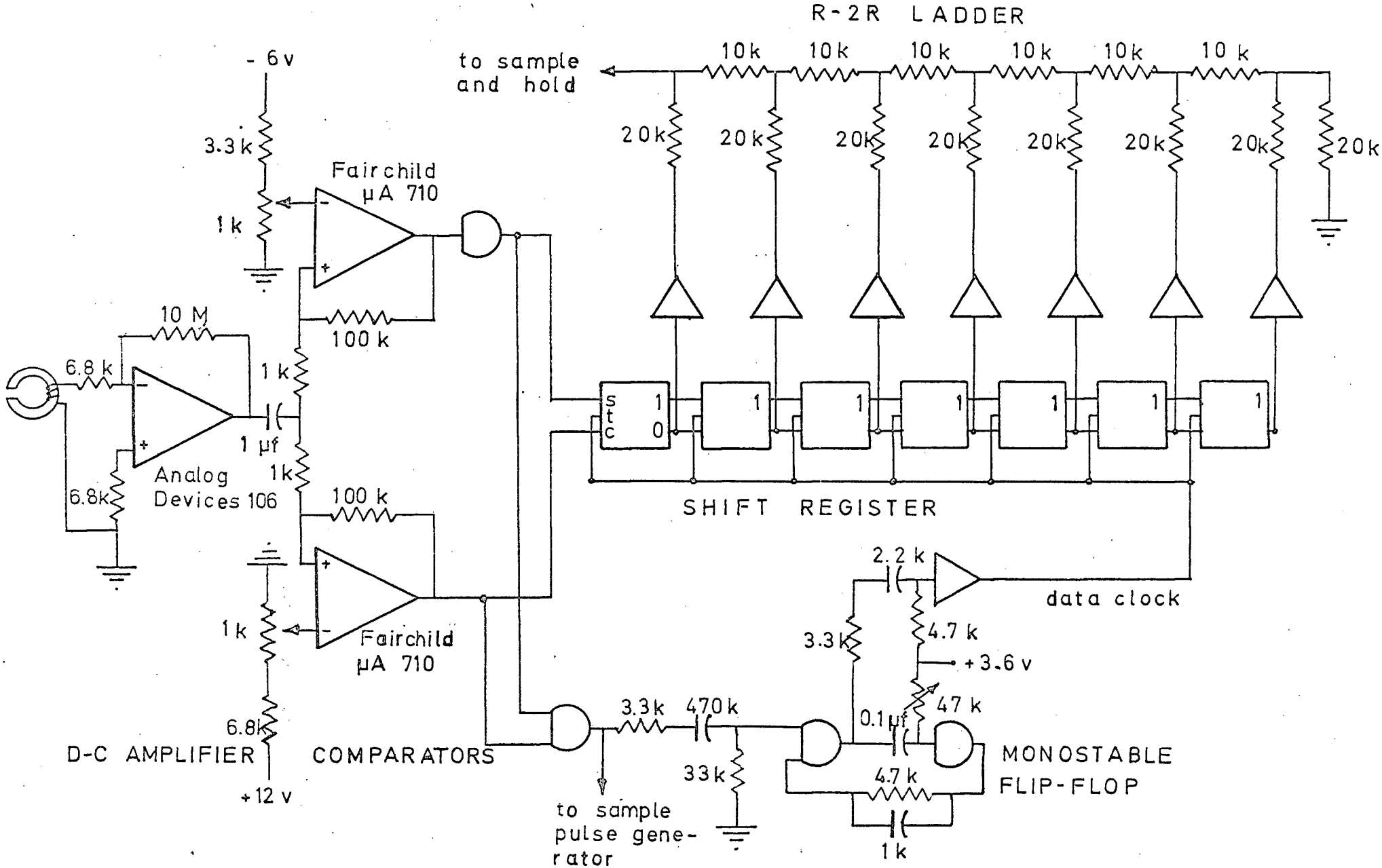
The sampling pulse is generated during the conversion interval between the individual pulse groups. (See Figure 6.10). The decommutator shift pulses are also generated at this time, providing proper channel synchronization. Finally a reset pulse for the decommutator is generated during the longer pause between frames, assuring proper frame synchronization. The relationship of the sample pulses, the shift pulses and the reset pulses to the playback signal is indicated in Figure 6.10.

6.2.1 The Integrator

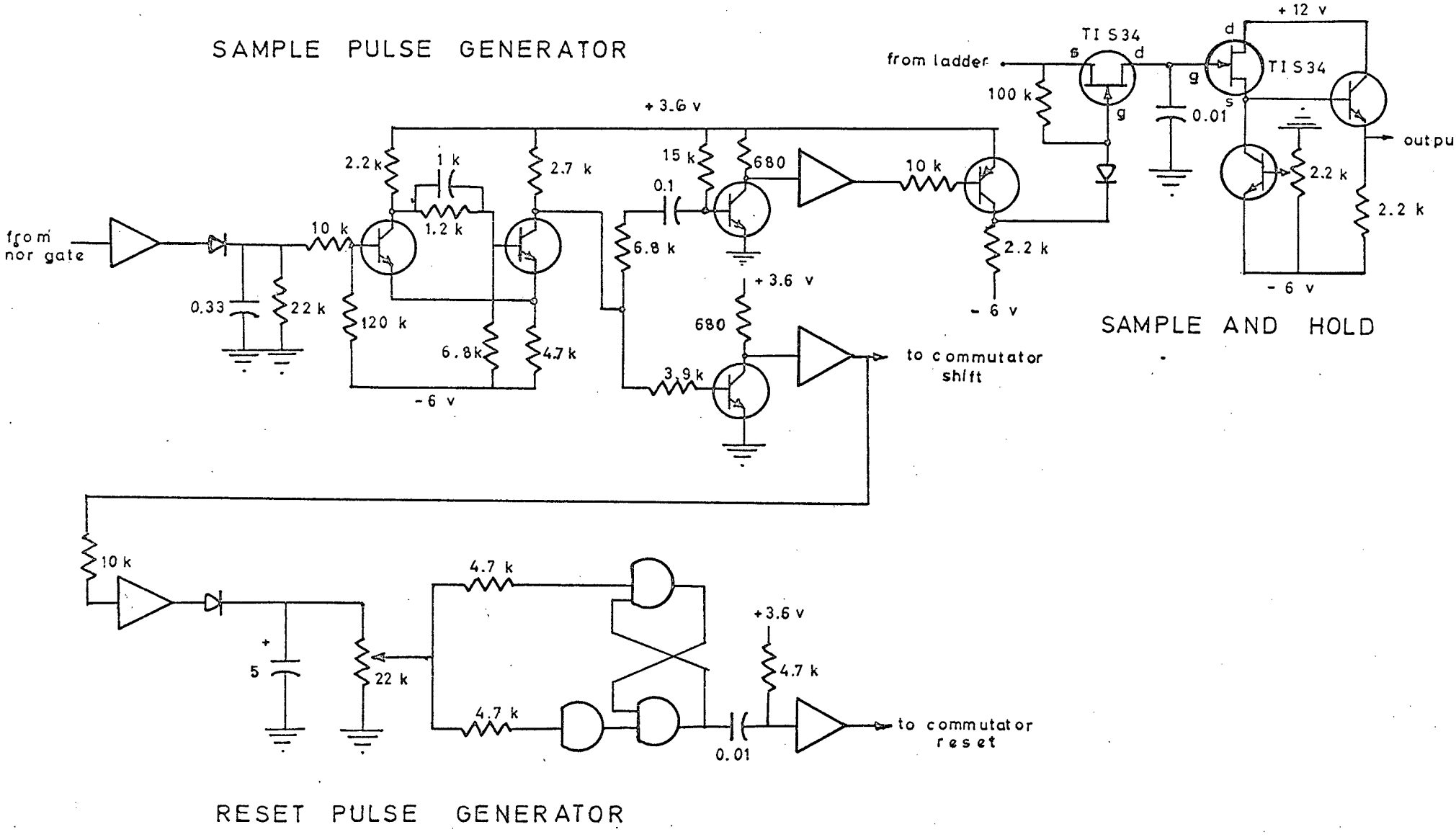
As explained in Chapter 4, the playback signal is a



6.11 Block Diagram of the Playback System



6.12 Circuit Diagram of the Playback System



6.12 Circuit Diagram of the Playback System (cont'd)

"differentiated" version of the recorded waveform. The decoding equipment therefore has to perform the inverse operation, namely integration. Although this is readily achieved in an analog manner, amplitude variations among the individual playback pulses cause base-line shifts that make the decision as to pulse polarity difficult. A digital method of integrating the output pulses is therefore used in this case, since it is completely independent of output pulse amplitudes.

The "integration" is readily performed by a flip-flop if positive pulses are fed to the set and negative pulses (after inversion) to the reset terminals. In this way the phase modulated code is recovered. To recover the binary code, we recall from Fig. 6.2 that in the phase modulated code only transitions coincident with negative transitions of the readout clock are significant. Therefore a clocked (JK) flip-flop is used to perform the integration. Only input pulses coincident with the clock can change the state of the flip-flop. Therefore the extra transitions inserted into the phase modulated code are ignored, and the binary code is recovered. The proper clock pulses are derived from the data itself, as will be shown below. These relations are evident in the decoding waveforms of Figure 6.13, which is a scope tracing of the (inverted) playback signal, the flip-flop reset and set inputs and the flip-flop output.

6.2.2 The Digital to Analog Converter

The binary code is recovered serially, starting with the least significant bit. These bits are shifted into a 7-bit register as they are read from the tape. The integrating flip-

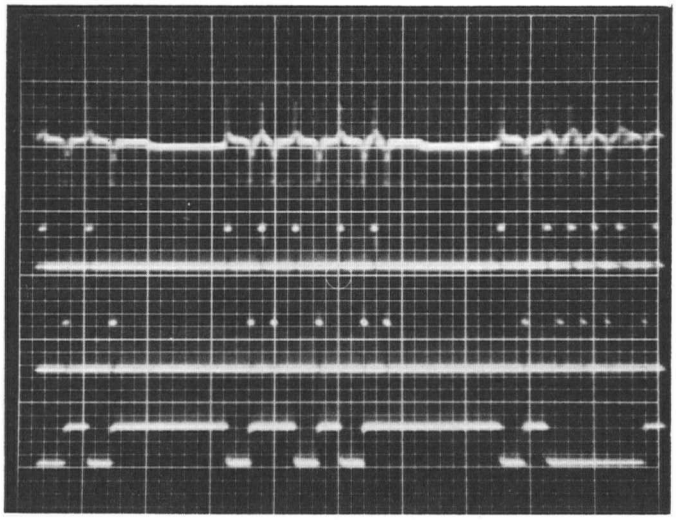


Figure 6.13 Typical Decoding Waveforms
Horizontal scale: 5msec/cm
Vertical scale: 5v/cm

flop is also the first stage of the register, and the data clock is the shift pulse. At the end of each code group the register thus contains the seven most significant bits of that group. (The first bit in the group carries no information and is shifted out at the end.)

The contents of the register are stored during the pause between code groups. As we shall see this interval is used to sample the decoded output.

The register outputs are buffered and decoded by an R-2R ladder network, as shown in Figure 6.12. It can be shown that the open circuit output voltage of such a network is[7]

$$V_{oc} = \frac{p}{2^n} V \qquad (6.2)$$

where p is the number being decoded

n is the number of bits

V is the supply voltage

Since the output inpedance of the network is R, the output across some load R_L is

$$V_o = V_{oc} \frac{R_L}{R + R_L} \qquad (6.3)$$

The maximum output voltage error due to resistor inaccuracy can be shown to be bounded by 0.7 times the voltage per bit for the case of 1% resistors and seven bits.[12] This corresponds to an error of 0.55% of the maximum output voltage.

The output of the ladder network is sampled during the pause between the code groups, as mentioned above. A field effect transistor (FET) performs the sampling, and the sampled value is held by a capacitor. An FET source follower, fed from a transistor current source, is used to isolate the holding capacitor, and the output is buffered by an emitter follower. (See Figure 6.12).

6.2.3 The Sync Pulse Generators

The sampling pulses and the decommutator shift and reset pulses are all derived from the data. This is achieved without the use of extra synchronization pulses to identify the channels and frames, the different duration pauses between adjacent channels and adjacent frames being used instead.

The pause between the different channels is identified

by integrating the pulse groups corresponding to the channels and applying the output to a Schmitt decision circuit. A short sample pulse is then generated between the groups by a delay circuit, and the Schmitt output is buffered to give the commutator shift pulse. (See Figure 6.12).

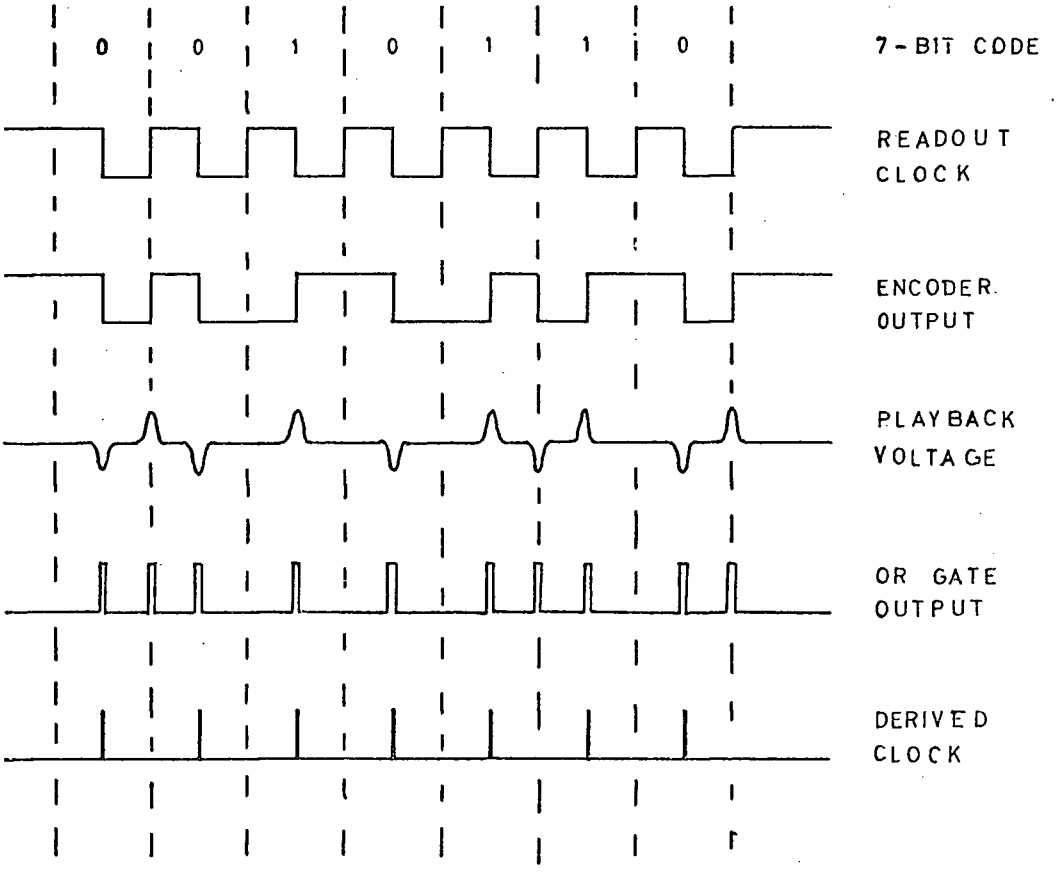
The larger pause between frames is identified in a similar manner. Thus the Schmitt output is integrated this time, and the result is applied to a second, integrated Schmitt circuit. A short reset pulse is then generated between the frames by a delay circuit, as shown in Figure 6.12.

6.2.4 The Data Clock Generator

As mentioned earlier, a major advantage of the phase modulated code is that the clock pulses are derivable from the code. Thus if the negative output pulses are inverted and combined with the positive ones, the resultant pulse train will contain two frequencies: the clock frequency and twice the clock frequency. An oscillator can therefore be synchronized to the lower of these two frequencies, ignoring the higher. This is readily achieved by a monostable multivibrator, with a delay set equal to 3/4 times the data clock period. Pulses at twice the data clock period are therefore ignored, and furthermore, the monostable will stay locked to the data clock for tape speed (and hence frequency) variations of up to 25%. (Larger speed variations can be tolerated if a phase-lock loop is used, but the extra complexity is not warranted in this case.) In order to achieve precise and clean triggering, the output pulses are differentiated before being

applied to the multivibrator.

Proper synchronization is still a problem. Thus we must make sure that the first trigger pulse of the multivibrator corresponds to a negative transition of the encoder readout clock, since only these transitions carry data information. This is achieved by inserting an extra pulse at the beginning of each code group, this pulse being always zero. Therefore the encoder output is made always high between code groups. The first transition is then always negative and coincides with a negative transition of the encoder readout clock. Thus the first pulse in the code group becomes the first clock pulse, and the data is always synchronized with the clock. These relations are made clear by the timing chart of Figure 6.14.

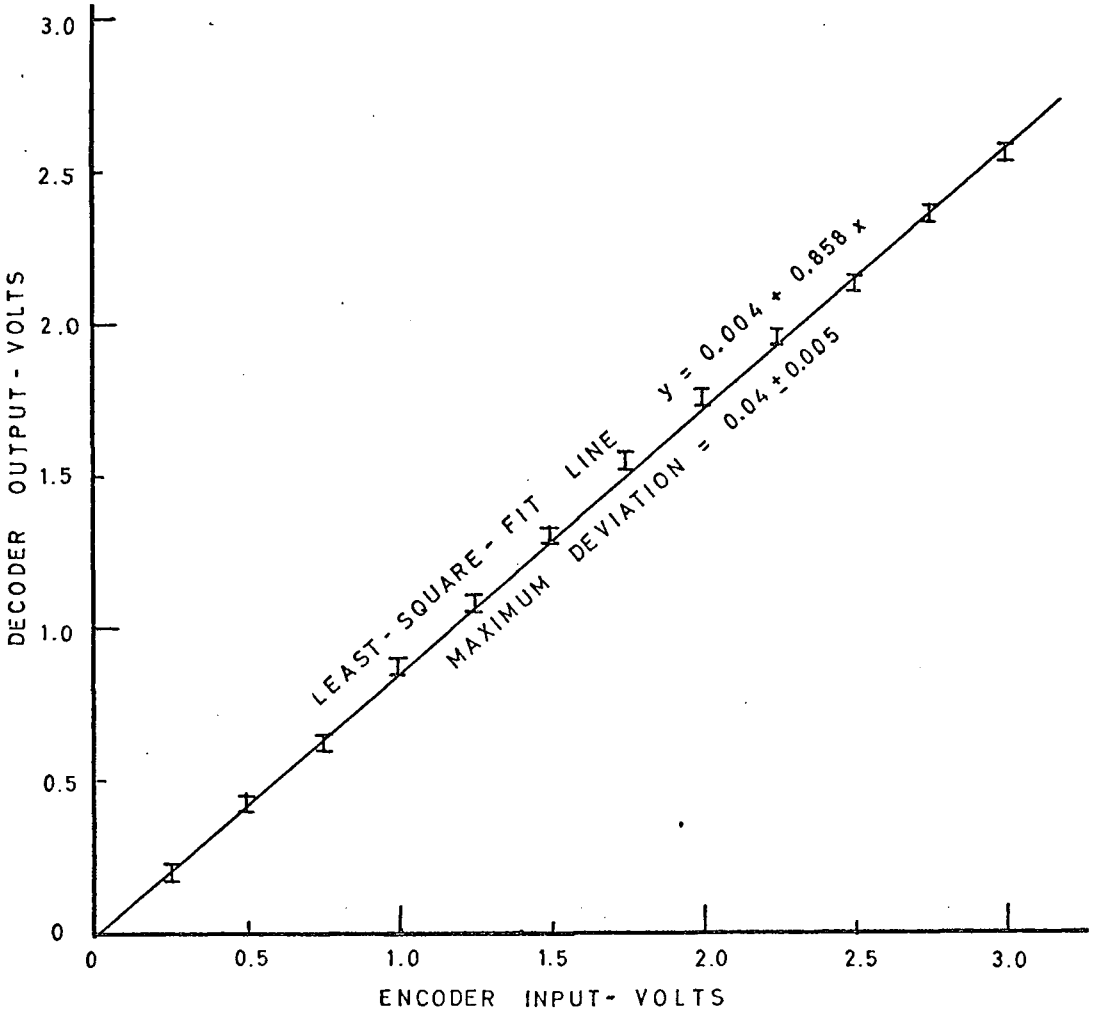


6.14 Derivation of the Data Clock

6.3 Results

A prototype of the system, including the input commutator, the encoder, the tape recorder, the decoder, and the output commutator, were extensively tested in the laboratory. The results of these tests are summarized below.

First a calibration curve of the system, from encoder to decoder, was obtained. The recorder was removed and the encoder output was differentiated to simulate the recording process. A known d-c voltage was then applied to the encoder input, and the corresponding decoder output was measured by a digital voltmeter. The result of this test is the calibration curve of Figure 6.15.



6.15 Calibration of the System

In the second test a single channel was used to record a linear ramp from a signal generator. The ramp amplitude was 3 volts, and the repetition frequency 0.05Hz. The tape was then played back and the output decoded, giving the scope tracing of Figure 6.16.

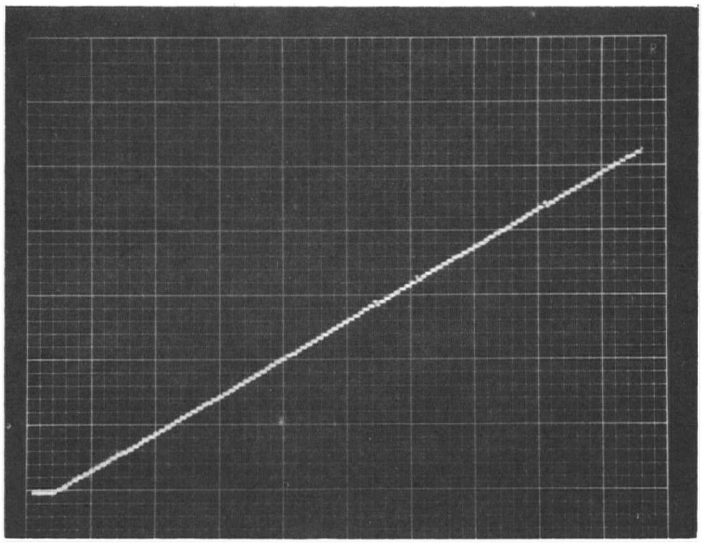


Figure 6.16 Decoder Output for Linear Ramp Output
Horizontal scale: 1 sec/cm
Vertical scale: 0.5 v/cm

Here the individual steps of the quantization process are clearly visible. We also see that there is an occasional deviation of one step size, or one bit. This occurs during the encoding quantization process, and is due to noise fluctuations of the input voltage. The frequency with which these deviations occur is a function of the ratio of the RMS voltage fluctuation of the input to the size of one quantization interval.

Finally the complete system was tested using six channels. Three channels were set to zero, and the others had a sine wave, a ramp and a d-c voltage as inputs. These are shown in Figure 6.17 where the time multiplexed version is also included. The time multiplexed waveform was encoded and recorded on tape. After playback and decoding they appeared as shown in Figure 6.18, where the top tracing is the multiplexed output. Due to the operation of the commutator each output channel has a negative baseline between samples, as can be seen on Figure 6.18.

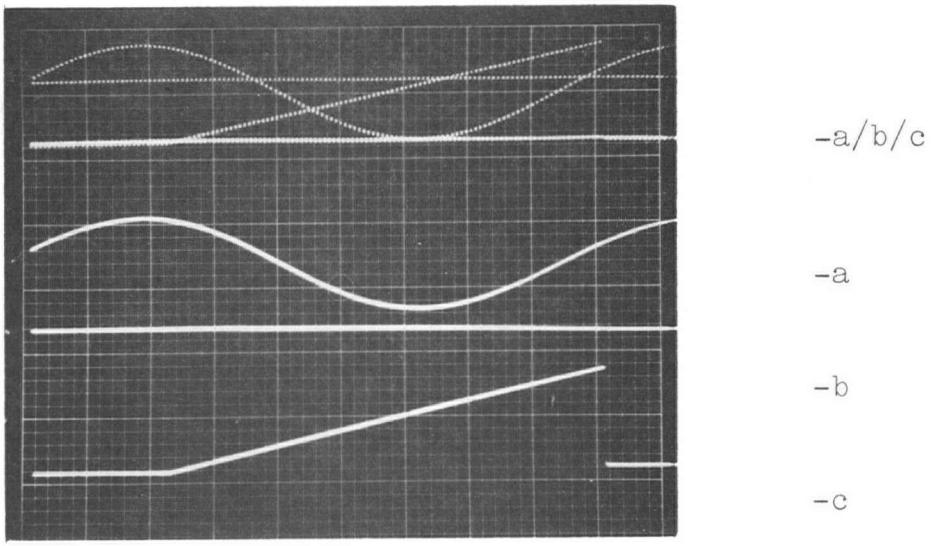


Figure 6.17 Encoder Input Test Voltages
Horizontal scale: 2 sec/cm
Vertical scale: 2 v/cm

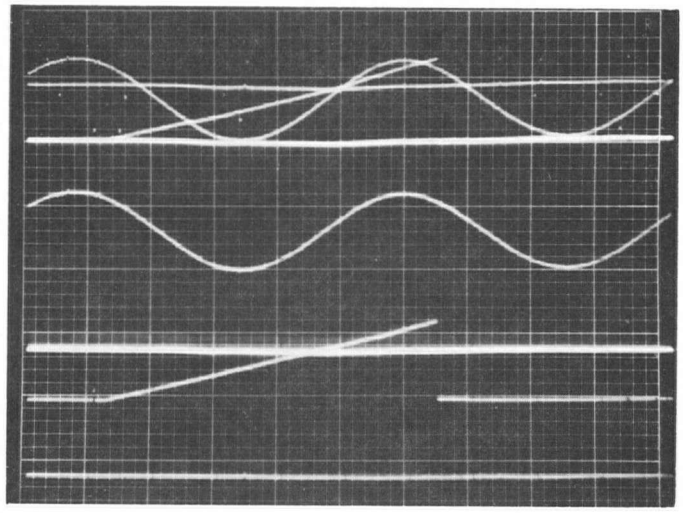


Figure 6.18 Decoder Outputs for Test Voltages

Horizontal scale: 5sec/cm
Vertical scale: 2v/cm

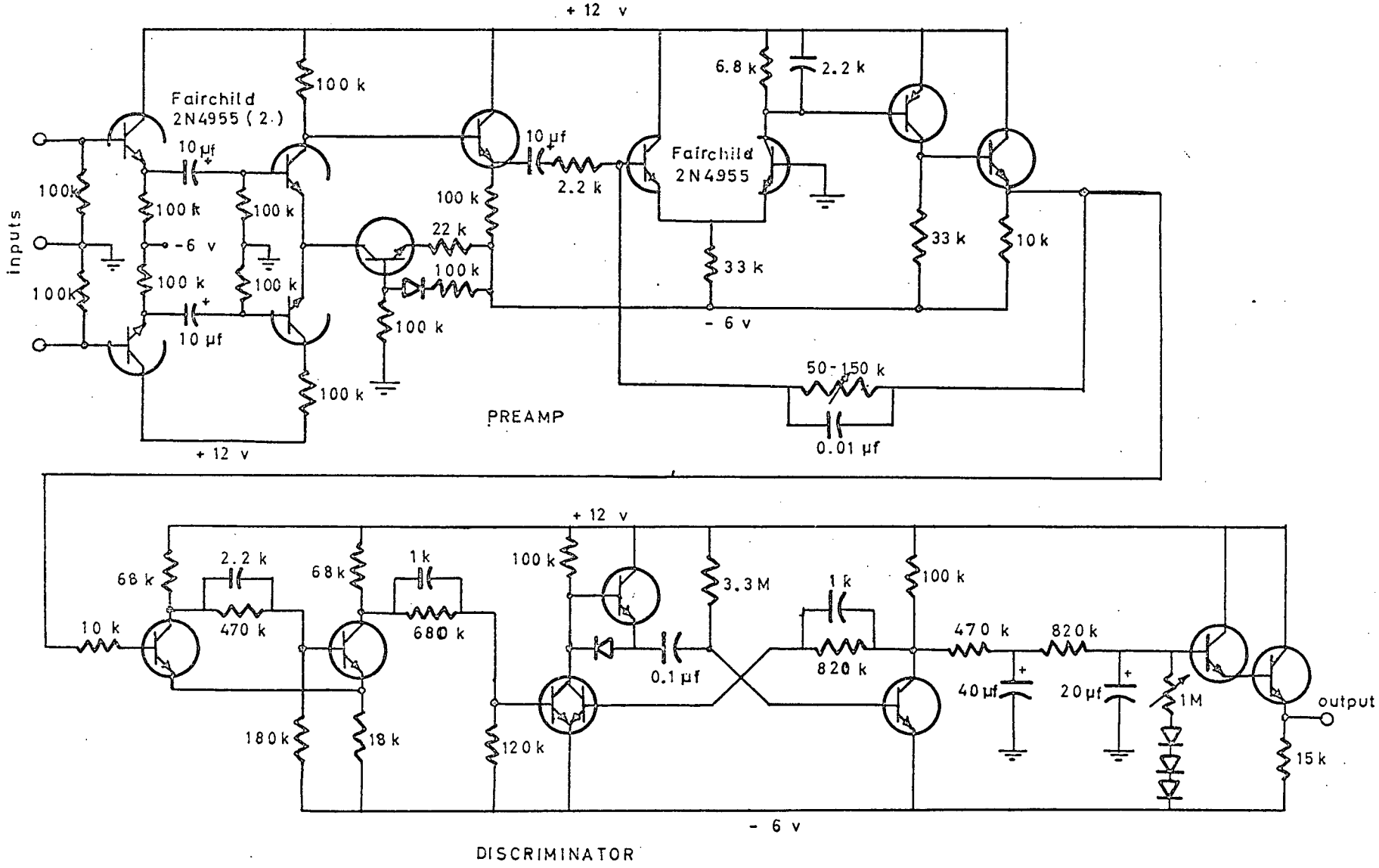
7. THE INPUT TRANSDUCERS

7.1 The Heart Rate Transducer

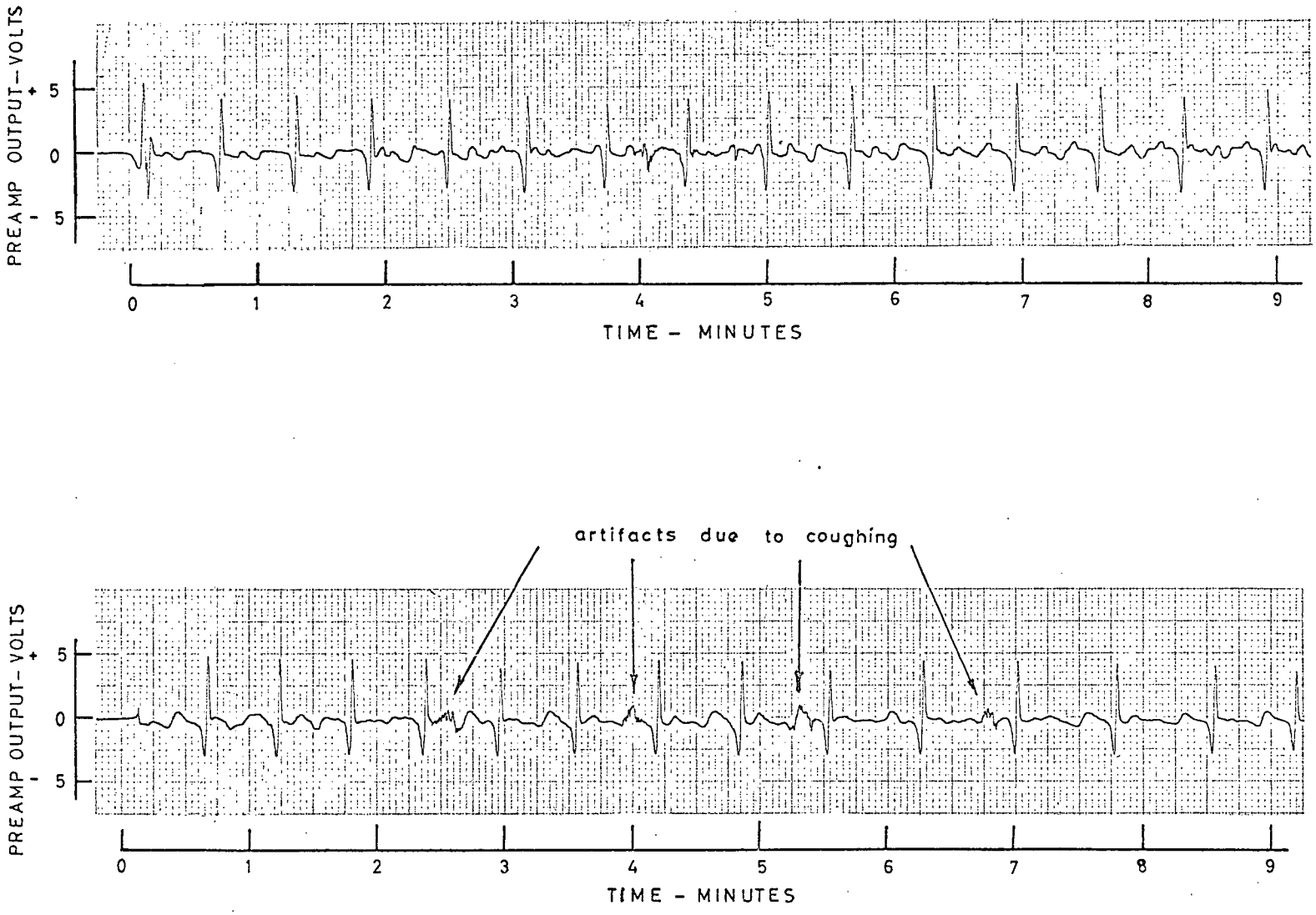
This transducer produces a voltage proportional to the average heart rate. A standard electrocardiograph (ECG) voltage is first obtained by means of chest electrodes and a preamplifier. A discriminator (frequency to voltage converter) transforms the pulse rate to a voltage, which is averaged over a 30 second interval.

The electrodes used were the Beckman silver-silver chloride low artifact type. The impedance between two of these when attached with proper preparation to the skin was measured to be 10 Kohms. To minimize pickup of signals from muscles other than the heart, the best positioning of the electrodes is on the sternum and between the 4th and 5th ribs just below and to the left of the heart. A third, ground electrode was found to reduce noise when placed close to the second electrode (between the ribs). The electrode position was found to be fairly critical, but muscle artifacts were not excessive even during strenuous exercise, once the proper placing was found, as shown by the tracings of Figure 7.2. Amplitude variations between six subjects were found to be quite small.

The preamplifier uses a circuit developed by NASA,[13] shown in Figure 7.1. It consists of symmetrical emitter follower input stages giving high input impedance. A differential pair fed from a transistor current source forms the first stage of amplification. An emitter follower isolates the second stage from the first. The second stage consists of a single ended differential amplifier followed by a common emitter stage. An emitter follower buffers the output, and local feedback is used to stabilize the



7.1 Circuit Diagram of the Heart Rate Transducer

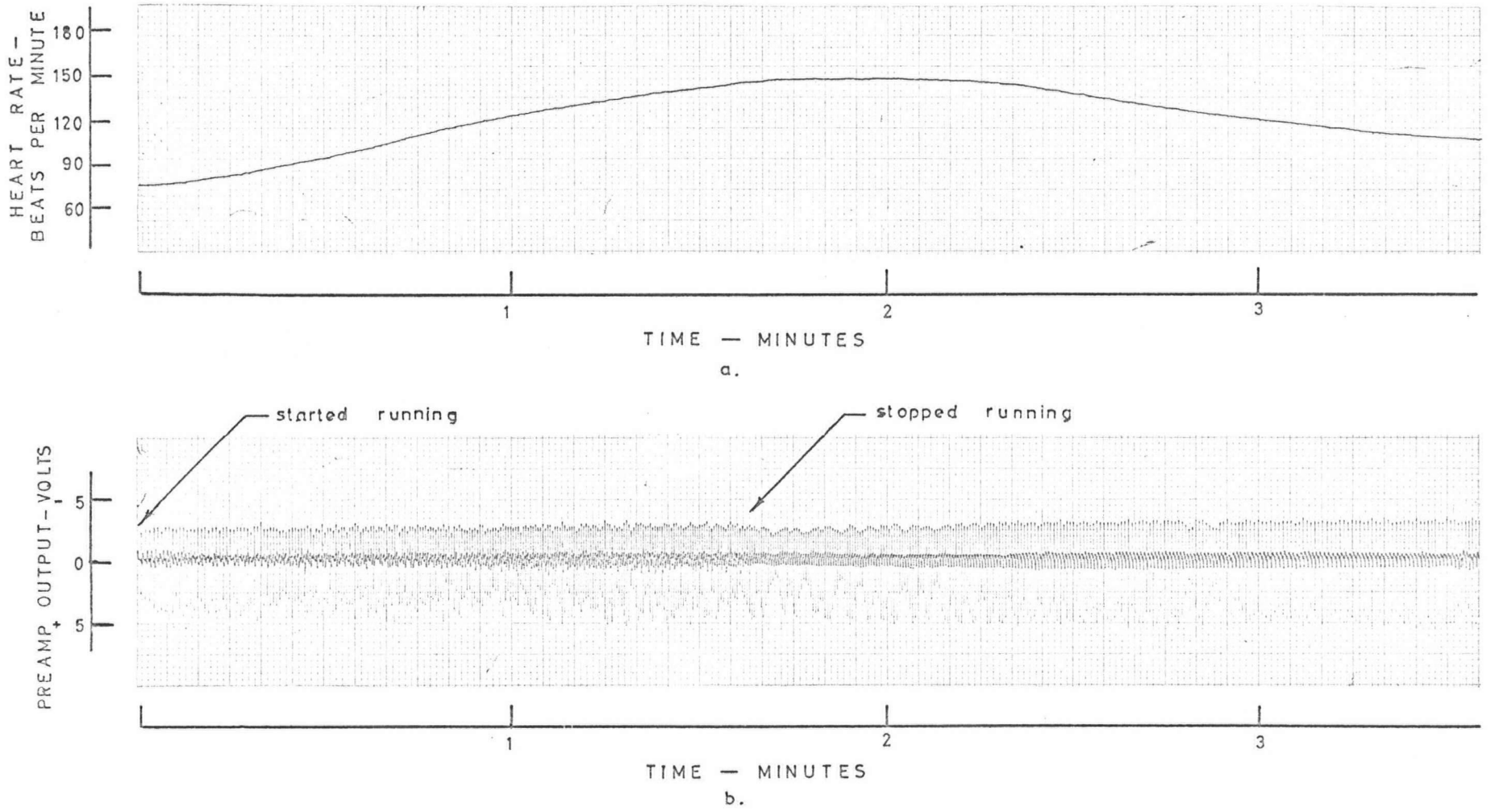


7.2 Typical Preamp Outputs (ECG's) of two Exercising Subjects

gain of the second stage. The gain is variable to permit adjustment of the output level for different subjects. The amplifier gives zero volts output for no input. Its characteristics are summarized in the following table:

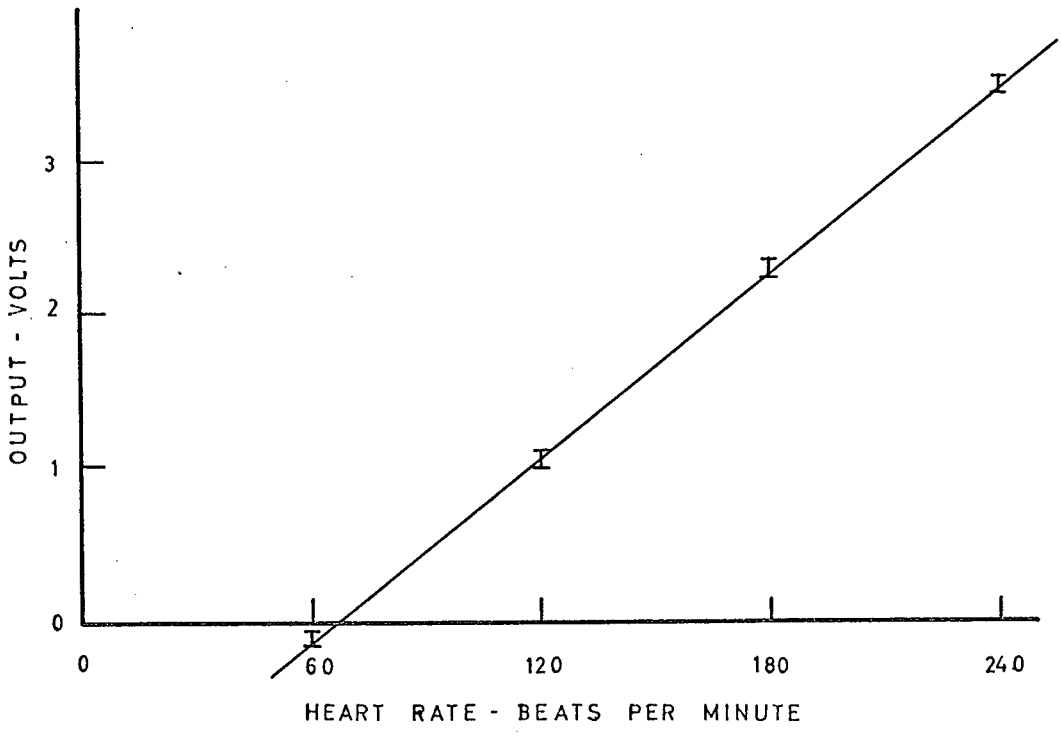
Differential input impedance	2megohm
Differential gain	1000 - 6000
Common mode rejection ratio	74 dB
Output impedance	100 ohm
Battery power	20 mwatts
Frequency of response	1 - 1000 Hz (3 dB)

The second part of the transducer is a discriminator followed by an averaging circuit, also shown in Figure 7.1. Since the records were found to be remarkably clean, simple amplitude clipping by a Schmitt circuit is used to eliminate the base line noise. (A phase-locked discriminator was considered in detail,[14] but was found to be unnecessary due to the high signal-to-noise ratio in the heart signals. Furthermore, it was difficult to construct a circuit that would cope with the large range of possible heart rates.) The Schmitt output is a set of sharp pulses which are fed into the discriminator, a modified one-shot flip-flop. (The collector of the input transistor is isolated from the timing capacitor by a diode, and the capacitor is recharged through an extra transistor. This reduces the recovery time of the flip-flop by a factor equal to the small signal gain of the transistor.) The delay time of the flip-flop is adjusted to be approximately 1/4 sec., which is less than the shortest expected heart beat period. The output of the flip-flop is a "square wave" with a duty cycle and a d-c com-



7.3 a. Averaged Heart Rate, b. Condensed ECG of Active Subject

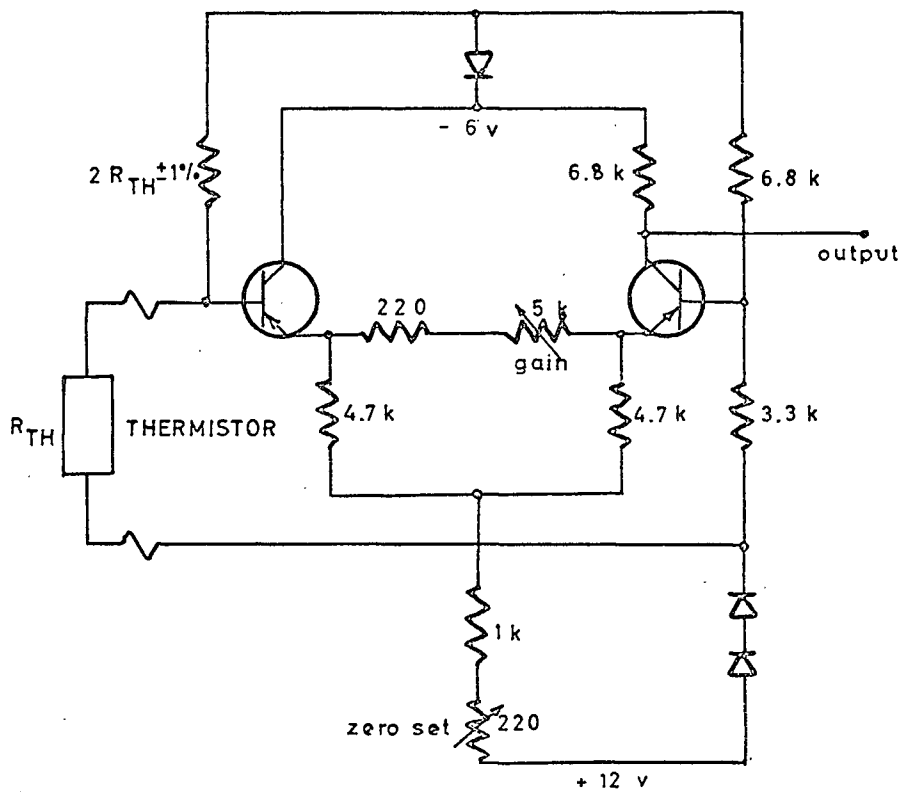
ponent which is a linear function of the input frequency. This square wave is then filtered and averaged over a 30 second interval. Finally it is level shifted and buffered to give the required output voltage range. A typical record of the output is shown in Figure 7.3, where a condensed version of the preamp output is also included. The calibration curve of the transducer is plotted in Figure 7.4.



7.4 Calibration of Heart Rate Transducer

7.2 The Temperature Transducer

This transducer monitors the skin temperature by means of a small thermistor taped to the skin. A Wheatstone bridge arrangement is used, the output being amplified by a differential amplifier. The bridge is initially balanced to within 1% by selecting the proper resistor, as indicated in Figure 7.5. A fine zero set adjustment



7.5 Circuit Diagram of Temperature Transducer

is then used to cancel any residual unbalance. A separate, orthogonal adjustment is available to set the gain, which is variable between about 10 and 70. Thus the output is adjusted to swing between 0 and 3 volts for the required input temperature range. For most purposes, this was chosen to be from 35°C to 40°C.

The effect of temperature variation of the base to emitter voltages (v_{BE}) is compensated for by using diodes in the supply lines as shown in Figure 7.5. Referring to the circuit values indicated we see that when the bridge is balanced and the zero set pot is 50 ohms, the output voltage is

$$v_D = \frac{12 - (v_B + v_{BE})}{6.8k} \times 6.8k - 6$$

$$= 6 - v_B - v_{BE}$$

and

$$v_B = (12 - 2v_D) \times \frac{6.8}{10.1} - (6 - v_D) \times \frac{3.3}{10.1}$$

$$= 6.1 - 1.0\ v_D$$

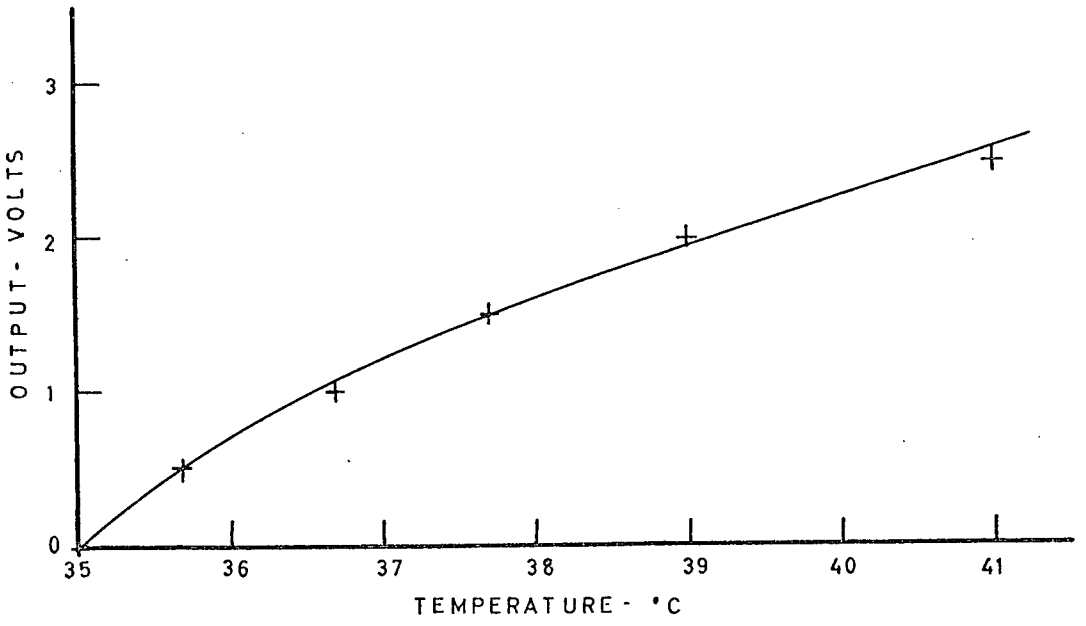
where v_B is the voltage at the base of Q_2

v_D is the diode voltage drop

since $v_{BE} \approx v_D$

we have that $v_o \approx -0.1$ volt

and the output is independent of temperature to a first approximation. The small output offset can now be reduced to zero by adjusting the zero-set pot. In tests it was found that the output was not a function of circuit temperature after an initial warm up period, over the temperature range 0°F to 70°F. A caliabration curve of this transducer is shown in Figure 7.6.



7.6 Calibration of Temperature Transducer

8. CONCLUSIONS

A novel concept of monitoring slowly varying parameters, involving the use of local digital recording, plastic integrated circuits, and low duty-cycle operation, has been implemented. An early prototype of the monitoring and recording equipment was field tested in Alaska during January 1968. A more complete prototype, including the playback decoding equipment and two types of physiological transducers was extensively tested in the laboratory.

These tests confirmed that the equipment will function in the field in the arctic, that it has the low power consumption necessary for long term operation, that it is accurate to 1%, and that the transducers function as specified.

Further work is still necessary, however. This includes the miniaturization of the monitoring equipment, the development of more transducers and the assembly and field testing of a final prototype.

In conclusion, the feasibility and practicality of local digital recording coupled with low duty-cycle operation to monitor slowly varying physiological parameters in the field has been demonstrated. It is expected that these techniques will find application in other areas of research.

REFERENCES

1. MacKay, R.S., Biomedical Telemetry, John Wiley & Sons, New York, 1968.

2. Carceres, C., Biomedical Telemetry, Academic Press, New York, 1965.

3. Hoagland, A.S., Digital Magnetic Recording, John Wiley & Sons, New York, 1963.

4. Mee, M.C., The Physics of Magnetic Recording, Interscience Publishers, New York, 1964.

5. Davies, G.L., Magnetic Tape Instrumentation, McGraw Hill Book Co., New York, 1961.

6. Stewart, W.E., Magnetic Recording Techniques, McGraw Hill Book Co., New York, 1957.

7. Susskind, A.K., Analog to Digital Conversion Techniques, MIT Technology Press, 1957.

8. McCullough, W.R., "A New and Unique Analog-to-Digital Conversion Technique", Trans. IEEE, Vol. IM-15, No. 4, P. 276, 1966.

9. Millman, J. and Taub, H., Pulse and Digital Circuits, McGraw Hill Book Co., New York, 1964.

10. Cleary, J.F., "Transistor Manual", General Electric Co., New York, Pp. 301-348, 1964

11. Powers, G., "Micrologic Shift Counters", Fairchild Semiconductor Application Bulletin, App. 85/2, Nov. 1965.

12. Donaldson, R.W., and Chan, D., "Calculation of Steady-State Errors in Digital-to-Analogue Ladder Converters", Electronics Letters, Vol. 3, No. 5, May, 1967.

13. Fryer, T.B., and Deboo, G.J., "A High Performance Miniaturized Preamplifier for Biological Applications", Med. Electron. Biol. Engn., Vol. 3, Pp. 203-204, 1965.

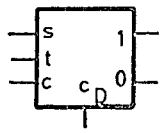
14. Byrne, C.J., "Properties and Design of a Phase Controlled Oscillator with Sawtooth Comparator", BSTJ, Vol. XLI, No. 2, P. 559, March, 1962.

15. Middlebrook, R.D., Differential Amplifiers, John Wiley & Sons, New York, 1963.

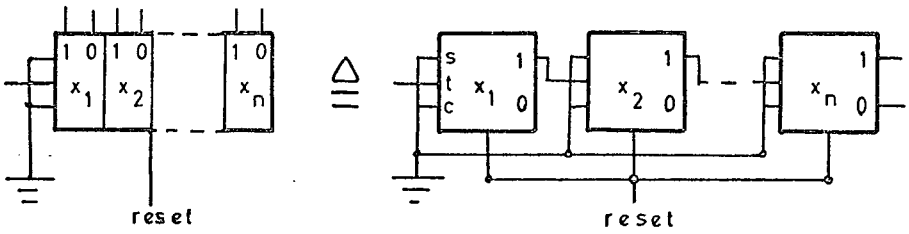
APPENDIX

All transistors are 2N4124 (npn) and 2N4126 (pnp) unless otherwise stated. The digital logic is Motorola plastic IC's, MC700P series. All resistors are in ohms, and all capacitors are in picofarads, unless otherwise indicated. k = x 10^3, M = x 10^5.

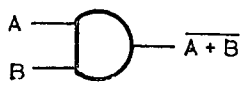
Logic Symbols



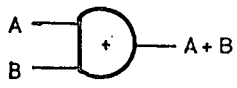
JK FLIP-FLOP



N STAGE BINARY COUNTER



NOR GATE



OR GATE

INVERTING BUFFER

NON INVERTING BUFFER