A CODER FOR PULSE CODE MODULATION
USING CIRCULATED PULSES

by

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ABSTRACT

This thesis is concerned with the construction of a pulse code modulation coder, the purpose of which is to code the information contained in a signal having no frequency components greater than $\frac{1}{4}$ kc into a series of binary pulses.

The major objective was the construction of a transistorized coder using the circulated pulse principle which involved only simple circuits and readily available components. The construction and operation of this system are described in full. The results of tests made on the circuit using d-c input signals are also given.
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1. INTRODUCTION

Several systems for transmitting the information contained in a continuous signal by means of pulses have been developed in an effort to improve the performance and efficiency of communication systems. Since a pulse has several parameters such as amplitude, duration, and position there are many modulation methods available. Some of the better known methods are pulse amplitude modulation (PAM), pulse width modulation (PWM), pulse position modulation (PPM), and pulse frequency modulation (PFM). These modulation methods are illustrated in figure 1.1.

As well as the usual frequency division multiplexing, most pulse modulation methods also lend themselves to time division multiplexing, or the sending of several signals over a single carrier frequency by interleaving their pulse trains in time.

One of the most serious problems of communications is the accumulation of noise in each link of a long transmission system. This noise determines the maximum length of a practical communication channel. Any modulation method, including the pulse methods mentioned above, which uses a continuously variable parameter is subject to this limitation. However, by using a parameter which is limited to a set of discrete values this accumulation of noise can be overcome. As long as the noise is limited to less than half the difference between two adjacent allowed values, the receiver will be able
Modulating Signal

Pulse Amplitude Modulation

Pulse Width Modulation

Pulse Position Modulation

Pulse Frequency Modulation

Figure 1.1 Pulse Modulation Methods
to identify correctly the value sent and so can reconstruct the exact signal. In a long transmission system each repeater would be able to regenerate the transmitted signal exactly, removing any noise picked up in the transmission medium. Therefore, the quality of reproduction would be independent of the number of links in the system.

Such discrete systems are usually referred to as digital systems. If there are only two allowed values of the transmitted signal, we have a binary digital system. These are of far simpler construction than those allowing several values since they require only two-state, or binary, devices.

Of course, if the original information is contained in a continuous signal, some process will have to be devised to code it into digital form. Two practical binary digital systems are in use today, delta modulation (DM) and pulse code modulation (PCM).

The freedom from accumulative noise which these systems achieve is paid for in three ways. The coding process, when a continuous signal is changed to a discrete one, introduces noise. The bandwidth required for transmission is greater than for direct transmission or conventional AM. The terminal equipment, consisting of coders and decoders, is more complex than for conventional systems. This is especially true of PCM.
2. PRINCIPLES OF PULSE CODE MODULATION

2.1 SAMPLING

The basic principle of all pulse communication systems is that the information contained in a continuous function of length T containing no frequency component greater than $W_0$ is contained in $2W_0T + 1$ amplitude samples of the function spaced $T_0$ seconds apart in time where $T_0 = \frac{1}{2W_0}$. Therefore, to transmit a continuous signal of bandwidth $W_0$ it is only necessary to send $2W_0$ sample amplitudes from samples taken at $\frac{1}{2W_0}$ seconds intervals.

The signal is reconstructed at the receiver by generating an impulse proportional to each sample amplitude and passing these impulses through an ideal low-pass filter.

2.2 QUANTIZATION

Any complex signal can be approximated by a signal having a discrete set of allowed amplitude levels. This process is called quantization, a quantum being the difference between two adjacent discrete levels. The degree of approximation desired determines the number of amplitude levels needed and hence the quantum size. The input-output characteristic of a linear quantizer is a series of steps as in figure 2.1.

The maximum error of this approximation is plus or minus one half quantum. This error causes a distortion in the reconstructed signal called quantizing noise. The distortion consists of harmonics and modulation products between signal
components and the sampling frequency. For a complex signal, such as speech, the quantizing noise is an essentially flat band of noise that sounds much like thermal noise. In order to pass the lowest amplitude sounds, the quantum size must be made small. However, if the quantum size is small, then to have a system capable of handling high levels a prohibitive number of steps, and hence pulses per code group, is required. The two conflicting requirements are made compatible by using a tapered step function as in figure 2.2 assigning a given number of steps in greater proportion to the low amplitudes than to the highs. The overall effect is to increase the signal-to-noise ratio of the small signals but at the same time decreasing that of the large ones.
Figure 2.2 Input-Output Characteristic of a Tapered Quantizer

2.3 CODING

Each quantized amplitude sample of the input signal, since there are now only a finite number of possible amplitude values, can be represented by a group of binary pulses. The $n$ pulses in a code group are weighted according to their position in the group, the $m^{th}$ pulse being weighted by $2^{n-m}$. The amplitude represented by a code group is the weighted sum of the pulses present. That is, each amplitude sample is coded into the form of an $n$-digit binary number with pulses forming the $n$ digits, a pulse standing for the 1 and a space for the 0 of the binary notation. A code having $n$ pulses per code group can represent $2^n$ amplitude levels. In some coders, the quantization is not a separate operation preceding coding but is a result of the coding operation itself.
Figure 2.3 Pulse Code Modulation
Of course, a code to any base b could be used by employing code pulses having b allowed amplitudes. A base b code having n pulses per code group could represent $b^n$ amplitude levels. The binary code is the simplest since it is easily represented by binary or two position devices.

2.4 REGENERATION

In most communication systems, the noise introduced by the individual links accumulates. A 100 link system would require a signal-to-noise ratio in each link 20 db better than the overall system requirement. Obviously, then, the length of a practical system is limited by the signal-to-noise ratio requirements.

PCM, since its reception depends only on the recognition of a standard pulse or space, can be regenerated at each repeater. The repeaters must only send out a standard pulse when a distorted one is received and nothing otherwise. Thus, as long as the noise in each link is limited to such a value that the pulses are still recognizable, each repeater will send out exactly the same signal as was originally produced by the coder. Therefore, the quality of transmission does not depend on the number of links in the system and so the system length is not limited by the signal-to-noise ratio requirements.

2.5 MULTIPLEXING

Modulated carrier systems such as AM and FM are multiplexed in frequency, several carrier frequencies being sent
simultaneously over the same channel. Pulse communication systems, since the pulse groups can be made to use only a fraction of the time available, can be multiplexed in time as well as in frequency. That is, the pulses from several modulating signals can be interleaved in time and sent over one channel or a common carrier frequency.

Of course, the time multiplexing of several signals imposes additional restraints on pulse build-up and decay times and pulse widths which implies a sufficiently wide pass band with good phase linearity.
3. PERFORMANCE CHARACTERISTICS OF PULSE CODE MODULATION

3.1 TRANSMISSION REQUIREMENTS

3.1.1 BANDWIDTH

To transmit a signal of bandwidth $W_0$ by PCM, it is necessary to send $2W_0$ code groups per second. Therefore, for an $n$-digit code, $2nW_0$ pulses per second must be transmitted over the channel. If the transmission channel has the characteristics of an ideal low-pass filter of bandwidth $nW_0$ and if the code pulses are short, then the received pulses would each be of the form (figure 3.1)

$$V = V_0 \frac{\sin 2\pi Wt}{2\pi Wt}$$

where $W = nW_0$.

A series of such pulses occurring at regular intervals $\frac{1}{2W}$ apart has the property that when one pulse is at its maximum all the others are zero. Thus, by sampling the signal
at appropriate intervals, the receiver can identify the individual pulses without any interference from adjacent pulses.

In a practical system, the transmission medium would not have this ideal characteristic and the received pulses would not have the exact form given above. As a result, there would be some interference between adjacent pulses. However, by using an effective bandwidth somewhat greater than $n\omega_0$, this interference can be made small and therefore can be considered merely as additional noise. It is then still possible for the receiver to decide whether a pulse was sent by sampling the signal at a single point.

For practical purposes then, the bandwidth required for the transmission of one pulse train is somewhat greater than $n\omega_0$. It is interesting to note, however, that much smaller transmission bandwidths could be used as long as the signal-to-noise ratio is good enough and the receiver is capable of disentangling the resulting interference between adjacent pulses.

3.1.2 POWER

If the received pulses are of the form given in the last section and are sampled at the appropriate times, then a pulse is said to be present if the sampled signal is greater than $\frac{V_o}{2}$ and absent if less than $\frac{V_o}{2}$. The decision will be wrong if the noise present at that instant is greater than $\frac{V_o}{2}$ in the right direction. Assuming gaussian noise
the probability of an error is proportional to the complementary error function of

\[
\frac{V_o}{2\sigma} = \sqrt{\frac{P_s}{4N}}
\]

where

\[
\sigma = \text{rms noise amplitude} \\
P_s = \text{signal "power"} = V_o^2 \\
N = \text{noise "power" in bandwidth} W = \sigma^2
\]

This is a rapidly decreasing function of \(\frac{P_s}{N}\) so that nearly perfect transmission can be achieved with a value of \(\frac{P_s}{N}\) just slightly larger than is required for only fair transmission. In fact, as can be seen from the graph (figure 3.2), there is a threshold at about 20 db above which interference is negligible. Therefore, compared with the 60-70 db required for high quality AM transmission, PCM requires much less signal power even though the noise power is increased by the \(n\)-fold increase in bandwidth.

3.2 INTERFERENCE AND CROSSTALK

One of the outstanding characteristics of PCM is its resistance to interference and crosstalk. Interference in a binary PCM system must reach a peak amplitude of greater than half the pulse height to have any effect on the transmission. Similarly, crosstalk from nearby channels has no effect unless the sum of the noise and crosstalk is greater than half a pulse height. Because of this, and the rapid increase of
signal-to-noise ratio with power, if an adequate power margin over threshold is provided the system will be essentially unaffected by interference and crosstalk. The use of regeneration at repeaters allows the system requirement for interference and crosstalk to be used for each link since the noise does not accumulate.

3.3 SIGNAL-TO-NOISE RATIO

There are two types of noise introduced by a PCM system, quantizing noise introduced at the coder and false pulse noise caused by incorrect interpretation of the signal at a repeater or the receiver. False pulse noise can arise anywhere along the system and is cumulative. However, as was seen in section 3.1.2, this noise is such a rapidly decreasing function of the signal power that it can be made negli-
gable by design. Therefore, the signal-to-noise ratio of a
PCM system is set by the quantizing noise alone.

For signals which are large compared to the size of a
quantum step, the errors introduced by quantization will be
essentially uncorrelated. All possible values of error up
to the maximum of plus or minus one half quantum are equally
probable. Therefore, the rms error introduced is \( \frac{1}{2\sqrt{3}} \) of a
quantum. The reconstructed signal consists of the original
signal plus a noise of uniform spectrum out to \( W_0 \) and of rms
amplitude \( \frac{1}{2\sqrt{3}} \) of a quantum. The ratio of peak-to-peak sig-
nal to rms noise is, therefore,

\[
R = 2 \sqrt{3} \ b^n
\]

since \( b^n \) is the number of levels. Expressing this ratio in
decibels, we have

\[
20 \log_{10} R = 20 \log_{10} 2 \sqrt{3} + n(20 \log_{10} b)
\]

Therefore, the signal-to-noise ratio in decibels for a binary
system, \( b = 2 \), is

\[
20 \log_{10} R = 10.8 + 6n
\]

Since \( W = nW_0 \), the signal-to-noise ratio is a linear function
of the bandwidth used in transmission. Of course, increased
bandwidth allows increased noise power and the signal power
would need to be increased to keep the false pulse noise neg-
ligible.
3.4 CHANNEL CAPACITY

The bandwidth efficiency can be measured as the information capacity of the system compared with the theoretical limit for a channel of the same bandwidth and power. The capacity of an ideal system is given by

\[ C = W \log_2 \left( 1 + \frac{P}{N} \right) \text{ binary digits/second} \]

where

- \( W \) = bandwidth
- \( P \) = average signal power
- \( N \) = white noise power

The capacity of a binary PCM system operating at a signal-to-noise ratio of 20 db so that the frequency of errors is negligible is

\[ C = 2W_0 n = 2W \]

For a symmetrical binary system (that is a system using positive and negative pulses of equal size rather than pulses and spaces) with pulses of amplitude \( \frac{V_o}{2} \) the peak power is the same as the average power and is \( \frac{V_o^2}{4} \). Therefore, for \( \frac{V_o^2}{N} = 20 \text{ db} \)

\[ \frac{P}{N} = \frac{V_o^2}{4N} = \frac{100}{4} = 25 \]

The theoretical capacity of a system with this signal-to-noise ratio is

\[ C = W \log_2 (1 + 25) = 4.7W \]
Therefore, PCM has only about 0.425 of the theoretical maximum channel capacity.

In order to approach closer to the theoretical limit, it is necessary to use error correcting codes. These are necessarily complex, requiring complex coding equipment. They also produce a delay in transmission since the receiver must wait for the errors to be corrected before the output is given.

Considering the simplicity of a PCM system and the fact that there is no delay, the channel capacity achieved is very good.
4. PULSE CODE MODULATION EQUIPMENT

The job of a PCM coder is to take an amplitude sample, quantize it, and represent this quantized value as a pattern of pulses (usually binary pulses). The decoder must take these pulse patterns and from them reconstruct the sample amplitudes. The samples can be derived from a single signal or from several signals each sampled in turn. If several signals are being sent over the same channel, the coder is preceded by a collection switch and the decoder is followed by a distribution switch which is synchronized with the collection switch. The actual coder and decoder would be the same as for a system transmitting only one signal.

4.1 CODERS

PCM coders can be grouped into the following three categories depending on their method of measuring the sample amplitude.

A. The amplitude of the sample is measured by counting the number of units contained in it one by one until the remainder is less than a quantum. This type of coder is of comparatively simple construction and is often used in pulse height analyzers. These coders are the slowest of the three groups.

B. The sample amplitude is measured in a single operation by comparison with a set of scaled values. This system is extremely fast, the whole coding operation can be done in about one microsecond. The circuitry, however, is
complex and usually involves special beam coding tubes.\(^5\)

These coders become economical only when used in systems with either many channels or wide bandwidth signals where their speed can be put to full use.

C. Amplitude is measured by comparing the sample with one digit value after another proceeding from the most significant digit to the least.\(^6\) There are two ways of doing this. A set of voltage comparators, each corresponding to a digit value, can be used, the signal being applied to each in turn, or a single comparator can be used the signal being circulated around a loop, amplified appropriately and applied to the same comparator for each level. Both these types of coders are of intermediate speed, the first being of intermediate complexity and the second of relative simplicity. They lend themselves to the coding of a few signals of moderate bandwidth, such as speech. The coder discussed in the following chapters is of the looped signal type.

4.2 DECODERS

PCM decoders are also of many types, two of which will be mentioned very briefly here.

The first type uses a delay line to obtain all the signal pulses at one time adding their weighted values to achieve the sample amplitude. They lend themselves to fast operation where the delay lines involved are short but of course suffer from the difficulties accompanying all delay lines.
The second uses a loop principle analogous to the looped signal coder and would be the type most logically associated with the coder with which this thesis is concerned.
5. OPERATION AND CONSTRUCTION OF THE CODER

We will now discuss the operation and construction of the coder which was designed and built as the subject of this thesis. A sampling rate of 8 kc and a 6-digit code were chosen as they are sufficient to transmit telephone quality speech and can be achieved with readily available transistors. The circuit was developed starting from the simple block diagram (figure 5.1).

It was decided that delay line was to be avoided in the signal path since the required delays were long for continuous lines and it was felt that better linearity and accuracy could be achieved with the use of holding capacitors. The holding system used also allows great flexibility in the speed of operation. To change the sampling rate and number of digits, only the timing circuits need to be adjusted.

The circuit in this final form is only a laboratory model. No great effort was expended trying to reduce the number of components to a minimum although simplicity of the overall circuit was a major criterion. The number of supply voltages could also be reduced without undue difficulty.

Only a single channel system was built but the speed of operation is sufficient to allow about 3 channels to be coded in the available time with only a re-design of the timing system. Using the existing components, the speed of the present circuit could probably be increased to handle about 5 channels.
5.1 OPERATION OF THE CODER

The operation of the coder will be explained on the basis of the simplified block diagram (figure 5.1).

Diode gate No. 1 is operated by pulses occurring at the 8 kc sampling frequency. When a gating pulse arrives, gate No. 1 allows a sample of the input signal to be applied to the voltage comparator. If the sample pulse amplitude is greater than $V$, the voltage corresponding to 32 units, the pulse generator gives an output. The action of the pulse generator when this output occurs also subtracts $V$ volts from the sample pulse in the subtraction circuit. The remaining signal pulse is then amplified by 2 and stored in the holding circuit until diode gate No. 2, which is operated by pulses of the same width as gate No. 1 but of 6 times the frequency, allows it to be applied to the comparator. If this amplified pulse is greater than $V$, an output pulse is generated. If no output pulse occurs, the signal pulse has nothing subtracted from it and is again doubled before being stored and then compared with $V$ again. In this way, the 6 binary pulses of weights 32, 16, 8, 4, 2, and 1 are generated in that order.

After the signal has been applied to the comparator for the sixth time, gate No. 2 is inhibited and the charge remaining in the holding circuit is removed. At the same time, gate No. 1 again samples the input signal and the coding operation begins again.
Figure 5.1 Simplified Block Diagram of Coder
Figure 5.2 Complete Block Diagram of Coder
The extra units in the complete block diagram (figure 5.2) do not alter the mode of operation of the circuit. The extra gate removes spikes from leading and trailing edges of the signal pulse which result from imperfect timing of the subtraction operation. The buffers match impedance levels and isolate certain circuits preventing unwanted feedback effects.

5.2 TIMING CIRCUITS

The circuits used to generate the necessary gating pulses are standard multivibrators. The master clock (figure 5.4), which sets the frequency for the whole circuit, is an ordinary astable multivibrator with a period of 20.8 microseconds for a 6-digit code and an 8 kc sampling rate. The potentiometers \( R_4 \) and \( R_6 \) provide adjustment of the period of the clock from about 15 microseconds to about 24 microseconds.

The frequency divider (figure 5.4) is another astable multivibrator which is synchronized to the master clock by pulses fed to the emitters of \( T_3 \) and \( T_4 \) through \( C_3 \) and \( C_6 \). The potentiometers \( R_{12} \) and \( R_{14} \) provide adjustment of the period and therefore the ratio of frequencies. Use of this adjustment in conjunction with adjustment of the master clock frequency allows the sampling rate and number of pulses per code group to be chosen over a fairly wide range.

The gating pulse generators (figure 5.5) are ordinary monostable multivibrators triggered by timing pips derived from the leading edges of the waveforms of the master clock.
Figure 5.3 Block Diagram of Timing Circuit
Figure 5.4 Circuit Diagram of Master Clock and Frequency Divider
Figure 5.5 Circuit Diagram of Gating Pulse Generator

Figure 5.6 Circuit Diagram of Delayed Pulse Amplifier
and frequency divider. The output pulses GP1- and GP2- must be of exactly 6 volts amplitude. The diodes on the collectors are used to set this level. Diodes are used on all the collectors to set the amplitude of the voltage swing and hence the pulse width at a well controlled value. The pulse generators give output pulses of 6 volts amplitude and 2.5 microseconds duration.

Gating pulses GP1+ and GP3- must be accurately synchronized since every sixth pulse of GP1+ is inhibited by GP3- in diode gate No. 1. The 0.4 microsecond delay line between the master clock and pulse generator No. 1 overcomes the discrepancies in this timing due to finite rise times and delay in synchronization. This delay line is not properly terminated but the reflected pulses are small and the diode D3 is so biased that only the top of the initial pulse is applied to the pulse generator.

The delayed pulse amplifier (figure 5.7) provides a one microsecond wide pulse delayed 1.0 microsecond with respect to GP1+. This pulse controls the emitter-follower gate. The delay line is correctly terminated at the receiving end and so provides a clean pulse to the amplifier.

5.3 DIODE GATES

The diode gates must be linear to about 1% accuracy over the range of a few millivolts to about 3.5 volts and have either no pedestal or else one of small constant amplitude. The gates must also feed a common load without interfering
with each other's operation. Unidirectional Lewis gates were chosen since they satisfy the above requirements and are of simple design.

Diode gate No. 1 (figure 5.8) is a simple unidirectional Lewis gate which is operated by gating pulse GP3+ which is applied through capacitor C17. This positive pulse turns off the normally conducting diode D10 thereby allowing the junction point of the three diodes to rise from -6 volts toward the +6 volt supply. This point, however, is caught at the signal voltage when D11 starts to conduct. The low impedance signal source therefore sets the level to which the junction point and hence the high impedance load point rises.

In this way, the gate allows a 2.5 microsecond wide sample of the input signal to enter the coding circuit every 125 microseconds.

Diode gate No. 2 (figure 5.9) is identical to No. 1 except for the inhibitor. The gating pulses GP1+ applied through capacitor C26 operate the gate. Coincident with every sixth pulse of GP1+ there is a pulse of GP3- applied through capacitor C27. This negative pulse prevents the junction point of the gate from rising to the signal level and hence inhibits the action of the gate. Therefore, the base of transistor T12 sees the signal from gate No. 1 and then for the next five gating periods it sees the signal from gate No. 2, the sixth signal once more coming from gate
Figure 5.8 Circuit Diagram of Diode Gate No. 1

Figure 5.9 Circuit Diagram of Diode Gate No. 2
No. 1.

The load for these gates is the input impedance of the buffer amplifier $T_{12}$. Resistor $R_{49}$ and diode $D_{13}$ bias $T_{12}$ at the correct level. When a positive pulse is applied to the base of $T_{12}$, $D_{13}$ is cut off. When the gate signal drops, $D_{12}$ is cut off and the base of $T_{12}$ decays toward $-13.5$ volts through $R_{49}$ being caught at $-4.5$ volts by $D_{13}$. If instead of $D_{13}$ a resistor to ground was used, the base of $T_{12}$ would decay toward $-4.5$ volts instead of $-13.5$ volts and so the trailing edge of the signal pulse would last much longer.

5.4 COMPARATOR PULSE GENERATOR

The comparator has to meet stringent requirements. It decides whether or not the signal coming to the pulse generator exceeds a fixed reference voltage; if it does, then the pulse generator is to send out a standard pulse. This decision should be made unambiguously and there should be no drift in the reference level. In practice, with a quantum size of about $50$ mv, a drift of $20$ mv and a "maybe-region" of $1$ mv are just about permissible.

The comparator and pulse generator (figure 5.10) are combined in a single unit which is a conventional Schmitt circuit. Transistor $T_{13}$ is normally conducting a current of $7$ ma. while transistor $T_{14}$ is normally off. A positive pulse of amplitude greater than or equal to $1.0$ volt applied through diode $D_{14}$ to the base of $T_{13}$ switches this current to $T_{14}$. The current is switched back to $T_{13}$ when the signal
Figure 5.10  Circuit Diagram of Comparator Pulse Generator and Subtractor

$T_{12}, T_{13}, T_{14} = 2N247$
$T_{15} = 2N585$
All Diodes = 1N497
$R_{40} = 33K$
$R_{41} = 470$

$R_{42} = 10K$
$R_{43} = 4.7K$
$R_{44} = 1.5K$
$R_{45} = 10K$
$R_{46} = 680$
$R_{47} = 4.7K$
$R_{48} = 1K$
$R_{49} = 470$
$R_{50} = 1K$
$C_{18} = 50-100$ uuf
voltage falls below another level $V'$ volts. The output pulse is taken from the collector of $T_{13}$.

Diode $D_{14}$ is included in the circuit to unhook the pulse generator when it switches states and so prevent it from affecting the signal output of $T_{12}$.

Diode $D_{15}$ catches the base of $T_{14}$ at -3 volts and produces there a flat-topped waveform. This ensures a constant current in $T_{14}$ during the subtraction period.

The d-c coupled Schmitt circuit was chosen rather than the a-c coupled for two reasons. First, by adjusting $C_{18}$, the circuit can be made relatively independent of the rise time of the triggering pulse. This is necessary since the initial sample pulse has a considerably faster rise time than the pulses which have circled the loop. The second reason for choosing the d-c coupled circuit is that the recovery time of a monostable emitter-coupled multivibrator is long compared to the output pulse width. This would require a long dead time between digit pulses which would seriously limit the speed of the system.

5.5 SUBTRACTING CIRCUIT

When the signal pulse applied to the comparator is greater than $V$, the current switched to $T_{14}$ is subtracted from the signal current in $T_{12}$ in the common load resistor $R_{48}$ (figure 5.10). The potentiometer $R_{48}$ is adjusted so that when the signal is just large enough to trigger the Schmitt circuit, the subtraction process leaves zero signal at the
base of $T_{15}$.

Transistors $T_{12}$ and $T_{15}$, as well as forming the subtractor and a buffer, also provide the required loop gain. Transistor $T_{15}$ is NPN to enable d-c coupling which gives faster possible operation than a-c coupling with d-c restoration. However, this is paid for with the resulting susceptibility to drifting of d-c levels and temperature instability.

Since the signal pulse has finite rise and fall times and the pulse generator only gives an output when the signal pulse amplitude is greater than $V$, there is a portion at the beginning and end of each signal pulse where the subtractor has no effect. For some signal levels, this causes spikes at each edge of the signal pulse after subtraction. To remove these spikes, the output of the subtractor must be regated before it reaches the holding circuit.

5.6 EMITTER-FOllOWER GATE

The emitter-follower gate (figure 5.11) removes the leading and trailing edges from the signal pulse after the subtraction. A diode gate could not be used here since current gain was needed in order to be able to charge the first holding capacitor to the maximum signal level in the one microsecond available.

The common emitter point is clamped at the voltage of whichever base is most negative, normally that of transistor $T_{17}$. When a large positive gating pulse $GP_{1d}$ is applied to $T_{17}$ through capacitor $C_{19}$, $T_{17}$ is cut off and the voltage on
the emitter rises toward +6 volts. However, when the emitter voltage reaches the level of the base of \( T_{16} \), it is clamped by the signal on the base of \( T_{16} \). Therefore, the first holding capacitor \( C_{20} \) is charged up to the signal level through diode \( D_{16} \).

5.7 HOLDING CIRCUIT

The holding circuit (figure 5.12) stores the signal pulse amplitude, after subtraction and doubling, until the coder is ready to apply it to the comparator to produce the next digit. Two stages are necessary in the holding circuit since it must be giving an output signal at the same time as the next digit signal is entering it. The third stage of the circuit, capacitor \( C_{22} \), is merely a means of displaying the signal for
Figure 5.12 Circuit Diagram of Holding Circuit

T₁₈, T₁₉ = 2N404
D₁₆, D₁₇, D₁₈, D₁₉ = 1N497

R₅₄ = 47
R₅₅ = 68
R₅₆ = 100
R₅₇ = 39K
R₅₈ = 10K

R₅₄ = 680 uuf
R₅₅ = 680 uuf
R₅₆ = 680-750 uuf
R₅₇ = .01 uf
R₅₈ = .01 uf
C₂₀ = 680 uuf
C₂₁ = 680 uuf
C₂₂ = 680-750 uuf
C₂₃ = .01 uf
C₂₄ = .01 uf
diode gate No. 2. It could be eliminated at the expense of providing some new timing pulses.

The holding is done by charging the first capacitor $C_{20}$ to the signal voltage through the diode $D_{16}$. When the signal pulse on the emitter of the emitter-follower gate falls, diode $D_{16}$ is cut off, and the voltage on $C_{20}$ remains constant since transistor $T_{18}$ is also off. Gating pulse $GP_2^-$, which is of accurately controlled constant amplitude, pulls the base and hence the emitter of $T_{18}$ down to $-6$ volts, thereby transferring the charge responsible for the voltage being greater than $-6$ volts onto capacitor $C_{21}$. The charge is held on $C_{21}$ until $GP_1^-$ once more transfers it to $C_{22}$ from where it is applied through the double emitter-follower and diode gate No. 2 to the comparator. $GP_2^-$, applied through $C_{23}$ to the junction of $D_{17}$ and $D_{18}$, discharges $C_{22}$ in preparation for the next cycle of operation.

$C_{22}$ is variable as a convenient means of having a fine adjustment on the loop gain of the circuit. This is possible since the charge on $C_{20}$ is set by the voltage output from the emitter-follower gate and the voltage on $C_{22}$ is then set by this charge. Therefore, the voltage on $C_{22}$ is dependent on the relative sizes of $C_{20}$ and $C_{22}$ but does not depend on $C_{21}$.

One fault of the circuit was that although the pulses $GP_2^-$ and $GP_1^-$ brought the bases of $T_{18}$ and $T_{19}$ to their correct levels, the emitters did not always follow depending on the charge on the respective capacitors. This was found to
be due to the variation of the transistor diffusion capacitances due to the heavy currents involved in switching the charges. Resistors $R_{54}$ and $R_{55}$ are included to limit these currents and effectively reduce the above effect.

Resistor $R_{56}$ squares up the round leading edge of the pulse given out of the holding circuit. In this way, the timing of the output of the pulse generator comparator is improved, and (since the pulse now resembles more closely the initial sample pulse), the rise time dependence of the comparator is of less importance.

Since the gain of the circuit is affected by the relative sizes of $C_{20}$ and $C_{22}$, the operation is sensitive to temperature variations of these components. As long as they have equal temperature coefficients and are placed close together so that their temperatures are equal, no effect on the gain of the circuit will be observed. In the coder constructed, to insure temperature stability, temperature compensated capacitors were used for $C_{20}$ and $C_{22}$.

5.8 DOUBLE EMITTER-FOLLOWER

The voltage on the third holding capacitor $C_{22}$ must be applied to the diode gate No. 2. This requires a buffer stage with an input impedance high enough so that the droop on the resulting waveform is held to a small value. The output impedance must at the same time be low enough to drive the relatively low-impedance gate. The buffer stage must
therefore yield considerable impedance transformation as well as changing the d-c level from -13.5 volts to -4.5 volts, thus requiring a-c coupling.

In order to achieve the necessary input and output impedances, two cascaded emitter-followers were necessary (figure 5.13). The input impedance obtained is about 120k giving an input time constant of about 55 microseconds. The diode D20 and divider chain R59, R60 provide d-c restoration after the a-c coupling through C25. The restoration time of about 6 microseconds limits the speed of operation of the present circuit.

Resistor R64 in the collector circuit of T21 merely keeps the power dissipated in T21 to a tolerable value.

The potentiometer R60 is used to adjust the d-c output
level of the emitter-follower to match exactly the input level of diode gate No. 2.
6. ADJUSTMENTS

Before putting the circuit into operation, it must be
adjusted correctly. These adjustments need not be made in
the order given but this procedure is the fastest method of
achieving correct operation. In order to adjust the coder,
we must be able to present at its input an adjustable d-c
signal. Transistor $T_{22}$ (figure 6.1) was added to the cir-
cuit to achieve this. The output level of $T_{22}$ is controlled
by the micro-pot $R_{69}$. All tests on the coder were done us-
ing this d-c input control.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{circuit_diagram}
\caption{Circuit Diagram of d-c Input Circuit}
\end{figure}

The first adjustment is to the d-c level at the output
of the double emitter-follower. Potentiometer $R_{60}$ must be
adjusted so that when there is no signal input to the coder

\begin{itemize}
  \item $T_{22} = 2N404$
  \item $D_{11} = 1N497$
  \item $R_{68} = 10K$
  \item $R_{69} = 10K$ Micro-pot
  \item $R_{70} = 2.2K$
  \item $R_{71} = 680$
\end{itemize}
there is no build-up of the zero signal pulses. These pulses are of about 0.1 volts amplitude at the emitter of $T_{12}$. To make the adjustment a complete set of signal pulses should be examined on the emitter of $T_{12}$ at zero input signal and $R_{60}$ adjusted until they are all of a constant small amplitude. If $R_{60}$ is set so that the d-c level of the double emitter-follower output is too positive, the zero signal pulses will be built up by the loop gain of the circuit. Therefore, the excess signal will be easily visible in the sixth digit. If the level is set too negative, the zero signal pulses will all be of the same size or non-existent. If they are of the same size, the adjustment is not necessarily correct. Therefore, the adjustment should be made working from a too positive level toward the correct value.

It is this adjustment that is most often in need of attention since it corrects for any d-c drift in the circuit.

Once the d-c level is adjusted, the subtractor can be set up. This is done by setting the input to the coder so that the pulse generator is just triggered by the sample pulse. Potentiometer $R_{48}$ is then adjusted so that the signal at the collector of $T_{12}$ is zero. The best way to determine the correct adjustment is by examining a complete pulse group at the emitter of $T_{12}$. When $R_{48}$ is set correctly, the pulse group should consist of one pulse, the sample, followed by five zero level pulses. A slight positive signal left over after subtraction will produce an easily visible signal in the sixth pulse position. On the other hand, if too much is
subtracted no effect will be visible. Therefore, the adjustment should be made by approaching the correct value from the direction of too small a subtraction.

This adjustment only needs attention if the reference level of the comparator drifts. As this level was very stable, the subtractor, once set up, did not require readjustment during the following tests.

The final adjustment to be made is that of the loop gain of the system. Capacitor C22 must be set so as to make the loop gain exactly two. The best way of accomplishing this is by making sure the quantum size for the levels 31 and 32 are the same as for the other values. Any variation from two in the loop gain will appear most readily in the sizes of these two quanta.
7. PERFORMANCE OF THE CODER

The operation of the coder involves many signal pulses of unusually accurate amplitudes and of various time relationships and is best studied with the aid of the d-c input circuit described in Chapter 6 and a fast pulse oscilloscope. Many weeks were spent studying the circuit operation and redesigning various parts in order to achieve better pulse-shapes, synchronization and stability. In the course of this work, many small but significant irregularities of transistor behaviour had to be overcome.

As it stands now, the circuitry is very satisfactory. None of the requirements on components, rise-times or pulse shapes are exceedingly critical and all components operate well within their ratings. The most difficult problem in the design of the coder, and the main imperfection still remaining, is the existence of small drifts in some of the d-c levels. Some of the tests to be described deal with the effects of these drifts.

Figure 7.1 shows the input-output characteristic of the coder using the d-c input circuit. Of course, the actual output of the coder is a series of binary pulses, but these have been given their decimal values for the purposes of plotting. There are two imperfections in this curve. The step sizes are not uniform and the centers of the steps do not all lie on a straight line.

Both effects may be due to a slight variation in the
Figure 7.1 Input-Output Characteristic of the Coder
loop gain with pulse height. The variation in step size increases the quantizing noise by about 10%, which is not too serious. The non-linearity of the curve occurs mainly at the ends. With a signal centered at the mid-point, it would affect only the large signal values and then only to the extent of about 4% which is probably tolerable.

The stability of the coder was tested by setting the d-c input level in the middle of a code step and measuring the time which elapsed before the output code changed. When first constructed, this stability was very poor, fluctuating by several steps in a few minutes. With improved design, the drift at normal room temperature is now less than one digit in two hours.

The coder is, however, still fairly sensitive to temperature changes and to drifts in battery voltage. Most of the remaining drift comes from the d-c coupled subtractor and amplifier T₁₂ and T₁₅ especially from the NPN transistor T₁₅ which gives most of the loop gain. It is felt that this drift and temperature sensitivity can be appreciably reduced by replacing this amplifier by a silicon transistor, such as the 2N332, used in a current amplifying configuration rather than the present voltage amplifier setup.

The major power requirements of the circuit are imposed on the -13.5 volt and +6 volt supplies which deliver about 110 ma. and 30 ma. respectively. The drain on the other supplies is nominal except for the -6 volts which delivers
about 9 ma. The total power consumption of the circuit is therefore about 1.8 watts. There was no particular effort made to keep the power requirements to a minimum and they could probably be reduced if desired.
CONCLUSIONS

The coder which was built was very successful. A 6-digit code at an 8 kc sampling rate was achieved with quite good stability. As it stands, the coder uses only readily available components and simple circuits.

Since the critical d-c voltage levels had to be held to an accuracy of a few tens of millivolts, stability was a major problem. Most of the difficulty arose in the tendency of the d-c coupled amplifying stages to drift. The use of silicon transistors or some means of temperature stabilization of the present circuit would be worthwhile investigating. Alternatively, use of a-c coupling and d-c restoration would relax some of the requirements on d-c drift. However, this would also reduce the upper limit on speed of operation.

Better stability, besides increasing the reliability of the coder, would enable the use of a 7-digit code.

The existing circuit could be made to handle up to 5 channels without changing to faster transistors. The d-c restoration time of the double emitter-follower and the charge-up time of the storage capacitors are all that would require improvement.

The power requirements of the system and the number of supply voltages could certainly be reduced. At the same time, the number of components could probably be reduced slightly.

The successful construction of this coder has demonstra-
ted the suitability of the looped pulse type of coder for applications involving one or a few signals at audio frequencies.

Although only a coder was built, there should be no great difficulty in designing and building a complete system including repeaters and a decoder.
REFERENCES


