HARDWARE FOR AN ELECTRICAL MACHINES LABORATORY COMPUTER DATA ACQUISITION SYSTEM

by

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ABSTRACT

Hardware for an electrical machines laboratory computer data acquisition system is considered. A survey of existing equipment and a study of the role of a computer system in laboratory instruction is made for the UBC electrical machines laboratory. From this, specifications for the hardware required for a data acquisition and processing system are studied and a system configuration proposed. Transducers for measuring voltage and current waveforms on a machine are considered and designed.

The performance of the transducers constructed is evaluated in two sets of measurements. In the first set, measurement error, offset drift, common-mode rejection ratio, and frequency cutoff are measured for the transducer set (by itself). Measurement errors are found to be less than 1% F.S. In the second set of measurements, a system similar to the one proposed for the machines laboratory is tested. Results from this set of measurements indicate that the system design proposed is workable.

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1. INTRODUCTION

This thesis is concerned with a proposed on-line computer data acquisition and processing system for an undergraduate electrical machines laboratory. The long-term objective of this project is to introduce a digital computer system into the educational environment of a laboratory as an instructional aid as well as a measurement and computation facility.

1.1 Description of System Desired

The system envisaged for the electrical machines laboratory will acquire measurement data from the electrical machines and compute experimental results for the users. Such a system could conceivably consist of a small digital computer, a set of transducers for each machine, and some form of interface between the transducers and computer. The system developed will not replace the existing measuring instruments. Instead, it will allow the machines and meters to be connected normally to retain the educational value of setting up the experiment and to permit visual monitoring of the machine's variables. In this way, the facility can be used in an instructional role as well. The students will commence the experiment by making measurements with the normal instruments and calculating experimental results as usual. Simultaneously, the computer will compute the correct values for the experiment and the student's results can be checked at this point. Once the students have demonstrated an understanding of the principles involved, the computer can perform the tedious task of calculating results for the remainder of the experiment. If desired, tutoring of the students could be incorporated as well. The transducers must be capable of making measurements which are as accurate as those obtained from conventional instruments. As well, it would be desirable to measure inputs with frequencies up to the ninth

harmonic of 60 Hz. to permit transients and harmonic waveforms on the machines to be studied. Such a system will hence be useful for general-purpose experimental work as well as laboratory instruction.

1.2 Scope of Thesis Project

The first part of this thesis project is the study and specification of the system just described. This work is presented in Chapter 2, System Configuration.

The second part of this project is the development, construction, and checkout of a set of transducers for the electrical machines laboratory. The design of these transducers is described in Chapter 3, Transducers.

In the last part, tests were conducted on the transducers developed and on a system simulating the one proposed for the machines laboratory to determine their actual performance. Results of these tests are summarized in Chapter 4, Results.

2. SYSTEM CONFIGURATION

2.1 System Study

The UBC electrical machines laboratory consists primarily of six electrical machine sets, each comprising an induction machine, a synchronous machine, and a d.c. machine, all on a common shaft. The laboratory is supplied with power from a 230 volt d.c. bus and a 208 volt (r.m.s.), 3-phase, 60 Hz. a.c. bus. The machines may be connected in various configurations using a patchboard arrangement by the experimenter. The details of their electrical characteristics are summarized in Table 2.1.

A number of instruments are normally used for making measurements on the electrical machines. Primarily, a multimeter is used for measuring resistance, voltage, and current (up to 10 amperes). A number of ammeters are available for measuring a.c. currents up to 300 amperes and d.c. currents up to 15 amperes. As well, current shunts and millivoltmeters are available for measuring currents up to 1000 amperes. Wattmeters are used for measuring electrical power in a number of ranges up to 15 kilowatts. The specifications of the instruments available are briefly outlined in Table 2.2. Of particular interest are the accuracy specifications, most of which are of the order of $\pm 1\%$ F.S. For mechanical measurements, a stroboscope is used to measure shaft angular velocity and a mechanical arm and spring balance are used to measure shaft torque.

The majority of experiments in the electrical machines laboratory involve the measurement of quantities on only one machine. However, a significant number of experiments use a second machine connected to the machine under test. By measuring the electrical power consumed or generated by the second machine, the mechanical power produced or absorbed by the machine under test can be calculated. By providing extra transducers to measure

Table 2.1: CHARACTERISTICS OF TAMPER ELECTRICAL MACHINE SETS

(a) Steady State:

Wound Rotor Induction Motor	D.C. Motor	Synchronous Motor
RPM - 1690	RPM - 1760	RPM - 1800
H.P. - 2.5	H.P. - 2.5	K.W. - 1.6
Stator Volts-208, 3Ø, 60 Hz.	Arm. Volts-230 VDC.	KVA - 2.0
Stator F.L. Amps.-8.0	Arm. F.L. Amps.-10.3	Arm. Volts-120/208, 3Ø, 60 Hz.
Rotor Volts - 274	Shunt Field Volts - 230 D.C.	Arm. F.L. Amps.-5.5 @ p.f.= 0.8
Rotor Amps. - 4.3	Shunt Field Amps. - .58/.44	Field Volts - 115 D.C. Field Amps. - 1.2

(b) Transients:

	Description of Condition	Max. Measured Value (unidirectional)
(1)	Induction Motor-Stator current for start-ups with no-load and shorted rotor	20 A.
(2)	Induction Motor-Rotor current for start-ups with no-load and shorted rotor	24 A.
(3)	Synchronous Motor-Stator current for induction-like start-ups; $I_f = 0$.	47 A. *
(4)	Induction Motor-connected as a synchronous motor for 1Ø, 2Ø, & 3Ø fault condition experiment	20 A.
(5)	D.C. Motor	20 A. cutout

Table 2.2: CONVENTIONAL MEASURING INSTRUMENTS

(a) AVO-Meter: Model 8:

(i) Ranges: D.C. Voltage: 1000, 500, 250, 100, 25, 10, 2.5 volts

A.C. Voltage: 1000, 250, 100, 25, 10, 2.5 volts

D.C. Current: 10, 1, .1, .01, .001, .000250, .000050 A.

A.C. Current: 10, 2.5, 1. .1, A.

Resistance: 0-2000, 0-200 K, 0-20 M Ω.

(ii) Accuracy: D.C. Voltage: 2% F.S.

D.C. Current: 1% F.S.

A.C. : 2 1/4 %F.S.

(iii) Input Requirements:

All D.C. Voltage Ranges: 20,000 Ω/V. (50μA. for full deflection)

D.C. Current Ranges: Potential drop = 0.5 V. at full load except 50 μA. range which absorbs 125 mV.

A.C. Voltage Ranges: Above 100 V. → 1000 Ω/V. (1 mA. for full deflection); 25 V. consumes 4 mA; 10 V. consumes 10 mA; 2.5 V. consumes 40 mA.

A.C. Current Ranges: 0.2 V. drop across terminals on all ranges.

(b) A.C. Ammeters:

(i) Input Ranges and (number of instruments):

300 A.(2); 100 A.(1); 50 A.(7); 25 A.(2); 15 A.(2); 5/10 A.(8); 5 A.(1); 2.5/5 A.(1); 2 A.(3); 1.5/3 A.(1); 1 A.(1); .25/.5 A.(2)

(ii) Typical Accuracy: 2% F.S.

(c) A.C. Voltmeters:

(i) Input Ranges and (number of instruments):

150/300/600 V.(2); 150/300 V.(14); 60/120 V.(1); 30/60 V.(3); 30 V.(2); 2.5/15/30/ 75 V. (1); 15/30 V. (1)

Table 2.2 (cont'd)

(d) Clamp-on Ammeters:

(i) Input Ranges and (number of instruments):

15/60/150/600 A.(1); 10/25/50/100/250/500 A.(1)

(e) D.C. Ammeters:

(i) Input Ranges and (number of instruments):

5 A.(1); 15 A.(1)

(f) Shunts;

(i) Input Ranges and (number of each type): [50 mV. output]

1000 A.(2); 500 A.(1); 300 A.(3); 200 A.(1); 150 A.(2); 100 A.(4); 80 A.(5); 75 A.(1); 50 A.(9); 25 A.(1); 24 A.(1); 15 A.(1); 5 A.(3); 1.5 A.(2).

(g) D.C. Millivoltmeters:

(i) Input Ranges and (number of instruments):

50 mV. (6); 50 mV. (2); 50 mV. (2)

(ii) Typical Accuracy:

1/4 to 1/2 of 1% F.S.

(h) D.C. Voltmeters:

(i) Input Ranges and (number of instruments):

6000 V.(1); 300 V.(1); 150/300 V.(1); 15/150 V.(2); 10/20 V.(1); 3/15/150 V.(4); 1.5/15/150 V.(3)

(i) Wattmeters:

(i) Input Ranges and (number of instruments):

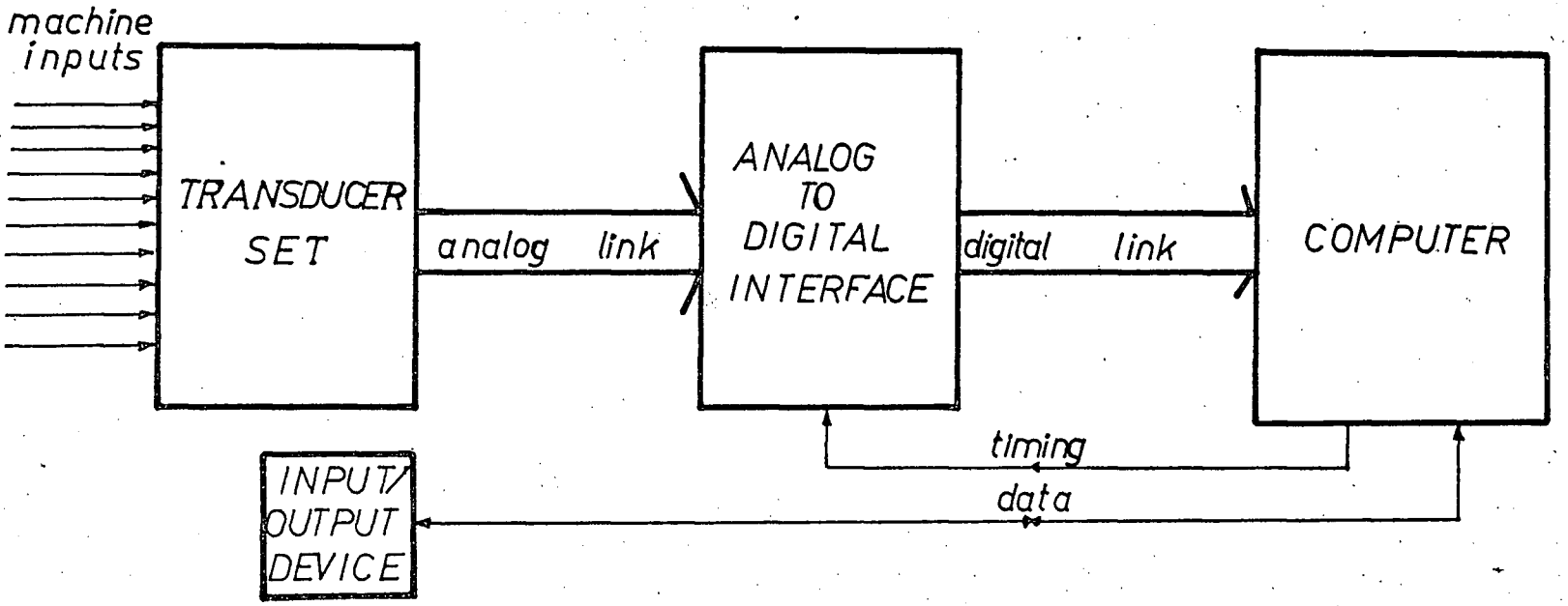
7.5/15 KW.(5); 3/6/12 KW.(1); 1.5 KW.(1); 1.5/3/6 KW.(1); 1.0 KW.(1); .750 KW.(2); 750 W.(1); 750 W.(3); 375/750/1500 W.(1); 150 W.(1); 100 W.(1); 37.5/75/150 W.(2)

(ii) Typical Accuracy:

1/2 to 3/4 of 1% F.S.

electrical quantities on the additional machine, a transducer to measure torque should not be required for most of the undergraduate experiments. Since the actual measurement of mechanical power would be desirable, a torquemeter might eventually be added or the load angle transducer developed by the Power Group[1] adapted for use with this system. Angular shaft velocity may be measured using a tachometer and voltage transducer. Hence, only transducers to measure electrical inputs are required. Since power may be calculated from voltage and current inputs using the computer, transducers for voltage and current are all that are required. For experiments using two a.c. machines, as many as eleven voltage transducers and ten current transducers could be used (one d.c. circuit, three 3-phase circuits, and tachometer output). However, a saving in the number of transducers can be realized by using only one a.c. machine in two-motor experiments or by measuring only two of three phases in two-a.c. machine experiments. A minimum of six current transducers and seven voltage transducers are required with this constraint. Since only one undergraduate experiment involves the use of two a.c. machines, this limitation appears to be justified.

A generalized block diagram for the laboratory computer system is shown in figure 2.1. It consists of six subsystems: a set of transducers, an analog link, an analog to digital interface, a digital link, a digital computer, and an input/output device for user communication. This diagram is generalized in the sense that either the digital or analog link may be short in length depending on the type and location of computer and the transmission scheme chosen. Specifications for the input/output device, the main transmission link, the analog to digital interface, and the computer are studied in the following sections. Suitable devices are chosen in each case and a system for the electrical machines laboratory is proposed.



BLOCK DIAGRAM OF SYSTEM :

FIGURE 2.1

2.2 Input/Output Device

An input/output device for user communication is required for several purposes. First of all, it will allow the experimenter to issue commands to the computer to govern the data acquisition and processing from the experiment. Secondly, it will permit the input of data concerning the experiment (e.g.: conversion units, transducer ranges, channel inputs, etc.). Finally, it will be required for the output of results from the computer.

The device required must be able to accept inputs from the user (typically alphanumeric characters at rates up to 120 five-character words/minute). Also, it must be able to produce outputs of a similar nature, preferably making permanent copies of this information. Finally, the device selected must be suitable for use in the electrical machines laboratory environment.

The most suitable input/output device for this project is the standard KSR Model 33 teletype. This device can be used to type in or print out information at a rate of up to 10 characters/second. Although a CRT display device would have a faster output response and would allow the output of graphic information as well, the teletype was chosen on the basis of cost.

2.3 Transmission Link

The transmission link is required to transmit measurement data from the electrical machines laboratory to the computer. Since the transducers are required to produce data which is accurate to $\pm 1\%$, the transmission link must be capable of conveying this information without a substantial degradation in accuracy. Also, the transmission link chosen must be able to handle data from inputs up to 540 Hz. in frequency (since the transducers accept inputs up to the ninth harmonic of 60 Hz.). Finally, it is important that the cost and complexity of the data link be minimized.

The two alternatives considered were analog and digital transmission. The principle advantage of digital transmission over analog transmission is its higher immunity to noise interference. However, the hardware required to implement digital transmission is generally more costly and more complex than that required for analog transmission. As well, the use of digital transmission would require the design of a dedicated electrical machines laboratory analog to digital interface. Since all the computers available in this department for this project are equipped with analog interfaces, it would be desirable to use analog transmission to take advantage of these existing facilities. Since analog transmission at levels in the order of ± 5 to ± 10 V.F.S. was expected to yield adequate performance for our purposes, this means of transmission was selected for use in the laboratory/computer transmission link.

2.4 Analog to Digital Interface

The analog to digital interface must meet several requirements. First of all, it must be able to handle at least thirteen analog inputs and preferably more with provisions for simultaneous sampling of all inputs (to permit calculation of power and phase relationships). Secondly, it must be able to handle input signals up to 540 Hz. (ninth harmonic of 60 Hz.) in frequency. Next, the quantization error which adds to the total uncertainty of the measurement must be an order of magnitude less than $\pm 1\%$ F.S. Hence, the digital representation of the input should be at least 10 bits[2] (for 9 bits, error is $\pm$ 1/2 level in 2^9 = 512 levels for unipolar input; hence, 10 bits yields an error of ± 1 part in 1024 parts for a bipolar input).

The specifications of the available interfaces are shown in Table 2.3. As these devices are now designed, the hybrid interface is the only suitable choice for this project since only it has individual sample-and-hold

Table 2.3: INTERFACE SPECIFICATIONS

Parameter	Hybrid Interface	Systems Lab. Interface
1. Multiplex Channels	16	8
2. Multiplex Input Level	±100 V. ±10 V. ±1 V.	±5 V.
3. Sample and Hold Units	1 per channel	-
4. Operating Frequency	≲ 20 KHz.	≤ 10 KHz.
5. A/D Conversion Time	20 μsec.	
6. A/D Word Length	12 bits	10 bits
7. Additional Features	-Analog Computer -D/A Converters -Sampling Frequency Control	-D/A Converters

units and enough input multiplexer channels. Upon modification to include these features, the systems laboratory interfaces for the PDP-8/L and NOVA computers would be as suitable as the hybrid interface.

2.5 Computers

The computer chosen for this project must meet several requirements.

First of all, the word length of the computer should be sufficient to permit an accurate digital representation of the input data to be stored in one word. For ±1% accuracy, a word length of at least 7 bits (max. error is ± 1/2 level in 2^6 levels for unipolar input) is required.

Secondly, the memory required to store the programs to operate the system must be estimated. Although it is feasible to segment the programs and store them on an external storage device, at least a portion of the programs must be stored in the computer's memory at any given time. An existing implementation[3] of software for this system divides the software into three portions, one of which occupies approximately 6 K words of memory. This implementation was made using the PDP-9 computer and its associated Monitor System Software. It may be possible to reduce the number of program instructions by writing a more specialized routine since the PDP-9 Resident Monitor occupies 1635 words[4] of memory alone. However, this is balanced by the need for additional software to permit time-sharing or polling of the various machine sets. As well, an additional software segment will be required for spectral analysis and transient analysis. A typical Fast Fourier Transform routine requires 6400 words of memory storage (both data and program) to handle 2048 time samples on the PDP-8/L computer.[5] Hence, it would be desirable to select a computer with a memory sufficiently large to handle at least 6 K words of program instructions.

A third consideration is the amount of data to be stored in memory. An upper limit on the amount of data which is produced from an experiment may be estimated by considering how much information is required for transient and spectral analysis. Since input waveforms will include frequency components up to the ninth harmonic of 60 Hz. and since it is desirable to observe these waveforms for intervals of time up to one second, as many as 1080 samples of data (Nyquist rate sampling) will be produced per channel per second. However, for steady-state measurements, much less data is required so that such a large data storage requirement may not be justified. As well, it may be possible to buffer the data in the computer and output it via the data transfer to an external bulk storage device between input samples. Thus, a memory of 8 K words or larger is recommended.

Other factors governing the decision of computer are speed, bulk storage capacity, existence of data acquisition software, and availability of high-level languages and compilers.

The computers available were the DEC PDP-9, the DEC PDP-8/L, and the DATA GENERAL NOVA. The specifications are compared in Table 2.4. Although the PDP-8/L and NOVA computers are portable and could be used directly in the laboratory, the PDP-9 was selected because of its 16 K word memory, its magnetic tape transports, and its existing data acquisition software. An important factor in this choice was the availability of a suitable analog interface.

2.6 Final System Configuration

The system specified uses a PDP-9 computer, the hybrid interface, a multi-wire $\pm$10 V.F.S. analog transmission link, a standard KSR Model 33 teletype, and a thirteen to sixteen input transducer set (to be discussed in Chapter 3).

TABLE 2.4: COMPUTER SPECIFICATIONS

Parameters	PDP-9	PDP-8/L	NOVA
1. Memory size	16 K words	4 K words	4 K words
2. Word Length	18 bits	12 bits	16 bits
3. Cycle Time	1 μsec.	1.6 μsec.	2.6 μsec.
4. Add Time	2 μsec.	3.2 μsec.	5.9 μsec.
5. Peripherals	-Teletype -Display -Hybrid Interface -Magnetic Tape Drives -Paper Tape	-Teletype -Paper Tape -Analog Interface	-Teletype -Paper Tape -Analog Interface
6. Bulk Storage Capacity	160 K words	-	-
7. Features	-Direct Memory Access -Data Channel -Program Interrupt -Extended Arithmetic Element -Monitor Software System	-Data Channel -Program Interrupt	-4 Accumulators -Data Channel -Program Interrupt

The system configuration specified is by no means absolute. Eventually, it might be desirable to use the PDP-8/L or NOVA because of the demands on the PDP-9 computer. The ±10 V.F.S. analog outputs of the transducers for signal transmission to the hybrid interface can easily be modified to a ±5 V.F.S. level suitable for use with the PDP-8/L and NOVA interfaces. However, use of the PDP-8/L or NOVA computers will require additional hardware such as an additional 4 K of memory, a bulk storage device such as a disc, and modification of the Systems laboratory interface to handle at least thirteen channels of input with simultaneous sampling of all channels using individual sample-and-hold devices. As well, a special laboratory interface and digital transmission link could be added should noise interference prove to be a serious problem.

3. TRANSDUCERS

3.1 Proposed Specifications

The following specifications are proposed as guidelines for the design of the transducers. The transducer set will consist of 13 to 16 units with at least 6 current transducers and 7 voltage transducers. Both types of transducers must be able to operate with inputs with frequencies up to 540 Hz. with an accuracy better than $\pm 1\%$ F.S. They must also be able to operate over a typical indoor temperature range of $21^{\circ} \pm 10^{\circ}C$. The current transducers must be able to handle currents up to 50 amperes, the largest current observed on the machine sets (see Table 2.1). As well, the design of the current transducers must permit current measurement in conductors at voltages as high as 500 volts above ground. The voltage transducers must be able to measure voltages up to 500 volts with common-mode voltages up to 500 volts (largest steady-state voltage anticipated was approximately 150% of the peak value of rated machine output voltage, i.e.: $1.5 \times \sqrt{2} \times 208$ V.). A number of input ranges should be provided with each transducer to permit accurate measurements at lower input levels. Finally, the design of the transducers must allow the conventional instruments to be connected normally.

3.2 Transducer Design

Six current transducers and ten voltage transducers were provided in this design. Though only six current transducers and seven voltage transducers were required, three additional voltage transducers were included because of the availability of 16 multiplexer channels and the low cost of the voltage transducers.

3.2.1 Current Transducers

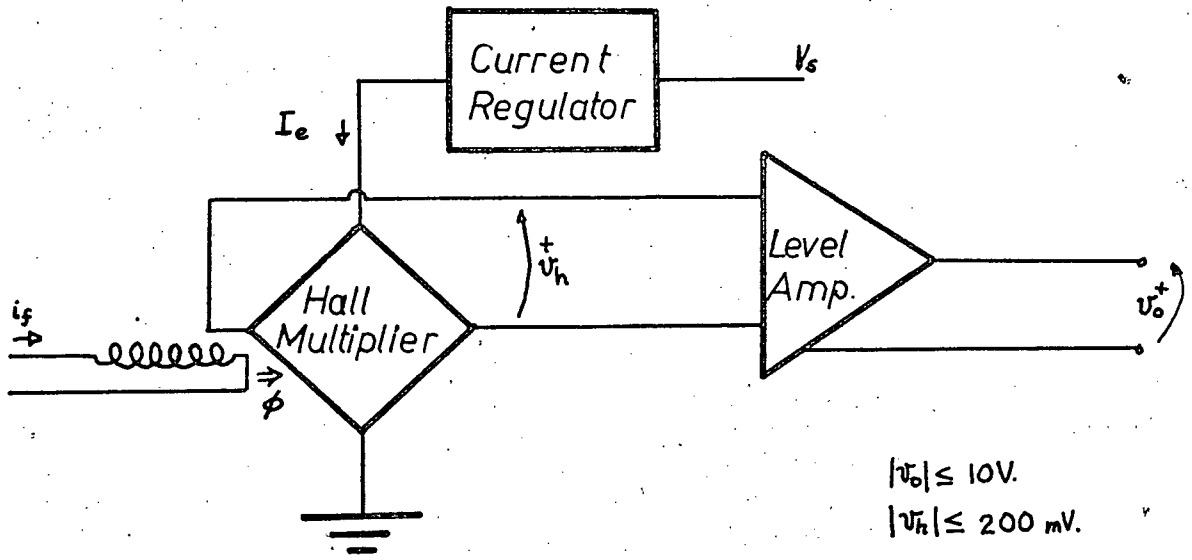
A Hall multiplier was chosen for use as a current transducer. The design used incorporates a constant-current source to provide excitation for the Hall multiplier, and a differential amplifier to boost the output signal for transmission to the computer. A block diagram of this configuration is shown in figure 3.1.

The Hall multiplier was selected in preference to a number of other devices, including series resistances, current transformers, and magnetorestrictive devices. Current transformers and magnetorestrictive devices were considered unsuitable because of d.c. cutoff and high cost, respectively. The Hall multiplier was chosen over series resistance primarily because of its electrical isolation between input and output and its availability in a number of input current ranges.

3.2.1.1 Hall Multiplier

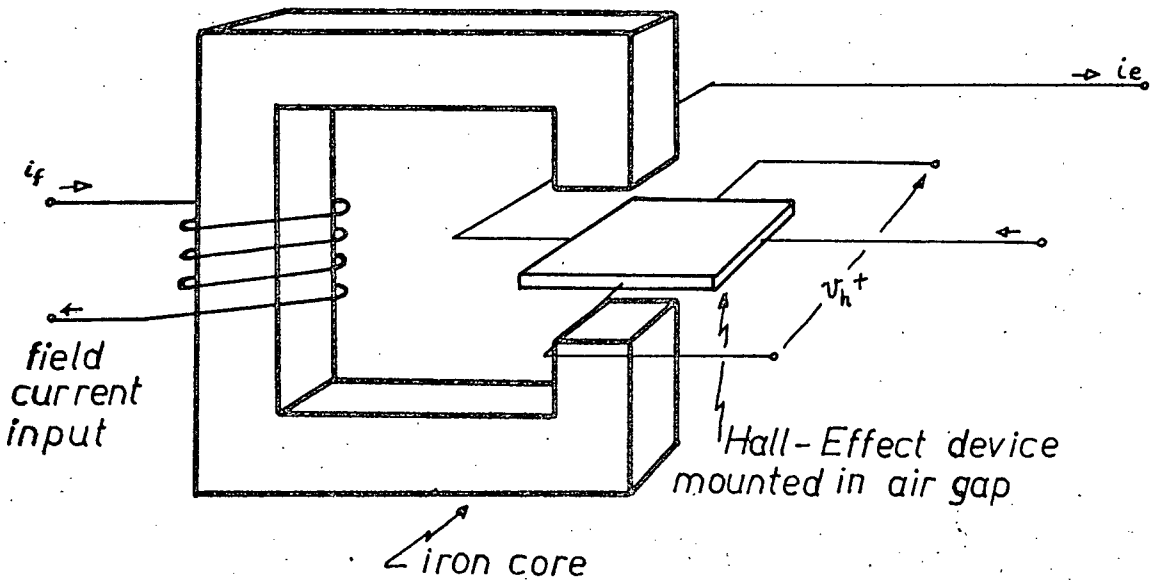
A simple diagram of a Hall-Effect multiplier is shown in figure 3.2. The current to be measured, i_f, flows through the winding encircling the iron core causing a proportional magnetic field to be set up in the air gap. The voltage at the output of the Hall-Effect device, v_h, is equal to $K_h i_e i_f$, where K_h is a constant, and i_e is the excitation current. If i_e is constant, v_h is equal to Ki_f, where K is a constant.

Two different multipliers were used in the current transducer design to provide several input current ranges. Six current transducers with input ranges, 0-40 amperes and 0-20 amperes, and six current transducers with input ranges, 0-3 amperes and 0-1.5 amperes, are provided for the six current inputs allowed. A list of specifications of the Hall multipliers utilized in the design is presented in Table 3.1.



CURRENT TRANSDUCER CONFIGURATION :

FIGURE 3.1



HALL MULTIPLIER :

FIGURE 3.2

Table 3.1: HALL MULTIPLIER SPECIFICATIONS (BELL INC.)

Parameter	Model No. HM-3500 (for parallel connected field coils)	Model No. HM-3010
A. Magnetic Field Input		
Resistance	1 mΩ.	0.06Ω.
Temp. Coeff. of above	0.39%/°C.	0.39%/°C.
Reactance	20 mΩ/KHz.	4 Ω/KHz.
Current Rating	40 A.	3 A.
Frequency Range	≤ 1 KHz.	≤ 1 KHz.
B. Hall Input		
Resistance (i_f = 0)	20 Ω.	2.5 Ω.
Temp. Coeff. of above	< +.02%/°C.	≤ +.15%/°C.
Magnetoresistance	< +2.5% of Rin	< 25% of Rin
Current Rating	330 mA.	330 mA.
Frequency Range	≤ 100 KHz.	≤ 500 KHz.
C. Hall Output		
Resistance	10 Ω.	10 Ω.
Load Resistance	50 Ω.	50 Ω.
Maximum Output	200 mV.	200 mV.
Temp. Coeff. of v_h		
0°C. to 50°C.	≤ ±.5%	≤ ±.5%
-25°C. to 75°C.	≤ ±1%	≤ ±1%
D. Hall Output vs. Field Input		
Linearity Error (i_f=K)	< .5% F.S.	< .5% F.S.
Remanent Residual	< .5% F.S.	< .5% F.S.
Phase Shift	3°/KHz.	3°/KHz.
Frequency Response	-.3 dB/KHz.	-.3 dB/KHz.
Inductive Error Voltage	< .2 mV/KHz.	< .1 mV/KHz.
E. Hall Output vs. Hall Input		
Linearity Error (i_f=K)	< .25% F.S.	< .25% F.S.
Resistive Error Voltage	< .3 mV.	< .1 mV.
Thermal Error Voltage	< .3 mV. d.c.	< 12 mV. d.c.

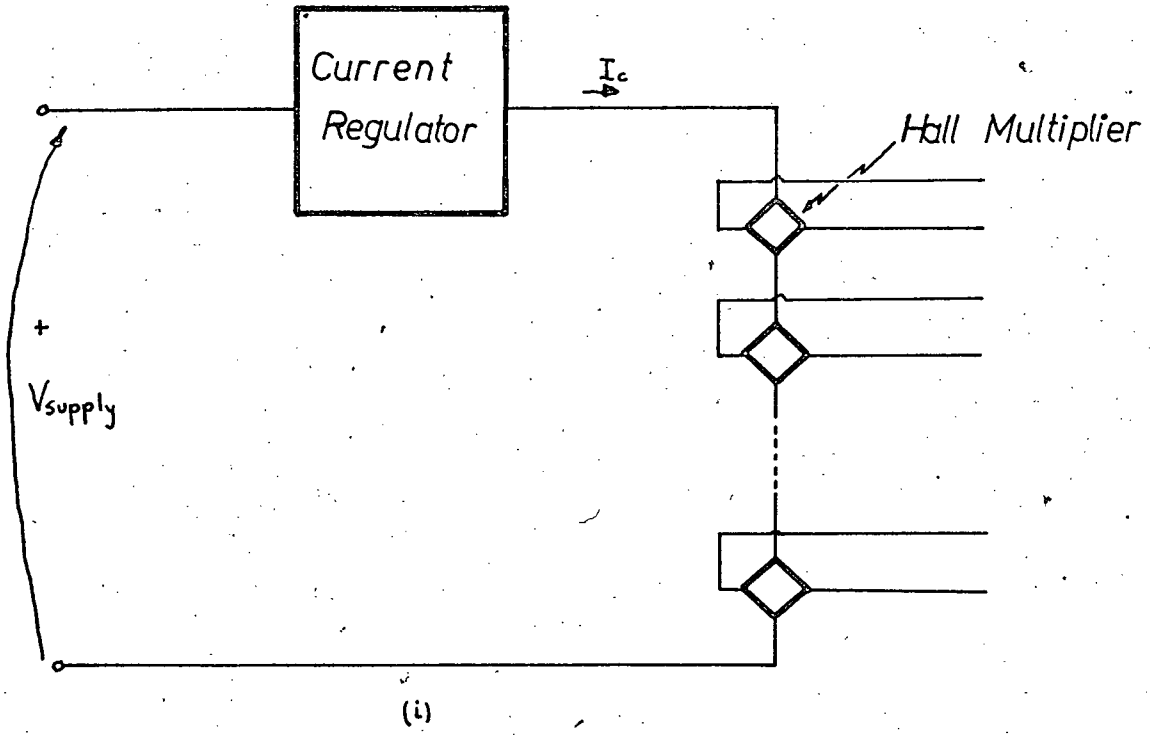
3.2.1.2 Constant-Current Source

A constant-current source was implemented using a voltage source and a current regulator. Both discrete-component "voltage/current cross-over" supplies[6] and integrated-circuit regulators were considered for use as current regulators. Several possible configurations, as shown in figure 3.3, were considered for supplying excitation current to the 12 Hall multipliers. In figure 3.3(i) and 3.3(ii), one main discrete-component regulator is used while in figure 3.3(iii) individual integrated-circuit regulators are used. Configuration 3.3(i) is superior to 3.3(ii) and 3.3(iii) for current regulation; however, a fairly large current regulator is needed to maintain the voltage drop across the multipliers (approx. 50 volts @ 300 mA). On the basis of lower cost, it was decided to use individual regulators as shown in figure 3.3(iii).

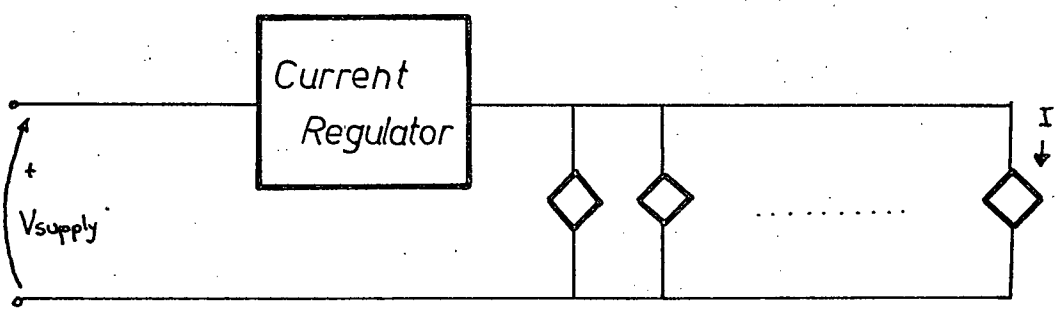
The design of the individual regulators was straightforward. Fairchild μA723C voltage regulators were used in the circuit shown in figure 3.4 to regulate the voltage drop across a current-sensing resistance. The specifications of the μA723C regulator are listed in Table 3.2. The current-handling capabilities of the regulators were extended by using power transistors at the outputs. This design provides a measured current regulation of 0.05% for load variations (0Ω. to 20Ω) under typical laboratory conditions.

3.2.1.3 Level Amplifier

A level amplifier is required to boost the ±200 mV.F.S. output of each Hall multiplier up to the ±10 V.F.S. transmission level. Since the Hall-Effect device has a common-mode voltage superimposed on its output due to the voltage drop in the resistive semiconductor material from the 300 mA. excitation current, a differential amplifier is required. This amplifier must have a differential gain of 50 and a common-mode rejection ratio better



(i)



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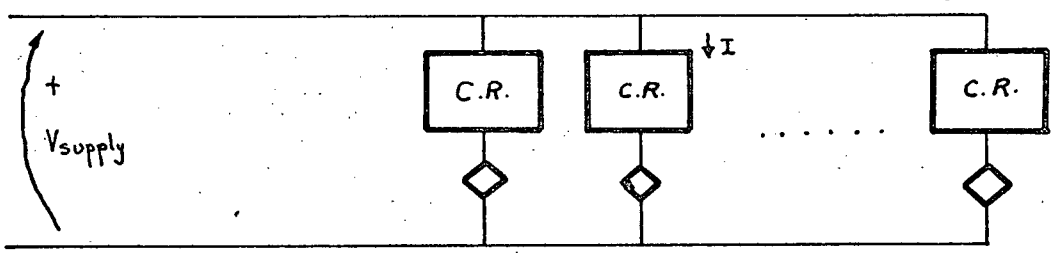
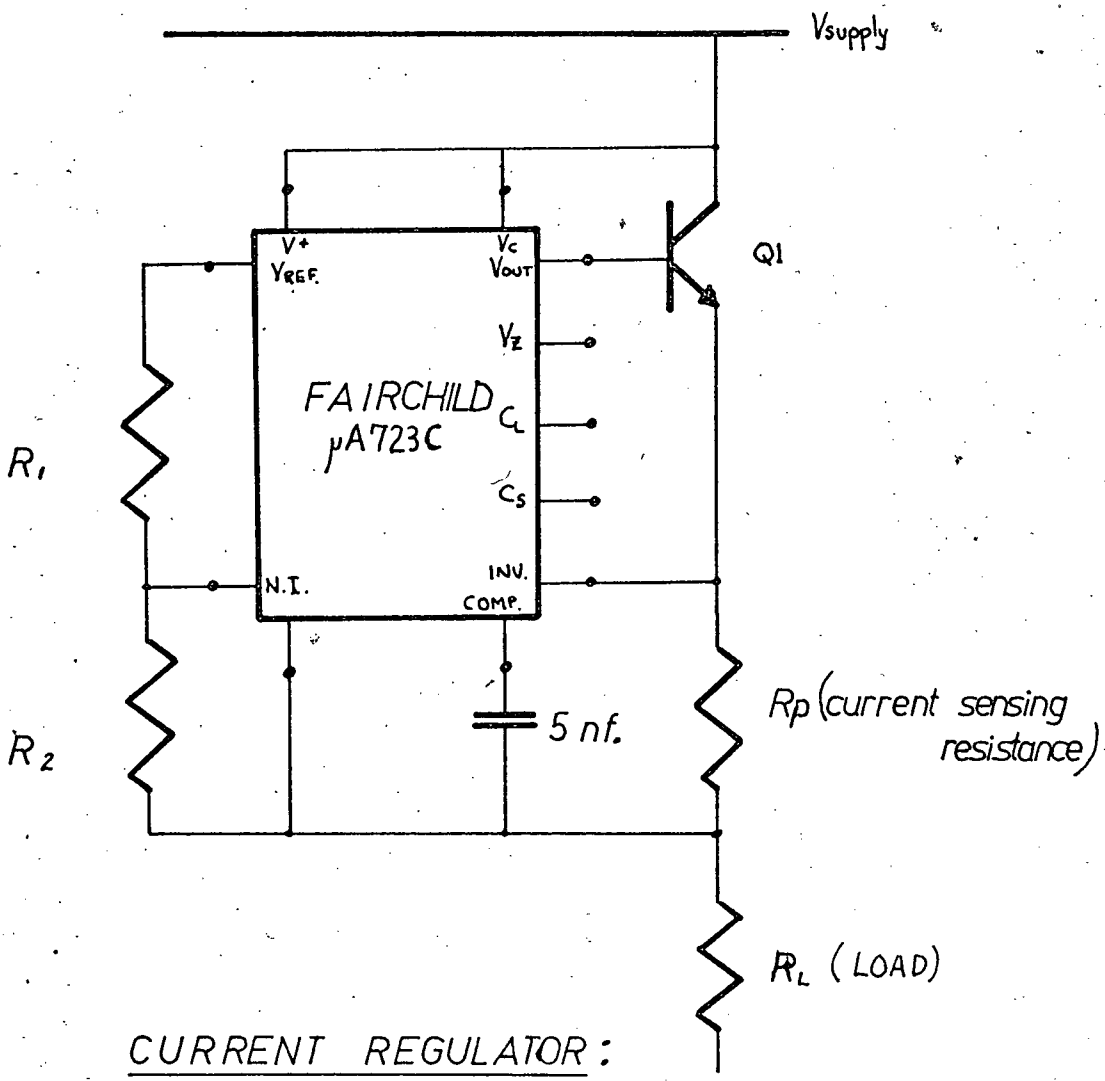


(iii)

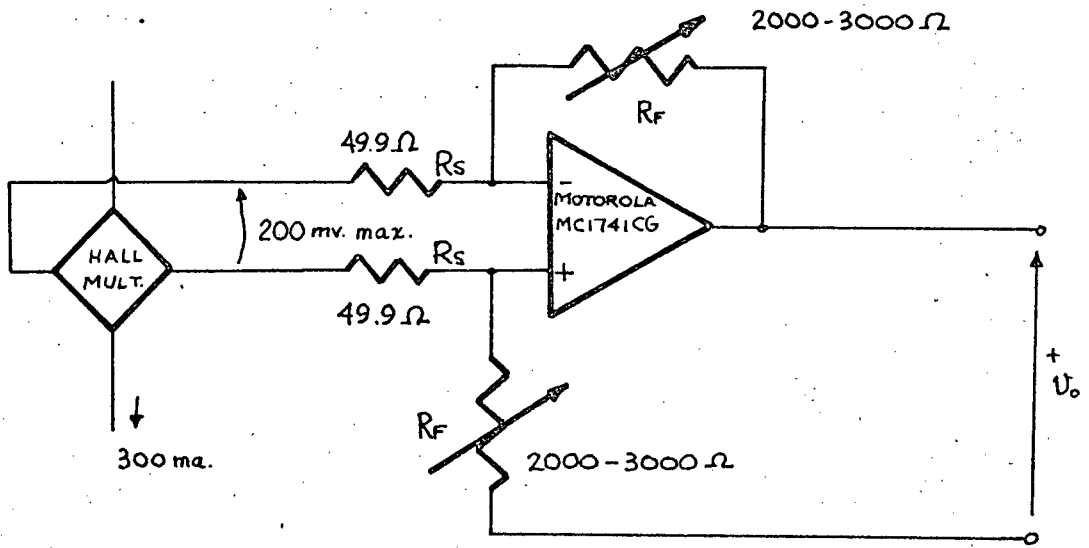
CURRENT REGULATOR CONFIGURATIONS :

FIGURE 3.3



CURRENT REGULATOR:

FIGURE 3.4



DIFFERENTIAL AMPLIFIER DESIGN:

FIGURE 3.5

Table 3.2: SPECIFICATIONS OF FAIRCHILD μA723C

Parameter	Condition	Min.	Typ.	Max.	Unit
Line Regulation	V_{supply}=12 V. to 15 V.		0.01	0.1	$\%V_{out}$
	V_{supply}=12 V. to 40 V.		0.1	0.5	$\%V_{out}$
	V_{supply}=12 V. to 15 V. ($0^o \leq T_A \leq 70^o$ C)			0.3	$\%V_{out}$
Load Regulation	Load Current=1 to 50 mA.		0.03	0.2	$\%V_{out}$
	Load Current=1 to 50 mA. ($0 \leq T_A \leq 70^oC$)			0.6	$\%V_{out}$
Ripple Rejection	f=50 Hz. to 10 KHz.		74		dB.
	f=50 Hz. to 10 KHz.		86		dB.
Average Temp. Coeff. of V_o	$0 \leq T_A \leq 70^oC$.		0.003	0.015	$\%/^oC$.
Reference Voltage		6.80	7.15	7.50	V.
Long Term Stability			0.1		%/1000 hrs.
Input Voltage Range		9.5		40	V.
Output Voltage Range		2.0		37	V.
Input-Output Voltage Differential		3.0		38	V.

ABSOLUTE MAXIMUM RATINGS

Input-Output Difference Voltage	40 V.
Maximum Output Current	150 mA.
Internal Power Dissipation	800 mW.
Operating Temperature Range	0^oC to 70^oC.
Current from V_{REF}	15 mA.

than 250:1. Finally, the output impedance of the amplifier should be as low as possible to facilitate proper signal transmission.

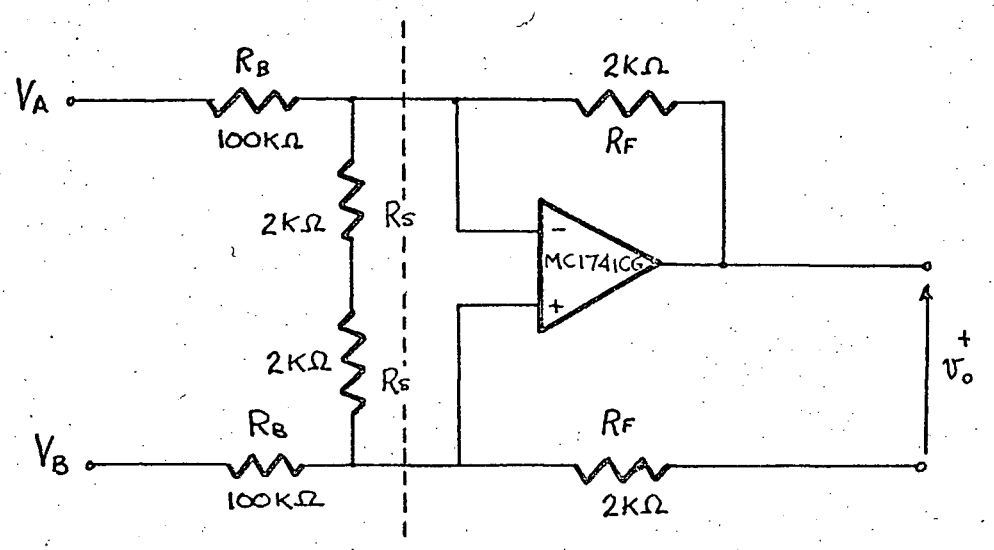
The amplifier designed for this purpose is shown in figure 3.5, using a Motorola MC1741CG operational amplifier with specifications as listed in Table 3.3. The details of the design of this amplifier are summarized in APPENDIX A.

3.2.2 Voltage Transducers

A voltage divider followed by a unity-gain buffer amplifier as shown in figure 3.6 were used in the design of the voltage transducer. This arrangement allows the reduction of the ±500 V.F.S. laboratory inputs to the ±10 V.F.S. transmission levels. To permit voltage measurements with respect to an ungrounded reference, a balanced divider and differential amplifier were used. Two measurement ranges, 0-500 volts and 0-10 volts, were provided. The details of the design of these transducers are summarized in APPENDIX B.

TABLE 3.3: SPECIFICATIONS OF MOTOROLA MC1741CG

Parameter	Condition	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10$ K Ω.		2.0	6.0	mV.
Input Offset Current			30.	200.	nA.
Input Bias Current			200.	500.	nA.
Input Resistance		0.3	1.0		mΩ.
Large Signal Voltage Gain	$R_L \geq 2K\Omega$., $V_{OUT} = 10$ V.	20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ KΩ.	±12	±14		V.
	$R_L \geq 2$ KΩ.	±10	±13		V.
Input Voltage Range		±12	±13		V.
CMRR	$R_S \leq 10$ KΩ.	70	90		dB.
Supply Voltage Rejection Ratio	$R_S \leq 10$ KΩ.		30	150	μV./V.
Power Consumption			50	85	mW.
Transient Response (unity gain)	$V_{IN} = 20$ mV. $R_L = 2$ KΩ.; $C_L \leq 100$ pf.				
-risetime			0.3		μsec.
-overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ KΩ.		0.5		V./μsec.
* The following apply for $0^oC \leq T_A \leq 70^oC$.					
Input Offset Voltage	$R_S \leq 10$ KΩ.			7.5	mV.
Input Offset Current				300.	nA.
Input Bias Current				800.	nA.
Large Signal Voltage Gain	$R_L \geq 2$ KΩ. $V_{OUT} = \pm 10$ V.	15,000			
Output Voltage Swing	$R_L \geq 2$ KΩ.	±10			V.



$|v_o| \leq 10$ v.

$|V_A - V_B| \leq 500$ v.

VOLTAGE TRANSDUCER DESIGN:

FIGURE 3.6

4. RESULTS

Two series of measurements were made on the transducer set to determine its performance.

4.1 First Set of Measurements

The first set was conducted on the transducer set by itself. Measurements were made to determine: (1) measurement error, (2) offset drift, (3) common-mode rejection ratio, and (4) frequency response. A description of the tests performed is included in APPENDIX C. The results of these tests are presented in Table 4.1.

To begin with, the performance of the current transducers under typical laboratory conditions was checked. The largest magnitude of measurement error observed was 0.82% F.S. for both the 0-40 and 0-3 ampere input ranges. The typical output offset drift over a period of three hours was found to be 0.12% F.S. for all input ranges. Finally, the typical frequency cutoff was measured to be approximately 30 KHz.(for the 0-3 ampere input range).

A similar set of measurements was made on the voltage transducers to check their performance. For the 0-500 volt input range, the largest measurement error observed was 0.39% F.S. The output offset drift in this case was negligible for a three-hour measurement period. The worst common-mode rejection ratio was 104:1. As well, the frequency response was flat to within ± 3 dB up to a frequency of 40 KHz. Though the 0-500 volt input range was found to perform adequately, the 0-10 volt input range was unsatisfactory because the 2:1 voltage divider used in the design did not provide for large common-mode voltages.

Table 4.1: MEASURED TRANSDUCER CHARACTERISTICS

Type of Transducer	Max. D.C. Measurement Error (%F.S.)	Typ. A.C. Measurement Error (%F.S.)	Output Offset Drift %F.S./3 hrs.	CMRR @D.C.	CMRR @A.C. 60 Hz.
Voltage (0-500 V.)	0.39	0.66	negligible	104:1	106:1
Current (0-40A)	0.82	-	0.115	-	-
Current (0-3A)	0.63	-	0.114	-	-

4.2 Second Set of Measurements

To evaluate the design more fully, a system similar to the one proposed for the electrical machines laboratory was set up. This system was implemented in the hybrid computer laboratory using the PDP-9 computer, the hybrid interface, and the transducer set developed. System errors were measured using d.c. inputs only. A full description of the tests conducted is included in Appendix C.

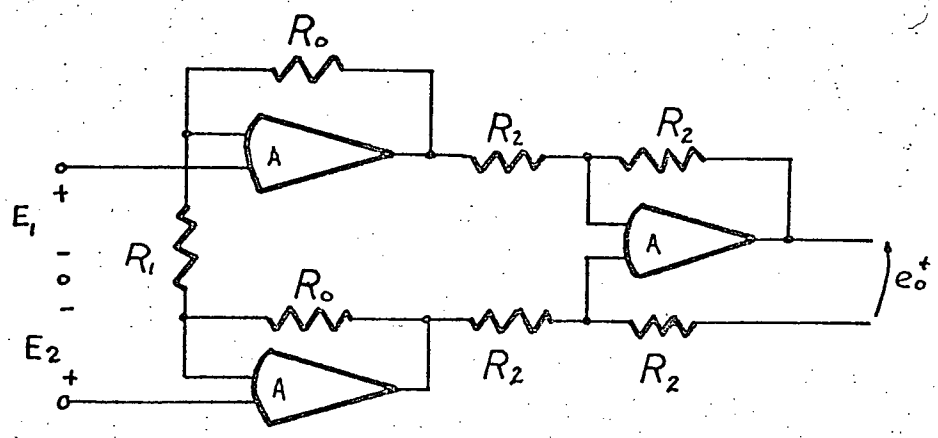
The worst measurement errors were found to be 2.2% F.S. for the current inputs and 1.4% F.S. for the voltage inputs. These values are somewhat larger than anticipated. The main source of error appears to be the offset voltage in the analog to digital interface. At the time of measurement, the input offset voltage on the hybrid interface was rather large ($\cong$ 70 mV.). Subsequent measurements show that the normal input offset voltage is of the order of 20 mV. Hence, better results may be expected with this system than were obtained in this test. As well, it should be feasible to reduce the overall error even more by compensating for the offset voltage either with hardware or software.

5. CONCLUSIONS AND SUGGESTIONS

A set of transducers for measuring current and voltage waveforms on an electrical machine set was designed, constructed, and tested. The results of this design have been presented and it is concluded that the hardware developed is useful as a part of a data acquisition and processing system for the electrical machines laboratory. A complete system is proposed for use with the transducers developed. Partial tests were made on this system. The results indicate that the system design proposed is workable.

Future development of this equipment will require additional hardware and software before practical computer-assisted laboratory instruction can commence.

For hardware, it is recommended that additional ranges for input to the transducers be provided. In particular, the addition of lower voltage ranges to the voltage transducer will require an improved differential level amplifier such as shown in figure 5.1. As well, transducers to measure shaft angle, velocity, and torque might be added. Overload protection for the current transducers must be investigated. Though the voltage transducers may be easily protected using back-to-back zener diodes at the inputs of the operational amplifiers, interruption of an overcurrent is more difficult. The use of fast-acting fuses designed for SCR protection is a possible solution. In addition, low-pass filters with lower cutoff frequencies than the ones now being used on the transducer inputs may be required. If the transducers are to be used with a PDP-8/L or NOVA computer, hardware such as an additional 4K of memory, an external bulk storage device such as a disc, and modifications to the multiplexer on the analog interface to handle 16 channels with individual sample-and-hold units will be desirable. Alternatively, use of the PDP-9 computer will require the installation of 16 lines



$$e_o = \left(1 + \frac{2R_o}{R_1}\right)(E_2 - E_1)$$

A SUPERIOR DIFFERENTIAL AMPLIFIER :

FIGURE 5.1 :

from the electrical machines laboratory to the hybrid computer laboratory. Eventually, a display or x-y plotter would be useful for the display of graphical information.

To provide a useful working system, an efficient software package is essential. Software is available for data acquisition and processing using the hybrid interface and PDP-9.[3,7] However, additional software will be required, even if these routines can be used, to calculate the proper values required for the experiment. Eventually, a dedicated executive routine may be required to permit time-sharing of a number of machines and to sequence the various routines in the proper order.

APPENDIX A

CURRENT TRANSDUCER AMPLIFIER DESIGN

The output voltage, e_o, from a differential amplifier of the configuration shown in figure 3.5 is[9]

$$\frac{-R_f}{R_s} (e_1-e_2) \quad ,$$

where R_f is the feedback resistance, R_s is the input resistance, and e_1-e_2 is the input differential voltage. For this design, R_f/R_s was set at 50 to boost the $\pm$200 mV.F.S. output from the Hall multiplier up to $\pm$10 V.F.S.

Several non-ideal aspects of the operational amplifier must be considered to avoid errors. First of all, an offset in the output voltage may exist due to the input offset voltage, the input offset current, and the input bias current. If a balanced circuit is used, the input bias current effects will tend to cancel each other out so that the output offset voltage[9] is essentially

$$\Delta V_{OUT} = [1 + R_f/R_s] V_{os} + R_f I_{os} \quad ,$$

where V_{os} is the input offset voltage and I_{os} is the input offset current. To reduce ΔV_{OUT}, R_s was set at a fairly low value, 49.9Ω., which does not attenuate the Hall multiplier output substantially. At 25°C., $\Delta V_{OUT\ max.}$ was calculated to be 0.306 volts. This voltage may be nulled using the zero null feature of the operational amplifier. Over the temperature range, 0° to 70°C., $\Delta V_{OUT\ max.}$ should not exceed 0.383 volts. Hence, the net maximum offset voltage after nulling is approximately 0.076 volts (error $\cong$ 0.76% F.S.). Though this calculation is rather crude, the actual implementation has verified that the offset voltage is not a serious problem.

Since the Hall multiplier is resistive in nature, the excitation current generates a common-mode voltage of approximately 0.5 volts at the output terminals. To check the error due to the common-mode voltage, the common-mode rejection ratio of the differential amplifier must be considered. The overall common-mode rejection ratio for the resistive network and operational amplifier configuration of figure 3.5 is[8]

$$CMRR_t = \frac{1}{\frac{1}{CMRR_c} + \frac{1}{CMRR_{op\ amp}}} ,$$

where the common-mode rejection ratio of the resistive network is given by

$$CMRR_c = \frac{1 + R_f/R_s}{4a} ,$$

where a represents the maximum fractional deviation in resistance. Using 1% tolerance resistors, the overall common-mode rejection ratio is approximately 1275 yielding an output error of approximately 0.196% F.S. A temperature coefficient specification of ± 50 ppm./^{o}C. limits resistance variations to $\pm 0.25\%$ from 0^{o} to 50^{o}C. which is more than adequate.

APPENDIX B

VOLTAGE TRANSDUCER AMPLIFIER DESIGN

The design of this amplifier is similar to that used for the current transducers. The circuit designed is shown in figure 3.6.

This circuit may be analyzed by taking the Thévenin equivalent circuit at the output of the resistive divider. The equivalent circuit is balanced with an equivalent voltage source of value

$$\frac{R_s}{R_s + R_B} (V_A - V_B) \text{ volts}$$

and two equivalent resistances of value

$$\frac{R_s R_B}{R_s + R_B} \quad \Omega .$$

This reduces the resistive network to the standard differential amplifier form as in figure 3.5. The output voltage is equal to

$$e_o = \frac{-R_f}{R_B} (V_A - V_B) .$$

A value of R_f/R_B equal to 1/50 was chosen for this design. To provide an input resistance of several thousand ohms, R_B was chosen to be 100 KΩ. and R_f to be 2 KΩ. To dissipate the power loss, 7 watt precision power resistors were used for R_B.

Since R_f/R_s is close to unity, the input offset voltage is not amplified. A net maximum output offset error of 0.08% F.S. was calculated for this design.

The output error due to common-mode voltages at the input is a serious problem. For a 500 volt common-mode voltage, an overall common-mode rejection ratio of 100 is required to limit the output error due to these voltages to 1% F.S.. Since the overall CMRR is approximately equal to

$$\frac{1 + R_f/R_s}{4a},$$

a must not exceed 0.005. Hence, resistances with a tolerance of $\pm 0.5\%$ were specified for this design. Also resistor temperature coefficients of ± 50 ppm./$^{\circ}$C. were used.

APPENDIX C

DESCRIPTION OF TESTS

C.1 Transducers Only

C.1.1 Measurement Error

The configuration shown in figure C.1 was used to measure the input/output characteristics of the transducers. Inputs were applied and measured and from this the correct outputs were calculated based on the desired transducer ratio. Next, the actual outputs were measured and the differences between the actual and calculated outputs were used to compute the measurement errors. This measurement also gives some indication of the linearity of the transducers since a number of inputs were used in the tests.

Measuring Equipment:

D.C. Voltage Source: Heathkit 0-400 V.D.C. reg. supply

D.C. Current Source: Lambda 1-4 V.D.C. reg. supply and precision resistances

A.C. Voltage Source: a.c. line (120 V.(r.m.s.)@ 60 Hz)

Dropping Resistances: precision 1(1-.0012) Ω.
.1(1+.0013) Ω.
.05(1+.0014) Ω.

Voltmeter: Fluke $4\frac{1}{2}$ digit Digital Voltmeter
accuracy: specified to be ≤.05% F. S.
measured to be ≤ .10% F.S.

Measurement Conditions:

-bench environment

-approx. 70°F. temperature

-1 hour warm-up period

Inputs Used:

D.C.: 420,300,200,100,50,0 volts

A.C.: 120 V.(r.m.s.)

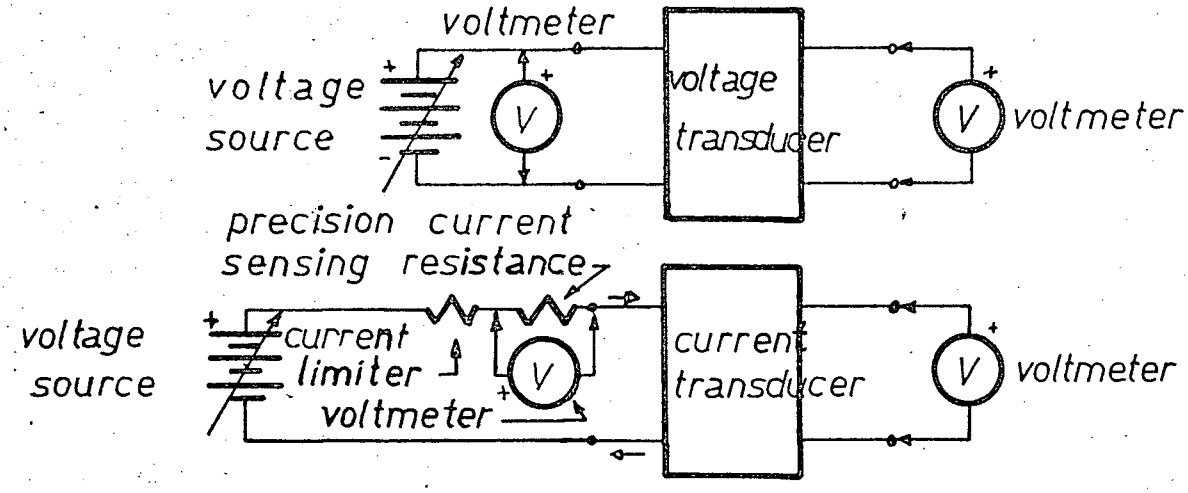


FIGURE C.1: MEASUREMENT ERROR TEST

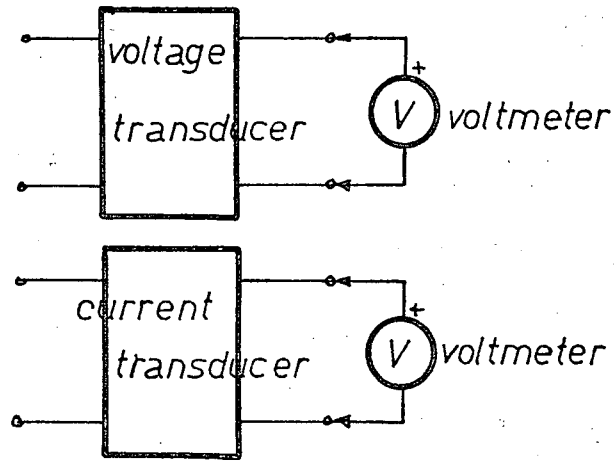


FIGURE C.2: OFFSET DRIFT TEST

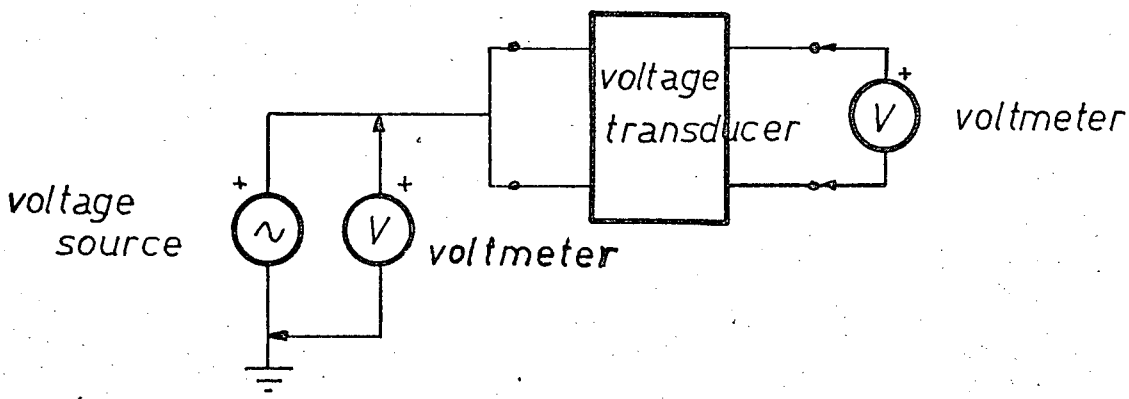


FIGURE C.3: CMRR MEASUREMENT

C.1.2 Offset Drift

With no inputs, the output voltage was monitored for a period of approximately three hours using the FLUKE digital voltmeter (as shown in figure C.2). The measurement conditions were the same as in C.1.1.

C.1.3 Common-Mode Rejection Ratio

In this case, test inputs of 250 volts d.c. and 120 volts a.c. (60 Hz.) were used as shown in figure C.3. From this, the common-mode gain of the voltage transducers was computed. The common-mode rejection ratio was calculated using

$$CMRR = \frac{G_D}{G_{cm}} \quad ,$$

assuming G_D equal to 1/50. In this set of measurements, the FLUKE digital voltmeter was used to measure the various voltages and the test conditions were identical to those of C.1.1.

C.1.4 Frequency Response

Inputs from a WAVETEK signal generator were used in this test as illustrated in figure C.4. The gain of the transducers was estimated using a TEKTRONICS TYPE 581 oscilloscope. The cutoff frequency was considered to be the lowest frequency at which the gain was reduced by 3 dB. The values obtained are only approximate.

C.2 System Test

The transducers developed were connected to the hybrid interface and PDP-9 computer in the hybrid computer laboratory as shown in figure C.5. Constant voltages and currents were used as test inputs and were measured using the FLUKE digital voltmeter. The PDP-9 computer was programmed as

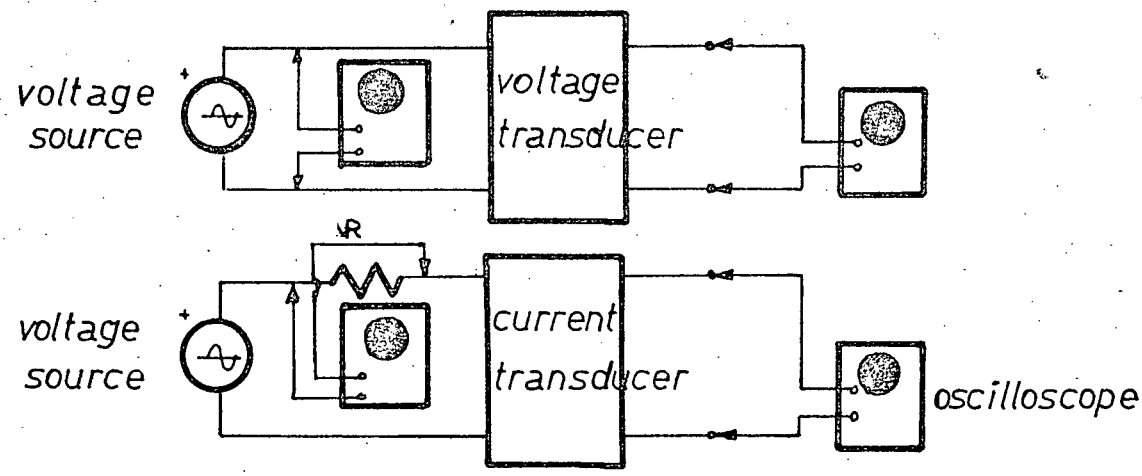


FIGURE C.4 : FREQ. RESPONSE TEST

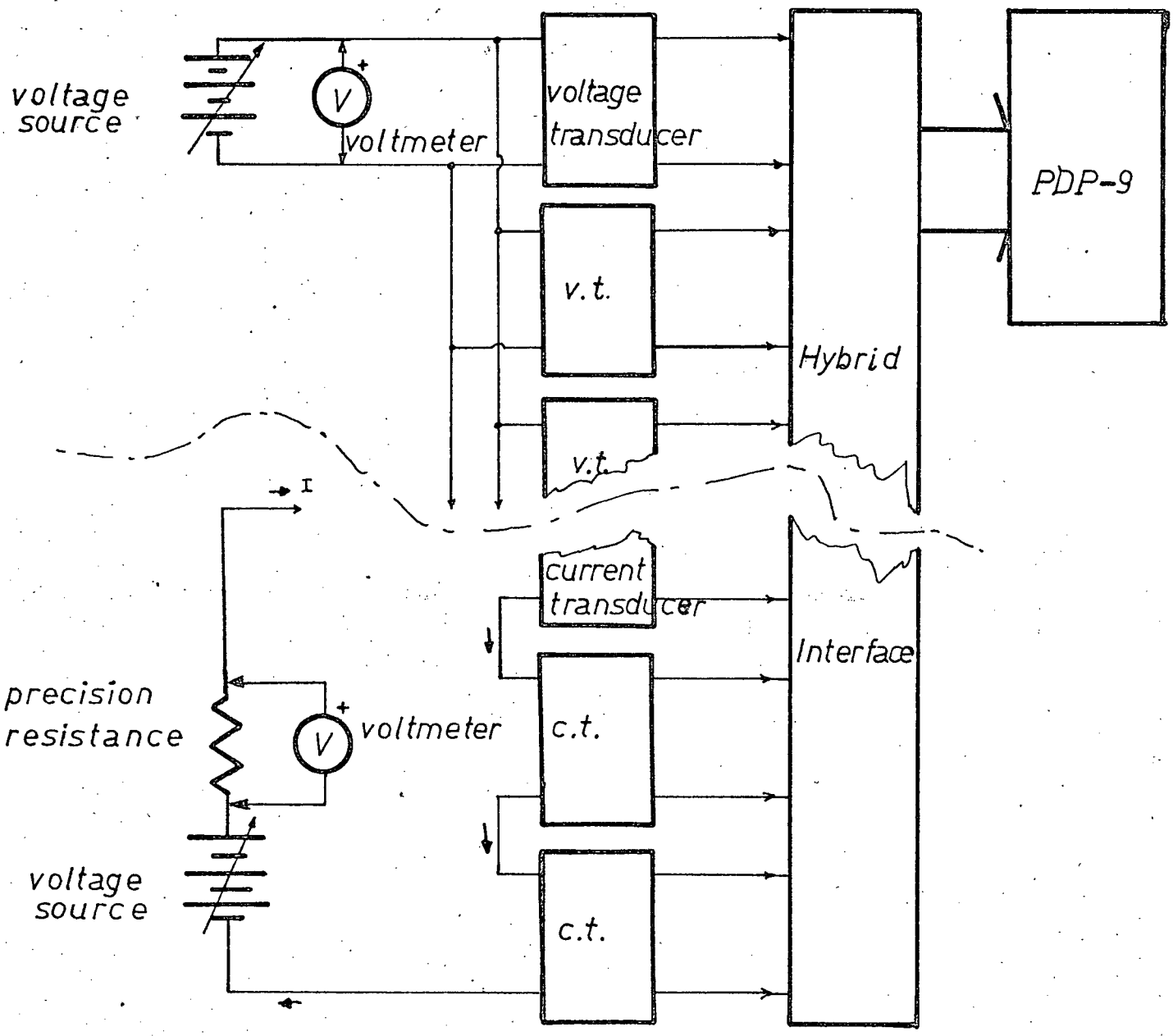


FIGURE C.5 : SYSTEM TEST

shown in the flow chart of figure C.6 and the program listing of figure C.7. In addition, measurements were made on the hybrid interface itself as shown in figure C.8 to determine its input/output characteristics. From this, the gain of the interface was computed assuming linearity and the measurement errors were calculated using this ratio.

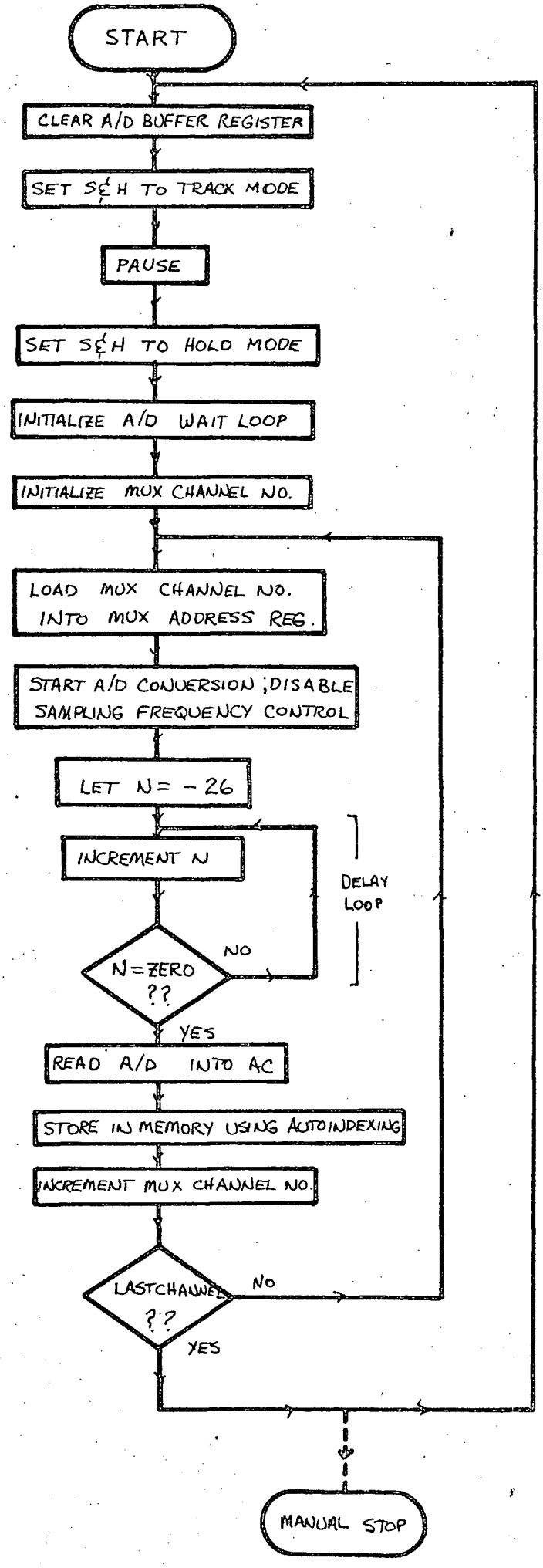
Test Conditions:

- approx. $66^{o}F$.
- hybrid computer laboratory environment
- gain of interface measured and used to compute measurement error
- sampling period approx. 101 μsec./channel
- error calculated from worst error committed in 10 successive samples.

Inputs:

D.C. Voltage: Heathkit 0-400 V.D.C. reg. supply; @ 420.4, 350.4, 300.4, 230.5, 160.5, 109.9, 20.18 volts

D.C. Current: Lambda 1-4 V.D.C. reg. supply; precision dropping resistances: 1(1-.0012), 0.1(1 + .0013), 0.05(1 + .0014)Ω. @ 38.19, 33.31, 24.98, 20.02, 15.00, 10.92, 2.50 amperes

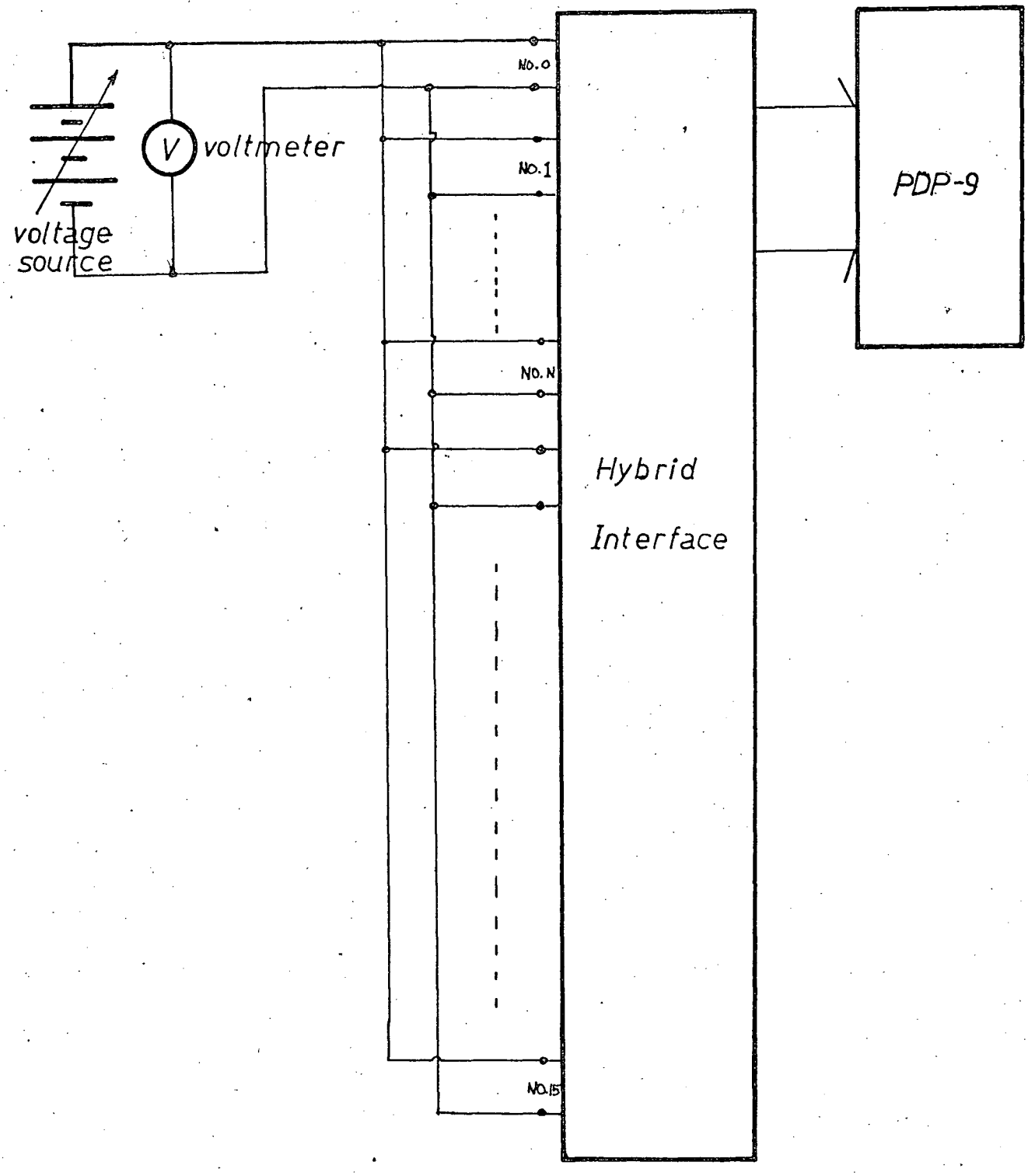


FLOW CHART
FIGURE C.6

Figure C.7: DATA ACQUISITION PROGRAM LISTING

```
1Ø                  3Ø3
 .                   .
 .                   .
 .                   .

1ØØ                 7Ø11Ø4      / CLEAR SII# 11 (A/D BUFFER REG.)
                    14Ø2ØØ      / DEPOSIT A ZERO IN 2ØØ
                    2ØØ2ØØ      / LAC 2ØØ
                    74ØØØ1      / COMPLEMENT AC
                    7Ø16Ø7      / LOAD S & H VIA SOI# 16 to TRACK
                    74ØØØØ      / NOP
                    74ØØØØ      / NOP
                    2ØØ2ØØ      / LAC 2ØØ
11Ø                 7Ø16Ø7      / LOAD S & H VIA SOI# 16 to HOLD
                    2ØØ2Ø1      / LAC 2Ø1 : (2Ø1) = 77776Ø
                    Ø4Ø3ØØ      / DAC 3ØØ : (3ØØ) ≡ COUNT
                    2ØØ2ØØ      / LAC 2ØØ : (2ØØ) = ØØØØØØ
                    Ø4Ø3Ø1      / DAC 3Ø1 : (3Ø1) ≡ MUXADD
115                 2ØØ3Ø1      / LAC 3Ø1
                    7Ø14Ø7      / LOAD MUX ADDRESS DIRECTLY
                    7Ø13Ø6      / START A/D CONV.; DISABLE SFC
12Ø                 2ØØ2Ø2      / LAC 2Ø2 : (2Ø2) = 777746
                    Ø4Ø3Ø2      / DAC 3Ø2 : (3Ø2) ≡ A/D COUNT
122                 44Ø3Ø2      / ISZ 3Ø2
                    6ØØ122      / JMP .-1
                    7Ø1117      / CLA-E.T.# 1, LOADBUFF, JAM AC
                    Ø6ØØ1Ø      / CLEAR BUFF /// DAC* 1Ø
                    44Ø3Ø1      / ISZ 3Ø1 (MUXADD)
                    44Ø3ØØ      / ISZ 3ØØ (COUNT)
13Ø                 6ØØ115      / JMP 115
131                 6ØØ1ØØ      / JMP 1ØØ
 .                   .
 .                   .
2ØØ                 ØØØØØØ
2Ø1                 77776Ø      / → COUNT
2Ø2                 777746      / → A/D COUNT
 .                   .
 .                   .
3ØØ                 ØØØØØØ
3Ø1                 ØØØØØØ
3Ø2                 ØØØØØØ
```



INTERFACE CHARACTERISTICS MEASUREMENTS:

FIGURE C.8:

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