SILICON THIN-FILMS

I. LOW-TEMPERATURE-SUBLIMED SILICON FILMS ON SAPPHIRE AND SPINEL SUBSTRATES,

II. A FIELD EFFECT STUDY OF THE METAL-INSULATOR-SEMICONDUCTOR STRUCTURE AND ITS APPLICATIONS IN NOTCH NETWORKS.

by

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ABSTRACT

A study of the structural and electrical properties of low-temperature-sublimed silicon films indicates that they are characterized by a high density of grain boundaries, hence crystal defects. A trapping model has been proposed to explain the experimentally observed temperature-dependencies of resistivity and carrier concentration of these films. The result shows that the defect density at the grain boundaries is of the order of $10^{12}$ cm$^{-2}$, and that it is independent of the doping concentrations in the films.

It has been shown that the thin-film metal-insulator-semiconductor (MIS) structure can be reduced to a transmission line problem by expressing the equivalent capacitance of the structure as a series combination of the depletion capacitance and the insulator capacitance.

The variations of both the capacitance and channel conductance of the MIS structure have been utilized to make notch filters in which the notch frequency can be varied over 200% by an external biasing voltage.

In view of the need for maintaining a constant null depth in the semiconductor notch filter under various biasing potentials, a new notch network has been proposed in which the optimal notch condition could be maintained simply by designing the ratios of the lengths and widths of the MIS structure to the appropriate values.
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Chapter 1
Introduction

The topics of this thesis are:-

(a) materials research in silicon thin-films grown at low substrate temperatures,
(b) a field-effect study on semiconductor thin-film distributed RC elements, and
(c) design, fabrication and characteristics of silicon thin-film notch filters.

1.1 Thin-Film Silicon on Sapphire and Spinel Substrates

Modern integrated circuit technology emphasizes high packing density as well as low parasitic capacitance in order to attain a higher frequency performance of both the passive and active devices fabricated on a single substrate wafer. In the monolithic integrated technology, the components are isolated by reverse biased p-n junctions at the substrate-device interface. Subsequently, the performance of such a circuit is often limited by undesirable high frequency coupling effects and dc leakage at the junctions. With silicon devices on insulating substrates, better electrical isolation is ensured by the removal of excess silicon around each circuit component. Recently, thin-film silicon devices on sapphire substrates have increased the operating frequencies of MOST digital integrated circuits beyond that of circuits with conventional MOSTs\textsuperscript{1}. In addition, feedback capacitance of less than 0.02 pF/electrode has been reported\textsuperscript{2} for MOS triodes and tetrodes which operate at 0.5-1 GHz.

Other advantages of silicon on insulating substrates include\textsuperscript{3}:

a) high strength and good heat conductivity, b) no parasitic capacitance to the substrate, c) very high packing density ($10^5$ complementary devices
per sq. in.), d) fewer processing steps required for CMOS memory cells as a result of complete substrate isolation and no space charge spread into the substrate, etc.

With chemical vapor deposition, epitaxial silicon on sapphire and magnesium-aluminum spinel substrates (SOS), having a carrier concentration of above $10^{17}$ cm$^{-3}$, can now be prepared with state-of-art properties similar to those of bulk silicon$^4$. However, an increasingly poor carrier mobility is observed at lower carrier concentration, with a maximum occurring at the doping level of $10^{16}$-$10^{17}$ cm$^{-3}$. Mobility degradation at higher carrier concentration is attributed to ionized impurity scattering similar to that observed in bulk silicon; and that at lower carrier concentration is caused by phonon scattering$^5$ and possibly by an increase in the space charge region around inhomogeneously distributed defects$^6$.

At temperatures above 1000°C, silicon attacks sapphire and spinel substrates resulting in aluminum contamination (autodoping$^7$) of the grown film. Direct correlation of mobility degradation at low carrier concentration with aluminum autodoping can be deduced from the fact that the peak in the hole mobility versus hole concentration relationship is approximately an order of magnitude lower in silicon on spinel as compared to silicon on sapphire$^8$, which is consistent with Robinson and Dumin's$^9$ observation that autodoping is an order of magnitude less in silicon on spinel than in silicon on sapphire.

The techniques of growing silicon films by vacuum sublimation is given in chapter 2. An investigation on the structural and electrical properties of these films is reported in chapter 3. The stress has been on a low enough substrate temperature so that autodoping of the silicon films could be neglected. Consequently, their electrical properties
should be dominated by the mechanism of film growth as well as their structural properties rather than by substrate contaminations.

1.2 Silicon Thin-film Distributed RC Structures

Since the inception of SOS technology by Manasevit et al.\textsuperscript{10} in 1963, a number of active devices\textsuperscript{11-15} using epitaxial silicon films have been reported. All these devices, with the exception of the bipolar transistors, utilize a thin layer of dielectric on top of the epitaxial semiconductor for field effect modulation. Similarly, for device passivation, isolation (cross over technique), and field-effect enhanced R and C elements, the same configuration of an oxidized SiO\textsubscript{2} layer on Si is often employed. This gives rise to the semiconductor distributed RC structure. The introduction of semiconductor into the system leads to a wide variety of problems which are non-existent in the conventional distributed RC filter structure. These problems pertain to the electrical properties of semiconductor films and the insulator-semiconductor interface.

In chapter 4 a theoretical study has been made on the field effect of a thin-film distributed RC structure based on the existing theories of semiconductor surface physics\textsuperscript{16}. The emphasis is on channel conductance in the semiconductor film. A detailed mathematical modelling of an idealized, homogeneous metal insulator-semiconductor thin-film structure is presented in section 4.5. This is followed by a small signal analysis of a thin-film structure having a non-uniform space-charge layer.

In chapters 5 and 6 the uniformly distributed RC (URC) structure is applied to notch networks. In contrast to the conventional thin-film notch filters, both capacitance and conductance variations have
been utilized for notch-frequency tuning. Device characteristics are derived in section 5.3 using the depletion layer approximation, and the experimental results are reported in section 6.4.

In section 5.5, a new notch network using double URC structures has been proposed. Such a circuit will eliminate the variation in notch parameters during frequency tuning thereby maintaining a constant attenuation at the null which is unattainable with any of the known notch-networks.

The concluding remarks are presented in chapter 7.
CHAPTER 2
Vacuum Sublimation of Silicon Thin-Films

2.1 Introduction

In general there are 2 common methods* for growing large areas of epitaxial silicon films on insulating substrates:

(i) In chemical vapour deposition (CVD), silicon epitaxy can be obtained by hydrogen reduction of silicon tetrachloride \((\text{SiCl}_4)\) or trichlorosilane \((\text{SiHCl}_3)\), and by the pyrolysis of silane \((\text{SiH}_4)\) in hydrogen or helium atmosphere. A water-cooled reaction chamber is used to provide a streamlined horizontal flow of the entering gas over the RF heated susceptor surface. The substrates, residing on top of the pyrolytic-carbon coated pure carbon susceptor, are prefired (to remove the mechanically damaged surface layer) in a \(\text{H}_2\) atmosphere 100–200°C above the deposition temperatures for 10–15 min., before the temperature is lowered to that required for growth. A gas stream of the source materials is then introduced into the quartz reaction chamber and silicon deposition is immediately obtained on the substrate surfaces. Impurity doping of the films is accomplished by addition of \(\text{PH}_3\), \(\text{B}_2\text{H}_6\), or \(\text{AsH}_3\) to the gas stream during growth.

(ii) In vacuum evaporation, the substrate and source materials (usually just a piece of silicon) can be heated separately by electron bombardment or other means. Deposition of

* Other available methods are: ultra-thin alloy-zone-recrystallization and temperature-gradient-zone-recrystallization. A summary of single crystal film formation is given in table 2 of ref. 19, and that of the epitaxial technology in ref. 20.
silicon is commenced by retracting the shutter lying between them. This is done inside a high vacuum chamber where contaminations of the silicon vapour can be kept to a minimum. Doping of the films can be achieved by initially picking the 'right' source impurity concentration or, it can be introduced by a separate evaporation of the dopants at the time of film growth. The substrates can be cleaned either before their insertion into the vacuum system by \( \text{H}_2 \) pre-firing, or they can be heated up under vacuum to a higher temperature, minutes before the start of evaporation.

Despite the fact that high quality epitaxial silicon films can now be grown by the technologically well-innovated CVD method, they still suffer a major draw-back in the appreciable autodoping of substrate impurities into the films at temperatures above 1000°C. Recently, the use of very high deposition rates had been proven significant in the suppression of chemical attack on insulating substrates by impinging silicon vapour at the film-substrate interface. But it is also known that a large amount of autodoping in the films comes from the back side of the substrates through gas transport. Another new endeavour undertaken by major industrial research centers has been the use of helium ambient instead of \( \text{H}_2 \) for pyrolysis of silane in order to lower the optimal growth temperature by 100-200°C from the conventional 1050-1200°C range. The growth of good quality epitaxial silicon films by normal vacuum techniques is equally limited by the need for high substrate temperatures of over 1000°C.

Additional advantages of growing epitaxial silicon films at lower substrate temperatures are: a decrease in chemical reaction on the substrate surfaces, a reduction in thermal stress resulting from
different thermal expansions of the films and substrates, and a lower impurity contamination coupled with a minimized impurity diffusion effect inside the grown films. Recent technological advancement in low-temperature deposited SiO₂ films together with organic and inorganic dielectric films has created much interest in low-temperature device processings. The present investigation on low-temperature grown (centered about 800°C) silicon thinfilms is a continuation of the work initiated by Weisberg for the growth of epitaxial silicon films by vacuum sublimation on sapphire and spinel substrates.

2.2 Experimental Method

2.2.1 Apparatus

The sublimation compartment was mounted inside an Ultek TNB vacuum system. Roughing of the vacuum chamber was accomplished in 2 steps by 2 molecular sieve sorption pumps operating consecutively. Final pumping was done by two 50 litre/sec ion pumps plus a Ti sublimation pump rated at 3600 litre/sec for air. Vacuum inside the chamber was monitored using a Bayard Alpert ion gauge. A typical vacuum of 4 × 10⁻⁸ torr was obtained by first baking the system for 2-3 hours under roughing with 8-250W G.E. infra-red heat lamps supplying radiant heat into the chamber through the 14" DIA pyrex bell jar, followed by continuous pumping with both the ion and sublimation pumps for 4-5 hours.

The sublimation apparatus (shown schematically in fig. 2.1), with the exception of the substrate lamp holder which was in type 306 stainless steel, was made of high purity tantalum sheets. The silicon source was in the form of a rectangular bar, 1 1/4" × 3/4" × 30mil thick. It was rigidly suspended between the 2 L-shaped supports with 2 C-clamps separated by a distance of 1". The substrate, locating in the recess of the substrate holder (fig. 2.2), could be externally rotated in and out of the sublimation compartment via a magnetically coupled drive.
Fig. 2.1 Schematic diagram of the vacuum sublimation chamber.

- Ta shutter (integral part of the Ta shield)
- Substrate holder
- Rotatable substrate holder arm (type 306 stainless steel)
- Supporting frame (to ground) (1/8" thick Ta sheet)
- Recess for substrate
- Ta "C" clamps
- Ta Shield
- Si filament
- Mica sheet for electrical isolation between electrodes
Source to substrate spacing could be adjusted by raising or lowering the substrate holder arm, and was usually maintained at 1/8" to 1/4" separations. Such close spacing was chosen not only because of the low vapour pressure of silicon during sublimation but also to avoid the wide departure from equilibrium conditions of the silicon vapour over the substrate surface. Nicoll\textsuperscript{43} asserted that if the source-substrate spacing is less than about 1/10 of the diameter of the source and substrate, the chemical transport conditions in between are largely independent of conditions elsewhere in the system. In addition, close spacing of source-substrate also means direct transport of each component of the source material across the space.

Substrate heating was created partially by radiation from the
silicon source and, partially by a DWY-650W Tungsten Halogen quartz lamp focused onto the substrate holder 3" below by a Ta parabolic reflector. The electric power delivered to the lamp was controlled by a variac. The silicon bar was connected in series with an external carbon resistor, the conductance of which could be adjusted by changing the pressure on the 80-odd pieces of carbon slab, each 1" square x 1/8" thick, through a tightening screw at one end. Sublimation was obtained by passing electric current \(^{44,45}\) through the silicon with a home-made transformer rated at 50A max current.

In a typical run, a silicon surface temperature of 1350 ±20°C was maintained at the centre of the filament during sublimation. A temperature gradient of less than 50°C was observed from the centre portion to the two ends. This corresponds to a loss of about 20\(\mu\) per hour from the silicon filament, and provided a deposition rate of about 5\(\mu\) per hour on the substrate through a 20 ml thick quartz mask located at 1/4" from the source. Temperature of the source was monitored by a Hartman & Braun Pyropto (optical pyrometer) corrected with the emissivity data of Allen \(^{46}\); but it could also be calculated from the resistance of the silicon bar with the knowledge of intrinsic silicon resistivity vs. temperature \(^{47}\). The substrate temperature was obtained by a chromel-alumel thermocouple pressing on the back of the 20 ml thick, 1/2" dia. sapphire or spinel substrate.

### 2.2.2 Source and Substrate Preparation

A silicon filament cut out from a lapped wafer was etched in 1:1:2-HF (49%):HNO\(_3\) (70%):C\(_2\)H\(_4\)O\(_2\) for 1/2 minute to remove roughly 0.5 ml from each surface and give the silicon a high polish. It was then rinsed in boiling distilled water and two baths of deionized water prior
to insertion into the sublimation system.

Both the structural and electrical properties of SOS have been shown to depend heavily on substrate preparation. Although various chemical polishing techniques are available in the literature\(^{48}\), they often involve strong etching solutions like the hot \(\text{H}_3\text{PO}_4 + \text{H}_2\text{SO}_4\), or \(\text{V}_2\text{O}_5\) at high temperatures, and they do not often give a satisfactory surface polish. Filby\(^{49}\) claimed that silicon in a silane and \(\text{H}_2\) atmosphere can be used to polish (1102) alumina at a substrate temperature of 1380°C. It is now believed that heating sapphire or spinel in a \(\text{H}_2\) ambient to a temperature 100-200°C above that used for epitaxial film growth will remove the work-damaged monolayer resulting from the mechanical polish\(^ {50,21}\) and produce a smooth and featureless substrate surface.

In this investigation, \(\text{H}_2\) prefiring of sapphire and spinel substrates for 15 minutes at a temperature as low as 950°C was found sufficient for single-crystalline growth of silicon at ~800°C. This was done inside a vertical quartz chamber (shown schematically in fig. 2.3) using a Philips PH1012/16 RF generator operated at 1 MHz. Prior to \(\text{H}_2\) prefiring, the as-received mechanically polished substrates were given a standard chemical rinse. They were then heated in a \(\text{H}_2\) ambient to 950°C for 15 minutes over the RF-heated carbon susceptor. Temperature was monitored by a chromel-alumel thermocouple sheathed inside the 1/4" dia. quartz tube which also supported the carbon susceptor. Standard grade \(\text{H}_2\) was made to pass through a dehydrated \(\text{CuSO}_4\) column before use. Its flow rate of 30ml/min. was monitored by a RGI flowmeter. Positive pressure inside the quartz cylinder was maintained by venting \(\text{H}_2\) through a flask containing \(\text{H}_2\text{O}\). After prefiring, the substrate temperature was lowered to 300°C in 1 minute and the substrate was allowed to cool by it-
self in the $H_2$ atmosphere before direct insertion into the vacuum chamber for deposition of silicon.

![Diagram of the H$_2$-prefiring apparatus]

Fig. 2.3 A schematic diagram of the $H_2$-prefiring apparatus.

2.2.3 Sublimation Procedure

The experiment was conducted using source temperatures in the range between 1300 and 1400°C, and substrate temperatures between 750-850°C. Various deposition rates were obtained by using different substrate-source separations, and source and substrate temperatures. A typical run was as follows:

1. After a vacuum of $5 \times 10^{-8}$ torr had been attained, the substrate heater lamp was turned on to about 70% of the variac voltage (110-V maximum) which gradually heated the substrate up to about 500°C. At this time, the substrate was located laterally at 2" from the
filament. The background pressure had now risen to $9 \times 10^{-8}$ torr; and it would stay at this level until the end of sublimation.

(2) 15-20V was tapped from the autotransformer to feed the silicon filament in series with the carbon resistor (at ~5Ω). Electrical current in the silicon filament was then gradually increased by adjusting the conductance of the carbon resistor down to about its minimum of 0.05Ω. This was done at a rate which would give a temperature rise of ~100°C per 15 sec. to the filament. The final source temperature would be around 100°C below that required for deposition of silicon films.

(3) In about 5 minutes, the left-most portion of the substrate holder was rotated to directly above the filament. This brought the substrate to within a lateral displacement of only 1" away from the edge of the source and yet, it was cut off from the main stream of the silicon vapour by the Ta shutter right underneath it (fig. 2.2). Temperature of the source was readjusted to that which would be used for deposition, and that of the substrate was raised to about 50°C higher than that used for film growth.

(4) After 15 minutes, a steady deposition rate was assumed to have established as well as a homogeneously silicon-vapour-filled ambient around the filament. Sublimation of silicon on to the substrate began when the latter was rotated to directly above the silicon source. Substrate temperature was co-ordinated simultaneously during substrate introduction by adjusting the electric power supplied to the heater lamp.

(5) Upon completion of film deposition, the substrate was quickly retracted out of the chamber; its temperature was then lowered at
a rate of 200°C per minute down to 300°C, whence the film would be annealed in vacuum for 1/2-hour.

Fig. 2.4 Silicon films on sapphire and spinel substrates; the film at the left was deposited through a quartz mask bearing a geometry for the Van der Pauw Hall and conductivity measurements.

2.3 Methods of Film Assessments

Since the structural properties of grown films affect their electrical properties, and since their electrical properties will determine the characteristics of any passive or active devices fabricated using them, an insight into both these properties is therefore essential for practical uses of thin-film materials. These interests will be taken up in detail for the sublimed silicon films grown at low substrate temperatures in chapter 3. The following section is to give a brief account of the criteria for semiconductor film assessments and to outline the measuring techniques used in this investigation.

2.3.1 Deposition Rate and Film Thickness Measurements

Average deposition rate for each run could be determined by measuring the film thickness and the deposition time. They varied from a maximum of 1μ/10min down to about 0.25μ/hr. As mentioned above (section 2.2.3), the growth rate was controlled by the temperatures of the source and substrate as well as their separation. The grown silicon-
films were between 1-4µ thick on Czochralski (0001), 60°, (1102) sapphire and (001), (111)) spinel substrates*. Their thicknesses were measured on a Sloan Angstrometer using a Na light source (λ=5890 Å). Accuracy of the Fizeau fringe displacement across the film-substrate step was estimated to be within ±150 Å.

2.3.2 Structural Properties

Eventhough no existing theory satisfactorily explains and predicts the epitaxial relation between a condensate and the substrate, it is believed that qualitatively the phenomenon of epitaxy is based on the nucleation of initially oriented critical nuclei, or the growth of a dominant orientation resulting from the coalescence of the variously oriented critical nuclei. Direct observation of nucleation and growth of thin-films can be done by depositing films directly inside the electron microscope or, to a lesser extent, by replica electron microscopy. Study of surface morphology of the grown films by optical microscopy and electron microprobe technique will supply information as to the nature of film growth -- to see whether they are of the three dimensional growth or layer growth type. The ideal case, of course, is a mirror-smooth, featureless surface finish. A metallurgical microscope of Union Bi-2395 series and a Hitachi JX3-3A electron microprobe analyser were used to observe the surface topography of the grown films. Further, crystal structure identifications were done by reflection-electron-diffraction (RED) using a Hitachi HU-11B electron microscope at a camera constant of 2.3198 A-cm, and by back-reflection Laue-diffraction on a X-ray machine using a molybdenum tube at 4.5 KV and 15A for 1/2 hr.

* Supplied by Union Carbide of Canada Ltd., Downsview, Ontario.
2.3.3 Electrical Properties

Single crystal semiconductor film is required for the best performance of active devices fabricated on it\textsuperscript{53}. In addition, for the purpose of reproducibility, a uniform thickness with smooth surface finish and a homogeneous distribution of impurity concentration across the surface of the grown film is desirable.

In this study, the majority carrier concentration type was identified by the standard thermal probe technique. Conductivity and Hall mobility were measured using the Van der Pauw geometry\textsuperscript{54}; such an

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**Fig. 2.5** Block diagram of the Hall apparatus.

For Hall voltage measurement, set switch-connections: D-1, B-2, A-3, and C-4.

For Van der Pauw conductivity measurement, set switch-connections: A-1, B-2, C-3, D-4, and set P2=0; repeat with: A-2, D-1, B-3, C-4, and set P2=0.
apparatus had already been described in detail elsewhere. The measuring circuit was given in fig. 2.5 and is a modified version of that designed by Fischer et al. Three Keithley model-602 electrometers were used as current meter and null detectors. Noise level of the Hall voltage is typically of the order of 0.05 mv, and the accuracy of the current and voltage measurements was at ± 5% of the electrometers' full scale readings. The magnetic field was supplied by an Alpha 8500 electromagnet powered by an Alpha P8500 power supply. A typical field strength of 0.42 weber m⁻² was used.
3.1 Introduction

The feasibility of epitaxial growth on a single-crystal foreign substrate is dependent on:

(1) the amount of lattice misfit between the substrate and the epitaxial deposit — but small misfit is neither a necessary nor sufficient condition for the occurrence of epitaxy,

(2) the degree of surface mobility of adatoms during the processes of nucleation, coalescence, and continuous film growth,

(3) the magnitude of the deposition rate at any given substrate temperature, and

(4) contamination of the ambient as well as the perfection of substrate surface.

The present work was conducted at the lower limit of the epitaxial temperature range and was not intended to determine the establishment of an optimal epitaxial growth condition. Weisberg et al. pointed out that their results for films grown below 900°C were erratic and irreproducible. The object of this chapter, then, is to look at such irregularities, and to explain the structural and electrical properties of these low-temperature-grown single-crystalline silicon thin-films. Further, since the growth parameters 2-4 listed above would critically influence an epitaxial growth under the present condition, any significant result introduced here would have to be derived from a large number of similar runs. We shall, therefore, only be interested in the general features of film growth at such a temperature rather than concentrating...
on their individual specifications.

Although no particular attempt was made to establish the lowest substrate temperature for epitaxial silicon growth on sapphire and spinel substrates, single-crystalline silicon films of 1µ and less were in fact obtained at substrate temperatures as low as 750°C.

3.2 Structural Properties

3.2.1 Surface Morphology

The majority of films grown at substrate temperatures near 800°C had a dull, metallic-grey surface finish, independent of the deposition rate in the range from 0.1µ/min down to 0.25µ/hr. A typical photomicrograph of such a film is shown in fig. 3.1.a. The irregular surface-feature could be easily identified as the grain boundaries.

Fig. 3.2.a shows an electron-probe topograph of a 2.1µ thick film grown at 800°C on (1102) sapphire at a rate of 4µ/hr from a boron-doped source (at 5 x 10^{18} \text{ cm}^{-3}). The measured Hall mobility of such a film was over 50% of bulk silicon with the same carrier concentration, and its resistivity was about 35% higher than that of the source. It had a mirror surface-finish and appeared slightly reddish when viewed at an angle. Under x1000 magnification, its surface feature resembled the epitaxial films grown by the pyrolysis of silane at 1050-1100°C. However, it is interesting to note that such a surface feature does not look too different from that observed on a poly-crystalline film grown under similar substrate temperature without the use of the H_2 prefiring treatment (fig. 3.2b).

The effect of extremely fast deposition rate (flash evaporation) was also studied. An initial thin layer of silicon, estimated at about 3000Å thick, was grown on a 60° sapphire at a rate of 2µ/hr at 780°C
Fig. 3.1 Photomicrographs of silicon films on sapphire and spinel substrates (a, b, and c), and (d) of silicon filament after 5 hours of sublimation at \(\sim 1400^\circ C\).
Fig. 3.2 Electron-probe topographs of silicon films on sapphire & spinel.
substrate temperature. This was followed by forcing an anomalous electric current through the silicon filament, thereby, creating instantaneously a large flux of high temperature silicon vapour. The source necked and burnt off in roughly 2 seconds. The film thus obtained was very shiny and appeared to have a continuous surface layer (fig. 5.2.c) despite heavy mechanical scratches on the sapphire surface, which are known to be good locations for generating pits and steps in normal film growth. Single crystalline Laue and electron-diffraction patterns were obtained from such a film, but the film's resistivity (\(-10^{5}\) \(\Omega\)-cm) was so high that electrical measurement was almost impossible. Its extremely high defect density was observed by Sirtl et al. etching it for 15 minutes.

3.2.2 Growth Mechanism

It is generally believed that film growth usually begins with the generation of three-dimensional nuclei. According to Ehrlich et al., each adatom has a finite lifetime before it re-evaporates; and there exists a critical size of a crystal nucleus above which it becomes energetically stable and takes up adatoms with the release of the heat of condensation. The maximum number of nuclei formed depends on the adsorption sites, impurities and imperfections, electrostatic charges present on the substrate surface, and the substrate temperature. The growth of a nucleus takes place partly by the capture of adatoms that diffuse across the substrate surface and strike its periphery, and partly by the capture of adatoms that land directly upon it. The stable nuclei grow to form islands and eventually coalesce resulting in a network structure which subsequently fills up to obtain a continuous film.

In the process of coalescence, the islands become elongated in the direction of preferred film growth and are separated by long, irregular, and narrow channels like those found in fig. 3.1.b. In fact, the photomicrograph of fig. 3.1.b reveals some of the major stages of epitaxial film growth (film is at the left-handed side) on a chemically polished (111) silicon substrate. These are: island formation (nucleation stage is somewhat obscured in this picture), coalescence, channel stage and continuous film growth. Observation of this 'wide' film-substrate interface was made possible by creating a narrow spacing between the surfaces of the substrate and a thin quartz mask at the time of deposition. The fact that such a liquid-like coalescence was not observed in SOS qualitatively supports the argument of poorer surface mobility of deposit atoms over the substrate surfaces in hetero-epitaxy vs homoepitaxy.

Yasudu et al. discovered that 4 preferred orientations were present in the initial stage (-100Å) of growth of Si on (0001) sapphire. This is analogous to the LEED observations of a mixed Si (111)-7 and Si (111)-5 structure developed during the initial growth stage of homoepitaxial silicon by Thomas et al. In addition, a mixed (110), (001) Si was observed in very thin films grown on (1102) sapphire by hydrogen reduction of silane. Similar electron diffraction patterns were also obtained from samples of the low-temperature-sublimed Si films on (0001) sapphire at film thicknesses of up to 1-2μ (fig. 3.3.a).

With increasing film thicknesses, Yasudu et al. observed changes in the structure of their films with the final orientation of (111)Si//(0001)Al2O3. This change in orientations can be interpreted as: (i) an improvement in the alignment of nuclei and islands as growth proceeds, and (ii) preferential growth of nuclei and islands of one preferred orientation at the expense of nuclei and islands of other preferred orientat-
Fig. 3.3 Reflection electron diffraction patterns of sublimed silicon films.
Fig. 3.4 X-ray Laue reflection diffraction patterns of silicon films on
(a) (0001) sapphire, (b) 60° sapphire substrates.
ions. For films grown at low substrate temperatures (as in our experiments), the reduction in free energy of the islands by coalescing differently oriented nuclei or islands to form one preferred orientation is often severely impeded by low surface mobility of the adatoms, resulting in a lack of recrystallization to form a single-crystalline structure.

3.2.3 Lattice Imperfections in Grown Films

The common structural defects in semiconductor films are stacking faults, twins, dislocations, and point-defect aggregations*. Accommodation of lattice misfit between substrate and overgrown film would be shared between interface dislocations and elastic strains in the film. Extended misfit dislocations occur primarily during the channel and hole stage of growth. In addition, the coalescence of differently oriented nuclei is thought to give rise to twins. The lack of adequate surface diffusivity of the deposits at low substrate temperatures impair plastic flow of adatoms between adjacent islands. As a result, many small holes are generated at these boundaries, initiating dislocation loops, and other defects.

Other mechanisms for the formation of lattice imperfections include:

1. propagation of substrate imperfections yielding an anomalous film growth around the substrate defects (fig. 3.1.c),
2. production of stacking faults due to surface contaminations of the substrates by impurities.

Further, with SOS, Heiman discovered that aluminum autodoping at the film/substrate interface had created a strongly ionizable 'glossy' layer which generated an inversion layer next to it in the silicon overgrowth.

* See for example section 8.4 in ref. 68.
One often finds a high degree of lattice imperfections in hetero-epitaxy because of (a) lattice mismatch between the nuclei of the deposit and the substrate, (b) difference in expansion coefficients of the two materials, and (c) chemical changes, as in the reaction of silicon with sapphire.

Fig. 3.5 Optical micrograph of an etched silicon film after 15 minutes in Sirtl etch. (magnification x400)

Fig. 3.5 shows the optical micrograph of an etched silicon film, which was optically flat before etching, formed on a spinel (111) surface after 15 minutes in Sirtl etch. A high number of 'holes' or pits were observed on the etched surface characterizing the imperfect coalescence and annihilation of grain boundaries during film growth. The familiar triangular etched pattern which is due to stacking faults on (111) silicon surface was not observed here. These, together with the irregular surface feature of fig. 3.1.a suggests that the initial,
3-dimensional nucleation and growth pattern of the low-temperature-sublimed silicon films persists even after the formation of a continuous film. Subsequently, we conclude that the poor electrical properties (see section 3.3) obtained from most of these films were essentially due to their high defect densities generated at the grain boundaries.

3.2.4 Additional Factors that May Influence the Structure of Sublimed Silicon Films

Layer or step growth pattern, similar to those identified by Abbink et al. and others in epitaxial silicon, was also observed in a 2.5μ thick polycrystalline film on 60° sapphire substrate grown at 740°C and at 3μ/hr deposition rate (fig. 3.2.d). Film continuity was pinned down at defect sites (pits), which had irregular crater shapes and cross-sectional areas but roughly the same depth. From the shadow of the dust particle casted on to the film, we can estimate their depths to be in the order of 5000 Å thick. It therefore seems logical to assume that such defects had been formed before a continuous layer deposit, and that they were originated from surface contaminations of the substrates by impurities.

Kikuchi lines in RED patterns, indicating a high angular perfection in the films, were obtained from Si on (001) and (111) spinel substrates. This is in contrary to the RED patterns obtained from films on sapphire (fig. 3.3.b), thus conceding that films having smaller lattice misfit with their substrates normally have better crystal structures.

Very often, when the substrate after film deposition was not withdrawn fast enough from the sublimation compartment, the silicon vapour would condense on the cooler surface of the retreating film resulting in a very thin layer of polycrystalline overgrowth (fig. 3.3.c). This indicates that the substrate temperature (~750°C) used in this
experiment was close to the temperature limit for epitaxial film growth.

Despite the fact that it was extremely difficult to attain high quality epitaxial silicon films grown at low temperatures, Kikuchi bands in RED similar to that of fig. 3.3.d demonstrated that it was not impossible to grow structurally good epitaxial films at low substrate temperatures using the in-situ sublimiation technique.

3.3 Electrical Properties

3.3.1 General

Table 3.1 shows a sample of the low-temperature-sublimed silicon films on sapphire and spinel substrates. The effective carrier concentration \( \bar{n} \) given in the last column were derived from measured resistivity \( \rho \) and Hall mobility \( u_H \) according to the formula \( \bar{n} = 1/(e\rho u_H) \). A few of their characteristics which were summed up from measurements taken from 50 or more film samples are as follows:

(1) With silicon sources of high doping concentration (\(-5 \times 10^{18} \text{ cm}^{-3}\)), the effective carrier concentration in the deposit films were, at the most, an order or so in magnitude lower than the doping concentrations of the source. However, as source impurity concentrations were reduced to that below \(10^{18} \text{ cm}^{-3}\), the films were invariably found to have higher resistivity and much lower effective carrier concentration (often 2-3 orders in magnitude) than their source materials. We are to postpone the discussion of this phenomenal observation until after we have considered the trapping model proposed in section 3.3.3.

* In fact, the drift mobility is the primary quantity of interest. It is related to Hall mobility by a factor of \((3/8)\pi\) which is found theoretically for acoustic-mode scattering and other types of scatterings in which the mean free path is independent of velocity\(^72\).
Table 3.1

<table>
<thead>
<tr>
<th>Film</th>
<th>Source Doping Conc. (cm⁻³)</th>
<th>Substrate Temperature</th>
<th>Substrate Type</th>
<th>Film Type</th>
<th>Film Thickness</th>
<th>Resistivity (Ω·cm)</th>
<th>Hall Mobility (cm²/V·sec)</th>
<th>Carrier Conc. (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q3</td>
<td>p-5x10¹⁸</td>
<td>820°C</td>
<td>(1002)</td>
<td>p</td>
<td>2.2μ</td>
<td>0.025</td>
<td>86</td>
<td>3x10¹⁸</td>
</tr>
<tr>
<td>M1</td>
<td></td>
<td>&quot;</td>
<td>(100)</td>
<td>p</td>
<td>4μ</td>
<td>0.069</td>
<td>26</td>
<td>3.4x10¹⁸</td>
</tr>
<tr>
<td>Q2</td>
<td></td>
<td>800°C</td>
<td>(111)</td>
<td>p</td>
<td>1.5μ</td>
<td>0.545</td>
<td>12.5</td>
<td>9x10¹⁷</td>
</tr>
<tr>
<td>Q1</td>
<td></td>
<td>820°C</td>
<td>(100)</td>
<td>p</td>
<td>1.7μ</td>
<td>0.46</td>
<td>15.5</td>
<td>8.8x10¹⁷</td>
</tr>
<tr>
<td>Q16</td>
<td></td>
<td>&quot; initially at 780°C, after 5min. used 820°C</td>
<td>(0001)</td>
<td>p</td>
<td>0.9μ</td>
<td>1.2</td>
<td>6.2</td>
<td>8.4x10¹⁷</td>
</tr>
<tr>
<td>SEC-2</td>
<td></td>
<td>780°C</td>
<td>on etched (100)</td>
<td>p</td>
<td>0.6μ</td>
<td>12.7</td>
<td>21.3</td>
<td>2.3x10¹⁶</td>
</tr>
<tr>
<td>Y14</td>
<td></td>
<td>790°C</td>
<td>(100) 60°</td>
<td>p</td>
<td>1.3μ</td>
<td>1.5</td>
<td>7.9</td>
<td>5.3x10¹⁷</td>
</tr>
<tr>
<td>X10</td>
<td>p-3x10¹⁵</td>
<td>790°C</td>
<td>&quot;</td>
<td>p</td>
<td>1.5μ</td>
<td>1.8x10⁴</td>
<td>59</td>
<td>5.8x10¹³</td>
</tr>
<tr>
<td>B12</td>
<td>n-6x10¹⁶</td>
<td>750°C</td>
<td>&quot;</td>
<td>n</td>
<td>1.7μ</td>
<td>230</td>
<td>21</td>
<td>1.3x10¹⁵</td>
</tr>
<tr>
<td>PRI-14</td>
<td></td>
<td>770°C</td>
<td>&quot;</td>
<td>n</td>
<td>2.3μ</td>
<td>295</td>
<td>28</td>
<td>7.6x10¹⁴</td>
</tr>
<tr>
<td>PLA01</td>
<td>'0'-free p-10¹⁶</td>
<td>800°C</td>
<td>&quot;</td>
<td>p</td>
<td>0.9μ</td>
<td>4.6x10⁴</td>
<td>39</td>
<td>3.5x10¹³</td>
</tr>
</tbody>
</table>
Varying the film thicknesses between 1-2µ did not appreciably affect the electrical properties of the deposit films. But, as their thicknesses were increased to more than 2-3 µ, a slight increase in Hall mobility, and a decrease in resistivity were observed, reflecting an improved crystal structure in the thicker films.

Low oxygen content had been found by Weisberg and others to give rise to better structural and electrical properties of grown films. But with the in-situ sublimation apparatus, no apparent improvement in the quality of films grown from the \(10^{15} - 10^{17} \text{ cm}^{-3}\) 'O'-free sources was observed. This may mean that the effect of oxygen inclusion in the films has been diminished by other growth parameters at low substrate temperatures.

The effect of aluminum and magnesium autodoping from the substrates, which is observed to predominate in all high-temperature-grown silicon films (by CVD as well as by vacuum deposition), was kept to a minimum. This made possible the growth of n-type films on sapphire at film thicknesses of less than 2µ and at a source doping level of \(-10^{16} \text{ cm}^{-3}\).

The crystallographic relations between films and substrates were:

- (001) silicon // 60° or (1\(\bar{1}\)02) sapphire
- (111) silicon // 0° or (0001) sapphire
- (001) silicon // (001) spinel
- (111) silicon // (111) spinel

* Supplied by Union Carbide of Canada Limited, Downsview, Ontario.
3.3.2 Temperature Dependence of Resistivity, Hall Mobility and Effective Carrier Concentration

Fig. 3.6 to fig. 3.8 show the variation of resistivity, Hall mobility and effective carrier concentration with temperature for 3 representative samples. Sample A represented a film with 'good' structural and electrical properties, samples B and C represented the majority of films grown from high and low doping silicon sources respectively.

For sample A, the variations of \( \rho \) and \( \mu_H \) are relatively small within the given temperature range. The observation of a maximum in Hall mobility agrees with that found by others. At low temperature, defect scattering predominates, and at high temperature, the decrease in \( \mu_H \) is caused by Coulombic scatterings due to ionized impurities. The variation of resistivity vs. temperature in this sample is also consistent with the electrical properties of heavily doped silicon studied by Chapman et al.

A marked exponential dependence of \( \rho \) and \( n \) with reciprocal temperature was observed for samples B and C. This is similar to the experimental results on silicon and other semiconductor thin-films grown by other investigators. Qualitatively, one can attribute the relatively rapid decrease, as compared to bulk silicon, of effective carrier concentration with decreasing temperature to the interaction of impurities with the defect structures. A quantitative model is given in the following section.

3.3.3 Trapping Model for Semiconductor Films with Defect Centers Locating at the Grain Boundaries.

The presence of crystalline defects acting as electron traps was demonstrated by Dumin et al. from measurement of the electron concentration in films of constant donor density but varying dislocation
Fig. 3.6 Film resistivity versus temperature.
Fig. 3.7 Hall mobility versus temperature.
Fig. 3.8 Effective carrier concentration versus temperature.
density. They noticed that $\bar{n}$ decreases as the defect density increases. Analysis of data taken from both p-type and n-type films indicates that the Fermi-level is pinned down by deep levels. These levels may occur at the grain boundaries, at the silicon-substrate interface, or they may be uniformly distributed in the film. From optical absorption and photoconductivity measurements, these donor and acceptor type traps appear to occur in approximately equal density, with density as high as $10^{17}$-10$^{18}$ cm$^{-3}$ being deduced. Deep levels due to dislocations in bulk silicon have been reported as well by Glaenzer et al. The general theory, therefore, is that these acceptor and donor type traps are caused primarily by the dangling silicon bonds at grain boundaries and distorted lattice in the neighbourhood of these grain boundaries; and, they may also be associated with precipitates.

Optical conductivity measurements were taken on a few of the low-temperature sublimed silicon films using a Bausch and Lomb monochromator in the 0.7 - 1.5$\mu$ range. The result showed qualitatively a gradual increase in photoconductivity of the samples with increasing incident photon energy, similar to that observed by Heiman. The following trapping model is based on 2 well-established experimental observations discussed above:

- a) Fermi-level is trapped deep inside the forbidden gap by ionized impurity centers,
- b) the majority of defects are located at the grain boundaries and, when ionized, they will cause band bending.

Let us assume that for an n-type semiconductor the surface density of traps caused by defects at the grain boundaries is $N_t$, with a capture cross-section $\sigma_n$ and a characteristic ionization energy level $E_t$ measured from the conduction band edge. If the surface density of filled traps is $n_t$ and the average electron velocity is $\bar{v}_n$, the rate
at which electrons combine with traps will be \( \bar{\gamma} n (N - n_t) \bar{n} / (l_1 + l_2) \),
where \( \bar{n} \) is the average density of free electrons in the inhomogeneous film, and \( (l_1 + l_2) \) is the average grain size. The interaction of trapping centers with crystal lattice releases electrons at the rate \( \bar{\gamma} n n_t n_2 / (l_1 + l_2) \), where \( n_2 \) is the density of electrons in the conduction band when the Fermi-level is at the trap level. The difference in these rates gives the net rate of change of trapped electrons \( \delta n_t / \delta t \),

\[
\frac{\delta n_t}{\delta t} = \bar{\gamma} n (N - n_t) \frac{\bar{n}}{(l_1 + l_2)^2} - \bar{\gamma} n n_t \frac{n_2}{1 + l_2} \quad (3.1)
\]

At equilibrium, the rate of change of trapped electrons has to be zero.

\[
\therefore \: \bar{n} (N_t - n_t) = n_t n_2 . \quad (3.2)
\]

Next, we consider the one-dimensional inhomogeneous film model of fig. 3.9. Here, we assume that the majority of the trapping centers are located at the grain boundaries. From the requirement of charge neutrality, a space charge region of opposite polarity to that of the ionized traps is generated. Its width of \( l_2 \) is related to the number

---

**Fig. 3.9** A one-dimensional in-homogeneous film model.
of trapped carriers at the grain boundaries by

\[ n_t = n_l \frac{1}{2} \quad , \quad (3.3) \]

where \( n_l \) is the doping level and is approximately equal to the free electron concentration in the neutral region.

Now, the number of free electrons at the top of the space charge barrier with respect to \( n_l \) is

\[ n_2 = n_l \exp - \frac{(E_C - E_F) - E_t}{kT} \quad , \quad \text{and} \quad (3.4) \]

according to the depletion approximation, the barrier height \( \phi = (E_C - E_F) - E_t \) may be written as

\[ (E_C - E_F) - E_t = \frac{e^2 n_l}{2e^*} \left( \frac{1}{2} \right)^2, \quad (3.5) \]

where \( e \) is the electronic charge, and \( e^* \) is the permittivity of the semiconductor. Using the values of \( n_l \), (3.3), and \( \phi \), (3.5), we obtain \( \bar{n} \) in terms of \( n_2 \) as

\[ \bar{n} = \frac{n_t}{N - n_t} \quad n_l \quad \exp - \left( \frac{e n_t^2}{8\pi k T n_l} \right) \quad . \quad (3.6) \]

The negative exponential dependence of \( \bar{n} \) on temperature as derived in (3.6) is consistent with both our experimental results and those of the others discussed in section 3.3.2. By assuming that \( n_l \) and \( n_t \) are both constant with temperature, and that \( n_l \) is approximately equal to the source impurity concentration, we obtain the values of \( n_t \) and \( N_t \) as \( 8 \times 10^{11} \text{cm}^{-2} \) and \( 1 \times 10^{12} \text{cm}^{-2} \) for sample B and \( 2 \times 10^{11} \text{cm}^{-2} \) and \( 3 \times 10^{12} \text{cm}^{-2} \) for sample C. From these results we conclude that the density of defects \( N_t \) is relatively insensitive to the source doping concentration \( (5 \times 10^{18} \text{cm}^{-3} \) for sample B vs. \( 6 \times 10^{16} \text{cm}^{-3} \) for sample C). The immediate implication is that the impurity segregation at the grain boundaries does not play a major role in defect generation, and that the apparently
poorer film quality at lower carrier concentrations may be attributed to impurity compensation by ionizable structural defects.

In fact, (3.6) tells us more than just the negative exponential dependence of $\bar{n}$ on $T$, it also confirms and explains the puzzling experimental observation that the effective carrier concentration deviated more from the actual impurity concentration of the source when the latter was at a lower doping level than at a higher doping level.* If we assume that $n_t$ varies slowly with different source doping level, then the exponential factor in (3.6) will be close to unity for large values of $n_1$, and $\bar{n}$ will differ from $n_1$ by a factor of $n_t/(N_t-n_t)$, which is not too much smaller than unity. Similarly, with low source doping level, and therefore $n_1$, the exponential factor will be much smaller than unity, and the measured value of $\bar{n}$ will deviate more from that of $n_1$.

To obtain a similar temperature-dependent expression for film resistivity, we proceed as follows:

In a stationary field, the current density $J$ within the inhomogeneous film should be the same for the neutral regions and at the grain boundaries.

From Ohm's law

$$J = \sigma_1 E_1 = \sigma_2 E_2,$$

(3.7)

where $\sigma_1$, $\sigma_2$ and the corresponding values of $E_1$, $E_2$ are respectively the conductivities and electric fields for the neutral regions, and at the grain boundaries.

But according to our inhomogeneous film model

* It is a reasonable assumption, since the function $N_t$ should have a stronger dependence on the growth parameters rather than on the segregation of impurities at the grain boundaries: the experimentally derived values of $n_t$ and $N_t$ confirm this statement.
\[ E_2 - E_1 = \frac{en_1}{2e} l_2, \]  

(3.8)

Combining (3.7) and (3.8), and using (3.3) for the value of \( l_2 \), we have

\[ E_1 = \frac{\sigma_2}{(\sigma_1 - \sigma_2)} \frac{en_t}{2e}. \]  

(3.9)

But, we can also express (3.7) in terms of the carriers' mean velocities \((v_1, v_2, \bar{v})\) as

\[ J = n_1 ev_1 = n_2 ev_2 = \bar{n} e \bar{v}. \]  

(3.10)

Using conservation of energy expression

\[ \frac{1}{2} m_e v_1^2 = \frac{1}{2} m_e v_2^2 - |e\phi|, \]

where \( m_e \) is the effective mass of the free electrons in the conduction band, we obtain the carrier's mean velocity, averaged over the neutral region and the grain boundaries, as

\[ \bar{v} = \frac{|e\phi|}{\frac{1}{2} m_e \bar{n}^2 \left( \frac{1}{n_2} - \frac{1}{n_1} \right)}. \]  

(3.11)

Further, (3.7) and (3.10) allow us to write

\[ E_1 = \frac{1}{\bar{n}} \bar{n} e \bar{v}. \]  

(3.12)

Substituting the value of \( \bar{v} \) from (3.11) into (3.12) and equating the value of \( E_1 \) in (3.9) and (3.12), we have, after some algebraic simplification,

\[ \rho_2 = \rho_1 + \frac{m e n_1}{2 e \bar{n}} \left( \frac{1}{n_2^2} - \frac{1}{n_1^2} \right), \]  

(3.13)

where \( \rho_1 \) and \( \rho_2 \) are respectively the resistivities for the neutral region and at the grain boundaries.

For \( n_2 \ll n_1 \),
\[ \rho_2 = \rho_1 + \frac{m}{n \varepsilon} \exp \left( \frac{e^2 n t^2}{8ckTn} \right) \]  

Equation (3.14) is in agreement with Volger's assertion that the grain boundary is a region having higher resistivity than that inside the grain. Using his qualitative result of the observed resistivity \( \bar{\rho} = \rho_1 + \rho_2 \frac{l_2}{l_1} \) we obtain an expression for \( \bar{\rho} \) which has an exponential temperature dependence similar to the one observed in the experiment. In addition, we can now understand why the measured film resistivity \( \bar{\rho} \) at low source carrier concentration \( n_1 \) is so much higher than that of \( \rho_1 \).

3.3.4 Effect of Post-oxidation on the Electrical Properties of Low-Temperature-Sublimed Silicon Films

For practical device application, it is essential that electrical properties of any semiconductor thin-film should not change appreciably during the thermal oxidation used in device processing. Post-firing of silicon in oxygen has been reported to remove acceptor-type impurities from the wafer and to push donor-type impurities back into the wafer; with silicon-on-sapphire and silicon-on-spinel, it is observed to remove aluminum impurity created by substrate auto-doping during silicon film growth. This is attributed to the high diffusivity of aluminum in silicon and for its tendency to segregate in the growing silicon oxide. However, appreciable electrical changes could also result from such a process. Ross et al. imputed the mobility degradation in the silicon films to the introduction of scattering centers by the precipitation of neutral aluminum-oxygen complexes.

In this experiment, thermal oxidation of silicon films was conducted inside a horizontal quartz tube (the detailed set-up will be
given in section 6.2.4) at 1050°C for 15 minutes in steam. The samples were subsequently annealed at 350°C in N₂ atmosphere for \( \frac{1}{2} \) hr. before they were taken out of the reaction chamber. The oxide films were removed using 49% HF and then rinsed in boiling distilled water. Ohmic contacts were applied, and the van der Pauw geometry was again used for both the conductivity and Hall mobility measurements. A few of the results are given in table 3.2.

Comparing the conductivity and Hall mobility measurements on the silicon films before and after thermal oxidation revealed only very minor changes in electrical properties of the low-temperature sublimed silicon films. This suggests that aluminum autodoping, which is commonly found in films grown at higher substrate temperatures and which may often cause a reduction in carrier concentration up to an order or so in magnitude after thermal oxidation, has been kept to a negligible amount by using low substrate temperatures for film growth.

<table>
<thead>
<tr>
<th>Film</th>
<th>Thermal Treatment</th>
<th>Substrate Type</th>
<th>Resistivity (Ω-cm)</th>
<th>Hall Mobility (cm²/V-sec)</th>
<th>Effective carrier Conc. (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q3</td>
<td>as-deposited oxidized</td>
<td>(1102)</td>
<td>0.025 0.026</td>
<td>86 83</td>
<td>3.1 x 10^{18} 3.1 x 10^{18}</td>
</tr>
<tr>
<td>KII</td>
<td>as-deposited oxidized</td>
<td>(111)</td>
<td>0.65 0.69</td>
<td>20.5 19.8</td>
<td>4.7 x 10^{17} 4.5 x 10^{17}</td>
</tr>
<tr>
<td>PRI-14</td>
<td>as-deposited oxidized</td>
<td>60°</td>
<td>295 302</td>
<td>28 22</td>
<td>7.6 x 10^{14} 9.3 x 10^{14}</td>
</tr>
<tr>
<td>X10</td>
<td>as-deposited oxidized</td>
<td>60°</td>
<td>1.8x10⁴ 2.5x10⁴</td>
<td>59 38</td>
<td>5.8 x 10^{13} 9 x 10^{13}</td>
</tr>
</tbody>
</table>

† See also figs. 3.6-3.8 for the variations of \( \rho, \mu, \) and \( \bar{n} \) on temperature for the sample KII after thermal oxidation.
CHAPTER 4
A Thin-Film U R C Structure

4.1 Introduction

A thin-film URC (uniformly distributed RC) structure normally consists of a dielectric layer sandwiched between a resistive layer and a highly conducting metal layer, all of which are deposited on an insulating substrate (fig. 4.1).

The resistive thin-film can be made of (a) an alloy, e.g. nichrome, (b) a single metal, e.g. tantalum or chromium, (c) a cermet, e.g. Cr-SiO, or (d) a semiconductor. The method of preparation can be: vacuum deposition, electroless plating, hydrolysis or pyrolysis, etc.

The most commonly used dielectric films are tantalum pentoxide, aluminum oxide, and silicon oxide. Deposition methods include thermal, anodic or plasma oxidation, reactive or RF sputtering, vacuum evaporation, chemical decomposition, and polymerization.

The substrate can be, for example, glass, alumina, quartz, or spinel. However, if a semiconductor is chosen for the resistive component, the selection of substrate becomes crucial if epitaxial semiconductor is needed: polycrystalline semiconductors have resistivities of the order of $10^5$-$10^6 \ \Omega \cdot \text{cm}$ and are hence not ideal for use in URC devices.

It is the purpose of this chapter to study the influence of semiconductor-insulator junction properties on a thin-film URC structure. To comply with useful solid state device dimensions, we shall from now on assume that the epitaxial semiconductor has a thickness of no more than 2-3μ, and no less than 1000Å. In particular, we shall use the n-type silicon and the thermally grown SiO₂ for our illustrations.
Fig. 4.1 A schematic diagram of a thin-film URC structure:—
(a) physical structure indicating (i) ohmic contacts (S-source, D-drain), (ii) semiconductor channel, (iii) dielectric layer, (iv) highly conducting metal layer (gate), and (v) insulating substrate; (b) electrical symbol of a URC structure.

Fig. 4.2 Energy band diagrams of an MIS structure (n-type semiconductor) showing different modes of operations: (a) the flat-band case, (b) accumulation mode, and (c) deep-depletion into the inversion mode.
4.2 Review of MIS Theory

4.2.1 Ideal C-V Characteristics of MIS Structures

For a metal-insulator-semiconductor (MIS) system, in which the metal and the semiconductor work functions are equal and there are no surface states at the semiconductor-insulator interface, the energy-band diagrams (n-type semiconductor) are as depicted in fig. 4.2.

When the gate is made positive relative to the n-type semiconductor, electrons from the bulk semiconductor are attracted to form an accumulation layer underneath the insulator-semiconductor interface. The small signal ac capacitance measured across this structure will be $C_i$, the intrinsic insulator capacitor. However, if the applied voltage $V_g$ is negative, electrons will be repelled away from the same interface and, a space charge region consisting of ionized donor impurities will develop. The growth of this space charge layer gives rise to an increasing depletion layer capacitance $C_d$ in series with $C_i$. Upon further decrease in biasing potential to a value such that the semiconductor surface potential $\psi_s$ at the interface is numerically equal to, or greater than, twice the Fermi-potential $\psi_F$, the semiconductor surface is said to be inverted and a very thin layer of positive charges begins to effectively shield the depletion region from any further increase in electric field. The measured small signal capacitance $C_t$ for large negative values in $V_g$ will approach that of $C_i$. But, for high frequency signals, such that the minority carriers in transition across the depletion layer are short in following the signal, the shielding effect disappears and $C_t$ will level off at the minimum value of $C_i$ in series with $C_d$.

4.2.2 MIS Structure Including Traps and Surface States

In a real MIS system, surface states together with impurity
and oxide traps play an important role in determining the actual semiconductor surface potential at the semiconductor-insulator interface. A few of the well established facts which are required for our analysis of a semiconductor URC structure are listed below:

(1) The amount and distributions of surface states and oxide traps are determined primarily by the method of oxide preparation, the lattice orientation of the semiconductor, the contaminants introduced during oxide growth, and the annealing treatments of the oxidized structure.

(2) The interface states in the oxide lie very close to the semiconductor-insulator interface and can in most practical cases be regarded as residing at the interface.

(3) For a carefully prepared sample, charges that are trapped at the interface are almost independent of the biasing voltage. This allows one to determine the amount of surface states at the interface (mainly the interface-trap density) by calculating from the flat-band voltage shift in the C-V characteristic.

4.3 Channel Conductance of Semiconductor Thin-Films After Thermal Oxidation

It is well known that redistribution of impurities at the surfaces of semiconductors will take place in the process of thermal oxide growth\(^{83,11}\). The doping profile underneath the interface of a thermally growth oxide had been shown to follow the normal diffusion theory\(^{83}\). In this section we shall look at the effect of thermal oxidation on the channel conductance of a semiconductor thin-film resistor.

Let us assume that a homogeneous n-channel semiconductor thin-film resistor has after thermal oxidation a thickness \(a\), width \(L\),
and length $L$. The redistribution of impurities causes a change in Fermi-potential $\psi_F$ from the surface down to a depth of $x' \leq a^*$. The change in channel conductance of the resistor can be calculated as follows:

The channel conductance

$$ g = \frac{Z}{L} \int_0^a \sigma(x) \, dx $$

$$ = \frac{Z}{L} \int_0^a q \mu_n \frac{\mu_p}{\mu_n} [p(x) + n(x)] \, dx, \quad (4.1) $$

where $\mu_n$, $\mu_p$ are the effective carrier mobilities for electrons and holes with densities of $p(x)$ and $n(x)$ respectively.

Now,

$$ n(x) = n_i \exp(-u_F - u) $$

$$ p(x) = n_i \exp(u_F - u), \quad (4.2) $$

where $n_i$ is the intrinsic carrier concentration and $u = \beta \psi$ is the electrostatic potential in $kT/e$ units.

So,

$$ g = \frac{Z}{L} \int_0^a q \mu_n n_i \frac{\mu_p}{\mu_n} \exp(u_F - u) + \exp(-(u_F - u)) \, dx, \quad (4.3) $$

We can separate the last integral into two parts, one containing the surface region, and the other the homogeneous underneath layer with constant $u_F$. Further, if we introduce a change in variable in the first integral from $dx$ to $1/(du/dx)$ with

$$ \frac{du}{dx} = \sqrt{\mathcal{L}} \left[ u \sinh u_F + \cosh (u_F - u) - \cosh u_F \right]^{1/2}, \quad (4.4) $$

in which $\mathcal{L} = \left( \frac{\epsilon_s}{2\beta q n_i} \right)^{1/2}$ is the intrinsic Debye length (see Appendix A),

we get,

---

* The redistributed region is limited to $4\sqrt{Dt}$ from the interface, with $D$ denoting the diffusion constant of the impurity, and $t$ the time of oxidation.
\[ g = \frac{Z}{L} \int_{u_s}^{u_F} n \left[ \frac{\mu_p}{\mu_n} \exp (u_F - u) + \exp -(u_F - u) \right] du \]

\[ + \frac{Z}{L} \int_{x'}^{a} q u \left[ \frac{\mu_p}{\mu_n} n \exp (u_F) + n \exp -(u_F) \right] dx \]  \hspace{1cm} (4.5)

The distance \( x' \) can be determined from (4.4) as

\[ x' = \int_{u_s}^{u_F} \frac{L \, du}{\sqrt{2} \left[ u \sinh u_F + \cosh (u_F - u) - \cosh u_F \right]^{1/2}} \]  \hspace{1cm} (4.6)

At room temperature, \( \exp (-u_F) \gg \frac{\mu_p}{\mu_n} \exp (u_F) \),

Hence, \[ \frac{g}{g_o} = \int_{u_s}^{u_F} \frac{\left[ \mu_p/\mu_n \exp (2u_F - u) + \exp (u) \right] du}{a^{1/2} \sqrt{2} \left[ u \sinh u_F + \cosh (u_F - u) - \cosh u_F \right]^{1/2}} + \frac{a - x'}{a} \]  \hspace{1cm} (4.7)

where \( g_o = Z \sigma a L \), is the conductance of an equivalent semiconductor thin-film resistor having a uniform electrical conductivity \( \sigma \) and the same physical dimensions as the one considered above.

Knowing what the bulk doping concentration \( N_B \) is for the semiconductor, which is almost the same as the homogeneous impurity concentration of an unoxidized sample, we can find the doping profile in the film either experimentally or, by calculations based on the conditions of thermal oxidation. Then numerical evaluation of (4.6) and (4.7) will give the change in channel conductance as required.

The above derivation has assumed that ohmic contacts to the semiconductor exist at the 2 ends of the resistive element, so that both holes and electrons can be the effective charge carriers. This assump-

* By convention \( u_F \) is negative for n-type semiconductor.
tion is to be taken for all other similar analyses contained in this chapter.

4.4 DC Channel Conductance of Semiconductor Thin-Films in a MIS Structure

4.4.1 Channel Conductance with $V_{DS} = 0$

For an epitaxial semiconductor grown on an insulating substrate, the substrate-semiconductor interface results in an extra complication to the simple MIS structure. However, for most of the practical thin-film devices, the field effect is normally confined to a region close to the oxide-semiconductor interface so that the space charge effect generated at the film-substrate interface can often be neglected in the first order approximation of analysis. We shall now look at the variation of channel conductance in a MIS structure as a result of varying the surface potential by an external biasing voltage. The effect of impurity redistribution after the oxide growth is neglected. Further, we are to include only the interface states in this analysis.

(1) Depletion Mode

We shall consider in this section the case in which the source and drain regions have the same potential with respect to the gate.

In static equilibrium,

$$V_G = V_o + \psi_s + \psi_{MS}$$  \hspace{1cm} (4.8)

$$Q_G = -Q_s - Q_{SS}$$  \hspace{1cm} (4.9)

where $V_o$ is the potential across the oxide,

---

+ A factor of 10 in the ratio of surface to bulk impurity concentration will affect the surface potential by less than one tenth of an e.v. at room temperature.
\( \psi_s \) is the semiconductor potential at the interface,
\( \psi_{MS} \) is the metal semiconductor work function difference,
\( Q_G, Q_s \) and \( Q_{ss} \) are respectively the charges on the metal gate, in the depletion region, and those in the interface states.

Using the depletion layer approximation, and assuming no free charge carriers in the depleted region, we have

\[ Q_s = -q N_D x_d. \]

where \( q \) is the electronic charge
\( N_D \) is the donor density in the semiconductor
\( x_d \) is the depletion layer width measured with respect to the oxide-semiconductor interface.

Now, the electric field \( E_s \) at the interface is given by (fig. 4.2c)

\[ E_s = -\frac{d\psi}{dx} \bigg|_{x=0^+} = -q N_D x_d / \varepsilon_s \]

so that,

\[ \psi = -\frac{q N_D}{2 \varepsilon_s} x_d^2 = \frac{Q_s}{C_0} + V_G - \psi_{MS} + \frac{Q_{ss}}{C_0}, \]

since,
\( Q_G = V_o C_0 \).

Equation (4.11) can be reduced to an ideal MIS case when we replace \( V'_G \) for \( (V_G - \psi_{MS} + Q_{ss}/C_0) \) as the equivalent gate potential. From continuity of the displacement vector \( \nabla \)

\[ \varepsilon_s \frac{\partial \psi}{\partial x} \bigg|_{x=0^+} = \varepsilon_I \frac{\partial \psi}{\partial x} \bigg|_{x=0^-} \]

where \( \varepsilon_s \) and \( \varepsilon_I \) are the dielectric permittivities of the semiconductor and the insulator respectively.
Substituting (4.10) into (4.12) gives
\[ \varepsilon_s q N_D x_d = \varepsilon_i \frac{V'_G - \psi}{-x_o}, \] (4.13)

and using the value of \( \psi \) from (4.11), we obtain the depletion layer width \( x_d \) as
\[ x_d = \frac{\varepsilon_s}{\varepsilon_i} x_o + \sqrt{\frac{\varepsilon_s}{\varepsilon_i} x_o^2 - \frac{2\varepsilon_s}{qN_D} V'_G}. \] (4.14)

The channel conductance can then be calculated from
\[ g = g_o (1 - x_d/a) \] (4.15)

where \( g_o = \sigma Z a/L = Z q \mu_n N_D a/L. \)

(2) Accumulation and Inversion Modes

In either the inversion or the accumulation mode of operation, part of the carriers responsible for conduction are confined to a region very close to the interface. For enhancement mode, we can find the enhanced conductance as follows:

Total charge/area in the enhanced layer is
\[ Q = -C V'_G = -\frac{\varepsilon_i}{x_o} V'_G. \] (4.16)

This charge distribution can be represented by containing it in a uniform layer of thickness \( \lambda \) and density \( n_s \), so that
\[ Q = -n_s \lambda q. \] (4.17)

Then the enhanced conductance is
\[ g' = n_s q \mu_n \lambda \frac{Z}{L} \]
\[ = \frac{\varepsilon_i \mu_n V'_G Z}{(x_o L)}; \] (4.18)

and the enhancement-mode channel conductance is given by
\[ \frac{g}{g_o} = 1 + g'/g_o \]
\[ = 1 + \frac{\varepsilon_i V'_G}{aq N_D x_o} \] (4.19)
However, potential \( V'_C \) cannot be increased indefinitely, because the electric field at avalanche breakdown is about \( 5 \times 10^5 \) V/cm for Si.

Another method for calculating surface conduction is to account for it in terms of surface potentials. To do this, we find the number of holes or electrons per unit area in the accumulation or inversion region resulting from a finite surface potential. The inversion charges in an n-type semiconductor are:

\[
Q_{\text{inv}} = q \int_{0}^{u_s} p(x) \, dx.
\]

So the change in channel conductance is

\[
\Delta g_h = q n_1 \frac{Z}{L} \int_{u_s}^{u_F} \mu_p^* \frac{\exp (u_F - u)}{\frac{du}{dx}} \, du,
\]

where \( \mu_p^* \) is the effective hole mobility in the inversion layer. The final expression for \( g \) is obtained by combining \( \Delta g_h \) with that value of \( g \) in (4.15) at maximum depletion layer width \( x_{d\text{max}} \) (see Appendix A for \( x_{d\text{max}} \)),

i.e.

\[
g_{\text{inv}} = g(x_d = x_{d\text{max}}) + \Delta g_h.
\]

For operation in accumulation mode, the enhanced conductance is due to an accumulation of majority carrier (electrons) at the semiconductor surface, so that

\[
\Delta n = n_1 \left[ \exp - (u_F - u) - \exp -u_F \right].
\]

Hence,

\[
\Delta g_e = q n_1 \frac{Z}{L} \int_{u_s}^{u_F} \mu_n^* \frac{\exp - u_F (\exp u - 1)}{\frac{d}{dx}} \, dn,
\]

where \( \mu_n^* \) is the electron surface mobility.

The actual channel conductance is therefore given by

\[
g_{\text{Acc}} = g_0 + \Delta g_e.
\]
4.4.2 Channel Conductance with $V_{DS} \neq 0$

In section 4.4.1, we have seen how the interface states and the metal-semiconductor contact potential difference can be taken care of by simply replacing the actual gate potential $V_G$ with its equivalence of $V'_G$. Henceforth, we shall only consider the electrical behavior of a semiconductor channel having an ideal C-V characteristic.

Fig. 4.3 A URC structure with $V_D \neq V_S$.

A URC differential subregion is defined by:

$$y_1 < y < y_2, \quad y = y_2 - y_1 \text{ small}$$

$$x_0 < x < a$$

$$0 < z < Z$$

With $V_{DS} \neq 0$ and $V_G > 0$, the second derivative of the channel potential $W(y)$ at distance $y$ from the source region is not identically equal to zero at the space charge boundary; here we have written $W(y)$ in place of $-(V_{GS} - V(y))$. However, if $\frac{\partial^2 W}{\partial y^2}$ is small compared to $qN_D/\varepsilon_s$, the one-dimensional approximation can be applied, and $W(y)$ can be related to the space charge width by the same relation as in the
case of $V_{DS} = 0$. Further, if the electric field $E_x$ varies much slower than $E_y$ at the space charge boundary with $y$, Shockley's gradual channel approximation can also be used.

The DC conduction current at $y$ is given by

$$I_D(y) = \int_{x_d}^{a} J_D(x,y) \, dx$$

$$= -Z \mu_n \int_{x_d}^{a} \frac{dV(y)}{dy} N(x) \, dx$$

Assuming constant doping profile all through the depth of the film, we integrate $I_D(y)$ from $y = 0$ to $y = L$,

$$I_D = -q n N_D L \int_0^{V_D} (a-x_d) \, dV$$

Now, the space charge width is as given in (4.14)

$$x_d(y) = -\frac{\varepsilon_s}{\varepsilon_I} x_o + \sqrt{\left(\frac{\varepsilon_s}{\varepsilon_I} x_o\right)^2 + \frac{2\varepsilon_s}{q N_D} W(y)}$$

$$= 1 + \frac{\varepsilon_s}{\varepsilon_I} \frac{x_o}{a} + \frac{2}{3a} \frac{q N_D}{2\varepsilon_s} V_D \left\{ \left(\frac{\varepsilon_s}{\varepsilon_I} x_o\right)^2 - \frac{2\varepsilon_s}{q N_D} V_G \right\}^{\frac{3}{2}}$$

$$= \left[ 1 + \frac{2\varepsilon_s}{q N_D} \frac{V_D}{\left(\frac{\varepsilon_s}{\varepsilon_I} x_o\right)^2 - \frac{2\varepsilon_s}{q N_D} V_G} \right]^{\frac{3}{2}}$$

where $I_o = -\mu_n q N_D V_D a Z L$.

If $V_D \leq V_G$, we can make use of the binomial expansion for the term in square brackets, and arrive at

$$\frac{I_D}{I_o} = 1 + \left(\frac{\varepsilon_s}{\varepsilon_I a} \right) - x_G - \frac{1}{4} \left(\frac{2\varepsilon_s}{q N_D a^2} \right) x_G^2 + \frac{1}{24} \left(\frac{2\varepsilon_s}{q N_D a^2} \right)^2 x_G^3$$

(4.29b)
\[ \varepsilon/\varepsilon_0 = 11.7, \quad \varepsilon/\varepsilon_0 = 3.9 \]

\[ a = 2 \times 10^{-4} \text{ cm.} \]

\[ X_0 = 1 \times 10^{-5} \text{ cm.} \]

For n-type Si, with \( V_S = 0 \).

Fig. 4.4.a Theoretical channel conductance of a Si-URC structure as a function of \( V_D \).
\[ \epsilon_s/\epsilon_0 = 11.7, \quad \epsilon_r/\epsilon_0 = 3.9; \]
\[ a = 2 \times 10^{-4} \text{ cm}; \]
\[ x_0 = 1 \times 10^{-5} \text{ cm}. \]

Fig. 4.4.b Theoretical channel conductance as function of the gate potential \( V_g \).
where \( x_G = \frac{\varepsilon_s x_o}{\varepsilon_I a} - \frac{2\varepsilon_s V_G}{qN_D a^2} \).

(4.31)

It can easily be shown* that the ratio of \( I_D/I_o \) is identically the same as \( g(V_D,V_G)/g_o(V_D,0) \), where \( g_o(V_D,0) \) is the channel conductance under the flat band condition.

### 4.4.3 Small Signal Parameters for Thin-Film MIS Structure

For a given channel potential, the channel conductance is given by (4.15)

\[
g(W) = \frac{Z q\mu_n N_D a/L (1 - x_d(W)/a)}{1 - qN_D a/L}.
\]

(4.32)

so we can rewrite (4.27) as

\[
I_D = -\int_{W_{GS}}^{W_{GD}} g(W) \, dW.
\]

(4.33)

From our definition of \( W(y) = -(V_{GS} - V(y)) \)

\[
\frac{\partial W_{GD}}{\partial V_{DS}} = -1, \quad \frac{\partial W_{GD}}{\partial V_{DS}} = 0.
\]

(4.34)

The small signal source-drain conductance \( g_{ds} \) defined by

\[
g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \bigg|_{V_{GS}} = \frac{\partial I_D}{\partial W_{GD}} \bigg|_{V_{GS}}
\]

(4.35)

is

\[
g_{ds} = g(W_{GD})
\]

\[
= g_o \left( 1 + \frac{\varepsilon_s x_o}{\varepsilon_I a} - \sqrt{\frac{(\varepsilon_s x_o/a)^2 + \frac{2\varepsilon_s}{qN_D a^2} W_{GD}}} \right).
\]

(4.36)

Similarly, we find the small signal transconductance \( g_m \) of the channel as

* \( g(V_D,V_G) = I_{DS}/V_{DS} = -I_D/V_D \). In the flat-band case \( g_o(V_D,0) = Zq\mu_n N_D a/L = -I_o/V_D \); so \( g(V_D,V_G)/g_o = I_D/I_o \).
4.4.4 Distribution of Channel Potential and the Shape of Space Charge Width Along the Channel

To find the distribution of potential along the channel, we use the expression

\[ \frac{V}{L} = \frac{\int_{W_{GS}}^{W_x} g(W) \, dW}{\int_{W_{GS}}^{W_{GD}} g(W) \, dW} \quad (4.39) \]

This will give us the ratio of \( y/L \) for a given \( W_{GS} \leq W_x \leq W_{GD} \).

To find the channel profile we first find \( \frac{dx_d}{dy} \) as

\[ \frac{dx_d}{dy} = \frac{\varepsilon_s}{qN_D} \left( \frac{1}{\varepsilon_1} - \frac{1}{\varepsilon_s} x_0 \right) \left( x_d + \frac{\varepsilon_s}{\varepsilon_1} x_0 \right) \quad (4.40) \]

then substitute \( dW/dy \) into (4.26), assuming constant doping profile all through the semiconductor film, we have

\[ I_D(y) = -Zq N_D \frac{dx_d}{dy} \frac{qN_D}{\varepsilon_s} \left( x_d + \frac{\varepsilon_s}{\varepsilon_1} x_0 \right) (a - x_d) \quad (4.41) \]

Integrating the above equation from \( y = 0 \) to \( y \), whence \( x_d = x_{ds} \) and \( x_d \) respectively, we find the ratio

\[ \frac{V}{L} = \frac{I_o}{I_D} \frac{1}{V_D} \frac{qN_D}{\varepsilon_s} \left[ x_0 \frac{\varepsilon_s}{\varepsilon_1} (x_d - x_{ds}) + \frac{1}{2} \left( 1 - \frac{\varepsilon_s x_0}{\varepsilon_1 a} \right) (x_d^2 - x_{ds}^2) - \frac{1}{3a} (x_d^3 - x_{ds}^3) \right] \quad (4.42) \]
$X_0 = 1 \times 10^{-5} \text{cm}$, $\alpha = 2 \times 10^{-4} \text{cm}$.

---

$N_D = 1 \times 10^{15}$

$N_D = 1 \times 10^{17}$

Space-charge width at the source:

$x_s/x_{d_{\text{max}}} : C_1 = 0.5$

$C_2 = 0.1$

---

Fig. 4.5.a Distribution of channel potentials in Si-URC structure.
$X_0 = 1. \times 10^{-5}\, \text{cm.} \quad ; \quad \alpha = 2. \times 10^{-4}\, \text{cm.}$

---

$N_D = 1. \times 10^{15}$

$N_D = 1. \times 10^7$

Space-charge width at the source:

$x_s/x_{d_{\text{max}}} : C_1 = 0.5$

$C_2 = 0.1$

---

Fig. 4.5.b Channel profile in a Si-URC structure.
where the value of $I_o$ is as given by (4.29b). From (4.42) we can compute $y/L$ for given values of $V_D$, $W_{GD}$ and $x_d(y)$.

4.5 AC Small Signal Modelling of Thin-Film URC Structure

4.5.1 Equation of State

Our present task is to come up with a small signal model which will facilitate the use of semiconductor distributed RC element as an electric circuit component.

The basic postulates used in the following analysis are:

1. The RC distributed structure is assumed to have a uniform cross-section of width $Z$, a semiconductor layer of thickness $a$, and an oxide layer thickness $x_o$.
2. The terminal contacts to the semiconductor are ohmic.
3. For a n-type semiconductor, the number of mobile charge carrier cm$^{-3}$ is taken identically equal to $N_D$, the doping concentration of the film.
4. The conducting channel in the semiconductor is assumed to have an equi-potential surface perpendicular to the direction of flow of charge carriers, and that the conducting current in the channel has only a $y$-component.
5. The quasi-static approximation valid at all points and at all time is to be assumed, so that $E(x,y,t) = \nabla \psi(x,y,t)$.
6. The dielectric material is assumed to be polarized uniformly and that it contains no free volume charge. In other words, the dielectric is lossless, and that the current density in it is zero.
7. We assume that $E_x$ is independent of $x$ in the dielectric, so that $E_x = E_x(y,t)$. 
Finally, for easy mathematical manipulation, we assume that any net charges within the semiconductor appear as interface states at the insulator-semiconductor junction.

We start by taking a differential subregion of the device defined by (fig. 4.3)

\[ y_1 \leq y \leq y_2, \quad y = y_2 - y_1 \text{ is small} \]
\[-x_o \leq x \leq a \]
\[ 0 \leq z \leq Z \]; and we assume that a space charge layer of depth 'd' exists. The electric current density enters and leaves the enclosed surfaces of the semiconductor subregion only at \( y_1 \) and \( y_2 \). Thus we can write

\[
\frac{dq}{dt} = \oint_S j \cdot n \, dS
\]  
(4.43)

\[
= Z \int_0^a j_y (x,y_1,t) \, dx - Z \int_0^a j_y (x,y_2,t) \, dx
\]  
(4.44)

\[
= i_1(t) - i_2(t).
\]  
(4.45)

Since the dielectric is assumed to be uniform, its volume charge density due to polarization is zero. Thus the charge density introduced by \( i_1 - i_2 \) is made to confine within the space charge region only, and

\[
\frac{dq}{dt} = \frac{\partial}{\partial t} \int_V \rho(x,y,t) \, dV
\]

\[
= Z \frac{\partial}{\partial t} \int_{y_1}^{y_2} \int_0^d (t) \rho(x,y,t) \, dx \, dy.
\]  
(4.46)

Now, (4.44) can be written as

\[
\frac{dq}{dt} = Z \int_0^a \left( \sigma(x,y_1) \frac{\partial v}{\partial y} (x,y_1,t) - \sigma(x,y_2) \frac{\partial v}{\partial y} (x,y_2,t) \right) \, dx
\]  
(4.47)

which is also equal to.
\[
Z \int_{0}^{d_2(t)} \sigma(x,y_2) \frac{\partial}{\partial y} [u(y_2,t) + w(x,y_2,t)] \, dx + Z \int_{d_2(t)}^{a} \sigma(x,y_2) \, dx = \\
\frac{\partial}{\partial y} [u(y_2,t) + w(x_2,y_2,t)] - Z \int_{0}^{d_1(t)} \sigma(x,y_1) \frac{\partial}{\partial y} [u(y_1,t) + w(x,y_1,t)] \, dx - \\
w(x,y_1,t) \, dx - Z \int_{d_1(t)}^{a} \sigma(x,y_1) \, dx \frac{\partial}{\partial y} [u(y_1,t) + w(x,y_1,t)] \] (4.48)

where the potentials \( u, v, w \) are as defined in fig. 4.3.

If the steady state space charge width is approximately uniform within the subregion, we can assume \( d_1(t) = d_2(t) = d(y,t) \). With the help of the following integration by parts relationship

\[
\int_{y_1}^{y_2} \frac{\partial^2 \psi}{\partial y^2}(x,y,t) \sigma(x,y) \, dy = \frac{\partial \psi}{\partial y}(x,y,t) \sigma(x,y) \bigg|_{y_1}^{y_2} - \\
\int_{y_1}^{y_2} \frac{\partial \sigma}{\partial y} \frac{\partial \psi}{\partial y} \, dy \] (4.49)

we can rewrite (4.48), which after equating to (4.46) will give

\[
\int_{0}^{d} \frac{\partial \rho}{\partial t}(x,y,t) \, dx = \int_{0}^{d} \left\{ \frac{\partial^2 (u+w)}{\partial y^2} \sigma(x,y) + \frac{\partial \sigma}{\partial y} \frac{\partial (u+w)}{\partial y} \right\} \, dx + \\
\int_{d}^{a} \left\{ \frac{\partial^2 (u+w')}{\partial y^2} \sigma(x,y) + \frac{\partial \sigma}{\partial y} \frac{\partial (u+w')}{\partial y} \right\} \, dx , \] (4.50)

where \( w' = w(d,y,t) \).

So the equation of state becomes

\[
\int_{0}^{d} \left\{ \frac{\partial \rho}{\partial t}(x,y,t) - \frac{\partial^2}{\partial y^2}(u+w) \sigma(x) - \frac{\partial \sigma}{\partial y} \frac{\partial (u+w)}{\partial y} \right\} \, dx = \\
\int_{d}^{a} \left\{ \frac{\partial^2 (u+w')}{\partial y^2} \sigma(x) + \frac{\partial \sigma}{\partial y} \frac{\partial (u+w')}{\partial y} \right\} \, dx \] (4.51)
For a semiconductor film deposited uniformly on to the substrate

\[ \sigma(x,y) = \sigma(x); \]

equation (4.51) can then be reduced to

\[
\int_0^d \frac{\partial}{\partial t} \rho(x,y,t) - \frac{\partial^2(u+w)}{\partial y^2} \sigma(x) \, dx
\]

\[ = \int_0^a \frac{\partial^2(u+w')}{\partial y^2} \sigma(x) \, dx, \quad (4.52) \]

for any subregion at distance y from the source.

Before going any further, it is demonstrative for us to see how the above result can be applied to a familiar case -- a distributed RC structure using metal resistors. Whence, \( w = 0, d \to 0, \) and \( \sigma(x) \) is a constant for all regions inside the film. In addition, the space charge layer is often so thin that it can be neglected; so that

\[
\int_0^d \frac{\partial \rho}{\partial t} \, dt = \int_0^d \frac{\partial \rho_s(x,y,t)}{\partial t} \delta(x) \, dx = \frac{\partial}{\partial t} \rho_s(0, y, t)
\]

and

\[
\int_0^a \sigma(x) \, dx = \sigma a
\]

Therefore, (4.52) is reduced to

\[
\frac{\partial^2 \rho_s(y,t)}{\partial t} = \frac{\partial^2 u(y,t)}{\partial y^2}. \quad (4.53)
\]

Replacing

\[
\frac{u(y,t)}{x_o} = \left. \frac{\partial u}{\partial x} \right|_{x=0} \quad \text{for} \quad \frac{\rho_s(y,t)}{\varepsilon_o}
\]

the familiar lossless transmission line equation follows

\[
\Delta c \Delta t \frac{\partial u(y,t)}{\partial t} = \frac{\partial^2 u(y,t)}{\partial y^2} \quad (4.54)
\]
where
\[ \Delta r = \frac{1}{\sigma z a} \]  \hspace{1cm} (4.55)
and
\[ \Delta c = \frac{\varepsilon Z}{x_0} \]  \hspace{1cm} (4.56)

4.5.2 Simplifying the Equation of State

The integral \( \int_0^d \frac{3 \rho(x,y,t)}{\partial t} \, dx \) in (4.52) actually represents the rate of change of total surface charge density in the space-charge layer, as well as in the interface states. It should numerically be equal to the rate of change of surface charge density \( Q_s \) on the metal gate since we had asserted no volume charge density inside the oxide by our postulate no. 6. Further, if we adopt the definition

\[ dQ_s = C_t \, d(u+w) \]  \hspace{1cm} (4.57)

where \( C_t \) is the capacitance per unit area of the insulator and the space-charge layer in series, equation (4.52) can be simplified to

\[
\int_0^d \frac{3 \rho(x,y,t)}{\partial t} \, dx = C_t \frac{3}{\partial t} (u+w) \\
= \int_d^a \frac{3}{\partial y^2} (u+w) \, \sigma(x) \, dx + \int_0^d \frac{3}{\partial y^2} (u+w) \, \sigma(x) \, dx \]  \hspace{1cm} (4.58)

From the depletion layer approximation, the conductivity in the space-charge region is practically zero,

\[
\int_0^d \frac{3}{\partial y^2} (u+w) \, \sigma(x) \, dx \ll \int_d^a \frac{3}{\partial y^2} (u+w') \, \sigma(x) \, dx \]  \hspace{1cm} (4.59)

Further, if we assume that \( \sigma(x) \) is a constant between \( d \leq x \leq a \) we arrive at the Kirchhoff's differential equation for the subregion \( y_1 \leq y \leq y_2 \),

\[ C_t \frac{dW}{dt} = \frac{3}{\partial y^2} \sigma(d-a) \]
\[ C_t(y) \frac{d\theta(y)}{dt} = \frac{\partial^2 \theta(y)}{\partial y^2} \]  

(4.60)

where \( r(y) = \frac{1}{\sigma} \frac{1}{(a-d)} \) is the resistance per unit length of the channel.

An equivalent circuit for the subregion can be derived from (4.60) and is depicted as in fig. 4.6.

For channels having different depletion layer thicknesses along the length of the device, we can obtain the differential equation for such a structure in much the same way as if we were treating a non-uniform transmission line case. The model in fig. 4.6 allows us to write in the phasor space

\[ \frac{dV(s,y)}{dy} = - \frac{1}{G(y)} I(s,y) \]  

(4.61)

\[ \frac{dI(s,y)}{dy} = - s C_t(y) V(s,y) \]  

(4.62)

Combining (4.61) and (4.62), we obtain

\[ \frac{d^2 V(y)}{dy^2} + \frac{d\ln G(y)}{dy} \frac{dV}{dy} (s,y) - s \frac{C_t(y)}{G(y)} V(s,y) = 0, \]  

(4.63)

which is the Riccati nonlinear differential equation. An analytical solution to (4.63) can only be obtained for a few exceptional cases.\(^{102}\)
In the next section, however, we shall use the conventional junction gate FET small signal model to arrive at a small signal equivalent circuit for the URC structure having a non-uniform depletion layer thickness.

4.6 Small Signal Analysis of a Generalized URC Structure

4.6.1 Small Signal Equations

We are to start from the equivalent circuit of a URC subregion (fig. 4.6).

From Ohm's law

\[ \frac{\Delta W(y,t)}{\Delta y} G(W) = -I(y,t), \]  

and from the continuity equation

\[ \Delta I(y,t) = -\frac{\partial}{\partial t} Q(W) \Delta y . \]  

The channel to gate potential \( \tilde{W} \) as well as the channel current \( \tilde{I} \) can be expressed as superposition of both dc and ac components

\[ \tilde{W}(y,t) = W'(y) + w(y,t) \]  

\[ \tilde{I}(y,t) = I'(y) + i(y,t) \]  

Expanding \( Q(W) \) and \( G(W) \) by Taylor's method, and neglecting all the second and higher order terms, we have in the limit as \( \Delta y \to 0 \)

\[ \left[ \frac{\partial W'(y)}{\partial y} + \frac{\partial w(y,t)}{\partial y} \right] G(W) + \frac{\partial G(W)}{\partial \tilde{W}} \bigg|_{\tilde{W}=W'} = -I(y) - i(y,t) \]  

\[ \left[ \frac{\partial I'(y)}{\partial y} + \frac{\partial i(y,t)}{\partial y} \right] = -\frac{\partial}{\partial t} \left[ Q(W') + \frac{\partial Q(W)}{\partial \tilde{W}} \bigg|_{\tilde{W}=W'} \right] . \]  

* One method of analyzing a non-uniform structure is by considering it as an infinite cascade of uniform structures.
Recognizing that
\[ \frac{\partial W'(y)}{\partial y} = -\frac{I'(y)}{G(W')} \tag{4.69} \]
\[ \frac{\partial I'}{\partial y} = 0, \quad \frac{\partial}{\partial t} Q(W') = 0 \]
and that for small ac signals, the capacitance \( C_t(W') \) is only a function of the dc component \( W' \)
\[ C_t(W') = \frac{dQ(W)}{dW} \bigg|_{W=W'(y)} \tag{4.70} \]
we simplify (4.67) and (4.68) to
\[ \frac{\partial W}{\partial y} = -\frac{I'}{G(W')} - \frac{W}{G(W')} \frac{dW}{dy} \frac{dG(W)}{dW} \bigg|_{W=W'} \tag{4.71} \]
and
\[ \frac{\partial I}{\partial y} = -C_t(W') \frac{\partial W}{\partial t} \tag{4.72} \]
This last set of partial differential equation is replaced in Laplace's transform by two ordinary differential equations. With zero initial conditions
\[ \frac{dW(s,y)}{dy} G(W') + \frac{dW}{dy} \frac{dG(W)}{dW} \bigg|_{W=W'} W(s,y) = -I(s,y) \tag{4.73} \]
and
\[ \frac{dI(s,y)}{dy} = -sC_t(W') W(s,y) \tag{4.74} \]

4.6.2 Solutions of the Small Signal Equations

We are to use the depletion approximation, and the notation
\[ b(W') = [1 - x_d(W')/a] \]
for the normalized channel thickness.
The dc conduction current is
\[ I_d = I' = G(W') \frac{dW}{dy} = g_0 b(W') \frac{dW}{dy} \tag{4.75} \]
The capacitance \( C_t \) as defined in (4.70) can be written as
\[ C_t(W') = ZqN_D \frac{db(N')}{dW'} \tag{4.76} \]
Making the approximation
\[
\frac{\text{db}(W)}{\text{dW}} \bigg|_{W=W'} = \frac{\text{db}(W')}{\text{dW}} = \frac{\text{db}(W')}{\text{dW}} \quad (4.77)
\]

(4.73) and (4.74) can be written as
\[
\frac{\text{dW}'}{\text{dy}} \left\{ \frac{\text{dW}}{\text{db}(W')} \right\} \varepsilon_0 \text{b}(W') + \varepsilon_0 \text{W}' = -I \quad (4.78)
\]
\[
\frac{\text{dW}'}{\text{dy}} \frac{\text{db}(W')}{\text{dy}} = s\varepsilon N a \frac{\text{db}(W')}{\text{dW'}} W' \quad (4.79)
\]
Differentiating (4.78) with respect to \( b(W') \),
\[
\frac{d^2I}{db^2} = s\varepsilon N a \frac{d}{\text{db}(W')} (W \frac{dy}{dy}) ;
\]
and substituting the value of \( \frac{dW'}{dy} \) from (4.75) and \( -I \frac{dy}{db} \) from (4.78),
we obtain
\[
\frac{d^2I}{db^2} = k^2 l b (1 - b + \frac{\varepsilon x_0}{\varepsilon I a}) \quad (4.80)
\]
where \( k^2 = -\frac{\varepsilon s}{\varepsilon s} \left( \frac{q N a^2 Z}{I D} \right)^2 \).
Solutions for (4.81) can be obtained by using the generalized power series
\[
I(b) = \sum_{n=0}^{\infty} A_n b^{p+n} \quad (4.83)
\]
Substituting the value of \( I \) and its second derivative into (4.71), putting \( n=0 \) and at the same time demanding that \( A_0 \) is not equal to zero, we arrive at the indicial equation
\[
p (p - 1) = 0 \quad (4.84)
\]
The roots are \( p = 0, \) or \( p = 1 \).
(4.85)
The choice of \( p = 1 \) does not yield an independent solution to (4.81), and is discarded. So, the final solution for (4.81) is
\[
I(b) = A_0 T(k,b) + A_1 R(k,b) \quad (4.86)
\]
where \( A_0, A_1 \) are arbitrary constants.
\[
T(k,b) = \left[ 1 - \frac{k^2}{3.2} (1 + \frac{\varepsilon x_0}{\varepsilon I a}) b^3 + \frac{k^2 b^4}{4.3} \\
\right]
+ \frac{k^2}{6.5.3.2} (1 + \frac{\varepsilon x_0}{\varepsilon I a}) b^6 - \frac{k^4}{7.6} (1 + \frac{\varepsilon x_0}{\varepsilon I a}) (\frac{1}{4.3} + \frac{1}{3.2}) b^7
\]
\[
R(k,b) = \left[ b - \frac{k^2}{4.3} \left( 1 + \frac{\epsilon S_X}{\epsilon I_a} \right) b^4 + \frac{k^2 b^5}{5.4} \right.
+ \frac{k^4}{7.6.4.3} \left( 1 + \frac{\epsilon S_X}{\epsilon I_a} \right) b^7 - \frac{k^4}{8.7} \left( 1 + \frac{\epsilon S_X}{\epsilon I_a} \right) \left( \frac{1}{5.4} + \frac{1}{4.3} \right) b^8
+ \frac{k^4 b^9}{9.8.5.4} + o(k^5) \quad \ldots \ldots \right] \quad (4.87)
\]

Very often, we are interested in the channel voltage instead of the current, which can be obtained by differentiating (4.86) with respect to \( b \) and substituting the result into (4.81) to get

\[
W(b) = -\frac{I_D}{S q N_D \sigma^2 a^2 b} \left( A_{3T} \partial a \partial b + A_{3R} \partial b \right) \quad (4.89)
\]

4.6.3 Common-Gate Admittance Matrix

We are now ready to represent the generalized URC structure by an equivalent 2-port network. The short circuit \( y \)-parameters in the common-gate configuration are:

\[
y_{11} = \left. \frac{i_s}{V_{sg}} \right|_{V_{sg}=0}, \quad y_{12} = \left. \frac{i_s}{V_{dg}} \right|_{V_{sg}=0}, \quad y_{21} = \left. \frac{i_d}{V_{sg}} \right|_{V_{dg}=0}, \quad y_{22} = \left. \frac{i_d}{V_{dg}} \right|_{V_{sg}=0} \quad (4.90)
\]

To evaluate \( y_{11} \) and \( y_{21} \), we use the boundary conditions:

1. \( W=V_{sg} \) and \( b=b_s \) at the source,
2. \( W=0 \) and \( b=b_d \) at the drain.

Similarly, for \( y_{12} \) and \( y_{22} \), the boundary conditions are:

1. \( W=V_{dg} \) and \( b=b_d \) at the drain,
2. \( W=0 \) and \( b=b_s \) at the source.

* The value of \( I_D \) can be evaluated from (4.75) as

\[
\int_0^L I_D dy = \int_b^d \left( \frac{\alpha a^3 q N_D}{\epsilon s} \right) b \left( 1 - b + \frac{\epsilon S_X}{\epsilon I_a} \right) db \left. \left. \right|_{b_s} \right|_{b_d}
\]

\[
I_D = \frac{Z \sigma a^3 q N_D}{L} \left[ \frac{b^2 - b_s^2}{2} \left( 1 + \frac{\epsilon S_X}{\epsilon I_a} \right) - \frac{b_d^3 - b_s^3}{3} \right], \quad (4.89b)
\]
The y-parameters in matrix form is

\[
Y = \frac{1}{\Delta} \begin{bmatrix}
(R_T R_s' - T_s R_d') & (R_T R_s' - T_s R_s') \\
(T_d R_s' - R_d R_s') & (T_d R_d' - R_d R_d')
\end{bmatrix}
\begin{bmatrix}
b_s \\
b_d
\end{bmatrix}
\tag{4.91}
\]

where
\[
\Delta = K (R_s' R_d' - T_s' R_d'),
\]
\[
K = - \frac{I_D}{(s \theta N_D \sigma Z^2 a^2)}.
\tag{4.92}
\]

After some strenuous algebra, it can be shown that

\[
Y = \frac{1}{(1 + st_0)} \begin{bmatrix}
(1 + st_1) & 1 \\
-1 & (1 + st_2)
\end{bmatrix}
\begin{bmatrix}
g(W_{SG}) \\
g(W_{DG})
\end{bmatrix}
\tag{4.94}
\]

where
\[
\tau_0 = \frac{\epsilon_s L^2}{\sigma a^2} \frac{b^5}{s^5} \frac{(1 + \frac{\epsilon_s x}{\epsilon_1 a})^2}{6} \left[ 1 - 5B^2 + 5B^3 - B^5 \right] \\
\quad - \frac{(1 + \frac{\epsilon_s x}{\epsilon_1 a})}{4} \left[ 1 - 3B^2 + 3B^4 - B^6 \right] \\
\quad + \frac{b^2 S}{14} \left[ 1 - 7B^3 + 7B^4 - B^7 \right],
\tag{4.95}
\]

\[
\tau_1 = \frac{\epsilon_s L^2}{\sigma a^2} \frac{b^3}{s^3} \frac{(1 + \frac{\epsilon_s x}{\epsilon_1 a})}{6} \left[ 1 - 3B^2 + 2B^3 \right] \\
\quad - \frac{b}{2} \left[ 1 - 4B^3 + 3B^4 \right],
\tag{4.96}
\]

\[
\tau_2 = \frac{\epsilon_s L^2}{\sigma a^2} \frac{b^3}{s^3} \frac{(1 + \frac{\epsilon_s x}{\epsilon_1 a})}{6} \left[ 2 - 3B + B^3 \right] \\
\quad - \frac{b}{2} \left[ 3 - 4B + B^4 \right],
\tag{4.97}
\]

\[
B = \frac{b_d}{b_s},
\tag{4.98}
\]

\[
D = \left[ \frac{b^2 - b_d^2}{s^2} \left( 1 + \frac{\epsilon_s x}{\epsilon_1 a} \right) - \frac{(b^3 - b_d^3)}{s^3} \right].
\tag{4.99}
\]

The corresponding open circuit impedance matrix is

\[
Z = \frac{(1 + st_0)}{s (t + \tau + s t \tau)} \begin{bmatrix}
1 & 0 \\
0 & 1
\end{bmatrix} \begin{bmatrix}
(1 + st_1) & 1 \\
1 & (1 + st_2)
\end{bmatrix}
\tag{4.100}
\]
Fig. 4.7 A general representation of a Z-parameter equivalent circuit.

Fig. 4.8 An equivalent circuit of the generalized URC structure.

\[ R_1 = \frac{1}{g(W_{SG})} \left( \frac{\tau_2}{(\tau_1 + \tau_2)} \right) ; \quad L_1 = \frac{\tau_0 \tau_2}{(\tau_1 + \tau_2)} \cdot \frac{1}{g(W_{SG})} \]

\[ R_2 = \frac{\tau_0}{g(W_{SG})} \left( \frac{(\tau_1 + \tau_2)}{(\tau_1 + \tau_2)} \right) ; \quad C_2 = (\tau_1 + \tau_2) \cdot g(W_{SG}) \]

\[ R_3 = \frac{g(W_{SG}) (\tau_0 + \tau_1) - \tau_0 g(W_{DG})}{(\tau_1 + \tau_2) g(W_{SG}) g(W_{DG})} \]

\[ C_3 = \frac{(\tau_1 + \tau_2) g(W_{SG}) g(W_{DG})}{g(W_{SG}) - g(W_{DG})} ; \quad \frac{Z_M}{Z_C} = \frac{1}{1 + s \frac{\tau_1 g(W_{SG})}{g(W_{SG}) - g(W_{DG})}} \]
A T-network can be set up to represent the above matrix (4.100). If we neglect higher order terms in $s^2$, i.e., for low frequency approximation, the lumped elements in such a circuit (fig. 4.7) are:

\[
Z_a = \frac{1}{g(W_{SG})} \frac{\tau_2 (1 + s \tau)}{(\tau + \tau)^2},
\]

(4.101)

\[
Z_b = \frac{1}{g(W_{SG})} \frac{1 + s \tau}{s(\tau + \tau)^2},
\]

(4.102)

\[
Z_c = \frac{1}{s(\tau + \tau)^2} \frac{g(W_{SG}) - g(W_{DG})}{g(W_{SG}) g(W_{DG})} + s \left[ g(W_{SG}) (\tau + \tau) - \tau g(W_{DG}) \right],
\]

(4.103)

\[
Z_M = \frac{g(W_{SG}) - g(W_{DG})}{s(\tau + \tau)^2} \frac{1}{g(W_{SG}) g(W_{DG})}.
\]

(4.104)

Using the basic electrical elements $R$, $L$, and $C$, it can be shown that a series combination of $R$ and $L$ will satisfy $Z_a$; and similarly for $Z_b$ and $Z_c$, the $R$, $C$ combinations like the ones given in the final equivalent circuit (fig. 4.8) are appropriate.
CHAPTER 5
Applications of URC Structures in Null Networks

5.1 Introduction

Distributed RC structures have many potential applications as electrical circuit components in microminiaturization. In a monolithic integrated circuit, such structures are often produced unintentionally when reversed-biased p-n junction isolation is used. For a basic 3-layer resistance-capacitance-resistance structure alone, Castro et al. illustrated that up to 13 non-redundant one-port and 21 non-redundant 2-port network functions are possible under various terminal connections. When used as a low-pass filter, a URC structure has an exponential cut-off in frequency response which is more ideal than many conventional filters using lumped parameters alone. A null network can be produced by connecting an appropriate lumped resistor in series with a URC structure. This narrow band rejection filter is useful as a component in high-Q tuned amplifiers, oscillators, and threshold transducers. For complex network functions, modern synthesis techniques on distributed-lumped-active networks, including the use of optimization, can result in fewer components than comparable realization using lumped elements alone.

It is the intention of this chapter to look at the physics of null networks which contain distributed RC sections that have used a semiconductor for the resistive component.

5.2 Review

In 1960, Kaufman proposed the first notch filter using a distributed RC section with a lumped resistor in series (fig. 5.1.a). Its operation can be understood by noting that a single URC structure is by itself a low-pass filter, and that its input impedance is capacitive.
Given a network as in fig. 5.1.b, the voltage $V_1$ across the distributed RC section lags the input $V_i$, and the input current and hence $V_3$, lead $V_i$. Now, the distributed section can produce more than 90° phase shift, so it is possible to construct $V_3$ equal in magnitude but opposite in phase to that of $V_2$ by choosing an appropriate value for the lumped resistor $R_n$.

An equivalent null network is obtained by replacing the resistor $R_n$ with a lumped capacitor $C_n$ in parallel with the distributed RC low-pass filter as in fig 5.1.c. In fact, Wyndrum\textsuperscript{110} showed that a whole class of notch networks can be produced by using combinations of $R$ and $C$ or, $R$ and $L$ in place of $R_n$. To generalise, the mechanism of any null network using distributed RC sections is as follows:

By analogy with transmission line theory, we can establish a π or T equivalent circuit (fig. 5.2) for an entire URC structure using the cascade of an infinite number of the subregions derived in section 4.5.2.
Fig. 5.2  \( \pi \) and \( T \) equivalent circuits for the URC low-pass filter. An admittance \( Y_p \) or a impedance \( Z_s \) can be connected to the URC for notch network formation.

A zero of transmission will occur when either an admittance \( Y_p = -Y_2 \) is placed in parallel with \( Y_2 \) or an impedance \( Z_s = -Z_b \) in series with \( Z_b \). If we plot the phase angles of \( Y_2 \) and \( Z_b \) as a function of normalized frequency \( \chi = \omega RC \) (fig. 5.3), with \( R \) as the resistance and \( C_t \) the capacitance of

![Diagram showing \( \pi \) and \( T \) equivalent circuits for the URC low-pass filter.](image)

Fig. 5.3 Phase angle of \( Y_2 \) and \( Z_b \) as a function of normalized frequency \( \chi = \omega RC \). (After J. Stein, ref. 112).
the distributed section, we obtain the phase requirement for either $Z_s$ or $Y_p$. For instance, a null is produced at the normalized frequency $\chi = 11.19$ when a resistor is placed in series with $Z_b$, and for the null to occur at $\chi = 30.84$, a capacitor will be required. The result is summarized in table 5.1.

**TABLE 5.1**

<table>
<thead>
<tr>
<th>$\chi=\omega RC_t$</th>
<th>$Z_s$</th>
<th>$Y_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0 &lt; \chi &lt; 11.19$</td>
<td>R,L</td>
<td>-G,C</td>
</tr>
<tr>
<td>11.19</td>
<td>R</td>
<td>C</td>
</tr>
<tr>
<td>$11.19 &lt; \chi &lt; 30.84$</td>
<td>R,C</td>
<td>G,C</td>
</tr>
<tr>
<td>30.84</td>
<td>C</td>
<td>G</td>
</tr>
<tr>
<td>$30.84 &lt; \chi &lt; 60.45$</td>
<td>-R,C</td>
<td>G,L</td>
</tr>
<tr>
<td>60.45</td>
<td>-R</td>
<td>L</td>
</tr>
<tr>
<td>$60.45 &lt; \chi &lt; 99.93$</td>
<td>-R,L</td>
<td>-G,L</td>
</tr>
<tr>
<td>99.93</td>
<td>L</td>
<td>-G</td>
</tr>
</tbody>
</table>

For $\chi > 99.93$, the whole pattern repeats itself.

Solutions for the differential equation (4.63) are straightforward when both $G(y)$ and $C_t(y)$ are constants, as is the case of a URC structure with uniform depletion layer width from source to drain. The impedance matrix is

$$Z = \begin{bmatrix} R \coth \gamma & R \coth \gamma \\ \frac{R}{\gamma} \coth \gamma & \frac{R}{\gamma} \coth \gamma \\ \frac{R}{\gamma} \coth \gamma & \frac{R}{\gamma} \coth \gamma \end{bmatrix}$$

(5.1)

where $\gamma = \sqrt{gRC_t} = \sqrt{j\chi}$, with $\chi = \omega RC_t$.

For the notch network with lumped resistor $R_n$ in series with the distributed section, the open circuit voltage transfer function is
A zero of transmission occurs when the numerator of $T$ is equal to zero, i.e. 
\[
\frac{R}{\gamma} \coth \sqrt{\chi} + R_n = 0 \quad (5.4)
\]

Equating the real and imaginary parts of this transcendental equation individually to zero, we obtain:
\[
\tanh \frac{\sqrt{\chi}}{2} = -\tan \frac{\sqrt{\chi}}{2} \quad (5.5)
\]
and the notch parameter
\[
\alpha = \frac{R}{R_n} = 2 \sqrt{\chi/2} \sin \sqrt{\chi/2} \cosh \sqrt{\chi/2} \quad (5.6)
\]

Equation (5.6) has an infinite set of solutions for $\chi$, denoted by \{\chi_n\}. Its fundamental solution is at $\chi_1 = 11.1902$, with the corresponding optimal notch parameter $\alpha_1 = 17.786$.

Kaufman also obtained a variation (tuning) in the notch frequency of his null network by adjusting the p-n junction capacitance $C_t$ with an external biasing voltage $V_B$ (fig. 5.1.a). In such a process, however, the value of $R$ is also altered by the different space charge width extending into the semiconductor resistor. Consequently, the optimal notch parameter $\alpha_1$, hence 'infinite' attenuation, is not obtained at all accessible values of the notch frequency. Similar imperfection occurs with the tunable notch network proposed by Golembeski. One solution, like that of Swart's filter, is to allow the distributed capacitance $C_t$ to be adjusted independently without any appreciable change in the value of $R$. A layer of heavily doped semiconductor, sandwiched between the resistive and the dielectric films, can be used to house the space charge capacitance $C_s$ of $C_t$, thereby preventing the semiconductor space charge region from spreading into the resistive film. A new and simpler notch network is proposed in section 5.4, in which an optimal null is maintained at all tunable frequencies.
5.4 Theoretical notch characteristics of a simple URC in series with an external resistor $R_n$
5.3 Notch Filter Comprising a Semiconductor URC Structure

5.3.1 Theoretical Tuning Characteristicies

Consider the notch network obtained from a thin-film semiconductor URC low-pass filter connected in series with an external impedance $Z_b$. It is assumed for the moment that $Z_b$ can adjust itself automatically to give an optimal notch at any accessible value of the notch frequency. At the notch, (5.5) is satisfied, which means that $\chi = \omega R C_t$ is a constant. If the tunability factor $\eta$ is defined as the percentage change in frequency

$$\eta = \frac{\omega_f - \omega_F}{\omega_F} = \frac{\omega_f}{\omega_F} - 1$$  \hspace{1cm} (5.7)

where the subscripts $f$ and $F$ denote flat-band and depletion cases respectively, the ratio $(R C_t)_F/\omega_f = \omega_f/\omega_F$ will offer a measure of the range of tunability under channel depletion of the URC structure.

Using the depletion layer approximation,

$$\frac{(R C_t)_F}{(R C_t)_f} = \frac{1}{1 - \frac{x_{dmax}}{a}} \frac{1}{1 + \frac{\varepsilon_s x_{dmax}}{\varepsilon_o a}}$$

$$\Rightarrow \frac{(R C_t)_F}{(R C_t)_f} = \eta_{max} + 1 = \frac{1}{1 - \frac{x_{dmax}}{a}} \frac{1}{1 + \frac{x_{dmax}}{a}}$$  \hspace{1cm} (5.8)

The above function is graphed in fig. 5.5 for a few $\zeta = \frac{\varepsilon_s x_{o}}{\varepsilon_o a}$.

In contrast to other tunable notch filters using only depletion capacitance as a means for frequency selection (e.g. Swart's filter), the present network has a wider choice in tunability, above and below the semiconductor flat-band frequency $\omega_f$. We shall elaborate this point further in the next section. The two operation modes are distinguished by $\eta > 0$ in mode 1 and $\eta < 0$ in mode 2.

A few interesting characteristics of $\eta$ derived from fig. 5.5 are noted below:
Fig. 5.5 Tunability factor $\eta$ vs. normalized space-charge width $x_d/a$ as a function of the notch parameter $\xi$. 
(1) Given a URC structure, thus $\xi$, variation in $n$ follows the locus of constant $\xi$ from $x_d=0$ to $x_{d_{\text{max}}}$.

(2) For a notch network having $\xi \leq 1$ and, $x_{d_{\text{max}}}/a > \xi$, the null can be tuned to a frequency $\omega_f$ either higher or lower than $\omega_f$. The minima in $\xi$, at $x_d/a = \frac{1}{2}(1 - \xi)$, pertain to maximum percentage changes in the range of tunability when the device is made to operate in mode 2.

(3) From (5.8) we observe that the value of $\xi$ depends entirely on the rates of change of $C_t$ and $R$ under depletion. At first, the rate of change of $C_t$ with respect to $x_d/a$ is more rapid than $R$, then the trend is reversed at $x_d/a = \frac{1}{2}(1 - \xi)$ whence, the rate of increase in $R$ will start to over-take that of the decrease in $C_t$. Beyond $x_d/a = \xi$, the change in $R$ will become the dominating factor in the control of $n$.

5.3.2 Practical Considerations in Design Optimization

An application engineer is often more interested to know the tradeoff in his design for achieving a particular tuning characteristic and, the means of attaining the maximum tunability factor for his null network. According to fig. 5.5, the optimal tunability factor $n_{\text{op}}$ for operation in mode 2 under constant $\xi$ is at $x_d/a = \frac{1}{2}(1 - \xi)$, and it can be approached in either one of the following two ways:

(i) For a given doping concentration of the semiconductor film, $x_{d_{\text{max}}}$ is a fixed value. To obtain $n_{\text{op}}$, one would have to choose the ratio $x_{d_{\text{max}}}/a$ equal to $\frac{1}{2}(1 - \xi)$. This value of $n_{\text{op}}$ is graphed in fig. 5.6.

(ii) For the notch network to be fabricated in conjunction with other passive or active elements on the same chip, the freedom in choosing film thicknesses $a$ and $x_0$, hence $\xi$, is often severely hampered in order to reduce the total number of processing steps to a minimum. Under such a circumstance, one would have to pick the impurity concentration of the semiconductor at a level which would result in $n$ as close to $n_{\text{op}}$ as
Fig. 5.6 Optimal tunability factor $\eta_{op}$ as a function of $\xi$ for devices operating in mode 2.

possible.

For optimal operation of the notch filter in mode 1, the URC should have the biggest possible values of $\xi$ and $x_{d_{\text{max}}}/a$.

Physical limitations in the selection of parameters $x_{d_{\text{max}}}/a$ and $\xi$ can be illustrated by using Si and its thermally grown oxide. Typical epitaxial silicon films have a doping concentration $\sim 10^{16} \text{ cm}^{-3}$, which corresponds to a maximum depletion layer width of $\sim 0.86 \times 10^{-4} \text{ cm}$. Also, commonly used epitaxial silicon films have thicknesses in the range of 1-2 $\mu$, hence thin-film silicon notch filters can be easily implemented to give a $x_{d_{\text{max}}}/a$ ratio close to unity; and, in reality, can have a large percentage change in notch frequencies when they are made to operate in mode 1. The trade-off in cutting down appreciably the size of a conductive channel by designing a relatively thick space charge layer will be a large increase in both the input and output impedances of the notch network.
Physical limitations on the values of $\xi$ are much more severe than those on $x_{d_{\text{max}}}/a$. In fact, for silicon and its thermally grown oxide, $\xi=.01$ and $\xi=1.0$ correspond to oxide thicknesses of $70\,\AA$ and $.7\,\mu$ respectively for a $2-\mu$ thick semiconductor. Thin oxide films are avoided because of electronic conduction$^{116}$ through the oxide; and extremely thick oxides are not desirable, because prolonged exposure to high temperature ambient during oxide growth may cause excessive impurity redistributions in the semiconductor.

The accuracy of this theoretical tuning characteristic is dependent on the precision of our definition of the space charge width $x_d$. According to Lehovec et al.$^{115}$, $x_d$ in its defining equation (A-9) actually corresponds to our terminology of $x_{d_{\text{max}}}$. If we plot the voltage-capacitance curve of a MIS structure using the depletion approximation and, superimpose on it the more accurate C-V curve arrived at by Grove et al.$^{121}$, we would observe good agreements between the two curves in the region of deep semiconductor surface depletion. Hence, we conclude that (5.8) is at the least qualitatively correct. Further, we are to expect a much larger deviation in the tuning characteristics from the above theory when the actual device is made to operate in accumulation or inversion mode.

5.4 A Tunable Notch Network using Double URC Sections

To obtain high attenuation in Kaufman's network$^{106}$, the notch parameter $a$ should be kept constant at all values of the notch frequency. But such a requirement can be met only if one is prepared to adjust the external resistor $R_n$ at the same time as one changes $C_t$. The reason is that the value of $R$ is altered with the space charge width in the process of tuning. The following circuit, however, is designed to eliminate the requirement of this extra parameter of control.

Consider two distributed sections connected in series as shown in fig. 5.7.a. For $R_B<<R$, the channel to gate potentials for the two URCs will
be $V_B$; which means that if both the semiconductor and oxide film thicknesses are alike, their space charge widths together with their conductive channel depths ($a - x_d$) for a given external biasing voltage $V_B$ will be the same. We shall see the significance of such an arrangement in the following analysis.

Using the results of standard transmission line solutions (Appendix B), we have for a 3-terminal URC structure

$$Z_{11} = \frac{R}{\gamma} \coth \gamma,$$

$$Z_{12} = \frac{R}{\gamma} \operatorname{cosech} \gamma; \quad (5.9)$$

and a 2-terminal URC structure, with its source and gate terminals connected together,

$$Z_{11} = \frac{Z_{11n}^2 - Z_{12n}^2}{Z_{11n}}. \quad (5.9.b)$$

For series connection of these two URC structures as in fig. 5.7.b, the open circuit voltage transfer function

$$T = \frac{Z_{12} + Z_n}{Z_{11} + Z_n} = \frac{R/\gamma \frac{R}{\gamma n} \operatorname{cosech} \gamma \coth \frac{\gamma}{n} + (R/\gamma n \operatorname{coth} \gamma n)^2 - R^2/\gamma n^2 \operatorname{cosech}^2 \gamma n}{R/\gamma \frac{R}{\gamma n} \operatorname{cosech} \gamma \coth \gamma n + (R/\gamma n \operatorname{coth} \gamma n)^2 - R^2/\gamma n^2 \operatorname{cosech}^2 \gamma n}.$$

For zero transmission, the numerator of (5.10) should be zero,
\[
\frac{R}{\gamma} \frac{1}{\sinh \gamma} + \frac{R_n}{\gamma_n} \frac{\cosech^2 \gamma_n - 1}{\sinh \gamma_n \cosh \gamma_n} = 0. \tag{5.11}
\]

If we adopt the following notations:
\[
\frac{R}{R_n} (\gamma_n/\gamma) = \alpha, \quad \gamma/\gamma_n = \beta, \quad \gamma = \sqrt{j \chi} = (1 + j)y, \tag{5.12}
\]
where \(\alpha = \omega R C_t\), \(y = \sqrt{y/2}\), equation (5.11) becomes
\[
\frac{2 \alpha}{\exp (1 + j)y - \exp -(1 + j)y} + \frac{\exp (1 + j)y_n - \exp -(1 + j)y_n}{\exp (1 + j)y_n + \exp -(1 + j)y_n} = 0. \tag{5.13}
\]

Equating the real and imaginary parts separately to zero, we get
\[
\alpha (\cos y)(\sinh y)(\cosh^2 \gamma_n - \sin^2 \gamma_n) + \sinh \gamma_n (\cosh \gamma_n)(\cosh^2 y - \cos^2 y) = 0, \tag{5.14}
\]
\[
\alpha (\sin y)(\cosh y)(\cosh^2 \gamma_n - \sin^2 \gamma_n) - \cos \gamma_n (\sin \gamma_n)(\cosh^2 y - \cos^2 y) = 0. \tag{5.15}
\]

This last set of simultaneous equations can be solved by using Newton's iteration method for a given value of \(\alpha\).

Numerical solution for (5.14) and (5.15) was done using the relationship \(\gamma_n/\gamma = \gamma_n/\gamma = 1/\beta\). A sample of the result which is within practical range of the notch parameters \(\alpha\) and \(\beta\) is given in table 5.2.

<table>
<thead>
<tr>
<th>(\alpha)</th>
<th>0.5</th>
<th>1.0</th>
<th>5.0</th>
<th>10.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\chi_1)</td>
<td>11.21</td>
<td>11.29</td>
<td>13.17</td>
<td>16.7</td>
</tr>
<tr>
<td>(\beta_1)</td>
<td>35.74</td>
<td>18.08</td>
<td>4.57</td>
<td>2.92</td>
</tr>
<tr>
<td>(\chi_2)</td>
<td>149.28</td>
<td>149.28</td>
<td>149.28</td>
<td></td>
</tr>
<tr>
<td>(\beta_2)</td>
<td>0.69 x10^5</td>
<td>0.345 x10^5</td>
<td>0.69 x10^4</td>
<td></td>
</tr>
</tbody>
</table>

* If we combine (5.14) and (5.15), we arrive at the transcendental equation for the double URC network
\[
\frac{\sinh^2 \gamma_n}{\sin^2 \gamma_n} \tanh y = - \tan y.
\]

In the limit as \(C\) goes to zero, \(\sinh^2 y / \sin^2 y\) goes to unity, and we have the transcendental equation (5.5) for series combination of a URC section with a lumped resistor \(R_n\).
Similar to the properties of the transcendental equation (5.5), there are infinite sets of solutions for \( \{x_n\} \) and \( \{\beta_n\} \) for a given value of \( \alpha \) in (5.14) and (5.15). But, due to the exceedingly rapid increase in the order of magnitude of \( \beta \), the second and higher order solutions are physically impossible to implement in a realistic device.

Let us consider the notch parameters \( \alpha \) and \( \beta \) in slightly more detail. According to our definition of \( \alpha \) and \( \beta \) given in (5.12), we have

\[
\alpha = \frac{R}{R_n} \frac{\gamma_n}{\gamma} = \sqrt{\frac{R}{R_n} \frac{C}{C_n}},
\]

(5.16)

\[
\beta = \frac{\gamma}{\gamma_n} = \sqrt{\frac{R}{R_n} \frac{C}{C_n}}.
\]

(5.17)

Since the two URC sections have the same semiconductor and oxide film thicknesses (they are fabricated on the same chip through the same processing steps) and, because the dc gate to channel potential would be the same in both of them (fig. 5.7.a), the ratios \( R_n/R \), \( C_n/C \) are simplified to

\[
\frac{R_n}{R} = \frac{\ell_n W_n}{\ell W_n},
\]

(5.18)

\[
\frac{C_n}{C} = \frac{\ell_n W_n}{\ell W},
\]

(5.19)

where \( \ell, \ell_n \) and \( W, W_n \) are respectively the lengths and widths of the two URC sections. With these, we arrive at the relationship

\[
\alpha = \frac{W_n}{W}, \quad \beta = \frac{\ell}{\ell_n}.
\]

(5.20)

In other words, to attain an optimal null in the tunable double-URCs notch network, we only need to design the lengths and widths of the 2 URC sections in accordance to the values of \( \alpha \) and \( \beta \) specified by (5.20). This will allow us, then, the freedom to choose the semiconductor and the oxide film thicknesses, as well as the impurity level in the semiconductor for attaining a maximum percentage change in tunable frequencies of the null device.
A typical design procedure for such a notch network is:

1. pick a convenient set of values $\alpha$ and $\beta$, from fig. 5.8,
2. find the corresponding normalized frequency $\chi$, and design the lengths and widths of the distributed sections to give the notch frequency $\omega_n$ as desired;
3. then optimize the maximum tunability factor according to the procedure outlined in section 5.3.2 and, arrive at the values for the semiconductor impurity concentration and the thicknesses $a$, and $x_o$.

In order to make the two distributed sections more compatible in size to each other, and the ratio of the length to width of each URC not too unreasonable, one would select the values of $\alpha$ and $\beta$ lying in the neighborhood of point Q in fig. 5.8. On the other hand, if the designer is more interested in compact miniaturization of the 2 URC sections, he would prefer to choose the set $(\alpha, \beta)$ given by point P in fig. 5.8, which corresponds to a minimum in total surface area occupied by the 2 URCs.

![Fig. 5.8 Notch parameters $\alpha$ and $\beta$ of the double-URCs notch filter.](image)
Fig. 5.10 Theoretical magnitude and phase response of a double URC notch filter \((\alpha=3.0, \beta=6.67)\).
5.10 Effect of notch parameter variations on the notch characteristics of a double-URC filter ($\alpha=3.0$, $\beta=6.74$).
CHAPTER 6

Experiments on Semiconductor Thin-Film URC Notch Filters

6.1 Introduction

Epitaxial silicon on spinel was chosen for the experiments because: (a) high quality wafers were commercially available, (b) conventional silicon technology can be used for the fabrication processes, and (c) SiO₂ can be readily prepared by thermal oxidation.

The URC structure used is similar to a coplanar-electrode TFT as introduced by Weimer¹¹⁷. This configuration has the advantage of allowing the semiconductor to be processed at elevated temperatures, as is required for thermal oxide growth, without the electrodes undergoing the same treatment. A typical structure is as shown in fig. 4.1. An external resistor $R_n$ was connected in series with the URC to generate a null network (fig. 5.1.b). The leads between ground, $R_n$, and the gate electrode were made as short as possible to minimize the parasitic inductance which affects the notch characteristics (see section 3.3.2 in ref. 115).

6.2 Fabrication Technique for a URC Structure

6.2.1 Fabrication Processes

The processing steps were:

1. A rectangular mesa was etched out of the epitaxial film in a solution of 5HNO₃(75%):3HF(49%):3HAc by volume. It was to bear the same length and width as the final URC structure.

2. A thin cap of thermally grown SiO₂ was prepared by oxidizing the silicon mesa in steam at 1050°C.

3. An aluminum film of 2-3 thousand Å thick was vacuum evaporated to cover the entire substrate surface.

4. The resulting structure was annealed in a N₂ atmosphere at 400°C for
1/2 hr.

(5) Photoresist masking was used to define the oxide region of the URC. The unwanted SiO₂ over the source and drain regions were removed in an etchant containing 3:1 by volume of HF with H₂O. This step was preceded by etching away the aluminum and the upper 200 Å of SiO₂ using a P-etch*, which was intended to remove any ions that were made to segregate at the aluminum/SiO₂ interface by the annealing step.

(6) An approximately 2000 Å thick of Au film doped with 0.1% Sb was vacuum deposited over the whole structure. It was sintered into the semiconductor source and drain regions at 425°C in a N₂ atmosphere, thereby forming ohmic contacts to the n-type channel.

(7) Finally, the metal electrodes were defined using photoresist masking.

6.2.2 Cleaning the Si and SiO₂ Surfaces

An epitaxial silicon chip that had been cut to about twice the size of a final URC structure was degreased in an ultrasonically agitated trichloroethylene bath for 5 minutes. This was followed by rinsing successively in acetone and distilled water. The surface was subsequently dried by blowing air from a plastic squeeze bottle over the epitaxial film surface.

Before thermal oxidation, the silicon sample was cleaned in a solution containing 1 part H₂O₂, 1 part NH₄OH and 4 parts of H₂O by volume for 15 minutes. The sample was then rinsed in 2 successive baths of ultrasonically agitated distilled water, followed by 1 bath of deionised water.

6.2.3 Photoresist Technique

Standard photolithography technique was used for device pattern formations. The photolithography masks used in the experiment were on a 2"x2"

* P-etch constituents are: 15ml 49% HF, 10ml 70% HNO₃, and 300ml H₂O.
It has an etching rate for thermally grown SiO₂ of 140Å/minute.
Fig. 6.1 Photographic masks used for device fabrication; from top to bottom, and left to right: (1) for the silicon mesa, (2) for the SiO₂ region, (3) for defining the metal-electrodes. The fourth mask has not been used, but it illustrates the source and drain regions of the 4 devices defined by (1).

A high resolution glass slide obtained from Shaw Studio*. The original artwork, at 20x magnification, was made on Keuffel & Esser "Cut n' Strip" mylar-backed artwork sheet. Three masks were required: one for defining the semiconductor mesa structure, one for the dielectric layer, and the third for isolating the contact electrodes (fig. 6.1).

5 drops of KTFR (diluted to a ratio of 4:5 with Kodak Thinner) was applied on to the sample spinning at 2000 rpm. The resist was applied through a syringe using a 0.45 Metricel filter. The sample was spun for at least 2 minutes before baking at 38" distance from a G.E. infra-red heat lamp (resulting in a temperature of about 75°C) for 15 minutes.

After cooling, the dried sample was placed on to a micro-manupulator and the photomask, with the emulsified side facing down, was lowered on to direct contact with the resist film. An exposure time of 6 minutes was used for a 1μ thick resist film 6" underneath a Westinghouse 275W sun lamp. This was followed by developing in Kodak Thin Film Developer for 1½ minutes and then rinsing for 30 seconds in Kodak Thin Film Rinser. An after-bake of 10 minutes was used.

* Shaw Photogrammetric Services Ltd., Ottawa, Ontario.
6.2.4 High Temperature Treatments

For thermal oxidation, SiO\textsubscript{2} annealing in N\textsubscript{2} atmosphere, and Sb-Au alloying with Si, a JMC electric furnance was used. The reaction chamber consisted of a 3' long, $\frac{1}{4}\text{"}\text{DIA}$ quartz tube with the central portion suspended inside a S-288 element. A clean piece of 1"x2" alumina wafer was used as sample holder. It could be slid in and out of the tube with the help of a $\frac{1}{8}\text{"}\text{DIA}$ quartz tubing having a peg at one end. The wafer was stabilized by laying its face flat and by resting its two parallel edges on the inner curved surface of the quartz tube.

Silicon oxidation was carried out at 1050\textdegree C in a steam atmosphere. The temperature was registered by a chromel-alumel thermocouple inserted into the tube from one end. After about 10 minutes, a typical oxide layer thickness of 2000 \AA\ is obtained. The steam was then cut-off, and N\textsubscript{2} was introduced. The sample was retracted from the hot zone at a rate of 1'/min. to one end of the tube where it was allowed to cool down to the room temperature.

A similar procedure was used for N\textsubscript{2} annealing and for Sb-Au alloying. Since Au has a high diffusivity in silicon, the sample was never left at the alloying temperature for more than 30 seconds.

6.2.5 Film Thickness Measurements

For SiO\textsubscript{2}, measurements were taken from an ellipsometer using a He/Ne laser (6328 \AA) and an incident angle of 60\textdegree. Optical constant of (3.86, 0.00452) was assumed for silicon. The oxide film thicknesses were derived from matching the computed thicknesses with the SiO\textsubscript{2} color chart. The error introduced by neglecting the substrate's refractive index and the interference of light inside the SiO\textsubscript{2} and Si films was estimated to be less than 50 \AA, and was beyond the accuracy required.

Silicon film thicknesses were calculated from the original epi-
taxial layer thicknesses and the amount that had been transformed into the SiO₂.

Fig. 6.2 A sample of the final devices (this chip contained 2 devices having the same length but different widths).

6.3 Channel Conductance under Non-uniformed Depletion Layer Width

For an n-type epitaxial silicon covered by its thermally grown SiO₂, the low temperature N₂ annealing treatment so described in section 6.2.1 for the URC structure produced a thin depletion layer at the Si-SiO₂ interface. The disappearance of donor surface states, which are normally present after thermal oxidation of silicon, is confirmed by the flat-band voltage shift in the capacitance-voltage characteristic of such a sample.

The variation of channel conductance was observed on a Tetronix type-575 Transistor Curve Tracer. The gate was at first electrically shorted to the drain; and by increasing the drain voltage (positive with respect to the source), a partial accumulation of the channel at the source end could be obtained. Next, the gate was connected to the source; and, with positive drain voltage, a channel depletion into the inversion mode could be apprehended at the drain terminal. Now, by assuming that the original channel had a uniform depletion layer width all the way from the source end to the drain end, the above arrangement would correspond to grounding the gate and the source, and varying the channel profile by the dc voltage applied to the drain. The drain current I_D and drain voltage V_D characteristic thus obtained would display the channel conductance under partial accumulation, depletion, and inversion (fig. 6.3). The purpose of using at all time positive I_D and V_D is to avoid misinterpretation of channel
conductance caused by non-uniformity of the silicon film, and by inhomogeneous source and drain contacts with the channel.

![Diagram](image)

Fig. 6.3 Qualitative description of the channel under
(a) deep-depletion at the drain, (b) accumulation at the drain.

The characteristics of two URC samples are shown in fig. 6.4. The regions marked I, II, III correspond to accumulation, depletion, and inversion at the drain terminal with the source and the gate both grounded (fig. 6.3). According to (4.29), the drain current for small magnitude of the drain voltage under channel depletion is a linear function of the drain voltage, such an effect can be observed around the origin of the \( I_D - V_D \) display in fig. 6.4. With increasing depletion layer width at the drain end, the channel conductance (from slope of the \( I_D - V_D \) curve) decreases until it either saturates (due to channel pinch-off (fig. 6.4.a)), or approaches a constant value after the depletion layer width at the drain terminal reaches a maximum (fig. 6.4.b).

However, for increasing channel accumulation at the drain end (fig. 6.3.b), which corresponds to reducing the total space-charge region in the channel, we observe, contrary to our prediction, a decrease rather than an increase in the overall channel conductance (fig. 6.4). This controversial observation may be attributed to charge redistribution at the silicon/sapphire
interface as a result of large horizontal electric field in the channel.

Fig. 6.4 $I_D-V_D$ characteristics of silicon thin-film URC structures;
(a) with channel pinch-off at the drain terminal, (b) without channel pinch-off.
6.4 Silicon Thin-Film URC Notch Filters

A low-inductance variable resistor $R_n$, e.g. a carbon resistor, was used in series with the URC structure for notch filter formation. The voltage transfer function of the filter was obtained by measuring its output voltage with the circuit shown in fig. 6.5. The bootstrapped follower had an overall attenuation factor of 0.92 in the frequency range of interest. A sinusoidal input signal of 100 mv was used.

Typical amplitude response of the filter is shown in fig. 6.6. Notch attenuation of 40-50 db was generally obtained. However, the measured notch characteristics always differ from the theoretical amplitude response (fig. 5.4) by as much as 20-30% in its Q-value*. This discrepancy was mainly caused by the load resistor that had been connected to the device, while the characteristics of fig. 5.4 were derived for the open-circuited voltage transfer function.

In this work, a larger discrepancy was also observed for the value of $R_n$ used in comparison to that predicted by (5.6) — a deviation of one order in magnitude lower was common. A major contributor to this discrepancy comes from spreading resistances underneath the source and drain regions of the device. An improvement could be made using diffused source and drain regions, and by fabricating the device in a cleaner atmosphere.

Occasionally, when there are structural faults in the semiconductor or SiO₂ thin-films, one would not only obtain less attenuations at the notch frequencies, but also distorted output waveforms similar to the one shown in fig. 6.7. But, interesting enough, one can still observe the 180° phase shift at the notch frequency, as predicted by the theory.

* The Q of the device as defined in here is $f_0/\Delta f$, where $f_0$ is the notch frequency, and $\Delta f$ is the notch gap at 25 db of attenuation.
Source (S): Tetronix type-191 Constant Amplitude Signal Generator.

![Circuit Diagram]

Fig. 6.5 A "bootstrapped" follower used in the measurement of the amplitude response of URC notch filters.
Fig. 6.6. Amplitude response of a thin-film semiconductor URC tunable notch filter.
Fig. 6.7 A display of the distorted waveform from a structurally defective notch filter; the 180° phase shift can be observed by comparing the two pictures taken at signal frequencies a little below (a) and above (b) the notch frequency.

6.5 Notch Frequency Tuning

Fig. 6.8 shows the range of tunability of two devices using the circuit shown in fig. 5.1.a. These filters had been designed to operate in mode 1, and had a maximum tunability of 200-300%. By comparison, a thin-film notch filter tuned by using only capacitance variations in the distributed RC structure gives tunability of only a few tens of per cent, e.g. the best notch filter fabricated by Swart had a tuning capability of 30% with a ± 15V bias voltage.

Fig. 6.9 shows the value of $R_n$ that was required to give an optimal null at the tunable notch frequencies of the two devices. For sample S, the depletion capacitance saturated at a depletion layer width which was less than the semiconductor film thickness. So, for a large negative gate potential, an inversion layer was developed at the Si/SiO₂ interface which lowered the total channel resistance $R$, hence $R_n$. Now, according to the notch condition $RC_t \omega = 11.19$, and with $C_t$ remaining almost
Fig. 6.8.a Notch frequency tunability for sample 0.

Fig. 6.9.a Variations of notch resistor $R_n$ and $C/C_0$ as function of the biased voltage $V_G$ in the tuning range of sample 0.
Fig. 6.8.b Notch frequency tunability for sample S.

Fig. 6.9.b Variations of notch resistor $R_n$ and $C/C_0$ as function of the biased voltage $V_G$ in the tuning range of sample S.
constant under channel inversion, the notch frequency $\omega$ would have to increase by the same amount as $R$ has decreased, which is what the experimental result indicates in fig. 6.8.b. For sample Q under depletion, the channel pinched off before a maximum depletion layer width had been attained. Consequently, for large negative gate potential, the notch frequency leveled off to a constant value.

The capacitance-voltage curves of fig. 6.9 were obtained from a Booton model 71A Capacitance/Inductance Meter with the output displayed on a X-Y recorder. The measurement was done by connecting both the source and drain to the ground terminal of the meter. Since the Booton Capacitance meter actually measures the reactive component of an impedance connected across its terminals, and because the channel conductance of the semiconductor thin-film is normally of the order of ten-thousandth of a mho, the readings recorded by the meter, therefore, does not give the exact capacitance of the URC structure. However, its normalized capacitance vs. voltage curve does qualitatively indicate the regions of channel accumulation, depletion, and inversion.
CHAPTER 7

CONCLUSION

The structural and electrical properties of low-temperature sublimed silicon thin-films on sapphire and spinel substrates has been studied in terms of their growth mechanisms and defect formations. The films were observed to have been formed by continuous nucleation and coalescence of the impinging silicon adatoms, irrespective of the grown-film thicknesses. Consequently, they were characterized by a high density of grain boundaries which were also locations for defect generations. Electron-reflection-diffraction patterns indicated that they consisted of singly oriented crystallites with high angular perfections similar to those obtained from epitaxial silicon films. Reduction in aluminum autodoping in films grown at low substrate temperatures was demonstrated by the growth of n-type films and by the suppression of changes in the film properties during post-deposition thermal oxidation.

When compared to epitaxial silicon films grown at the optimal substrate temperatures, these films were observed to have lower carrier Hall mobilities and higher film resistivities. However, they show the same exponential dependence of resistivities, mobilities, and carrier concentration or temperature. From this we can infer that while aluminum autodoping does cause mobility degradation in epitaxial silicon films grown on sapphire and spinel substrates at the optimal growth temperatures, carrier-scattering by structural defects is still the predominant factor in the control of film qualities.

By using various source doping concentrations but the same growth conditions, it was found that the effective carrier concentrations
deviated more from the source doping level when the latter was at a lower rather than at a higher impurity doping concentration. A defect scattering model using only a single ionization energy level inside the forbidden gap has been proposed. The result was found to be in qualitative agreement with experimental observations. Using this model, the defect density was found to be independent of source doping concentrations, hence the impurity levels in the grown films. They amounted to $10^{12}$ cm$^{-2}$ in films grown at $\sim 800^\circ$C substrate temperature.

The conductance of semiconductor resistors in a distributed RC structure was studied under various channel biasing potentials. While the theory seemed to agree with experimental observations under channel depletion and inversion, a somewhat controversial result was obtained for channel accumulation, the exact origin of which is for the moment unknown.

A detailed mathematical modelling of a URC structure using semiconductor for the resistive component has been made. By using the notation of $C_d = Q_s/\psi_s$ for the depletion layer capacitance the URC structure was shown to be analogous to that of a lossless transmission line.

An ac small signal analysis of a URC structure having a non-uniform channel profile was presented. The result is general enough that it can also be used as an equivalent circuit for a SOS deep-depletion MOST.

The semiconductor URC structure was applied to frequency-tunable notch networks. Analysis based on the depletion approximation showed that both capacitance and conductance variations were incorporated
in the process of notch frequency tuning. Two distinct operation modes are possible. They correspond to using predominantly either the capacitance variations or the conductance variations. In contrast to the traditional tunable thin-film notch filters using only capacitance variations, the present configuration was shown to give a much better tuning capability of up to a few hundreds of per cent.

A new notch network comprising of two URC sections has been proposed. It is characterised by its maintenance of an optimal notch at all tunable values of the notch frequency. Consequently, it makes possible the realization of tunable semiconductor thin-film notch filters for practical device applications.
APPENDIX A

Space Charge at the Semiconductor Surface of a MIS Structure

For semiconductor, the space charge density $\rho(x)$ is given by

$$\rho(x) = q\ (p - n + N_D - N_A) \quad (A-1)$$

where $(N_D - N_A)$ is the net impurity level in the semiconductor.

In a non-degenerate case,

$$n = n_i \exp \left(-\frac{u_F - u}{kT}\right)$$

$$p = n_i \exp \left(\frac{u_F - u}{kT}\right) \quad (A-2)$$

where $u = q\ \psi/kT$, denotes the electrostatic potential relative to the intrinsic Fermi-level in the bulk in $kT/q$ units.

Now, charge neutrality has to be maintained in the bulk semiconductor with $\rho(x) = 0$. This gives

$$N_D - N_A = 2\ n_i\ sinh\ u_F \quad (A-3)$$

Substituting (A-2) and (A-3) back into (A-1), we can write the Poisson's equation as

$$\frac{d^2u}{dx^2} = -\frac{2qn_i}{\epsilon_s} \left[ sinh \left(\frac{u_F - u}{kT}\right) - sinh \frac{u_F}{kT} \right] \quad (A-4)$$

Integrating once from $x = 0$ to $x = \infty$, whereas $u$ and $du/dx$ are both zero, we have for an n-type semiconductor

$$\frac{du}{dx} = \sqrt{\frac{2\epsilon_s}{kT}} \left[ u\ sinh\ u_F + \cosh \left(\frac{u_F - u}{kT}\right) - \cosh \frac{u_F}{kT} \right]^{1/2} \quad (A-5)$$

where $L = \left[\frac{\epsilon_s}{2\beta}\frac{1}{qn_i}\right]^{1/2}$ is the intrinsic Debye-Length,

$$\beta = \frac{q}{kT}$$

By Gauss Law, the total charge per unit area within the semiconductor

$$Q_s = -E_s = \frac{\epsilon_s}{\beta L} \left[ u_s\ sinh\ u_F + \cosh \left(\frac{u_F - u_s}{kT}\right) - \cosh \frac{u_F}{kT} \right]^{1/2} \quad (A-6)$$
The defining equation for depletion layer width is

\[ Q_S = Q_N + q N_D x_d , \tag{A-7} \]

where \( Q_N \) is the inversion layer charge given by

\[ Q_N = q \int_{u_s}^{u_F} n_i \exp \left( \frac{u_F - u}{kT/q} \right) \frac{du}{dx} \tag{A-8} \]

The maximum depletion layer width is assumed to occur at surface potential \( \psi_S = 2 \psi_F \). For \( Q_N \ll Q_S \), we find \( x_d \) by integrating Poisson's equation twice; with \( \rho(x) = q N_D \),

\[ \psi_S = 2 \psi_F = -q \int_0^{x_{d_{\text{max}}}} N_D \times dx + \frac{-qN_D x_{d_{\text{max}}}^2}{2 \epsilon_S} \tag{A-9} \]

so, \( x_{d_{\text{max}}} = \left( \frac{4e^2}{qN_D} \frac{kT}{q} \ln \left| \frac{N_D}{n_i} \right| \right)^{1/2} \). \tag{A-10}

APPENDIX B

Solutions of Lossless Transmission Line Equations

For a lossless transmission line of length \( \lambda \), the equations of state are:

\[
\frac{\partial i(z,t)}{\partial z} = - c \frac{\partial r(z,t)}{\partial t}
\]  

(A-11)

where \( r \) and \( c \) are respectively the distributed resistance and capacitance per unit length.

Taking the Laplace's transform on both sides of (A-11) and assuming zero initial conditions, we have

\[
\frac{dV(s,z)}{dz} = - r I(s,z)
\]  

(A-12)

\[
\frac{dI(s,z)}{dz} = - s c V(s,z)
\]  

(A-13)

Differentiating (A-12) w.r.t. \( z \) and substituting \( dI(s,z)/dz \) from (A-13), we get

\[
\frac{d^2 V(s,z)}{dz^2} = s c r V(s,z)
\]  

(A-14)

The final solution for (A-14) is

\[
V(s,z) = A \exp(az) + B \exp(-az)
\]  

(A-15)

where \( a = \sqrt{src} \) is called the attenuation coefficient.

Using the boundary conditions

\[
V(s,0) = V_1, \quad I(s,0) = I_1, \\
V(s,\lambda) = V_2, \quad V(s,\lambda) = I_2,
\]

we obtain

\[
z_{11} = z_{22} = Z_o \coth \gamma
\]  

(A-16)
\[ z_{12} = z_{21} = Z_o \text{cosech } \gamma, \]

where \( Z_o = \sqrt{r/sc} \) is the characteristic impedance

\[ \gamma = \sqrt{sc/ \omega^2} = \sqrt{sRC} \]

is called the complex propagation factor

\( R = r \lambda = \text{total series resistance} \)

\( C = c \lambda = \text{total capacitance} \)

In a T-network, (fig. 5.2)

\[ Z_a = Z_{11} - Z_{12} \quad (A-17) \]

\[ Z_b = Z_{12} \quad (A-18) \]

This 3-terminal URC structure can also be used as a two-terminal device by connecting terminals (s) and (d) or terminal (s) and (g) together.

When the source and gate of the URC structure are connected together, the impedance of the resulting structure becomes

\[ Z = Z_a + \frac{Z_a Z_b}{Z_a + Z_b} \]

\[ = \frac{Z_{11} - Z_{12}^2}{Z_{11}} \]

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59. A general review is given in:


