A 75-dB DIGITALLY PROGRAMMABLE CMOS VARIABLE GAIN AMPLIFIER

by

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ABSTRACT

A 75-dB DIGITALLY PROGRAMMABLE CMOS VARIABLE GAIN AMPLIFIER

Variable-gain amplifiers (VGAs) are essential building blocks of many communication systems. In this thesis, a monolithic low-power digitally programmable VGA with 75dB of gain range is presented. The VGA is targeted for power line communication systems in particular for automotive application; however, it is a generic block that can be use in other applications. The core of the design is based on the low-distortion source-degenerated differential amplifier structure. A g_m-boosting circuit is also used to provide higher gain and improve gain accuracy.

In this work, to control the gain a new technique is used which is based on digitally controlling: 1) the source-degeneration resistance, and 2) an additional resistance between the differential output nodes of each gain stage. The changes in the source-degeneration resistance handle the coarse tuning, and the changes in the latter resistance are used for fine gain tuning.

The overall VGA consists of three such gain stages. As a proof of concept, a single gain stage with a gain range of 24dB and programmable in 2dB gain steps has been fabricated in a 0.18μm CMOS technology. The chip is tested and measurement results are obtained. Based on these measurement results, the design of the gain stage is optimized and a three-stage 75dB VGA is designed. Each stage has a digitally tunable gain range of 25dB, and fine gain tuning of 2.5dB per step. The bandwidth of the VGA is higher than 140MHz, and the gain error is less than 0.3dB. The overall VGA draws 6.5mA from a 1.8V supply. The noise figure of the system at maximum gain is 12.5dB, and the IIP3 is 14.4dBm at minimum gain. These performance parameters are either better or compare favorably with the reported state-of-the-art VGAs.

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Chapter 1

INTRODUCTION

Programmable gain circuits are essential components of many communication and electronics systems. In particular, a variable gain amplifier (VGA) embedded in an automatic gain control (AGC) system plays a crucial role in the front-end of wireless [1][2][3][4] and wireline [5][6] communication transceivers. As an example of a wireline application, a simplified block diagram of a power line communication (PLC) transceiver is presented in Figure 1.1. As shown, the VGA is used in the receiver portion of the transceiver.

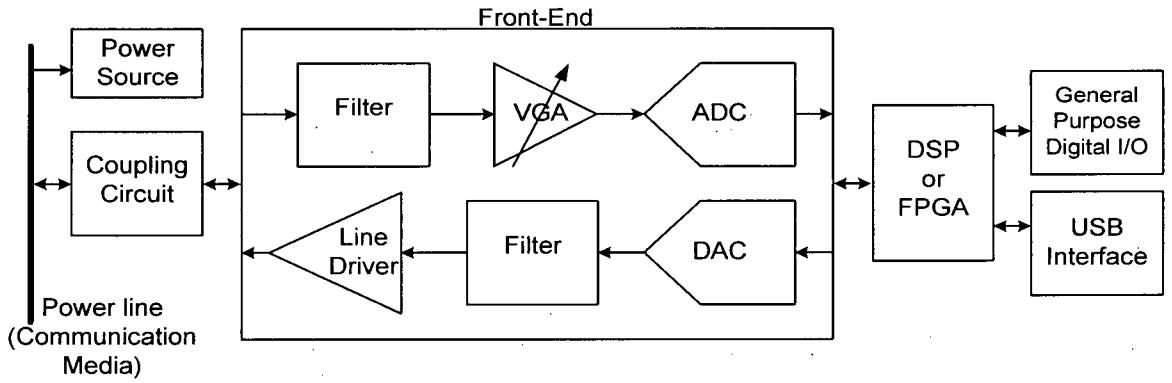


Figure 1.1 A simplified PLC transceiver layout.

In such applications, the VGA is required to control the amplitude and properly adjust the dynamic range of the signal for the following blocks such as ADCs. Basically, the VGA amplifies or attenuates the input signal to provide a known signal range for the next stage, e.g., input of the ADC. This adjustment facilitates optimizing the system performance and reducing

the overall circuit complexity.

Several VGA designs targeting a number of different applications have been described in the literature. In general, designing a VGA involves careful consideration of the trade-offs between different performance parameters. In many cases, the most important trade-off is between the gain range and the bandwidth of the VGA. In such designs, achieving a high gain range compromises the bandwidth and vice versa. One target application of this research is power line communications, in particular automotive PLC systems. The in-vehicle power line communication is relatively new and significantly more challenging environment as compared to other PLC media. Some standards for home PLC systems already exist; a bandwidth of 30MHz and a 42dB gain range [7] are required for some such systems. For automotive PLC systems, the communication protocols and channel specifications of the hostile vehicle power line environment are still under development [8][9] and are not standardized yet. Furthermore, there are possible applications for PLC systems with higher bandwidth [10] than the existing PLC networks. Therefore, as a research challenge, we aim for pushing the performance envelope of CMOS VGA architectures in terms of bandwidth, gain range, and power consumption. We achieve this by developing a new design technique based on combining a number of gain control methods.

In this thesis, a monolithic 140MHz digitally programmable VGA with 75dB of gain range is presented. To benefit from low power, low cost, and small area of CMOS integrated circuit (IC) technology, this design is implemented in a 0.18μm CMOS process. To take advantage of the many features of a DSP core this design is digitally controlled. The overall design consists of

three gain stages. As a proof of concept, a single gain stage with a gain range of 24dB has been fabricated. Based on the measurement results of this IC, the design of the gain stage is optimized and a three-stage 75dB VGA is realized. Each stage has a digitally tunable gain range of 25dB and a fine gain tuning of 2.5dB per step. Various issues that are addressed in this work include gain, bandwidth, linearity, noise, and power consumption.

This thesis is organized as follows. Chapter 2 gives an overview of VGA and summarizes the different VGA topologies that are reported in the literature. Chapter 3 introduces the architecture of the VGA core, its sub-circuits, and the gain control technique. In Chapter 4, simulation and measurement results for a monolithic 24dB single-stage VGA that is implemented in a 0.18μm CMOS process are provided. Chapter 5 presents the design of the proposed 75dB multi-stage VGA. The concluding remarks are provided in Chapter 6.

Chapter 2

BACKGROUND AND PREVIOUS WORK

Various VGA topologies have been proposed in the literature, each with its unique strengths and weaknesses. The choice of VGA architecture is dependent on the capability of the structure to meet the performance requirements of the application at hand. The key performance parameters of a VGA include gain (range and step), bandwidth, noise, and linearity.

In this chapter, the main performance parameters of a VGA are discussed. In addition, an overview of different VGA architectures, their important features and shortcomings are provided.

2.1 VGA Performance Parameters

The target application determines the required value of the performance parameters of a design. Reasonable insight into these parameters and their relationships is essential prior to the start of the design. This section provides background on the focal performance parameters of a VGA, namely noise, linearity, gain, and bandwidth.

2.1.1 Noise

In analog circuits, any undesired or random interference unrelated to the desired signal is considered noise. The importance of noise comes from the restriction it puts on the minimum

signal that can be successfully processed by the system. In most analog circuits, noise trades off with other metrics such as linearity, gain, or power of the system. A simple statistical model presenting noise is power spectral density (PSD) where the average power of a noise waveform is presented in one-hertz bandwidths [11].

There are three important sources of noise that dominate the noise contribution of active and passive components of any circuit. These are shot noise, flicker noise, and thermal noise. Shot noise is mostly a concern in bipolar transistors [12] and is generally negligible in CMOS technologies. Flicker noise, or pink noise, is a more significant source of noise in CMOS transistors. The spectral density of flicker noise resembles 1/f. Therefore, flicker noise is most significant at lower frequencies. For a detailed description and model of this type of noise, the reader is referred to [11]. The third significant noise source is thermal noise, which occurs in both the resistors and the channel of MOSFET transistors. The thermal noise of a resistor R has a PSD of [11]:

$$\overline{V_n^2} = 4\mathrm{kT}R\,\Delta f \qquad (2.1)$$

where k is the Boltzman's constant, T is the absolute temperature, and Δf is the bandwidth of interest. For MOS transistors, the thermal noise is typically represented by the thermal noise drain current. For a transistor with transconductance of g_m, this is given by [11]:

$$\overline{I_n^2} = 4\mathrm{kT}\gamma\,\mathrm{g_m} \qquad (2.2)$$

where γ is the thermal noise coefficient which is 2/3 for long channel transistors and larger for the deep submicron MOSFET [11]. Other kinds of thermal noise, such as resistive gate thermal noise, are usually negligible as compared with the previous noise sources and therefore can be ignored in noise calculations.

For performance comparison between different circuits, designers usually consider the total noise of the circuit (with less emphasis on each single noise source). Furthermore, to achieve a fair comparison between different circuits, the total noise can be presented as input-referred noise. This parameter is a conceptual quantity and indicates the level of corruption caused by the system's noise on input signal [11]. The input-referred noise presents the sensitivity of a system and therefore can provide a fair comparison between different circuits. A detailed description and analysis on noise presentation in circuits is provided in [11]. The signal-to-noise ratio (SNR) of the circuit, which is the ratio of signal power to noise power, can be calculated from the input-referred noise of the system. In some analog circuits, such as VGAs, noise figure (NF) is commonly used to characterize the noise performance of the circuit. NF is defined to be the ratio of SNR at the input of the system to SNR at the output.

The NF presentation of noise proves especially convenient when considering systems with cascade stages. According to Friis [13], the total NF of a cascade of stages is given by:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{A_1} + \frac{NF_3 - 1}{A_1 A_2} + \cdots + \frac{NF_n - 1}{A_1 A_2 \cdots A_{n-1}} \tag{2.3}$$

where NF_i and A_i are the NF and gain of the i^{th} stage. As can be seen from this equation, the NF of the first stage is the most dominant term and is the only term that directly adds to the total value. The NF of each subsequent stage is divided by the total gain of the previous stages. This makes the total NF highly dependent on the gain of the first stage. The noise performance of the subsequent stages is not as significant when the gain of the first stage is large. This fact comes into play for noise optimization of cascaded multi-block systems or multi-stage circuits such as the design in this thesis.

2.1.2 Linearity

Circuit linearity is another important performance parameter of a VGA. This parameter provides a measure for the amount of nonlinear distortion that the system adds to the input signal. In many designs, to simply obtain the small-signal response, a nonlinear system is treated as a linear system for a specific DC operating point. However, nonlinear distortion effects become more pronounced once a large AC signal is applied to the system and changes the transistors DC operating points. The nonlinear effects of the circuit usually determine the maximum signal that can be processed by the system.

A generic representation of a nonlinear system is:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots \qquad (2.4)$$

where y is the output, x is the input signal, and $\alpha 1$, $\alpha 2$, $\alpha 3$,... are the polynomial expansion coefficients. To characterize the nonlinearity of such a circuit, measurement metrics such as 1-dB compression point and third-order intercept point are used [14].

Practical amplifiers typically have a compressive behavior. As depicted in Figure 2.1, the 1-dB compression point is defined as the input power at which the gain of the circuit drops 1dB below its small signal asymptotic value.

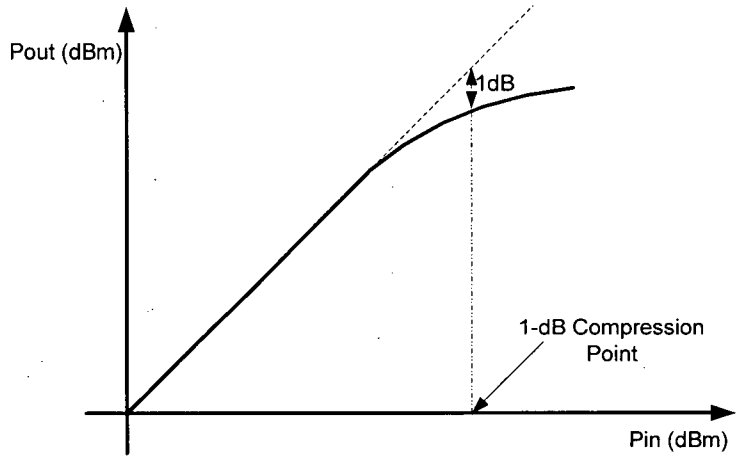


Figure 2.1 The plot of 1-dB compression point.

This phenomenon results from the fact that the output or gain of the system starts to saturate for a sufficiently large input signal. The 1-dB compression point can be calculated by the following expression [14]:

$$A_{1dB} = \sqrt{0.145\left|\frac{\alpha 1}{\alpha 3}\right|} \qquad (2.5)$$

where $\alpha 1$, and $\alpha 3$ are the first and third polynomial coefficients as previously presented in Equation (2.4).

The third-order intercept point is another measure of the linearity of the circuit. This nonlinear effect can be observed when two signals with small frequency separation are applied to a nonlinear system. In addition to higher order harmonics of the two signals, the output includes unwanted components, known as inter-modulation products (IMP), that appear close to fundamental tones and in the frequency band of interest (see Figure 2.2). The inter-modulation products consequently cause distortion.

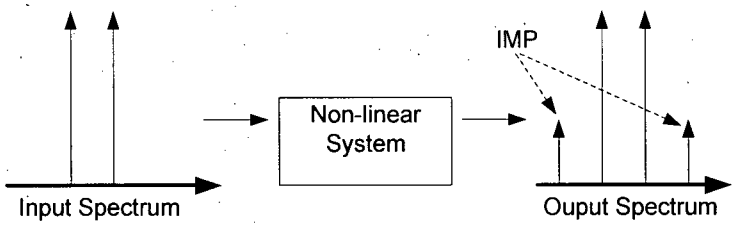


Figure 2.2 Illustration of inter-modulation product.

In a fully differential architecture, such as the design in this thesis, the even order harmonics are ideally eliminated due to the differential symmetry of the system, and the most severe distortion is caused by the third-order term, x^3. For small signals, the magnitude of the first order term is much larger than the inter-modulation terms. However, as the amplitude of the input signal increases, the third order inter-modulation term increases three times faster than the first order term as presented in Figure 2.3.

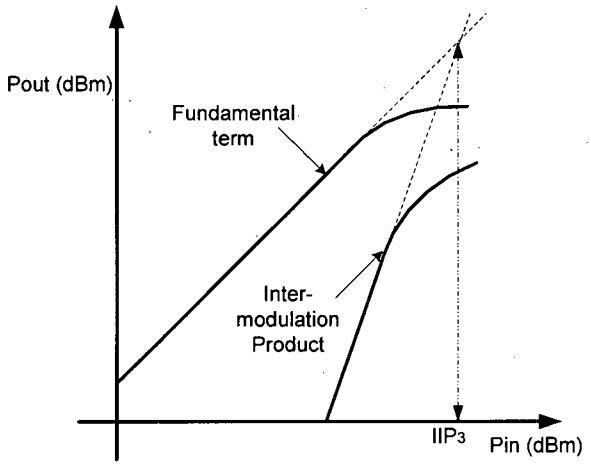


Figure 2.3 The Plot of IIP3.

As shown in Figure 2.3, the third-order input intercept point (IIP3) is the input power at which the third-order inter-modulation product, extrapolated from the small signal value, has the same

power as the extrapolated fundamental term. The following formula presents the expression for IIP3 in terms of first and third coefficients [14]:

$$A_{IP3} = \sqrt{\frac{3}{4}\left|\frac{\alpha 1}{\alpha 3}\right|} \qquad (2.6)$$

The IIP3 (dBm) can also be calculated experimentally and without extrapolation by applying a single-tone input and using the following expression [15]:

$$IIP_3 = \frac{P_{out} - P_{out,IM3}}{2} + P_{in} \qquad (2.7)$$

where P_{in} is the input power, P_{out} is the fundamental output power, and $P_{out,IM3}$ is the third-order inter-modulation output power.

The IIP3 parameter is used to measure the distortion level of a circuit. It is generally utilized as a means to compare the linearity of different systems.

It is also important to understand the overall distortion effects in systems with multiple cascaded blocks. The IIP3 of the whole system can be estimated with the following formula [14]:

$$\frac{1}{IIP_{3,tot}^2} \approx \frac{1}{IIP_{3,1}^2} + \frac{A_1^2}{IIP_{3,2}^2} + \cdots + \frac{A_1^2 \cdots A_{n-1}^2}{IIP_{3,n}^2} \qquad (2.8)$$

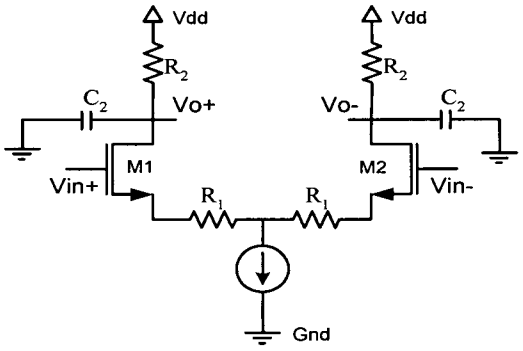
where $IIP3_i$ and A_i are the IIP3 and the gain of the i^{th} cascade stage. It can be observed that the linearity of the system depends on both the linearity and the gain of each stage; and more importantly, for a stage gain larger than unity, the overall linearity of the system is dominated by the latter stages. In contrast to the noise scenario for cascade stages, linearity decreases as the gain of the first stage increases. This indicates that there is a direct trade-off between noise and

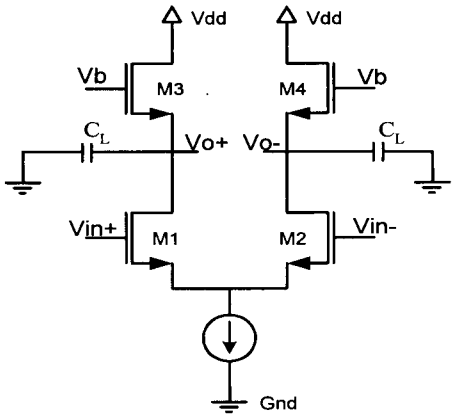
linearity and a compromise has to be made between these parameters to achieve the design requirements.

2.1.3 Gain and Bandwidth

As discussed in the previous section, for a cascade of stages the overall linearity and noise of the system are dependent on the gain of each stage. Furthermore, the gain variation in each stage has opposing effects on overall noise and linearity.

Another important parameter is the bandwidth of the amplifier, which is also dependent on the gain. Figure 2.4 shows two commonly used amplifier structures along with their gain and bandwidth equations.





$$|A_v| = \frac{R_2}{R_1 + 1/g_m}, \quad \omega_{-3dB} \approx \frac{1}{R_2 C_2}$$

$$|A_v| = g_m(r_{o2} \parallel r_{o4}), \quad \omega_{-3dB} \approx \frac{1}{C_L(r_{o2} \parallel r_{o4})}$$

Figure 2.4 Simple Amplifiers with their gain and bandwidth equations.

As can be observed, increasing the output resistance increases the gain. However, this increase will also reduce the bandwidth of the amplifier. This shows the trade-off between the gain and the bandwidth of a simple amplifier. This relationship gets more complicated for more complex

amplifiers; however, the inverse relationship almost always exists and compromises have to be made to meet the system requirements.

Depending on the application requirements and the amplifier structure used, there are different methods available to enhance the gain and bandwidth performance of a system. Multi-stage amplifiers can be used to increase the gain at the cost of power dissipation and bandwidth reduction. To achieve lower power dissipation and better frequency response for the same gain of a multi-stage amplifier, a cascode structure can be used. The headroom limitation of this design can be avoided by using a folded cascode structure at the cost of gain and bandwidth [11]. Other techniques, such as capacitive neutralization, have been introduced to increase the bandwidth of multi-stage amplifiers [16]. Also, gain-boosting techniques have been employed to enhance the gain performance of amplifiers [17]. Some of these methods have been used for the VGA design proposed in this thesis and further discussion is provided in the following chapters.

2.2 VGA Architectures

Automatic gain control (AGC) circuits are essential in many systems where wide gain range variation of input signal amplitude can result in loss of data and eventually a system malfunction. The AGC circuit performs signal amplitude adjustments in order to minimize the gain range requirement of the following stages. The VGA is the main component of an AGC circuit. In an AGC, the gain of the VGA is controlled in response to the amplitude of the input signal leading to a constant-amplitude output signal. To maintain the settling time of an AGC loop constant and independent of input signal level, the gain of the VGA is required to be an exponential function of the gain control signal, which means a VGA with a dB-linear control gain characteristic is essential [18].

There are many ways to realize a linear-in-dB VGA. However, VGAs can be categorized into two major groups based on their control circuitry, namely, VGAs with analog or digital control circuits. These two groups are described in the following subsections.

2.2.1 Analog VGA

Conventional VGA circuits are mostly based on analog control circuits. Figure 2.5 [19] demonstrates the use of an analog control VGA in a conventional AGC loop.

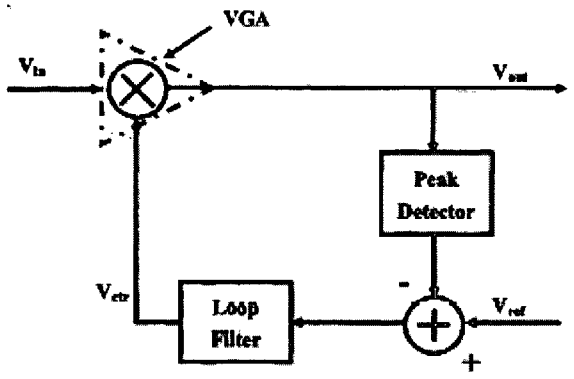


Figure 2.5 Conventional AGC block diagram [19].

Traditional analog VGAs are mostly based on Gilbert multiplier cells implemented in bipolar technology. Due to natural exponential I-V characteristics of the bipolar devices, high gain range and dB-linear gain variation can be attained in these circuits [20]. However, these designs are not quite portable to CMOS technology due to square-law/linear characteristic of MOSFETs. The alternative BiCMOS technology is not always a feasible solution due to the high production costs.

In the late 1980s, bipolar control techniques were applied to CMOS technology by utilizing parasitic bipolar transistors [21]. The advantage of this technique is that parasitic lateral and vertical bipolar junction transistors can be implemented in the standard CMOS technology and

no additional IC processing steps are required. However, these devices have limited bandwidth and their performance characteristics are not well defined, making them unsuitable for practical purposes [22].

As a result, many topologies were investigated in attempts to realize linear-in-dB function employing MOS only transistors. One approach is to make use of the exponential relationship between gate voltage and drain current of these devices in the weak inversion or sub-threshold region. The master-slave control technique using MOS transistors biased in the sub-threshold region in [1] achieves a dB-linear gain range of approximately 20dB per stage. However, this topology is also not very practical as it puts limitations on the acceptable input signal amplitude, exhibits poor high-frequency response, and requires extensive biasing circuitry.

The other possibility for generating an exponential function in all CMOS processes is based on approximation techniques. There are several approximation methods/functions proposed to mimic the desired exponential behavior based on MOS transistors operating in their natural square or linear regions. One such method, which was first proposed by [23], is based on the following approximation:

$$e^{2x} \approx \frac{1+x}{1-x} \qquad (2.10)$$

where x presents an independent variable. Various VGA topologies have incorporated such approximation techniques to implement CMOS circuits achieving dB-linear characteristics [24][25][26][27]. For example, the control circuitry in [26] is an exponential current-to-voltage converter (or pseudo-exponential voltage generator) based on the above function. The exponential control voltage generated is applied to a CMOS Gilbert style multiplier to obtain an

exponential variation in the overall gain range. This is only one typical solution using this approximation method. There are many other configurations available [24][25].

Taylor series approximation is another method used to generate an approximate exponential function with MOS transistors biased in the saturation region. Neglecting the higher order terms, the second-order Taylor series approximation can be expressed as [2]:

$$e^x \approx 1 + x + \frac{1}{2}x^2 \qquad (2.11)$$

where x is an independent variable. There are also several configurations proposed based on Taylor series approximation [2][27][28]. In general, the CMOS VGA, based on pseudo-exponential and Taylor series approximation functions, does not offer a high gain range. Thus, the high gain range reported for some of these architectures is sometimes achieved at the cost of significant gain error [29].

A new approximation exponential equation recently presented by [3] is:

$$f(x) = \frac{[k + (1 + ax)^2]}{[k + (1 - ax)^2]} \qquad (2.12)$$

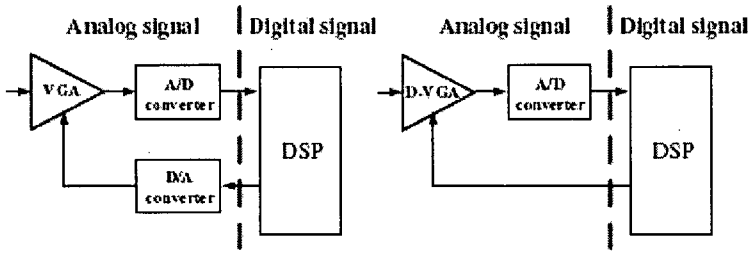
where k and a are constants and x is an independent variable. The VGA topology based on this equation [3] is reported to provide significant improvement in terms of gain range in comparison to previous approximation methods. However, the bandwidth of this VGA varies significantly as gain changes. The bandwidth changes from below 40MHz for the highest gain to more than 1GHz for the lowest gain.

Another proposed CMOS analog VGA architecture is based on signal summing techniques. The signal summing technique proposed in [4] utilizes two types of gain compensation techniques to achieve linear-in-dB gain control. This topology achieves high frequency bandwidth of up to 380MHz and improved noise and linearity performance. However, the gain range per stage is only 20dB and even with the two gain compensation techniques utilized, the gain error is reported to be as large as 3dB.

Many of the analog VGA architectures can also be implemented as digitally controlled VGAs. There are also topologies that are specific to digitally controlled VGAs. The following section presents some of these digital VGA topologies.

2.2.2 Digitally Controlled VGA

As mentioned before, in most of today's modern mixed-signal applications, a VGA is usually required to maintain a reasonable signal level at the input of the ADC. Once in the digital domain, complex data manipulation and precise control gain computation can be performed using digital signal processing (DSP) techniques. Hence, in these mixed-signal ICs, the gain control part of the AGC can be implemented in the digital part of the IC. Now, if an analog-controlled VGA is used, the digital control output from the DSP circuit is required to be converted to an analog signal using a digital-to-analog converter (DAC) as shown in Figure 2.6 (a) [30]. However, if a digitally controlled VGA is used, the VGA can be directly controlled by the digital bits transmitted from the DSP core. This configuration, as shown in Figure 2.6 (b) [30], reduces the circuit complexity and simplifies the digital to analog interface. Thus, a digitally controlled VGA, or a programmable gain amplifier (PGA), has become increasingly popular since the late 1990s to simplify the interface with the digital core [31].



a) Analog AGC. b) Digital AGC

Figure 2.6 AGC interface [30].

One common topology is based on an op-amp with resistive array gain stages. This technique is not favorable in analog VGA architecture because it is difficult to generate linear variable analog-control resistors. However, this technique is popular in digitally controlled VGAs. A conventional resistive array VGA is composed of an amplifier and resistor ladders as presented in Figure 2.7 [6].

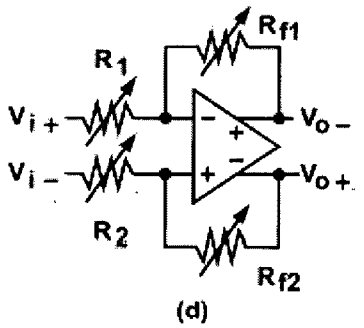


Figure 2.7 Variable resistive array VGA topology [6].

The gain is determined by the ratio of R_{f1}/R_1 and R_{f2}/R_2 and can be controlled by changing any of these resistors: R_{f1}, R_1, R_{f2}, and R_2. This simple gain control system can be implemented in

different ways. One approach is to use a voltage-mode op-amp, and change R_f to vary the gain as presented by Figure 2.8 [3].

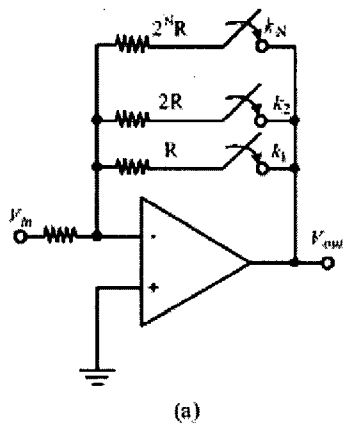


Figure 2.8 Digitally controlled variable feedback resistive array VGA [3].

The advantage of this design is its simplicity and the ease of implementation of the feedback resistive network. However, the variation in the feedback resistor R_f results in the feedback factor and output pole variation and consequently bandwidth variation. Compensation techniques have been proposed to compensate for the variation of the bandwidth throughout the gain range [5]. However, the highest bandwidth reported is less than 12MHz with 0.5 dB gain error when extra compensation circuitry is utilized [5].

Another approach is to use a high-gain current-mode amplifier with a low input impedance. As presented in Figure 2.9 [6], the gain is varied by changing the resistors R_1 and R_2.

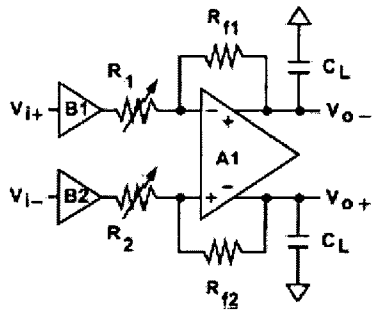


Figure 2.9 Digitally controlled variable input resistive array VGA [6].

In this method, R_{f1} and R_{f2} are fixed resulting in a constant closed loop bandwidth throughout the gain range. A fairly constant bandwidth of 125MHz is achieved in [6], but the gain range reported is limited to 19dB with a gain error of 1dB.

Aside from the different resistive feedback techniques mentioned above, there are other topologies that use changing the resistive array or modifying the number of op-amp stages. One topology, presented in [32], is based on switched capacitors. In this structure, the resistance array is replaced by a variable capacitor array in a two stage VGA. The resulting low power VGA achieves a dynamic gain range of 24 dB, but the highest bandwidth achieved utilizing this technique is typically limited to few tens of MHz.

Another variation of resistive feedback topology uses current division network blocks instead of R-2R ladder resistor structure. This technique proposed by [33] is based on the inherent linear MOS-only current division technique first presented in [34]. Several variations of this technique are also proposed [35][36], however, the bandwidth is again limited to a few tens of MHz.

In general, VGA designs, such as the ones reported in [6] and [5] that use amplifiers with feedback, are not suitable for applications requiring both high bandwidth and wide gain range. It is difficult to achieve an amplifier with a large gain bandwidth product. This result in either low frequency bandwidth, small gain range, or significant variation of the bandwidth in these architectures.

Another common topology is based on a source-degeneration differential pair with a resistive load. This topology can be realized with both analog and digital control signals. Figure 2.11 presents a basic analog realization of this topology where a transistor in the triode region is used as a variable source-degeneration resistor. Analog control voltage, Vc, applied to this transistor varies the value of the variable resistor and therefore changes the transconductance of the source coupled differential pair to adjust the gain. For large input signals, a large source-degeneration resistor is required to achieve high linearity and low gain, and for low input signals, a small resistor is needed to provide low noise distortion and high gain for the system. Using this technique, a small gain range variation is achieved, but it is difficult to achieve a wide resistance variation for a high gain range with the use of only one transistor.

A simple digital realization of this topology is achieved by replacing the triode region transistor (or the load resistor) with a digital variable resistor. The gain of this amplifier can vary by changing either the source-degeneration resistor or the load resistor. The use of the source-degeneration resistor makes this topology very popular for applications where high linearity is required.

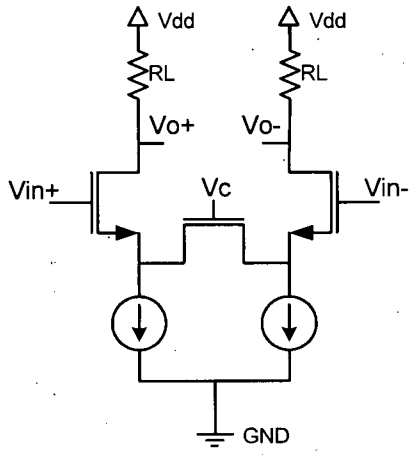


Figure 2.10 Analog source-degeneration differential pair.

More sophisticated and advanced realizations have been provided by Rijns [37], Wang [30], and Mostafa [17]. The overall performance of these circuits are better as compared with the previously introduced digitally controlled VGA designs. In this thesis, some of the techniques used in the previous structures with source-degeneration [17][30][37] have been improved and combined to achieve a VGA architecture with a high gain range (75dB), high bandwidth(few hundred's of MHz), and relatively low bandwidth variation. The details of the proposed VGA are presented in the following chapter.

Chapter 3

VGA DESIGN CONSIDERATION

There are many potential design solutions for a variable gain amplifier. In the previous chapter, a number of these design topologies were reported. Furthermore, the advantages and drawbacks of these topologies were outlined. In this chapter, a design based on the source-degeneration structure, targeted for automotive PLC applications, is presented. The VGA circuit design approach, source-degeneration core, purpose of different sub-circuits, and gain control technique for this VGA architecture are explained in the subsequent sections.

3.1 Design Architecture

Among various digitally controlled VGA design methods, the source-degeneration topology with inherent low distortion characteristic has the potential to achieve a wide gain range and high bandwidth.

The source-degeneration technique previously presented in [37] provides a fairly constant 3-dB bandwidth for the entire gain range. However, the gain range is limited to 14dB. A higher gain range is provided by another version of the source-degeneration topology given in [17]. However, this method results in a high bandwidth variation. In addition, these two techniques require a large number of switches for controlling the gain of the system. In this work, to take advantage of low bandwidth variation presented by the changing R_S, and high gain range

provided by changing R_{Ld}, these two techniques have been combined. The resulting architecture achieves high gain range with lower or equal number of control signal switches, and low bandwidth variation.

The following sections presents the architecture of the VGA core and sub-circuits as well as gain control technique implemented.

3.1.1 VGA Core

The core of the VGA designed in this work is based on the source-degeneration topology. A simple source-degenerated differential amplifier is shown in Figure 3.1.

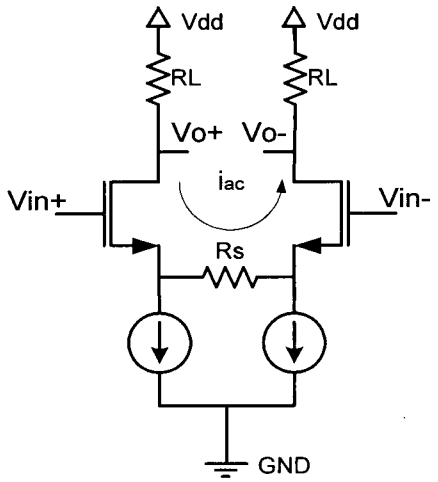


Figure 3.1 Basic source-degeneration differential amplifier with resistive loads.

In this configuration, the input voltage signal is converted to an output current signal as given by Equation (3.1). This current flows through R_L.

$$i_{ac} = \frac{v_{in}}{R_S + \frac{2}{g_m}} \qquad (3.1)$$

The gain of this circuit is then given by Equation (3.2), (assuming that the output impedance of the circuit is much larger than R_L).

$$A_V = \frac{2R_L}{R_S + \frac{2}{g_m}} \qquad (3.2)$$

As it can be seen in Figure 3.1, the architecture incorporates the use of two constant current sources at the source of the input transistors. For the small signal differential input signal of v_{in+} and v_{in-} , the small signal current of i_{ac} flows through resistor R_S. Because of the two constant current sources, the small signal drain current of the input transistors are therefore I_b-i_{ac} and I_b+i_{ac} . This difference in the drain current of the input transistors results in a small change in the V_{gs} of the two input transistors and ultimately causes g_m variation. Furthermore, g_m is a process dependent parameter with dependence on the mobility, transistor size, and threshold voltage. This parameter therefore cannot be precisely controlled. As can be seen from the gain equation, the gain of the circuit is dependent on the g_m of the input transistor. Therefore, as a drawback of the architecture, the variation in g_m causes inaccuracy in the gain of the amplifier.

To reduce gain error and enhance the gain of the amplifier, the effect of g_m variation needs to be reduced and g_m should be increased. This enhancement can be attained by the increase of g_m through transistor size and/or bias current increase. However, this is not a feasible solution due to the increase in power consumption and area. An alternative solution to increase g_m is to use a g_m-boosting circuitry.

3.1.2 G_m-Boosting

Figure 3.2(a) presents a g_m-boosting structure. This circuit is proposed to increase the effective transconductance, g_m, of the circuit and hence minimize the dependence of the gain of the circuit on the *gm* of the input transistors. The overall transconductance, G_m, is defined as the ratio of the small signal output current, i_{out} to the input voltage, v_{in}. Figure 3.2 (b) is provided to clarify how the architecture provides g_m-boosting.

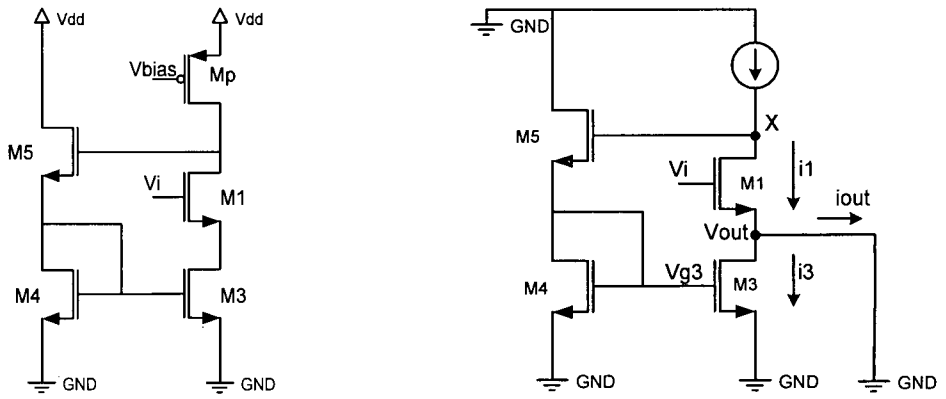


Figure 3.2 (a) *Gm*-boosting circuitry. (b) Model to calculate *Gm* of the circuit.

The total G_m of this structure can be derived as follows.

$$G_m = \frac{i_{out}}{v_i}$$

$$i_{out} = i_1 - i_3$$

$$i_1 = (v_i - v_{out})g_{m1} \ , \ v_{out} = 0 , \ i_1 = v_i g_{m1}$$

$$i_3 = v_{g3} g_{m3}$$

$$v_X \cong v_{g3}$$

$$v_X = -i_1 R_O \ , \ v_{g3} = -i_1 R_O$$

$i_3 = -i_1 R_O g_{m3}$

$i_{out} = (i_1 + i_1 R_O g_{m3})$, $i_{out} = i_1(1 + R_O g_{m3})$

thus,

$$G_m = \frac{i_{out}}{v_i} = g_{m1}(1 + R_O g_{m3}) \qquad (3.3)$$

As can be seen from the Equation (3.3), the transconductance of this circuit is boosted by $1+g_{m3}R_O$, where g_{m3} is the transconductance of transistor M_3 and R_O is the equivalent output impedance at node X.

The result of adding g_m-boosting circuitry to the differential source-degenerated amplifier is presented in Figure 3.3. As mentioned before, the problem for the basic amplifier structure is caused by the small difference in the current flow through the input transistors resulting in the difference in their respective V_{gs}. The modified circuit with g_m-boosting enhancement eliminates this effect.

As can be seen from Figure 3.3, the current through each input transistor is fixed by the constant current source, I_b. These input transistors now act as source followers, or level shifters, buffering input signal voltages to the two ends of the resistor R_S. That is, any change in the input voltage is copied to the source of the transistors and, therefore to the first order, drain currents and V_{gs} of the input transistors are kept constant. Now the copied voltages to the source of the transistors result in an AC current through the resistor R_S. This current is determined only by the differential input voltage and value of R_S resistor. The current then adds to and/or subtracts from the DC current flowing through the two transistors M_3 and M_4 as I_b-I_{ac} and I_b+I_{ac}. The currents of M_3 and M_4 are then mirrored to the output branch transistors, M_7 and M_8.

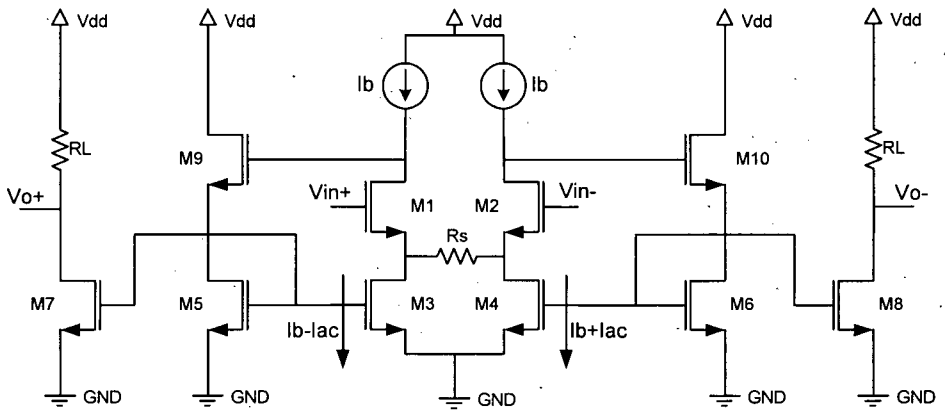


Figure 3.3 The differential source-degeneration with gm-boosting enhancement circuitry.

The use of g_m-boosting circuitry results in an increase in the effective transconductance of the differential pair, and consequently provides higher gain and minimizes the gain error caused by g_m variations. In addition, the dc value of gate-source voltage of the input transistors, and therefore their bias currents, is roughly independent of the input voltage. The input voltage difference is only seen across R_S and is then copied to the output. Thus, the gain is only dependent on the value of output load, R_L, and source-degeneration resistor, R_S. The gain of the final circuit is given by:

$$A_V = N\frac{R_L}{\frac{R_S}{2}} \qquad (3.4)$$

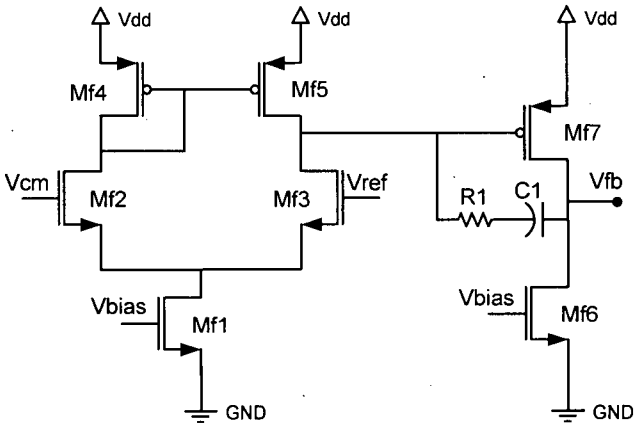
Where N is the current mirror ratio of transistor M_3 to M_7.

3.1.3 Common-mode Feedback

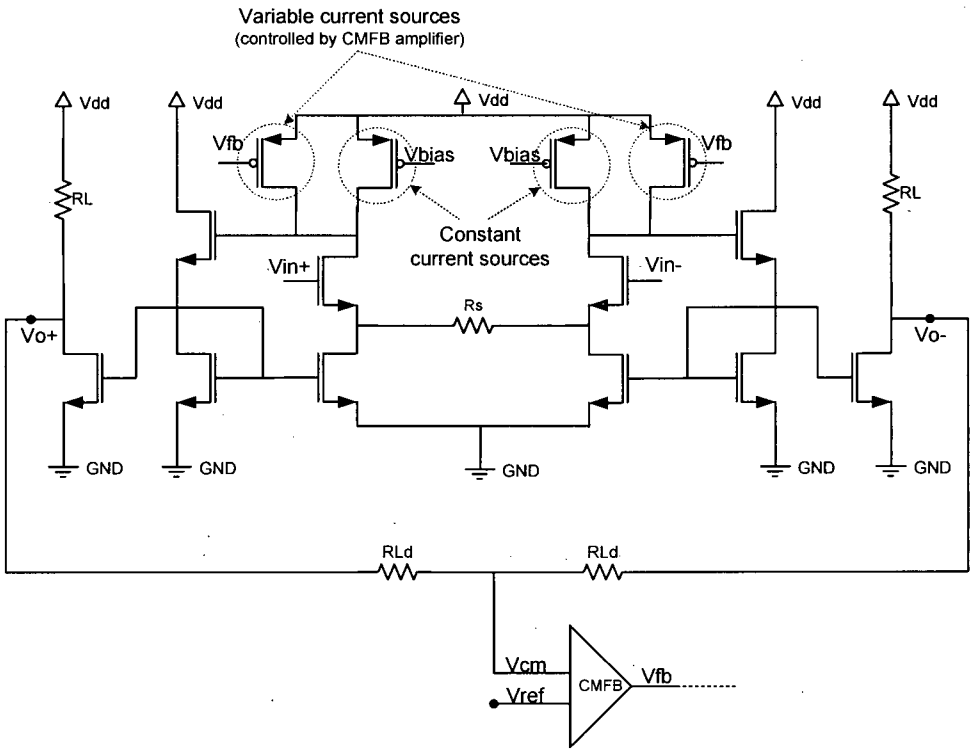
Before proceeding to the gain control methodology of this amplifier structure, the common-mode feedback (CMFB) circuit used in this work is presented. The common-mode (CM) output voltage of a fully differential amplifier is very sensitive to device properties and mismatch [11].

A CMFB structure is therefore necessary to maintain the CM voltage level of the output signal at a specified value. There are many possible solutions to implement the CMFB circuit of differential amplifier [11]. The CMFB circuit functions by sensing the CM output level, comparing it with a reference level, and then adjusting the biasing circuitry to maintain the desired DC output level. The CM voltage can be sensed by connecting two capacitors or resistors in series between the two output nodes. However, using capacitors changes the output pole location and consequently the bandwidth. Although using resistors also contributes to the bandwidth or gain reduction, they are used in this work because they can also serve as gain control elements. This gain control approach is further discussed in the next section.

The CMFB circuit is a conventional two stage differential-to-single-ended amplifier with *RC* compensation circuitry, shown in Figure 3.5 (a). The CM voltage is compared to a reference voltage, V_{ref}, by a differential op-amp and fed back to the main amplifier. The output of CMFB op-amp is connected to the input current sources of the core amplifier circuit. The current sources of the core amplifier, presented as I_b in Figure 3.3, consist of two parts: a constant current source and a variable current source. As illustrated in Figure 3.5 (b), the variable current source is controlled by the CMFB loop output. The change to the output CM is detected and the bias current of the variable current source of the main circuit is adjusted accordingly to minimize the CM variation.



(a)



(b)

Figure 3.4 (a) Common-mode feedback circuitry. (b) Main differential amplifier with CMFB controlling part of the main current sources.

3.1.4 Gain Control

As mentioned in the previous section, the resistors added between the output nodes for CM sensing can also be used for gain tuning. The gain formula, previously given in Equation (3.4) should be modified as below to include the effect of added resistance, R_{Ld}:

$$A_V = N\frac{R_L // R_{Ld}}{\frac{R_S}{2}} \qquad (3.5)$$

The gain can be adjusted by changing N, or the resistor values, R_L, R_{Ld}, and R_S. The method of gain tuning by changing the current mirror ratio is presented in [30], where a fully differential source-degenerated amplifier with constant source-degeneration resistor utilizes an array of current mirrors. The current mirror blocks are digitally controlled to determine the gain of the VGA. This technique provides a high gain range and a moderate gain accuracy. However, for high-frequency applications, the large capacitance resulting from the array of current mirrors limits the bandwidth of the VGA.

The gain can also be controlled by changing the value of resistors. To achieve an approximately constant bandwidth for the entire gain range, only the source-degeneration resistor, R_S, should be changed. A digital realization of this topology is presented in [37], where a constant bandwidth of 15MHz is reported. However, the gain range resulted from changing this resistor is limited. For example the gain range in [37] is limited to 14dB. To achieve higher gain range, R_S can be kept constant, and R_L and R_{Ld} can be simultaneously changed as introduced in [17]. The gain is controlled by selecting the output branch including R_L, R_{Ld}, and switch transistors. This technique achieves a high gain range and a relatively high bandwidth. However, changes in

resistors R_L and R_{Ld} could change the output pole location and consequently results in variation in the bandwidth. For high gain range, this bandwidth variation could be large.

Using output resistor, R_L, for gain selection introduces another problem due to the effect of R_L variation on the operation of CMFB circuitry. The feedback loop implemented is designed to keep the CM of the output at a constant level. However, if the value of the load resistance, R_L, is significantly changed to achieve high gain range, the voltage drop across R_L will drastically change the CM level. To maintain the output CM, the CMFB loop will have to considerably change the biasing of the main differential branch. However, unlike changing R_L, the changes in the resistors between the output nodes, namely R_{Ld}, to the first order does not affect the CM level. Therefore, to keep the biasing levels fairly constant, R_{Ld} should be used for gain control.

To take advantage of low bandwidth variation presented by the work in [37], and high gain range provided by the technique in [17], these two techniques have been combined in this work. In the combined architecture, both source-degeneration resistance and added output resistors are changed simultaneously. The source-degeneration resistance is used to achieve lower bandwidth variation, and the added resistors between the output nodes are used to provide higher gain range. The first source-degeneration resistance handles the coarse tuning, and the output resistance handles the fine gain control. The proposed combined technique, which is further described in the next chapters, achieves high gain range and low bandwidth variation with equal and/or lower number of control switches.

As a proof of concept, a single-stage 24dB VGA with g_m-boosting circuitry based on the proposed gain control technique is designed. This single-stage design has been fabricated in a 0.18μm CMOS technology. The IC is tested and measurement results are obtained. The gain control method, circuit simulations, and measurement results of the fabricated design are presented in the Chapter 4. The implementation details of the final 75dB VGA design is based on the results obtained from the one-stage fabricated IC. The information regarding the final design is provided in Chapter 5.

Chapter 4

SINGLE-STAGE VGA: DESIGN, LAYOUT AND TESTING

A 24dB single-stage VGA designed as a proof of concept is presented in this chapter. Section 4.1 begins with the proposed design for the single gain stage VGA. In Section 4.2, the simulation results for the VGA, designed in a 0.18μm CMOS process, are presented. Section 4.3 describes the layout technique and implementation issues for the fabricated design. The last section, Section 4.4, describes the test method and presents the measurement results of the fabricated IC.

4.1 Single-stage VGA Design

The schematic-level diagram of a 24dB single-stage VGA design implemented in this work is presented in Figure 4.1.

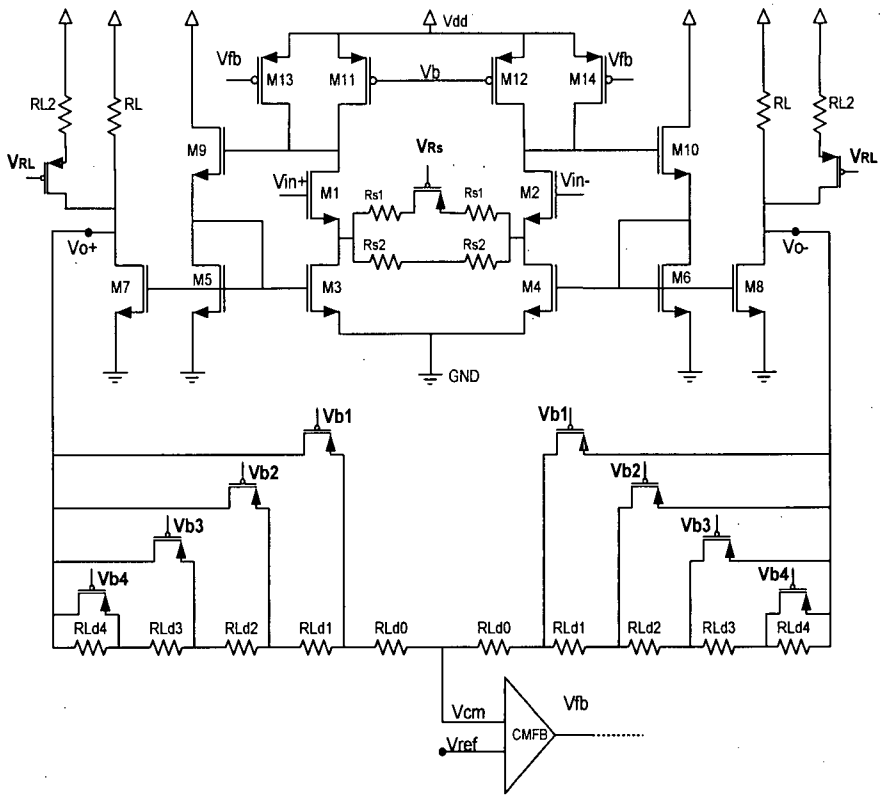


Figure 4.1 Proposed single-stage 24dB gain range VGA.

The gain is controlled by using the MOS switches to vary the source-degeneration resistor, the load resistor, or the added resistor between the differential output nodes. These resistors can set the 24dB VGA gain, ranging from −10dB to 14dB, as previously derived by Equation (3.5):

$$A_V = N\frac{R_L // R_{Ld}}{\frac{R_S}{2}} \qquad (4.1)$$

It is worth mentioning that in multi-stage VGA design, coarse and fine gain tuning are usually taken care of in different stages. However, since this VGA is only one stage, it includes both coarse and fine gain tuning control in this one stage. The source-degeneration resistor and output load resistors are dedicated for coarse tuning. The added resistors between the output branches are dedicated for fine gain control. The source-degeneration resistor and output load resistor each have one control signal, V_{Rs} and V_{RL}, respectively. As shown in Figure 4.1, the added resistors

between the output nodes are controlled by four switch voltages, V_{b1}, V_{b2}, V_{b3}, and V_{b4}. Table 4.1 summarizes the value of each tuning resistor based on the status of the MOS switches.

R_s	V_{Rs} (V)
$2X(R_{s1} \| R_{S2})$	1.8
$2X\ R_{S2}$	0

(a)

R_L	V_{RL} (V)
$R_{L1} \| R_{L2}$	1.8
R_{L1}	0

(b)

R_{Ld}	V_{b1} (V)	V_{b2} (V)	V_{b3} (V)	V_{b4} (V)
$R_{Ld0}+R_{Ld1}+R_{Ld2}+R_{Ld3}+R_{Ld4}$	1.8	1.8	1.8	1.8
$R_{Ld0}+R_{Ld1}+R_{Ld2}+R_{Ld3}$	1.8	1.8	1.8	0
$R_{Ld0}+R_{Ld1}+R_{Ld2}$	1.8	1.8	0	1.8
$R_{Ld0}+R_{Ld1}$	1.8	0	1.8	1.8
R_{Ld0}	0	1.8	1.8	1.8

(c)

Table 4.1 (a) Source-degeneration resistor values based on V_{Rs} switch. (b) Load resistor values based on V_{RL} switch. (c) Added resistor between the output nodes values based on V_{b1}, V_{b2}, V_{b3}, and V_{b4} switches.

In terms of coarse tuning, the gain range is divided into three main sections: high, medium, and low gain range. One of the coarse tuning signals, V_{RL}, is designed to switch the gain of the VGA between the high and medium range. The other coarse tuning signal, V_{Rs}, is intended to further extend the range to the low gain section. Once in a high, medium, or low gain range section, the gain can be finely tuned, in 2dB steps, using the other four control signals, V_{b1}, V_{b2}, V_{b3}, and V_{b4}. The gain control signal setting for the 24dB gain range is summarized in Table 4.2.

Gain (dB)	V_{Rs} (V)	V_{RL} (V)	V_{b1} (V)	V_{b2} (V)	V_{b3} (V)	V_{b4} (V)
14	1.8	1.8	1.8	1.8	1.8	1.8
12	1.8	1.8	1.8	1.8	1.8	0
10	1.8	1.8	1.8	1.8	0	1.8
8	1.8	1.8	1.8	0	1.8	1.8
6	1.8	1.8	0	1.8	1.8	1.8
4	1.8	0	1.8	1.8	1.8	1.8
2	1.8	0	1.8	1.8	1.8	0
0	1.8	0	1.8	1.8	0	1.8
-2	1.8	0	1.8	0	1.8	1.8
-4	1.8	0	0	1.8	1.8	1.8
-6	0	0	1.8	1.8	1.8	0
-8	0	0	1.8	0	1.8	1.8
-10	0	0	0	1.8	1.8	1.8

Table 4.2 Gain control signal setting for the 24dB gain range.

4.2 Simulations Results

In this section, simulation results for the single-stage VGA designed in a 0.18um CMOS technology are presented. TSMC Foundry provided design kits, and the Spectre/SpectreRF simulator in the Cadence design environment have been utilized to perform the simulations. Several analysis engines such as DC, AC, Transient, Noise, Periodic Steady State (PSS), and Quasi-Periodic Steady State (QPSS) are used to obtain the required performance metrics. The following subsections present the test bench used and performance parameters obtained, such as frequency response, gain range, bandwidth, noise, and linearity.

4.2.1 Simulation Test Bench

The diagram in Figure 4.2 presents the test bench used to simulate the 24dB VGA design in this work.

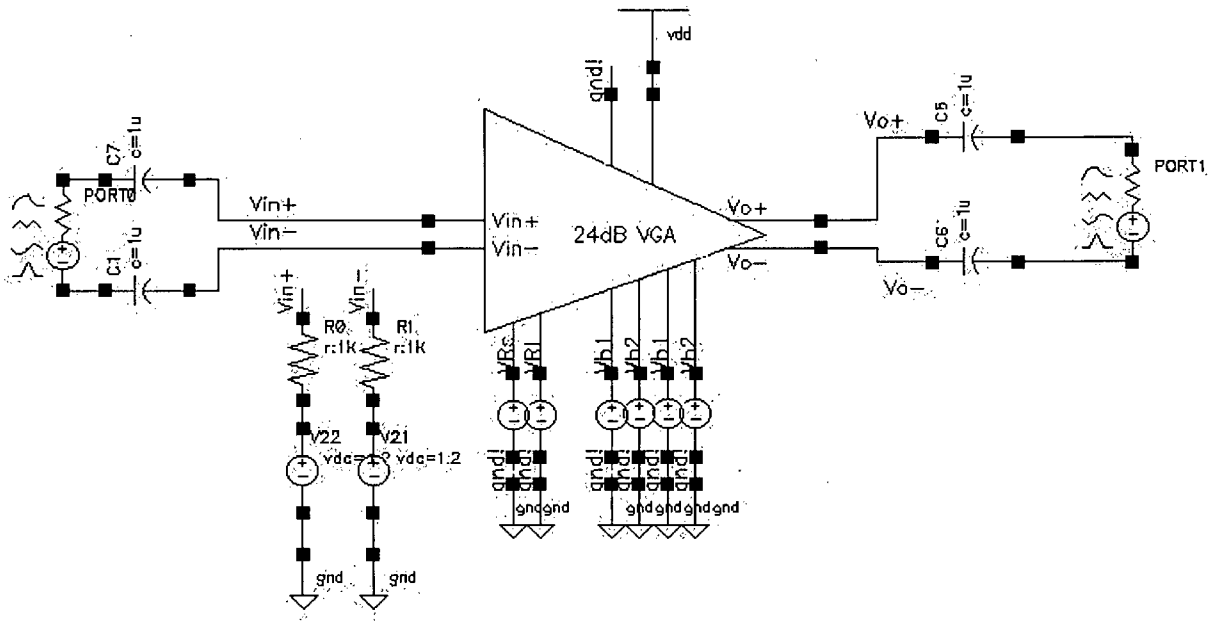


Figure 4.2 The 24dB VGA test bench.

This test bench is used to obtain noise and linearity performance of the VGA using Noise, PSS, and QPSS analysis. The differential output is terminated by a high impedance port since, in reality, this output is connected to the high impedance input gate of the next VGA stage or the output buffer. To obtain other performance parameters using DC, AC, and Transient analysis, the test bench is slightly modified from Figure 4.1. The ports are removed and the differential signal sources, AC or DC, are directly connected to the inputs. Each differential output branch is then terminated by a high impedance in parallel with a 200fF capacitor load, which represents the gate of the next stage. This is a reasonable load since in the final multi-stage design this VGA is will be connected to the gate of the next VGA or the gate of a buffer driving a higher capacitor of about 5pF.

4.2.2 Frequency Response

The simulated frequency response of the 24dB VGA for all the gain settings is shown in Figure 4.3. The reasonably flat frequency response of each gain state indicates the small gain variation over the entire frequency range of interest as desired.

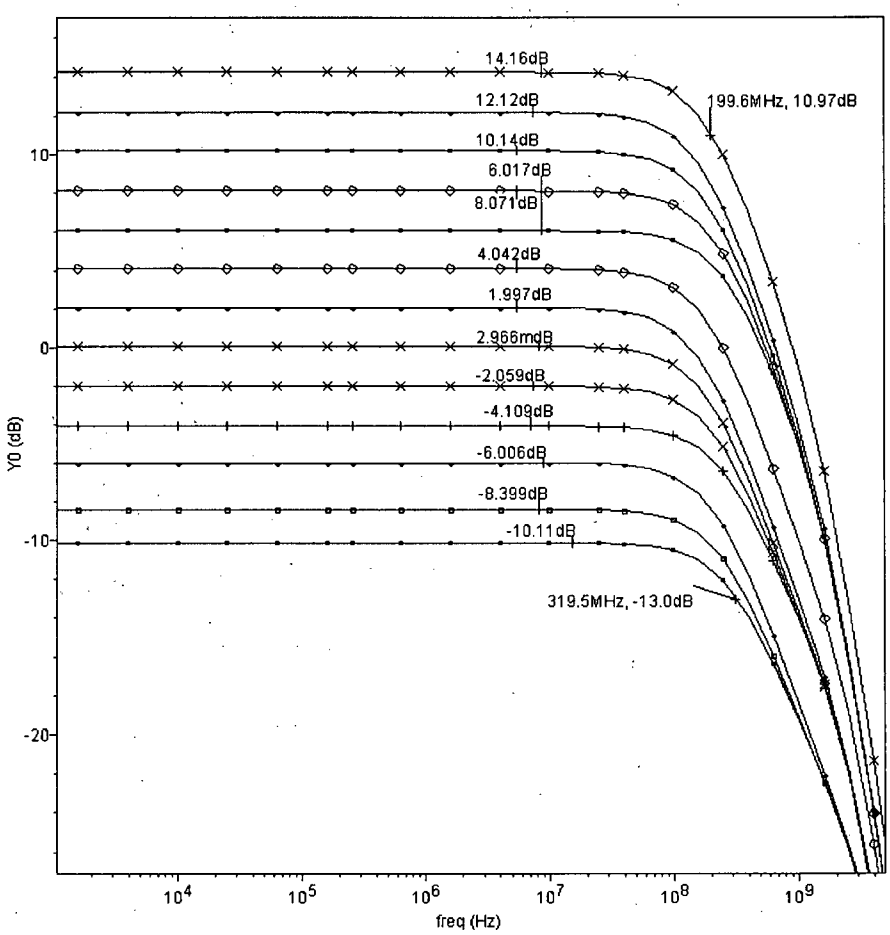


Figure 4.3 Frequency response of the VGA for all gain settings.

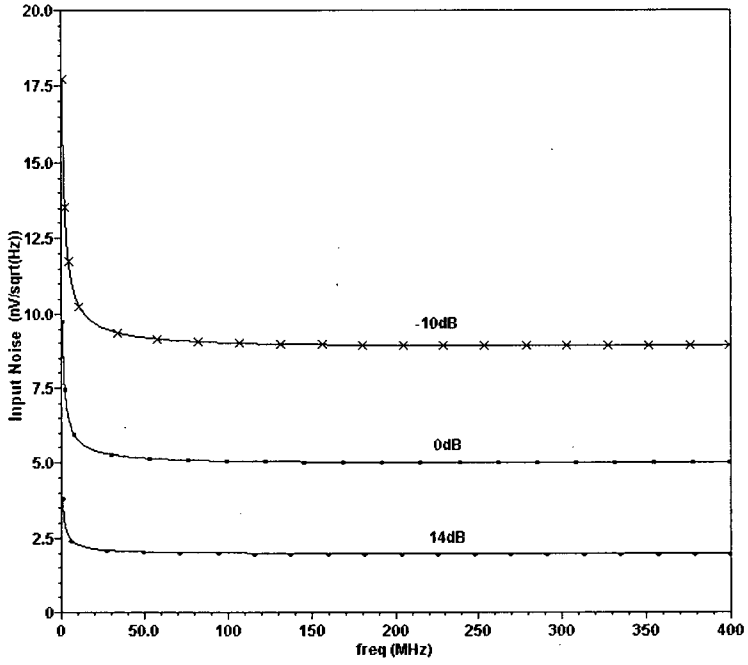
The gain range and bandwidth of the VGA can be extracted from the plots of Figure 4.3. The gain is linear in dB and varies from −10dB to 14dB in 2dB steps. The gain error is measured to be less than ±0.4dB. As can be seen from the plot, the available 3dB frequency bandwidth of this VGA is more than 199MHz while driving a 200fF capacitor load. The bandwidth varies from

approximately 199MHz to 320MHz, for a maximum gain of 14dB to the minimum gain of −10dB, respectively.

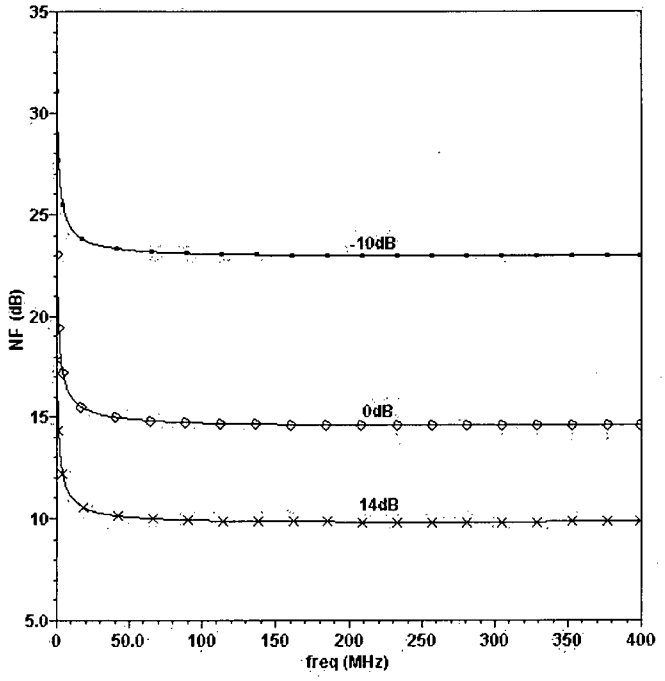
4.2.3 Noise

Noise is another important characteristic that has been evaluated using the Noise analysis engine. As was stated in the background section, the noise performance can be presented using noise figure or input-referred noise spectral density. The total root-mean-squared input noise can then be found by integrating the input noise spectral density over the entire bandwidth of interest [5]. Figure 4.4 presents the input-referred noise response and noise figure of the VGA for three gain settings. This design provides the best noise performance for the highest gain setting, which is valuable since the noise is most important when the input signal is weak and the gain of the system is high. In fact, the noise performance of the highest gain setting determines the minimum input signal acceptable by the system.

The high noise level at low frequencies is due to the flicker noise of the devices of the amplifier. As the frequency increases, the main noise contributors turn out to be the thermal noise of transistors and resistors, and the noise spectral density flattens out as seen in the diagram.



(a)



(b)

Figure 4.4 (a) Input-referred noise response of the VGA for three gain settings. (b) Noise figure vs. frequency for 14dB, 0dB, and −10dB gain settings.

4.2.4 Linearity

Linearity is another important characteristic of any amplifier. As discussed in Chapter 2, the linearity can be presented by IIP3 and 1-dB compression point. The IIP3 is evaluated using the two-tone test of the QPSS engine. Linearity is most important for the low gain setting where the VGA is responsible for larger input signals. Figure 4.5 presents the plot of fundamental power and third-order inter-modulation power versus input power extrapolated to determine IIP3. As the plot illustrates, the value of IIP3 is 11.85dBm for the low gain setting of −10dB.

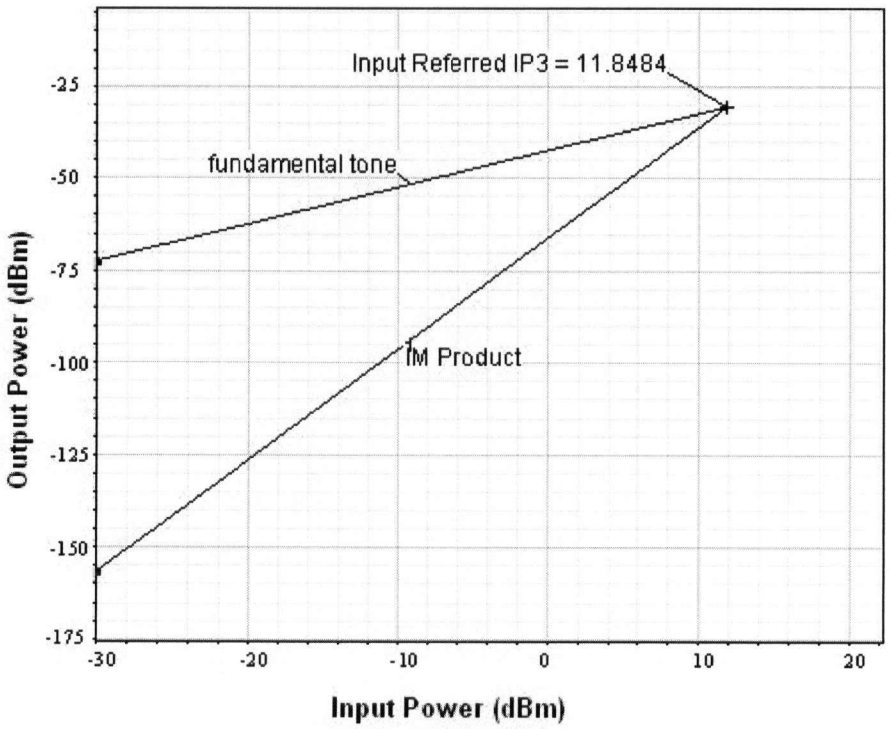


Figure 4.5 QPSS plot of IIP3 for low gain setting of −10dB.

The IIP3 simulation results for several gain settings are summarized in Table 4.3.

Gain(dB)	IIP3 (dBm)
14	0.761
0	3.19
-10	11.85

Table 4.3 The IIP3 for several gain settings.

In Figure 4.6, the output power is plotted versus the input power for zero gain setting. This figure can be used to obtain the 1-dB compression point of the system. As shown in the figure, the 1-dB compression point at zero gain setting is −1.69dBm.

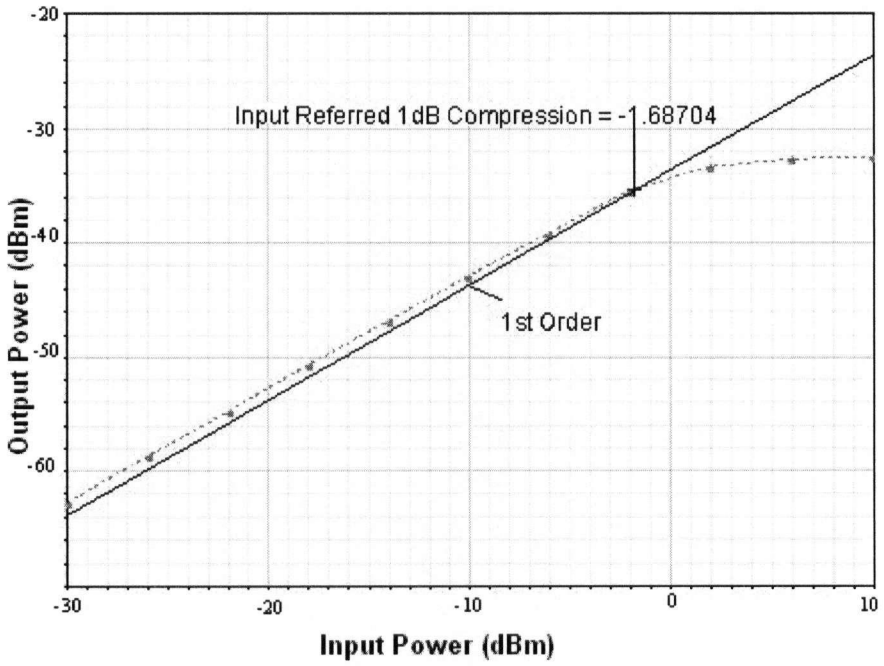


Figure 4.6 PSS plot of 1-dB compression point for zero gain setting.

The 1-dB compression points for several gain settings are summarized in Table 4.4.

Gain(dB)	1-dB compression point (dBm)
14	-12
0	-1.69
-10	8

Table 4.4 The 1-dB compression point for several gain settings.

4.3 Layout and Fabrication

The IC layout is considered the last stage of the IC design flow. The process-voltage-temperature (PVT) variations caused by fabrication process are very important. Careful layout considerations

and attention are essential for a successful design. Even with a successfully simulated circuit design, a poor layout can cause major circuit degradation or even a malfunction due to PVT variation. This VGA is designed and laid out in a six metal layer 0.18μm CMOS technology. The layout is done using the Cadence Virtuoso layout tool. Some of the layout issues and techniques used in this design along with the final layout are presented in this section.

4.3.1 Layout Consideration

Careful floor-planning and layout is very important when a differential topology is employed in the design. Device mismatch and symmetry issues can cause major problems in differential designs such as this work. For transistor layout, methods such as interdigitation and common centroid layout techniques can be used to reduce mismatch by ensuring the two half of the structure get affected almost equally by PVT variations [38].

A common layout technique known as gate-splitting is used to reduce gate resistance whose noise adds up to the total noise of the system. To ensure proper body contact and to minimize the substrate noise coupling, several body contacts are places closed to the each transistor. The matching for the resistors is very important in this design since the gain of the VGA is set by the ratio of these resistor networks. Matching for resistors is done by interdigitation and dummy insertion. Multiple via connections are used to ensure connectivity and to reduce parasitic resistance of the vias. Also, to reduce the IR drops, the pad connections are routed by wide traces on the top metal layer that has lower sheet resistance.

The layout of the single-stage VGA design without the pads is shown in Figure 4.7. The size of this layout is approximately 170μm by 115μm.

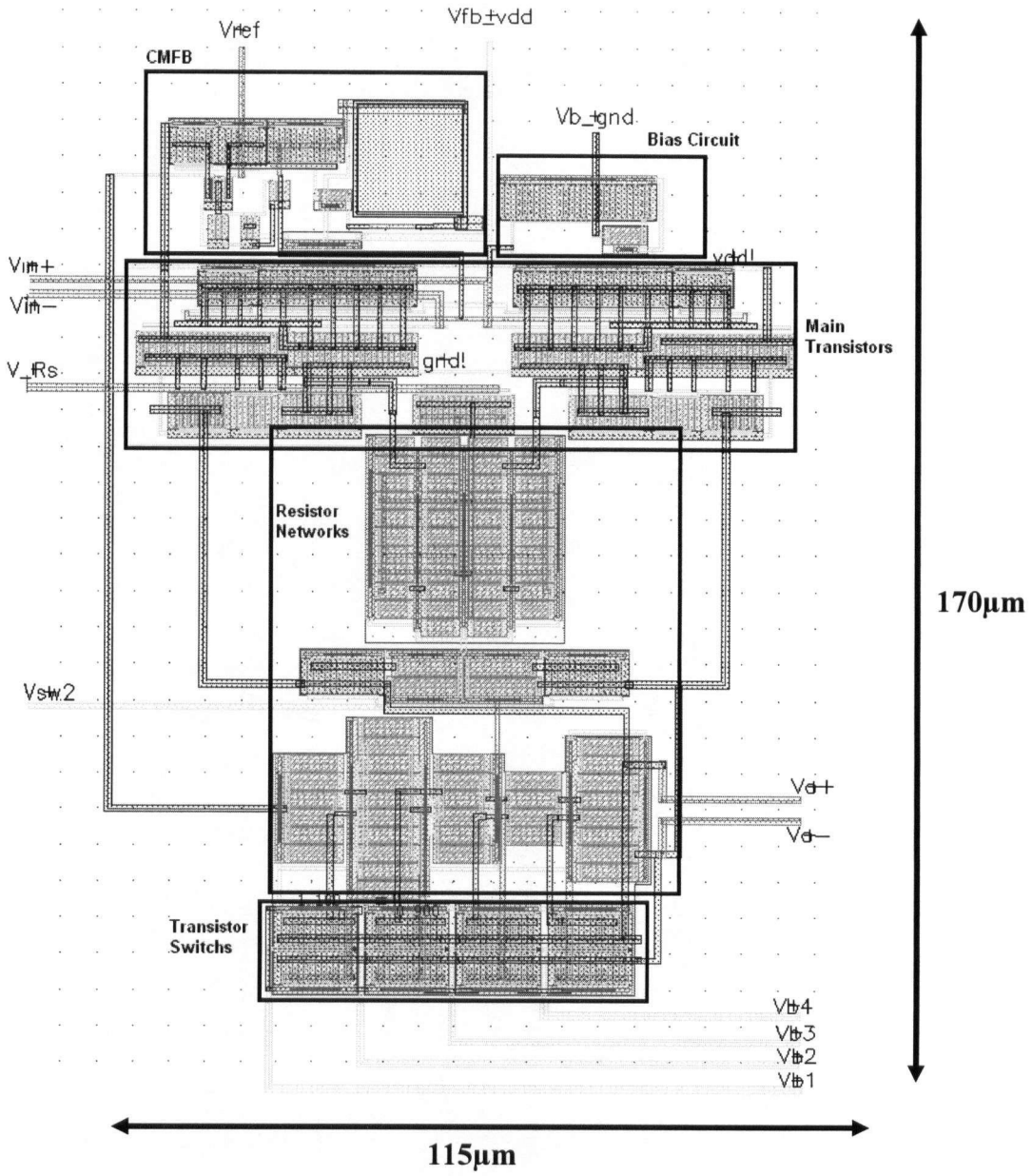


Figure 4.7 VGA Layout.

4.3.2 IC Fabrication

The single-stage test VGA is fabricated in the TSMC 0.18µm CMOS process and is fabricated by Canadian Microsystems Corporation (CMC). The micrograph of the fabricated IC is shown in

Figure 4.8 and the VGA signals are summarized in Table 4.5. The total dimensions of this IC, including the VGA circuit and pads, are 1mm by 1.2mm.

Pin(s)	Description
Vi+, Vi-	Differential inputs
Vo+, Vo-	Differential outputs
G	Ground
V_{DD}	1.8 DC supply
V_{b1}, V_{b2}, V_{b3}, V_{b4}, V_{Rs} , V_{RL}	Digital Control signals
V_{B_vdd}, V_{B_gnd}	Bias signals
V_{ref}	CMFB reference signal

Table 4.5 The Fabricated VGA pin/out.

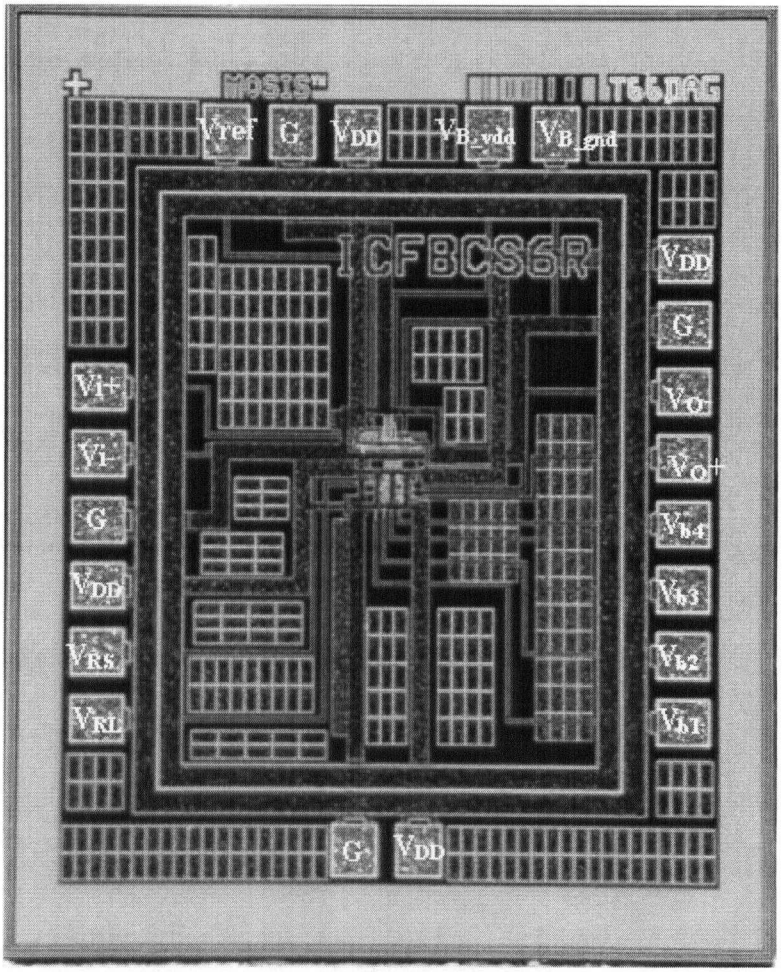


Figure 4.8 VGA IC microphotograph.

To take advantage of an existing CFP80TF test fixture provided by CMC, the IC is packaged using the standard 80 pin package QFP80 (Quad flat pack 80 pin). A photograph of the test setup including the packaged IC, test fixture, and the added control switches is shown in Figure 4.9.

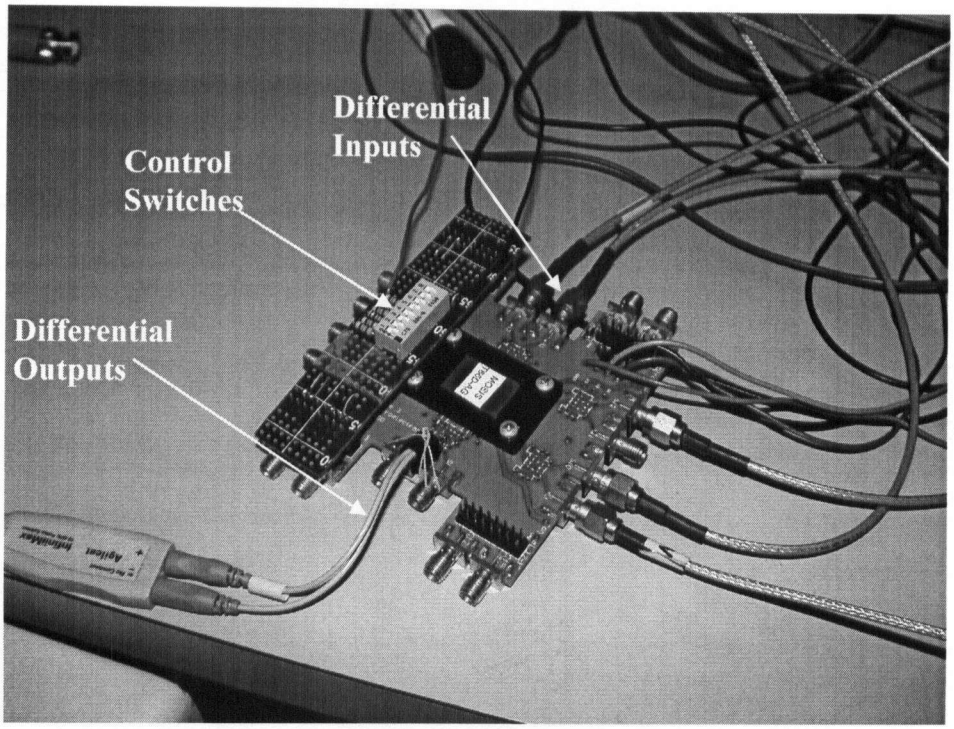


Figure 4.9 Photograph of the VGA IC with external control switches on the test fixture.

4.4 Test Results

In this section, test-related challenges and measurement results (gain, bandwidth, linearity, and noise) of the fabricated IC are presented.

4.4.1 Test planning

From the initial stages of a design, careful consideration and planning have to be made to account for the restrictions posed by the test equipment and measurement environment. In this work, the fabricated IC consists of a single stage of a 75dB three-stage integrated VGA. Therefore, the I/O effects of isolating a single stage must be taken into account.

There are two main issues that need to be addressed for successful testing of this stand-alone single-stage design. One issue arises from the differential nature of the input and output signals in this design. In general, differential driving and measurements can be complicated. Signal generators driving the inputs are usually single-ended. The spectrum analyzers used for frequency measurements are also single-ended in nature. The second issue is the output driving capability of the design. In the main 75dB VGA design, the single-stage is meant to drive the gate of the next stage, i.e. a load of 200fF. However, once fabricated individually, the standalone stage cannot properly drive the input impedance of the common oscilloscopes (10 MΩ || 12pF) or the spectrum analyzers (50 Ω).

There are various ways to overcome these obstacles. Some of the practical solutions used in this work are provided below:

- A Pulse/Pattern generator HP8110A can be used to generate square-wave differential voltages. This generator is suitable for large input signals since the minimum signal generated is limited. This generator is sufficient for frequency response measurements.
- A wide bandwidth 180° voltage splitter ZFSCJ-2-1 can be used to generate sinusoidal differential input voltage from a single-ended sinusoidal signal generator. This splitter has an insertion loss that varies with frequency, and consequently, this method is not adequate for frequency response measurements. However, it is suitable for linearity measurements such as IIP3 and 1-dB compression points.
- The Agilent oscilloscope, infiniium DS081304A, has on-the-fly mathematical analysis capabilities. Therefore, the fast-Fourier transform capabilities of this oscilloscope can also be used in place of a single-ended spectrum analyzer.

- The high impedance active probe of the above Oscilloscope, infinniMax II series, makes the differential output measurements possible. This solder-in differential probe has high differential impedance on the order of 50kΩ || 0.27pF. This probe satisfies two concerns: high impedance driving capability and differential output measurement.

4.4.2 Frequency Response

The measurement setup presented in Figure 4.10 is used to determine the frequency response of the VGA for all the gain settings.

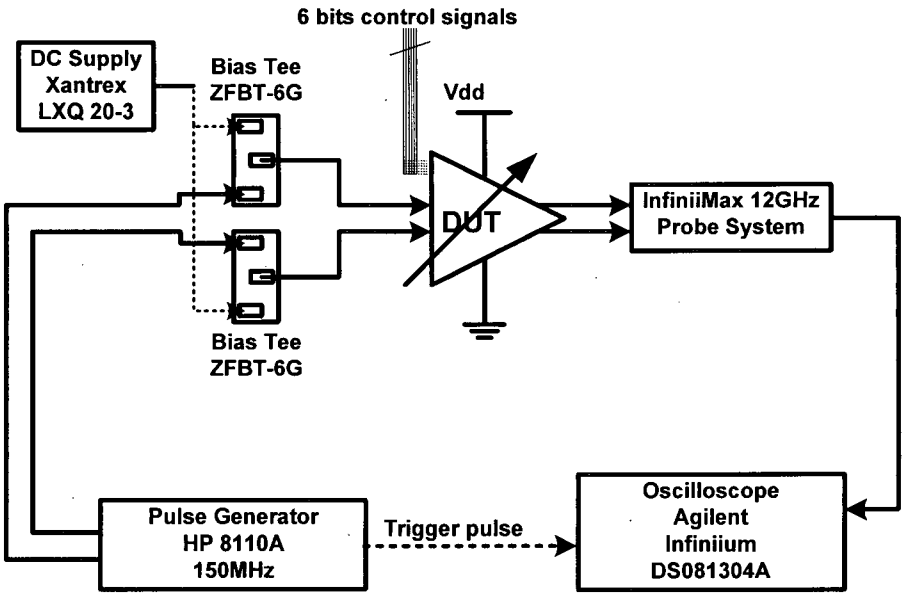


Figure 4.10 The test setup for frequency response measurements.

To obtain the frequency response for the entire gain range, the HP 8110A pulse generator is used to produce two output square wave signals of $50mV_{p.p}$ with 180° phase difference. This AC signal is then superimposed with the DC bias of 1.2 V through the bias tees, ZFBT-6G. The VGA is supplied with a 1.8V supply voltage. The six bit control signals are used to vary the gain

from −10dB to 14dB in 2 dB steps. The test chip drives a differential load of 50kΩ || 0.27pF which is the differential impedance of the Agilent InfiniiMax active probe.

The frequency response results are obtained by calculating the gain of the VGA from the input and output voltages measured at nineteen different frequency points across the signal bandwidth for each gain setting. The data obtained from the oscilloscope is used in MATLAB to analyze the results and plot the frequency response diagram presented in Figure 4.11.

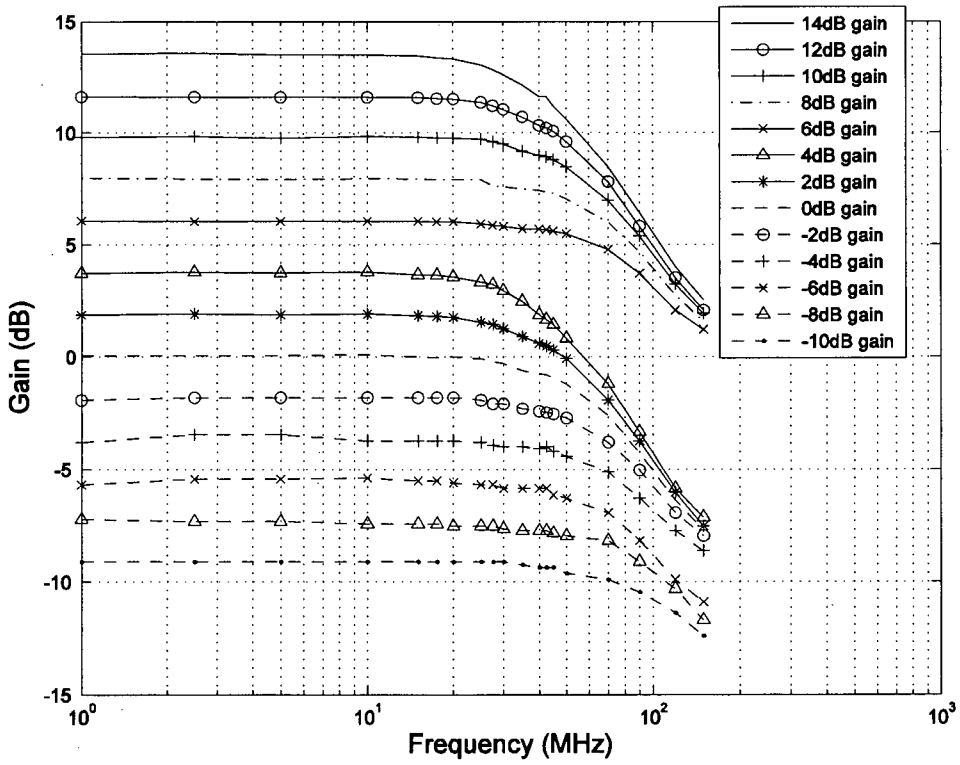


Figure 4.11 Gain response based on measurement results of the fabricated IC.

The diagram in Figure 4.11 contains all thirteen gain settings from −10dB to 14dB gain range with a 2dB step size. The gain measurements are taken from three sample chips (average value for each gain setting is reported in Figure 4.11) and the test was conducted over a span of two

weeks. For each gain setting, the measured results of three samples were within ±1.5% of the corresponding average value. As can be seen from the gain plots, the frequency response is reasonably flat indicating small gain variation over the entire frequency. This matches the simulation results previously presented. The gain error is determined to be less than ±0.8dB for gain settings.

The 3-dB frequency bandwidth can also be extracted from the measurement data or the plots of frequency response presented. The bandwidth varies from approximately 50MHz to 140MHz, for a maximum gain of 14dB to the minimum gain of −10dB, respectively. This bandwidth variation of 90MHz is comparable to the bandwidth variation of 120 MHz for the simulation results. However, the minimum and maximum bandwidths obtained from the measurements are quite different from the simulation results. This discrepancy is attributed to the load capacitance. In the simulation stage, a 200fF load capacitance has been used to present gate of the next stage in the multi-stage VGA. However, once this stage is fabricated alone, the output pad capacitance, package capacitance, and the input load capacitance of the oscilloscope increase the capacitance seen by this stage resulting in a decrease in measurement bandwidth. From the simulation results, this total load capacitance can be estimated to be less than 1.9pF, which is reasonable considering the typical values of the above-mentioned parasitic effects.

4.4.3 Linearity

As explained in Chapter 2 and the simulation section of this chapter, both IIP3 and 1-dB compression points are used as a measure of the linearity of the system. The two-tone test measurement setup is illustrated in Figure 4.12.

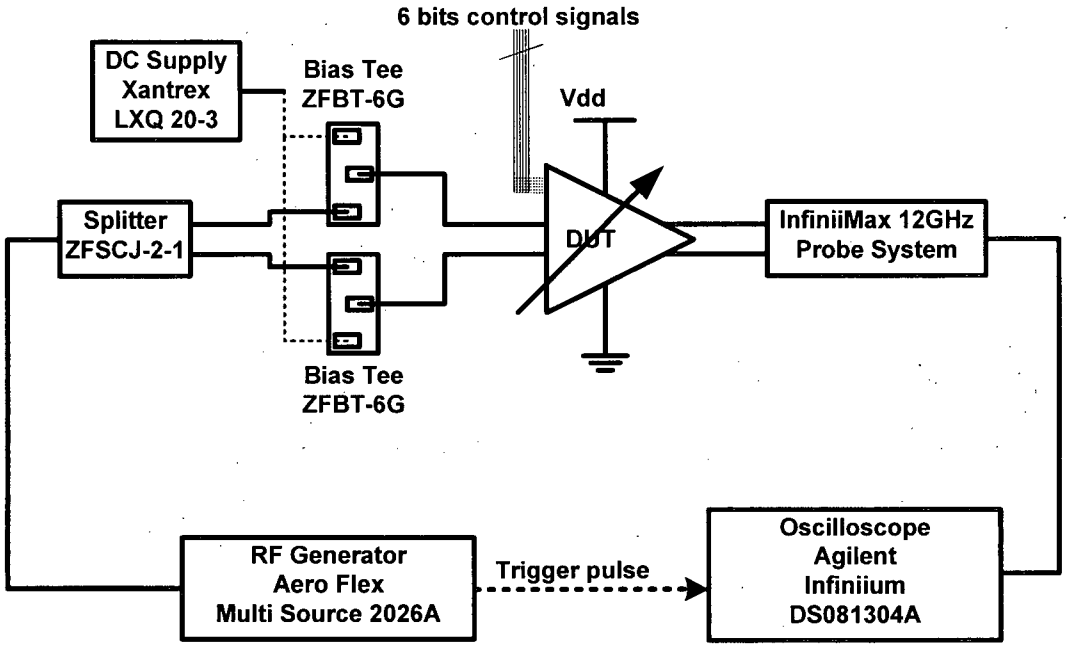


Figure 4.12 The test setup for IIP3 and 1-dB compression point.

This setup is very similar to the frequency response measurement setup. In this arrangement, the multi-source Aero Flex 2026A RF generator is used instead of the pulse generator as a signal generator. This multi-purpose signal generator is capable of internally combining two equal amplitude and closely spaced signals (e.g., 20.01MHz and 19.99MHz). The combined signal is then passed through a 2-way 180° signal splitter, ZFSCJ-2-1, to provide the differential two tone signals. The signals are then fed through the DUT and the outputs are measured through the InfiniiMax active probe. The FFT function capability provided by the Agilent Infiniium oscilloscope is used to calculate the output power at the fundamental frequencies (20.01MHz and 19.99MHz) and IM frequencies (19.97MHz and 20.03MHz). An example of the fundamental power and IM product power presented on the screen of the oscilloscope by utilizing the FFT functionality is shown in Figure 4.13.

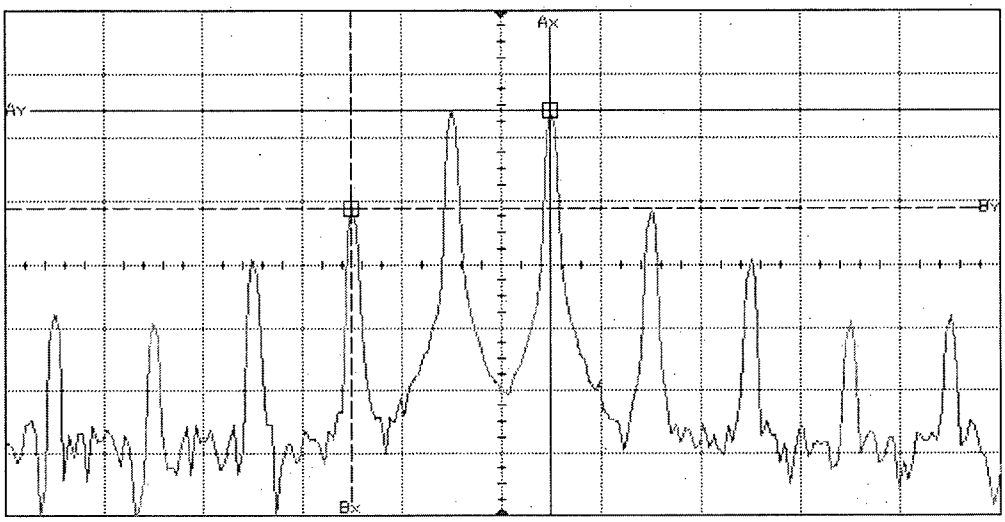


Figure 4.13 The result of two-tone test using FFT function of the oscilloscope.

The power of the two-tone signals are simultaneously increased and the output power of both the fundamental tones and the IM product are obtained from the oscilloscope. The MATLAB software is then used to analyze the data and extrapolate the IIP3 point. Figure 4.14 presents the measured result of the two-tone test for the −10 gain setting. The IIP3 for this gain setting is measured to be 11.26dBm.

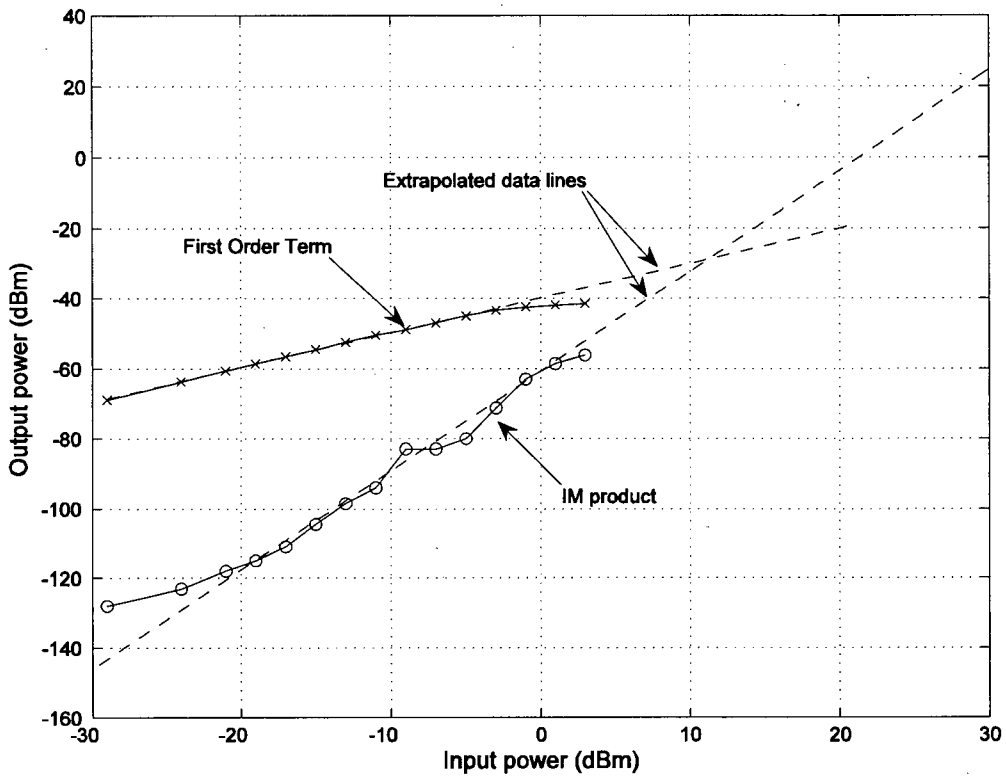


Figure 4.14 The Measured result of the two-tone test for gain of −10dB.

A similar process is applied for different gain settings and the analyzed results are presented in Table 4.6.

Gain(dB)	IIP3 (dBm)
14	0
0	4
-10	11.26

Table 4.6 The Measured IIP3 for several gain settings.

It is worth noting that the output power presented by the oscilloscope, based on the FFT function, calculates the power $(10\log(\frac{V^2/R}{0.001}))$ based on 50Ω termination. In the simulation section, the differential load of 1MΩ has been used for IIP3 power calculations leading to a

-40dBm ($10\log(\frac{50}{0.5M})$) discrepancy in output power between measurements and simulations. To take care of this inconsistency, in this work the measurement data obtained from FFT function are computed in MATLAB considering the 1MΩ differential (or 0.5MΩ single ended) impedance termination, as shown in Figure 4.14.

For the 1dB-compresion point measurements, the same setup presented in Figure 4.12 is utilized. For this test, the multi-source Aero Flex 2026A RF generator is used to generate single-tone input at 20MHz. The input is passed through a 2-way 180° signal splitter and fed to the IC. The output power at 20MHz frequency is measured using the FFT function of the oscilloscope. The input amplitude of the signal is increased until the gain of the signal is compressed. The graph in Figure 4.15 is obtained by setting the gain to 0dB, manually increasing the input power, measuring the output power, entering the values in MATLAB for analysis, and finally plotting the data. The measured 1-dB compression point for 0dB gain setting is 0.3dBm.

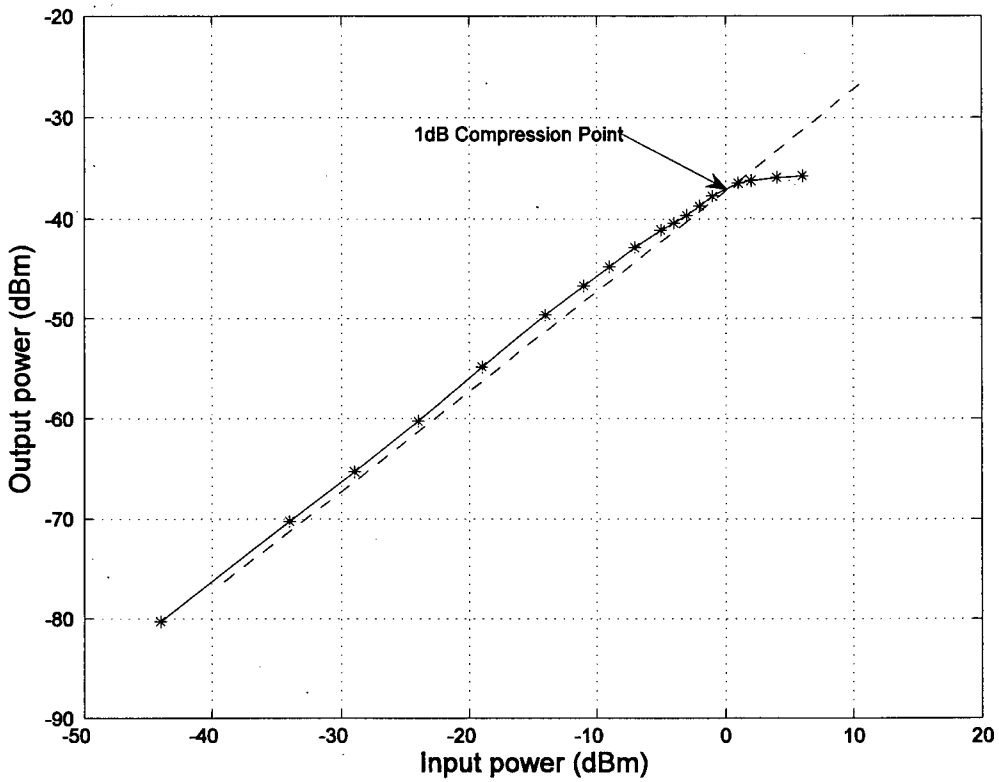


Figure 4.15 Measured 1-dB compression point for 0dB gain setting.

The same measurement process is applied for several gain settings and the analyzed results are summarized in Table 4.7.

Gain(dB)	1-dB compression point (dBm)
14	-14
0	0.3
−10	3.5

Table 4.7 The measured 1-dB compression point for several gain settings.

4.4.4 Noise

Unfortunately, noise measurements were not possible since differential noise figure measurement equipment with active probing capability was not available.

4.5 Single-stage VGA Design Results Summary

Table 4.8 summarizes the simulated and measured results of the performance parameters for the single-stage VGA designed, fabricated, and tested in this work. The power dissipation is also provided in this table. The gain and linearity performance are comparable in simulation and measurement. As explained earlier, the bandwidth discrepancy between the measurement and the simulation results is attributed to the parasitic capacitances of the package, and the measurement equipment probe.

Parameter	Circuit level Simulated	Fabricated IC Results	Comments
Gain range	−10 to 14 dB	−10 to 14 dB	Step size =2dB
Gain error	< 0.4 dB	< 0.8 dB	
Bandwidth range	199MHz -320MHz	50 MHz -140MHz	Different loads
IIP3	11.85 dBm	11.26 dBm	G = −10dB
1-dB Compression Point	8 dBm	3.5dBm	G = −10dB
NF	10 dB	-	G = 14dB & f = 20MHz
Input-referred noise	2.5nV/√Hz	-	G = 14dB & f = 20MHz
Output Load	200fF	>1.9pF*	*Includes Package and test equipment capacitor

Table 4.8 Single-stage VGA result summary.

Chapter 5

MULTI-STAGE VGA DESIGN

The single-stage 24dB VGA IC, presented in the previous chapter, is designed as a proof of concept. Based on the experimental results of the test chip, further modifications and analysis have been performed to enhance the performance parameters of the final design. The final design is a multi-stage 75dB VGA that consists of three variable gain stages with 25dB of gain range. The design details and simulation results are presented in this chapter. Section 5.1 describes different stages of the final design architecture. In Section 5.2, simulation results for the multi-stage VGA, using 0.18μm CMOS models, are presented. The performance summary and comparison with previous work are summarized in Section 5.3.

5.1 Design of the Three-Stage VGA

The block diagram of the multi-stage VGA is shown in Figure 5.1. To achieve the wide gain range of 75dB, the VGA consists of three cascaded gain stages where each stage covers a gain range of −5dB to +20dB. The first two stages are designed to have a coarse gain tuning control while the third stage provides the fine gain tuning. The first two stages are comprised of a dB-linear 25dB gain range with a 5dB gain step. Extra circuitry is embedded in the third stage to provide the 25dB gain range with a finer gain step of 2.5dB. Thus, the multi-stage design covers an overall gain range of 75dB, from −15 to +60dB, with 2.5dB step resolution.

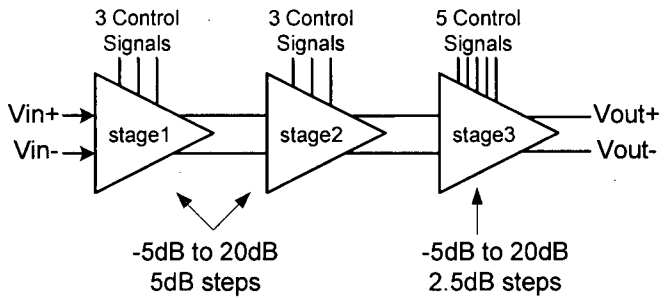


Figure 5.1 The basic block diagram of the multi-stage 75dB VGA.

This structure is designed and optimized to achieve a high gain range and large bandwidth. Other performance parameters such as linearity, noise, and power consumption have been carefully studied and optimized during the design stage. As mentioned before, the differential source-degenerated structure used for the core of this design has already enhanced linearity performance. Therefore, for this structure, focus has been shifted to optimization of the noise performance of the system.

Not only can the structure of each sub-section be optimized for noise performance, the gain distribution over the three sub-stages can be performed in a way to boost this performance parameter. As provided by Equation (2.3) in the Chapter 2, the NF of the first stage is the most dominant factor in the total NF of any multi-stage structure. This parameter is directly added to the noise of the entire system. Thus, noise optimization efforts should be mostly geared towards the first stage. Another very important fact from Equation (2.3) is that a high gain in the first stage can enhance the NF of the system. Therefore, in this work, the gain of the first stage is kept at maximum as much as possible to enhance the noise performance of the overall VGA system for the small input signal. In contrast, the gain of the first stage is lowered for large input signals where the noise performance of the amplifiers is not critical [17].

The detailed design and schematics of the amplifier stages are provided in the following sub-sections.

5.1.1 First and Second Stages

The schematic of the first two stages of the proposed multi-stage VGA is presented in Figure 5.2. As shown in this figure, the first two stages use three control signals, V_{Rs}, V_{b1}, and V_{b2}, for gain tuning. The V_{Rs} signal controls the source-degeneration resistor and is used for coarse tuning. It switches the gain between the high (10dB to 20dB) and low (−5dB to 5dB) gain range. Once in a high or a low gain range section, the gain can be further tuned, in 5dB steps. This is achieved by the two gain-control signals, V_{b1} and V_{b2}, which change the value of the resistors between the output nodes. The signal settings for the gain control of these two stages are summarized in Table 5.1.

Gain (dB)	V_{Rs} (V)	V_{b1} (V)	V_{b2} (V)
20	1.8	1.8	1.8
15	1.8	1.8	0
10	1.8	0	0
5	0	1.8	1.8
0	0	1.8	0
-5	0	0	0

Table 5.1 Gain control signal settings of the first and second stages.

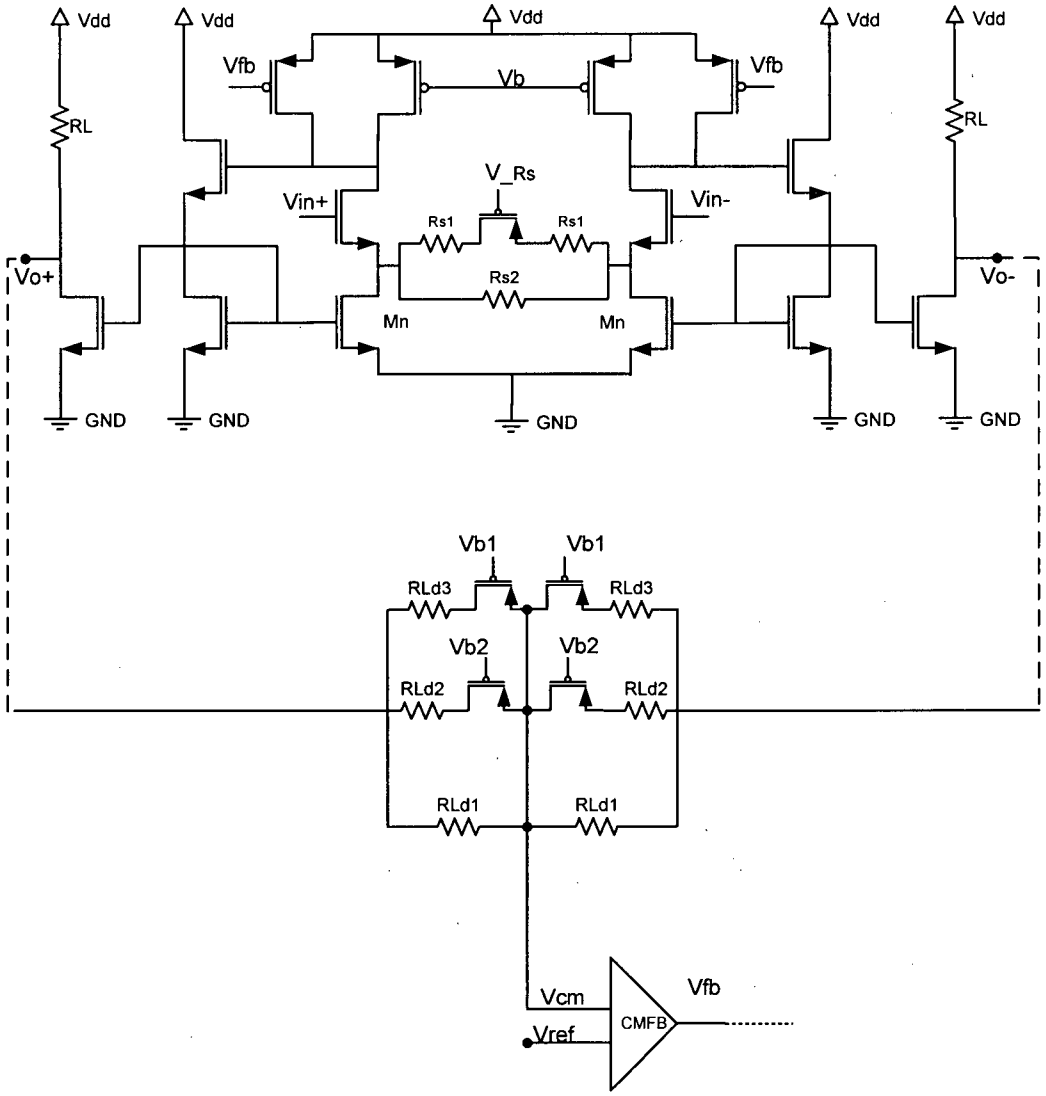


Figure 5.2 Schematics of first and second stages of the multi-stage VGA.

5.1.2 Third Stage

The structure of the third stage is similar to the first two stages. However, the third stage is further modified to provide smaller gain steps. This is achieved by adding two more resistor branches between the output nodes, as shown in Figure 5.3. In this stage, V_{Rs} is again dedicated for coarse gain control. The gain is finely-tuned, in 2.5dB steps, using the other four control

signals, V_{b1}, V_{b2}, V_{b3}, and V_{b4}. The signal settings for gain control of these two stages are summarized in Table 5.2.

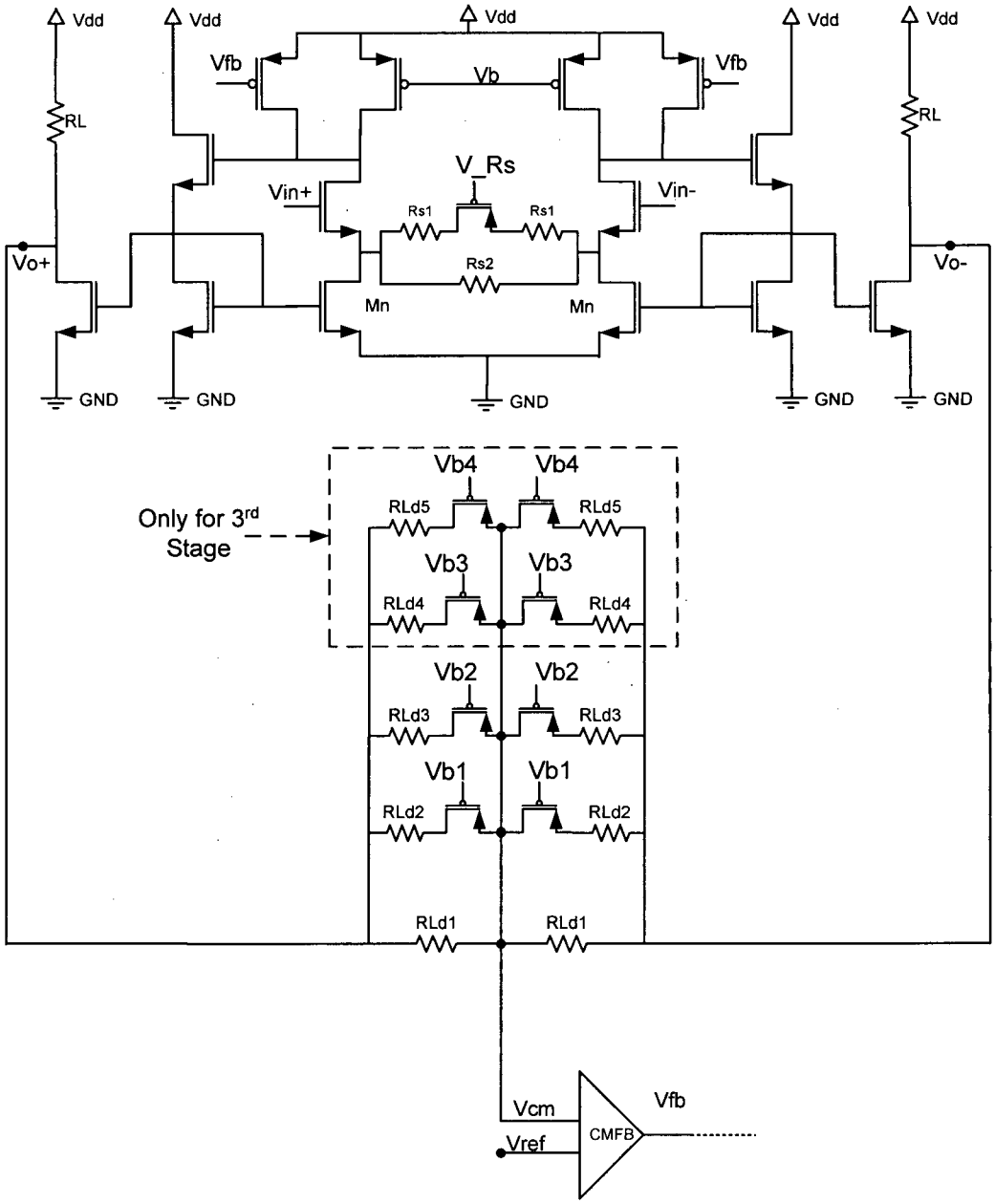


Figure 5.3 Schematics of the third stage of the multi-stage VGA.

Gain (dB)	V_{Rs} (V)	V_{b1} (V)	V_{b2} (V)	V_{b3} (V)	V_{b4} (V)
20	1.8	1.8	1.8	1.8	1.8
17.5	1.8	1.8	1.8	1.8	0
15	1.8	1.8	0	1.8	1.8
12.5	1.8	1.8	1.8	0	1.8
10	1.8	0	0	1.8	1.8
7.5	1.8	0	1.8	0	0
5	0	1.8	1.8	1.8	1.8
2.5	0	1.8	1.8	1.8	0
0	0	1.8	0	1.8	1.8
-2.5	0	1.8	1.8	0	1.8
-5	0	0	0	1.8	1.8

Table 5.2 Gain control signal setting of third sub-stage.

5.2 Simulation Results

This section presents the simulation results of the multi-stage VGA using the 0.18um CMOS models. An example of the test bench used for characterizing the performance of the multi-stage VGA is shown in Figure 5.4.

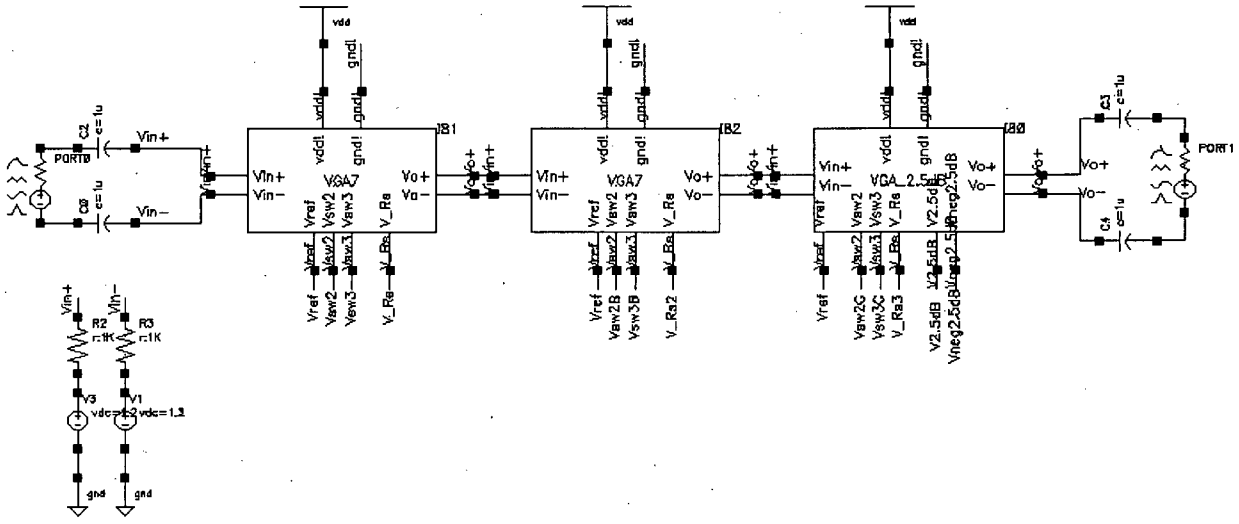


Figure 5.4 Multi-stage VGA test bench.

This test bench is similar to that of the single-stage VGA. Basically, the single-stage VGA is replaced by the cascade of three single-stage VGA blocks. The following sections present the

performance parameters obtained, such as frequency response, gain range, bandwidth, noise, and linearity.

5.2.1 Frequency Response

Figure 5.5 presents the simulated frequency response of the VGA over the entire gain range. As shown, the frequency response of each gain setting is flat resulting in small gain variation over the entire frequency range of interest.

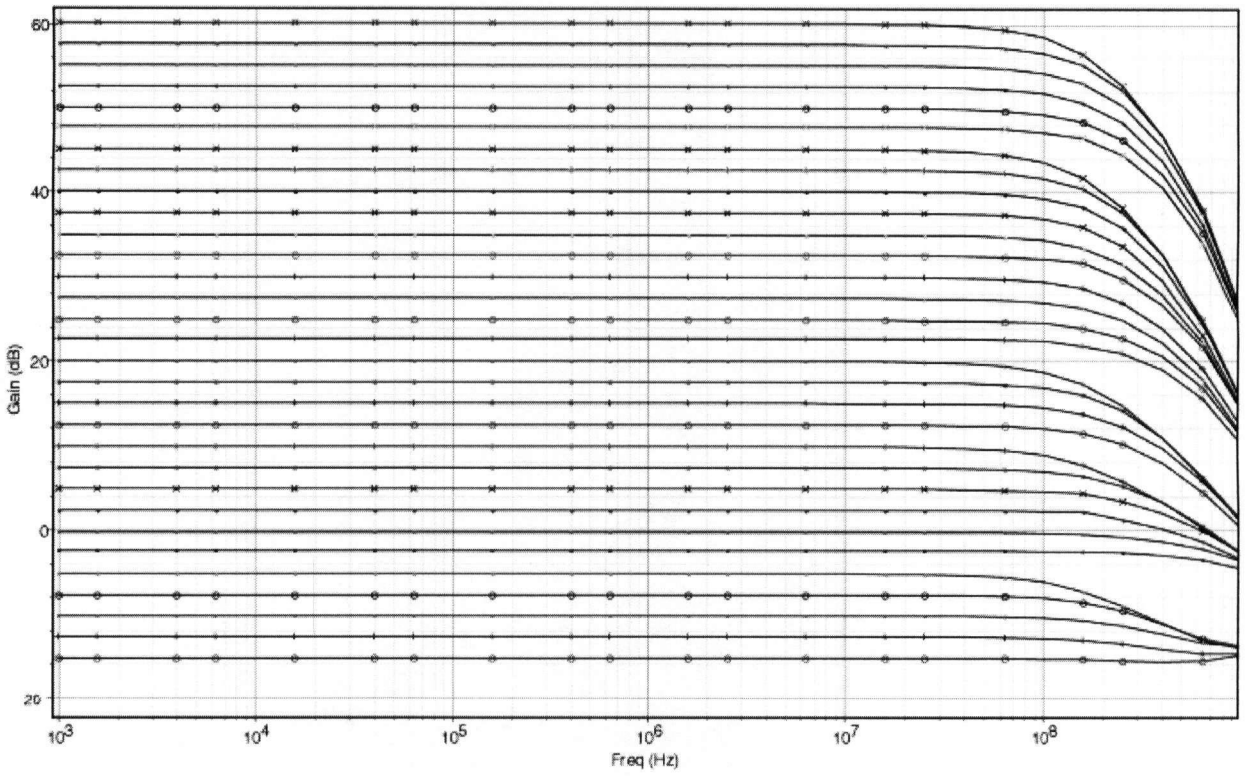
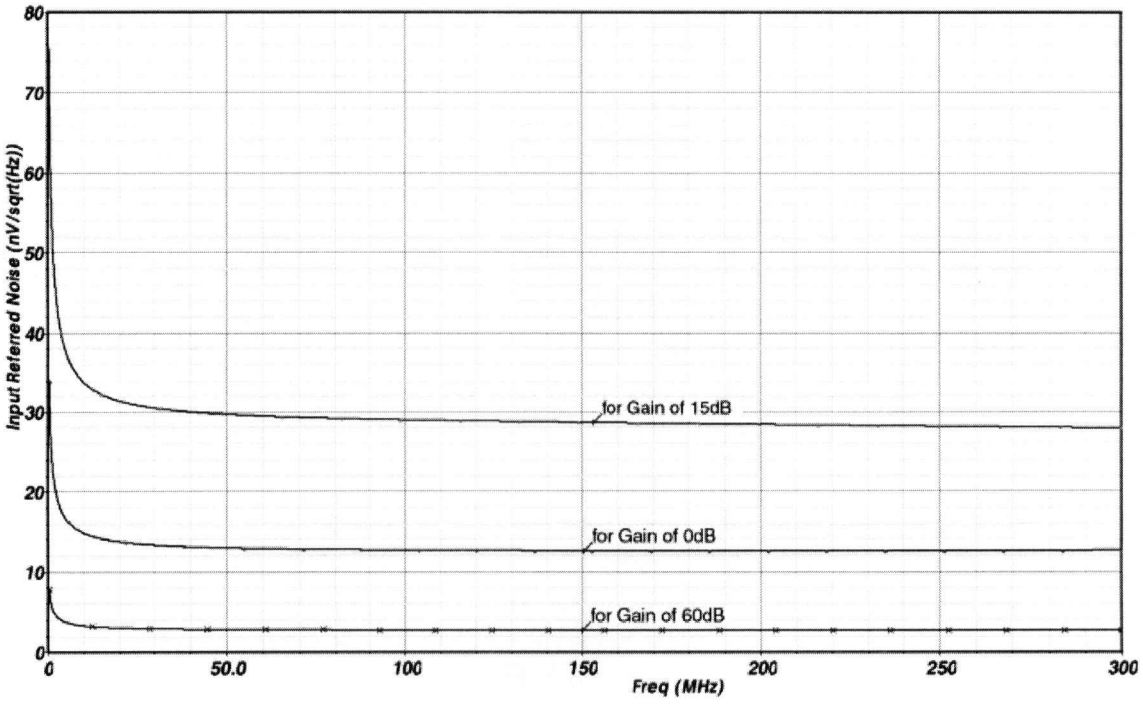


Figure 5.5 Frequency response of the multi-stage VGA, from −15 to +60dB, in 2.5dB steps.

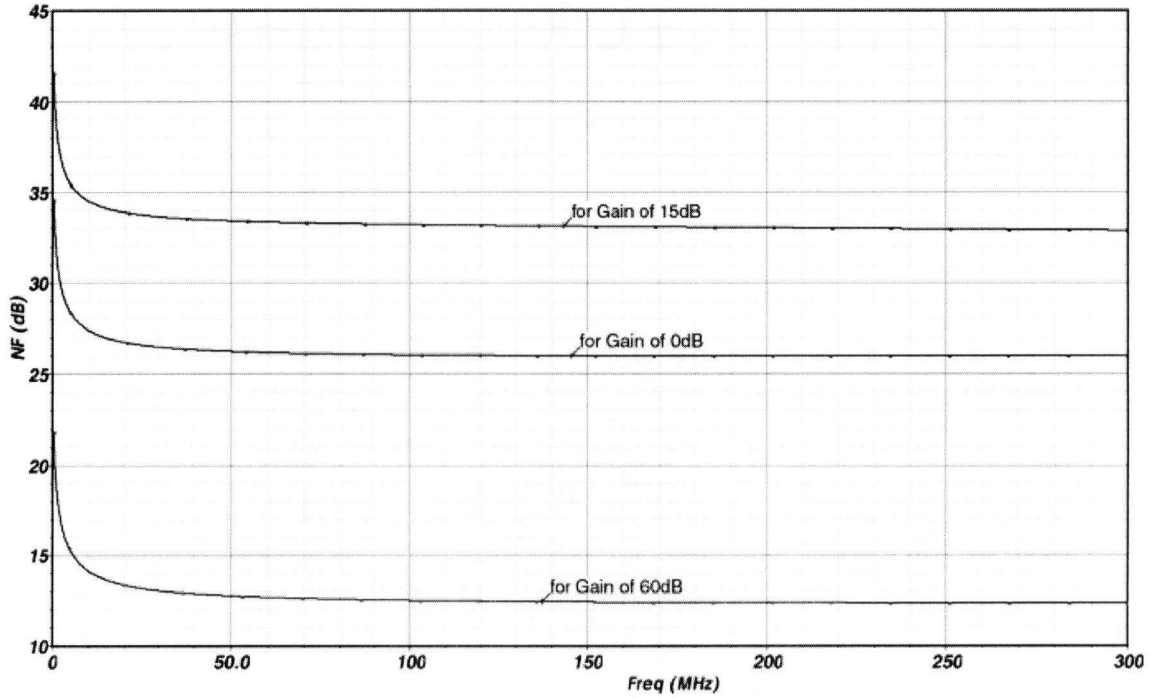
The proposed design achieves the overall gain range of 75dB, from −15 to +60dB, in 2.5dB gain steps. The gain error is less than ±0.3dB. The bandwidth varies from approximately 140MHz to 270MHz, for a maximum gain of 60dB to the minimum gain of −15dB, respectively. for an output load of 200fF.

5.2.2 Noise

Figure 5.6 presents the simulated input-referred noise and NF of the VGA for the three gain settings.



(a)



(b)

Figure 5.6 (a) Input-referred noise response and (b) NF for 60dB, 0dB, and −15dB gain settings.

5.2.3 Linearity

In this section, the simulated IIP3 and 1-dB compression points are presented as the measures of linearity of the system. Figure 5.7 presents the plot of fundamental power and third-order inter-modulation power versus input power extrapolated to determine IIP3. As the plot illustrates, the value of IIP3 is 14.38dBm for the low gain setting of −10dB.

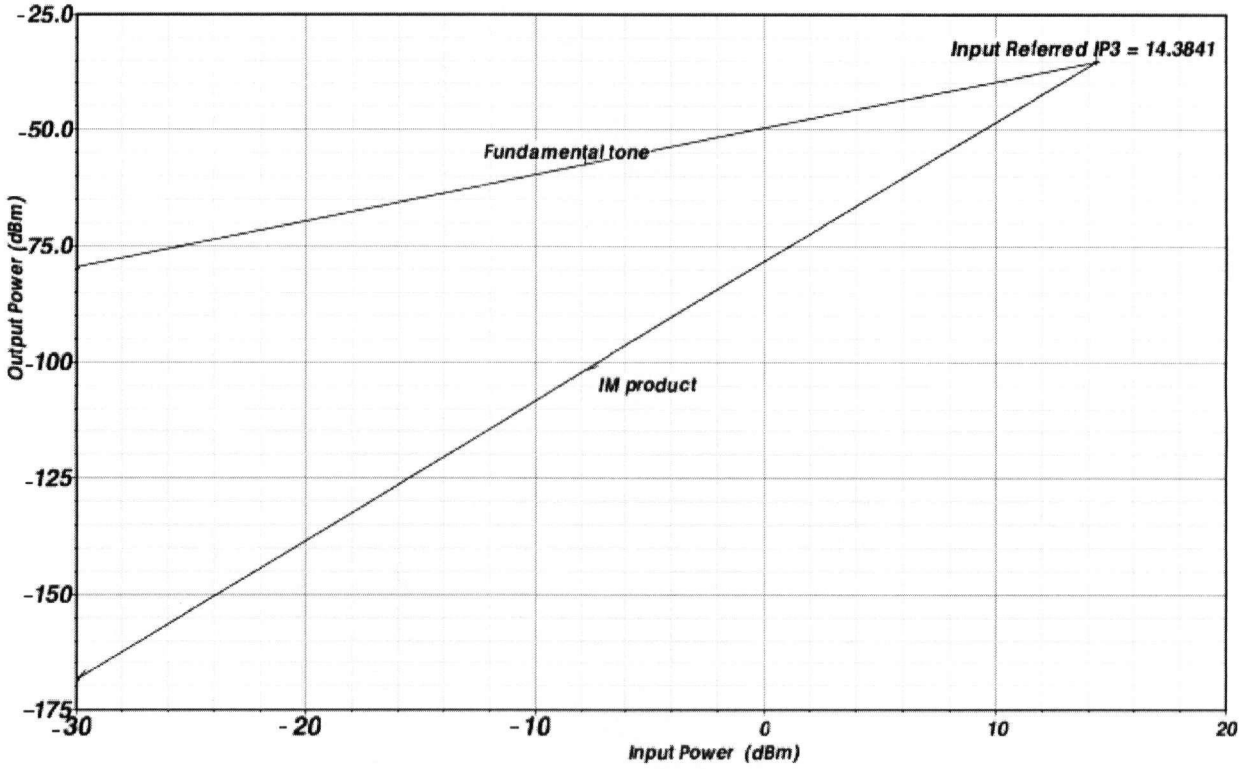


Figure 5.7 QPSS plot of IIP3 for low gain setting of −15dB.

The IIP3 simulation results using the QPSS analysis engine for several gain settings are presented in Table 5.3.

Gain(dB)	IIP3 (dBm)
60	−18.5
0	11.86
-15	14.38

Table 5.3 The IIP3 for several gain settings.

Figure 5.8 shows the 1-dB compression point where the output power is plotted versus the input power. As the figure presents, the 1-dB compression point at zero gain setting is −2.35dBm.

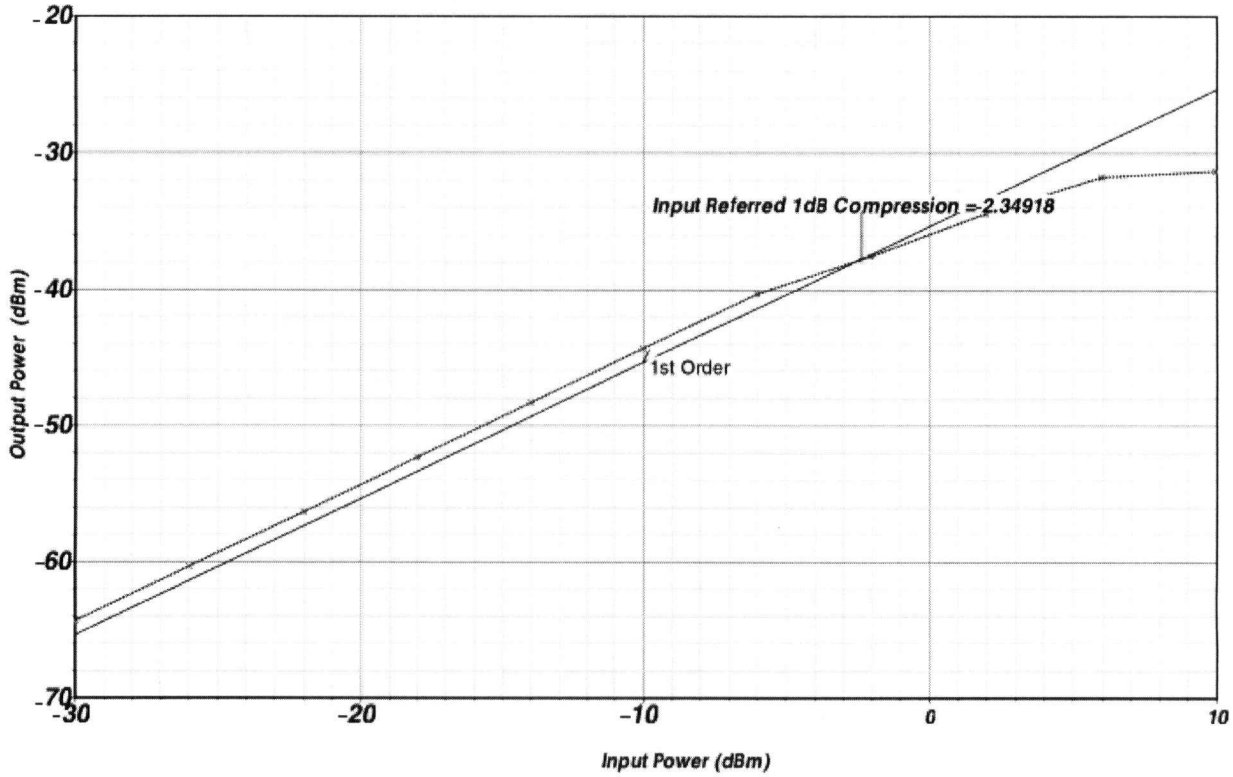


Figure 5.8 PSS plot of 1-dB compression point for zero gain setting.

The 1-dB compression points for several gain settings are summarized in Table 5.5.

Gain(dB)	1-dB compression point (dBm)
60	-29
0	-2.349
-15	-1.521

Table 5.4 The 1-dB compression point for several gain settings.

5.3 Comparison with Previous Work

The overall performance of the multi-stage VGA is summarized in Table 5.5, and is compared with previously reported work. As presented in this table, in most designs, either the bandwidth

is low or the gain range is low and in only a few topologies (such as our design) both are reasonably high. In addition, the proposed VGA achieves the best performance in terms of linearity and active area. It also achieves the highest gain range and best power consumption among the digitally controllable VGA designs. The VGA in general has competitive linearity, gain range, bandwidth, power consumption, and active area as compared to other designs.

Ref.	CMOS Techno -logy	Bandwidth (MHz)	Voltage (V)	Power Consumption (mW)	IIP3 (dBm) @Gmin	P1dB (dBm) @Gmin	Gain Variation (dB) / Number of stages	Gain range (dB)	Gain error (dB)	NF (dB) @ Gmax	Input-referred input noise (nV/√Hz)	area (mm^2)	Control method	Year
[1]**	0.25μm	30~210	2.5	27.5	7	-8	80/4	-35 ~ 55	3	8	*	0.49	Analog	2002
[24]	0.5μm	150	3.3	12.5	*	*	15/1	-5 ~ 10	1	*	*	0.15	Analog	1998
[25]	0.35μm	21	1.5	24.8	*	*	26/1	-6 ~ 20	*	*	10.18	*	Analog	2000
[26]**	2μm	~ 6	3	2.88	*	*	30/1	-0.4 ~ 29.6	*	*	308	*	Analog	1998
[2]	0.35μm	10	3	35	*	*	60/3	*	*	*	*	*	Analog	2004
[3]**	0.18μm	32~ 1050	1.8	6.48	*	-17	95/2	-52 ~ 43	1	*	*	0.4	Analog	2006
[4]**	0.25μm	380	2.5	63.25	*	*	80/4	-70 ~ 11	3	11	*	2.0164	Analog	2002
[35]**	1.2μm	18	3	*	*	*	60/2		0.5	*	21	0.442	Digital	2000
[6]**	0.35μm	125	3.3	21	35	*	19/1	0~19	1	*	8.63	0.18	Digital	2003
[39]	0.18μm	20	1.8	13.284	*	*	60/3	0~ 60	*	*	*	*	Digital	2005
[32]**	0.25μm	18	3.1	18.7	*	*	24/2	*	*	*	*	0.2401	Digital	2004
[37]	0.8μm	15	5	25	*	*	14/1	-2 ~ 12	0.05	*	*	0.175	Digital	1996
[17]**	0.35μm	246	3	27	-4	*	60/3	-15 ~ 45	0.3	<15	*	0.64	Digital	2001
[30]**	0.35μm	95	3.3	32.7	-1.962	0.61	70/3	-30 ~ 40	0.3	*	*	0.286	Digital	2005
This work	0.18μm	140~270	1.8	11.8	14.38	-2.35	75/3	-15 ~ 60	0.3	12.5	2.6	0.0571	Digital	2006

*** Not reported.**

**** Measured results.**

Table 5.5 The performance parameter comparison between the proposed multi-stage VGA and previously reported VGA designs.

Chapter 6

CONCLUSIONS AND FUTURE WORK

A digitally controllable VGA in a 0.18μm CMOS technology is presented in this thesis. This VGA is designed for automotive PLC systems; however, it is a general purpose and could be used in other communication applications.

This thesis provides an overview of the key performance parameters of a VGA, such as gain range, bandwidth, noise, and linearity. The existing VGA architectures are reviewed, along with their advantages and shortcomings. A low-distortion source-degenerated structure is then proposed for the core of the VGA. To provide higher gain and minimize the gain error, a G_m-boosting circuitry is also included.

The design in this work (for the first time) combines two gain control techniques to enhance the performance parameters of the resulting VGA. In the combined architecture, the source-degeneration resistance is used to achieve low bandwidth variation across the gain range, and the added resistors between the output nodes are used to provide high gain range. The changes in the source-degeneration resistance handle the coarse tuning and the changes in the latter resistance are used for fine gain control.

As a proof of concept, a prototype single-stage 24dB VGA based on the proposed technique is

designed, simulated, and fabricated using a 0.18μm CMOS process. The IC is tested and measurement results are compared to that of the simulation. Based on these measurement results, the design of the gain stage is optimized and a 75dB VGA is designed.

The digitally controllable 75dB VGA consists of three gain stages. The gain of each stage varies from −5dB to +20dB in fine gain steps of 2.5dB. The total gain range varies from −15dB to +60dB with a gain error of less than 0.3dB. The final design achieves a 3-dB bandwidth of higher than 140MHz. The overall VGA draws 6.5mA from a 1.8V supply. The noise figure of the system at maximum gain is 12.5dB, and the IIP3 of the system at minimum gain is 14.4dBm. These performance parameters are either better or comparable with the reported state-of-the-art VGA designs.

6.1 Future Work

Several tasks can be performed to continue this work, some of which are:

1. IC fabrication: Fabricate the proposed three-stage VGA in a 0.18μm CMOS technology and measure its performance.
2. Buffer Implementation: In the main 75dB VGA design, the single-stage is designed to drive the gate of the next stage (a 200fF load). While testing this single-stage design, the VGA cannot properly drive the input impedance of oscilloscopes (either 10 MΩ || 12pF or 50 Ω) or the spectrum analyzers (50 Ω). This loading could result in the VGA overload and bandwidth reduction. A proper buffering design to remove the effect of loading on the VGA would facilitate the testing.
3. AGC loop implementation: The analog challenge of implementing an AGC system using the proposed VGA and a DSP core could be a new research topic.

4. Noise and linearity optimization: Although the noise and linearity performance of the designed VGA is satisfactory, further optimization to achieve an even better performance would be beneficial.
5. Integration to other feature-sizes: The CMOS process selected for design and fabrication of an IC ultimately depends on the application at hand. The proposed VGA can be used in a smaller or possibly even a larger feature size process. Therefore, the integration challenges of using other processes should be examined.
6. PVT variation optimization: For a product to be commercialized, the effect of PVT variation on the device should be carefully examined. The investigation and optimization of PVT variation on the VGA proposed in this work should be explored.

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