Application of Complex Quantized Feedback in Direct Conversion Receivers for Wireless Applications

by

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Abstract

The recent resurgence in radio frequency (RF) transceiver design for wireless applications is accompanied by aggressive design goals such as low cost, low power dissipation, small form factor, and high-speed data transfer. To address these objectives, extensive research has been focused on the development of monolithic transceiver architectures, especially using low-cost CMOS technology. It is in this context that there is renewed interest in the direct-conversion receiver (DCR) architecture, the subject of this research. Currently, the use of DCRs involves a number of challenges. Issues of DC offset, flicker noise, LO leakage and radiation, I/Q mismatch, and intermodulation distortion should be carefully considered and addressed in a DCR design. Also, because of cost incentives and performance, one of the main trends in the evolution of wireless receivers is to implement more and more functionality by way of digital signal processing (DSP). The main objective of this thesis is the development and implementation of solutions to overcome these impairments in the DCR architecture and facilitate DCR design using DSP.

To achieve this goal, we begin by using AC coupling to remove DC offset and to reduce flicker noise. Then, quantized feedback (QFB) is employed in both I and Q channels to reduce the baseline wander effect caused by AC-coupling. Such modifications are unable to combat carrier phase error and I/Q mismatch problems. However, they can be effectively reduced using a cross-coupled or complex QFB (CQFB), the key contribution in the thesis. The performance of this CQFB-enhanced DCR architecture is theoretically analyzed and experimentally validated. Next, the design issues for adaptive implementation of CQFB using DSP techniques are addressed. Further, its use is illustrated in the context of a direct-conversion orthogonal frequency-division multiplexing (OFDM) receiver. We show that digital CQFB is very effective in compensation of DC offset, I/Q mismatch, and carrier phase error in a DCR for OFDM signaling. To assist in validation of the developed approach, a prototype RF front-end of the receiver is designed and fabricated in TSMC 0.18μm CMOS process for 2.4GHz wireless applications. The developed prototype provides for user control of I/Q mismatch and includes all the main blocks of the RF front-end of the receiver, namely, a low-noise amplifier (LNA), two mixers and a voltage-controlled oscillator (VCO). This prototype can be used as test vehicle for evaluation of various I/Q mismatch compensation methods implemented in the back-end.
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List of Abbreviations

A/D  Analog to Digital Converter
ADC  Analog to Digital Converter
AM   Amplitude Modulation
BER  Bit-Error-Rate
BFSK Binary Frequency-Shift Keying
BW   Bandwidth
CMOS Complementary Metal Oxide Semiconductor
CQFB Complex Quantized Feedback
DAC  Digital-to-Analog Converter
DCR  Direct Conversion Receiver
DSP  Digital Signal Processing
DR   Dynamic Range
DRP  Digital Radio Processing
EH   Even Harmonic
FM   Frequency Modulation
GMSK Gaussian Minimum Shift Keying
GPS  Global Positioning System
HPF  High-Pass Filter
I    In-Phase
IC   Integrated Circuit
IEEE Institute of Electrical and Electronics Engineers
IF   Intermediate Frequency
IM2  2nd Order Intermodulation
IM3  3rd Order Intermodulation
IIP2 2nd Order Input Intercept Point
IIP3 3rd Order Input Intercept Point
ISI  Intersymbol Interference
K    Boltzmann Constant
LMS  Least Mean Squares
LNA  Low-Noise Amplifier
LO   Local Oscillator
LPF  Low-Pass Filter
MOSFET Metal Oxide Semiconductor Field Effect transistor
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<tr>
<td>OFDM</td>
<td>Orthogonal Frequency-Division Multiplexing</td>
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<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
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<tr>
<td>Q</td>
<td>Quadrature-Phase</td>
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<tr>
<td>Q</td>
<td>Quality Factor</td>
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<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
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<td>QFB</td>
<td>Quantized Feedback</td>
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<tr>
<td>QPSK</td>
<td>Quadrature Phase-Shift Keying</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>RLS</td>
<td>Recursive Least squares</td>
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<tr>
<td>SAW</td>
<td>Surface Acoustic Wave</td>
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<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
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<tr>
<td>SoC</td>
<td>System-on-a-Chip</td>
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<tr>
<td>SOI</td>
<td>Silicon-on-Insulator</td>
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<td>TDMA</td>
<td>Time division multiple access</td>
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<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
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<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
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<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
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Chapter 1

Introduction

1.1 Motivation

Single-chip wireless transceivers with the long-established requirements of low-cost, low power dissipation, and small form factor while still achieving high performance are now a reality. Advances in deep submicron complementary metal-oxide semiconductor (CMOS) processes and technologies have resulted in radio-frequency (RF) circuits on scalable digital CMOS processes. As a result, it is now possible to combine the best of both digital and analog worlds to truly enable the paradigm of digital radio processing (DRP) technology [5].

Designing RF and analog blocks in deep submicron digital CMOS processes is a significant challenge. Some of the reasons are listed below:

1. Because of technology scaling, the process node shrinks every 18 months; therefore, the RF and analog area should shrink with the same rate for the solution to be cost effective. However, analog design does not scale at the same rate.

2. Analog/RF must not require too many extra fabrication processing step because of cost. At present, analog and RF require many special process features.
3. The supply voltage is being reduced but the analog blocks must still maintain their dynamic range. Today, typically analog designs use higher supply voltages than digital design.

4. Substrate noise coupling from digital to analog/RF requires careful design and isolation techniques.

5. The device characteristics are constantly updated, so the RF and analog circuits are often designed on an immature process where simulation models and device characterization are not finalized.

Thus, conventional design techniques cannot be relied on in this new paradigm of a complete wireless mixed signal system-on-chip (SoC) design. On the other hand, analog and digital signal processing concepts can be used to alleviate some of the complexity of analog/RF design and, in fact, greatly simplify it.

Architectures that have been known to result in smaller bill of materials (BOM), but were never implemented due to technology limitations are now being revisited. A direct conversion receiver (DCR) is one such architecture that allows monolithic integration. However, the DCR architecture suffers from classical RF impairments common to all kinds of receivers. The impact of some of these impairments is much more critical for DCR compared with other architectures such as heterodyne receivers. The major impairments of concern in DCRs are DC offset, flicker noise, even-order harmonic distortions and I/Q mismatch [1]. This research will mainly focus on addressing the impairments associated with the DCR architecture using digital techniques.

In direct conversion receivers, the DC offset experiences a large gain in the stages
following the down-conversion process [6]. If not controlled, DC offset can cause saturation of subsequent A/D converters. A related impairment of concern in DCRs is flicker or $1/f$ noise that arises from random trapping of charge at the oxide-silicon interface of metal-oxide-semiconductor field-effect transistor (MOSFET) devices. Flicker noise introduces unwanted signal content close to DC. Even-order harmonic distortion, usually dominated by the 2nd-order harmonic, results in DC offset and possibly distortion in the frequency band around DC in the presence of a single strong interferer signal. If two strong interferer signals are present such that their difference frequency falls in the band of interest, then an unwanted signal will again be created in the band of interest. Finally, gain and phase mismatches between the I and Q channels in a quadrature receiver result in an unwanted image, which can cause degradation in the effective signal-to-noise ratio (SNR) in the presence of a large nearby modulated interferer.

A slight variation in DCR results in what is called the low-IF (low intermediate frequency) architecture. In this architecture, instead of direct-conversion or zero-IF, the RF signal is down-converted to a very small IF, usually half of the channel bandwidth. The advantage of this architecture is that it is less vulnerable to DC offset and flicker noise, compared with zero-IF. However, it is also prone to problems that arise from I and Q mismatches.

The objective of this research is to address the most important of these problems using digital techniques. Flicker noise is generally controlled by the dimensions of the transistors and it will be addressed with the same technique as DC offset compensation. The effect of flicker noise on receiver performance is reduced by using a higher IF frequency.
Although the techniques proposed in this research are applicable to all receivers implemented using DCR or low-IF architectures, they are applied to a IEEE 802.11g standard direct-conversion receiver in this thesis.

1.2 Research Goals and Challenges

Having described the motivation and necessary background, it is now possible to describe the objectives of this research. First, a succinct research objective is as follows:

To develop techniques that help alleviate analog impairments that plague DCR architectures, hence resulting in a robust receiver design.

A more detailed set of research objectives is outlined below:

- Develop a new technique for compensation of DC offset and low-frequency disturbance, with minimal degradation of the wanted signal.

- Develop a new technique for I/Q mismatch compensation. These circuits should be robust against interferer environment in which the receiver operates.

- Develop a flexible RF front-end such that the user has some control over the degree of I/Q mismatch by changing the mixer’s specifications.

- Implement the proposed algorithms and circuits for a IEEE 802.11g (quadrature amplitude modulation (QAM) signaling) and present results to show the validity of the proposed algorithms and circuits. The proposed techniques should be applicable to standards other than wireless local area network (WLAN) standards.
1.3 Thesis Organization

Chapter 2 describes receiver architectures in detail along with major receiver impairments and divides them into two categories: the ones that can be improved primarily by following good analog circuit design techniques and the others that can be improved using digital compensation techniques. The latter category includes DC offset, I/Q mismatch and, to a certain extent, even-order harmonic distortion. The sources of these three impairments as well as their impact on receiver performance and the variation of these impairments over temperature, process and frequency, are described in detail in Chapter 2. A brief survey of previously proposed solutions to address these impairments is also given in Chapter 2.

A new approach, complex cross-coupled quantized feedback, is introduced to solve most of the important issues of DCR and explained in detail in Chapter 3. A large number of simulations in MATLAB/Simulink are carried out to demonstrate the effectiveness of complex quantized feedback system. It is shown that a complex quantized feedback (CQFB) system can effectively correct DC offset and compensate for receiver carrier phase error as well as I/Q mismatch.

In Chapter 4, cross-coupled complex quantized feedback is implemented using digital signal processing techniques. Adaptive filters between I and Q channel data are used for correcting gain and phase mismatches. The non-idealities are estimated and complex filters are modified adaptively to compensate for I/Q mismatch and phase offset. The convergence issues of adaptive filters are also described. An example of a system with orthogonal frequency-division multiplexing (OFDM) signaling using complex quantized feedback is presented in Appendix A.
Chapter 5 describes the design and implementation of an RF-front end of IEEE 802.11g DCR, using CMOS TSMC\(^1\) 0.18 \(\mu\)m technology. The design of a low-noise amplifier, down-conversion mixer and quadrature voltage-controlled oscillator for 2.4 GHz ISM\(^2\) band is explained in detail. The down-conversion mixer is designed in a way that the I and Q mixer gain can be controlled externally. Two benefits arise from this option: First, the known I/Q mismatch can be entered to system, so this RF front-end can be used to compare different I/Q mismatch cancellation techniques. Second, if the I/Q mismatch of the RF front-end has been estimated, it can be compensated efficiently, by using the change in the gain of one of the mixers.

Chapter 6 provides conclusions and direction for future work.

\(^{1}\)Taiwan Semiconductor Manufacturing Company
\(^{2}\)The industrial, scientific and medical (ISM) radio bands were originally reserved internationally for non-commercial use of RF electromagnetic fields for industrial, scientific and medical purposes.
Chapter 2

Background

2.1 Receiver Architectures

The recent resurgence in RF transceiver design for wireless applications has been accompanied by aggressive design goals such as low cost, low power dissipation, small form factor, and high-speed data transfer. These goals are driven by the need for better portability and better affordability. To address these objectives, recent research has been focused toward the development of monolithic transceiver architectures, especially using low-cost CMOS technology [7]. It is in this context that there is renewed interest in the direct-conversion architecture [1][8][9], which is the subject of this research. In this chapter, two traditional receiver architectures will be described, followed by a brief description of DCR and low-IF architectures. Some of the issues associated with these architectures will also be presented.

2.1.1 Heterodyne Architecture

Many commercial radio receivers are designed based on a super-heterodyne architecture [7]. In its simplest form, a two-stage conversion process is used as shown in Figure 2.1. In such topologies, the input RF signal is down-converted to an intermediate frequency (IF),
where it is amplified and filtered before the final demodulation by a low-frequency demodulator. Typically, this demodulator is built to operate at frequencies below 100 MHz. Therefore, two intermediate conversions are sometimes needed to facilitate image filtering by using an additional IF sufficiently different from the RF signal. Signal amplification at IF, however, requires IF filters to be biased with large currents, causing substantial power dissipation. Further, these filters are typically off-chip passive components, adding to the receiver size and cost. Consequently, these multiple stages of filtering and amplification add to the complexity and the cost of the receiver.

![Super-heterodyne receiver diagram](image)

**Figure 2.1: Super-heterodyne receiver.**

The principal issue in super-heterodyne is the trade off between image rejection and adjacent channel suppression [1]. For given filter quality factors and losses, if the IF
is high, the image is greatly attenuated whereas nearby interferers remain at significant levels, as shown in Figure 2.2. Conversely, if the IF is low, the image corrupts the down-converted signal but the interferers are suppressed. For this reason, both the image reject filter and the channel select filter require high-selectivity and expensive analog RF filters. Because of such stringent requirements, the image rejection (IR) filter of Figure 2.2 is difficult to design. The requirements can be relaxed by using a dual-conversion (two IF) or a triple-conversion (three IF) architectures at the cost of added receiver complexity and size [9].

![Diagram of super-heterodyne receiver with image rejection filters](image)

Figure 2.2: The problem of image rejection in super-heterodyne receivers [1].
2.1.2 Image Reject Architecture

The image reject (IR) architecture attempts to address the problem of image rejection by using a complex exponential local oscillator (LO), instead of a real LO, to down-convert RF signal to the first IF frequency. The final down-conversion to baseband is also done using another complex down-conversion stage at the IF frequency. There are two common topologies of an IR architecture: Hartley [10] and Weaver [10, 11]; both work on the same principle. Figure 2.3 shows a block diagram of the Weaver architecture [12].

![Image reject (Weaver) architecture](image)

Figure 2.3: Image reject (Weaver) architecture.

In Figure 2.3, the received signal is passed through an RF filter and amplified by low noise amplifier (LNA) before entering the first complex mixer, which shifts the wanted signal to the IF frequency. The filters following the complex mixer remove frequency components at $2f_c - f_{IF}$. Next, another complex mixer translates the wanted signal to baseband. The baseband signal is then amplified, filtered and converted to the digital domain.

The most serious issue with the IR architecture is that it is vulnerable to gain and
phase mismatches between I and Q channels. As will be explained later, gain and phase mismatches cause an attenuated version of the signal at the image frequency to fold back on the wanted signal. The amount of fold back is described by image rejection ratio (IRR) and it is determined by the gain and phase mismatches between I and Q channels. Usually, the IR architecture requires two complex down-conversion stages in the analog domain and at least two filtering stages, which makes it challenging for highly-integrated designs.

2.1.3 Direct-Conversion Receiver (DCR) Architecture

One approach to reduce the number of stages in the RF front-end is to convert a received RF carrier signal down to DC (zero IF) in a single step. This is called direct conversion and is carried out in receivers known as homodyne, zero-IF, and DCR. In DCRs, the received radio frequency signals are directly converted into baseband signals; thus, separate intermediate frequency stages are not required [13, 14]. Therefore, the number of high-frequency components of a direct-conversion receiver is less than in the conventional one. Because of their simplicity, a DCR can be much more easily integrated as compared to a heterodyne receiver [1, 15]. The basic architecture of a direct-conversion receiver is shown in Figure 2.4.

In DCRs, after the desired signal is translated to the baseband, the analog-to-digital (A/D) converter and digital signal processing (DSP) circuits perform demodulation and other ancillary functions [15]. Intermediate stages are removed and the need for high-frequency IR filters is eliminated. Since bulky off-chip IR filters are no longer required,
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Figure 2.4: Direct conversion architecture

the RF LNA is not required to drive a typically low-impedance off-chip IR filter. The functions of channel selection and subsequent amplification at non-zero IF are replaced with low-pass filtering and baseband amplification, which are amenable to monolithic integration at lower power [1][7][8].

To carry out direct conversion, a local oscillator signal with the same frequency as the RF carrier is mixed with the received signal. The frequency content of the mixer output contains the sum and the difference of the LO and the carrier frequencies. Thus, copies of the spectrum of the desired signal are at twice the carrier frequency and at DC (zero Hz). The high-frequency spectrum can be removed by a suitable low-pass filter. The copy of the spectrum left at zero frequency (baseband) can be demodulated (e.g., FM\textsuperscript{1} demodulator can be used to recover an FM-modulated signal or, I/Q demodulator for an I/Q modulated signal).

\textsuperscript{1}Frequency modulation
2.2 Direct Conversion Receiver Challenges

The use of a direct-conversion receiver is not without certain drawbacks. One of the main problems, and widely-recognized, is that of DC offset. DC offset is undesired DC signal at the output of the RF front-end and can cause considerable distortion in the desired signal if it is large enough. Because DC is in the IF bandwidth, the DC offset at the RF front-end output (and that contributed by the IF amplifiers) severely limits the sensitivity of the receiver if it is not removed. Low-frequency noise sources, such as flicker noise and spurious amplitude modulation (AM), can also cause similar problems.

Figure 2.5 shows the frequency content at the output of DCR and heterodyne receivers and highlights the intermodulation distortions and other interfering signals that are of concern for each topology. In direct conversion receivers, the higher frequency components of the output can be easily removed by active or passive low-pass filtering in the baseband. However, because of the presence of the DC offsets and second-order (IM2) and third-order (IM3) intermodulations, the separation of the down-converted output from all of the extraneous signals can be challenging. In the heterodyne approach, however, DC offsets and IM2 can be easily eliminated through simple capacitive coupling, but the image interference and IM3 remain in-band. The major design considerations for a DCR can be summarized as DC offset, flicker noise, LO leakage and radiation, I/Q mismatch, and intermodulation distortion that are briefly discussed in the following.
Figure 2.5: Frequency content of heterodyne (top) and DCR (bottom) output spectrum

2.2.1 DC Offsets

The main sources of DC offset are leakage of the LO signal and RF signal self-mixing due to leakage of a near-channel interferer to the LO, as described below.

LO signal leakage into LNA and mixer

The LO signal may reach the mixer’s RF input port through the substrate or bondwire coupling, thus effectively mixing with itself and producing an unwanted DC component at the mixer output. Figure 2.6 shows the leakage of the LO signal to the input of the LNA and mixer. Since the isolation is not perfect between the LO port and the inputs of the LNA and mixer, the LO signal leaks into the input of the LNA and mixer. The leakage signal is mixed with the LO signal resulting in a constant DC offset. The level of
the offset depends on the amount of leakage and the phase shift between the LO signal and leakage. The resulting DC offset at the mixer output can be orders of magnitude larger than the desired signal.

![Diagram of LO signal leakage to input of LNA and Mixer](image)

**Figure 2.6: LO signal leakage to the input of LNA and Mixer**

**In-band interferer leakage to the LO**

The leakage of a near-channel interferer to the LO port is shown in Figure 2.7. The resulting distortion component has a DC term and a spectrum, which depends on the envelope (amplitude) modulation characteristic and average power of the interferer [16]. Moreover, the phase shift between the interferer signals at RF and LO ports of the mixer affects the power of the resulting distortion component. DC offset cancellation schemes are effective only in removing constant DC offset [17]. Since it is very difficult to remove the in-channel baseband distortion component due to RF self-mixing of an amplitude modulated interferer after down-conversion, the leakage of a near-channel interferer to the LO port of the mixer should be suppressed to a sufficiently low level.
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Figure 2.7: Near-channel interferer leakage to the LO port of mixer.

**LO signal leakage to the antenna**

Since DCR requires a LO signal frequency identical to the RF input carrier frequency, the LO signal is considered to be in-band interference. Because LO is usually a high-power signal, it can couple into the antenna, radiate out into the receiver band of other users, and saturate the RF front-end [1].

The LO signal can leak into and radiate from the antenna. The leaked LO signal may also reflect from external objects. Since the environment contains both stationary and moving objects, the magnitude and phase of the reflected LO signal varies accordingly. If the LO signal is reflected back from moving objects, the frequency of the reflected signal has a Doppler shift. Therefore, the reflected LO signal is down-converted to a nonzero baseband frequency that depends on the speed of the reflecting object. The impact of the low-frequency component generated due to the reflected LO signal depends on the amount of LO signal at the RF input. In addition, directly converting the RF signal to the baseband leads to signal filtering and amplification to be performed in the frequency band between DC and the signal bandwidth. Thus, the DC offset in the signal path is
amplified and degrades the dynamic range of the receiver. The generated DC offset due to LO signal leakage has to be suppressed to relatively lower levels to maintain the receiver sensitivity at an acceptable level [17].

![Diagram of LO signal leakage to the antenna](image)

**Figure 2.8: LO signal leakage to the antenna**

Most of the popular wireless standards only allow in-band LO radiations of less than \(-80\) dBm, which would require 80 to 90 dB isolation between the LO signal source and the antenna. High reverse isolation in the front-end and good shielding of the receiver can reduce the LO leakage and radiation; however, alternative schemes such as sub-harmonic mixing can also be used to simplify this problem by moving the LO signal out of the RF frequency band of interest [18].

**Circuit imbalance**

Another cause of DC offset is the imbalance between the two sides of a differential circuit. This imbalance can be due to threshold voltage mismatch in MOSFETs or unbalanced bias currents in the two sides of a symmetric circuit. For example, consider a differential amplifier as a baseband amplifier in I or Q path with a resistive load as shown in Figure 2.9. Assume that transistors M1 and M2 have threshold voltage mismatch and the
Figure 2.9: Differential amplifier with mismatch

Load resistors are not matched due to the process variation. The mismatches of transistors and loads are modeled as:

\[ R_{L1,2} = R_L \pm \frac{\Delta R}{2} \]
\[ V_{t1,2} = V_t \pm \frac{\Delta V_t}{2} \]

The threshold voltage mismatch makes the bias currents of the two sides unbalanced:

\[ I_{1,2} = \frac{I_B}{2} \pm \frac{I_B}{2} \left( \frac{\Delta V_t}{V_{GS} - V_t} \right) \].

The non-symmetry of the circuit, caused by these mismatches, results in DC offset voltage at the output given by:

\[ V_{DC} = \frac{\Delta R}{2} I_B + R_I B \frac{\Delta V_t}{V_{GS} - V_t} \]  \hspace{1cm} (2.1)

Therefore, it is observed that the mismatch in a differential circuit generates DC-offset.
Impact of DC Offsets on ADC Dynamic Range

The filtered output from the mixer is fed to an amplifier and then to an A/D converter (ADC). A large DC offset at the input of an ADC reduces the effective dynamic range of the ADC. DC offset can also saturate amplifiers following the mixer. In a wireless receiver, there is a trade-off between the available dynamic range of the ADC and the required filtering. A higher dynamic range ADC allows relaxed filtering requirements and vice-versa. It is hard to design cost-effective high dynamic range ADCs; therefore, it is important to reduce the DC offset at the ADC input.

Impact of DC Offset on Receiver SNR

If uncorrected, DC offset results in degraded receiver performance. This is particularly true for zero-IF receivers and with modulation schemes that have strong signal energy at DC. A few examples are Gaussian minimum shift keying (GMSK) modulation, QPSK and Quadrature amplitude modulation (QAM) followed by (root) raised-cosine filtering. A commonly used receiver performance metric is the ratio of energy per bit ($E_b$) to noise power density ($N_0$), represented as $E_b/N_0$. Baudin and Belveze in [6] give a closed-form expression of $E_b/N_0$ degradation due to DC offset for a direct-sequence code-division multiple access (DS-CDMA) system that serves as a good example to explain the problem. The modified $E_b/N_0$ is given by:

$$\frac{E_b^m}{N_0^m} = \frac{E_b^0}{N_0^0} \frac{1}{1 + \frac{dc^2}{N_0 R_c}}. \quad (2.2)$$
In Equation (2.2), $E^0_b/N^0_0$ represents $E_b/N_0$ without any receiver impairments and $R_c$ is the chip rate. $N^0_0 R_c$ is the additive white Gaussian noise (AWGN) power in the band of interest and $dc^2$ represents power in the DC signal. Hence, Equation (2.2) reveals that DC offset is as deleterious to receiver SNR as is AWGN noise.

### 2.2.2 Flicker Noise

Since the signal is directly down-converted to baseband, flicker noise causes an in-band distortion. Figure 2.5 shows the co-existence of the demodulated signal and the flicker noise in the output of a DCR receiver [19].

Flicker noise arises from random trapping of charge at the oxide-silicon interface of MOSFET\(^2\) devices. It is represented as a voltage source in series with the gate. The noise power density is given by [10]:

$$\tilde{V}_n^2 = \frac{K}{W L C_{OX}} \frac{1}{f} \tag{2.3}$$

where $W$ and $L$ are the width and length of the gate and $C_{OX}$ is the gate capacitance. $K$ is a process-dependent constant and $f$ is the frequency. Since this noise is inversely proportional to frequency, it is also called $1/f$ noise. As shown by Equation (2.3), one way of reducing flicker noise is by making the transistor dimensions larger and this is possible because the stages following the mixer in a receiver run at relatively lower frequencies; therefore, these stages can use relatively larger devices to minimize the effect of flicker noise. Another way of reducing flicker noise is to use PMOS devices instead of NMOS, because PMOS has smaller value of $K$ compared with NMOS [20].

---

\(^2\)The MOSFET is composed of a channel of n-type or p-type semiconductor material, and is accordingly called an NMOS or a PMOS
Figure 2.10: Flicker noise and concept of $1/f$ noise corner

Figure 2.10 shows flicker noise that has $1/f$ characteristics and thermal noise has flat characteristics over the frequencies of interest. This figure also defines the $1/f$ noise corner, $f_{FL}$, as the frequency at which flicker noise equals the level of thermal noise. It is highly desirable to make $f_{FL}$ as small as possible. This is of critical importance for a DCR architecture and for modulation schemes that have highest energy in the middle of the band (e.g., GMSK [21]).

Flicker noise of each individual transistor in the baseband circuitry contributes to the overall flicker noise effect; therefore, reducing the number of active devices in the baseband reduces this effect. Higher-gain front-end circuitry can also help to reduce the impact of flicker noise; however, this may compromise the overall linearity of the receiver. The choice of semiconductor process also affects the level of flicker noise associated with each active element. Compound semiconductor and silicon (Si) bipolar processes typically have
a lower flicker noise corner-frequency than the popular CMOS processes [19].

2.2.3 Amplitude and Phase Imbalances

Ideally, the sine and cosine signals from the local oscillator should be exactly 90 degrees out of phase and the gain and filtering of I and Q channels should also be identical. In practice, however, due to various imperfections that will be described later, the sine and cosine signals are not exactly 90 degrees out of phase. Also, the gain and filtering on I and Q channels do not exactly match. All of these mismatches result in the creation of an unwanted image signal that deteriorates the receiver performance.

With no mismatch, the ideal LO signal is\(^3\) \(x_{LO}(t) = 2\cos\omega_{LO}t + j2\sin\omega_{LO}t\). However, in DCRs, I and Q demodulations are typically performed in the analog domain and thus are susceptible to component mismatches. In practice, all analog components in the I and Q paths, such as oscillators, mixers, filters, and A/D converters, contribute to the total receiver imbalance. Typically, the individual imbalances between the I and Q branches in the analog parts are combined and modeled as a single gain and phase imbalance in LO signal [13, 22], \(x_{LO}(t) = 2\cos\omega_{LO}t + 2j(1 + \epsilon)\sin(\omega_{LO}t + \Delta\phi)\), where \(\epsilon\) is the gain mismatch and \(\Delta\phi\) is the phase mismatch. This I/Q mismatch causes amplitude and phase distortions in the received signal and consequently degrades the bit-error-rate (BER) of the system. Ideally, the incoming real signal is multiplied by a complex exponential \(e^{-j\omega_{LO}t}\). The effect of I/Q mismatch is equivalent to multiplying the RF signal with the following expression [10]:

\(^3\)The 2 factor is just for convenience in calculation
Figure 2.11: IRR calculation for different gain and phase mismatch.

\[ c(t) = \frac{1 + (1 + \epsilon)e^{j\Delta\phi}}{2}e^{j\omega_{LO}t} + \frac{1 - (1 + \epsilon)e^{-j\Delta\phi}}{2}e^{-j\omega_{LO}t} \]  

(2.4)

where, \( c(t) \) is the complex exponential carrier in the presence of mismatches. Note that if \( \epsilon \) and \( \Delta\phi \) are zero, the second exponential disappears. From the expression in Equation (2.4), an expression for image rejection ratio (IRR)\(^4\) can now be derived. It is simply the ratio of the amplitude of the positive exponential to the amplitude of the negative exponential. In terms of dB, this ratio is expressed as:

\[ IRR_{dB} = 10\log_{10} \frac{1 + 2(1 + \epsilon)\cos\Delta\phi + (1 + \epsilon)^2}{1 - 2(1 + \epsilon)\cos\Delta\phi + (1 + \epsilon)^2}. \]  

(2.5)

Figure 2.11 shows a graph of IRR dependence on both gain and phase mismatches. The IRR will be infinite at the origin when there are no mismatches. It drops off quickly for non-zero values of \( \epsilon \) and \( \Delta\phi \). The impact of I/Q mismatch is illustrated in Figure 2.12 in a

\(^4\)IRR is the ratio of the intermediate-frequency (IF) signal level produced by the desired input frequency to that produced by the image frequency.
constellation diagram of a 4-QAM system. The dark dots are the ideal positions whereas the light dots are due to a specific I/Q mismatch ($\epsilon = 0.1$ and $\Delta \phi = 10^\circ$). Also shown here are the time-domain effects of this mismatch on the I and Q waveforms. Note the changes in voltage levels in the quadrature phase case.

Figure 2.12: The effect of I/Q mismatch
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Sources of I/Q Mismatch

Even with careful layout and circuit design, the \( \cos(w_{LO}t) \) and \( \sin(w_{LO}t) \) signals from LO to mixer have layout and parasitics differences. These differences disturb the 90° phase difference between \( \cos(w_{LO}t) \) and \( \sin(w_{LO}t) \), resulting in phase mismatch. In addition, phase and gain mismatches are generated by the mixer itself because of MOSFET threshold voltage mismatch between the transistors in a differential circuit [23]. In general, the \( \cos(w_{LO}t) \) and \( \sin(w_{LO}t) \) signals reaching the mixer may have a phase difference that is between 80-100 degrees, i.e., a phase mismatch of \( \pm 10 \) degrees.

The gain mismatch primarily arises from the mismatch between the characteristics of transistors on the two channels used to achieve amplification and it can be as high as \( \pm 10\% \) in existing receiver implementations. Another factor that produces both phase and gain mismatches is the difference in filtering between I and Q channels.

2.2.4 Second-Order Intermodulation (IM2) Distortion

DCRs are susceptible to both odd and even order intermodulations. For the purpose of distortion analysis, the transfer characteristics of a circuit may be expressed by a Taylor series expansion:

\[
F[x(t)] = K_0 + K_1[x(t)] + K_2[x(t)]^2 + K_3[x(t)]^3 + ... \tag{2.6}
\]

The term \( K_2[x(t)]^2 \) represents the second-order nonlinearity, which can cause severe performance degradation in a DCR, especially when exposed to strong signals. Consider the
scenario in which two strong signals, \( \cos \omega_1 t \) and \( \cos \omega_2 t \), are within the bandwidth of the receiver's preselection filter but differ in frequency by an amount less than or equal to the signal bandwidth of interest (as defined by the receiver's channel select filter). When these signals are exposed to a second-order nonlinear circuit behavior, undesirable baseband spectral components are generated. These include a DC component and a baseband spectral component centered at \( \omega_1 - \omega_2 \). This is based on the fact that:

\[
(\cos \omega_1 t + \cos \omega_2 t)^2 = 1 + 0.5 \cos 2\omega_1 t + 0.5 \cos 2\omega_2 t + \cos (\omega_1 t + \omega_2 t) + \cos (\omega_2 t - \omega_1 t)
\]

Only the first and the last term (i.e., 1 and \( \cos (\omega_2 t - \omega_1 t) \)), where \( (\omega_2 - \omega_1) < \omega_{\text{channel}} \) lie within the signal spectrum. These spectral components degrade the reception of the desired signal.

Another undesirable effect is the result of exposing a single strong interferer to a second-order nonlinearity. This effect generates a beat, \( a^2(t)/2 \), directly interfering with the desired signal, as given in Equation (2.7):

\[
(a(t)\cos(\omega t + \phi(t)))^2 = \frac{a^2(t)}{2} (1 + \cos(2\omega t + 2\phi(t))) \tag{2.7}
\]

Depending on the envelope, \( a(t) \), of this single strong interferer, IM2 will generate specific baseband components affecting the performance of a DCR. For a constant envelope interferer, \( a(t) = A_c \), IM2 generates an undesirable DC component which can be treated by methods of DC offset reduction. For a non-constant envelope, \( a(t) = A_c(1 + m(t)) \), where \( m(t) \) is a function of time for amplitude modulation, the baseband beat generated from IM2 will be composed of several undesirable spectral components given by Equation
These components include a DC component, $A_c^2/2$, which can be addressed by known mitigation methods, and other more troublesome baseband spectral components, $A_c^2 [2m(t) + m(t)^2]$, for which mitigation would be very difficult. Protection of DCR against these undesirable effects requires a high second-order intermodulation rejection ratio (IMR2) between the amplitude level of the interferer(s) and resulting IM2 component. Typically, a figure of merit is specified by IIP2, which specifies a fictitious input amplitude at which the desired signal becomes equal in amplitude to the spectral component generated from IM2 (see Figure 2.13). Thus, a high IIP2 down-conversion mixer is required to minimize the effect of IM2 within a DCR [19].

### 2.3 DC offset Reduction Methods

One obvious solution to eliminate DC offset is to employ AC coupling; that is, use a highpass filter (HPF) in the down-converted data path, as in Figure 2.14(a). The transfer function of the AC coupling is $H_{AC}(s) = \frac{sRC}{1+sRC}$.

This method has some drawbacks:

1. Many modulation schemes, e.g., GMSK and QPSK or QAM followed by (root) raised-cosine pulse shaping, have significant signal energy in the center of the spectrum. The center of the spectrum lies exactly at DC after down-conversion to zero-IF. In addition to removing unwanted DC, HPF also removes the desired signal
energy and this results in degradation of BER. If the modulation has no significant DC component (i.e., if there is no information close to DC), high-pass filters can remove DC offsets without significant degradation of the signal quality. This is the case in pagers using 2-FSK. This may also be a viable option for modulation schemes that have relatively wider channel bandwidth, e.g., WCDMA\textsuperscript{5}.

2. The HPF is required to have a very small corner frequency to make sure that it does not unnecessarily filter out the spectral contents of the signal. As a rule-of-thumb, it is estimated that the 3-dB cut-off frequency of a high-pass filter should be approximately 0.1\% of the symbol rate in these systems if significant degradation

\textsuperscript{5}Wideband code division multiple access (WCDMA) is a type of 3G cellular network.
Figure 2.14: DC offset cancellation techniques using (a) capacitive coupling, (b) linear feedback; and (c) sampling

in the signal quality is to be avoided [24]. Such a low corner frequency requires prohibitively large capacitors (of the order nF) and resistors, or equivalent capacitors if implemented using switched capacitors.

3. Another major problem with AC coupling is that the coupling capacitors can take a significant time to charge up which means that the receiver can take tens of milliseconds to settle. In this regard, pre-charging techniques are often required.

Another approach is a DC feedback loop, which uses negative feedback to cancel the DC offset, as depicted in Figure 2.14(b). A DC feedback loop forms a negative feedback at frequencies close to DC, thus filtering out the DC offsets. Both the DC offset of the
input signal and the DC offsets of the amplifier are canceled at the output. The transfer function of the block diagram of Figure 2.14(b) becomes

$$H_{FB}(s) = \frac{A(sRC+1)}{1+As+sRC}.$$

A major advantage of this approach over that in Figure 2.14(a) is that it employs only grounded capacitors and can therefore utilize MOSFETs [25]. Since the capacitance density of MOSFETs is much higher than standard parallel plate structures, this approach has a major area advantage compared to that in Figure 2.14(a). However, the nonlinearity of MOS capacitors can limit the system performance. The high-gain amplifier needed in this approach can also reduce the overall linearity of the system.

A third approach uses the idle time intervals in digital wireless standards to carry out offset cancellation as shown in Figure 2.14(c). During the idle time intervals, the switch is closed and the offset is measured and stored on the capacitor. However, thermal noise of the switch mandates large values for the capacitor.

Analog as well as mixed-mode solutions have been previously proposed to address the DC offset problem. Most solutions rely on good design and layout to reduce leakage and imbalances that cause these offsets. An on-chip LO reduces DC offsets due to LO leakage, but this alone is not enough [16].

Some representative analog solutions are presented in references [2, 26–28]. All of these employ some form of a negative feedback loop to reduce DC offset. Figure 2.15 shows the architecture of the offset canceler proposed by Wang et al. in [2]. The summing amplifier has four inputs: in+ and in– are differential signals with DC offset component, Vref is a reference voltage and ctrl signal is a DC offset cancellation signal from the loop filter. The charge pump circuit will charge the loop filter if the comparator output is
high and it will discharge the loop filter if the comparator output is low. Effectively, the output of comparator will have a 50% duty cycle in the absence of any DC offset in the input signal. If there is some non-zero DC offset, this will be reflected in the duty cycle of comparator output. When the loop converges, ctrl will be adjusted to cancel the DC offset. The operation is similar to a Phase-Locked Loop (PLL). The response time and stability of this loop are determined by the charge pump and parameters of the loop filter. In summary, this solution has problems similar to an HPF and it is not sufficient by itself to remove DC offsets. As reported by Wang et al. in [2], after correction, the DC level is reduced to 5 mV and still needs further correction.

Mixed-mode offset cancellation schemes are presented in references [2–4, 26–31]. While Lindquist and Isberg [26] and Shoval et al. [31] describe only one-step offset cancellation, Nezami [29] and Yoshida et al. [3] describe a two-step cancellation. Here, the solution presented by Yoshida et al. in [3], which is depicted in Figure 2.16, will be briefly described.
In this scheme, time-invariant or static offsets are removed in the analog, or feedback, mode. The feedback loop includes ADC, averaging circuit, memory, DAC, summing circuit and LPF. Static DC offset is estimated by disconnecting the LNA from the antenna before the start of each burst.

Time-varying or dynamic offsets are canceled in the digital feed-forward mode. The same averaging circuit in Figure 2.16 is used to estimate the DC level present at the ADC output and this estimate is then subtracted from ADC output to obtain a DC free signal. The presented approach is applicable to burst-based systems and the DC estimate made on one burst is applied to the data on the following burst. This will provide acceptable results only if data in contiguous bursts have more or less the same DC value; this may not be true for practical TDMA systems, especially in the presence of...
large nearby interferers. Some solutions utilize a known training data sequence to correct for DC offsets. An example of this method is described in [30] where 5 training symbols in the preamble are used for offset correction. These schemes are not applicable to systems that do not have preamble and it also requires a very close collaboration with the digital baseband detector to achieve offset cancellation.

In references [4, 32], an even harmonic mixer is proposed that, by design, eliminates LO leakage offsets if the transconductance (Gm) mismatch is considered negligibly small. Figure 2.17 shows a single-balanced version of the CMOS even-harmonic mixer as proposed by Fang et al. in [4]. The basic principle of an even-harmonic mixer is that the input RF signal is effectively mixed with the second harmonic of the LO generated frequency. Therefore, any LO leakage from LO to RF input does not get mixed down to DC. Rather, it is translated to the LO frequency and is easily filtered by receiver filters.

![Figure 2.17: Single-balanced CMOS even-harmonic mixer [4].](image)
2.4 I/Q Mismatch Compensation

As observed in Figure 2.11, to achieve an IRR of 30 dB or larger, phase and gain mismatches of 3° and 3% (or less) are required. Such values are very hard to achieve without employing any mismatch correction techniques, either in the analog domain or in the digital domain. Both analog and digital correction techniques have been used to mitigate the effects of phase and gain mismatches. All of these techniques use some form of an adaptive algorithm to find the coefficients of a correction filter.

An example of a more recent mixed-signal technique is presented by Der and Razavi in [23]. A sign-sign (SS) least-mean squares (LMS) method is used to calibrate gain and phase errors of a Weaver image-reject receiver to achieve an IRR of 57 dB.

A pure analog approach is presented by Behbahani et al. in [33]. A five-stage polyphase filter is used to achieve an IRR of 60 dB for wireless LAN applications. As explained in [33], the higher the number of polyphase filter stages, the higher the IRR. However, the area impact of this technique precludes its use in a low-cost, low-power design.

Amongst the digital methods, the work of Yu and Snelgrove [34] is representative of signal separation techniques in the digital domain to improve receiver image rejection. A complex LMS algorithm is employed to separate the image from signal.

Two other techniques are presented in references [35, 36]. Valkama and Renfors [36] proposed a method that requires separate complex digital mixers and filters for the image and signal paths to achieve a cleaner reference signal for LMS/RLS\(^6\) adaptation. Having separate demodulation and filtering paths for signal and image is an unnecessary compli-

\(^6\)The LMS (least means square) and RLS (recursive least squares) algorithms used for determining the coefficients of an adaptive filter.
cation. Tubbax et al. in [35] assumed that the training sequence is available as part of the preamble of a TDM burst. This is not true for some of the wireless standards such as GSM [21], where the training sequences are in the midamble.

2.5 Summary

In this chapter, different receiver architectures have been reviewed, and since DCR has the lowest cost and power, this work focuses on it. DCR design issues have been addressed in detail, and the existing methods to address these problems have been reported.

As mentioned before, DC offset, flicker noise and I/Q mismatch issues should be resolved carefully in DCR design. The existing methods to address these problems are divided in two categories, analog and digital. The trend is to perform as much as possible in the digital domain and to minimize the RF front-end (analog). Also, most of these methods focused on the problem for a specific case (a standard or a system) rather than providing a general solution. In the next chapters, we introduce a novel system-level approach which addresses DC offset, flicker noise and I/Q mismatch problems more generally, and can be implemented in digital or analog.
Chapter 3

Complex Quantized Feedback

As emphasized in previous sections, there is a need to address the important issues of DCR design including DC-offset, baseline wander effect, I/Q mismatch and low-frequency noise. In this chapter, we address these issues with a general approach applicable to an arbitrary DCR receiver. The basic idea is to use the information available in the I and Q paths to minimize the effect of low-frequency noise, phase error, and mismatch in both paths. Communication systems using quadrature demodulation whose baseband signal spectrum have considerable energy near DC can benefit from this approach.

3.1 Overview of the New Approach

First a simple QFB system is used in both I and Q channels to reduce the effects of baseline wander due to AC-coupling as well as the effects of 1/f noise. Then, the use of complex (in the mathematical sense) cross-coupled QFB is proposed and it is shown that the system can reduce the undesired effects of carrier phase error and I/Q mismatch.

A cost-effective approach to remove such low-frequency disturbances is to use simple AC-coupling, i.e., a high-pass filter (HPF) in the down-converted signal path. This approach has been successfully applied in pager systems to receive frequency-shift-keying
(FSK) modulated signals [8][37]. Since the baseband spectrum of FSK signal has little energy around DC, AC-coupling allows low-frequency disturbance to be removed with minimal distortion to the signal spectrum.

For more spectrally efficient modulation schemes, such as quadrature amplitude modulation, the baseband signal spectrum has significant energy at low frequencies. Employing AC-coupling HPF in the I and Q paths, as shown in Figure 3.1, can remove and/or minimize the unwanted effects of DC-offset and $1/f$ noise. However, this filtering also removes low-frequency portions of the desired signal. The filtering of the desired signal can cause significant performance loss and introduce severe intersymbol interference (ISI) [9].

Figure 3.1: A direct-conversion receiver with AC-coupling

This inadvertent filtering out of the information bearing the low-frequency part of the signal, typically referred to as baseline wander (in connection with one-dimensional modulation schemes such as pulse amplitude modulation), makes the detection of the signal difficult and causes reduction of noise margin [38][39].

To remove the baseline wander effect introduced by AC-coupling, a quantized feed-
back (QFB) circuit can be used [40]. QFB is a DC restoration technique in which the low-frequency components of the desired signal are restored by post-decision feedback. Employing QFB is essential for operation with input patterns having large low-frequency content [41]. For example, in 100 BASE-T Fast Ethernet systems, QFB is used to reduce the baseline wander effect [42]. A conceptual block diagram of QFB (also known as baseline wander correction) is shown in Figure 3.2. The corresponding time-domain waveforms at different nodes of the system are also shown.

The basic idea behind this scheme is as follows: the low-pass filter (LPF) in the feedback path restores the low-frequency components from the output signal (assuming correct decisions) and adds it to the high-pass filtered input signal to reconstruct the entire spectrum [40][43][44]. Ideally, the LPF in the feedback loop has the same order and cut-off frequency as the HPF in the feed-forward path. A cross-coupled (CC) QFB, an extension of the simple QFB system, is the one of the main contributions in this dissertation, and is described in more detail in the next section.

![Figure 3.2: Conventional quantized feedback technique](image-url)
Simple AC-coupling and quantized feedback can be combined to obtain a cost-effective approach for removal of DC-offset and 1/f noise. This scheme is shown in Figure 3.3.

The received signal is down-converted into its I and Q components with high-pass filters $H_{ACI}(s)$ and $H_{ACQ}(s)$ performing AC-coupling in I and Q branches, respectively, and low-pass filters, $H_{II}(s)$ and $H_{QQ}(s)$, complete the QFB system.

![Figure 3.3: Simple system including high-pass filter and quantized feedback](image)

To improve this basic system, we propose the use of cross-coupled feedback circuits [45] to compensate for the carrier phase error and/or I/Q mismatch and to eliminate the crosstalk between the in-phase and quadrature paths. Figure 3.4 shows such a system which can be considered as a complex QFB system. Cross-coupled filters are added between the two channels for carrier phase error compensation and/or I/Q mismatch.
correction. $H_{IQ}(s)$, for example, represents the feedback system from in-phase channel to quadrature channel. $H_{ACI}(s)$ and $H_{ACQ}(s)$ are the transfer functions of the AC-coupling blocks in the in-phase and quadrature channels. The purpose of the in-phase feedback blocks, $H_{II}(s)$ and $H_{QQ}(s)$, is DC restoration.

![Figure 3.4: Complex QFB system](image)

In this complex QFB system, assuming that the properties of the high-pass filters, $H_{ACI}$ and $H_{ACQ}$, are known, it is possible to derive the expressions for other filters in the system (namely, $H_{II}$, $H_{IQ}$, $H_{QI}$ and $H_{QQ}$) that achieve approximate carrier phase error compensation and/or I/Q mismatch correction.

Suppose the received signal is $r(t) = a(t)\cos(\omega_c t) + b(t)\sin(\omega_c t)$, where the carrier frequency is $\omega_c$, and $a(t)$ and $b(t)$ are information bearing baseband signals. As is done in
in the context of an equalizer, if we assume that there are no decision errors, one can replace the output signals $\hat{a}$ and $\hat{b}$ with $a$ and $b$, respectively. Therefore, in the Laplace transform domain, we can write:

\[
X(s) = H_{ACI}(s)I(s) + H_{II}(s)A(s) + H_{QI}(s)B(s) \quad (3.1)
\]

\[
Y(s) = H_{ACQ}(s)Q(s) + H_{QQ}(s)B(s) + H_{IQ}(s)A(s). \quad (3.2)
\]

Also, under ideal conditions and in the absence of noise, the slicer’s output is the same as its input: $X(s) = A(s)$ and $Y(s) = B(s)$. Using the above equations and assumptions, the QFB filters’ transfer function can be derived, as discussed in the following subsections.

### 3.2 Carrier Phase Error Compensation

In this section, we assume that there is a carrier phase error $\theta$ between the transmitter and receiver LO. That is, both in-phase and quadrature LO signals encounter the same carrier phase error, $\theta$. It is shown that a cross-coupled QFB system can be used for compensating this carrier phase error.

Recall that the received signal is $r(t) = a(t)\cos(\omega_c t) + b(t)\sin(\omega_c t)$. Now let us assume that the carrier recovery system in the receiver has successfully recovered the carrier frequency; however, there is still a residual carrier phase error $\theta$. That is, the LO signals are $x_{LO,I}(t) = \cos(\omega_c t + \theta)$ and $x_{LO,Q}(t) = \sin(\omega_c t + \theta)$. Multiplying $r(t)$ by these two LO signals and filtering out the higher frequency components, the following baseband signals are obtained: $x_{BB,I}(t) = a(t)\cos \theta - b(t)\sin \theta$ and $x_{BB,Q}(t) = b(t)\cos \theta + a(t)\sin \theta$. Note
that the I and Q signals are now correlated and, in the s-domain, we have:

\[ I(s) = \alpha A(s) - \beta B(s), \]  
\[ Q(s) = \alpha A(s) + \beta B(s), \]

where \( \alpha = \cos \theta \) and \( \beta = \sin \theta \).

At the summing nodes of Figure 3.4 in the I and Q signal paths, we have:

\[ A(s) = H_{ACI}(s)I(s) + H_{II}(s)A(s) + H_{QI}(s)B(s) \]  
\[ B(s) = H_{ACQ}(s)Q(s) + H_{QQ}(s)B(s) + H_{IQ}(s)A(s) \]

Substituting \( I(s) \) and \( Q(s) \) from Equation (3.3) and (3.4) into (3.5) and (3.6), we obtain:

\[ 0 = \{\alpha H_{ACI}(s) + H_{II}(s) - 1\}A(s) + \{-\beta H_{ACI}(s) + H_{QI}(s)\}B(s) \]
\[ 0 = \{\beta H_{ACQ}(s) + H_{IQ}(s)\}A(s) + \{\alpha H_{ACQ}(s) + H_{QQ}(s) - 1\}B(s) \]

Therefore, the following relationships can be established between the six filters:

\[ H_{II}(s) = 1 - \alpha H_{ACI}(s) \]  
\[ H_{QI}(s) = \beta H_{ACI}(s) \]  
\[ H_{IQ}(s) = -\beta H_{ACQ}(s) \]  
\[ H_{QQ}(s) = 1 - \alpha H_{ACQ}(s) \]
This shows that the four QFB filters, $H_N$, $H_IQ$, $H_QI$ and $H_QQ$, are functions of the AC-coupling filters and residual carrier phase error. Assuming that Equation (3.7)-(3.10) are satisfied, the crosstalk can be minimized. Note that, in practice, the assumption of no decision errors is only valid for small phase errors, as confirmed by simulation results in Sections 3.3 and 3.4.

3.2.1 I/Q Mismatch Compensation

I/Q mismatch can be characterized by two parameters: the amplitude or gain imbalance between I and Q branches, $\epsilon$, and the phase orthogonality mismatch, $\Delta \phi$. Therefore, the LO signal for I and Q branches can be written as:

$$x_{LO,I}(t) = 2\cos\omega_C t$$
$$x_{LO,Q}(t) = 2(1 + \epsilon)\sin(\omega_C t + \Delta \phi)$$

After multiplying the received signal by the two LO components and low-pass filtering the result, we obtain the following baseband signals:

$$x_{BB,I}(t) = a(t)$$
$$x_{BB,Q}(t) = (1 + \epsilon)a(t)\sin\Delta \phi + (1 + \epsilon)b(t)\cos\Delta \phi$$

or equivalently:

$$I(s) = A(s) \quad (3.11)$$
Chapter 3. Complex Quantized Feedback

\[ Q(s) = [(1 + \epsilon)\sin\Delta\phi]A(s) + [(1 + \epsilon)\cos\Delta\phi]B(s). \] (3.12)

Substituting \( I(s) \) and \( Q(s) \) from the above in the Equations (3.5) and (3.6), we obtain:

\[
\begin{align*}
H_{II}(s) & = 1 - H_{ACI}(s) \quad (3.13) \\
H_{QI}(s) & = 0 \quad (3.14) \\
H_{IQ}(s) & = -(1 + \epsilon)\sin\Delta\phi H_{ACQ}(s) \quad (3.15) \\
H_{QQ}(s) & = 1 - (1 + \epsilon)\cos\Delta\phi H_{ACQ}(s) \quad (3.16)
\end{align*}
\]

In the presence of both carrier phase error and I/Q mismatch, we have:

\[
\begin{align*}
H_{II}(s) & = 1 - \cos\theta H_{ACI}(s), \quad (3.17) \\
H_{QI}(s) & = \sin\theta H_{ACI}(s), \quad (3.18) \\
H_{IQ}(s) & = -(1 + \epsilon)\sin(\theta + \Delta\phi) H_{ACQ}(s), \quad (3.19) \\
H_{QQ}(s) & = 1 - (1 + \epsilon)\cos(\theta + \Delta\phi) H_{ACQ}(s), \quad (3.20)
\end{align*}
\]

By satisfying these equations, the effects of these non-idealities on BER can be minimized.

3.3 Simulation Results

To demonstrate the advantages of the use of simple and complex QFB in AC-coupled integrated receivers, a DCR using a 4-QAM scheme is simulated. In all simulations, root-raised-cosine pulse-shaping filters with 30% excess bandwidth are used. A flat communi-
cation channel with AWGN is considered. The simulations are performed using MATLAB and Simulink. The simulation results for the base system, i.e., AWGN channel with no AC-coupling are verified with the theoretical bit error rate versus SNR per symbol for square M-QAM constellations [47] to ensure testbench correctness. Further simulations on the testbench are then carried out to illustrate the benefits of employing simple and complex QFB in an AC-coupled DCR. Each simulation is performed with a set of noise levels (resulting in SNRs between 0dB and 12dB). Depending on the noise level, an adequate number of symbols are transmitted and received to collect reliable results. For each SNR level, the corresponding BER is calculated. Simulation results are presented using BER versus SNR graphs.

The results of the first simulation demonstrate the effect of baseline wander caused by AC-coupling, as shown in Figure 3.5. In this setup, a first-order HPF \( H_{ACI} = H_{ACQ} = \frac{s}{s + 2\pi f_c} \) is added in the received I and Q baseband paths (as shown in Figure 3.1). It is seen that BER increases significantly as the HPF cut-off frequency \( f_c \) increases, primarily due to baseline wander effects. Note that the cut-off frequency of HPF is normalized to the baud rate of the system. It can be seen that when the cut-off frequency of the HPF is below 0.1% of the data rate, BER degradations are negligible, as mentioned in [1].

Since the amount of ISI introduced increases as the AC-coupling cut-off frequency increases, a smaller cut-off frequency for the AC-coupling filters is preferable. However, the smaller the cut-off frequency of the AC-coupling filter, the larger is its associated time constant, resulting in a slower response time. On the other hand, in connection with DC-offset and \( 1/f \) noise removal, a larger cut-off frequency of the AC-coupling filter is more
Figure 3.5: Simulation results (DCR with HPF of different cut-off frequencies)

desirable. Therefore, the selection of the AC-coupling cut-off frequency requires a careful balance between two conflicting objectives: minimizing ISI and maximizing immunity against DC-offset and $1/f$ noise.

To compensate for baseline wander effects, a simple QFB (DC-restorer) is added to the I and Q baseband paths, as illustrated in Figure 3.3. It can be seen from Figure 3.6 that the BER performance of the system is noticeably improved compared to that of Figure 3.5 where no QFB is used.

Further simulations are performed in Figure 3.7 to show the effect of the residual
carrier phase error in the receiver's LO. First, a system with HPF cut-off frequency of 1% of the baud rate and simple QFB DC-restorer is used as the base system. A set of phase errors (referred to as ph in the simulation results) from 0° to 20° are applied to the system. Figure 3.7 shows the BER versus SNR curves in the presence of different phase errors. It is worth noting that when the carrier phase error is below 1°, the performance degradation of the overall system due to carrier phase error is negligible. However, when carrier phase error becomes larger, system performance is considerably degraded.

To compensate for carrier phase error in an AC-coupled DCR, a complex QFB system
Figure 3.7: Simulation results (DCR with HPF, QFB and carrier phase error)

similar to Figure 3.4 is simulated. The complex QFB blocks are designed according to the equations derived in Section 3.2. The simulation results are presented in Figure 3.8.

A comparison between Figure 3.7 and Figure 3.8 indicates that, relative to simple QFB, complex QFB drastically improves the BER performance of an AC-Coupled DCR in the presence of carrier phase error. As another illustrative comparison, Figure 3.9 shows simulation results of a DCR in the presence of HPF and carrier phase error without any QFB. As can be seen by referring back to Figure 3.8, complex QFB compensates the carrier phase error and, especially for phase errors of 10° or smaller, the result is very close
Figure 3.8: Simulation results (DCR using complex QFB with carrier phase error)

to ideal. By comparing the results illustrated in Figure 3.7, Figure 3.8, and Figure 3.9 the effectiveness of the simple QFB and the improvement due to the complex QFB approach are validated.

In all these experiments, carrier phase error is assumed to be constant and known, but in reality carrier phase error may change with time, and it is unknown. To verify the performance of the proposed system in the presence of time-varying carrier phase error, systems with the carrier phase error shown in Figure 3.10 are simulated.

This time-varying phase is given as a carrier phase error to different systems. First,
a system is simulated with only HPF (cut-off frequency=1% of the baud rate), then a system with HPF and simple QFB, and finally a system with the complex QFB. The result is shown in Figure 3.11. Since the carrier phase error is changing with time, the result is shown as cumulative error versus time. As can be seen from this figure, the performance improvement due to the complex QFB is significant. The result of complex QFB is very close to an ideal system without any carrier phase error.

Also, simulations are performed to show the effect of I/Q mismatch. First, a system with amplitude mismatch ($\epsilon = 10\%$) and phase mismatch ($\Delta \phi = 10^\circ$) is considered.
Figure 3.10: Time-varying carrier phase error

Figure 3.11: Simulation result of time-varying carrier phase error effect on different systems
Several scenarios are considered: 1) a system with only HPF with cut-off frequency of 1% of the baud rate, 2) a system with HPF and simple QFB, and 3) the complete system including HPF and complex QFB. In Figure 3.12, the results are compared with that of an ideal system (without I/Q mismatch). The effectiveness of the proposed complex QFB approach for I/Q mismatch compensation can be seen from this figure.

![Figure 3.12: Simulation result of I/Q mismatch ($\epsilon = 10\%$ and $\Delta \phi = 10^\circ$) effect on different systems](image)

Figure 3.12: Simulation result of I/Q mismatch ($\epsilon = 10\%$ and $\Delta \phi = 10^\circ$) effect on different systems

Figure 3.13 shows the simulation results for a system with different I/Q mismatch parameters (different amplitude and phase mismatch). As can be seen from this figure, the performance of the system in the presence of different mismatch parameters are very
close to the case where there is no mismatch. This indicates the effectiveness of the complex QFB approach in compensating I/Q mismatch, assuming that the I/Q mismatch parameters are known.

Any carrier phase error estimation scheme is prone to inaccuracies, but the system should be able to tolerate them to some degree. To show that the proposed system is relatively robust to inaccuracies in carrier phase error and mismatch estimations, the system is simulated with different values for these errors.

In the first experiment, the complete system including HPF, QFB and cross-coupled
filters is simulated in the presence of noisy phase error estimations (Figure 3.14). The effect of an inaccurate carrier phase error estimation is modeled by adding a random zero-mean Gaussian variable to the nominal value of the phase error. The standard deviation of this variable is 5% of the nominal value of the carrier phase error.

To demonstrate that the proposed system is stable to error in the carrier phase error and mismatch estimation, the system with different types of error has been simulated. In first experiment, the complete system including HPF and QFB and cross coupled filter with carrier phase error was simulated. These results are shown in Figure 3.14. Here we assumed that the estimation of the real carrier phase error in the system is not accurate and is a random number with the same average as the real carrier phase error and 5% standard deviation.

As observed in Figure 3.14, the results for accurate and noisy carrier phase error estimations are comparable. That is, the system is capable of tolerating a modest amount of noise in the estimation of the carrier phase error.

The next experiment is designed to examine the behavior of the system with I/Q mismatch in the presence of noise and estimation errors (Figure 3.15). The complete system, including HPF and QFB and cross-coupled filters, is simulated first with mismatch parameters of $\epsilon = 5\%$ and $\Delta \phi = 5^\circ$. Then, the system with the same mismatch parameters, but with an error (zero-mean Gaussian with a 5% relative standard deviation) in mismatch estimation is simulated. The next simulation is for the system with time-varying I/Q mismatch parameters at the LO signal with a 5% standard deviation. In the last step, the system with the same mismatch parameters as before, plus 2% and $2^\circ$ mismatch in the
QFB is simulated. The results show that the system is robust with respect to estimation errors of carrier phase error and mismatch, as well as variable mismatch parameters at the LO and mismatch in QFB.

### 3.4 Design Issues

In this section, some design issues of complex QFB systems are discussed. Since the objective of this work is to develop a cost-effective and integrable technique for DC-offset removal and carrier phase error and/or I/Q mismatch compensation, a receiver design
Using CQFB in addition to AC coupling can make an AC coupling a practical solution. Since the CQFB technique recovers the low-frequency part of the desired signal, it can be used for modulation with low-frequency or DC component, and also the HPF is not required to have a very small corner frequency to make sure that it does not unnecessarily filter out the spectral contents of the signal.

In the complex QFB system, shown in Figure 3.4, each AC-coupling filter can be a simple first-order HPF. However, the design of the four feedback and cross-coupling filters

Figure 3.15: Simulation result for effect of noise in system with mismatch estimation that uses this technique should deliver on these objectives.
is more involved. Ideally, these filters have to be monolithic and they need to be adjustable or adaptive to track the possible changes in the carrier phase error of the receiver LO. Therefore, one of the key challenges is the design of adaptive filters.

### 3.4.1 Design Considerations for Adaptive Filters

At low data rates, adaptive filtering is easily and efficiently performed using digital circuits. On the other hand, analog filters are preferable at high speeds when low power consumption, small integrated area, and moderate linearity are required [48].

The designer of a modern analog adaptive filter is required to simultaneously consider both system-level and circuit-level issues. The first step is to choose an adaptive algorithm. The algorithm adjusts the parameters of the filters to optimize their performance in an unknown and possibly time-varying environment. Two widely-used adaptive algorithms for filters are least-mean-square (LMS) algorithms and heuristic algorithms [48][49].

The best adaptive algorithm for a particular situation is often dictated by the filter’s structure. An important criterion in selecting a filter structure is that a suitable adaptive algorithm exists, preferably with a straight-forward and robust hardware implementation. Also, the filter structure should not go unstable during adaptation. Possible choices of filter structure are transversal filters, biquad filters, Laguerre filters, and orthonormal ladder filters [48][49].
3.4.2 Experiments on Adaptive Filters

Considering the equations for low-pass filters and cross-coupled filters, the adaptive design for two cross-coupled filters is relatively straight-forward, because the changes in the carrier phase error merely affect the gain of the filters. However, for low-pass filters in the QFB, the changes in the carrier phase error affect both gain and cut-off frequency characteristics of the filters.

Several experiments on the behavior of the feedback filters in the QFB system were conducted. For a system with known HPF (AC-coupling filter), the transfer functions of the feedback QFB filters for different values of carrier phase error are shown in Figure 3.16. It should be noted that the poles and zeros of $H_{IQ}$ and $H_{QI}$ filters are fixed. However, for $H_{II}$ and $H_{QQ}$ filters, the poles are fixed, but the zeros positions alter as the carrier phase error changes. Therefore, the cut-off frequencies of the $H_{II}$ and $H_{QQ}$ filters change slightly as a function of carrier phase error.

For a first-order HPF with cut-off frequency, $f_c$, the cut-off frequency of the QFB filters for different phase errors can be calculated as:

$$f_{cut-off} = \frac{f_c}{\sqrt{1 - 2(1 - \cos\theta)^2}}$$  \hspace{1cm} (3.21)

The results for different phase errors are plotted in Figure 3.17. When there is no carrier phase error, the LPF cut-off frequency is the same as that of the HPF. When there is carrier phase error, it increases rapidly beyond 30° in the manner shown in Figure 3.17. For phase errors smaller than 30°, the change of cut-off frequency is negligible. This
observation is very important in design, because there are some clever single QFB circuits (same cut-off frequency for low-pass and high-pass) [38] that would be useful for systems with small phase errors.

### 3.4.3 Carrier Phase Error Estimation

Of course, carrier phase error in the receiver LO can be time-varying. In order to accomplish carrier phase error compensation in this case, the QFB filters account for a time-varying carrier phase error. As a consequence, the ability to estimate or detect the carrier phase error is required. In the following, one of the standard methods of carrier
On the topic of carrier recovery in [46], a method to estimate carrier phase error is discussed. In the equation below, \((x_k, y_k)\) and \((\hat{a}_k, \hat{b}_k)\) are samples of the received signal before and after the decision maker (the slicer), respectively. Samples of carrier phase error in the demodulator are denoted as \(\theta_k\). Carrier phase error can be estimated with the following expression [46]:

\[
\theta_k = \sin^{-1}\left(\frac{\text{Im}\{(x_k + jy_k)(a_k + jb_k)^*\}}{|a_k + jb_k|^2}\right)
\]

In Figure 3.18, a system that attempts to implement the above technique to estimate the carrier phase error and accordingly calculate the complex filters is shown. Note that the estimation of carrier phase error is mathematical, but the implementation can be
carried out using techniques such as look-up tables. The results of the experiments for this system are shown in Figure 3.19. As seen in this figure, the performance of the system for phase errors smaller than 10° is very close to ideal.

### 3.5 Summary

In direct conversion receivers using bandwidth-efficient modulation-schemes (e.g., QAM), DC-offset and 1/f noise are problematic. If they are not compensated for, the overall system performance will deteriorate. It is shown that a complex QFB system can effectively correct baseline wander effect and compensate for receiver carrier phase error as well as I/Q mismatch. A large number of simulations in MATLAB/Simulink were carried out to
Chapter 3. Complex Quantized Feedback

Figure 3.19: Simulation result (Complex QFB with phase estimator)

demonstrate the effectiveness of complex quantized feedback system.

Design considerations for adaptive filtering has been described, and based on the experiments, we found that for small amount of phase error, the changes in the filters characteristics are not significant. Also, a standard method to estimate the receiver's carrier phase error was reviewed. It is observed that, for carrier phase error of less than 10°, the system performs reasonably well when the carrier phase error is estimated using the aforementioned standard method.
Chapter 4

Adaptive Digital Signal Processing Techniques for CQFB

4.1 Introduction

One of the main trends in the evolution of radio receivers and other wireless devices is to implement more and more of the receiver functionalities using digital signal processing (DSP). The design and implementation of radio receivers for wireless terminals is currently dictated by the strong push towards flexible and software configurable receiver structures able to operate over multiple frequency bands. The terms multimode, multiband, and multistandard radios are commonly used in this context. A key ingredient in building flexible radios is the efficient use of DSP.

Enabled by the recent advances in DSP techniques, both at the algorithmic and the implementation levels, as well as in the ADC technologies, more and more of the receiver functionalities can be implemented using DSP. However, due to the fundamental gap in the used radio frequencies (typically on the order of 1 to 10 GHz) and supported maximum sampling frequencies (up to a few hundred megahertz, depending on the needed resolution and dynamic range), some receiver analog front-end stages are still needed. With the
ever-increasing demand for the system performance and supported data rates on one side, and the terminal flexibility and implementation costs on the other, the requirements for these remaining analog front-end stages become extremely challenging to achieve. One interesting idea in this context is to apply sophisticated DSP-based techniques to compensate for some of the most fundamental nonidealities of the receiver analog front-end.

The proposed mitigation techniques are based on purely digital processing of the received signal and can be used to suppress distortions including carrier phase error, I/Q mismatch, DC offset and other low frequencies disturbances. In this chapter, we focus on developing and demonstrating the application of CQFB techniques to mitigate the effects of the analog RF front-end using digital adaptive filtering. The approach in general is practically-oriented and largely based on analyzing and processing measured real-world receiver front-end signals.

Our approach is illustrated in Figure 4.1 which shows where the DSP implementation of CQFB fits into the overall system. The figure depicts a simplified receiver, from antenna (input) to detected symbol (output). As mentioned before, it is desirable to minimize the analog front-end. Therefore, the CQFB is implemented in a DSP processor after A/D converters.
4.2 I/Q Down-Conversion Based Front-End

4.2.1 I/Q Processing Principles

Understanding the nature of bandpass signals and systems is the key in building efficient radio transmitters and receivers. In addition to the basic envelope and phase representation, the so-called I/Q (in-phase/quadrature-phase) interpretation forms the basis for various spectrally-efficient modulation and demodulation techniques [46].

More generally, I/Q processing can be used in the receiver and transmitter front-end for efficient up/down conversion processing, independently of the applied modulation
Chapter 4. Adaptive Digital Signal Processing Techniques for CQFB

Given a general bandpass signal:

\[
2\text{Re}[x(t)\exp(j\omega_0 t)] = x(t)\exp(j\omega_0 t) + x^*(t)\exp(-j\omega_0 t)
\]

\[
= 2x_I(t)\cos(\omega_0 t) - 2x_Q(t)\sin(\omega_0 t)
\]

the (formal) baseband equivalent \( x(t) = x_I(t) + jx_Q(t) \) can be recovered by multiplying the modulated signal with a complex exponential and low-pass filtering. This is illustrated in Figure 4.2, which also depicts the practical implementation structure based on two parallel real signals. In the receiver architecture context, the differences come basically from the interpretation of the down-converted signal structure. In general, both the direct-conversion and low-IF receivers utilize the I/Q down-conversion principle and are discussed in more detail in the following.

![Diagram](image)

Figure 4.2: Basic I/Q downconversion principle in terms of: (a) complex signals and (b) parallel real signals.
4.2.2 Architectural Aspects

As mentioned before, DCR or homodyne receiver is based on the idea of I/Q down-converting the channel of interest from RF directly to baseband. Thus, in a basic single-channel context, the down-converted signal after low-pass filtering is basically ready for modulation-specific processing such as equalization and detection. This is, in general, an interesting approach in the sense that it eliminates the use of any IFs results in a rather simple front-end processing, especially in terms of the needed RF/IF filtering.

In the previous chapter, we showed that by using a complex quantized feedback (Figure 3.4), the circuit design criteria can be simplified. The proposed receiver architecture mitigated DC offset, carrier phase error and I/Q amplitude and phase mismatches. They, however, assumed that the mismatch and error parameters are known (except for DC offset which is removed blindly). These parameters are then used to compute the decision feedback filters.

In previous works, e.g. [50, 51], complex quantized structures were used to mitigate non-idealities of a DCR architecture. Although they do not assume that the non-idealities are known, both methods require a training mode prior to operation. We assume that the baseband signals after mixing are fed to the matched filters before being digitized. In Figure 4.3, the matched filters and anti-aliasing filters are represented as baseband filters. This way, the required sampling rate equals the symbol rate of the system – much less than the sampling rate necessary to perform matched filtering digitally.

Following the previous chapter, we model the effects of noise \((n_i, n_q)\), carrier phase error \((\theta)\), phase mismatch \((\Delta \phi)\), DC offset \((i_{DC} \text{ and } q_{DC})\) and amplitude mismatch \((\varepsilon)\) on
the receiver signal \((a[n], b[n])\) by the formula given below:

\[
\begin{pmatrix}
i[n] \\
q[n]
\end{pmatrix} = \begin{pmatrix}
cos \theta & -\sin \theta \\
(1 + \epsilon) \sin(\Delta \phi + \theta) & (1 + \epsilon) \cos(\Delta \phi + \theta)
\end{pmatrix} \begin{pmatrix}
a[n] + n_i[n] \\
b[n] + n_q[n]
\end{pmatrix} + \begin{pmatrix}
i_{DC} \\
q_{DC}
\end{pmatrix},
\]

(4.1)

where \(\begin{pmatrix} i[n] \\ q[n] \end{pmatrix}\) is the digitized QAM signal to be demodulated digitally. The effects of the noise and other non-idealities are illustrated in Figure 4.4. The results of a high SNR= 20 dB are provided in Figure 4.4(a), and a low SNR= 5 dB in Figure 4.4(b). They are superimposed on the ideal 16-QAM constellation. Clearly, the effects of \(\theta, \epsilon, \Delta \phi,\) and DC offset are significant when no compensation is performed, especially for low SNR values.
4.3 Adaptive implementation of complex QFB

4.3.1 DC-offset removal filters

To keep the detector circuit simple, we have to remove any DC offset prior to detection. A computationally-efficient way of removing the DC offset is to use a recursive first-order filter given by the following equation:

\[ y[n] = \frac{1+\alpha}{2}(x[n] - x[n-1]) + \alpha y[n-1] \]  \hspace{1cm} (4.2)

in which \( x[n] \) and \( y[n] \) denote the input and output signals of the filter, respectively (not to be mistaken with I/Q signals before decision). The frequency response of this filter is shown in Figure 4.5. By choosing an \( \alpha \) closer to one, a sharper transition to zero \(( -\infty \)
in dB) can be achieved at the cost of a longer time constant. The problem with a very sharp first-order filter is that it can become unstable when implemented in fixed-point arithmetic. In such a case, one may opt for a higher-order filter, which provides the same sharp transition to zero and remains stable when implemented in fixed-point [52].

Figure 4.5: Frequency response of the first order DC-offset removal filter for $\alpha = 0.9$.

### 4.3.2 Complex QFB receiver

We begin by assuming that the symbols are still uncorrelated at the output of the DC offset removal filter\(^1\). Thus, the feedback filters given by Equations (3.17) to (3.20) can

\(^1\)Later in section 4.3.6, the system with ISI is considered.
be simplified to the following:

\[ H_{II}(z) = 1 - \cos\theta, \]
\[ H_{QI}(z) = \sin\theta, \]
\[ H_{IQ}(z) = -(1 + \epsilon)\sin(\theta + \Delta\phi), \]
\[ H_{QQ}(z) = 1 - (1 + \epsilon)\cos(\theta + \Delta\phi), \]

which are simply gains. Let us define

\[
H = \begin{pmatrix} H_{II} & H_{QI} \\ H_{IQ} & H_{QQ} \end{pmatrix} = \begin{pmatrix} 1 - \cos\theta & \sin\theta \\ -(1 + \epsilon)\sin(\Delta\phi + \theta) & 1 - (1 + \epsilon)\cos(\Delta\phi + \theta) \end{pmatrix} \quad (4.3)
\]

Therefore, the complex quantized feedback detector should solve the following nonlinear equation for \((x[n] y[n])^T\) to detect each received symbol:

\[
\begin{pmatrix} x[n] \\ y[n] \end{pmatrix} = \begin{pmatrix} i_{no\text{DC}}[n] \\ q_{no\text{DC}}[n] \end{pmatrix} + H \cdot Q \begin{pmatrix} x[n] \\ y[n] \end{pmatrix} \quad (4.4)
\]

in which \((i_{no\text{DC}}[n] q_{no\text{DC}}[n])^T\) denotes the output of DC-offset removal filters for each symbol, and \(Q(x[n] y[n])^T\) is the detected symbol. The quantizer function \(Q(.)\) becomes \(\text{sgn}(.)\) in the case of 4-QAM signaling. A computationally efficient algorithm to solve this nonlinear equation is given in the following pseudo-code segment, in which IQ represents \((i_{noDC}[n] q_{noDC}[n])^T\). One may argue that it suffices to find one \((x[n] y[n])^T\) to satisfy the equation above. That is actually true in close-to-ideal detection (i.e., when noise and
other non-idealities are small). In other cases, Equation (4.4) may have multiple solutions, among which we are interested in the one that minimizes the error (i.e., the distance from the ideal constellation).

\[ AB = \text{All possible detected QAM symbols;} \]
\[
// \text{For example } AB = \{(-1, 1), (1, -1), (-1, -1), (1 1)\} \text{ in } 4\text{-QAM.}
\]
\[
\text{For } k=1 \text{ to } \text{length}(AB),
\]
\[
XY(k) = IQ + H * AB(k);
D(k) = \text{distance } XY(k) \text{ and } AB(k);
\]
\[
\text{End}
\]
\[
L = \text{index of the smallest } D
\]
\[
The \text{detected symbol is } AB(L)
\]
\[
The \text{input to quantizer is } XY(L)
\]

To perform complex QFB detection, we assumed that the non-ideality parameters \( \epsilon, \theta, \) and \( \Delta \phi \) are known by measuring them in a training mode before operation. However, adding a training mode can complicate the receiver system. Besides, these parameters can vary in time and switching to training mode periodically may degrade the receiver performance. Thus, we employed a simple adaptive filter described later.

4.3.3 Estimation of non-ideality parameters

The most intuitive approach to the problem, as suggested in [53], is to estimate the non-ideality parameters \( (\epsilon, \theta, \text{ and } \Delta \phi) \) and to update the QFB filters accordingly. To that end, we re-write Equation (4.1) in the following form:

\[
\begin{bmatrix}
\hat{i}_{\text{noDC}}[n] \\
\hat{q}_{\text{noDC}}[n]
\end{bmatrix}
= \begin{bmatrix}
\cos \theta & -\sin \theta \\
(1 + \epsilon) \sin(\Delta \phi + \theta) & (1 + \epsilon) \cos(\Delta \phi + \theta)
\end{bmatrix}
\begin{bmatrix}
a[n] \\
b[n]
\end{bmatrix}
+ \text{noise (4.5)}
\]
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Assuming that the noise power is small, we can attempt to compute the parameterized matrix, $W$, by pseudo-matrix inversion in a least-squares sense, since for each received symbol, we have $(i_{noDC}[n] q_{noDC}[n])^T$ and a good estimate of the decision output, $(a[n] b[n])^T$.

A less computationally demanding solution to this problem is adaptive filtering as illustrated in Figure 4.6 [54]. This approach also accommodates variations of the $\theta$, $\epsilon$, and $\Delta\phi$ parameters. In Figure 4.6, $(a[n] b[n])^T$ is the input signal $x[n]$, the adaptive time-varying filter $W$ is the digital filter block, the output $W(a[n] b[n])^T$ is $y[n]$, and $(i_{noDC}[n] q_{noDC}[n])^T$ is shown by $d[n]$. We would like to find $W$ and update it over time, so that the output comes as close as possible to the ideal output.

Figure 4.6: Adaptive filter block diagram.

As indicated by the adaptive algorithm block in Figure 4.6, we need an adaptive algorithm for the filter implementation. The simplest algorithm, both intuitively and computationally, to perform this optimization is the well-known least mean squares (LMS)
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[54] algorithm given by the following equations:

\[
W[n + 1] = w[n] + \mu X[n]e[n],
\]

\[
e[n] = d[n] - y[n],
\]

\[
y[n] = W^T[n]X[n].
\]

LMS provides the updated filter weights using the input \(x[n]\) and the error \(e[n]\) which is the difference between the actual and the ideal outputs. Provided that the proportionality coefficient, \(\mu\), is small enough, \(W[n]\) always converges to the optimal FIR filter. However, with a small \(\mu\), LMS requires a long time to converge. Details of selection of a proper \(\mu\) given the signal statistics can be found in [54]. The LMS in our problem takes the following form:

\[
(W_{11}[n + 1] \ W_{12}[n + 1]) = (W_{11}[n] \ W_{12}[n]) + \mu(a[n] \ b[n])e_i[n],
\]

\[
e_i[n] = \nu_{noDC}[n] - (W_{11}[n] \ W_{12}[n])(a[n] \ b[n])^T
\]

\[
\text{and}
\]

\[
(W_{21}[n + 1] \ W_{22}[n + 1]) = (W_{21}[n] \ W_{22}[n]) + \mu(a[n] \ b[n])e_q[n],
\]

\[
e_q[n] = \nu_{noDC}[n] - (W_{21}[n] \ W_{22}[n])(a[n] \ b[n])^T
\]

in which \(W_{ij}[n]\) is the element of the matrix \(W[n]\) at \(i^{th}\) row and \(j^{th}\) column. The non-
ideality parameters can be estimated from $W$ by the following equations:

\[
\theta = -\tan^{-1}\frac{W_{12}}{W_{11}},
\]
\[
\Delta \phi = \tan^{-1}\frac{W_{21}}{W_{11}} - \theta,
\]
\[
\epsilon = \sqrt{W_{21}^2 + W_{22}^2} - 1.
\]

which are used to update the complex QFB filters given by Equation (4.3).

Assuming that the non-idealities are small, the first-order approximations can be used for the computation of nonlinear functions in the following manner:

\[
\theta \approx -\frac{W_{12}}{W_{11}},
\]
\[
\Delta \phi \approx \frac{W_{21}}{W_{11}} - \theta,
\]
\[
\epsilon \approx W_{22} - 1.
\]

The initial value of $W$ should be selected close to the final value, or the adaptive algorithm will experience slow convergence. That is, more symbols will not be correctly detected initially or more symbols are required in the training mode, if such a mode of operation is provided. Assuming that the non-ideality parameters are small, a good initial estimate of their values is zero. From Equation (4.5), the initial value of $W$ is thus $I_{2 \times 2}$.
4.3.4 Direct adaptive decision feedback

In this section, a computationally simpler solution, as compared to that of Section 4.3.3, is introduced. The method of this section is also numerically more stable than that of Section 4.3.3.

After solving Equation (4.4) for a received symbol, we can consider the equation as a filter with \( H \) (given by Equation (4.3)) as the adaptive filter, and \( Q(x[n] \ y[n])^T \) and \( (x[n] \ y[n])^T \) as the input and output, respectively. The desired output, \( d[n] \) of Equation (4.7), is \( Q(x[n] \ y[n])^T \). By application of LMS, we reach the following update equation for \( H \):

\[
(H_{11}[n+1] \ H_{12}[n+1]) = (H_{11}[n] \ H_{12}[n]) + \mu(a[n] \ b[n])e_i[n],
\]
\[
e_i[n] = a[n] - i_{noDC}[n] - (H_{11}[n] \ H_{12}[n])(a[n] \ b[n])^T
\]
and

\[
(H_{21}[n+1] \ H_{22}[n+1]) = (H_{21}[n] \ H_{22}[n]) + \mu(a[n] \ b[n])e_q[n],
\]
\[
e_q[n] = b[n] - q_{noDC}[n] - (H_{21}[n] \ H_{22}[n])(a[n] \ b[n])^T
\]

in which \( (a[n] \ b[n])^T \) is the decision output (i.e., \( Q(x[n] \ y[n])^T \)) and \( (i_{noDC}[n] \ q_{noDC}[n])^T \) denote the output of DC-offset removal filters for each symbol.

The non-ideality parameters can be computed from \( H \) in order to monitor how well the adaptive filter compensates for the non-idealities. From Equation (4.3), we have:

\[
\theta = -\tan^{-1} \frac{H_{12}}{1 - H_{11}},
\]
\[
\Delta \phi = \tan^{-1} \frac{H_{21}}{H_{22} - 1} - \theta,
\]
\[
\epsilon = \sqrt{H_{21}^2 + (1 - H_{22}^2)^2} - 1.
\]

Note that estimation of the non-ideality parameters is not necessary for detection (i.e., in the normal operation mode of the receiver). Thus, the computational complexity of this estimation should not be included in the overall complexity of the method.

Unlike the method given in Section 4.3.3, the update formulas in the direct method, that do not include any nonlinear computations can be efficiently implemented in fixed-point arithmetic with no risk of instability.

It is worth noting that, in floating point implementations of both methods, their BER performance is almost the same although the estimates of non-ideality parameters differ for low levels of SNR.

For the reasons given at the end of Section 4.3.3 and from Equation (4.3), \( H \) is initially set to \( 0_{2 \times 2} \).

### 4.3.5 Simulation results

To demonstrate the performance of adaptive compensation of non-ideality parameters in simulation, we generated a 1000-symbol 16-QAM sequence, with constant parameters of \( \theta = 0.2 \) rad, \( \Delta \phi = -0.25 \) rad, and \( \epsilon = 15\% \). With AWGN and SNR of 10 dB, only 3 (out of 1000) symbols were incorrectly detected whereas without the adaptive algorithm (i.e., \( H \) or \( W \) are not adaptively updated), 49 symbols were incorrectly detected. The same setup was used in both cases including the same pseudo-noise sequence, for fair
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It is also observed that by increasing the SNR, adaptive compensation of non-idealities results in considerable improvement of symbol error rate \(^2\). Figure 4.7 shows the experiment performed with a 5000-symbol sequence while other parameters are the same as the first experiment. Clearly, the performance of the adaptive scheme is superior to the basic scheme. Using the CQFB compensation, the performance is close to the ideal symbol error rate as illustrated in the figure.

\[ \text{Figure 4.7: The effect of the proposed method ("Compensation on") on symbol error rate vs. no compensation and ideal 16-QAM reception and detection (i.e., all non-ideality parameters, namely } \theta, \epsilon \text{ and } \Delta \phi \text{ are zero).} \]

\[^2\text{The symbol error rate is shown as } P_e.\]
Figure 4.8. Other parameters of this experiment were held the same values as in the first experiment. By initially setting $W$ to $I_{2 \times 2}$, the adaptive algorithm converges quickly (within the first 100 symbols) and fluctuates around the true values of non-ideality parameters. By initially setting $W$ to $0.5I_{2 \times 2}$, convergence takes 400 symbols to occur. During the time-to-convergence, 266 symbols are incorrectly detected! In contrast, the direct method has only a single detection error within the first 400 symbols.

Figure 4.8: The effect of initial value of the filter ($W$; $0.5I_{2 \times 2}$ (light) and $I_{2 \times 2}$ (dark)) on convergence to non-ideality parameters. The SNR is set to 10 dB and the same pseudo-noise sequence is used for fair comparison. The 1000-symbol 16-QAM signal is generated with $\theta = 0.2\text{rad}$, $\Delta\phi = -0.25\text{rad}$, and $\epsilon = 15\%$.

The effect of gain mismatch on symbol error rate is shown in Figure 4.9. The other parameters are the same as the first experiment. It is observed that the adaptive compensation of non-idealities successfully controls the effect of gain mismatch on the symbol error rate. Note that in a well-designed circuit, the gain mismatch is ideally zero and will
not exceed 10%.

![Graph showing the effect of gain mismatch on symbol error rate.](image)

**Figure 4.9:** The effect of gain mismatch ($\epsilon$) on symbol error rate, with and without adaptive compensation of non-idealities.

The effect of angular non-idealities (carrier phase error, $\theta$, and phase mismatch, $\Delta \phi$) on symbol error rate is shown in Figure 4.10. A 3000-symbol 16-QAM sequence is used in this experiment with carrier phase error, $\theta$, and phase mismatch, $\Delta \phi$, varying between -0.9 and 0.9 rad ($\approx 51^\circ$). The other parameters are the same as the first experiment. The right figure shows the symbol error probability is low (dark points are desired since they mean close to zero values) for very small values of $\theta$ and $\Delta \phi$. After CQFB compensation, for most of $\theta$ and $\Delta \phi$ values, the symbol error probability is small. Therefore, it is
observed that the adaptive compensation of non-idealities is successful (large dark area implies near zero symbol error rate for a wide range of non-ideality values). Also, note that if the carrier phase error ($\theta$) is small (the middle area of left image), the adaptive algorithm is effective for a large range of phase mismatch ($\Delta \phi$) value. That is good news, as all receivers include a carrier synchronization mechanism that keeps $\theta$ small.

![Figure 4.10: Effect of carrier phase error ($\theta$) and phase mismatch ($\Delta \phi$) on symbol error rate represented by image intensity (i.e., dark areas = small error rate), with (left) and without (right) adaptive compensation of non-idealities. $\theta$ and $\Delta \phi$ vary between -0.9 and 0.9 rad ($\cong 51^\circ$).](image)

4.3.6 Direct adaptive decision feedback with ISI

In communication systems, one of the effects of the channel on the transmitted symbols is inter-symbol interference (ISI). That is due to the fact that the frequency response of the channel is not ideal, i.e., not constant for all frequencies. Thus, the impulse response of the channel is not ideal, so a shifted impulse can result. Therefore, a convolution
of the channel impulse response with the transmitted signal, comprised of a sequence of modulated pulses, mixes a number of consecutive symbol pulses together. With no special provision to combat this effect, each symbol demodulated at the receiver is a linear combination of a number of the transmitted symbols. That is, the symbols that were uncorrelated at the transmitter can overlap and become correlated at the receiver.

This ISI effect is well-known [55]. If the channel response is not known or varies with time, one way of ISI compensation is to use adaptive techniques [50]. To that end, a certain sequence of symbols known as a training sequence, which is known at the receiver, is sent once. At the receiver, the filters are adjusted to compensate for the ISI, and to de-correlate the received symbols.

Here, we show that our method of adaptive compensation for non-ideality parameters can be generalized to remove small levels of ISI by decision feedback - with no need to use a training sequence.

In Chapter 3, it was mentioned that decision feedback in the complex QFB architecture is used to restore the DC components of the two signal channels lost by high-pass filtering. From another viewpoint, the high-pass filters, $H_{ACI}(s)$ and $H_{ACQ}(s)$ in Figure 3.4, generate a known ISI in I and Q channels and decision feedback filters are designed to remove ISI.

When the ISI model is known, for example the ISI generated by DC offset removal filters, $H_{ACI}(s)$ and $H_{ACQ}(s)$ in Figure 3.4, the optimal decision feedback is simply given by Equations (3.17) to (3.20). Generally, the ISI is partly due to the channel and partly due to the DC removal filters and can be unknown and time-varying. That is why adaptive
compensation for ISI is necessary.

Using the form of Equation (4.4), the new decision equation for the case with ISI becomes the following:

\[
x[n] = i_{noDC}[n] + \bar{a}[n] \ast h_{ii}[n] + \bar{b}[n] \ast h_{qi}[n]
\]
\[
y[n] = q_{noDC}[n] + \bar{a}[n] \ast h_{iq}[n] + \bar{b}[n] \ast h_{qq}[n]
\]

and the symbol \(^*\) denotes the convolution. For example,

\[
(\begin{align*}
    h_{iq}[0] \\
    h_{iq}[1] \\
    \vdots \\
    h_{iq}[N-1]
\end{align*})
\]

\[
\bar{a}[n] \ast h_{iq}[n] = (a[n], a[n-1], \ldots, a[n-N+1])
\]

in which \((\bar{a}[n] \quad \bar{b}[n])^T\) is the decision sequence, and \(h_{lm}[n]\) is the impulse response of the filter that conveys the decision feedback from channel \(l\) to channel \(m\). \(N\) is the length of each of the decision feedback filters.

For detection, the nonlinear decision equation given above should be solved for every received symbol. The pseudo-code of Section 4.3.2 can now be used with the following definition:

\[
IQ = \left(\begin{array}{c}
    i_{noDC}[n] + \bar{a}[n-1] \ast (h_{ii}[n+1]u[n]) + \bar{b}[n-1] \ast (h_{qi}[n+1]u[n]) \\
    q_{noDC}[n] + \bar{a}[n-1] \ast (h_{iq}[n+1]u[n]) + \bar{b}[n-1] \ast (h_{qq}[n+1]u[n])
\end{array}\right)
\]

That is, IQ represents the effect of current value of I and Q signals, plus the feedback of the decisions made so far filtered by the second coefficient of \(h_{lm}[n]\) until the end. The
first coefficients of $h_{nn}[n]$ comprise the $H$ that is used to filter the current decision.

Following a procedure similar to that of Section 4.3.4, we reach the filter update equations below:

$$h_{ii}^{k+1}[n] = h_{ii}^k[n] + \mu(a[n], a[n-1], \cdots, a[n_N + 1])^T(a[n] - x[n])$$

$$h_{qi}^{k+1}[n] = h_{qi}^k[n] + \mu(b[n], b[n-1], \cdots, b[n_N + 1])^T(a[n] - x[n])$$

$$h_{qi}^{k+1}[n] = h_{qi}^k[n] + \mu(a[n], a[n-1], \cdots, a[n_N + 1])^T(b[n] - y[n])$$

$$h_{qq}^{k+1}[n] = h_{qq}^k[n] + \mu(b[n], b[n-1], \cdots, b[n_N + 1])^T(b[n] - y[n])$$

For reasons similar to those given in the previous section, all filters are initialized with zeros.

The upper limit on $\mu$ (required for convergence of LMS) is inversely proportional to the filter length, $N$ [54]. Thus, we must choose a much smaller $\mu$ as compared to the two-point adaptive filters used in the non-ISI case. This implies that the time-to-convergence will be much longer.

Note that the decision feedback filters can be infinite-length impulse response (IIR). For example, if the recursive DC-offset removal filter of Section 4.3.1 is used in the architecture shown in Figure 3.4, Equations (3.17) to (3.20) suggest IIR decision feedback for optimal compensation. In practice, however, IIR adaptive filters are usually avoided as they can become unstable if certain precautions are not taken. Also, the update algorithm for adaptive IIR filters is more computationally costly than LMS. For the same reason, in

---

3 The constant $\mu$ is a step-size, which controls the amount of gradient information used to update each coefficient. Also, it directly affects how quickly the adaptive filter will converge toward the unknown system.
this work, we adhere to finite-length impulse response (FIR) adaptive filters for decision feedback. Since the impulse response of a stable IIR filter decays with time, it can be approximated by a sufficiently long FIR to the desired accuracy.

4.3.7 Simultaneous compensation for ISI and non-ideality parameters

To demonstrate good performance of the proposed method in ISI cancellation, we generated a 5000-symbol 16-QAM sequence, with constant parameters of $\theta = 0.2\text{rad}$, $\Delta\phi = -0.25\text{rad}$, and $\epsilon = 15\%$, polluted by AWGN (SNR = 15 dB) with different types of ISI listed below:

(i) FIR, $h[n] = \delta[n] - \frac{1}{16} u[n] u[16 - n - 1]$.
(ii) FIR, $h[n] = \{1, \frac{1}{3}, \frac{1}{3}, \frac{1}{3}\}$.
(iii) IIR (the system described by Equation 4.2, $\alpha = 0.9$),
(iv) FIR, $h[n] = \{0.1106, 0.7364, 0.7369, 0.6431\}$ (samples taken from $U[0, 1]$).

in which $\delta[n]$ and $u[n]$ denote discrete-time impulse and step functions.

As an example, let us consider ISI type (ii) listed above. Each received symbol is a linear combination of the current and three previous transmitted symbols, each weighted by 1/3. From Equations (3.17) to (3.20), we have:

$$H_{II}(z) = 1 - \cos \theta H_{ACI}(z),$$

$$H_{QI}(z) = \sin \theta H_{ACI}(z),$$

$$H_{IQ}(z) = -(1 + \epsilon) \sin(\theta + \Delta\phi) H_{ACQ}(z),$$
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\[ H_{QQ}(z) = 1 - (1 + \epsilon)\cos(\theta + \Delta \phi)H_{ACQ}(z), \]

The nature of ISI in the context of Chapter 3 can be expressed as follows:

\[ H_{ACI}(z) = H_{ACQ}(z) = 1 + \frac{1}{3}z^{-1} + \frac{1}{3}z^{-2} + \frac{1}{3}z^{-3} \]

By substituting \( H_{ACI}(z) \) and \( H_{ACQ}(z) \) in the equations for the optimal decision feedback for compensation of ISI and non-idealities and taking the inverse z-transform we reach the following:

\[ h_{ii}[n] = \{0.0199, -0.3267, -0.3267, -0.3267\}, \]

\[ h_{qi}[n] = \{0.01987, 0.0662, 0.0662, 0.0662\}, \]

\[ h_{iq}[n] = \{0.0575, 0.0192, 0.0192, 0.0192\}, \]

\[ h_{qq}[n] = \{-0.1486, -0.3829, -0.3829, -0.3829\}. \]

Now, let us assume that ISI is unknown and that we use the method of Section 4.3.6 for adaptive compensation by decision feedback. At the last iteration (i.e., in processing the last symbol and long after convergence) the decision feedback filters are the following:

\[ h_{ii}[n] = \{0.0206, -0.3331, -0.3364, -0.3306\}, \]

\[ h_{qi}[n] = \{0.1988, 0.0687, 0.0761, 0.0734\}, \]

\[ h_{iq}[n] = \{0.0583, 0.0199, 0.0173, 0.0233\}, \]

\[ h_{qq}[n] = \{-0.1441, -0.3780, -0.3830, -0.3827\}. \]
Figure 4.11: Left: 16-QAM received signal (at the output of DC removal filters in Figure 1) with ISI and receiver non-idealities. Right: The same signal after adaptive compensation of ISI and non-idealities (at the input of the threshold blocks in Figure 1; only the last 1500 symbols are mapped to ensure convergence occurred).

It is observed that the adaptive algorithm successfully computes the decision feedback filters. This can be also seen in Figure 4.11, in which the signal constellation before and after adaptive compensation is shown. Convergence of the adaptive filters, however, requires a significant amount of time, as illustrated in Figure 4.12. As we can see in that figure, the CQFB adaptive filters can compensate the non-idealities ($\theta = 0.2\text{rad}$, $\Delta\phi = -0.25\text{rad}$, and $\epsilon = 15\%$) in the presence of IS type (ii) completely after 500 symbols.

The performance of the proposed method is tested with the four types of ISI listed earlier (Figure 4.13). Assuming that the channel does not introduce any ISI or it is already equalized, and the system function of the channel is equivalent to pure delay, ISI types (i) and (iii) are likely to happen, as the effect of DC-offset removal filters. In fact, ISI type (i) is the impulse response of a 16-point moving average DC removal filter, and ISI type
Figure 4.12: Convergence of adaptive compensation of ISI and non-idealities: because of high SNR (15 dB) no error occurred after convergence (after about 600 symbols).

(iii) is the system function of recursive DC-removal discussed in Section 4.3.1. In the case of IIR ISI, the ideal decision feedback filters are IIR as well. Nevertheless, it is observed that 4-point FIR filters can effectively approximate the ideal IIR decision feedback filters. In the case of FIR ISI (types i, ii and iv), the adaptive filters of the same order (i.e., 16, 4 and 4) are used. It is also observed that when the ISI is significant, as in type (iv) where the effect of the three past symbols is much stronger than the current symbol, the algorithm does not converge, at least within the period of the 5000 symbols simulated.
Figure 4.13: Cumulative sum of reception errors for various types of ISIs. For ISI type (iv) the method does not converge within 5000 symbols.

4.4 Summary

In this chapter, the idea of CQFB is implemented using DSP techniques. The adaptive system to compensate for carrier phase error and I/Q gain and phase mismatch, as well as ISI is implemented. As the results demonstrated, CQBF is a very effective approach to minimize the front-end non-idealities impacts, so it also relaxes some of the receivers front-end specification.

To illustrate that CQFB is general and can be used in many applications, CQFB is ap-
applied to an orthogonal frequency division multiplexing (OFDM) system. OFDM has been successful in numerous wireless applications in which superior performance in multipath environments is desirable. Because of its popularity and performance, we investigated the effect of CQFB on OFDM systems in Appendix A. Good performance of the system is demonstrated by simulations, the results of which are reported in the appendix.
Chapter 5

Mismatch-Controllable RF Front-end Test Platform

5.1 Introduction and Motivation

In this chapter, the design and implementation of a prototype integrated receiver front-end are described. The prototype is intended to assist in validation of a DSP CQFB scheme for compensation of non-idealities. The developed front-end provides user control of I/Q mismatch and includes a low-noise amplifier (LNA), two mixers and a voltage-controlled oscillator (VCO). It can be used as test vehicle for evaluation of various I/Q mismatch compensation methods implemented in the back-end. The prototype was fabricated using TSMC 0.18\mu m CMOS technology.

The idea of having an RF front-end with externally adjustable I/Q mismatch parameter is attractive. The controllable front-end not only can be used as test bench for different DSP-based I/Q mismatch cancellation techniques, but it also enables the user to manually compensate I/Q mismatch gain completely. Therefore, it is possible to determine how effective the DSP processor is at mitigating the effects of I/Q mismatch.

Figure 5.1 shows a complete digital wireless receiver, from antenna (input) to detected
symbol (output), using the DSP CQFB technique. Although control of the I/Q mismatch for the RF front-end is desirable for system test, the implementation should be close to a real DCR. In Figure 5.1, the dotted box showing DSP CQFB was described in previous chapter while the solid box, which is the RF front-end chip, is described in this chapter.

In general, all analog components of the I and Q branches, such as mixers, filters, and A/D converters, contribute to the receiver imbalance properties [22]. However, the combined effect of these imbalances is such that the image attenuation produced by the down-converting is finite, causing the image signal to alias on top of the desired signal. As a consequence, the whole imbalance between the I and Q branches is usually modeled at the quadrature mixer as an imbalanced LO signal (Chapter 2). Since the mixer structure is simpler and more stable compared to a VCO, introducing mismatch is more feasible at
the mixer. Another important factor is that the mixer is in every RF front-end structure while VCOs can be external.

This RF front-end is intended for the ISM band at 2.4GHz. The block diagram of the implemented design is shown in Figure 5.2.

![Block diagram of the implemented RF front-end](image)

Figure 5.2: The block diagram of the implemented RF front-end

To create an amplitude mismatch between I and Q channels, I and Q mixer gain is controlled externally. This is implemented using a modified single-balanced mixer with controllable shunt current to provide a variable-conversion gain, as described in Section 5.4. In our prototype front-end, the gains of I and Q mixers are externally controlled by shunt current $I_{bcI}$ and $I_{bcQ}$, as shown in Figure 5.1. Since we intend to investigate the common
DCR output, a switch is placed to have the option of fixed (equivalent) mixers. Using a switch, the user controls the Ibc I and Ibc Q which can adjust the I and Q mixer gains, respectively. If a regular (non-adjustable) front-end is desired, the switch is turned off and the I and Q mixers gains are fixed. The details of switch and shunt current operation and the key contribution of this chapter are described in Section 5.4.

As the proposed RF front-end can introduce mismatch, it can be used as a test vehicle to validate CQFB implementation at the back-end. Also, it can be used as test vehicle for other I/Q compensation techniques implemented in DSP. In addition, such gain adjustment improves the I/Q amplitude imbalance, which results in dramatic increase in image rejection ratio (IRR). As a result the DSP techniques to compensate for the residual I/Q imbalance can be more successful.

If we assume that we can get the estimation of gain mismatch ($\epsilon$), then we can manually adjust I and Q gains using the proposed RF front-end, so there will be no more gain mismatch. Therefore, IRR of the receiver would improve. In Figure 5.3, the amount of IRR improvement versus I/Q gain mismatch ($\epsilon$) is shown, for different phase mismatch ($\Delta \phi$) values, based on assuming completely compensating I/Q gain mismatch using controllable-gain I and Q mixers. For example, in the case of $\epsilon = 12\%$ and $\Delta \phi = 3^\circ$, using the proposed RF front-end can improve IRR by 7.5dB, shown by 'X' on the Figure 5.3. From this figure, it is observed that IRR can be improved by up to 20 dB. A high IRR can relax some of the design constraints of the RF front-end blocks.

In the next section, the overall RF front-end specifications and design process are given. Later, the blocks of the RF front-end are explained in more detail.
As mentioned before, the block design of a direct conversion receiver is very crucial in the overall receiver performance. A poor system design can place difficult design constraints on the underlying blocks, thus making the block specifications impossible to achieve. That is why a proper allocation of performance specifications to each block facilitates design success and speeds up the design cycle.

To start the design, it is necessary to either assume or derive a set of overall receiver specifications. Some of the key criteria for receivers include sensitivity, dynamic range, out-of-band suppression, SNR, bandwidth (BW), and BER. Most of these performance criteria are very specific to the system being designed and are not set by the standards committees. However, the overall system generally has to stay within a set of limitations.
such as maximum radiated power, out-of-band radiation, and total bandwidth that are set in well-defined standards. Other performance criteria can be derived from these well-defined criteria as it applies to a specific system.

5.2.1 Receiver System Specifications

The key system specifications for the RF front-end building blocks can be broadly categorized in terms of conversion gain (or loss), linearity, and noise figure. These specifications can be further fine-tuned into a set of specifications consisting of (a) conversion gain (or loss), (b) overall noise figure (NF), (c) input PldB, (d) IIP3, (e) IIP2, and (f) I/Q imbalance, as appropriate. Also, the interfacing impedances play a role in an integrated environment.

Noise Figure

The noise figure referred to the antenna is calculated as follows [19]:

\[NF = S_0 - SNR + 174dBm/Hz - 10\log_{10}(BW)\] (5.1)

where \(S_0\) denotes the minimum signal level; \(BW\) denotes the noise bandwidth (22 MHz); and SNR is the signal-to-noise ratio given by:

\[SNR = 10\log_{10}(E_b/N_0) + 10\log_{10}(E_s/E_b)\] (5.2)
Table 5.1: SNR and NF requirement for various modulation schemes in IEEE 802.11a/g

<table>
<thead>
<tr>
<th>Rate (Mbps)</th>
<th>Modulation</th>
<th>Coding rate</th>
<th>$S_0$ (dBm)</th>
<th>$E_s/E_b$ (symbols/bit)</th>
<th>$E_b/N_0$ (dB)</th>
<th>SNR (dB)</th>
<th>NF (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>BPSK</td>
<td>1/2</td>
<td>-88</td>
<td>1/2</td>
<td>7</td>
<td>4</td>
<td>9</td>
</tr>
<tr>
<td>9</td>
<td>BPSK</td>
<td>3/4</td>
<td>-87</td>
<td>3/4</td>
<td>6.25</td>
<td>5</td>
<td>9</td>
</tr>
<tr>
<td>12</td>
<td>QPSK</td>
<td>1/2</td>
<td>-85</td>
<td>1</td>
<td>6.5</td>
<td>6.5</td>
<td>9.5</td>
</tr>
<tr>
<td>18</td>
<td>QPSK</td>
<td>3/4</td>
<td>-83</td>
<td>3/2</td>
<td>6.74</td>
<td>8.5</td>
<td>7.5</td>
</tr>
<tr>
<td>24</td>
<td>16-QAM</td>
<td>1/2</td>
<td>-80</td>
<td>2</td>
<td>8</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>36</td>
<td>16-QAM</td>
<td>3/4</td>
<td>-76</td>
<td>3</td>
<td>9.73</td>
<td>14.5</td>
<td>10.5</td>
</tr>
<tr>
<td>48</td>
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<td>2/3</td>
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<td>4</td>
<td>12.97</td>
<td>19</td>
<td>10</td>
</tr>
<tr>
<td>54</td>
<td>64-QAM</td>
<td>3/4</td>
<td>-71</td>
<td>9/2</td>
<td>13.46</td>
<td>20</td>
<td>10</td>
</tr>
</tbody>
</table>

where $E_b$ and $E_s$ are the average energy per bit and symbol, respectively. Equation (5.2) can be written as:

$$SNR = \frac{E_b}{N_0} + 10 \log_{10}\left\{\log_2 M \ast R\right\}$$

where $R$ denotes the coding rate (1/2, 2/3, 3/4) and $M$ denotes the constellation density (2, 4, 16, or 64). Table 5.1 lists the SNR and NF requirements for various modulation schemes. In the Table 5.1, $S_0$ is set to 8 dB more stringent than specified to consider implementation losses. $E_b/N_0$ requirements for 10% BER are used for coherent demodulation.

As we can see from the Table 5.1, the NF requirement for different modulation scheme is very close. So, the system target noise figure is set to 10 dB with 5 dB of implementation margin. I/Q imbalance is targeted for 0.4 dB in amplitude and 3.7° in phase. Input PldB has been set to -16 dBm. The overall front-end gain can be set to 20 dB as a compromise between the overall system noise figure and linearity.

The RF front-end is a critical building block in the receiver that greatly affects the sensitivity and linearity of the system. The one described here consists of a LNA, two
down-conversion mixers and a quadrature VCO (QVCO). All the circuits have been developed with a 0.18\(\mu\)m CMOS process. In the next sections, the circuit design steps are described.

### 5.3 Low Noise Amplifier

A LNA serves as the first amplification block in an RF receiver. Since typical incoming RF signals are relatively small, which leads to a small SNR, any additional noise will further degrade the overall SNR and therefore the receiver performance. Because the LNA is the first gain stage along the receiver chain, its noise and gain play the dominant role in the amount of total noise in a multiple stage circuit. The total noise figure of cascode stages is given by:

\[
NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1G_2} + \cdots + \frac{NF_n - 1}{G_1\cdots G_{n-1}}
\] (5.4)

where \(NF_1\), noise figure of the first stage, sets the lower boundary of \(NF\). \(NF\) can be efficiently reduced by minimizing \(NF_1\) and maximizing \(G_1\).

For a receiver, \(NF_1\) and \(G_1\) are the noise figure and the gain of the LNA, respectively. The noise figure of the LNA has to be low enough, as the name suggests, to keep the overall system NF low, and the gain of the LNA needs to be high enough to reduce the noise contribution from the mixer and next stages, but not too high to degrade the overall system linearity.

In addition, because of the RF filters (typically required to be matched to 50\(\Omega\)) in
front of the LNA, impedance matching is part of LNA’s specifications. In summary, the key features of a LNA are: low noise figure, sufficient gain, and good linearity.

There are two topologies commonly used to design an LNA in RF MOS circuits: common-gate and cascode. While the common-gate topology provides a wide-band input matching and is less sensitive to parasitics, it has an inherently high noise figure.

The cascode topology has the inherent advantage of separating the output and input optimization criteria. Input and output matching are also independent. Also, the reverse isolation is higher as compared to the other topologies. Cascode topology is better-suited to our design needs and is used here.

![Circuit Schematic](image)

Figure 5.4: Low Noise Amplifier (LNA).

Figure 5.4 shows the circuit schematic of the cascode LNA under consideration. It is a single-stage inductive source-degenerated architecture. Transistor M1 in a common-source configuration is the amplifying stage, while M2 in a common-gate configuration is
the cascode stage. Cascoding transistor $M_2$ is used to reduce the interaction of the tuned output with the tuned input and also to reduce the effect of $M_1$'s $C_{gd}$. The total node capacitance at the drain of $M_2$ resonates with inductance $L_{out}$ both to increase gain at the center frequency and simultaneously provide an additional level of highly-desirable bandpass filtering. Inductor, $L_s$, in the source implemented by using the bond wires, provides degeneration to create a positive component for its input impedance. Another inductor, $L_g$, is the gate inductance to help with input impedance matching. $L_{out}$ and $C_{out}$ create an output tank circuit to help with output impedance matching. $M_3$ is a current mirror with $M_1$, which provides the bias voltage for the input port together with resistor $R$ and $I_{bias}$.

To complete the biasing, DC blocking capacitor $C_1$ must be present to prevent any effects on the bias of $M_1$. The value of $C_1$ is chosen to have a negligible impedance at the signal frequency. To keep the design cost low, it is important not to use components with very large area. In this design, the largest size metal-insulator-metal (MIM) capacitor we used has a capacitance of 951.6$fF$ (size of $30\mu \times 30\mu$). The $L_{out}$ is an on-chip spiral inductor (5.6 nH) and is implemented using an octagon shape spiral on metal 6 layer. The inductor is described in more detail in Appendix B. The LNA performance is optimized to have a high gain and low noise figure for the 2.4 GHz ISM band.

The input impedance of the common source stage can be expressed as:

$$Z_{in} = R_i + R_g + \left(\frac{g_m}{C_{gs}}\right)L_s + s(L_s + L_g) + \frac{1}{sC_{gs}} \quad (5.5)$$

As observed in the equation above, $L_g$ and $L_s$ are used to cancel out the effect of the
capacitors. The required input impedance is $50\,\Omega$ at the central frequency 2.44GHz. The imaginary part of $Z_{\text{in}}$ should be zero at the central frequency. To avoid the large on-chip inductor required, it is common practice to use the inductance of the bondwires. However, because of their small inductance and inaccurate model, external impedance matching circuit on the board is also required to achieve $50\,\Omega$ impedance (Lext and Cext in Figure 5.5).

### 5.3.1 Simulation Results

To provide a close to real situation, the simulation was performed on the post-layout extraction, while assuming that the external input matching was ideal. The gain vs. frequency of the LNA is plotted in Figure 5.6. The LNA has a voltage gain of more than 28dB and a bandwidth of 100MHz.
As mentioned before, it is very important to keep the noise figure of the LNA very small and the gain very high. By changing the inductor and capacitor values and the biasing, the LNA is optimized in a way that, in the frequency of interest, the gain would be at its maximum value while the noise figure is at its minimum value. The approach in [15] is used to achieve the minimum NF for CMOS LNA. As it is shown in Figure 5.7, the LNA noise figure is 1dB around a frequency of 2.44 GHz.

$S_{11}$ is an important parameter for input matching. The $S_{11}$ of the LNA, including an external matching circuit, is -15dB at 2.44GHz, as shown in Figure 5.8. In the our design, a 5.6nH for $L_{out}$ is used. LNA performance parameters are given in Table 5.2.
5.4 Down-Conversion Mixer

The mixer is one of the most critical building blocks in modern RF wireless communication systems. As a part of RF front-end circuits, its performance directly impacts the performance of the whole system. This block was chosen to implement the controllable mismatch feature. A single-balanced active mixer is presented in this dissertation, and is implemented in a 6-metal-1-poly 0.18μm RF CMOS process.

A simplified schematic of a single-balanced active mixer is shown in Figure 5.9. It consists of a driving stage, i.e., an input transconductance device (M1), and a switching stage (symmetric switched differential pairs M2 and M3), and loads ($R_L$). The conversion gain of the mixer is determined by the product of the transconductance of M1 and load
resistors [15]:

\[ A_v = \frac{2}{\pi} g_m R_L \]  \hspace{1cm} (5.6)

in which \( g_m \) is the \( M_1 \) transconductance and \( R_L \) is the load resistor. If the \( g_m \) can be controlled, then a variable gain can be achieved.

As the second set of blocks in a direct down-conversion receiver, it is desirable that the mixers have high conversion gains and low noise figures. To increase the gain, one can increase the transconductance of \( M_1 \). The transconductance of \( M_1 \) is given by the following equation:

\[ g_m = \frac{\partial I_{\text{mix}}}{\partial V_{GS}} = \frac{2I_D}{V_{gs} - V_T} \]  \hspace{1cm} (5.7)
Table 5.2: LNA Performance Summary.

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18μ</td>
</tr>
<tr>
<td>Supply voltage(V)</td>
<td>1.8</td>
</tr>
<tr>
<td>Operation freq.(GHz)</td>
<td>2.44</td>
</tr>
<tr>
<td>Power dissipation(mW)</td>
<td>5.89</td>
</tr>
<tr>
<td>Voltage gain(dB)</td>
<td>28.6</td>
</tr>
<tr>
<td>Noise figure(dB)</td>
<td>1.07</td>
</tr>
<tr>
<td>BW (-3dB)</td>
<td>130MHz</td>
</tr>
<tr>
<td>$S_{11}$(dB)</td>
<td>-12</td>
</tr>
<tr>
<td>P1dB(dBm)</td>
<td>-8</td>
</tr>
</tbody>
</table>

Figure 5.9: Single-balanced down conversion mixer

Where $V_{gs}$ is the gate-source voltage of $M_1$, $V_T$ is the $M_1$ threshold voltage and $I_D$ is the DC drain current.

The proposed method increases the gain of the mixer circuit by providing a shunt current, $I_{shunt}$, into the drain of transistor $M_1$. A active mixer topology, based on the single-balanced design, was used for our application. The proposed mixer’s gain is adjusted by using a current shunt circuit to modify the transconductance, as shown in Figure 5.10. The mixer includes a gain stage comprised of a pair of NMOS transistors, $M_2$ and $M_3$, coupled to the supply voltage $V_{dd}$ through a pair of load resistors. It also includes a bias
circuit comprised of NMOS transistor M7 having a gate coupled to a coupling capacitor C3.

The mixer gain can be increased by increasing $I_{\text{mix}}$. This allows the differential input stage to operate at lower DC currents, which will result in less noise, and also allows for a larger output swing across the load resistors.

![Diagram of the implemented down conversion mixer.](image)

Figure 5.10: The implemented down conversion mixer.

The generator of the shunt current, $I_{\text{shunt}}$, is comprised of transistors M4 and M5. This mixer is designed in a way that $I_{\text{shunt}}$ can be controllable. The shunt current can come from the bias circuit that is on-chip ($I_{\text{shunt}}$ would be fixed), or from an I/O pin externally ($I_{\text{shunt}}$ would be controllable). By setting $V_{\text{switch}}$, one has the choice to select the $I_{\text{shunt}}$ set externally or internally. If $V_{\text{switch}}$ is Vdd then the $I_{\text{bc}}$ pin can be disconnected and the $I_{\text{shunt}}$ is fixed current provided by bias circuitry. But if we connect the $V_{\text{switch}}$
to ground then $I_{bc}$ can be applied externally, and we have full control on $I_{shunt}$. This is only added for validation of the approach, but would be removed when the method has been demonstrated to work properly. In that case, $V_{switch}$ alone would control the shunt current.

There are several advantages to this structure: first, by using the shunt current, the conversion gain of the mixer can be increased dramatically. Second, by putting a switch we have the option of controlling the shunt current, which means we have control over conversion gain of the mixer. Note that this applies to both I and Q mixers.

Since we use quadrature down-conversion, we have two identical mixers for I and Q path. This structure not only can increase/control their gains, it can also reduce the I/Q mismatch by controlling the mixers on I and Q path.

The RF signal reaches the mixer input at the gate of $M_1$. The signal is AC coupled through coupling capacitor $C_1$ and applied to the gate of transistor $M_1$. The RF signal is amplified and generates a modulated bias current $I_{mix}$. The DC bias current component of $I_{mix}$ consists of current components through differential transistors $M_2$ and $M_3$, and shunt circuit $I_{shunt}$. The gate of $M_2$ and $M_3$ are biased by two anti-phase sinusoidal signals of period $T (= 1/f_{LO})$, i.e., $V_{LO+} = V_G + A_{LO} \sin \omega_{LO} t$ and $V_{LO} = V_G - A_{LO} \sin \omega_{LO} t$, where $V_G$ is the common voltage and $A_{LO}$ is the amplitude. These LO signals are generated by a local quadrature oscillator that is placed on the same integrated circuit as the mixer circuit. The output of the mixer circuit is taken at nodes $out+$ and $out-$, after a low-pass RC filter at the output that filters out the high frequency components.

Considering noise due to the switches, the loads and the transconductance stage, the
total white noise at the mixer output is [56]:

\[ V_{n,2}^2 = 8kTR_L + 8kT\gamma \frac{R_L^2 I}{\pi A_{LO}} + 4kT\gamma \frac{g_m R_L^2}{2} \]  

(5.8)

where the first term is due to the two load resistors, the second term is due to the two switches (in which \( I = I_{mix} - I_{shunt} \) and \( \gamma \) is the channel noise factor), and the third term shows the noise of the transconductance stage transferred to the mixer output.

As observed in the design, \( I \) is fixed while \( I_{shunt} \) and \( I_{mix} \) can increase. Therefore, the conversion gain can increase while the noise of the switch stage does not change.

The results of transient analysis of the mixer is shown in Figure 5.11. As shown in the figure, the conversion gain of the mixer is around 22 dB when the switch is on and \( I_{shunt} \) is fixed (1.3mA, and \( I_{bc} \) is 100\( \mu \)A from inside the chip). If \( V_{switch} \) is GND and \( I_{bc} = 0 \) then the mixer does not have any gain (-2.5 dB; the minimum value of \( I_{bc} \) such that the mixer works properly is 20\( \mu \)A).

Conversion gains for some \( I_{bc} \) values are listed in Table 5.3. Each of the two mixers can be controlled separately to provide the desired level of mismatch. For example, the I mixer with \( I_{bc} = 20\mu A \) has a gain of 7.0dB while the Q mixer with \( I_{bc} = 60\mu A \) has a gain of 19.2dB. The gain mismatch for this case is 12.2dB. A summary of mixer’s characteristics is given in Table 5.4. Note that the values for \( IIP3 \) and \( P1dB \) are measured at the highest gain.
Table 5.3: Mixer’s conversion gain for different Ibc

<table>
<thead>
<tr>
<th>Ibc (μA)</th>
<th>Conversion Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>7.0</td>
</tr>
<tr>
<td>30</td>
<td>11.5</td>
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<tr>
<td>40</td>
<td>13.3</td>
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<tr>
<td>50</td>
<td>15.6</td>
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<td>60</td>
<td>19.2</td>
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<td>70</td>
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</tr>
<tr>
<td>80</td>
<td>21.9</td>
</tr>
<tr>
<td>100</td>
<td>22.0</td>
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Table 5.4: Mixer Performance Summary.

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<th>Process</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage(V)</td>
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<tr>
<td>IF</td>
<td>5MHz</td>
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<td>Power dissipation(mW)</td>
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<tr>
<td>Noise figure(dB)</td>
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</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-5.68</td>
</tr>
<tr>
<td>P1dB(dBm)</td>
<td>-15.35</td>
</tr>
</tbody>
</table>

5.5 Voltage-Controlled Oscillator

Voltage-controlled oscillators with quadrature outputs (referred to as quadrature voltage-controlled oscillators, QVCOs) are the key building blocks in many wireless and wired communication systems [10, 57]. The conventional method for generating I/Q signals is to use a non-quadrature VCO and feed it to a polyphase filter. Another technique is the design of a VCO with double the frequency and a divider for generating quadrature signals. Both of above-mentioned methods are power hungry. Using cross-coupled VCO’s for generating I/Q signals not only consumes less power but it also achieves better phase noise performance. In this section, the design of a low phase noise, quadrature CMOS VCO is discussed.

A two-stage differential ring oscillator can be employed to generate quadrature phases
in a straightforward way, but its notorious poor spectral purity (for a given power budget) disqualifies this choice for most applications. A more attractive approach for quadrature signal synthesis relies on the possibility of coupling two identical LC-tank oscillators to each other, taking advantage of the superior phase noise performances achievable with the LC tanks [58]. For this purpose, several methods are available in the literature. The best known implementation of the idea is the parallel-coupling quadrature oscillator [59].

Figure 5.12 shows a very well-known implementation of a CMOS QVCO (symmetrical components have been named only once for better readability). Two identical oscillators, \(I\) and \(Q\), are connected to each other by means of two additional differential pairs. Direct connection from \(Q\) to \(I\) and cross-connection of \(I\) to \(Q\) ensures a quadrature relation between the phases of the output waveforms. Also, the common source nodes of the differential pairs driving the \(I\)-tank and the \(Q\)-tank are connected together. As a consequence, both oscillators are tied together and biased with the same current. In the following, we derive the oscillation frequency and signal amplitude for this circuit.

Assuming full current switching and negligible parasitic capacitances, the resonator currents are pulses of a quarter-period duration, aligned with the corresponding driving voltages. Figure 5.13 depicts the resonator currents for the left oscillator. By Fourier analysis, the amplitude of the fundamental component is [58]:

\[
I = \frac{\sqrt{2}}{\pi} I_B
\]  

(5.9)

On the other hand, we assume that the selectivity of the tank is high enough that the differential output voltages \(V_I\) and \(V_Q\) can be considered sinusoidal with very good ap-
proximation, and expressed as:

\[ V_I(t) = V_I \cos(\omega_{osc}t) \quad (5.10) \]
\[ V_Q(t) = V_Q \cos(\omega_{osc}t + \phi) \quad (5.11) \]

where \( \omega_{osc} \) is the oscillation frequency and \( \phi \) is the phase difference between the two waveforms. Figure 5.13 depicts this situation for the left oscillator. The load seen by each oscillator is an equivalent parallel RLC resonator with admittance:

\[ A(\omega) = \frac{1}{R} + j \frac{Q}{R} \left( \frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) = G + jY(\omega) \quad (5.12) \]

where \( \omega_0 = 1/\sqrt{LC} \) is the resonance frequency of the unloaded resonator, \( R \) is the tank impedance at resonance, and \( Q \) is the quality factor of the tank at resonance.

From Figure 5.13, it is clear that the current flowing in each resonator is made up of two components, each in phase with the voltage driving the respective differential pair. This composite current, on the other hand, generates a tank voltage that is in phase with the fundamental component of the current in the cross-coupled differential pair. In exponential notation, the behavior of the quadrature oscillator is described by the following system of equations:

\[ V_I = \frac{I + Ie^{j(\phi)}}{G + jY\omega_{osc}} \quad (5.13) \]
\[ V_Qe^{j(\phi)} = \frac{-I + Ie^{j(\phi)}}{G + jY\omega_{osc}} \quad (5.14) \]
From the above equations, the amplitudes of the output waveforms are:

\[ V_I = V_Q = \frac{I}{G} = \frac{\sqrt{2} I_B}{\pi G} \]  

(5.15)

and the oscillation frequency is given by:

\[ \omega_{osc} = \omega_0 \sqrt{1 + \frac{1}{4Q^2}} \pm \frac{\omega_0}{2Q} \approx \omega_0 \pm \frac{\omega_0}{2Q} \]  

(5.16)

The phase noise performance of an oscillator at an offset frequency \( \Delta \omega \), from the center frequency \( \omega_0 \), is given by [60]:

\[ L(\Delta \omega) = 10 \log \left\{ \frac{2F(\Delta \omega)KT}{P_{sig}} \left[ 1 + \left( \frac{\omega_0}{2Q \Delta \omega} \right)^2 \left( 1 + \frac{\Delta \omega^2}{|\Delta \omega|^3} \right) \right] \right\} \]  

(5.17)

where \( F \) is an excess noise factor, and can be calculated by [61]

\[ F(\Delta \omega) = \frac{1}{\text{tank resistance noise}} + \frac{2\gamma I_B R}{\pi V_I} + \frac{4g_{dohm3}R_p}{M1 \text{ and } M2 \text{ noise}} + \frac{\gamma_3}{M3 \text{ noise}} \]  

(5.18)

and \( P_{sig} \) is the output power of the oscillator, \( Q \) is the quality factor of the tank, and \( \Delta \omega \) is the corner frequency between the \( 1/f^2 \) and \( 1/f^3 \) regions. Thus, the oscillator phase noise can be improved by increasing \( P_{sig} \) and \( Q \). Also, to achieve the minimum phase noise, one has to minimize \( F(\Delta \omega) \) [61].
5.6 Simulation results

The inductors and varactors used in our design are specified in Appendix B. The first step in VCO design is choosing the bias current. As the bias current, $I_B$, is increased, based on Equation 5.15, the VCO swing is also increased. Figure 5.14 shows the variation of amplitude and frequency of the VCO versus varactor voltage control.
Figure 5.11: Result of transient analysis of the mixer.
Figure 5.12: Circuit schematic of QVCO.

Figure 5.13: Output voltages and resonator currents when the output waveforms are perfectly balanced.
Figure 5.14: VCO's amplitude and frequency versus Vctrl (varactor voltage control)
A good choice for VCO voltage control is 1.45V which is in the middle of 1.1V and 1.8V. The phase noise is highly-degraded when the control voltage is between 0.8V to 1.1V where the oscillating amplitude has some variations.

The simulation performance of the QVCO is summarized in Table 5.5 for the typical-typical (TT) process corner. It is observed that in the fast-fast (FF) mode, the value

<table>
<thead>
<tr>
<th>Vctrl</th>
<th>Freq. (GHz)</th>
<th>Amp. (mV)</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.097</td>
<td>352</td>
<td>-116</td>
</tr>
<tr>
<td>1.8</td>
<td>2.768</td>
<td>663</td>
<td>-95.2</td>
</tr>
<tr>
<td>1.3</td>
<td>2.451</td>
<td>505</td>
<td>-85.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vctrl</th>
<th>Freq. (GHz)</th>
<th>Amp. (mV)</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1.991</td>
<td>100</td>
<td>-106.5</td>
</tr>
<tr>
<td>1.8</td>
<td>2.652</td>
<td>440</td>
<td>-96.4</td>
</tr>
<tr>
<td>1.3</td>
<td>2.368</td>
<td>305</td>
<td>-85.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Vctrl</th>
<th>Freq. (GHz)</th>
<th>Amp. (mV)</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.185</td>
<td>530</td>
<td>-110.2</td>
</tr>
<tr>
<td>1.8</td>
<td>2.851</td>
<td>795</td>
<td>-93</td>
</tr>
<tr>
<td>1.3</td>
<td>2.476</td>
<td>640</td>
<td>-86.1</td>
</tr>
</tbody>
</table>

Table 5.5: VCO's characteristics

of L and C is decreased and the oscillating frequency is increased. But in the slow-slow (SS) mode, the Q and R of the inductor are degraded which leads to lower swing in the VCO's output. The worst condition for the circuit is the SS corner case when Vctrl=0.

The QVCO's output (for TT process corner, Temp=27°C) is shown in Figure 5.15 (just three out of four signals are shown). The QVCO has four outputs with 90° phase difference as $LO_I^+$, $LO_I^-$, $LO_Q^+$, and $LO_Q^-$.

Figure 5.16 shows the VCO's phase noise for different control voltages.

The design represented in Figure 5.2 was implemented in a TSMC 0.18µm CMOS
process. A picture of the fabricated chip is shown in Figure 5.17. Because of the number of I/Os, the 44CQFP package was used. The design has 27 pads, as shown in Figure 5.17, of which 23 are I/Os.

The testing procedure for this chip is outlined in Appendix C. The measurements are not reported here since the part was not fully functional. The main test was to apply a 2.4GHz signal at the input and observe the corresponding outputs. We expected to see 40dB gain for the whole RF front-end with down conversion, but we saw very small gain (around 8dB). Further probing of each block (LNA, Mixers, QVCO) required a new board, which is still under construction. While full chip testing is not completed, the basic approach has been demonstrated using simulation in this chapter.
5.7 Summary

In this chapter, the RF-front end design was described and the simulation results of the extracted layouts of all blocks were reported. Also, the novel mixer design which has a controllable gain was introduced: we showed that with changes of $I_{bc}$, the gains of mixers for I and Q can be controlled separately. Since all mismatches of all blocks and components can be modeled as I/Q mismatch at the mixer, separate gain control of I and Q mixer can minimize the effect of I/Q gain mismatch. At the beginning of this chapter, it was shown that with minimizing I/Q gain mismatch, $\epsilon$, the IRR of the RF front-end can improved by up to 20dB, which means that with this technique one of the important requirements of the RF front-end can be relaxed.

The completion of the work will require a new board and another sequence of testing.
to determine the problem with this initial design. The next stage is to fabricate a second chip with the overall RF front-end and DSP back-end to validate the entire approach with controllable mismatch. This will be part of the future work. However, the basic approach has been validated in simulation and is expected to be functional with another iteration through silicon and test.
Chapter 6

Conclusions

6.1 Research Summary

This research introduced a new approach to mitigate the effects of certain analog impairments that plague the direct conversion receiver architecture. For the first time, an AC coupling plus a cross-coupled quantized feedback is applied to a DCR. By using a cross-coupled quantized feedback (CQFB) in DCR, not only are DC offset and 1/f noise removed without wander effect, but also carrier phase error and I/Q mismatch effects are reduced. The proposed approach can be applied to many application while addressing many of the DCR design issues in one solution. It can be implemented in the digital domain for many wireless applications. Motivated by a new paradigm of digital RF processing (DRP) that reduces the complexity of the receiver by maximizing the use of digital signal processing techniques, CQFB is implemented in DSP. Extensive use of digital control and digital signal processing techniques will hopefully relax the requirements on RF and analog circuits.

The main conclusions of this dissertation are as follows:

- The Cross-coupled quantized feedback is a very effective method to address important issues of the DCR, including DC offset and low frequency disturbance; phase
error, and I/Q mismatch and may have a wider range of applications than illustrated in this thesis.

- The completely digital CQFB is implemented to minimize the analog RF front-end non-idealities and to relax it requirements. Since it is better to remove the DC offset before ADC, it would be better to implement the AC-coupling filters in analog domain, and other CQFB filters in digital, and the feedback from digital goes to analog.

- The CQFB is very effective for amplitude-based modulations, however, it is very difficult to implement frequency-based modulation schemes, e.g. GMSK, and GFSK. These contributions are described in more details in next section.

6.2 Thesis Summary

In Chapter 2, various receiver architectures were investigated and their design challenges discussed. The direct conversion receiver architecture offers many advantages over the conventional heterodyne receivers including smaller size, lower cost, and reduced power consumption. However, the design of monolithic receivers using direct-conversion involves many challenges including low-frequency disturbances, namely, DC-offset and 1/f noise (especially in CMOS implementations), I/Q amplitude and phase mismatch, LO leakage, and even-order distortions. The necessary background was described to help understand the nature and severity of various analog impairments. Also, the existing methods to address the DCR design challenges were reported extensively.
We noted that most of the existing methods work only for a specific application or focus on one or two issues. In contrast, we tried to develop a rather general solution to a number of problems with the direct conversion receivers. More specifically, in Chapter 3, a system solution was introduced that mitigates the effects of low-frequency disturbance, phase error and I/Q mismatch. The DC offset and $1/f$ noise are the main design issues of the DCR. A cost-effective method to minimize the low-frequency disturbances is to use AC-coupling in the baseband signal path. Such an approach, however, results in baseline wander effects as the low-frequency part of the signal is filtered out. This is more critical in spectrally efficient modulation schemes such as quadrature amplitude modulation (QAM) where the baseband signal spectrum contains a significant amount of energy near DC. Our system-level solution uses quantized feedback (QFB) in conjunction with AC-coupling to minimize the baseline wander effects. Also, cross-coupled filters are added to the quantized feedback to compensate for the receiver LO phase error and the I/Q mismatch. Theoretical analysis and simulation results, along with practical and implementation issues were reported in this chapter.

In Chapter 4, a digital implementation of the CQFB technique using adaptive filtering was discussed. Our simulation results indicated that the proposed compensation technique can be used to suppress non-ideality effects of receiver front-end sections under realistic signaling assumptions. The low-complexity DC compensation system can be used in a wide variety of applications. I/Q mismatch compensation was addressed using adaptive filtering. Our analysis showed the evolution of adaptive decorrelation from a LMS algorithm for the cases that the mismatches can be assumed constant over the
operating frequency band. Also, a method to estimate the non-ideality parameters was reported that is used along with the CQFB adaptive implementation. Also in Chapter 4, the performance and convergence of the CQFB adaptive algorithm in systems with ISI was derived. The effectiveness of the DSP implementation was validated by a number of results to demonstrate the efficiency of CQFB system to compensate for the most important DCR design issues. This was followed by an optimized implementation for the application of 16QAM signaling that is used in IEEE 802.11g WLAN standard. In addition, successful application of the adaptive CQFB algorithm to OFDM signaling, which has become particularly successful in wireless applications where superb performance in multipath environments is essential, is reported in Appendix A.

In Chapter 5, design and fabrication of a mismatch-controllable RF front-end capable of introducing a desired level of I/Q gain mismatch was reported. The I/Q mismatch parameter of the circuit can be controlled externally by adjusting the shunt current, and hence gain, of I and Q mixers. Therefore, it can be used as a front-end testbench for I/Q mismatch compensation techniques implemented at the back-end. Also, with the capability of compensating I/Q mismatch gain completely, IRR can be increased by 20dB, which relaxes the requirements of RF front-end blocks. A fully-integrated 0.18\(\mu\)m CMOS direct-conversion receiver RF front-end for 2.4 GHz ISM band was implemented for this purpose. This design includes a low-noise amplifier (LNA), two mixers (quadrature down conversion) and a quadrature VCO. The I and Q path mixers can operate in normal mode, or they can be controlled externally to introduce a known mismatch or to compensate for the estimated mismatch. It achieves a conversion gain of 40 dB, and a noise figure of 8.1
dB. The circuit dissipates 25 mW and occupies an active area of 2.5 mm$^2$.

6.3 Future Work

In the current trend of decreasing cost and increasing complexity, delivering more functionality and flexibility is driving the future of integrated wireless devices. Today’s wireless research is now focusing on design of a multi-mode, multi-band radio systems. Since CQFB is not application-specific, it would be useful to investigate an effectiveness and limitation of the application of CQFB in multi-mode, multi-band radio systems, in future.

The methods of Chapter 4 can be implemented in DSP by automatic conversion of Matlab and Simulink codes into a target digital signal processor. The power dissipation of this approach may be high, so this aspect should be investigated further. For industrial implementation of the system, however, the algorithms should be studied from a hardware/software co-design perspective to determine what parts should be hardwired (i.e., the optimal hardware) and what parts should be programmable, to achieve the least-expensive implementation strategy, given the application-specific constraints such as power consumption, frequency band, bit-rate, etc.

The complete design with the controllable front-end and the DSP back-end should be implemented to fully demonstrate the approach. It would be also be useful to study mismatch compensation by using the front-end adjustable I and Q gains. This way, it may be possible to compensate for all non-idealities that cause I/Q mismatch (such as slightly different characteristics of A/Ds) that are not included in our study altogether, by embedding them in the decision feedback loop.
Extension of the adaptive CQFB circuit to wider bandwidth systems, where the mismatches can have larger changes over frequency, is another good subject for further research.

Although 1/f noise was identified to be one of the major problems in direct conversion receiver (DCR) architecture, this research removed 1/f noise as a side-effect of our approach but did not address any specific solution for 1/f noise. It was mentioned in Chapter 2 that 1/f noise belongs to the class of impairments that can primarily be improved using only circuit techniques, for example, by using larger transistors. An extension of CQFB to solve this problem may be possible and should be pursued.

To conclude, this research demonstrated the power of system-level reduction of the impairments of the blocks using a new CQFB approach. Of course, the eventual objective in wireless receivers is to achieve an all digital receiver by converting the signal right at the antenna output to digital. While this may not be feasible today, DRP allows a gradual move in that direction.
Appendix A

Application: OFDM signaling

In this section, the application of the proposed DSP-based receiver architecture in orthogonal frequency division multiplexing (OFDM signaling) is described.

Over the last 20 years, OFDM techniques and, in particular, discrete multitone (DMT) implementation, have been used in a wide variety of applications. OFDM has been particularly successful in numerous wireless applications in which superior performance in multipath environments is desirable. Because of its popularity and performance, we investigate the effect of CQFB on OFDM system.

To that end, a brief description of OFDM is given first. Then, an implementation of OFDM that we used in the simulations is described. Good performance of the system is demonstrated by simulations, the results of which are reported in Section 4.3.5. More details on OFDM signaling can be found in [55], although our implementation (described below) is a bit different.

A.1 Basics of OFDM

OFDM, in conjunction with proper coding and interleaving, is a powerful technique for combating wireless channel impairments. Figure A.1 shows a system block diagram for
OFDM.

Figure A.1: Spectral overlap of subcarriers in OFDM

The frequency response of the ideal channel has a flat magnitude and pseudo-linear (i.e., linear + constant) phase. In the time domain, this translates to pure delay and frequency-constant gain. In the real world, the channels are not ideal thus introducing ISI (as well as noise) in the signal.

However, if the pass-band of the channel is divided into several small bands, each of those bands can be considered a nearly ideal narrowband sub-channel: the magnitude of the frequency response is almost constant and the phase can be considered almost pseudo-linear. The basic idea of OFDM is to modulate several carriers with the center frequencies of each sub-channel at a symbol rate \(K\) times less than the single-carrier system that uses the same channel. The sub-carriers can transmit different bits/symbol (e.g., use M-QAM with various Ms). This way, for example, sub-channels with smaller attenuations (i.e., higher SNRs) can carry more of the data.

The major contribution to the OFDM complexity problem was the application of the FFT algorithm to the modulation and demodulation processes. At the same time,
DSP techniques were being introduced in modems. The technique involved assembling the input information into blocks of $N$ complex numbers, one for each subchannel. An inverse FFT is performed on each block, and the resultant is transmitted serially. At the receiver, the information is recovered by performing an FFT on the received block of signal samples. This form of OFDM is referred to as discrete multitone (DMT). The spectrum of the signal on the line is identical to that of $N$ separate QAM signals at $N$ frequencies separated by the signaling rate. Each such QAM signal carries one of the original input complex numbers. The spectrum of each QAM signal is of the form $\sin(kf)/f$, with nulls at the center of the other subcarriers, as shown in Figure A.1. Figure A.2 shows the OFDM spectrum.

Care must be taken to avoid the overlap of consecutive transmitted blocks. This is solved by the use of a cyclic prefix. The process of symbol transmission is straightforward if the signal is to be further modulated by a modulator with I and Q inputs. Otherwise, it is necessary to transmit real quantities. This can be accomplished by first appending the
Appendix A. Application: OFDM signaling

complex conjugate to the original input block. A $2N$ point IFFT yields $2N$ real numbers to be transmitted per block, which is equivalent to $N$ complex numbers.

A.1.1 OFDM Implementation

In the following, we describe an implementation of OFDM signaling that is used in our simulations. The block diagram of the transmitter is given in Figure A.3. The serial-to-parallel converter divides each $B$ bits of the input data to $K$ groups, with the $i$th group having $b_i$ bits. Using $M_i$-QAM for sub-channel $i$, the multi-carrier modulator selects one of $M_i = 2^{b_i}$ symbols, depending on the data. This way, we will have $K$ symbols for every $B$ bits of the system’s input. Inverse DFT is then applied to the sequence of $K$ symbols. The reason for this operation will be seen later. The real $(x_n; n = 0, \cdots, K - 1)$ part of this sequence is then prefixed by cyclic repetition to make $x_{K-m}, x_{K-m+1}, \cdots, x_{K-1}, x_0, x_1, \cdots, x_{K-1}$, in which $m$ is the length of the channel sampled impulse response. The imaginary part of the signal, $y_n$, undergoes the same process. The resulted sequences are converted to analog signals and are mixed with the carrier sine and cosine carriers to make the band-pass signal to be sent over the channel.

![Figure A.3: OFDM transmission.](image)

Unlike the OFDM implementation of [55] that gives real baseband signals, we used quadrature signaling that is complex in the baseband, but gives real quadrature and
in-phase band-pass components.

Figure A.4: OFDM reception.

The input to the receiver depicted in Figure A.4 is supplied by the RF front end shown in Figure 4.3. In [55], it is shown that the channel ISI corrupts the cyclic prefix (which is easily removed) and affects signal in the following manner.

\[ \hat{X}_i = C_i X_i + \text{Noise}, \quad i = 0, 1, \ldots, K - 1, \]

in which \( X_i \) is the QAM symbol transmitted through the \( i \)th sub-channel, \( \{C_i\} \) is the K-point DFT of the sampled impulse response of the channel \( \{c_0, c_1, \ldots, c_{m-1}\} \) (padded by \( K - m \) zeros), and \( \{\hat{X}_i\} \) is what we have (polluted by noise). Note that the procedure automatically de-correlates the received symbols, thus removing ISI. To recover the transmitted symbols, \( \{X_i\} \), we can measure \( \{C_i\} \) by passing a training sequence through the channel. Alternatively, assuming that we have a good initial guess for \( \{C_i\} \) and that the channel characteristics is constant through time or varies slowly, we can use LMS to adaptively find \( \{C_i\} \).

Since ISI is automatically handled in OFDM signaling as described above, CQFB filters are simply gains in this case. The detection equation becomes the following:
\[
\begin{pmatrix}
Re\{X_i\} \\
Im\{X_i\}
\end{pmatrix} =
\begin{pmatrix}
1/C_i & 0 \\
0 & 1/C_i
\end{pmatrix}
\begin{pmatrix}
I_i \\
Q_i
\end{pmatrix}
+ H Q_i
\begin{pmatrix}
Re\{X_i\} \\
Im\{X_i\}
\end{pmatrix}, \quad i = 0, \ldots, K - 1 (A.1)
\]

in which \( \{I_i + jQ_i\} = DFT_k\{i[n] + jq[n]\}, \quad n = KN, \ldots, KN + K - 1 \) and \( Q_i(.) \) is \( M \)-QAM detector used for demodulation of the \( i \)-th sub-channel. \( H \) is the CQFB gain matrix that is given by Equation (4.3), if the receiver non-ideality parameters are known. Note that we assumed the same \( H \) for all sub-channels. That may not be the case as the sub-carrier frequencies are different for different sub-channels. If the receiver's characteristics significantly vary for different sub-channels, we can consider different \( H \)s.

Equation (A.1) above should be solved for every received symbol, although the DFT operation is performed once for every batch of \( K \) symbols. For an adaptive solution, we assume \( H \) and \( \{C - i\} \) (or an initial guess of them) are known and use the method of Section 4.3.2 to detect the symbols. Once Equation A.1 is solved, it can be considered as two linear filtering equations: (a) with input \( Q_i\{(Re\{X - i\}, Im\{X_i\})^T\} \) (the decided symbol), output \( (Re\{X_i\}, Im\{X_i\})^T \), filter \( H \), and ideal output \( Q_i\{(Re\{X - i\}, Im\{X_i\})^T\} \), and (b) with input \( (I_i, Q_i)^T \), output \( (Re\{X_i\}, Im\{X_i\})^T \), filter \( diag\{(1/C_i, 1/C - i)\} \), and ideal output \( Q_i\{(Re\{X - i\}, Im\{X_i\})^T\} \). Using LMS, the update equations for \( \{C_i\} \) and \( H \) become the following. For \( i = 0, \ldots, K - 1 \):

\[
e_i =
\begin{pmatrix}
A_i \\
B_i
\end{pmatrix}
- \begin{pmatrix}
Re\{X_i\} \\
Im\{X_i\}
\end{pmatrix},
\]

\[
H = H + \mu e_i (A_i \ B_i),
\]
\[ C_i = C_i + \mu (I_i, Q_i) e_i \]

in which \( C_i = 1/C_i \) and \((A_i, B_i) = Q_i \{(Re\{X_i\}, Im\{X_i\})^T\}\) denotes the decision for the \( i \)th sub-channel. Note that \( C_i \) is assumed to be real or the update equations would be a bit different.

A.2 Adaptive ISI and non-ideality compensation in OFDM signaling

In this section, an experiment and its results are reported that confirm good performance of the method described in Chapter 4.

6000 bits of randomly generated bits are to be transmitted by OFDM signaling through AWGN channel with SNR of 15 dB. OFDM employs two sub-channels, the first one with 4-QAM (2 bits/symbol) and the second one with 16-QAM (i.e., carrying 4 bits/symbol) modulation. Therefore, the 6000 bits are transmitted via 2000 symbols. The effects of the channel and the DC-offset removal filter are considered as a single 5-point discrete filter, with the impulse response given below:

\[ h_{ISI}[n] = \{0.82, -0.18, -0.18, -0.18, -0.18\}. \]

Note that in OFDM signaling we cannot use a DC-removal filter with zero DC gain or use a channel that has a zero gain somewhere within the allocated signaling bandwidth. That is because the \( C_i \) corresponding to the sub-carrier that falls on the zero, becomes very
small, making the detection equation (Equation (A.1)) ill-conditioned. In other words, if the channel (i.e., channel + DC-removal filter) has very small gain in a certain frequency (e.g., a zero gain at DC if a DC-removal filter is used), that sub-channel is not suitable for communication and the transmission will suffer from a large probability of error.

In practice, the channel does not have a zero in its pass-band but the DC-offset removal filter at the receiver can make negligible, and make $C_0$ the first sub-channel unusable. To alleviate this problem, we can simply put aside the first sub-channel and use the rest of them for transmission. Alternatively, we can use a filter with non-zero (but small) DC gain for DC-offset reduction. Such a filter reduces the DC-offset that is necessary for good performance of the receiver and, at the same time, allows for using of the first sub-channel perhaps at a lower bit-rate as compared to the rest of sub-channels with higher gains and thus higher SNRs.

In this experiment, we used the second approach above (the frequency response of $h_{ISI}[n]$ is shown in Figure A.5): the DC-offset reduction filter has a small DC gain (-20dB). The receiver non-ideality parameters are considered $\theta = 0.2$rad, $\phi = -0/25$rad, and $\epsilon = 15\%$.

The initial guesses we used for this experiment are $0_2$ and $1_{2\times2}$ for $H$ and $\{C_i\}$, respectively.

The results are shown in Figure A.6. It is observed that the receiver converges within the first 600 symbols, and because of rather high SNR, no error occurs after convergence.

The application of CQFB on the OFDM receiver has been reported, and the result is promising.
Appendix A. Application: OFDM signaling

Figure A.5: The frequency response of the DC-offset reduction filter.

Figure A.6: Cumulative sum of reception errors for adaptive compensation of receiver non-idealities and ISI for OFDM signaling.
Appendix B

On-chip Inductor and Varactor

B.1 Spiral Inductors

The equivalent circuit model of a spiral inductor (not symmetric, with two ends) is shown in Figure B.1, where $L_1$ and $L_2$ are the series inductance and $R_1$ and $R_2$ are the series resistance of the metal lines. $C_{12}$ is the coupling capacitance between the two ports. $C_{ox1}$, $C_{ox2}$, and $C_{ox3}$ are the oxide capacitances between the spiral and the substrate. $C_{sub1}$, $C_{sub2}$, and $C_{sub3}$ are the capacitances of the silicon substrate, and $R_{sub1}$, $R_{sub2}$, and $R_{sub3}$ are the resistances of the silicon substrate. $L_{s1}$ ($L_{s2}$) and $R_{s1}$ ($R_{s2}$) are the inductance and resistance to model the skin effect of the metal track. The quality factor of a spiral inductor is defined as the ratio of energy stored in it over the energy lost in one oscillation cycle. Metal wire resistance, capacitive coupling to the substrate, and magnetic coupling to the substrate limit the Q-factors of on-chip spiral inductors.

The Q factor of the implemented inductor used for the LNA is plotted in Figure B.2. It is observed that for the frequency of our interest, the Q of the on-chip inductor is around 9, which is very good for on-chip inductor.

For the inductor used in VCO, a symmetric inductance with central tap is used. The equivalent circuit model of a symmetric spiral inductor is shown in Figure B.3, which
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is the same as spiral model just L1 and L2 have mutual inductance M and Lct are the inductances due to the central tap metal and Rct is the resistance due to the central tap metal.

If the curve of the Q (Quality factor) of inductor is plotted versus frequency, it is observed that the Q is first increased by increasing frequency due to increase of XL (Inductor impedance) and then decreased because of the impedance of the inductor with parasitic capacitors is decreased.

Moreover, the Q is increased by (1) Increasing f (f < 5GHz), (2) Decreasing T (number of Turns), and (3) Decreasing Radius, R.

Note that as R and T are increased, the $\Delta L/\Delta f$ is also increased which causes the inductor value to change sharply with frequency. In the selection of L and C for resonator, it is important that (1) L be large enough to provide the necessary parallel resistance at the output, and (2) the value of L should be chosen properly, in order to achieve the minimum $\Delta L/\Delta f$. 

Figure B.1: Inductor Model.
B.2 Varactors

We used MOS Varactor. The equivalent circuit representation of the MOS varactor is shown in Figure B.6.

The definitions of the parameters are:

- $L_{gate}$: overall inductance of port 1 vias and gate.
- $L_{sd}$: overall inductance of port 2 vias and bulk.
- $R_{gate}$: resistance of the unit cell vias/contacts as port 1 and gate.
- $R_{sd}$: resistance of the unit cell vias/contacts as port 2 and bulk.
- $C_{gate}$: variable capacitance of the MOS varactor.

\[
C_{gate} = \left( C_{g\ min} + dC_{g} \times \left( 1 + \tanh \frac{V_{g} - dV_{g}}{V_{gnorm}} \right) \right)
\]  

(B.1)
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Figure B.3: Symmetric inductor with tap Model.

Figure B.4: The quality factor of inductor vs. frequency for different values of R
Figure B.5: The inductor value vs. frequency for different values of $R$

Figure B.6: Equivalent circuit of a MOS varactor
Appendix C

Testing of the RF Front-end Chip

In this section, the measurement sequence for the developed receiver front-end is presented. This testing sequence is tailored to the equipment available at the SoC test Lab, and work is still in progress.

For testing, we decided to design two PCB\(^1\) boards, a high-frequency board for the chip itself, and another to generate the low-frequency signals required for biasing and control of the chip. The two boards are connected together using two wire buses. A picture of the two test boards are shown in Figure C.1. The schematics of two boards are shown Figure C.2 and C.3.

The first step was to set up the DC bias points for the circuit under test (labeled as receiver under test or RUT in the following figures), and observe the DC currents flowing through the IC. The bias current can be monitored by using an ammeter. The supply voltage in the circuit should be adjusted to the nominal value as per the simulation. If the current through the circuit is much higher than expected, there might be a short in the circuit, and the DC operating condition will not be satisfied. In this case, another IC sample should be tried. Also, if the circuit is functional, the DC test arrangement can be used for splitting up the current consumption for different receiver blocks. For example, a

\(^1\)Printed Circuit Board
DC test on the entire receiver would indicate the power dissipation of the LNA, mixer, and VCO separately. With biasing, the total power consumption of this design was 2.5mW.

After the DC bias points have been set up, a test was carried out to determine whether the circuit is functional. For the RF front-end, it must down-convert the incoming RF signal to a desired IF frequency. The bias values can be adjusted a little bit to obtain the proper functionality of the circuit. In this specific test, one RF frequency source is used at frequencies of 2.445 GHz (Signal Generator Agilent 8648D is used) and an oscilloscope is used to observe the 5MHz down-converted IF signal. This provides the indication that the circuit is functional as a down-converter. If the circuit does not pass this test, there is a chance that the VCO does not work properly. This design did not pass the functionality
test. However, this contingency was considered and VCO can be turned off, and the quadrature LO signal can be applied externally. Unfortunately, a new board is required for this purpose.

Next, a one-port S-parameter test was performed on the receiver to observe the matching at the input port of the circuit, shown in Figure C.4(a). The calibration for this measurement is performed off-chip. This test should be performed prior to any other tests in the receiver, to verify that maximum power transfer occurs from the RF signal generator to the RUT. Only DC supplies are required for the one-port S-parameter test and vector network analyzer (VNA Agilent 8362B) to measure $S_{11}$.

To measure receiver conversion gain, DC supplies and signal generator for RF input
Figure C.3: Schematic of bias board for testing the chip.

signal are required, as in Figure C.4(b). The two differential output ($IF_{I+}$ and $IF_{I-}$) are connected to the Agilent DSO81304A Scope to measure the conversion gain. For measuring noise figure, DC supplies, a NF meter (Agilent E4440A PSA Series Spectrum Analyzer), and a balun (to obtain a single-ended signal from the differential IF output) are required, as in Figure C.5(a).

For I/Q imbalance and DC-offset test, DC supplies and signal generator for RF input signal are required, as per Figure C.5(b). The four differential output ($IF_{I+}$, $IF_{I-}$, $IF_{Q+}$, $IF_{Q-}$) are connected to the Agilent DSO81304A Scope to obtain the waveform statistics (amplitude and phase information, along with their mean and variance values). From this information, the I/Q imbalance can be extracted. It is important to use exactly identical cables in this test, as the imbalances in the cables might otherwise introduce some I/Q
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(a) Test Setup for S11 parameter

(b) Test Setup for conversion gain measurement

Figure C.4: Test setup for (a) S11 and (b) conversion gain measurements

imbalance during the measurement. The same test setup can be also used for DC offset measurement, just two IF terminals are interfaced with the scope to measure the voltage difference.
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Spectrum Analyzer Agilent E4440A

(a) Test Setup for noise figure measurement

Bias Board

RF

I_F I+

I_F I-

I_F Q+

I_F Q-

Balun

Signal Generator Agilent 8648D

Scope Agilent DSO81304A

(b) Test Setup for I/Q imbalance and DC offset measurement

Figure C.5: Test setup for (a) NF and (b) I/Q imbalance measurements
Bibliography


