ANALYSIS AND FABRICATION OF MIS SOLAR CELLS WITH MAJORITY CARRIER CONDUCTION CHARACTERISTICS

by

HO PIU LAU

B.Sc. (Physics), Chinese University of Hong Kong, 1969
M.Sc. (Physics), University of Toronto, 1974

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Department of ELECTRICAL ENGINEERING

The University of British Columbia
2075 Wesbrook Place
Vancouver, Canada
V6T 1W5

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ABSTRACT

A simple model for a MIS solar cell incorporating the effects of inversion layer charge and non-uniform surface state charge has been generated. The inclusion of these terms in the analysis results in theoretical ln I-V characteristics which, under forward bias in the dark, have a two slope nature very similar to that of practical MIS solar cells that have been reported to be operating in a minority carrier conduction mode. As the present model considers solely majority carrier conduction, an alternative explanation of the operation of these devices can be proposed. Experimental data were obtained from $Al/SiO_x/pSi$ solar cells and good agreement with the proposed theory was obtained.

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CHAPTER 1

INTRODUCTION

The major handicap to using photovoltaic solar energy conversion for large-scale terrestrial applications is the high cost of solar cells. Schottky barrier solar cells seem to be the number one candidates for overcoming this problem because they are very simple to fabricate and need not use high quality substrates. In practice, however, intimate contact metal/semiconductor solar cells exhibit a serious deficiency in the form of very poor photovoltage response. This stems from the fact that the usual thermionic emission dark current in a Schottky barrier junction leads to a considerably higher dark current than in many homojunction and heterojunction structures. Recent experimental work [1] has shown that the presence of a thin interfacial oxide layer between metal and semiconductor in the Schottky barrier cell can increase the photovoltaic conversion efficiency of such a cell.

In the MIS structure the thermionic emission dark current can be reduced by either increasing the effective metal/semiconductor barrier height, decreasing the probability of majority carrier tunnelling, encouraging interface states with a large capture cross-section for majority carriers, or reducing the number of majority carriers at the semiconductor surface.

In several Si MIS structures the dark current has been sufficiently reduced that open circuit voltages appraching those of the very best homojunction diodes have been obtained, i.e. $V_{oc} > 600$ mV [2,3].

A feature of these diodes is that they possess a double exponential forward bias In I-V characteristic which can be described by

$$I = I_{01} \exp \frac{eV}{n_1 kT} + I_{02} \exp \frac{eV}{n_2 kT}$$

where $I_{02} >> I_{01}$, $n_1 \approx 1$ and $n_2 \approx 2$. Such a characteristic is markedly different from the single exponential relationship expected for Schottky barrier diodes and has led to the belief that diodes exhibiting this former characteristic are behaving as induced junction p-n diodes [2]. If this is indeed true then this is a most exciting prospect for photovoltaics in view of the simplicity and cheapness of the MIS technology as opposed to conventional p-n junction technology. The forward bias dark current characteristic in these MIS diodes is thought to be related to the recombination-generation current in the induced depletion layer and the injection-diffusion current in the bulk semiconductor. As these are minority carrier currents and the usual majority carrier current (thermionic emission) is considered to be totally suppressed, such diodes are termed minority carrier diodes [4-6].

A detailed theory has been presented to describe the operation of minority carrier diodes [6] and this is described at the beginning of Chapter 2. However it is postulated by the present author that the features of double exponential I-V curve and good solar conversion efficiency in MIS diodes can also be described by considering the diode dark current to be dominated by classical thermionic emission current (majority carrier current), provided the action of surface states at the insulator/semiconductor interface is taken into account. This new theory is developed in chapter 2, following a brief review of classical thermionic emission theory related to Schottky barrier diodes.

In the present study Al/SiO_x/pSi MIS diodes were fabricated (see chapter 3) and shown (chapter 4) to exhibit good conversion efficiency and double exponential ln I-V characteristics. Chapter 4 also presents some data on the stability of these devices. Taking the experimental data in conjunction with the proposed model allows a description of the distribution of surface states with energy across the band gap of the silicon at the silicon/insulator interface to be formulated. The procedure used is described in chapter 5. The resultant surface state distribution appears very reasonable, thus confirming that the existence of a double exponential ln I-V relationship cannot be taken a priori as evidence of minority carrier diodes. The conclusion is presented in chapter 6, along with suggestions for future work.

CHAPTER 2

SILICON MIS SOLAR CELL THEORIES

As discussed in the preceeding chapter, one school of thought maintains that efficient MIS Si solar cells exhibiting double exponential, forward bias, dark, ln I-V curves may be described as minority carrier tunnel solar cells. However it is the present author's intention to indicate that diodes with such features may also be described as majority carrier devices, where the current is dominated by thermionic emission and device performance is strongly affected by surface states. The theory of minority carrier tunnel solar cells is briefly reviewed in this chapter and then the more classical thermionic emission theory is presented and then developed to include the effect of surface states which is required to describe the experimental data.

2.1 Review of the theory of minority carrier MIS tunnel diodes

Minority carrier MIS tunnel diodes are identical to conventional p-n junction devices as regards their operation at low bias, except for the location of the depletion region. In this kind of MIS diode the contact metal work function and the dopant species in the semiconductor are chosen to ensure that the dominant component of the diode current tunnels between the metal and the minority carrier energy band in the semiconductor. As an illustration, let us choose a p- type substrate.

Figure 1 shows that near zero bias, the surface of the p-type silicon is inverted if the metal contact has a low enough value of work function ϕ_m, (e.g. aluminum). The system fermi level is nearer in energy to the conduction band edge then to the valence band edge and correspondingly

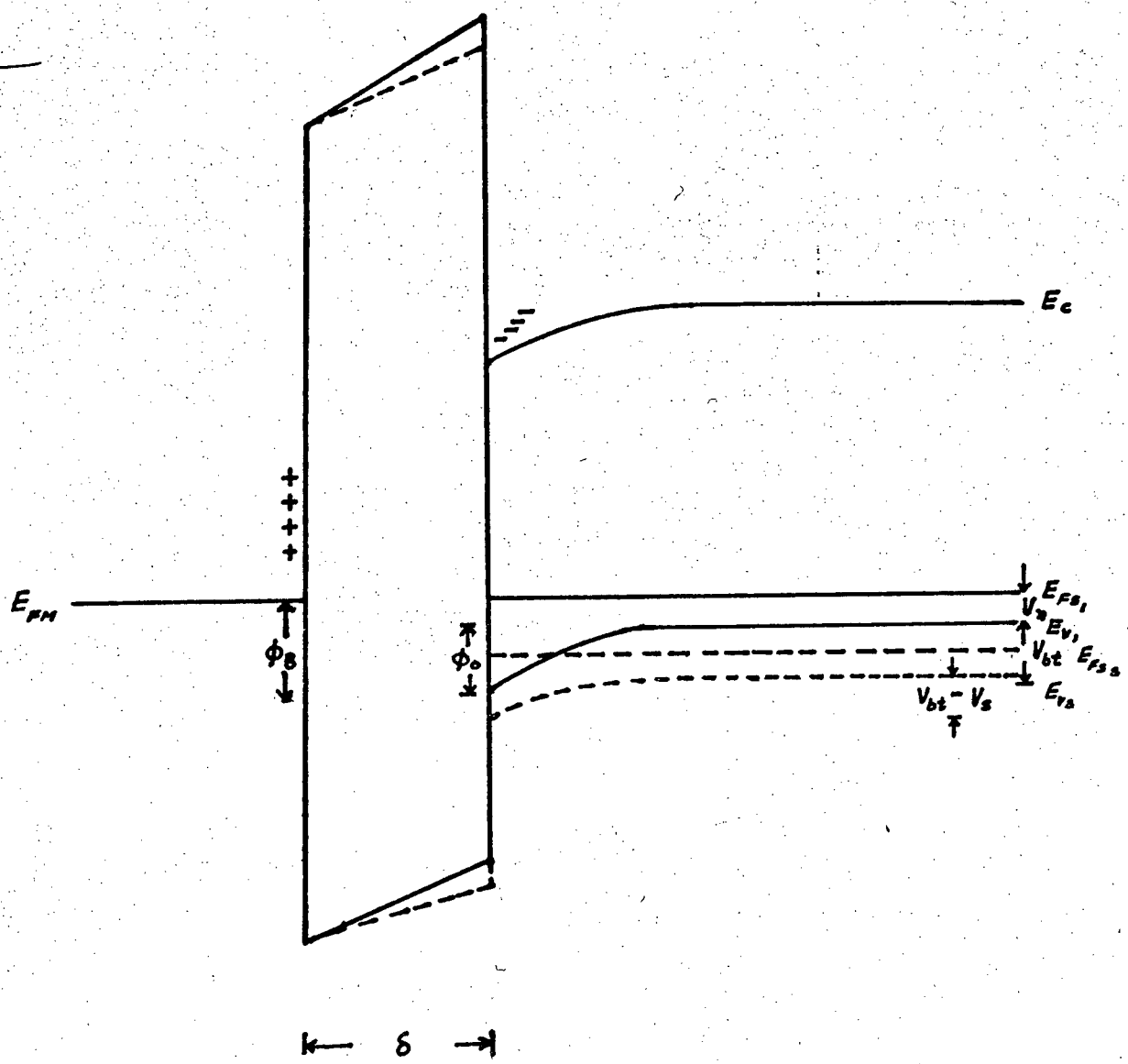


Fig.1. Band Diagram for P-Type MIS Cell

there is a much larger probability that a state of given energy above the conduction band edge is occupied by an electron then a corresponding state in the valence band by a hole. Therefore it is much easier for an electron to tunnel through the oxide and then occupy a vacancy in the conduction band than it is for a hole from the semiconductor to tunnel through the oxide into the metal. These statements are embodied in the tunneling integrals [6].

$$J_{cT} = \frac{q}{2\pi^2 h} \int_{\text{conduction band}} dE(f_m - f_s) \int_s ds\, e^{-\eta} \qquad (1)$$

$$J_{vT} = \frac{q}{2\pi^2 h} \int_{\text{valence band}} dE'(f_s' - f_m') \int_s ds'e^{-\eta} \qquad (2)$$

where $f_{s,m}' = 1 - f_{s,m}$ J_{cT} is the current from the semiconductor conduction band to the metal and J_{vT} is the current from the semiconductor valence band to the metal; f_m, f_s are the probabilities of occupancy of states of energy E in the metal and in the semiconductor. Defining the "shadow" of a constant energy surface to be its projection in wave number space onto a plane parallel to the barrier, the integral is over the overlap of shadows of the metal and the semiconductor constant energy surfaces for energy E. η is given by

$$\eta = \frac{2}{h} \int_{x_a}^{x_b} (P_{Ti}^2 - P_i^2)^{\frac{1}{2}}\, dx \qquad (3)$$

where x is the direction perpendicular to the barrier, x_a and x_b are the classical turning points, and P_{Ti} and P_i are the transverse and total momentum of the tunneling particles in the insulator region.

For the above reasons, in an $Al/SiO_2/Si$ MIS tunnel diode, electrons dominate the carriers which transport current from the semiconductor to the metal. Since the oxide between the metal and the

semiconductor is very thin, the tunnelling current is so large such that it can disturb the MIS diode from thermal equilibrium. Green et al. [6] by using Poisson's equation, the electron and hole continuity equations and the current density expressions in terms of drift and diffusion components and recombination formulae in the bulk semiconductor based on Shockley-Read-Hall recombination statistics, have generated a set of curves for the nonequilibrium MIS diode as shown in figure 2. At high forward bias (>0.3V), the current flow increases rapidly with decreasing insulator thickness. In this region, the diode current is limited by the rate of which particles can tunnel between the metal and semiconductor, which varies approximately exponentially with the insulator thickness. However, at small forward bias and moderate reverse bias, the diode current is virtually independent of the insulator thickness for thicknesses less than 28A°. This difference arises because under reverse and small forward bias, the diode current is limited by transport through the semiconductor rather than by tunnelling through the insulator.

It should be realized that in the minority carrier diodes under discussion the semiconductor surface is inverted near zero bias. This condition remains unchanged for small forward bias. It means that, on moving from the interface into the semiconductor the inversion region is followed by a depletion region and finally a space change neutral region. Therefore according to conventional p-n diode theory, we have the sum of the diffusion current in the space charge neutral region of the device and the generation-recombination current associated with depletion region. One must notice that the diffusive minority carriers in the bulk semiconductor are electrons. Moreover J_{cT} can be split into two portions $J_{cT} = J_{CM} - J_{MC}$

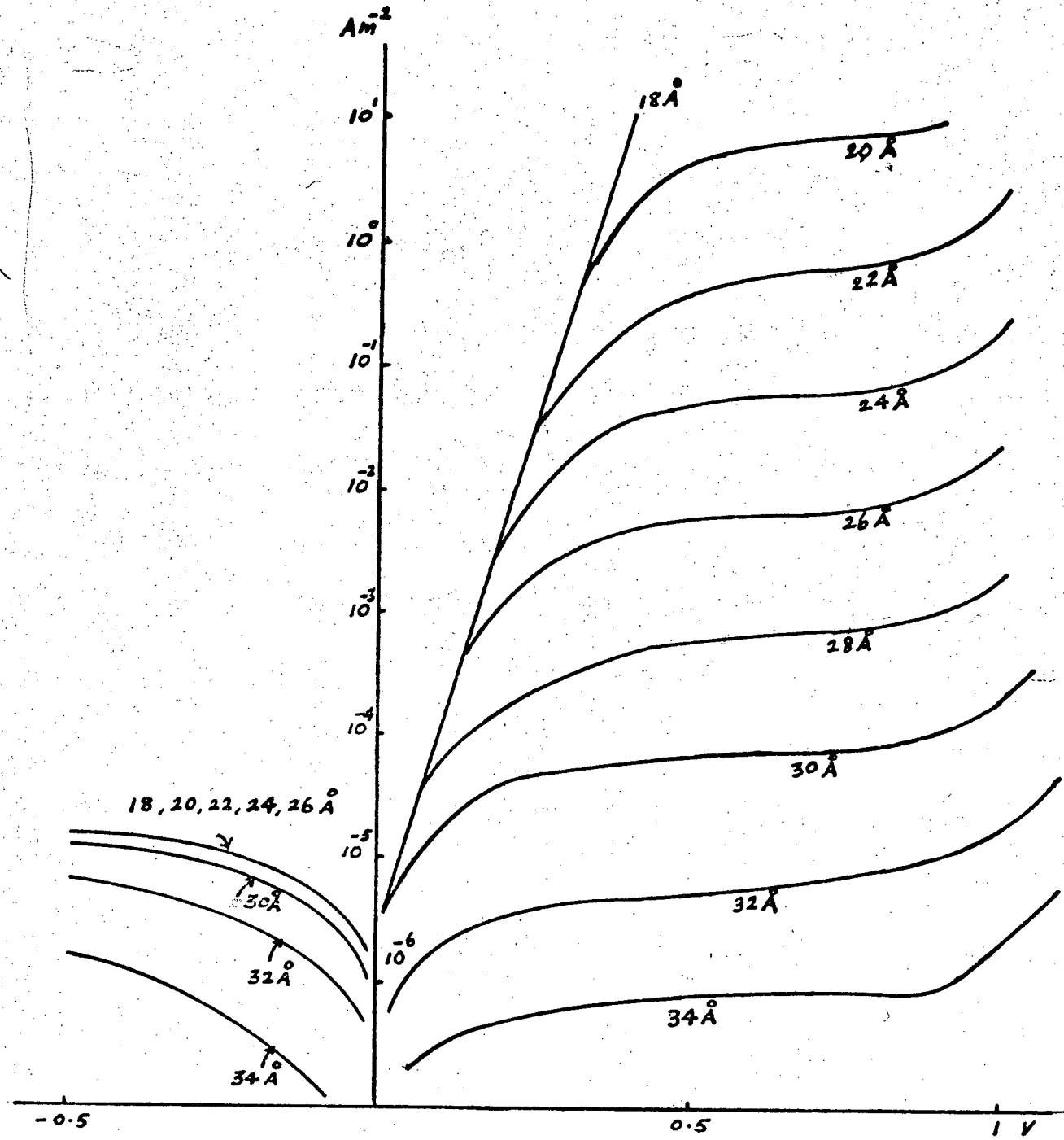


Fig.2. Computed I-V characteristics for "non-equilibrium" MIS diodes for various insulator thicknesses. ϕ_m = 3.2eV, ρ = 2Ω cm. (From Green et al. [6])

where

$$J_{CM} = \frac{q}{2\pi^2 h} \int_{\text{conduction band}} dE\, f_m \int ds\, e^{-\eta} \tag{4}$$

$$J_{MC} = \frac{q}{2\pi^2 h} \int_{\text{conduction band}} dE f_s \int ds\, e^{-\eta} \tag{5}$$

Employing the conventional assumptions of junction diode theory one obtains

$$J_{CM} - J_{MC} = J_d + J_{rg} \tag{6}$$

where J_d is the diffusive component.

J_{rg} is the recombination-generation component of the current.

As the oxide becomes thin, both J_{CM} and J_{MC} increase rapidly and eventually each becomes much larger than the terms on the right hand side of equation (6), at least at reverse and small forward bias. In these bias regions, J_{CM} and J_{MC} must adjust so that their difference is much smaller than either J_{CM} or J_{MC} i.e.

$$J_{CM} \simeq J_{MC} \tag{7}$$

f_m and f_s are the energy distributions of electrons in the metal and semiconductor conduction band respectively. Under thermal equilibrium conditions they are identical and are given by the Fermi Dirac distribution function

$$f_m = f_s = \{1 + \exp [(E - E_F)/kT]\}^{-1} \tag{8}$$

where E_F is the system fermi level. At least for moderate departure from thermal equilibrium, the electron energy distributions can be described in terms of this distribution law by using quasi-fermi levels.

For the metal E_F is replaced by E_{Fm}, the metal quasi-fermi level, while for the semiconductor E_F is replaced E_{Fsn} the electron quasi-fermi level. Then from equations (4), (5), (7) and (8) we get $f_m \simeq f_s$ or $E_{Fsn} = E_{Fm}$, showing that for a thin insulator, the semiconductor electron quasi-fermi level is effectively pinned to the metal fermi level under reverse and small forward bias.

The injection-diffusion and recombination-generation current components can be described by

$$J_{df} = J_{dfo} \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{9}$$

and

$$J_{rg} = J_{rgo} \left[\exp\left(\frac{eV}{2kT}\right) - 1\right] \tag{10}$$

respectively. As for conventional p-n diodes, J_{rgo} is a few orders of magnitude greater than J_{dfo} [4]. This explains the double exponential nature of the forward bias curve for MIS diodes.

As the diode bias is increased in the forward direction, the diode current given by (6) increases rapidly. Eventually J_{CM} and J_{MC} are no longer large compared to the term on the right hand side of equation (6). The fermi levels become unpinned and the current flow becomes tunnel limited. This phenomenon of pinning is described in more detail below.

A voltage V applied to the diode is absorbed as a change in the voltage drop across the insulator and a change in ψ_s, the semiconductor surface potential. If the insulator is thick and the pinning of the fermi level as described above does not occur, the situation is identical to that of a conventional MIS capacitor. A positive voltage V would cause ψ_s to change by an amount less then V reducing the electron concentration in the surface region which in turn reduces the electric field at the

semiconductor surface. V would therefore be absorbed partly as a reduction in voltage across the insulator and partly as a change in surface potential. However, if the electron quasi-fermi is pinned to the metal fermi level, as has been established for thin insulator diodes the fermi level would change by V due to application of this bias. If the electron concentration is to decrease, the potential of the conduction band edge and consequently ψ_s must be changed by more than V. A decrease in electron concentration at the surface again implies a reduction in the surface field. Thus some of V would be absorbed as a reduction in the voltage across the insulator. This is not possible since more than V has already been absorbed in the change of ψ_s. It is concluded that when the electron quasi-fermi level is pinned, the electron concentration in the surface region does not decrease with bias as in a conventional MIS capacitor. In fact, by continuing the above argument it can be shown to increase slightly. It follows that the conduction band edge is also effectively pinned with respect to the metal fermi level in the semiconductor limited regime. Thus the voltage is effectively absorbed by the depletion layer.

Therefore, in summary, the behavior of the diode is related to the pinning of the metal fermi level and the semiconductor minority carrier quasi-fermi level under reverse and small forward bias conditions. This effect tends to clamp the minority carrier concentration in the semiconductor-insulator interface region to its value under zero bias conditions. Thus, for the minority carrier diodes under discussion, this means there is an inversion layer at the semiconductor-insulator interface under both reverse and moderate forward bias. This corresponds to the differently doped regions in a conventional p-n junction diode. As the forward bias becomes large the diode current is eventually limited by tunnelling through

the insulator rather than by diffusion through the semiconductor and the inversion layer disappears. The usual thermionic emission current (majority carrier) is completely suppressed as there are no majority carriers at the interface to communicate with the metal [1].

2.2 Classical Thermionic Emission Theory for MIS Cells

The thermionic emission theory is derived from the assumptions that (1) the barrier height of ϕ_B is much larger than kT (2) electron collisions within the depletion region are neglected and (3) the effect of image forces is also neglected. Because of the above assumptions the shape of the barrier profile is immaterial and the current flow depends solely on the barrier height. The current density $J_{s \to m}$ from the semiconductor to metal is then given by the standard thermionic emission equation [7]

$$J_{s \to m} = \frac{qp(m^*)^{3/2}}{(2\pi kT)^{3/2}} \int_{-\infty}^{\infty} dv_y \int_{-\infty}^{\infty} dv_z \int_{v_{ox}}^{\infty} v_x \exp \ldots$$

$$\left[- \frac{m^*(v_x^2 + v_y^2 + v_z^2)}{2kT} \right] dv_x$$

$$= qp \left(\frac{m^*}{2\pi kT}\right)^{\frac{1}{2}} \int_{v_{ox}}^{\infty} v_x \exp \left(- \frac{m^* v_x^2}{2kT} \right) dv_x$$

$$= qp \left(\frac{kT}{2\pi m^*}\right)^{\frac{1}{2}} \exp \left(- \frac{m^* v_{ox}^2}{2kT} \right) \qquad (10)$$

where x is the direction perpendicular to the barrier, p is the hole concentration and m* is the hole effective mass. The velocity v_{ox} is the minimum velocity required in the x - direction to surmount the barrier and is given by the relation

$$\tfrac{1}{2} m^* v_{ox}^2 = q (V_{bi} - V_s) \qquad (11)$$

where V_s is the potential of the semiconductor surface at the insulator if V_{bi}, the built in voltage is zero. The relationship

$$V = V_i + V_s \tag{12}$$

must hold where V_i is the change of potential drop across the insulator under an external bias V.

The hole concentration p is given by

$$p = N_v \exp\left(-\frac{E_F - E_v}{kT}\right) = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \exp\left(-\frac{qV_n}{kT}\right) \tag{13}$$

Substitution of eqns. (13) and (11) into (10) yields

$$J_{s \to m} = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left(\frac{qV_s}{kT}\right)$$

$$= A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \tag{14}$$

where $A^* \triangleq \frac{4\pi q m^* k^2}{h^3}$ and n is the diode ideality factor, given by

$$n = \frac{V_s}{V} \tag{15}$$

Since the barrier height for the holes moving from the metal into the semiconductor remains the same during external bias, the current flowing into the semiconductor is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor to the metal when thermal equilibrium prevails, ie. when V = 0. The corresponding current density is obtained from Eq. (14) by setting V = 0

$$J_{m \to s} = -A^* T^2 \exp\left(-\frac{q\phi B}{kT}\right) \triangleq J_{sT} \tag{16}$$

The total current density is given by the sum of eqns. (16) and (14)

$$J_p = J_{sT} \left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{17}$$

We shall make use of eqns. (14) and (17) later in the development of the following section.

2.3 Development of the Thermionic Emission Theory to Include the Effect of Surface States in an MIS Structure

2.3.1 The case of a uniform distribution of surface states with energy and neglecting the presence of inversion layer charge

In this first, simple, development the semiconductor space charge is given by $Q_{sc} = - qN_A W$ (18)

where N_A is the acceptor concentration and W the depletion region width.

From Poisson's equation we get

$$\frac{\partial^2 \psi}{\partial x^2} = + \frac{qN_A}{\varepsilon_s}$$

which after integration, yields

$$\varepsilon_s \frac{\partial \psi}{\partial x} = \varepsilon_s E = qN_A x + c$$

Applying the boundary condition

$E = 0$ at $x = W$, yields $\varepsilon_s E = qN_A(x - W)$

Therefore the potential is

$$- \varepsilon_s V = qN_A \left(\frac{x^2}{2} - Wx\right) + c'$$

as $V = 0$ $x = w$ $c' = 0$

$\therefore$ at $x = 0$ $\varepsilon_s V_s = qN_A \frac{W^2}{2}$

Therefore in thermal equilibrium

$$Q_{SC} = - (2\varepsilon_s \, qN_A \, V_{bt})^{\frac{1}{2}} \tag{19}$$

The charge in the interface states is given by

$$Q_{ss} = - q \, D_{ss}(\phi_B - \phi_o) = = q \, D_{ss}(E_{Fss} - E_v - \phi_o) \tag{20}$$

where ϕ_B is the barrier height and ϕ_o is defined as the energy level below which the interface states are donors and above which the states are acceptors and is necessary to fulfil the condition of charge neutrality at the surface. E_{Fss} is the relevant fermi level at the surface, having possible positions between the metal fermi surface and semiconductor fermi surface. We may call it the surface state quasi-fermi level.

Under forward voltage bias in the dark we get, following the same argument preceeding equation (19).

$$Q_{SC}' = - (2\varepsilon_s qN_A(V_{bt} - V_s)]^{\frac{1}{2}} \tag{21}$$

$$Q_{ss}' = - q \, D_{ss}(\phi_B - \phi_o - (\phi_B' - (E_{Fss} - E_v)) \tag{22}$$

Any fixed charge in the interfacial layer is assumed to be uniformly distributed and is given by

$$Q_{fix} = q \, N_{fix} \, \delta \tag{22a}$$

where δ is the insulator thickness and N_{Fix} the volume density of fixed charge. The effect of fixed charge in the insulator region is virtually indistinguishable from change in the metal to insulator barrier height. For the silicon system, a positive charge density of 10^{16} m^{-2} located near the semiconductor-insulator interface causes an effective reduction in barrier height of 0·1eV [10]. However, as a rule of thumb,

the barrier height of a MIS cell is approximately as much as the open circuit voltage of MIS cell at 100 mw/cm^2 [8]. This turned out to be the case in the experimental work presented in chapter 4.

The electric field across the oxide layer is

$$E_i(x) = \frac{1}{\varepsilon_i} [qN_{Fix}\, x - (Q_{ss} + Q_{sc})] \tag{23}$$

From Gauss's law applied to the semiconductor/insulator interface (x = 0) we have

$$-\varepsilon_i E_i(0) - \varepsilon_s E_s(0) = Q_{ss} \tag{24}$$

where $E_s(0)$ is obtained from the following equation evaluated at x = 0

$$E_s(x) = -\frac{1}{\varepsilon_s} \int qN_A dx = \frac{qN_A}{\varepsilon_s}(x - W) \tag{25}$$

Therefore Δ, the potential across the oxide is (at thermal equilibrium),

$$\Delta = \int_{-\delta}^{0} E_i dx = -\frac{1}{\varepsilon_i} qN_{fix} \frac{\delta^2}{2} + \frac{\delta}{\varepsilon_i}(Q_{sc} + Q_{ss}) \tag{26}$$

Similarly, the potential under bias is

$$\Delta' = \int_{-\delta}^{0} E_i' dx = -\frac{1}{\varepsilon_i} qN_{fix} \frac{\delta^2}{2} + \frac{\delta}{\varepsilon_i}(Q'_{sc} + Q'_{ss}) \tag{27}$$

$$\therefore \quad V_i = \Delta' - \Delta = \frac{\delta}{\varepsilon_i}[(Q'_{ss} - Q_{ss}) + (Q'_{sc} - Q_{sc})] \tag{28}$$

From (19), (20), (21), (22) we get

$$V_i = \frac{\delta}{\varepsilon_i}[-q^2 D_{ss}(\phi_B - (E_{Fss} - E_v)) + (2\varepsilon_s qN_A)^{\frac{1}{2}}\{V_{bt}^{\frac{1}{2}} - (V_{bt} - V_s)^{\frac{1}{2}}\}] \tag{29}$$

Where $\phi_B - (E_{Fss} - E_v)$ ranges from $+V_i$ to $-V_s$ [10] and can be conveniently expressed as

$$-(\phi_B - (E_{Fss} - E_v)) = \alpha\, q\, V_i - \beta\, q\, V_s \tag{30}$$

where $\alpha + \beta = 1$ and $0 \leq \alpha \leq 1$

$$\therefore V_i = \frac{\delta}{\varepsilon_i}\left(-qD_{ss}\, q\,\alpha(V_i + V_s) + q^2 D_{ss} V_s + (2\varepsilon_s q N_A)^{\frac{1}{2}}\{V_{bt}^{\frac{1}{2}} - (V_{bt} - V_s)^{\frac{1}{2}}\}\right)$$

(31)

Here α can be conveniently used as the parameter which depends on how E_{Fss} changes with applied voltages. $\alpha = 1$ implies that the effective fermi surface follows the metal fermi surface and $\alpha = 0$ implies that the effective fermi surface follows the semiconductor fermi surface .

If D_{ss} is in $eV^{-1}\ cm^{-2}$ we get

$$V_i = \frac{\delta}{\varepsilon_i}\left(qD_{ss}V_i - qD_{ss}\alpha(V_i + V_s) + (2\varepsilon_s qN_A)^{\frac{1}{2}}\{V_{bt}^{\frac{1}{2}} - (V_{bt} - V_s)^{\frac{1}{2}}\}\right)$$

$$= \frac{\delta}{\varepsilon_i}\left(qD_{ss}(1-\alpha)V_s - qD_{ss}\alpha V_i + (2\varepsilon_s qN_A)^{\frac{1}{2}}\{V_{bt}^{\frac{1}{2}} - (V_{bt} - V_s)^{\frac{1}{2}}\}\right)$$

After arranging terms, this yields

$$(1 + \alpha\frac{\delta}{\varepsilon_i} qD_{ss})n = 1 + \frac{\delta}{\varepsilon_i} D_{ss} + \frac{\delta}{\varepsilon_i}\frac{(2\varepsilon_s qN_A)^{\frac{1}{2}}}{V} n\ \{V_{bt}^{\frac{1}{2}} - (V_{bt} - \frac{V}{n})^{\frac{1}{2}}\}$$

Let $$\gamma = 1 + \alpha\frac{\delta}{\varepsilon_i} qD_{ss}$$

$$A = 1 + \frac{\delta}{\varepsilon_i} qD_{ss}$$

and $$B = \frac{\delta}{\varepsilon_i}(2\varepsilon_s qN_A)^{\frac{1}{2}}$$

Therefore $$\gamma n = A + \frac{Bn}{V}[V_{bt}^{\frac{1}{2}} - (V_{bt} - \frac{V}{n})^{\frac{1}{2}}]$$

$$\gamma n - \frac{Bn}{V} V_{bt}^{\frac{1}{2}} - A = -\frac{Bn}{V}(V_{bt} - \frac{V}{n})^{\frac{1}{2}}$$

Finally a quadratic equation for n emerges namely

$$A^2V^2 + (\gamma^2V^2 - 2\gamma BV_{bt}^{\frac{1}{2}}V)n^2 + (B^2V - 2A\gamma V^2 + 2ABV_{bt}^{\frac{1}{2}}V)n = 0$$

(30)

The solution to (31) is

$$n = \frac{-(2ABV_{bt}^{\frac{1}{2}}V + B^2V - 2A\gamma V^2) + \sqrt{(2ABV_{bt}^{\frac{1}{2}}V + B^2V - 2A\gamma V^2)^2 - 4A^2V^2(\gamma^2V^2 - 2\gamma BV_{bt}^{\frac{1}{2}}V)}}{2(\gamma^2V^2 - 2\gamma BV_{bt}^{\frac{1}{2}}V)} \qquad (31)$$

In estimating n to fit the experimental data (see chapter 4), it was found that D_{ss} should be around 10^{13} $eV^{-1}cm^{-2}$, ϕ_B around 0·8 eV, $\delta \simeq 20$ Å and $\alpha \simeq 0{\cdot}23$. As a sensitivity test various ln I - V curves were generated using equations (31) and (17) for ranges of the parameters ϕ_B, D_{ss}, δ and α in the neighbourhood of the values quoted above. Calculations were performed on a Texas Instrument TI 59 programmable calculator and the results are given in Fig. 3-6.

It is apparent from Figs. 3-6 that the ℓn I-V curves beyond 0·1V are straight lines with, for a given parameter set, a single slope. In order to obtain a double exponential characteristic it was postulated that a variable surface state density should be used, and this would certainly be expected to obtain in practice [7]. The theory just described was therefore refined to include a non-uniform surface state distribution and in view of the more complete nature of this model, the effects of an inversion layer were also considered, see below.

2.3.2 The case of a non-uniform distribution of surface states with the presence of an inversion layer

As a first step in this more detailed analysis, the relations between the surface potential, space charge and electric field are derived [7]. The general situation is depicted in Fig. 7, where the potential ψ is defined as zero in the bulk of the semiconductor and is measured with

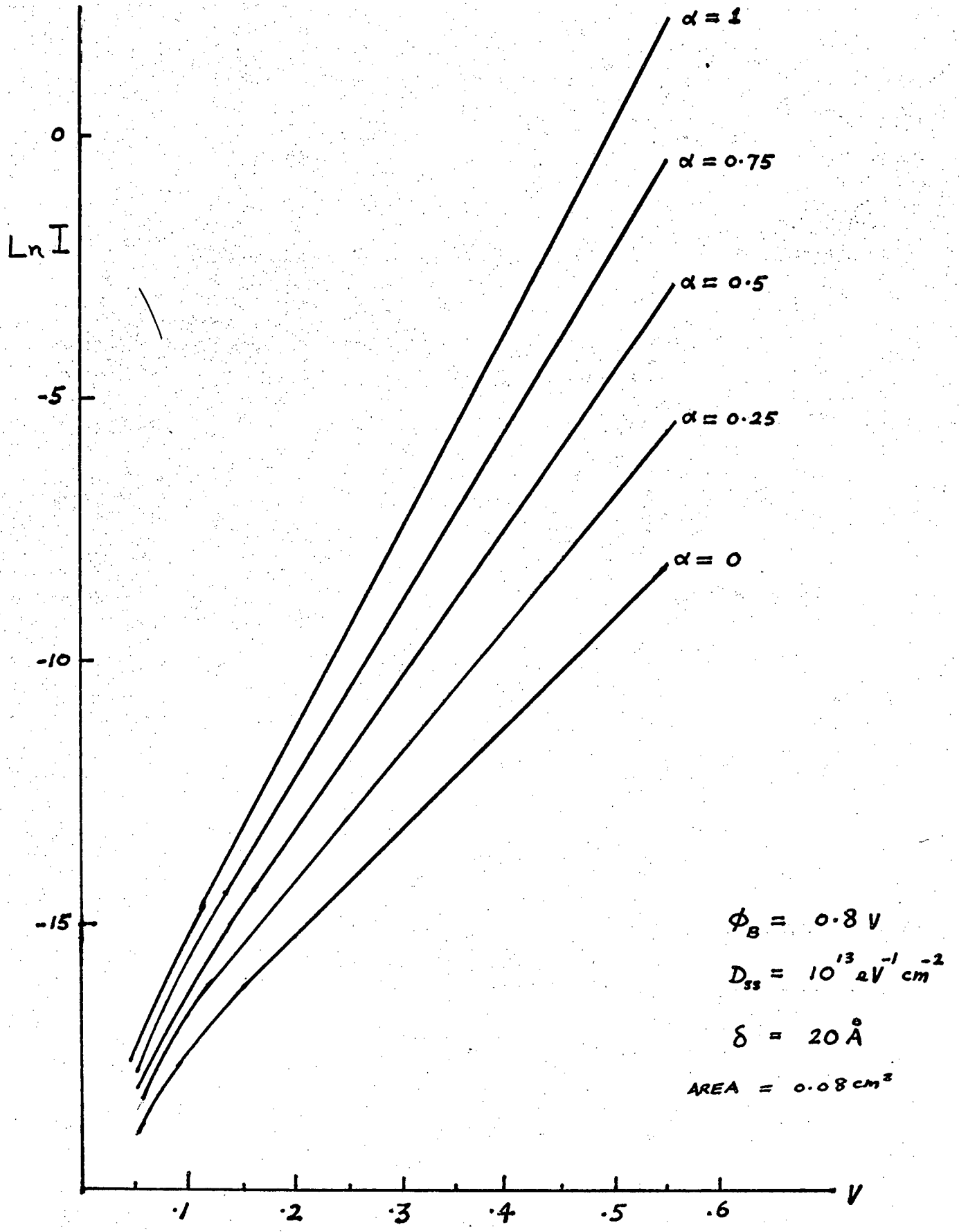


Fig.3. Sensitivity curve (1) for the model of section 2.3.1.

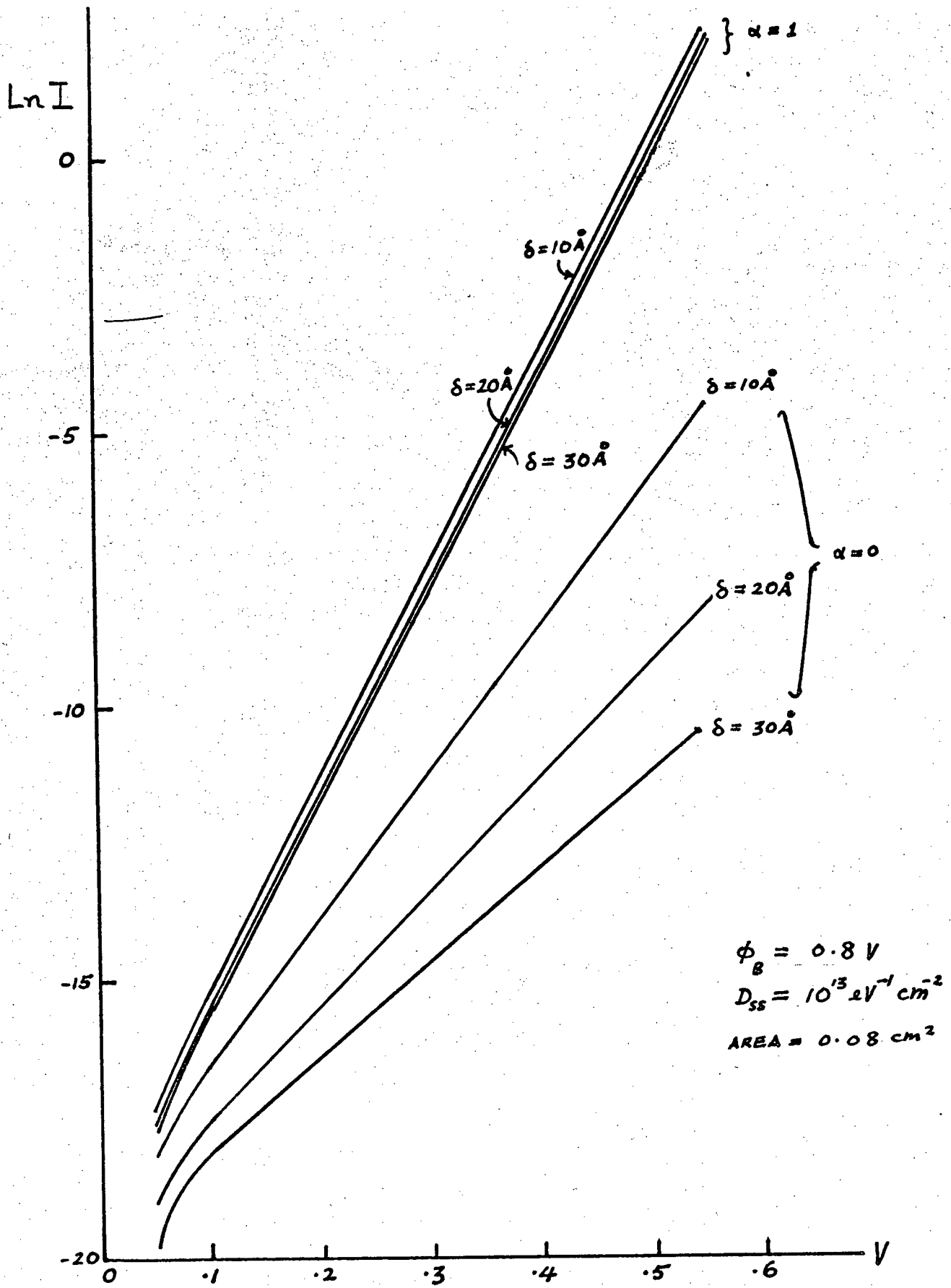


Fig.4. Sensitivity curve (2) for the model of section 2.3.1.

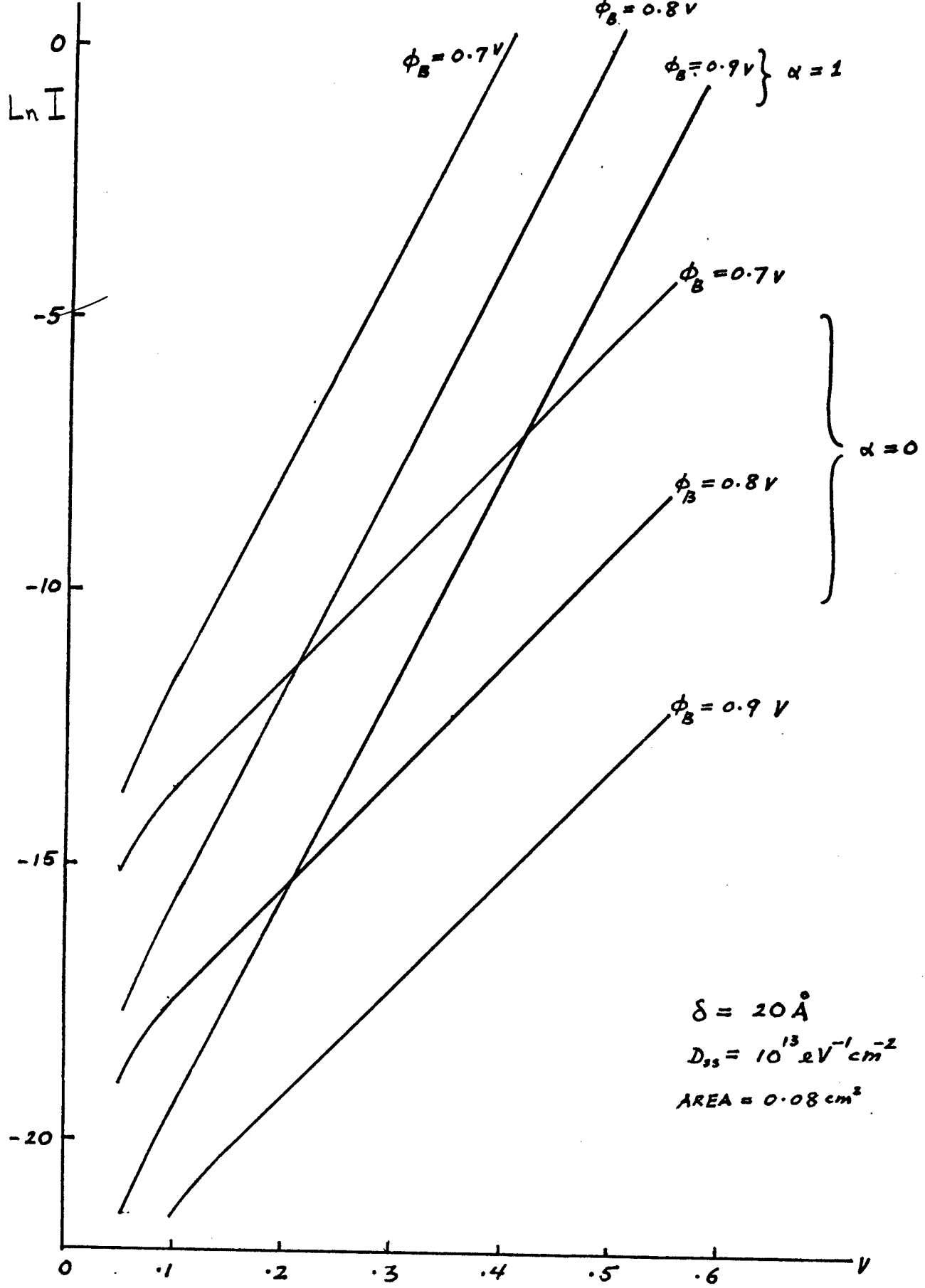


Fig.5. Sensitivity curve (3) for the model of section 2.3.1.

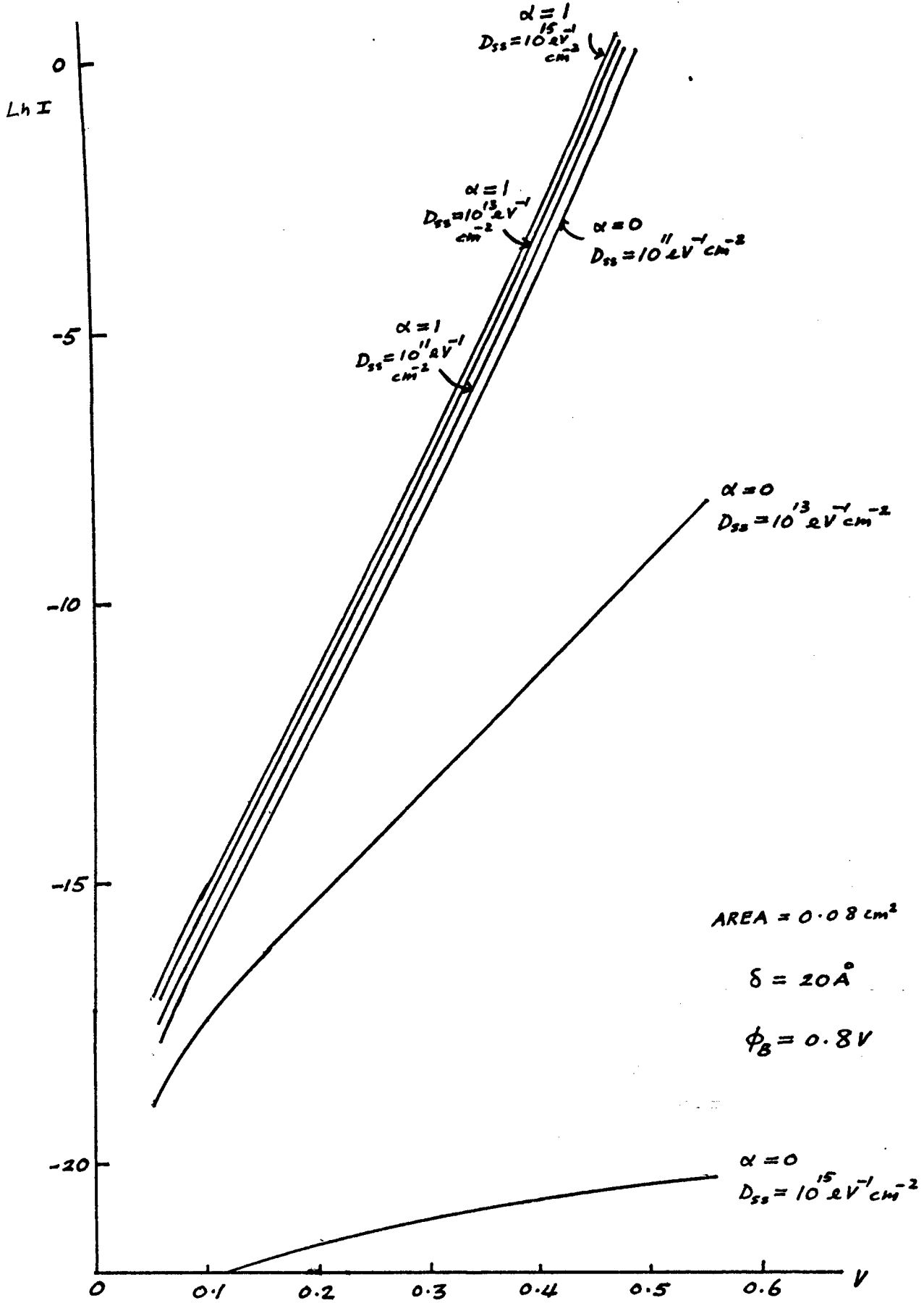


Fig.6. Sensitivity curve (4) for the model of section 2.3.1.

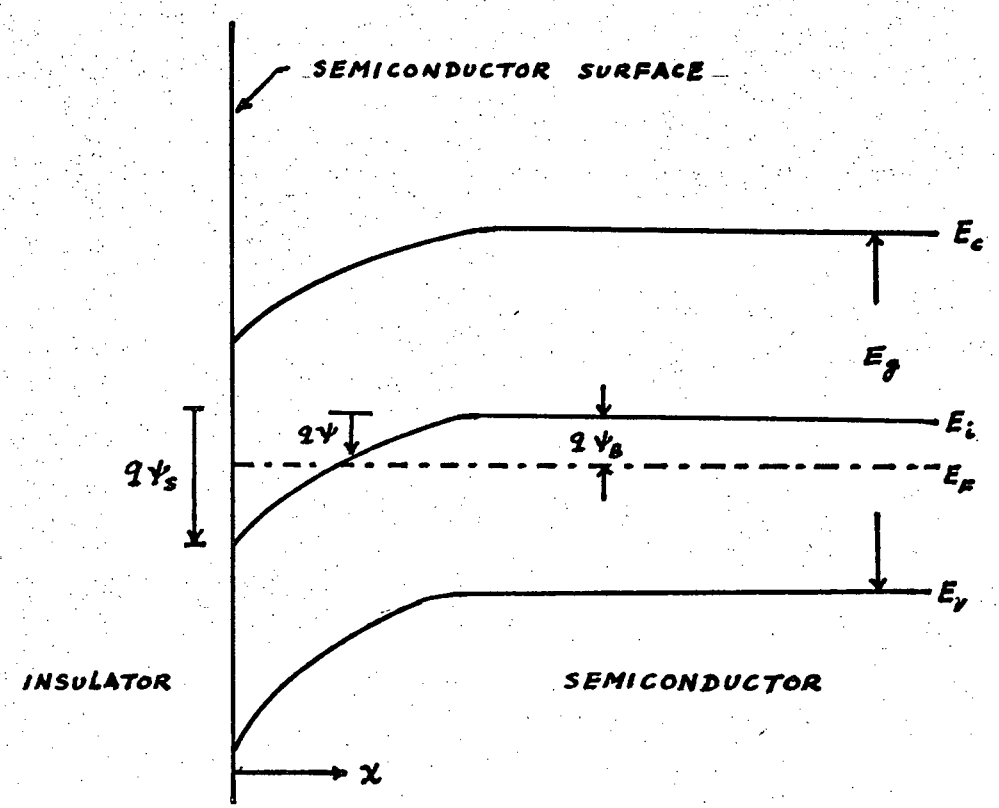


Fig.7. Band Diagram at the Surface of P-Type Semiconductor from SZE [7]

respect to the intrinsic Fermi level E_i. At the semiconductor surface $\psi = \psi_s$ and ψ_s is called the surface potential. The electron and hole concentrations as functions of ψ are given by the following relationships [7].

$$n_p = n_{po} \exp(q\psi/kT) = n_{po} \exp(\beta' \psi) \tag{33}$$

$$P_p = P_{po} \exp(-q\psi/kT) = P_{po} \exp(-\beta' \psi) \tag{34}$$

where ψ is positive when the band is bent downward (as shown in Fig. 7), n_{po} and p_{po} are the equilibrium densities of electrons and holes respectively in the bulk of the semiconductor and $\beta' = \frac{q}{kT}$. At the surface the densities are

$$n_s = n_{po} \exp(\beta' \psi s) \tag{35}$$

$$p_s = p_{po} \exp(-\beta' \psi s) \tag{36}$$

The potential ψ as a function of distance can be obtained by using the one dimensional Poisson equation -

$$\frac{\delta^2 \psi}{\delta x^2} = -\frac{\rho(x)}{\varepsilon_s}$$

where ε_s is the permittivity of the semiconductor and $\rho(x)$ is the total space charge density given by $\rho(x) = q(N_D^+ - N_A^- + p_p - n_p)$ where N_D^+ and N_A^- are the density of ionized donors and acceptors respectively. Now, in the bulk of the semiconductor, far from the surface, charge neutrality must exist. Therefore $\rho(x) = 0$ and $\psi=0$ and we have

$$N_D^+ - N_A^- = n_{po} - p_{po}$$

In general for any value of ψ we have from equations (33) and (34)

$$p_p - n_p = p_{po} \exp(-\beta' \psi) \tag{37}$$

The resultant Poisson's equation to be solved is therefore

$$\frac{\delta^2\psi}{\delta x^2} = -\frac{q}{\varepsilon_s}\left[p_{po}\left(e^{-\beta'\psi} - 1\right) - n_{po}\left(e^{\beta'\psi} - 1\right)\right] \tag{38}$$

Integration of Eq.(38) from the bulk towards the surface yields

$$\int_0^{\frac{\delta\psi}{\delta x}} \left(\frac{\delta\psi}{\delta x}\right) d\left(\frac{\delta\psi}{\delta x}\right) = -\frac{q}{\varepsilon_s}\int_0^{\psi}\left[p_{po}\left(e^{-\beta'\psi} - 1\right) - p_{po}\left(e^{\beta'\psi} - 1\right)\right]d\psi$$

thus giving the relation between the electric field $\vec{E}$ and potential ψ as

$$E^2 = \left(\frac{2kT}{q}\right)^2 \left(\frac{p_{po}\beta'}{2\varepsilon_s}\right)\left[\left(e^{-\beta'\psi} + \beta'\psi - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{\beta\psi} - \beta\psi - 1\right)\right] \tag{39}$$

Let

$$L_D \triangleq \sqrt{\frac{2kT\varepsilon_s}{p_{po}q^2}} \qquad \triangleq \sqrt{\frac{2\varepsilon_s}{qp_{po}\beta'}} \tag{40}$$

and

$$F\left(\beta'\psi, \frac{n_{po}}{p_{po}}\right) \triangleq \left[\left(e^{-\beta'\psi} + \beta'\psi - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{\beta'\psi} - \beta'\psi - 1\right)\right]^{\frac{1}{2}} \geq 0 \tag{41}$$

where L_D is called the extrinsic Debye length for holes. Thus the electric field becomes

$$E = -\frac{\delta\psi}{\delta x} = \pm\frac{2kT}{qL_D}\, F\left(\beta'\psi, \frac{n_{po}}{p_{po}}\right) \tag{42}$$

with positive sign for $\psi < 0$ and negative sign for $\psi > 0$. To determine the electric field at the surface, we let $\psi = \psi_s$ and thus

$$E_s = \pm\frac{2kT}{qL_D}\, F\left(\beta'\psi_s, \frac{n_{po}}{p_{po}}\right) \tag{43}$$

Similarly, by Gauss' law the space charge per unit area required to produce this field is

$$Q_{sc} = \varepsilon_s E_s = \mp \frac{2\varepsilon_s kT}{qL_D} F(\beta'\psi_s, \frac{n_{po}}{p_{po}}) \tag{44}$$

As it becomes rather cumbersome to proceed with the treatment in a completely general way, some numerical parameters relevant to the experimental $A\ell/SiO_x/pSi$ devices described in chapter 4 are inserted at this point namely

$n_i = 1{\cdot}6 \times 10^{10}$ cm^{-3}

$N_A = 1{\cdot}5 \times 10^{15}$ cm^{-3} [13] (taken from the resistivity of chosen sample)

$\varepsilon_s = 1{\cdot}04 \times 10^{-12}$ farad/cm

$T = 300°K$

giving $L_D = 1{\cdot}50 \times 10^{-5}$ cm

As at room temperature $N_A = p_{po}$ it follows from eqn.(44) that

$$Q_{sc} = -\frac{2\varepsilon_s kT}{qL_D}\left[(e^{-\beta' V_{bt}} + \beta' V_{bt} - 1) + 1{\cdot}138 \times 10^{-10}(e^{\beta' bt - \beta' V_{bt}} - 1)\right]^{\frac{1}{2}} \tag{45a}$$

and

$$Q'_{sc} = -\frac{2\varepsilon_s kT}{qL_D}\left[(e^{-\beta'(V_{bt} - V_s)} + \beta'(V_{bt} - V_s) - 1) + 1{\cdot}38 \times 10^{-10}(e^{\beta'(V_{bt} - V_s)} - \beta'(V_{bt} - V_s) - 1)\right]^{\frac{1}{2}} \tag{45b}$$

Notice that if $(V_{bt} - V_s) = 0{\cdot}6$V the second term inside the square brackets in (45b), which corresponds to the inversion layer charge, is about 5% of the first term which corresponds to the depletion layer charge. Therefore this error is present in previous treatments [10] which

have neglected the effect of the inversion layer charge.

The surface states charge, for the case of zero and positive bias are given respectively by

$$Q_{ss} = -q \int_{\phi o}^{E_{Fss}} D_{ss} dE = -q \int_{\phi o}^{\phi_B} D_{ss} dE$$

$$Q'_{ss} = -q \int_{\phi o}^{E'_{Fss}} D_{ss} dE = -q \int_{\phi_o}^{\phi_B - q\beta V_s + q\alpha V_i} D_{ss} dE = -q \int_{\phi_o}^{\phi_B + q\alpha(V_i+V_s) - qV_s} D_{ss} dE$$

The difference is thus

$$Q'_{ss} - Q_{ss} = -q \int_{\phi_B}^{\phi_B + q\alpha(V_i + V_s) - qV_s} D_{ss} dE \qquad (46)$$

where $V_i + V_s = V$

$$V_s = \frac{V}{n}$$

$$V_i = (1 - \frac{1}{n})V, \quad n > 1 \text{ is the diode ideality factor} \qquad (47)$$

The required equation linking n and V turns out to be non linear and follows from equation (28) i.e.

$$0 = -\frac{(n-1)}{n} V + \frac{\delta}{\varepsilon_i} \left[-q \int_{\phi_B}^{\phi_B + q\alpha V - q\frac{V}{n}} D_{ss} dE + \frac{2\varepsilon_s kT}{qL_D} \left[(e^{-\beta' V_{bt}} + \beta' V_{bt} - 1)\right.\right.$$

$$\left. + (1{\cdot}138 \times 10^{-10}) \times (e^{\beta' V_{bt}} - \beta' V_{bt} - 1)\right]^{\frac{1}{2}}$$

$$- \frac{2\varepsilon_s kT}{qL_D} \left[(e^{-\beta'(V_{bt} - \frac{V}{n})} + \beta'(V_{bt} - \frac{V}{n}) - 1) + (1.38 \times 10^{-10})\right.$$

$$\left.\left. \times (e^{\beta'(V_{bt} - \frac{V}{n})} - \beta'(V_{bt} - \frac{V}{n}) - 1)\right]^{\frac{1}{2}}\right] \qquad (48)$$

where $V_{bt} = \phi_B - V_n$ and $V_n = 0{\cdot}23$ in the present case. The above equations were solved using the IBM 370 digital computer at UBC and employing UBC files zero 1 for solving nonlinear equations and QINT4P for integrating among unequal space data points (program shown in appendix 1).

As a check on the computer computation and for the sake of comparing the difference in ln I-V characteristics occasioned by the inclusion of the inversion layer term several curves were generated using uniform values of D_{ss}. The results are shown in fig. 8 and 9 and should be compared with figure 3-6.

Notice that for a given potential, the current is smaller than that in the case when only the depletion layer was considered. This can be explained by noting that with the inclusion of the inversion layer, the potential barrier of the holes is higher for a given potential therefore the corresponding current is smaller because the holes have to overcome a higher barrier to contribute to the conduction current.

Finally, the full equation (48) was solved for the various surface states profiles shown in Fig. 10. The starting profile shown in Fig.10 was taken from Sze [7] and the subsequent modifications were made to arrive at a profile that would fit the experimental data (see section 4·1). The theorectical ln I-V curves corresponding to the above surface state profiles are given in Fig.11. The ln I-V curves show distinctly that a single linear relationship no longer obtains. In fact n is a rapidly varying function of voltage in these cases, see Fig. 12. It is possible however to graphically extract two representative n values for each curve, see table 1, so justifying the description "douple exponential" curve.

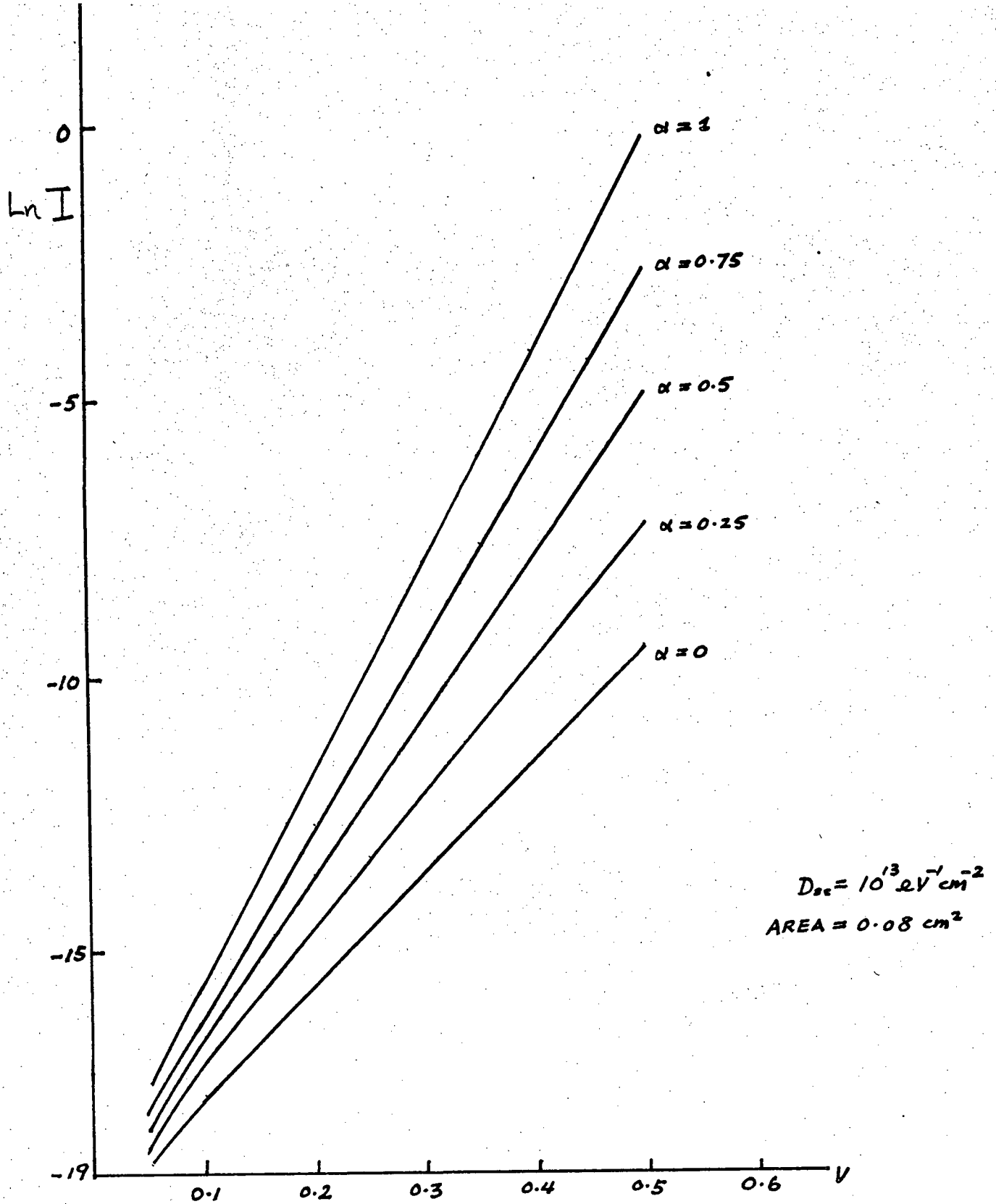


Fig.8. Sensitivity curve (5) for the model of section 2.3.2 for the case of uniform distribution of surface states

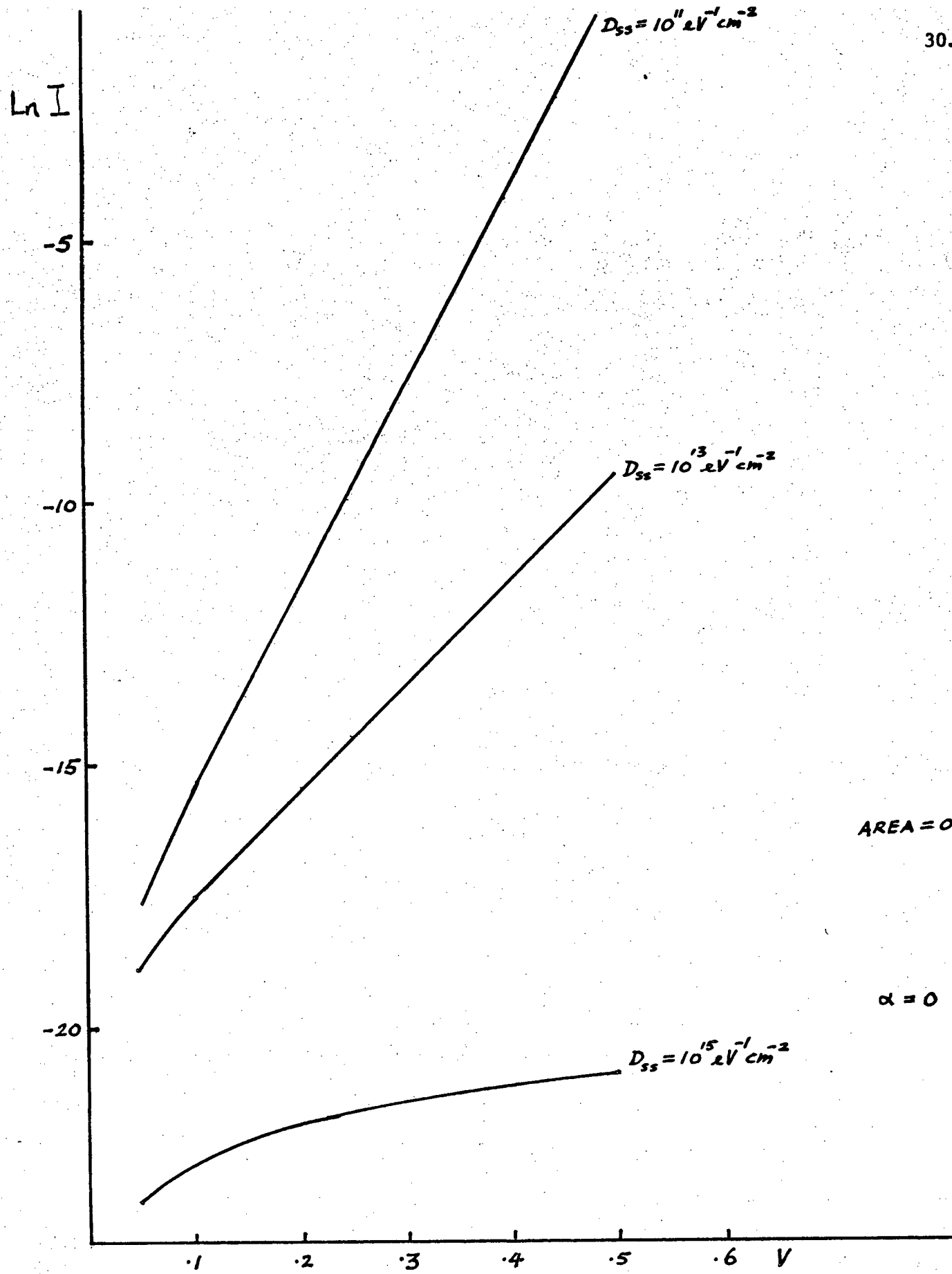


Fig.9. Sensitivity curve (6) for the model of section 2.3.2 for the case of uniform distribution of surface states

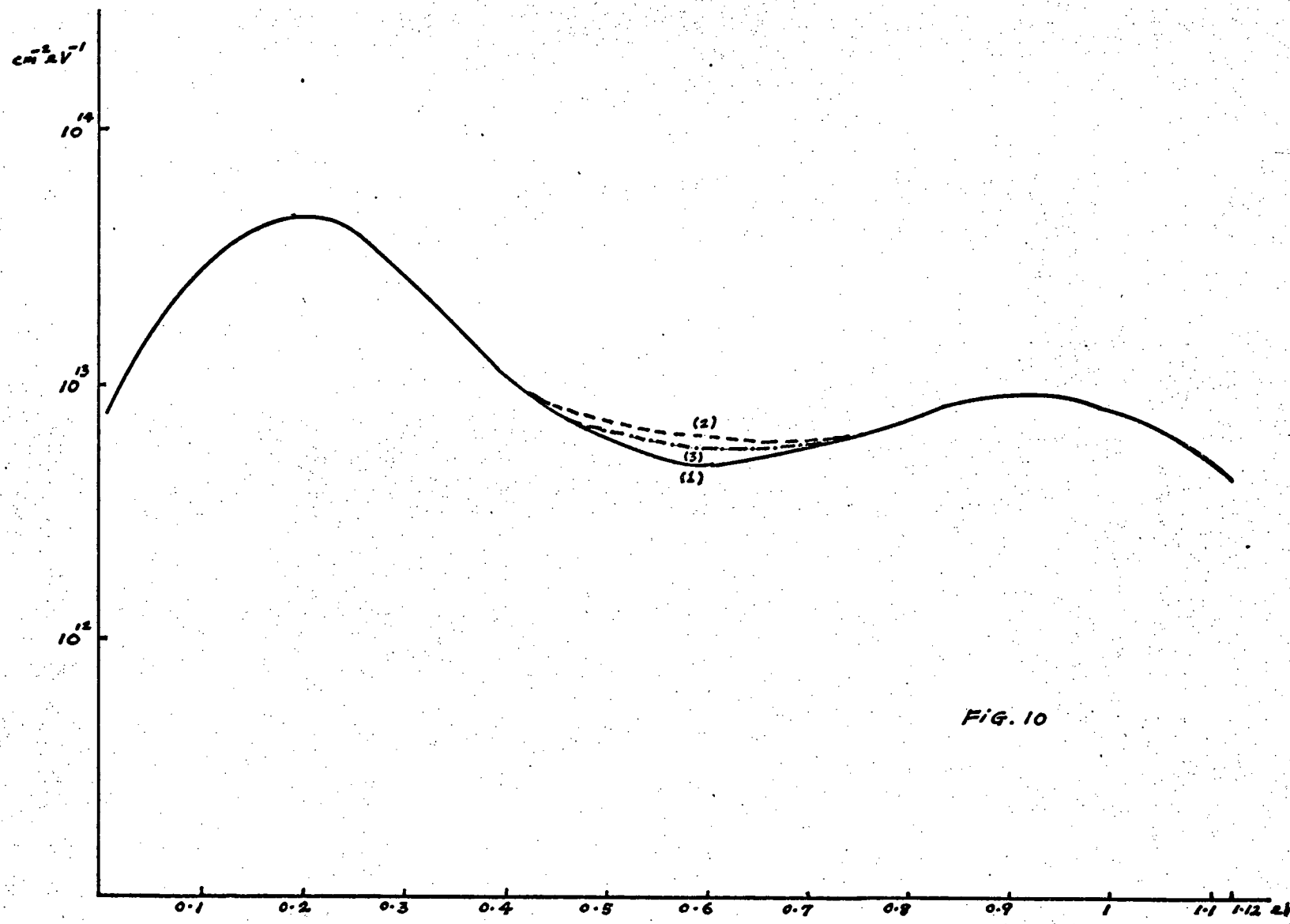


Fig.10. Surface state profiles

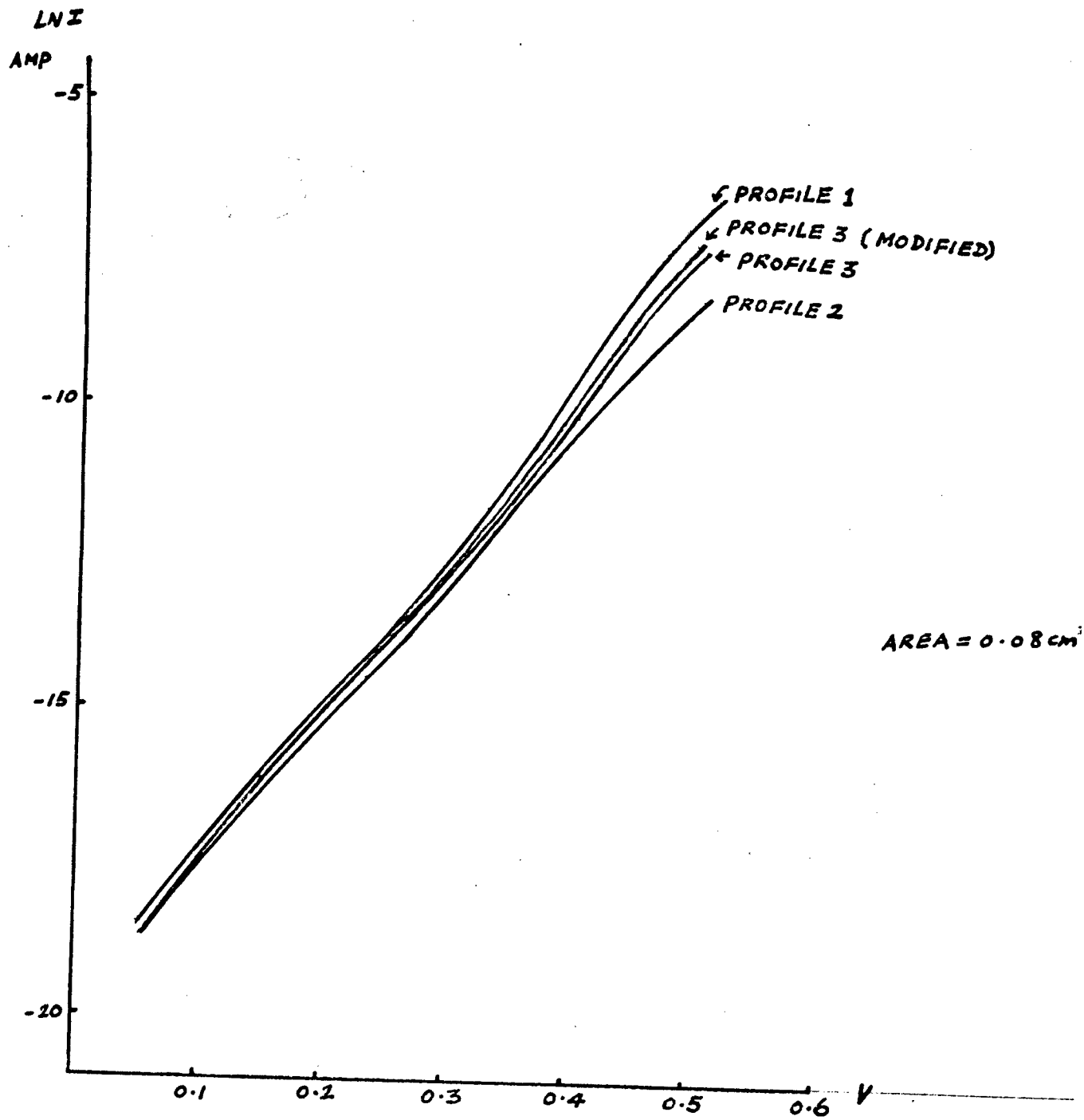


Fig.11. Theoretical Curves for Various Surface State Profiles

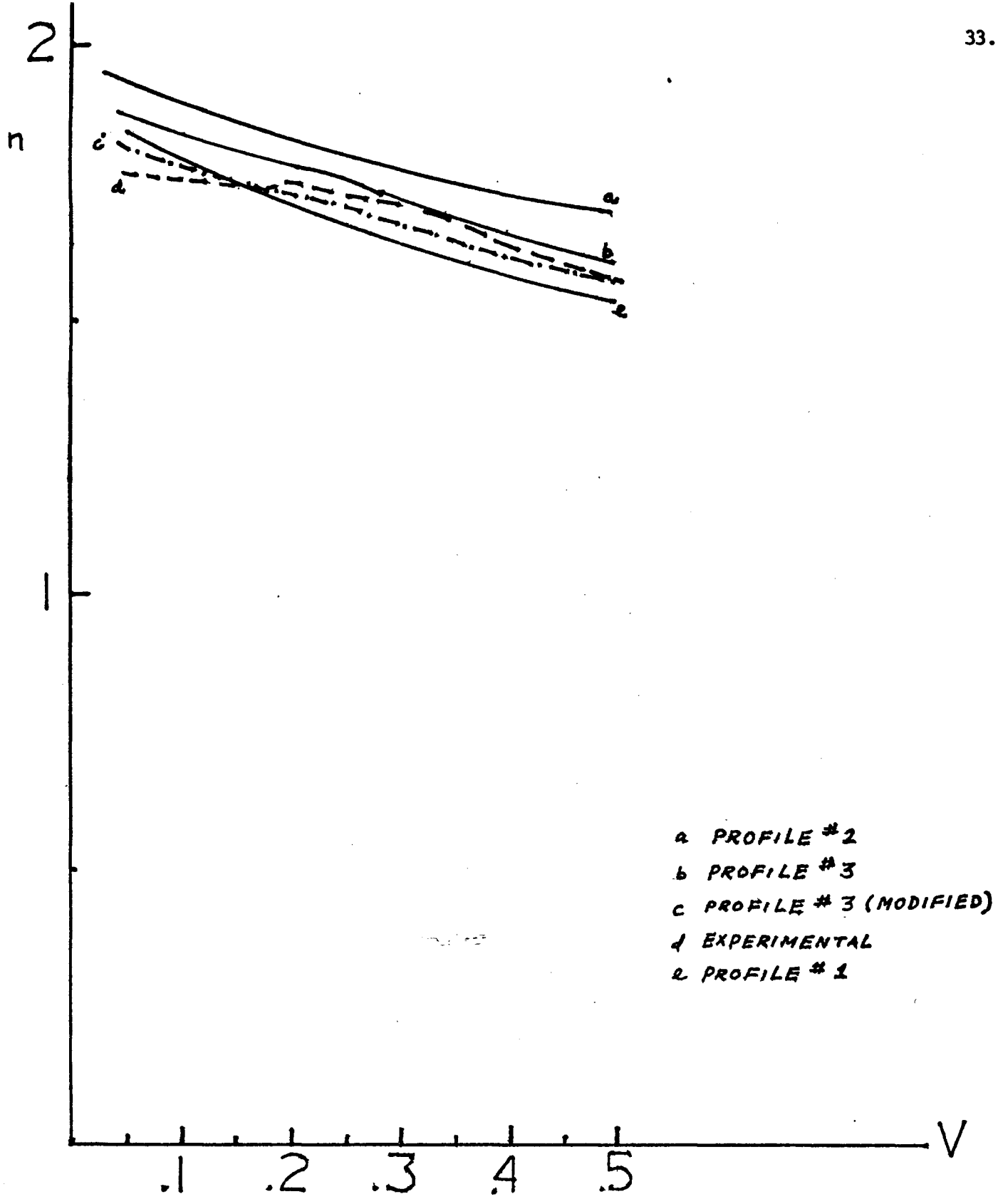


Fig.12. Diode factor (n) vs. voltage plot using data of TABLE 1

TABLE 1: COMPARISON OF THEORETICAL AND EXPERIMENTAL n VALUES

V	PROFILE #1	#2	#3	#3 modified	exp
0.5	1.845	1.938	1.873	1.777	
0.10	1.799	1.906	1.849	1.753	1.756
0.15	1.759	1.869	1.892	1.801	1.753
0.20	1.723	1.839	1.824	1.753	1.753
0.25	1.684	1.811	1.772	1.716	1.745
0.30	1.652	1.786	1.731	1.687	1.745
0.35	1.621	1.767	1.703	1.666	1.722
0.40	1.592	1.748	1.672	1.637	1.67
0.45	1.564	1.727	1.636	1.606	1.625
0.50	1.540	1.698	1.610	1.585	1.585
REPRESENTATIVE n	$n_1 = 1.80$	$n_1 = 1.90$	$n_1 = 1.85$	$n_1 = 1.75$	$n_1 = 1.75$
	$n_2 = 1.50$	$n_2 = 1.70$	$n_2 = 1.62$	$n_2 = 1.60$	$n_2 = 1.62$

Each of the surface state profiles was originally drawn on a 15" x 12" diagram. An electronic digitizer was used to generate data points. There were 10 points per inch. Therefore altogether there were 150 points for each profile.

CHAPTER 3

EXPERIMENTAL PROCEDURES

3.1 Sample Preparation [9]

The thickness and resistivity of 6 < 100 > orientation p-type Si slices was first determined using a micrometer and a four point probe respectively. The bookkeeping indecies of these six slices were P31,P32, P33,P34,P35,P36. The circular slices were of 1.990"to 2.010" diameter of nominal resistivity 2-8 ohm cm, and were polished on the front side. In order to be able to grow oxides of the required thickness for MIS cells (< 30Å), the silicon surface must be thoroughly cleaned prior to oxidation. The cleaning procedure used is described below.

TABLE 2: TEST SAMPLE PARAMETERS

SAMPLE	THICKNESS	RESISTIVITY
P31	310 μm	7.43 Ω-cm
P32	291 μm	6.26 Ω-cm
P33	315 μm	7.57 Ω-cm
P34	313 μm	7.50 Ω-cm
P35	325 μm	7.35 Ω-cm
P36	305 μm	7.42 Ω-cm

(i) The wafers were loaded into a teflon cleaning basket. Two 500 ml. beakers filled with 400 ml. of clean D.I. water were heated to the boiling point. The volume of water was reduced to 360 ml. by pouring some of it out of the beaker. 60 ml. of NH_4OH and 60 ml. of H_2O_2 were then added to the water. Keeping the temperature at 75 - 80°C, the slices were then completely immersed into the solution for 10 minutes. This procedure

was designed to remove organic contaminants which are attacked by both the solvating action of ammonium hydroxide and the powerful oxidizing action of hydrogen peroxide. The ammonium hydroxide also serves to complex some group I and II metals such as Cu, Ag, Ni, Co and Cd.

(ii) The basket of slices was rinsed in D.I. water for 10 minutes.

(iii) A nalgene beaker was filled with 450 ml. of DI water and 50 ml.HF. The slices were kept in this solution for 30 seconds.

(iv) The basket of slices was again rinsed in D.I. water for 10 minutes.

(v) When the water in the second beaker began to boil, the hot water in this beaker was reduced to 360 ml.; 60 ml. of HCl and 60 ml. of H_2O_2 were added to the water. Keeping the temperature at 75 - 80°C, the slices were immersed completely in the solution for 10 minutes. This procedure was designed to remove heavy metals and to prevent displacement replating from the solution by forming soluble complexes with the resulting ions.

(vi) The slices were again rinsed in D.I. water for 10 minutes.

(vii) The slices were blown dry in a stream of nitrogen gas.

Before fabrication of the solar cells, a p^+ diffusion in the back side was made to facilitate making an ohmic contact. The procedure employed was as follows [9].

(i) oxidation:- The target of the thickness for the masking oxidation was 6000Å. The furnace temperature profile was established and set so that the centre zone temperature was 1100 ± 5 °C. The gas flow rates used were

O_2 1 litre/min

H_2 1.6 litre/min

N_2 1.0 litre/min

Hcl 50 cc/min

and the gas cycle was

5 - 5 - 2Hrs - 5 - 30

which has the following meaning::

5 minutes for O_2 to grow a thin oxide against Hcl pitting and to initiate the heat up cycle.

5 minutes for O_2 and 5% HCl. The usage of the HCl was to passivate the first thin layer of oxide and to clean the silicon system.

2 hrs $H_2 + O_2 + HCl$ to enhance "wet" oxidation and the usage of HCl was to keep SiO_2 from contamination by sodium. The next 5 minutes of O_2 was used for safety reasons to purge the HCl.

The final N_2 step was used to densify the SiO_2, to reduce surface states and to redistribute any possible phosphorous that may have "plowed under" due to rapid oxidation. After the above oxidation procedure, the batch of slices was pulled out from the furnace and allowed to cool down. One side (the polished side) of each slice was then skillfully waxed before the whole batch was dipped into a 75% HF solution for 15 minutes. Then, after rinsing for 10 minutes in D.I. water and blowing dry in nitrogen, the batch was sequentially dipped into two beakers of boiling trichlorethylene for periods of 10 minutes each. After blowing dry, chromic acid was used to clean from the slice the dirt which was contributed by the wax and not removed by the trichlorethylene treatment. After

rinsing in D.I. water, the whole batch was then put through the complete cleaning procedure described at the beginning of section 3.1, prior to carrying out the p^+ back side diffusion.

The p^+ diffusion consisted of two parts, the first part was the predeposition and the second part was the drive-in step.

(a) Boron Predeposition

The boat for loading the slice was predoped for the cycle mentioned below except that the doping time was prolonged to 15-20 minutes.

With the following characteristics, a 10 - 5 - 15 cycle was carried out:-

Furnace temperature :- 1090 ± 5°C

Dopant (source):- B_2O_2 is methyl alcohol plus some HCl

Source temperature :- 15°C

Gas flows :- Coarse or carrier N_2 2 litres/min, Fine or source N_2 60 c.c./min

Besides the main batch of slices four test-pieces of N type (four half slices) were loaded into the boat for sheet resistance, and junction depth measuring. The characteristics of the test slices were as tabulated in table 3.

The cycles were 10 - 5 - 15

Explanation	Function
10 minutes of coarse N_2	Heat up part of cycle
5 minutes of souce + coarse N_2	Doping part of the cycle
15 minutes of course N_2	purge dopant plus slight diffusion

TABLE 3

CHARACTERISTICS OF TEST SLICES USED TO INVESTIGATE BORON DIFFUSION

SAMPLE n-type	THICKNESS μm	RESISTIVITY BEFORE DOPING Ω-cm	RESISTIVITY AFTER DOPING Ω-cm	JUNCTION DEPTH μm
B1	300	0.0131	Not measured	8.4
B2	303	0.0131	0.0025 (p-type)	Not measured
B3	303	0.0129	Not measured	8.8
B4	301	0.0128	0.0026 (p-type)	Not measured

(b) Drive in step:-

The diffusion conditions were:-

Furnace temperature:- 1090 ± 1°C

Gases O_2 1·5 litre/min

N_2 1·5 litre/min

Cycle $2\frac{1}{2}$ hr - $\frac{1}{2}$ hr

$2\frac{1}{2}$ hr for dry oxygen, $\frac{1}{2}$ hr. nitrogen (purge and surface state reduction).

After these procedures, the batch was pulled out from the furnance and cooled down then stored in Fluroware plastic 1" diameter boxes.

As required the wafers were removed from the storage container and immersed in a 75% HF solution for 15 minutes to strip the protecting oxide away. After rinsing and blowing dry, the slice was carefully cut into four quarters by a diamond scriber and the slices were returned to the storage container. When needed for final solar cell fabrication each quarter slice was loaded into a specially designed basket suitable for handling quarter slices and the normal cleaning procedure as mentioned on page 35 was performed. Gold was then deposited on the unpolished side of the quarter slice under 7×10^{-6} mm Hg vacuum in a Veeco vacuum system using a specially designed planetary fixture. The thickness was determined to be 2000Å, using an Inficon 321 thickness monitor.

The next step was to alloy in the gold film and was a critical procedure as the very thin interfacial oxide was also grown at this time. The sample was inserted into a furnace held at 495°C and subject to an oxygen flow of 1·0 lm^{-1} for times of 2-10 minutes, depending on the thickness of the interfacial oxide required. The gas environment was then changed to nitrogen (1·0 lm^{-1}) and alloying was continued for 20 minutes. After this the sample was withdrawn to the end of the furnace tube and allowed to cool down in the nitrogen stream. The previously bright appearance of the gold took on a mottled character if the alloying had been successful.

The next processing step was the barrier metal deposition and this was achieved by thermal evaporation of aluminum through a metal mask (shown in Fig. 13) in a vacuum of 8×10^{-6} mmHg. The mask had four circular holes with area 0.08 cm^2 each and a very thin transparent aluminum film ($\simeq$ 100Å) was deposited on the slice at a rate of 10Å/sec. This low evaporation rate and thickness was to optimize the trade-off between transparency and sheet resistance [8]. The first mask was replaced by a second mask which defined the area for a contact stripe to each diode. An aluminium thickness of 1000Å was used for the contact fingers.

3.2 The I-V Characteristic Testing Station

In order to measure both the dark and illuminated I-V characteristics of the diodes a special testing station was built, see Fig. 14. The aluminum enclosure was painted black on the inside and could be sealed by a tight fitting lid, also painted black, to permit the taking of dark I-V characteristics. For measurements under simulated sunlight the lid was removed and the sample illuminated by light from four ELH tungsten halogen lamps (colour temperature = 3200°K) filtered by a wide band hot mirror. The irradiance was adjusted to 100mWcm^{-2} (AM1 sunlight intensity) by varying the power supplied to the lamp and the intensity was measured by a JEA 450B optical power meter. This instument was also used to calibrate a commercial photosensor (model HAV -4000B from EG and G) which was mounted in the measurement enclosure alongside the test cell. As the operational amplifer inside the photosenser could only deliver about 5 mA (which was not large enough to supply the photodiode under 100 mW/cm^2 irradiation) a booster circuit was built to allow operation at 1 Sun

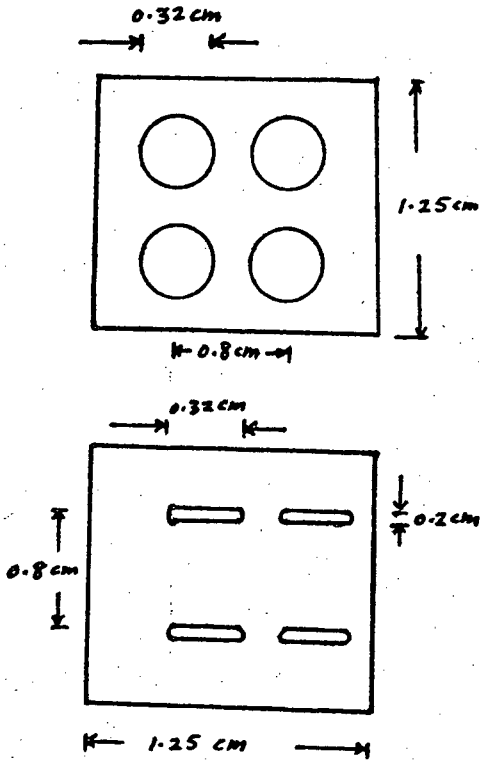


Fig.13. Masks for Aluminum Barrier Metal and Contact Finger Evaporations

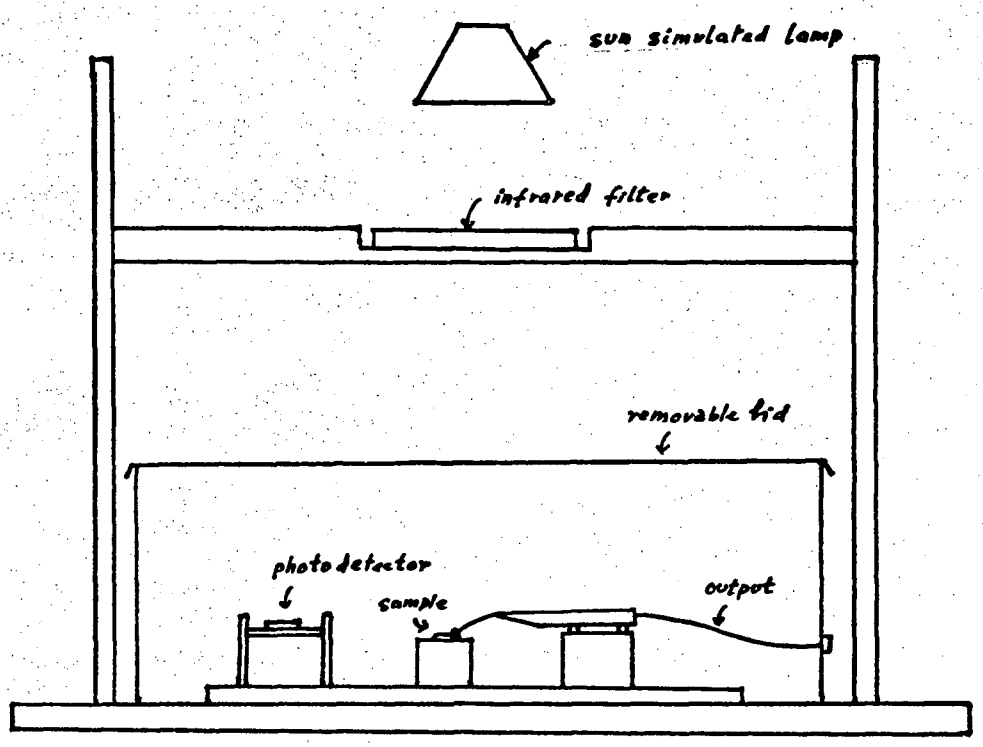


Fig.14. I-V Test Station

intensity, see Fig. 15. Prior to the testing of each experimental solar cell, the desired simulated sunlight intensity was set using the commercial sensor and then the base on which the sensor and test cell was mounted was moved so that the test cell assumed the position previously occupied by the sensor. The test wafer was supported on a gold plated brass block, using a vacuum chuck to ensure good contact to the back side, and the top contact was made via a gold probe fixed to a micropositioner. Standard BNC coaxial sockets mounted on the wall of the enclosure served to connect the test cell to the outside measuring equipment. The circuit for measuring the dark current is shown in Fig. 16. The important point is that the voltmeter which was used to measure the voltage across the diode is connected after the electrometer to avoid drawing current from the diode. The potential drop across the electrometer was calculated and was taken into account for obtaining the voltage across the diode. The circuit for measuring the light current is shown in Fig. 17. A 1 ohm resistance was added to the circuit for measuring the current. The reason for choosing such a low value of resistance was to ensure nearly short circuit conditions when measuring the current with the load resistance shorted out.

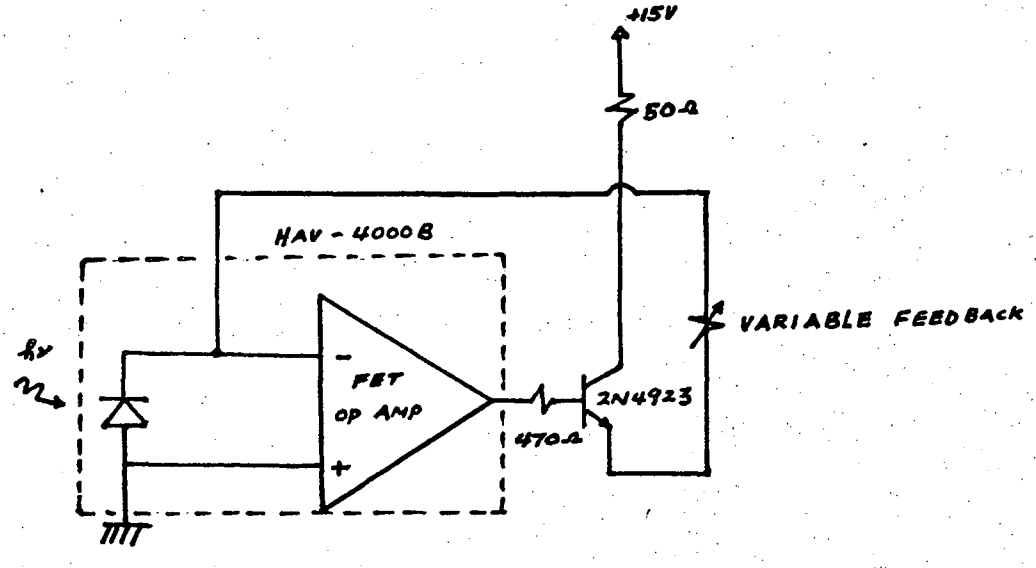


Fig.15. Booster Circuit for Reference Photocell

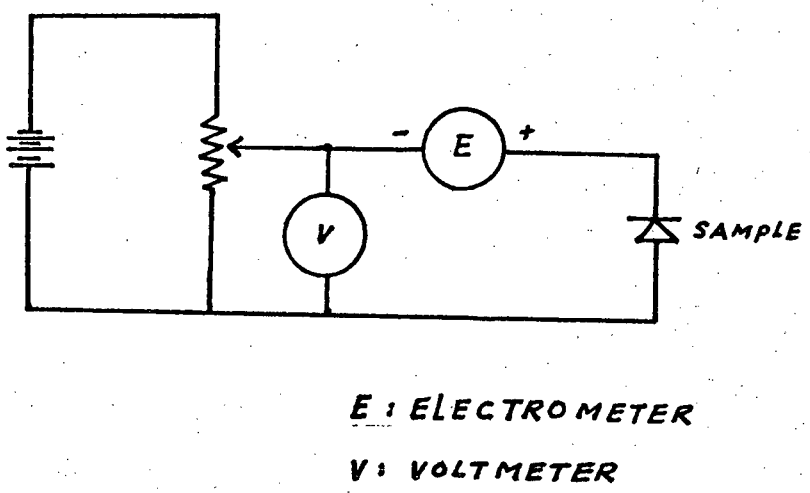
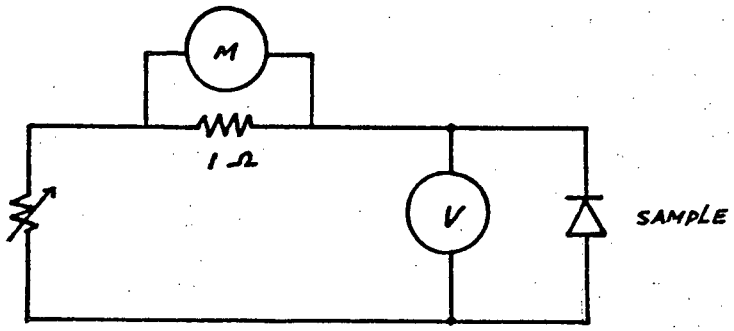


Fig.16. Dark I-V Measuring Circuit

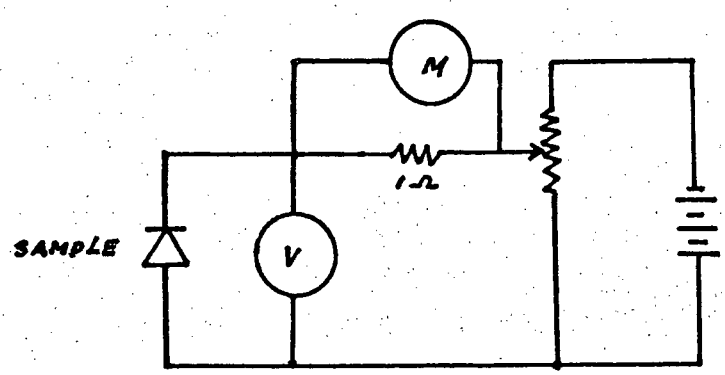
LIGHT I-V MEASURING CIRCUIT



M : MICROVOLTMETER

V : VOLTMETER

LIGHT BIAS I-V MEASURING CIRCUIT



M : MICROVOLTMETER

V : VOLTMETER

Fig.17. Light and Light Bias I-V Measuring Circuit

CHAPTER 4

RESULTS

4.1 Dark I-V Curves

The dark forward current-voltage characteristics of MIS solar cells for devices with interfacial oxide formation times of 10,5,2,0 minutes are shown in Fig. 18. The diode factors for these curves ranged from 1.4 to 1.9 for low and relatively high bias respectively. The I_{01}, I_{02}, n_1 and n_2 values which correspond to the terms in the equation

$$I = I_{01} \exp \frac{eV}{n_1 kT} + I_{02} \exp \frac{eV}{n_2 kT}$$

are shown in Table 4. Beyond 550 mV, series resistance or tunnel limiting effects dominate and the curves bend down toward the voltage axis. The curious effect that the solar cell with thick oxide (5 min. oxidation time) has larger dark current then the solar cell with thinner oxide (2 mins oxidation time) beyond 400mV seems to be contradictory to a recent theory [12] (in which the thicker oxide cells should have smaller dark current). However, this could be explained by allowing that the surface state distributions may have been widely different for the two cells [6]. The double exponential effect in these curves was not very conspicuous except for the "5 minute" diodes. Again this could be explained by the surface effect.

4.2 Light Characteristics

The I-V characteristics of the 4 diodes under illumination both with and without electrical bias are shown a Fig.19 and Fig.20 respectively.

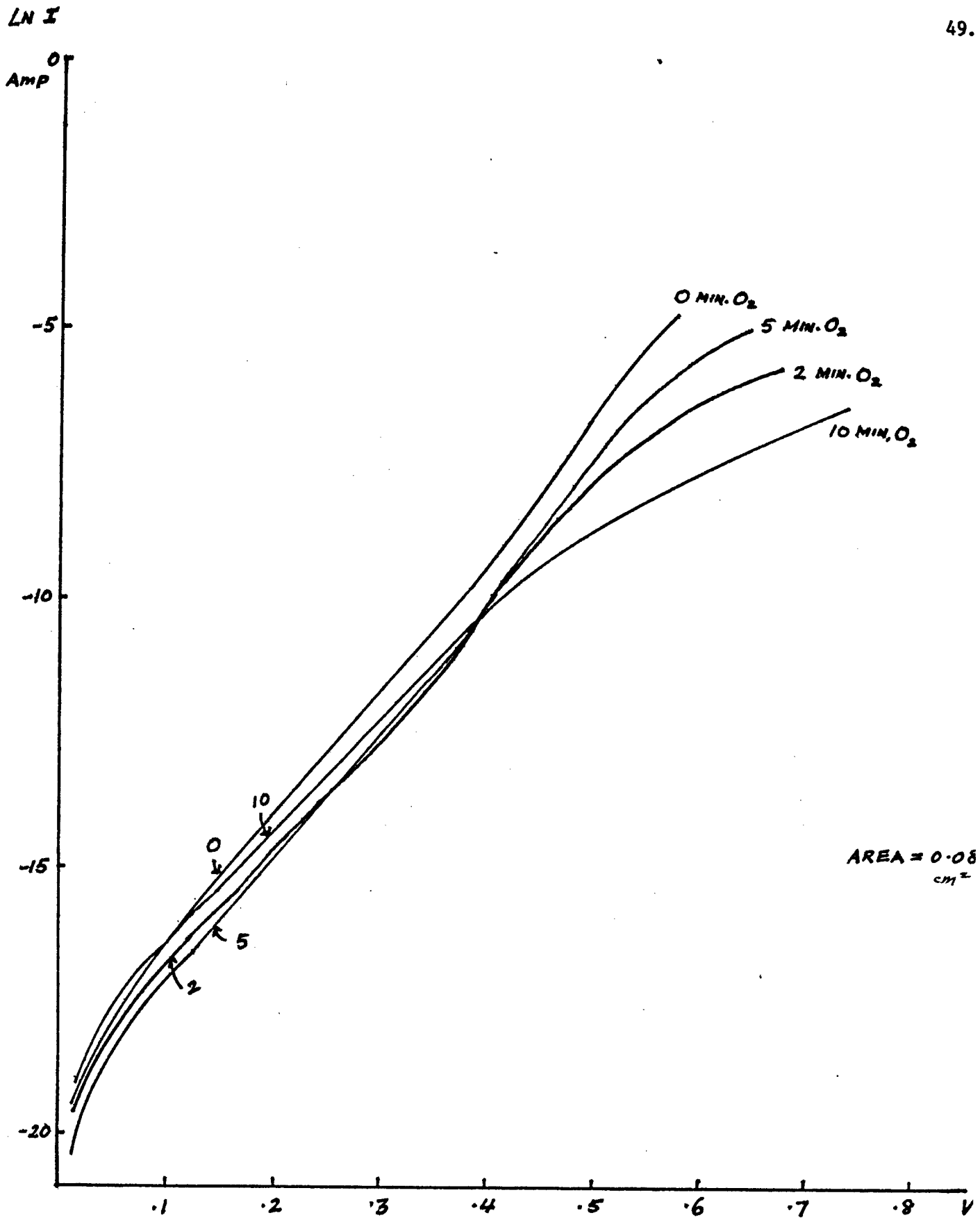


Fig.18. Experimental Dark I-V Curves

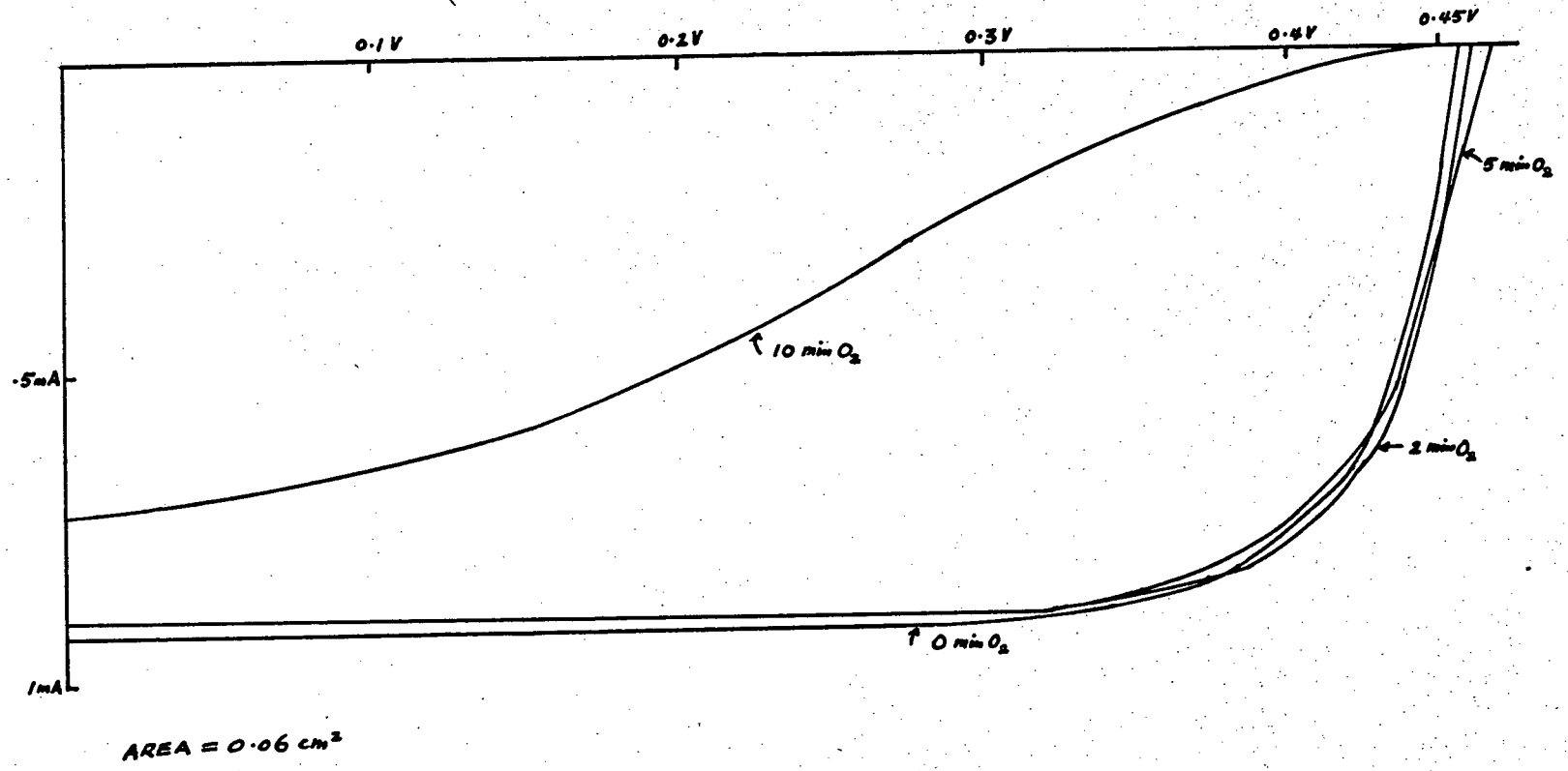


Fig.19. Experimental Light I-V Curves

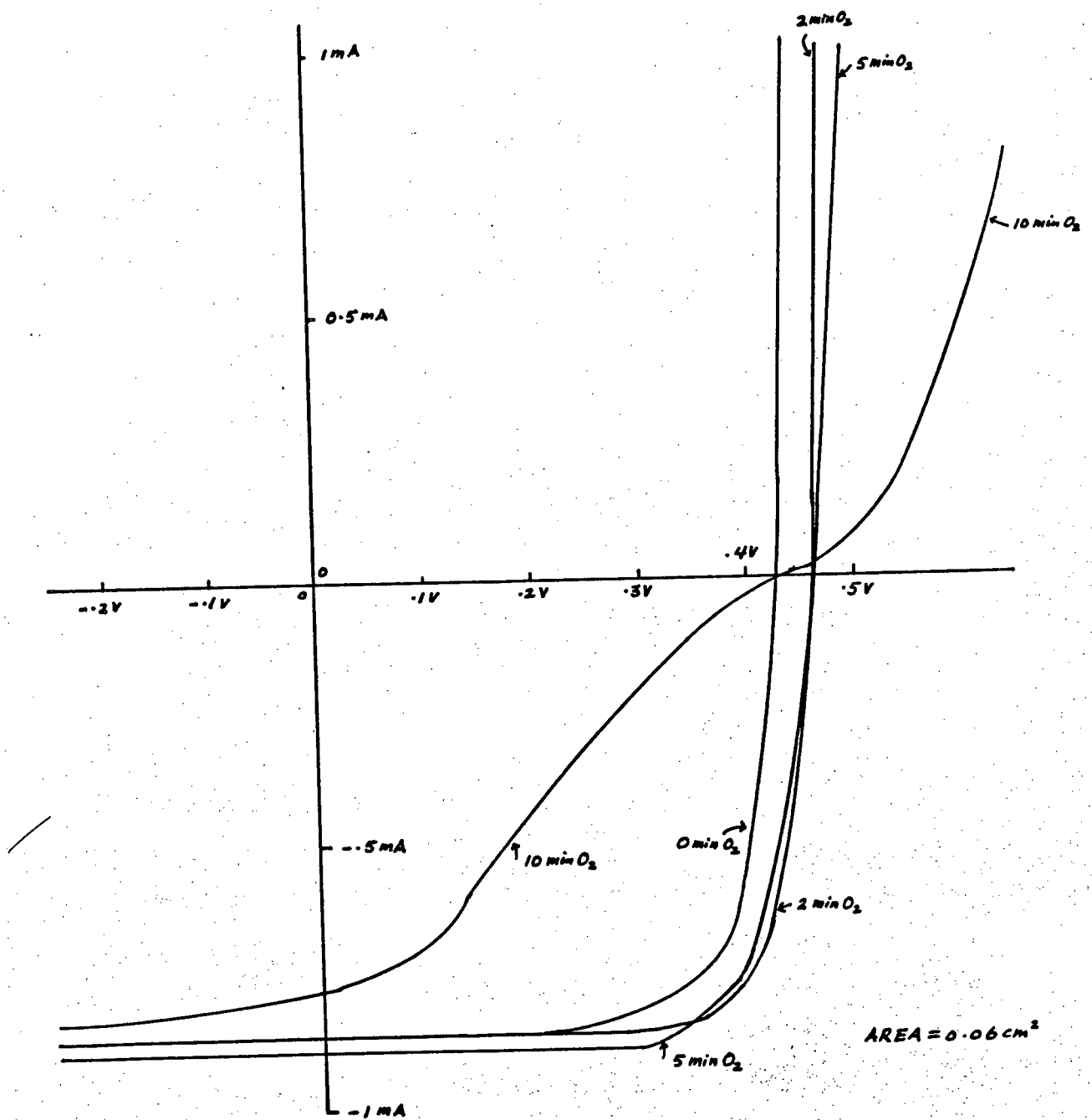


Fig.20. Experimental Light Bias I-V Curves

TABLE 4

SUMMARY OF EXPERIMENTAL DIODE DATA SHOWN IN FIG. 18

REF#	OT(min)	$I_{01} \times 10^{-9}$ AMP	$I_{02} \times 10^{-9}$	n_1	n_2
P33(4)b	0	10.21	1.69	1.84	1.41
P33(3)a	2	6.19	1.69	1.88	1.51
P33(1)a	5	3.76	0.76	1.80	1.41
P33(2)b	10	7.56	7.56	1.64	1.64

TABLE 5

SUMMARY OF EXPERIMENTAL DIODE DATA SHOWN IN FIGS. 19 AND 20

REF#	OT(min)	Voc (VOLTAGE)	I_{sc} $(\frac{mA}{cm^2})$	FF	η
P33(4)b	0	0.476	15.3	0.72	5%
P33(3)a	2	0.480	15.0	0.74	5.2%
P33(1)a	5	0.486	15.5	0.69	5%
P33(2)b	10	0.462	11.8	0.25	1.2%

OT = OXIDATION TIME

One may observe that the photovoltaic performance of the diodes is very sensitive to the oxidation time. For the "10 minute" diode, the fill factor is very poor ($\sim$ 0.2). However very good fill factors were observed (around 0.72) for the diodes ultilizing 5,2,0 minutes oxidation times. The efficiencies of the latter cells was around 5% under 100 mW/cm^2 illumination with a short circuit current density around 17 mA/cm^2 (see Table 5). The rather low values of short circuit current are likely due to the fact that the Al thickness was not optimal and no AR coating was used. One may also observe that the difference in light characteristics for the "5,2,0 minutes" devices did not vary very much. This can be explained in terms of the following. Tunneling for these devices can occur at such a rate that the resistance via this process is insignificant. Thus all the available current from the semiconductor for extraction is obtained and changes can only occur with change in illumination.

4.3 Stability of I-V Characteristics

The completed solar cells were stored in a nitrogen gas environment for 12 days and the I-V characteristics were determined at various intervals. After this time the nitrogen gas supply was allowed to become exhausted but the samples were maintained in the covered enclosure. A further measurement was taken 79 days after processing of the solar cells. Results are shown in Figs. 21-28.

P 33 (3) a DARK FORWARD I-V (2 min. O_2)

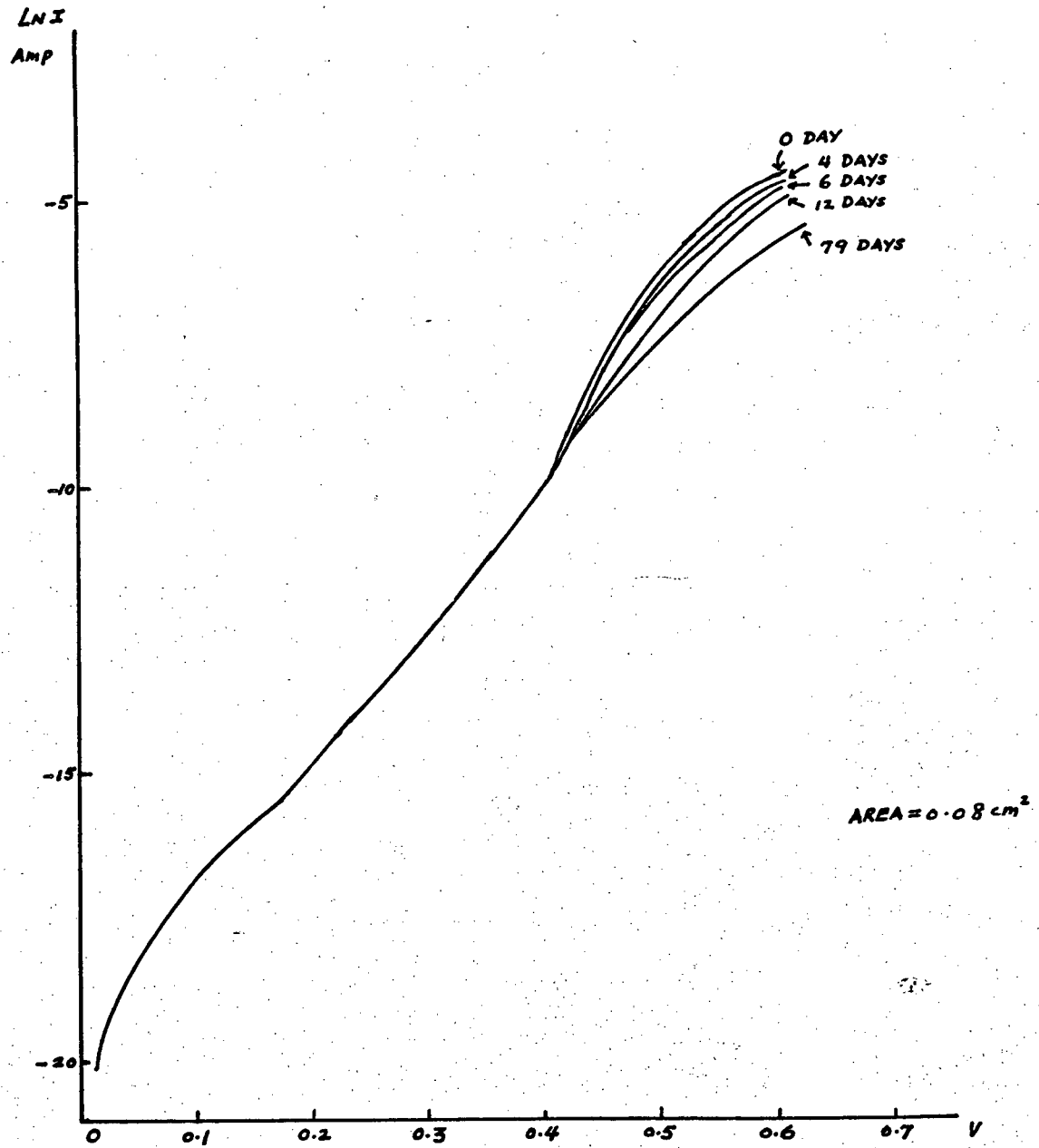
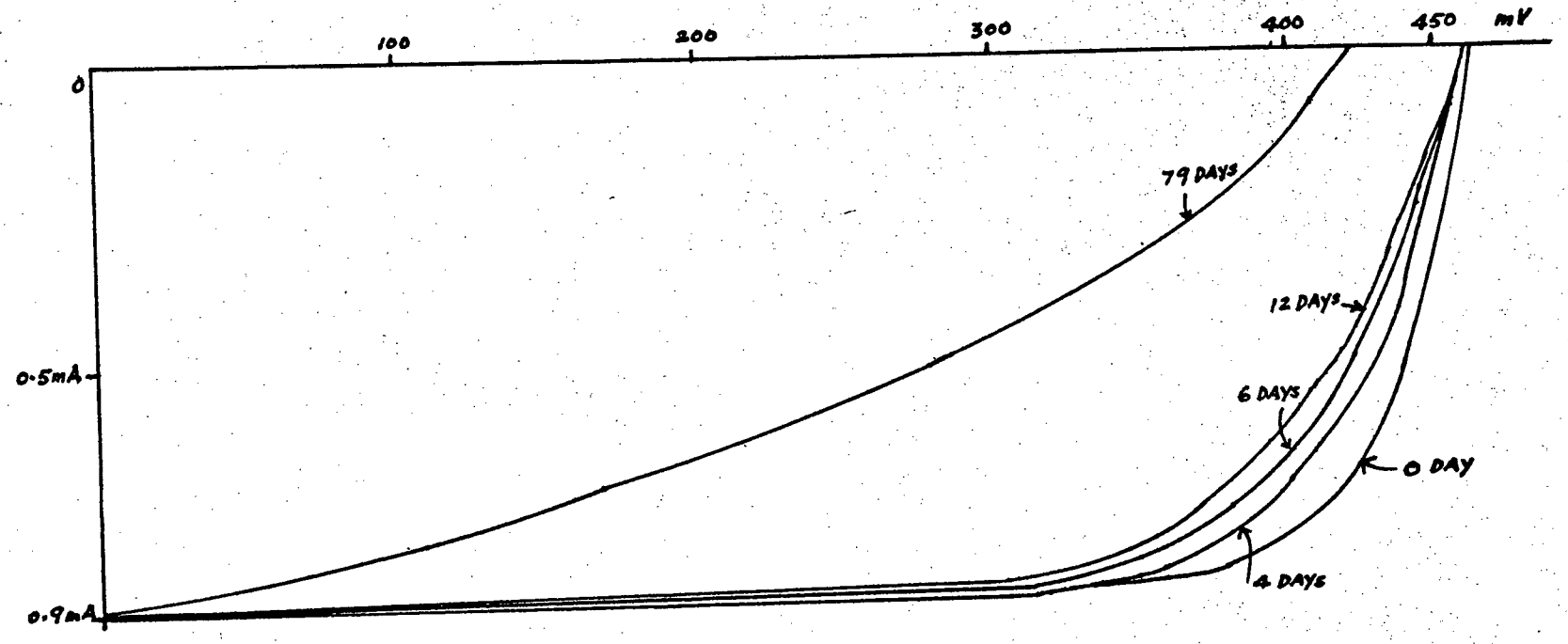


Fig.21. Experimental Stability Data (1)



P 33 (3) a LIGHT I-V (2 min O_2)

AREA = 0·06 cm^2

Fig.22. Experimental Stability Data (2)

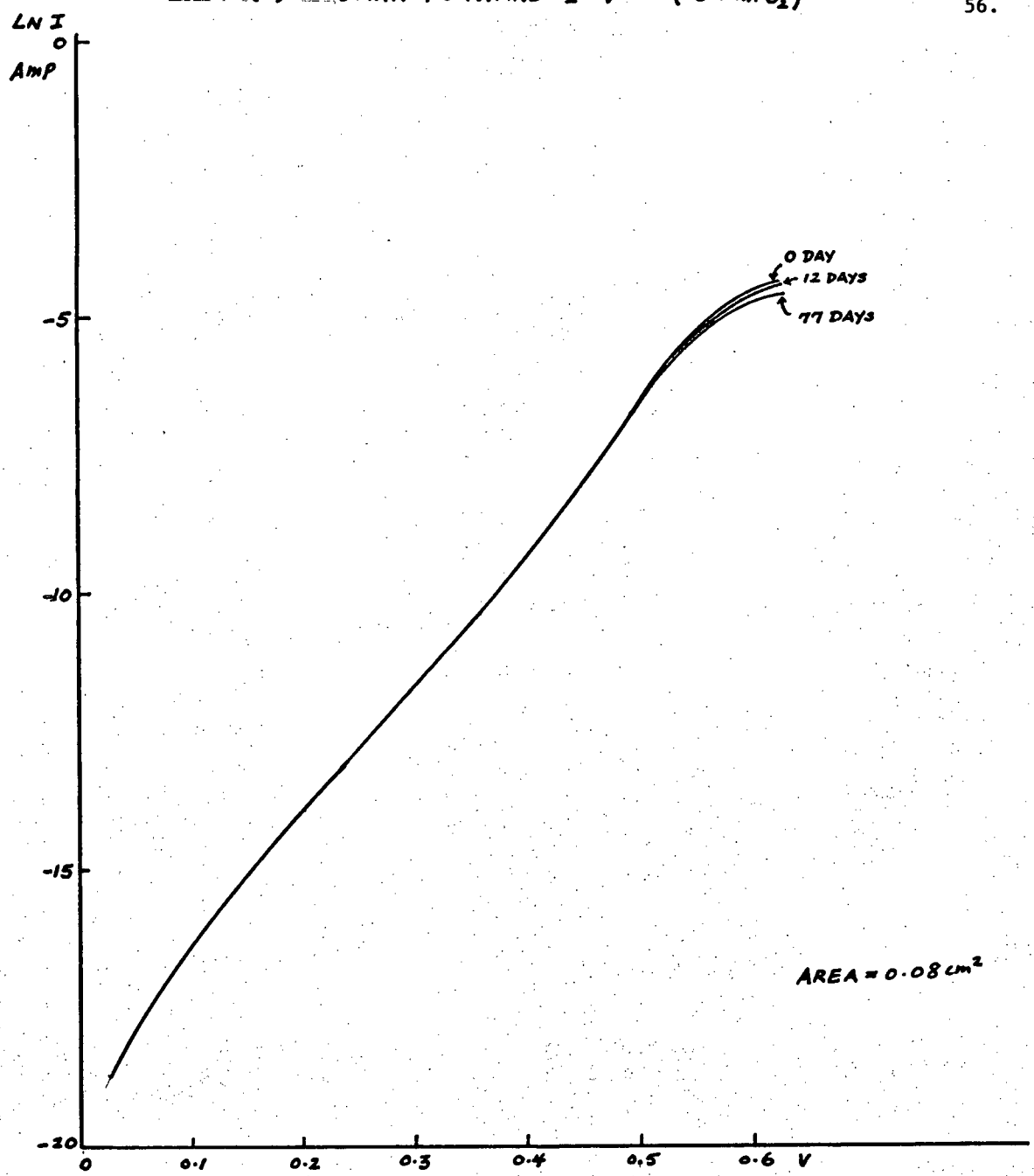


Fig.23. Experimental Stability Data (3)

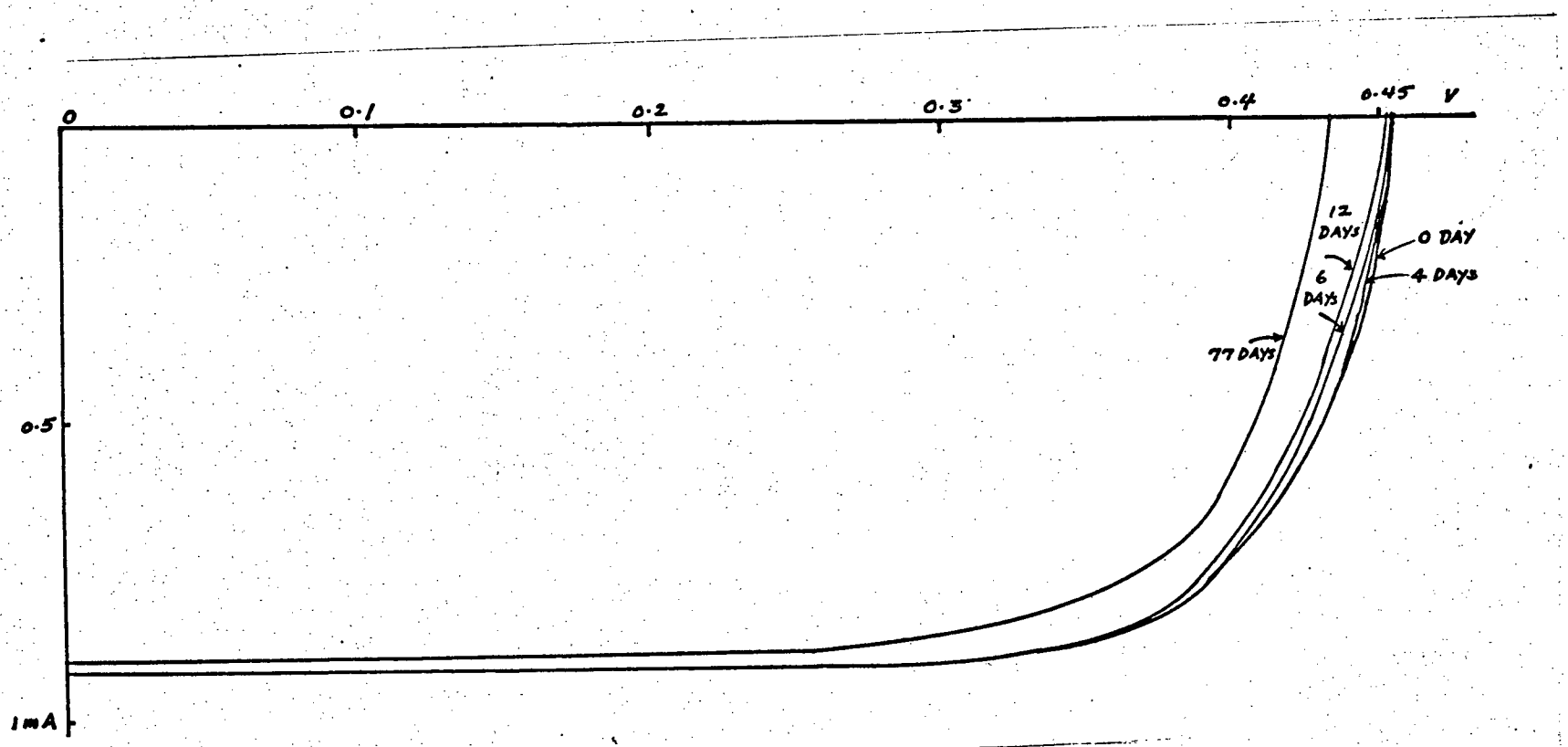


Fig.24. Experimental Stability Data (4)

P 33 (1) a DARK FORWARD I-V (5 min. O_2)

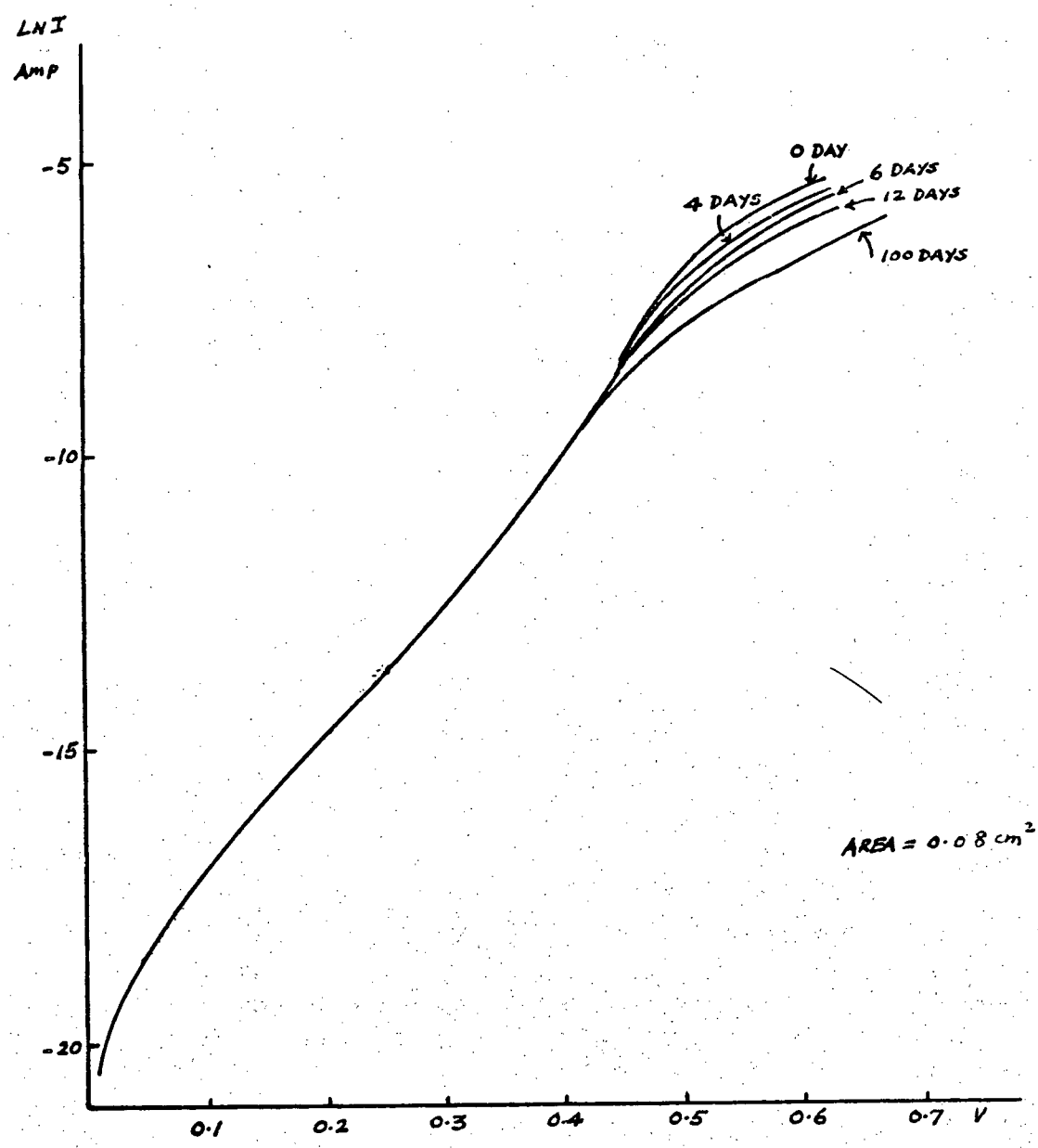


Fig.25. Experimental Stability Data (5)

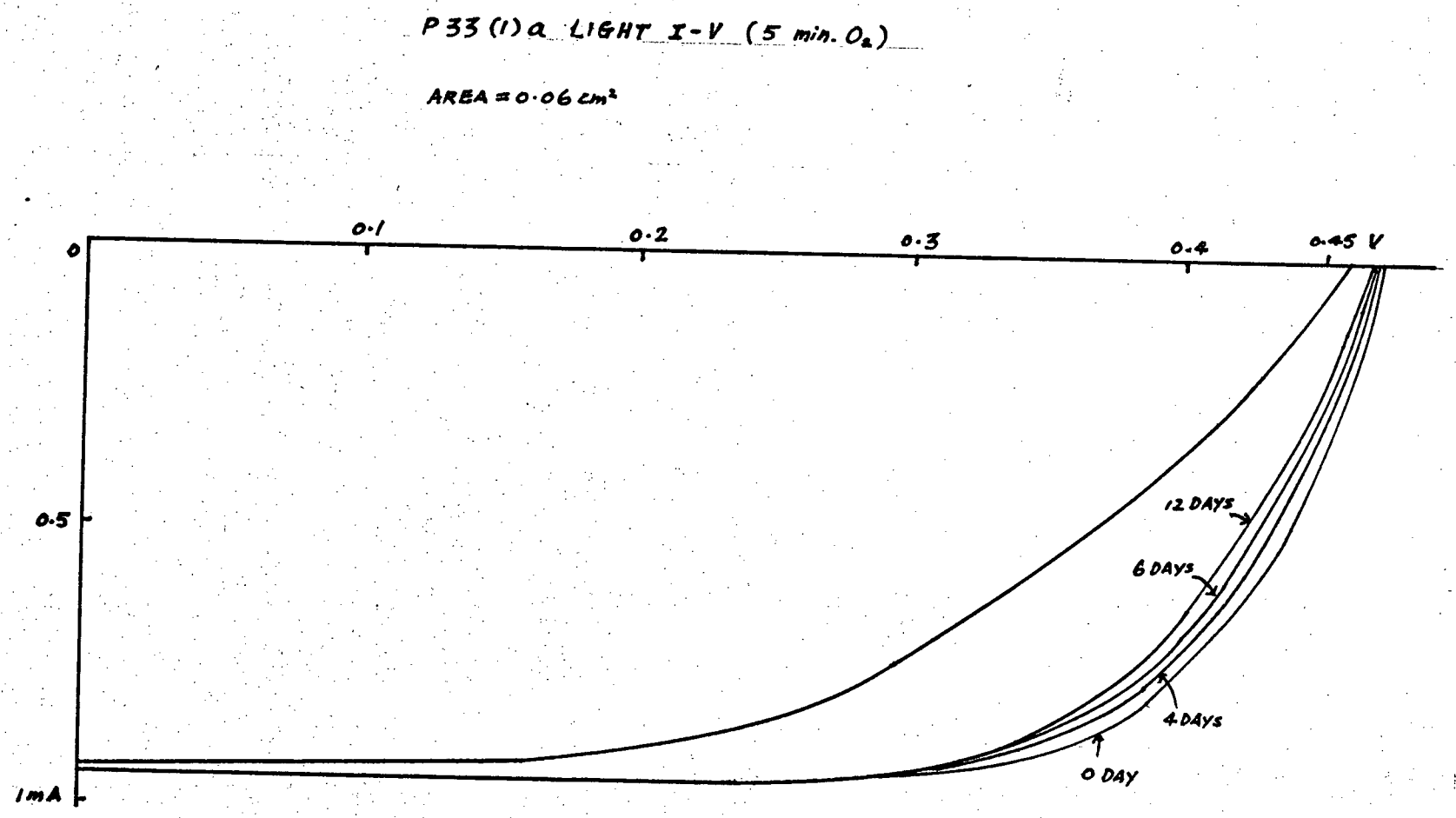


Fig.26. Experimental Stability Data (6)

P33(2)b DARK FORWARD I-V (10 min. O_2)

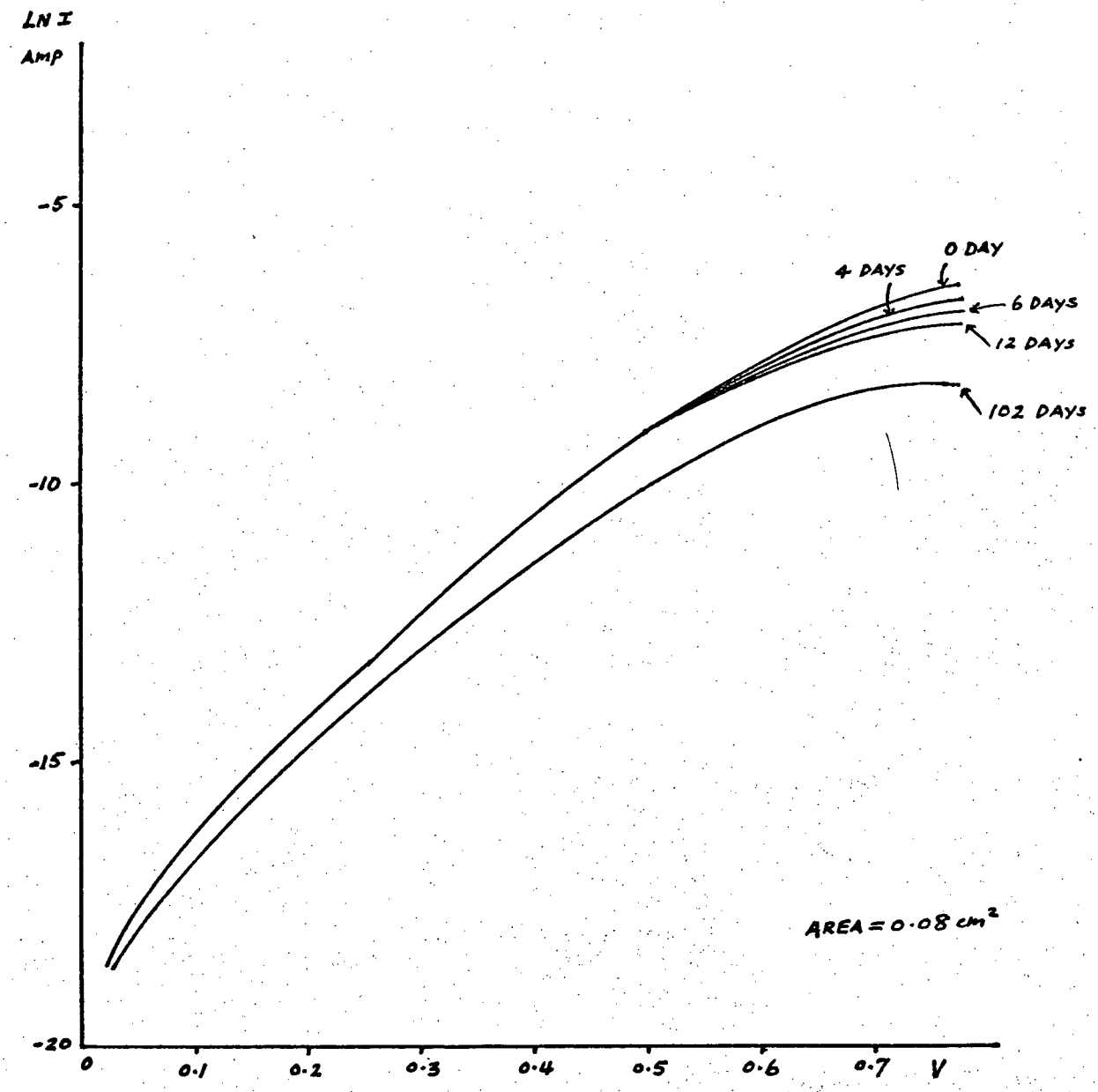


Fig.27. Experimental Stability Data (7)

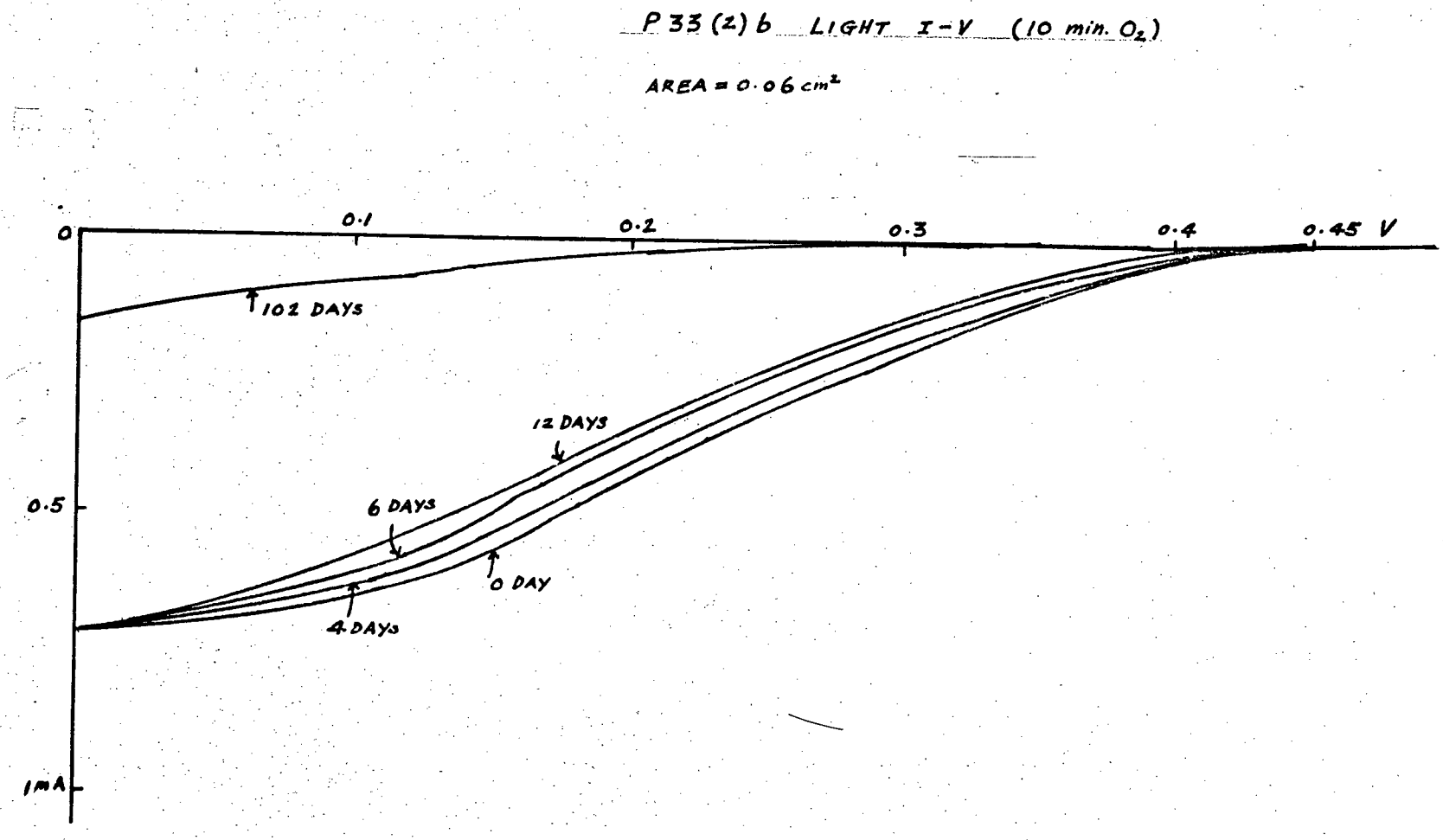


Fig.28. Experimental Stability Data (8)

CHAPTER 5

DISCUSSION

5.1 Comparison of Theoretical and Practical Dark I-V Characteristics

As described in section 2.3.2 four profiles of surface state density were generated based on the curve given in ref. [7]. These profiles were shown in Fig. 10 and the resulting ln I-V curves in Fig.11. For the purpose of comparing theoretical and experimental data, the results from the best (most efficient) solar cell were taken, namely those of diode P33(1) for which the interfacial oxide formation time was 5 minutes. The theoretical and practical data are brought together in Fig.29. It can be seen that the curve corresponding to profile 3 (modified) fits the experimental curve very well over the bias range of 50 mV - 550 mV. No attempt was made to generate a theoretical curve beyond 550 mV because after 550 mV series resistance and tunnel limiting effects will be dominant. The features of these theoretical curves are (1) the effective fermi level for surface state occupation was the majority carrier fermi level; (2) the surface state density was around $10^{13} eV^{-1} cm^{-2}$ near the centre of the band gap; (3) the oxide thickness was assumed to be 20Å; (4) the barrier height was 0.82eV. The reasons for choosing these values are discussed below:-

(1) Actually the choice of the effective Fermi level between that of the metal and the semiconductor was dependent on the properties of the interfacial layer [14]. If the communication between interface states and metal is extremely efficient, then the effective fermi level would follow that of the metal. However, on the other hand if tunneling were extremely difficult, the effective fermi level would tend to follow the semiconductor

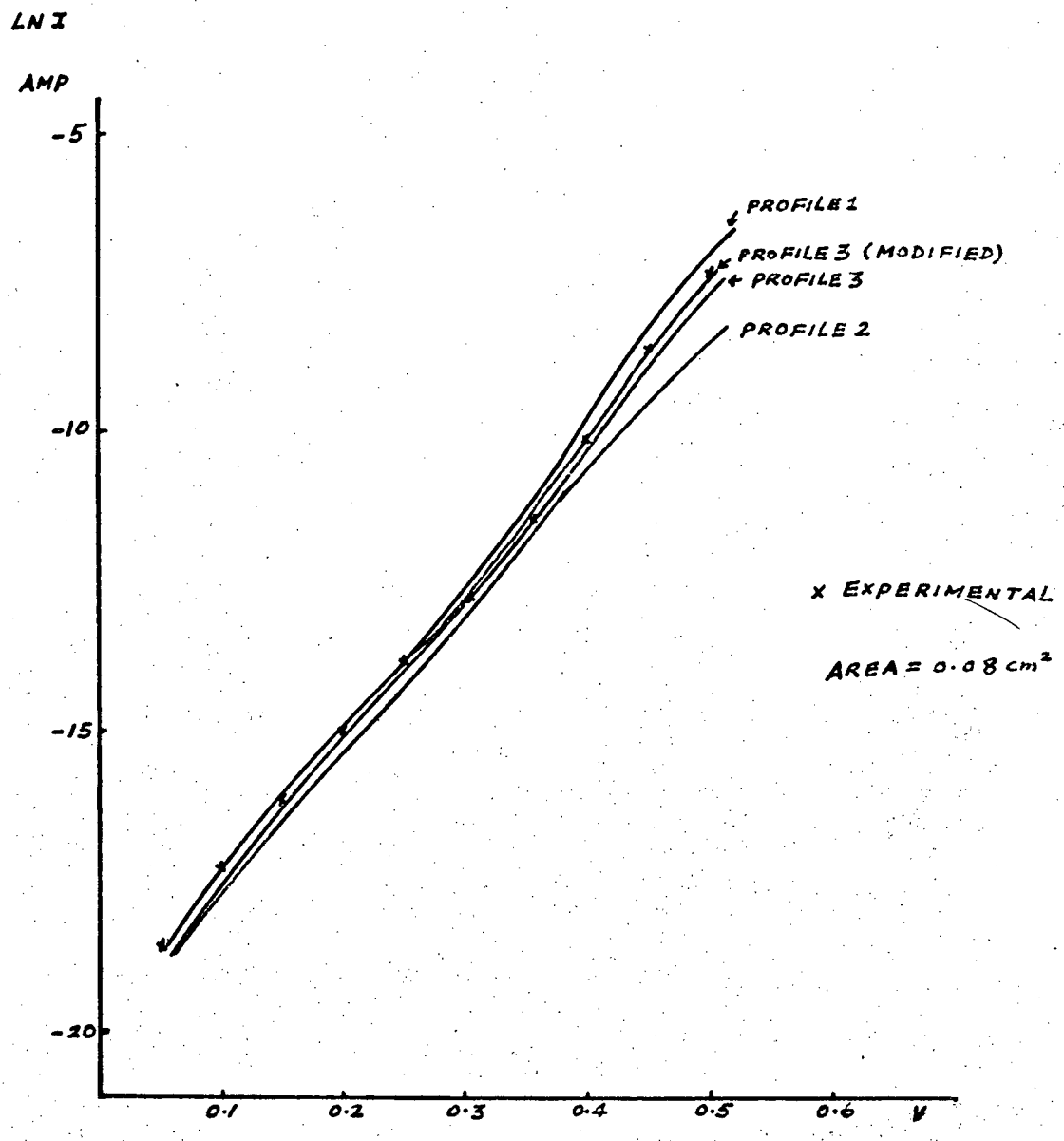


Fig.29. Comparison of Theoretical and Experimental Dark I-V Data

Fermi level. In the experimental work which has been done to support the thesis, (see sensitivity curve (4) Fig.6 and experimental dark forward I-V curve, Fig. 18), there is evidence that the communication between interfacial states and metal is not so efficient as that between the semiconductor and the interfacial states. This is because the slope of the set of curves (corresponding to x = 1, see Fig.6), is far from the experimental one. Although the insulator layer is extremely thin (assumed to be 20Å), better communication exists between the interface states and the semiconductor. It was therefore concluded that the effective fermi level has to be nearer to the semiconductor fermi level than to the metal fermi level.

(2) The surface state density of $10^{13} ev^{-1} cm^{-2}$ is quite a reasonable one and follows from ref.[3] and ref.[7].

(3) The reason for choosing an oxide thickness of 20Å stems from the theoretical results of ref.[6], (see figure 2). i.e. the magnitude of the current obtained in the present work agrees well with the theoretical curves for 20Å diodes. Obviously the choosing of the above figure is not unique. Further experimental work has to be done before all the parameters concerned can be unequivocally determined.

(4) The barrier height could be easily found by extrapolating the dark I-V curve back to the ln I axis (see Fig.18). However 0.82 eV also agrees with a previous suggestion [8] which states that the barrier height is approximately twice the open circuit voltage at 100 mm/cm^2 i.e. in the present case ϕ_B = 2 x 0·4V (see Fig.20).

The excellent fit obtained between the experimental data and the results from the modified thermionic emission theory indicates that the present Al/SiO_x/pSi diodes can be described as majority carrier diodes.

The importance of surface states in affecting the I-V characteristics is thus brought out in the present work. However, it should be noted that by suitably passivating these states and obtaining significant inversion of the semiconductor near the oxide/insulator interface the majority carrier current could be suppressed so that the minority carrier current would dominate [2].

5.2 Surface States Present in MIS Cell

Surface states can be broadly classified as being either acceptor-like (neutral or negatively charged) or donor-like (neutral or positively charged). For acceptor-like interface states there is a layer (if $F_{Fss} > \phi_o$) of negative charge at the insulator-semiconductor interface. This negative charge exerts a shielding effect which blocks the electric field from the positive charge on the metal, thus lowering the surface potential of the semiconductor. This means that a lowering of the barrier height may occur. Due to this fact, the dark current is correspondingly increased. As the dark current is opposed to the light current, the open circuit voltage is reduced. Therefore the efficiency is reduced. This means that acceptor-like interface states have an adverse effect on the light performance of the p-type MIS solar cell [10]. The reverse applies for donor-like surface states.

The light bias characteristics are shown in Fig.20. One may observe that the open circuit voltage of the solar cell prepared with no deliberate oxidation step is smaller than that resulting from the diodes fabricated with an oxidation step of 2-5 min. Also there is an optimal value of the thickness of the oxide which seems to correspond to the thickness of 2 minutes oxidation time. This is in good agreement with

Viktorovitch etal's result [11], which concludes that there is an optimal thickness of interfacial layer as regards the photovoltaic properties of open circuit voltage and fill factor. Furthermore two very interesting features of these curves are observed for the solar cell with 10 minutes oxidation time:- (1) there is an inflexion point about the current axis of the curve. (2) the reverse bias current increases for a certain extent in the 3rd quadrant before it becomes saturated, i.e. photocurrent suppression occurs on account of the oxide being too thick.

5.3 Stability of the MIS Cells

The degradation in performance observed in some of the MIS cells fabricated in this work (Figs. 22-29) should not be interpreted as indicative of a basic instability in these cells. It is emphasized that these cells were not encapsulated in any fashion, and were not even covered by an anti-reflection coating. [A suitable AR coating and encapsulant would have to be developed that were compatible with the thin film nature of the barrier metal and interfacial layer]. The experimental data do, however, serve to indicate that to be useful any encapsulant used must satisfactorily exclude air from reaching the active junction of the device. It appears that degradation in the characteristics such as reduced current at high forward voltage, decreased fill factor under illumination, (practically no changes at low bias)is caused by an increase in series resistance. This could arise either from oxidation of the Al or migration of oxygen through the Al to the SiO_x leading to an increase in the thickness of the latter.

CHAPTER 6

CONCLUSION

An alternative explanation of the mode of conduction in so-called minority carrier MIS diodes has been proposed. In the proposed model the dark current characteristics are explained by the classical thermionic emission theory modified to include a suitable profile of surface states at the insulator/semiconductor interface. The new proposal is based on the solution of Poisson's equation under appropriate conditions of semiconductor space charge and non-uniform surface state charge. The effective fermi level at the I/S interface is assumed to lie at a level intermediate between the metal Fermi level and the majority carrier Fermi level. The theoretical dark current-voltage characteristics are in excellent agreement with experimental data.

Four sets of MIS solar cells have been fabricated and the critical influence of the oxide thickness on the performance of these cells has been observed. The best performance was achieved with an insulator formation step which utilized a 2 minute oxidation time.

Some preliminary data on the stability of MIS cells has been obtained and the need for encapsulating the basic $Al/SiO_x/Si$ structure has been established.

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APPENDIX 1

Program for solving non-linear equation (48) in p 27 using UBC files Zero 1 and QINT4P

```
MICHIGAN TERMINAL SYSTEM FORTRAN G(41136)          MAIN          05-11-78    17:12:41

0001                  IMPLICIT REAL*8(A-H,O-Z)                                  1.000
0002                  DIMENSION V(20),IX(150),IY(150)                           2.000
0003                  COMMON V,FIB,DELTA,ALPHA,IX,IY,J                          3.000
0004                  EXTERNAL FN                                               4.000
0005                  LOGICAL LZ                                                5.000
0006                  READ102,XC,YC                                             6.000
0007              102 FORMAT(F4.1,1X,F5.1)                                      7.000
0008                  V(1)=0.0500                                               8.000
0009                  V(2)=0.100                                                9.000
0010                  V(3)=0.1500                                              10.000
0011                  V(4)=0.200                                               11.000
0012                  V(5)=0.2500                                              12.000
0013                  V(6)=0.300                                               13.000
0014                  V(7)=0.3500                                              14.000
0015                  V(8)=0.400                                               15.000
0016                  V(9)=0.4500                                              16.000
0017                  V(10)=0.500                                              17.000
0018                  READ103,DELTA,FIB,ALPHA                                  18.000
0019              103 FORMAT(D9.1,1X,F4.1,1X,F5.2)                             19.000
0020                  DO 50 I=1,30                                             20.000
0021               50 READ101,(IX((I-1)*5+JJ),IY((I-1)*5+JJ),JJ=1,5)           21.000
0022              101 FORMAT(5X,5(I6,I6,1X))                                   22.000
0023                  DO 96 J=1,10                                             23.000
0024                  E1=5.D0-7                                                24.000
0025                  XL=XC                                                    25.000
0026                  YU=YC                                                    26.000
0027                  CALL ZERO1(XL,YU,FN,E1,LZ)                               27.000
0028                  IF(.NOT. LZ) GO TO 30                                    28.000
0029                  PRINT20,V(J),XL                                          29.000
0030              20  FORMAT(' ',F6.2,2X,F8.3)                                 30.000
0031              96  CONTINUE                                                 31.000
0032                  STOP                                                     32.000
0033              30  PRINT40,V(J)                                             33.000
0034              40  FORMAT(' ',F6.2,2X,'ZERO1 FAILS')                        34.000
0035                  STOP                                                     35.000
0036                  END                                                      36.000
 *OPTIONS IN EFFECT*   ID,EBCDIC,SOURCE,NOLIST,NODECK,LOAD,NOMAP
 *OPTIONS IN EFFECT*   NAME = MAIN      , LINECNT =     60
 *STATISTICS*     SOURCE STATEMENTS =     36,PROGRAM SIZE =    1042
 *STATISTICS*   NO DIAGNOSTICS GENERATED
NO ERRORS IN MAIN
```

```
MICHIGAN TERMINAL SYSTEM FORTRAN G(41436)          FN          05-11-76      17:12:41

0001                FUNCTION FN(XL)                                          37.000
0002                IMPLICIT REAL*8(A-H,O-Z)                                 38.000
0003                DIMENSION V(20),IX(150),IY(150),XX(150),YY(150),YIM(150)  39.000
0004                COMMON V,FIR,DELTA,ALPHA,IX,IY,J                         40.000
0005                REAL*8 XX,YY,XFIR,XLIT,XLITL,AREA1,AREA2,AREA3,AREA31,YIM 41.000
0006                IA=1                                                     42.000
                C CONVERT IX,IY INTO XX,YY TO FIT ACTUAL SCALE               43.000
                C TRUNCATE TO GET IPS FOR TWO INTEGRAL                       44.000
                C CALL GINT4P TWO TIMES PASS XL TO UPPER LIMIT OF INTEGRAL   45.000
                C WRITE DOWN FUNCTION                                        46.000
0007                DO 21 K=1,150                                            47.000
0008                XX(K)=IX(K)/10000.0                                      48.000
0009                YIM(K)=IY(K)/1000.0                                      49.000
0010             21 YY(K)=10.0**YIM(K)                                       50.000
0011                XFIR=FIR*100.0                                           51.000
0012                IR1=INT(XFIR)+1                                          52.000
                C PASS XL TO UPPER LIMIT OF INTEGRAL                         53.000
0013                XLIT=(FIR+V(J)*ALPHA-V(J)/XL)*100.0                      54.000
0014                IR2=INT(XLIT)+1                                          55.000
0015                IR3=IR2+1                                                56.000
0016                XLITL=FLOAT(IR2-1)                                       57.000
0017                AREA1=GINT4P(XX,YY,150,IA,IR1)                           58.000
0018                AREA2=GINT4P(XX,YY,150,IA,IR2)                           59.000
0019                AREA3=GINT4P(XX,YY,150,IR2,IR3)                          60.000
0020                AREA31=(XLIT-XLITL)*AREA3                                61.000
                C HAVE TO MULTIPLIED BY 0                                    62.000
                C WRITE DOWN FUNCTION                                        63.000
0021                VRT=FIR-0.23                                             64.000
                C LO= 1.50-5                                                 65.000
                C CONSTANT LEAD 3.6D-9                                       66.000
0022                O=1.6020-19                                              67.000
0023                AREA11=O*AREA1                                           68.000
0024                AREA22=O*AREA2                                           69.000
0025                AREA33=O*AREA31                                          70.000
0026                TERM1=DEXP(-38.61D0*VRT)+38.61D0*VRT-1.D0+1.1380-10*(DEXP(38.61D0*  71.000
                   1VRT)-38.61D0*VRT-1.D0)                                   72.000
0027                TERM2=DEXP(-38.61D0*(VRT-V(J)/XL))+38.61D0*(VRT-V(J)/XL)-1.D0+1.13  73.000
                   280-10*(DEXP(38.61D0*(VRT-V(J)/XL))-38.61D0*(VRT-V(J)/XL)-1.D0)  74.000
002A                FN=(DELTA/3.4D-13)*(AREA11-AREA22-AREA33+3.6D-9*DSQRT(TERM1)-3.6D-  75.000
                   39*DSQRT(TERM2))-(XL-1.D0)*V(J)/XL                        76.000
0029                RETURN                                                   77.000
0030                END                                                      78.000
 *OPTIONS IN EFFECT*   ID,EBCDIC,SOURCE,NOLIST,NODECK,LOAD,NOMAP
 *OPTIONS IN EFFECT*   NAME = FN       , LINECNT =      60
 *STATISTICS*     SOURCE STATEMENTS =       30,PROGRAM SIZE =     3296
 *STATISTICS*   NO DIAGNOSTICS GENERATED
NO ERRORS IN FN

NO STATEMENTS FLAGGED IN THE ABOVE COMPILATIONS.


NAME      NUMBER OF ERRORS/WARNINGS  SEVERITY

MAIN                 0                  0
FN                   0                  0
EXECUTION TERMINATED   17:12:42  T=.33  RC=0      $.31
```