A GaAs CERMET GATE CHARGE-COUPLED DEVICE

By

MAURICE LeNOBLE

B.A.Sc., University of British Columbia, 1984

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF
THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

in

THE FACULTY OF GRADUATE STUDIES

Department of Electrical Engineering

We accept this thesis as conforming
to the required standard

THE UNIVERSITY OF BRITISH COLUMBIA

April 1989

In presenting this thesis in partial fulfilment of the requirements for an advanced degree at the University of British Columbia, I agree that the Library shall make it freely available for reference and study. I further agree that permission for extensive copying of this thesis for scholarly purposes may be granted by the head of my department or by his or her representatives. It is understood that copying or publication of this thesis for financial gain shall not be allowed without my written permission.

Department of Elec. Engr.

The University of British Columbia
1956 Main Mall
Vancouver, Canada
V6T 1Y3

Date 1 July 1989

Abstract

The design, implementation and evaluation of a 64-pixel, 4-phase GaAs cermet gate charge-coupled device (CMCCD) are described. It is demonstrated that the signal charge confinement and the signal charge capacity of the CMCCD are maximized when thin, highly doped active layers are used for implementing the device. The cermet/GaAs junction within an interelectrode gap of the CMCCD forms a barrier similar to a metal/GaAs Schottky barrier, as revealed by an investigation of the dc current-voltage characteristic of a cermet/GaAs Schottky barrier diode. A transmission line model is described for the cermet/GaAs junction within an interelectrode gap of the CMCCD and is used to demonstrate the relationship of the surface potential variation along the gap as a function of the clock frequency and the material parameters. It is shown that the surface potential variation is monotonic for all frequencies, which is desirable for minimizing the formation of energy troughs within the active layer. Energy troughs trap and release charge from passing charge packets, causing unwanted signal dispersion. A two-dimensional computer model is used to determine a theoretical maximum frequency of operation of the CMCCD. It is shown that a short transport electrode length for a fixed transport electrode pitch is preferable as it results in the maximum high frequency performance of the CMCCD for the lowest clock power. A computer simulation of a single electrode transfer of a charge packet is demonstrated using the two-dimensional computer model. The computer simulation indicates that efficient charge transfer takes place, suggesting that the CMCCD will have good performance. A GaAs CMCCD with an on-chip GaAs MESFET source follower amplifier has been produced using a six mask level fabrication procedure. The CMCCD and the output source follower amplifier are demonstrated to operate at 100 MHz. Charge transfer efficiencies of 1.00 and 0.998 for 100 MHz operation are obtained for the CMCCD using the impulse response method and the insertion loss method.

Table of Contents

List of Symbols

$a(y,\omega)$	real part of $(L_g - y)\gamma(\omega)$
$A, \ldots, G$	constants
A_{dB}	logarithmic amplitude
A_0	amplitude constant
A^*	modified Richardson's constant
$b(y,\omega)$	imaginary part of $(L_g - y)\gamma(\omega)$
$c(\omega)$	real part of $L_g\gamma(\omega)$
c_1	integration constant
C_m	maximum potential contour
C_{CM}	distributed cermet film capacitance
C_D	distributed depletion layer capacitance
$C_{O/P}$	parasitic output capacitance
$\bar{C}_{CM}$	lumped cermet film capacitance
$\bar{C}_D$	lumped depletion layer capacitance
$d(\omega)$	imaginary part of $L_g\gamma(\omega)$
$d\vec{r}$	differential contour vector
E	normalized electric field
E_C	critical electric field
E_I	intrinsic energy
E_0	empirical constant
f_c	clock frequency
f^l_{k+1}	finite difference equation
f_{max}	maximum clock frequency
g, h	functions comprising the finite difference equation
$H(y,\omega)$	normalized surface potential amplitude

i, j	x, y grid point indices
i_{aux}, j_{aux}	x, y auxiliary grid point indices
i_{int}	active layer depth grid point index
i_{max}	wafer thickness grid point index
$I(y)$	dc tangential current
I_0	saturation current
j_{max}	pixel length grid point index
J	electron current density
J_0	saturation electron current density
k	time-step index
k_{max}	stop time index
k_1, k_2	integration constants
l	iteration index
L_g	interelectrode gap length
L_p	transport electrode pitch
m	integer index
n_i	intrinsic carrier density
N_{peak}	number of pixel transfers between the peak of the observed impulse response and the peak of the ideal impulse response
N_C	effective density of states in the conduction band
N_D	uniform donor density
N_T	number of single electrode transfers
$\bar{n}$	normalized electron density
$\bar{n}_{gap}$	normalized cermet/GaAs junction electron density
$\bar{n}_0$	normalized metal/GaAs junction electron density
$\bar{N}_D$	normalized uniform donor density

p	number of pixels
q	electron charge
$Q_{int,j}$	interface charge density
Q_s	signal charge density
$Q_{s,max}$	maximum signal charge density
$Q_{Ph.1+Ph.2}$	phase 1 and phase 2 signal charge density
$Q_{Ph.2+Ph.3}$	phase 2 and phase 3 signal charge density
r	geometric series constant
R_{CM}	distributed cermet film resistance
R_L	load resistance
R_S	series resistance
$\bar{R}_{CM}$	lumped cermet film resistance
S	derivative of the tangential current $I(y)$
t	time
t_{del}	delay time
t_{tr}	clock transition period
T	temperature
u	normalized potential
u_{gap}	normalized cermet/GaAs junction potential
u_0	normalized metal/GaAs junction potential
U_T	thermal voltage
v	normalized electron quasi-Fermi potential
$V(y)$	dc surface potential
$V(y,\omega)$	ac surface potential
V_g	applied gate voltage
V_{gap}	potential difference across the gap
V_{in}, I_{in}	diode terminal voltage and current

V_p	pinch-off voltage
V_0	incident voltage
w	cermet gate width
w_n	space charge region depth
w_r	relaxation parameter
x, y	spatial coordinates
x_i, y_j	spatial position at the i, j^{th} grid point
x_{int}	active layer depth
x_m	x-coordinate of the maximum potential
x_{max}	wafer thickness
$\hat{x}, \hat{y}$	x, y unit vectors
$^{x}_{,}{}^{y}$	x-component or y-component
y_{max}	pixel length
y_{mL}, y_{mR}	transport electrode endpoints
Y	distributed shunt admittance
z	complex variable
Z	distributed series impedance
β	diode ideality factor
δj_{gap}	relative position along the gap
$\delta u_{i_{max}}$	normalized potential difference between the Fermi level and the intrinsic energy level at $x = x_{max}$
δt	time increment
δx	grid spacing in the x-direction
δx_a	uniform active layer subdomain grid spacing
$\delta x_i, \delta y$	grid spacings at the i, j^{th} grid point
$\delta \psi_{max}$	charge confinement
$\delta \zeta^l_{k+1}$	correction factor

ϵ	dielectric constant of GaAs
η	charge transfer efficiency
$\gamma(\omega)$	propagation constant
μ	electron drift mobility
μ_0	low-field electron drift mobility
ν	electron drift velocity
ω	radian frequency
ψ	electrostatic potential
ψ_{max}	maximum potential
ψ_{min}	minimum value of the maximum potential
ϕ_{BC}	cermet/GaAs Schottky barrier height
ϕ_{BM}	metal/GaAs Schottky barrier height
ψ_0	metal/GaAs junction potential
ϕ_n	electron quasi-Fermi potential
σ	length constant
τ	electron transit time
$\Theta(y,\omega)$	surface potential phase shift
υ	electron drift velocity function
φ	fractional constant
ξ	binary variable
ζ	finite difference variable
$\zeta^{l+1}_{i,j,k+1}$	ordinary iterated solution for $\zeta_{i,j,k+1}$
${}^{r}\zeta^{l+1}_{i,j,k+1}$	relaxed solution for $\zeta_{i,j,k+1}$

List of Tables

List of Figures

Acknowledgements

I would like to express my thanks to my thesis supervisor, Professor Lawrence Young, for his assistance and guidance throughout this work. I would also like to thank Professor David L. Pulfrey, Professor Richard R. Johnson and Mr. John V. Cresswell for co-supervising this project.

My deepest thanks go out to Mr. John V. Cresswell, who is a Senior Research Engineer at TRIUMF, for introducing me to the broad subject of GaAs CCDs. Mr. Cresswell and I have spent many long hours exploring the nuances of these devices. He has my heartfelt thanks for his invaluable assistance throughout this project.

A special note of thanks to Dr. R. Sahai of Rockwell International Corporation for the discussions that we had on the various points of interest that we share on the subject of GaAs CCDs. The knowledge gained from these discussions proved to be quite beneficial.

There are a number of people that I am indebted to for their help dealing with the many technical aspects concerning this project: Raymond Bula, Miles Constable, Hiroshi Kato, Yvonne Langley, Peter LeNoble, Michael LeRoss, Tony Leugner, Naomi Shibaoka, Peter Townsley and David Webster. I would also like to thank my colleagues in the Solid State Group within the Department of Electrical Engineering at UBC for the assistance they have given me.

Finally, to my beautiful wife, Eveline, for having the patience to endure—I express my love and appreciation.

Chapter 1

Introduction

The original proposal of a GaAs charge-coupled device was made in 1972 by Schuermeyer et al [1]. The transport electrodes of the proposed CCD structure consisted of metal/semiconductor Schottky barriers instead of the MOS structures commonly used with silicon CCDs. The Schottky barrier CCD has the advantage that it can be fabricated on GaAs using well developed GaAs MESFET fabrication techniques. This is important, as will be described later, for the monolithic integration of GaAs CCDs with auxiliary GaAs MESFET support circuits.

A 3-phase GaAs capacitive gate CCD (CGCCD) employing metal/GaAs Schottky barriers separated by narrow (approximately 1 micron long) dielectric filled interelectrode gaps was demonstrated in 1977 by Kellner et al [2], and shortly thereafter in 1978 by Deyhimy et al [3]. One, two and four-phase GaAs CGCCDs have been produced and operated since the initial demonstrations of the 3-phase GaAs CGCCD [4,5,6]. GaAs CCDs have wider operating bandwidths than silicon CCDs as a result of the approximately five times greater electron mobility within GaAs at low to moderate electric fields. A limitation for the high frequency operation of a silicon CCD is attributed to the lower bandwidths and greater power requirements of the support circuits integrated with the device [1,7]. The highest clock frequency that a silicon CCD has been operated at, that this author is aware of, is 180 MHz which was reported by Esser and Sangster [8]. In comparison, a GaAs CMCCD was operated at 4.2 GHz as demonstrated by Sovero et al [9]. The best reported charge transfer efficiencies (CTEs) attained by GaAs CCDs approach 0.9999 for CCD clock frequencies lying between 1.0 MHz and 1.0 GHz [10,9]. This level of performance has made the GaAs CCD desirable for signal processing applications that extend into the UHF band

(0.30 GHz–1.12 GHz) [11,12,13,14,15,16,17].

A limitation that is encountered with using GaAs CGCCDs in UHF signal processing applications arises from the difficulty of monolithically integrating GaAs CGCCDs with GaAs MESFETs. This difficulty is a consequence of the different active layer requirements of the two devices. A GaAs CGCCD is typically fabricated on a 1–2 micron deep n-type epitaxial layer grown on a n^--buffer on a semi-insulating GaAs substrate. The donor density for the n-type epitaxial layer is chosen to lie within the range from 10^{15} cm^{-3} to 10^{16} cm^{-3} to maintain a reasonable pinch-off voltage suitable for the high frequency operation of the CGCCD. The active layer parameters described above for the GaAs CGCCD are not optimal for a typical GaAs MESFET which requires a thinner, more highly doped active layer. It is impractical to grow segregated regions of doped GaAs for CGCCDs and MESFETs using epitaxy, as the present epitaxial growth methods are not well suited to this task [18]. Ion-implantation would yield selectively doped regions of GaAs, but possesses some difficulty providing the deep active layers required for the fabrication of a GaAs CGCCD [19].

The performance of a GaAs CGCCD in a signal processing application is further limited by the charge transfer loss that arises from the formation of energy troughs within the active layer bounded on the GaAs surface by the interelectrode gaps [7,20]. An energy trough within a gap of a GaAs CGCCD has a minimum electron energy less than that of the regions under the transport electrodes adjacent to the gap. This energy trough will form within a gap of a GaAs CGCCD as a result of a non-monotonic surface potential distribution along the gap [7]. During the charge transfer process, the energy trough captures a quantity of charge from a charge packet as it passes through the region of minimum energy. The captured electrons are transferred to the CGCCD output at a later time or lost through recombination resulting in increased signal dispersion. Deyhimy et al [7] used a two-dimensional electrical analog for the GaAs CGCCD to show that the energy trough within a gap of a GaAs CGCCD was

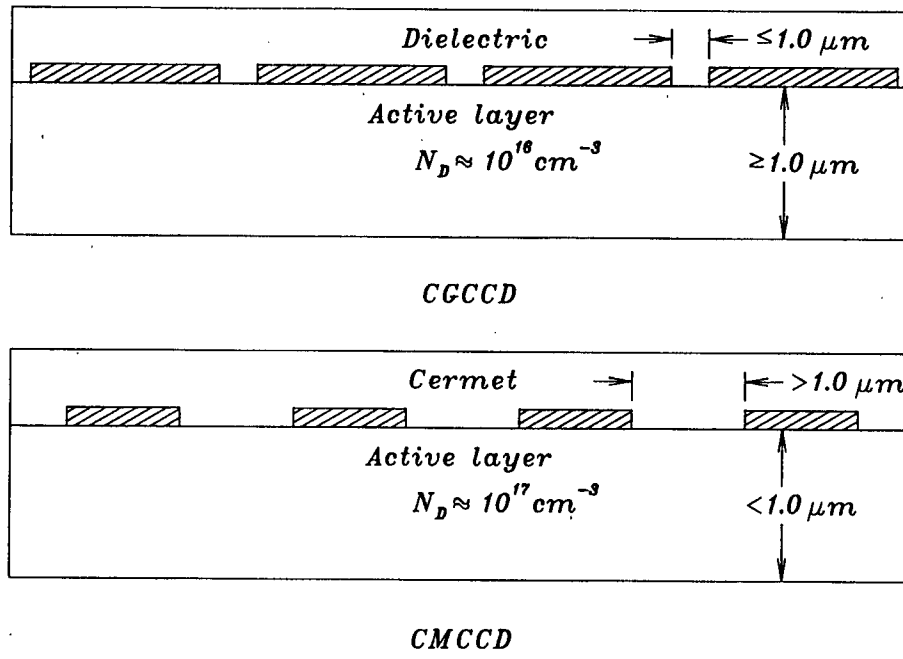

Figure 1.1: The cross-sectional views of a single pixel of a GaAs CGCCD and a GaAs CMCCD illustrating the basic physical differences between the two devices.

considerably reduced when the gap length was decreased. It was demonstrated that a gap length of less than 1 micron would result in the formation of a minimal energy trough in a GaAs CGCCD having a 2 micron deep active layer uniformly doped with a donor density of $1 \cdot 10^{16}$ cm^{-3}.

The GaAs CMCCD demonstrated in 1982 by Higgins et al overcomes the practical limitations of using a GaAs CGCCD in a signal processing application [18]. The cross-sectional views of a single pixel of a GaAs CMCCD and a GaAs CGCCD are shown in Figure 1.1. The CMCCD is fabricated on a GaAs MESFET compatible active layer enabling the CMCCD to be monolithically integrated with MESFET support circuitry. The transport electrodes of a CMCCD are thinner than the transport electrodes of a CGCCD and are separated by a wider interelectrode gap. A thinner transport electrode provides an increased tangential electric field component under the electrode, resulting in improved charge transfer within the CMCCD [18,21]. The wider interelectrode separation of the CMCCD provides a considerable reduction in the dimensional tolerance

required to fabricate the device.

The GaAs surface comprising the interelectrode gaps of a GaAs CMCCD is encapsulated with a cermet film. The cermet/GaAs junction was demonstrated in 1974 by Wronski et al [22] to form a Schottky barrier with a series gate impedance comprised of a parallel resistance and capacitance. During the operation of the CMCCD, a current will flow from a transport electrode through the cermet film to an adjacent transport electrode when a voltage difference exists between the two electrodes. The current through the cermet film establishes a potential distribution along the cermet/GaAs junction that varies monotonically in the direction of flow. Walden et al [23] determined, using two-dimensional computer modeling, that a monotonic surface potential variation across each of the interelectrode gaps of a CCD will prevent the formation of energy troughs within the device. This result suggests that a CMCCD will have reduced charge transfer loss during operation, and consequently will exhibit improved performance.

The performance of the GaAs CMCCD has been demonstrated in two signal processing applications: a high speed GaAs detector array/CMCCD multiplexer [24] and a GaAs VHF/UHF agile bandpass filter [25]. These applications have been developed by a group at the Rockwell International Microelectronics Research and Development Center (Thousand Oaks, California) and are the only demonstrated applications of GaAs CCDs that this author is aware of.

The high speed GaAs detector array/CMCCD multiplexer has been developed for an acousto-optic spectrum analyzer. In this application, an array of thirty-two GaAs photodiodes are multiplexed by a 64-pixel, 4-phase GaAs CMCCD using a side-feed arrangement. The photodiodes and the CMCCD are interconnected by a gating circuit provided by GaAs MESFETs integrated on-chip. The currents generated by each of the photodiodes are integrated onto hold capacitors producing thirty-two discrete charge packets. The charge packets are injected into the CMCCD channel in a parallel manner

using the MESFET gating circuit and are subsequently transferred to the CMCCD output for further processing. Real-time signal processing with this device has been demonstrated using a CMCCD clock frequency of 1.0 GHz.

The GaAs VHF/UHF agile bandpass filter has been developed for frequency selective filtering applications. This device employs GaAs CMCCDs arranged in a pipe-organ structure to provide weighted sampling, programmable delay and summing of analog signals. Supervisory functions are provided by GaAs MESFET circuits integrated monolithically with the CMCCDs. The CMCCD agile bandpass filter has demonstrated in excess of 60 dB of dynamic range for lowpass, bandpass and highpass filter operations using a 1.0 GHz input sampling rate [26]. The two GaAs CMCCD applications described above have demonstrated the ability to monolithically integrate the CMCCD with other circuits to provide sophisticated signal processing functions.

A GaAs CMCCD signal processing system is presently being developed at TRIUMF (Tri-University Meson Facility, Vancouver) to satisfy the instrumentation requirements for a nuclear physics experiment—BNL Experiment 787. A 64-pixel, 4-phase GaAs CMCCD comprises an essential part of a wideband data acquisition system capable of recording 250 MHz bandlimited analog signals. The nuclear physics experiment and the GaAs CMCCD wideband data acquisition system are described in Appendix A.

The purpose of this work is to provide a theoretical and practical development of a 64-pixel, 4-phase GaAs CMCCD. The design, implementation and evaluation of this device are described in the following chapters.

Chapter 2

Theory

2.1 Principle of Operation

A GaAs CMCCD functions as a programmable delay line. The input signal is applied to the input ohmic contact (I/O) and is sampled by the input section at fixed time intervals producing a sequence of discrete charge packets. The charge packets are sequentially injected into the CMCCD transport region where they are transferred to the output ohmic contact (O/P) under the control of the quadrature clocks. At the output section of the CMCCD, the charge packets are converted to an analog signal corresponding to the original input signal delayed by an amount of time

$$t_{del} = \frac{p}{f_c} \tag{2.1}$$

where t_{del} is the delay time assuming ideal operation, p is the number of pixels comprising the CMCCD and f_c is the CMCCD clock frequency. A cross-sectional view of a 4-phase GaAs CMCCD with representative signal levels applied to the device nodes is shown in Figure 2.1.

The signals applied to the nodes of the CMCCD are engaged in a sequential manner during the initial start-up of the device. The bottom surface of the semi-insulating GaAs substrate, the input ohmic contact and the output ohmic contact are biased first, to the reference potential of 0 volts. Next, the control gates G_1, G_2 and G_3 are biased negatively with respect to the ohmic contacts by amounts that are less than or equal to the pinch-off voltage of the CMCCD active layer (typically -2.0 volts), depleting the volume of semiconductor under these gates. The quadrature clocks with voltage levels of 0 volts and -5 volts are subsequently applied to the CMCCD, transferring the remaining electrons within the channel to the output of the device

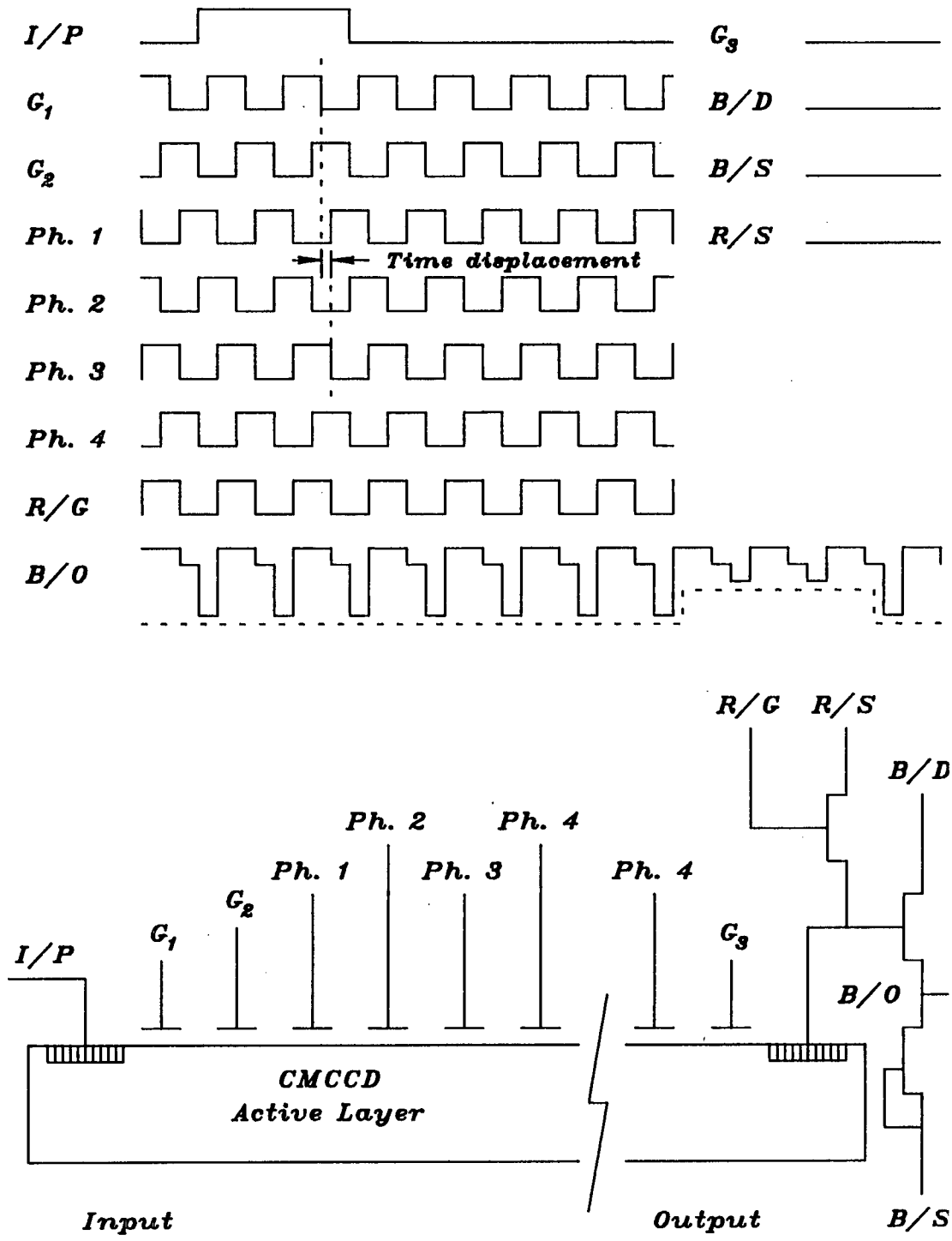

Figure 2.1: A cross-sectional view of the 4-phase GaAs CMCCD with representative signal levels applied to the device nodes.

where they are removed. The input signal is applied to the input ohmic contact once the fully depleted condition is achieved within the channel.

Charge packet generation and injection at the input section of the GaAs CMCCD is accomplished using the diode cutoff method developed by Séquin and Mohsen [27]. The input signal is ac coupled to the input ohmic contact and offset by a positive dc bias, resulting in an applied input signal ranging positively from 0 volts. The phase 3 and phase 4 clock signals are ac coupled to the two input control gates G_1 and G_2, ensuring synchronization between the generation of the charge packet at the input section and the subsequent injection of the charge packet into the transport region. An apparent negative time delay is added to the phase 3 clock signal applied to the input control gate G_1 to minimize forward charge injection during the charge packet generation sequence. The negative time delay is achieved by delaying the phase 3 clock signal applied to G_1 by a positive amount equal to the clock period less a small time displacement (typically 0.5 nanoseconds for a 10 nanosecond clock period).

Figure 2.2 illustrates the theoretical sequence of events that occur to create a discrete charge packet under the control gate G_2 using the diode cutoff method. Initially, the active layer extending from the vicinity of the right-hand edge of the input ohmic contact to the right-hand edge of G_2 is depleted of electrons. Electrons flow into the potential well formed under G_1 from the input ohmic contact during the positive transition of the delayed phase 3 clock applied to G_1. A steady-state condition for the electron density distribution within the potential well under G_1 is achieved during the intervening time prior to the positive transition of the phase 4 clock applied to G_2. Electrons from the input ohmic contact and from the potential well formed under G_1 flow into the potential well formed under G_2 during the positive transition of the phase 4 clock applied to G_2. A steady-state electron density distribution is achieved within the composite potential well formed under both of the input control gates during the remainder of the positive half cycle of the delayed phase 3 clock. During the negative

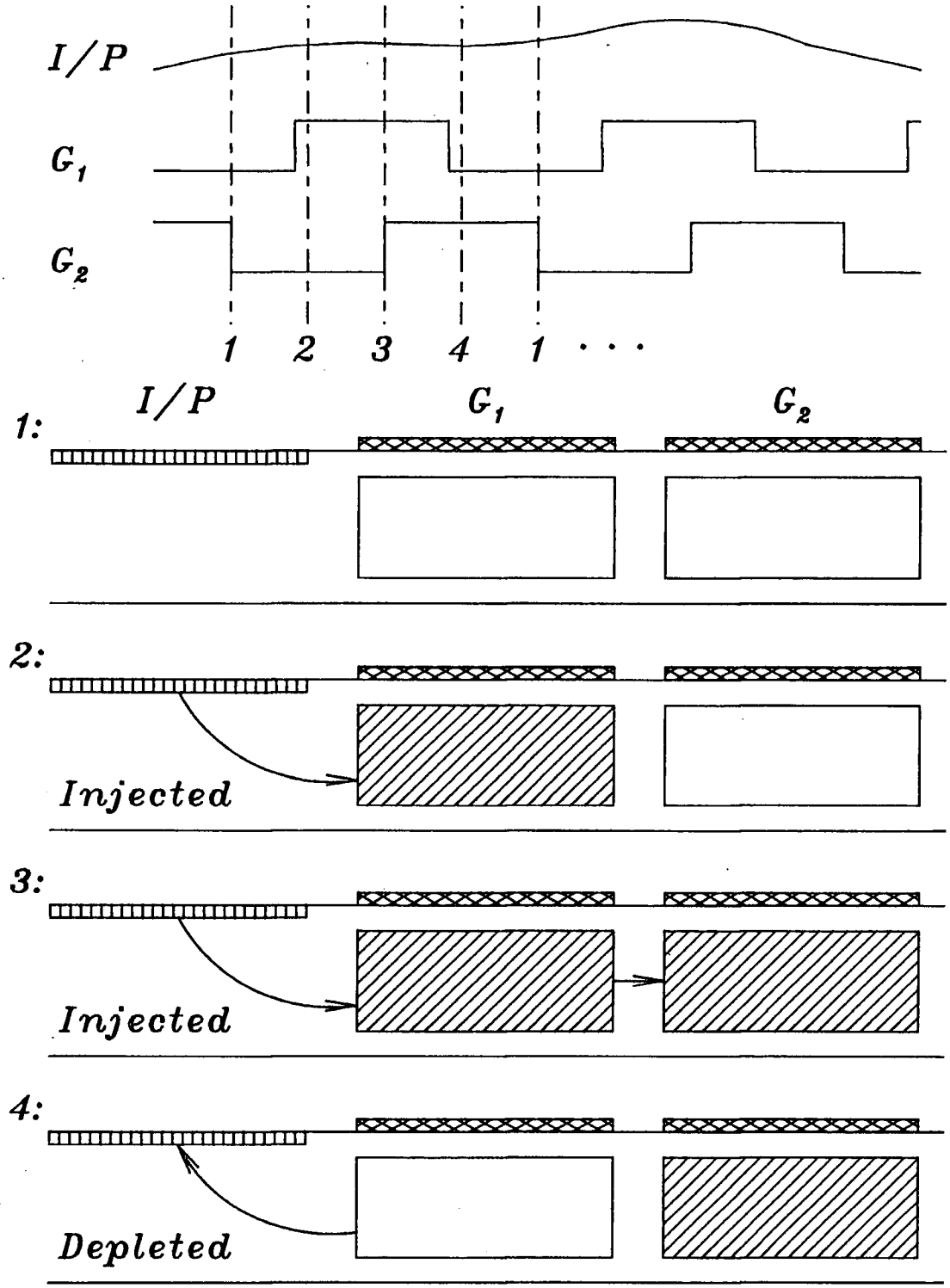

Figure 2.2: The theoretical generation of a charge packet at the input section of a GaAs CMCCD using the diode cutoff method [27].

transition of the delayed phase 3 clock applied to G_1, the electrons residing within the potential well formed under this gate are swept out through the input ohmic contact leaving a discrete charge packet within a potential well residing under the control gate G_2. The magnitude of the localized charge packet within this potential well is a function of the active layer depth, the active layer donor density distribution and the voltage difference between the input ohmic contact and the control gate G_2 at the time of the negative transition of the delayed phase 3 clock applied to the control gate G_1. A full well of charge is produced under the control gate G_2 when this voltage difference is at its minimum value (approximately 0 volts).

The charge packet residing in the potential well formed under G_2 is subsequently injected into the transport region where it is transferred to the output ohmic contact. The injection of the charge packet into the transport region occurs on the positive transition of the phase 1 clock. Figure 2.3 illustrates the theoretical transfer of a charge packet through one pixel of a 4-phase GaAs CMCCD. As indicated in Figure 2.3, the charge packet occupies a potential well that spans two transport electrodes during the transfer process. This is a consequence of the 4-phase clocking scheme that is used. The directionality of charge motion is achieved by the tangential electric fields that arise within the CMCCD channel as a result of the differences between the clock voltage levels applied to the transport electrodes.

The clocking scheme chosen for operating the CMCCD is important as it determines the complexity of both the CMCCD and the clock circuits. The 4-phase structure was chosen for the CMCCD as it has the advantage of not requiring 'built-in' directionality of charge motion, resulting in reduced fabrication requirements to produce the device. The reduced fabrication requirements for producing the 4-phase CMCCD are made at the expense of increased clock circuit complexity. The quadrature clocks that are needed to operate the 4-phase CMCCD require a modest level of circuit design sophistication to achieve the wide bandwidths necessary to operate the device in

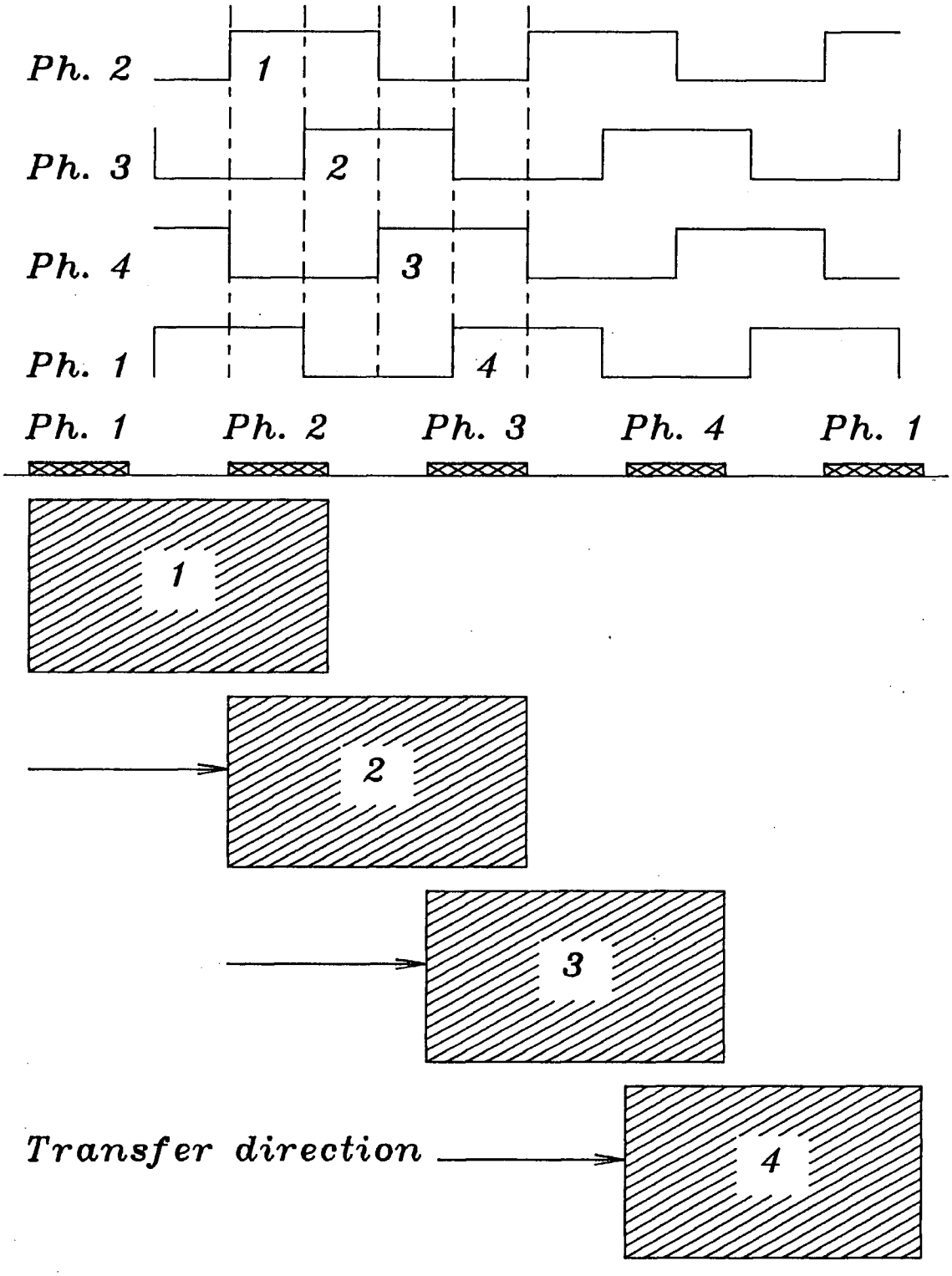

Figure 2.3: The theoretical transfer of a charge packet through one pixel of a 4-phase GaAs CMCCD.

the UHF band. The key issue is the difficulty obtaining stable wideband 90° phase shifts between successive clock phases. The current GaAs MESFET integrated circuit technology is capable of providing a solution to this difficulty [12,13,15,16].

A charge packet transferred to the potential well residing under the final phase 4 transport electrode of the GaAs CMCCD is transmitted to the output ohmic contact on the negative excursion of the phase 4 clock. The output ohmic contact of the CMCCD is precharged to 0 volts during the positive half cycle of the phase 3 clock using the external reset GaAs MESFET. The reset MESFET is disabled during the negative half cycle of the phase 3 clock allowing the output ohmic contact to float at its precharged value. The electrons passing through the potential well formed under G_3 exit the CMCCD through the floating output ohmic contact, charging the parasitic capacitance $C_{O/P}$ and driving the output ohmic contact voltage negatively with respect to its precharged value. A full well of charge arriving at the output ohmic contact will drive the output ohmic contact voltage to its most negative level. The signal produced at the output ohmic contact is buffered from the external output signal processing circuitry using a MESFET source follower amplifier integrated monolithically with the CMCCD. There is usually some distortion observed in the signal obtained from the output of the source follower amplifier which is a consequence of the passive feedthrough of the quadrature clocks to the output ohmic contact. This is reflected as a level change at each occurrence of a clock transition and is illustrated in the output sequence shown in Figure 2.4.

2.2 One-dimensional Potential Distributions

The one-dimensional solution of Poisson's equation for the potential distribution underneath the center of a CMCCD transport electrode, perpendicular to the surface, was determined using the abrupt charge approximation shown in Figure 2.5. The charge distribution illustrated in Figure 2.5 is similar to the one used by Hansell [20] with the

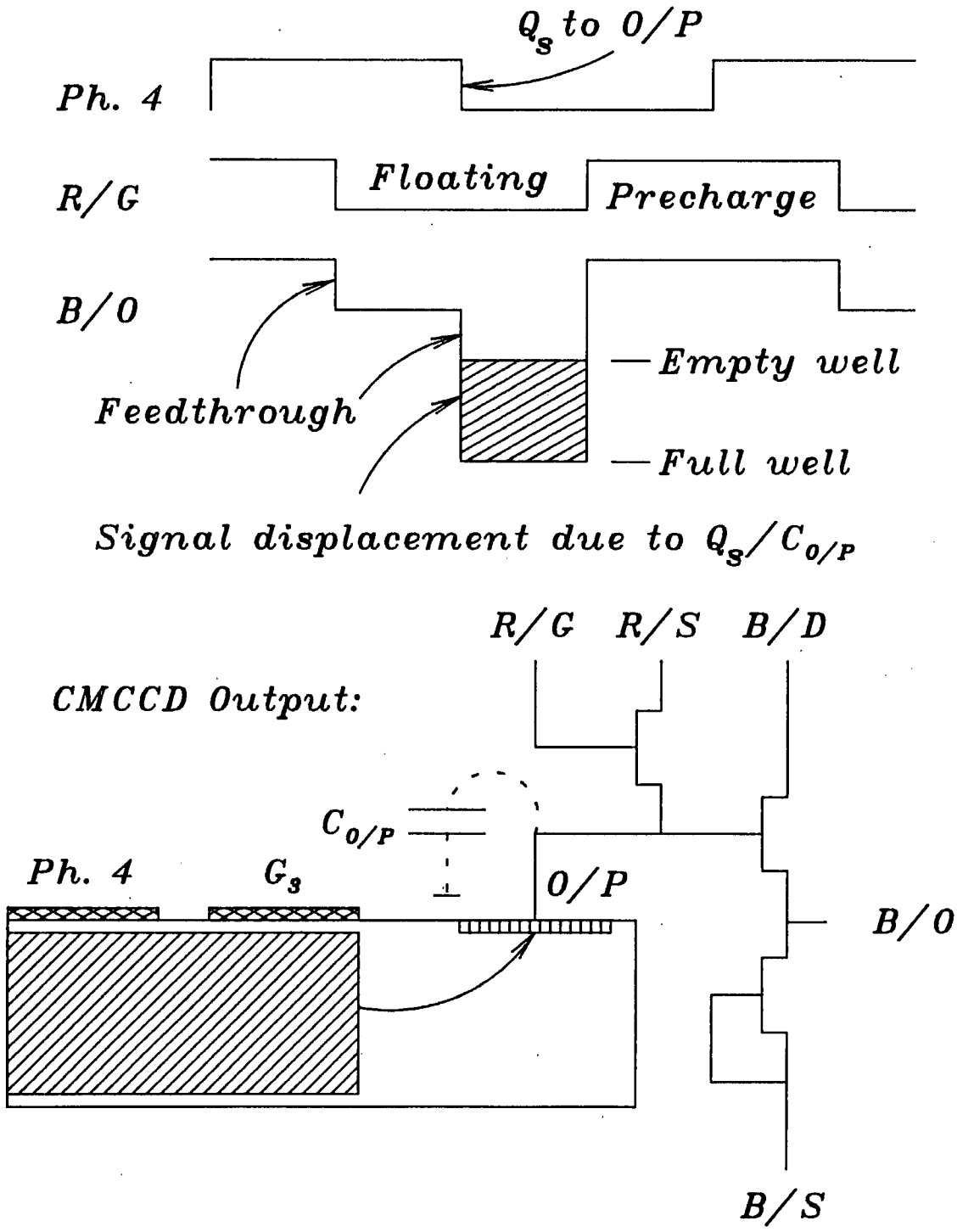

Figure 2.4: The output sequence of a GaAs CMCCD. The signal obtained from the output of the source follower amplifier includes the effects of passive feedthrough from the clocks to the output ohmic contact.

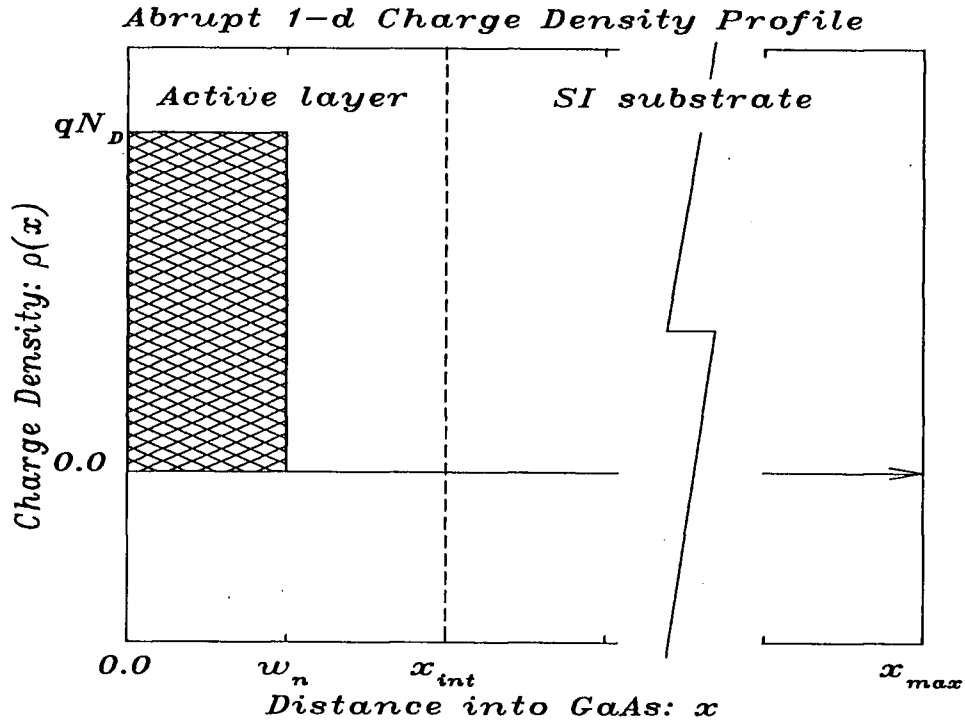

Figure 2.5: The abrupt charge approximation used in the one-dimensional analysis of the potential $\psi(x)$ underneath the center of a CMCCD transport electrode.

exception that the depth of the space charge region is variable. Poisson's equation for the illustrated charge distribution is

$$\frac{d^2\psi(x)}{dx^2} = -\frac{qN_D}{\epsilon} \qquad 0 \leq x \leq w_n \tag{2.2}$$

for the space charge region within the active layer and

$$\frac{d^2\psi(x)}{dx^2} = 0 \qquad w_n \leq x \leq x_{max} \tag{2.3}$$

for the quasi-neutral region within the active layer and for the semi-insulating substrate. The signal charge

$$|Q_s| = qN_D(x_{int} - w_n) \tag{2.4}$$

resides within the channel defined by the quasi-neutral region $w_n \leq x \leq x_{int}$. Here $\psi(x)$ is the potential, N_D is the uniform active layer donor density, q is the charge of

an electron, ϵ is the dielectric constant of GaAs, x_{int} is the active layer depth, x_{max} is the wafer thickness and w_n is the depth of the space charge region under the transport electrode. The potential $\psi(x)$ is related to the intrinsic energy $E_I(x)$ within the GaAs by the relationship $-q\psi(x) = E_I(x) - E_I(x_{max})$.

The boundary conditions are described below. The surface potential is equal to the potential difference V_g between the Fermi level at the surface and the Fermi level at the bottom of the substrate less the potential difference between the metal/GaAs Schottky barrier height at the surface $\phi_{BM,0}$ and the metal/GaAs Schottky barrier height at the bottom of the substrate $\phi_{BM,x_{max}}$

$$\psi(0) = \psi_0 = V_g - (\phi_{BM,0} - \phi_{BM,x_{max}}) \quad ; \tag{2.5}$$

the potential and the electric field across the interface at $x = w_n$ are continuous

$$\psi(w_{n-}) = \psi(w_{n+}) \quad , \tag{2.6}$$

$$\left.\frac{d\psi}{dx}\right|_{w_{n-}} = \left.\frac{d\psi}{dx}\right|_{w_{n+}} \tag{2.7}$$

and the reference energy level is $E_I(x_{max})$.

The solutions for equation 2.2 and equation 2.3 using the boundary conditions 2.5,...,2.7 are

$$\psi(x) = -\frac{qN_D x^2}{2\epsilon} + \left(\frac{qN_D w_n x_{max}}{\epsilon} - \frac{qN_D w_n^2}{2\epsilon} - \psi_0\right)\frac{x}{x_{max}} + \psi_0 \qquad 0 \le x \le w_n \tag{2.8}$$

and

$$\psi(x) = -\left(\frac{qN_D w_n^2}{2\epsilon} + \psi_0\right)\frac{x}{x_{max}} + \frac{qN_D w_n^2}{2\epsilon} + \psi_0 \qquad w_n \le x \le x_{max} \quad . \tag{2.9}$$

The potential variation holding the surface potential ψ_0 constant at zero volts and varying the magnitude of the signal charge $|Q_s|$ within the CMCCD is shown in Figure 2.6 and similarly the potential variation for the empty well condition $|Q_s| = 0$ within the CMCCD and varying the surface potential is shown in Figure 2.7. The peak poten-

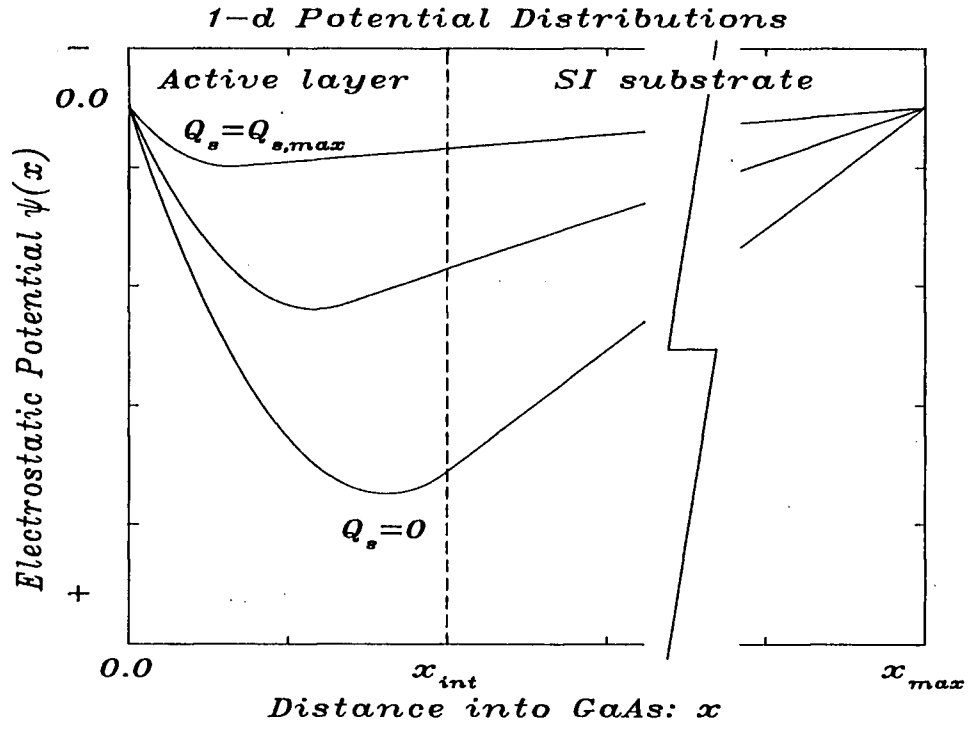

Figure 2.6: The potential as a function of position underneath the center of a CMCCD transport electrode. The surface potential ψ_0 is held constant at zero volts and the signal charge density is varied.

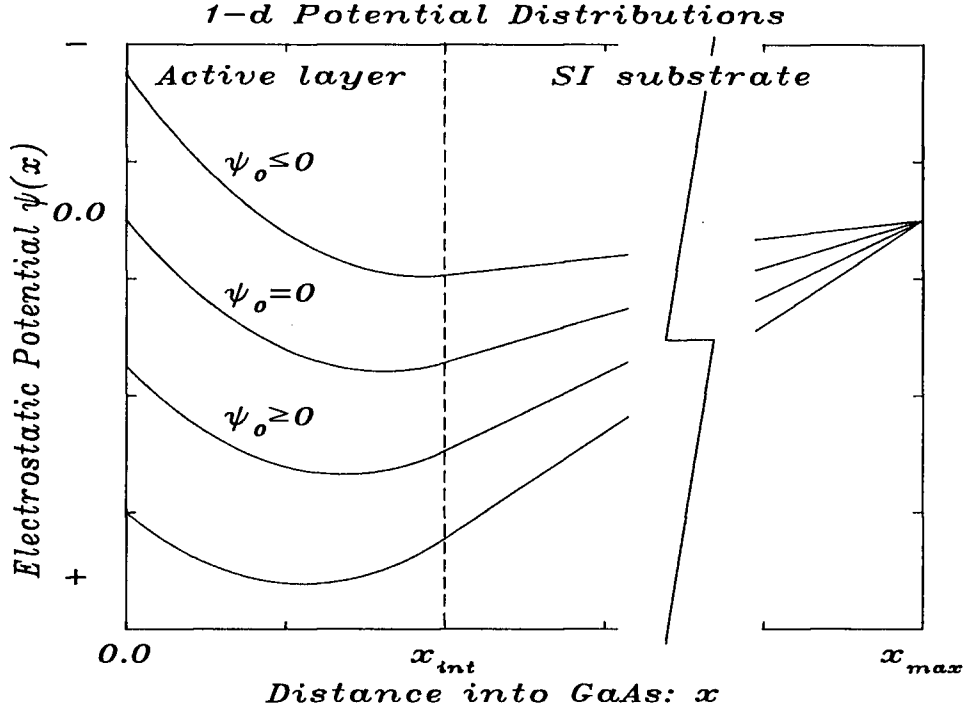

Figure 2.7: The potential as a function of position underneath the center of a CMCCD transport electrode. The signal charge density is held at the empty well condition $|Q_s| = 0$ and the surface potential ψ_0 is varied.

tial within the CMCCD active layer occurs near the depletion region boundary at the location x_m

$$x_m = w_n - \frac{w_n^2}{2x_{max}} - \frac{\epsilon\psi_0}{qN_D x_{max}} \quad . \tag{2.10}$$

The corresponding maximum potential ψ_{max} at this location is

$$\psi_{max} = \psi_0 + \frac{\epsilon\psi_0^2}{2qN_D x_{max}^2} - \left(1 + \frac{w_n}{x_{max}}\right)\frac{w_n\psi_0}{x_{max}} + \left(1 - \frac{w_n}{2x_{max}} + \frac{w_n^2}{x_{max}^2}\right)\frac{qN_D w_n^2}{2\epsilon} \quad . \tag{2.11}$$

2.3 Active Layer Specification

The design of a GaAs CMCCD requires choosing an active layer depth x_{int} and an active layer donor density N_D that are compatible with GaAs MESFETs. The pinch-off voltage of a typical n-type depletion mode GaAs MESFET usually lies between -3 volts and -1 volt constraining the pinch-off voltage of the CMCCD active layer to lie between these two values. The active layer parameters x_{int} and N_D for the GaAs CGCCD were determined by Deyhimy et al [7] and by Hansell [20] to provide a predetermined maximum potential ψ_{max}. The active layer parameters of the GaAs CMCCD were determined using a new method which simultaneously maximizes the charge confinement and the signal charge capacity.

Consider the two adjacent transport electrodes of a CMCCD illustrated schematically in Figure 2.8. Under the left-hand electrode resides a full well of charge as defined by equation 2.4 with w_n equal to a small fraction $\varphi \approx 0$ of the active layer depth x_{int}

$$|Q_{s,max}| = qN_D(1-\varphi)x_{int} \approx qN_D x_{int} \quad . \tag{2.12}$$

Furthermore, assume that the left-hand electrode is biased to the most positive clock voltage level such that $\psi_{0,left} = 0$ volts. The resultant maximum potential under this electrode using equation 2.11 is

$$\psi_{max,left} = \varphi^2\left(1 - \frac{\varphi x_{int}}{2x_{max}} + \frac{\varphi^2 x_{int}^2}{x_{max}^2}\right)\frac{qN_D x_{int}^2}{2\epsilon} \approx 0 \quad . \tag{2.13}$$

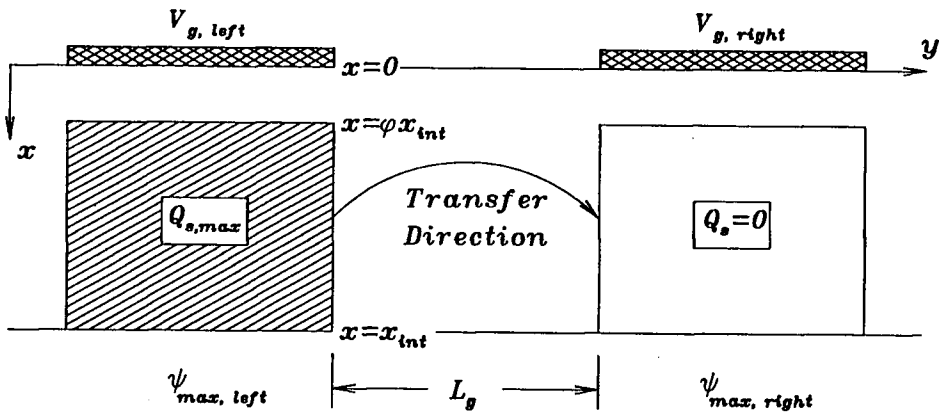

Figure 2.8: The two electrode model for the charge storage mode within a GaAs CM-CCD. A full well of charge resides in the potential well formed under the left-hand electrode. The two electrodes are biased such that $\psi_{max,left} > \psi_{max,right}$.

Similarly, an empty well resides under the right-hand electrode which is biased to the most negative clock voltage level such that $\psi_{0,right} = \psi_{min} < 0$ volts. The maximum potential that results under the right-hand electrode using equation 2.11 is

$$\psi_{max,right} = \psi_{min} + \frac{\epsilon\psi_{min}^2}{2qN_D x_{max}^2} - \left(1 + \frac{x_{int}}{x_{max}}\right)\frac{x_{int}\psi_{min}}{x_{max}} + \left(1 - \frac{x_{int}}{2x_{max}} + \frac{x_{int}^2}{x_{max}^2}\right)\frac{qN_D x_{int}^2}{2\epsilon} \quad . \tag{2.14}$$

The configuration described above corresponds to the case where a charge packet is confined to a potential well residing under the left-hand electrode as a result of a blocking voltage applied to the right-hand electrode. It is necessary that $\psi_{max,left} > \psi_{max,right}$ for charge confinement. The charge confinement $\delta\psi_{max}$ is defined as the potential difference between $\psi_{max,left}$ and $\psi_{max,right}$. The following equation for $\delta\psi_{max}$ is obtained from equations 2.13 and 2.14

$$\delta\psi_{max} = \psi_{max,left} - \psi_{max,right} \approx (|\psi_{min}| - |V_p|) - \left(|\psi_{min}| - \frac{|V_p|}{2}\right)\frac{x_{int}}{x_{max}} \tag{2.15}$$

where it has been assumed that $x_{max} \gg x_{int}$ and

$$|V_p| = \frac{qN_D x_{int}^2}{2\epsilon} < |\psi_{min}| \tag{2.16}$$

is the magnitude of the pinch-off voltage for a uniformly doped n-type active layer [28]. The following relationship for the maximum signal charge density

$$|Q_{s,max}| \propto \frac{|V_p|}{x_{int}} \tag{2.17}$$

is obtained from equation 2.12 and equation 2.16.

The values of x_{int} and N_D for the GaAs CMCCD are determined using the design equations 2.15, 2.16 and 2.17 with the assumption that the pinch-off voltage V_p is a constant value. To simultaneously maximize the charge confinement $\delta\psi_{max}$ and the signal charge capacity $Q_{s,max}$ it is necessary to use a thin, highly doped active layer. Equations 2.15 and 2.17 indicate that $\delta\psi_{max}$ and $Q_{s,max}$ approach maximum values when the active layer depth x_{int} approaches a minimum value. Under the assumption of a constant pinch-off voltage, equation 2.16 indicates that the active layer donor density N_D approaches a maximum value when the active layer depth approaches a minimum value. The above qualitative analysis supports one of the principal advantages of a GaAs CMCCD, the signal charge capacity and the charge packet confinement are optimum for devices fabricated on active layers that are suitable for MESFETs. The GaAs CMCCDs that were fabricated as part of this research utilized epi-wafers possessing a uniform active layer donor density of $4.5 \cdot 10^{16}$ cm^{-3} and an active layer depth of 0.25 microns, corresponding to a pinch-off voltage of approximately -2.0 volts.

Chapter 3

The Cermet/GaAs Junction

3.1 Barrier Properties

A distributed resistive gate Schottky barrier (SB) diode model is described in this section. This model was used to determine the barrier properties of the cermet/GaAs junction from the measured dc current-voltage characteristic of a fabricated cermet/GaAs SB-diode.

The experimental current-voltage measurements were conducted with the planar cermet/GaAs SB-diode illustrated in Figure 3.1. The diode consisted of a Cr:SiO (nominal 45 wt. % Cr) cermet gate attached at one end to a gold contact, a Au-Ge/Ni/Au ohmic contact separated from the cermet gate by a 5.0 micron gap and an active layer possessing a donor density of $4.5 \cdot 10^{16}$ cm^{-3} to a depth of 0.25 microns. The dc current through the diode as a function of the applied dc voltage difference between the gold cermet gate contact and the ohmic contact was measured using a Hewlett-Packard HP-4145A Semiconductor Parameter Analyzer connected to a Wentworth probe station. The measurements were conducted in the dark to minimize photocurrent generation within the diode. The diode current I_{in} measured for discrete input voltages V_{in} lying between -5 volts and +5 volts is shown in Figure 3.2.

It is apparent upon inspection of Figure 3.2 that the cermet/GaAs SB-diode exhibits rectification properties similar to that of a metal/GaAs SB-diode possessing a large series gate resistance. The dc operation of the cermet/GaAs SB-diode illustrated in Figure 3.1 is modeled using the distributed resistive gate SB-diode model shown in Figure 3.3. The resistor R_S is the series resistance (ohms) between the gold cermet gate contact and the active region of the diode plus the series resistance of the bulk GaAs, and R_{CM} is the distributed resistance (ohms/unit length) of the cermet film.

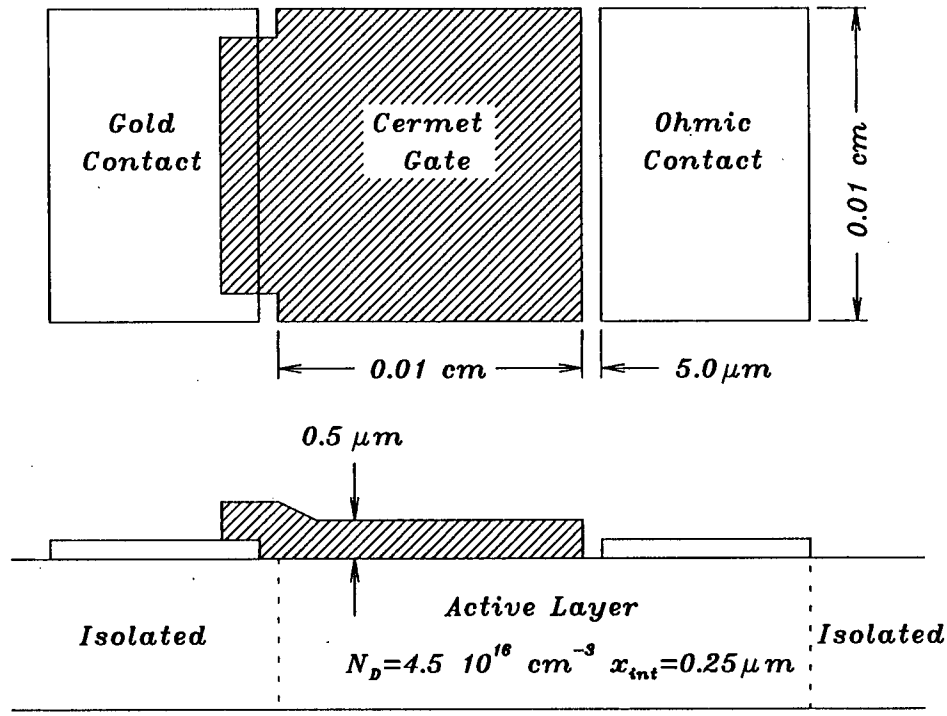

Figure 3.1: The cermet/GaAs Schottky barrier diode used to investigate the barrier properties of the cermet/GaAs junction.

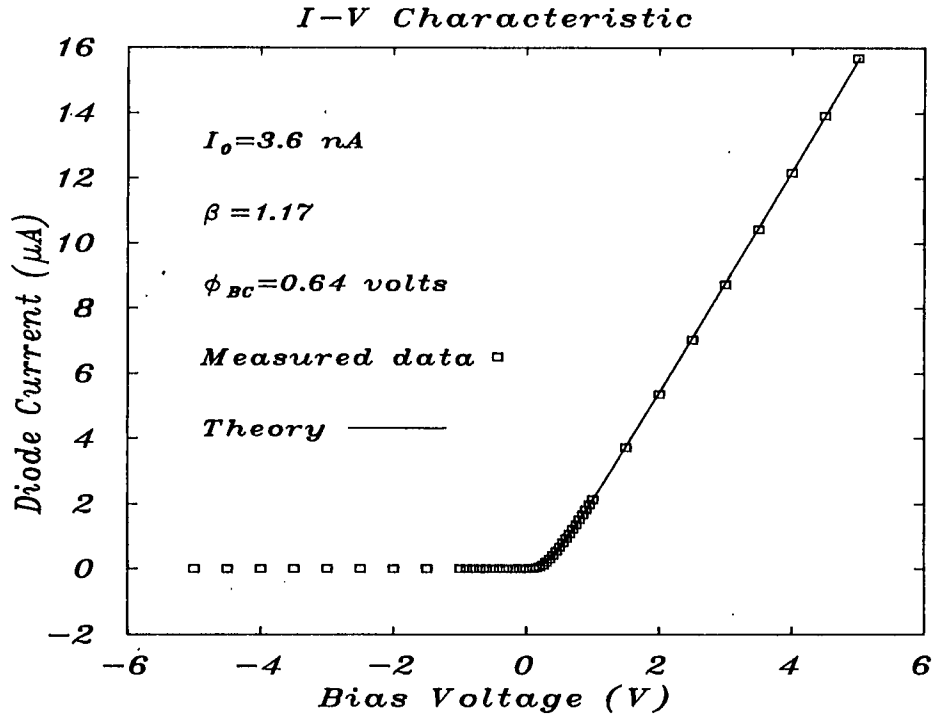

Figure 3.2: The dc current-voltage characteristic of the cermet/GaAs Schottky barrier diode. The solid line is obtained after fitting equation 3.20 to the data.

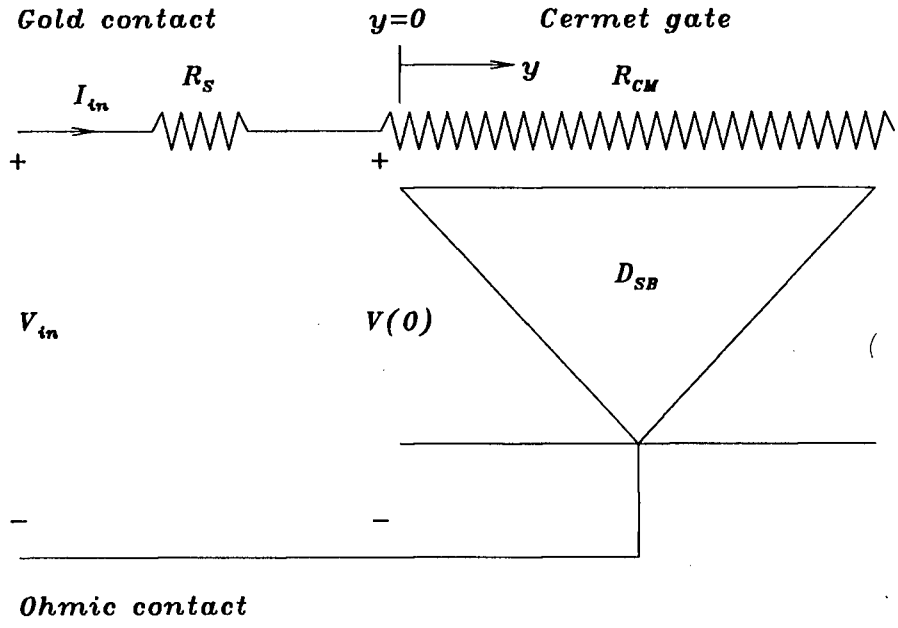

Figure 3.3: The distributed resistive gate Schottky barrier diode model of the cermet/GaAs Schottky barrier diode.

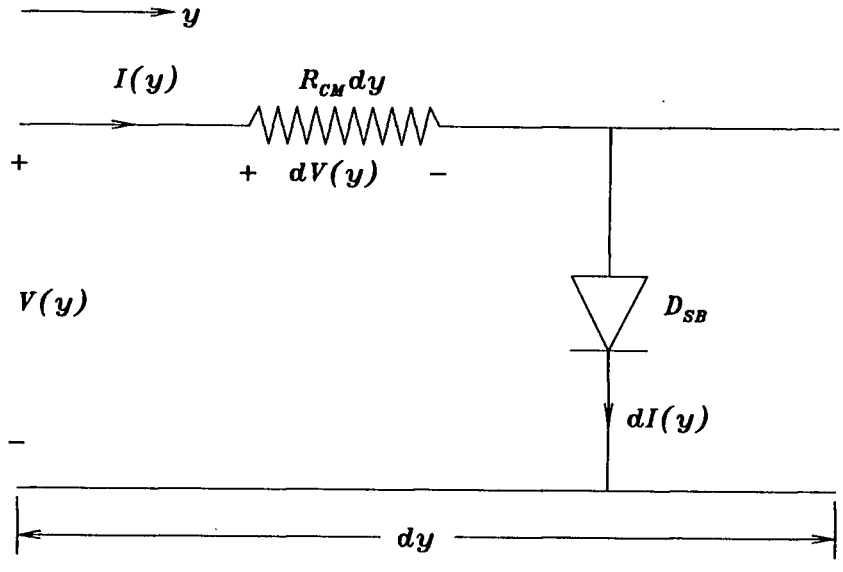

Figure 3.4: A differential length of the distributed resistive gate Schottky barrier diode model.

The current normal to the cermet/GaAs junction is modeled using the distributed SB-diode, D_{SB}.

A differential length of the distributed resistive gate SB-diode model is shown in Figure 3.4. The differential voltage drop along this length and the differential current normal to the cermet/GaAs junction are

$$dV(y) = R_{CM} I(y) dy \tag{3.1}$$

$$dI(y) = w J_0 \left[\exp\left(\frac{V(y)}{\beta U_T} \right) - 1 \right] dy \tag{3.2}$$

where y is the position variable, w is the cermet gate width, β is the ideality factor, U_T is the thermal voltage and J_0 is the saturation current density. The saturation current density is given by [29]

$$J_0 = A^* T^2 \exp\left(\frac{-\phi_{BC}}{U_T} \right) \tag{3.3}$$

where A^* is the modified Richardson's constant, ϕ_{BC} is the cermet/GaAs Schottky barrier height and T is the temperature. Differentiating equation 3.2 with respect to the variable y gives

$$\frac{d^2 I}{dy^2} = \frac{w J_0}{\beta U_T} \exp\left(\frac{V}{\beta U_T} \right) \frac{dV}{dy} \quad . \tag{3.4}$$

Substituting equation 3.1 and equation 3.2 into equation 3.4 yields

$$\frac{d^2 I}{dy^2} - aI \frac{dI}{dy} - bI = 0 \tag{3.5}$$

where $a = R_{CM}/\beta U_T$ and $b = w R_{CM} J_0 / \beta U_T$ are constants.

The nonlinear second-order differential equation 3.5 describes the spatial variation of the tangential current along the cermet/GaAs junction. This equation can be solved analytically in the following manner [30]. Substitute

$$S = \frac{dI}{dy} \tag{3.6}$$

and

$$\frac{d^2 I}{dy^2} = \frac{dS}{dy} = \frac{dS}{dI} \frac{dI}{dy} = S \frac{dS}{dI} \tag{3.7}$$

into equation 3.5 to give the following first-order linear differential equation

$$S\frac{dS}{dI} - (aS + b)I = 0 \quad . \tag{3.8}$$

The solution to equation 3.8 is obtained using separation of variables

$$S - \frac{b}{a}\ln\left(S + \frac{b}{a}\right) = \frac{aI^2}{2} + c_1 \tag{3.9}$$

where c_1 is a constant of integration determined as follows. As the tangential current I approaches zero the derivative of the tangential current with respect to the variable y also approaches zero. Hence, the boundary condition for equation 3.9 is

$$S(I = 0) = 0 \tag{3.10}$$

which yields

$$c_1 = -\frac{b}{a}\ln\left(\frac{b}{a}\right) \quad . \tag{3.11}$$

Substituting equation 3.11 into equation 3.9 gives

$$S - \frac{b}{a}\ln\left(1 + \frac{aS}{b}\right) = \frac{aI^2}{2} \quad . \tag{3.12}$$

Equation 3.2, equation 3.6 and the relationship $b/a = wJ_0$ yields

$$S = \frac{b}{a}\left[\exp\left(\frac{V}{\beta U_T}\right) - 1\right] \quad . \tag{3.13}$$

Substituting equation 3.13 into equation 3.12 gives

$$\exp\left(\frac{V(y)}{\beta U_T}\right) - \frac{V(y)}{\beta U_T} - 1 = \frac{a^2 I^2(y)}{2b} \quad . \tag{3.14}$$

Rearranging equation 3.14 results in an expression for the current $I(y)$ as a function of the voltage $V(y)$

$$I(y) = I_0\sqrt{\exp\left(\frac{V(y)}{\beta U_T}\right) - \frac{V(y)}{\beta U_T} - 1} \tag{3.15}$$

where

$$I_0 = \pm\frac{\sqrt{2b}}{a} = \pm\sqrt{\frac{2w\beta U_T J_0}{R_{CM}}} \tag{3.16}$$

is the saturation current. The sign of the saturation current is chosen to be the same as the sign of the voltage $V(y)$.

The ideality factor, the saturation current and the Schottky barrier height of the cermet/GaAs Schottky barrier were determined from the measured current-voltage data of the cermet/GaAs SB-diode shown in Figure 3.1. The distributed resistive gate SB-diode model illustrated in Figure 3.3 yields

$$V_{in} = R_S I_{in} + V(0) \tag{3.17}$$

for the dc terminal parameters of the cermet/GaAs SB-diode. The diode voltage $V(0)$ is obtained from equation 3.15 with $I(0) = I_{in}$

$$I_{in} = I_0 \sqrt{\exp\left(\frac{V(0)}{\beta U_T}\right) - \frac{V(0)}{\beta U_T} - 1} \quad . \tag{3.18}$$

Under forward bias conditions where $V(0)/\beta U_T > 3$, equation 3.18 yields

$$V(0) \approx 2\beta U_T \ln\left(\frac{I_{in}}{I_0}\right) \quad . \tag{3.19}$$

Substituting equation 3.19 into equation 3.17 gives

$$V_{in} = R_s I_{in} + 2\beta U_T \ln\left(\frac{I_{in}}{I_0}\right) \quad . \tag{3.20}$$

Fitting equation 3.20 to the measured current-voltage data of the cermet/GaAs SB-diode for $V_{in} \geq 0.2$ volts yields the solid line illustrated in Figure 3.2 and the barrier parameters listed in Table I.

3.2 Surface Potentials

It was demonstrated in the previous section that the cermet/GaAs junction forms a Schottky barrier. This characteristic is used to control the surface potential within the interelectrode gaps of the GaAs CMCCD. It will be demonstrated in this section using a cermet/GaAs transmission line model that the surface potential varies monotonically along the gap of a GaAs CMCCD.

Parameter	Value
T	300 K
U_T	0.0259 volts
w	100 μm
A^*	$7.8 \cdot 10^{-8}$ A/μm^2·K^2
R_S	287.9 kΩ
R_{CM}	55 kΩ/μm
β	1.17
I_0	3.60 nA
ϕ_{BC}	0.64 volts

Table I: A summary of the cermet/GaAs Schottky barrier parameters.

The proposed cermet/GaAs transmission line model of a uniform cermet/GaAs contact within an interelectrode gap of a GaAs CMCCD is illustrated in Figure 3.5 with a differential length of the cermet/GaAs transmission line shown in Figure 3.6. The distributed series impedance Z (ohms/unit length) is modeled using the parallel network [22] comprised of the distributed cermet film resistance R_{CM} (ohms/unit length) and the distributed cermet film capacitance C_{CM} (farads·unit length)

$$Z = \frac{R_{CM}}{1 + \jmath\omega R_{CM} C_{CM}} \tag{3.21}$$

where ω is the radian frequency. The distributed shunt admittance Y (siemens/unit length) is modeled using the distributed depletion layer capacitance of the active layer C_D (farads/unit length)

$$Y = \jmath\omega C_D \quad . \tag{3.22}$$

The position along the gap is denoted by the variable y with $y = 0$ defined at the right-hand edge of the left-hand transport electrode and $y = L_g$ defined at the left-hand edge of the right-hand transport electrode.

The spatial variation of the surface potential along the gap is described by the voltage wave equation for a uniform transmission line [31]. For harmonically varying

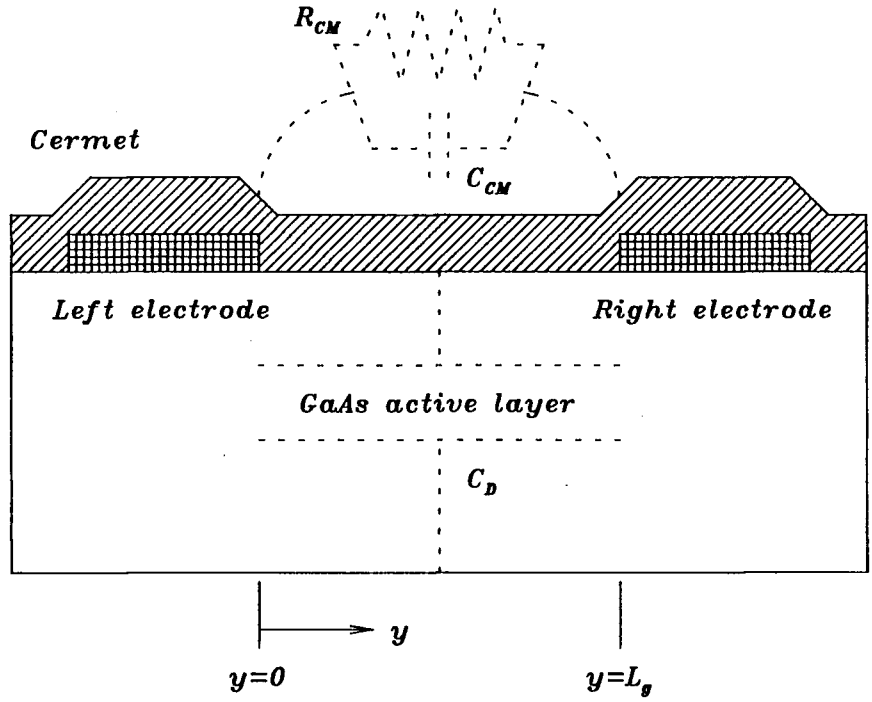

Figure 3.5: The cermet/GaAs transmission line model of the uniform cermet/GaAs contact within an interelectrode gap of a GaAs CMCCD.

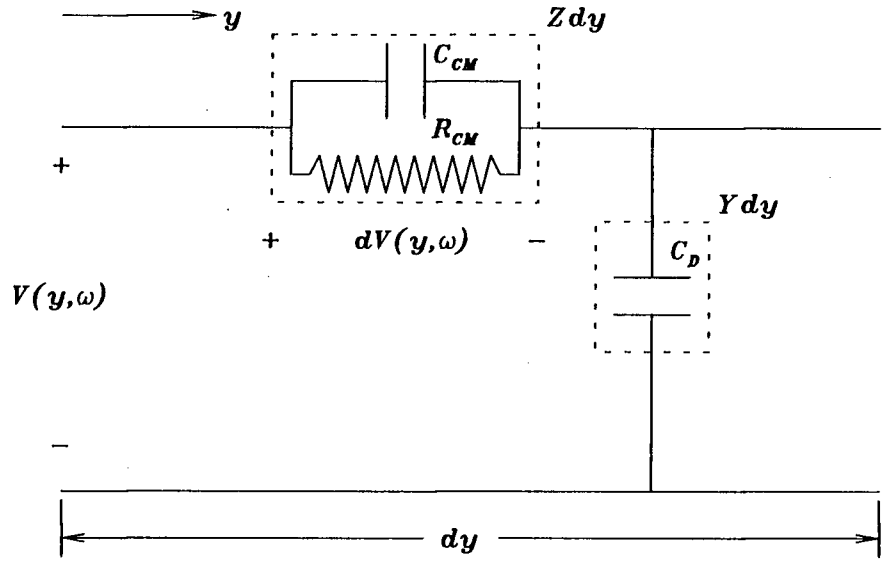

Figure 3.6: A differential length of the cermet/GaAs transmission line model.

voltages this equation is

$$\frac{\partial^2 V(y,\omega)}{\partial y^2} = YZV(y,\omega) \quad . \tag{3.23}$$

where the factor $e^{\jmath\omega t}$ has been suppressed. The solution to equation 3.23 is

$$V(y,\omega) = k_1 e^{\gamma(\omega)y} + k_2 e^{-\gamma(\omega)y} \tag{3.24}$$

where k_1, k_2 are integration constants and $\gamma(\omega)$ is the propagation constant

$$\begin{aligned} \gamma(\omega) &= \sqrt{YZ} \\ &= \sqrt{\frac{\jmath\omega R_{CM} C_D}{1 + \jmath\omega R_{CM} C_{CM}}} \\ &= \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}} \right) \exp\left[\frac{\jmath}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}} \right) \right] \quad . \end{aligned} \tag{3.25}$$

The boundary conditions imposed on the solution 3.24 are

$$V(y=0) = V_0 \tag{3.26}$$

$$V(y=L_g) = 0 \tag{3.27}$$

where $V_0 > 0$ is the incident voltage amplitude. The integration constants k_1 and k_2 are obtained by substituting the boundary conditions 3.26 and 3.27 into equation 3.24 to give

$$k_1 = \frac{-e^{-2L_g\gamma(\omega)} V_0}{1 - e^{-2L_g\gamma(\omega)}} \tag{3.28}$$

$$k_2 = \frac{V_0}{1 - e^{-2L_g\gamma(\omega)}} \quad . \tag{3.29}$$

Substituting equation 3.28 and equation 3.29 into equation 3.24 yields the solution for the surface potential along the gap as a function of position and frequency

$$V(y,\omega) = \frac{\sinh\left[(L_g - y)\gamma(\omega)\right]}{\sinh[L_g\gamma(\omega)]} V_0 \quad . \tag{3.30}$$

The surface potential $V(y,\omega)$ is conveniently expressed in polar form as

$$V(y,\omega) = V_0 H(y,\omega) \angle \Theta(y,\omega) \tag{3.31}$$

where $H(y,\omega)$ is the normalized magnitude of the surface potential

$$H(y,\omega) = \left(\frac{\cosh^2[a(y,\omega)] - \cos^2[b(y,\omega)]}{\cosh^2[c(\omega)] - \cos^2[d(\omega)]} \right)^{\frac{1}{2}} \tag{3.32}$$

and $\Theta(y,\omega)$ is the phase shift of the surface potential

$$\Theta(y,\omega) = \arctan(\coth[a(y,\omega)]\tan[b(y,\omega)]) - \arctan(\coth[c(\omega)]\tan[d(\omega)]) \quad . \tag{3.33}$$

The functions $a(y,\omega)$, $b(y,\omega)$, $c(\omega)$ and $d(\omega)$ are

$$a(y,\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1+(\omega R_{CM} C_{CM})^2}} \right)^{\frac{1}{2}} (L_g - y) \cos\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}} \right) \right], \tag{3.34}$$

$$b(y,\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1+(\omega R_{CM} C_{CM})^2}} \right)^{\frac{1}{2}} (L_g - y) \sin\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}} \right) \right], \tag{3.35}$$

$$c(\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1+(\omega R_{CM} C_{CM})^2}} \right)^{\frac{1}{2}} L_g \cos\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}} \right) \right], \tag{3.36}$$

$$d(\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1+(\omega R_{CM} C_{CM})^2}} \right)^{\frac{1}{2}} L_g \sin\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}} \right) \right] \quad . \tag{3.37}$$

The derivation of the polar form of $V(y,\omega)$ is described in Appendix B.

The function $H(y,\omega)$ described by equation 3.32 decreases monotonically for the choice of boundary conditions 3.26 and 3.27 used above. Interchanging the boundary conditions will result in the surface potential increasing monotonically, as the cermet/GaAs transmission line model illustrated in Figure 3.5 is symmetric. It is sufficient to show that equation 3.32 satisfies the condition

$$\left. \frac{\partial H(y,\omega)}{\partial y} \right|_{\omega = constant} \leq 0 \tag{3.38}$$

to demonstrate that the surface potential varies monotonically on the interval $0 \leq y \leq L_g$ for all frequencies $\omega \geq 0$. Differentiating equation 3.32 with respect to the variable y gives

$$\frac{\partial H(y,\omega)}{\partial y} = \frac{\cosh[a(y,\omega)]\sinh[a(y,\omega)]\frac{\partial a(y,\omega)}{\partial y} + \cos[b(y,\omega)]\sin[b(y,\omega)]\frac{\partial b(y,\omega)}{\partial y}}{\left(\cosh^2[a(y,\omega)] - \cos^2[b(y,\omega)]\right)^{\frac{1}{2}} \left(\cosh^2[c(\omega)] - \cos^2[d(\omega)]\right)^{\frac{1}{2}}} \quad . \tag{3.39}$$

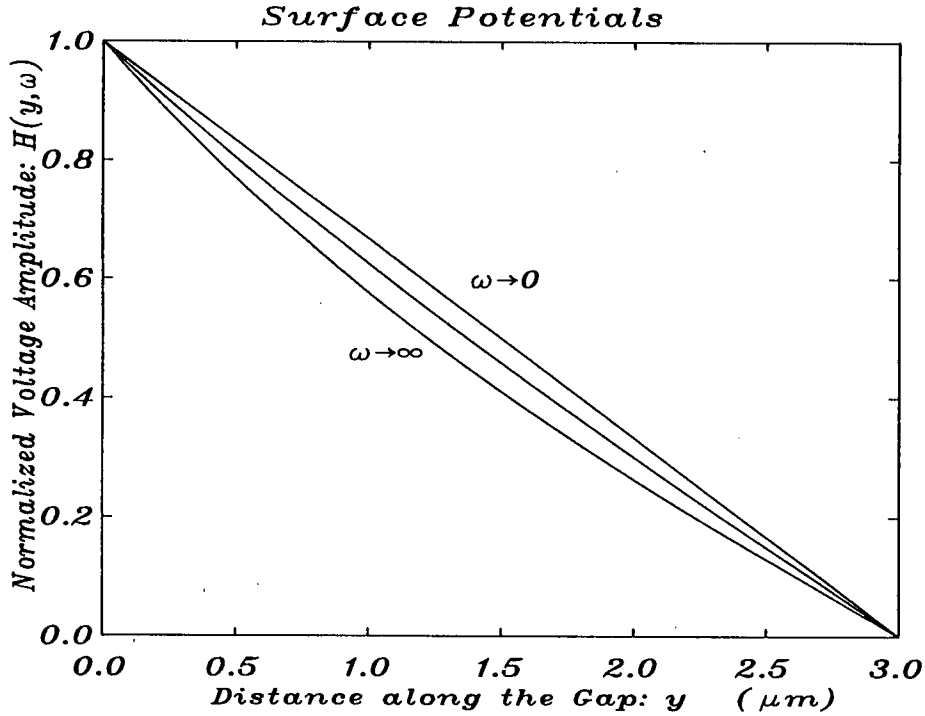

Figure 3.7: The variation of the normalized surface potential along the gap of a GaAs CMCCD as a function of frequency.

The functions $a(y,\omega)$, $b(y,\omega)$, $c(\omega)$ and $d(\omega)$ are positive functions of y and ω, and the derivatives $\partial a(y,\omega)/\partial y$ and $\partial b(y,\omega)/\partial y$ are negative functions of ω. Consequently, the derivative of the normalized surface potential $H(y,\omega)$ with respect to the variable y is negative, satisfying the condition 3.38.

The variation of the normalized surface potential along a gap of a GaAs CMCCD as a function of frequency is illustrated in Figure 3.7. Equation 3.32 and the parameter values listed in Table II were used to produce the curves. The parameter values were obtained using a Hewlett-Packard HP-4275A Multi-Frequency LCR Meter and an Alessi probe station to perform low-frequency (10 kHz) impedance measurements on a fabricated cermet/GaAs test structure. It is apparent from Figure 3.7 that the surface potential decreases monotonically along the gap for all positive frequencies. There are two special cases which are of interest: the case when the frequency approaches zero and the case when the frequency approaches infinity.

Parameter	Value	Scale Factor
R_{CM}	55 kΩ/μm	$L_g/127$
C_{CM}	0.8 pF$\cdot\mu$m	$127/L_g$
C_D	15 fF/μm	$127L_g$
L_g	3.0 μm	—

Table II: The distributed circuit parameters of the cermet/GaAs contact.

The dc surface potential variation along a gap of a GaAs CMCCD is linear. The propagation constant $\gamma(\omega)$ is zero when $\omega = 0$ resulting in an indeterminate form for the normalized surface potential $H(y, \omega = 0)$. L'Hospital's rule is used to resolve the indeterminate form

$$\begin{aligned} H(y,\omega=0) &= \lim_{\gamma(\omega)\to 0} \frac{\sinh\left[(L_g-y)\gamma(\omega)\right]}{\sinh[L_g\gamma(\omega)]} \\ &= \lim_{\gamma(\omega)\to 0} \frac{(L_g-y)\cosh\left[(L_g-y)\gamma(\omega)\right]}{L_g\cosh[L_g\gamma(\omega)]} \\ &= \left(1-\frac{y}{L_g}\right) \quad . \end{aligned} \tag{3.40}$$

Equation 3.40 is intuitively correct. At low frequencies the electric current through the cermet/GaAs contact would be dominantly through the distributed cermet film resistance R_{CM} and would result in a linear surface potential variation. This intuitive argument was probably the basis for deriving the name *resistive gate CCD* applied to the original cermet gate CCD described in reference [18]. The adjective *resistive* used in the cited reference is considered to be a misnomer [32] as it implies that the surface potential variation along a gap of a GaAs CMCCD is established via resistive conduction only, and does not take into consideration the effect of capacitive coupling within the cermet film at higher clock frequencies. The adjective *cermet* has been used instead to avoid the implications of the term *resistive*.

The high frequency normalized surface potential variation along a gap of a GaAs

CMCCD is

$$H(y,\omega \to \infty) = \frac{\sinh\left[\sqrt{\frac{C_D}{C_{CM}}}(L_g - y)\right]}{\sinh\left(\sqrt{\frac{C_D}{C_{CM}}}L_g\right)} \tag{3.41}$$

where the high frequency value for the propagation constant $\gamma(\omega)$ is determined using equation 3.25

$$\gamma(\omega \to \infty) = \sqrt{\frac{C_D}{C_{CM}}} \quad . \tag{3.42}$$

Equation 3.41 is independent of the distributed cermet film resistance R_{CM}. This suggests that a wide range of cermet film resistivities can be used in the design of a GaAs CMCCD. A requirement that must be satisfied by the cermet film resistivity is that it must be large enough to comply with the power constraints of the CMCCD quadrature clock drivers.

The capacitive coupling between the cermet film and the underlying GaAs is responsible for establishing the high frequency surface potential variation along a gap of a GaAs CMCCD. Figure 3.8 illustrates the effect of different ratios of C_D/C_{CM} on the normalized high frequency surface potential $H(y,\omega \to \infty)$. It is apparent from the curves illustrated in Figure 3.8 that it is desirable to minimize the ratio C_D/C_{CM} in order to maintain a nearly linear surface potential variation for all frequencies. The reason for this is that a virtual equipotential zone extends along the surface into the gap near the right-hand transport electrode at $y = L_g$ for large ratios of C_D/C_{CM}. The extent of this zone increases with this ratio. This is undesirable as the tangential electric field within the active layer would be reduced underneath the equipotential zone along the surface, creating a source of potential loss of performance in a GaAs CMCCD operating at high frequencies. Minimizing the ratio C_D/C_{CM} would reduce this negative effect.

3.3 Verification

Frequency response measurements performed on a 2-port cermet/GaAs test structure were used to test the validity of the cermet/GaAs transmission line model. The test

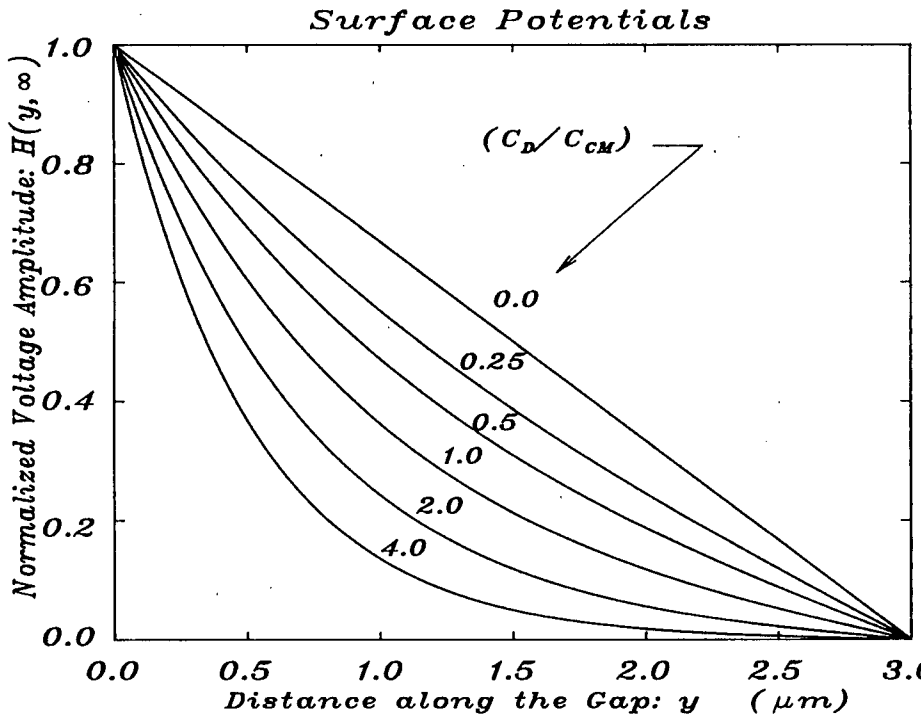

Figure 3.8: The variation of the normalized high frequency surface potential along the gap of a GaAs CMCCD as a function of the ratio C_D/C_{CM}.

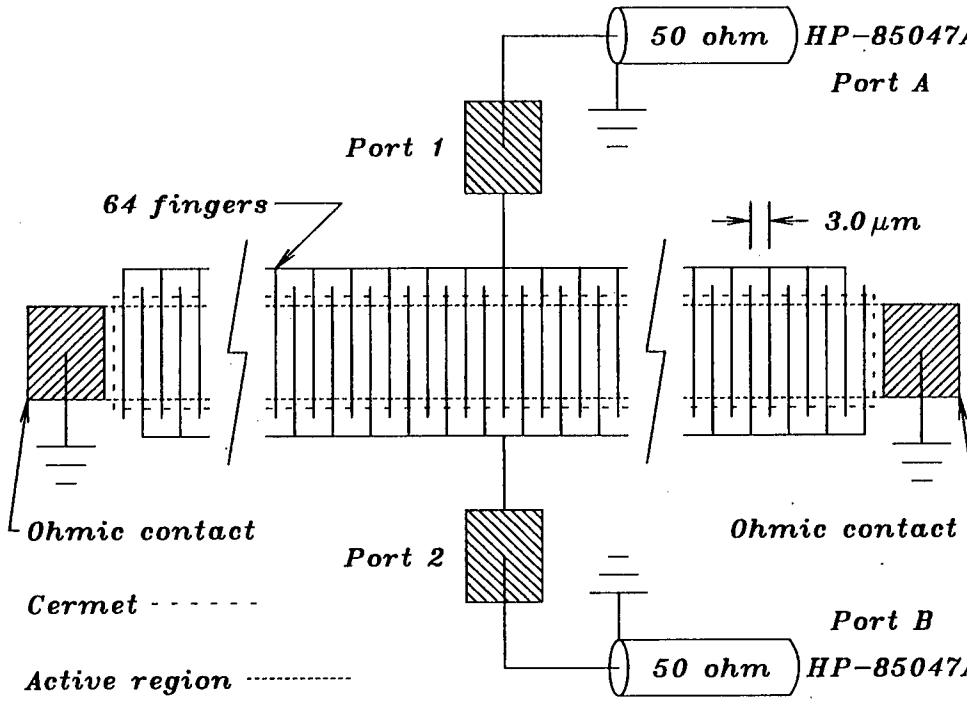

Figure 3.9: The test structure and the test circuit used to demonstrate the validity of the transmission line model for the cermet/GaAs contact within a gap of a GaAs CMCCD.

structure was fabricated on a n-type active layer ($N_D = 4.5 \cdot 10^{16}$ cm^{-3}, $x_{int} = 0.25$ microns) and consisted of two interleaved arrays of sixty-four, 3 micron long Ti-Pt-Au Schottky barriers encapsulated with a nominal 5000 Å thick cermet film deposition of Cr:SiO (nominal 45 wt. % Cr). The separation between adjacent metal fingers was 3 microns. Two Au/Ge-Ni-Au ohmic contacts were provided at each end of the 100 micron wide active region. The test structure was packaged in a leadless chip carrier which permitted external connections to be made to the two ports. The ohmic contacts were connected to the reference potential and the two electrode arrays were connected to the measurement apparatus using 50 ohm rigid copper coaxial cables. The test structure and the test circuit are shown schematically in Figure 3.9.

The frequency response measurements consisted of measuring the amplitude response and the phase response of the cermet/GaAs test structure. The measurement apparatus consisted of a Hewlett-Packard HP-8753B network analyzer and an HP-85047A s-parameter test set. The 50 ohm port A and port B terminals of the s-parameter test set were connected to the two ports of the test structure. The amplitude response and the phase response were measured using a 0 dBm, 300 kHz–500 MHz swept rf signal and are shown in Figure 3.10. The reference levels are indicated in each of the two plots by the arrows. The marker triangle labeled with the number '1' coincides with the maximum observed phase shift of 53.1° at 12.8 MHz.

The lumped equivalent circuit shown in Figure 3.11 was used to model the theoretical frequency response of the cermet/GaAs transmission line test circuit. The transmission line length $L_g = 3$ microns is much less than the effective wavelength of the cermet/GaAs transmission line below 500 MHz operation, hence the one hundred twenty-seven parallel connected cermet/GaAs transmission lines are modeled approximately using the lumped elements $\bar{R}_{CM}$, $\bar{C}_{CM}$ and $\bar{C}_D$. The lumped element values are obtained from the distributed element values listed in Table II after multiplying by the scale factors listed in the third column of this table. The theoretical amplitude

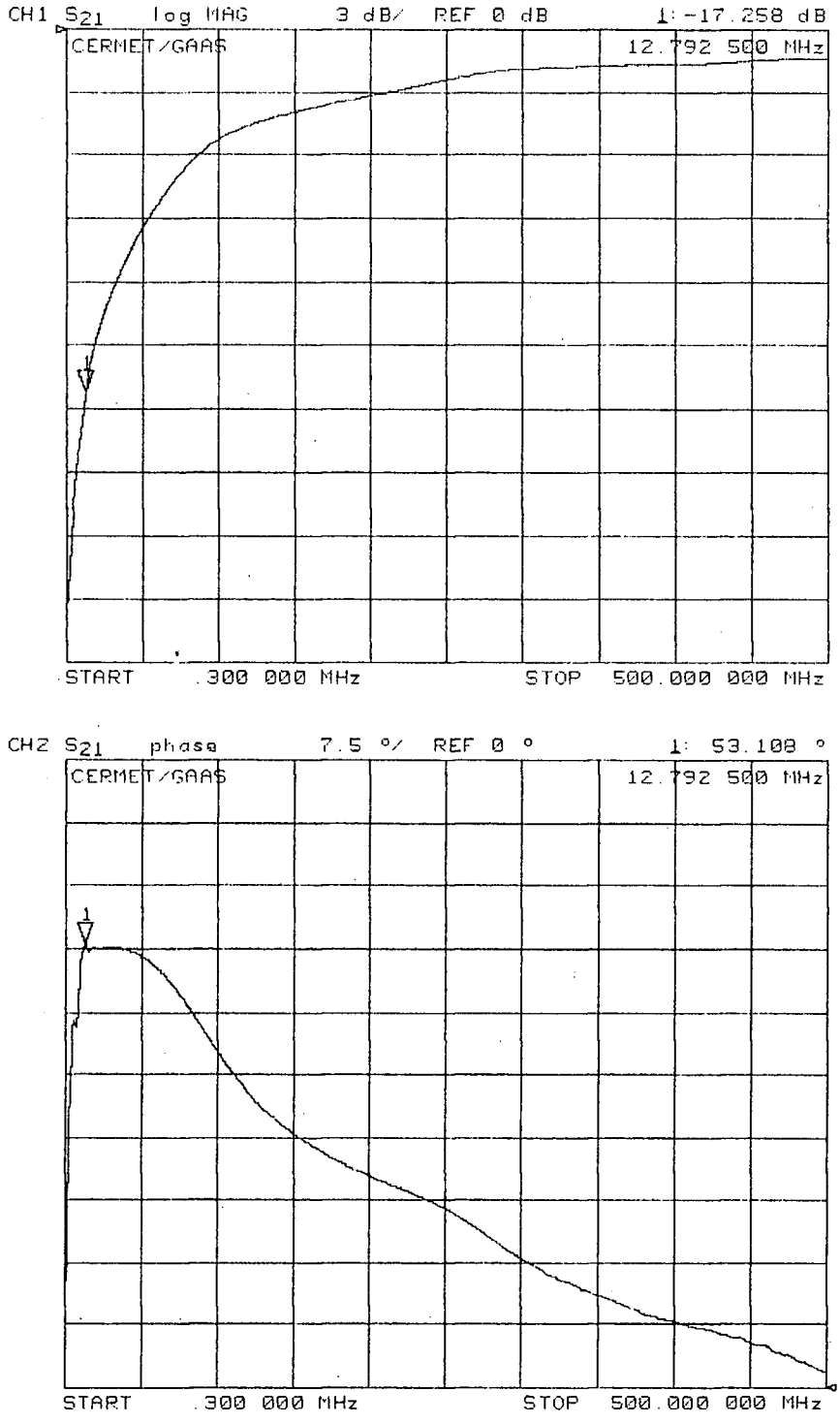

Figure 3.10: The amplitude response (3 dB/division) and the phase response (7.5°/division) of the cermet/GaAs test circuit measured from 300 kHz to 500 MHz.

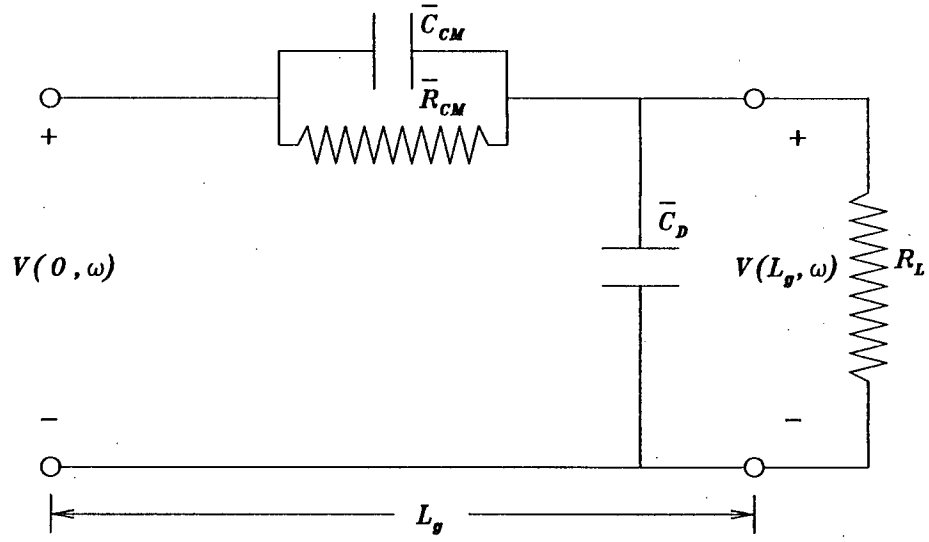

Figure 3.11: The lumped equivalent circuit of the cermet/GaAs transmission line test circuit.

response of the test circuit is

$$A_{dB} = -20\log\left|\frac{V(L_g,\omega)}{V(0,\omega)}\right| = -10\log\left(\frac{R_L^2 + (\omega R_L \bar{R}_{CM}\bar{C}_{CM})^2}{(R_L + \bar{R}_{CM})^2 + (\omega R_L \bar{R}_{CM}[\bar{C}_D + \bar{C}_{CM}])^2}\right) \tag{3.43}$$

and the theoretical phase response of the test circuit is

$$\Phi = \arctan\left(\omega \bar{R}_{CM}\bar{C}_{CM}\right) - \arctan\left(\frac{\omega R_L \bar{R}_{CM}(\bar{C}_D + \bar{C}_{CM})}{R_L + \bar{R}_{CM}}\right) \tag{3.44}$$

The theoretical amplitude and phase responses of the cermet/GaAs test circuit are illustrated in Figures 3.12 and 3.13, respectively. The theoretical and measured responses are in reasonable agreement, supporting the cermet/GaAs transmission line model described in the previous section. The deviation between the theoretical and measured responses is a result of the parasitic components associated with the interconnect wiring between the cermet/GaAs test circuit and the network analyzer, which are neglected in the above analysis.

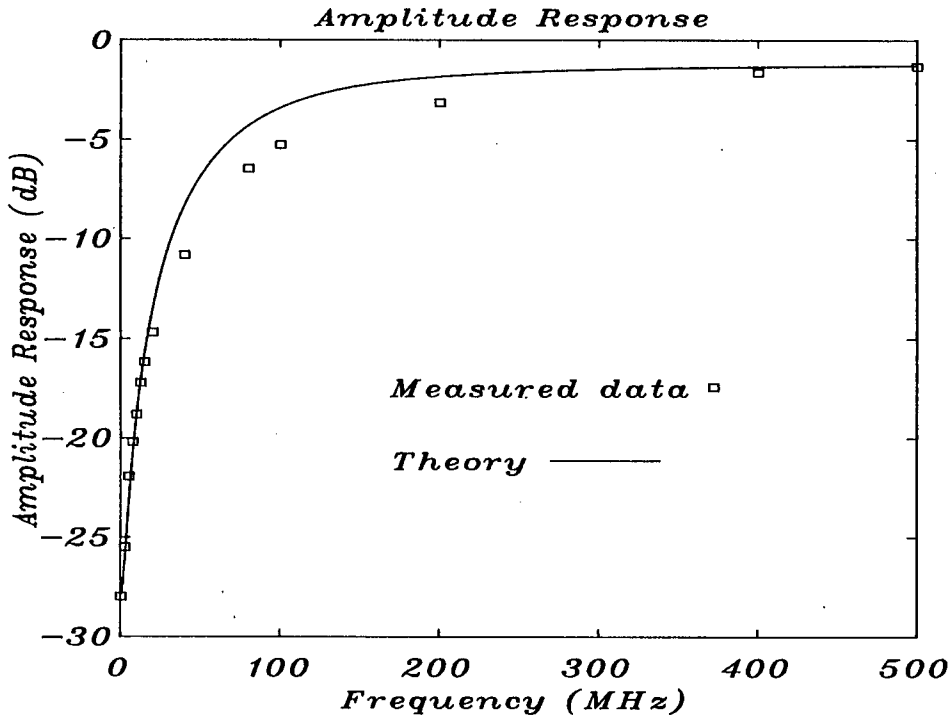

Figure 3.12: The theoretical amplitude response of the cermet/GaAs test circuit for frequencies lying between dc and 500 MHz.

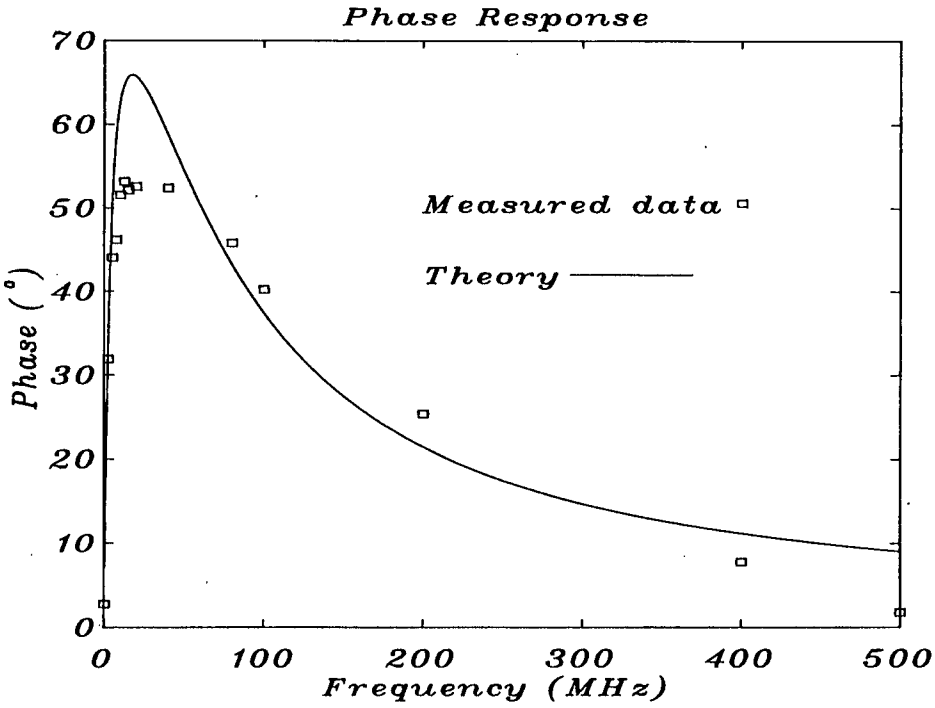

Figure 3.13: The theoretical phase response of the cermet/GaAs test circuit for frequencies lying between dc and 500 MHz.

Chapter 4

Two-dimensional GaAs CMCCD Model

4.1 Geometric Representation

The unit cell for the 4-phase GaAs CMCCD model shown in Figure 4.1 consists of a two-dimensional slice through a single pixel. The slice is assumed to lie on a plane coincident with the central axis of the CMCCD so that the potential and the charge density are considered invariant along the axis normal to this plane. Cartesian coordinate axes are defined as indicated, with the origin located at the intersection between the upper boundary segment and the left-hand boundary segment.

The unit cell occupies a domain comprised of two subdomains: the active layer subdomain ($0 \leq x \leq x_{int}, 0 \leq y \leq y_{max}$) and the semi-insulating substrate subdomain ($x_{int} \leq x \leq x_{max}, 0 \leq y \leq y_{max}$). Along the intersection of the two subdomains at $x = x_{int}$ is an internal boundary segment. The upper boundary segment at $x = 0$ consists of the union of two boundary segment sets. The first set includes the four transport electrode boundary segments and the second set consists of the five cermet/GaAs junction boundary segments. The lengths used in the computer model are listed in Table III.

4.2 Device Equations

The equations used to describe the variation of both the potential and the electron density in nondegenerate n-type GaAs are [33]:

$$\nabla^2 u(x,y) = \sigma[\bar{n}(x,y) - \bar{N}_D] \quad , \tag{4.1}$$

$$J(x,y) = qn_i U_T \mu(x,y)[\nabla \bar{n}(x,y) + \bar{n}(x,y)E(x,y)] \tag{4.2}$$

and

$$\frac{\partial \bar{n}(x,y)}{\partial t} = \frac{1}{qn_i} \nabla \cdot J(x,y) \tag{4.3}$$

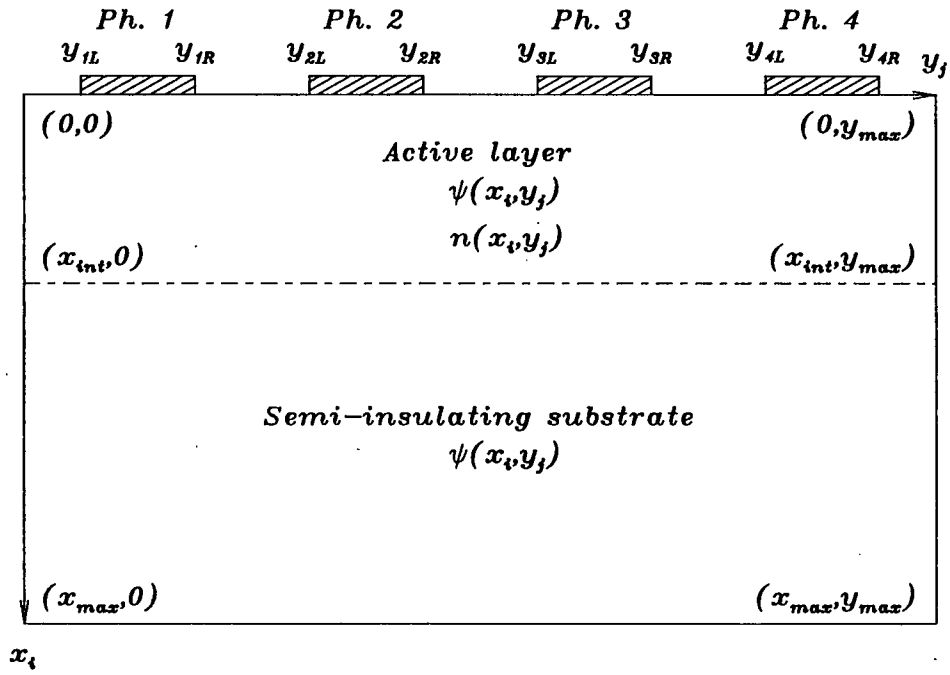

Figure 4.1: The unit cell for modeling the GaAs CMCCD.

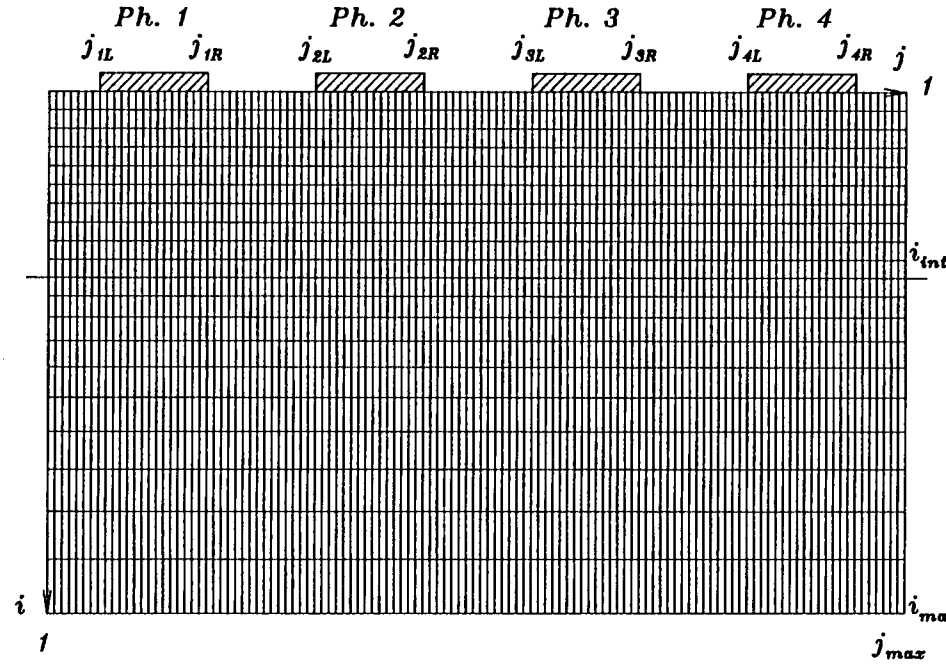

Figure 4.2: The main finite difference for the GaAs CMCCD model.

Parameter	Value
x_{int}	0.25 μm
$x_{max} - x_{int}$	100 μm
y_{max}	23.8 μm
$y_{mR} - y_{mL}$	3.0 μm for $m = 1, \ldots, 4$
y_{1L}	1.4 μm
$y_{max} - y_{4R}$	1.4 μm
$y_{(m+1)L} - y_{mR}$	3.0 μm for $m = 1, 2, 3$

Table III: The lengths used in the two-dimensional computer model.

where n_i is the intrinsic carrier density of GaAs, $\bar{N}_D = N_D/n_i$ is the normalized donor density, $\bar{n}(x,y) = n(x,y)/n_i$ is the normalized electron density, $u(x,y) = \psi(x,y)/U_T$ is the normalized potential, $E(x,y) = -\nabla u(x,y)$ is the normalized electric field, $J(x,y)$ is the electron current density and $\sigma = qn_i/\epsilon U_T$ is a constant. The minority carriers and the electron generation/recombination processes within the active layer are neglected in the model.

4.3 Finite Difference Grid and the Computational Kernel

The model equations 4.1,...,4.3 are discretized on a finite difference grid superimposed onto the unit cell. The potential is computed at each main grid point lying within the unit cell, while the electron density is computed at each main grid point lying within the active layer subdomain. An auxiliary grid is interleaved with the main grid lying within the active layer subdomain, on which, the intermediate calculation of the electron current density is made. The auxiliary grid points are located at the midpoints of the main grid intervals. The main grid layout within the unit cell is shown in Figure 4.2.

The main grid is composed of 21 by 120 grid points with $1 \leq i \leq i_{max} = 21$ and $1 \leq j \leq j_{max} = 120$. The grid spacing along the i-axis is uniform within the active layer interval $1 \leq i \leq i_{int} = 11$ and is nonuniform within the semi-insulating substrate

interval $i_{int} \leq i \leq i_{max}$. A uniform grid spacing is maintained along the j-axis of the unit cell. The auxiliary grid within the active layer subdomain is shifted from the main grid as described above with $(i_{aux}, j_{aux}) = (i + \frac{1}{2}, j + \frac{1}{2})$.

The grid spacings $\delta x_i = x_{i+1} - x_i$ and $\delta y = y_{j+1} - y_j$ within the unit cell are determined from the geometry of the unit cell and the number of grid points lying within the region of interest. The constant grid spacing along the i-axis within the active layer subdomain is

$$\delta x_i = \delta x_a = \frac{x_{int}}{i_{int} - 1} = 0.025 \text{ microns for } 1 \leq i \leq i_{int} - 1 \quad . \tag{4.4}$$

Within the semi-insulating substrate subdomain the grid spacing along the i-axis is nonuniform and is defined using a finite geometric series

$$\delta x_i = \delta x_a r^{i - i_{int}} \quad \text{for } i_{int} \leq i \leq i_{max} - 1 \tag{4.5}$$

where r is a constant determined from the summation

$$x_{max} - x_{int} = \sum_{i=i_{int}}^{i_{max}-1} \delta x_i = \frac{(1 - r^{i_{max} - i_{int}})\delta x_a}{1 - r} \quad . \tag{4.6}$$

The value of the constant r is 2.364316 for $\delta x_a = 0.025$ microns and $x_{max} - x_{int} = 100$ microns. The uniform grid spacing along the j-axis within the unit cell is

$$\delta y = \frac{y_{max}}{j_{max} - 1} = 0.2 \text{ microns for } 1 \leq i \leq j_{max} - 1 \quad . \tag{4.7}$$

The potential or the electron density at each grid point (i, j) is evaluated using the discrete nine-point computational kernel shown in Figure 4.3. The potential and the electron density are associated with the five main grid points and the components of the electron current density are coupled with the four auxiliary grid points.

4.4 Finite Difference Equations for $u(x, y)$

The generalized two-variable Taylor series for the dimensionless potential $u(x, y)$ near the point (x_i, y_j) is

$$u(x_i \pm \delta x, y_j \pm \delta y) \;=\; u(x, y)|_{(x_i, y_j)} + \left(\pm \delta x \frac{\partial}{\partial x} \pm \delta y \frac{\partial}{\partial y} \right) u(x, y)|_{(x_i, y_j)}$$

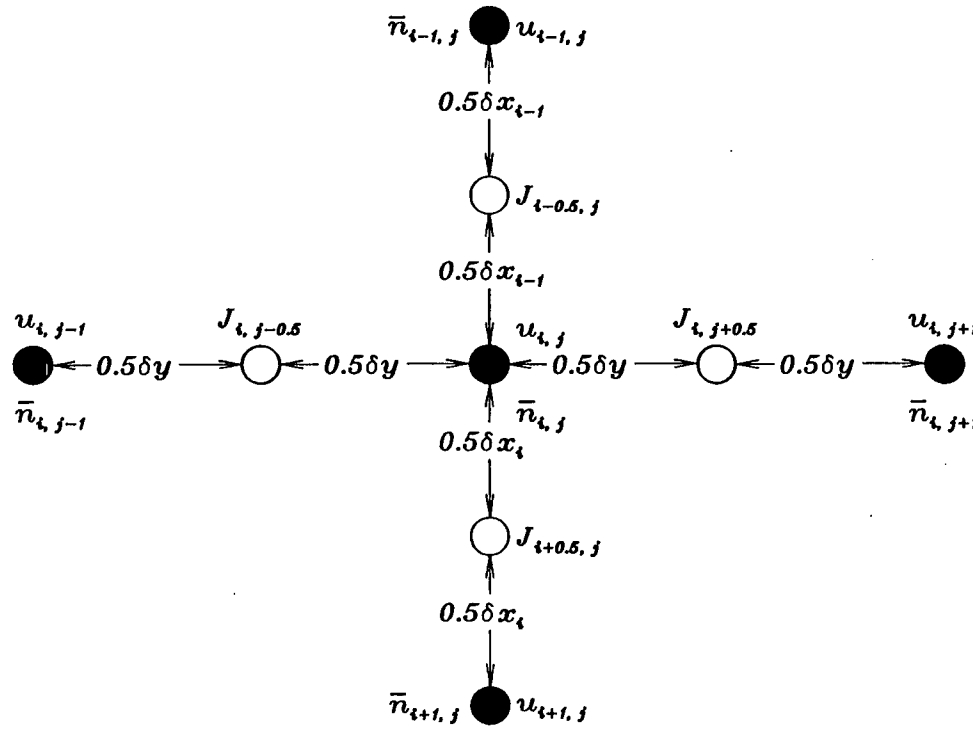

Figure 4.3: The nine-point computational kernel used in the calculation of the potential or the electron density within the unit cell. The five disks represent the main grid points and the four circles denote the interleaved auxiliary grid points.

$$+ \quad \frac{1}{2!}\left(\pm\delta x\frac{\partial}{\partial x} \pm \delta y\frac{\partial}{\partial y}\right)^2 u(x,y)|_{(x_i,y_j)} + \cdots$$
$$+ \quad \frac{1}{m!}\left(\pm\delta x\frac{\partial}{\partial x} \pm \delta y\frac{\partial}{\partial y}\right)^m u(x,y)|_{(x_i,y_j)} + \cdots \qquad (4.8)$$

where $+\delta x = \delta x_i$, $-\delta x = \delta x_{i-1}$ and m is an integer variable. Applying equation 4.8 to each of the four main grid points surrounding the central point of the computational kernel and neglecting third and higher order terms of the resulting Taylor series yields the following set of four equations:

$$u_{i-1,j} = u_{i,j} - \delta x_{i-1}\frac{\partial}{\partial x}u_{i,j} + \frac{\delta x_{i-1}^2}{2}\frac{\partial^2}{\partial^2 x}u_{i,j} \quad , \qquad (4.9)$$

$$u_{i,j-1} = u_{i,j} - \delta y\frac{\partial}{\partial y}u_{i,j} + \frac{\delta y^2}{2}\frac{\partial^2}{\partial^2 y}u_{i,j} \quad , \qquad (4.10)$$

$$u_{i,j+1} = u_{i,j} + \delta y\frac{\partial}{\partial y}u_{i,j} + \frac{\delta y^2}{2}\frac{\partial^2}{\partial^2 y}u_{i,j} \quad , \qquad (4.11)$$

$$u_{i+1,j} = u_{i,j} + \delta x_i\frac{\partial}{\partial x}u_{i,j} + \frac{\delta x_i^2}{2}\frac{\partial^2}{\partial^2 x}u_{i,j} \qquad (4.12)$$

where the shorthand notation $u_{i,j} \equiv u(x,y)|_{(x_i,y_j)}$ is used. Adding equation 4.9 to equation 4.12 gives

$$\frac{\partial^2}{\partial^2 x}u_{i,j} = \frac{2}{\delta x_{i-1}+\delta x_i}\left[\frac{1}{\delta x_{i-1}}u_{i-1,j} - \left(\frac{\delta x_{i-1}+\delta x_i}{\delta x_{i-1}\delta x_i}\right)u_{i,j} + \frac{1}{\delta x_i}u_{i+1,j}\right] \tag{4.13}$$

and similarly, adding equation 4.10 to equation 4.11 yields

$$\frac{\partial^2}{\partial^2 y}u_{i,j} = \frac{1}{\delta^2 y}\left(u_{i,j-1} - 2u_{i,j} + u_{i,j+1}\right) \quad . \tag{4.14}$$

The sum of equation 4.13 and equation 4.14 produces the finite difference equation for the Laplacian of the potential $u_{i,j}$

$$\begin{aligned}\nabla^2 u_{i,j} &= \frac{2}{\delta x_{i-1}(\delta x_{i-1}+\delta x_i)}u_{i-1,j} + \frac{1}{\delta^2 y}u_{i,j-1} - \left(\frac{2}{\delta x_{i-1}\delta x_i} + \frac{2}{\delta^2 y}\right)u_{i,j} \\ &+ \frac{1}{\delta^2 y}u_{i,j+1} + \frac{2}{\delta x_i(\delta x_{i-1}+\delta x_i)}u_{i+1,j} \quad .\end{aligned} \tag{4.15}$$

Equation 4.15 can be simplified when the point (i,j) resides within the active layer subdomain. Recall that the grid spacing along the i-axis within the active layer subdomain is a constant, as defined by equation 4.4. Hence, equation 4.15 reduces to

$$\nabla^2 u_{i,j} = \frac{1}{\delta^2 x_a}u_{i-1,j} + \frac{1}{\delta^2 y}u_{i,j-1} - \frac{2(\delta^2 x_a + \delta^2 y)}{\delta^2 x_a \delta^2 y}u_{i,j} + \frac{1}{\delta^2 y}u_{i,j+1} + \frac{1}{\delta^2 x_a}u_{i+1,j} \quad . \tag{4.16}$$

The discretization of the Poisson equation 4.1 within the active layer subdomain is obtained using equation 4.16

$$\begin{aligned}\sigma(\bar{n}_{i,j} - \bar{N}_D) &= \frac{1}{\delta^2 x_a}u_{i-1,j} + \frac{1}{\delta^2 y}u_{i,j-1} \\ &- \frac{2(\delta^2 x_a + \delta^2 y)}{\delta^2 x_a \delta^2 y}u_{i,j} + \frac{1}{\delta^2 y}u_{i,j+1} + \frac{1}{\delta^2 x_a}u_{i+1,j}\end{aligned} \tag{4.17}$$

and within the semi-insulating substrate subdomain using equation 4.15

$$\begin{aligned}0 &= \frac{2}{\delta x_{i-1}(\delta x_{i-1}+\delta x_i)}u_{i-1,j} + \frac{1}{\delta^2 y}u_{i,j-1} \\ &- \left(\frac{2}{\delta x_{i-1}\delta x_i} + \frac{2}{\delta^2 y}\right)u_{i,j} + \frac{1}{\delta^2 y}u_{i,j+1} + \frac{2}{\delta x_i(\delta x_{i-1}+\delta x_i)}u_{i+1,j}\end{aligned} \tag{4.18}$$

where it is assumed that no charge is present within this region.

4.5 Boundary Conditions for $u(x, y)$

The boundary conditions for the potential $u_{i,j}$ are an extension of the one-dimensional boundary conditions described in Chapter 2. The normalized reference potential along the lower boundary segment at $i = i_{max}$ is assigned a value of zero

$$u_{i_{max},j} = 0 \quad . \tag{4.19}$$

The unit cell is considered to be part of a repetitive structure resulting in a periodic boundary condition for the potential that is described by the following two equations

$$u_{i,0} = u_{i,j_{max}} \tag{4.20}$$

and

$$u_{i,j_{max}+1} = u_{i,1} \quad . \tag{4.21}$$

The potential along the internal boundary segment at $i = i_{int}$ is continuous and satisfies Gauss's law

$$\frac{\partial}{\partial x} u_{i_{int}^+,j} - \frac{\partial}{\partial x} u_{i_{int}^-,j} = \frac{Q_{int,j}}{\epsilon} = 0 \tag{4.22}$$

where the interface charge density $Q_{int,j}$ is assumed to be zero. From equations 4.1, 4.9, 4.14 and noting that $\delta x_{i_{int}-1} = \delta x_{i_{int}} = \delta x_a$ obtain

$$\begin{aligned} \frac{\partial}{\partial x} u_{i_{int}^-,j} &= \frac{\delta x_a}{2} \left[\sigma(\bar{n}_{i_{int},j} - \bar{N}_D) - \frac{2}{\delta^2 x_a} u_{i_{int}-1,j} \right. \\ &- \left. \frac{1}{\delta^2 y} u_{i_{int},j-1} + \frac{2(\delta^2 x_a + \delta^2 y)}{\delta^2 x_a \delta^2 y} u_{i_{int},j} - \frac{1}{\delta^2 y} u_{i_{int},j+1} \right] \quad . \end{aligned} \tag{4.23}$$

Similarly, equation 4.1 with the right-hand side set to zero, equation 4.12 and equation 4.14 yield

$$\frac{\partial}{\partial x} u_{i_{int}^+,j} = \frac{\delta x_a}{2} \left[\frac{1}{\delta^2 y} u_{i_{int},j-1} - \frac{2(\delta^2 x_a + \delta^2 y)}{\delta^2 x_a \delta^2 y} u_{i_{int},j} + \frac{1}{\delta^2 y} u_{i_{int},j+1} + \frac{2}{\delta^2 x_a} u_{i_{int}+1,j} \right] \quad . \tag{4.24}$$

Substituting equation 4.23 and equation 4.24 into equation 4.22 gives

$$\begin{aligned}\frac{\sigma}{2}\left(\bar{n}_{i_{int},j}-\bar{N}_D\right) &= \frac{1}{\delta^2 x_a}u_{i_{int-1},j}+\frac{1}{\delta^2 y}u_{i_{int},j-1} \\ &- \frac{2(\delta^2 x_a+\delta^2 y)}{\delta^2 x_a \delta^2 y}u_{i_{int},j}+\frac{1}{\delta^2 y}u_{i_{int},j+1}+\frac{1}{\delta^2 x_a}u_{i_{int+1},j} \quad . \end{aligned} \tag{4.25}$$

The potential along a transport electrode boundary segment along the upper boundary segment at $i = 1$ is defined as

$$u_0 = \frac{1}{U_T}\left[V_g - (\phi_{BM,0} - \phi_{BM,x_{max}})\right] \quad . \tag{4.26}$$

The potential along an interelectrode gap boundary segment along the upper boundary segment at $i = 1$ is approximated as a linear function of the voltages applied to the two adjacent transport electrodes, which is consistent with the cermet/GaAs junction theory presented in Chapter 3. The potential along a gap boundary segment is

$$u_{gap} = \frac{1}{U_T}\left[V_{g,left} + \delta j_{gap} V_{gap} - (\phi_{BC} - \phi_{BM,x_{max}})\right] \tag{4.27}$$

where $V_{g,left}$ is the potential of the transport electrode to the immediate left of the gap, V_{gap} is the potential difference across the gap relative to this electrode and $0 < \delta j_{gap} < 1$ is the relative position along the gap.

4.6 Finite Difference Equation for $J(x, y)$

The Scharfetter-Gummel (SG) method [34,35] is used for discretizing the electron current density equation 4.2. To illustrate this method, the positive x-component of the current density $J_{i+\frac{1}{2},j}$ will be determined.

The x-component of the electron current density at a point (x, y) using equation 4.2 is

$$J^x(x,y) = qn_i U_T \mu^x(x,y)\left[\frac{\partial}{\partial x}\bar{n}(x,y) + \bar{n}(x,y)E^x(x,y)\right] \tag{4.28}$$

where the superscript x denotes the x-component of the variable. Rearranging equation 4.28 results in a first order differential equation for the electron density

$$\frac{\partial}{\partial x}\bar{n}(x,y) - a\bar{n}(x,y) - b = 0 \tag{4.29}$$

where $a = -E^x(x,y)$ and $b = J^x(x,y)/qn_iU_T\mu^x(x,y)$. The Scharfetter-Gummel method assumes that the electron current density and the electric field within the semiconductor vary more slowly than the electron density and consequently can be approximated as local constants. This approximation enables equation 4.29 to be solved analytically using an integrating factor $\exp[-a(x-x_i)]$ to give

$$\bar{n}(x,y) = \frac{b}{a}\left(\exp\left[a(x-x_i)\right] - 1\right) + \bar{n}(x_i,y)\exp\left[a(x-x_i)\right] \tag{4.30}$$

where $\bar{n}(x_i,y)$ is the initial condition. Assigning $\bar{n}(x_i,y) = \bar{n}_{i,j}$, fixing $x = x_i + \delta x_a$ and setting $\bar{n}(x_i+\delta x_a, y) = \bar{n}_{i+1,j}$ yields

$$\begin{aligned} J_{i+\frac{1}{2},j} &= 0.5qn_iU_T\mu_{i+\frac{1}{2},j}\left[E_{i+\frac{1}{2},j}\coth(0.5E_{i+\frac{1}{2},j}\delta x_a)(\bar{n}_{i+1,j} - \bar{n}_{i,j})\right. \\ &+ \left.(\bar{n}_{i+1,j} + \bar{n}_{i,j})E_{i+\frac{1}{2},j}\right] \end{aligned} \tag{4.31}$$

where the x-components of the electron current density, the electric field and the electron drift mobility are computed at the auxiliary grid point $(i+\frac{1}{2}, j)$. Similar finite difference equations are obtained for the three remaining components of the electron current density surrounding the point (i,j)

$$\begin{aligned} J_{i-\frac{1}{2},j} &= 0.5qn_iU_T\mu_{i-\frac{1}{2},j}[E_{i-\frac{1}{2},j}\coth(0.5E_{i-\frac{1}{2},j}\delta x_a)(\bar{n}_{i,j} - \bar{n}_{i-1,j}) \\ &+ (\bar{n}_{i-1,j} + \bar{n}_{i,j})E_{i-\frac{1}{2},j}] \quad , \end{aligned} \tag{4.32}$$

$$\begin{aligned} J_{i,j-\frac{1}{2}} &= 0.5qn_iU_T\mu_{i,j-\frac{1}{2}}[E_{i,j-\frac{1}{2}}\coth(0.5E_{i,j-\frac{1}{2}}\delta y)(\bar{n}_{i,j} - \bar{n}_{i,j-1}) \\ &+ (\bar{n}_{i,j-1} + \bar{n}_{i,j})E_{i,j-\frac{1}{2}}] \quad , \end{aligned} \tag{4.33}$$

$$\begin{aligned} J_{i,j+\frac{1}{2}} &= 0.5qn_iU_T\mu_{i,j+\frac{1}{2}}[E_{i,j+\frac{1}{2}}\coth(0.5E_{i,j+\frac{1}{2}}\delta y)(\bar{n}_{i,j+1} - \bar{n}_{i,j}) \\ &+ (\bar{n}_{i,j+1} + \bar{n}_{i,j})E_{i,j+\frac{1}{2}}] \quad . \end{aligned} \tag{4.34}$$

4.7 Discretization of the Continuity Equation

The electron continuity equation 4.3 is descretized using the Crank-Nicolson equation [36]

$$\frac{\bar{n}_{i,j,k+1} - \bar{n}_{i,j,k}}{\delta t} = \frac{1}{2}\left[\frac{\partial}{\partial t}\bar{n}(x_i,y_j,t_{k+1}) + \frac{\partial}{\partial t}\bar{n}(x_i,y_j,t_k)\right]$$

$$= \frac{1}{2qn_i}(\nabla \cdot J_{i,j,k+1} + \nabla \cdot J_{i,j,k}) \tag{4.35}$$

where δt is the time increment and the subscript k is the discrete time-step. The spatial derivatives on the right-hand side of equation 4.35 are discretized using central differences of the form

$$\nabla \cdot J_{i,j} = \frac{J_{i+\frac{1}{2},j} - J_{i-\frac{1}{2},j}}{\delta x_a} + \frac{J_{i,j+\frac{1}{2}} - J_{i,j-\frac{1}{2}}}{\delta y} \tag{4.36}$$

Substituting equations 4.31,...,4.34 into equation 4.36 yields

$$\begin{aligned}
\frac{2}{qn_i}\nabla \cdot J_{i,j} &= \left(\frac{\upsilon_{i-\frac{1}{2},j} - \nu_{i-\frac{1}{2},j}}{\delta x_a}\right)\bar{n}_{i-1,j} + \left(\frac{\upsilon_{i,j-\frac{1}{2}} - \nu_{i,j-\frac{1}{2}}}{\delta y}\right)\bar{n}_{i,j-1} \\
&+ \left(\frac{-\upsilon_{i-\frac{1}{2},j} - \nu_{i-\frac{1}{2},j} - \upsilon_{i+\frac{1}{2},j} + \nu_{i+\frac{1}{2},j}}{\delta x_a}\right. \\
&+ \left.\frac{-\upsilon_{i,j-\frac{1}{2}} - \nu_{i,j-\frac{1}{2}} - \upsilon_{i,j+\frac{1}{2}} + \nu_{i,j+\frac{1}{2}}}{\delta y}\right)\bar{n}_{i,j} \\
&+ \left(\frac{\upsilon_{i,j+\frac{1}{2}} + \nu_{i,j+\frac{1}{2}}}{\delta y}\right)\bar{n}_{i,j+1} + \left(\frac{\upsilon_{i+\frac{1}{2},j} + \nu_{i+\frac{1}{2},j}}{\delta x_a}\right)\bar{n}_{i+1,j}
\end{aligned} \tag{4.37}$$

where $\nu = \mu U_T E$ is the nonlinear electron drift velocity of GaAs and $\upsilon = \nu \coth(0.5E\delta x_a)$. A finite difference equation for the electron density at the point (i,j) for the $k+1^{st}$ time-step is obtained upon substituting equation 4.37 into equation 4.35 to give

$$\begin{aligned}
0 &= \left(\frac{\upsilon_{i-\frac{1}{2},j,k+1} - \nu_{i-\frac{1}{2},j,k+1}}{\delta x_a}\right)\bar{n}_{i-1,j,k+1} + \left(\frac{\upsilon_{i,j-\frac{1}{2},k+1} - \nu_{i,j-\frac{1}{2},k+1}}{\delta y}\right)\bar{n}_{i,j-1,k+1} \\
&+ \left(\frac{-\upsilon_{i-\frac{1}{2},j,k+1} - \nu_{i-\frac{1}{2},j,k+1} - \upsilon_{i+\frac{1}{2},j,k+1} + \nu_{i+\frac{1}{2},j,k+1}}{\delta x_a}\right. \\
&+ \left.\frac{-\upsilon_{i,j-\frac{1}{2},k+1} - \nu_{i,j-\frac{1}{2},k+1} - \upsilon_{i,j+\frac{1}{2},k+1} + \nu_{i,j+\frac{1}{2},k+1}}{\delta y} - \frac{4}{\delta t}\right)\bar{n}_{i,j,k+1} \\
&+ \left(\frac{\upsilon_{i,j+\frac{1}{2},k+1} + \nu_{i,j+\frac{1}{2},k+1}}{\delta y}\right)\bar{n}_{i,j+1,k+1} + \left(\frac{\upsilon_{i+\frac{1}{2},j,k+1} + \nu_{i+\frac{1}{2},j,k+1}}{\delta x_a}\right)\bar{n}_{i+1,j,k+1} \\
&+ \nabla \cdot J_{i,j,k} + \frac{4}{\delta t}\bar{n}_{i,j,k} \quad .
\end{aligned} \tag{4.38}$$

The electron drift velocity of GaAs is a nonlinear function of the electric field strength. To incorporate this into the model, the empirical relationship between the

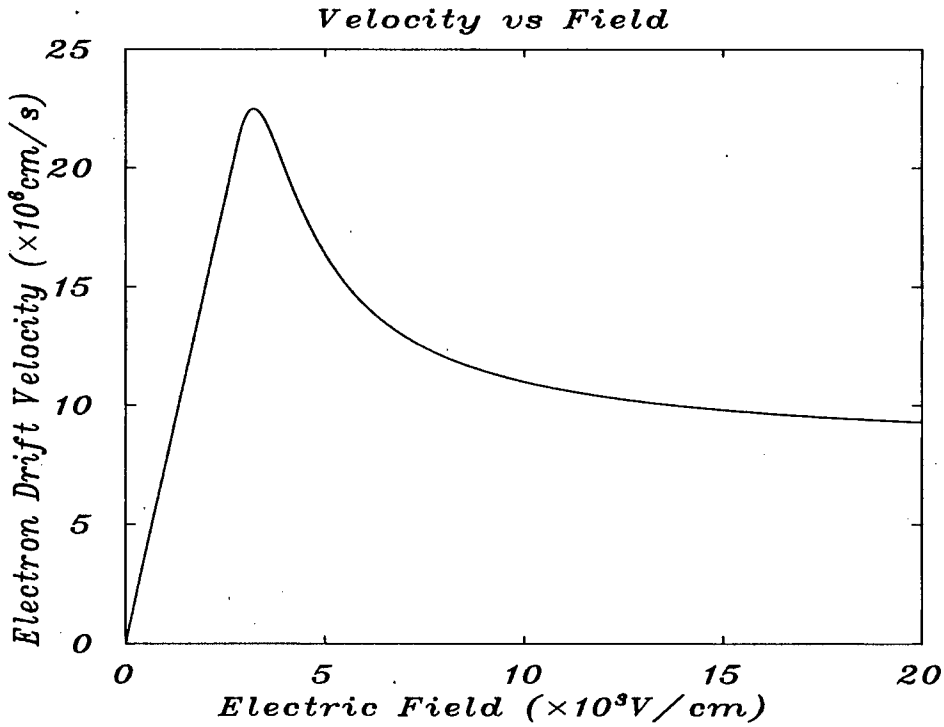

Figure 4.4: The nonlinear electron velocity-field characteristic of GaAs obtained from the empirical equation 4.39, developed by Chang and Fetterman [37].

electron velocity and the electric field strength developed by Chang and Fetterman is used [37]

$$\nu = \frac{\mu_0 U_T E}{\sqrt{1 + (|U_T E| - E_0)^2 E_C^{-2} u(|U_T E| - E_0)}} \tag{4.39}$$

where $u(|U_T E| - E_0)$ is a unit step function equal to zero for $|U_T E| < E_0$. The remaining constants are: $\mu_0 = 7500$ cm^2/V-sec, $E_0 = 2800$ V/cm and $E_C = 1100$ V/cm. The nonlinear electron velocity-field characteristic obtained from this equation is shown in Figure 4.4.

4.8 Boundary Conditions for $n(x, y)$

The electron density along the upper boundary segment at $i = 1$ is assumed to be equal to the equilibrium electron density at the surface neglecting Schottky barrier height lowering. For the metal/GaAs junction the electron density is

$$\bar{n}_0 = \frac{N_C}{n_i} \exp\left(-\frac{\phi_{BM,0}}{U_T}\right) \tag{4.40}$$

and for the cermet/GaAs junction the electron density is

$$\bar{n}_{gap} = \frac{N_C}{n_i} \exp\left(-\frac{\phi_{BC}}{U_T}\right) \tag{4.41}$$

where N_C is the effective density of states within the conduction band of GaAs. The periodic boundary condition for the electron density is described by the following two equations

$$\bar{n}_{i,0} = \bar{n}_{i,j_{max}} \tag{4.42}$$

and

$$\bar{n}_{i,j_{max}+1} = \bar{n}_{i,1} \tag{4.43}$$

for $1 \leq i \leq i_{int}$. The electron density along the internal boundary segment at $i = i_{int}$ is assumed to be equal to the equilibrium electron density along this boundary

$$\bar{n}_{i_{int},j} = \exp\left(u_{i_{int},j} - \delta u_{i_{max}}\right) \tag{4.44}$$

where $\delta u_{i_{max}}$ is the normalized potential difference between the Fermi level and the intrinsic energy level along the bottom of the substrate at $i = i_{max}$.

4.9 Numerical Solution of the Difference Equations

Newton iteration with successive relaxation [20,38,39,40] is used for solving the CMCCD model equations summarized in Table IV. The finite difference equations summarized in this table are expressed as the sum of two functions

$$f^l_{k+1} = g(\zeta^l_{i-1,j,k+1}, \zeta^l_{i,j-1,k+1}, \zeta^l_{i,j,k+1}, \zeta^l_{i,j+1,k+1}, \zeta^l_{i+1,j,k+1}) + h(\bar{n}_{i,j,k}) = 0 \tag{4.45}$$

where $l = 0, 1, 2, 3, \ldots$ is the iteration counter, ζ represents either the potential u or the electron density $\bar{n}$ and the function h is a constant during the $k + 1^{st}$ time-step. The functions g and h are

$$g = A\zeta^l_{i-1,j,k+1} + B\zeta^l_{i,j-1,k+1} + C\zeta^l_{i,j,k+1} + D\zeta^l_{i,j+1,k+1} + E\zeta^l_{i+1,j,k+1} \tag{4.46}$$

Potential	Electron Density	Region of Application
4.17	4.38	Active layer subdomain
4.18	—	Semi-insulating substrate subdomain
4.19	—	Lower boundary segment
4.20	4.42	Left-hand boundary segment
4.21	4.43	Right-hand boundary segment
4.25	4.44	Internal boundary segment
4.26	4.40	Electrode boundary segments
4.27	4.41	Gap boundary segments

Table IV: A summary of the equations used in the CMCCD model.

and

$$h = F\bar{n}_{i,j,k} + G \tag{4.47}$$

where $A, \ldots, G$ are constants obtained from the finite difference equations. The function f^l_{k+1} defined by equation 4.45 is a function of either the potential u^l_{k+1} or the electron density $\bar{n}^l_{k+1}$ implying that the finite difference equations are decoupled. This enables the potential and the electron density distributions to be computed independently at each discrete time-step. The solution for the potential distribution within the unit cell is iterated first, followed by the iterated solution for the electron density distribution within the active layer subdomain.

The potential distribution at the $k+1^{st}$ time-step within the unit cell is iterated first using the electron density distribution computed at the k^{th} time-step, as the electron density distribution at the $k+1^{st}$ time-step is unavailable. The rate of convergence of the iterates is accelerated if the electron density distribution at the k^{th} time-step is replaced by an estimated distribution for the $k+1^{st}$ time-step. This estimate is obtained using the Boltzmann equation and is

$$\bar{n}^l_{i,j,k+1} \approx e^{u^l_{i,j,k+1} - v_{i,j,k}} = \bar{n}_{i,j,k} e^{-u_{i,j,k}} e^{u^l_{i,j,k+1}} \tag{4.48}$$

where $v_{i,j,k} = \phi_n(x_i, y_j, t_k)/U_T$ is the normalized quasi-Fermi potential for the electrons

within the active layer subdomain. Substituting equation 4.48 into equation 4.47 yields the revised equation for the function h

$$h = F\bar{n}_{i,j,k} \exp[\xi(u^l_{i,j,k+1} - u_{i,j,k})] + G \tag{4.49}$$

where $\xi = 0$ if $\zeta = \bar{n}$ or $\xi = 1$ if $\zeta = u$.

A single Newton iteration step consists of adding a correction factor $\delta\zeta^l_{k+1} = \zeta^{l+1}_{k+1} - \zeta^l_{k+1}$ to each of the unknown variables in equation 4.45 using the following relation described in Appendix C

$$f^l_{k+1} + \delta\zeta^l_{k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{k+1}} = 0 \quad . \tag{4.50}$$

The following expansion is obtained for equation 4.50

$$\begin{aligned} 0 &= f^l_{k+1} + \delta\zeta^l_{i-1,j,k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{i-1,j,k+1}} + \delta\zeta^l_{i,j-1,k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{i,j-1,k+1}} + \delta\zeta^l_{i,j,k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{i,j,k+1}} \\ &+ \delta\zeta^l_{i,j+1,k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{i,j+1,k+1}} + \delta\zeta^l_{i+1,j,k+1} \frac{\partial f^l_{k+1}}{\partial \zeta^l_{i+1,j,k+1}} \quad . \end{aligned} \tag{4.51}$$

Substituting equation 4.45 into equation 4.51 and recalling the definitions for the functions g and h given by equations 4.46 and 4.49 yields the following equation for a single Newton iteration of the variable ζ

$$\begin{aligned} 0 &= A\zeta^{l+1}_{i-1,j,k+1} + B\zeta^{l+1}_{i,j-1,k+1} + \left(C + F\bar{n}_{i,j,k}\xi \exp\left[\xi(u^l_{i,j,k+1} - u_{i,j,k})\right]\right) \zeta^{l+1}_{i,j,k+1} \\ &+ D\zeta^{l+1}_{i,j,k+1} + E\zeta^{l+1}_{i+1,j,k+1} + F\bar{n}_{i,j,k}(1 - \xi\zeta^l_{i,j,k+1}) \exp\left[\xi(u^l_{i,j,k+1} - u_{i,j,k})\right] \\ &+ G \quad . \end{aligned} \tag{4.52}$$

A single Newton iteration step through the matrix of unknowns proceeds in the usual reading order. The rate of convergence of the sequence of iterates is accelerated using successive relaxation. The ordinary iterated solution for $\zeta^{l+1}_{i,j,k+1}$ is obtained from equation 4.52

$$\begin{aligned} \zeta^{l+1}_{i,j,k+1} &= -\left(C + F\bar{n}_{i,j,k}\xi \exp\left[\xi(u^l_{i,j,k+1} - u_{i,j,k})\right]\right)^{-1} \left(A\zeta^{l+1}_{i-1,j,k+1} + B\zeta^{l+1}_{i,j-1,k+1}\right. \\ &+ D\zeta^l_{i,j+1,k+1} + E\zeta^l_{i+1,j,k+1} + F\bar{n}_{i,j,k}(1 - \xi\zeta^l_{i,j,k+1}) \exp\left[\xi(u^l_{i,j,k+1} - u_{i,j,k})\right] \\ &+ \left. G\right) \end{aligned} \tag{4.53}$$

where the most recently iterated values for the variables are used. The accelerated solution ${}^{r}\zeta_{i,j,k+1}^{l+1}$ using successive relaxation is

$$ {}^{r}\zeta_{i,j,k+1}^{l+1} = {}^{r}\zeta_{i,j,k+1}^{l} + w_r \left(\zeta_{i,j,k+1}^{l+1} - {}^{r}\zeta_{i,j,k+1}^{l} \right) \tag{4.54} $$

where w_r is the relaxation parameter defined as

$$ w_r \equiv \begin{cases} 0 < w_r < 1 & \text{for under-relaxation} \\ 1 < w_r < 2 & \text{for over-relaxation} \end{cases} . $$

The ordinary iterated solution is obtained from equation 4.54 if $w_r = 1$.

4.10 Computer Simulations

A flow diagram for a two-dimensional computer simulation is illustrated in Figure 4.5. A simulation begins from an initial guess for the potential and the electron density distributions within the unit cell for the initial bias conditions at $k = 0$. The bias voltages are adjusted, the time-step counter k is incremented by 1 and the simulation proceeds. The potential u at each grid point within the unit cell is iterated until the maximum absolute residual for the potential within the active layer subdomain is less than 0.0005. The electron density at each grid point within the active layer subdomain is subsequently iterated until the maximum relative error for the electron density is less than 0.001. The simulation continues until a stop time k_{max} is reached. This simulation procedure was used to produce the two-dimensional potential and charge density distributions for investigating the maximum frequency of operation and the charge transfer performance of a 4-phase GaAs CMCCD.

The theoretical maximum frequency of operation of a GaAs CMCCD was determined using the single electron transit time model developed by Deyhimy et al [7] and Prokop'ev [41]. The transit time τ required for an electron to travel within the fully depleted active layer between the centers of two adjacent transport electrodes is given by the line integral

$$ \tau = \int_{C_m} \left[\frac{\hat{x}}{\nu^x(x_m(y), y)} + \frac{\hat{y}}{\nu^y(x_m(y), y)} \right] \cdot d\vec{r} \tag{4.55} $$

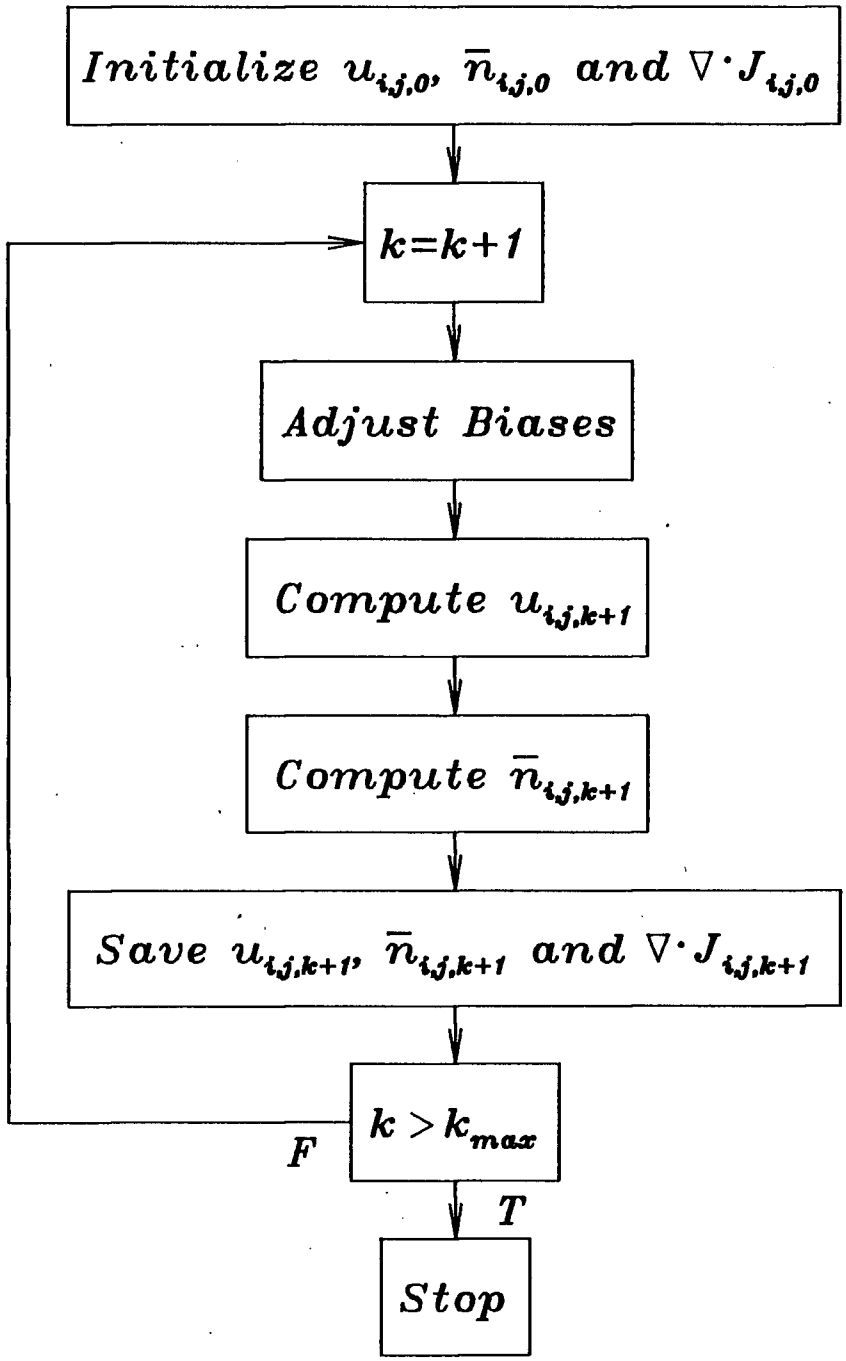

Figure 4.5: The flow diagram for the two-dimensional computer simulations.

where C_m is the curve coinciding with the maximum potential contour between the electrode centers, $\nu^x(x_m(y), y)$ and $\nu^y(x_m(y), y)$ are the x-component and the y-component of the electron velocity vector along this curve, $d\vec{r} = \hat{x}dx + \hat{y}dy$ is the differential contour vector and $x_m(y)$ is the depth of the maximum potential as a function of the position y between the electrode centers. Equation 2.10 is used to determine an approximate value for the depth of the maximum potential. If $w_n = x_{int} = 0.25$ microns, $N_D = 4.5 \cdot 10^{16}$ cm^{-3}, $x_{max} \gg x_{int}$ and $|\psi_0| < 10$ volts then the second and third terms on the right-hand side of equation 2.10 are negligible which gives

$$x_m(y) \approx w_n = x_{int} \tag{4.56}$$

for the depth of the maximum potential between the electrode centers. Substituting equation 4.56 into equation 4.55 yields

$$\tau \approx \int_0^{L_p} \frac{dy}{\nu^y(x_{int}, y)} \tag{4.57}$$

where L_p is the distance between the two adjacent transport electrode centers. The electron transit time is computed with the electron velocity $\nu^y(x_{int}, y)$ described by equation 4.39 with the y-component of the normalized electric field $E^y(x_{int}, y)$ determined from a static two-dimensional potential distribution.

The theoretical maximum frequency of operation f_{max} of a 4-phase GaAs CMCCD is

$$f_{max} = \frac{1}{4\tau} \quad . \tag{4.58}$$

The maximum frequency of operation of a 4-phase GaAs CMCCD as a function of the clock voltage amplitude and the interelectrode gap length for a constant transport electrode pitch L_p is illustrated in Figure 4.6. As indicated in this figure, the maximum frequency of operation of the CMCCD increases with the clock voltage amplitude and with the interelectrode gap length. This relationship is intuitively correct as the electron

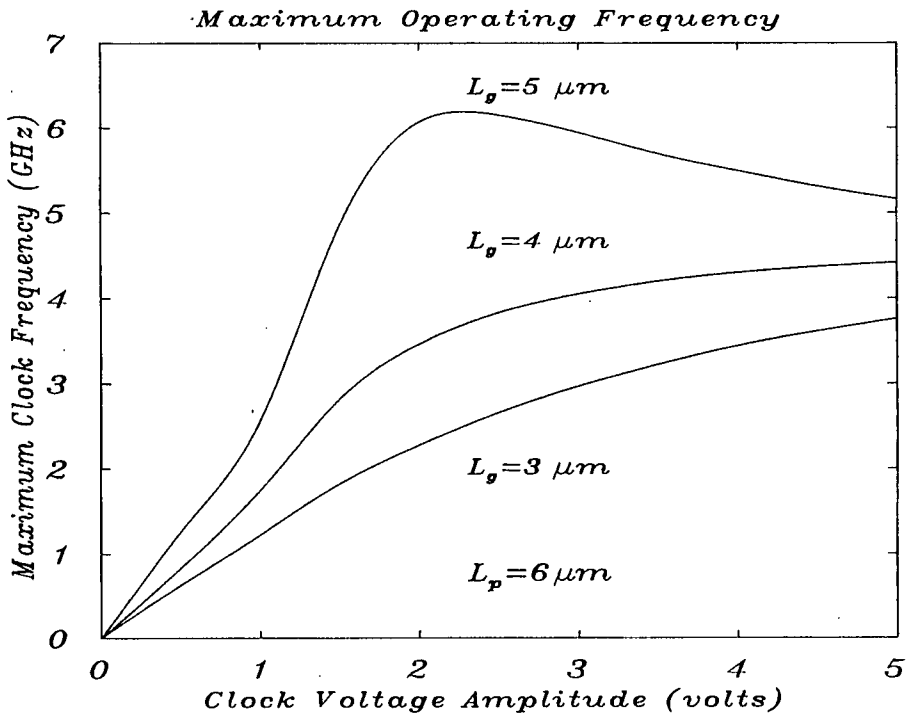

Figure 4.6: The maximum frequency of operation of a GaAs CMCCD as a function of the clock voltage amplitude and the transport electrode length.

transit time is dominated by the time required for the electron to travel through the low-field region underneath the transport electrode. The electron transit time underneath the transport electrode is reduced by increasing the fringing field penetration from the adjacent transport electrode. This is accomplished either by increasing the clock voltage amplitude or by reducing the transport electrode length. It would appear from the above description, that the transport electrodes of a GaAs CMCCD should have a minimum length in order to achieve the maximum operating bandwidth possible for the lowest clock power requirements.

The charge transfer performance of a GaAs CMCCD was investigated in a manner similar to that used by Sodini et al [42]. A simulated single electrode transfer of a half full well charge packet ($Q_s = 0.5 \cdot 10^{-10}$ coul/cm) was performed and is illustrated in Figure 4.7. The charge packet initially resides under the phase one and phase two transport electrodes and is transferred to the region under the phase two and phase

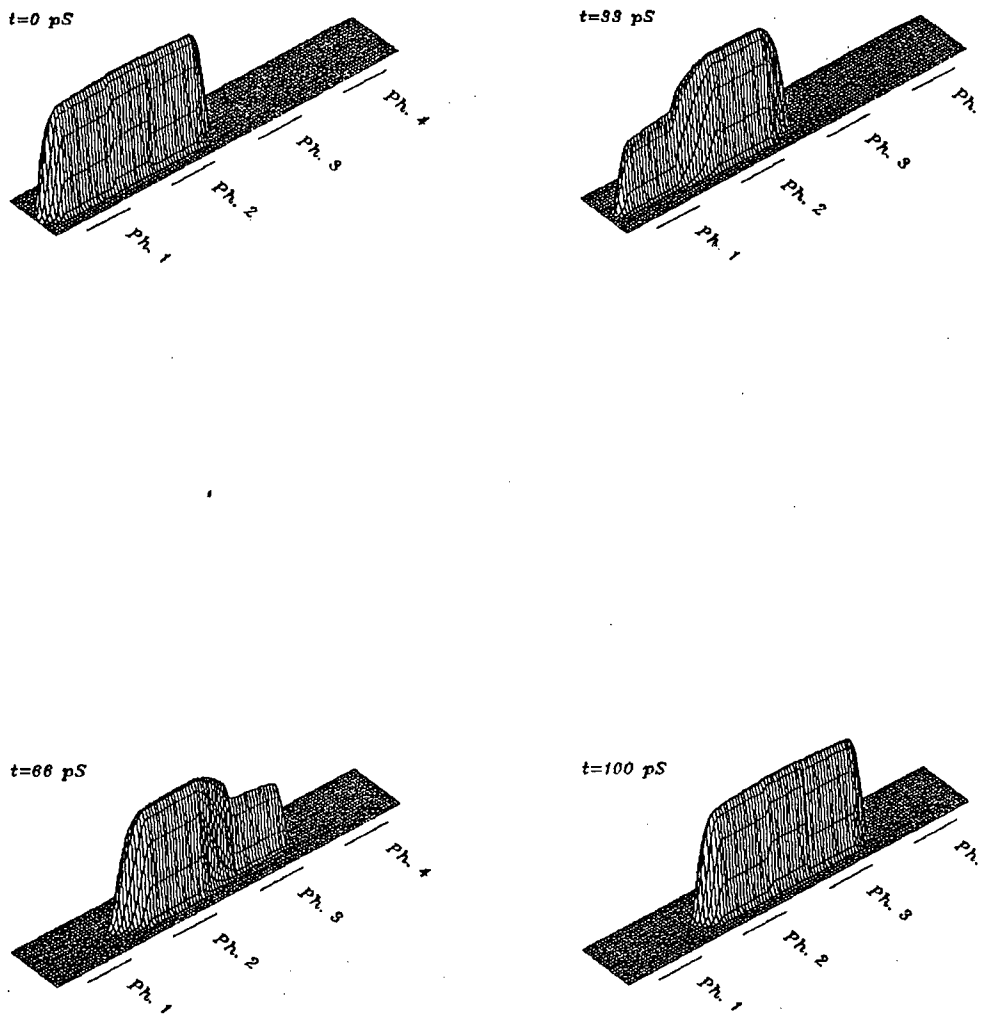

Figure 4.7: The simulated single electrode transfer of a charge packet. The transport electrode length is 3.0 microns.

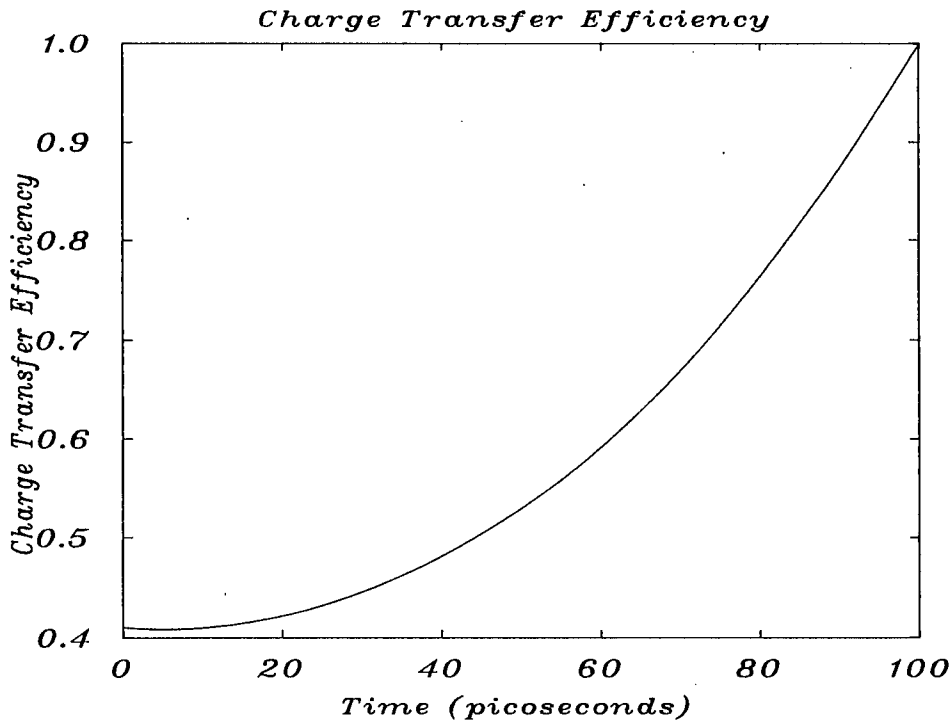

Figure 4.8: The theoretical charge transfer efficiency as a function of time for the GaAs CMCCD obtained from the simulated single electrode transfer of a charge packet.

three transport electrodes. The quadrature clock voltage function consisted of a 2 volt amplitude trapezoidal pulse with 100 picosecond edge transitions. A time increment of $\delta t = 0.1$ picoseconds was used in the simulation.

The theoretical charge transfer efficiency as a function of time for the GaAs CMCCD was obtained from the simulation results. The charge transfer efficiency $\eta(t)$ is defined as the ratio of the charge transferred to the transfer well to the charge initially residing in the storage well. For the simulation of the 4-phase GaAs CMCCD

$$\eta(t) = \frac{Q_{Ph.2+Ph.3}(t)}{Q_{Ph.1+Ph.2}(t=0)} \quad . \tag{4.59}$$

Figure 4.8 illustrates the theoretical charge transfer efficiency of the GaAs CMCCD obtained from the computer simulation described above. This figure indicates that the packet of charge is essentially fully transferred at the completion of the clock transition period $t_{tr} = 100$ picoseconds. This result implies that the simulated transfer of the

charge packet was not transit time limited and that the 4-phase GaAs CMCCD should exhibit good charge transfer at clock frequencies approaching $f_c = 1/4t_{tr} = 2.5$ GHz. Sovero et al [9] measured a charge transfer efficiency of 0.99 per transfer for a GaAs CMCCD operating at a clock frequency of 2.5 GHz, supporting the above theoretical result.

Chapter 5

Device Fabrication

Figure 5.1 shows a microphotograph of a 64-pixel, 4-phase GaAs CMCCD. The input section is located on the left-hand end of the device and is shown in detail in Figure 5.2. The control gates G_1 and G_2 are nominally 5 microns in length and are separated by 2 micron gaps from the input ohmic contact, from the first transport electrode and from each other, respectively. There are 256 transport electrodes comprising the sixty-four pixels within the transport section of the CMCCD. The transport electrodes are 3 microns in length and are separated by 3 micron gaps. The phase one transport electrodes and the phase three transport electrodes are interconnected along the lower side of the device while the phase two transport electrodes and the phase four transport electrodes are interconnected along the upper side of the device. The entire transport section is encapsulated with a cermet film. The output section is located at the right-hand end of the device and is shown in detail in Figure 5.3. The output ohmic contact, the control gate G_3 and the output source follower amplifier comprise this section. The control gate G_3 is 5 microns in length and is separated by 2 micron gaps from the final transport electrode and from the output ohmic contact. The CMCCD channel is nominally 100 microns wide.

The GaAs wafer that was used for producing the CMCCD was an undoped (100) oriented semi-insulating substrate onto which an n-type epitaxial layer was grown. The substrate was grown using the liquid encapsulated Czochralski technique [43] and had a sheet resistivity exceeding 10^7 ohm-cm. Metal-organic chemical vapour phase deposition [44] was used to grow the n-type active layer onto the substrate. This layer consisted of a nominal 1–2 micron thick n^--buffer layer onto which the 0.25 micron n-type active layer was grown. The active layer was uniformly doped, with N_D =

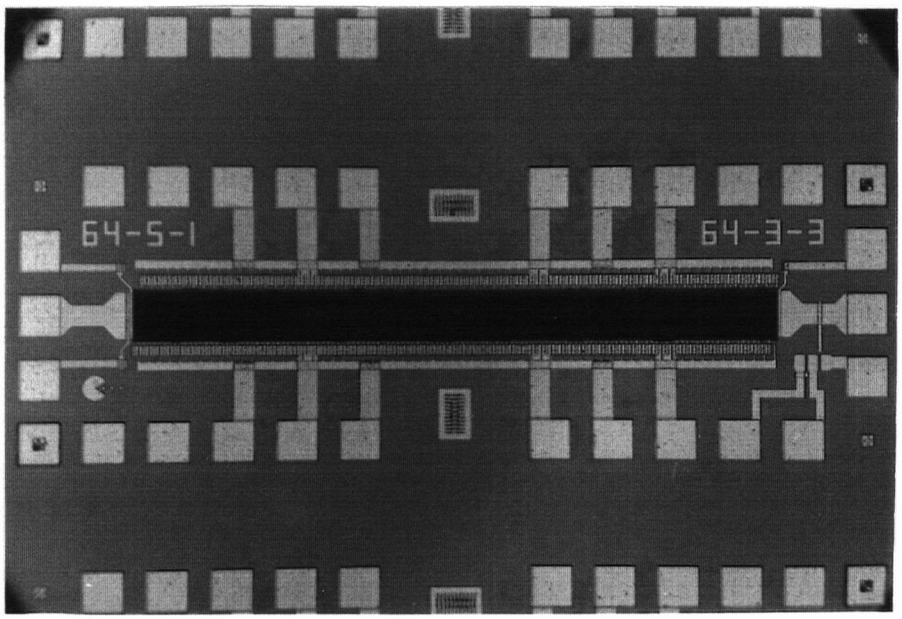

Figure 5.1: A microphotograph of the fabricated GaAs CMCCD. The bonding pads are 100 micron squares.

$4.5 \cdot 10^{16}$ cm^{-3}.

The fabrication of the GaAs CMCCD required six mask levels that employed a 2.0 micron minimum design rule. The mask levels provided the patterns for fabricating the ohmic contacts, the isolated active regions, the metal/GaAs Schottky barriers, the cermet/GaAs Schottky barriers, the interconnect vias and the second level metallization. Conventional contact lithography was used to produce the device. A detailed list of the fabrication steps is described in Appendix D.

The ohmic contacts [45] of the CMCCD and the MESFETs were fabricated initially. A 1.2 micron thick positive photoresist film was patterned onto the wafer surface. A nominal 1200 Å Au-Ge (12 wt. % Ge), 200 Å Ni and 1400 Å Au ohmic contact metallization was sequentially deposited onto the wafer surface using thermal evaporation and electron-beam evaporation in a high vacuum chamber. The unwanted metal was removed from the wafer surface using the photoresist liftoff method [46]. The

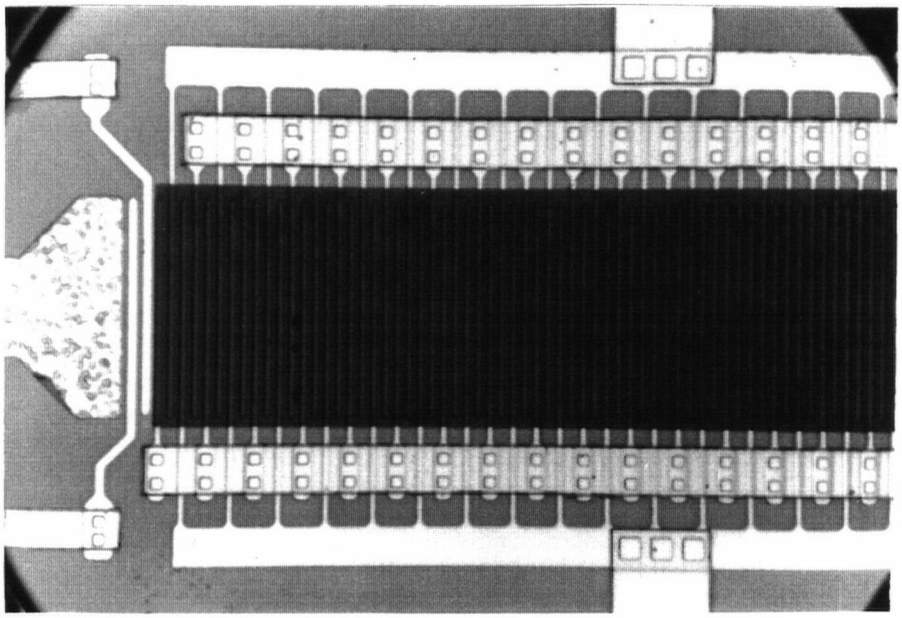

Figure 5.2: A microphotograph of the input section of the GaAs CMCCD.

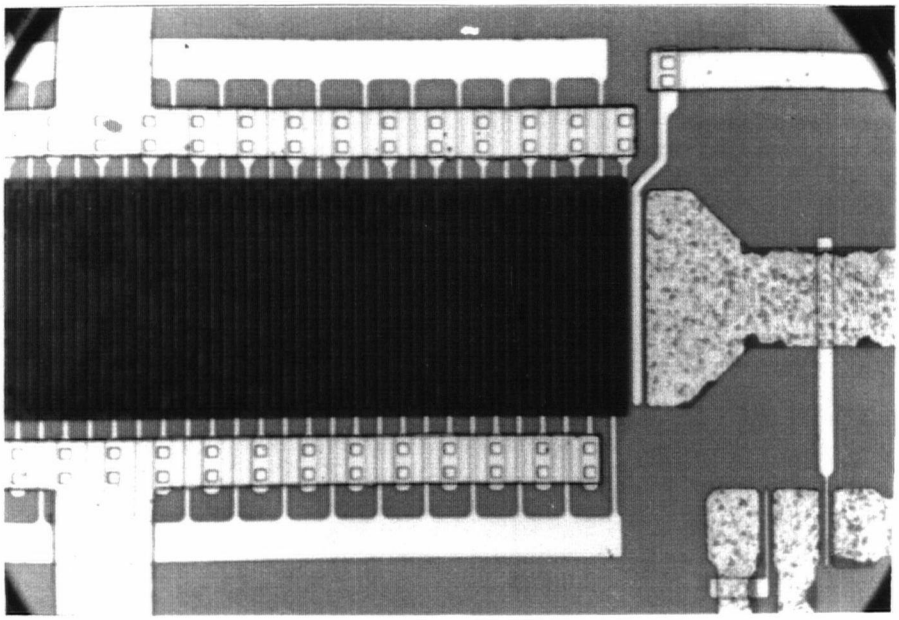

Figure 5.3: A microphotograph of the output section of the GaAs CMCCD.

ohmic contacts were completed by alloying the ohmic contact metallization with the underlying GaAs.

To achieve a planar device structure, multiple energy proton isolation implants were used to isolate the active device regions. Early investigators of the GaAs CGCCD used a mesa etch to achieve the required isolation [47,48]. Although this technique is simple to implement and provides good isolation, it has the drawback that the subsequent lithography is hampered by the different elevations between the mesa plateaus and the surrounding valleys. A planar GaAs CGCCD was realized using Schottky barrier channel stops [49] to isolate the active device regions. A channel stop must completely surround the active device region to be effective, which is a disadvantage as it becomes difficult to run first level metallizations directly between isolated regions. Proton bombardment was used to isolate the active device regions of a GaAs CGCCD [50]. This method has the desirable feature that it does not alter the GaAs surface profile and thus does not have the associated problems of the above isolation techniques.

The active regions for the CMCCD and the MESFETs were electrically isolated using a sequence of three proton implants at different beam energies. A nominal 7 micron thick patterned photoresist film was used as a barrier to protect the active device regions during the implants. The exposed GaAs was sequentially bombarded using protons at ion energies of 180 keV, 90 keV and 30 keV. Fluences of 10^{13} cm^{-2} and $5 \cdot 10^{13}$ cm^{-2} were used for the first two implants and the final implant, respectively. No post-implantation anneal was performed. Good electrical isolation was achieved, with the measured resistivity of the deactivated GaAs exceeding 10^5 ohm-cm.

The metal/GaAs Schottky barriers comprising the transport electrodes and the MESFET gates were patterned using the photoresist liftoff method. A nominal 500 Å Ti, 100 Å Pt and 2150 Å Au multilayer film was sequentially electron beam evaporated onto the wafer surface through a 1.2 micron thick photoresist mask. The

photoresist and the unwanted metallization were removed in an ultrasonic N-methyl-2-pyrrolidone solvent bath.

The cermet/GaAs Schottky barriers within the interelectrode gaps of the CMCCD were patterned using the photoresist liftoff process. A nominal 5000 Å thick film of Cr-SiO (nominal 45 wt. % Cr) was rf diode sputtered from a 6 inch composite target onto the wafer surface through a 2.1 micron thick photoresist mask. The target was separated from the substrate table by 1.5 inches and was sputtered at 13.56 MHz in a 10 mTorr argon environment [51]. The input power to the target was approximately 250 watts rms, achieving a dc target bias of -800 volts relative to the substrate table. It was observed that a target bias of less than -1000 volts was detrimental to the photoresist film. An extended 24 hour chamber preconditioning period was required prior to the 30 minute deposition to achieve a uniform Cr:SiO film. The photoresist and the unwanted cermet film were removed in an ultrasonic N-methyl-2-pyrrolidone solvent bath subsequent to the deposition. Figure 5.4 shows a transmission electron microphotograph of the structure of the Cr:SiO film. The dark areas correspond to the regions of highest atomic density and are believed to be the result of chromium compounds [52]. Energy dispersive x-ray analysis (EDX) was used to ascertain the chemical composition of the film and it was found to be 41.7 weight percent chromium, which is in agreement with the manufacturer's target specification of 45 weight percent chromium.

A 1.8 micron thick interlayer dielectric film of polyimide was used to protect the active GaAs surface and to separate the two metallization levels from each other. A layer of diluted Du Pont PYRALIN PI-2550 polyimide was applied to the GaAs wafer surface using a spin-on technique [53]. The polyimide was diluted to a lower viscosity using Du Pont T-9039 thinner at a 1:1 dilution ratio. The polyimide was imidized in a controlled forced air convection oven using a low temperature 250 °C heating cycle for nearly 3 hours [54]. This heating cycle was below the eutectic temperature of the ohmic

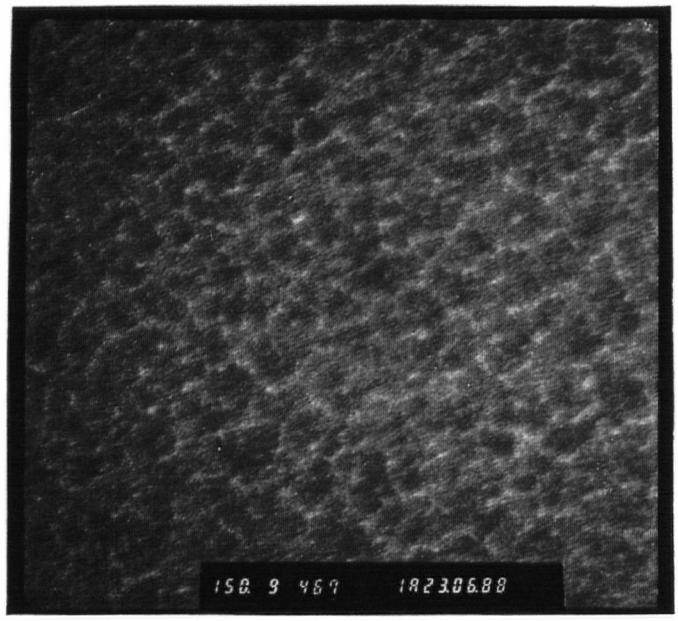

Figure 5.4: A transmission electron microphotograph of the Cr:SiO (45 wt. % Cr) film at 150,000 times magnification. The number '1' in the label corresponds to a height of 2.0 mm at this magnification.

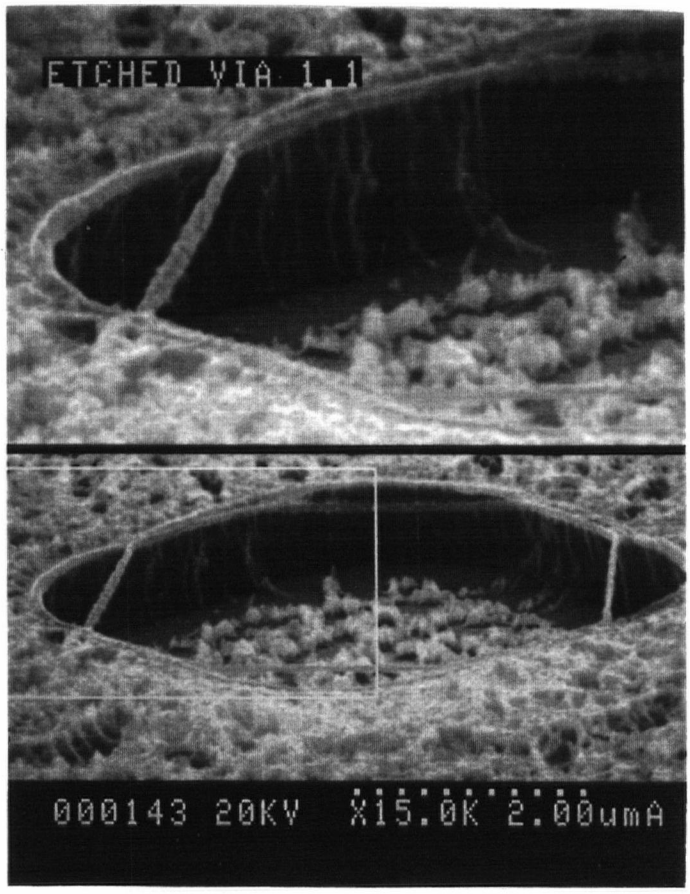

Figure 5.5: A microphotograph of the plasma etch profile of a 5 micron square via etched through a 1.8 micron thick polyimide film.

contacts [45] and the annealing temperature of the proton isolation implants [55,56] and consequently did not alter the electrical characteristics of these fabricated structures.

The interconnect vias between the first level metallization and the second level metallization were chemically etched through the imidized polyimide film using a three step plasma etch process employing plasma enhanced chemical vapour etching [57,58]. A nominal 600 Å thick titanium film was deposited onto the imidized polyimide surface using electron beam evaporation. The surface of the titanium film was subsequently covered with a 1.2 micron thick patterned photoresist mask. The exposed regions of the titanium film were etched through the photoresist mask using a CF_4/O_2 plasma, transferring the photoresist pattern to the titanium film. The exposed regions of the polyimide film were etched through the titanium mask using an O_2 plasma, transferring the original photoresist pattern to the polyimide film. The photoresist film was also removed from the titanium surface during this etch. The titanium mask was removed in a final CF_4/O_2 plasma etch. Figure 5.5 shows the resultant vertical etch profile of a 5 micron square interconnect via etched through the polyimide film using the above plasma etch process.

The second level metallization was patterned using the photoresist liftoff method. A nominal 500 Å Ti and 4000 Å Au multilayer metallization was sequentially electron beam evaporated onto the wafer surface through a 2.1 micron thick photoresist mask and the subsequent liftoff was performed in an ultrasonic acetone bath, completing the fabrication of the GaAs CMCCD. The intermediate titanium layer provided the required adhesion between the polyimide film and the second level metallization gold layer.

Chapter 6

Testing and Evaluation

A series of dc threshold voltage measurements were performed on the GaAs CMCCD prior to packaging the device to determine if the control gates and the transport electrode arrays were functional. A Tektronix TEK-576 curve tracer attached to an Alessi probe station was used to make these measurements. The input ohmic contact and the output ohmic contact of the CMCCD were used as the drain and the source, respectively. A 5 volt drain to source bias was applied to the device. Each of the three control gates and each of the four transport electrode arrays were biased, in turn, negatively with respect to the source node until no further change was observed in the drain to source current. The observed gate to source voltage corresponding to this condition was recorded as the threshold voltage. Table V contains a list of the measured threshold voltages of the GaAs CMCCD.

The CMCCD was mounted in a 32 pin ceramic flat package. A discrete DEXCEL-2502 GaAs MESFET die was also mounted in the package for use as a reset switch at the output ohmic contact of the CMCCD. The CMCCD, the on-chip GaAs MESFET source follower amplifier and the discrete GaAs MESFET die were wire-bonded in the package using the configuration shown in Figure 6.1. This packaging configuration resulted in a minimum parasitic capacitance $C_{O/P}$ at the output ohmic contact of the CMCCD. This is desirable for obtaining maximum output signal amplitudes from the CMCCD, as the signal charge arriving at the output ohmic contact is converted to a voltage with an amplitude inversely proportional to $C_{O/P}$.

The on-chip GaAs MESFET source follower amplifier buffered the output ohmic contact of the CMCCD from the external output electronics. It consisted of two depletion mode 2 micron by 30 micron MESFETs configured in a totem pole arrangement

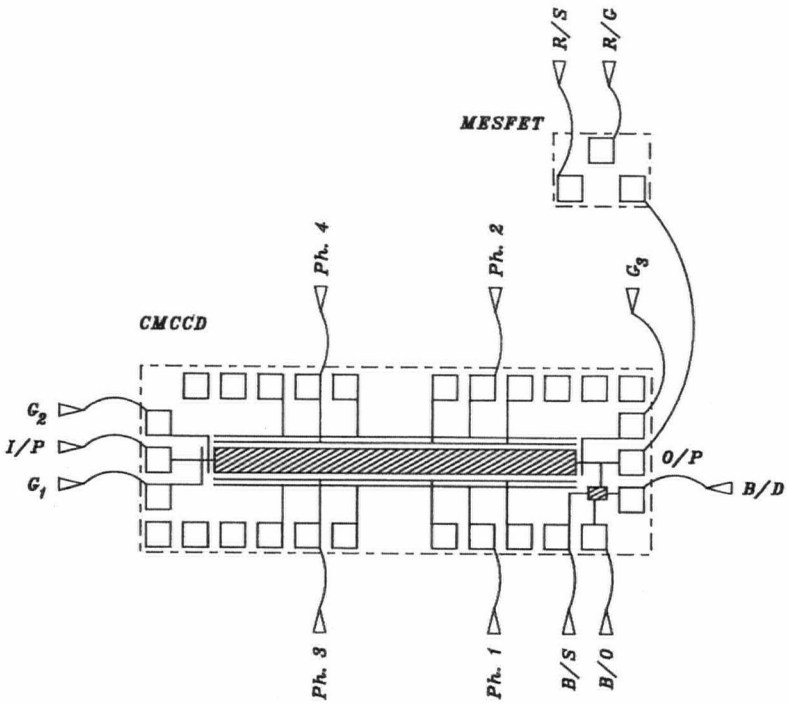

Figure 6.1: The wire-bonding configuration used to interconnect the CMCCD, the on-chip GaAs MESFET source follower amplifier and the discrete GaAs MESFET die.

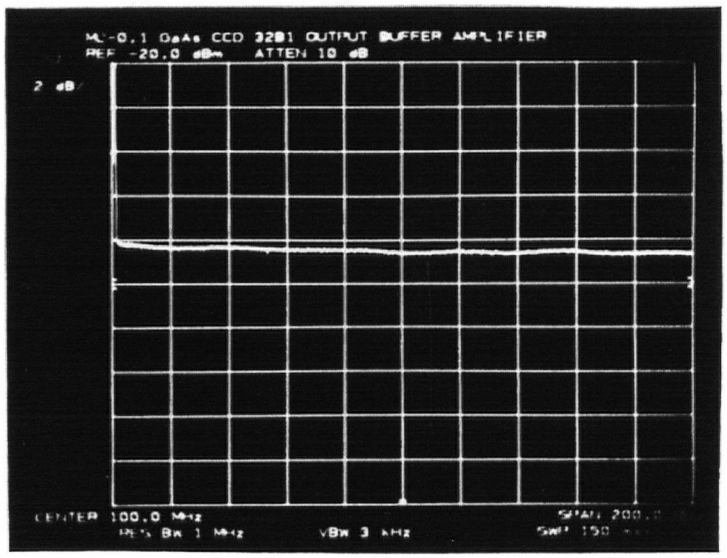

Figure 6.2: The insertion loss of the on-chip GaAs MESFET source follower amplifier measured from 300 kHz to 200 MHz.

Gate	Threshold Voltage (Volts)
G_1	-2.4
G_2	-2.45
G_3	-2.4
Ph. 1	-1.8
Ph. 2	-1.8
Ph. 3	-1.85
Ph. 4	-1.7

Table V: The measured threshold voltages of the GaAs CMCCD.

which provided a low capacitance, high impedance load to the output ohmic contact of the CMCCD. A threshold voltage of approximately -2.2 volts and a saturation current of approximately 5.0 milliampères was measured for these transistors using a Tektronix TEK-579 curve tracer. The insertion loss of the source follower amplifier terminated in 50 ohm source and load impedances was measured from 300 kHz to 200 MHz using a Hewlett-Packard HP-8753A network analyzer and an HP-85046A s-parameter test set. The measured insertion loss is shown in Figure 6.2.

The GaAs CMCCD was operated in the VHF band at 100 MHz and was evaluated for operation at this frequency using the impulse response method [59] and the insertion loss method [60]. The CMCCD was operated using the signal levels listed in Table VI, which were provided by a test circuit comprised of emitter-coupled logic ICs and discrete GaAs MESFETs. A schematic diagram of the CMCCD test circuit is provided in Appendix E. Charge injection into the CMCCD was obtained using the diode cutoff method described in Chapter 2. The test circuit had a bandwidth of approximately 150 MHz and was the limiting factor for testing the CMCCD at higher clock frequencies. A Tektronix PG-502 250 MHz pulse generator and a TEK-7904 oscilloscope frame mounted with a 7A24 dual trace amplifier and a 7B92A dual timebase unit were used for the impulse response measurement and a Hewlett-Packard HP-8753A network analyzer with an HP-85046A s-parameter test set was used for the insertion loss measurement.

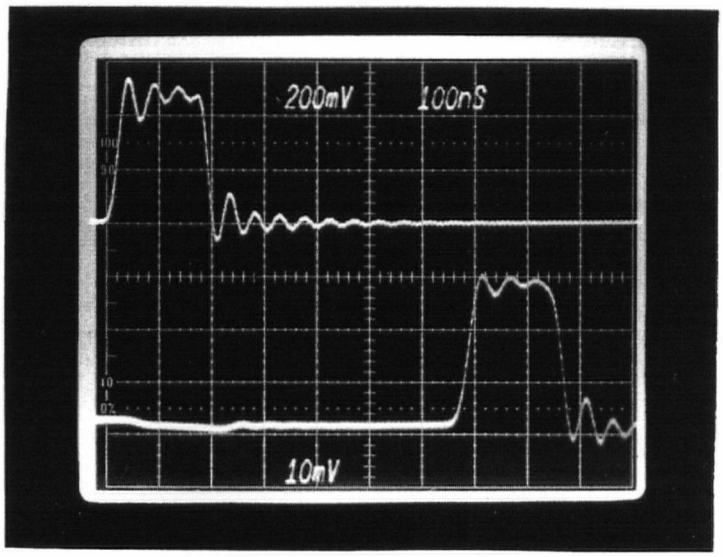

Figure 6.3: The qualitative demonstration of the performance of the GaAs CMCCD for 100 MHz operation.

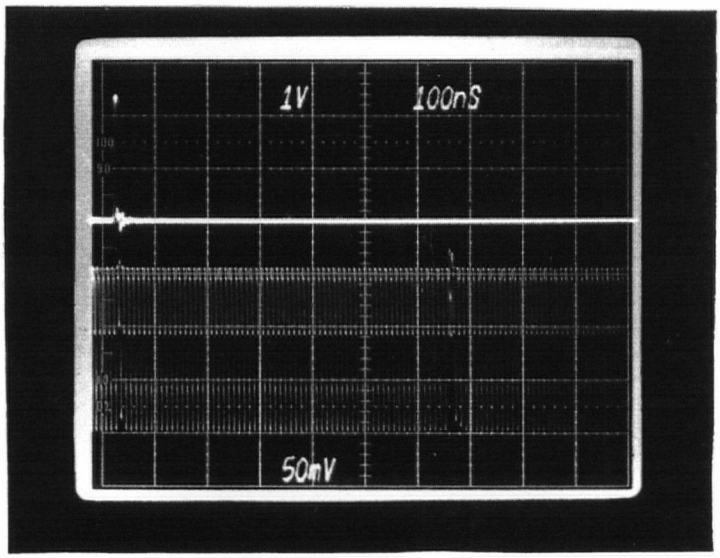

Figure 6.4: The impulse response of the GaAs CMCCD for 100 MHz operation.

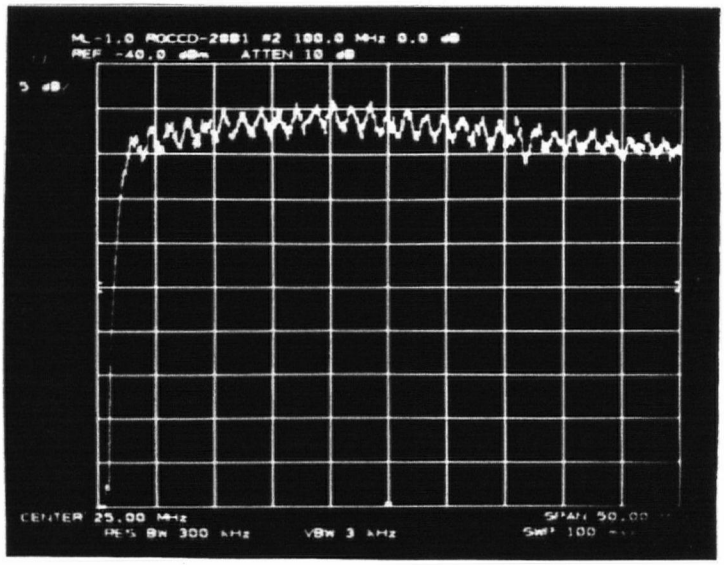

Figure 6.5: The insertion loss of the GaAs CMCCD for 100 MHz operation.

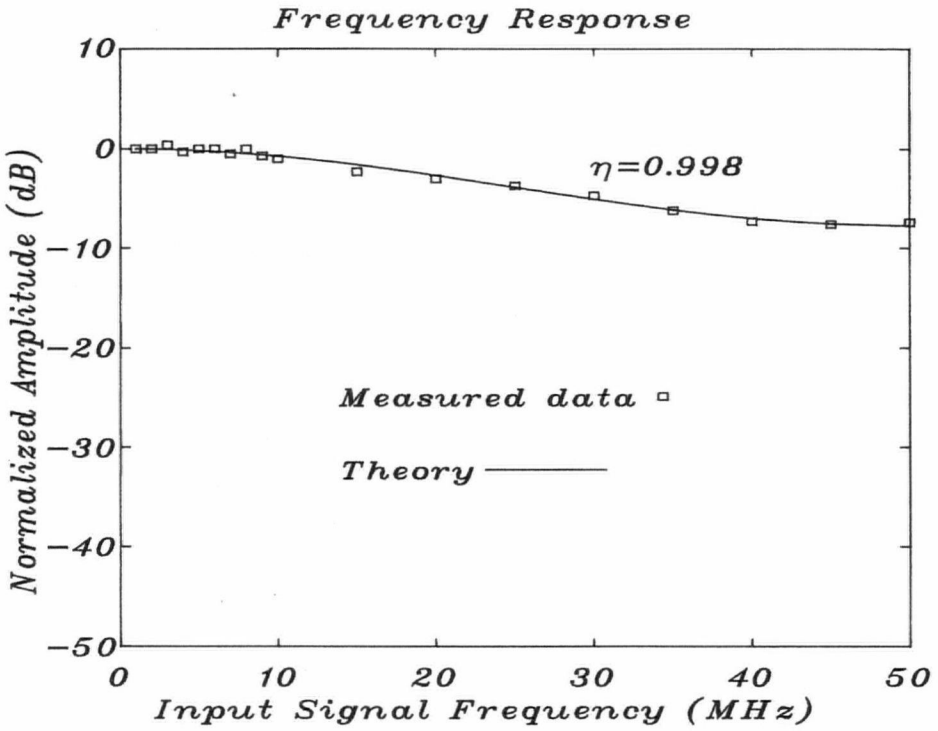

Figure 6.6: The theoretical insertion loss of the GaAs CMCCD for 100 MHz operation.

Gate	Signal level(s) (volts)
I/P	0 to +0.5
G_1	-0.8 to -5.8
G_2	+0.3 to -4.7
Ph. 1	0 to -5.0
Ph. 2	0 to -5.0
Ph. 3	0 to -5.0
Ph. 4	0 to -5.0
R/G	0 to -5.0
G_3	-2.7 to -2.7
B/D	+5.0 to +5.0
B/S	-5.2 to -5.2
R/S	0 to 0

Table VI: The signal levels applied to the GaAs CMCCD for operation at 100 MHz.

A qualitative demonstration of the performance of the GaAs CMCCD for 100 MHz operation is shown in Figure 6.3. The oscillograph contained in this figure displays the CMCCD input signal along the upper signal trace and the processed CMCCD output signal along the lower signal trace. The input signal was obtained by passing a trapezoidal pulse through a passive lowpass filter having a cutoff frequency of 20.5 MHz. The damped oscillations were a result of the filter response to the 1 nanosecond transitions of the input pulse. The processed CMCCD output signal was obtained by filtering the buffered CMCCD output signal using a lowpass filter similar to the one used at the input. Figure 6.3 demonstrates the good signal fidelity of the CMCCD for 100 MHz operation.

Figure 6.4 shows an oscillograph of the impulse response of the CMCCD for 100 MHz operation. The CMCCD input signal is along the upper signal trace and the buffered CMCCD output signal is along the lower signal trace. The input signal consisted of a 5 nanosecond wide, 2.4-volt amplitude, 1 nanosecond transition trapezoidal impulse. The buffered CMCCD output waveform contains the modulation envelope of the impulse and the passive feedthrough of the quadrature clocks. The modulation

Method	Charge Transfer Efficiency
Impulse Response	1.00
Insertion Loss	0.998

Table VII: The charge transfer efficiencies of the GaAs CMCCD for 100 MHz operation.

envelope of the impulse consists of a single pulse transient delayed by 640 nanoseconds with respect to the input signal. The charge transfer efficiency of the CMCCD was determined from the CMCCD impulse response using the calculation [59]

$$N_{peak} = N_T(1 - \eta) \tag{6.1}$$

where N_T is the number of single electrode transfers through the CMCCD and N_{peak} is the number of pixel transfers between the peak of the observed CMCCD impulse response and the peak of the ideal CMCCD impulse response. The computed charge transfer efficiency is listed in Table VII.

The insertion loss of the GaAs CMCCD for 100 MHz operation is shown in Figure 6.5. A -10 dBm swept frequency sinusoidal signal spanning the range from 300 kHz to the Nyquist frequency of 50 MHz was applied to the input ohmic contact of the CMCCD and the insertion loss of the device was measured. Figure 6.5 indicates that the CMCCD has a nearly uniform insertion loss over the entire 50 MHz input signal bandwidth, which is indicative of good performance. The charge transfer efficiency of the CMCCD was determined by fitting the equation [60]

$$A_{dB} = 20 \log \left[A_0 \exp \left(-N_T(1 - \eta) \left[1 - \cos \left(\frac{\omega}{f_c} \right) \right] \right) \right] \tag{6.2}$$

to the measured data. Here A_{dB} is the insertion loss, A_0 is a constant amplitude term, ω is the input signal frequency and f_c is the CMCCD clock frequency. The calculated charge transfer efficiency using the insertion loss method is listed in Table VII and the curve fit to the measured data is shown in Figure 6.6.

Chapter 7

Comments

7.1 Summary

Contributions were made towards developing the GaAs CMCCD for high frequency signal processing applications. The design, implementation and evaluation of the CMCCD were considered and are summarized in this section.

The design equations for determining the active layer requirements of the GaAs CMCCD were described in Chapter 2. The design protocol that was outlined assumes that the active layer was uniformly doped and was constrained to have a pinch-off voltage that was typical of an n-type depletion mode MESFET. It was demonstrated that the full well charge confinement and the full well capacity of the CMCCD were simultaneously maximized if the device was fabricated on a thin, highly doped active layer. This result suggested that the optimum CMCCD active layer was similar to the active layer of a low to medium power n-type depletion mode GaAs MESFET, which was advantageous when the two devices were integrated monolithically. It was indicated in Chapter 1 that the GaAs CGCCD could not be monolithically integrated with GaAs MESFETs in a simple manner as the CGCCD was typically fabricated on thick, lightly doped active layers which were not directly compatible with MESFETs.

It was demonstrated in Chapter 3 that a cermet/GaAs Schottky barrier diode exhibits rectification properties similar to that of a metal/GaAs Schottky barrier diode with a large series resistance. The Schottky barrier height and the ideality factor of the cermet/GaAs junction were determined using a distributed resistive gate Schottky barrier diode model of the fabricated planar cermet/GaAs Schottky barrier diode. A Schottky barrier height of 0.64 eV and an ideality factor of 1.17 were determined for the cermet/GaAs junction.

A transmission line model described in Chapter 3 for the cermet/GaAs junction within an interelectrode gap of the CMCCD was used to demonstrate that the surface potential distribution along the gap was monotonic for all frequencies. A differential length of the transmission line model consisted of a differential series impedance and a differential shunt admittance. The series impedance modeled the cermet film and was comprised of a parallel resistance and capacitance. The shunt admittance modeled the depletion layer capacitance of the underlying GaAs. It was determined from an analysis of the transmission line model that the high frequency surface potential variation along a gap of the CMCCD was independent of the distributed cermet film resistance. This was an important result as it indicated that the operation of the CMCCD was not critically dependent upon the distributed cermet film resistance, provided that it was large enough to satisfy the power constraints of the quadrature clocks. It was further demonstrated in Chapter 3 using the transmission line model that the distributed cermet film capacitance was preferably greater than the distributed depletion layer capacitance in order to maintain a nearly linear surface potential variation along the gap of a CMCCD for all frequencies. This was desirable for achieving an optimal uniform tangential electric field distribution within the CMCCD active layer to assist charge transfer.

A two-dimensional computer model for investigating the operation of the GaAs CMCCD was described in Chapter 4. A unit cell representing a single pixel of a 4-phase GaAs CMCCD consisted of a domain comprised of the active layer subdomain and the semi-insulating substrate subdomain. The transport electrodes were defined as equipotential boundaries and the interelectrode gaps were defined as linear potential boundaries. A finite difference grid was superimposed onto the unit cell, on which the semiconductor equations were solved. A Newton iteration scheme with successive relaxation was used to solve the finite difference equations for the potential and the electron density. Computer simulations for the static potential distributions within the

CMCCD were used to determine the theoretical maximum frequency of operation of the device as a function of the interelectrode gap length and the peak clock voltage amplitude for a constant transport electrode pitch. It was demonstrated that the CMCCD transport electrodes should have a minimum length to achieve the maximum frequency of operation for the lowest possible power requirements. A simulation of the dynamic single electrode transfer of a half full well of charge in 100 picoseconds was demonstrated. This simulation indicated that the charge packet was essentially fully transferred by the end of the transfer interval, suggesting that the CMCCD will demonstrate good performance at frequencies approaching 2.5 GHz.

A six mask level fabrication process for producing the GaAs CMCCD was described in Chapter 5. Conventional contact lithography was used to fabricate the device. The six mask levels provided the patterns for the ohmic contacts, the proton isolation implants, the metal/GaAs Schottky barriers, the cermet/GaAs Schottky barriers, the interconnect vias and the second level metallization. The Au-Ge/Ni/Au ohmic contacts, the Ti/Pt/Au metal/GaAs Schottky barriers and the Cr:SiO cermet/GaAs Schottky barriers were patterned directly on the n-type active layer. Three proton implants at different beam energies were used to isolate the CMCCD active region and the MESFET source follower amplifier active region, maintaining a planar device structure. A polyimide interlayer dielectric film was used to separate the first level metallization from the second level metallization. Connections between the two metallization levels were made through interconnect vias that were plasma etched through the polyimide film.

The operation of the GaAs CMCCD was described in Chapter 6. The dc threshold voltage measurements were used to select the CMCCD from the fabricated devices. The CMCCD, the on-chip MESFET source follower amplifier and a discrete GaAs MESFET die were wire-bonded in a 32 pin ceramic package. The MESFET was used as a reset switch on the output ohmic contact of the CMCCD. A test circuit was used to

provide the signals to the packaged components. The diode cutoff method described in Chapter 2 was used to inject charge into the CMCCD. The CMCCD was operated using a clock frequency of 100 MHz and was evaluated at this operating frequency using the impulse response method and the insertion loss method. The CMCCD demonstrated good performance at 100 MHz clock frequency with charge transfer efficiencies of 1.00 and 0.998 calculated respectively using the above two evaluation techniques.

7.2 Considerations for Future Work

This work was focused on the design, implementation and evaluation of a 64-pixel, 4-phase GaAs CMCCD. The issues which could be addressed in further developing this device are described in this section.

The 64-pixel, 4-phase GaAs CMCCD that was developed in this work was not fully optimized. The fabricated CMCCD had an active layer with a uniform donor density of $4.5 \cdot 10^{16}$ cm^{-3} to a depth of 0.25 microns. These active layer parameters were satisfactory for demonstrating the operation of the CMCCD with a GaAs MESFET, but would not necessarily yield the best possible device performance. The 3 micron CMCCD transport electrode length was chosen for convenience, in order that the fabrication requirements to produce the device would be reduced. A revision to the above CMCCD structure would consist of using a CMCCD active layer with a uniform donor density of approximately $2.0 \cdot 10^{17}$ cm^{-3} to a depth of approximately 0.1 microns which is more consistent with the active layer requirements of a nominal -2.0 volt n-type depletion mode GaAs MESFET. Furthermore, the analysis described in Chapter 2 indicates that the revised active layer parameters are preferred, as the signal charge confinement and the signal charge capacity of the CMCCD would be improved. The revised CMCCD transport electrode length would be 1.0 microns or less in order that the high frequency performance and the associated power requirements of the CMCCD would be improved as described in Chapter 4.

The monolithic integration of the peripheral support electronics with the GaAs CMCCD is essential for obtaining maximum performance from the device. In particular the output reset switch and the output signal processing circuitry should be directly integrated with the CMCCD. This level of integration would increase the operating bandwidth, increase the dynamic range and increase the signal to noise ratio of the CMCCD. This would be a consequence of the reduction in the parasitic component values attached to the output node of the CMCCD.

A 2-phase GaAs CMCCD structure could also be considered for further investigation as it would maximize the utilization of the active device area by achieving a greater pixel density and it would significantly reduce the clock driver circuit requirements. Hansell developed a castellated 2-phase GaAs CGCCD that exhibited a charge transfer efficiency of 0.93 [20]. It was determined by Hansell that the reduced charge transfer efficiency of the 2-phase CGCCD was largely due to the presence of energy troughs within the active layer volume bounded on the surface by the interelectrode gaps. A proposed 2-phase GaAs CMCCD would consist of a castellated structure similar to that used by Hansell, except that the interelectrode gaps would be encapsulated with a cermet film and the active layer parameters would be closely matched to those of a GaAs MESFET. The proposed structure should minimize the performance loss resulting from the formation of energy troughs within the active layer. Further investigation of the proposed 2-phase CMCCD using two-dimensional computer modeling is required to assess this device.

Bibliography

[1] F.L. Schuermeyer, R.A. Belt, C.R. Young, and J.M. Blasingame. New structures for charge-coupled devices. *Proc. IEEE*, **60**:1444–1445, Nov. 1972.

[2] W. Kellner, H. Bierhenke, and H. Kniepkamp. A Schottky barrier CCD on GaAs. *Int. Electron Devices Meeting*, 599–602, 1977.

[3] I. Deyhimy, J.S. Harris, Jr., R.C. Eden, D.D. Edwall, S.J. Anderson, and L.O. Bubulac. GaAs charge-coupled devices. *Appl. Phys. Lett.*, **32**(6):383–385, Mar. 1978.

[4] A.J. Hayes, J.T. Davies, and W. Eccleston. Operation of a single-phase CCD on GaAs at 560 MHz. *IEE Proc. I*, **132**(1):34–36, Feb. 1985.

[5] W. Kellner, U. Ablassmeier, and H. Kniepkamp. A two-phase CCD on GaAs with 0.3-μm-wide electrode gaps. *IEEE Trans. Electron Devices*, **ED-27**(6):1195–1197, Jun. 1980.

[6] I. Deyhimy, R.C. Eden, R.J. Anderson, and J.S. Harris, Jr. A 500-MHz GaAs charge-coupled device. *Appl. Phys. Lett.*, **36**(2):151–153, Jan. 1980.

[7] I. Deyhimy, R.C. Eden, and J.S. Harris, Jr. GaAs and related heterojunction charge-coupled devices. *IEEE Trans. Electron Devices*, **ED-27**(6):1172–1180, 1980.

[8] L.J.M. Esser and F.L.J. Sangster. *Handbook on Semiconductors*, pages 335–421. Volume 4, North-Holland Publishing Company, Amsterdam, 1981.

[9] E.A. Sovero, R. Sahai, W.A. Hill, and J.A. Higgins. Microwave frequency GaAs charge-coupled devices. In *GaAs IC Symposium Technical Digest*, pages 101–104, IEEE, New York, 1984.

[10] K.B. Nichols and B.E. Burke. A gallium arsenide overlapping-gate charge-coupled device. *IEEE Electron Device Lett.*, **EDL-6**(5):237–240, May 1985.

[11] M.J. Cohen. GaAs charge coupled devices for high speed signal processing applications. *Int. Electron Devices Meeting*, 622–625, 1981.

[12] R.C. Eden and I. Deyhimy. GaAs integrated circuits and charged-coupled devices for high speed signal processing. *Opt. Eng.*, **20**(6):947–952, Nov.-Dec. 1981.

[13] R.C. Eden and I. Deyhimy. Application of GaAs integrated circuits and charge-coupled devices (CCDs) for high speed signal processing. *Proc. Soc. Photo-opt. Instrum. Eng.*, **214**:39–47, 1979.

[14] I. Deyhimy, J.S. Harris, Jr., R.C Eden, and R.J Anderson. Reduced geometry GaAs CCD for high speed signal processing. *Jpn. J. Appl Phys.*, **19**(19-1):269–272, 1979.

[15] R.C. Eden and I. Deyhimy. GaAs integrated circuits and charge-coupled devices (CCDs) for high-speed signal processing. *Proc. Soc. Photo-opt. Instrum. Eng.*, **180**:182–189, 1979.

[16] R.C. Eden and I. Deyhimy. Application of GaAs integrated circuits and CCDs for high speed signal processing. In *IEEE Electronics and Aerospace Systems Conference*, pages 78–86, IEEE, New York, 1979.

[17] R. Sahai, W.A. Hill, B. Mathur, S. Pittman, and J.A. Higgins. GaAs CCDs for analog signal processing ICs. In *IEEE 1986 Custom Integrated Circuits Conference*, pages 521–527, IEEE, New York, 1986.

[18] J.A. Higgins, R.A. Milano, E.A. Sovero, and R. Sahai. Resistive gate GaAs charge coupled devices. In *GaAs IC Symposium Technical Digest*, pages 49–52, IEEE, New York, 1982.

[19] M.R. Wilson, P.B. Kosel, and C. Geesner. Rapid thermal annealing of implanted layers for GaAs MESFETs and CCDs. In *Proceedings of the Symposium on Dielectric Films on Compound Semiconductors*, pages 259–273, Electrochemical Society, New Jersey, 1986.

[20] G.L. Hansell. *GaAs Schottky-Barrier Charge-coupled Devices.* PhD thesis, Massachusetts Institute of Technology, Jun. 1982.

[21] J.I. Song and E.R. Fossum. Inhibition of charge packet broadening in GaAs charge-coupled devices. *Appl. Phys. Lett.*, **51**(19):1539–1541, 1987.

[22] C.R. Wronski, B. Abeles, R.E. Daniel, and Y. Arie. Granular metal-semiconductor Schottky barriers. *J. Appl. Phys.*, **45**(1):295–299, Jan. 1974.

[23] R.H Walden, R.H. Krambeck, R.J. Strain, J. McKenna, N.L. Schryer, and G.E. Smith. The buried channel charge coupled device. *Bell System Tech. J.*, **51**(9):1635–1640, Sept. 1972.

[24] R. Sahai, R.L. Pierson, Jr., E.H. Martin, and J.A. Higgins. High speed GaAs detector array/CCD multiplexer for acousto-optic spectrum analyzer. *Proc. SPIE Int. Soc. Opt. Eng.*, **477**:165–173, 1984.

[25] E.A. Sovero, W.A. Hill, R. Sahai, J.A. Higgins, S. Pittman, E.H. Martin, and R.L. Pierson, Jr. Transversal filter application of a high speed gallium arsenide CCD. In *GaAs IC Symposium Technical Digest*, pages 92–95, IEEE, New York, 1983.

[26] W.A. Hill, E.A. Sovero, J.A. Higgins, E.H. Martin, and S. Pittman. 1 GHz sample rate GaAs CCD transversal filter. In *GaAs IC Symposium Technical Digest*, pages 27–30, IEEE, New York, 1985.

[27] C.H. Sequin and A.M. Mohsen. Linearity of electrical charge injection into charge-coupled devices. *IEEE J. Solid State Circuits*, **SC-10**:81–92, 1975.

[28] S.M. Sze. *Physics of Semiconductor Devices*, page 320. John Wiley and Sons, USA, Second edition, 1981.

[29] B.L. Sharma, editor. *Metal-Semiconductor Schottky Barrier Junctions and Their Applications*, pages 38–40. Plenum Press, New York, 1984.

[30] W.F. Ames. *Nonlinear Ordinary Differential Equations in Transport Processes*, pages 44–47. Academic Press, New York, 1968.

[31] J.D. Kraus and K.R. Carver. *Electromagnetics*, pages 485–490. McGraw Hill, New York, Second edition, 1973.

[32] M. LeNoble, J.V. Cresswell, R. Sahai, and J.A. Higgins. TRIUMF/Rockwell International Microelectronics Research and Development Center, private communications.

[33] W. Fichtner, D.J. Rose, and R.E. Bank. Semiconductor device simulation. *IEEE Trans. Electron Devices*, **ED-30**(9):1018–1030, Sept. 1983.

[34] D.L. Scharfetter and H.K. Gummel. Large-signal analysis of a silicon Read diode oscillator. *IEEE Trans. Electron Devices*, **ED-16**(1):64–77, Jan. 1969.

[35] J.P. Lavine and B.C Burkey. Extensions of the Scharfetter-Gummel approach to charge transfer. *Solid-State Electronics*, **23**(1):75–77, 1980.

[36] C.F. Gerald. *Applied Numerical Analysis*, pages 224–227. Addison-Wesley Publishing Company, Philippines, 1970.

[37] C.S. Chang and H.R. Fetterman. Electron drift velocity versus electric field in GaAs. *Solid-State Electronics*, **29**(12):1295–1296, 1986.

[38] M.G. Collet and A.C. Vliegenthart. Calculations on potential and charge distributions in the peristaltic charge-coupled device. *Philips Res. Repts.*, **29**:25–44, 1974.

[39] C.F. Gerald. *Applied Numerical Analysis*, pages 7–16. Addison-Wesley Publishing Company, Philippines, 1970.

[40] C.F. Gerald. *Applied Numerical Analysis*, pages 207–208. Addison-Wesley Publishing Company, Philippines, 1970.

[41] A.I. Prokop'ev. Analysis of the transit time of a single electron for estimating the speed of response of gallium-arsenide charge-coupled devices. *Izv. VUZ. Radioelektron. (USSR)*, **28**(5):78–79, 1985.

[42] D. Sodini, K. Torbati, D. Rigaud, and A. Touboul. Numerical simulation of the charge transfer in GaAs BCCDs. *Solid-State Electronics*, **29**(9):969–976, 1986.

[43] R.E. Williams. *Gallium Arsenide Processing Techniques*, pages 37–42. Artech House, Dedham, MA, 1984.

[44] R.E. Williams. *Gallium Arsenide Processing Techniques*, pages 44–45. Artech House, Dedham, MA, 1984.

[45] A. Piotrowska, A. Guivarc'h, and G.Pelous. Ohmic contacts to III-V compound semiconductors: a review of fabrication techniques. *Solid-State Electronics*, **26**(3):179–197, 1983.

[46] R.E. Williams. *Gallium Arsenide Processing Techniques*, pages 125–127. Artech House, Dedham, MA, 1984.

[47] I. Deyhimy, J.S. Harris, Jr, R.C. Eden, R.J. Anderson, and D.D. Edwall. An ultra high speed GaAs CCD. *Int. Electron Devices Meeting*, 619–621, 1979.

[48] I. Deyhimy, R.J. Anderson, and S. Lane. GaAs CCD. In *IEEE Electronics and Aerospace Systems Conference*, pages 151–154, IEEE, New York, 1980.

[49] M.D. Clark, C.L. Anderson, R.A. Jullens, and G.S. Kamath. Planar sealed-channel gallium arsenide Schottky-barrier charge-coupled devices. *IEEE Trans. Electron Devices*, **ED-27**(6):1183–1188, Jun. 1980.

[50] Y.Z. Liu, R.J. Anderson, I. Deyhimy, and L.R. Tomasetta. Proton-bombardment isolated GaAlAs/GaAs charge-coupled devices. *Electron. Lett.*, **16**(9):327–329, Apr. 1980.

[51] H. Matino and T. Ushiroda. Effect of substrate bias on properties of rf-sputtered Cr-SiO films. *IBM J. Res. Develop.*, 576–579, Nov. 1977.

[52] M. Mager. UBC Metallurgy, private communication.

[53] Du Pont Company. PYRALIN polyimide coatings: preliminary information bulletin spin coating techniques. May 1985. Bulletin: PC-2.

[54] Du Pont Company. PYRALIN polyimide coatings for electronics. Apr. 1982. Bulletin: PC-1.

[55] A.G. Foyt, W.T. Lindley, C.M. Wolfe, and J.P. Donnelly. Isolation of junction devices in GaAs using proton bombardment. *Solid-State Electronics*, **12**:209–214, 1969.

[56] D.C. D'Avanzo. Proton isolation for GaAs integrated circuits. *IEEE Trans. Electron Devices*, **ED-29**(7):1051–1058, Jul. 1982.

[57] J.W. Coburn. Plasma-assisted etching. *Plasma Chemistry and Plasma Processing*, **2**(1):1–40, 1982.

[58] F.D. Egitto, F. Emmi, R.S. Horwath, and V. Vukanovic. Plasma etching of organic materials. 1. polyimide in O_2-CF_4. *J. Vac. Sci. Technol. B*, **3**(3):893–904, May 1985.

[59] C.H. Sequin and M.F. Tompsett. *Charge Transfer Devices*, pages 73–76. Academic Press, New York, 1975.

[60] G.F. Vanstone, J.B.G. Roberts, and A.E. Long. The measurement of the charge residual for CCD transfer using impulse and frequency responses. *Solid-State Electronics*, **17**:889–895, 1974.

[61] J.V. Cresswell, I. Carvahlo, M. LeNoble, O. Berolo, and R. Kule. A 500 MHz CCD serial analog memory. *IEEE Trans. Nucl. Sci.*, **NS-33**(1):90–91, Feb. 1986.

[62] D.A. Bryman. TRIUMF, private communication.

[63] BNL, Princeton, TRIUMF Collaboration. *Current Goals, R&D, Design, and Construction Status of Detector for AGS Experiment #787—A Study of the Decay* $K^+ \to \pi^+ \nu\bar{\nu}$. Technical Report, TRIUMF, Oct. 1985.

[64] J.V. Cresswell, S. Ahmad, E.W. Blackmore, D.A. Bryman, N. Kahn, Y. Kuno, and T. Numao. A cylindrical drift chamber for the measurement of $K \to \pi\nu\bar{\nu}$ decay. *IEEE Trans. Nucl. Sci.*, **35**(1):460–463, Feb. 1988.

[65] J.V. Cresswell. TRIUMF, private communication.

Appendix A

BNL Experiment 787

The development of the GaAs CMCCD was inspired by the need for a wideband data acquisition system for Experiment 787, which is currently being prepared for implementation at the Brookhaven National Laboratory [61]. This nuclear physics experiment is being conducted collaboratively with scientists and engineers from Brookhaven, Princeton University and TRIUMF. The experimental goals of Experiment 787, the relevant technical aspects of the detector apparatus for this experiment and the application of a CMCCD in the data acquisition system for instrumenting the detector are described in this appendix.

The development of a comprehensive Standard Model for describing the interactions that occur amongst the elementary subatomic particles is of current interest to nuclear physicists. The existence of three neutrino generations has been established within the current framework of this model and must be experimentally verified. A test for the number of neutrino generations will be attempted in Experiment 787 by directly observing and measuring the rate of decay of a kaon to a pion and neutrino/anti-neutrino pair. This particular decay sequence is extremely rare and is anticipated to occur once in approximately every ten billion kaon decays [62]. Should the observed decay rate lie in the vicinity of the expected rate, then a positive test for the existence of three neutrino generations will have been made. It has been suggested that new generations of neutrinos, or perhaps, new elementary particles may exist if the observed rate of decay of a kaon to a pion and neutrino/anti-neutrino pair is greater than about five times the anticipated rate [63].

A sophisticated rare kaon decay spectrometer is currently being developed for Experiment 787 to provide the required detection capability for observing the decay

of a kaon to a pion and neutrino/anti-neutrino pair. A cross-sectional view of this apparatus displaying its relevant features is shown in Figure A.1. The detector is cylindrical in shape with overall dimensions of approximately 6 metres in length by 5 metres in diameter. The target is located along the central axis of the detector core and is surrounded by a cylindrical drift chamber [64] that is enclosed within a scintillation counter range stack.

A burst of highly energetic kaons from the BNL accelerator arrives along the central axis of the detector penetrating the target. The majority of incident kaons are stopped within the target and decay into other particles. The newly formed decay particles traverse the detector in a manner that is dependent upon their energy, momentum and lifetime. The cylindrical drift chamber is used to monitor the energies and the trajectories of the particles as they are emitted from the target. The pions that result from a decaying kaon pass through the cylindrical drift chamber and are ultimately stopped within the scintillation counter range stack where they decay into other particles. A primary function of the scintillation counter range stack is to provide the positive identification of the pions that emerge from the drift chamber. This is achieved by tracking the decay of the pion to a muon and the subsequent decay of the muon to an electron using energy versus time measurements. These interactions are detected as electrical signals at the output of the photomultiplier tubes that are attached to the scintillation counter range stack. The ideal output waveform obtained from a range stack photomultiplier tube for the pion to muon to electron decay sequence is shown in Figure A.2.

The waveform shown in Figure A.2 is a simplification of the complex series of interactions that occur between the energetic particles and the nuclear instruments. In principle, the observed pulses tend to pile up onto each other due to the previous history within the spectrometer. Consequently, the waveform illustrated in Figure A.2 for the practical case will consist of many superimposed pulses having peak separations that

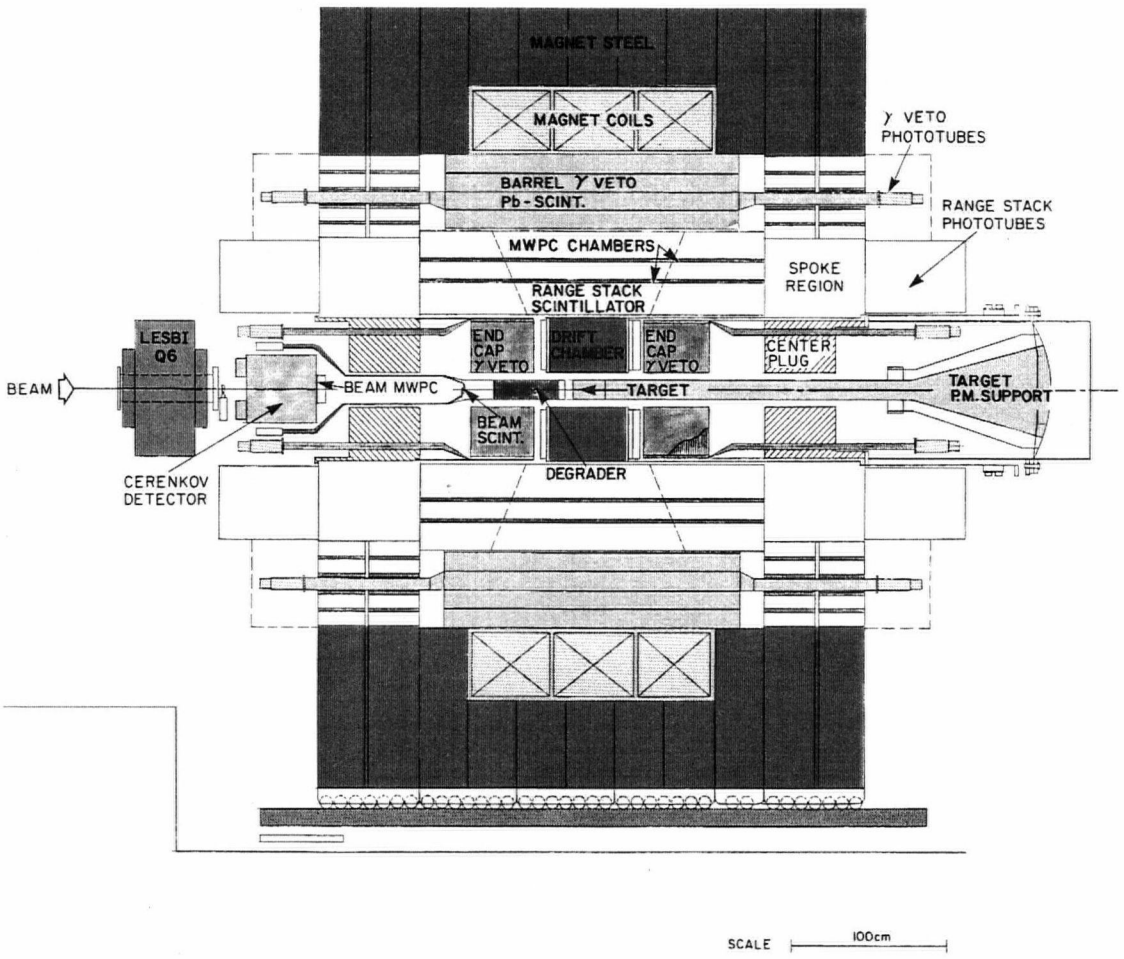

Figure A.1: A cross-sectional view of the BNL Experiment 787 rare kaon decay spectrometer.

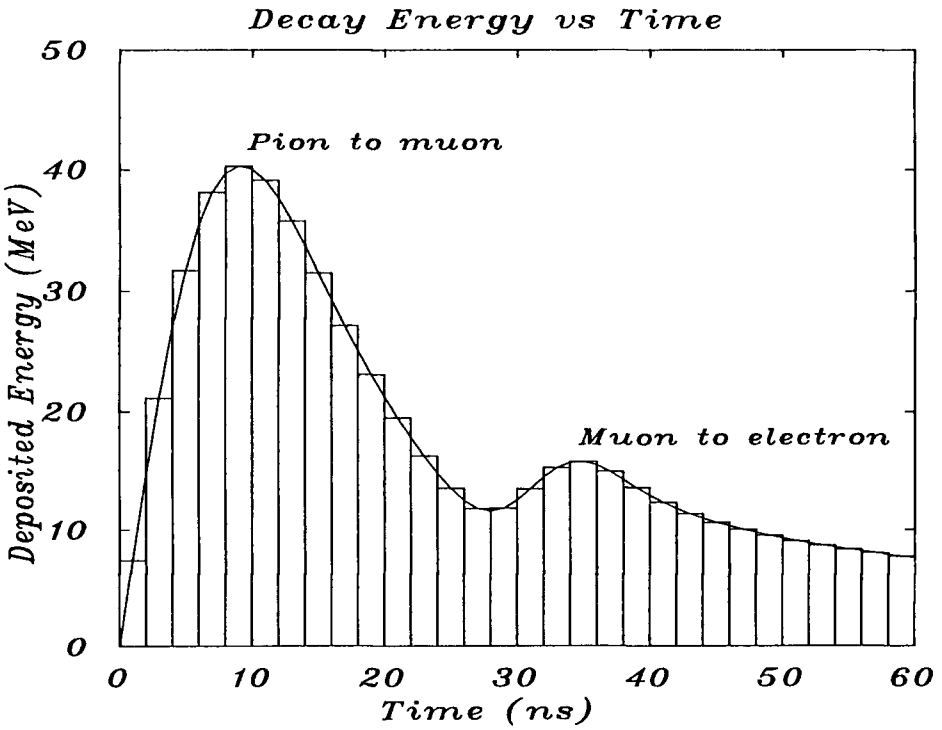

Figure A.2: The ideal output waveform for a pion to muon to electron decay sequence obtained from a photomultiplier tube attached to the end of the scintillation counter range stack. The leading peak corresponds to the energy deposited by a pion to muon decay and the trailing peak corresponds to the energy deposited by the subsequent muon to electron decay. The vertical bars represent discrete pulse amplitudes obtained for a 2 nanosecond sampling rate [62].

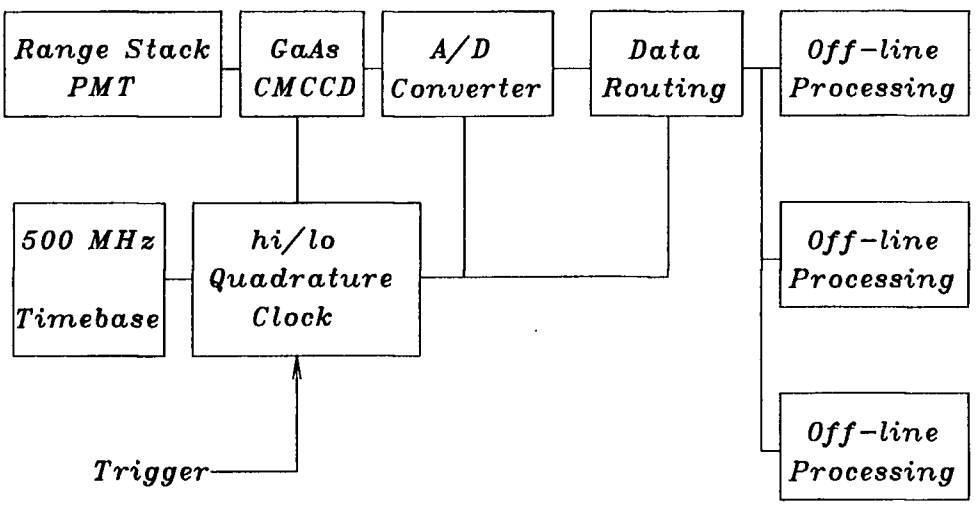

Figure A.3: A system block diagram of the GaAs CMCCD based data acquisition system for the analog to digital conversion of a signal from a range stack photomultiplier tube [65].

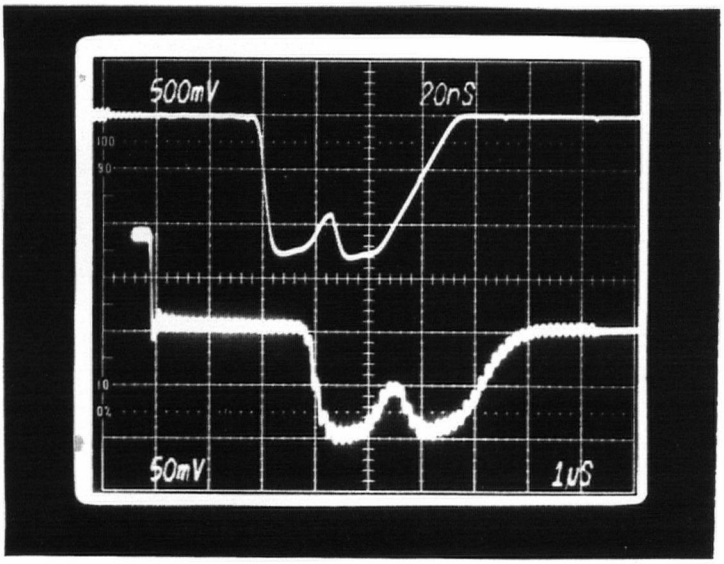

Figure A.4: The 64-pixel, 4-phase GaAs CMCCD providing frequency compression. The input signal along the upper trace (20 ns/cm) acquired at 483 MHz consists of two superimposed 30 ns pulses. The output signal along the lower trace (1 μs/cm) shows the processed input signal after frequency compression.

vary from zero to many tens of nanoseconds. A data acquisition system employing a 64-pixel, 4-phase GaAs CMCCD is currently being developed at TRIUMF for recording these waveforms.

A block diagram of the GaAs CMCCD data acquisition system [65] is shown in Figure A.3. In this application the GaAs CMCCD provides frequency compression of a 250 MHz band-limited analog input signal. The input signal applied to the CMCCD is obtained from a photomultiplier tube attached to the scintillation counter range stack. An externally generated acquisition trigger pulse enables the application of a 500 MHz high frequency clock to the CMCCD. The acquisition cycle occurs for 128 nanoseconds filling the CMCCD with sixty-four discrete samples of the input signal. The two nanosecond resolution of the input signal is considered sufficient for discriminating the two energy peaks that are observed during the pion to muon to electron decay se-

quence [62]. Subsequent to the completion of the data acquisition cycle, a 7.81 MHz low frequency clock pulse burst is applied to the CMCCD compressing the acquired signal by a factor of sixty-four. The compressed signal is transmitted to an analog to digital converter and the binary data resulting from the analog to digital transformation is routed to a data bus for sparse data processing and distribution to off-line computer resources. Figure A.4 shows an oscillograph illustrating the preliminary results obtained for a 64-pixel, 4-phase GaAs CMCCD operating in the frequency compression mode.

Appendix B

Polar Transformation of $V(y)$

The complex harmonically varying surface potential is given as

$$V(y,\omega) = \frac{\sinh\left[(L_g - y)\gamma(\omega)\right]}{\sinh[L_g\gamma(\omega)]} V_0 \quad . \tag{B.1}$$

where the factor $e^{\jmath\omega t}$ has been suppressed. Let

$$(L_g - y)\gamma(\omega) = a(y,\omega) + \jmath b(y,\omega) \quad \text{and} \tag{B.2}$$

$$L_g\gamma(\omega) = c(\omega) + \jmath d(\omega) \tag{B.3}$$

with $\gamma(\omega)$ defined as

$$\gamma(\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}}\right) \exp\left[\frac{\jmath}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}}\right)\right] \quad . \tag{B.4}$$

The functions $a(y,\omega)$, $b(y,\omega)$, $c(\omega)$ and $d(\omega)$ are

$$a(y,\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}}\right)^{\frac{1}{2}} (L_g - y) \cos\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}}\right)\right] \tag{B.5}$$

$$b(y,\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}}\right)^{\frac{1}{2}} (L_g - y) \sin\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}}\right)\right] \tag{B.6}$$

$$c(\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}}\right)^{\frac{1}{2}} L_g \cos\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}}\right)\right] \tag{B.7}$$

$$d(\omega) = \left(\frac{\omega R_{CM} C_D}{\sqrt{1 + (\omega R_{CM} C_{CM})^2}}\right)^{\frac{1}{2}} L_g \sin\left[\frac{1}{2} \arctan\left(\frac{1}{\omega R_{CM} C_{CM}}\right)\right] \quad . \tag{B.8}$$

Substitute equation B.2 and equation B.3 into equation B.1 yields

$$\begin{aligned} V(y,\omega) &= \frac{\sinh(a + \jmath b)}{\sinh(c + \jmath d)} V_0 \\ &= \frac{e^a e^{\jmath b} - e^{-a} e^{-\jmath b}}{e^c e^{\jmath d} - e^{-c} e^{-\jmath d}} V_0 \\ &= \frac{e^a\left[\cos(b) + \jmath \sin(b)\right] - e^{-a}\left[\cos(b) - \jmath \sin(b)\right]}{e^c\left[\cos(d) + \jmath \sin(d)\right] - e^{-c}\left[\cos(d) - \jmath \sin(d)\right]} V_0 \\ &= \frac{\sinh(a)\cos(b) + \jmath \cosh(a)\sin(b)}{\sinh(c)\cos(d) + \jmath \cosh(c)\sin(d)} V_0 \end{aligned} \tag{B.9}$$

Transforming equation B.9 into polar form yields

$$V(y,\omega) = \frac{\sqrt{\sinh^2(a)\cos^2(b) + \cosh^2(a)\sin^2(b)}\angle \arctan\left(\frac{\cosh(a)\sin(b)}{\sinh(a)\cos(b)}\right)}{\sqrt{\sinh^2(c)\cos^2(d) + \cosh^2(c)\sin^2(d)}\angle \arctan\left(\frac{\cosh(c)\sin(d)}{\sinh(c)\cos(d)}\right)} V_0 \quad . \tag{B.10}$$

Using the trigonometric identities

$$\sinh^2(z) = \cosh^2(z) - 1 \quad \text{and} \tag{B.11}$$

$$\sin^2(z) = 1 - \cos^2(z) \tag{B.12}$$

gives

$$V(y,\omega) = V_0 H(y,\omega)\angle\Theta(y,\omega) \tag{B.13}$$

where $H(y,\omega)$ is the normalized magnitude of the surface potential

$$H(y,\omega) = \left(\frac{\cosh^2[a(y,\omega)] - \cos^2[b(y,\omega)]}{\cosh^2[c(\omega)] - \cos^2[d(\omega)]}\right)^{\frac{1}{2}} \tag{B.14}$$

and $\Theta(y,\omega)$ is the phase shift of the surface potential

$$\Theta(y,\omega) = \arctan\left(\coth[a(y,\omega)]\tan[b(y,\omega)]\right) - \arctan\left(\coth[c(\omega)]\tan[d(\omega)]\right) \quad . \tag{B.15}$$

Appendix C

Newton's Method

Newton's method [39] is a numerical technique for finding the roots of a general function $f(\zeta) = 0$ and is described in this appendix.

Consider a point ζ_i that is in the vicinity of a root of the function $f(\zeta)$. The function $f(\zeta)$ can be expanded in a Taylor series about the point ζ_i to give

$$f(\zeta) = f(\zeta)|_{\zeta_i} + (\zeta - \zeta_i)f'(\zeta)|_{\zeta_i} + \cdots + \frac{1}{m!}(\zeta - \zeta_i)^m f^{(m)}(\zeta)|_{\zeta_i} + \cdots \quad . \tag{C.1}$$

A root of the equation $f(\zeta) = 0$ can be obtained approximately by replacing $f(\zeta)$ with the first two terms of the expansion given in equation C.1

$$f(\zeta)|_{\zeta_i} + (\zeta - \zeta_i)f'(\zeta)|_{\zeta_i} = 0 \quad . \tag{C.2}$$

Rearranging equation C.2 and performing the function evaluations at ζ_i gives

$$\zeta = \zeta_i - \frac{f(\zeta_i)}{f'(\zeta_i)} \quad . \tag{C.3}$$

The value of ζ computed in this manner is an improved estimate for the original root ζ_i of the function $f(\zeta)$, and can replace ζ_i in equation C.3 to provide an even better estimate for the root. This can be written in the generalized form

$$\zeta^{l+1} = \zeta^l - \frac{f(\zeta^l)}{f'(\zeta^l)} \tag{C.4}$$

from which the correction factor for the l^{th} iterate is

$$\delta\zeta^l = \zeta^{l+1} - \zeta^l \quad . \tag{C.5}$$

From equations C.4 and C.5 one obtains

$$f(\zeta^l) + \delta\zeta^l f'(\zeta^l) = 0 \tag{C.6}$$

which forms the basis of the Newton iteration technique for numerically solving the set of finite difference equations listed in Table IV.

Appendix D

Detailed Device Fabrication Procedure

1. Ohmic contact formation

1.1— 3 min. immersion in an ultrasonic acetone bath.

1.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

1.3— 1 min. N_2 wafer dry.

1.4— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4110 photoresist.

1.5— Softbake the photoresist coated wafer in a forced air oven @ 90 ± 2 °C for 30 min.

1.6— Expose the photoresist coated wafer to 405 nm, 4.5 $mWcm^{-2}$ ultraviolet light for 14 sec through the 'ohmic contact' mask.

1.7— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

1.8— Immerse the wafer in a 20 ml:200 ml, NH_4OH:DI H_2O oxide etch bath for 30 sec.

1.9— 1 min. DI H_2O rinse and subsequent 1 min. N_2 wafer dry.

1.10— Sequentially evaporate the following metal films under high vacuum

1.10.1— 1150 Å Au-Ge (12 wt. % Ge),

1.10.2— 200 Å Ni,

1.10.3— 1400 Å Au.

1.11— 3 min. immersion in an ultrasonic acetone bath to lift-off the unwanted metal.

1.12— 3 min. immersion in an ultrasonic acetone bath.

1.13— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

1.14— 1 min. N_2 wafer dry.

1.15— Alloy ohmic contacts @ 468 °C for 1.5 min. in a zone controlled quartz tube furnace with 0.8 l/min N_2 flowing through the tube.

2. Proton isolation implants

2.1— 3 min. immersion in an ultrasonic acetone bath.

2.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

2.3— 1 min. N_2 wafer dry.

2.4— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4620 photoresist.

2.5— Softbake the photoresist coated wafer in a forced air oven @ 90 ± 2 °C for 30 min.

2.6— Expose the photoresist coated wafer to 405 nm, 4.5 $mWcm^{-2}$ ultraviolet light for 98 sec through the 'proton implant' mask

2.7— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

2.8— Postbake the photoresist coated wafer in a forced air oven @ 120 ± 2 °C for 30 min.

2.9— Perform the multiple-energy proton implants

2.9.1— $E_1 = 180$ keV, $D_1 = 10^{13}$ cm^{-2},

2.9.2— $E_2 = 90$ keV, $D_2 = 10^{13}$ cm^{-2},

2.9.3— $E_3 = 30$ keV, $D_3 = 5 \cdot 10^{13}$ cm^{-2}.

2.10— 15 min. immersion in a hot N-methyl-2-pyrrolidone bath to remove the photoresist.

3. Metal/GaAs Schottky barrier formation

3.1— 3 min. immersion in an ultrasonic acetone bath.

3.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

3.3— 1 min. N_2 wafer dry.

3.4— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4110 photoresist.

3.5— Softbake the photoresist coated wafer in a forced air oven @ 90 ± 2 °C for 30 min.

3.6— Expose the photoresist coated wafer to 405 nm, 4.5 $mWcm^{-2}$ ultraviolet light for 14 sec through the 'metal/GaAs Schottky barrier' mask.

3.7— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

3.8— Immerse the wafer in a 20 ml:200 ml, NH_4OH:DI H_2O oxide etch bath for 30 sec.

3.9— 1 min. DI H_2O rinse and subsequent 1 min. N_2 wafer dry.

3.10— Sequentially evaporate the following metal films under high vacuum

3.10.1— 500 Å Ti,

3.10.2— 100 Å Pt,

3.10.3— 2150 Å Au.

3.11— 15 min. immersion in a hot N-methyl-2-pyrrolidone ultrasonic bath to lift-off the unwanted metal.

3.12— 5 min. immersion in an ultrasonic acetone bath.

4. Cermet/GaAs Schottky barrier formation

4.1— 3 min. immersion in an ultrasonic acetone bath.

4.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

4.3— 1 min. N_2 wafer dry.

4.4— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4210 photoresist.

4.5— Softbake the photoresist coated wafer in a forced air oven @ 90 ± 2 °C for 30 min.

4.6— Expose the photoresist coated wafer to 405 nm, 4.5 $mWcm^{-2}$ ultraviolet light for 28 sec through the 'cermet/GaAs Schottky barrier' mask.

4.7— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

4.8— Postbake the photoresist coated wafer in a forced air oven @ 120 ± 2 °C for 30 min.

4.9— Immerse the wafer in a 20 ml:200 ml, NH_4OH:DI H_2O oxide etch bath for 30 sec.

4.10— 1 min. DI H_2O rinse and subsequent 1 min. N_2 wafer dry.

4.11— rf diode sputter Cr-SiO (45 wt. % Cr.) onto the surface
—frequency: 13.56 MHz,
—background chamber pressure: $\leq 2 \cdot 10^{-6}$ mTorr,
—gas: Ar,
—deposition chamber pressure: 10 mTorr,

—rf forward power: $\approx$ 250 Watts, rf reflected power: $\leq$ 13 Watts resulting in a target bias of -800 volts,
—Precondition time: 24 hrs.,
—Deposition time: 30 min.

4.12— 5 min. immersion in a hot N-methyl-2-pyrrolidone ultrasonic bath to lift-off the unwanted cermet film.

4.13— 5 min. immersion in an ultrasonic acetone bath.

5. Interconnect via formation

5.1— 3 min. immersion in an ultrasonic acetone bath.

5.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

5.3— Immerse the wafer in a 20 ml:200 ml, NH_4OH:DI H_2O oxide etch bath for 30 sec.

5.4— 1 min. DI H_2O rinse and subsequent 1 min. N_2 wafer dry.

5.5— Spin-coat the wafer @ 4000 RPM for 1 min. with Du Pont PYRALIN PI-2550 polyimide diluted to a volume ratio of 1:1 with Du Pont T-9039 thinner.

5.6— Imidize polyimide in a forced air oven @ 250 $\pm$ 2 °C for 3 hrs.

5.7— Evaporate 600 Å of Ti onto the polyimide surface under high vacuum.

5.8— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4110 photoresist.

5.9— Softbake the photoresist coated wafer in a forced air oven @ 90 $\pm$ 2 °C for 30 min.

5.10— Expose the photoresist coated wafer to 405 nm, 4.5 mWcm^{-2} ultraviolet light for 14 sec through the 'interconnect vias' mask.

5.11— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

5.12— Plasma etch the interconnect vias
—background chamber pressure: $\leq$ 25 mTorr,
—rf power: 150 Watts,

5.12.1— P_{CF_4} = 256 mTorr, P_{O_2} = 23 mTorr and $P_{chamber}$ = 279 mTorr for 90 sec.

5.12.2— P_{CF_4} = 0 mTorr, P_{O_2} = 250 mTorr and $P_{chamber}$ = 250 mTorr for 10 min.

5.12.3— P_{CF_4} = 256 mTorr, P_{O_2} = 23 mTorr and $P_{chamber}$ = 279 mTorr for 90 sec.

6. Second level interconnect metal formation

6.1— 3 min. immersion in an ultrasonic acetone bath.

6.2— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

6.3— 1 min. N_2 wafer dry.

6.4— Spin-coat the wafer @ 4000 RPM for 30 sec. with AZ 4210 photoresist.

6.5— Softbake the photoresist coated wafer in a forced air oven @ 90 ± 2 °C for 30 min.

6.6— Expose the photoresist coated wafer to 405 nm, 4.5 $mWcm^{-2}$ ultraviolet light for 28 sec through the 'second level metallization' mask.

6.7— Spray develop the exposed photoresist using AZ 400K developer diluted to a volume ratio of 1:3 with DI H_2O.

6.8— Sequentially evaporate the following metal films under high vacuum

6.8.1— 500 Å Ti,

6.8.2— 4000 Å Au.

6.9— 3 min. immersion in an ultrasonic acetone bath to lift-off the unwanted metal.

6.10— 3 min. immersion in an ultrasonic acetone bath.

6.11— 3 min. sequential immersion in each of hot trichloroethylene, hot acetone, and hot 2-propanol baths.

6.12— 1 min. N_2 wafer dry.

Appendix E

Test Circuit for VHF Operation

The GaAs CMCCD was operated in the VHF band at 100 MHz using the test circuit illustrated in Figure E.1.

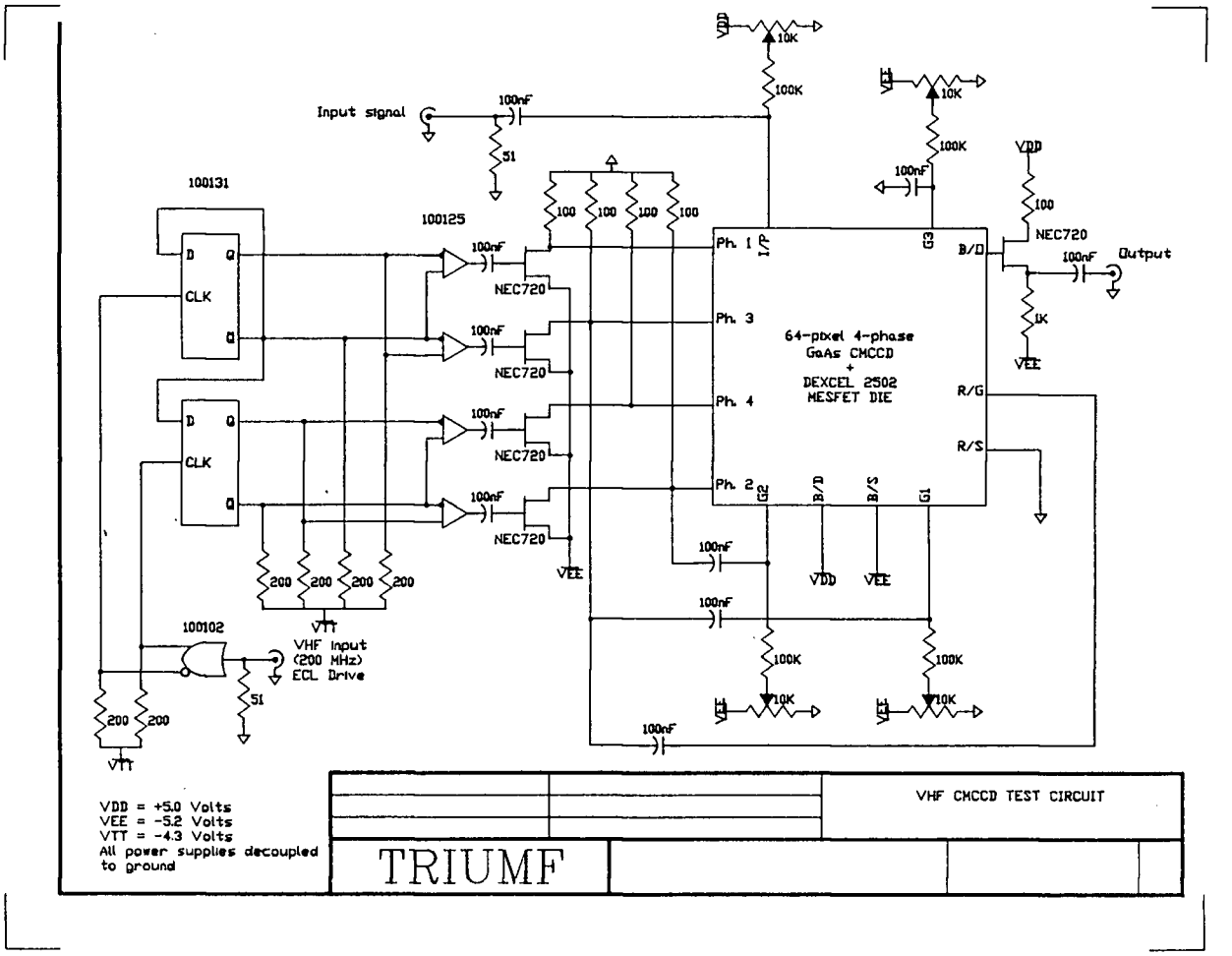

Figure E.1: The schematic diagram of the test circuit used to operate the CMCCD in the VHF band.