SELF-ALIGNED GALLIUM ARSENIDE MESFETs FOR MICROWAVE INTEGRATED CIRCUITS

by

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ABSTRACT

A refractory self-aligned gate fabrication process for gallium arsenide MESFETs has been developed and applied to a sample and hold circuit. The process has been shown to reduce the parasitic end resistance of MESFETs which can be a limiting factor in their microwave performance. A mask set was designed to be compatible with Cascade Inc. probes which allowed on chip microwave measurements to be made. Usable gain was measured up to 18GHz on FETs and 5GHz on buffer amplifiers with the microwave probes at the Communications Research Centre in Ottawa Ontario. The microwave probes were also used to test sample and hold operation. The maximum tested sampling rate was limited by the test equipment to 250 MHz.

The fabrication process included a plasma etch for producing an undercut 'T' gate structure for self-aligned ion implantation. A method of sputtering a thermally stable alloy of TiW refractory metal was developed to provide suitable Schottky contacts to GaAs. It was found that a rapid thermal anneal following the self-aligned implant maintained suitable TiW/GaAs Schottky characteristics and yielded MESFETs with reduced end resistance when compared to those fabricated by the more conventional selective implant process. A technique was developed to reduce the gate resistance of self-aligned MESFETs using an evaporated metal overlayer. Also, procedures for fabricating airbridges using a single evaporation and Metal-Insulator-Metal (MIM) capacitors using silicon nitride as the dielectric were developed.
The effect of gate resistance on the microwave performance of the self-aligned MESFETs was investigated by modeling with the EEsof Inc. microwave software package, Touchstone. The modeling showed that self-aligned MESFETs are capable of giving greater high frequency gain than are selective implant devices with the same design geometry. The operation of the sample and hold circuit was simulated using a version of SPICE that included the Sussman Fort GaAs MESFET model. The simulations showed that the sample and hold could be used for gigahertz sampling.
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1. INTRODUCTION

The object of the work described in this thesis was to examine the application of a gallium arsenide self-aligned implantation technology to microwave devices and in particular to a GaAs sample and hold circuit. Devices were fabricated using a refractory metal gate process. Static and microwave characteristics were measured and compared to those obtained from devices fabricated by the more conventional selective implant process. Modeling was used to determine the ultimate performance that can be achieved with the technology.

1.1 GaAs MESFET Technologies

The majority of work on GaAs self-aligned fabrication technologies has been related to the development of enhancement mode MESFETs for digital logic circuits. The first GaAs digital logic approaches, Buffered FET Logic (BFL) and Schottky Diode FET Logic (SDFL), implemented only depletion mode devices. These approaches were successful in achieving high speeds using GaAs [1,2] however, high power dissipation prevented their use in VLSI applications.

The low power GaAs logic approach of Direct Coupled FET Logic (DCFL) using Enhancement-Depletion FET Logic (EDFL) requires the development of a consistent fabrication technique for enhancement mode devices [3]. Enhancement mode devices require very tight control of the threshold voltage (typically 0.1 - 0.2V) in order to allow for adequate voltage swing and
noise margins [4]. Also it is necessary to make the unmodulated channel of an enhancement mode device short because it is depleted by surface state pinning of the Fermi level and is therefore highly resistive [5].

The most important methods used to reduce the unmodulated channel resistance are the recessed gate and the self-aligned implantation technologies. In the recessed gate process (figure 1.1), a single implant is used to dope active regions n type or a wafer with an n type epitaxial layer is used. A window is opened over channel regions using the photoresist pattern that is used to define the gates of the MESFETs. The channel is etched so that MESFETs with the desired threshold voltage are obtained when the Schottky gate metal is deposited. A difficulty with the recessed gate process is that the gate recess etch must be well characterized in order to give reproducible threshold voltages of MESFETs [6].

Two basic types of self-aligned implant technologies for GaAs MESFETs have been demonstrated. One, the "Self-Aligned Implantation for N⁺-layer Technology," or SAINT process [7] uses a temporary gate structure to block the self-aligned implant. The gate is removed for the post-implant anneal, then a second gate is deposited to form the Schottky contact. The other process uses a refractory metal gate which must withstand the high temperature post-implant anneal.

The refractory self-aligned gate process (figure 1.2) involves undercutting a 'dummy' gate [8] so as to leave a small lateral gap between the self-aligned source/drain n⁺ implant and the gate itself. This is done to decrease gate capacitance and to increase the reverse breakdown voltage of the Schottky
contacts while minimizing the length of the unmodulated channel. The reduced length of the unmodulated channel can be expected to increase the device transconductance over that achieved using a selective implant fabrication technology (figure 1.3). For a MESFET fabricated using a selective implant process, the lateral gap between the source/drain n+ implant and the gate is defined by the mask layout and cannot be reduced beyond the limits set by lithography and mask alignment.

- pattern for device wells
- implant
- anneal

- pattern for ohmic contacts
- evaporate and liftoff AuGe
- alloy

- pattern for Schottky gate
- etch channel
- evaporate and liftoff gate

- completed MESFET

Figure 1.1. Recessed gate fabrication process
Figure 1.2. Refractory self-aligned gate fabrication process
Figure 1.3. Selective implant fabrication process
1.2. Microwave Performance

An equivalent circuit that was used by Liechti [9] for high-frequency modeling of the GaAs MESFET in the common-source configuration is shown in figure 1.4. The figure shows both the intrinsic model as well as the extrinsic model which includes parasitic elements.

![Intrinsic Model Diagram](image)

Figure 1.4. A high frequency equivalent circuit for a GaAs MESFET in the common-source configuration.

Using the intrinsic model shown in figure 1.4 and assuming the feedback capacitance $C_{dg}$ is very small and can be neglected, the cutoff frequency $f_T$ where the current through $C_{gs}$ is equal to $g_m V_g$ is given by

$$f_T = \frac{g_m}{2 \pi C_{gs}} = \frac{1}{2 \pi \tau} \quad [1.1]$$
Here $\tau = L/v_0$ is the carrier transit time through the channel, $v_0$ is the electron saturation drift velocity and $L$ is the modulated channel length. The maximum frequency of oscillation $f_{\text{max}}$ where unity power gain is achieved is given by:

$$f_{\text{max}} = \frac{f_T}{2} \left( \frac{R_{ds}}{R_i} \right)^{1/2} \quad [1.2]$$

Equation 1.2 can be generalized [9] for the non-unilateral extrinsic GaAs MESFET model as

$$f_{\text{max}} = \frac{f_T}{2} \left( \frac{R_{ds}}{R_g + R_i + R_s + R_{ds} (2\pi f_{\text{max}} R_g C_{dg})} \right)^{1/2} \quad [1.3]$$

It can be seen that the length of the gate $L$ and the source series resistance $R_s$ are critical in determining the frequency response of a MESFET. The refractory self-aligned gate technique can yield MESFETs with low source series resistance [10]. Also, self-aligned gates can be made smaller using optical lithography than can those fabricated by selective implant or recessed gate techniques since the actual gate length is undercut from the mask gate length. As a result, self-aligned devices have application in microwave circuits. Refractory gate metal can be more resistive than the gate metalizations used in other processes and as a result, the effective gate series resistance $R_g$ may be greater. Plating the refractory gate metal may be desirable if the effect of the gate resistance on the microwave performance of the device is significant.
1.3 The Sample and Hold

The basic structure of a sample and hold circuit consists of a sampling switch and a hold capacitor (figure 1.5.).

![Diagram of sample and hold circuit]

Figure 1.5. Basic structure of sample and hold

The most common application of sample and hold circuits is in analogue to digital conversion. A sample and hold is used at the front end of an analogue to digital converter (ADC) to relieve some of the aperture time problems associated with ADCs. The short acquisition time of the sample and hold provides a constant signal level period for A/D conversion to take place.

1.4 Sample and Hold Performance

The main measures of a sample and hold's performance are its acquisition time, input impedance, droop rate, and output impedance.

The acquisition time is the key performance specification of a sample and hold. It is the time required to
store on the hold capacitor the level of the signal present at the sample and hold input. The acquisition time limits the maximum sampling frequency of the sample and hold.

The importance of the sample and hold input impedance depends upon the impedance of the input signal path. For example, if the input signal is presented to the sample and hold on a high impedance line and is required to supply the current to charge the hold capacitor, then the frequency response of the sample and hold may be very limited.

The droop rate is the rate of decay of the hold node potential. It can become important if it approaches the sampling rate.

The output impedance is important if the sample and hold must drive current to a load. If the hold capacitor is directly connected to the output, then the load may affect the droop rate.

1.5 Sample and Hold Structures

The most common types of sampling switches used in sample and holds are diode bridges and FETs. A major disadvantage of the diode bridge arrangement is the fact that the diode bridge must be very well balanced to give an accurate sampled representation of the input signal at the output. Variations in characteristics across a wafer surface could therefore cause integrated diode bridges to give inconsistent results. Also, complementary strobe pulses are required to prevent pulse feedthrough from being observed on the output.
GaAs diode bridge sample and holds have been described by Poulton et al [11] and by Wong and Fawcett [12].

The MESFET sampling switch (figure 1.6) is often implemented in GaAs for high speed sampling. The advantages of a MESFET over the diode bridge arrangement are that it requires only a single sampling pulse and that it is not as sensitive to fabrication nonuniformities. One disadvantage of using a MESFET as the sampling gate is that its gate to source capacitance ($C_{gs}$) acts as a voltage divider with the hold node capacitance. As a result, the sampling pulse is fed through to the hold node to a certain extent. GaAs MESFET sampling switches are described by Akers et. al. [13] and Swierkowski et al [14].
The sample and hold circuit followed that used by Barta and Rode [15]. The circuit consisted of a GaAs MESFET sampling gate followed by a hold capacitor and a buffer amplifier stage (figure 2.1). The layout was modified from that of Rutherford [16] in order to allow high frequency testing of sample and hold performance using Cascade Inc. probes. The probes allow on chip microwave measurements to be made but require a regular contact pad arrangement.

Figure 2.1. Sample and hold schematic diagram.
The sample and hold circuit was designed for implementation in both selective and self-aligned implant integrated circuit technologies using eight mask levels.

1) Registration for subsequent level alignment.
2) n⁻ implant FET channels.
3) TiW self-aligned gates, MIM bottoms.
4) n⁺ implant FET sources/drain.
5) AuGe/Ni ohmic contacts.
6) Dielectric MIM insulator.
7) Schottky diodes, MIM tops, airbridge footings.
8) Au plating airbridge body, bonding pad thickening.

2.1 The Sampling Gate

Barta and Rode addressed the problem of pulse feedthrough with a MESFET sampling gate by the use of a triple gate sampling MESFET as shown in figure 2.2. They found that feedthrough of the sampling pulse to the input and to the hold node of the sample and hold was smaller when the pulse was applied to the centre 'sampling' gate rather than the outer 'guard' gates. Rutherford showed using SPICE simulations that the reduction in pulse feedthrough could be attributed to momentary forward conduction of the guard gates which remove carriers displaced by the pulse. For comparative purposes, single and triple gates, all of 1µm length, were included in the sample and hold layouts.
Another effect examined by Rutherford was that of signal propagation on the gate. TiW gate metal is quite resistive ($\approx 3\Omega$/square) and being over the channel it has approximately $1\text{fF}/\mu\text{m}^2$ capacitance per unit area depending on gate bias. The transmission line nature of the gate causes a phase shift of an applied signal along its width. The effect is not important for small width gates such as those used in digital integrated circuits, but becomes important for analogue and power MESFETs. SPICE simulations show that a pulse input would take about 20ps to propagate 100$\mu$m along a gate of length 0.5$\mu$m.

To reduce this phase shift effect, the sampling gate designed by Rutherford was driven by a contact pad which was connected at the center of the gate's 60 $\mu$m width. The t-junction structure of the sampling gate was not compatible with the Cascade Inc. microwave probes because it required the source contact pad of the sampling gate to be split. This
restriction on contact pad layout made it necessary to drive the gate of the sampling MESFET from one end in the present design.

2.2 The Hold Capacitor

The input time constant of the sample and hold limits the signal frequency that can be sampled. The input time constant is approximately given by the product of the sampling MESFET channel resistance and the capacitance of the hold node. The value of the hold capacitance was chosen to give an input time constant of 25ps for both the triple and single sampling gate arrangements. The hold node capacitance is approximately half due to parasitic and depletion layer capacitance and half due to the fixed hold capacitance.

A 60μm wide FET typically has a channel resistance in the order of 100Ω. The hold node capacitor for such a sampling FET was then set to 0.13pF in order to give a total node capacitance of 0.25pF. If the value of the hold capacitor were reduced significantly from this value, nonlinearities in the depletion layer capacitance might cause signal distortion. In addition, pulse feedthrough and the signal droop rate would increase.

Two types of hold node capacitors were incorporated in the sample and hold layouts. The first consisted of 2μm wide interdigitated fingers of Schottky metal with 2μm gaps (figure 2.3).
Figure 2.3. Interdigitated capacitor layout.

The second was a metal insulator metal (MIM) structure (figure 2.4). An MIM capacitor requires less substrate area than an interdigitated capacitor of equal value but is more difficult to fabricate. Pinholes in the dielectric could cause shorting of its terminals. The TiW metalization could be used as the MIM bottom plate or AuGe/Ni could be employed as in Rutherford's design. AuGe tends to become quite rough after alloying to form ohmic contacts so the yield of these capacitors is quite low as reported by Barta and Rode [15]. TiW on the other hand remains smooth even after annealing and therefore was used in this design.
2.3 Buffer Amplifiers

A sample and hold circuit can be as simple as a sampling switch and a hold capacitor. However, if the impedance of the signal source is high, it may be necessary to add a buffer amplifier in front of the sampling switch to provide the current needed to charge the hold capacitor. Similarly, if the sample and hold is required to drive significant current to the output, a buffer may be needed so that the hold capacitor sees a high impedance at the output. This is the case in A/D conversion where sample and hold's are added in front of flash quantizers which have large input capacitance [17]. A sample and hold with input and output buffers is shown schematically in figure 2.5.
Figure 2.5. Sample and hold with buffer amplifiers.

An output buffer amplifier was implemented in the design to give about 3dB gain and to insure that the hold node droop rate was unaffected by the load. The amplifier was a buffered FET logic inverter with feedback and has been examined by Hornbuckle, Van Tuyl and Estreich [18-21]. A similar amplifier could have been added before the sampling gate but was not because the sample and hold has a high input impedance as is. The sample and hold appears as a 0.25pF capacitor through 100Ω. Provided the input signal path has sufficient current drive, the buffer would only serve to increase circuit complexity.

2.4 Layout

The pad arrangements for sample and holds, an isolated buffer amplifier and discrete MESFETs were designed to be compatible with the Cascade Inc. microwave probes.
Elements 1-8 on the chip layout shown in figure 2.6 were for implementation in a self-aligned gate technology whereas 9-11 were selectively implanted. 12-14 were diagnostic elements including Van Der Pauw cross, fat FET, transmission line, and ring-dot structures. A TiW stepped resistor was included so that the resistivity of the self-aligned gate metalization could be determined.
3. FABRICATION

3.1 Special Structures

Before performing a full fabrication run, experiments were conducted to develop procedures for making structures that were required for the sample and holds.

3.1.1 Fine Line Resist Profiles

The most common technique for patterning metalizations on GaAs is lift-off. The lift-off process involves opening windows in a layer of positive photoresist by exposure to UV light followed by development. The metal is deposited on the wafer by evaporation. The wafer is then soaked in a photoresist stripper such as acetone. The metal that was deposited on top of the photoresist is lifted off leaving behind metal only where the windows were opened to the substrate.

Difficulties can arise in lift-off if the sidewall profile of the patterned photoresist is rounded or tapered. Evaporated metal will then form a continuous film which may not lift off or may leave metal 'wings' on the edges of the defined pattern. It is therefore most desirable to create an undercut or reverse tapered sidewall resist profile. This can be done using techniques that involve two levels of resist or dielectric assisted lift-off [22], however a chlorobenzene technique was employed in this work.
An overhang structure can be created in a single layer of resist by soaking the resist in a developer inhibitor such as chlorobenzene prior to development. The surface layer of the resist is modified by the soak so that it develops slower than the underlying resist so as to leave an overhang. Figure 3.1 is an SEM of a 1 μm resist profile produced using the chlorobenzene technique. It shows good vertical sidewalls and undercut.

Figure 3.1. SEM showing resist profile of 1μm lines with 2 μm gaps.
3.1.2 Self-aligned 'T' Gate Structure

A 'T' gate structure is not necessary for the refractory self-aligned gate process. A refractory gate with vertical sidewalls may serve both as the mask for the heavy n⁺ source/drain implant and as the Schottky gate itself [23]. It is advantageous however if a T gate structure (figure 3.2) is used to leave a lateral gap between the n⁺ regions and the refractory gate. The effect of the gap is to decrease gate capacitance, reduce MESFET short channel effects, and increase the reverse breakdown voltage [24] so that larger values of $V_{ds}$ may be switched when compared with MESFETs fabricated with no T gate structure. The lateral gap also helps to reduce gate orientation sensitivity [25,26].

The technique used to produce the T gate structure was similar to that used by Sadler and Eastman [10] except that a CF₄ plasma etch of the TiW was used to produce the undercut rather than a reactive ion etch.
Figure 3.2. Production of 'T' gate structure for self-aligned implant.

The most critical aspect of this process was in determining the duration of the plasma etch required to give suitable undercut. The situation was complicated when the composition and thickness of the refractory metal was changed.
For this reason, the wafer was optically checked periodically during the etching process to determine an appropriate etch time. An SEM of a 'T' gate structure produced using the described process is shown in figure 3.3.

Figure 3.3. SEM showing 'T' gate structure for self-aligned ion implantation.
3.1.3. Post-anneal Gate Thickening

For the best microwave performance of a MESFET, it is desirable that the resistivity of the gate metal be small as discussed in section 1.2. The simplest way to obtain a highly conductive gate would be to leave the 'dummy' gate of the 'T' gate structure in place during and after annealing the self-aligned source/drain n⁺ implant. Unfortunately, severe interdiffusion and alloying of metal occurred during the annealing cycle when either Cr or Pd/Au dummy gates were used. Sadler [27] reported similar effects when Al, Ni, Au, or Pt 'T' gate tops were left in place during annealing. As a result, Al dummy gates were used to serve as the n⁺ implant mask, then they were removed for the anneal.

Geissberger et al. [28] deposited metal on top of self-aligned gates after annealing by planarizing a layer of SiON then patterning and evaporating an overlayer of Au. Rutherford [16] suggested an electroplating technique that required all MESFET gates to be contacted by a removable metal interconnect web and all areas where plating was not desired to be masked off.

In this work, an evaporation method using two levels of photoresist was developed for obtaining a metal overlayer on the self-aligned gates. The technique involved planarizing and hardbaking a lower level of resist in order to prevent the overlayer from contacting the n⁺ regions and to allow line width and alignment tolerances on the overlayer to be relaxed. The procedure is outlined in figure 3.4.
Figure 3.4. Procedure for depositing a metal overlayer on self-aligned gates.

An SEM of a TiW self-aligned gate with an Al overlayer is shown in figure 3.5. The structure was not symmetric because precise alignment of the Al to the TiW was not possible. The yield of gates with the overlayer was low due to poor adhesion of the Al to the TiW. It is possible that the planarization etch was not sufficient to clear the resist from the top of the TiW gate.
Airbridges are an integral part of most monolithic microwave integrated circuit (MMIC) processes. They are used for making connections to the top electrode of MIM capacitors, for spiral inductors, and as a second level of metalization for interconnects. Airbridges are used because there is less parasitic capacitance associated with them than there is for metalizations on a dielectric layer.

The most common technique for producing airbridges utilizes two levels of resist, an evaporation, an etch, and an
electroplating step [29]. This procedure is outlined in figure 3.6.

Figure 3.6. Airbridge fabrication by a conventional technique.
A technique was developed to produce airbridges using two levels of resist and a single evaporation and liftoff (figure 3.7). The procedure involved a hardbake to prevent the lower level resist from being dissolved when the second level was applied. The chlorobenzene treatment was not applied to the lower level of resist so that its edge profile was rounded to give good metal sidewall coverage.

Figure 3.7. Airbridge fabrication by single evaporation and liftoff.
Gold airbridges could be made up to 1\(\mu\)m thick with this technique giving them a sheet resistivity of about 0.05\(\Omega\)/square [30]. Thicker metal is sometimes used to improve mechanical strength for long span airbridges. The sheet resistivity is not normally a concern, particularly for short span interconnects such as those employed in the sample and hold circuit. An SEM of an airbridge fabricated using the liftoff method is shown in figure 3.8.

![Figure 3.8. SEM of airbridge.](image)

3.1.5 MIM Capacitors

Metal-insulator-metal (MIM) capacitors are used extensively in MMIC designs for RF tuning and bypassing. The
MIM consists of a thin layer of dielectric sandwiched between two metal plates. Since the dielectric is generally much thinner than the bottom metal plate, the top metal plate must be connected with an airbridge in order to avoid shorting. An MIM with thick dielectric can be fabricated without the use of an airbridge [31], however such an element requires more area.

The MIMs fabricated in this work used a plasma enhanced chemical vapor deposition of approximately 800Å of silicon nitride for the dielectric layer. The top electrode of the MIM was evaporated as an airbridge footing and TiW was used as the lower electrode. Figure 3.9 shows an SEM of an MIM capacitor that was fabricated as described.

Figure 3.9. SEM of MIM capacitor
3.2 The Refractory Metal/GaAs Contact

The most critical aspect of the self-aligned implant process is that of the high-temperature-stable refractory metal gate which must exhibit good Schottky characteristics after post-implant annealing at temperatures of 800°C or greater. An elemental refractory metal such as tungsten is the most easily characterized for reproducible deposition by sputtering. Tungsten has the desirable properties of low electrical resistivity and high temperature chemical stability on GaAs [32], however it was found to crack and peel due to thermal stress when annealed [33].

An alloy of Ti$_{0.3}$W$_{0.7}$ was reported by Yokoyama et al. [34] to give better adhesion to GaAs than pure tungsten. Mukherjee et al. [35] found that if the alloy was too rich in titanium, a GaAs/Ti reaction degraded the quality of the Schottky barrier. Considerable work on other materials for the self-aligned process such as refractory metal silicides and nitrides has been published [36-41]. Also, pure tungsten has been used for self-aligned gates without adhesion problems when it was sputtered under particular conditions to reduce stress [42]. In this work, an alloy of TiW was used as the refractory metal.

A procedure involving the MSI Electronics Inc. mercury contact probe was devised to test the effects of various annealing parameters on the TiW/GaAs interface without requiring a complete fabrication run to be conducted. The mercury contact probe is used for C-V profiling without requiring electrodes to be evaporated on samples [43].
Instead, two mercury electrodes are temporarily drawn into contact with the implanted surface of a specimen. The mercury contacts to the surface act as two Schottky diodes placed back to back [44].

The series capacitance of the two Schottky junctions was measured between the mercury contacts with a Hewlett Packard model 4275A LCR meter. Since the area of one contact was much greater than that of the other, the measured capacitance was very close to the capacitance of the small contact junction. A reverse bias was applied to the small contact to allow conventional C-V curves and doping profiles to be made.

The following test procedure allowed doping profiles of implanted wafers annealed with TiW present on the surface to be obtained with a minimal number of processing steps.

1) Etch wafer surface \( \simeq 3 \mu \text{m} \).
2) Implant without patterning (blanket implant \( 3 \times 10^{12} \text{ cm}^{-2} \)).
3) Light chemical etch.
4) Sputter with TiW.
5) Anneal with TiW as encapsulant using test parameters.
6) Remove TiW in CF\(_4\) plasma.
7) Obtain doping profile with mercury probe.
3.2.1 Effect of a Furnace Anneal

Tests using the mercury probe were made on TiW encapsulated quarter wafers that had been annealed in the furnace at 800°C for 25 minutes. The TiW surface on removal from the furnace appeared to be oxidized. A residual film was observed on the GaAs substrate surface after the oxidized TiW was removed in a CF$_4$ plasma.

To prevent oxidation of the TiW surface during annealing, hydrogen gas was added to the nitrogen flow in the furnace. The gases flowed for 15 minutes with the substrates in a load lock before the boat was pushed to the heated part of the furnace. Another wait was allowed after the boat was pulled from the heated part of the furnace. Using this procedure, oxidation of the TiW surface during annealing was greatly reduced.

After a CF$_4$ plasma etch of the TiW, a residual surface film on the substrate was observed even on samples annealed in the reducing atmosphere. The film was presumed to be evidence of a high temperature GaAs/TiW reaction rather than oxidation. Doping profiles could be obtained from some areas of the samples which were apparently cleared of the surface film. The profiles showed only a tail of activated dopant as seen in figure 3.10.
Figure 3.10. Doping profile tail obtained from the mercury contact probe on a sample annealed at 800°C for 25 minutes with TiW encapsulant.

3.2.2 Effect of Rapid Thermal Anneal

Similar results were observed for quarter wafers subjected to a rapid thermal anneal (RTA) at 950°C for 5 seconds. By varying the RTA time and temperature, it was found that the amount of activated dopant observed using the mercury probe could be increased. The best results were obtained using the RTA at 850°C for 60s as shown in figure 3.11. The area under Gaussian curves fitted to doping profiles obtained at 6 positions on two wafer quarters gave an activated dose of $1.6\times10^{12} \pm 0.4\times10^{12} \text{cm}^{-2}$ or 40±10%.
3.2.3 Effect of Change of TiW Composition

Further improvement in doping activation was obtained by increasing the tungsten content of the sputter deposited TiW. The tungsten content of the sputtered film was increased by attaching a piece of tungsten foil to the sputtering target using conductive epoxy. The foil which covered approximately 50% of the surface area of the target was expected to proportionately reduce the amount of titanium in the deposited film. The mercury contact test procedure was conducted on samples sputtered with the TiW target and W foil in place then annealed in the RTA. The rapid thermal anneals were conducted on samples without encapsulation but with a GaAs wafer in proximity to provide some arsenic overpressure. It has been
found that significant out-diffusion of arsenic occurs when a capless RTA is performed with no arsenic overpressure [45]. The activated dose measured from two wafer quarters given an RTA at 950°C for 5 seconds was $2.8 \times 10^{12} \pm 0.2 \times 10^{12} \text{cm}^{-2}$ or $70 \pm 5\%$.

![Graph showing concentration versus depth](image)

**Figure 3.12.** Doping profile obtained from the mercury contact probe on a sample sputtered with W foil on the TiW target then given an RTA at 950°C for 5s.

### 3.3 The Microwave Integrated Circuit Fabrication Process

The GaAs substrates were initially etched about 3 μm to remove any damage caused by the supplier's polishing process [46]. The alignment mask was then used to pattern the wafer quarters for the registration etch. The subsequent processing steps are outlined in figure 3.13. The metal overlayer on the self-aligned gates is not shown in figure 3.13 because the procedure was not conducted until after the devices were measured. Details of the process are given in appendix A.
5.1. GaAs substrate

a) Substrate cleaned, etched, and about 300Å silicon nitride deposited.

b) Photoresist patterned for device wells then implanted n−.

c) Annealed in furnace with silicon nitride cap. Cap removed and about 3000Å of TiW sputtered on surface.

d) Patterned for dummy gates and MIM bottoms. About 5000Å Al evaporated on surface.

Figure 3.13. The microwave integrated circuit process employing self-aligned MESFETs.
Figure 3.13. continued

e) Al lifted off.

f) Undercut etched in CF₄ plasma.

g) Patterned and implanted n⁺.

b) Removed Al, annealed in RTA, patterned and evaporated AuGe ohmic contacts.
i) Lifted off AuGe, alloyed to form ohmic contacts, and deposited silicon nitride dielectric.

j) Resist defined for MIM and silicon nitride etched.

k) Ti/Pd/Au Schottky metal evaporated, and lifted off.

l) Au airbridges evaporated, sample and holds completed.

Figure 3.13. continued
Scanning electron micrographs of a microwave FET and a sample and hold circuit fabricated using the described self-aligned technique are shown in figures 3.14 and 3.15 respectively.

Figure 3.14. A self-aligned microwave FET.

Figure 3.15. A completed sample and hold amplifier.
4. MEASUREMENT AND TESTING

4.1 Static Measurements

Static measurements were made on MESFETs and diagnostic structures using a Hewlett Packard model 4145A semiconductor parameter analyzer. The measurements were used to evaluate the benefits of using the self-aligned process rather than the selective implant process. Also, measured parameters were used in the modeling of devices (chapter 5).

4.1.1 The TiW/GaAs Schottky Junction

Measurements on the TiW/GaAs Schottky junction were made to determine whether suitable characteristics existed after the rapid thermal anneal of the self-aligned n⁺ implant. It is desirable that the Schottky gate of a MESFET have a large barrier height and low reverse leakage current [47]. Enhancement mode MESFETs which operate with the gate forward biased require the barrier to be sufficiently high to allow an adequate voltage swing [48]. The reverse leakage current is important in microwave devices for low noise applications [49]. The current-voltage relationship of a diode neglecting series resistance is given by

$$I = I_o \exp \left( \frac{qV}{nkT} \right) \quad \text{for} \quad V >> \frac{kT}{q} \quad [4.1]$$

Plots of the logarithm of forward diode current I versus
applied voltage $V$ for TiW Schottky gates were linear for currents from 30nA to 100µA. The slope of the linear portion of such curves gave an ideality factor of $n = 1.20 \pm 0.05$ and a reverse leakage current of $I_r = 6 \pm 2nA$ at a reverse bias of $-0.5V$. The stated values are the mean and estimated standard deviation for data collected from 10 MESFETs on two quarter wafers.

$$\frac{kT}{q} \ln(I)$$

\[ (V) \quad -100.0 \quad E-03 \]

\[ 70.00 \quad /\text{div} \]

\[ -800.0 \quad -5000 \quad 0 \quad .2500/\text{div} \quad (V) \quad 2.000 \]

Figure 4.1. $(kT/q) \ln(I/\text{amps})$ vs. $V$ for a self-aligned TiW/GaAs Schottky junction.

The barrier heights of Schottky contacts were compared by observing the 'knee' in the diode current-voltage relationship when plotted on an appropriate current scale [50]. The knee voltage obtained for TiW/GaAs contacts was slightly higher than was obtained with the Ti/Pd/Au contacts which did not undergo thermal processing (figure 4.2).
Figure 4.2. I vs. V for TiW (solid) and Ti/Pd/Au (dashed) Schottky junctions to GaAs.

4.1.2 Sheet Resistance of Implanted Layers

Although thermal annealing must not damage the TiW/GaAs Schottky interface, it must be sufficient to activate the implanted donors and thus reduce the sheet resistivity of the source, drain and other regions doped n⁺. The sheet resistivity of n⁺ doped regions was measured using both Van der Pauw cross and transmission line structures. The Van der Pauw cross is a four terminal structure in which two terminals are used for carrying current while the other two are used as voltage probes [51]. Using the Van der Pauw technique at 10 locations on two quarter wafers fabricated by the self-aligned
process gave sheet resistances of 190±40 Ω/square for regions doped n⁺ (2.0x10¹³ ions/cm²) and 1700 ±300 Ω/square for regions doped n⁻ (3.0x10¹² ions/cm²). Sadler [27] obtained sheet resistances of 270 Ω/square and 1600 Ω/square on n⁺ and n⁻ regions respectively.

The sheet resistance of the n⁺ doped layer was also obtained from transmission line measurements at 10 locations on two quarter wafers. The transmission line structure consisted of a series of ohmic contact pads with mask spacings of 2, 4, 6, 8, and 10μm on the n⁺ implanted layer. A plot of pad to pad resistance versus spacing is shown in figure 4.3. From the slope of the fitted line, the n⁺ sheet resistance was found to be $R_{sh} = 200 ± 60$ Ω/square.

Figure 4.3. Pad to pad resistance vs. pad separation for ohmic contacts to n⁺ implanted transmission line.
4.1.3 Ohmic Contact Resistance

The 'y' intercept of the fitted line in figure 4.3 represents the resistance of two ohmic contacts in series. The product of contact resistance and pad width gave a normalized contact resistance of 0.4 ± 0.2 Ωmm. Contact resistances of 0.3 Ωmm have been reported by Murakami and Price [52].

4.1.4 Source Series Resistance

One reason for fabricating MESFETs using the refractory self-aligned gate process was to make the source series resistance small. The source series resistance can be measured by passing forward current through the Schottky gate contact of the MESFET while using the drain contact as a voltage probe [53]. The 'end' resistance of the MESFET is then defined as

$$R_{end} = \frac{dV_{ds}}{dI_g}$$ [4.2]

where $V_{ds}$ is the drain-source voltage that results from current $I_g$ being passed from gate to source. Since the gate current is distributed along the length of the channel (figure 4.4), then the end resistance as defined includes a contribution from the resistance of the conducting channel $R_{ch}$.

$$R_{end} = R_s + \alpha R_{ch}$$ [4.3]

Here $\alpha$ is a constant that is determined by the current
distribution in the channel. The end resistance as measured in this way is then an overestimate of the source series resistance. Several techniques for determining the source series resistance [53-55] require knowledge of the nature of the channel doping profile in order to eliminate the effect of the channel resistance on the measured end resistance. Lee et al. [56] have shown that the contribution of the channel resistance can be determined directly by measuring the differential end resistance for various values of drain current $I_d$ applied.

![Diagram of current distribution for end resistance measurement.](image)

Figure 4.4. Current distribution for end resistance measurement.

The measured drain-source voltage when both gate and drain currents are applied is given by

$$V_{ds} = (I_d+I_g)R_s + I_d R_{ch} + I_g(nkT/qI_d) + R_d I_d \quad [4.4]$$

where $R_s$ and $R_d$ are the source and drain series resistances.
respectively [56]. From equation 4.2 we find

\[ R_{\text{end}} = R_s + (nkT/qI_d) \]  \[ \text{[4.5]} \]

The source series resistance may then be found by fitting a line of slope \( nkT/q \) to a plot of \( R_{\text{end}} \) vs. \( 1/I_d \). End resistance measurements were made at 10 locations on two self-aligned and two selective implant quarter wafers. The value of the source series resistance obtained using this technique was \( R_s = 38 \pm 7 \Omega \) for selective and \( R_s = 5 \pm 1 \Omega \) for self-aligned devices.

![Graph](https://via.placeholder.com/150)

Figure 4.5. \( R_{\text{end}} = \frac{dV_{ds}}{dI_q} \) vs. \( 1/I_d \) for selective implant and self-aligned MESFETs.
4.1.5 Sheet Resistance of TiW Films

The speed of signal propagation on the gate of a MESFET increases as the resistivity of the gate metal is reduced [57-60]. The sheet resistance of the sputtered TiW film was measured using the stepped resistor pattern included on the chip layout. The structure consisted of six contacts, two for applying current to the TiW resistor and four as voltage probes along the length of the resistor. The stepped resistor pattern was also used to measure sheet resistance after the overlayer of Al was evaporated on top of the TiW.

The measured resistance \( R = \frac{V_{\text{measured}}}{I_{\text{applied}}} \) is plotted in figure 4.6 against the number of squares between the voltage probes used. The measured sheet resistivities are applicable at low frequencies. At high frequencies, the effective thickness of the metalizations becomes smaller as a result of the skin effect. The skin depth \( \delta \) of a material with resistivity \( \rho \) and permeability \( \mu \) is given by

\[
\delta = \left( \frac{\rho}{nf\mu} \right)^{1/2}
\]

where \( f \) is the signal frequency [61]. The skin depths of Al and TiW at 40GHz are 4100 Å and 10000 Å respectively. Profilometer scans revealed that the TiW film was 3700 ± 200 Å thick and the Al overlayer was 4000 Å ± 200 Å thick. As a result, the skin effect only becomes important for the metal films at frequencies greater than 40GHz.

The slopes of the lines in figure 4.6 gave sheet resistances of \( R_{sh} = 0.87 \pm 0.06 \ \Omega/\text{square} \) for the TiW.
metalization and $R_{sh} = 0.11 \pm 0.01 \Omega$/square for TiW with the Al overlayer. Sadler [27] reported a sheet resistance of $R = 3.7 \Omega$/square on a 2000Å TiW film. The lower resistivity of the TiW film in this work may be a result of the enhanced tungsten content of the sputter deposited film. The bulk resistivity of Ti is eight times that of W [62].

![Figure 4.6](image)

**Figure 4.6.** Measured resistance of TiW and of TiW with Al overlayer vs. number of squares.

### 4.1.6 Isolation

Transmission line structures 480μm long and separated by 30μm of semi-insulating GaAs were used to measure the isolation provided by the semi-insulating GaAs substrate. A current of
200 ± 50nA was measured when a potential of 10V was applied across the transmission line contacts. This is typical of the isolation achieved in many GaAs fabrication processes [63].

4.1.7 MESFET Characteristic Curves

Drain current characteristics for a typical depletion mode MESFET fabricated by the self-aligned process are shown in figure 4.7.

![I-V characteristic curve for a self-aligned depletion mode MESFET with 0.8µm gate length and 200µm gate width.](image)

Figure 4.7. I-V characteristics for a self-aligned depletion mode MESFET with 0.8µm gate length and 200µm gate width.

The channel implant dose used for depletion mode MESFETs was 3.0x10^{12} cm^{-2}. Enhancement mode MESFETs were fabricated
using a lighter channel implant dose of $2.0 \times 10^{12}$ cm$^{-2}$. Drain current characteristics for such a MESFET are shown in figure 4.8.

![I-V characteristics graph](image)

Figure 4.8. I-V characteristics for a self-aligned enhancement mode MESFET with 0.8\(\mu\)m gate length and 200\(\mu\)m gate width.

4.1.8 Threshold Voltage

Plots of the square root of the drain current $\sqrt{I_d}$ versus the applied gate-source voltage $V_{gs}$ were near linear for $0.5 \text{ mA} < I_d < 5\text{ mA}$. The threshold voltage $V_{th}$ was determined by fitting a line to such plots and extrapolating to $\sqrt{I_d} = 0$. Sample plots are shown in figure 4.9 for enhancement and depletion mode devices. Measurements of 10 MESFETs on 2 quarter wafers gave $V_{th} = -1.7 \pm 0.2\text{V}$ for the depletion mode devices.
Figure 4.9. $\sqrt{I_d}$ vs. $V_{gs}$ for a) a depletion MESFET and b) an enhancement MESFET.
4.1.9 Low Frequency Transconductance

The transconductance of a MESFET, $g_m$, can be related to the channel resistance ($R_{ch}$) and source and drain series resistances ($R_s$ and $R_d$) by

$$ g_m = \frac{dI_d}{dV_{gs}} = \frac{d(1/(R_s+R_d+R_{ch}))}{dV_{gs}}V_{ds} $$

$$ = \frac{V_{ds}}{(R_s+R_d+R_{ch})^2} \left( -\frac{dR_{ch}}{dV_{gs}} \right) \quad [4.7] $$

The small source and drain series resistances associated with self-aligned MESFETs should therefore result in improved device transconductance when compared with selective implant MESFETs. The measured transconductance of 10 MESFETs from two self-aligned and two selective implant quarter wafers gave $g_m = 140 \pm 10$ mS/mm and $g_m = 100 \pm 10$ mS/mm respectively. A sample curve of $g_m$ vs. gate bias for a self-aligned MESFET is given in figure 4.10.
Figure 4.10. Low frequency transconductance \( g_m \) vs. gate bias \( V_{gs} \) for a 100\( \mu \)m wide self-aligned MESFET.
4.2 Microwave Measurements

Microwave measurements were made using an HP 8510 network analyzer and a Cascade Inc. model 54 automated microwave probing apparatus at the Communications Research Centre in Ottawa Ontario. The microwave probes are coplanar waveguides that bring a 50Ω characteristic impedance to the device bonding pads [64]. Because the probes allowed calibration of the measurement system right at the probe tips, it was not necessary to de-embed device measurements from bond wires and fixture effects. The probing arrangement allowed on-wafer measurement of devices and circuits without requiring chips to be diced, mounted, and bonded to microwave jigs. Microwave measurements were made on the self-aligned devices before the Al overlayer was evaporated on the TiW gates.

4.2.1 S-Parameters of MESFETs

The scattering parameters of 80 MESFETs from two quarter wafers fabricated by the self-aligned process and two quarter wafers fabricated by the selective implant process were measured using the Cascade Inc. probing stage. Estimated standard deviations from the mean magnitude and phase of these parameters were computed for both types of devices. Five self-aligned and eight selective implant MESFETs were excluded from the computations due to apparent fabrication failures such as shorted gates. Figure 4.11 shows the mean magnitude of the measured forward transmission coefficient $S_{21}$ with deviation
limits in dB from 2 to 18GHz. The self-aligned devices (solid curves) showed greater gain in the 50Ω system than did the selective implant devices (dashed curves) with \( V_{gs} = 0V \) and \( V_{ds} = 4V \). Smith chart plots of \( S_{11} \) and \( S_{22} \) are shown in figure 4.12 a) and b) respectively. The measured S-parameters for the self-aligned devices were more uniform than those of the selective implant devices. This is likely a result of the sensitivity of the source series resistance to misalignment of the gate for selective implant devices.

Figure 4.11. Mean with standard deviation limits of \(|S_{21}|\) in dB for self-aligned FETs (solid curves) and selective implant FETs (dashed curves).
Figure 4.12. Smith chart plots of mean with standard deviation limits of a) $S_{11}$ and b) $S_{22}$ from 2 to 18GHz for self-aligned FETs (solid curves) and selective implant FETs (dashed curves).
4.2.2 S-Parameters of the Buffer Amplifier Stage

The buffer amplifier was needed in the sample and hold circuit to present a sufficiently high impedance to the hold node to prevent signal droop, and to present the buffered output signal to a 50Ω line. An isolated buffer amplifier implemented with self-aligned FETs was included on the chip layout. The measured S-parameters for five buffer amplifiers were averaged and the results are shown in figures 4.13 and 4.14. Figure 4.13 shows that the amplifier provided gain in a 50Ω system up to 2.6GHz. The input impedance of the amplifier is nearly an open circuit and the output is very closely matched to 50Ω as seen in figure 4.14.

Figure 4.13. $|S_{21}|$ in dB for buffer amplifier circuit implemented with self-aligned FETs.
Figure 4.14. Smith chart plots of a) $S_{11}$ and b) $S_{22}$ from 0.1 to 5GHz for buffer amplifier circuit.
4.3. Testing of the Sample and Hold Circuits

Using three microwave probes, a sinusoidal signal was applied to the RF input of the sample and hold, a pulse train was fed into the sampling gate, and the sampled version of the input signal was observed at the output on a sampling oscilloscope (fig. 4.15).

Figure 4.15. Sample and hold layout and probing configuration used for testing.
Oscilloscope traces of a 10MHz sinusoidal signal applied at the sample and hold input, an 80MHz pulse train fed into the sampling gate, and the sampled output signal are shown in figure 4.16 a). The sample and hold output signal was a sampled representation of the input sinusoid. The droop of the held signal level in the 12ns sampling period was less than 2% of the amplitude of the signal. The feedthrough of the sampling pulse to the sample and hold output was 100mV with a 1V pulse applied to the sampling gate. Figure 4.16b) shows the input and output signals when the input frequency was increased to 36MHz and the sampling rate was increased to 250MHz.

The maximum tested sampling rate was limited by the available pulse generator. The minimum rise and fall time that could be obtained with the Tektronix 115 pulse generator was 0.8ns. As a result, the pulse train became nearly sinusoidal for sampling frequencies greater than 250MHz.

Simulations conducted by Rutherford [16] showed lower feedthrough of the sampling pulse to the output of a sample and hold implemented with a triple gate rather than a single gate sampling MESFET. This effect was not observed when the two types of sample and hold were measured. The guard gates of the sample and hold were not contacted by a microwave probe in the arrangement used to measure the devices. It is suspected that the low frequency 'bias' probe used acted as an RF choke to any momentary current which would otherwise be induced in the guard gate contact. As a result, the effect of the guard gates on the RF output of the sample and hold was suppressed. Because of the probe stage configuration, it was not possible to use a
fourth microwave probe for the guard gate contact while supplying the biases $V_{dd}$ and $V_{ss}$ to the circuit.

Figure 4.16. Oscilloscope traces of input and output signals from a sample and hold. The sample and hold was implemented with self-aligned FETs.
5. ANALYSIS AND MODELING

Modeling of the microwave performance of MESFETs was done using the EEsof Inc. software package, Touchstone. The modeling was primarily intended to determine the effect of the gate resistance on the self-aligned device performance and to estimate the improvement that can be expected for gates given a metal overlayer. The MESFET model used by Touchstone is the same as that shown in figure 1.4. A version of SPICE that included the Sussman Fort GaAs MESFET model [65,66] was used to simulate the sample and hold devices.

5.1. Modeling of MESFETs

The potential along the width of a self-aligned gate is not generally uniform because of the gate's transmission line nature. A lumped element model was used to approximate the effect of a distributed gate resistance and capacitance. The lumped element model (figure 5.1) consisted of eight MESFETs, each having the properties of a 1/8 slice of the self-aligned MESFET.
Figure 5.1. Lumped element model of MESFET.

The transconductance of each of the MESFET elements was set to 1/8 of the low frequency value measured in section 4.1.9. The source and drain series resistances, $R_s$ and $R_d$, were given values eight times greater than the end resistance measured from the devices in section 4.1.4. The value of the gate series resistance $R_g$ for 1/8 of the gate width was determined from the measured sheet resistance of the TiW film (section 4.1.5). The gate-source capacitance $C_{gs}$ was given a value corresponding to the capacitance per unit area that was found from C-V measurements (section 3.2.3) with zero bias applied to the Schottky contact. The other capacitors in the model of the MESFET (namely $C_{dg}$, $C_{dc}$, and $C_{ds}$) were given values 1/10 that of $C_{gs}$. $R_{ds}$ and $R_i$ were chosen to give a good fit of the S-parameters obtained by the model to those that were measured for the self-aligned MESFETs in section 4.2.1. The input listing with the values of the components used in the lumped element model for Touchstone is in appendix B.
5.1.1 Scattering parameters

The lumped element model was used to obtain $S$-parameters for MESFETs with gate series resistance $R_g$ corresponding to TiW gates and for MESFETs with TiW gates with an Al (or Au) overlayer. $S$-parameters obtained from modeling and from measurements of self-aligned MESFETs are shown in figures 5.2 and 5.3. The effect of the gate overlayer is seen primarily in $S_{21}$ and $S_{11}$.

![Graph showing $|S_{21}|$ vs. frequency from model (lines) and measured data (points).]
Figure 5.3. $S_{11}$ and $S_{22}$ from 2 to 18GHz from model (solid lines) and measured data (cross-hatch).

5.1.2 Maximum Gain of MESFETS

The maximum available gain of a two port device is achieved when a simultaneous conjugate match of input and output port impedances is provided. The maximum available gain is not always attainable because the required terminations may cause the device to be unstable. In this case, the input or output loop of the device has an impedance with a negative real part when conjugately matched terminations are provided. The negative resistive impedance yields a source or load reflection coefficient ($\Gamma_c$ or $\Gamma_l$) with magnitude greater than unity.
A brief summary of power gains and their relationship to S-parameters is given in Appendix C. Figure 5.4 shows the maximum available gain of self-aligned devices as determined from measured S-parameters and from the lumped element model. The maximum stable gain is plotted in place of the maximum available gain where $|\Gamma_c| > 1$ or $|\Gamma_L| > 1$. Data from the measured selective implant devices is also included. The model of the self-aligned device with a gate overlayer gave greater high frequency gain than was measured from the selective implant devices.

Figure 5.4. Maximum gain of self-aligned MESFETs from model (lines) and measured data from self-aligned and selective implant devices (points).
By modeling the velocity of carriers through the channel of a GaAs MESFET, Maloney and Frey [67] gave a theoretical relationship between the cutoff frequency and the gate length L. The model gave $f_T = 25\text{GHz}$ for $L = 0.8\,\mu\text{m}$. The parameters used in the Touchstone model of the self-aligned MESFET gave $f_T = \frac{g_m}{2\pi C_{ds}} = 27\text{GHz}$. A cutoff frequency of $f_T = 30\text{GHz}$ was obtained by Chao et al. [68] from a MESFET with $L = 0.3\,\mu\text{m}$.

Morgan and Howes [69] have shown that if the parasitic elements of a MESFET ($R_s$, $R_d$, $R_g$, and $C_{ds}$) are so small that they can be neglected, then the maximum frequency of oscillation $f_{max}$ is given by [69]:

$$f_{max} \text{ (GHz)} = \frac{33}{L \text{ (\mu m)}}$$

From figure 5.4, $f_{max} > 40\text{GHz}$ for the self-aligned MESFET modeled with an Al overlayer on the gate. Since $L \approx 0.8\,\mu\text{m}$, equation 5.1 indicates that the effect of parasitics on the microwave performance of the MESFET is small. North et al. [29] obtained $f_{max} = 20\text{GHz}$ with selective implant MESFETs with $L = 0.5\,\mu\text{m}$.
5.2. Simulation of Sample and Hold Operation

The values for $R_g$, $R_d$, $R_s$, $C_{gs}$, $C_{dg}$, and $C_{ds}$ used for modeling with Touchstone were used in the SPICE simulations of the sample and hold. A lumped element model was also used. Simulation of the sample and hold under the test conditions of section 4.2 gave an output waveform (figure 5.5) similar to that observed in figure 4.16.

![Simulated input and output waveforms](image)

Figure 5.5. Simulated input and output waveforms for a sample and hold under the test conditions of section 4.2.

Simulation at higher sampling frequency (figure 5.6) showed that the acquisition time of the sample and hold could be as small as $\tau = 100\text{ps}$ if a gate overlayer was evaporated on all the MESFETs in the circuit. An acquisition time of
\( \tau = 500 \text{ps} \) was obtained by Wong and Fawcett [12] using a diode bridge scheme. Swierkowski et al. [14] achieved \( \tau = 200 \text{ps} \) using a GaAs MESFET sample and hold.

![Waveform diagram](image)

Figure 5.6. Simulated input and output waveforms for a sample and hold for 2.7GHz sampling of a 360MHz signal.

Complete input listings for the SPICE simulations are included in appendix B.
6. CONCLUSIONS

A gallium arsenide monolithic microwave integrated circuit fabrication process employing MESFETs with self-aligned gates was developed. The self-aligned implant yielded MESFETs with lower source series resistance and larger transconductance than MESFETs fabricated by selective implantation. Also, the fabrication of enhancement mode devices was demonstrated.

Measured microwave scattering parameters of the self-aligned MESFETs were more uniform across the GaAs wafer surface and between wafers than were those measured from selective implant MESFETs. Modeling showed that the maximum available gain of the self-aligned MESFETs would be superior to that of the selective implant MESFETs if the resistance of the gate metalization was reduced. A method of reducing the resistance of the self-aligned gates by evaporating a metal overlayer was demonstrated.

A GaAs sample and hold circuit was fabricated using the self-aligned process. The circuit was tested to a sampling rate of 250MHz. Simulations were used to show that the sample and hold would be capable of state-of-the-art performance if a gate overlayer was evaporated on the MESFETs in the circuit.
REFERENCES


33. R.A. Sadler, Ph.D., ITT GaAs Technology Center, verbal communication.


APPENDIX A - Fabrication Procedure

The details of the developed fabrication process are listed as follows:

1) Scribe 3 inch wafer.
2) Degrease in boiling acetone followed by rinse in boiling methanol and blow dry.
3) GaAs etch in $8:1:1/H_2SO_4:H_2O_2:H_2O$ for 2m45s - removes 3µm of GaAs from wafer surface.
4) Rinse in De-Ionized (D.I.) $H_2O$ cascade for 4min and blow dry.
5) Cleave wafer into quarters.
6) Oxide etch in 10% NH$_4$OH for 15s and blow dry.
7) Plasma deposit silicon nitride.
   i) NH$_3$ plasma preclean. Parameters:
      Gas: NH$_3$         Temp: 300°C
      Pressure: 500mTorr  Power: 100W/500cm$^2$
      NH$_3$ Flow: 42.5sccm/min   Time: 1min
   ii) Silicon nitride deposition. Parameters:
      Gases: He, SiH$_4$, NH$_3$  Temp: 300°C
      Pressure: 1500mTorr  Power: 100W/500cm$^2$
      He Flow: 500sccm/min   Time: 4min
      SiH$_4$ Flow: 540sccm/min
      NH$_3$ Flow: 42.5sccm/min
8) Spin on Shipley 1400-30 photoresist (PR) at 4700rpm for 30s.
9) Soft bake at 95°C for 25min.
10) Expose under registration mask #1 at 25mW/cm² for 45s.
11) Post exposure bake at 95°C for 20min.
12) Develop in MF312 developer for 50s.
13) Rinse in D.I. H₂O cascade for 1min and blow dry.
14) Remove nitride from registration marks in Buffered HF for 30s.
15) Rinse in D.I. H₂O cascade for 10min and blow dry.
16) Etch registration marks in 5:2:240/NH₄OH:H₂O₂:H₂O for 50s.
17) Rinse in D.I. H₂O cascade for 4min and blow dry.
18) Remove PR in boiling acetone followed by boiling methanol and blow dry.
19) ..24) Pattern for implant with n⁻ mask #2 same as steps 8-13.
25) Channel implant
   Parameters: Species: °²Si Dose: 2.0 - 3.0x10¹²
   Energy: 90 - 125 KeV
26) Remove photoresist in 80°C microstrip.
27) Rinse in D.I. H₂O cascade for 4min. and blow dry.
28) Thicken silicon nitride as in 7) (time=2min).
29) Furnace anneal channel implant at 850°C for 25min.
30) Remove silicon nitride.
   i) With Buffered HF for 7min and 10min D.I. cascade rinse.
   ii) CF₄ plasma. Parameters:
       Gas: CF₄ Temp: 100°C
       Pressure: 300mTorr Power: 100W/500cm²
       CF₄ Flow: 140sccm/min Time: 2min
31) Light etch in 1:1:240/NH\textsubscript{4}OH:H\textsubscript{2}O\textsubscript{2}:H\textsubscript{2}O for 3sec.
32) D.I. rinse for 4min in cascade bath.
33) Oxide etch in 10% NH\textsubscript{4}OH for 15s and blow dry.

A 'T' gate structure with suitable undercut for self-aligned ion implantation was obtained using steps 34)–43):

34) Sputter TiW refractory gate metal.
   Parameters: Bias sputter mode
   Gas: Argon  Power: 200W/180cm\textsuperscript{2}
   Pressure: 20mTorr  Time: 20min

Patterning of 1\textmu m lines was achieved using steps 35)–40)

35) Spin on Shipley 1400-30 photoresist at 4700rpm for 35s.
36) Soft bake at 70\textdegree C for 25min and allow to cool.
37) Soak in chlorobenzene for 7min and blow dry.
38) Expose under TiW dummy gate mask #3 at 25mW/cm\textsuperscript{2} for 45s.
39) Develop in MF-312 developer for 60s.
40) Rinse in DI water cascade for 1min. and blow dry.
41) Evaporate 5000\textAA Al.
42) Liftoff metal in boiling acetone followed by boiling methanol rinse and blow dry.
43) Undercut etch in CF\textsubscript{4} plasma.
   Parameters: Gas: CF\textsubscript{4}  Temp: 100\textdegree C
   Pressure: 300mTorr  Power: 100W/500cm\textsuperscript{2}
   CF\textsubscript{4} Flow: 140sccm/min  Time: 15min
44)–49) Pattern for n\textsuperscript{+} implant with mask #4 as steps 8–13.
50) Source/drain implant.

Parameters:  
Species: $^{29}\text{Si}$  
Dose: $1.0 - 2.0 \times 10^{13}$  
Energy: 130 - 150 KeV

51) Remove photoresist in 80°C microstrip.

52) Rinse in D.I. H$_2$O cascade for 4min. and blow dry.

53) Remove Al dummy gates in 50% H$_3$PO$_4$ at 55°C for 2min.

54) Rinse in D.I. H$_2$O cascade for 4min. and blow dry.

55) Anneal source/drain in RTA at 950 °C for 5s (capless anneal with GaAs wafer in proximity).

A metal overlayer on the TiW gates was evaporated as described in steps 56) . . . 67). These steps were actually performed after completion of the devices but would be better done at this point in the fabrication. Evaporating Pd/Au would be preferred to Al as was used here.

56) Spin on Shipley 1400-30 photoresist at 4700rpm for 30s.

57) Soft bake at 95°C for 25min.

58) Hardbake  
   i) ramp oven from 140 °C to 150 °C over 20min.
   
   ii) let cool to 120°C over 20min.

59) Planarization etch in O$_2$ plasma.

Parameters:  
Gas: O$_2$  
Temp: 100°C  
Pressure: 300mTorr  
Power: 100W/500cm$^2$

O$_2$ Flow: 200sccm/min  
Time: 60min

60) . . . 65) Pattern second level of resist for liftoff using TiW dummy gate mask #8 as in steps 35-40.

66) Evaporate 5000Å Al.
67) Liftoff metal in boiling acetone followed by boiling methanol rinse and blow dry.
68) Pattern for liftoff with ohmic mask #5 as in steps 35-40.
74) Evaporate 2000Å AuGe then 300Å Ni.
75) Liftoff metal in boiling acetone followed by boiling methanol rinse and blow dry.
76) Alloy ohmic contacts in furnace at $425^\circ C$ for 2min.
77) Test FETs.

Steps 78)..111) were for formation of the silicon nitride dielectric layer and the MIM top plate.

78) Plasma deposit silicon nitride.

Parameters: Gases: He, SiH$_4$, NH$_3$  Temp: 300$^\circ$C
Pressure: 1500mTorr  Power: 100W/500cm$^2$
He Flow: 500sccm/min  Time: 8min
SiH$_4$ Flow: 540sccm/min
NH$_3$ Flow: 42.5sccm/min

79) Spin on Waycoat HRN 200 negative photoresist.
80) Softbake at 60$^\circ$C for 20min.
81) Expose at 25mW/cm$^2$ for 10s.
82) Develop in xylene for 90s.
83) Rinse in isopropyl alcohol and blow dry.
84) Etch nitride in HF to leave islands at MIM sites.
85) Rinse in D.I. water cascade bath for 10min.
86) Remove photoresist in boiling acetone followed by boiling methanol rinse and blow dry.
Steps 87-95 are not required for MIMs but for Schottky diode contacts and selective implant gates.

87) ..92) Pattern for liftoff using Schottky plate #7 as in steps 35-40.

93) Oxide etch in 10% NH₄OH.

94) Evaporate 3000Å of Ti/Pd/Au Schottky metal.

95) Liftoff metal in boiling acetone followed by boiling methanol rinse and blow dry.

Airbridges were fabricated in steps 96) ..111).

96) Spin on Shipley 1400-30 photoresist at 4700rpm for 30s.

97) Soft bake at 95°C for 25min.

98) Expose under Schottky mask #7 at 25mW/cm² for 45s.

99) Develop in MF312 developer for 50s.

100) Rinse in DI water cascade for 1min. and blow dry.

101) Hardbake 
    i) ramp oven from 140°C to 150°C over 20min. 
    ii) let cool to 120°C over 20min.

102) ..107) Pattern second level of resist for liftoff using Au plate mask #8 as in steps 35-40.

108) Evaporate Au airbridges.

109) Liftoff metal in boiling acetone followed by boiling methanol rinse and blow dry.

110) Remove lower level resist in hot microstrip.

111) Rinse in D.I. water cascade for 4 min. and blow dry.

112) Test sample and hold amplifiers.
APPENDIX B - Input Listings for Modeling

B.1 Touchstone Input

! Lumped element model of self-aligned MESFET

DIM

FREQ GHZ
RES OH
IND NH
CAP PF
LNG MIL
TIME PS
COND /OH
ANG DEG

VAR

G = 0.0025  (g_m A/V)
T = 6  (τ ps)
C1 = 0.035  (C_{gs} pF)
G1 = 1E-8  (g_g A/V)
R1 = 20  (R_i Ohms)
C2 = 0.004  (C_{ds} pF)
C3 = 0.004  (C_{dc} pF)
C4 = 0.004  (C_{ds} pF)
R4 = 4000  (R_{ds} Ohms)
RS = 24  (R_s Ohms)
RG = 5  (or RG = 0.63 for gate with Al or Au overlayer)
RD = 24 (Ohms)
L=0 (nH)

CKT
SRL 4 2 R^RD L=0
SRL 3 1 R^RG L=0
FET2 3 4 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 6 2 R^RD L=0
SRL 5 3 R^RG L=0
FET2 5 6 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 8 2 R^RD L=0
SRL 7 5 R^RG L=0
FET2 7 8 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 10 2 R^RD L=0
SRL 9 7 R^RG L=0
FET2 9 10 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 12 2 R^RD L=0
SRL 11 9 R^RG L=0
FET2 11 12 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 14 2 R^RD L=0
SRL 13 11 R^RG L=0
FET2 13 14 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 16 2 R^RD L=0
SRL 15 13 R^RG L=0
FET2 15 16 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
SRL 18 2 R^RD L=0
SRL 17 15 R^RG L=0
FET2 17 18 0 G^G T^T F^F CGS^C1 GGS^G1 RI^R1 CDG^C2 CDC^C3
+ CDS^C4 RDS^R4 RS^RS
DEF2P 1 2 TRA

OUT
    TRA DB[S21] GR1
    TRA DB[S12] GR2
    TRA DB[GMAX] GR3

!    TRA SB1
    TRA S11
    TRA S22

!    TRA SB2

FREQ
    SWEEP 2 40 2

GRID
    RANGE 2 40 2
    GR1 -2 8 1
    GR2 -40 0 4
    GR3 0 20 2
B.2 Spice Input

Sample and hold - test conditions

*Cycle Controls
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE
.WIDTH OUT=80
*

*Active Elements
*

*Sampling Switch
BSWI 10 20 3 RSAG12 60
*

*Fixed Hold Node Capacitance
CHOLD 3 0 13OFF
*

*Amplifier
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
*
*Standard Active Element Models

*model is for 1 um slice of MESFET or DIODE

*.MODEL RSAG12 GASFET(VTO=-1.7, VBI=1.23, RG=1, ALPHA=2.3,
+ BETA=9E-5, LAMBDA=0.055, CGS0=1.0FF, CGD=0.1FF, CDS=0.05FF,
+ IS=2.0E-15, RD=600, RS=600, TAU=3.0PS)
*

*.MODEL TD4 D(IS=1.24E-14, RS=1300, N=1.2, TT=2PS, CJO=8.0E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*

*Independent Sources

VDD 2 0 DC 5.25
VSS 1 0 DC -2.25
VIN 10 0 SIN(-0.65 0.32 36MEGHZ)
VCTRL 20 0 PULSE(-3.0 -1.9 700PS 700PS 700PS 700PS 3700PS)
*

*Transient Analysis Parameters

*.TRAN TSTEP TSTOP <TSTART TMAX UIO>

.TRAN 100PS 50NS
*

*Output Parameters

.PRINT DC V(10) V(3) V(5)

.PRINT TRAN V(10) V(20) V(3) V(5)

.END
Sample and hold - ultimate performance

*Cycle Controls

.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE
.WIDTH OUT=80
*

*Active Elements
*

*Sampling Switch

BSWI 10 20 3 RSAG12 60
*

*Fixed Hold Node Capacitance

CHOLD 3 0 13OFF
*

*Amplifier

BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
*

*Standard Active Element Models

*model is for 1 um slice of MESFET or DIODE
*
.MODEL RSAG12 GASFET(VTO=-1.7, VBI=1.23, RG=0.1, ALPHA=2.3,
+ BETA=9E-5, LAMBDA=0.055, CGS0=1.0FF, CGD=0.1FF, CDS=0.05FF,
+ IS=2.0E-15, RD=600, RS=600, TAU=3.0PS)
*
.MODEL TD4 D(IS=1.24E-14, RS=1300, N=1.2, TT=2PS, CJO=8.0E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 DC 5.25
VSS 1 0 DC -2.25
VIN 10 0 SIN(-0.65 0.32 360MEGHZ)
VCTRL 20 0 PULSE(-3.0 -2.9 70PS 20PS 20PS 20PS 370PS)
*
*Transient Analysis Parameters
.TRAN 10PS 5NS
*
*Output Parameters
.PRINT DC V(10) V(3) V(5)
.PRINT TRAN V(10) V(20) V(3) V(5)
.END
APPENDIX C - Microwave Gain Definitions

Figure C.1. Power gain block diagram.

The gains (or power ratios) are related to the scattering parameters of the MESFET by [70]:

\[
\frac{P_{\text{out}}}{P_{\text{in}}} = \text{Transducer power gain in 50-ohm system} \quad G_T = |S_{21}|^2 \tag{C.1}
\]

\[
\frac{P_L}{P_S} = \text{Transducer power gain for arbitrary } \Gamma_C \text{ and } \Gamma_L \quad G_T = \frac{(1 - |\Gamma_C|^2)|S_{21}|^2 (1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_C)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_C\Gamma_L|^2} \tag{C.2}
\]

\[
\frac{P_L}{P_{\text{in}}} = \text{Power gain with input conjugate matched} \quad G = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L| (1 - |S_{11}|^2)} = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \tag{C.3}
\]

\[
\frac{P_{\text{out}}}{P_S} = \text{Available power gain with output conjugate matched} \quad G_d = \frac{|S_{21}|^2 (1 - |\Gamma_C|^2)}{|1 - S_{11}\Gamma_C|^2 (1 - |S_{22}|^2)} = \frac{|S_{21}|^2}{1 - |S_{22}|^2} \tag{C.4}
\]

(for \( \Gamma_C = 0 \))

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Unilateral transducer power gain
\[ G_{TU} = \frac{|S_{21}|^2 (1 - |\Gamma_C|^2)(1 - |\Gamma_L|^2)}{|1 - S_{11} \Gamma_C|^2 |1 - S_{22} \Gamma_L|^2} \] [C. 5]

Maximum unilateral transducer power gain
\[ G_{TU \text{ max}} = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \] [C. 6]

Maximum available power gain
\[ G_{ma} = \frac{|S_{21}|}{|S_{12}|} (k - \sqrt{k^2 - 1}) \] [C. 7]

Maximum stable power gain
\[ G_{mu} = \frac{|S_{21}|}{|S_{12}|} \] [C. 8]

where \( k \) is the stability factor as given by:
\[ k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 |S_{12} S_{21}|} > 1 \] for stability [C. 9]

here
\[ |\Delta| = |S_{11} S_{22} - S_{12} S_{21}| \] [C. 10]

and \( \Gamma_C \) and \( \Gamma_L \) are the source and load reflection coefficients and can be related to impedances by:
\[ \Gamma_C = \frac{Z_C - Z_o}{Z_C + Z_o} \] [C. 11]

\[ \Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \] [C. 12]