**FET UPCONVERTER DESIGN
USING LOAD DEPENDENT
MIXING TRANSCONDUCTANCE**

by

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ABSTRACT

The conversion gain of GaAs MESFET mixers is known to be dependent on the impedances seen by the applied signals and the resulting mixing products at all ports of the device. For an accurate representation, all these loading conditions should be considered; however, the design of gate and drain networks then becomes rather difficult. As a result, no sufficiently accurate and yet usable design procedures exist for MESFET mixers; instead, a few simple rules involving short- and open-circuit terminations have been given by various authors. Unfortunately, these rules are often inappropriate, particularly in upconverter applications.

In this thesis, the conversion efficiency dependence on the drain loading at the local oscillator frequency has been studied for a gate upconverter; the local oscillator signal is by far the most dominant in terms of its influence on mixer performance. It has been found that the conversion gain can significantly deteriorate for a narrow range of load values. In addition, the local oscillator drain termination resulting in highest gain has been found to be generally different from the short-circuit recommended in the literature.

Based on these findings, a novel FET upconverter design procedure has been developed that incorporates the local oscillator loading phenomenon in the FET equivalent circuit by means of a load dependent mixing transconductance. It allows the optimization of the drain network for an acceptable match at the selected sideband and desired local oscillator rejection while avoiding impedance values in the local oscillator frequency range which would otherwise cause severe degradation in conversion gain.

TABLE OF CONTENTS

	Page
ABSTRACT	ii
TABLE OF CONTENTS	iii
LIST OF SYMBOLS AND ACRONYMS	v
LIST OF TABLES	vi
LIST OF FIGURES	vii
ACKNOWLEDGEMENTS	ix
CHAPTER 1: INTRODUCTION	1
CHAPTER 2: BASIC ASSUMPTIONS AND CONSTRAINTS	5
CHAPTER 3: DESCRIPTION OF THE METHOD	10
3.1 Conversion gain measurements	10
3.1.1 Broadband 50 Ω termination	10
3.1.2 LO reflection	16
3.2 Proposed model	20
3.2.1 Equivalent circuits	20
3.2.2 Nonlinearity expression	23
3.3 Determining the mixing transconductance	28
3.4 Method summary	32
CHAPTER 4: ACCURACY OF THE METHOD AND ITS PHYSICAL FOUNDATION: DISCUSSION	34
4.1 Additional experimental details	34

4.2 Element acquisition and accuracy enhancement	36
4.3 Simulation details and accuracy	43
4.4 Physical link between the LO voltages and conversion efficiency	51
4.4.1 Circuit - voltages relation	52
4.4.2 Transconductance - voltages interaction	53
CHAPTER 5: APPLICATIONS OF THE METHOD	58
5.1 Drain network synthesis	58
5.2 Additional considerations in using the method	62
5.3 Dual-gate FET	64
CHAPTER 6: CONCLUSION	72
REFERENCES	73
APPENDIX A: THE CLASSICAL MIXER THEORY	75
APPENDIX B: HIGH FREQUENCY SIMULATION IMPROVEMENT	81
APPENDIX C: LISTING OF PROGRAM TO CALCULATE THE BEST DATA FIT	84
APPENDIX D: EQUIVALENT CIRCUIT ELEMENT ACQUISITION WITH TOUCHSTONE	87
APPENDIX E: CONVERSION GAIN SIMULATIONS FOR SAMPLE 3	91
APPENDIX F: FREQUENCY RESPONSE OF LO VOLTAGES FOR $\Gamma = 1$	100
APPENDIX G: DERIVATION OF MIXING TRANSCONDUCTANCE EXPRESSION FROM A LINEAR MODEL	107
APPENDIX H: UPCONVERTER SIMULATION WITH TOUCHSTONE	110

LIST OF SYMBOLS AND ACRONYMS

LO	: Local Oscillator
IF	: Intermediate Frequency
RF	: Radio Frequency
USB	: Upper SideBand
LSB	: Lower SideBand
SSB	: Single SideBand
IP3	: Third order output intercept point, dBm
FOM	: Figure Of Merit, dB
CG	: Conversion Gain, dB
CG_{max}	: Conversion gain maximum, dB
CG_{min}	: Conversion gain minimum, dB
ΔCG	: $CG_{max} - CG_{min}$, dB
V_{GG}	: Gate bias, V
V_{GGmax}	: Gate bias yielding maximum conversion gain, V
V_{GGopt}	: Gate bias yielding "optimum" conversion gain, V
V_{DD}	: Drain bias, V
V_p	: Pinch-off voltage, V
V_{Cgs}	: Voltage magnitude across Cgs, V
V_{Rds}	: Voltage magnitude across Rds, V
$\Delta\psi$	: Phase of V_{Cgs} - phase of V_{Rds} , degrees
I_{DS}	: DC drain to source current, A
Γ	: Magnitude of LO drain reflection coefficient
Θ	: Angle of LO drain reflection coefficient, degrees
Θ_{min}	: Angle of reflection coefficient at conversion gain minimum
Θ_{max}	: Angle of reflection coefficient at conversion gain maximum
Φ	: Electrical length of drain transmission line, degrees
R_L	: Load resistance of drain reflection circuit, Ω
gm^{MIX}	: Mixing transconductance, mS
gm	: Linear small-signal transconductance, mS
Cgs	: Gate to source capacitance, pF
Rds	: Drain to source resistance, Ω
Cgd	: Drain to gate capacitance, pF
Rs	: Source resistance, Ω
Ls	: Source inductance, nH
α, η, ρ	: Coefficients of mixing transconductance function
T, E, G	: Exponents of mixing transconductance function
RL	: Return Loss, dB
Q	: Quality factor
F	: Frequency

LIST OF TABLES

TABLE	Page
I : Measured and calculated output/input mapping	38
II : Typical FET equivalent circuit element values	40
III : Upconverter data for several samples for $F_{IF} = 70$ MHz	45

LIST OF FIGURES

FIGURE	Page
1: V_{GG} and circuit performance -vs- LO power at 1.52 GHz	12
2: "Optimum" circuit performance -vs- LO power at 1.52 GHz	14
3: Conversion gain -vs- frequency for "optimum" conditions	16
4: LO reflection measurement setup	17
5: Typical CG -vs- LO reflection coefficient at 1.46 GHz	19
6: Typical large-signal S parameters	21
7: Complete packaged FET equivalent circuit	24
8: LO reflection circuit	25
9: Typical LO voltages at 1.39 GHz for $\Gamma = 0.8$	26
10: RF/IF equivalent circuit	29
11: Typical simulation results at 1.46 GHz for $\Gamma = 0.8$	31
12: ΔCG and FOM -vs- LO power at 1.5 GHz	35
13: Experimental output/input mapping at 2.03 GHz for $\Gamma = 0.8$	38
14: Simplified FET equivalent circuit	40
15: LO voltages for $\Gamma = 1$ at 10 GHz	41
16: Large-signal S parameter measurement diagrams	42
17: CG -vs- LO reflection coefficient for sample 3	47
18: CG -vs- LO reflection coefficient including uncertainty	50
19: Typical DC characteristics of NE70083	54
20: Matching network 1	59

21: CG -vs- frequency with network 1	60
22: Matching network 2	61
23: CG and RL -vs- frequency with network 2	61
24: Dual-gate FET equivalent circuit	66
25: CG -vs- LO reflection coefficient at 1.5 GHz with $\Gamma = .83$	67
26: Dual-gate FET LO reflection circuit	68
27: LO voltages -vs- reflection coefficient at 1.5 GHz with $\Gamma = 1$	69
A.1: Nonlinear FET equivalent circuit	75
A.2: FET equivalent circuit with element harmonics	77
A.3: Conversion equations and diagram	78
A.4: Conversion equations circuit representation	79
A.5: LSB/USB interaction	79
A.6: Second LO harmonic effects	80
A.7: Approximations of this method	80
B.1: Modified RF/IF circuit for arbitrary loadings	83
E: Conversion Gain Simulations for Sample 3	91
F: Frequency Response of LO Voltages for $\Gamma = 1$	100

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CHAPTER 1: INTRODUCTION

The first GaAs MESFET mixer results were reported in 1973 by Sitch & Robson [1]. Since then, a good deal of research has been conducted on their application in various frequency conversion circuits. The understanding of this device has evolved to the point where fairly sophisticated models now yield good prediction accuracy of its nonlinear circuit behavior. Compared to the more popular GaAs Schottky-barrier diode, FETs offer conversion gain and better saturation characteristics, both of which are obtained with much simpler circuit configurations and lower LO drive. Their principal disadvantage is the relatively poor noise figures that they show under large-signal operation. However, since our interest is to study MESFETs as upconverters, the noise figure is not of particular importance. To quote state-of-the-art performance of both devices, Maas [2] has obtained, for an X band mixer with low IF (30 MHz range), single sideband noise figures of 4 to 5 dB, conversion gains of 6 to 10 dB, and third-order output intercept point of 20 dBm, for 6 to 10 dBm of LO power. A good GaAs Schottky-barrier diode balanced mixer typically has 5 to 9 dB of conversion loss, LO power requirements of 8 to 18 dBm, and third-order output intercept point of 0 to 13 dBm, with a lower bound for the noise figure of about 3.5 dB.

The drive behind this work originates from FET mixer experiments conducted at MPR. The conversion gain and the input/output impedances of gate upconverters were measured in a 50 Ω system at C band. Small-signal techniques were used to conjugate-match the gate at IF and the drain at RF. Normally, this would then yield a predictable value of conversion gain based on the original measurements. However, when

prototypes were built and tested, they had much lower conversion gain than expected. By means of these results and various publications on this topic, it was concluded that the impedance seen by other signals present in the mixer, which had been neglected in the analysis, is also very important in determining conversion efficiency.

So far, much of the research effort on MESFET mixers has concentrated on the conversion efficiency dependence on bias, input LO power, and in some cases, terminating impedances at both ports for the various signal frequencies. Apart from the obvious input and output matching requirements, the general consensus is that only terminations at IF, RF, image (possibly), and LO frequencies need to be considered. For a gate down-converter, the trend is to short-circuit the IF at the gate and the RF and LO at the drain. Yet, given the major influence of the LO, the importance of its drain termination appears to have been somewhat underestimated. Since Harrop & Claasen's work identified the optimal LO impedance to be a short-circuit [3], little detailed supporting evidence for that particular result has been offered. More recently, Maas [2] justified that choice by stating that a "well-behaved" FET transconductance mixer should always operate in the current saturation region with the smallest LO drain voltage variation; Camacho-Peñalosa & Aitchison [4] suggested that the conversion gain eventually drops as a function of LO power when the LO drain termination is not a short-circuit because the FET operates outside of the saturation region.

To design a FET mixer circuit, the frequency response of the embedding networks thus requires careful analysis. At the input, the combining circuit must offer good match and signal isolation. At the output, selected sideband match and LO rejection must be realized. Both circuits must also provide optimum terminations for the other signals. For

downconverters, where the IF and LO are quite far apart, the LO short-circuit at the drain appears to be a satisfactory and easily realizable approximation of optimum LO loading. For upconverters, the usual proximity of the RF and LO frequencies makes a simultaneous realization of the above three requirements difficult, especially over a substantial LO/RF bandwidth. Furthermore, the experience gained with FET upconverter measurements in this study revealed that the optimum LO loading at the drain is dependent on FET parameters and operating frequency and thus not always identical to a short-circuit. In general, the conversion gain was fairly flat and LO-termination insensitive around the optimum impedance while a sharp dip of up to 20 dB occurred over a narrow range of impedance values. Therefore, *avoiding the minimum region* rather than *maximizing gain* should be the goal sought when designing FET mixers.

It is the aim of this work to contribute to more accurate MESFET upconverter design by thoroughly investigating the LO loading phenomenon and integrating the results into a design method. The approach taken relies on a combination of RF measurements and equivalent circuit representations with commercial frequency-domain CAD tools to create a simple but realistic mixer model simulating the LO dynamic loading, thereby allowing interactive circuit analysis and synthesis. Specifically, Touchstone and SPICE will be used as analysis tools in this work.

The thesis is structured as follows: First, Chapter 2 outlines the basic philosophy of the design method, including the assumptions that will be used throughout this work. Then, Chapter 3 describes the development of the method from basic theoretical concepts supported by corresponding experimental evidence and accompanied by actual results in a summary fashion. Chapter 4 provides more experimental, computational, and

simulation details and attempts a thorough investigation of the concepts involved.

Chapter 5 then discusses some applications.

CHAPTER 2: BASIC ASSUMPTIONS AND CONSTRAINTS

In the context of accuracy enhancement due to proper LO loading characterization, the principal thrust of this design method is to simplify data acquisition procedures and modelling steps by using standard microwave measurements and suitable equivalent circuits.

When dealing with nonlinear components, the accuracy and repeatability afforded by a design method are important concerns. Yet, the complexity of many of the available modelling techniques considered accurate enough makes the characterization of a large number of samples, necessary for any scale of production, rather unrealistic. For practical circuit design, the methods introduced by Curtice [5] and a few others [6,7,8] could be considered, but they normally deal with the nonlinearities by means of analytical expressions with their parameters fitted to DC data, the pertinence of which at microwave frequencies is not assured. The time-domain models require iterative techniques for their solution which make them involved computationally. The package of the FET must also be thoroughly characterized, since these methods usually apply best to chip devices.

Given a good qualitative understanding of the device/circuit interaction, it is possible to restrict the FET to its most efficient operational mode. Our efforts are aimed toward realizing a "pure" transconductance mixer, since it usually yields maximum linearity consistent with good conversion efficiency. This choice can result in a simpler, but more restrictive model. In addition, a relaxation of the mixer's sensitivity to the test environment is required. Specifically, the conversion efficiency of a FET gate mixer will normally be

affected by the device/drain circuit interaction not only at the LO frequency (which is the object of this study) but also at the LO harmonics. Separate control of these two effects is almost impossible for realistic microwave measurements. However, if the mixer is made weakly nonlinear by restricting the LO pumping effect and consequently reducing the harmonics level, the problem is considerably simplified. The resulting trade-offs in performance are necessary to achieve the goals of predictability and repeatability.

With this condition enforced, the effect of the second and third LO harmonics (the most influential ones) is neglected experimentally and analytically. Likewise, all the sideband terminations other than the upper sideband, on which we concentrate in this work, are neglected. This is common to most mixer analyses. Hence, only the IF, RF and LO signals concern us here.

Since the other signals present in the mixer are of much lower amplitude than the LO, they can be treated with the standard small-signal techniques. This design method thus reflects the main philosophy of the classical mixer theory where both large-signal and small-signal solutions are featured. At this point, it is worth discussing briefly the parallel between the classical theory and this approach.

The mechanisms of the classical mixer theory and relevant details of its application are described in Appendix A. Maas [2] is a good reference for its adaptation to FET mixers. The classical theory relies on equivalent circuits and splits a mixer problem into large-signal time-domain and small-signal frequency-domain solutions. This formulation is based on the common situation where the LO pumps the device and thus actually sets the operating conditions. All the other signals present are considered as small perturba-

tions superimposed on the LO swing and do not contribute to the pumping. Hence, the application of the theory is limited to cases where all the signals involved have small amplitudes.

First, a nonlinear circuit model of the FET must be devised where each nonlinear element is expressed as a function of selected voltages of the device. The large-signal problem then consists in solving for the controlling voltages, given amplitude and frequency of the source and the FET embedding impedances. Currently, the most popular solution technique is the Harmonic Balance method: it separates the network into linear (frequency-domain) and nonlinear (time-domain) parts and attempts a simultaneous solution of their I/V equations. The voltage waveforms allow the calculation of the nonlinear elements' time dependence; after Fourier analysis, an equivalent circuit is constructed where the harmonics are represented as voltage-controlled current or voltage sources. The resulting *linear* circuit is now processed to calculate the conversion matrix. This matrix can be represented by impedances, in which case its calculation is similar to the common Z parameters but with the difference that several frequencies are involved. In practice, the number of harmonics of the elements' spectra is restricted. Also, as mentioned in Chapter 1, extensive simulations by researchers have allowed further simplifications of the matrix by neglecting sidebands and signals other than the IF, RF and the image.

The matrix is dependent both on the signal frequencies and terminations and on the values of the elements' harmonics, which relate it to the pumping solution. With the latter being a function of the embedding impedances and LO frequency, the matrix must be recalculated every time these are changed. On the other hand, if the pumping solution

is obtained over a bandwidth for a series of different loadings, then the elements' harmonics are characterized within these ranges and the matrix becomes only signal-frequency and -termination dependent: any IF/RF pair can be used as long as the LO variables are kept in the ranges set. The convenience of frequency-domain analysis also allows the derivation of relatively simple analytical conversion gain expressions under certain assumptions [9].

The proposed method uses similar small-signal equivalent circuits to represent the conversion matrix but actually proceeds backwards. Instead of attributing a priori a specific time-domain function to the transconductance and calculating the resulting conversion characteristics, we use measured conversion characteristics to extract the function describing the transconductance factor involved in conversion, but in the frequency domain; the latter is possible due to the fact that we limit the analysis to the LO fundamental.

In essence, the work described here is not so much concerned with different ways of manipulating the conversion matrix but rather with obtaining the matrix elements' dependence on the LO conditions in the circuit. This dependence is obtained from measurements rather than from a predefined mathematical description of the nonlinearities. Otherwise, the same approximations and limitations as in the classical theory prevail. As an additional simplification, the reverse transfers (RF to IF) of the FET mixer are neglected in our model due to the relatively low range of IF and RF frequencies commonly used. As is shown in Figure A.7, this is the equivalent of setting four terms of the conversion matrix equal to zero.

When mixer operation at "higher" RF frequencies is sought ("higher" is actually dependent on the specific transistor chosen), the accuracy of the model can be increased by a slight modification of the corresponding equivalent circuit to account for the degradation of the isolation between the gate and the drain. This improvement is described in Appendix B. In addition, the IF frequency used during a mixer simulation can also be varied and does not need to be fixed to the experimental value. Appendix B also shows how these variations can be easily implemented in the model.

CHAPTER 3: DESCRIPTION OF THE METHOD

3.1 Conversion gain measurements

The characterization is performed on several NEC NE70083 single-gate transistors from two separate batches (#1, #2) at room temperature (25 °C). The device has a 0.5 μm gate length and a typical pinch-off voltage (V_p) of -0.9 V.

The transconductance mixing mode requires that both IF and LO be fed to the gate, with the output (RF) taken at the drain. We are considering an upconverter whose gate is fed from a *broadband* 50 Ω source. To realize the goals stated in Chapter 2, we utilize three degrees of freedom afforded by the FET structure: the bias, the input LO power, and the port terminations. V_p is an additional parameter affecting the achievable conversion efficiency for a given LO level.

Due to test components availability and other practical limitations, the test frequencies and power levels have been chosen as follows:

IF : 70 MHz, -20 dBm

LO : 1.39 - 2.03 GHz, 0 - 6 dBm

RF : 1.46 - 2.1 GHz

3.1.1 Broadband 50 Ω termination

The bias and LO power are the two first parameters to be fixed. A broadband 50 Ω termination is connected at the drain for this purpose. The drain bias is fixed at 3.0 V, the device's standard value for operation in saturation. Optimization of this value never showed significant improvements. In accordance with the preceding discussion, both the

gate bias and the LO power are set to their "optimum" values, meaning values providing the best compromise between conversion gain, third-order output intercept point, figure of merit, and the minimum output level of both the second and third LO harmonics. The harmonics are kept at below -20 dBc; the adjustment of the other parameters is subjective.

The figure of merit (FOM) is a quantity defined especially for this application. It rates the upconverter by the relative amount of RF (P_{RF}) and LO (P_{LO}) power present at its output ($FOM = P_{RF}/P_{LO}$), which directly determines the filtering necessary to achieve a desired LO rejection. The standard two-tone test (same as for the third-order intercept point measurement) is used to determine P_{RF} , the output power of the upconverter for a third-order intermodulation distortion specification of -30 dB. The implications are obvious. For instance, an upconverter generating +10 dBm of RF and 0 dBm of LO requires only 30 dB of filtering to achieve a rejection of 40 dB; with +10 dBm of LO, 40 dB of attenuation is necessary.

0 dBm LO power and a typical gate bias of -0.4 V (compared with -0.6 to -0.7 V for maximum conversion gain) yield the "optimum" performance. Typically, a -2 dB conversion gain, a 6 dBm third-order output intercept point, and a -19 dB figure of merit were measured at 1.52 GHz. The small pinch-off voltage of the NE70083 allows a reasonable conversion gain at this low level, which in turn is attractive for measurement simplicity and subsystems considerations. Fig. 1 depicts some of this data for one sample at 1.52 GHz. The gate bias, conversion gain, third-order output intercept point, and figure of merit are plotted against LO power for both "maximum" and "optimum" conversion gate biases. The gate biases have opposite slopes as the LO power increases:

Figure 1: V_{GG} and circuit performance -vs- LO power at 1.52 GHz

Fig. 1-a: Gate bias -vs- LO power

Fig. 1-b: Broadband 50 Ohm CG -vs- LO power

Fig. 1-c: FOM -vs- LO power

Fig. 1-d: IP3 -vs- LO power

for the "maximum" bias case, it gets closer to pinch-off; for the "optimum" bias case, it tends toward 0 V. As can be seen, the maxima of the three circuit quantities do not necessarily coincide. In particular, for the "maximum" bias case, the figure of merit peaks at a lower LO power than its counterparts, but its slope is much smaller than for the "optimum" bias case; maxima of both conversion gain and third-order output intercept point appear simultaneously. For the "optimum" bias case, the maximum conversion gain occurs around 2-3 dBm, but the third-order output intercept point and figure of merit degrade quickly with LO power increase; however, at 0 dBm, they are only 2 and 5 dB below the "maximum" bias values, respectively, while the corresponding conversion gain is 3 dB worse. Fig. 2 shows the same quantities ("optimum" bias and 0 dBm LO power case) for several samples of batch 2. A good consistency is observed. The

Figure 2: "Optimum" circuit performance -vs- LO power at 1.52 GHz

Fig. 2-a : Broadband 50 Ohm CG -vs- LO power

Fig. 2-b: FOM -vs- LO power

Fig. 2-c: IP3 -vs- LO power

"optimum" LO power choice thus depends on a somewhat subjective compromise between conversion gain and linearity. This does not affect the validity of the method outlined here as long as the harmonics levels are as stated above. Fig. 3 depicts the frequency response of several samples of the same batch for the "optimum" bias and LO power case. As expected, a slight negative slope is present.

3.1.2 LO reflection

The reflection measurements are now performed with the "optimum" gate bias and LO power. The experimental setup is shown in Fig. 4. This is a modified load-pull measurement: the phase of the reflection coefficient is variable at LO frequency while a good return loss is maintained at the selected sideband. The circuit works as follows: the bandpass filter is tuned for good return loss at RF and is narrowband enough to reflect

HP 8350A LO signal generator

MPD 1-3 GHz amplifier

HP 3200B

70 MHz IF source

3 dB att.

NARDA
5072

directional coupler

6 dB att.

HP
11590B

bias T

ANATEK 6020

power supply

HP 428B

dc ammeter

u/A mc70172

circulator

HP
11590B

bias T

sliding
short-circuit

interdigital
bandpass filter

HP 8566B

spectrum analyzer

Figure 4: LO reflection measurement setup

completely the LO which is 70 MHz away. The LO wave then travels to the third port of the circulator whose sliding short-circuit causes an additional delay before reflecting it back to the drain of the FET. The full Smith chart can be spanned by varying the position of the stub. The magnitude of the LO reflection coefficient can be varied by inserting an attenuator between the sliding short and the circulator; its maximum is limited primarily by the circulator losses. Hence both the magnitude and the phase of the LO reflection coefficient can be varied (almost) independently.

An IF short-circuit is added at the drain; its presence eliminates IF impedance variations inherent to the setup, but more importantly, it reduces considerably the direct contribution from the channel conductance. This is desirable to further enhance our "pure" transconductance mixing approximation.

As an intermediate step, the "narrowband" $50\ \Omega$ conversion gain is measured by terminating the third port of the circulator in $50\ \Omega$. In general, it is slightly higher than the values obtained in Section 3.1.1 and shows little frequency dependence.

A plot of the conversion gain as a function of the phase of the LO reflection coefficient with its magnitude as a parameter is shown in Fig. 5 for a typical case. It is similar to the results of Hirota & Ogawa [10]. Note the sharp dip at high magnitudes of the reflection coefficient (up to -8.5 dB) and the reasonably flat maximum (0 dB), somewhat off the short-circuit point. The dip progressively decreases as the magnitude of the reflection coefficient does, and the whole curve eventually converges to the $50\ \Omega$ "narrowband" conversion gain. Clearly, the dip region must be carefully avoided when designing any drain network for this mixer.

Figure 5: Typical CG -vs- LO reflection coefficient at 1.46 GHz

3.2 Proposed model

3.2.1 Equivalent circuits

A FET model suitable for simulating the conversion efficiency dependence on this LO loading is now constructed. The first concerns are the choice of the equivalent circuits and the acquisition of the value of their elements.

An extension of small-signal Scattering parameters measurement, now performed at the "optimum" LO power, enables the characterization of the device. This gives a kind of large-signal S parameters where both the input and output parameters are measured by feeding the respective ports with the same test signal level, as for regular small-signal measurements. The impedances obtained reflect some of the non-linearities of their voltage dependence. Only small bias current variations were observed during the LO reflection experiments ($\approx \pm 7\%$ between maximum and minimum conversion gain, respectively), and for practical purposes, the resulting S parameters are essentially constant, consequently supporting our fixed element values approximation. This technique is rather crude, but the good accuracy we have obtained shows that it is sufficient for our purpose.

One important aspect of microwave transistor measurement is deembedding the microstrip test fixture, whether chips or packaged devices are used. For the best accuracy, a thorough characterization of the fixture is necessary to construct its equivalent circuit. From the embedded S parameters and the fixture's model, the actual S parameters can be extracted. In practice, a good fixture can be considered essentially as a linear phase-shifting element. Given the time delays of the input and output lines which can be

calculated, the S parameters can be deembedded in real-time on the network analyzer. This has proven satisfactory for our purpose. Fig. 6 shows typical "large-signal" S parameters of the NE70083 measured accordingly with an HP8510A network

Figure 6: Typical large-signal S parameters

analyzer. It appears that only $|S_{21}|$ shows compression compared to its small-signal value, depicted simultaneously in Fig. 6-c. Generally, apart from compression, the frequency response of S_{21} has sizeable fluctuations, and it needs to be smoothed out with filtering controls on the network analyzer to allow representation by an equivalent circuit.

With Touchstone and its circuit optimizer, the standard FET small-signal equivalent circuit including package and chip parasitics, shown in Fig. 7, is fitted to the measured S parameters, and the values of its elements extracted. With reference to the classical mixer theory, three separate equivalent circuits (for the LO, IF and RF signals) are constructed using these element values. It appears that using large-signal element values for the IF and RF circuits is more accurate than using the small-signal ones: the low level IF and RF signals essentially see the impedances created by the wide LO swing in an average sense. For example, this approximation is found in [9].

Thus, the LO circuit herein obtained reflects the pumping mechanism, while the combination of the IF and RF circuits allows a representation of the conversion matrix. Indeed, we are actually seeking to model the dependence of the elements of this matrix on the LO pumping.

3.2.2 Nonlinearity expression

Based on the experimental conditions we have enforced, we postulate that only the transconductance is nonlinear, neglecting the reactive pumping as is commonly done elsewhere [5, 9], and we study the loading of the pumped circuit (LO) in the frequency domain with a network as depicted in Fig. 8 (simplified here for clarity). The drive behind this is the intuition that *the observed conversion gain behavior must be the result*

Figure 7: Complete packaged FET equivalent circuit

Figure 8: LO reflection circuit

of voltage patterns across one or more nonlinear elements of the FET directly affecting its conversion mechanism as a function of the drain load.

The experimental load model of Fig. 8 allows the variation of both the magnitude (Γ) and phase (Θ) of the reflection coefficient. The equations relating them to the circuit variables are:

$$\Phi = (180 - \Theta)/2 \quad (1)$$

$$R_L = 50 \frac{(1-\Gamma)}{(1+\Gamma)} \quad (2)$$

where Φ is the electrical length of the lossless transmission line at a given frequency and R_L the value of the load resistance.

In FET quasi-static models, the gate-source capacitance (V_{Cgs}) and drain-source resistance (V_{Rds}) voltages control the nonlinearity of every element so defined. By calculating the voltages on various elements, it is found that the magnitudes of both V_{Cgs} and V_{Rds} indeed show very good correlation with the measured conversion gain patterns. These two quantities and their phase difference were generated with SPICE and are plotted in Fig. 9 for a typical case. The reflection coefficient phase corresponding to the voltages' maxima lines up very closely with the minimum conversion gain locus, and vice versa (Fig. 5). We postulate (for the time being without any "physical" foundation) that these two voltages directly modify the magnitude of the first harmonic of the transconductance spectrum (Chapter 2), the "sideband generator", without significantly altering the average

Figure 9: Typical LO voltages at 1.39 GHz for $\Gamma = 0.8$

Fig. 9-a: Vcgs -vs- LO reflection coefficient angle

Fig. 9-b: V_{rds} -vs- LO reflection coefficient angle

Fig. 9-c: Phase difference -vs- LO reflection coefficient angle

value. This first harmonic is thereafter termed "mixing transconductance" (gm^{MIX}). Hence, we model the upconverter's LO reflection mechanism in the RF circuit via gm^{MIX} which is dependent on voltages obtained at the LO frequency in the pumped circuit and by V_{Cgs} as calculated from the IF circuit. Thus,

$$I(F_{RF}) = gm^{MIX} \left[V_{Cgs}^{LO}, V_{Rds}^{LO} \right] V_{Cgs}(F_{IF}) \quad (3)$$

Fig. 10 depicts the resulting IF/RF circuit combination and Fig. A.7 shows the corresponding IF/RF interconnection and the conversion matrix that it represents. Given the linear relationship between gm^{MIX} and the $|S_{21}|$ (IF to RF transmission coefficient) of this circuit, and the latter's equality, by definition, to conversion gain, the experimental conversion gain data along with the calculated LO voltages are used to extract the above gm^{MIX} function.

This analysis thus naturally couples internal FET parameters and LO voltages to the sideband conversion gain. This formulation is specific to the FET structure and is expected to be more universal than if gm^{MIX} was related directly to the external circuit. Practically, a significant computation economy can also be achieved since the LO voltage variables are implicitly functions of frequency.

3.3 Determining the mixing transconductance

To obtain $gm^{MIX}(V_{Cgs}^{LO}, V_{Rds}^{LO})$, the standard technique of multivariable least-square curve fitting is used to match a polynomial expression in V_{Cgs} and V_{Rds} to the mixing transconductance values obtained from the experimental conversion gain data, independently

Figure 10: RF/IF equivalent circuit

of frequency and of the magnitude and phase of the reflection coefficient. An approximate form for the function has been guessed by studying some of the published transconductance expressions, and by trial and error. The phase difference between V_{Cgs} and V_{Rds} ($\Delta\psi$) is an important variable for the best fit. Its physical meaning is discussed in Section 4.4. The following expression was found to give the best results for each sample studied:

$$gm^{MIX}(V_{Cgs}^{LO}, V_{Rds}^{LO}) = \alpha V_{Cgs}^T + \eta |V_{Rds} \cos(\Delta\psi)|^E + \rho |V_{Rds} \cos(\Delta\psi)|^G \quad (4)$$

with V_{Cgs} and V_{Rds} representing the voltage magnitudes. The optimum fit is then obtained by a grid search seeking to minimize an error function which gives an equal effective weight for each data point. It is expressed as:

$$\epsilon = \frac{1}{(N-m)} \sum_i^N \left[\frac{gm^{MIX}_{CALCi} - gm^{MIX}_{MEASi}}{gm^{MIX}_{MEASi}} \right]^2 \quad (5)$$

where N is the number of data points and m the number of independent variables. It is the equivalent of the usual Standard Error of least-square regressions. The listing of the computer program used to solve that equation is presented in Appendix C.

A typical example of a fit that can be obtained using this function is shown in Fig. 11. The peak error in the predicted values of conversion gain for any phase of the reflection coefficient at 1.46 GHz is about 1 dB. Equation (4) is discussed in more detail in Section 4.3.

Figure 11: Typical simulation results at 1.46 GHz for $\Gamma = 0.8$

3.4 Method summary

In summary, the proposed design method involves the following steps:

- a] With the drain terminated in a broadband $50\ \Omega$ load, find the bias and the input LO power which yield the "optimum" operation of the FET, where all three of conversion gain, third-order output intercept point, and figure of merit are maximized while the output level of the second and third LO harmonics is kept as low as possible.
- b] Use a modified load-pull method to measure the conversion gain over an LO frequency tuning range at least as wide as the intended bandwidth of operation. This renders conversion gain CG as a function of the magnitude (Γ) and phase (Θ) of the reflection coefficient, and the LO frequency F_{LO} :

$$CG = CG(\Gamma, \Theta, F_{LO}) \quad (6)$$

- c] Construct three equivalent circuits representing the FET at IF, RF and LO; extract their element values from S parameters measured at the LO level and bias obtained in a].
- d] Assume the transconductance is the sole nonlinear element of the FET. In the RF equivalent circuit, define a conversion current source, to be controlled by the IF gate voltage, with an associated mixing transconductance gm^{MIX} . The latter must obviously be a function of Γ , Θ and F_{LO} :

$$gm^{MIX} = gm^{MIX}(\Gamma, \Theta, F_{LO}) \quad (7)$$

- e] Use the IF and RF equivalent circuits to determine the theoretical $|S_{21}|$ from IF to RF. First, in the loaded IF circuit, the voltage on the gate-source capacitance ($V_{C_{gs}}$) is calculated over the desired bandwidth; next, via the conversion source, the theoretical $|S_{21}|$ is determined as a function of gm^{MIX} and sideband frequency F_{RF} . By definition, $|S_{21}|$ must be equal to the measured conversion gain CG:

$$|S_{21}|(gm^{MIX}, F_{RF}) = CG(\Gamma, \Theta, F_{LO}) \quad (8)$$

with F_{RF} and F_{LO} related by F_{IF} . The solution of this equation for gm^{MIX} allows the extraction of (7).

- f] Study the voltage patterns in the LO circuit with a model of the experimental load of b]. This yields functions of the type:

$$V_i^{LO} = V_i^{LO}(\Gamma, \Theta, F_{LO}) \quad (9)$$

where V_i^{LO} represent the voltage on the elements of the equivalent circuit. Correlating (6) and (9), the gate-source capacitance C_{gs} and drain-source resistance R_{ds} are selected as the key elements.

- g] Assume that the conversion gain variations are caused by a mechanism linking gm^{MIX} to $V_{C_{gs}}$ and $V_{R_{ds}}$ at LO. Then, gm^{MIX} can be written as:

$$gm^{MIX} = gm^{MIX}(V_{C_{gs}}^{LO}, V_{R_{ds}}^{LO}) \quad (10)$$

Using least-square curve fitting, solve (10) by combining (7) and (9).

- h] Upconverter performance optimization can now be performed as the effect of a particular drain network on the two selected LO voltages can be evaluated, and in turn the conversion gain predicted.

CHAPTER 4: ACCURACY OF THE METHOD AND ITS PHYSICAL FOUNDATION: DISCUSSION

4.1 Additional experimental details

During the course of these experiments, it became clear that the choice of the gate bias has an impact on the depth of the conversion gain dip. This was investigated for the case of the "maximum" bias (near pinch-off). Fig. 12 depicts ΔCG ($\equiv$ conversion gain maximum - conversion gain minimum) and FOM (figure of merit) as a function of LO power for the cases of "maximum" and "optimum" bias at $F_{RF} = 1.50$ GHz. Two samples of batch 1 were used for these measurements; this batch shows a much higher sensitivity to the LO loading than batch 2. ΔCG is indeed smaller when the device is biased near pinch-off: the neighborhood of 0 - 2 dBm yields simultaneously the best FOM and the smallest ΔCG . ΔCG is about 4 dB there. For the "optimum" bias case, the results of Section 3.1.1 are reproduced at 0 dBm (best FOM); ΔCG is also the smallest there, but it now goes as high as 18 dB (for sample 9). This shows how sensitive certain devices can be to the drain loading (compare with a typical ΔCG of 9 dB for batch 2). Batch 2, at the "maximum" bias, showed a typical ΔCG of 3.5 dB at 2.1 GHz and 0 dBm LO power. It is clear that the choice of operating conditions influences the magnitude of ΔCG .

However, for the "maximum" bias case, the drain-source DC current variation between the maximum and minimum conversion gain for a large value of the magnitude of the LO reflection coefficient is now close to 50% of its 50 Ω value, compared with only 14% for the "optimum" bias. Hence, the S parameters are likely to vary substantially. Furthermore, the reflection coefficient phase angle corresponding to

Figure 12: Δ CG and FOM -vs- LO power at 1.5 GHz

Fig. 12-a: CG range -vs- LO power

Fig. 12-b: FOM -vs- LO power

the minimum conversion gain is not the same as for the "optimum" bias. This is also verified by monitoring the LO power at the drain of the FET (simply by inserting a directional coupler after the bias T in Fig. 4) as a function of the load: the phase angle at the maximum power no longer corresponds to the minimum conversion gain's phase angle, although no precise deviation can be quoted. Nevertheless, even the relatively small conversion gain difference obtained for the "maximum" bias can be significant when a combination of input LO power, temperature, bias variation, frequency, and device non-linearity variations are involved. The design method reported here would not be applicable for this case.

An apparent experimental discrepancy was revealed in Section 3.1.2 which occurs for the conversion gain measurement between the broadband and the narrowband 50 Ω loads. The latter causes a conversion gain increase of more than 1 dB over the former. This could be due to the LO harmonics, still influential, or to feedback effects at IF. Calculations using the IF equivalent circuit show that the voltage across the drain-source resistance is decreasing significantly between these two loads and suggest that there is a channel conductance contribution which interferes destructively with the transconductance when the drain is terminated in 50 Ω at IF.

4.2 Element acquisition and accuracy enhancement

The LO controlling voltages (V_{Cgs} and V_{Rds}) are quite sensitive to the value of some elements of the equivalent circuit. It is therefore important to extract these with the best accuracy possible. Two sources of uncertainties are involved: first, the ability of the equivalent circuit to represent closely a real FET; second, the accuracy of the S parame-

ters themselves. Unfortunately, there is a trade-off between the certainty in the value of an element and the variable-element count of an equivalent circuit [11]. Wide bandwidth (to 18 GHz) S parameters and direct measurement of a number of elements are the only ways to increase certainty and keep the correct internal physical representation of the FET. Even extensive wideband (12 GHz) S parameters fitting performed during this work still yielded wide ranges for the sensitive elements.

Using packaged FETs creates an even more complex situation. It is our experience that with only S parameter and manufacturer (such as package and chip parasitics) data available, simple parasitic elements whose values are variable together with a narrower optimization bandwidth are preferable to ensure a closer fit, within measurement uncertainties. These simplifications require meeting additional constraints to fix internal circuit relationships. For that purpose, FET output/input mappings at selected frequencies and values of the reflection coefficient magnitude can be enforced simultaneously with the S parameters during the element acquisition procedure. A direct byproduct of our analysis, these mapping relations can be easily verified experimentally, and provide further support for our constant element assumption. Fig. 13 depicts such a mapping obtained experimentally for a full 360 degrees span at the drain. The magnitude of the drain reflection coefficient is ≈ 0.83 , the LO power is 0 dBm, and the frequency is 2.03 GHz. The same setup as in Fig. 4 is used but with the HP8510A directly connected to the gate of the FET. The plot shows that the FET has a negative input resistance over a region of the Smith chart which does not appear to have direct relations with the conversion gain patterns.

Figure 13: Experimental output/input mapping at 2.03 GHz for $\Gamma = 0.83$

Table I presents a comparison of the measured and calculated (with Touchstone and the large-signal S parameters) input reflection coefficients for two samples. These values agree quite well.

Table I: Measured and calculated output/input mapping at 2.03 GHz

Sample #	Γ, Θ (mag,ang)	Input reflection coefficient (mag,ang)	
	Measured	Measured	Calculated
2	.822/45.5	1.000/-53.7	.999/-53.5
	.833/64.8	1.042/-49.1	1.035/-49.5
	.854/111.6	1.000/-43.7	1.000/-44.5
4	.823/44.9	1.000/-53.9	1.001/-53.3
	.839/71.3	1.043/-47.5	1.038/-47.9
	.829/105.2	1.000/-43.5	1.006/-44.5

All the simulations reported here were obtained with that approach. The simplified equivalent circuit is shown in Fig. 14, and a set of typical element values is presented in Table II. A 2 GHz bandwidth of S parameters was used together with the output/input mapping of the drain load (calculated from the measured S parameters) at 1.39 and 2.03 GHz for two values of the LO reflection coefficient magnitude. The loci of maximum and unity magnitude of the resulting input reflection coefficient were chosen for convenience. This adds 12 extra optimization goals to the basic S parameters fit. A sample Touchstone file used to extract the elements of the circuit is shown in Appendix D.

Of course, the elements of this simplified circuit are more distant from their "correct" physical values, but by nature, equivalent circuits are limited in scope. Nevertheless, as long as the circuit models correctly the external characteristics of the upconverter, this "black box" representation is the most attractive in terms of accuracy, measurement efforts, and modelling complexity.

Straight wideband S parameter fitting is still valuable. It enables a quick qualitative assessment of the upconverter's frequency response based on the frequency response of the LO voltages. For example, Fig. 15 depicts calculated gate-source capacitance and drain-source resistance voltage patterns at 10 GHz. It is clearly shown that in this case, by analogy with the correlation previously demonstrated between voltages and conversion gain, the occurrence of a drain-source voltage peak and a gate-source voltage dip around the short-circuit angle, the usual approximation to optimum LO loading, would seriously degrade the mixer performance of the transistor studied here.

Figure 14: Simplified FET equivalent circuit

Table II: Typical element values

Element	Value	units
R_g	7.8637	Ω
R_d	0.29302	
R_s	7.08732	
L_g	0.04031	nH
L_d	0.2069	
L_s	0.1228	
C_{in}	0.31203	pF
C_{out}	0.31017	
C_{gs}	0.391	
C_{gd}	0.01948	
C_{ds}	0.09327	
R_i	17.92754	Ω
R_{ds}	138.5854	
gm	0.06317	S
τ	0	ps

Figure 15: LO voltages for $\Gamma = 1$ at 10 GHz

Fig. 15-a: V_{cgs} -vs- LO reflection coefficient angle

Fig. 15-b: V_{rds} -vs- LO reflection coefficient angle

An improvement to our method could be achieved by a more realistic measurement of the large-signal S parameters. Our technique indiscriminately characterizes both FET ports with the same power level. More rigorous large-signal characterization methods can be found in the literature; yet, an attractive and practical alternative is to increase the test power level used to measure S_{22} and S_{12} , both particularly important for the design of output networks. As we proceeded, the S_{11} and S_{21} measurements gave realistic results in a $50\ \Omega$ system. However, the device gain considerably increases the RF power present at the output and a 0 dBm testing somewhat underestimates the proper large-signal dependence of S_{22} and S_{12} . For example, reciprocity could be applied to find the most realistic test power level. Referring to Fig. 16-a, P_1 represents the LO power measured on a $50\ \Omega$ termination during the experiment of Section 3.1.1. Fig. 16-b depicts an impedance measurement where the power of the source is adjusted while measuring S_{22} and calculating P_2 until $P_2 = P_1$. Then both S_{12} and S_{22} can be measured at that level. This method will not give the rigorous situation where all the harmonics are correctly reproduced in the drain circuit but will yield much closer results for the LO fundamental.

Figure 16: Large-signal S parameter measurement diagrams

4.3 Simulation details and accuracy

Our results suggest that the range of validity of Equation (4) is limited only by the experimental conversion gain data available. The S parameters are easily measured on an automated system, but the conversion gain experiments are limited in the possible range of reflection coefficient magnitude (Γ) and LO frequency range by the insertion loss and the frequency response of the components available. The conversion gain measurements are performed manually and can be laborious, especially at high frequencies. To reduce the experimental burden, a minimum amount of data points should allow the widest conversion gain simulation range in the reflection coefficient and frequency space. As is realized from Fig. 11, the dip region, with its steep slope, is much more prone to simulation errors. The small value of the mixing transconductance (gm^{MIX}) at the minimum makes Equation (4) extremely sensitive to the drain-source resistance voltage which can become very large for a FET subjected to a load with a high Γ . It is therefore important to have data of conversion gain extremes for the largest value of Γ possible. If the losses of the test components hinder the measurement of high Γ conversion gain extremes, then their values must be estimated to fix the combination of the drain-source resistance and gate-source capacitance voltages at $\Gamma = 1$ in the regression. Otherwise, the simulations are essentially limited (in the upper range) to the maximum measured Γ for accurate results.

The frequency limitation in the accuracy of Equation (4) depends on the correlation between the frequency response of the LO voltages and the actual conversion gain extremes. Our data does not indicate a significant frequency dependence of the conversion gain extremes over that bandwidth while the LO voltages do vary slightly.

Consequently, the LO voltages combination for the highest reflection coefficient available must be enforced over a frequency range to obtain the best overall fit.

Based on these considerations, a very acceptable fit is obtained by actually using a relatively small amount of data. The conversion gain dependence on the phase of the reflection coefficient for three values of the coefficient's magnitude at a frequency where the error in predicting the angle corresponding to the conversion gain minimum (for the maximum reflection coefficient) is small (2 - 3 degrees) plus the extreme points (minimum and maximum conversion gain) at selected inband frequencies yield a good overall match of the reflection coefficient dependence for each test frequency. The economy of data required (about 35 points here) is an attractive feature.

Table III presents a set of data pertaining to six different samples of the NE70083 and one sample of the NE71084. Predicted and measured values of the reflection coefficient angle corresponding to the conversion gain extremes (also listed) are compared; the values of the "optimum" bias and of the parameters of Equation (4) yielding the best fit are also shown for each case. Consistency is observed among all these samples. The reflection coefficient phase angles for the minimum conversion gain are in fact very close to the conjugate of the measured S_{22} angles and are predicted with a worse case inaccuracy of 8 degrees; for the maximum conversion gain, the angles deviate more but can tolerate larger error because of the flatness of the curve in that region. The minimum conversion gain decreases with RF frequency increase but as mentioned above, it may be caused more by inherent reflection coefficient magnitude variations at this point (also listed) than by true frequency response. The exponents of Equation (4) differ slightly, but

SAMPLE #	FREQUENCY (GHz)											
	1.46						1.52					
	measured (dB)		$\Theta_{\min} (^{\circ})^3$		$\Theta_{\max} (^{\circ})^4$		measured (dB)		$\Theta_{\min} (^{\circ})^5$		$\Theta_{\max} (^{\circ})^6$	
	$CG_{\min}$	$CG_{\max}$	meas	calc	meas	calc	$CG_{\min}$	$CG_{\max}$	meas	calc	meas	calc
1	-8.6	-0.3	22.7	21.9	-166.4	-172.4	-9.7	-0.2	29.9	23.0	-159.8	-171.9
2	-8.5	0.8	20.9	23.4	-157	-171.7	-10.1	0.9	27.0	24.4	-163.8	-170.8
3	-8.5	0.1	24.8	23.3	-155.3	-171.9	-10.0	0.0	24.9	24.3	-172.4	-171.4
4	-8.1	0.5	21.5	21.4	-156.2	-170	-9.3	1.0	25.7	22.4	-164.0	-169.5
5	-8.5	0.5	23.4	N/A	-155.1	N/A	-9.3	0.9	27.6	N/A	-162.9	N/A
7 ¹	-8.5	0.6	19.6	N/A	-155.5	N/A	-9.4	0.5	24.4	N/A	-167.6	N/A
16 ²	-12.9	0.7	21.6	N/A	-153.6	N/A	-16.9	-0.4	26.7	N/A	178.3	N/A

SAMPLE #	FREQUENCY (GHz)												V_{GGopt} (V)
	1.59						2.1						
	measured (dB)		$\Theta_{min} (^{\circ})^7$		$\Theta_{max} (^{\circ})^8$		measured (dB)		$\Theta_{min} (^{\circ})^9$		$\Theta_{max} (^{\circ})^{10}$		
	CG_{min}	CG_{max}	meas	calc	meas	calc	CG_{min}	CG_{max}	meas	calc	meas	calc	
1	-10.8	-0.4	31.7	24	-160.4	-171.6	-11.8	-0.5	35.7	31.5	-154.1	-168.6	-0.64
2	-12	0.8	28.7	25.5	-164.9	-170.8	-14.3	0.6	37.3	33.3	-160.4	-171.7	-0.36
3	-11.4	0.0	27.9	25.4	-169.1	-171	-12.1	-0.6	35.3	33.1	-155.9	-167.9	-0.61
4	-11.6	0.6	29.6	23.5	-172.5	-168.9	-12.2	0.6	36.4	30.8	-155.8	-165.5	-0.4
5	-11.6	0.5	28.2	N/A	-169.2	N/A	-12.9	0.0	35.9	N/A	-163.1	N/A	-0.34
7 ¹	N/A	N/A	N/A	N/A	N/A	N/A	-15.3	-0.2	35.3	N/A	-170.5	N/A	-0.29
16 ²	-20.7	-0.3	28.3	N/A	-170.1	N/A	-25.3	-2.1	35.5	N/A	-156	N/A	-0.34

1: NE71084 2: NE70083, batch 1 3: $\Gamma = .757$ 4: $\Gamma = .825$ 5: $\Gamma = .782$ 6: $\Gamma = .817$ 7: $\Gamma = .803$ 8: $\Gamma = .792$ 9: $\Gamma = .814$ 10: $\Gamma = .825$

SAMPLE #	EQUATION PARAMETERS					
	T	E	G	$\alpha (*10^{-2})$	$\eta (*10^{-2})$	$\rho (*10^{-4})$
1	0.6	0.2	2.5	3.59	-1.24	-1.46
2	1.2	0.3	2.4	3.09	-0.55	-1.6
3	0.7	0.2	2.9	3.03	-1.01	-0.61
4	0.7	0.2	2.7	2.44	-0.69	-0.7

Table III: Upconverter data for several samples for $F_{IF} = 70$ MHz

are within an acceptable range given device variations (e.g. "optimum" bias). For the coefficients, patterns are observed for α and η . Coefficient α is reasonably constant for all the samples and η is similar for each pair of sample with similar "optimum" bias. Coefficient ρ does not follow any particular pattern. A simplified version of Equation (4) (without the last term) was the next best approximation to Equation (7). It could be used advantageously for small bandwidth simulations.

More calculated and measured curves of the conversion gain as a function of the LO reflection coefficient are presented in Fig. 17 for sample 3; Appendix E shows the simulation results over the full bandwidth. The maximum magnitude of the reflection coefficient is ≈ 0.8 at each frequency across the band. The measured and calculated conversion gain curves agree quite closely in shape but there can be a considerable error for points within the dip, reaching almost 3 dB for the largest reflection coefficient. However, given the very steep slope of this notch and the inevitable measurement and simulation errors, these deviations are still relatively small. In fact, the error in predicting the phase angle of the conversion gain minimum at a particular frequency directly influences the magnitude of these deviations, which increase as the Q of the load does. Better match can be obtained despite these phase angles inaccuracies if the regression is performed over smaller bandwidths and/or more data points used.

In order to show the potential accuracy of the simulation part of the method, a worst case uncertainty of 5 degrees is assigned to all the measured reflection coefficient phase angles (precision of manual measurement technique and measurement uncertainty with an HP8510A, calculated from the equations presented in [12]) at several

Figure 17: CG -vs- LO reflection coefficient for sample 3

Fig. 17-a: mag = 0.6, F = 1.46 GHz

Fig. 17-b: mag = 0.4, F = 1.46

Fig. 17-c: mag = 0.8, F = 2.1 GHz

frequencies. The measured curve is then shifted by 5 degrees to the left. Using the same equation parameters as for Fig. 17, the conversion gain is resimulated. The new results are shown on Fig. 18 at 1.59 and 2.1 GHz for a reflection coefficient magnitude of ≈ 0.8 . The peak error in the dip is now about 1 dB. Of course, this is an arbitrary comparison. The curve could also be shifted 5 degrees to the right, in which case the fit would be even worse. But it shows the potential accuracy that can be expected *without recalculating the regression*.

In addition, the uncertainty on each measured S parameter will influence the accuracy of the phase angle prediction of the conversion gain minimum. A rigorous assessment of these uncertainties is not straightforward. Given the limitations of Touchstone for that purpose and the impracticality of the task, a simple procedure was devised which gives a feel for the sensitivity of the LO voltages on specific elements of the equivalent circuit when the S parameter uncertainties are considered. The measured S parameters and their uncertainties are entered as ranges in the OPT block of Touchstone for a single frequency. Each element of the best set (as obtained in Chapter 3) is perturbed in turn while keeping the others constant to find the particular range over which the error function calculated by Touchstone is below an arbitrary small value. The calculations must be performed at each desired frequency. The resulting variations in the locus and value of the LO voltages extremes can be determined for each element also with Touchstone. Typically, each S parameter angle has a 4 degrees uncertainty and the magnitudes of S_{11} , S_{21} , S_{12} and S_{22} have uncertainties of 0.06, 0.16, 0.007 and .04, respectively.

Figure 18: CG -vs- LO reflection coefficient including uncertainty

Fig. 18-a: mag = 0.8, F = 1.59 GHz

Fig. 18-b: mag = 0.8, F = 2.1 GHz

For the minimum conversion gain phase angle, the gate-drain, drain-source, and output capacitances give the largest variation, reaching 7 degrees for the drain-source resistance voltage and 6 degrees for the gate-source capacitance voltage, and its sign changes over the bandwidth; for the maximum conversion gain phase angle, the drain inductance could shift both LO voltages by up to 20 degrees. Such shifts will indeed make a significant difference in the accuracy of the simulations. Likewise, the drain-source resistance voltage could be changed by up to 1 V by varying the drain-source resistance and the transconductance. This method is not absolutely rigorous since only one element is allowed to vary at any time but nevertheless it provides some insight into the uncertainties associated with the element values. The sensitivity shown to elements such as the gate-drain and drain-source capacitances supports the need to increase the measurement accuracy of S_{12} and S_{22} as mentioned in Section 4.2.

4.4 Physical link between the LO voltages and conversion efficiency

A scrutiny of the coefficients in Equation (4) (Table III) reveals that gm^{MIX} is dependent directly on a power of the gate-source capacitance voltage (V_{Cgs}) and is corrected by two *negative* factors dependent on the drain-source resistance voltage (V_{Rds}). Intuitively, this corresponds well to the normal situation where V_{Cgs} predominantly controls the action of the transconductance but the presence of these corrective factors which "perturb" the gate action cannot be the result of pure mathematical artifice: they should bear some relation to the physics of MESFETs. This section attempts to shed some light on the mechanisms involved and suggest a possible explanation.

4.4.1 Circuit - voltages relation

Referring back to Fig. 9, the minimum and maximum of V_{Rds} simply correspond to series and parallel resonance at the drain of the FET, while the minimum and maximum of V_{Cgs} are caused by extremes of negative and positive feedback. Over the bandwidth studied, this feedback appears to act as a self-regulator of the drain-resonance destructive interference by simultaneously creating a V_{Cgs} maximum. Consider the frequency response of the extremes of V_{Rds} , V_{Cgs} , and conversion gain (the LO voltages are depicted in Appendix F over a 1 to 12 GHz bandwidth). V_{Rds} has negative slopes for both. Based on Equation (4), this implies positive slopes for both the minimum and maximum conversion gain. However, V_{Cgs} 's slopes are also negative and contribute to counteract V_{Rds} 's; as apparent from Appendix F, a positive to negative feedback reversal even occurs around 5 GHz. Thus, a physically sound situation evolves from the combination of the frequency response of the two voltages, but it remains to be seen how much weight V_{Cgs} has at higher frequencies since the actual frequency response of the conversion gain extremes is not clear from our data.

In this context, our results reinforce the findings of Hirota & Ogawa [10] and Rauscher [13] in showing that feedback and resonances at the LO frequency, caused by the transistor's internal elements and package parasitics, directly influence the conversion gain behavior, but with the difference that a nonlinear circuit/device interaction is clearly present.

Further study of the parasitics and feedback elements influence on V_{Cgs} and V_{Rds} based on the results of Section 4.3 reveals that V_{Cgs} is quite sensitive to the value of the gate-

drain capacitance (C_{gd}), the source resistance (R_s), and the source inductance (L_s). R_s causes its extremes to occur simultaneously with V_{Rds} 's while L_s , but mainly C_{gd} , can shift them apart appreciably; the latter also provides an increased gradient of the frequency response of the magnitude and phase angle locus of the maximum V_{Rds} and eventually causes the positive to negative feedback reversal for V_{Cgs} . Therefore, it appears that the behavior of the internal voltages is directly dependent on the proper balance between these elements. A rigorous parameter acquisition technique with accurate test fixture deembedding, accurate package model, wideband (18 GHz) S parameter - equivalent circuit match, and several independent measurements would be necessary to unambiguously fix the value of each internal element with good certainty, but the efforts required are beyond practicality.

4.4.2 Transconductance - voltages interaction

The nonlinear circuit/device interaction mentioned above could be explained by the drain-voltage induced pinch-off voltage shift, a short-channel MESFET DC phenomenon reported by many researchers [5, 14, 15] and judged important for best modelling accuracy. Typical plots of the DC drain-source current as a function of the gate and drain voltages are shown in Fig. 19-a and -b for the FET studied. In 19-b, the gate nonlinear region is located at pinch-off, whose shift as a function of the drain voltage is obvious. At large values of the drain voltage, the curve becomes almost completely linear. As a dynamic process, this shift would modify the second-order characteristic of the transfer function. When the corresponding transconductance is plotted, as in Fig. 19-c, its modulation by the drain voltage is serious. Now both the pinch-off and near 0 V regions are

being modified.

Figure 19: Typical DC characteristics of NE70083

Fig. 19-a: I_{DS} -vs- V_{DD} , $V_{GG} = -1.0 - 0.25$

Fig. 19-b: I_{DS} -vs- V_{GG} , $V_{DD} = 0.5 - 6.0$

Fig. 19-c: gm -vs- V_{GG} , $V_{DD} = 0.5 - 6.0$

It is not clear to what extent this effect is modified by relaxation phenomena at microwave frequencies. However, the following observations appear to be more than purely coincidental. The study of these DC curves and of their possible relation to the equivalent circuit suggests that drain parallel resonance, where the drain-source resistance voltage (V_{Rds}) is maximum and where the gate-source capacitance voltage (V_{Cgs}) and V_{Rds} are out of phase, would effectively reduce the drain current/gate voltage second-order nonlinearity to create the most severe conversion efficiency degradation: the positive V_{Rds} swing renders the pinch-off region progressively more linear while V_{Cgs} swings into it and the negative V_{Rds} swing makes the pinch-off region progressively more parabolic but V_{Cgs} swings away from it. The effect can be sizeable even if V_{Rds} does not swing out of the saturation region. The drain current waveform's second harmonic has

decreased: we claim that it is minimum there. At the other extreme, drain series resonance, which corresponds to minimum drain voltage modulation of the drain current/gate voltage characteristics, would create the maximum conversion efficiency for the gate bias used. The 180 degrees phase shift naturally occurs at parallel resonance since all the current from the controlled source of the equivalent circuit essentially flows through the channel conductance from the source end.

As a further demonstration of this phenomenon, the mixing transconductance is derived from a well-known GaAs MESFET drain current expression [16] modified to include the pinch-off voltage shift effect. The following expression is used to calculate the transconductance which is Fourier analyzed:

$$I_{DS} = \beta (V_G(t) - V_p')^2 (1 + \lambda V_D(t)) \tanh(\gamma V_D(t)) \quad (11)$$

where $V_p' = V_p(1 + \sigma(V_D(t) - V_{DD0}))$;

V_p is the pinch-off voltage measured at the drain voltage V_{DD0} ;

$V_G(t) = V_{GG} + A \cos(\omega t)$, the gate voltage;

and $V_D(t) = V_{DD0} + B \cos(\omega t + \phi)$, the drain voltage phase shifted by ϕ from $V_G(t)$.

The second term of the series is

$$gm_1 = \beta (1 + \lambda V_{DD0}) (A - \sigma B V_p e^{j\phi}) \quad (12)$$

which is minimum at $\phi = \pi$ because V_p is negative. The complete derivation is presented in Appendix G. Equation (12) demonstrates for this simple model that a 180 degrees phase shift yields the maximum destructive interference from the drain voltage and tends to reconcile our approach with quasi-static models.

The sensitivity of the second-order nonlinearity to the pinch-off voltage shift process

is obviously affected by the gate bias chosen. If the FET is biased close to pinch-off, the drain current waveform is still strongly rectified regardless of the drain-source resistance voltage swing and the conversion gain range will be small (see Section 4.1). However, as the gate bias increases (positively), the mechanism described above will become more and more detrimental. This qualitatively agrees with the experimental observations and our simulation of the FET upconverter behavior.

If this phenomenon is actually responsible for the conversion gain behavior and if the transconductance's voltage dependence can be considered constant over a large enough microwave frequency band, the frequency response of the drain-source resistance voltage renders a progressively decreasing transconductance modulation which implies a diminishing conversion gain dip. As mentioned above, the feedback on the gate-source capacitance may counterbalance this but the necessary information to corroborate this hypothesis is not readily available.

Actual simulations were performed using the curves of Fig. 19-c over a limited range of the drain voltage (1 to 5 V). The 180 degrees phase difference corresponded to the minimum mixing transconductance and the sensitivity to the gate bias as described above was verified, but the simulations failed to predict the degree of variation necessary to account for the observed conversion gain range. More data relevant to high-frequency current-voltage characteristics as obtained with Smith et al's technique [17], for instance, would be necessary to pursue further this idea. Nevertheless, this pinch-off voltage shift concept brings enough physical insight to support our simulations.

CHAPTER 5: APPLICATIONS OF THE METHOD

5.1 Drain network synthesis

In this section, we briefly examine the mechanics of analyzing the performance of an upconverter using Touchstone. For example, a simple drain matching network without rejection specification is to be designed.

- 1) Frequency choice. A fixed IF of 280 MHz and an RF bandwidth of 100 MHz centered at 1.95 GHz are selected. The LO range is thus 1.62 to 1.72 GHz and falls within the previously characterized bandwidth; however, a slightly wider range will be used to study the conversion gain behavior.
- 2) Embedding impedances. The gate is broadband 50 Ω , the drain is short-circuited at IF, and a conjugate match is desired at RF.
- 3) A first approximation for the drain network can be calculated. Here, the initial interest is to match the drain of the FET to a 50 Ω load and disregard any LO frequency loading dependence. A Chebyshev polynomial realization with minimum ripple is calculated with a CAD circuit synthesis program. The resulting network is shown in Fig. 20.
- 4) Appendix H presents a sample Touchstone file used to calculate the IF and LO voltages plus the resulting upper sideband conversion gain. First, the matching network and all the scaling factors, parameters, and element values are input.

Figure 20: Matching network 1

Using the TUNE mode, a first sweep gives both the IF voltages at 70 and 280 MHz for the drain short-circuited and the LO voltages over the bandwidth. $V_{Cgs}(F_{IF})'$ in Equation (5) of Appendix B is calculated (its value is 0.99 here), entered as the IF_{VOL} parameter and the LO quantities are input for one frequency at a time, the file swept again, the calculated conversion gain recorded, and so on until the full bandwidth has been swept. The TUNE mode facilitates the adjustment of the drain network without rerunning the complete program. Any element can be changed and the same procedure repeated. The output return loss can be monitored simultaneously.

Fig. 21 depicts the resulting conversion gain frequency response. In the band of interest, the conversion gain is about -3.4 dB with a slope of only 0.4 dB. Given that the 50 Ω conversion gain was about -1.8 dB and that matching the drain should give a 2 dB improvement, the degraded conversion gain in Fig. 21 is obviously due to suboptimal LO reflection.

Figure 21: CG -vs- frequency with network 1

In fact, based on Fig. 17, the condition to achieve for optimum LO reflection is the largest magnitude of the reflection coefficient possible within a span of about 140 degrees around the series-resonance angle. This guideline can be used to facilitate the design of a first iteration.

- 5) To improve the first design, another Chebyshev network but with a larger ripple (0.3 dB) to steepen its skirts is designed. Fig. 22 depicts the network while Fig. 23 shows its output return loss and the resulting conversion gain over the bandwidth. The conversion gain is now higher (-0.2 to -1.5 dB) but it shows a significant negative slope (1 dB) and the return loss is only marginally acceptable. If better 50 Ω match is required for a specific application, an isolator could be connected in cascade with that network.

Figure 22: Matching network 2

Figure 23: CG and RL -vs- frequency with network 2

Fig. 23-a: CG -vs- frequency

Fig. 23-b: RL -vs- frequency

As can be seen in this simple case, the model allows the selection and optimization of drain networks to obtain a desired upconverter performance. The above process can be continued to narrow down the best network prototype. A good improvement was already noted with the second iteration. The simulation results, depicted over a 250 MHz bandwidth, also suggest that it would be hard to maintain a good flatness over such a wide range and would therefore lead to a practical restriction on the useful and desirable LO tuning range.

5.2 Additional considerations in using the method

1) Gate loading at LO.

The LO level and the gate termination used in the experiment must be carefully reproduced in the simulations, otherwise the model does not hold since the voltage

patterns would now be different. However, in view of the discussion of Section 4.4, it can be expected that if the gate were matched, the conversion gain range would become even larger. In this case, to maintain predictability, the practical solution would be to reduce the test LO power to create internal LO voltage levels at par with the original ones.

2) IF termination at drain and other small-signal impedances.

For maximum gate-source capacitance voltage, the IF drain termination should ideally correspond to the conjugate of the output impedance. However, we have concluded in Section 4.1 that the termination at IF is causing a destructive interference with conversion gain due to the channel conductance. Therefore, the short-circuit cannot be varied without creating extra simulation uncertainty because it contributes to the large-signal solution by limiting the channel conductance contribution.

Yet, both the gate loading at IF and the gate and drain loadings at RF can now be studied with this model and their influence on conversion gain assessed. For example, the gate can be matched at IF to increase conversion gain, and this improvement can be easily calculated; the RF gate termination resulting from the input IF/LO diplexer can also be included in the simulations for more accuracy.

3) Calculation of LO rejection.

This is an important circuit performance variable that can be calculated with this method. The Touchstone file of Appendix H can also output the $|S_{21}|$ of the LO circuit. Given the input LO and IF powers used experimentally, the rejection is simply

calculated as:

$$Rej_{LO} (dB) = P_{IF} + CG - |S_{21}(F_{LO})| - P_{LO} \quad (13)$$

where CG is the conversion gain calculated from the IF/RF circuit, P_{IF} is the input IF power, P_{LO} the input LO power, and all the variables are in dB. Note that the value calculated is only valid for the particular IF power used in the experiment.

4) Limitations of characterization method on upconverter performance.

The choice of the "optimum" bias and LO power has been shown previously to limit somewhat the upper frequency and maximum output RF power performances of a given upconverter. For the former, the broadband 50 Ω conversion gain is about 3 dB lower than that for the "maximum" bias value; given the frequency response of the FET itself, this may cause marginally low conversion gain at higher frequencies. On the other hand, the maximum conversion gain obtained under optimum LO reflection conditions is reduced by less than 1 dB from the "maximum" bias value, and therefore this choice actually does not degrade appreciably the upconverter response. However, for its power handling capability, the relatively low third-order output intercept point and figure of merit obtained indeed make the transistor more suitable for a low- to medium-power intermediate stage of an upconversion chain.

5.3 Dual-gate FET

This is a very interesting structure for many applications. Specifically, for mixers, the second gate allows the injection of LO directly without the need of an IF/LO diplexer since reasonable isolation already exists between the two gates. MMIC applications benefit greatly from its use. The topology of this transistor is very complex; the task of

equivalent circuit element acquisition is much more involved than with the single-gate FET and an accurate physical representation is very difficult to obtain. Nevertheless, its understanding and use would increase appreciably if a simplified design approach could be devised for nonlinear applications.

A simplified equivalent circuit is shown in Fig. 24; its elements are extracted as before. Together, the two FET parts can function in four distinct operational modes (each can operate in either linear or saturated mode); specifying the particular mode enables one to find which element(s) should be nonlinear. This requires thorough DC characterization and the acquisition of the parameters of a DC dual-gate FET model such as in [18]. Even without considering the latter, more insight can be gained by studying the device in a manner similar to the single-gate FET. Preliminary tests of conversion gain as a function of the LO reflection coefficient were performed at 1.50 GHz ($F_{IF} = 70 \text{ MHz}$) with an NEC NE41137 dual-gate FET, an UHF band device, for an LO power of 10 dBm. The FET is biased with -0.95 V on the first gate, -0.83 V on the second gate, and 5.0 V on the drain. No IF drain short-circuit was used and no attempt was made to reduce the level of the LO harmonics, which were already about -18 dBc. Fig. 25 depicts the results; the conversion gain range is only about 3 dB, and the curve is irregular (probably due to the varying IF impedance). For the minimum conversion gain locus, the reflection coefficient has a magnitude of 0.866 and its angle is 48.2 degrees; for the maximum conversion gain locus, the reflection coefficient magnitude is 0.823 and its angle is -131.9 degrees. With a LO reflection circuit as in Fig. 26, where the circuit diagram of Fig. 24 has been redrawn into an equivalent single-gate FET configuration in which the source impedance appears as an active load, the gate-source capacitance ($V_{C_{gs}}$)

Figure 24: Dual-gate FET equivalent circuit

Figure 25: CG -vs- LO reflection coefficient at 1.5 GHz with $\Gamma = 0.83$

and drain-source resistance (V_{Rds}) voltages of the two FET parts are calculated (for a reflection coefficient magnitude of 1) and depicted in Fig. 27. A correlation is observed between the voltage patterns and the measured conversion gain: V_{Rds2} and V_{Cgs2} both peak at about 15 degrees below the measured conversion gain minimum angle and $V_{Rds2}'s$ minimum locus is very close to the measured conversion gain maximum angle; V_{Cgs1} and V_{Rds1} both dip further away from the conversion gain minimum and are flat otherwise, but their amplitude variations are small. Despite these relatively large deviations (given our lack of "complete" experimental control of the upconverter behavior), the correlations observed suggest that our method could apply to this structure, although singling out a particular nonlinear mode is now more difficult.

Figure 26: Dual-gate FET LO reflection circuit

Figure 27: LO voltages -vs- reflection coefficient at 1.5 GHz for $\Gamma = 1$

Fig. 27-a: Vcgs1 -vs- reflection coefficient angle

Fig. 27-b: Vrds1 -vs- reflection coefficient angle

Fig. 27-c: Vcg2 -vs- reflection coefficient angle

Fig. 27-d: Vrds2 -vs- reflection coefficient angle

Fig. 27-e: Phase difference in FET2 -vs- reflection coefficient angle

CHAPTER 6: CONCLUSION

The method presented in this thesis allows conversion gain simulations of FET upconverters over specific bandwidths using a few microwave measurements and three simple equivalent circuits. It is more suitable than Harmonic Balance-based models as a tool for practical design. Using the concept of LO-load dependent mixing transconductance, commercial microwave circuit CAD tools can serve to simulate conversion gain with any particular drain network and allow the optimization of its parameters to obtain desired gain, flatness, and LO rejection over the complete bandwidth. The model will be most useful for monolithic implementations lacking tuning capabilities.

In reality, pure transconductance mixing is not feasible. The modulation of the drain current/gate voltage characteristics by the drain voltage involves an inevitable transconductance-channel conductance coupling; reactive pumping is also present but its contribution simply neglected. Our formulation therefore lumps these various small effects with the transconductance in an elegant fashion.

From a more general point of view, this work has demonstrated the acute importance of the LO drain termination of a gate mixer in determining conversion efficiency. It has been shown that in general, neither the short- nor the open-circuit drain termination at the LO frequency will cause conversion gain extremes.

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APPENDIX A: THE CLASSICAL MIXER THEORY

This appendix gives an overview of the mechanics of the classical mixer theory and makes a parallel between the conversion matrix and the interconnected equivalent circuits which allows an intuitive representation of approximations made in this work.

A-1: Mathematical formulation

First, the time-domain solution of a FET equivalent circuit must be obtained. The characterization of each nonlinear element of the circuit as a function of the controlling voltages can be performed by various methods: direct measurement, analytical models with parameters to be extracted from measured DC and RF data, or from S parameters measured at different bias voltages. Fig. A.1 depicts the extrinsic FET network to be analyzed. The embedding impedances are included at each port. The input voltage level and frequency are set and using a numerical iterative technique such as the

Figure A.1: Nonlinear FET equivalent circuit

Harmonic Balance method, the circuit is solved for the two controlling voltages V_g and V_d ; this represents the large-signal or pump solution. Given the latter which implicitly includes contributions from all the defined nonlinear elements and the equations relating these elements to the voltages, the time dependence of each element can be calculated: its period is equal to that of the pump. With ω_p denoting the pump (LO) radian frequency, each defined nonlinear element (z_i) can be expressed in a complex Fourier series as:

$$z_i(t) = \sum_{k=-\infty}^{\infty} z_{ik} e^{jk\omega_p t} \quad (1)$$

Now, assume that a small-signal $v(t)$ of frequency ω is impressed on the FET. By the mixing action of $z_i(t)$, sideband currents ($= v(t) z_i(t)$) will be created at frequencies:

$$\omega_n = \omega + n\omega_p \quad (2)$$

with n taking all integer values.

We can now proceed to the small-signal solution of the mixer problem. Each of the Fourier components of Equation (1) can be included in the frequency-domain equivalent circuit as voltage-controlled current sources (for example). This is depicted in Fig. A.2. A loop analysis of this circuit considering all the different frequencies but where each transfer relation calculated (IF at gate to IF at drain, IF at gate to RF at drain, etc.) uses only the corresponding controlled sources (one per nonlinear element) then yields:

$$[E] = [Z_m] [I] + [Z_i] [I] \quad (3)$$

where $[E]$ is the input signal(s) vector, $[Z_i]$ is the sideband termination matrix (diagonal), and $[Z_m]$ the results of the loop analysis. The row numbering is arbitrary and corresponds to frequency and port assignments. If the desired output frequency is the result of the subtraction of the LO frequency with $v(t)$'s frequency, then the complex conjugate of $v(t)$ must be used for the calculation of the small-signal solution. Solving for a given sideband requires to calculate the corresponding term of $[I]$ (here denoted by I_o , for output current). The available conversion gain CG_{av} is expressed as:

$$CG_{av} = 4 \frac{|I_o|^2 \operatorname{Re}[Z_o] \operatorname{Re}[Z_{in}]}{|E_{in}|^2} \quad (4)$$

and holds for any desired sideband. Since the FET has two ports and considering k signals (input and sidebands) for the analysis, $[Z_m]$ has $(2k)^2$ elements. For practical reasons the number of elements of the matrix (number of sidebands) is reduced. Generally, only the image, the RF and the IF are considered.

Figure A.2: FET equivalent circuit with element harmonics

A-2: Equivalent circuit interconnections

The conversion matrix can be represented by a series of cross-coupled frequency-selective equivalent circuits because the same I/V equations hold for both. First, Fig. A.3 shows the subdivided conversion matrix obtained from Fig. A.2 with only the IF and RF signals considered when its elements have been positioned to present more clearly the IF/RF port impedance relations. Fig. A.4 depicts the equivalent circuits representation of this matrix. Only the transconductance and the drain-source resistance (the main nonlinearities of a MESFET) are included for simplicity. The source feedback is also neglected for this discussion. The use of these frequency-selective equivalent circuits allows a simple representation of the conversion matrix in frequency-domain CAD programs. Various signal interactions can be visualized in a simple fashion. For instance, Fig. A.5 depicts the case of the lower sideband (LSB) to upper sideband (USB) interaction. As apparent, the USB can only be affected from the transconductance via two feedback couplings: one at LSB generating an inverse conversion to IF, and one at IF creating a new voltage component across the gate-source capacitance, which then perturbs USB. Likewise, LSB is perturbed following a similar path from the USB circuit. However, the drain-source resistance couples these two via the IF drain voltage. Clearly, with the good gate-drain isolation afforded by MESFETs, the low IF frequencies usually involved, and the proper IF drain termination, this perturbation is negligible.

Figure A.3: Conversion equations and diagram

$$\begin{aligned}
 [E] &= \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} + \begin{bmatrix} Z_{t1} & 0 \\ 0 & Z_{t2} \\ 0 & Z_{t3} \\ 0 & Z_{t4} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \\
 &= \begin{bmatrix} Z_{11} & Z_{13} & Z_{12} & Z_{14} \\ Z_{31} & Z_{33} & Z_{32} & Z_{34} \\ Z_{21} & Z_{23} & Z_{22} & Z_{24} \\ Z_{41} & Z_{43} & Z_{42} & Z_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_3 \\ I_2 \\ I_4 \end{bmatrix} + \begin{bmatrix} Z_{t1} & 0 \\ 0 & Z_{t3} \\ 0 & Z_{t2} \\ 0 & Z_{t4} \end{bmatrix} \begin{bmatrix} I_1 \\ I_3 \\ I_2 \\ I_4 \end{bmatrix} \\
 &= \begin{bmatrix} [Z_{IF}] & [Z_{IF/RF}] \\ [Z_{RF/IF}] & [Z_{RF}] \end{bmatrix} \begin{bmatrix} I' \\ I' \end{bmatrix} + \begin{bmatrix} Z_t' \\ Z_t' \end{bmatrix} \begin{bmatrix} I' \\ I' \end{bmatrix}
 \end{aligned}$$

In a similar fashion, the effect of the second LO harmonic on the upper sideband (USB) conversion can be visualized, and this is shown in Fig. A.6. In this case, the third-order characteristics of the FET is of interest, represented by the second harmonic of the nonlinear elements. Now, the lower sideband (LSB) and the USB are coupled by only one feedback via the transconductance, since $2 \text{ LO} - \text{LSB} = \text{USB}$, but they are coupled directly via the drain-source resistance by the same relation. With sizeable second harmonic levels, this will yield larger discrepancies, especially as the operating frequency is increased and as large drain voltage swings occur.

Fig. A.7 depicts the conversion matrix and the resulting RF/IF circuit interconnections that arise from the present method and its approximations. Apart from neglecting the influence of the LSB and of the drain-source resistance (because of the IF drain short-circuit), only the reverse transfer RF/IF coupling terms are omitted, an approximation which is quite reasonable given the frequencies involved and the relatively good gate/drain isolation of MESFETs.

Figure A.4: Conversion equations circuit representation

Figure A.5: LSB/USB interaction

Figure A.6: Second LO harmonic effects

Figure A.7: Approximations of this method

$$[E] = \begin{bmatrix} [Z_{IF}] & [0] \\ [Z_{RF/IF}] & [Z_{RF}] \end{bmatrix} [I'] + [Z_t'] [I']$$

APPENDIX B: HIGH FREQUENCY SIMULATION IMPROVEMENT

B-1: Arbitrary loading at RF

For conceptual simplicity and ease of calculations, the case of gate and drain $50\ \Omega$ loading at the upper sideband frequency was chosen as a basis for determining the mixing transconductance and for subsequent simulations. This approach should be satisfactory when relatively low frequencies are being used since GaAs MESFETs have inherently good gate-to-drain isolation. However, in the general case and particularly at higher frequencies when the gate and drain terminations are not $50\ \Omega$, e.g. for conjugate matching, this representation is not accurate enough. The calculated S_{22} can be substantially different from the measured one when S_{12} is finite and sizeable. Therefore, the "time-averaged" transconductance (the one corresponding to the first term of the transconductance Fourier series) is added to the original IF/RF circuit. This is shown in Fig. B.1. The time-averaged transconductance is simply equal to the value obtained from the large-signal S parameter measurements. The correction to the mixing transconductance (gm^{MIX}) is done as follows:

In the circuit of Fig. 10, from Equation (3), $|S_{21}|$ is written as:

$$|S_{21}| = I(F_{RF}) X(Z_G, Z_D, F_{RF}) \quad (1)$$

where Z_G and Z_D are the gate and drain loading impedances, respectively. When considering the circuit of Fig. B.1,

$$I(F_{RF})' = gm^{MIX'} V_{C_{gs}}(F_{IF}) \quad (2)$$

where $V_{C_{gs}}$ is the gate-source capacitance voltage, so that

$$|S_{21}|' = I(F_{RF})' Y(Z_G, Z_D, F_{RF}) \quad (3)$$

Now when $Z_G = Z_D = 50\ \Omega$, $|S_{21}|' = |S_{21}|$, and

$$gm^{MIX'} = gm^{MIX}(V_{C_{gs}}^{LO}, V_{Rds}^{LO}) \frac{X(50, 50, F_{RF})}{Y(50, 50, F_{RF})} \quad (4)$$

The circuit of Fig. B.1 can now be used with $gm^{MIX'}$ for any type of gate and drain termination at RF.

B-2: IF voltage scaling

Again for simplicity in the calculation procedures with Touchstone, the gate-source capacitance voltage at IF ($V_{C_{gs}}(F_{IF})$) was fixed to 1 to determine Equation (7). In a realistic situation, the value of this voltage is dependent on the gate and drain impedances at IF and on its frequency response over a desired bandwidth. The original experiments leading to the gm^{MIX} expression were conducted at an IF of 70 MHz with the drain short-

circuited and a broadband $50\ \Omega$ source. $V_{C_{gs}}(F_{IF})$ is then corrected for the new IF frequency and gate/drain impedances:

$$V_{C_{gs}}(F_{IF})' = \frac{V_{C_{gs}}(F_{IF})^{new\ loads}}{V_{C_{gs}}(70MHz)^{short-circuit}} \quad (5)$$

Figure B.1: Modified RF/IF circuit for arbitrary loadings

APPENDIX C: LISTING OF PROGRAM TO CALCULATE THE BEST DATA FIT

```

10      REM 12/02/87 BASIC PROGRAM TO PERFORM MULTIVARIABLE
20      REM LINEAR REGRESSION AND FIND THE PARAMETERS GIVING THE
30      REM MINIMUM OF AN ERROR FUNCTION BY A GRID SEARCH.
35      REM USES HP9836 COMPUTER WITH BASIC 3.0 MAT STATEMENTS.
40      REM UP TO 100 DATA POINTS CAN BE INPUT.
50      REM NUMBER OF DATA POINTS MUST BE LARGER THAN NUMBER OF
60      REM VARIABLES.
70      REM FOR UPCONVERTER MIXING TRANSCONDUCTANCE ANALYSIS.
80      REM DATA NECESSARY: EXPERIMENTAL CONVERSION GAIN AND
90      REM CORRESPONDING Vcgs, Vrds, AND THEIR PHASE
100     REM DIFFERENCE IN THIS ORDER.
110     !
120     OPTION BASE 1
130     DEG
140     INTEGER J,K, Choice
150     Nvar = 3                ! number of independent variables
160                               ! dimensioning data arrays
170     DIM Coeff_arr(Nvar,Nvar), Yval_arr(Nvar),Reg_res(Nvar)
180     DIM Data_arr(100,Nvar),Dum2_arr(10,100), Vrc_arr(100)
190     DIM Dum3_arr(10,10), Dum4_arr(10,10), Dum5_arr(10,1)
200     DIM Err_arr(100), Pol_coef(4), Index_kpt(5), Val_arr(100,4)
210     !
220     !
230     BEEP 200, .2
240     INPUT "ENTER # OF DATA POINTS ", Ndata
250     INPUT "ENTER NAME OF DATA FILE ", File_name$
255     INPUT "ENTER S21 TO GMMIX PROPORTIONAL CONSTANT", Sgm
260     !
270     REDIM Data_arr(Ndata,Nvar), Ord_arr(Ndata), Val_arr(Ndata,4)
280     REDIM Est_arr(Ndata),Err_arr(Ndata),Vrc_arr(Ndata)
290     !
300     !                      reads data file
310     ASSIGN @Data_read TO File_name$
320     ENTER @Data_read;Val_arr(*)
330     ASSIGN @Data_read TO *
340     !                      calculates gmmix and Vrds*cos(delta)
350     FOR J=1 TO Ndata
360         Ord_arr(J)=Sgm*(10^(Val_arr(J,1)/20))
370         Vrc_arr(J)=ABS(Val_arr(J,3)*COS(Val_arr(J,4)))
380     NEXT J
390     !
400     Memse = 1                ! initial value for error function
405     !                      main loop

```

```

410     FOR R=0 TO 1 STEP 0.1
420         FOR L=2 TO 4 STEP 0.4
430             FOR P=1 TO 3 STEP 0.4
440                 DISP "R=";R;"L=";L;"P=";P
450                 FOR J=1 TO Ndata      !fills arrays for regression
460                     Data_arr(J,1)=Val_arr(J,2)^R
470                     Data_arr(J,2)=Vrc_arr(J)^L
480                     Data_arr(J,3)=Vrc_arr(J)^P
490                 NEXT J
500                 GOSUB Linreg          ! go calculate regression
510             !
520             IF Se < Memse THEN        ! stores parameters for min
530                 Index_kpt(1)=R
540                 Index_kpt(2)=L
550                 Index_kpt(3)=P
560                 Pol_coef(1)=Reg_res(1)
570                 Pol_coef(2)=Reg_res(2)
580                 Pol_coef(3)=Reg_res(3)
590                 Pol_coef(4)=Se^0.5
600                 Memse = Se
610             END IF
620         NEXT P
630     NEXT L
640 NEXT R
650 !
660 PRINT
670 PRINT "BEST COMBINATION FOUND IS: L= ";Index_kpt(1);"P=";
Index_kpt(2);"R=";Index_kpt(3)
680 PRINT
690 PRINT "COEFFICIENTS ARE: ";Pol_coef(1), Pol_coef(2),
Pol_coef(3)
700 PRINT "STANDARD ERROR :";Pol_coef(4)
710 GOTO 870
720 !
730 Linreg: ! calculates the linear regression
740     MAT Dum2_arr = TRN(Data_arr)
750     MAT Dum3_arr = Dum2_arr * Data_arr
760     MAT Dum4_arr = INV(Dum3_arr)
770     MAT Dum5_arr = Dum2_arr * Ord_arr
780     MAT Reg_res = Dum4_arr * Dum5_arr
790 !
800 ! Calculates the standard error of estimate
810     MAT Est_arr = Data_arr * Reg_res
820     FOR J=1 TO Ndata      ! calculates the error function
830         Err_arr(J)=(Est_arr(J)-Ord_arr(J))/Ord_arr(J)
840     NEXT J

```

```
850      Se = DOT(Err_arr,Err_arr)/(Ndata-Nvar)
860      RETURN
870      END
```


APPENDIX D: EQUIVALENT CIRCUIT ELEMENT ACQUISITION WITH TOUCHSTONE

!9/21/87 File to fit an equivalent circuit to the measured Spar of a
! single-gate FET circuit with simple parasitics for upconverter modelling

VAR

```
Rg # 0 8.36680 15
Rd # 0 7.52852 15
Rs # 0 3.45270 10
Lg # 0 0.63350 1
Ld # .0 0.58499 1
Ls # .0 0.05455 .5
Cin # 0 0.23099 .7
Cout # 0 0.20792 .5
C1 # 0.1 0.33006 .41 ! Cgs
C2 # .01 0.02498 .07 ! Cdg
C3 # .0 0.13315 .51 ! Cds
Ri # 0 17.40076 30
Rds # 150 161.12150 250
gm # .03 0.05023 .075
t = 0
```

```
! drain load angles of maximum input reflection
teta1 = 57.2 ! coefficient @ 2.03 GHz and
teta2 = 68.2
teta3 = 50.2 ! @ 1.39 GHz
teta4 = 60.7
```

```
teta5 = 37.2 ! drain load angles of input reflection
teta6 = 117.5 ! coefficient = 1 @ 2.03 GHz
teta7 = 47.1
teta8 = 107.6
teta9 = 28.0 ! @ 1.39
teta10 = 127.1
teta11 = 34.6
teta12 = 120.5
```

EQN ! corresponding electrical lengths

```
ea = (180-teta1)/2
eb = (180-teta2)/2
ec = (180-teta3)/2
ed = (180-teta4)/2
```

```

ee = (180-teta5)/2
ef = (180-teta6)/2
eg = (180-teta7)/2
eh = (180-teta8)/2
ei = (180-teta9)/2
ej = (180-teta10)/2
ek = (180-teta11)/2
el = (180-teta12)/2

```

CKT

```

s2pa 1 2 0 b:ne7001b    ! measured S parameters
def2p 1 2 nmod

srl 1 2 r^Rg l^Lg      ! equivalent circuit
cap 1 0 c^Cin
fet 2 3 10 g^gm t^t f=0 cgs^C1 ggs=0 ri^Ri cdg^C2 cdc=0 cds^C3 rds^Rds
srl 10 0 r^Rs l^Ls
srl 3 4 r^Rd l^Ld
cap 4 0 c^Cout

```

```
def2p 1 4 neckt1
```

! reflection circuits to fix particular values of impedances

```

neckt1 1 2
tlin 2 4 z=50 e^ea f=2.03
shor 4
def1p 1 gamamax1
    neckt1 1 2
    tlin 2 4 z=50 e^eb f=2.03
    res 4 0 r=5.55556
    def1p 1 gamamax2
neckt1 1 2
tlin 2 4 z=50 e^ec f=1.39
shor 4
def1p 1 gamamax3
    neckt1 1 2
    tlin 2 4 z=50 e^ed f=1.39
    res 4 0 r=5.55556
    def1p 1 gamamax4
neckt1 1 2
tlin 2 4 z=50 e^ee f=2.03
shor 4
def1p 1 gammamain1
    neckt1 1 2

```

```

tlin 2 4 z=50 e^ef f=2.03
shor 4
deflp 1 gammain2
neckt1 1 2
tlin 2 4 z=50 e^eg f=2.03
res 4 0 r=5.55556
deflp 1 gammain3
neckt1 1 2
tlin 2 4 z=50 e^eh f=2.03
res 4 0 r=5.55556
deflp 1 gammain4
neckt1 1 2
tlin 2 4 z=50 e^ei f=1.39
shor 4
deflp 1 gammain5
neckt1 1 2
tlin 2 4 z=50 e^ej f=1.39
shor 4
deflp 1 gammain6
neckt1 1 2
tlin 2 4 z=50 e^ek f=1.39
res 4 0 r=5.55556
deflp 1 gammain7
neckt1 1 2
tlin 2 4 z=50 e^el f=1.39
res 4 0 r=5.55556
deflp 1 gammain8

```

PROC ! to calculate the error function for the S parameters

```

moddif = neckt1 - nemod
ratio = moddif / nemod

```

OUT

FREQ

```

sweep .15 2.480 .238

```

OPT

```

! goals for S parameters fit
ratio mag[s11] = 0
ratio mag[s12] = 0
ratio mag[s21] = 0
ratio mag[s22] = 0

```

! goals for input reflection coefficient fit
range 2.0299 2.0301

!

gamamax1 mag[s11] = 1.11
gamamax2 mag[s11] = 1.03
gammain1 mag[s11] = 1
gammain2 mag[s11] = 1
gammain3 mag[s11] = 1
gammain4 mag[s11] = 1

range 1.3899 1.3901

!

gamamax3 mag[s11] = 1.1
gamamax4 mag[s11] = 1.04
gammain5 mag[s11] = 1
gammain6 mag[s11] = 1
gammain7 mag[s11] = 1
gammain8 mag[s11] = 1

APPENDIX E: CONVERSION GAIN SIMULATIONS FOR SAMPLE 3

Fig. E-1: Mag = 0.6, F = 1.46 GHz

Fig. E-2: Mag = 0.4, F = 1.46 GHz

Fig. E-3: Mag = 0.8, F = 1.46 GHz

Fig. E-4: Mag = 0.8, F = 1.52 GHz

Fig. E-5: Mag = 0.8, F = 1.59 GHz

Fig. E-6: Mag = 0.8, 0.6, 0.3, F = 1.8 GHz; calculated

Fig. E-7: Mag = 0.8, 0.6, 0.3, F = 1.9 GHz, calculated

Fig. E-8: Mag = 0.8, 0.6, 0.3, F = 2 GHz, calculated

Fig. E-9: Mag = 0.8, F = 2.1 GHz

Fig. E-10: Mag = 0.6, F = 2.1 GHz

Fig. E-11: Mag = 0.4, F = 2.1 GHz

APPENDIX F: FREQUENCY RESPONSE OF LO VOLTAGES FOR $\Gamma = 1$

Fig. F-1: Freq = 1 GHz

Fig. F-2: Freq.= 3 GHz

Fig. F-3: Freq = 5 GHz

Fig. F-4: Freq = 7 GHz

Fig. F-5: Freq = 9 GHz

Fig. F-6: Freq = 10 GHz

Fig. F-7: Freq = 12 GHz

APPENDIX G: DERIVATION OF MIXING TRANSCONDUCTANCE EXPRESSION FROM A LINEAR MODEL

In this appendix, I derive the expression for the second term of the Fourier series of the transconductance obtained from a quasi-static MESFET model [16].

The original drain-source current expression of reference [16] is slightly modified in this context and is written as:

$$I_{DS} = \beta (V_G - V_p)^2 (1 + \lambda V_D) \tanh(\gamma V_D) \quad (1)$$

where V_p is the terminal pinch-off voltage (the equivalent of V_T of [16]), V_G is the gate voltage, V_D is the drain voltage, and where the other parameters have their usual meaning. The transconductance gm is defined as:

$$gm = \left. \frac{\partial I_{DS}}{\partial V_G} \right|_{V_D} \quad (2)$$

and from (1), its expression is

$$gm = 2\beta (V_G - V_p) (1 + \lambda V_D) \tanh(\gamma V_D) \quad (3)$$

Now let V_p be replaced by $V_p' = V_p (1 + \sigma \Delta V_D)$ to model the pinch-off voltage shift, in which $\Delta V_D = V_D - V_{DD0}$ (V_{DD0} is the drain bias voltage at which V_p is measured) and σ is the linear pinch-off voltage shift factor.

Expressing V_G as $V_G(t) = V_{GG} + A \cos(\omega t)$, where V_{GG} is the gate bias, and V_D as $V_D(t) = V_{DD0} + B \cos(\omega t + \phi)$, where ϕ is the phase of $V_D(t)$ relative to $V_G(t)$, and inserting these in (3) gives:

$$gm(t) = 2\beta \left[V_{GG} + A \cos(\omega t) - V_p - \sigma V_p B \cos(\omega t + \phi) \right] \times \left[1 + \lambda (B \cos(\omega t + \phi) + V_{DD0}) \right] \tanh \left[\gamma (V_{DD0} + B \cos(\omega t + \phi)) \right] \quad (4)$$

Expanded as a complex Fourier series, $gm(t)$ can be written as:

$$gm(t) = \sum_{k=-\infty}^{\infty} gm_k e^{j\omega_k t} \quad (5)$$

where

$$gm_k = \frac{1}{2\pi} \int_{-\pi}^{\pi} gm(t) e^{-j\omega_k t} d\omega t \quad (6)$$

At this point, a simplification is necessary in equation (4) in order to carry out the integrations analytically. By noting that

$$\tanh\left[\gamma(V_{DD0} + B \cos(\omega t + \phi))\right] = \frac{\tanh\left[\gamma V_{DD0}\right] + \tanh\left[\gamma B \cos(\omega t + \phi)\right]}{1 + \tanh\left[\gamma V_{DD0}\right] \tanh\left[\gamma B \cos(\omega t + \phi)\right]} \quad (7)$$

and if the FET is operated well in its current saturation region, then $\tanh\left[\gamma V_{DD0}\right] \approx 1$ so that (7) ≈ 1 .

For $k = 1$, Equation (4) is inserted in Equation (6) and

$$gm_1 = \frac{\beta}{\pi} \int_{-\pi}^{\pi} \left[V_{GG} + A \cos(\omega t) - V_p - \sigma V_p B \cos(\omega t + \phi) \right] \left[1 + \lambda (V_{DD0} + B \cos(\omega t + \phi)) \right] e^{-j\omega t} d\omega t \quad (8)$$

This integral can be separated in two parts:

$$gm_1^A = \frac{\beta}{\pi} \int_{-\pi}^{\pi} \left[V_{GG} + A \cos(\omega t) - V_p - \sigma V_p B \cos(\omega t + \phi) \right] (1 + \lambda V_{DD0}) e^{-j\omega t} d\omega t \quad (9)$$

$$gm_1^B = \frac{\beta}{\pi} \int_{-\pi}^{\pi} \left[V_{GG} + A \cos(\omega t) - V_p - \sigma V_p B \cos(\omega t + \phi) \right] \left[\lambda B \cos(\omega t + \phi) \right] e^{-j\omega t} d\omega t \quad (10)$$

With

$$\cos(\omega t) = \frac{e^{j\omega t} + e^{-j\omega t}}{2} \quad (11)$$

$$gm_1^A = \frac{\beta}{2\pi} (1 + \lambda V_{DD0}) \int_{-\pi}^{\pi} \left[A + A e^{-2j\omega t} - \sigma V_p B e^{j\phi} - \sigma V_p B e^{-2j\omega t - j\phi} + V_{GG} e^{-j\omega t} - V_p e^{-j\omega t} \right] d\omega t \quad (12)$$

This is easily evaluated, and gives

$$gm_1^A = \beta (1 + \lambda V_{DD0}) (A - \sigma V_p B e^{j\phi}) \quad (13)$$

Likewise, gm_1^B is evaluated using (11) and simply equals 0.

Hence,

$$gm_1 = \beta (1 + \lambda V_{DD0}) (A - \sigma V_p B e^{j\phi}) \quad (14)$$

We want to find the angle ϕ at which gm_1 will be minimized, corresponding to the case of maximum mixing transconductance degradation due to the drain voltage.

The modulus of gm_1 is:

$$|gm_1|^2 = \left[\beta(1 + \lambda V_{DD0}) \right]^2 \left[(A - \sigma V_p B \cos\phi)^2 + (\sigma V_p B \sin\phi)^2 \right] \quad (15)$$

Expanding the rightmost bracketed term gives:

$$A^2 - 2A \sigma V_p B \cos\phi + \sigma^2 V_p^2 B^2 \quad (16)$$

By inspection, this term is maximum at $\phi = \pi$ and minimum at $\phi = 0$. However, since V_p is negative, gm_1 becomes minimum at $\phi = \pi$.

Hence this simple formulation using a linear (gatewise) transconductance with a linear pinch-off shift factor shows that the calculated π phase shift between drain and gate voltages would lead to maximum drain voltage interference. Furthermore, it shows that a close correlation exists between a common quasi-static expression (Eq. (16)) and the mixing transconductance function we have experimentally obtained in this work, both involving the magnitude of the voltages and the cosine of their phase difference.

APPENDIX H: UPCONVERTER SIMULATION WITH TOUCHSTONE

! 3/15/88 File to allow optimization of output circuit in the design of
! FET upconverters by calculating the dependence of a mixing
! transconductance on LO voltages as well as matching and
! filtering at the chosen sideband. All the signals' equivalent
! circuits are considered here: an IF circuit to calculate the
! IF coupling on the gate cap, that subsequently scales the
! gmmix expression; an LO circuit which is used to calculate
! the internal driving voltages given the output circuit used
! and which links them to gmmix; an RF circuit which is
! used with a dummy input voltage source to calculate the conver-
! sion gain when the mixing source is included

VAR

Rg = 7.8637
Rd = .29302
Rs = 7.08732
Lg = .04031
Ld = .2069
Ls = .1228
Cin = .31203
Cout = .31017
Cgs = .391
Cgd = .01948
Cds = .09327
Ri = 17.92754
Rds = 138.5854

gm = .06317 ! time-averaged transconductance

l1 = 1.316801 ! drain matching network

l2 = 44.48747

l3 = 98.21057

c1 = 6

c2 = .212947

ifvol = .9979 ! IF voltage coupling on Cgs at IF

scal1 = 1.3049 ! gmmix expression scaling factor

exp1 = .7 ! parameters of the gmmix expression

exp2 = .2

exp3 = 2.9


```
coef1 = .030288
coef2 = -.01012858
coef3 = -.00006069084
```

```
vcg = 1.504      ! calculated LO voltages
vrd = 7.8
teta = 194.95    ! phase difference
```

EQN

```
vrdc = -vrd * cos(teta) / 2
gmm = coef1 * (vcg / 2)**exp1 + coef2 * vrdc**exp2 + coef3 * vrdc**exp3
gmmix = gmm * ifvol * scal1
```

CKT

```
plc 1 0 l^l1 c^c1 ! matching network derived earlier
ind 1 2 l^l2
ind 2 0 l^l3
cap 2 3 c^c2
def2p 1 3 matchnet
```

```
srl 1 2 r^Rg l^Lg    ! FET common to IF, LO, and RF
cap 1 0 c^Cin
vccs 2 3 5 10 m^gm a=0 r1=0 r2^Rds f=0 t=0 ! time-average source
cap 2 5 c^Cgs
cap 2 3 c^Cgd
cap 3 10 c^Cds
res 5 10 r^Ri
srl 10 0 r^Rs l^Ls
srl 3 4 r^Rd l^Ld
cap 4 0 c^Cout
```

```
opamp 5 2 20 5 0 m=1 a=0 r1=0 r2=0 r3=0 r4=0 f=0 t=0 ! cgs probing
opamp 10 3 25 10 0 m=1 a=0 r1=0 r2=0 r3=0 r4=0 f=0 t=0 ! rds probing
```

```
vccs 50 3 0 10 m^gmmix a=0 r1=0 r2=0 f=0 t=0 ! mixing source
```

```
def5p 1 20 25 50 7 comfet
```

```
comfet 1 2 3 4 5
matchnet 5 6
match 6
match 4
def3p 1 2 3 lorefl    ! circuit for LO voltages calc
```

```
comfet 1 2 3 4 5
```

```

short 5
match 4
match 3
def2p 1 2 ifcoup      ! circuit for calculation of Vcgs at IF

```

```

comfet 1 2 3 4 5
match 1              ! gate term at RF
match 2
match 3
def2p 4 5 rfupc      ! circuit for IF to RF conversion calc

```

OUT

```

ifcoup mag[s21]      ! mag Vcgs at IF
lorefl s21           ! Vcgs, mag and phase at LO
lorefl s31           ! Vrds, mag and phase at LO
rfupc db[s21]        ! conversion gain
rfupc db[s22]        ! return loss at output

```

FREQ

```

step .07 .28         ! IF frequencies
sweep 1.57 1.82 .05  ! LO band
sweep 1.85 2.1 .05   ! RF band

```