GaAs MESFETS AND THEIR APPLICATIONS IN DIGITAL LOGIC AND DIGITAL TO ANALOG CONVERSION

by

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ABSTRACT

The purpose of the work described in this thesis was to study the use of GaAs MESFETs in digital logic and digital to analog conversion. A part of this work was to test ideas by actually fabricating GaAs MESFET devices in our laboratory by implanting Si into LEC SI GaAs. Initially, the Rockwell "ion implanted planar process" was used. With this process high source and drain resistance result when the magnitude of the threshold voltage is reduced. A recessed gate process was then tried in order to reduce the series resistance, but it was difficult to control in order to achieve an acceptable uniformity. Sadler's self-aligned gate technique was then tried but an acceptable yield was found to be hard to achieve.

Based on the experience with the above methods, a Self Aligned Gate Technique Using Polyimide (SAGUPI) was developed. Using this technique it was found to be possible to reduce the series resistance of the transistor and achieve acceptable yields and uniformities.

The characteristics of devices fabricated using the ion implanted planar process were measured. The transistor I-V characteristic parameters, Schottky and ohmic contact parameters and implanted region parameters were measured at room temperature and as a function of temperature over the range from -80°C to 80°C. It was found that no large change in the speed of the circuit occurs over this range.

A new digital logic (the Common Drain FET Logic, CDFL) was developed for the application in Ultra High Speed Very Large Scale of Integration. The performance of the new logic was compared with that of other GaAs MESFET logic using computer simulation. The simulation results showed that the

CDFL has potential for meeting the UHS VLSI requirements.

Two 3 bit Digital to Analog Converters (DAC) (one with MESFETS as current sources and the other with saturated resistors) were developed. MESFETs gave better current source characteristics than saturated resistors.

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LIST OF SYMBOLS

a (m)	channel thickness
a^* (m)	effective channel thickness
A (m^2)	area
A^{**} (cm^2/K^2)	effective Richardson constant
C (F/m^2)	capacitance per unit area
C_g (F)	gate capacitance
C_{gd} (F)	gate drain capacitance
C_{gs} (F)	gate source capacitance
C_L (F)	load capacitance
d (m)	pad length
G (S)	total conductance
g_d (S)	channel conductance
g_m (S)	transconductance
I_{ds} (A)	drain source current
I_{dsat} (A)	saturation drain source current
I_f (A)	forward bias current
I_s (A)	saturation current
J_f (A/m^2)	forward current density
J_s (A/m^2)	saturation current density
k	Boltzmann's constant
ℓ (m)	length of the space between pads
L_c (m)	length of the source drain separation
L_T (m)	transfer length
N (cm^{-3})	electron concentration

n	ideality factor
n' (cm^{-3})	peak impurity density
N_D (cm^{-3})	concentration of the ionized donor atoms
P (W)	power
q (C)	charge of the electron
R_C (Ω)	contact resistance
R_d (Ω)	drain resistance
R_E (Ω)	end resistance
R_p (m)	projected range
R_s (Ω)	source resistance
R_{SH} (Ω)	sheet resistance
R_{SK} (Ω)	sheet resistance of the layer directly under the contact
R_T (Ω)	total resistance
$T_{(K)}$	temperature
V_{ds} (V)	drain-source voltage
V_f (V)	forward voltage
V_{fs} (V)	full scale output voltage
V_{gd} (V)	gate-drain voltage
V_{gs} (V)	gate-source voltage
V_i (V)	input voltage
V_m (V)	voltage swing
V_o (V)	output voltage
V_p (V)	pinch-off voltage
V_{sat} (V)	saturation voltage

V_{th} (V)	threshold voltage
W (m)	pad width
W_d (m)	depletion region width
W_g (m)	gate width
β (A/V^2)	transconductance parameter
ε (F/cm)	permittivity
η (%)	efficiency
μ (cm^2/Vs)	mobility
ρ (Ω/cm)	specific resistance
ρ_c (Ω/cm^2)	contact specific resistance
σ_p (m)	standard deviation in projected range
τ_d (s)	delay time
ϕ'(ions/cm^2)	fluence of the activated atoms
ϕ(ions/cm^2)	implanted dose
ϕ_{bn} (V)	barrier height

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LIST OF ACRONYMS

BFL	Buffered FET Logic
CCL	Capacitor Coupled Logic
CDFL	Common Drain FET Logic
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DCFL	Directly Coupled FET Logic
FET	Field Effect Transistor
FFS	Feed Forward Static
I.C.s	Integrated Circuits
JFET	Junction Field Effect Transistor
LEC	Liquid-Encapsulated Czochralski
LPFL	Low Pinch-off FET Logic
LSI	Large Scale of Integration
MESFET	Metal Semiconductor Field Effect Transistor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	n-channel MOS
PMOS	p-channel MOS
PFM	Polytetra-Fluoropropyl Methacrylate
SAGUPI	Self Aligned Gate using Polyimide
SAINT	Self-Aligned Implantation for n^+ layer Technique

SCFL	Source Coupled FET Logic
SDFL	Schottky Diode FET Logic
SEM	Scanning Electron Microscope
SOS	Silicon-On-Sapphire
UFL	Unbuffered FET Logic
VLSI	Very Large Scale Integration

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To my wife Manal

CHAPTER (1)

INTRODUCTION

Since Van Tuyl and Liechti [1] reported the first GaAs digital logic in 1974 using Metal semiconductor Field Effect Transistors (MESFETS), great progress has been achieved in the GaAs Integrated circuits (I.C.s) area. The driving force behind this progress was the urgent need for Ultra High Speed (UHS) I.C.s which can potentially be achieved by using GaAs because of the higher electron mobility and the semi-insulating property of the GaAs material.

The intrinsic electron mobility of GaAs is 8500 cm^2/Vs compared to 1500 cm^2/Vs for silicon [2]. A typical GaAs MESFET transistor with channel doping concentration of about 2×10^{17} cm^{-3} and has electron mobility of about 4500 cm^2/Vs compared to a typical 800 cm^2/Vs for silicon Metal Oxide Semiconductor (MOS) devices [3]. In addition to the higher mobility, GaAs has a higher peak electron velocity, Fig.(1-1), which leads to a reduced transit time between electrodes, intrinsic high-frequency capability [4], and increased high frequency gain for microwave FETs. The high electron mobility as well as the peak electron velocity are achieved at low electric field. Therefore, high speed of operation with low power dissipation can be achieved at the same time.

The semi-insulating property of GaAs makes it possible for direct isolation between devices on the same chip without the need for isolating islands (as in the case of Si). It leads also to a reduced chip parasitic capacitance which leads in turn to a faster speed of operation.

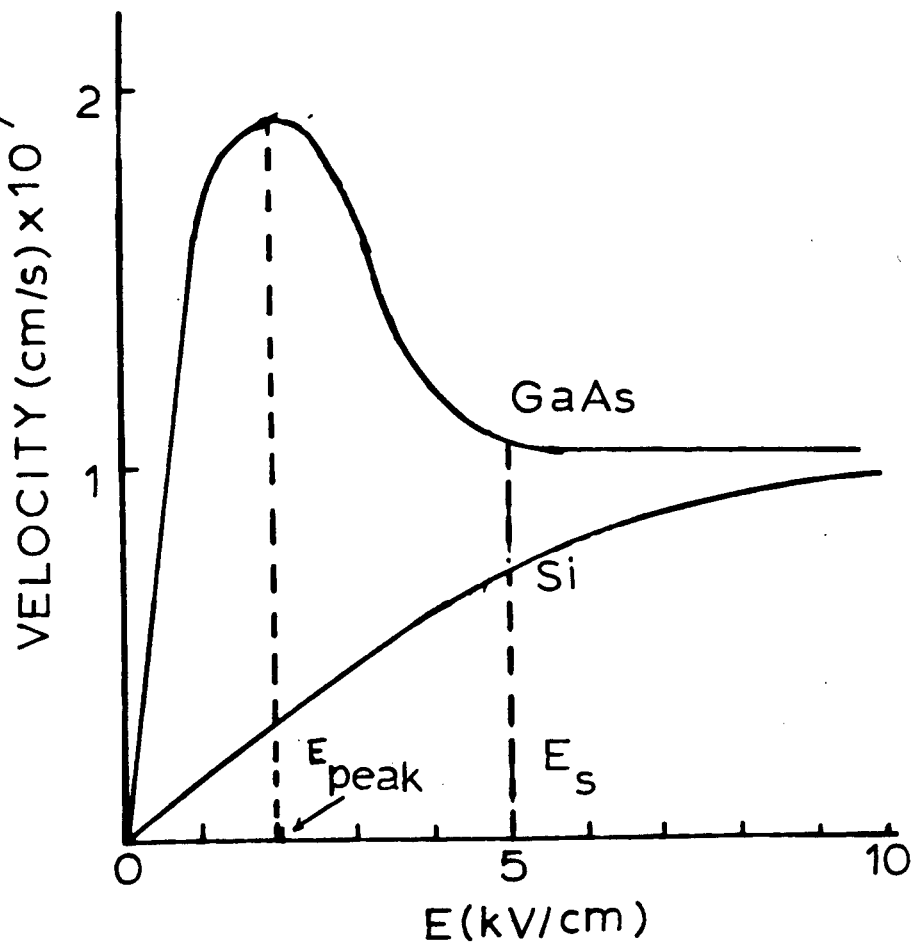


Fig.(1-1) Steady state velocity-field characteristics for electrons in Si and GaAs [6].

To appreciate the advantages of GaAs, let us look back at the history of Si technology. Most of the early MOS work used p-type MOS (PMOS) because of the higher yield of enhancement mode transistors with p channels as compared to n channels. However, to gain the advantage of the 2.5 times higher mobility of electrons in silicon compared to holes, the n-type MOS (NMOS) technology was developed. On the other hand, Complementary MOS (CMOS) was developed to achieve low power circuits and the CMOS/silicon-on-sapphire (SOS) to take advantage of the low parasitic capacitance of the semi-insulating, SOS material. The emerging question now is whether it is worthwhile to spend a great deal of money and time on GaAs research to exploit the six times higher electron mobility and the semi-insulating property at the same time. The answer, I believe, should be yes.

InP has electric properties similar to those of GaAs, therefore, it is considered as an alternative material to produce I.C.s operating in the gigabit range. Maloney and Frey [5] have shown that the maximum switching frequency for unity gain InP Field Effect Transistors (FETs) at room temperature should be about 48% higher than that of GaAs FETs having the same dimensions. However, InP MESFETs have poor logic performance due to:
(a) low Schottky barrier height (0.5eV) [6] which leads to a reduced gate-drain reverse bias voltage
(b) relatively large drain current flow when the device is pinched off [7].

InP fabrication technologies for MESFETs and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are still in their early stages. However, InP MOSFETs have great potential for being used in the future due to their low surface states density which will make them function properly at low

frequencies, < 5KHz (which is not the case for GaAs MOSFETs). However, high yield fabrication techniques must be developed for InP before its advantages can be realized.

GaInAs has higher low field mobility and peak velocity than GaAs, but it has a very low Schottky barrier height (0.3eV) [6]. Since other materials, which may have similar characteristics to GaAs, do not have a developed fabrication technique, their chance of being used commercially in the near future is very slim. Therefore, GaAs is considered the best candidate, in the near future, for UHS I.C.s in terms of material properties and fabrication technology.

The major area of application for GaAs, besides analog microwave applications, is UHS I.C.s. This area covers the application in high speed transmission data systems, high speed signal processing, satellite communications, high speed computers, and test and measurement systems. The above applications need very complex systems, therefore they need not only Ultra High Speed (UHS) of operation but also Very Large Scale of Integration (VLSI). Eden et al. [3] have defined the principal requirements for UHS-VLSI systems as:

(a) very high density of integration (low chip area per gate)

(b) low power dissipation

(c) high speed of operation (very low gate time delay)

(d) extremely low power - time delay product

(e) very high process yield (sufficient to achieve acceptable chip yields)

These requirements are not listed here according to priority; no priority is

possible since all must be met at the same time to realize high performance UHS-VLSI systems.

Si based technology can meet requirements (a) and (e) due to the impressive advances in lithography and fabrication technology. However, it is hard for it to meet the other requirements at the same time since higher electron velocity in Si requires higher field and consequently higher power dissipation, see Fig.(1-1).

On the contrary, GaAs requires lower field for high electron velocity, therefore, requirements (b), (c), and (d) can be met at the same time. The other two requirements can be met if appropriate logic approaches and fabrication techniques can be developed. However, the most important fact is that the problems facing GaAs are design and technological problems which can be solved if enough money and effort are assigned to GaAs research. With Si, on the contrary, the problems are due to basic physical limitations.

The objective of the work described in this thesis was to study GaAs I.C.'s using ion implantation. The main achievements were:

(a) The development of a fabrication process.

(b) The characterization of MESFET transistors fabricated in our laboratory using this process.

(c) The development of a new digital logic family.

(d) The development of a 3-bit digital to analog converter.

In Chapter(2), the analysis of GaAs MESFETs, Schottky diodes, saturated resistors, and resistors is discussed. The saturated resistor is used in this work as a current source for the Digital to Analog Converter (DAC). An overview of GaAs fabrication techniques is given in this chapter. In

Chapter(3), the ion implanted planar process, recessed gate process, and Self Aligned Gate Using Polyimide (SAGUPI) process are discussed. The DC and temperature measurements of GaAs MESFET are presented in Chapter(4). An overview of the different GaAs logic approaches is presented in the first section of Chapter(5). In the second section, the analysis, fabrication, and measurements of the Common Drain FET Logic (CDFL) approach are presented. A comparative study within the GaAs MESFET logic groups is presented in Chapter(5). The JFET Model of the SPICE.2G program [14] was used to simulate the performance of these approaches. In Chapter(7), the analysis, fabrication and measurement of two 3-bit DAC are discussed. In the second section of Chapter(7) the saturated resistor is evaluated as a current source. Conclusions and suggestions for future work are discussed in Chapter(8).

CHAPTER(2)

REVIEW OF GaAs DEVICES AND TECHNOLOGIES

Different types and structures of transistors have been developed to realize GaAs high speed I.C.s. Next to the Metal Semiconductor Field Effect Transistor (MESFET), the Junction Field Effect Transistor (JFET) is the most developed transistor. JFETs have a higher gate barrier height than MESFETs. This makes them attractive for use in Directly Coupled FET Logic (DCFL). Despite the need for an extra implant to give the p type region, JFETs have higher gate capacitance than MESFETs because the junction area between the p^+ region and a channel is normally larger than the junction area between the gate metal and the channel in MESFETs.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Metal Insulator Field Effect Transistor (MISFET) were developed primarily for the use in the DCFL (see Chapter(5)) where (unlike MESFETs) no excessive current would flow if a positive voltage >0.8 V was applied to the gate and consequently high voltage swing could be used. The main problem facing the above two types, besides the fabrication difficulties, is the oxide instability and the high surface state density which made them impossible to work properly at D.C.

Other GaAs transistors such as bipolar, heterojunction, and permeable base transistors have good potential for future applications; however, high yield and reproducible fabrication techniques suitable for a high level of integration have not been developed as yet.

2-1 GaAs MESFETS

The two types of MESFETs used in GaAs I.C.s are the depletion type, which has negative threshold voltage, and the enhancement type, with a positive threshold voltage. Fig.(2-1) shows the structure of both depletion and enhancement MESFET transistors. The channel of the depletion one is not fully depleted at gate to source voltage $V_{gs} = 0$, therefore, a negative gate to source voltage is required to deplete the channel and turn the transistor OFF. While the channel of the enhancement transistor is fully depleted at $V_{gs} = 0$, a positive gate to source voltage is required to turn the transistor ON. A fully depleted channel at $V_{gs} = 0$ V requires the channel to be thin and lightly doped and this leads in turn to a higher channel resistance.

The maximum V_{gs} voltage allowed (for both depletion and enhancement modes) is about 0.7 volt, otherwise an excessive current will flow from the gate to the source. Therefore, the voltage swing of the enhancement mode transistors is limited to 0.7 volt since the lower value of the threshold voltage V_{th} is 0 V. A tight control of the threshold voltage is required, in this case, to prevent the degradation of the swing voltage.

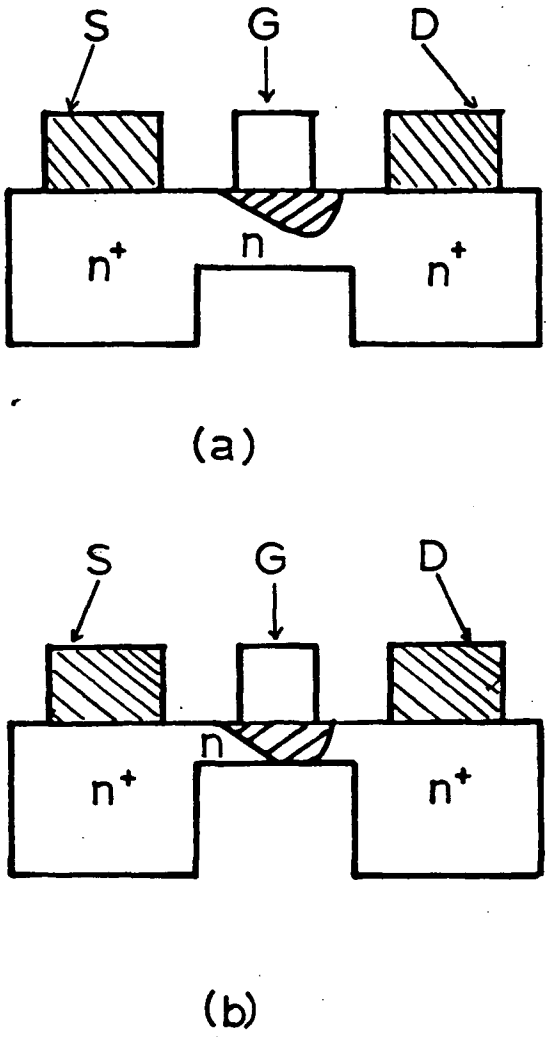


Fig.(2-1) MESFET structure (a) depletion mode and (b) enhancement mode; the shaded areas under the gates are the depletion region areas. (S = source, G = gate, and D = drain)

In general, depletion mode transistors operate at higher speed due to their larger voltage swing and lower channel resistance. They are also easier to fabricate because less tight control on the threshold voltage is required. Enhancement mode transistors have high series resistance, and low voltage swing. In spite of this, the enhancement mode transistor has a great potential since it allows DCFL to be simplified [38].

Many models for GaAs MESFETs have been developed over the last fifteen years. Some of them are analytical models [8-11] and others are numerical models [12-13]. However, the MOS-like analytical model [3] will be considered in this discussion because it is simple, suitable for understanding the transistor physics, and used for circuit simulation in the SPICE2 program [14].

The steady state I-V characteristics for a uniformly doped channel have been derived by Shockley [15]. According to this theory the drain current (assuming $v = \mu E$) is

$$I_{ds} = (\mu\varepsilon W_g/aL_g)[(V_{gs} - V_{th})V_{ds} - V^2_{ds}/2] \qquad (2\text{-}1)$$

and the current saturates for

$$V_{ds} > V_{sat} = V_{gs} - V_{th} \qquad (2\text{-}2)$$

when the channel pinches off.

The saturation current then will be

$$I_{dsat} = \beta(V_{gs} - V_{th})^2 \qquad (2\text{-}3)$$

where

$$\beta = \mu\varepsilon W_g/2aL_g \tag{2-4}$$

For an ion implanted channel, equation (2-3) is still accurate with β replaced by [47]

$$\beta_1 = W_g\mu\varepsilon/2a_{eff}L_g \tag{2-5}$$

where

$$a_{eff} = R_p + 2\sqrt{\sigma p} \tag{2-6}$$

For short channel transistors ($L_g < 2\mu m$), the current saturates before the channel is pinched off due to the electron velocity saturation. For enhancement mode transistors, expression (2-3) can be modified [16] for drift field-velocity saturation by replacing

$\mu V_{sat}/L_g = \mu(V_{gs} - V_{th})/L_g$ by v_s which results in

$$I_{dsat} = (W_g\varepsilon v_s/2a)(V_{gs}-V_{th}) \tag{2-7}$$

For short channel depletion mode transistors, expression (2-3) is still accurate [17] with the replacement of β by

$$\beta_2 = (2\varepsilon\mu v_s W_g/a(\mu V_p + 3v_s L_g)) \tag{2-8}$$

The FET transconductance expression is

$$g_m = dI_{ds}/dV_{gs} \text{ at constant } V_{ds} \tag{2-9}$$

taking $V_{ds} > V_{sat}$, the transconductance will be

$$g_m = d(\beta(V_{gs} - V_{th})^2)/dV_{gs} = 2\beta(V_{gs} - V_{th}) \tag{2-10}$$

The channel conductance of a FET is

$$g_d = dI_{ds}/dV_{ds} \text{at constant } V_{gs} \tag{2-11}$$

from equation (2-1), equation (2-11) will be

$$g_d = 2\beta[(V_{gs} - V_{th}) - V_{ds}] \tag{2-12}$$

When V_{ds} tends to 0, equation (2-12) becomes

$$g_d = 2\beta(V_{gs} - V_{th}) \qquad (2\text{-}13)$$

which is similar to equation (2-10)

2-2 GaAs Saturated Resistors

The saturated resistor is a two terminal device which can be used as a load element for digital logic [18]. The structure of this device is an n layer, similar to that of a MESFET, terminated by two n+ regions for ohmic contacts, Fig.(2-2.a). The I-V characteristic of the saturated resistor, shown in Fig.(2-2.b), is similar to that of a MESFET with fixed V_{gs} value except that the current saturates due to the electron drift velocity saturation rather than due to the pinch off of the channel.

Assuming a uniformly doped channel, the saturation current will be

$$I_{ds} = qW_g n v_s a \qquad (2\text{-}14)$$

while the current in the linear region can be obtained from

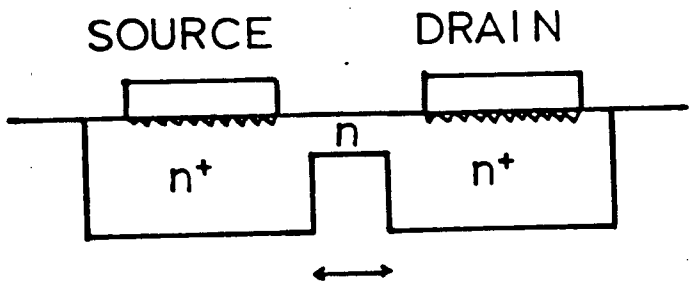
$$I_{ds} = qW_g n a \mu V_{ds}/L_{ch} \qquad (2\text{-}15)$$

The high saturation field of Si (20 kV/cm compared to 3 kV/cm in GaAs) makes it hard to fabricate Si saturated resistors with practical dimensions, since a very small channel length is required to get saturation at a reasonably low voltage.

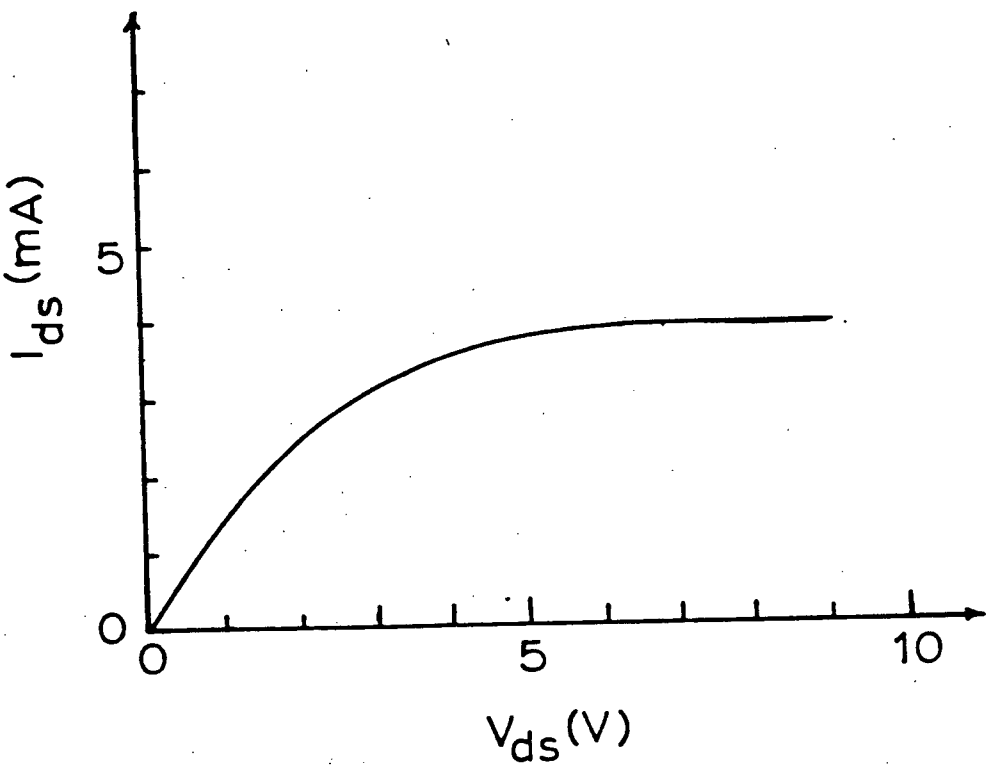
Lee et al. [18] have reported that the use of saturated resistor has the following advantages over the use of MESFET load:

(a) lower capacitance,

(b) higher integration density,



(a)



(b)

Fig.(2-2) Saturated resistor (a) structure and (b) I-V characteristics

(c) better parameter uniformity across the wafer, and

(d) fewer fabrication steps than a MESFET.

For these reasons, one of our objectives is to evaluate this device as a load and a current source.

2-3 GaAs Schottky Diode

The Schottky diode has an ohmic contact to a highly doped layer and a rectifying Schottky contact with a lightly doped layer, Fig.(2-3.a). The I-V characteristic of a Schottky diode is shown in Fig.(2-3.b). The saturation current density is governed by the equation

$$J_s = A^{**}T^2 \exp(-q\phi_{bn}/kT) \tag{2-15}$$

and the forward biased current density is governed by

$$J_f = J_s[\exp(qV_f/nkT) - 1] \tag{2-16}$$

or

$$J_f = J_s[\exp(qV_f/nkT)] \tag{2-17}$$

for $qV_f >> 3nkT$.

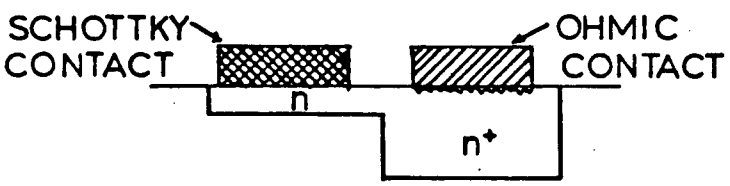
The saturation current density J_s can be obtained experimentally by extrapolating the current density from the log-linear region to intersect with the line V = 0. The ideality factor n can be obtained from the relation

$$n = (q/kT)(dV/d(\ln(J_f))) \tag{2-18}$$

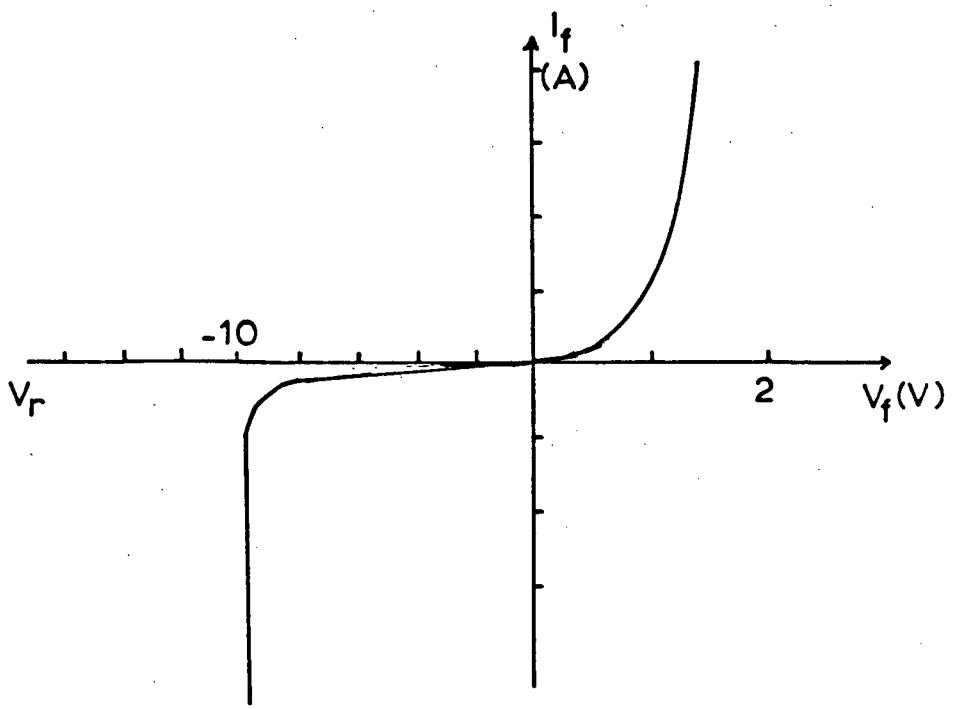
and the barrier height ϕ_{bn} from

$$\phi_{bn} = (kT/q)\ln(A^{**}T^2/J_s) \tag{2-19}$$

The barrier height values depend on the doping concentration, the semiconductor material, and the contact metal [2]. For a given metal and



(a)



(b)

Fig.(2-3) Schottky diode (a) structure and (b) I-V characteristics

semiconductor, the barrier height, the reverse bias breakdown voltage, and the forward switching ON voltage decrease with the increase of the doping concentration, Fig.(2-3.b). Optimum Schottky diodes have ideality factor n close to unity, saturation current density J_s value as small as possible, barrier height as high as possible, and reverse bias breakdown voltage as high as possible. Clean surface between the metal and the semiconductor can lead to better Schottky diodes assuming that suitable doping concentration is used.

2-1 Resistors

Resistors in monolithic I.C.s can be obtained by utilizing the bulk resistivity of a diffused or implanted area, an epitaxial layer, or a deposited thin film (usually nichrome NiCr). In this work resistors were made by implantation. Since the GaAs substrate is a semi-insulating material and can be converted to a conducting one by implantation, a very wide range of sheet resistances (from less than a hundred to several hundred thousand ohms per square) can be obtained by varying the implantation dose and energy. The ability to have this wide range of sheet resistance makes it possible to fabricate resistors with resistances ranging from a few ohms to several hundreds of kilo-ohms with practical dimensions.

The structure of a resistor, shown in Fig.(2-4), consists of a doped layer terminated with two ohmic contacts. The resistance of this resistor can be obtained from the relation

$$R = R_{SH} \cdot (L/W) \qquad (2\text{-}20)$$

where L is the resistor length, W is its width, and R_{SH} is the sheet resistance which is obtained from the relation

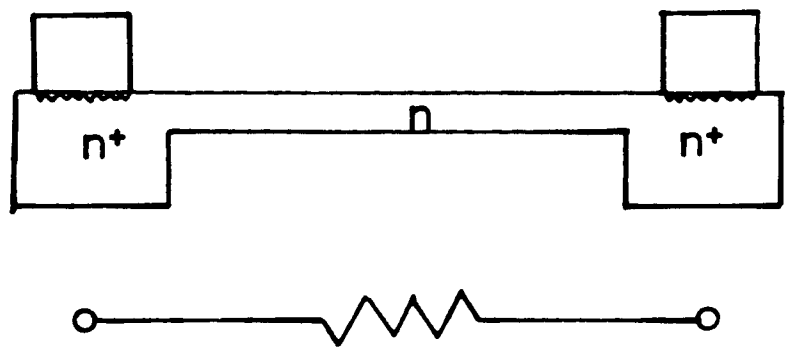


Fig.(2-4) Ion-implanted resistor.

$$R_{SH} = \rho/a \qquad (2\text{-}21)$$

and ρ is the specific resistance and a is the thickness of the resistor implanted layer. The resistance of the ohmic contacts should be estimated added to the value resulting from equation (2-20).

The width of the resistor should be long enough that the resistor-tolerance percentage due to line width variation, mask misalignment or photographic resolution becomes significant. The resistor length should not be too small, not only because of the resistor tolerance percentage but also to avoid current saturation as occurs in saturated resistors. The minimum length at which no saturation occurs can be obtained using the empirical relation

$$L_{min} = V_{max}/0.5\ \mu m \qquad (2\text{-}22)$$

where V_{max} is the maximum voltage drop across the resistor in volts. The 0.5 factor in equation (2-22) comes from the experimental observation that the current saturates at 0.5V/μm of the channel length.

2-5 Major Ion Implanted Fabrication Steps for GaAs MESFETs

The early GaAs MESFETs were depletion mode types; they were fabricated by the mesa fabrication technology to be used as low noise microwave FETs [3]. In this approach, isolation between devices was accomplished by etching a mesa through the epitaxial or the implanted layer. Two layers of metal were used to interconnect the various circuit elements with a dielectric layer to isolate the first and second layer of metal. Connections between these two layers were accomplished through holes in the dielectric.

At first, epitaxial techniques were used to form the active layer. Problems were found in achieving the uniformity and reproducibility required for I.C.s. Although the use of ion implantation (in the mesa technique) has solved the uniformity and reproducibility problems, it has been unable to optimize more than one device on the same chip [19]. Using both ion implantation and epitaxial techniques made it possible to optimize more than one device, however, it was hard to achieve an acceptable channel uniformity and yield especially for LSI applications [3].

The ion implantation of the dopant directly into a semi-insulating GaAs material or a buffer layer has shown very good results in terms of channel uniformity, reproducibility, and yield. The isolation between adjacent devices is directly achieved by the semi-insulating (undoped) areas between them. Better isolation can be achieved by implanting these areas (undoped areas) with boron [20].

Several fabrication techniques (other than the mesa) which utilize ion-implantation have been developed. Although each of them is devoted to control or optimization of one (or more) of the device parameters, such as threshold voltage or series resistance, they use in general nearly the same fabrication steps. These techniques will be discussed in the next section.

Only the ion-implanted GaAs MESFET fabrication technique will be considered, since it is the most developed and the one we used in our processes. The major steps of this process can be summarized as:

(a) substrate precleaning,

(b) implantation of the channel and ohmic contact areas,

(c) post-implantation annealing,

(d) ohmic contact metal deposition and alloying,

(e) gate metal (metals) deposition, and

(f) first and second level metallization.

(a) Substrate precleaning

The precleaning starts with degreasing the wafer using hot solvents such as acetone, 2-propanol, methanol, and trichlorethylene. These solvents are intended to dissolve away any grease or wax remaining after cutting, shipping, and handling. Then the wafer is etched to remove several hundreds to several thousands of angstroms to yield a damage free surface. A solution with a small concentration of bromine in methanol can be used for this purpose. The bromine serves the dual role of being a strong oxidizing agent, and also dissolving the oxidation product to form soluble bromides. A mixture of H_2O_2 and an acid or base can be used also for etching the GaAs surface. In this case, the oxide resulting from the reaction with H_2O_2 will be dissolved by the acid or the base used. Sulphuric, nitric, hydrochloric, and citric acids as well as ammonia and sodium hydroxide are used for this purpose [21]. Since the above etchants, as mentioned before, have an oxidizing nature, the wafer must be boiled in a concentrated acid such as HCl for about 2 minutes to remove any residues of oxide.

(b) Ion-Implantation

Conventionally, the introduction of desired impurity atoms into the lattice site in a semiconductor crystal (to form an n- or -p type material) is achieved either during the growth process (epitaxial layer) or by thermal diffusion. The thermal diffusion technology for n-type dopants has not been

developed for compound semiconductors such as GaAs or InP. Epitaxial techniques were the first to be used with GaAs, but they have had problems in achieving the uniformity and reproducibility required for I.C.s [3]. The other alternative process is to implant the dopant ions into the GaAs substrate.

Morgan et al. [22] have listed the advantages of implantation as:
(a) the doping level and the thickness of the implanted layer can be easily controlled,
(b) the doping is uniform and reproducible,
(c) it is more directional than the diffusion, and
(d) it has the ability to achieve doping profiles which cannot be easily obtained by other techniques.

Materials such as S, Se, and Si have been used successfully as n-type dopants in GaAs, while materials such as boron and zinc are used as p-type dopants. Our discussion here will be restricted to the n-type dopants because no p-material will be used in our process.

Fig.(2-5) shows the calculated and the measured electron concentration profiles for S, Se, and Si. From the figure one can see that activation of the implanted S atoms is only 20%, and the depth of the implanted layer is much greater than expected from the S range statistics. This broader thickness is due to the diffusion of the S during the post-implantation annealing.

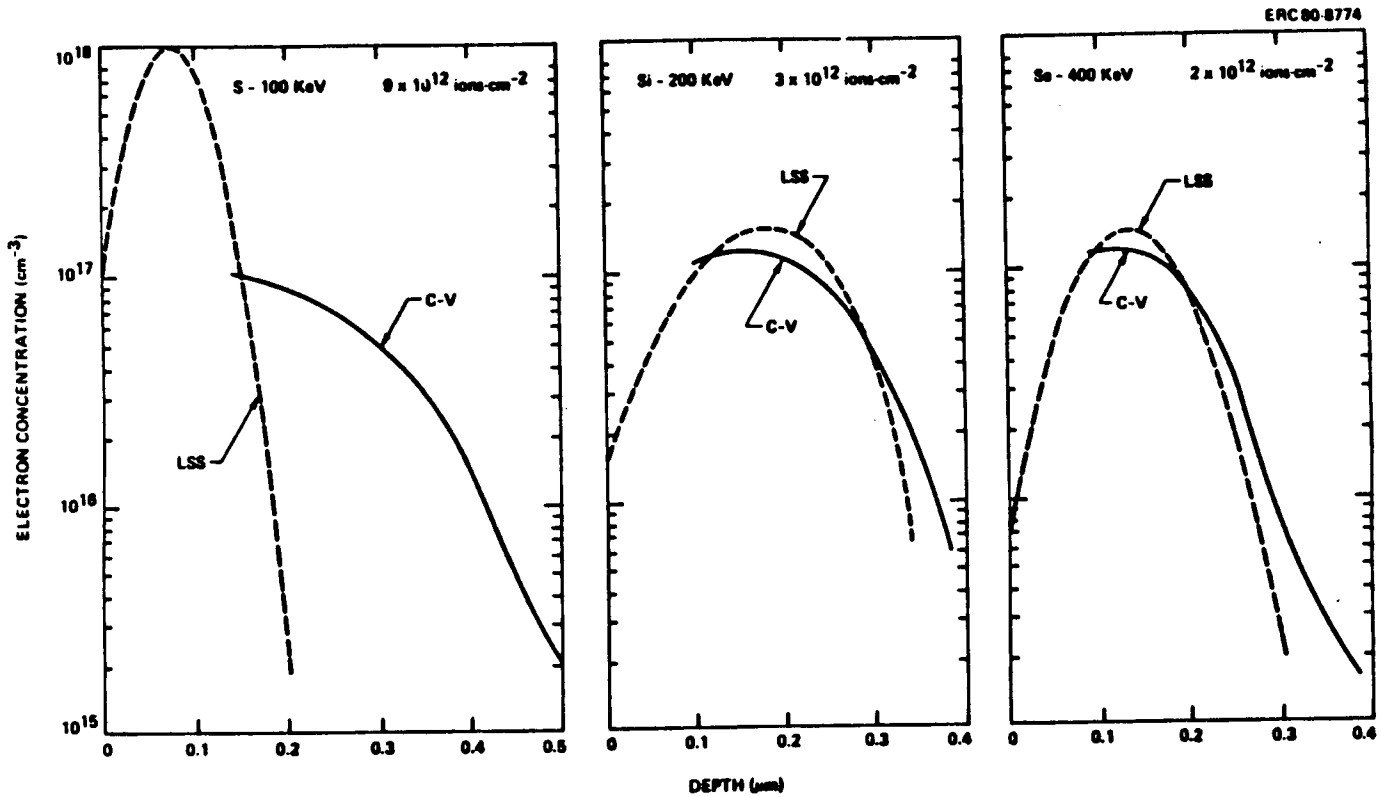


Fig.(2-5) Measured (from C-V measurements) and calculated electron concentration profiles for S, Si and Se implants [26].

Si and Se measured electron concentration profiles are quite similar to the calculated ones [26]. This indicates that Si and Se have higher activation efficiencies and lower diffusion constants.

S and Se need to be implanted at elevated temperatures to improve the activation efficiency while Si can achieve high activation while implanted at room temperature [23]. Si is considered the best candidate for GaAs implantation since it has low diffusion constant, high activation, and no elevated temperature is required during the implantation.

Following the implantation, the wafer must be annealed at 800 to 900°C to remove the crystalline defects induced by the implanted ions. However, at such high temperatures (>600°C), GaAs is subject to dissociation. Therefore, the wafer surface must be protected by an encapsulant, or annealed in a special ambient (normally As overpressure) to prevent dissociation and inhibit outdiffusion of the implanted impurities.

(c) Annealing

Many materials have been used as a cap for GaAs annealing. The most used materials are SiO_2, Si_3N_4, and AlN. SiO_2 was the earliest capping material employed. The most serious problem with SiO_2 is the outdiffusion of the Ga through it [24]. Si_3N_4 can alleviate this problem, as well as As outdiffusion and O_2 indiffusion, provided it has low O_2 content. Yokayama et al. [25] have observed lower trapping densities for samples capped with Si_3N_4. The electron concentration density profiles for samples capped with SiO_2, Si_3N_4, and AlN are shown in Fig.(2-6) [26]. The figure shows that the samples capped with AlN have severe carrier diffusion. These factors have resulted in general aceptance of Si_4N_4 as a suitable encapsulant material.

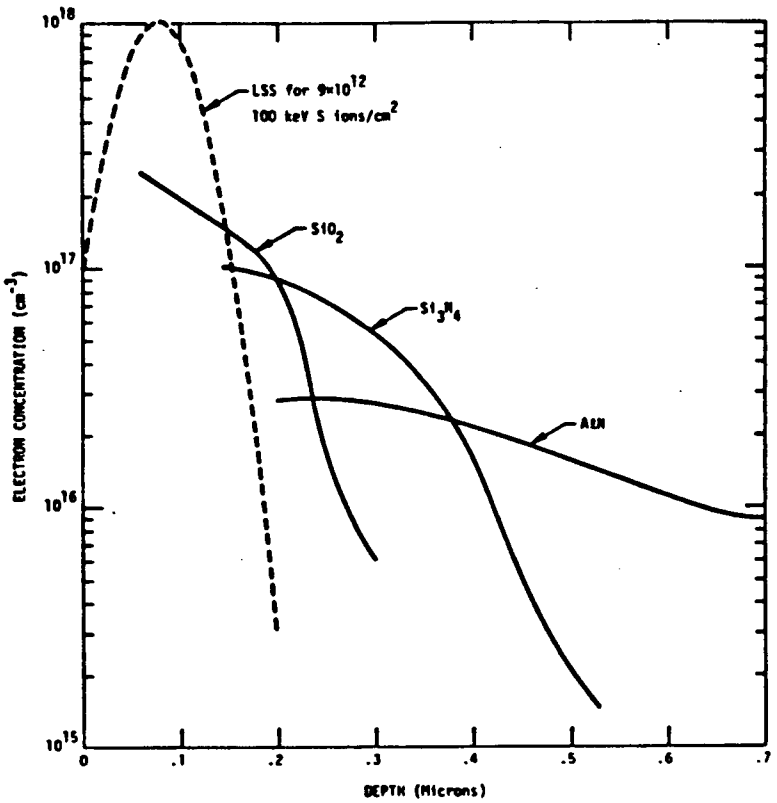


Fig.(2-6) Electron concentration profiles for SI GaAs samples implanted and annealed at 850°C for 30 minutes [24].

The thickness of the Si_3N_4 cap layer should not exceed 1000Å, otherwise the film will crack during annealing.

In addition to the encapsulation techniques, a number of capless annealing techniques have been developed. One of these techniques is the proximity cap annealing developed by Mandal et al. [27]. Mandal used a polished GaAs wafer in mechanical contact with the implanted wafer in the presence of a controlled As vapor pressure. Both the polished GaAs wafer and the As vapor prevent any outdiffusion of As atoms from the implanted wafer. The second technique is the capless annealing technique in which an As overpressure is used to prevent any As outdiffusion. The source of the As overpressure can be InAs [28] or crushed high-purity GaAs [29]. Due to the fact that both proximity cap annealing and capless annealing techniques use toxic gases and complicated systems, they are not attractive techniques without industrial infrastructure support.

The rapid thermal annealing technique can be a capless annealing technique. In our AG Associates system, no toxic gases are used. In this technique, the sample temperature is raised to around 950°C in about 3 seconds and kept at this temperature for about 5 seconds more and then cooled down before appreciable decomposition of the material takes place. The GaAs wafer is placed between two Si wafers in an N_2 atmosphere during annealing. Argon arc [30] or halogen lamps [31] can be used as a source of heat.

Some recent studies have employed laser or electron beam irradiation to anneal the lattice damage and activate implanted dopants in GaAs [32]. Although high electron concentrations have been achieved for high dose

implants, mobilities have remained poor, and for low implant doses, low levels of activation have been observed so far.

(d) Ohmic Contact Metallization

After activating the implanted areas, ohmic contact metals (AuGe or AuGe/Ni [25]) are deposited and alloyed at a temperature of about 450°C. Alloying causes some Ge atoms to diffuse into the GaAs material and form a very highly doped layer. The contact between this highly doped layer and the AuGe alloy is non-rectifying due to the low barrier height between them [2]. The alloying time and the temperature vary from one laboratory to another. The surface of the alloyed AuGe is rough, however Ni can be deposited on the top before alloying to improve the surface morphology. Measurements of the ohmic contact using the Transmission Line Model (TLM) theory [52] are discussed in chapter (4).

(e) Schottky Contacts

The Schottky contact required for the gate is formed by depositing the gate metal on the GaAs surface. Although most metals form a Schottky contact with GaAs, not all of them form an acceptable one. The requirements for an acceptable contact are

(a) sufficiently large barrier height,

(b) ageing and temperature degradation resistance, and

(c) good adhesion between the metal and the semiconductor.

Al was the first metal to be used for this purpose. It is very simple to deposit and has low specific resistivity. Ti/Pt/Au are the preferred Schottky metals especially for commercial production. In this system, Ti provides good Schottky contact while Au provides high electrical

conductivity. Pt provides a good diffusion barrier between the Ti and the Au.

(f) First and Second Level of Metallization

To connect devices with each other, two levels of metallization are required to enable crossovers. Implanted layers are preferably not used as interconnects due to their high resistivity. Very high doses (of about 10^{15} cm^2) and energies (about 1000keV) give sheet resistances of about 80 ohms per square [89] compared to 0.025 ohm per square for a 1 μm sheet of Al.

The two levels of metallization must be electrically isolated except when a contact between them is required. The isolation material is normally a dielectric such as SiO_2, Si_3N_4, or polyimide. SiO_2 and Si_3N_4 are the most used materials for this purpose, however Aditya et al. [33] do not recommend using Si_3N_4 because it may cause the degradation of the ohmic contacts and the channel. They attributed this to the collision of the plasma molecules with the surface of the wafer. They recommend the use of the polyimide for high quality transistors.

In general, polyimide has these advantages over both SiO_2 and Si_3N_4:
(a) it is laid down by spinning,
(b) holes in the polyimide can be opened using the developer of a positive photoresist such as MF312 Shipley developer, therefore the development of the photoresist and the etching of these holes can be done in one step,
(c) it has lower dielectric constant leading to lower stray capacitance, and
(d) it is resistant to nearly all chemical etchants.

Metals with low resistivity should be used for both levels of metallization. Electrical contacts between the two levels are achieved through holes etched in the isolating dielectric.

2-6 GaAs I.C.s Technologies

Four techniques will be considered in this section: the planar ion-implanted, the recessed gate, the Pt gate, and the self-aligned gate techniques.

(a) The Planar Ion-implanted Technique

The first approach is the planar ion-implanted process developed by Rockwell in 1979 [34]. Using this approach, more than one device can be optimized at the same time by choosing the right doses and energy for the n and n+ implantation as shown in Fig.(2-7). The value of the device parameters depend not only on the implantation parameter, but also on the material quality. In order to achieve the required parameter uniformity and reproducibility using this technique, "qualified" wafers must be used which satisfy the following conditions [6]:

(a) high purity substrate with less than 5×10^{15} cm^{-3} donor and acceptor impurities,

(b) freedom from harmful crystalline defects,

(c) high resistivity ($> 10^7$ ohm-cm),

(d) thermal stability at the annealing temperature, and

(e) high percentage activation of implanted ions.

The fabrication process starts with the wafer cleaning using hot solvents and etchants for damaged layer removal. Ion implantation is carried

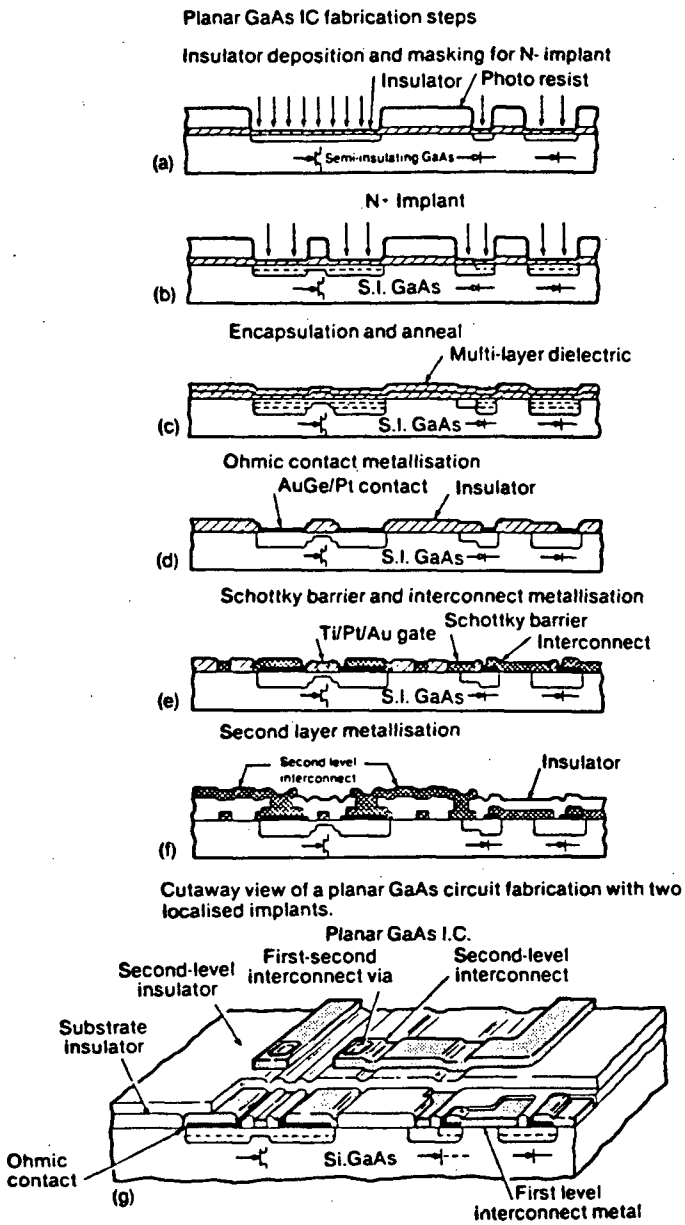


Fig.(2-7) Ion-implanted planar process [34].

out through a Si_3N_4 layer which will be used as a cap for annealing after the implantation. Ohmic contact metals are deposited through openings in the Si_3N_4 layer and then alloyed at about 450°C for 2 minutes. Schottky contact metals are deposited to form the gate where Ti/Pt/Au metals are used for this purpose. The same metals are used for the first and second level of metallization. Si_3N_4 is used as an intermediate dielectric between the two levels of metallization. However, for high quality devices, polyimide is used as a dielectric.

(b) Recessed Gate Technique

At Plessey, another technique has been adopted in order to control the pinch-off voltage (Fig.(2-8)) [6]. Monitor FETs were used to check the saturation current before laying down the gate metals. If the saturation current value is not acceptable, the channel is etched to obtain the required current value which results, in turn, in the required pinch-off voltage. This technique ensures that the pinch-off voltage lies within a certain range, but a tight control may not be easy to achieve.

The fabrication steps can be summarized as: precleaning the substrate, n implantation, n^+ implantation, ohmic contact metal deposition and alloying, gate mask patterning and source drain current measuring, channel etching for getting the required saturation current, gate metals deposition, first level of metallization, intermediate dielectric deposition, and second level of metallization.

(c) Pt Gate Technique

The third alternative to control the pinch-off voltage is the use of Pt

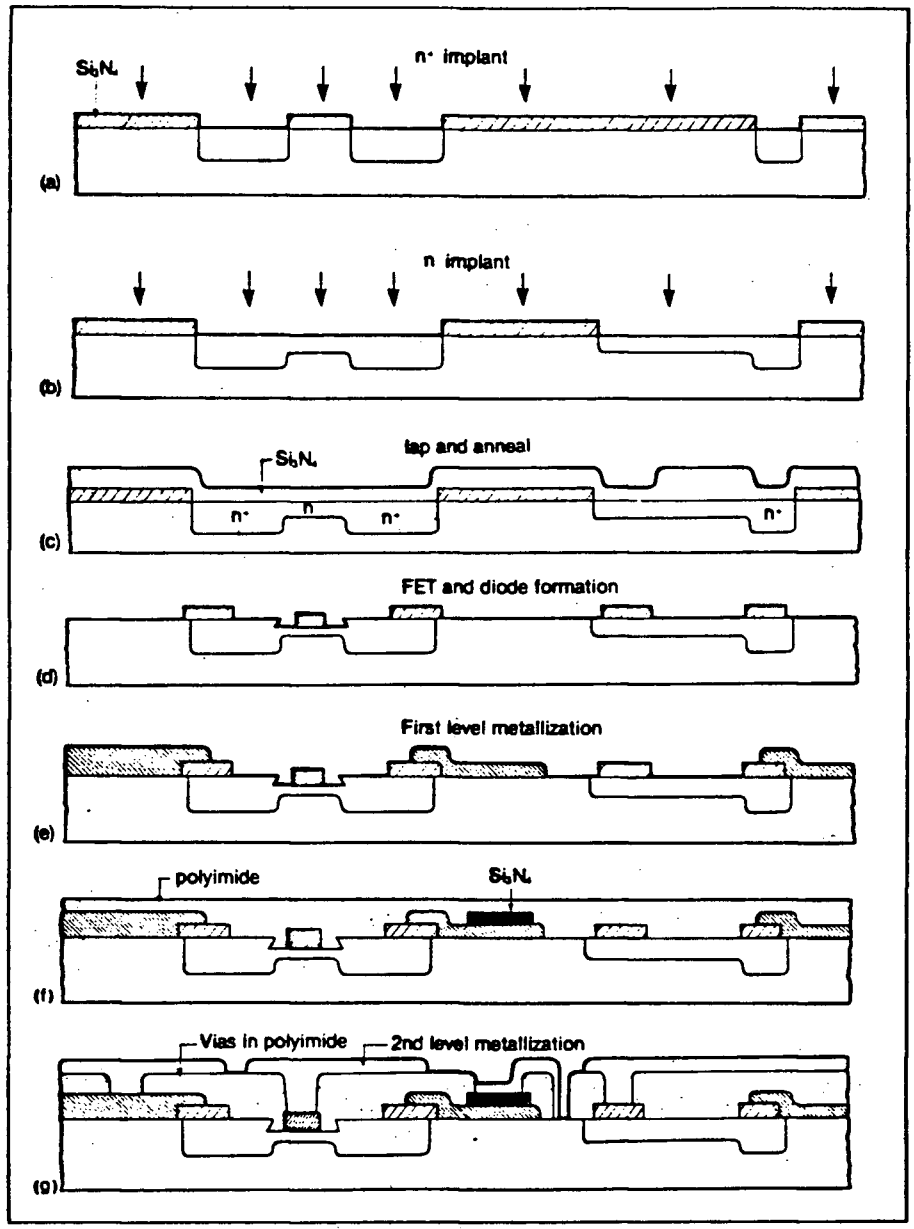


Fig.(2-8) Plessey fabrication process [6].

gates. Pt reacts with GaAs at temperatures of 300-500°C and forms several compounds including PtGa, Pt_3Ga, and Pt_2As [35-36]. Ga atoms diffuse through the intermetallic layer and the compound $PtAs_2$ forms adjacent to the GaAs. As the reaction progresses, the Schottky contact characteristic changes from Pt-GaAs to $PtAs_2$-GaAs and the GaAs surface moves down leading to a reduction in the channel thickness and consequently a reduction in the pinch-off voltage. The rate by which the pinch-off voltage decreases depends on the sintering temperature and time. The fabrication procedure for this technique is similar to that of the ion-implanted planar technique except the gate metal should be Pt and should be sintered for a specific period of time for threshold voltage control. Using this method, Toyada et al. [37] were able to control precisely the pinch-off voltage within 0.1 volt for more than 10 wafers.

(d) Self-Aligned Gate Techniques

One of the MESFET fabrication problems is to lay down the gate metal accurately between the source and the drain regions and, at the least, to avoid hitting the source or the drain. This requires that enough space should be left between the source and the drain. However, more space solves the problem of the gate alignment, but introduces the problem of having higher source and drain resistances.

Large distances between the source and the drain can be tolerated for transistors with threshold voltages of large negative values because of their low channel resistance (which is not the case for enhancement mode devices or depletion mode devices with low negative threshold voltage values.

Therefore, some sort of self-aligning process must be used to align the gate automatically between the source and the drain region.

The first GaAs self aligned gate technique was developed by Cathelin et al. [6]. Then two more advanced techniques were developed; the first was the "self aligned implantation for n+ layer" (SAINT) and the second was the self aligned gate using refractory metals or silicides.

(i) Self-Aligned Implantation for n+ Layer Technique (SAINT)

The SAINT process, developed by Yamasaki [38], starts by forming the channel layer then depositing 1500Å of Si_3N_4 on the top of the wafer (see Fig.(2-9)). On the top of the Si_3N_4 layer a multilayer scheme is formed. This scheme consists of 0.8 μm of polytetra-fluoropropyl methacrylate (PFM) resist, 0.3 μm of SiO_2, and 1350J photoresist on the top. The top resist is patterned and the SiO_2 is etched by a reactive ion beam etching using CF_4+H_2. The bottom resist is then etched using a reactive ion etching in O_2 discharge. The top photoresist on the top of the SiO_2 layer is also etched during the etch of the bottom one. This process resulted in an undercut structure because of the resistance of SiO_2 to the O_2 plasma. The amount of the undercut is a function of the etching time of the resist. The n+ implantation is then carried out using high dose and energy; the area under the undercut will not be implanted by the n+ implantation where it is protected by the SiO_2 layer. Next, a second layer of SiO_2 is deposited. The SiO_2 adhering to the side wall of the multilayer is removed by immersing in buffered HF for a few seconds while the SiO_2 layer on the top of the resist is removed by lifting it off in acetone. At this point, the wafer is covered with SiO_2 except for the areas which were covered by the multilayer

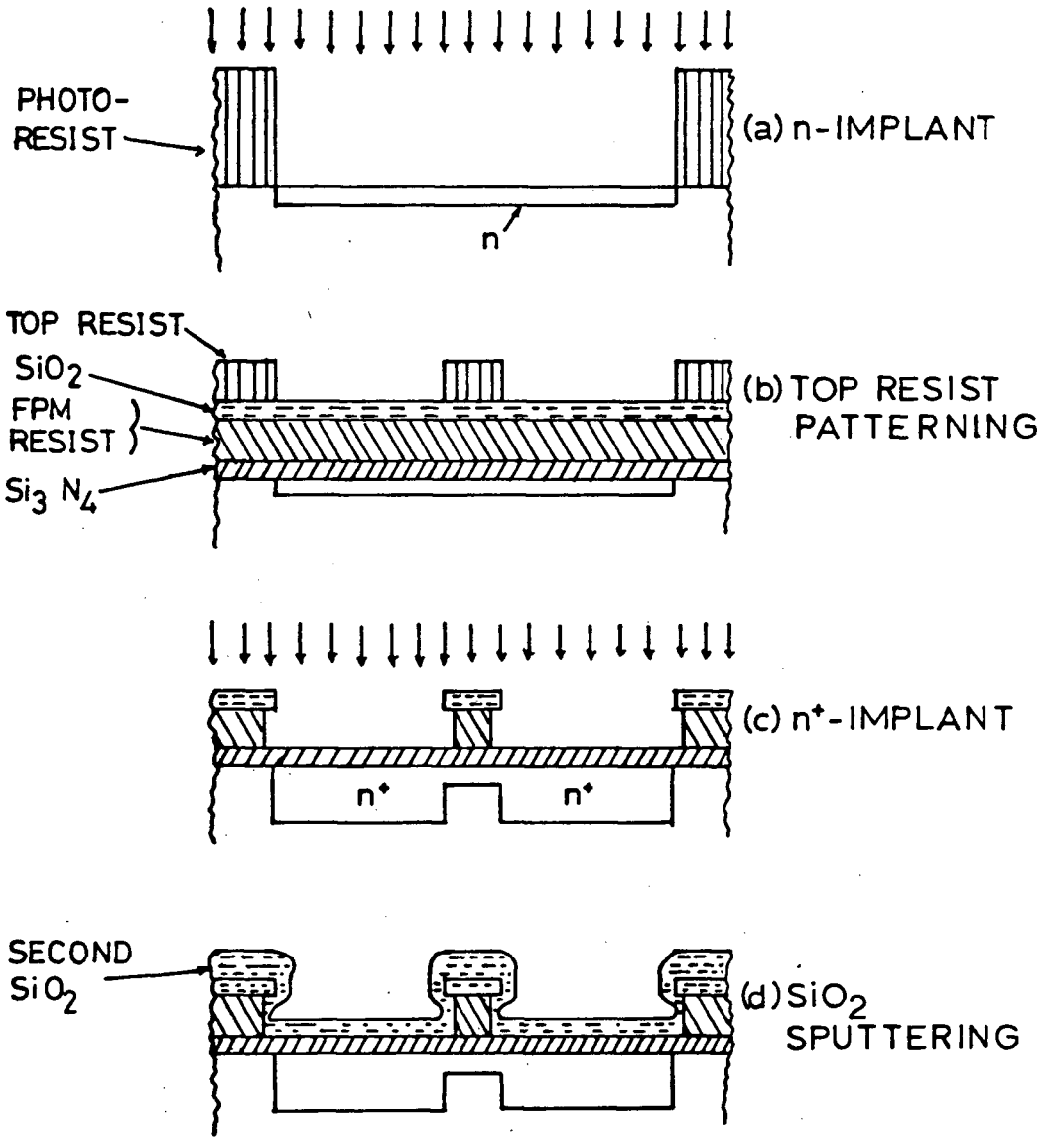


Fig.(2-9) SAINT process.

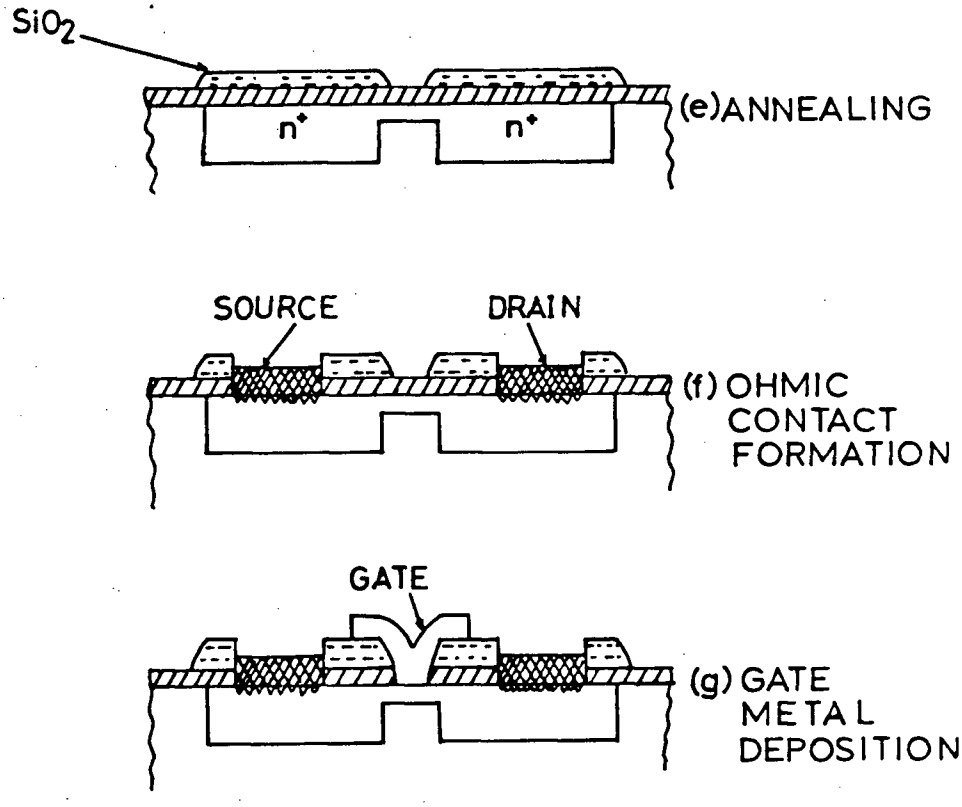

SiO2
n+
n+
(e)ANNEALING
SOURCE
DRAIN
(f) OHMIC
CONTACT
FORMATION
GATE
(g) GATE
METAL
DEPOSITION

Fig.(2-9) Cont.

structure, or in other words, except for the gate areas. After annealing and alloying the ohmic contact metals, the wafer is etched in CF_4 plasma to etch the Si_3N_4 over the gate areas. The SiO_2 layer protects the other areas because the etching rate of it is 1/5 that of the Si_3N_4 [38]. Gate metal is then deposited. The metal will be in contact with the GaAs surface at the area predetermined by the multilayer structure which is automatically aligned between the n+ areas.

Electron beam lithography was used in the SAINT process by Kato et al. [39] to fabricate short channel devices. In this approach a four layer multiresist of negative photoresist CMS, molybdenum, SiO_2, and positive photoresist AZ 1470 were used. Using this approach it was possible to fabricate a ring oscillator with 0.3μm gate length which resulted in a 16.7 ps delay per gate.

(ii) Refractory Metals Self-Aligned Gate Techniques

The other self-aligned gate technique developed by Abe et al. [40] and others utilizes refractory metals or silicides. The idea is to perform the n+ implantation with the gate metal acting as a mask to protect the channel from the high dose implantation. The sample is then annealed with the gate in place. The gate metal must be able to withstand the annealing temperature without degradation in barrier height or ideality factor of the contact.

The fabrication steps of this technique can, using TiW or refractory metal, be summarized as

(a) wafer precleaning,

(b) n-implantation,

(c) deposition of TiW gates (TiW alloy is 10:90wt.% Ti:W),

(d) n+ implantation,

(e) SiO_2 or Si_3N_4 deposition and annealing, and

(f) ohmic contact deposition and alloying.

In this approach, there is direct contact between the gate metal and the n+ areas, therefore the n+ implantation energy should be high enough to bury the implantation carrier concentration peak far from the surface. Abe et al. [40] have shown that for an implantation dose of 1.7×10^{13} ions/cm^2 and energy of 175 KeV the gate drain breakdown voltage was about 6 volts.

Another approach for solving the low drain-gate breakdown voltage is the use of the T-gate structure developed by Levy et al. [41], Sadler et al. [42] and others. The idea of this structure is to have a dummy gate over the TiW which will give a T-structure when the TiW is etched in CF4 plasma. The dummy gate metal should be resistant to the CF4 plasma etching. The candidate metals are Al or Ni.

Fig.(2-10) shows the fabrication steps of this approach as described by Sadler which are:

(a) wafer precleaning,

(b) channel implant,

(c) TiW deposition (by sputtering),

(d) dummy gate metal deposition (by optical lithography),

(e) etching the unmasked TiW using CF_4 or CF_4O_2 plasma etching (this leads to the undercut as shown in Fig.(2-10.e)),

(f) n+ implant,

(g) capping and annealing,

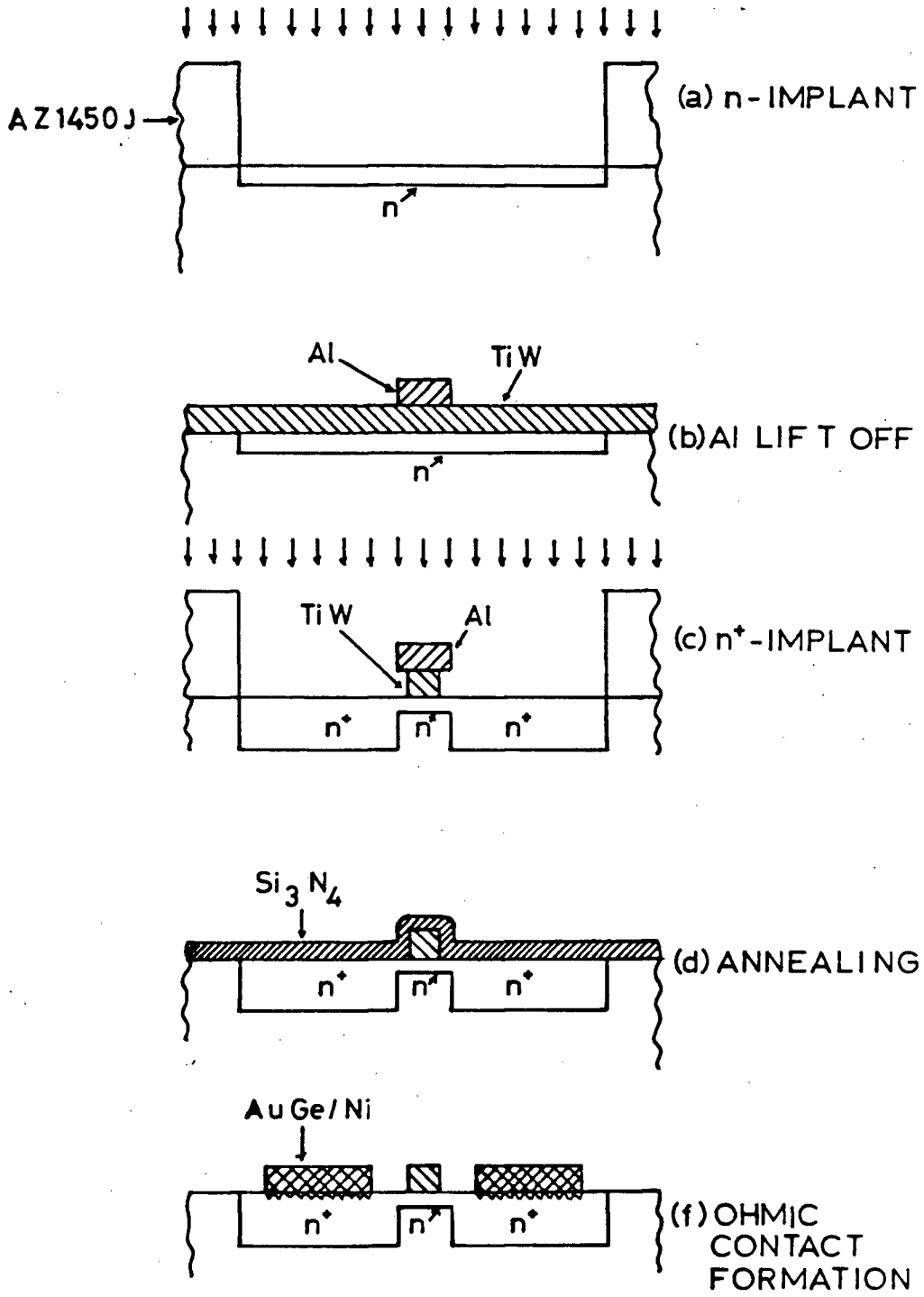


Fig.(2-10) TiW self aligned gate process.

(h) ohmic contact metal deposition and alloying,

(i) B^{11} implantation for the isolation between devices,

(j) crossover dielectric deposition, and

(k) second level metal deposition.

Levy et al. [41] has reported a transit time delay of 25 ps and a power time delay product of 18 fJ for a transistor fabricated using this technique.

Sadler et al. [42] have shown that TiW alloy exhibited unstable Schottky diode characteristics with short annealing cycles at temperatures higher than 750°C, due to metallurgical reaction between the Ti, W, and GaAs. For this reason, Yokayama et al. [43] used TiW silicide instead. They claimed that no reaction was noticed between the TiW silicide and GaAs after 1 hour of annealing at 850°C, however they showed some irregularity in barrier height and ideality factor [44]. Tungsten silicides [44] or tantalum silicide [45] can be used also as a gate metal. In any case, it is desirable that the gate alloy or silicide should have a thermal expansion coefficient value close to that of the GaAs, stable diode characteristics after annealing, and low resistance in order to be used in this self-aligned gate technique.

CHAPTER(3)

DEVICE AND CIRCUIT FABRICATION

The fabrication processes used in our work will be presented in this chapter. These processes include the ion-implanted planar technique, the recessed gate technique, and a new self-aligned gate technique using polyimide, developed in our laboratory.

3-1 The Chip Layout

The software layout pattern was generated using the UBC CIF program. This pattern was cut on a 30×40 inch rubylith using the cutter program in the PDP8E computer. The rubylith was sent to Precision Photomask Co. for photoreduction, step, and repeat. Masks for registration marks, channel implant, n^+ implant, ohmic contact metallization, gate metallization, first level of metallization, via holes between first and second levels of metallization, and second level of metallization were designed. The first four masks, shown in Fig.(3-1.a), were put on one photographic plate and the second four, shown in Fig. (3-1.b), on another.

The chip consists of five major sections (as shown in Fig.(3-2)). The first section consists of 7 subsections which contain: a 2μm gate length MESFET, a 4μm MESFET, a diode, 3 pads for measuring the sheet resistance of th n+ implant, 3 pads for measuring the sheet resistance of the n and n+ implant, and a fat FET for mesuring the drift mobility and the carrier concentration profiles of the channel. These subsections are labelled A1, A2, A3, A4, A5, A6, and A7 respectively. The second section (B) is a 3 bit

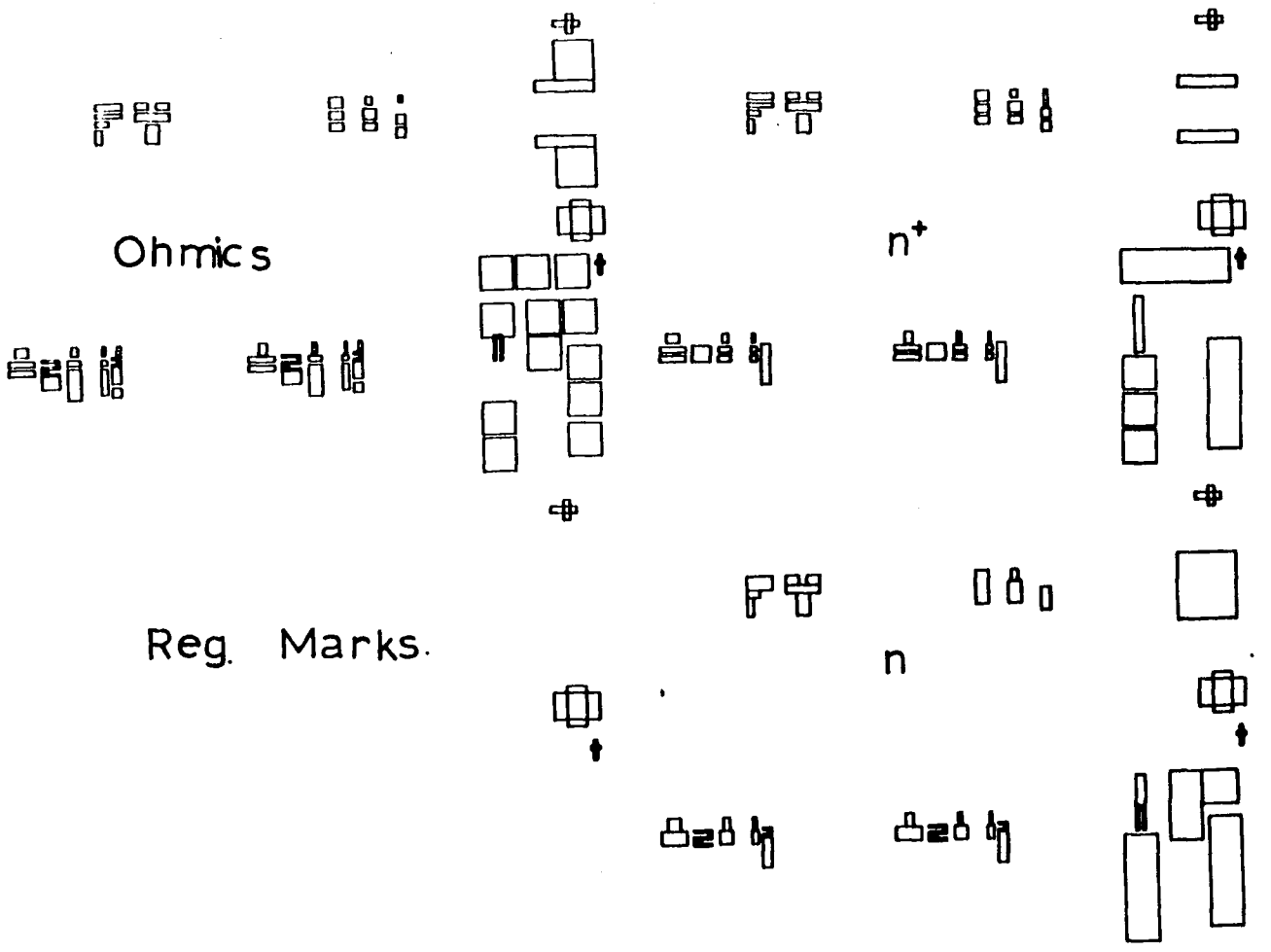


Fig.(3-1) Chip masks layout (a) registration marks, n, n^+, and ohmic contact metallization; (b) gate, first level metallization, via holes, and second level metallization.

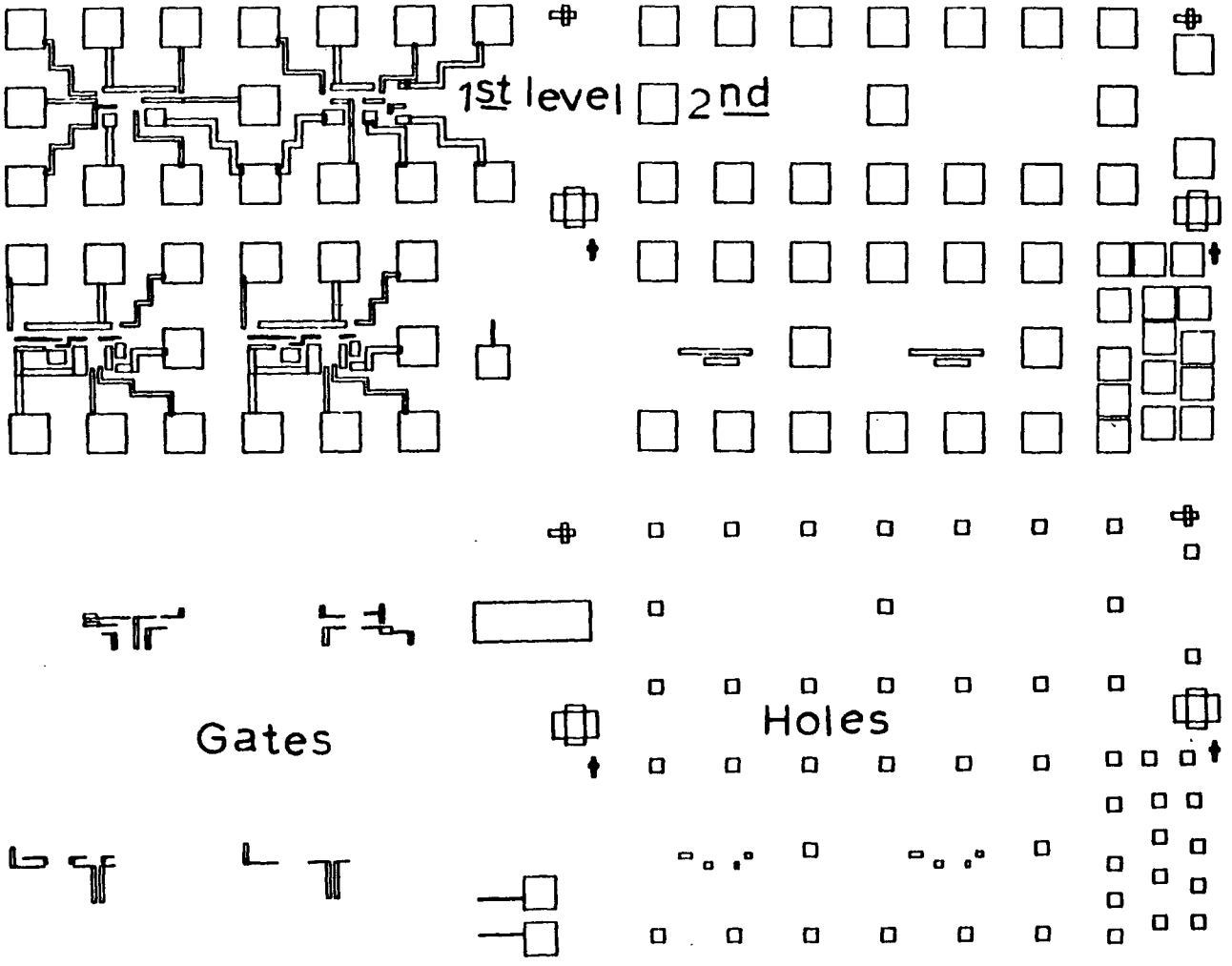


Fig.(3-1) (b)

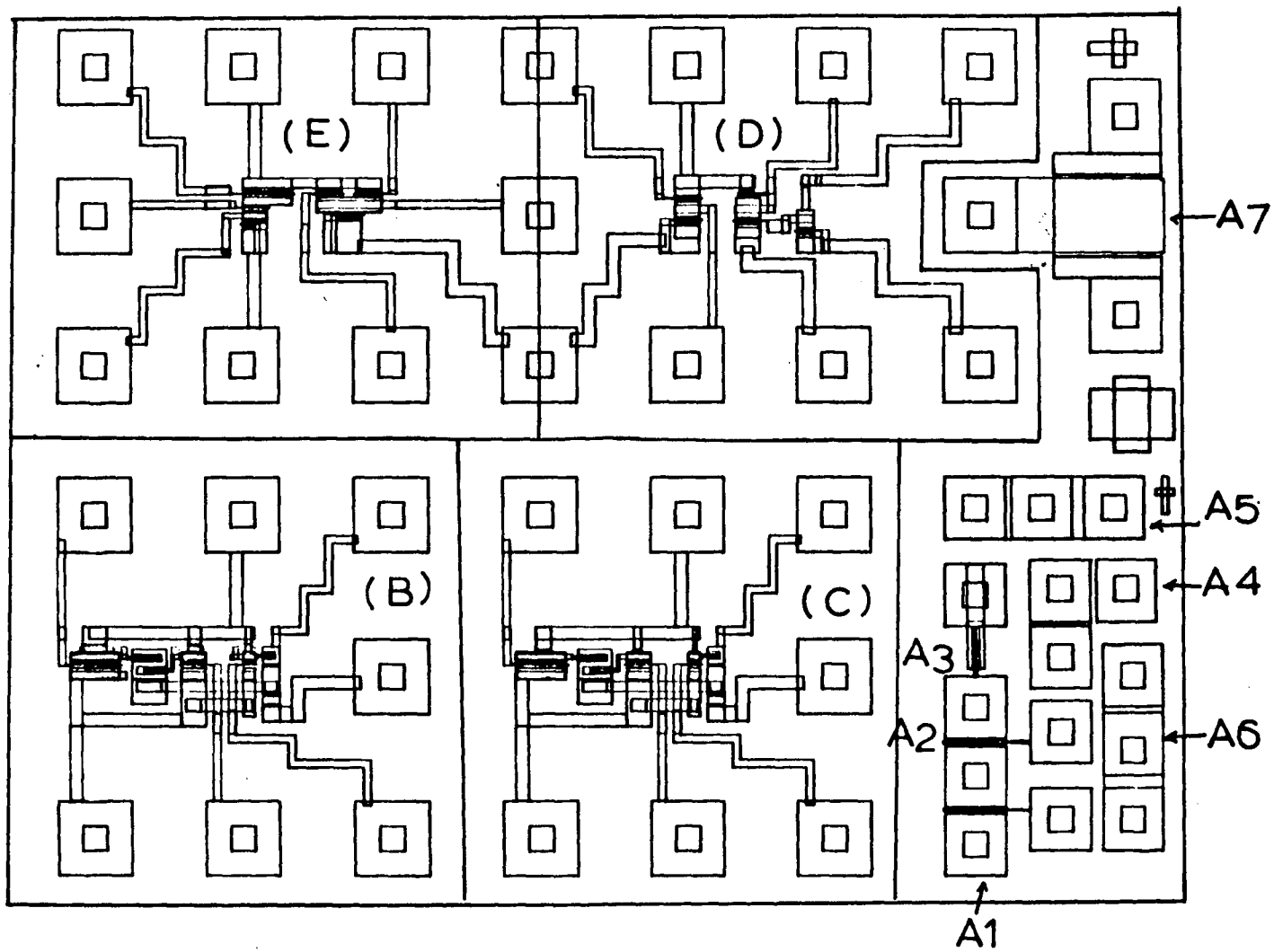


Fig.(3-2) Chip layout.

DAC with 4μm MESFETs used as current sources while the third (C) section is a 3 bit DAC but with saturated resistors as current sources instead. The fourth section (D) contains an inverter (on the right) and a buffer circuit (on the left) for the CDFL. The fifth section (E) contains an OR gate (on the right) and an AND gate (on the left) for the same logic.

3-2 Fabrication Processes

Three different techniques were used. These were the ion-implanted planar technique, the recessed gate technique, and the self aligned gate technique using polyimide. The ion-implanted planar technique was used at the beginning to fabricate devices with threshold voltages around -1.0 V and to realize the ability to control the pinch-off voltage using ion implantation. However, unacceptable series resistances were observed when |Vth| was reduced to less than 0.5 V. These high resistances can be attributed to the use of thin and lightly doped channels (which have led in turn to the increase of the sheet resistance) and the depletion of most of the unmodulated channel due to the surface states.

The recessed gate technique was then attempted in order to alleviate this problem; however, uniformity of the device parameters was not acceptable. The TiW self-aligned gate was then tried, but possible reaction between the TiW and the GaAs resulted in an unacceptable yield (see Chapter(2)). The SAINT process has not been tried due to the process complexity and the requirement of a sophisticated multilayer resist. Instead, a new self aligned gate

technique using polyimide was developed. In this technique, no refractory metals or multilayer resists were used. Therefore, nearly 100% production yield was obtained for 3 samples.

(a) The Ion-implanted Planar Technique

The ion-implanted planar technique developed by Rockwell [3] was the first to be used. The fabrication steps are shown schematically in Fig.(3-3). The starting material was Cominco semi-insulating LEC GaAs wafer. This was first degreased using acetone, 2-propanol, and trichloroethylene to dissolve any wax or grease remaining after shipping and handling. The wafer was then etched in [21]

$$4H_2SO_4 : 1H_2O_2 : 1H_2O$$

by volume to remove the damaged layer (as discussed in Chapter(2)). This step is critical because it could result in a very rough surface, therefore the temperature and the solution concentration must be controlled. Another etching procedure can be used [93] where the wafer was immersed in filtered 1% Alconox for about 3 minutes and then etched in

$$5NH_4OH : 2H_2O_2 : 240H_2O$$

by volume for 30 seconds (see Appendix(C-1)). The above solution resulted in the dissolution of about 50nm of GaAs.

Photoresist was used to pattern the registration marks, then the wafer was dipped into 10% HCl for 1 minute to dissolve the natural oxide. The registration marks were then etched into the GaAs using

$$5\%\ H_3PO_4 : 2.5\%\ H_2O_2 : 92.5\%\ H_2O$$

by volume for 70 seconds to dissolve about 80 nm of GaAs.

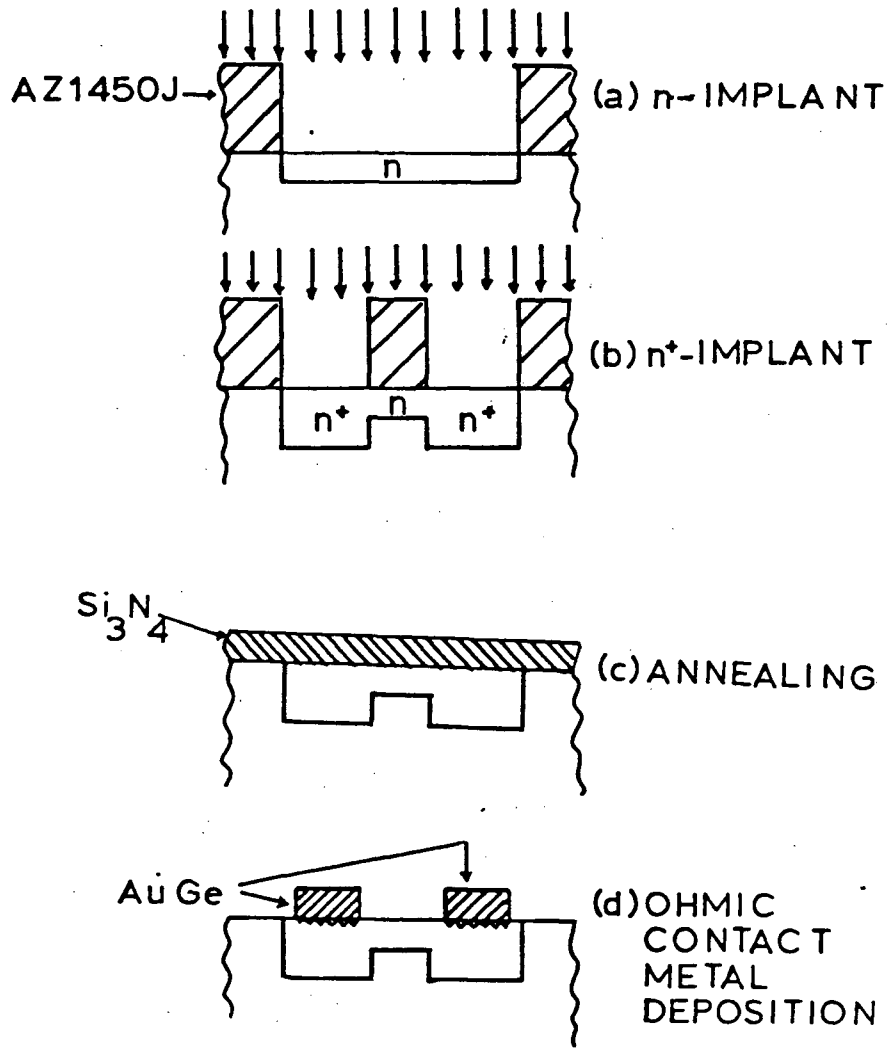


Fig.(3-3) Ion-implanted planar fabrication process adapted at UBC.

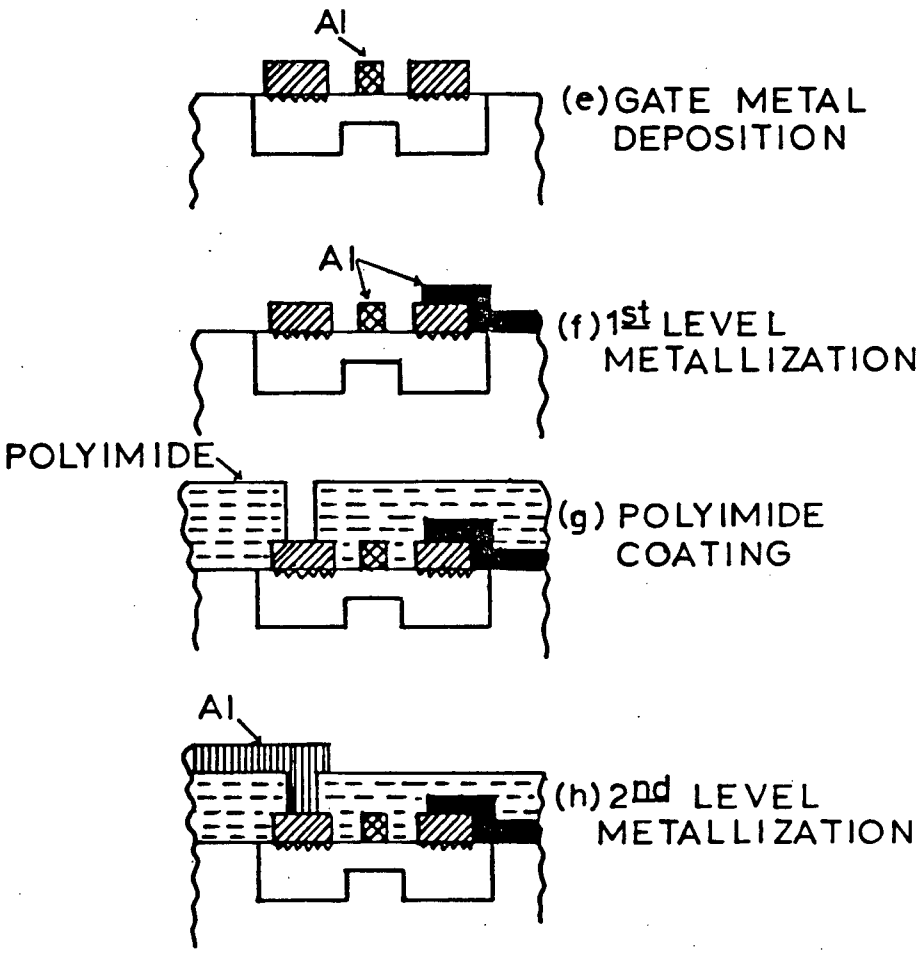

Al
(e) GATE METAL DEPOSITION
Al
(f) 1st LEVEL METALLIZATION
POLYIMIDE
(g) POLYIMIDE COATING
Al
(h) 2nd LEVEL METALLIZATION

Fig.(3-3) Cont.

The channel and the n+ layer were formed by implanting Si^{28} or Si^{29} (Figs.(3-3.2) and (3-3.b). The doses and energies used are tabulated in Table (3-1). Photoresist was used as an implantation mask for both implants. Acetone was used to remove the photoresist after the channel implantation and hot negative microstrip resist (Philip A Hunt Chemical Corp.) or O_2 plasma (see Appendix(C-2)) were used to remove the residues of the photoresist. These residues were hard to remove after the n^+ implantation, especially if high doses and energies were used.

Annealing was the major problem in the past where full or partial cap lift-off after annealing were taking place, Fig.(3-4). The reason for the cap lift-off was the existence of some O_2 atoms inside the dielectric or on the GaAs surface. An experiment has been performed to solve this problem which includes the study of the effect of the treatment with O_2 plasma, ammonia plasma N_2 plasma, immersing in buffered HF immediately before loading, purging the chamber immediately after loading, and flushing the chamber with Ar before applying the gases (see Table(3-2)). This experiment has shown that, for successful annealing, the following steps are needed when depositing the Si_3N_4 layer:

(a) natural oxide must be etched,

(b) the chamber must be purged to remove any dust entered during the loading of the samples,

(c) the system must be flushed with Ar before admitting the gases,

(d) no O_2 treatment should be performed in situ before depositing the film, and

TABLE(3-1)

Implanted doses and energies and the resultant threshold voltages

Wafer #	Sample #	n		n^+		V_{th}
		Dose $10^{12}/cm^2$	Energy keV	Dose $10^{12}/cm^2$	Energy keV	(V)
344S8	1	2.24	125	4.8	125	-1
	2	2.24	100	4.8	100	-2.5
	3	1.6	100	4	100	-1.8
	4	1.45	100	3.37	100	-1.35
	A4	1.6	75	4	100	-0.65
175S52	A5	1.6	80	4	100	-1.2
	B5	1.3	75	1.9	100	-0.6
	C5	1.6	70	1.6	100	-1.0
	D5	1.3	70	1.6	100	-0.5
	E5	1.6	60	1.6	100	-0.6
175S53	F6	1.5	60	1.6	100	-0.6
175S54	C7	3.25	120	-	-	-0.6
	D7	3.25	120	-	-	-0.6
	E7	3.25	120	4.8	180	-2.5

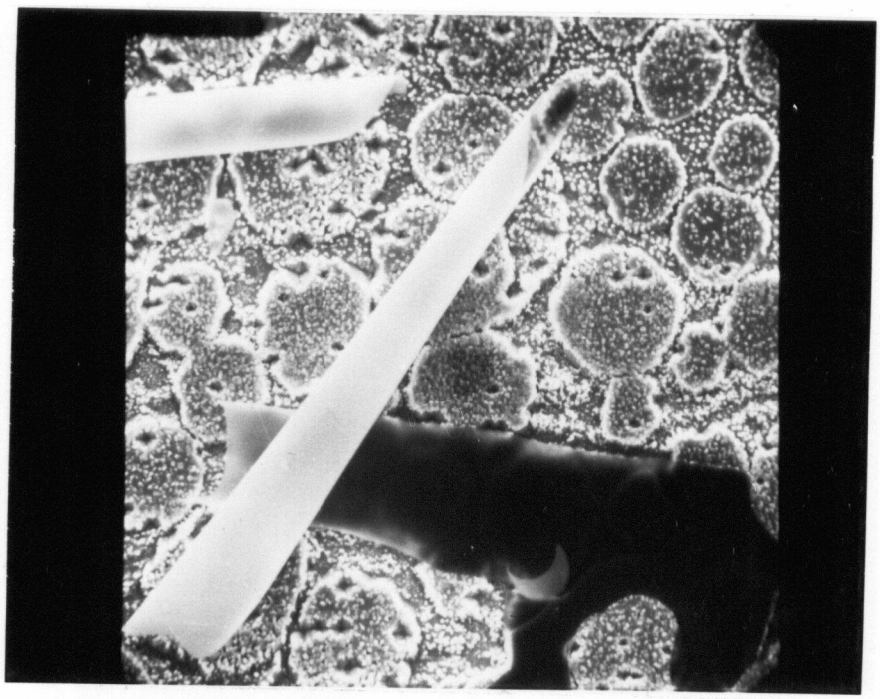


Fig.(3-4) Photograph of Si_3N_4 lift-off after annealing.

TABLE(3-2)

Effect of different treatments prior to the deposition of Si_3N_4

sample #	O_2 plasma treatment before Si_3N_4 deposition	Oxide removal prior to the loading using HCl	Ammonia plasma pre-treatment	N_2 plasma treatment	System flushing before deposition	Si_3N_4 lift-off
A1	yes	-	-	-	yes	yes
B1	yes	-	-	-	-	yes
C1	-	-	-	-	yes	partial
D1	-	-	-	-	-	partial
G1	yes	yes	-	-	yes	partial
H1	-	yes	yes	-	yes	no
H2	-	yes	-	yes	yes	no

(d) ammonia or nitrogen plasma must be applied to remove, in situ, any residues of oxide.

Successful annealing was obtained after applying these steps. It was found that the thickness of the Si_3N_4 film should not exceed 80 nm otherwise the film will crack. Annealing was performed in N_2 atmosphere at 830°C for 25 minutes. The wafer was then cooled down and the Si3N4 was stripped using concentrated HF.

The next step was to lay down the ohmic contact metal. The alloy used in our experiment was AuGe with 12% Ge by weight. The single lift-off technique developed by IBM [46] was used. As shown in Fig.(3-5), AZ 1450J photoresist was spun over the wafer at 4500 rpm, soft-baked at 70°C for 30 minutes, and then exposed using the appropriate mask for 1.5 minutes. The photoresist was then soaked in chlorobenzene for about 3 minutes. Chlorobenzene caused the top photoresist layer to be hardened against the developer which resulted in an undercut when developed, as shown in Fig.(3-5.e). This undercut made it easy to remove the unwanted evaporated metal when the wafer was immersed in hot acetone or another photoresist stripper.

To ensure good ohmic contact the wafer was dipped into buffered HF or 10% NH_4OH in de-ionized water for about 30 seconds to remove any oxide which might have grown during previous steps. Immediately after that, the wafer was loaded into the evaporator (VEECO) and the metal was evaporated. The AuGe was then lifted off using hot acetone and agitated in an ultrasonic agitator. The result of the lift-off step is shown in Fig.(3-5.g). The

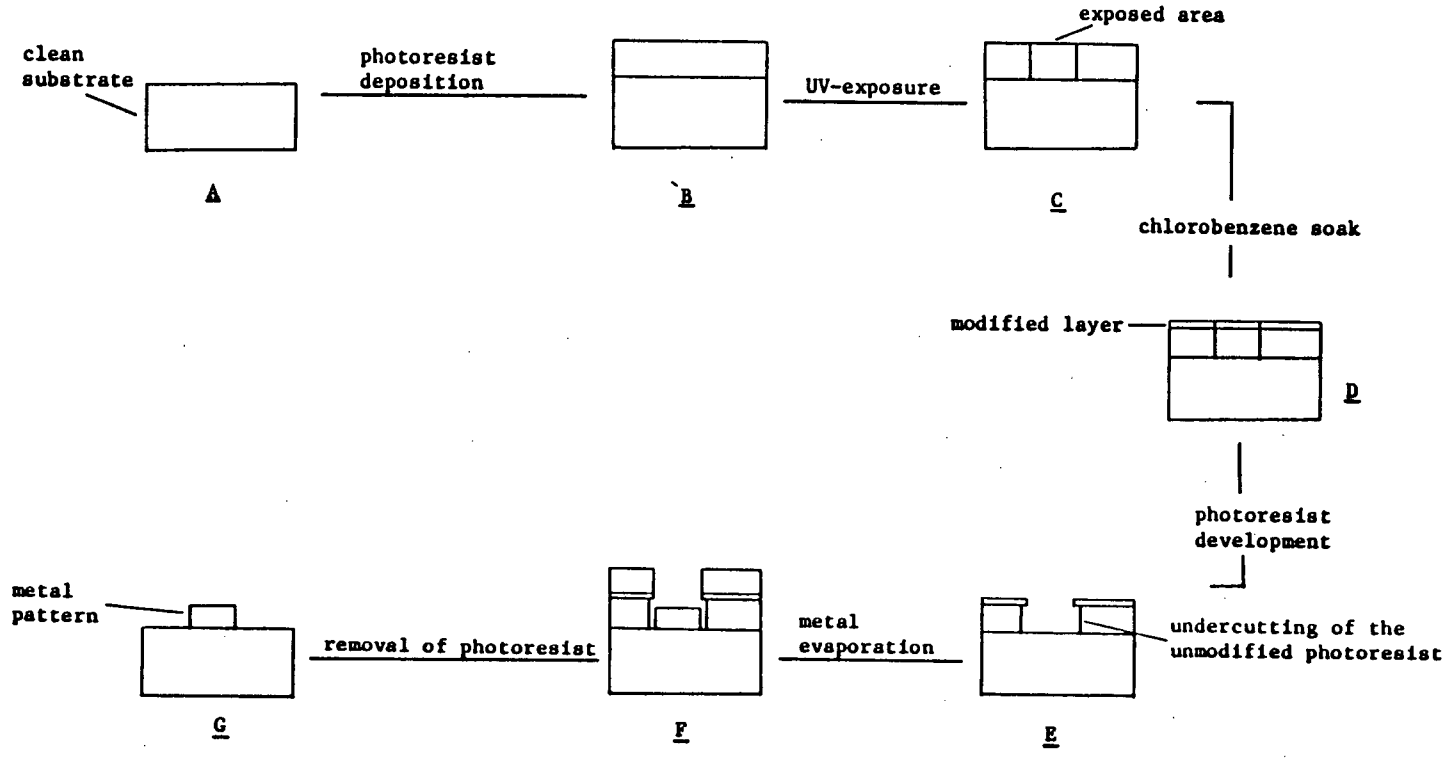


Fig.(3-5) Single lift-off procedure.

ohmic contact was obtained by alloying the AuGe in N_2 atmosphere at 450°C for 5 minutes.

Al was used for the gate contacts and both first and second levels of metallization. A single lift-off technique was used also for the Al deposition. The first level of metallization was separated from the second one by a layer of polyimide. Si_3N_4 was used first, but it caused damage to the channel. Annealing at 450°C could not cure this damage. Therefore, polyimide PI 2550 from DuPont was used instead. Polyimide, diluted with thinner (1:1), was spun at 8000 rpm to give a layer of about 8000 Å. The wafer was soft baked at 150°C for 30 minutes and then cooled down to room temperature. Photoresist AZ 1450J was spun over the polyimide, soft baked, and exposed. The wafer was then developed in 1MF312 : $1H_2O$ solution by volume for about 1 minute to etch both the photoresist and the polyimide in one step.

The wafer was then loaded into the evaporator and the via holes were filled with Al. After lifting off the unwanted metal, the polyimide was hard baked at 180°C for 2 hours to make it resistant to the developer. Finally, the second level of metallization was deposited using the single lift-off technique. Fig(3-6) shows a micrograph picture of the test and monitoring devices fabricated using this technique.

The I-V characteristics of both a 2μm gate and a fat FET transistors fabricated using this technique are shown in Fig.(3-7). The transconductance for the 2 μm gate transistor, with threshold voltage of -2.4 V, was found to be 53 mS/mm which is considered reasonable for these gate dimensions [47].

Good uniformity for both the threshold voltage and the current saturation across the wafer was observed. The standard deviation for V_{th} was

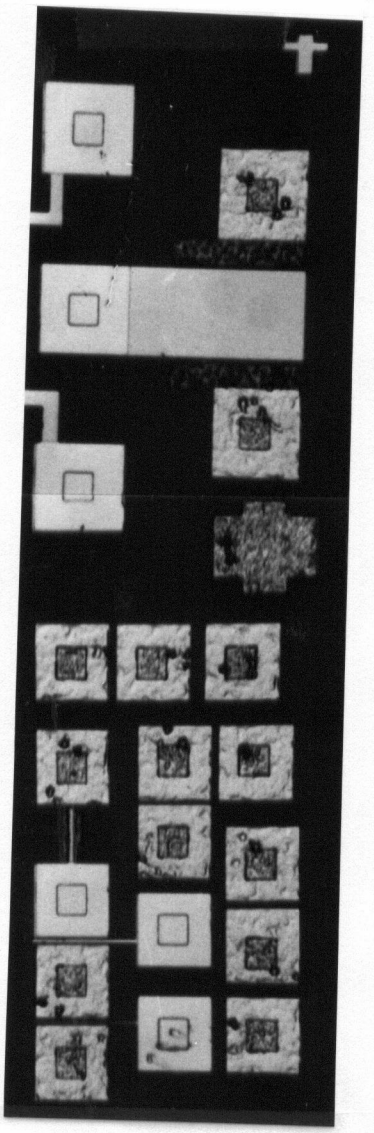


Fig.(3-6) Micrograph picture of the test and monitoring devices.

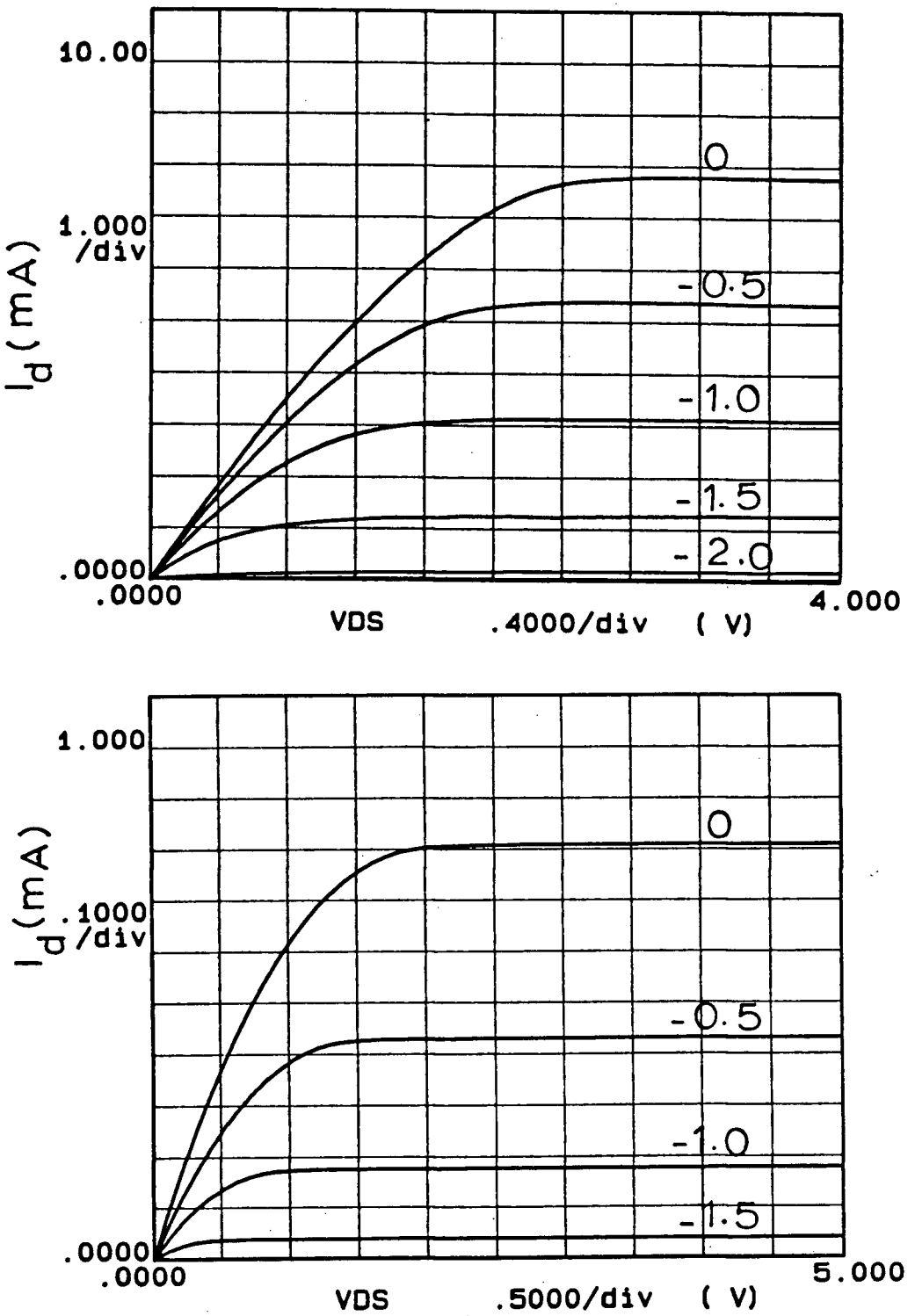


Fig.(3-7) I-V characteristics of (a) 2μm gate and (b) fat FET trnasistors fabricated using the ion-implanted planar process.

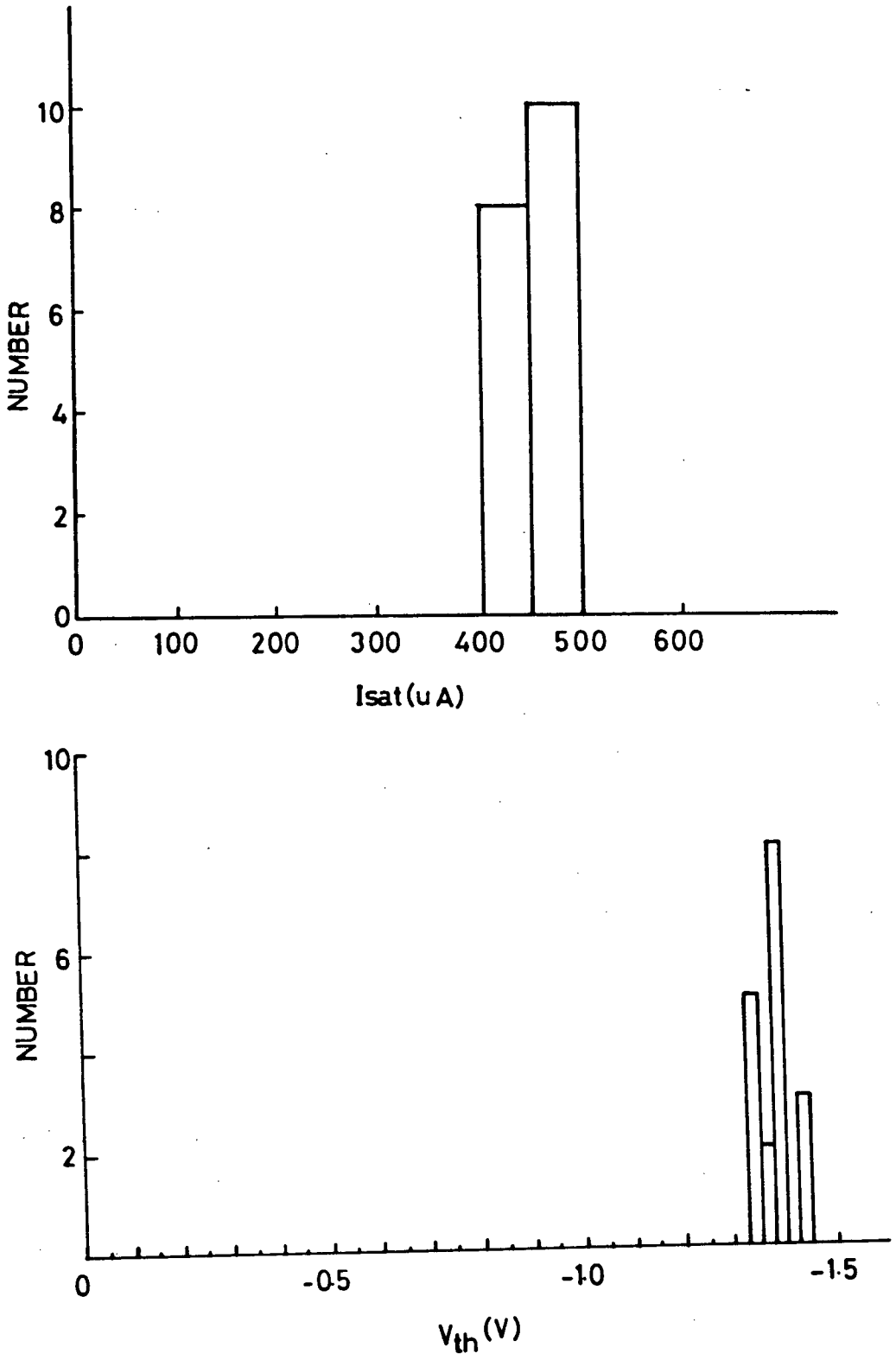


Fig.(3-8) V_{th} and I_{sat} histograms for sample #4.

found to be 35 mV for an average value of -1.38 V, Fig.(3-8.a). The standard deviation for the saturation current was 21 μA for an average value of 447 μA, Fig.(3-8.b). The fat FET was used in this study instead of the 2μm gate FET in order to reduce the effect of the series resistance, where in this case the channel resistance was much higher than the series resistance. The good uniformity can be attributed to the high quality for the channel due to the successful annealing.

(b) Recessed Gate Technique

This process is, in general, similar to the ion-implanted planar process except that the channel is etched for the gate recess. The wafer was cleaned using the Rockwell precleaning procedure (see Appendix(C-1)), then the registration marks were etched as explained in the previous section. The channel was formed by implanting Si^{29} with a dose of 3.25×10^{12} ions/cm^2 and energy of 120 keV (see Fig.(3-9)). For simplicity no n^+ layer was formed where the n layer was thick enough and highly doped. 80 nm of Si_3N_4 was deposited for annealing which was performed at 830°C for 25 minutes. AuGe was deposited and alloyed at 450°C for 5 minutes.

The gate was recessed by patterning the photoresist, as discussed before, then the wafer was dipped into 10% HCl to remove the oxide before it was immersed in a solution of

5% H_2PO_4 : 2.5% H_2O_2 : 92.5% H_2O

by volume for 85 seconds to remove about 100 nm of GaAs. Removing the oxide resulting from the etching process was done by immersion into buffered HF for 30 seconds immediately before loading into the metal evaporator for gate metal deposition.

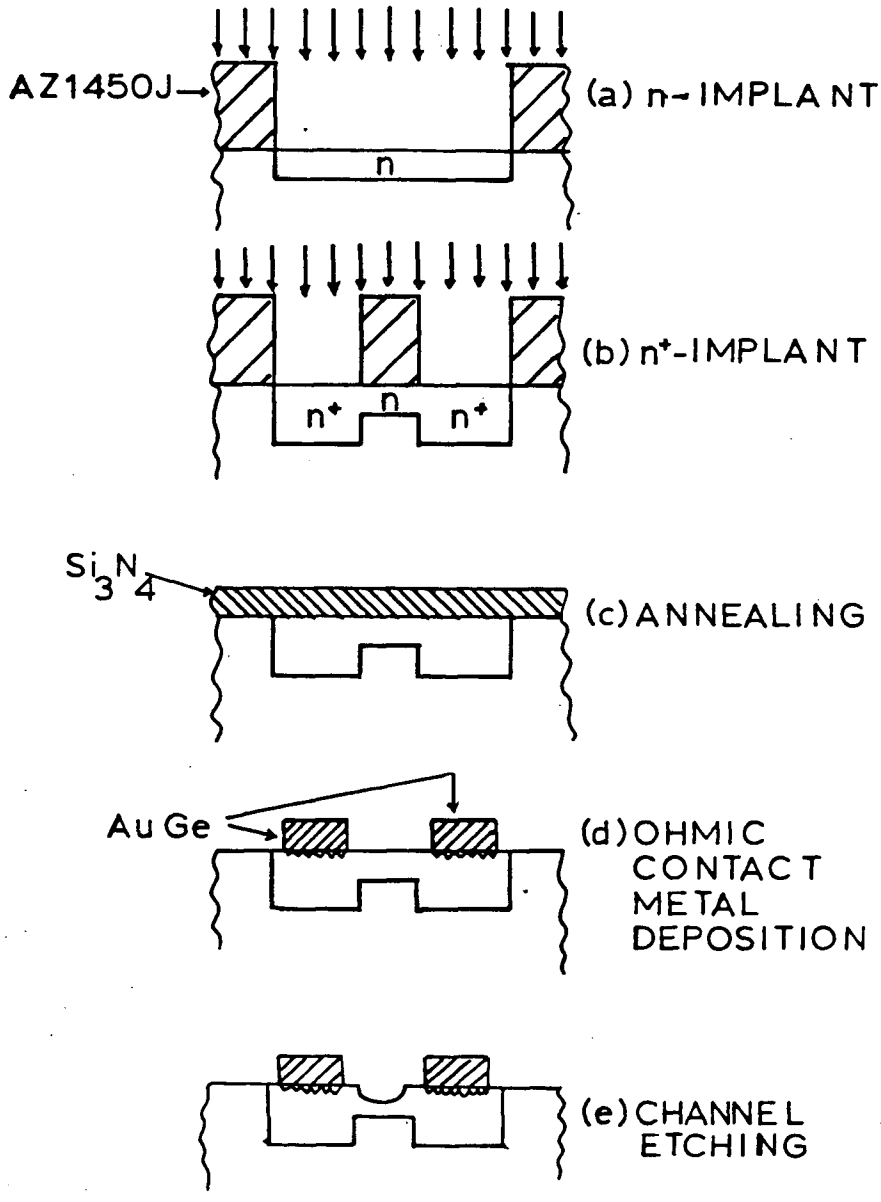


Fig.(3-9) Recessed gate process adapted at UBC.

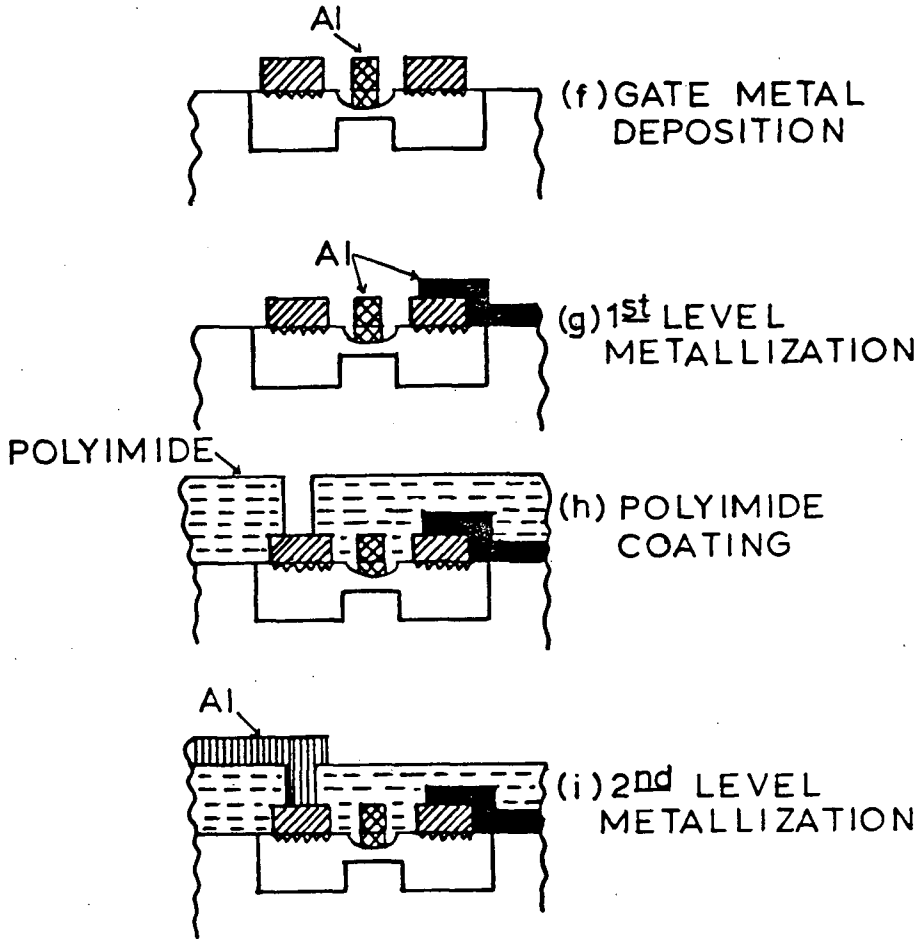

Al
(f) GATE METAL DEPOSITION
Al
(g) 1st LEVEL METALLIZATION
POLYIMIDE
(h) POLYIMIDE COATING
Al
(i) 2nd LEVEL METALLIZATION

Fig.(3-9) Cont.

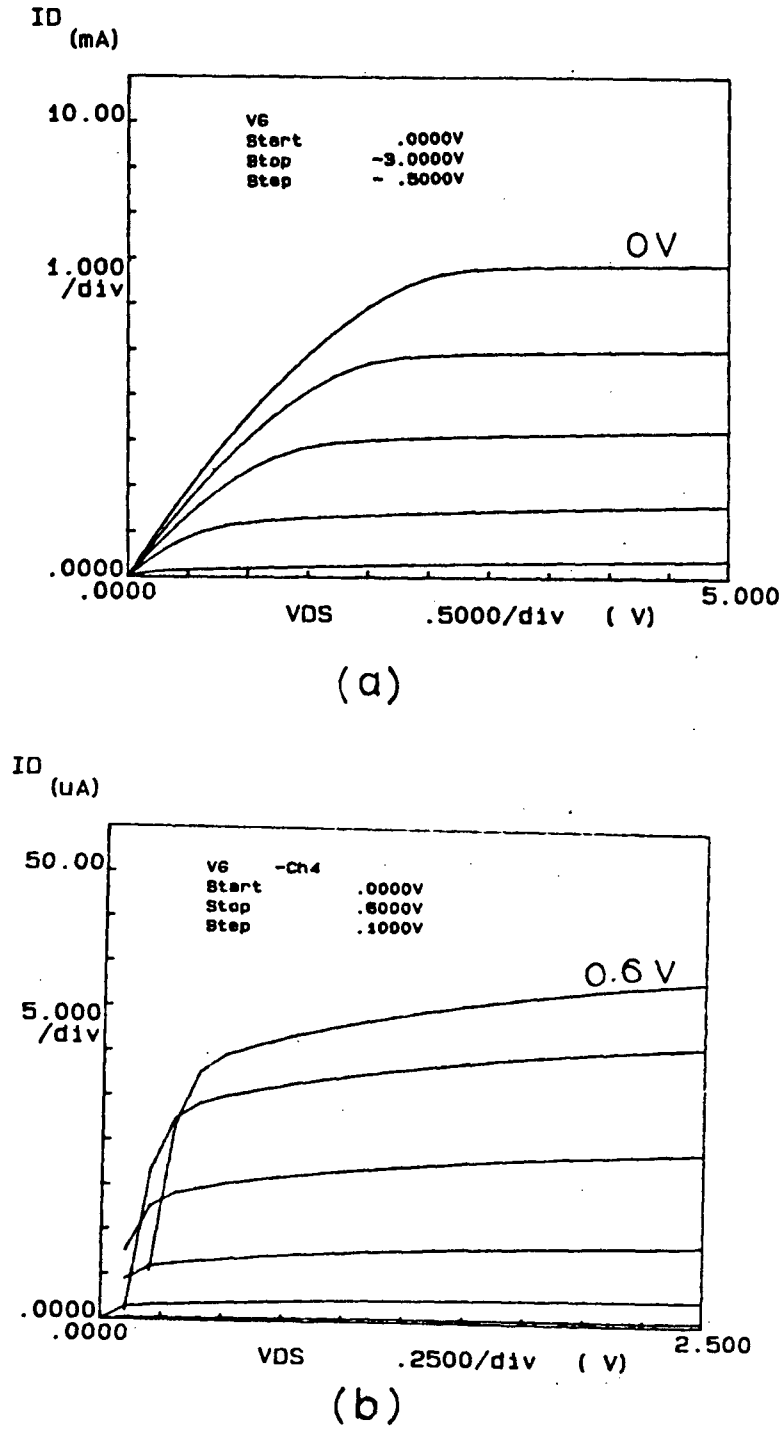


Fig.(3-10) I-V characteristics of (a) 2μm gate and (b) fat FET transistors fabricated using the recessed gate process.

Fig.(3-10) shows the I-V characteristics of a 2 μm gate and a fat FET transistor fabricated using this technique. As shown in the figure, the fat FET transistor is an enhancement-mode device while the 2 μm gate transistor is a depletion mode transistor with a -2.5 volt threshold voltage. The big difference in the threshold voltages is believed to be due to a difference in the amount of GaAs etched from the channel. Both transistors were fabricated on the same chip, but the etching rate was perhaps different due to the strong effect of the surface tension in the case of short line widths. The dependence of the etching rate on the gate dimensions may make it harder to control the threshold voltage of more than one set of devices with different gate lengths on the same chip.

The transconductance for the 2 μm gate one was found to be 40 mS/mm which is nearly 25% less than that of the ion-implanted planar process. This reduction in the transconductance can be attributed to the low electron mobility due to the use of high doses to form the channel, see relation (1-10).

The standard deviation for the threshold voltage was -1.15 V with an average value of -2.34 V as shown in Fig.(3-11.a). The saturation current uniformity was even worse, exhibiting a standard deviation of 3.9 mA for an average value of 5.1 mA (Fig.(3-11.b). The scattering of V_{th} and I_{sat} can be attributed to the nonuniform etching of the channel because of the etching rate sensitivity to the etchant temperature and concentration across the wafer. However more controlled etching can be obtained, it may be hard to achieve a uniformity similar to that of the ion-implanted planar process.

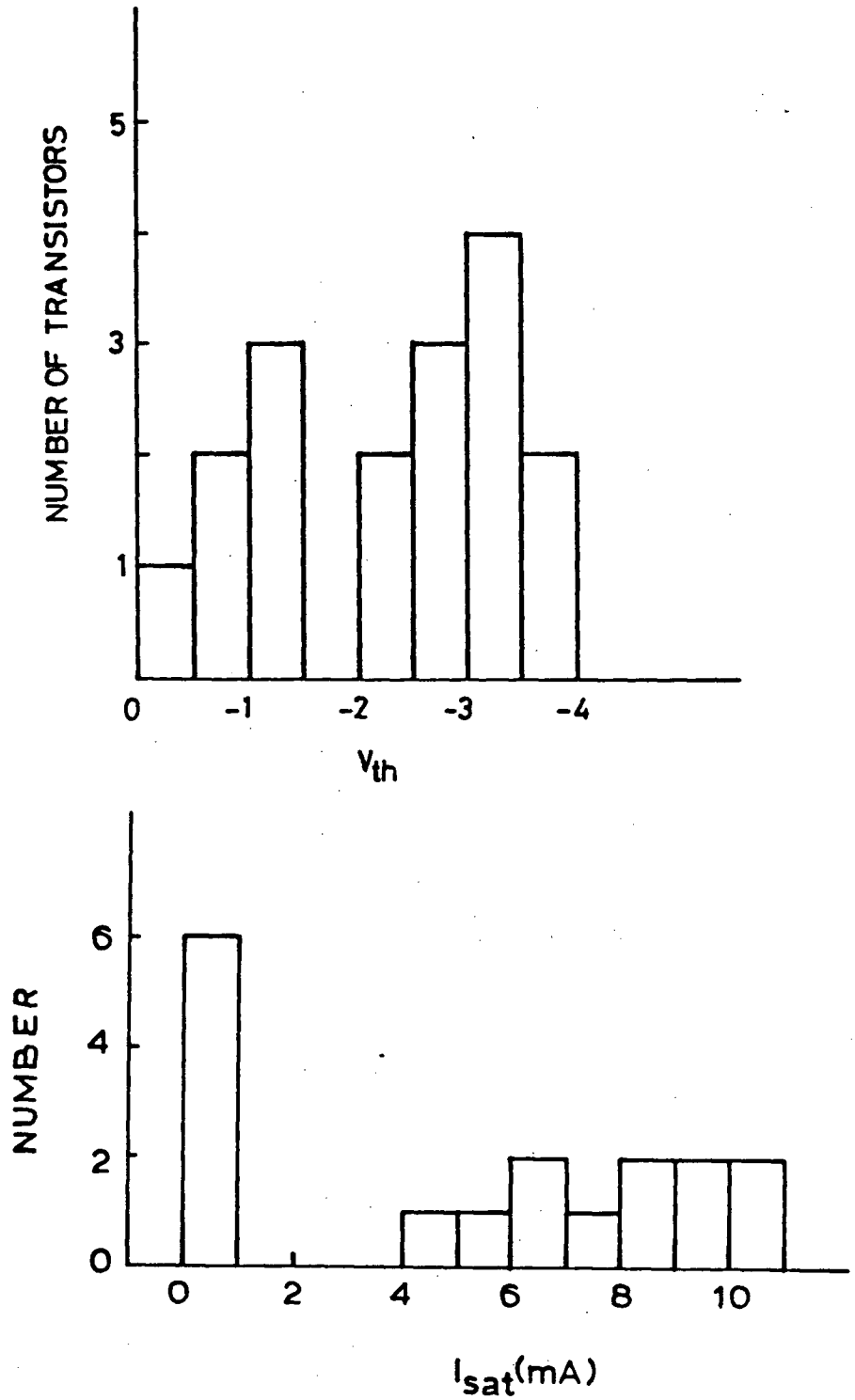


Fig.(3-11) V_{th} and I_{sat} histograms for sample D7.

(c) The Self-Aligned Gate Using Polyimide (SAGUPI)

In this process, polyimide PI2550 from DuPont is used as an intermediate layer. A schematic diagram of the SAGUPI is shown in Fig.(3-12). The process starts with the regular cleaning procedure as discussed in section (3-2(a)). Channel implantation of Si^{28} or Si^{29} was carried out using AZ1450J photoresist as a mask. The doses and energies used ranged from 1.61×10^{12} to 3.25×10^{12} ions/cm^2 and from 60 to 120 keV respectively. A layer of Si_3N_4 was deposited (see Appendix(C-3)) to serve later as a cap for annealing. Polyimide (1 PI : 2 thinner by volume) was spun over the Si_3N_4 layer at 5000 rpm for 30 seconds, then soft baked at 180°C for 30 minutes to increase its resistance to the positive resist developer (MF312).

Dummy gates of Al were deposited over the polyimide using the single lift off, described before in this Chapter. The unmasked polyimide was etched using O_2 plasma (see Appendix(C-2)). A T-structure resulted because of the resistance of the dummy gate to the O_2 plasma etch (see Fig.(3-12.c)). This undercut was used to protect the area underneath from being implanted with n^+. This would allow about 300 nm space between the gate metal and the n^+ areas. After the n^+ implantation, SiO_2 was sputtered using Ar only (without O_2) to reduce the risk of the polyimide being etched by O_2 plasma (see Appendix(C-4)). After the SiO_2 deposition, the polyimide was dissolved in hot n-methyl-2-pyrrolidone to lift off the dummy gates as shown in Fig.(3-12.f). This step resulted in covering the whole wafer except the gate areas with SiO_2. The wafer was then ready for annealing which was carried out at 830°C for 25 minutes in N_2 atmosphere.

Holes for the ohmic contact metals (AuGe were etched in the SiO_2 and

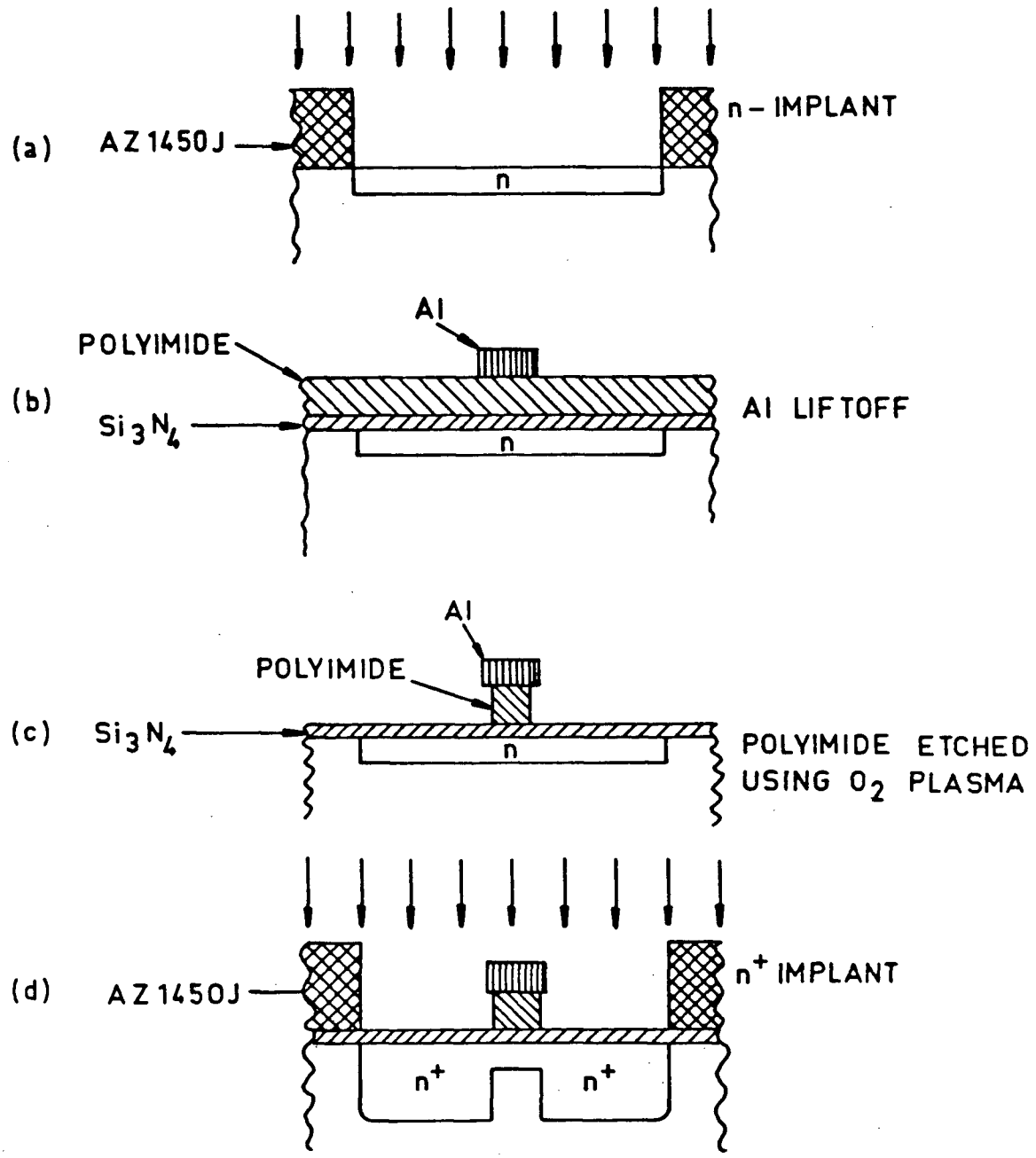


Fig.(3-12) Self-aligned gate technique using polyimide (SAGUPI).

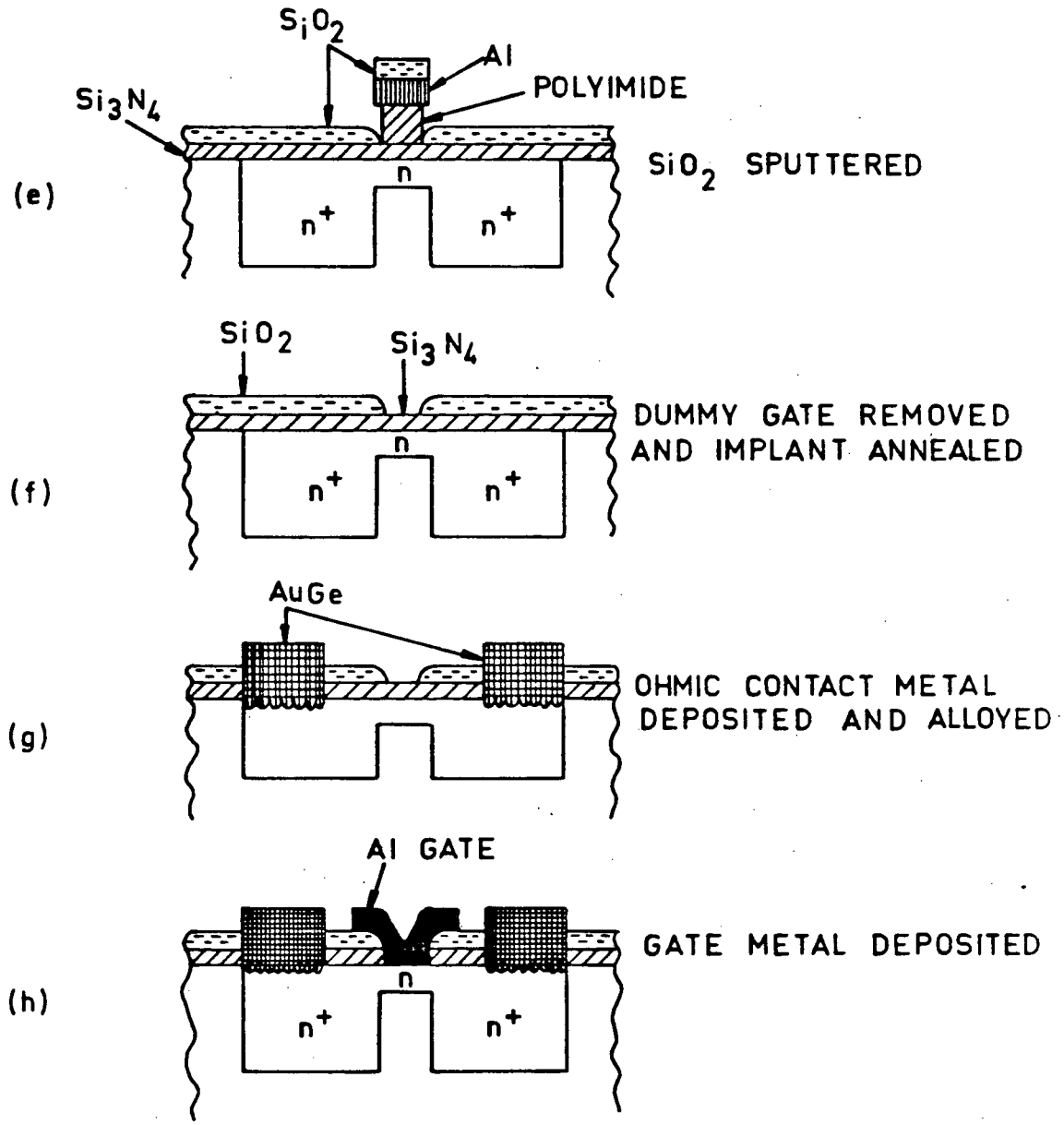

(e)
Si_3N_4
SiO_2
Al
POLYIMIDE
n
n^+
n^+
SiO_2 SPUTTERED
(f)
SiO_2
Si_3N_4
n
n^+
n^+
DUMMY GATE REMOVED
AND IMPLANT ANNEALED
(g)
AuGe
OHMIC CONTACT METAL
DEPOSITED AND ALLOYED
(h)
Al GATE
n
n^+
n^+
GATE METAL DEPOSITED

Fig.(3-12) Cont.

Si_3N_4 layers using buffered HF and CF_4 plasma respectively (see Appendix(C-5)). After alloying the AuGe at 450°C for 5 minutes the Si_3N_4 over the gate areas was etched using CF_4 plasma while the SiO_2 served as a mask to protect other areas. The gate metal was then deposited. The gates were in contact with the channel in the areas which were not covered with SiO_2. Finally, the first and the second level of metallization was deposited as discussed in the first section of this chapter.

Fig.(3-13) shows the I-V characteristic of a 2 μm gate and a fat FET transistor fabricated using this process. The transconductance for the 2 μm gate transistor was 62 mS/mm which is about 50% higher than that of the recessed gate transistor and 17% higher than that of the ion-implanted planar transistor. The increase of the g_m in the present technique can be attributed to the reduction in the series resistance and may be due to the reduction in the gate length due to the dummy gate undercut.

In terms of uniformity, this technique gave much better uniformity than the recessed process. The uniformity could be similar to that of the ion-implanted planar process, where in both cases no channel etching has taken place. Fig.(3-14) shows the histogram of both V_{th} and I_{sat}. The figures show a standard deviation of V_{th} of -0.145 for an average of -2.62 V and I_{sat} standard deviation of 240 uA for an average of 1.74 mA.

The SAGUPI process differs from the SAINT process in that instead of the photoresist (FPM or AZ) above the Si_3N_4 to obtain an undercut, we use polyimide. This has several advantages:

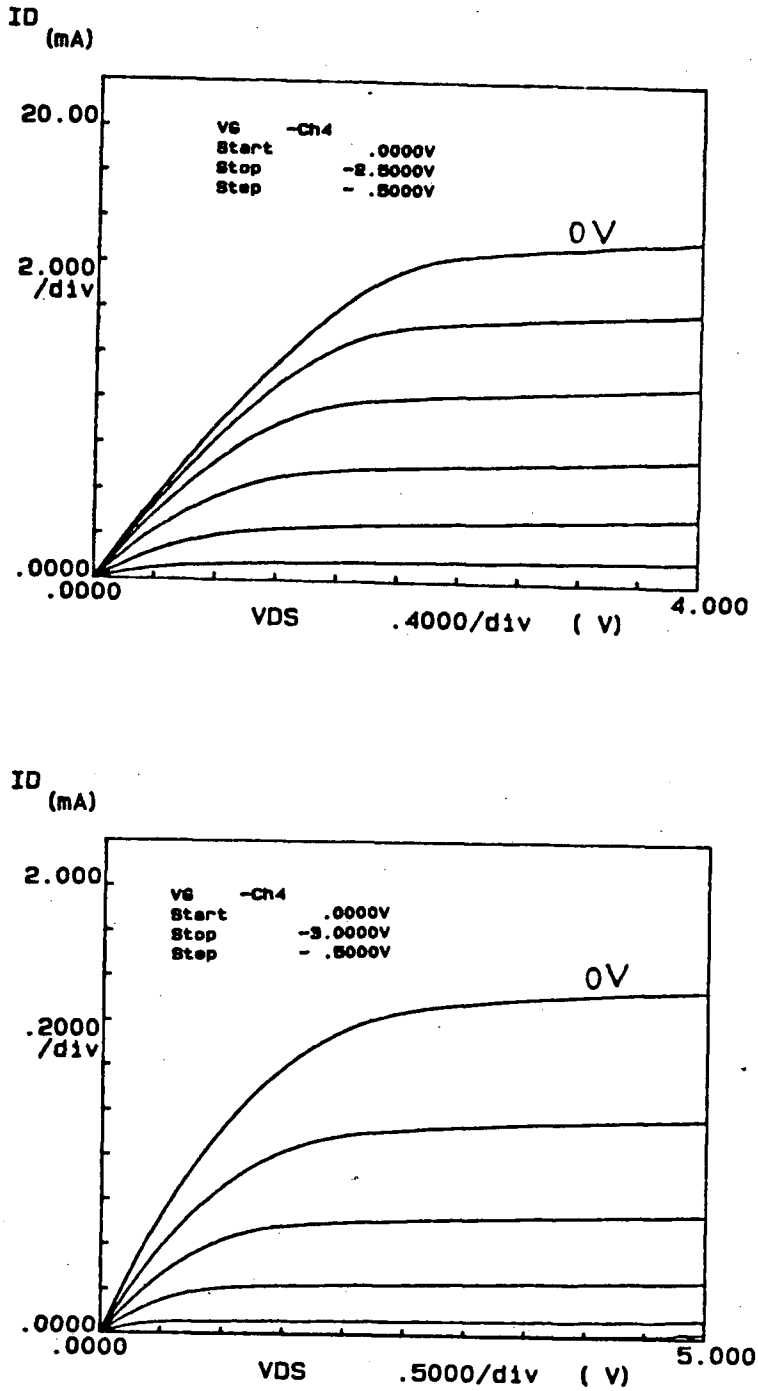


Fig.(3-13) I-V characteristics of (a) 2μm gate and (b) fat FET transistors fabricated using SAGUPI technique.

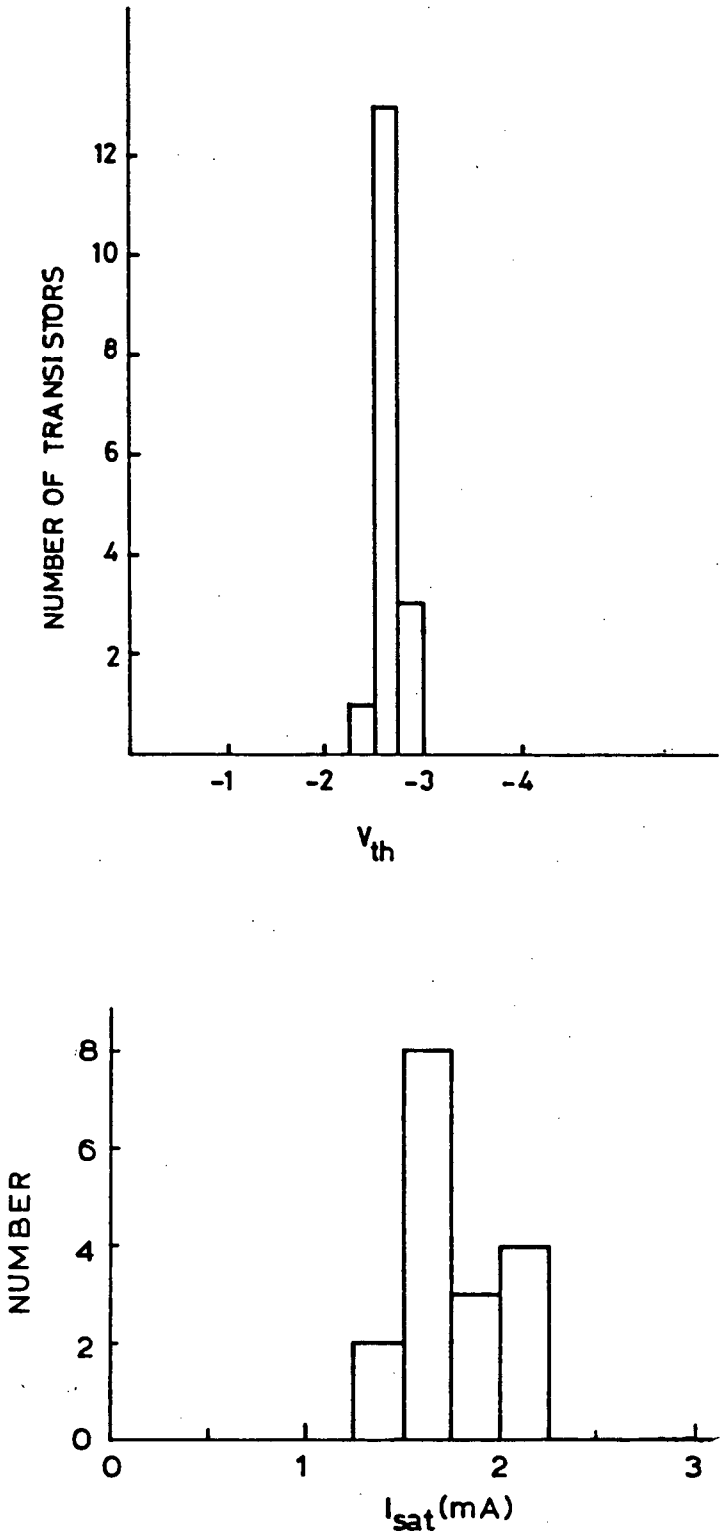


Fig.(3-14) V_{th} and I_{sat} histograms for sample E7.

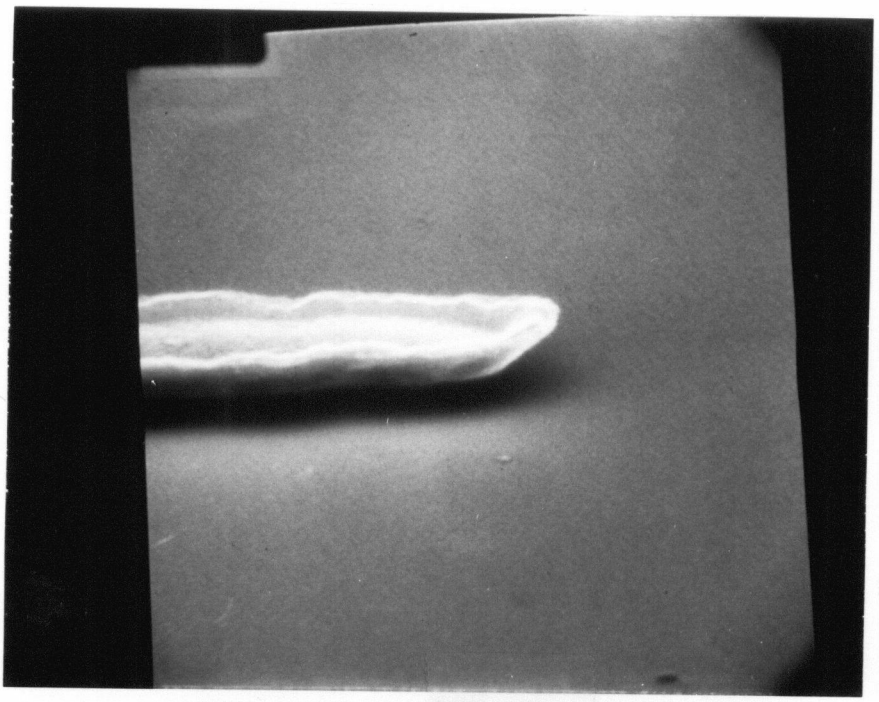


Fig.(3-15) SEM micrograph for gate undercut after O_2 plasma etching of polyimide.

(a) it has greater heat resistance, thus allowing more choice of metal deposition;

(b) it is more resistant to the sputtering process used to deposit SiO_2;

(c) the polyimide is not photosensitive, therefore a simple lift-off process can be used to deposit the dummy gate instead of the multiple layer resist in the SAINT process.

As compared to the refractory metal (or silicide) gate processes, the final gate metallization has to be in good alignment with the holes etched for it in the Si_3N_4 (instead of being in place throughout). However, this is not too difficult since the overlap necessary to ensure covering the hole goes over the relatively thick SiO_2+Si_3N_4 and hence should not produce excessive extra capacitance. The main advantage of the new technique over the refractory metal one is the lack of the requirements that

(a) the gate should withstand the high temperature post-implantation anneal,

(b) no reaction should take place between the gate metal and the GaAs substrate,

(c) the thermal expansion of both the gate metal and the GaAs should be matched to avoid the gate lifting off during the annealing,

(d) good adhesion must be ensured between the gate metal and both the GaAs wafer and the dummy gate, and

(e) an extremely clean and O_2 free interface between the gate metal and the GaAs material must be ensured.

The lack of these requirements gave more freedom in choosing a gate materials structure to satisfy the electrical requirements of a good Schottky diode and low series resistance. Moreover, adhesion can be enhanced between

the polyimide and the Si_3N_4 by using an adhesion promoter, such as VM-651 from DuPont, and between the dummy gate and the polyimide by etching the latter in O_2 plasma for 5 seconds to increase the roughness of the polyimide surface.

CHAPTER(4)

DC MEASUREMENTS

In this Chapter, the D.C. measurements and the temperature dependence of the depletion mode transistors are presented. Fat FETs, 2μm gate transistors, and pads for ohmic contact and implanted layer characterization were used.

Transistor parameters (V_{th}, I_{sat}, g_m, and g_d), Schottky contact parameters (ideality factor n, saturation current I_s and barrier height ϕ_{bn}), implanted layer parameters (sheet resistance R_{SH}, mobility μ, and carrier concentration profile, N(x)), and ohmic contact parameters (contact specific resistance ρ_c) were measured. The sample yield was measured by counting the number of working devices and measuring the transistor parameters (V_{th} and I_{sat}) to test for uniformity across the wafer. The transistor I-V characteristics were simulated using Spice2.G [14] and these results were compared with the experimental ones.

The simulation parameters β, R_s, R_d, C_{gs}, C_{gd}, and V_{th} were obtained from the experimental results. β was determined from the relation

$$I_{sat} = \beta(V_{gs} - V_{th} - I_{sat} \cdot R_s) \qquad (4\text{-}1)$$

for the fat FET and from relation (1-8) from the 2μm FET transistor [17].

R_s and R_d were calculated from the channel sheet resistance, measured using the test pad structure (A3), and the spacing between the gate and both the source and the drain. The ohmic contact resistances were taken into consideration in calculating R_s and R_d. The threshold voltages were measured from the square law relation of $\sqrt{I_{sat}}$ vs. V_{gs} by extrapolating the linear

region to intersect with the V_{gs} axis to give the value of V_{th}, as shown in Fig.(4-1). The gate capacitance ($C_g = 2C_{gs} = 2C_{gd}$) was measured with the HP 4275A Multi-Frequency LCR meter.

Fig.(4-2) shows both the experimental and the simulated I-V curves of the 2μm and fat FET transistors. The simulation parameters are shown in Table(4-1). The experimental and simulated curves coincided for the long gate transistor. In case of the short gate one (2μm FET), the two sets of curves coincided in the saturation regions and deviated in the linear regions. The deviation became less noticeable for larger negative values of V_{gs}. These results are in agreement with those obtained by others [48]. The deviation of the simulated curve from the experimental one is due to the difference in the saturation mechanism of the current where the current saturates in the case of short channel transistors (<2μm) due to the electron velocity saturation while the program considers the saturation to be due to channel pinch off.

The chip yield and the device parameter uniformity across the wafer were investigated. The yield was as high as 100% for most of the samples. The yield was less than 100% for some samples due to the destruction of transistors at the edge of the wafer during the fabrication process. Although the yield obtained in our laboratory cannot be compared with that obtained by industrial firms where a very large number of devices are fabricated on complete wafers, our results can still give an indication of the yield. Sample#4 was chosen for ths study because it was the biggest piece, with 18 transistors on it. The uniformity of sample#4 was discussed in Chapter(3).

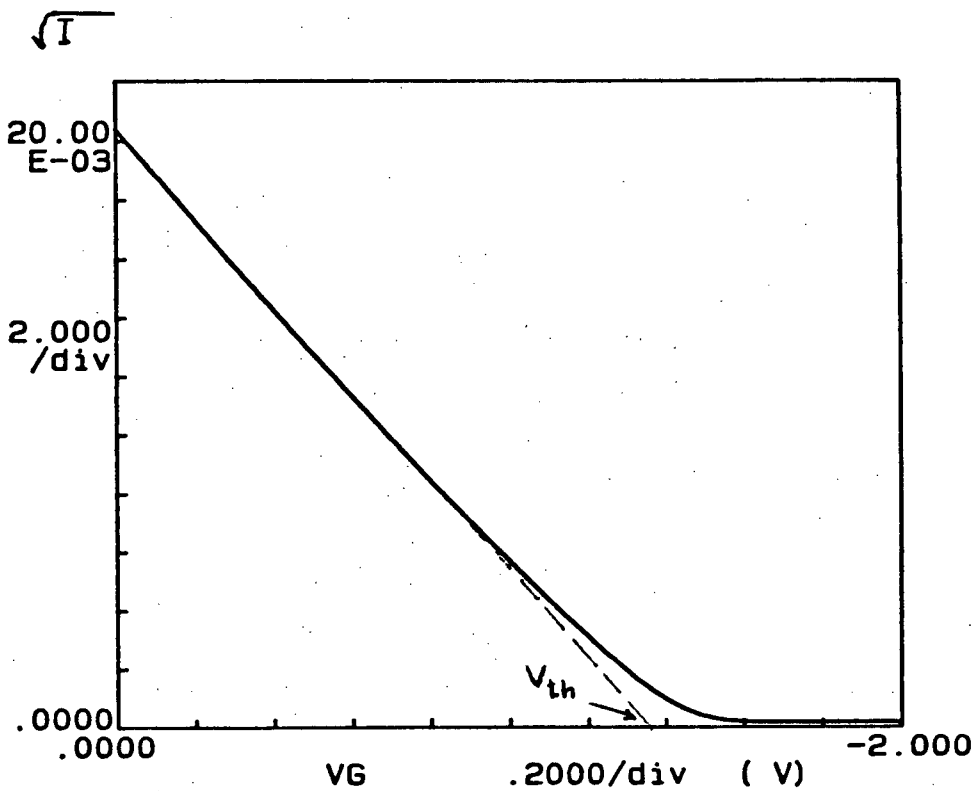
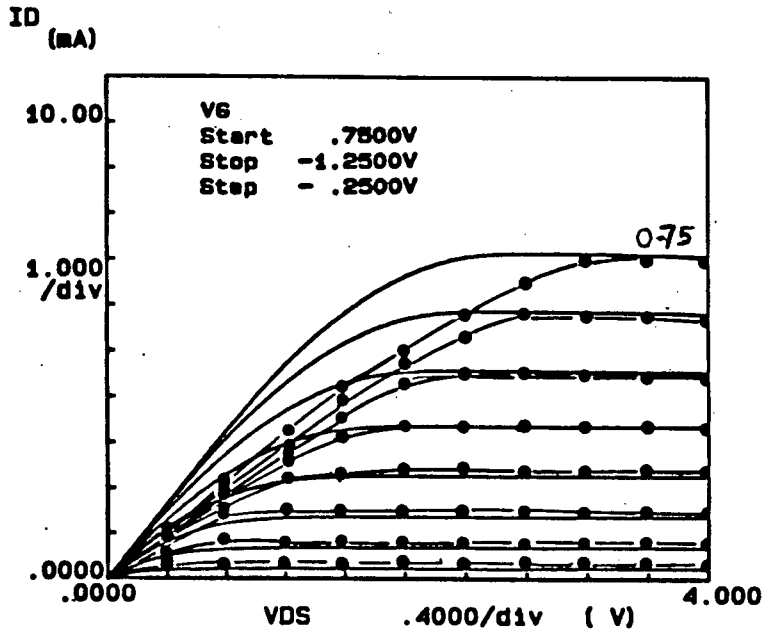
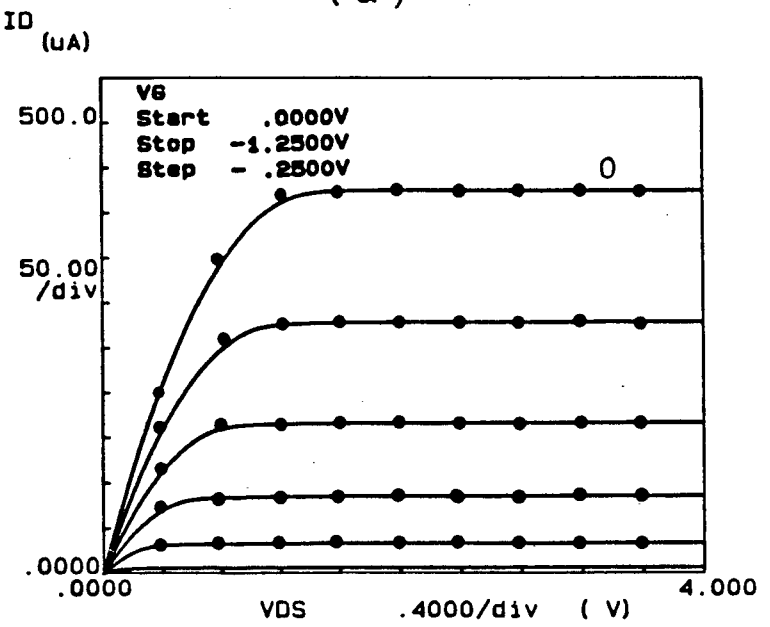


Fig.(4-1) $\sqrt{I_{ds}}$ vs. V_{gs} for a fat FET transistor.



(a)



(b)

Fig.(4-2) Experimental and simulated I-V characteristics of (a) 2μm gate and (b) fat FET transistors from sample#4 (_____ measured and ..... simulated).

TABLE(4-1)

Simulation parameters for 2 μm gate and fat FET transistors from sample#4

Parameter	2 μm FET	Fat FET
$R_s(\Omega)$	68	62
$R_d(\Omega)$	180	104
$V_{th}(V)$	-1.37	-1.32
$\beta(A/V^2)$	2.8×10^{13}	2.5×10^{-4}
C_{gs}	100 fF	10.8 pF
C_{gd}	100 fF	10.8 pF

Schottky contacts were characterized by measuring the saturation current I_s, the ideality factor n, and the barrier height ϕ_{bn}. As discussed in section (2-3), $\ell n(I_f)$ vs. V_f curves were plotted and extrapolated to intersect with the $\ln(I_f)$ axis to give I_s (Fig.(4-3)). ϕ_{bn} was then calculated from the relations [2]

$$\phi_{bn} = (kT/q)\ \ln(A^{**}\ T^2/J_s) \qquad (4\text{-}2)$$

with $A^{**} = 50\ cm^{-2}K^{-2}$ [72]. n was obtained from the relation

$$n = (q/kT)(dV/d(\ell n(I_f))) \qquad (4\text{-}3)$$

The measured ideality factor and barrier height for the transistor Schottky contacts were 1.13 and 0.795 eV respectively at room temperature.

Test patterns A3, A4, and A5 were used to measure the implanted layer sheet resistances and the ohmic contact specific resistivity. The transmission line model (TLM) was used to obtain the values of these parameters. The TLM was originally proposed by Shockley [49] and modified by others [50-51].

Fig.(4-4) shows a schematic diagram of 3 pads where $\ell 1$ are $\ell 2$ are the the distances between the pads and d is the length of the pads. The total resistance between any two pads is given by

$$R_T = 2R_C + (R_{SH} \cdot 1/W) \qquad (4\text{-}4)$$

where R_C is the ohmic contact resistance, R_{SH} is the sheet resistance of the layer between the pads, and W is the pad width. Harrison et al. [50] show that contact resistance is equal to

$$R_c = (R_{SK} \cdot L_T/W) \cdot \coth(d/L_T) \qquad (4\text{-}5)$$

where R_{SK} is the sheet resistance of the layer under the pads and L_T is the so called transfer length. L_T is given by

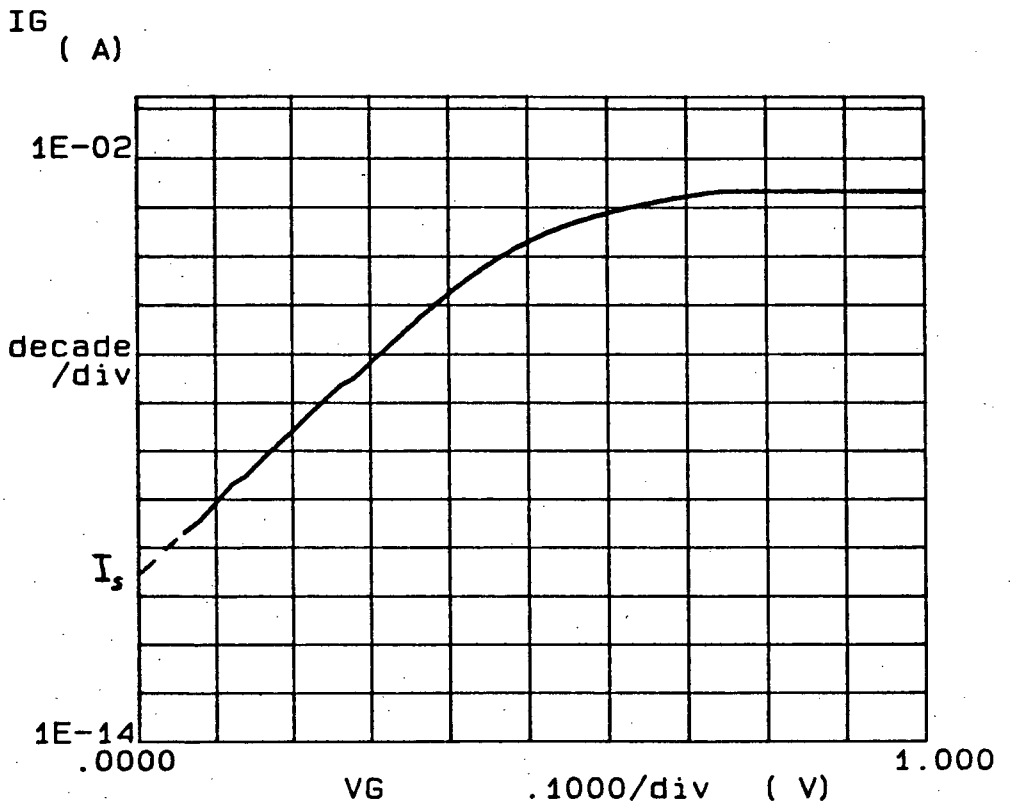


Fig.(4-3) $Ln(I_g)$ vs V_g for a fat FET.

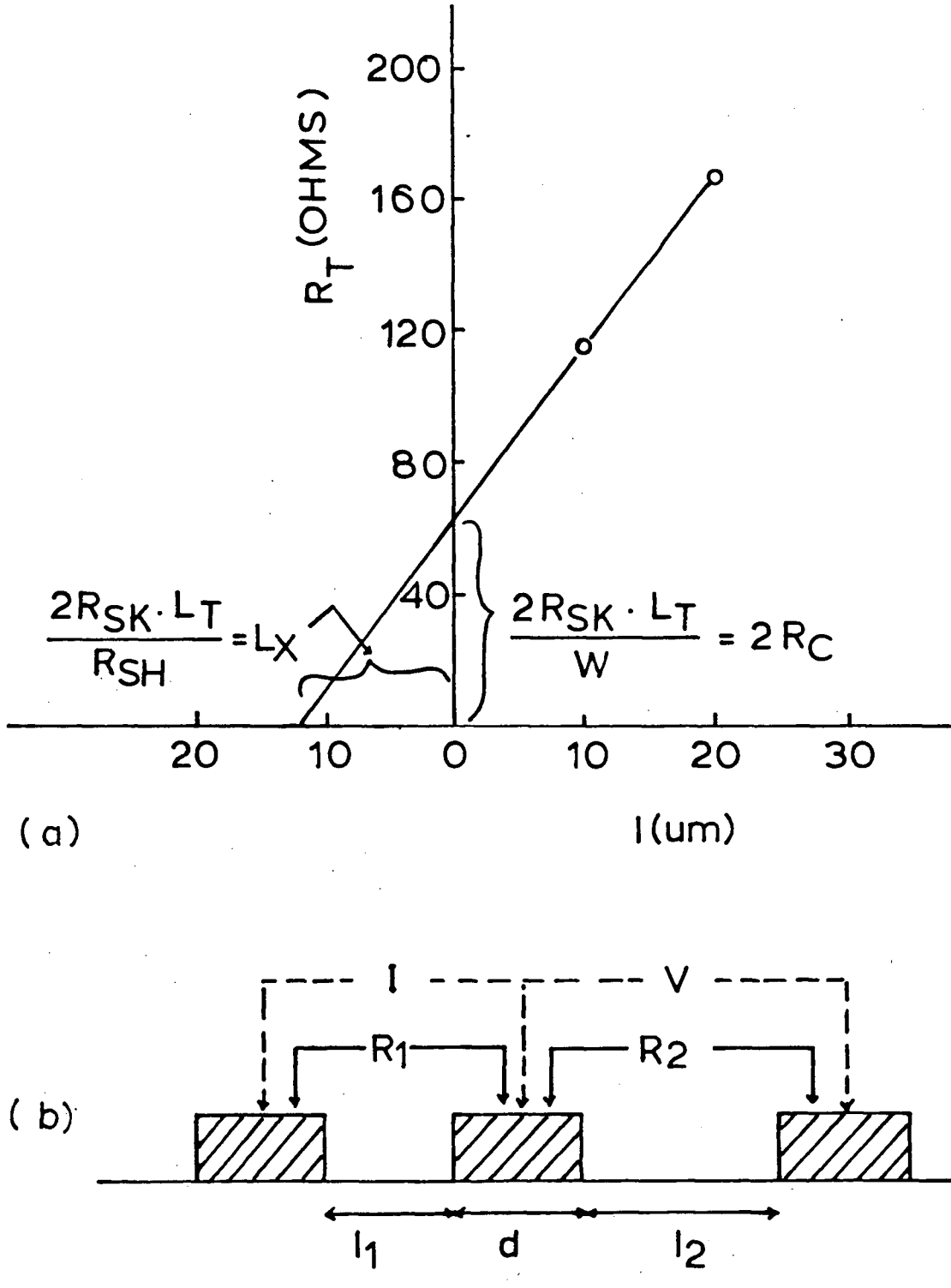


Fig.(4-4) Transmission Line Model (TLM) (a) plot of total contact to contact resistance and (b) experimental measurements for obtaining the total resistance and the contact end resistance values.

$$L_T = \sqrt{\rho_c / R_{SK}} \qquad (4\text{-}6)$$

ρ_c is the contact specific resistance in ohm-cm^2. For $d > 2L_T$, relation (4.5) leads to

$$R_T = (2R_{SK} \cdot L_T)/W + (R_{SH} \cdot 1)/W \qquad (4\text{-}7)$$

Reeves et al. [51] considered a value of d of 50 μm greater than $2L_T$. Therefore, the previous condition was valid in our case where pads of 100 μm length were used.

Relation (4-6) is plotted in Fig.(4-4) for sample#4. The intersection with the vertical and horizontal axes give the values of R_C and L_X respectively, where

$$2R_c = 2R_{SH} \cdot L_T/W \qquad (4\text{-}8)$$

and

$$L_X = 2R_{SK} \cdot L_T/R_{SH} \qquad (4\text{-}9)$$

Solving equations (4-8) and (4-9) together, one can get the value of R_{SH}. Knowing the value of either L_T or R_{SK}, the other can be obtained from relation (4-9) and ρ_c from relation (4-5).

R_{SK} can be taken to be equal to R_{SH} if the sintering did not modify significantly the layer underneath. If it did, the measurement of the so-called contact end resistance R_E is required to obtain the value of L_T from the relation [50]

$$R_C/R_E = \cosh(d/L_T) \qquad (4\text{-}10)$$

The classical way of measuring R_E is to apply constant current between two contacts and measure the potential between one of these contacts and an opposite outside contact, as shown in Fig.(4-4). R_E will be V/I. Reeves

et al. [51] have shown that

$$R_E = 1/2(R1 + R2 + R3) \qquad (4\text{-}11)$$

where R1, R2, and R3 are the total resistances between pads (1 and 2), (2 and 3) and (3 and 1) respectively.

The sheet resistance of the implanted layers with n, n^+ and n plus n^+ were measured and shown in Table(4-2). The specific contact resistance of our samples was measured and found to range from high values of about 1.8×10^{-3} ohm-cm^2 from sample#2 to about 6.5×10^{-4} ohm-cm^2 for sample E7. The high values might be due to the failure to etch the native oxide immediately before depositing the AuGe alloy.

The low values of ρ_c are reasonable for the low implantation doses used and agree with the results reported by others [51]. The reason for using such low n^+ implantation is the need to use this layer to control the resistors used in the DACs and the inverter.

The C-V measurements were used to measure the doping and the mobility profiles of the channel implantation. The fat FET was used for this purpose. Pucel et al. [53] have shown that by measuring the gate capacitance C_g, and both the transconductance g_m and the channel conductance G at very low drain-source voltage (about 50 mV) one can get the mobility and the carrier concentration profiles of the channel implantation. At a distance X from the surface, the corresponding mobility can be obtained from

$$\mu(X) = (g_m/C_g)(L^2_g/V_{ds}) \frac{1}{[1 - (R_s + R_d)G]^2} \qquad (4\text{-}12)$$

and the carrier concentration

$$N(X) = (C^3/q\varepsilon)(dC/dV_{gs})^{-1} \qquad (4\text{-}13)$$

where

$$X = \varepsilon_r \varepsilon_0 W_g L_g (1 - g_m R_s)/C_g \qquad (4\text{-}14)$$

and C_g is the gate capacitance/unit area.

The mobility and carrier concentration profiles are shown in Fig.(4-5) and Fig.(4-6) respectively. A mobility of about 4500 cm^2/Vs for a carrier concentration of about 1×10^{17} ions/cm^3 was obtained.

The activation percentage was roughly calculated from the carrier concentration profile. The profile was considered to be gaussian since the Si diffusion constant is small [26]. Therefore, the fluence of the activated atoms ϕ' was calculated from the relation [54].

$$n' = \frac{0.4\phi'}{\sigma_\rho} \qquad (4\text{-}15)$$

where

n' is the peak carrier concentration and σ_ρ is the projected standard deviation. The activation percentage (efficiency) in this case is

$$\eta = \phi'/\phi \qquad (4\text{-}16)$$

where ϕ is the implanted dose [54].

The activation efficiencies for samples #2 and #4 were 73 and 85% respectively. The higher carrier concentration of sample#2 is responsible for the lower activation percentage it has [87]. In general, the activation percentages achieved are considered reasonable for similar dose values [87].

4-1 Implantation Through Si_3N_4

In some published work the dopant ions were implanted directly into GaAs

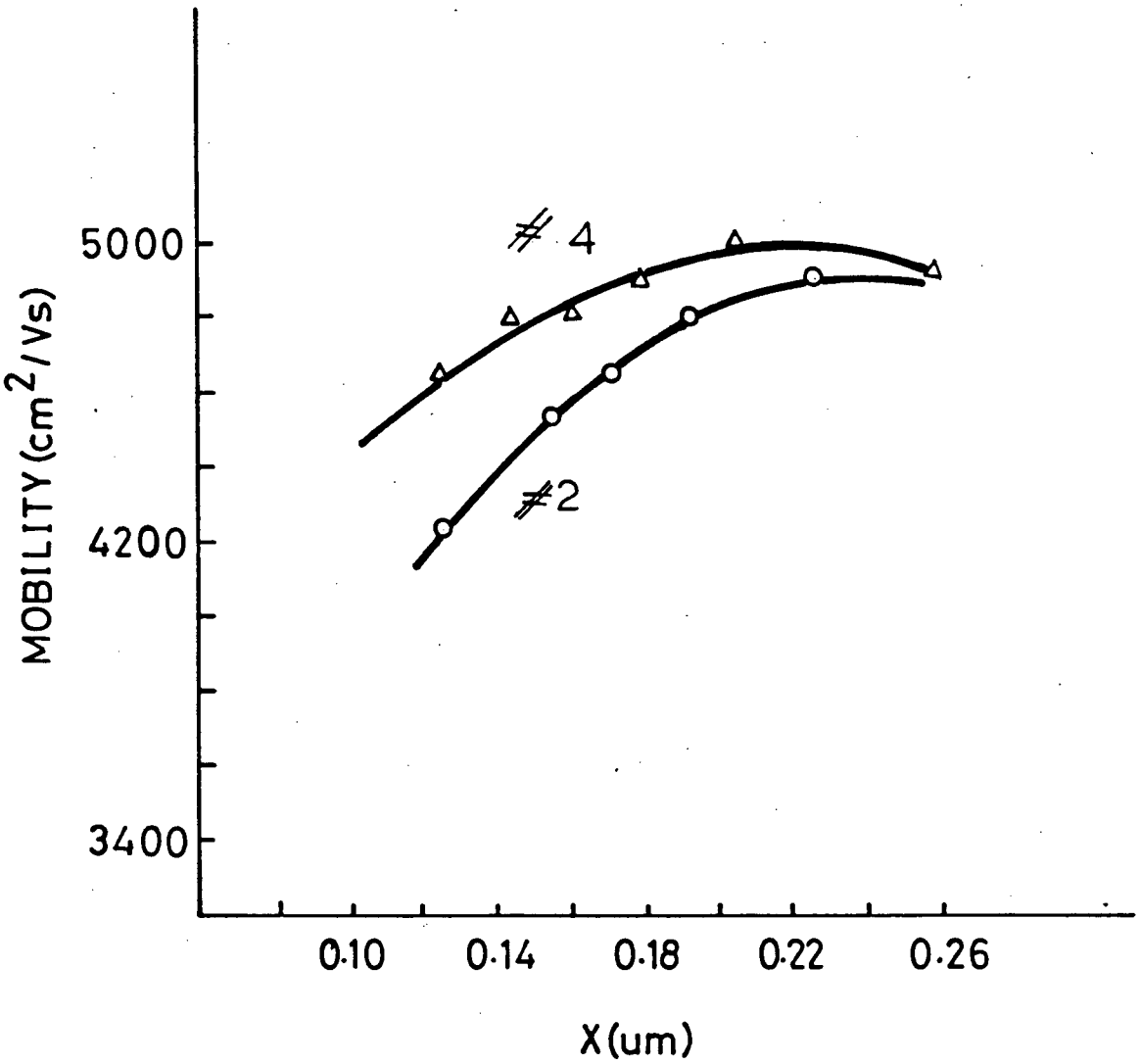


Fig.(4-5) Mobility profiles for sample#2 and sample#4.

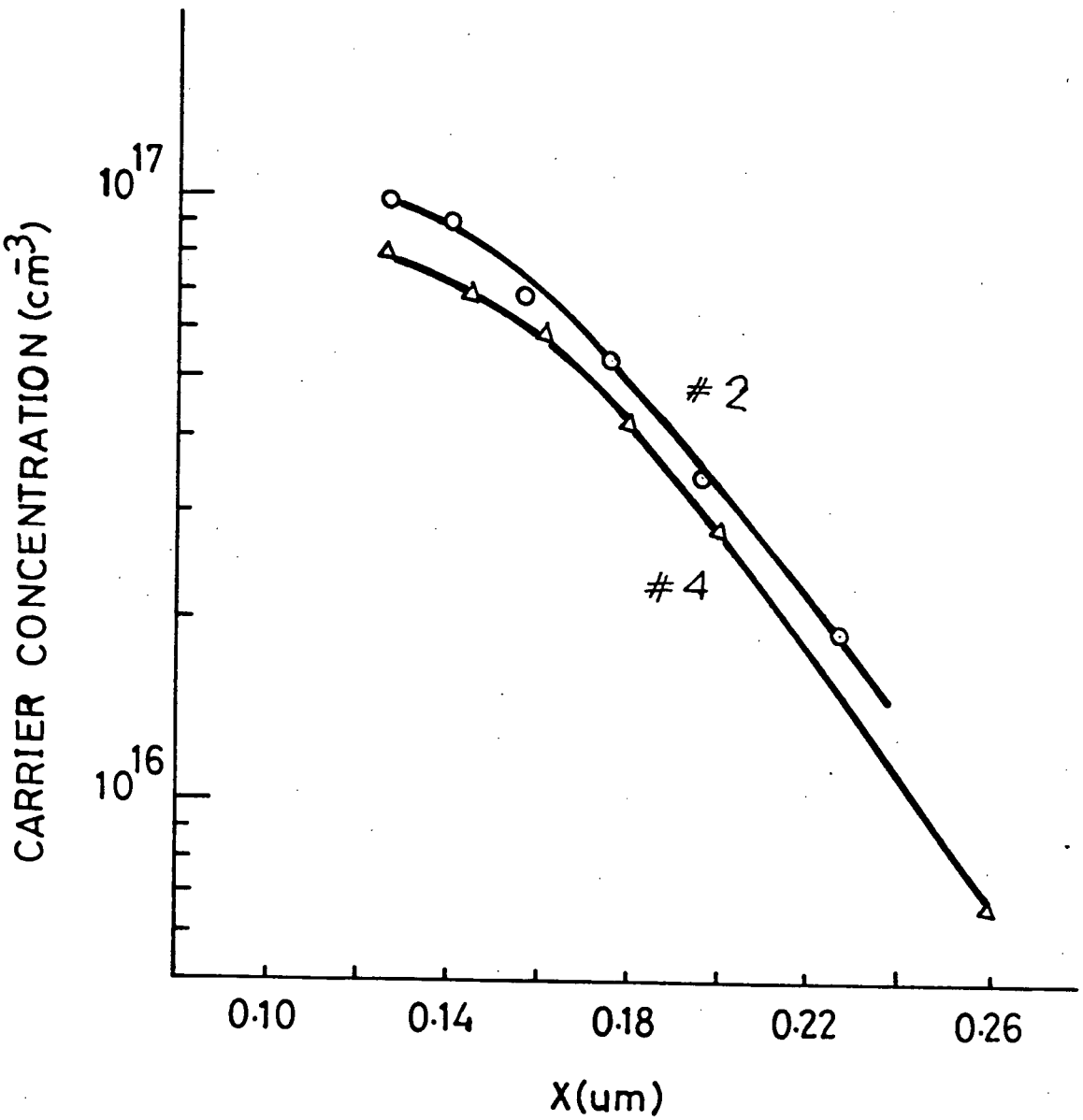


Fig.(4-6) Electron concentration profiles for sample#2 and sample#4.

TABLE(4-2)

Specific ohmic contact resistivity $\rho_c(\Omega/cm^2)$

Sample #	n		n^+		ρ_c
	Dose $10^{12}/cm^2$	Energy keV	Dose $10^{12}/cm^2$	Energy keV	Ω/cm^2
2	2.24	100	4.8	100	1.8×10^{-3}
3	1.6	100	4	100	2×10^{-3}
4	1.45	100	3.37	100	0.9×10^{-3}
B5	1.3	75	1.9	100	1.9×10^{-3}
G6	-	-	9.7	180	2.2×10^{-4}
E7	3.25	120	4.8	180	6×10^{-4}

through a layer of Si_3N_4 [34]. The reason for implanting through a Si_3N_4 layer is to protect the channel surface during the fabrication. In this study, the effect of implantation through Si_3N_4 on the device parameters was investigated.

Two samples were fabricated: the first (sample#1) was implanted through a 40 nm layer of Si_3N_4 while the second (sample#4) was implanted directly into GaAs. Both samples were annealed at 830°C for 25 minutes with Si_3N_4 caps 80 nm thick. The implantation dose and energy for the first one were 2.25×10^{12} ions/cm^2 and 120 keV while the second implantation dose and energy were 1.4×10^{12} ions/cm^2 and 100 keV respectively. The implanted dose and energy of sample#1 was chosen to be high to make sure that enough dopant atoms have reached the bulk of the GaAs through the Si_3N_4 layer to get devices of about -1 V threshold voltage.

The threshold voltage and the saturation current uniformity were investigated for both samples. The histogram of V_{th} and I_{sat} was shown in Fig.(4-7) for the first sample (sample#1) and Fig.(3-8) for the second sample (sample#4). The standard deviation of the threshold voltages were 336 mV and 35 mV for sample#1 and sample#4 respectively. For the saturation current, the standard deviations were 57 uA and 21 uA respectively. As shown in these figures, both V_{th} and I_{sat} are more scattered in the case of sample#1 than those of sample#4. The scattering of these parameters (in case of sample#1) can be attributed to the change in the thickness of the Si_3N_4 layer across the wafer. The nonuniformity of the Si_3N_4 layer has led to variation in the channel thickness across the wafer which has led in turn to the scattering of V_{th} and I_{sat} values. A variation of 10% in the channel thickness leads to

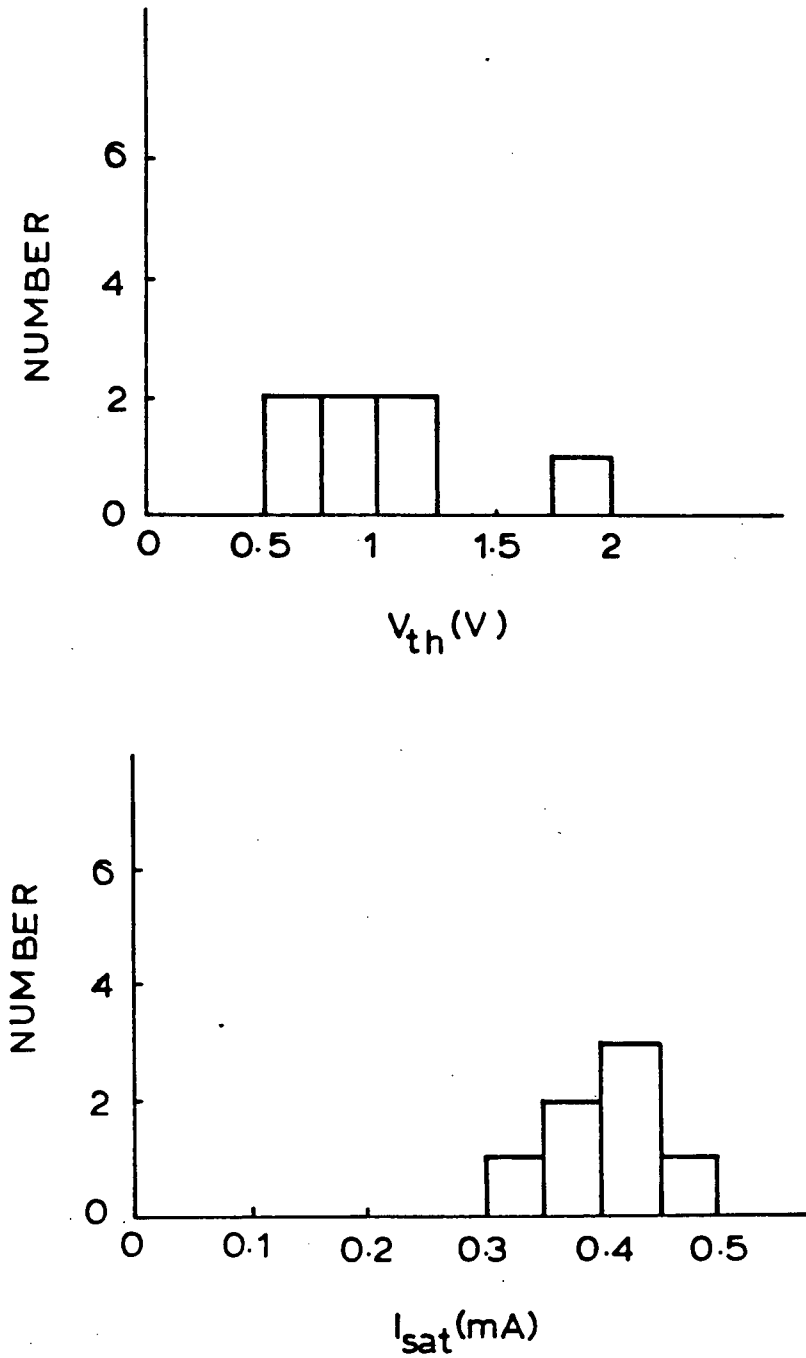


Fig.(4-7) V_{th} and I_{sat} histograms from sample#1.

20% variation in the threshold voltage and up to 35% in the saturation current.

The mobility and carrier concentration profiles are shown in Figs.(4-5) and (4-6) for sample#4 and in Figs.(4-8) and (4-9) for sample#1 respectively. The mobility profile of the sample implanted through Si_3N_4 drops at the interface between the channel and the semi-insulating material (SI) while it rises for the other sample. Jervis et al. [89] have shown that the implantation through Si_3N_4 increased the deep trap concentration. The drop of the mobility profile was correlated to the deep trap, at the channel SI material interface [90] which confirm the results of [89] as well as the idea that the implantation through Si_3N_4 may be responsible for giving low quality devices.

Immorlica et al. [90] have shown that devices with low drift mobility in the active layer-substrate interface exhibit substantial backgating, slow pulse response of drain current to applied gate voltage (lag effect), and premature saturation of output power. Tang et al. [91] have studied the backgating of the samples used in this study. Similar results to that of [90] have been found.

Implantation through Si_3N_4 also shifts the carrier concentration peak closer to the surface which may lead to higher ideality factors, higher saturation current and lower barrier height for the gate contact [2] due to the increase of the carrier concentration. It will also lead to a higher gate capacitance due to the reduction in the depletion region thickness for the same reason. A fat FET from sample#1 with $V_{th} = -1.1$ V has a C_{gs} value at $V_{gs} = 0$ of about 30 pf compared to 19.7 pf for sample#4 fat FET transistor

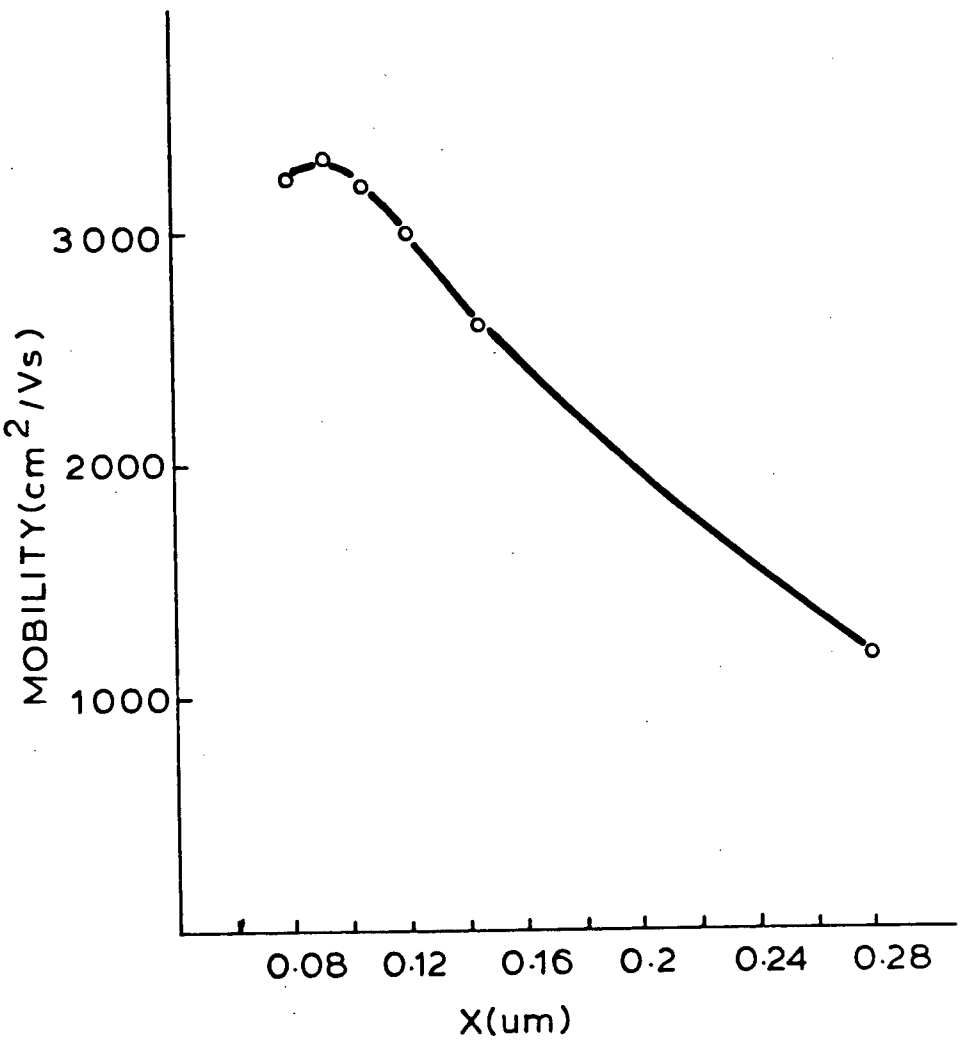


Fig.(4-8) Mobility profile for sample#1.

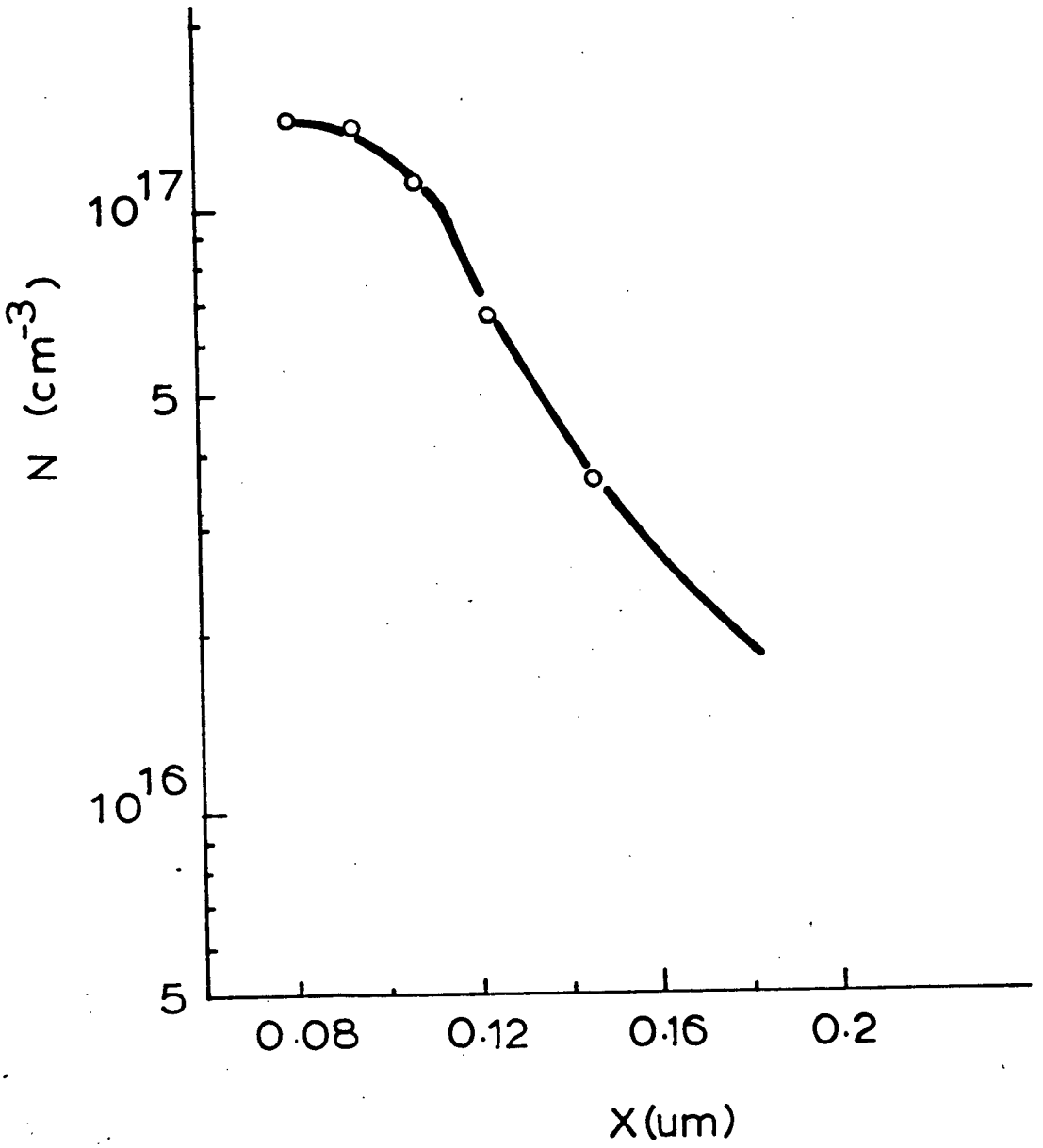


Fig.(4-9) Electron concentration profile for sample#1.

with V_{th} = -1.38 which is about 50% higher. Smaller depletion region thickness leads also to lower breakdown voltage.

4-2 Temperature Measurements

The temperature dependence of MESFET characteristics is clearly important in practice and also gives information of fundamental significance for the understanding of device operation. Temperature measurements were carried out in our laboratory on a fat FET transistor from sample#1. The range of measurement was from -80°C to +80°C. The implanted dose and energy used for sample#1 are listed in Table(3-1). The fabrication process is described in a previous section of this chapter. The gate length (L_g) and width (W_g) of the fat FET are 120 and 180 μm respectively.

The square law relation of $\sqrt{I_{ds}}$ vs. V_{gs} was plotted over the temperature range using the HP 4145A semiconductor parameter analyzer. From this relation both V_{th} and I_{sat} were determined. It was found that V_{th} increased with temperature (Fig.(4-10)), which agrees with the results obtained by others [55]. A 17% change in V_{th} was observed over the range used in the experiment. The saturation current increased also with temperature as shown in Fig.(4-11). The increase of V_{th} and I_{sat} with temperature can be attributed to the reduction in the depletion region width at both the Schottky and SI channel junctions [55] which means an increase in the effective channel thickness.

The values of β were then determined from the relation

$$I_{sat} = \beta(V_{gs} - V_{th} - I_{sat} \cdot R_s)^2 \qquad (4\text{-}17)$$

β was found to decrease with temperature, Fig.(4-12). A reduction of about 15% was observed over the temperature range. Lee et al. [55] observed a 30%

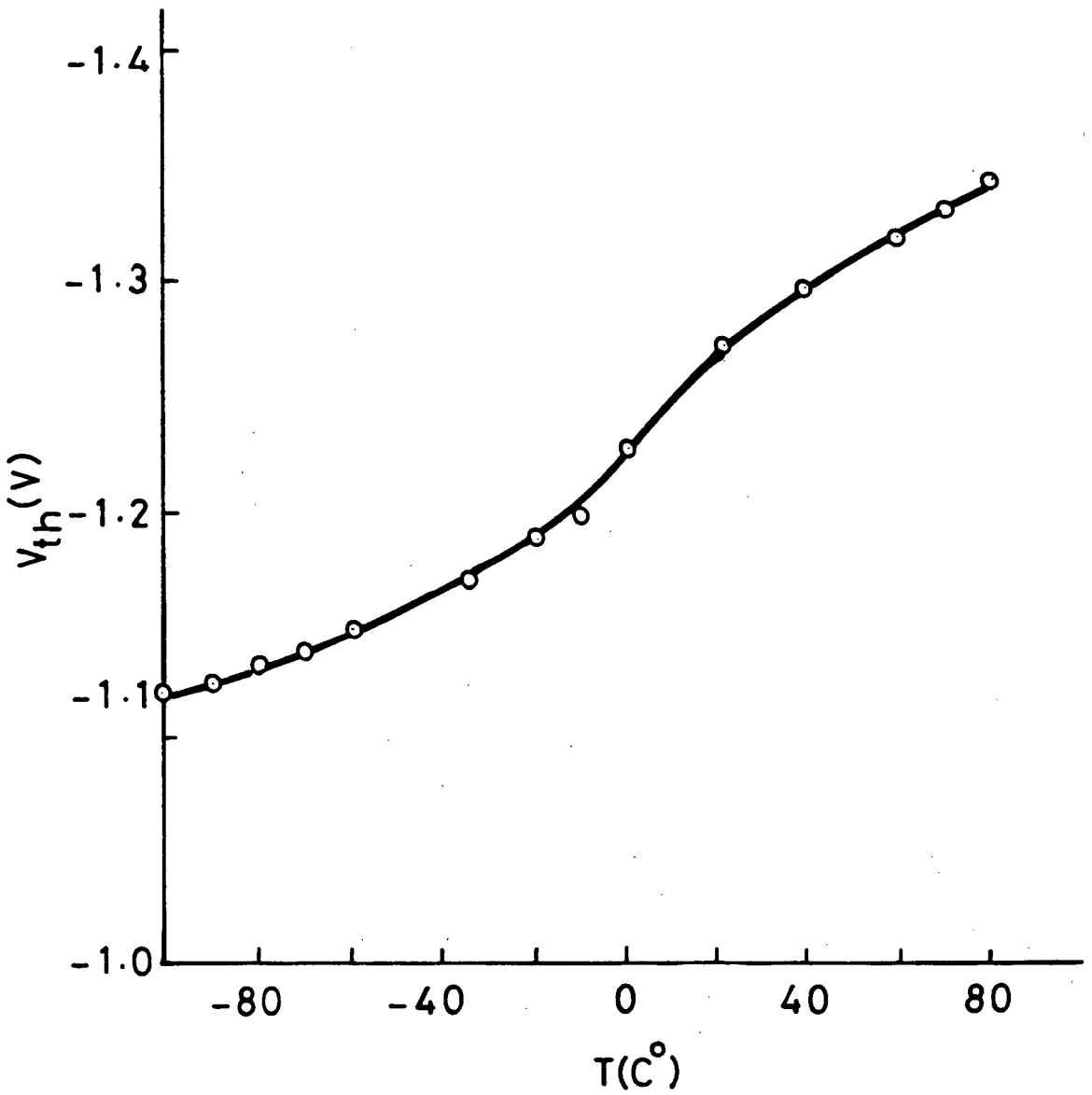


Fig.(4-10) Plot of V_{th} vs. T.

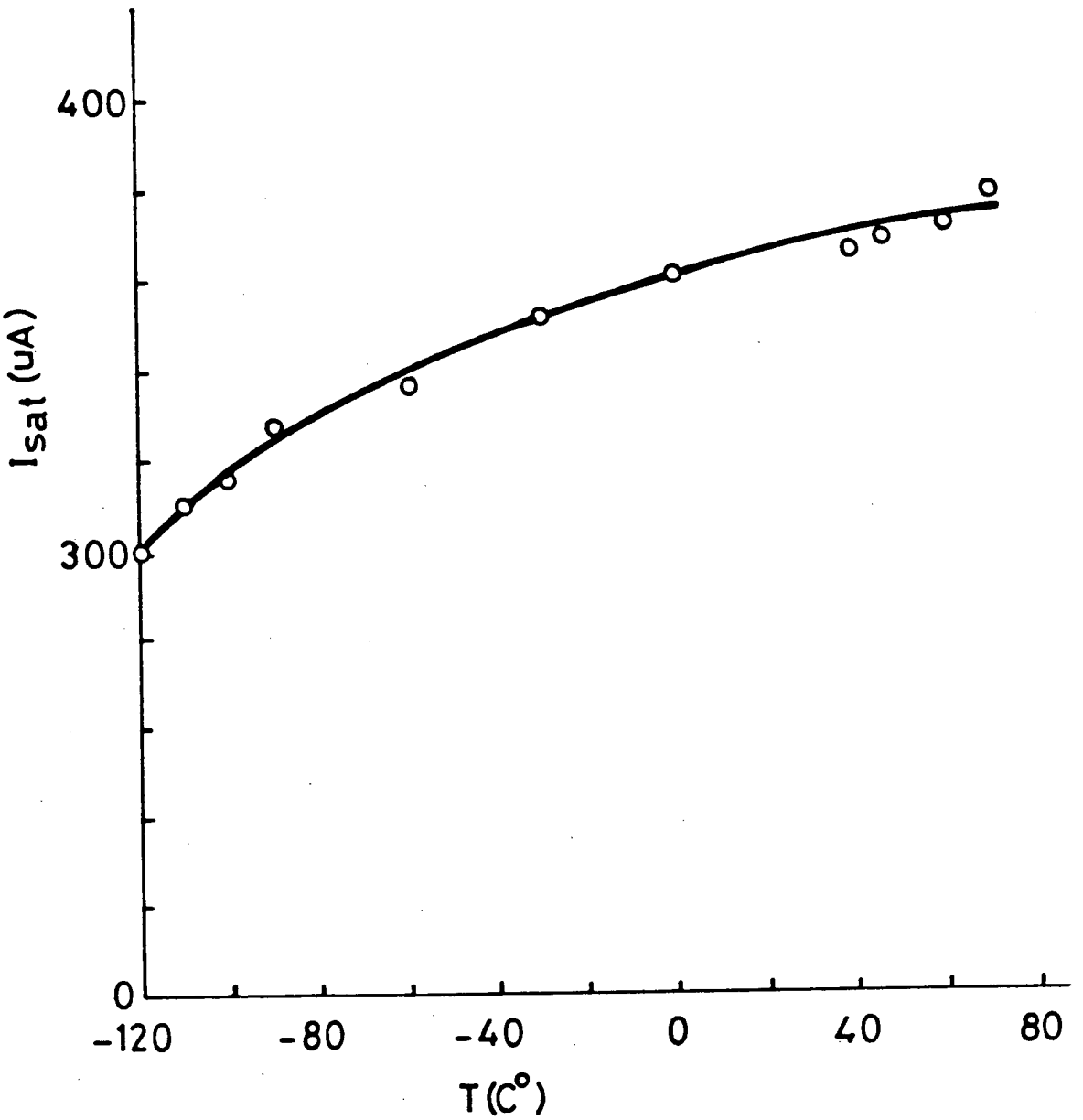


Fig.(4-11) Plot of I_{sat} vs. T.

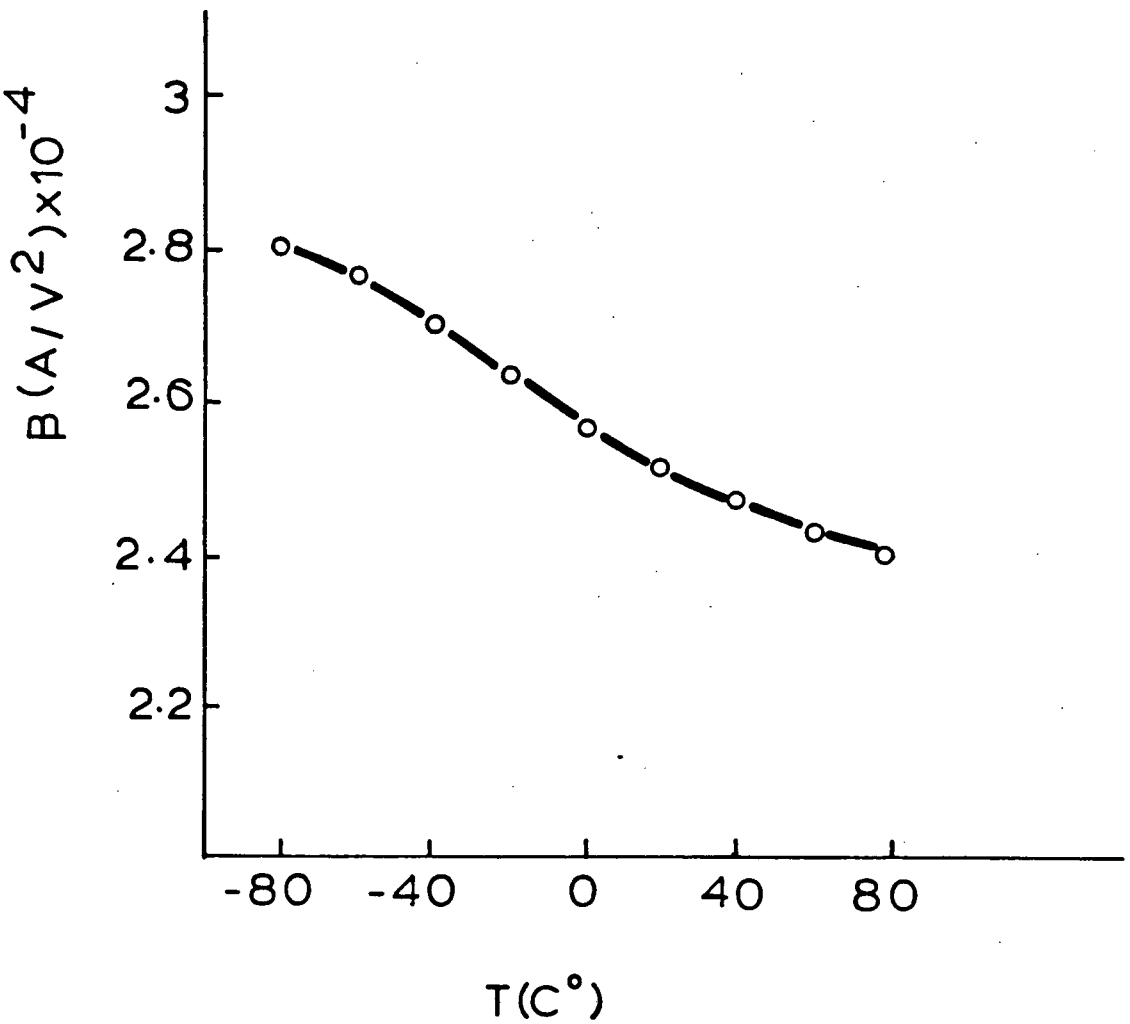


Fig.(4-12) Plot of β vs. T.

decrease in the value of β with temperature over a range from -50°C to 100°C for a 1 μm gate transistor. They attributed the reduction in β to the increase of the effective channel thickness a* and the reduction of the mobility where [9]

$$\beta = W_g \varepsilon \mu / 2 L_g a^* \tag{4-18}$$

The device transconductance g_m and channel conductance g_d were also measured. In the saturation region at $V_{th} = 0$, it was found that g_m showed less sensitivity to temperature, only about 2% change being observed. The theoretical calculations from the relation

$$g_m = 2\beta(V_{gs} - V_{th} - I_{sat} \cdot R_s)/[1 + 2\beta(V_{gs} - V_{th} - I_{sat} \cdot R_s)R_s] \tag{4-19}$$

agree with the experimental results as shown in Fig.(4-13). From the above relation one can see that the two terms of the numerator (2β and (0 - V - $I_{sat} \cdot R_s$)) vary by nearly the same percentage in opposite directions resulting in a constant value over the temperature range. With a denominator nearly equal to unity, g_m is expected to be constant over this temperature range.

In contrast, g_d showed large sensitivity to temperature; a 20% variation was observed, Fig.(4-14). The calculations from the simple model of g_d which is

$$g_d = 2\beta(v_{gs} - V_{th})/[1 + 2\beta(V_{gs} - V_{th})(R_s + R_d)] \tag{4-20}$$

were plotted, Fig.(4-14), and found to be not in very good agreement with the experimental results especially at low temperatures. All the measurements in the linear region such as g_m and the total conductance G did not match exactly the simple theoretical models.

The Schottky contact saturation current I_s was measured over the

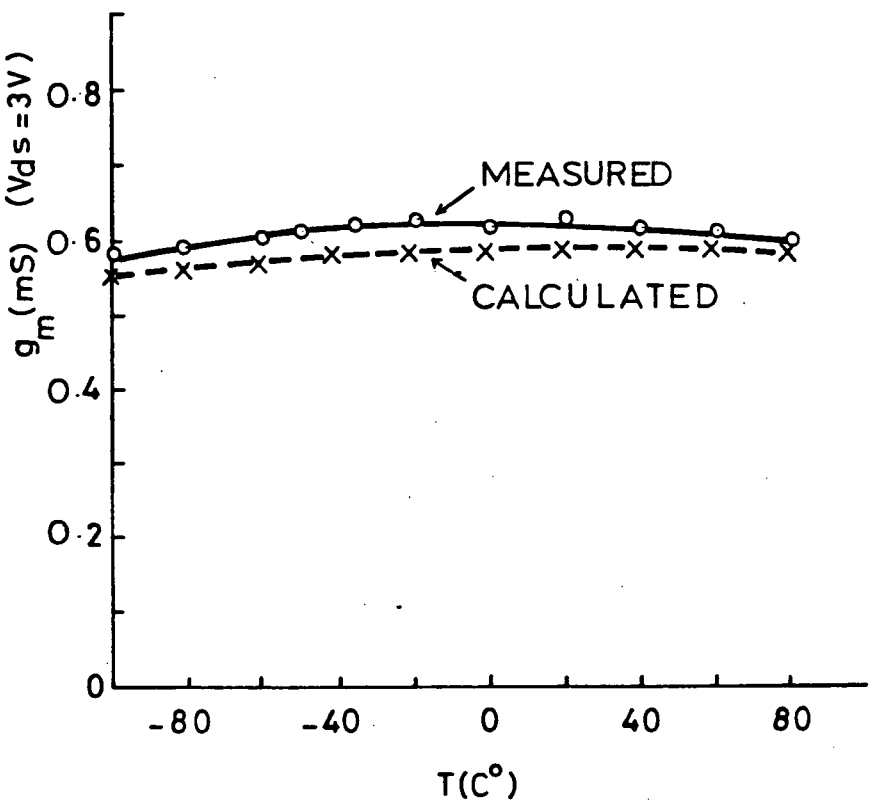


Fig.(4-13) Plot of g_m (at V_{gs}=0 and V_{ds}=3 V) vs. T.

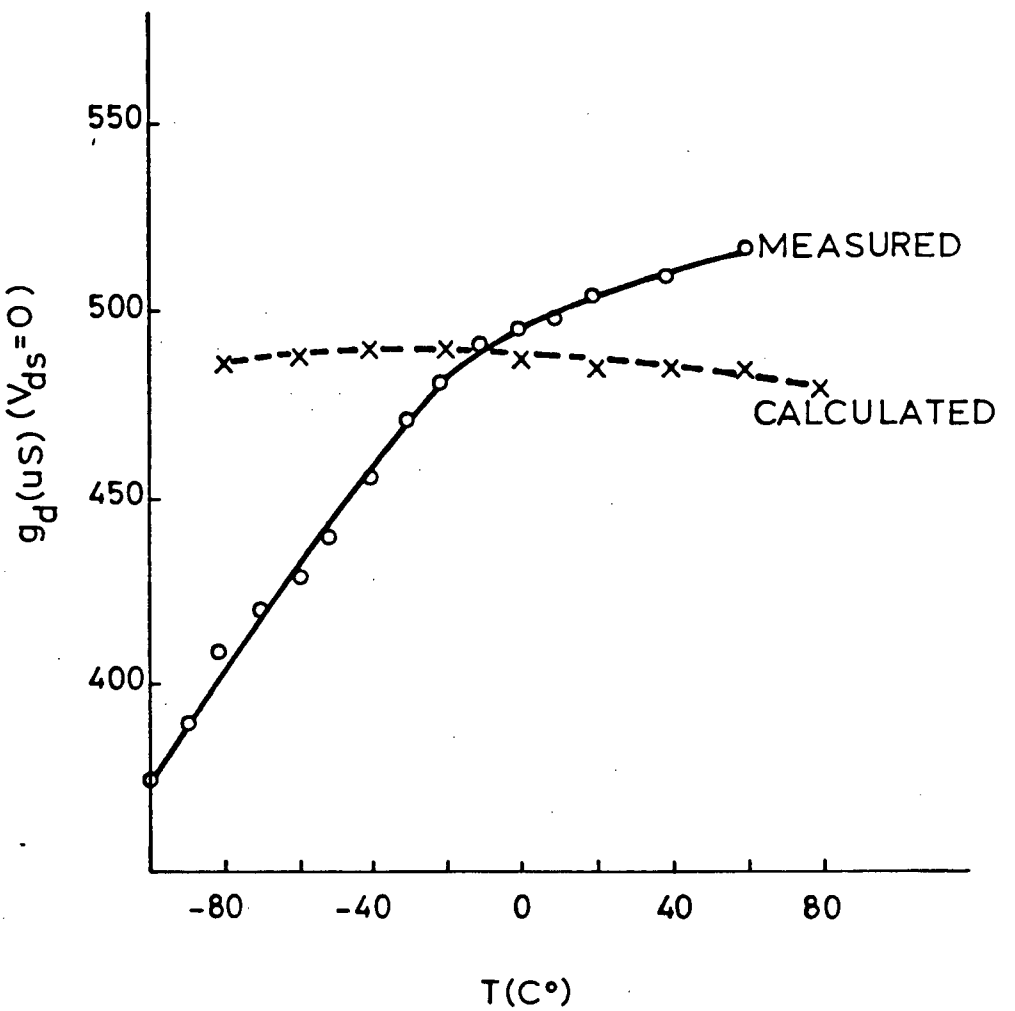


Fig.(4-14) Plot of g_d (at V_{gs}=0 and V_{ds}=0 V) vs. T.

temperature range. It was found to increase with temperature as shown in Fig.(4-15). This increase can be attributed to the decrease of the depletion region width with temperature. It can also be explained from the relation

$$J_s = A^{**} \cdot T^2 \exp(-g\phi_{bn}/kT) \qquad (4\text{-}21)$$

where T^2 is the dominant temperature term.

The ideality factor n was calculated from the relation (3-2). This calculation shows that n decreases with the increase of temperature, as shown in Fig.(4-16). The behaviour of n can be attributed to the effect of the term 1/T in the relation (4-2) where it is the dominant temperature term. The variation of n with temperature agrees with that reported in [2] for Au-Si contacts.

The barrier height ϕ_{bn}, calculated from relation (4-3), has shown an increase with temperature of about 30% over the temperature range, Fig.(4-17). This behaviour is attributed to the effect of the term T in relation (4-3).

The gate capacitance, and both the transconductance g_m and the total conductance G at V_{ds} = 0.05 V were measured to calculate the channel mobility and the carrier concentration profile. The gate capacitance at V_{gs} = 0.0V was plotted against the temperature as shown in Fig.(4-18). The figure shows that C_g increases with temperature which can be attributed to the reduction of the depletion region width W_d where

$$C_g = \varepsilon A/W_d \qquad (4\text{-}23)$$

g_m and G in the linear region are plotted in Figs.(4-19) and (4-20) respectively. The calculated values for g_m were obtained from the relation

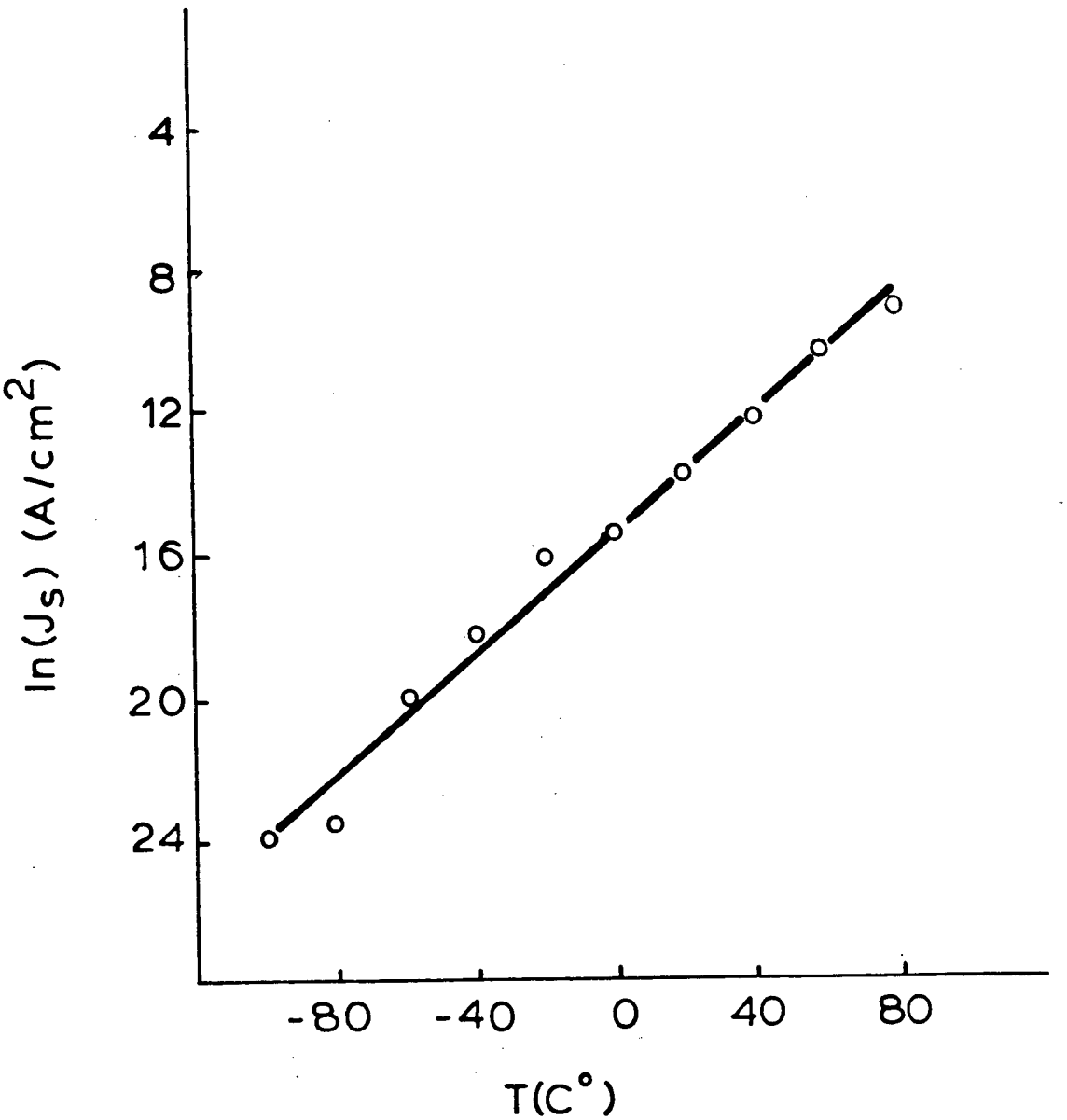


Fig.(4-15) Plot of $\ln(J_s)$ vs. T.

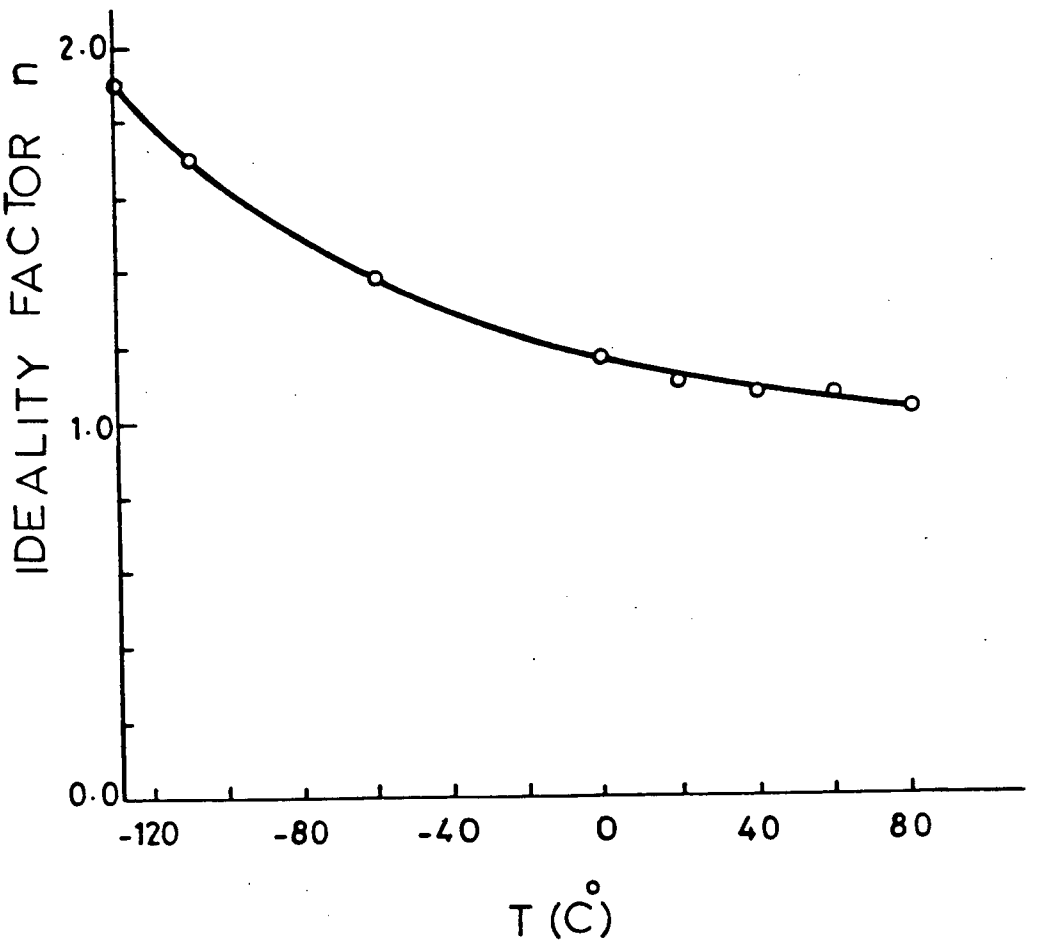


Fig.(4-16) Plot of n vs. T.

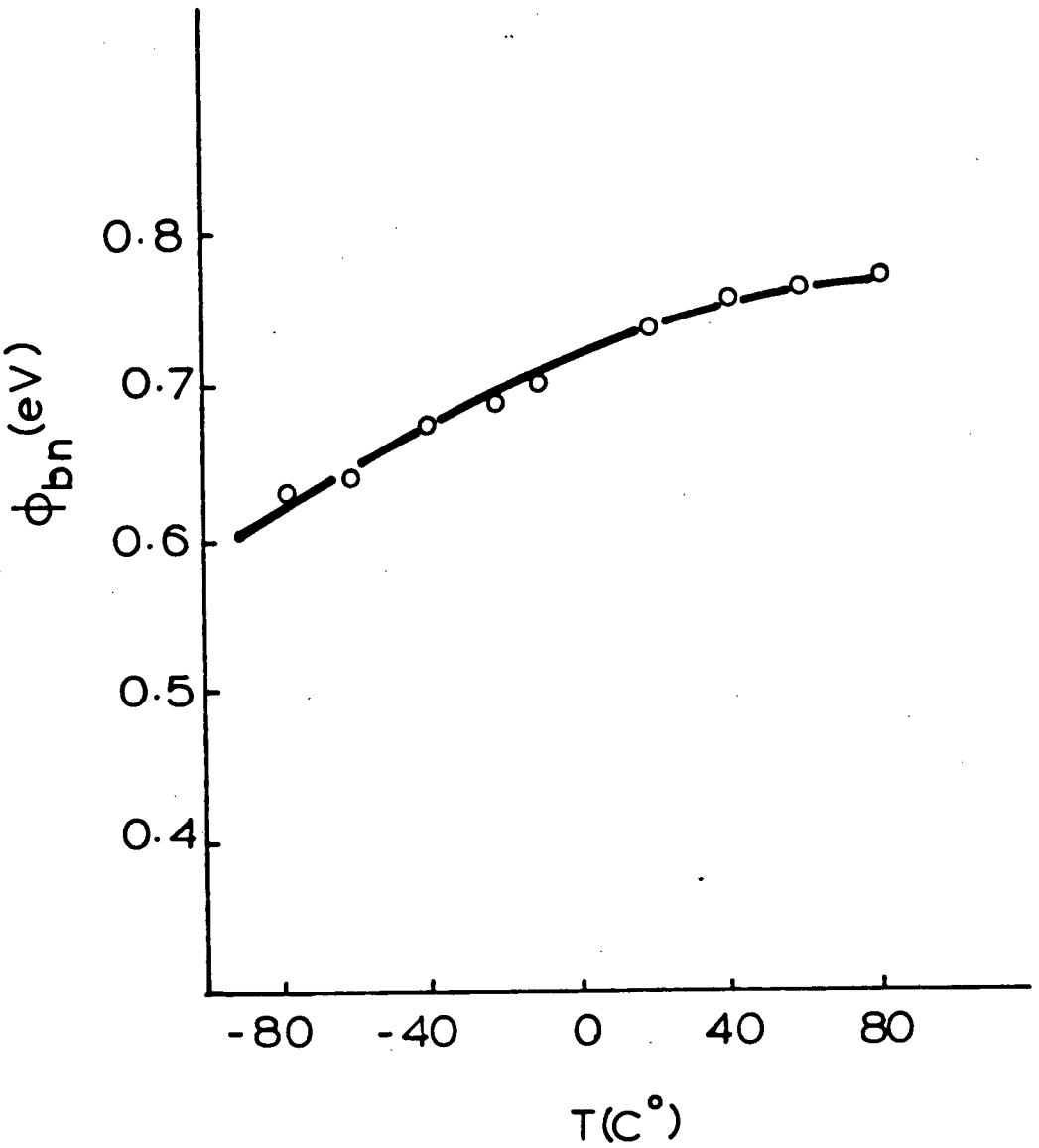


Fig.(4-17) Plot of ϕ_{bn} vs. T.

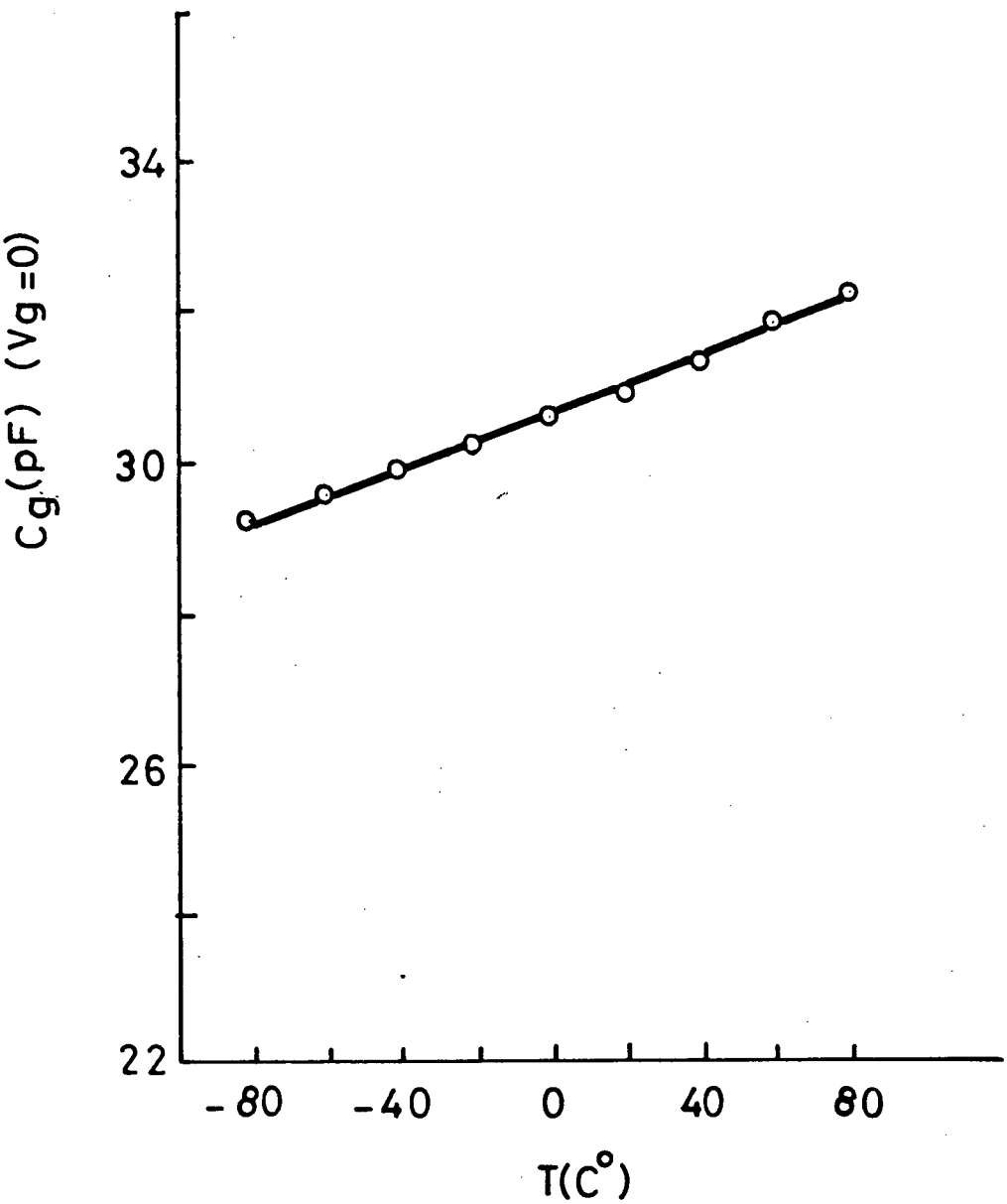


Fig.(4-18) Plot of C_{gs} vs. T.

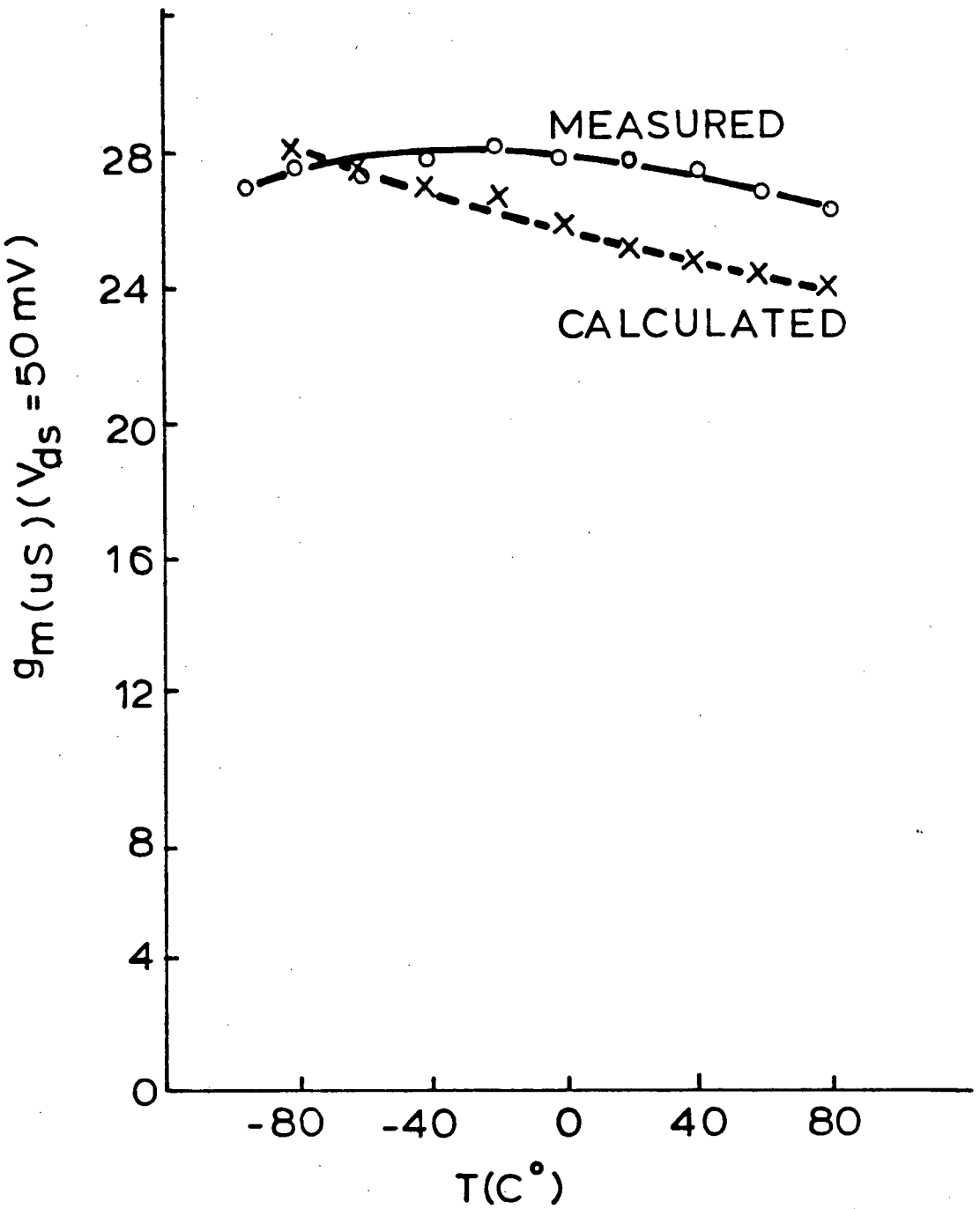


Fig.(4-19) Plot of g_m (at V_{gs}=0 and V_{ds}=0.05 V) vs. T.

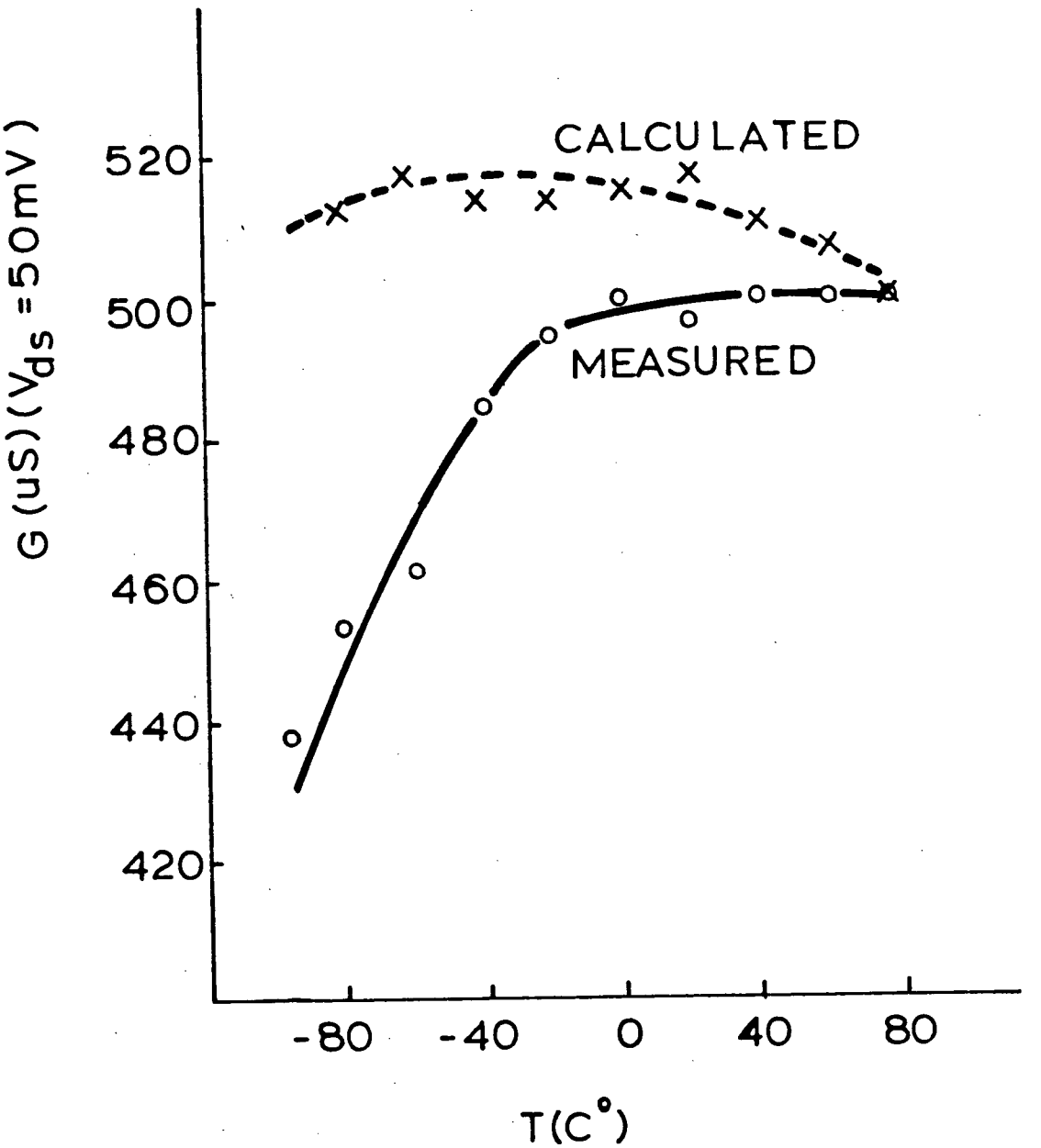


Fig.(4-20) Plot of G (at V_{gs}=0 and V_{ds}=0.05 V) vs. T.

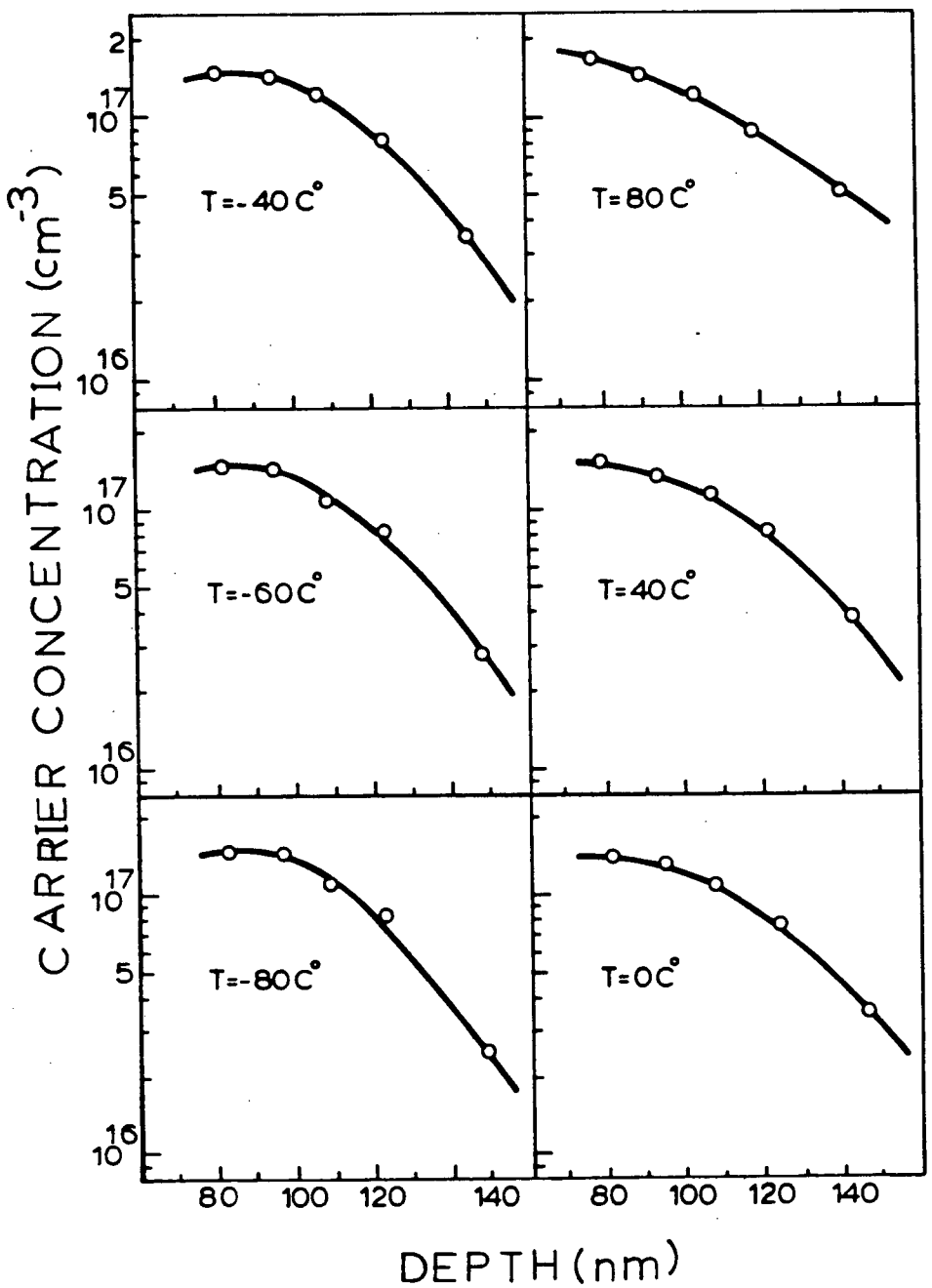


Fig.(4-21) Plot of electron concentration profile vs. T.

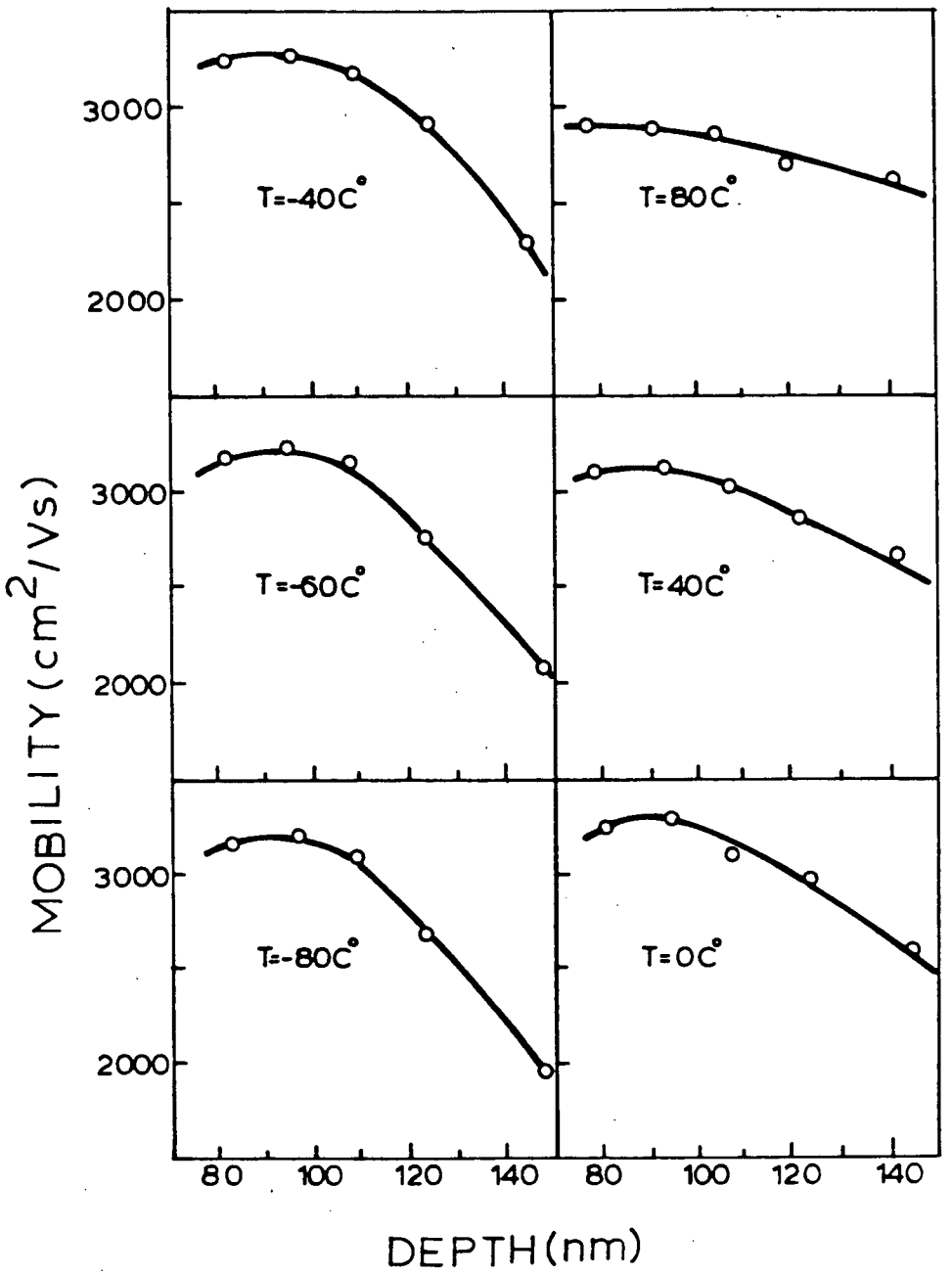


Fig.(4-22) Plot of mobility profile vs. T.

$$g_m = dI_{ds}/dV_{gs} = 2\beta V_{ds} \quad (4\text{-}24)$$

and G from the relation

$$G = I_{ds}/V_{ds} = 2\beta[(V_{gs} - V_{th}) - V_{ds}/2] \quad (4\text{-}25$$

Mobility and carrier concentration profiles were calculated from relations (4-12), (4-13) and (4-14). The carrier concentration profiles at different temperatures, shown in Fig.(4-21), are nearly identical except at the interface between the channel and the SI material. The mobility falls radically at the active layer SI material interface due to the high concentration of the deep trap levels in this region (see section 4-1). However, at the temperature of the maximum emission rate from the trap centres, the mobility goes up at the interface (or does not fall down very radically) due to the emission of carriers from these centres [56]. In our case, the maximum emission rate has been found at 80°C [57]. Therefore, the carrier concentration density did not drop radically at the interface at 80°C.

The mobility profiles, Fig.(4-22), show that at the channel SI material interface the mobility decreases except at 80°C due also to the emission or carriers from the trap centres at 80°C [56]. The mobility at 100 nm was measured and plotted in Fig.(4-23). This Figure shows that the mobility increases with temperature to a maximum at 0°C, then decreases again. The same behaviour has been observed by others [56].

The depletion region width W_d, at V_{gs} = 0 V, was calculated from the relation (4-14). W_d was observed to decrease with temperature, Fig.(4-24), due to the decrease of the built-in potential V_{bi} [55] as shown from the relation

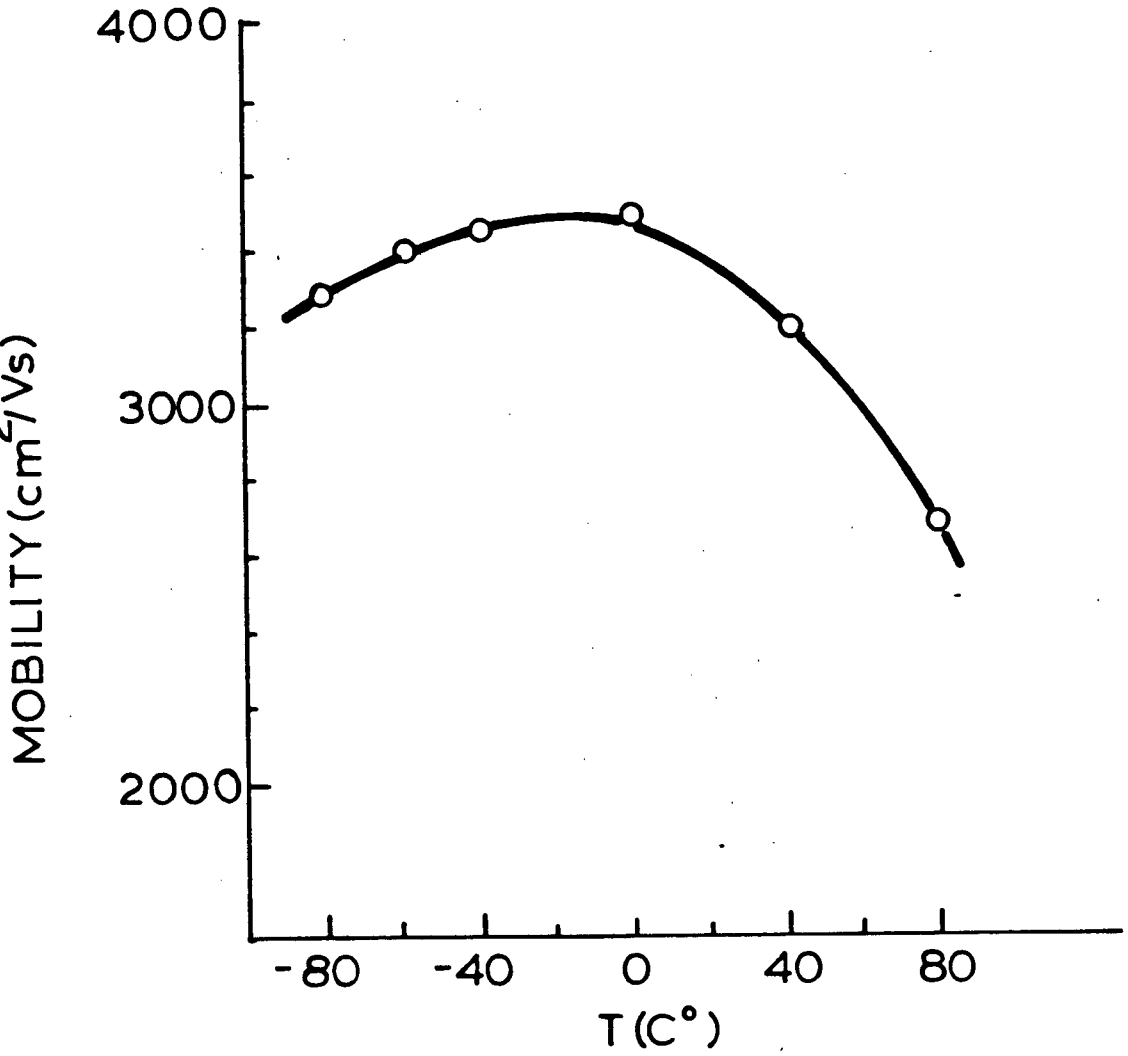


Fig.(4-23) Plot of the mobility at 100 nm vs. T.

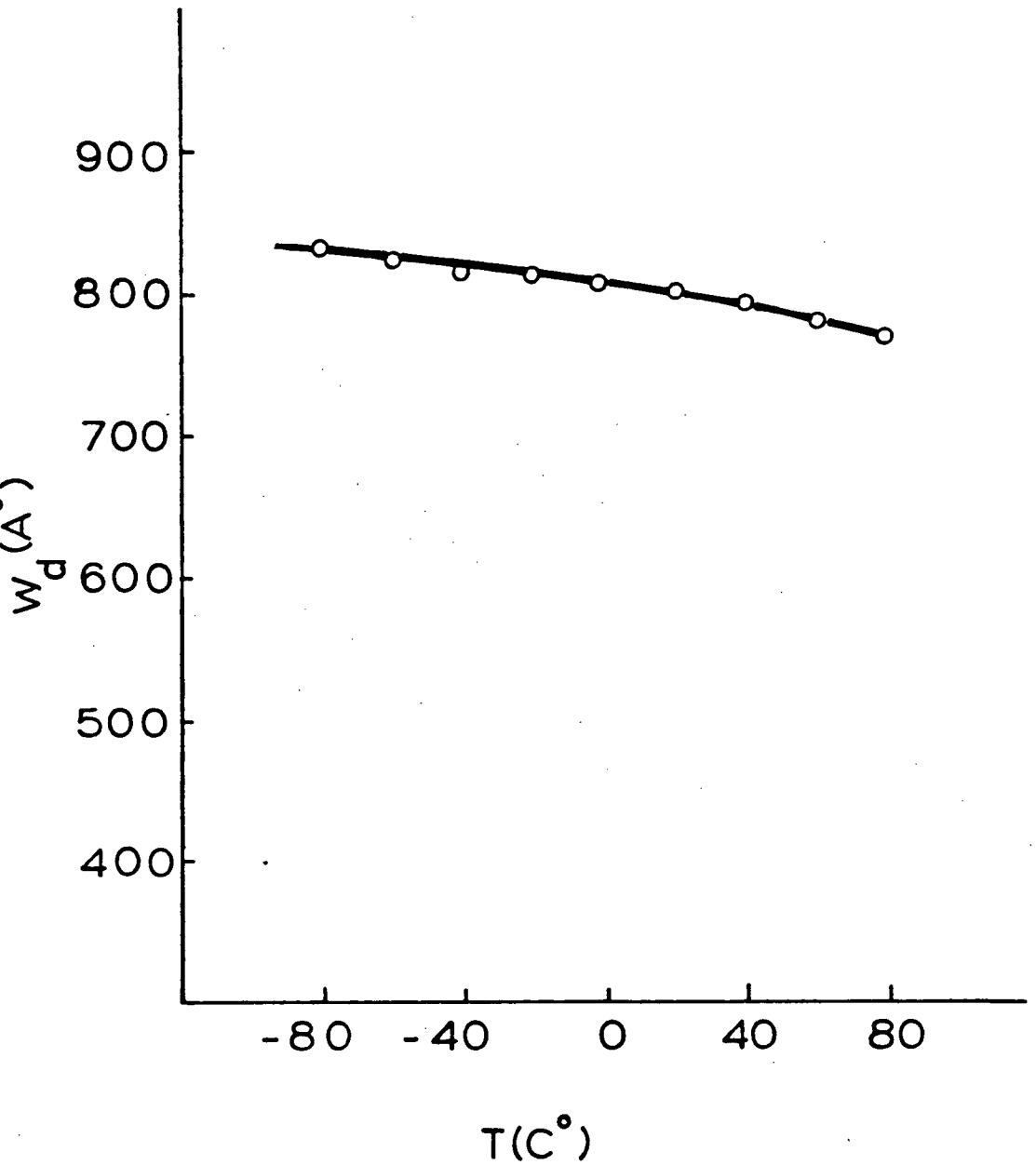


Fig.(4-24) Plot of W_d vs. T.

$$W_d = \sqrt{(2\varepsilon(V_{bi} - 2kT/q)/qN_D)} \qquad (4\text{-}26)$$

The time delay for an inverter can be expressed as [3]

$$\tau_d = 4C_L/3\beta V_m \qquad (4\text{-}27)$$

where C_L is the load capacitance and $V_m = V_{gs} - V_{th}$. From relation (2-10), relation (4-27) leads to

$$\tau_d = 2C_L/3g_m \qquad (4\text{-}28)$$

Since g_m is nearly constant within the temperature range from -80°C to 80°C and C_L is expected to vary by about 9% only, Fig(4-18), τ_d is expected to be nearly constant within the same range.

CHAPTER(5)

COMMON DRAIN FET LOGIC

5-1 Review of GaAs Digital Logic Approaches

In the first section of this chapter, previous GaAs logic approaches are reviewed. In the second section, my new Common Drain FET Logic is discussed.

During the past ten years many approaches have been developed for GaAs digital circuits. They can be classified into three groups:
(a) depletion mode FET logic in which only depletion type MESFETs are used,
(b) enhancement mode FET logic in which enhancement type MESFETs are used as switching transistors, and
(c) quasi-normally-off logic in which transistors with a slightly positive or slightly negative or zero threshold voltage can be used.

(a) Depletion Mode FET Logic

(i) The buffered FET Logic (BFL)

BFL was the first GaAs logic approach to be developed [1]. The logic (as shown in Fig.(5-1.a)) consists of two stages: the logic amplifier stage and the load driver/level shifter stage. The load driver stage is used to shift the output voltage levels of the logic amplifier to the same values of the input voltage levels in order to be able to drive the next stage. Van Tuyl et al. [1] have used a threshold voltage of -2.5 volts and low and high logic levels of -2.5 and 0.5 volts respectively.

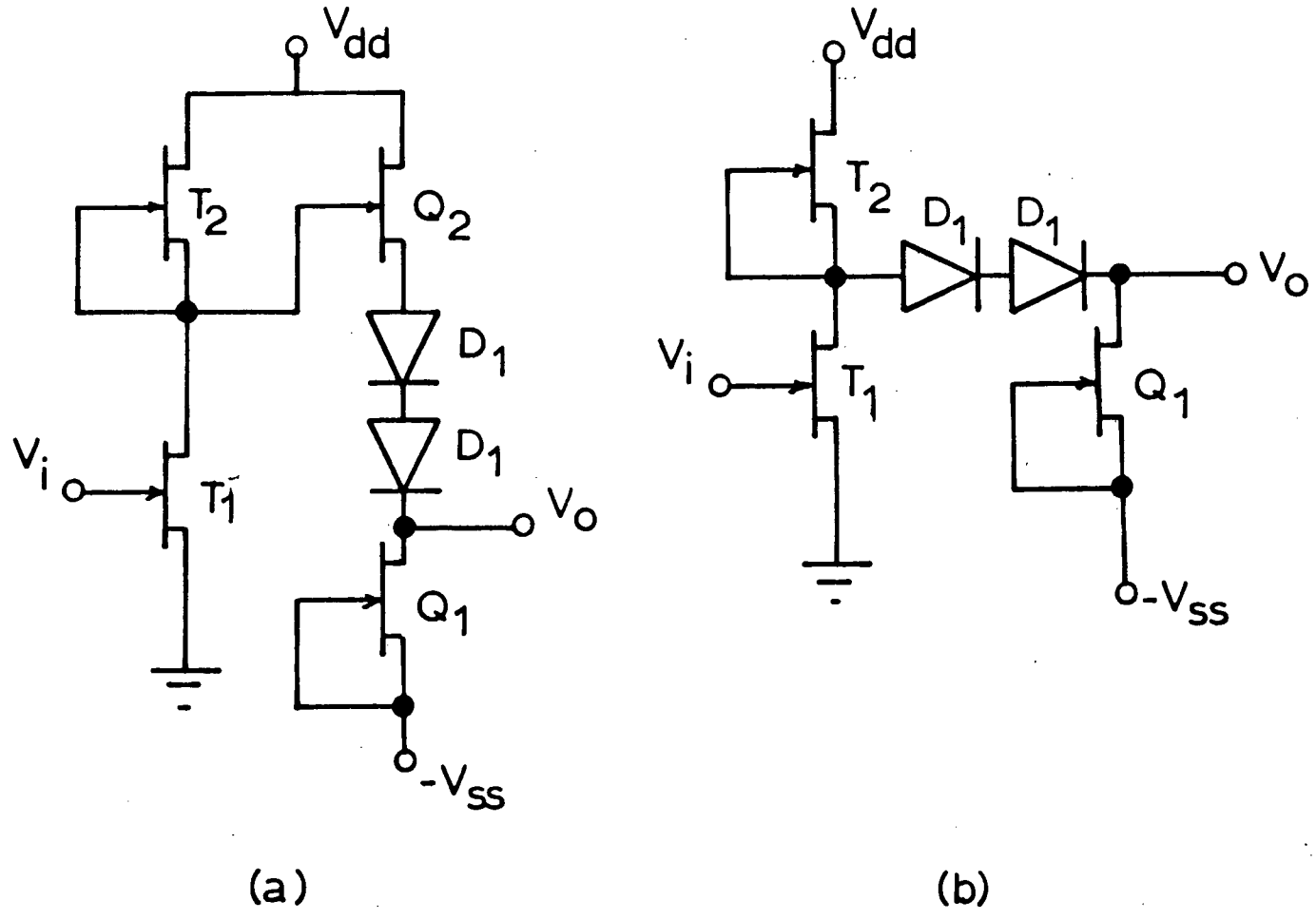


Fig.(5-1) Schematic diagram of (a) BFL inverter and (b) UFL inverter.

The main advantages of this approach are:

(a) operation at high speeds;

(b) insensitivity to the pinch-off voltage.

However, it suffers from serious problems:

(a) high power consumption;

(b) low integration density capability due to the use of a large number of elements with large dimensions.

The power dissipation of the BFL can be reduced either by reducing the threshold voltage or by eliminating the load driver source follower transistor as shown in Fig.(5-1.b) [58]. The new structure is called the Unbuffered FET Logic (UFL). The reduction of the power dissipation in both cases will be at the expense of the speed.

Perea et al. [59] have reported a Programmable Logic Array (PLA) using the BFL where they were able to achieve a maximum clocking frequency of 2.2 GHz at 8 mW/gate. Yamamoto et al. [60] have succeeded in fabricating an FM demodulator using this logic with a speed of operation 20 times that of silicon devices.

(ii) Schottky Diode FET Logic (SDFL)

Rockwell researchers developed the Schottky Diode FET logic in 1977 [61]. This logic, as shown in Fig.(5-2), shifts the level of the signal at the input by using two types of diodes. The switching diodes (D1), which form the NOR structure when used in parallel, and the shifting diodes (D2) which are used to shift the input levels. Low doses of implantation were used for the switching diodes to provide better switching capability while

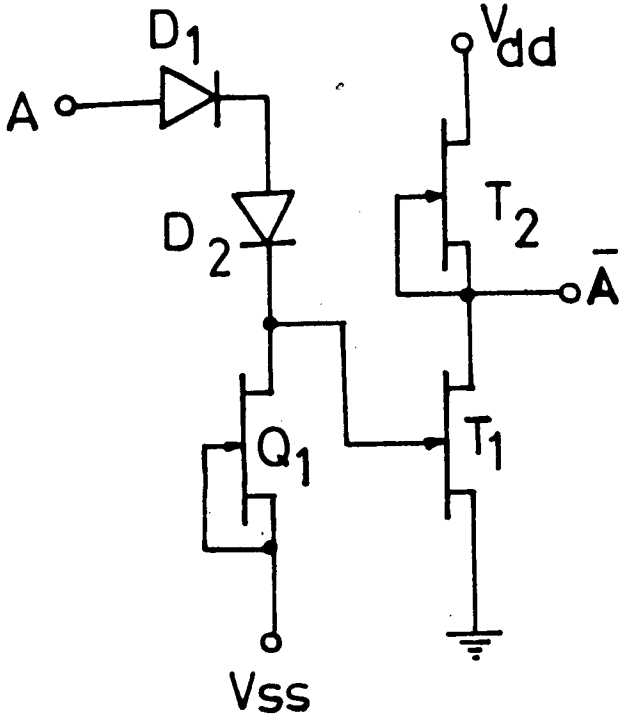


Fig.(5-2) Schematic diagram of the SDFL inverter.

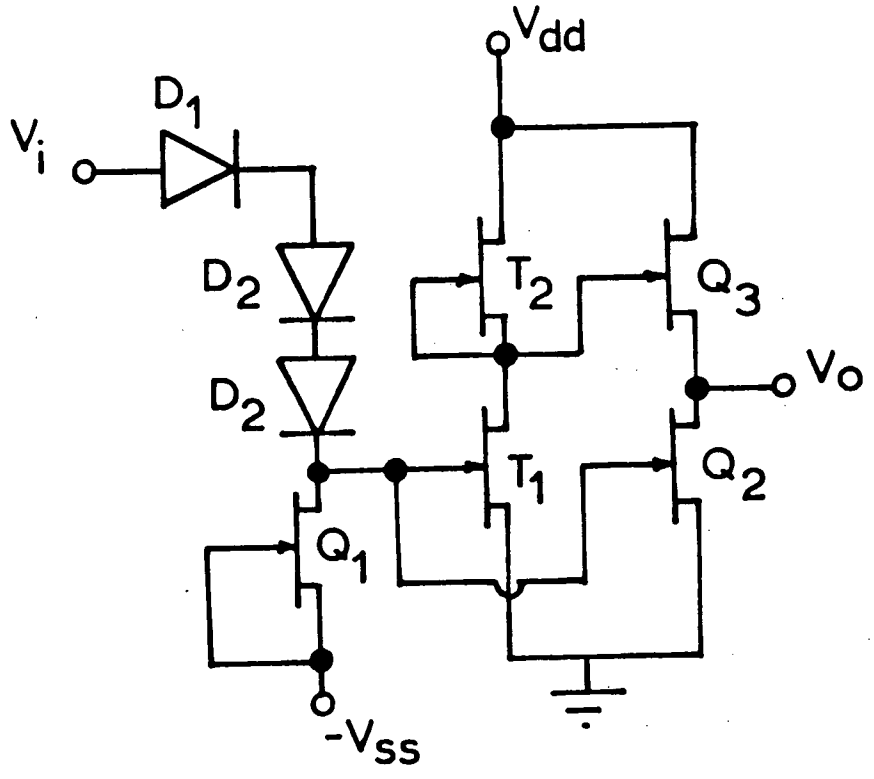


Fig.(5-3) Schematic diagram of the SDFL inverter with pull pull buffer.

higher doses were used for the shifting diodes to make them able to carry large currents with an almost constant voltage drop. To reduce the occupied area/gate, the switching and the shifting diodes were made very small, 1×2 μm^2 and 3×3 μm^2 respectively.

The SDFL approach has two advantages with respect to BFL:

(a) it occupies a smaller area per gate;

(b) it dissipates lower power

However, it suffers from these problems:

(a) difficulties in fabricating the small diodes [62];

(b) poor fan-out capability because a very large current is required to be driven into the input of the next stage.

The most serious problem that faces the SDFL approach is (b) that it restricts the fan-out to 1 which leads to the use of a large number of gates to implement a circuit. The other alternative is the use of a load transistor with large width to be able to supply the required current. In both cases, the logic will dissipate a large amount of power and occupy a large area.

Eden et al. [3] have reported 60ps and 1.1mW/gate for a SDFL NOR gate with a switching transistor gate length of 1μm, gate width of 10μm and fan-in/fan-out of 2/1. More complex circuits have been fabricated using the SDFL such as a high speed divider circuit with a maximum clock frequency of about 1.85GHz [63], a 320 gate logic array with 184 ps time delay/gate measured by a 19 stage ring oscillator [64], and a 256 bit RAM with access time of 1ns and 267mW power consumption [65].

(iii) SDFL with Push Pull Buffer

This approach was developed at Honeywell [66] to reduce the fan-out sensitivity of the SDFL by adding a push pull amplifier at the output as shown in Fig.(5-3). Almost constant gate delay of 100ps/gate was obtained for fan-outs of 1 to 3 when this buffer was used. Using this logic, Vu et al. [67] have fabricated a Schottky gate array with three options: unbuffered NOR gates, buffered NOR gates, and dual NOR/NAND gates. The yield of this chip was 70% for a 101 stage ring oscillator. The main problem with this approach is the high power dissipated and the large area occupied per gate compared to the original SDFL.

(iv) Capacitor Coupled Logic (CCL)

Livingstone et al. [68] have developed the CCL approach, Fig.(5-4), where a coupling capacitor is used to shift the signal levels at the input. The mechanism of the level shifting using the coupling capacitor has been described by Livingstone [69] as follows. When node A is high (=Vdd), node B is clamped by the forward biased gate current of transistor T1 to about 0.5 V, and the capacitor (or the reverse biased diode) is charged through T2 of the previous stage to about 4.5 V when using 5 V supply. When node A moves to its low logic level a portion of the capacitor voltage is retained, taking node B to a negative voltage, beyond pinch-off, turning the next stage OFF. When node A goes back to the high level, node B returns back to its high level value (0.5 V) causing the transistor to turn ON.

The coupling capacitor can be replaced by a reverse biased Schottky diode which is preferable since it requires the same fabrication steps as used for the MESFETs. The coupling capacitor Schottky diode size should be

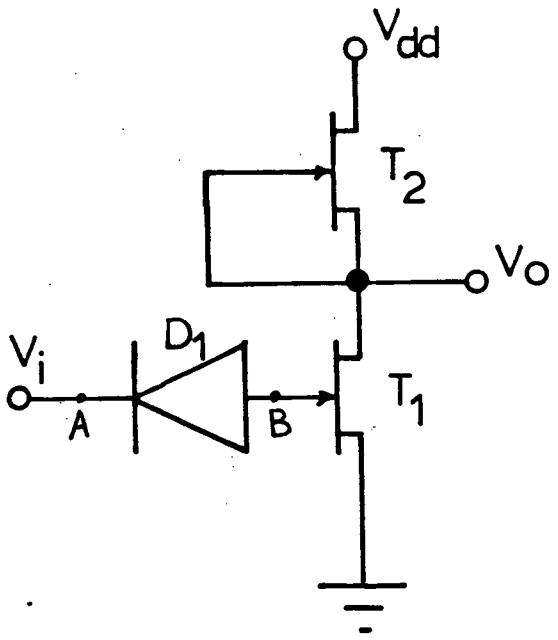


Fig.(5-4) Schematic diagram of the CCL inverter.

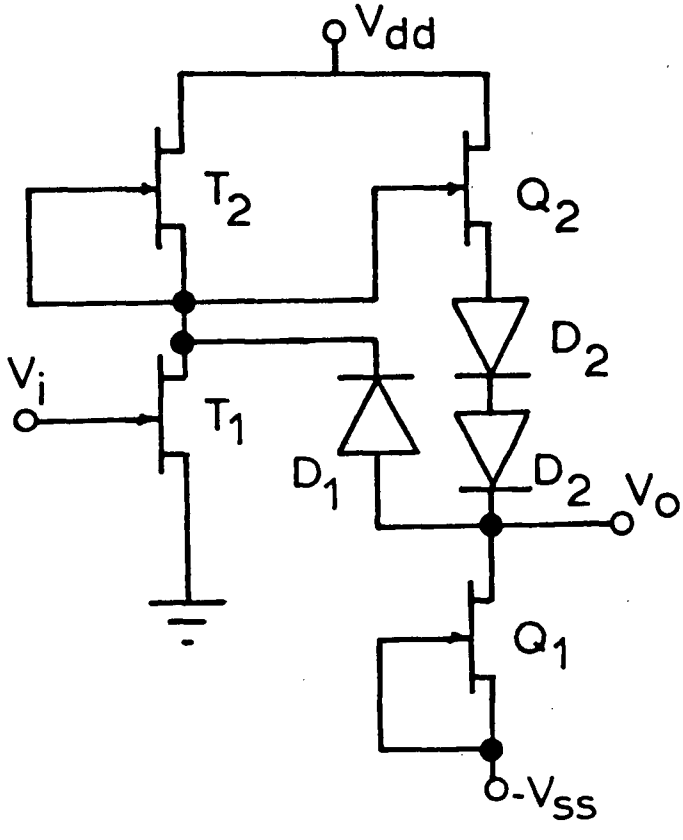


Fig.(5-5) Schematic diagram of the FFS inverter.

large enough to be able to drive the next logic stage [69]. And this, in turn, leads to the occupation of a large area/gate.

The main disadvantage of this logic lies in its inability to operate at frequencies less than 20 kHz. Livingstone et al. [68] have shown that the capacitor coupling mechanism for shifting the levels does not work at low frequencies due to the leakage current of the coupling capacitor and the following gate. They have shown also that the logic needs to be initialized before proper operation can be proceeded. A time delay of 105 ps per gate for the CCL has been reported [70].

(v) Feed Forward Static Approach (FFS)

The FFS approach, developed at Texas Instruments [71], is a combination of the BFL and the CCL, as shown in Fig.(5-5). This approach has no low frequency limit, dissipates power equal to that dissipated by the CCL, and has maximum switching frequency equal to that of the BFL. The FFS can operate at a speed 30% higher than that of the BFL with a 30% lower power dissipation [71]. However, this approach occupies large area/gate and dissipates high power (see Chapter(6)). A propagation delay of 59 ps and power dissipation of 18.8 mW per gate for an FFS inverter with transistors of 1μm gate length, 20μm gate width, and unity fan-out have been reported [71].

(b) Enhancement Mode FET Logic

(i) Directly Coupled FET Logic (DCFL)

DCFL uses enhancement mode transistors as switching elements [72]. The load can be an enhancement mode transistor, a depletion mode transistor, a resistor, a tunnel diode, or a saturated resistor [16]. Only a depletion

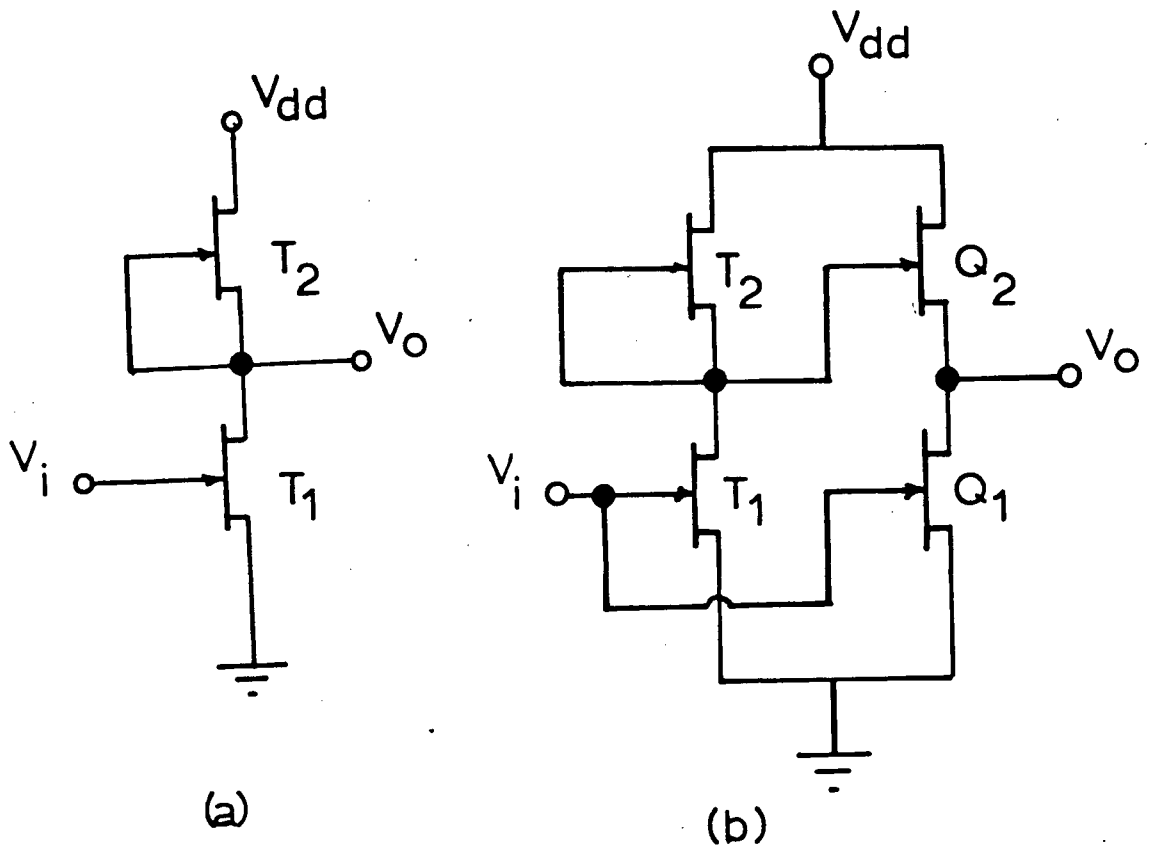


Fig.(5-6) Schematic diagram of (a) DCFL and (b) buffered DCFL.

mode transistor load will be considered in this discussion (Fig.(5-6.a)). The mechanism of operation of the DCFL is similar to that of the Si DCFL. If the input is high (0.7 V), the switching transistor T1 turns ON and the output is shorted to ground. If node A is low (0 V), the transistor T1 turns OFF and the output becomes shorted to Vdd instead. The DCFL is sensitive to the fan-out, therefore the structure of Fig.(5-6.b) was developed to reduce this sensitivity. This structure uses a buffer circuit at the output to provide enough current to switch the next stages within reasonable time.

The advantages of this logic lie in the simplicity of its structure and its extremely low power dissipation which make it very attractive to VLSI applications. However, it suffers from these problems:

(a) the requirement for a tight control on the pinch-off voltage (leading to lower production yield);

(b) high series resistance due to a thin or lightly doped channel;

(c) low voltage swing due to the restriction on the high level voltage to 0.7 V, as discussed in Chapter(2).

This high resistance is one of the reasons for the low to medium speed of operation of this logic. Low voltage swing leads to low speed of operation and high possibility of false triggering.

The pinch-off voltage can be controlled by using the Pt gate or the recessed gate technology while the series resistance can be reduced by using either the self-aligned gate or the Pt gate or the recessed gate technology (see Chapter(2)).

Using a self-aligned gate technique, Kiehl et al. [82] have fabricated a DCFL ring oscillator with 16.1 ps/gate at 77K; the gate length (Lg) was 1 μm

while the gate width was 20 μm. Other researchers have reported similar delay time values using the same fabrication technique [38,39,42].

(c) Quasi-normally-off Approaches

(i) Low Pinch-off FET Logic (LPFL)

The LPFL (Fig.(5-7)) has been developed by Nuzillat et al. [73], primarily to have an approach with low dissipated power and less sensitity to the pinch-off voltage. The advantages of the LPFL over the DCFL can be summarized as [73]:

(a) low logic level, almost equal to the ground potential, is used, and is thus independent of the characteristics of the elements,

(b) no degeneration of the transfer curve with increasing pinch-off voltage,

(c) high logic swing (typically 0.8 V instead of 0.5 V for the DCFL) with slight dependence on Vth, and

(d) smaller shift of the switching voltage (65% of Vth compared to 85% for DCFL).

Six alternative configurations of the LPFL have been proposed, Fig.(5-7). Types 2 and 4 Fig.(5-7.c,f) did not work properly, therefore the authors did not report their logic level values. These two types have been also ignored in recent publications [74-75]. A complete study of the LPFL performance will be presented in Chapter(6).

Comparing the LPFL with the DCFL and the SDFL [74-75], one can see that:

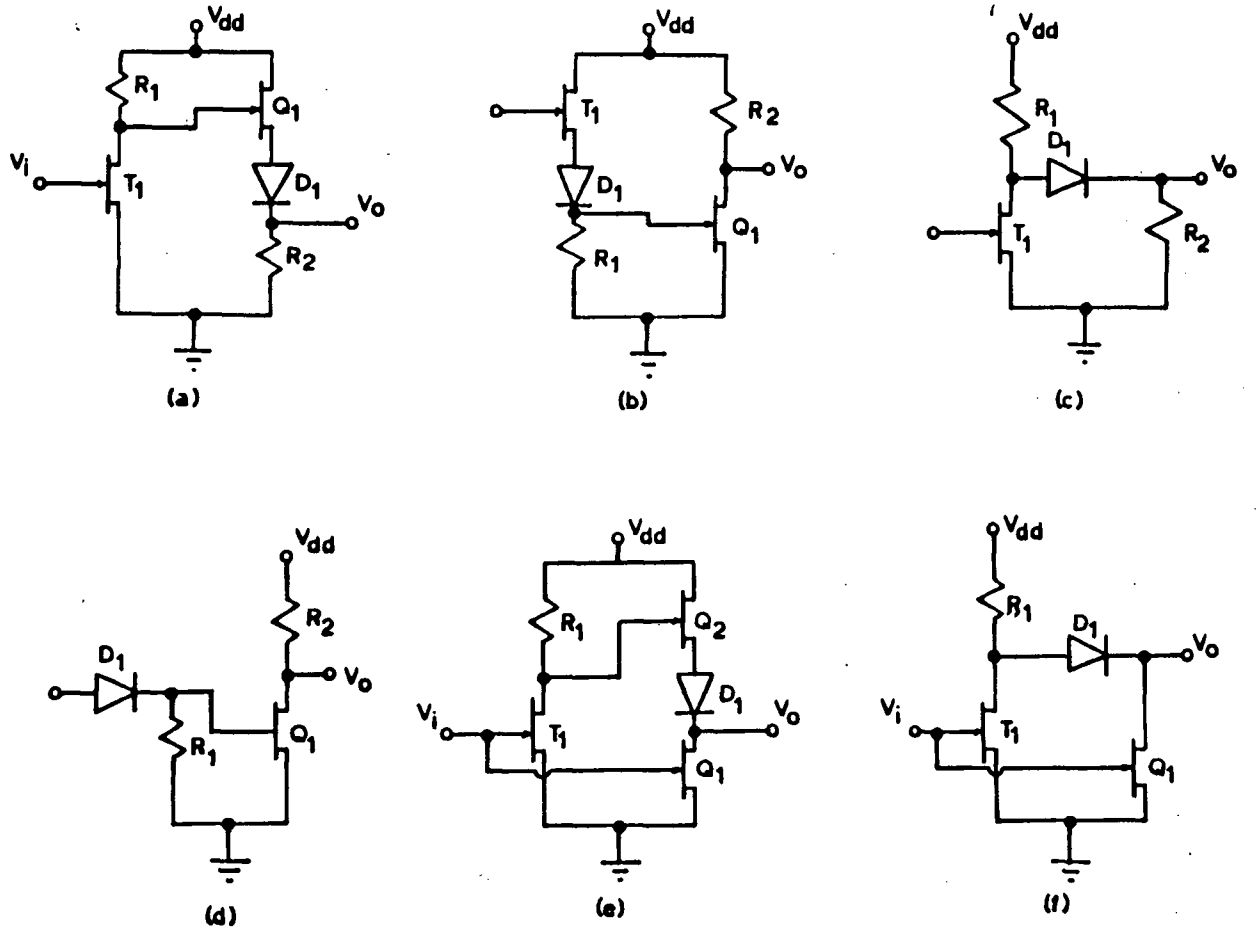


Fig.(5-7) Schematic diagram of the LPFL inverter; types (a) 1-D, (b) 1-I, (c) 2, (d) 3-D, (e) 3-I, and (f) 4.

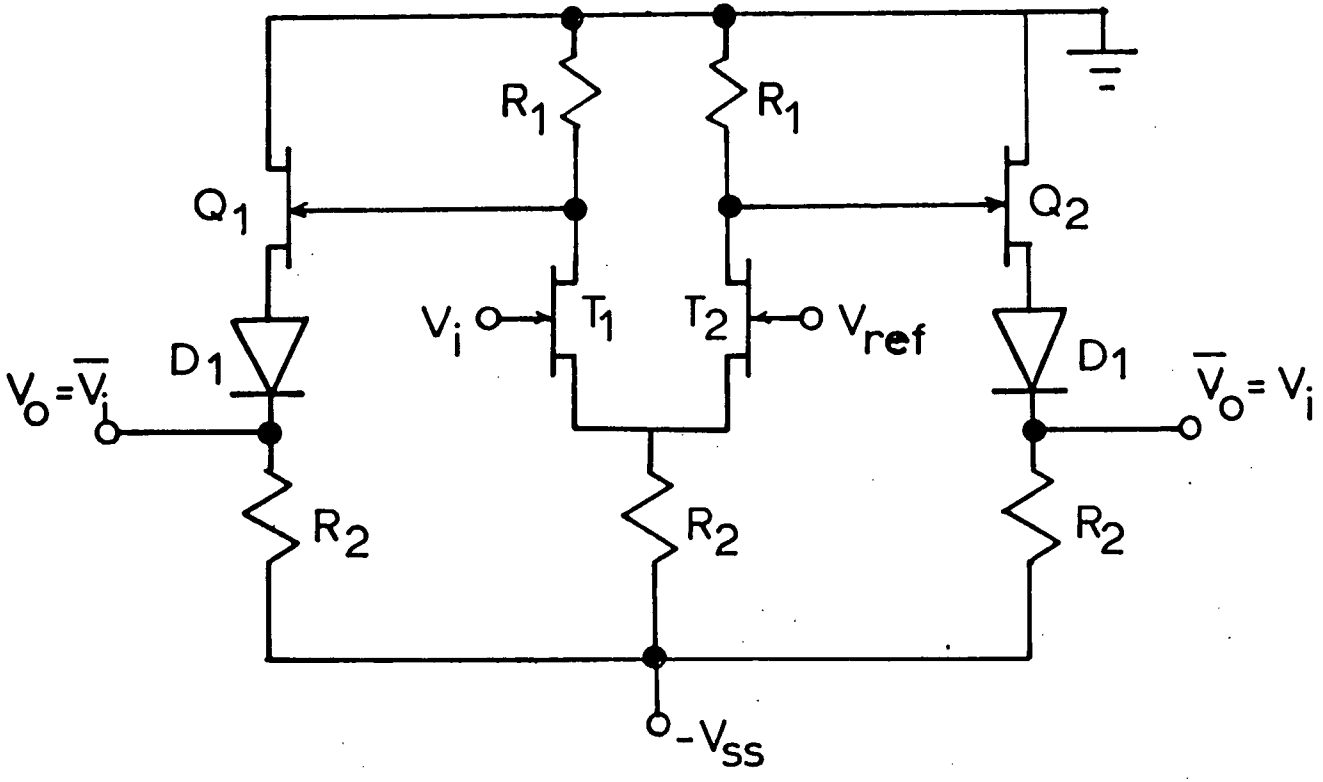


Fig.(5-8) Schematic diagram of the SCFL inverter

(a) LPFL is more complex than DCFL,

(b) it dissipates higher power than DCFL without an equivalent gain in the speed, and

(c) it does not achieve any significant performance improvement over the SDFL, where the SDFL, in addition to the use of depletion mode transistors, can operate at higher frequency for nearly the same power dissipation per gate, integration density, and time delay power product. More than that, LPFL may require the use of small diodes, has high series resistance, and requires a tight pinch-off control (may not be as tight as that required for the DCFL, but not as loose as that can be used for the depletion mode FET logic).

A divider with a maximum toggle frequency of 2.8 GHz at power dissipation equal to 15mW/gate and a 1 kbit RAM with 1.1ns access time and power dissipation of 850mW, have been realized using the LPFL [76].

(ii) Source Coupled FET Logic (SCFL)

The source coupled FET logic (SCFL) has been developed at Matsushita Corporation [77]. The basic SCFL inverter consists of a differential amplifier and two source follower buffers with diode level shifters, as shown in Fig.(5-8). The main advantage of this logic, as reported by Katsu et al. [77], is the insensitivity to the threshold voltage variations. A variation from -0.6 to 0.3 V can be tolerated. This variation is wider than those accepted by the LPFL. Shimano et al. [78] have shown experimentally that V_{th} can vary from -1.0 to 0.2 V without degradation of the performance.

The other major advantage of the SCFL is the ability to operate at very high speeds. Idda et al. [79] have reported a time delay of 25 ps/gate for a MESFET of 1μm gate length and 10μm gate width.

Although this logic has eliminated some of the problems, it has introduced some others which can be summarized as:

(a) the occupation of a very large area per gate,

(b) the dissipation of high power compared to the DCFL and the LPFL, and

(c) the need for up to four power supplies [79].

Comparing the DCFL, the SCFL achieves double the speed but dissipates twice the power, leading to the same power time delay product. While as a comparison to the BFL, one can see that both can work over nearly the same frequency range, dissipate similar amount of power, and are not sensitive to V_{th}.

From the previous discussion, it is noticed that the main problems associated with the use of depletion mode transistors are the occupation of a large area, the dissipation of high power, and the necessity for using very big diodes (in case of CCL and FFS) or very small diodes (as in the case of SDFL and SDFL with push pull buffer).

On the other hand, the use of the normally and quasi-normally off transistors leads to logic approaches which may require a tight control on the threshold voltage, be sensitive to the loading (as in case of the DCFL), have a complex system (as in the case of the SCFL and the LPFL), have low voltage swing (as in the case of the DCFL and the LPFL), and use small diodes or occupy very large area.

Therefore, the development of a new logic which can provide high yield, high speed, low power dissipation, and high integration density is required. The Common Drain FET Logic (CDFL) approach was developed in our laboratory in order to attempt to meet these previous requirements.

5-2 The Common Drain FET Logic (CDFL)

The new logic, presented here, uses transistors with drain connected to the positive supply voltage, V_{dd}; the source is allowed to swing. Two basic circuits were developed. The first is the buffer circuit and is shown in Fig.(5-9.a). It has two transistors; the switching transistor which is a common drain transistor and the load transistor with the gate tied to the source. Because the input of the buffer appears at the output without inversion, an AND or an OR gate can be built using this circuit, as shown in Fig.(5-9.b,c). The buffer circuit is similar to the isolating buffer described by Hartgring et al. [80].

The common drain transistor characteristics can be derived from that of the common source transistor (where the source voltage V_{gs} is constant [3]). For the common source transistor, we may approximate the drain source current by

$$I_{ds} = 2\beta[(V_{gs} - V_{th})V_{ds} - V^2_{ds}/2] \qquad (5\text{-}1)$$

below saturation where

$$V_{ds} < V_{gs} - V_{th} \qquad (5\text{-}2)$$

and,

$$I_{ds} = \beta(V_{gs} - V_{th})^2 \qquad (5\text{-}3)$$

at saturation, where

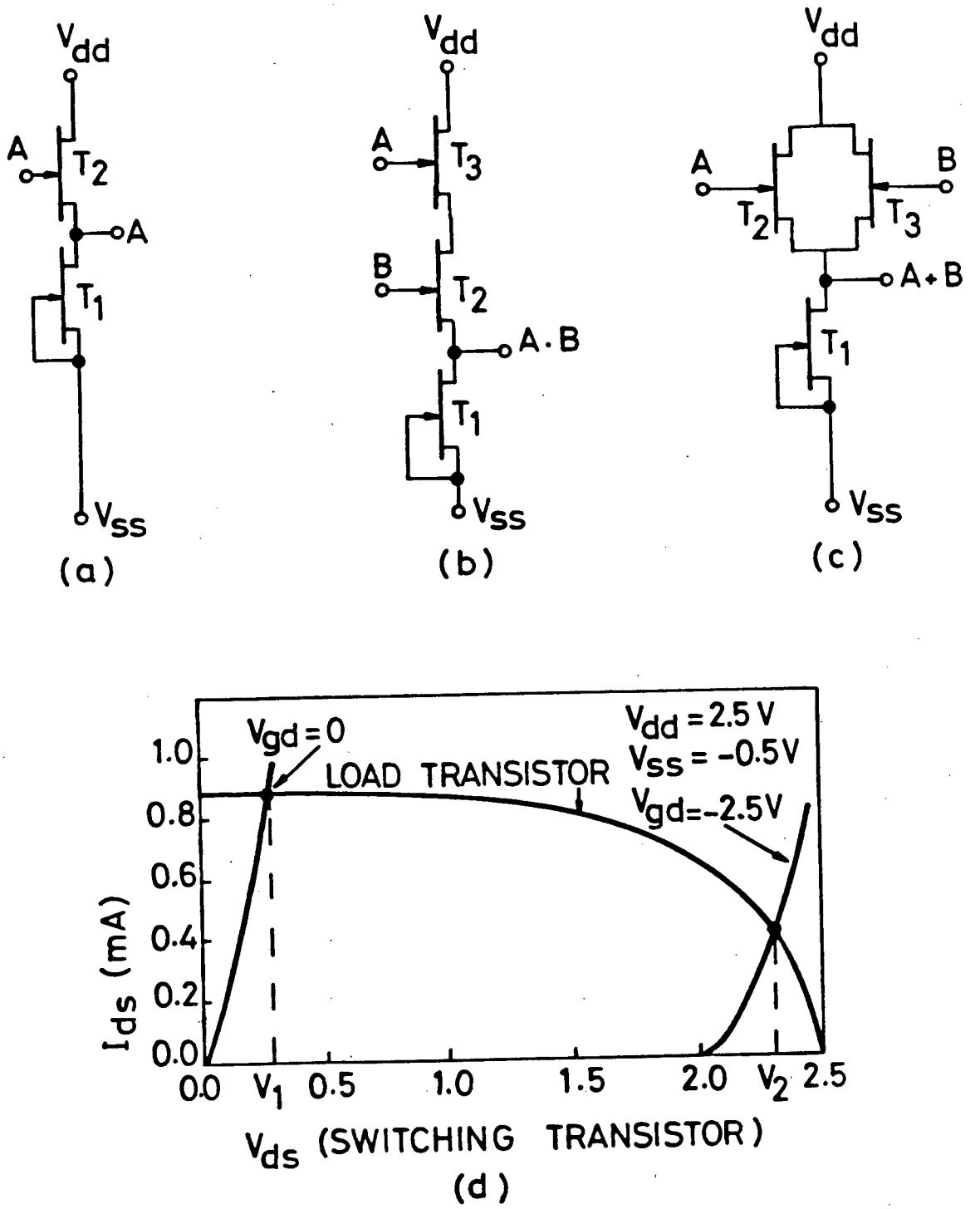


Fig.(5-9) Schematic diagram of the CDFL (a) buffer circuit, (b) AND gate, and (c) OR gate; (d) I-V characteristics of the buffer circuit.

$$V_{ds} > V_{gs} - V_{th} \tag{5-4}$$

The I-V characteristic of common drain transistors can be derived by substituting the relation

$$V_{gs} = V_{gd} + V_{ds} \tag{5-5}$$

in relation (5-1).

The common drain transistor turns ON if

$$V_{gd} > |V_{th}| \tag{5-6}$$

and the drain current will be

$$I_{ds} = 2\beta[(V_{gd} - V_{th})V_{ds} + V^2_{ds}/2] \tag{5-7}$$

The transistor will be considered OFF if

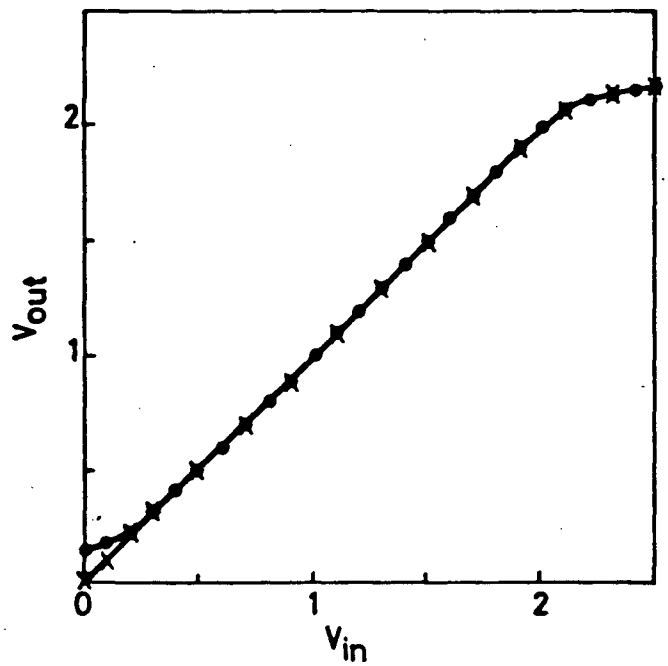
$$V_{gd} < |V_{th}| \tag{5-8}$$

and the corresponding drain current will be in this case equal to

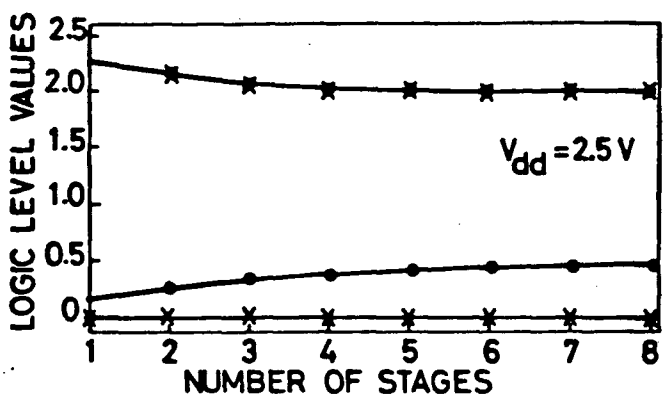
$$I_{ds} = \beta[V_{ds} - (V_{th} - V_{gd})]^2 \tag{5-9}$$

The relation between I_{ds} and V_{ds} for the buffer circuit is shown in Fig.(5-9.d). The intersections of the load curve with the two curves, drawn from equation (5-7) and (5-9), give the 1 and 0 states of the logic.

Computer simulation for the buffer circuit (Appendix(A)) was done using the JFET model of the SPICE.2G program [14]. The simulated transfer characteristic is shown in Fig.(5-10.a). The simulation shows that, for identical switching and load transistors, the voltage gain ($G_M = -dV_o/dV_i$) is equal to 1 in the range $V_{th} < V_{in} < V_{dd} - V_{th}$ approximately. The simulation of 8 successive stages of the buffer, shown in Fig.(5-10.b), shows that the 0 and 1 levels saturate to approximately V_{th} and $V_{dd} - V_{th}$ respectively which



(a)



(b)

Fig.(5-10) (a) Transfer characteristics of the buffer and (b) output of 8 successive stages of buffer circuits; (....)V_{ss}=0 and (xxxx)V_{ss}=-0.5 V.

agrees with the results obtained from the transfer characteristic. The 0 level will saturate at 0 V if a negative bias is used instead of the ground potential (Fig.(5-10.a)).

The result shown in the previous paragraph is valid only if the slope is exactly equal to 1 which may be hard to satisfy practically. If G_m is not equal to 1, the logic levels might be lost after a certain number of stages. Therefore, an inverter with a voltage gain greater than unity was required to regenerate the original values of the logic levels and to build the negative logic. The proposed inverter, shown in Fig.(5-11.a), has two stages; the input stage for shifting the logic levels from V_{dd} and 0 V to 0 V and $-V_{th}$, and the output stage for inverting the signal.

The advantage of this inverter are:

(a) the use of only depletion mode transistors;

(b) the use of a resistor for level shifting instead of diodes.

The advantage of using resistors are:

(i) shifting capability can be changed without a change in its size because the resistance value can be determined using the implantation parameters;

(ii) it is easy to fabricate because no restrictions on the size are imposed and less fabrication steps are required (no Schottky contacts are needed).

In contrast, the level shifting capability of the diode varies with the variation of its size, therefore, smaller diodes ($1\times2\mu m^2$ in the case of the SDFL) should be used if the shifting capability is required to increase without an increase in the number of diodes. These very small diodes have very low yield. On the other hand, if high yield with the same shifting capability is required, a large number of diodes with large sizes must be

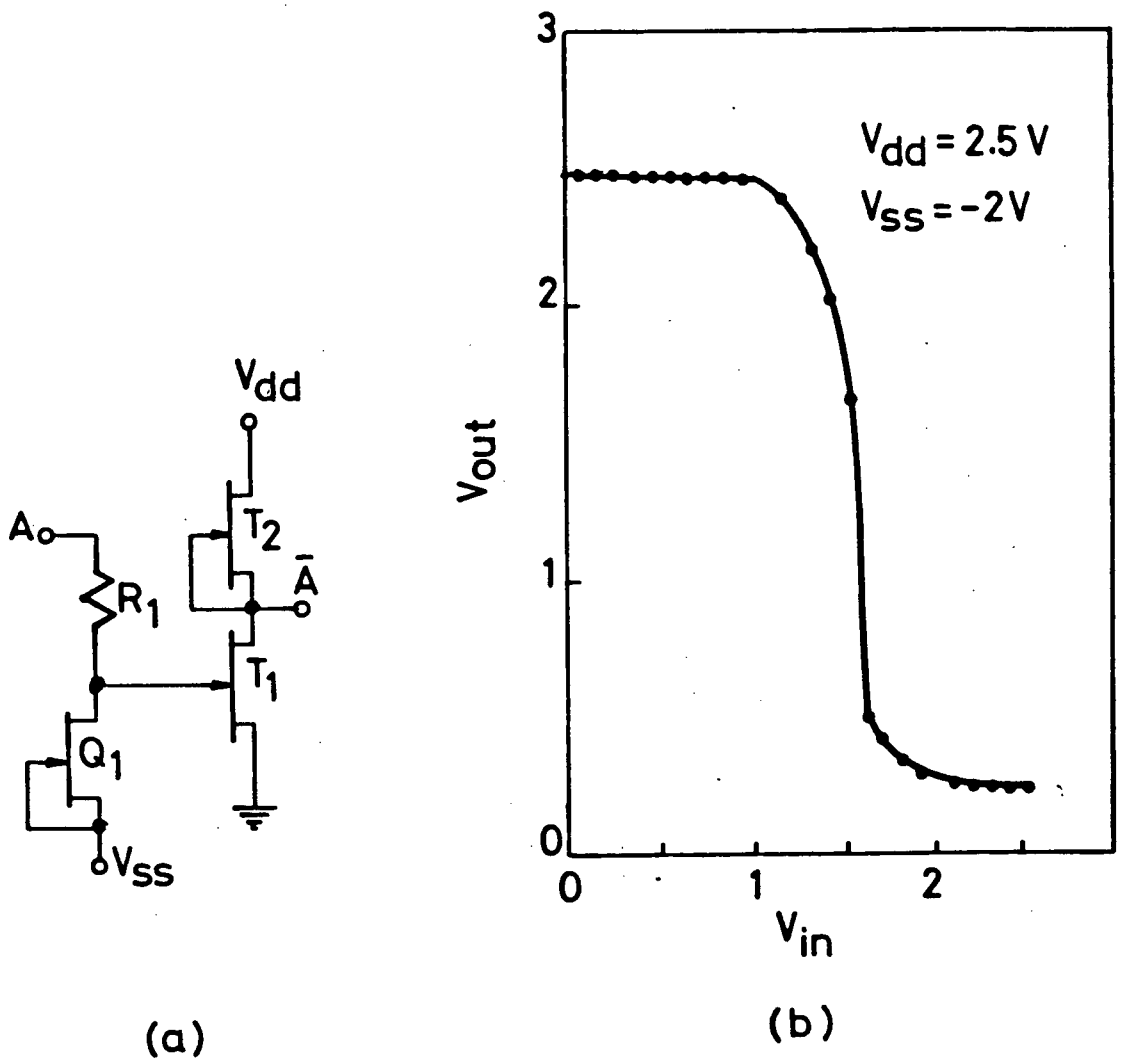


Fig.(5-11) (a) Schematic diagram of the CDFL inverter and (b) transfer characteristics.

used. This leads to the reduction of the integration capability of the logic.

A computer simulation of the transfer characteristic of the inverter is shown in Fig.(5-11.b). The figure shows that the voltage gain of the inverter in 12.8. The simulation program is shown in Appendix (A).

The main problem of this inverter is its poor fan-in and fan-out capabilities. Similar to the SDFL, a large current must be driven into the input of the next stage. However, these problems can be eliminated if the buffer circuit, Fig.(5-9.a), is added to the inverter to form the buffered inverter of Fig.(5-12.a). The simulation of the transfer characteristic of the buffered inverter is shown in Fig.(5-13). The value of the voltage gain of this inverter is similar to that of the unbuffered one since the voltage gain of the buffer circuit is 1.

The AND gate has a problem in that it cannot be used with a 1 level voltage higher than 0.8 V, otherwise, a massive current will flow from the gate if transistor T_2 is ON and T_3 is OFF. This massive current will not flow in case of an OR circuit where the switching transistors are identical to that of the buffer. Therefore, if a voltage swing larger than 0.5 V is required, the structure (CDFL1) of Fig.(5-13.a) must be used. This structure is similar to that of the SDFL. On the other hand, if a voltage swing of 0.5 V is needed, the structure (CDFL2) of Fig.(5-13.b) can be used.

The main advantage of the CDFL2 structure is that it dissipates a very low amount of power, however, this is at the expense of speed.

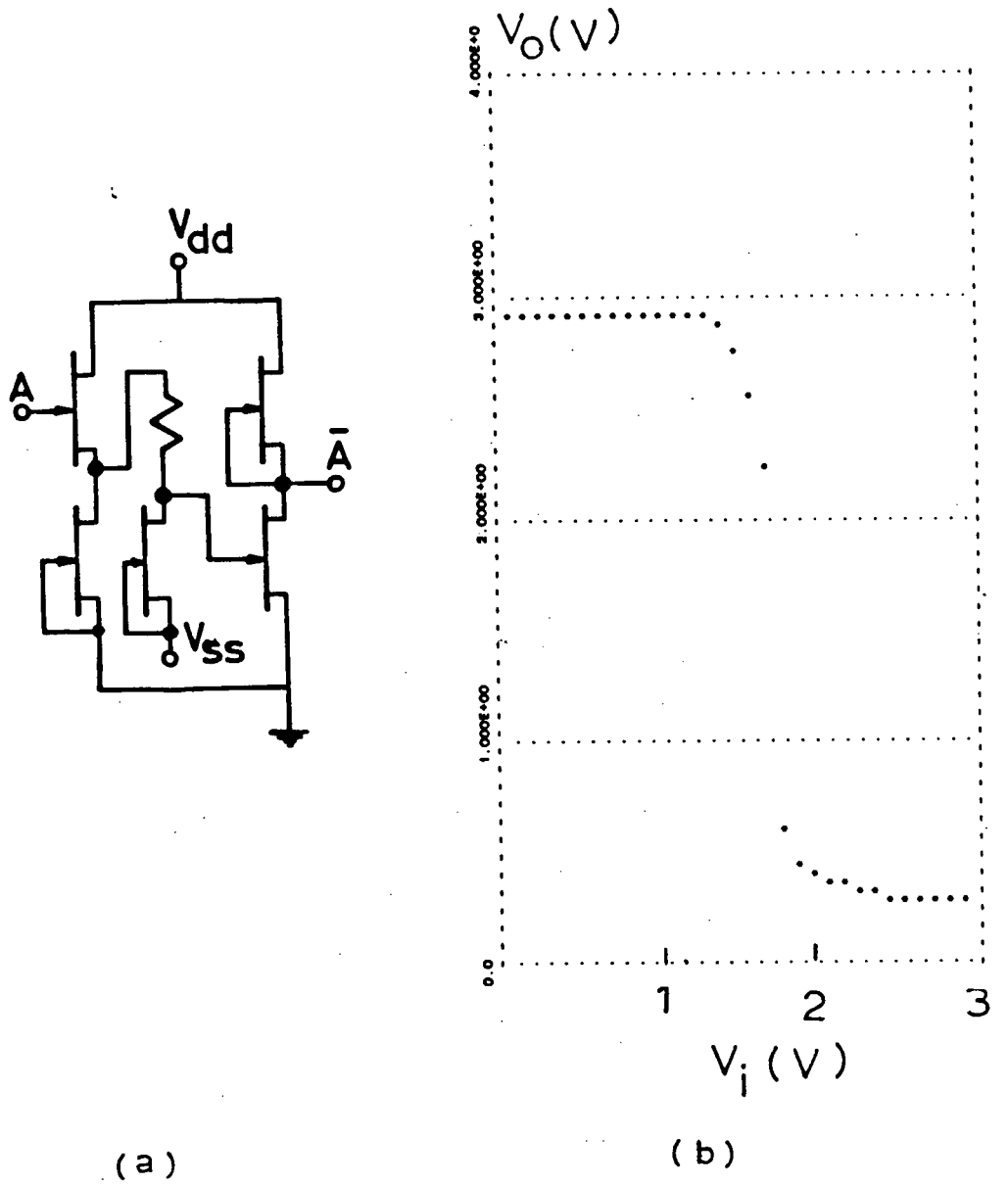


Fig.(5-12) (a) Schematic diagram of the CDFL buffered inverter, and (b) transfer characteristics.

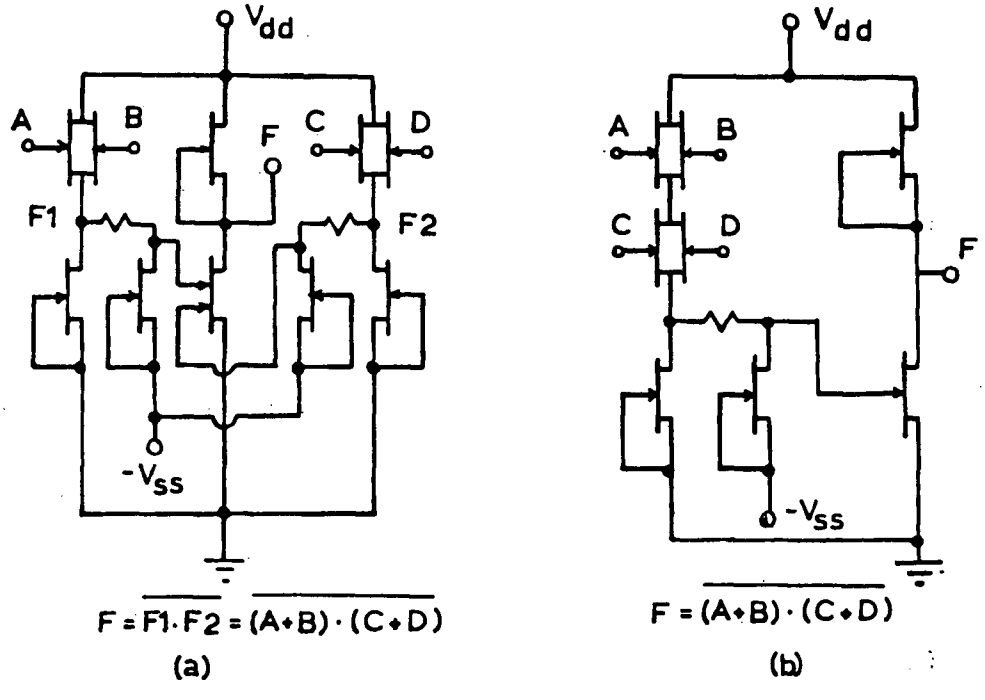


Fig.(5-13) Two possible design methods using the CDFL approach.

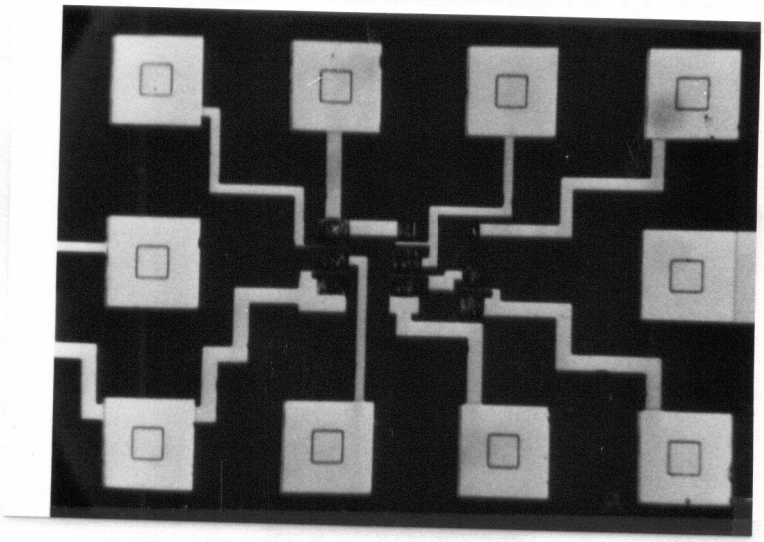
Compared to the DSFL, the CDFL1 has the advantage of low sensitivity to the fan out and not using small diodes. A comparison between the CDFL and the other GaAs logic scheme is presented later in Chapter(6).

5-3 Fabrication Process and Experimental Results

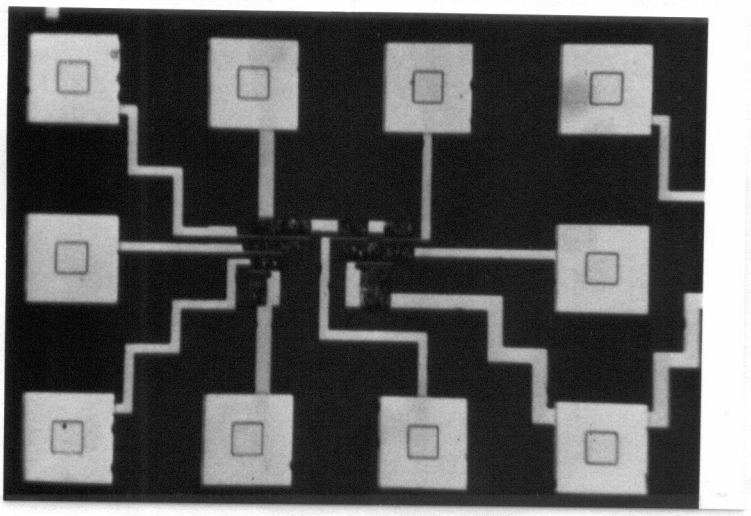
The fabrication process used was the ion-implanted planar process described in Chapter(3). Four logic circuits were fabricated; buffer circuit, an inverter, 2 input AND gate, and 2 inputs OR gate. 2μm gate lengths were used to design these circuits. This considerably long gate technology was used to avoid the very short channel fabrication problems.

Samples with different threshold voltages were fabricated. The threshold voltages varied from -2.5 V to -0.5 V. The ohmic contact region implantations (n+) were used to determine the value of the digital to analog inverter load resistor. Therefore, low doses for n+ implantation were used with the samples on which the inverter was optimized. Other samples with very high n+ dose were fabricated for optimizing the buffer, OR and AND gates. A SEM photograph of these circuits is shown in Fig.(5-14).

The DC characteristic of the buffer and the unbuffered inverter were measured using the HP 4145A semiconductor parameter analyzer. The transfer characteristic of the buffer is shown in Fig.(5-15.a). The voltage gain $G_m = - dV_o/dV_i$ was found to be 1, which agrees with the simulation result. Fig.(5-15.b) shows that the 0 level value saturates to 0 V if a sufficient negative bias is used instead of the ground potential (or a low negative voltage) assuming that the input is 0 V.



(a)



(b)

Fig.(5-14) Micrograph picture for (a) a buffer circuit and inverter; (b) an AND and OR gate.

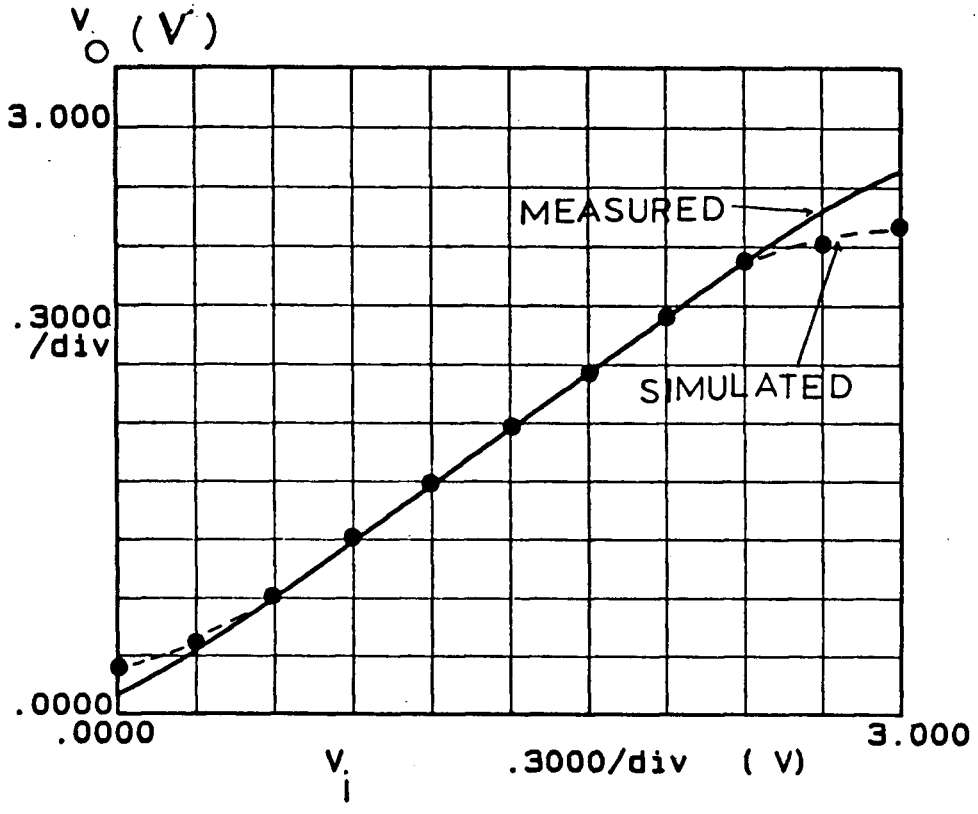


Fig.(5-15) Experimental and simulated transfer characteristics of the CDFL buffer circuit with V_{ss}=-0.5 V; (b) experimental transfer characteristics of the buffer with V_{ss}=-1 V.

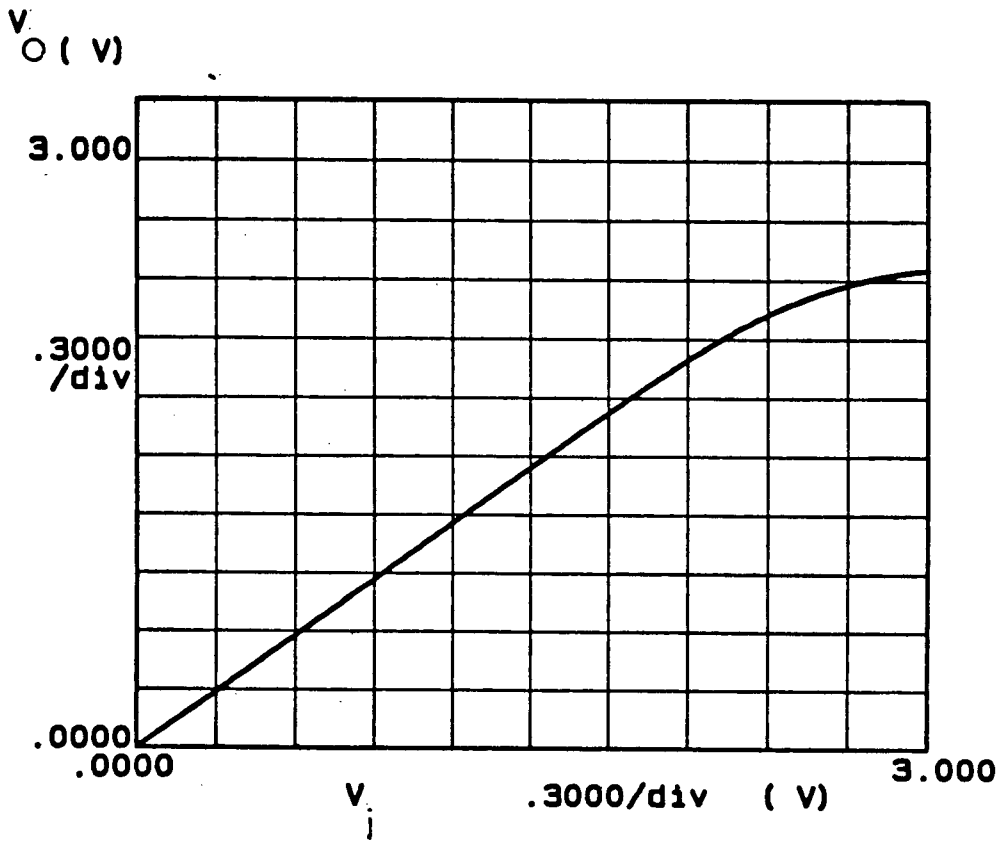


Fig.(5-15.b)

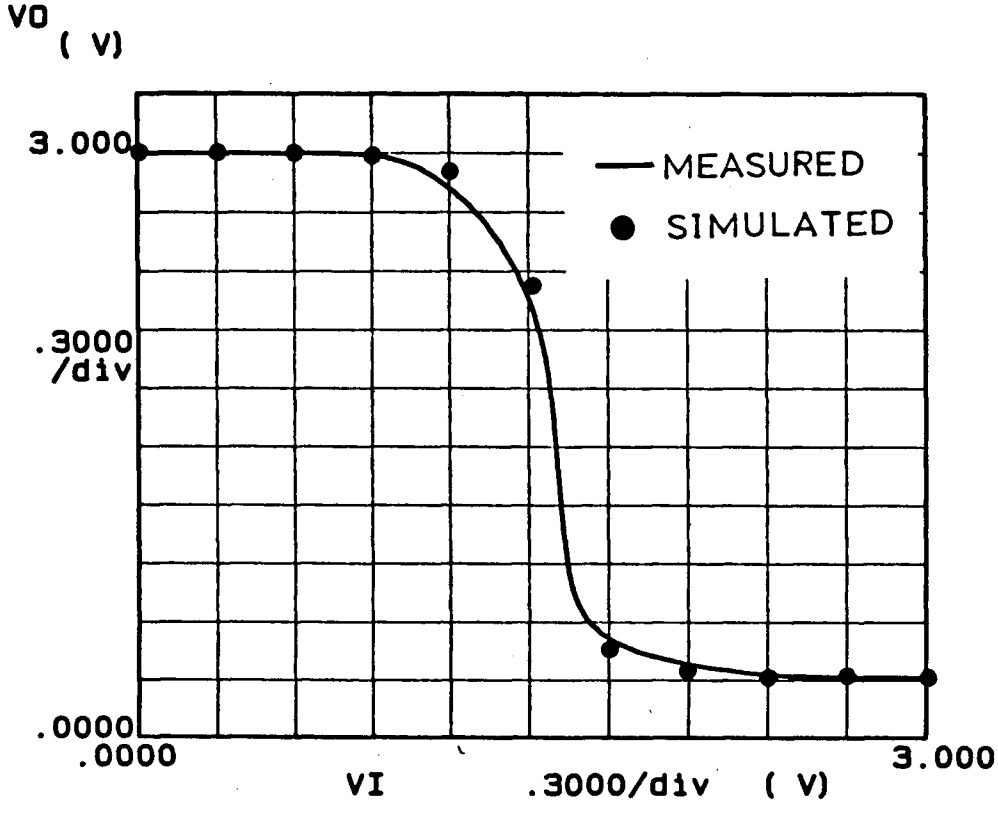


Fig.(5-16) Experimental and simulated transfer characteristics of the CDFL inverter.

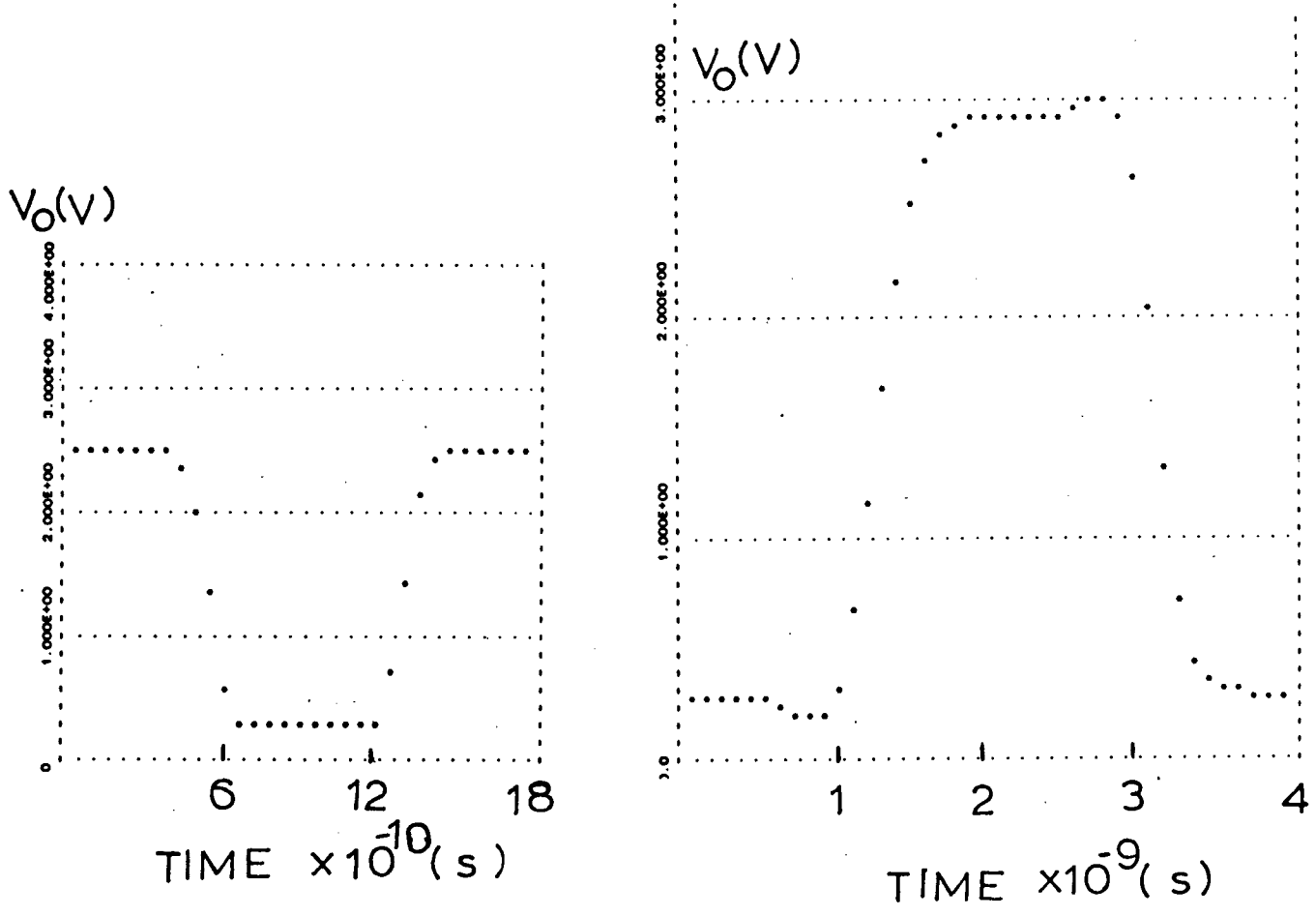


Fig.(5-17) Simulated high frequency response for (a) buffer circuit and (b) CDFL inverter

The inverter transfer characteristic is shown in Fig.(5-16). The simulation parameters of Table(4-1), used for simulating the 2μm gate MESFET, were used to simulate the transfer characteristics and the high frequency response of both the buffer circuit and the inverter (see Appendix(A)). As shown in Figs.(5-15) and (5-16), the simulated and the experimental curves are in very good agreement. The small deviation between the curves of the buffer circuit is due to the deviation between the experimental and the simulated I-V curves of the transistor at $V_{gs} > 0$ V, as shown in Fig.(4-2).

The high frequency response of the buffer is shown in Fig.(5-17.a). The time delay was 120 ps for a fan out of 1, therefore, it is expected to operate at up to 8.3 GHz. The power dissipation and the power-time delay product were 4 mW and 0.48 pJ per gate respectively.

For the inverter, the high frequency response, shown in Fig.(5-17.b), shows a time delay of 500 ps/gate or a speed of about 2 GHz. The power dissipation and the power time delay product (a buffer circuit was used as a load circuit) are 4 mW and 2.6 pJ per gate respectively. Adding the buffer to the inverter, to form the buffered inverter of Fig.(5-12.a), would result in a time delay of 620 ps, power dissipation of 8 mW and power-time delay product of 4.96 pJ.

Before evaluating the high frequency response, we have to take into consideration two factors: the first is that 2 and 4 μm gate transistors (with large gate capacitance) were used; the second is that these circuits are not optimized. Using load transistors of shorter gate length will improve the speed of the inverter because it reduces the values of C_{gs} and C_{gd} while using transistors with lower $|-V_{th}|$ will reduce the power

dissipation and consequently the power time delay product.

CHAPTER(6)

COMPUTER SIMULATION OF GaAs DIGITAL LOGIC PERFORMANCE

Computer simulation was done to compare the various GaAs logic approaches including CDFL. Using the published data on devices for comparison was difficult, if not impossible, due to the use of different transistors with different parameters for each case. The only available alternative was to simulate the performance of these logic arrangements using the JFET model of the SPICE program [14]. The logic approaches were classified into three groups. The first was the deep depletion group with a threshold voltage of -2.5 V. The second group was the depletion mode one with a threshold voltage of -1 V. The third group was the normally and quasi-normally off group with threshold voltages ranging from -0.5 to 0.2 V.

The first group logic contained the CCL, FFL, BFL, and UFL. The second group contained the CCL, BFL, UFL, SDFL1, SDFL2, CDFL.I1, and CDFL.I2. SDFL1 is the logic of Fig.(5-2) [3], while SDFL.I2 is the logic of Fig.(5-3) [66]. CDFL.I1 and CDFL.I2 are the CDFL buffered inverter of Fig.(5-12.a) but with load transistor widths of W_g and $W_g/2$ respectively. W_g is the gate width of the switching transistor. The CCL, BFL, and UFL were simulated with both the first and second group because they can be built with both threshold voltages. The third group contained the SCFL, CDFL, LPFL (1D, 1I, 3D, and 3I), and CDFL.B. The LPFL (1D, 3D, 1I, and 3I) will be labelled as LP1D, LP3D, LP1I, and LP3I respectively and the CDFL.B is the buffer circuit of Fig.(5-9.a). The biasing voltage values and the relative dimensions of the

other elements were taken from published data. The values of these parameters were then adjusted to give the optimum logic characteristics.

The aim of this study is to compare the time delay, the loading effect on the transfer characteristic, the power dissipation, the power time delay product, and the integration density capability of the simulated logic.

The stray capacitance was not taken into consideration because it is difficult to determine its value and only one or two stages are simulated. In addition to that, the study is a comparative one. However, the logic with large numbers of elements were expected to have higher stray capacitance and consequently slower speeds.

The integration density capabilities are determined by the area occupied by the logic. This area is measured in units of equivalent transistor areas based on the area of the switching transistor. The size of other transistors was calculated from the relative area to the switching transistor. The diodes sizes were also calculated from their areas relative to that of the switching transistor. Resistors were considered to occupy half the switching transistor area if only one resistor value is used. If more than one resistor with more than one value were used, the size of the resistor with the lowest resistance value was considered to occupy half the area of the switching transistor. The size of the other resistors were calculated according to their values relative to the first one. The assumption that the resistor size is half that of the transistor was calculated from the minimum length and width that can be used without causing the saturation of the electron velocity and consequently the saturation of the current, as will be discussed later.

The switching transistors, taken from [3], were 1 μm gate length, 10 μm gate width, and 1 μm spacing between the gate and both the source and the drain. The overall dimension of the transistor was 5×10 μm. The minimum resistor length is the minimum length at which no current saturation occurs. The saturation occurs at 0.5 V/μm of the channel length (or the length of the source chain separation) [18]. The maximum biasing voltage was 5 V, therefore the minimum transistor length should be 10 μm. The minimum resistor width is the minimum dimension of the technology used (1 μm in our case). Taking into consideration the areas of the ohmic contact, the resistor dimension was considered to be about 2×10 μm approximately.

The above calculation is not very accurate because it does not take into consideration the spacing between the branches and the devices, relative orientation which may affect the overall dimension of the logic. However, it can still give a good indication about the relative size of each logic.

The area of the devices can also be expressed, as a first approximation, by their widths relative to that of the switching transistor [81] since the gate length is the same for all the transistors. The dimensions of the switching transistor used in the simulation for the three groups are tabulated in Table(6-1). Relative dimensions of the elements and the biasing voltages for the logic of the first, second, and third group are shown in the simulation programs in Appendices (B), (C), and (D). The schematic diagrams of the three groups are shown in Chapter(5).

6-1 The Deep Depletion Group (Group#1)

The power dissipation for this group is generally high. The dissipated

TABLE(6-1)

Transistors Parameters used to simulate groups #1, 2, and 3

Group #	$R_s(\Omega)$	$R_d(\Omega)$	C_{gs}(fF)	C_{gd}(fF)	$\beta(A/V^2)$	V_{th}(V)
1	100	100	5	5	4.4×10^{-4}	-2.5
2	200	200	5	5	7×10^{-4}	-1.0
3	400	400	5	5	1×10^{-3}	-0.5
	400	400	5	5	1.4×10^{-3}	0

power for the BFL, FFS, UFL, and the CCL are 28.1, 12.6, 9, and 7.2 mW/gate respectively. The high power dissipation of the BFL can be attributed to the use of a large load driver source follower transistor. Using a small load driver source follower transistor can lead to lower power dissipations in the case of the FFS (see Table(6-2)). The ratio between the power dissipated by the FFS and the BFL, if the same transistor dimensions were used, is near that reported by Namordi et al. [71].

Eliminating the load driver transistor has led to the reduction of about 70% of the power in case of the UFL. The CCL dissipates comparatively low amounts of power due to the use of only branches between V_{dd} and the ground and only one voltage source.

The power time delay product for this group is shown in Table(6-2). The BFL has the highest value (1.26 pJ) while the FFS and the UFL have nearly the same $P.\tau_d$ (0.63 pJ and 0.67 pJ respectively). The CCL $P.\tau_d$ is the lowest (0.37 pJ) because of its low power dissipation and low time delay.

The relative area occupied by this group are 9.6, 11.1, 6.1, and 4.1 W_g for the CCL, FFS, BFL, and the UFL, respectively. The large area occupied by the FFS is due to the use of a large number of elements; some of them have large dimensions. The large dimensions of the diode used with the CCL is responsible for the occupation of a large area by the logic. The time delays for unity fan-out are 50, 55, 45, and 75 ps for the CCL, FFS, BFL, and the UFL respectively (Fig.(6-1).

The logic level and the voltage gain (Fig.(6-2)) for these logics are not sensitive to the loading. The time delay sensitivities are 7.5, 17.5, 17.5, 32.5 ps for the CCL, FFS, BFL, and the UFL respectively, Fig.(6-1).

Comparing the logics of this group to each other one can see that the

TABLE(6-2)

Simulation results for GaAs digital logic approaches

Group #	Logic	Power (mW)	P•τ (pJ)	Area (W_g)	Number of elements	Logic level sensitivity (high level)	Time delay (fanout = 1) (PS)	Voltage gain (fanout = 1)	Time delay sensitivity (PS)	Voltage gain sensitivity
1	CCL	7.2	0.36	9.6	3	0%	50	not available	12.5	not available
	FFS	12.6	0.7	11.1	7	0%	55	15.8	17.5	0
	BFL	28.1	1.25	6.1	6	0%	45	14.9	17.5	0
	UFL	9	0.675	4.1	6	0%	75	3.7	1.5	0
2	CCL	1	0.086	9.6	3	0%	88	not available	14	not available
	BFL	3.25	0.325	6.1	6	0%	100	14.75	10	0
	UFL	1.5	0.225	4.1	6	0%	150	9	50	0
	SDFL1	5	0.4	4.3	5	33%	80	7.3	95	2.02
	SDFL2	6.25	0.468	12.5	8	13%	75	7.5	10	0.9
	CDFL-I1	3.9	0.316	5.2	6	0%	80	8.5	7.5	0
	CDFL-I2	3	0.27	4.7	6	0%	90	12.35	10	0
3	SCFL	4.7	0.235	24	11	0%	45	1.4	5	0
	DCFL	0.1	0.007	2.5	2	5%	70	3	20	0.085
	LP1D	2.42	0.217	5	5	8%	90	4.4	15	0
	LP1I	1.4	0.133	5	5	0%	95	4.1	32.5	0.23
	LP3D	1	0.06	3.5	4	0%	65	1.5	30	0
	LP3I	0.6	0.033	4	4	15%	55	1.4	not available	not available
	CDFL-B	0.7	0.007	2	2	0%	10	1	5	0

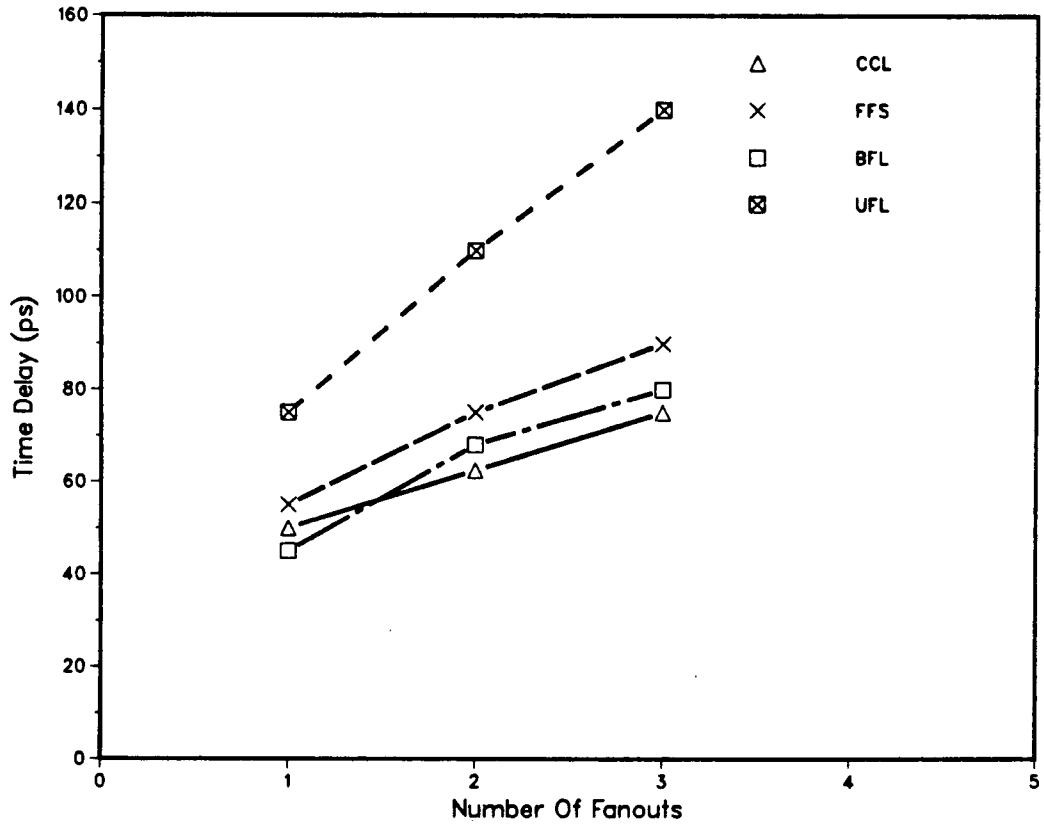


Fig.(6-1) Plot of τ_d vs. number of fan-outs for group#1.

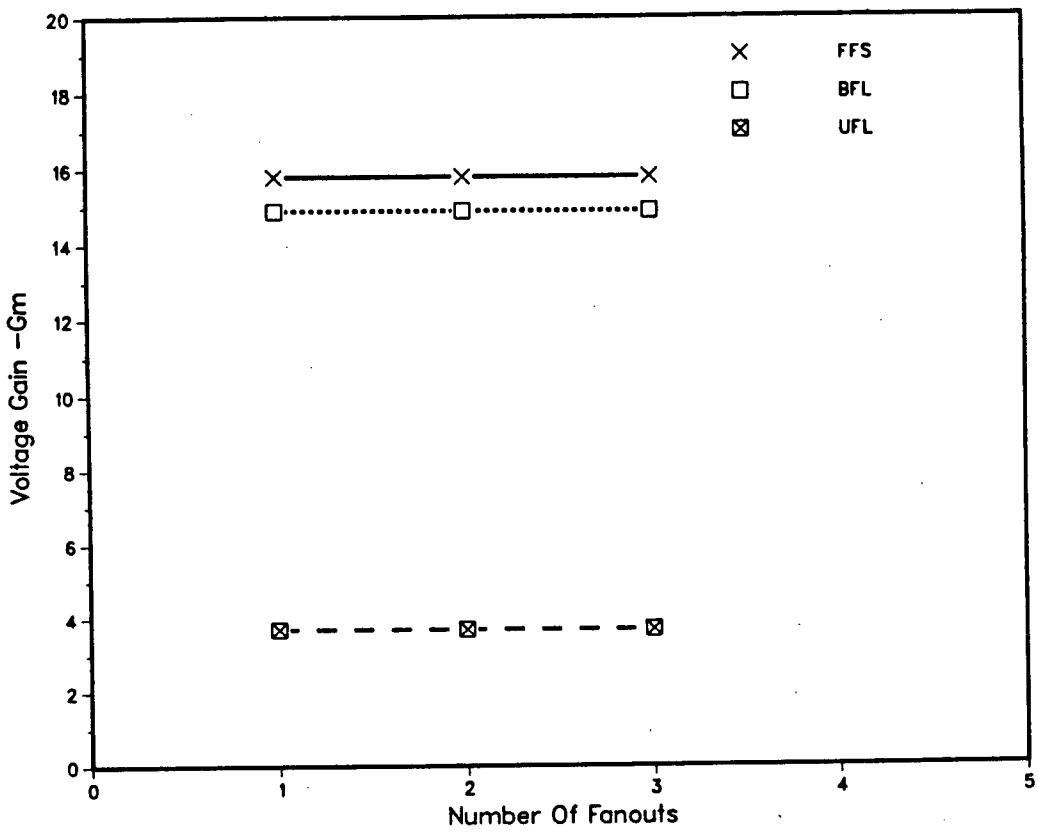


Fig.(6-2) Plot of G_m vs. number of fan-outs for group#1.

CCL cannot operate at frequencies less than 20 kHz, the FF1 occupies the largest area, the BFL consumes the largest amount of power, and the UBFL is the slowest and the most sensitive to the loading. Therefore, these logic families may not be able to meet all the requirements of UHS VLSI.

6-2 Low Power Depletion Mode Logic (Group#2)

The logic of this group dissipate lower power than those of group#1 due to the use of low pinch-off voltage (-1 V). The power dissipation for the CCL, BFL, UFL, SDFL1, SDFL2, CDFL.I1, and the CDFL.I2 are 1, 3.25, 1.5, 5, 6.25, 3.95, and 3 mW/gate respectively. The highest power was dissipated by the DSFL2 due to the use of more branches, 3, between the high and the low biasing voltage in parallel as shown in Fig.(5-3). SDFL1 dissipates considerably high power due to the use of large load transistor (1.5 the switching one). The BFL, CDFL.I1, and CDFL.I2 dissipate moderate amounts of power compared to the other, while the CCL and the UBF dissipate the lowest power in this group.

As shown in Fig.(6-3), the time delays for the logics of this group are higher than those of the first one. The time delay of the CCL, SDFL1, SDFL2, CDFL.I1, and the CDFL.I2 are 88, 80, 75, 80, and 90 ps respectively. The time delay for the BFL and the UFL are 100 and 150 ps/gate respectively which are higher than those of the rest.

The delay time sensitivities to the loading are not so high compared to those of the first one except for the SDFL1 and the UFL which have a sensitivity of 90, and 50 ps respectively. The levels of the SDFL1 were even completely lost for a fan out of 3. The reason for the high sensitivity is

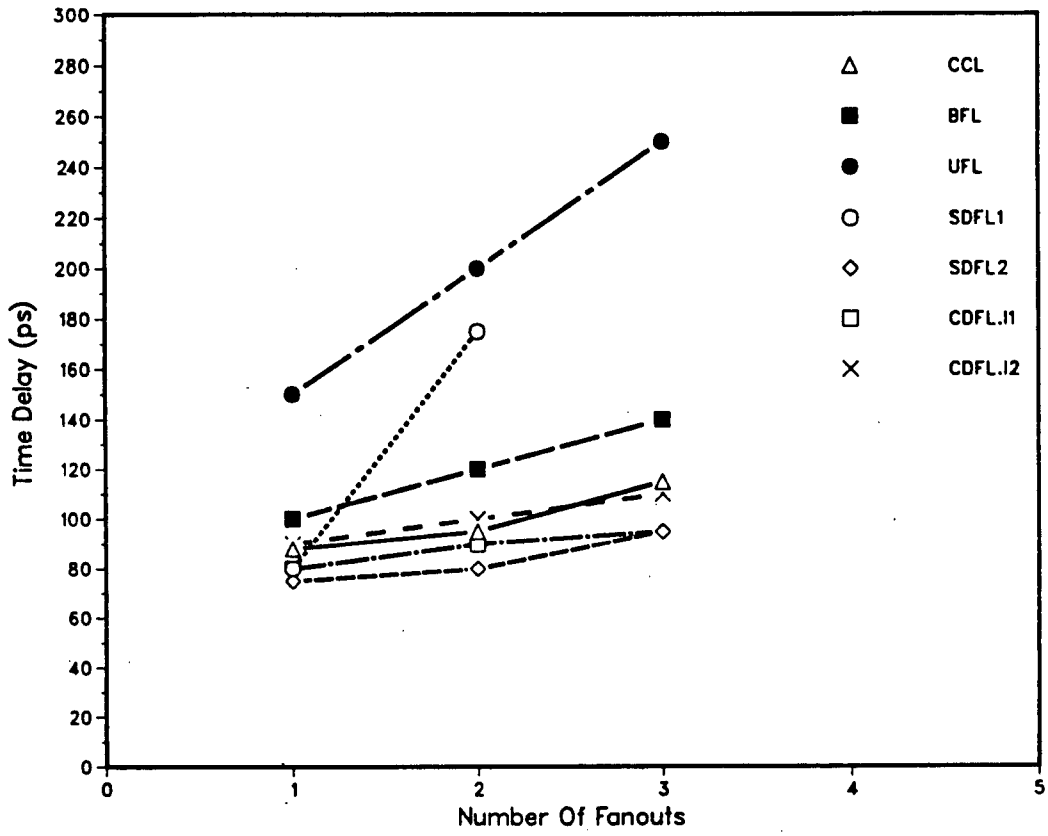


Fig.(6-3) Plot of τ_d vs. number of fan-outs for group#2.

the requirement for a very large current to be driven into the next stage (as explained at the beginning of Chapter(4)).

The $P.\tau_d$ product is shown in Table(6-2). The CCL has the lowest $P.\tau_d$ with 0.08 pJ while the SDFL2 has the highest of 0.468 pJ per gate. The CDFL.I2 has 0.27 pJ/gate power time delay product.

The logic levels and the voltage gain sensitivity to the loading is shown in Table(6-2) and Fig.(6-4) respectively. While most of the logics of this group are not sensitive to the loading, the SDFL1 and SDFL2 are very sensitive. They have G_m sensitivity of 2 and 0.9 respectively.

As a conclusion, this study has shown that the CCL has no proper D.C. characteristics; the UFL is the slowest logic; the SDFL1 is the most sensitive logic to the loading; the SDFL2 dissipates the highest power and occupies the largest area per gate; and the BFL is slower and occupies larger than the CDFL.I1 and CDFL.I2. Therefore, the CDFL.I may be the other alternative which can provide high speed, low power dissipation, and less loading effect at the same time.

6-3 Normally and Quasi-normally Off Mode Logic (Group#3)

The last group includes the normally and quasi-normally off logic. The main problem facing this group is the low yield of production due to the necessity for a tight control of the threshold voltage. The main advantage is that they dissipate low power/gate (see Table(6-2)). SCFL, CDFL, LP1D, LP1I, LP3D, LP3I, and CDFL.B dissipate 4.7, 0.1, 2.42, 1.4, 1, 0.6, and 0.7 mW/gate respectively. The DCFL dissipates the lowest power in all GaAs logics. The SCFL not only dissipates the highest amount of power compared to

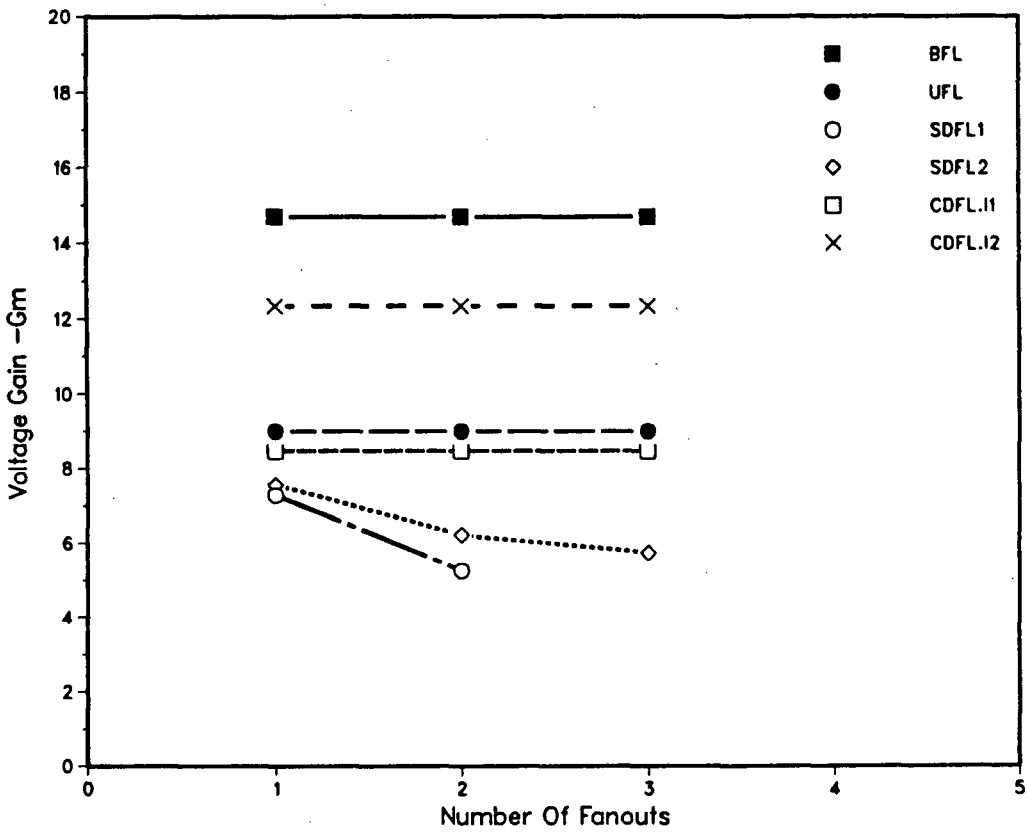


Fig.(6-4) Plot of G_m vs. number of fan-outs for group#2.

the rest of this group logic, but it occupies the largest area per gate compared to all GaAs logics, as shown in Table(6-2). The CDFL.B occupies the smallest area of all.

The time delays for unity fan-out for SCFL, DCFL, LP1D, LP1I, LP3D, LP3I, and CDFL.B are 45, 70, 90, 95, 65, 55, and 10 ps per gate respectively with time delay loading sensitivities of 5, 20, 15, 32.5, 30, not available, and 5 ps respectively. This shows that the CDFL.B can provide the lowest time delay and loading sensitivity, Fig.(6.5). The power time delay products, shown in Table(6-2), shows that both DCFL and CDFL.B have the lowest $P.\tau_d$ of about 0.07 pJ compared to 0.235 pJ for the SCFL. Table (6-2) and Fig.(6-6) shows also that the DCFL, LP1D, LP3D, and LP3I logic levels are sensitive to the loading.

Comparing these logic families to each other, one can see that the SCFL dissipates the largest power and occupies the largest area. The DCFL dissipates the lowest power, however it is sensitive to the loading. The LP1I and LP3D, LP3I logics are the most sensitive to the loading and LP1D is the slowest. On the other hand, the CDFL.B has the lowest time delay, the lowest $P.\tau_d$, and occupies the smallest area per gate.

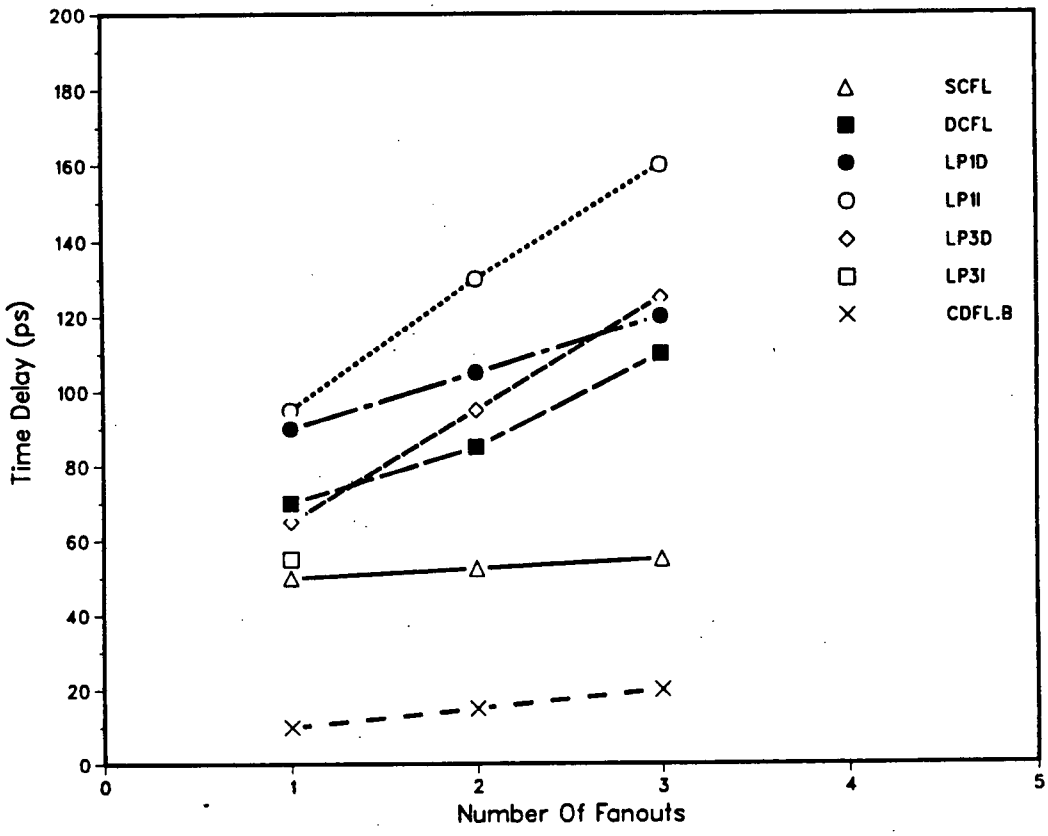


Fig.(6-5) Plot of τ_d vs. number of fan-outs for group#3.

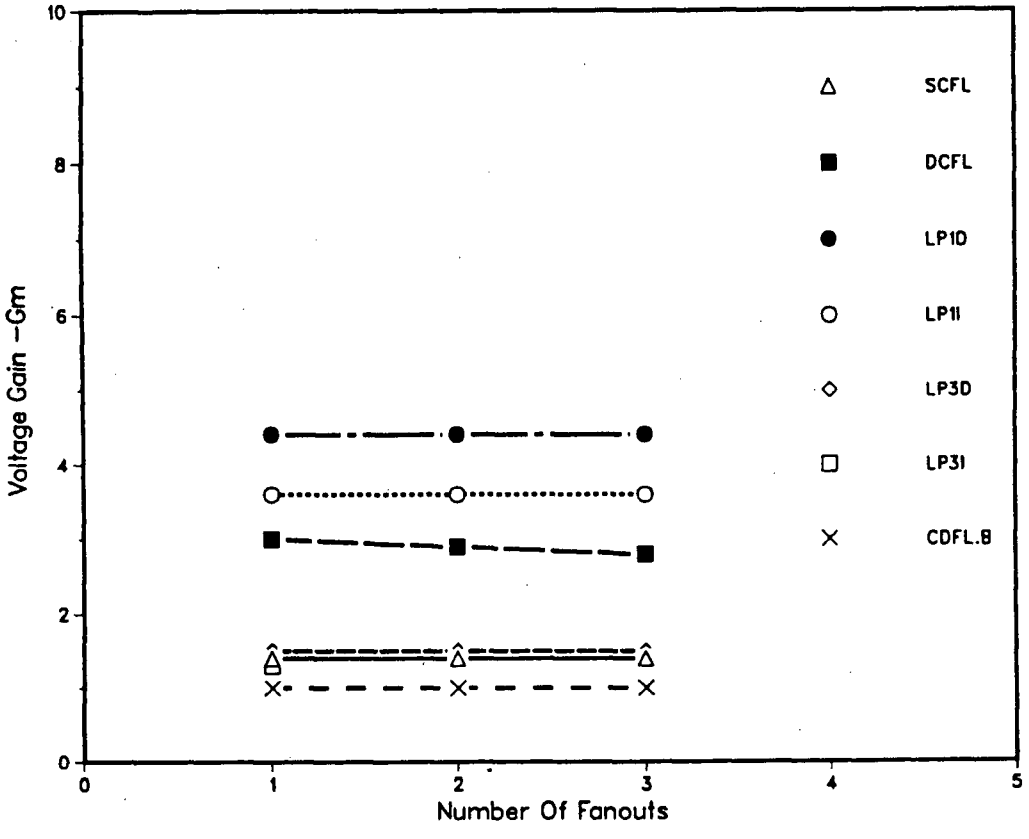


Fig.(6-6) Plot of G_m vs. number of fan-outs for group#3.

CHAPTER(7)

THREE BIT GaAs DIGITAL TO ANALOG CONVERTER (DAC)

Digital to analog converters (DAC) provide an interface between the digital signals of computer systems and the continuous signal of the analog world. The digital input and the reference voltage combine to control the output which will be in this case [92]

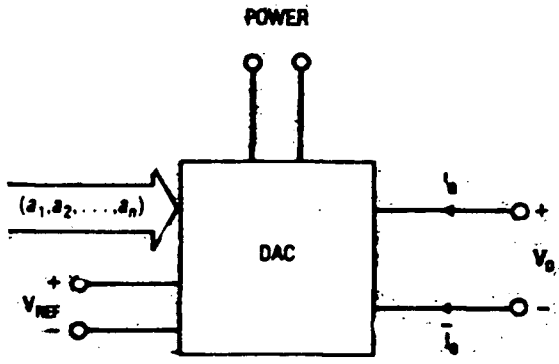
$$V_o = K\, V_{fs}[a_1.2^{-1} + a_2.2^{-2} + \ldots + a_n.2^{-n}] + V_{os} \qquad (7\text{-}1)$$

as shown in Fig.(7-1).

For most converters, the input word is in either binary or binary-coded decimal form. The converter output can be available as either an output current or output voltage depending upon the design and the application requirements.

In the current mode DAC, the voltage on the load transistors (current sources) remains essentially constant while the current path is changed to effect a change in the ouput voltage [82]. This type is faster than the voltage mode DAC where the load transistors do not contribute to the time delay of the converter since their capacitance need not be charged or discharged during the operation.

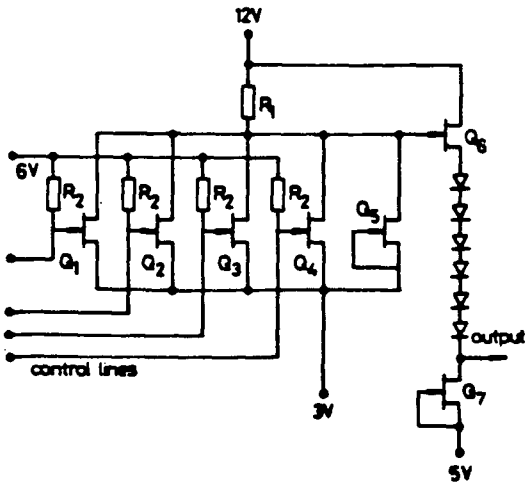
When this project started in 1982, there had been no publication of work on GaAs DACs [83]. Later, two DACs were reported [84-85]. Saunier et al. [84] have designed a DAC with a structure similar to that of the BFL as shown in Fig.(7-2.a). The application for this converter was to control the gain of power dual gate FETs. The main disadvantage of this converter is the use of



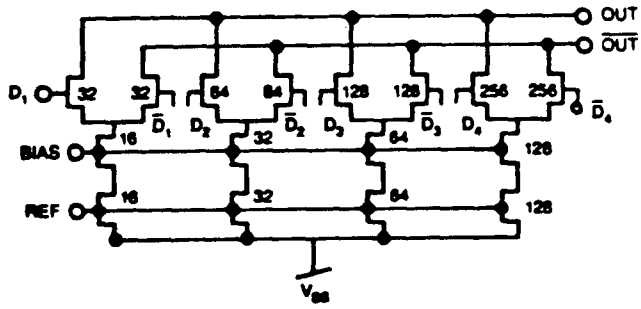
$$V_0 = K V_{FS} [a_1 2^{-1} + a_2 2^{-2} + \ldots + a_n 2^{-n}] + V_{OS}$$

V_0 = OUTPUT VOLTAGE
K = GAIN
V_{FS} = FULL-SCALE OUTPUT VOLTAGE
$a_1, a_2, \ldots, a_n$ = n-BIT INPUT WORD
V_{OS} = OFFSET VOLTAGE
V_{REF} = REFERENCE VOLTAGE
I = CURRENT

Fig.(7-1) Diagram of a digital to analog converter [92].



(a)



(b)

Fig.(7-2) Schematic diagrams of DACs developed by (a) [84] and (b) [85].

a large number of elements especially diodes. The second converter, developed by Tektronix [85], was a current mode type, therefore, it is expected to operate at higher frequencies. The disadvantages of this converter lies in its use of 3 power supplies and the need for the complement signals of the outputs as shown in Fig.(7-2.b).

In this project, current mode DACs were designed, Fig.(7-3). Depletion mode transistors and diodes were used. The diodes allow current to flow into the load resistor but not in the opposite direction. The width of the load transistors (current sources) Q_1, Q_2, and Q_3 were scaled by the ratio 1:2:4 to provide current scaled by the same ratio. The switching transistors T_1, T_2, and T_3 were also scaled by the same ratio in order to provide equal rise and fall times for all branches.

The operation mechanism of this converter is that when the switching transistor (T_1 for example) is switched ON, the current of the load transistor of the corresponding branch (Q_1 in this case) flows to ground through the switching transistor. The voltage at the point A will be about 0.2 V which is not enough to switch the diode ON. On the other hand, if transistor T_1 is off, the voltage at point A reaches V_{dd} causing the diode to switch ON and the current from transistor Q_1 to flow through the load resistor causing a voltage drop across it. The voltage of point A can be adjusted to switch between V_{dd} and a negative value if a negative biased voltage is used at node B.

The layout of the 3-bit DAC is shown in Fig.(3-2). As shown in this figure, the pull down transistors T_1, T_2, and T_3 have gate lengths of 2 μm and gate widths of 20, 40, and 80 μm respectively. The gate length of the

load transistors Q_1, Q_2, and Q_3 is 4 μm and the gate widths are 10, 20, and 40 μm respectively. The diodes are made big enough to avoid any fabrication problems which may result if very small dimensions were used. The diodes dimensions are 4×8, 4×16, and 4×22 for D_1, D_2, and D_3 respectively.

The same DAC has been redesigned with saturated resistors as current sources, see Fig.(7-3). The same dimensions have been used for the diodes and the switching transistors (pulldown transistors) T_1, T_2, and T_3. The length of the saturated resistors (separation between the two electrodes) was 4 μm and the widths were 6, 12, and 24 μm for R_{sat1}, R_{sat2} and R_{sat3} respectively. The saturated resistors were used because of the potential increase of the speed of the converter it might be gained. The operation mechanism of this DAC is similar to the DAC with transistors as current sources. Fig.(7-4) shows a micrograph picture of both converters.

7-1 Fabrication process and measurement

The DACs were fabricated on the same chip along with the CDFL gates and the monitoring devices. Therefore, the DC measurements of Chapter(2) apply to the transistors used in the DACs. The ion-implanted planar fabrication technique was used. Although all the fabricated samples contain both converters, only sample#2, sample#4, sample B5, and sample C5 have a second level metallization which allowed us to test the converters. The doses and energies used for these samples are tabulated in Table(3-1). The doses and energies of the n^+ implantation were chosen to give resistance from 200 to 300 ohms for the load resistor of the converters. The sample was annealed at 830°C for 25 minutes with Si_3N_4 as a cap.

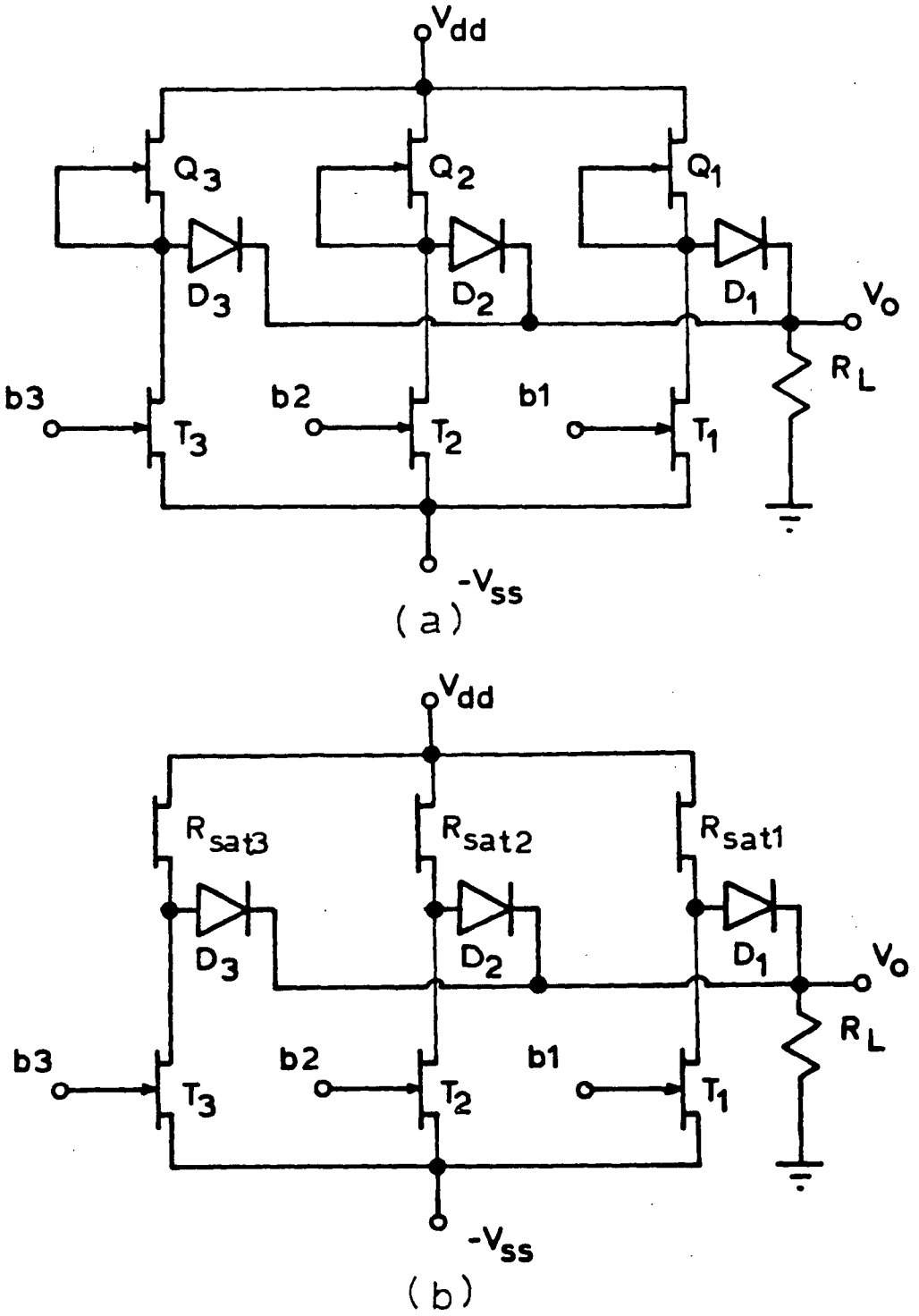
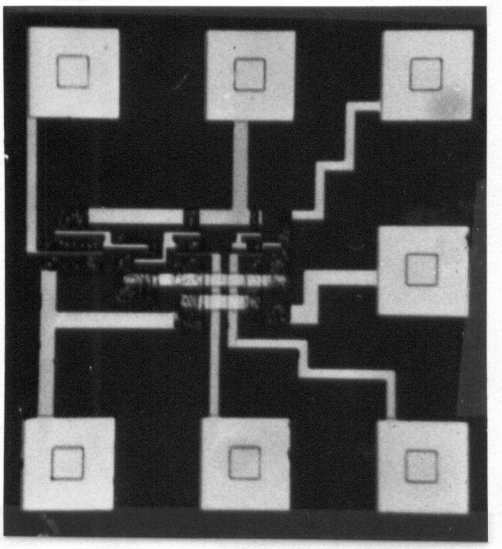
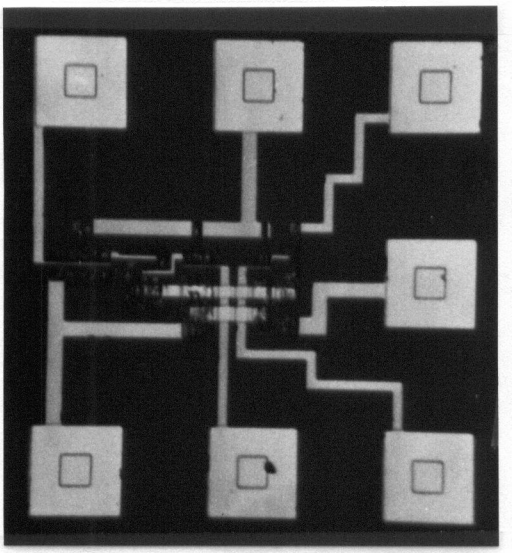


Fig.(7-3) Schematic diagrams of d-bit DAC with (a) MESFETs as current sources and (b) saturated resistors as current source.



(a)



(b)

Fig.(7-4) Micrograph picture for DACs of (a) Fig.(7-3.a) and (b) Fig.(7-3.b).

AuGe was used for ohmic contacts where it was alloyed at 450°C for about 5 minutes. Al was the choice for the gate, first, and second level of metallization. Si_3N_4 was used at the beginning as a dielectric between the two levels of metallization, however it caused the destruction of the channel. Then, sputtered SiO_2 was tried, but it was hard to etch holes through it using CF_4 plasma (which is not the right plasma for SiO_2). Although C_2F_6 gas can be easily installed, it was not available at this time. Buffered HF was not used for etching SiO_2 because it would etch the metal (Al) underneath. We did not proceed in using SiO_2 because of the fact that during sputtering the sample was subject to energetic atoms which may cause the same problem as Si_3N_4 does. Therefore, polyimide PI 2550 from DuPont was used instead. This organic material has better properties than both Si_3N_4 and SiO_2 as a dielectric with no sign of channel degradation when used. See Chapter(2) for more details about the fabrication process.

The DAC performances were tested by measuring the output from each individual branch. The measurements showed that the output voltages for both converters are scaled by the ratio 1:2:4, as shown in Figs.(7-5) and (7-6), which is the required ratio. Both converters gave nearly the same output when the saturated resistors dimensions were chosen to give nearly the same saturation current as that of the transistors. The DAC performance was simulated using the parameters of the transistors of sample#4 (see Table(4-1)). The time delay of the most significant bit (MSB) was found to be 100 ps when a load of 300 ohms was derived as shown in Fig.(7-7). This indicates that the converter can operate at a frequency of up to 10 GHz. The total D.C power dissipation was 10 mW.

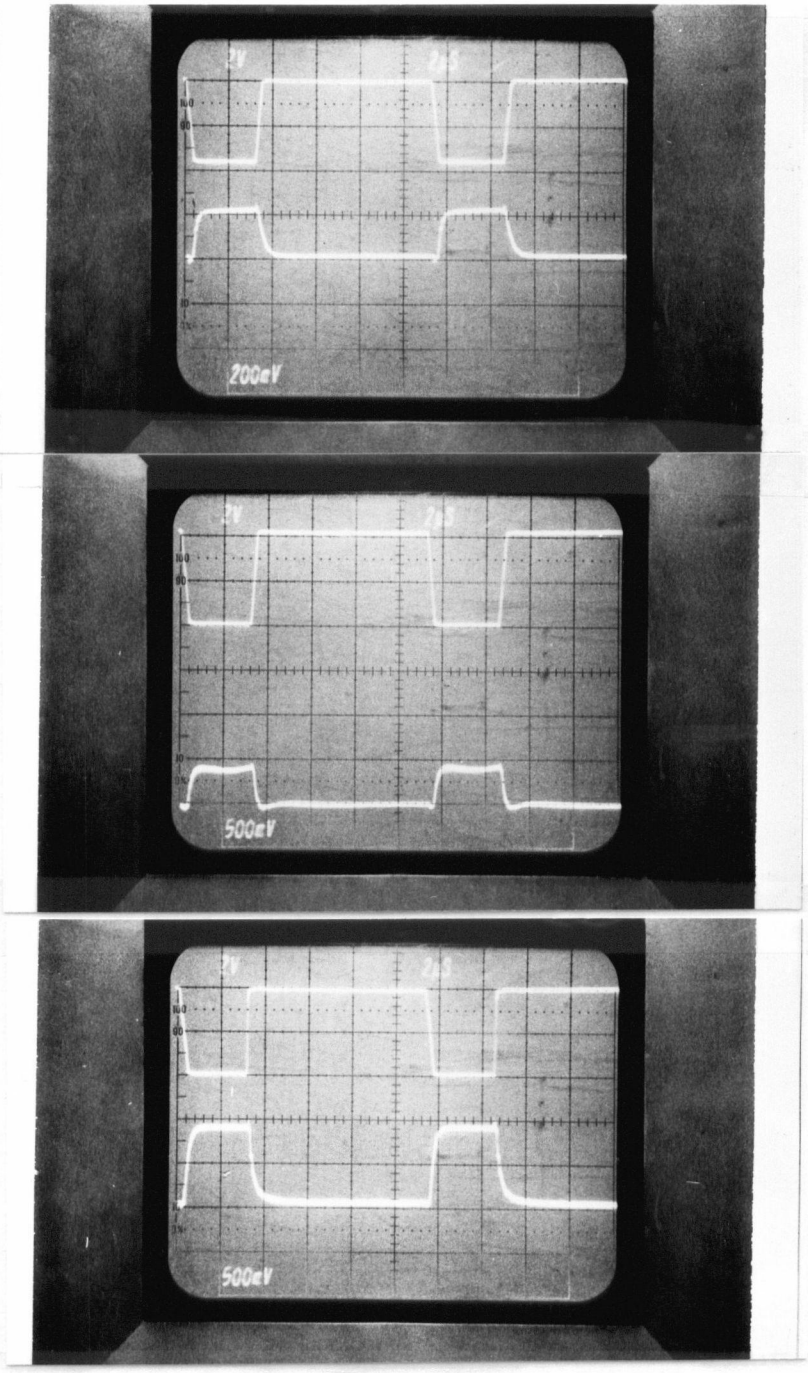


Fig.(7-5) Output voltage of the 3 branches of the DAC of Fig.(7-3.a)

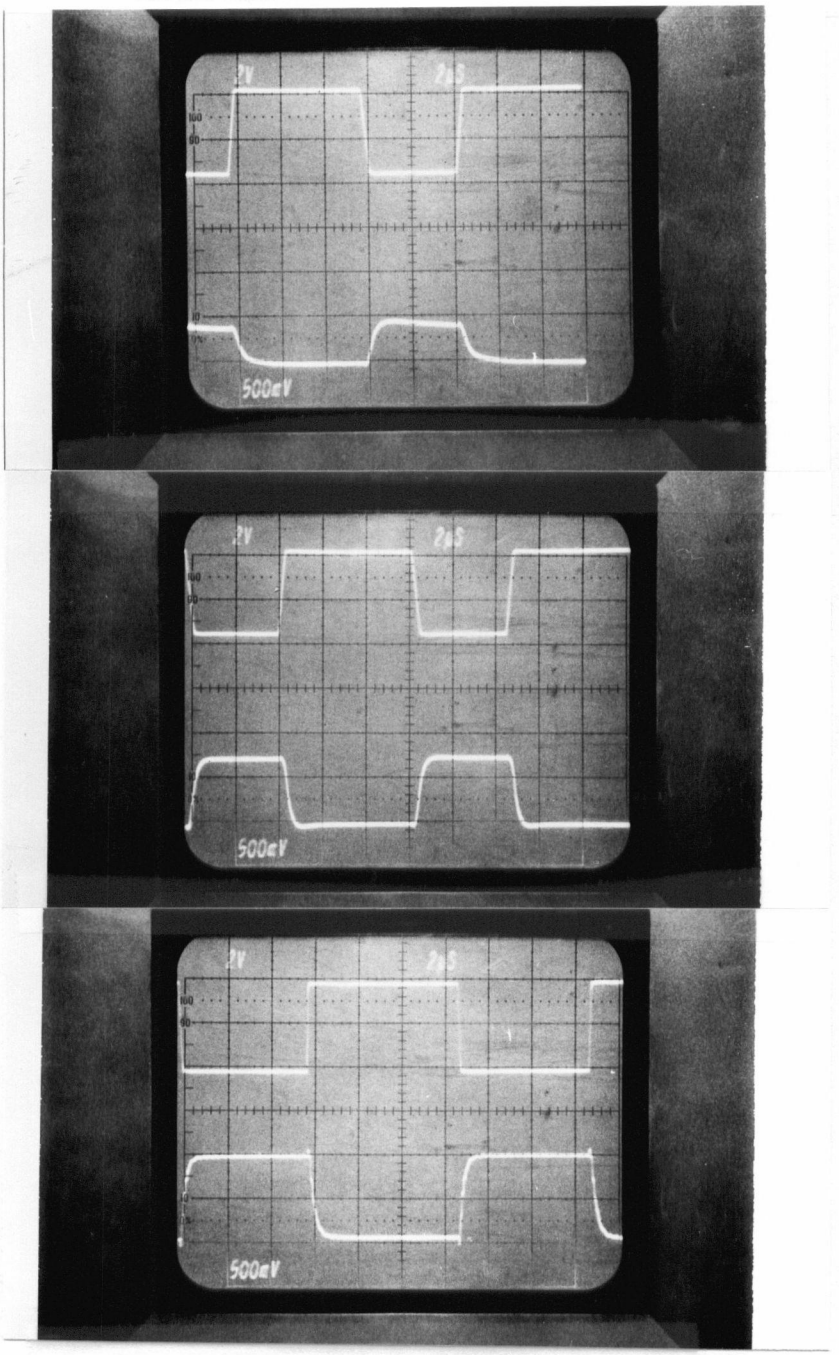


Fig.(7-6) Output voltage of the 3 branches of the DAC of Fig.(7-3.b)

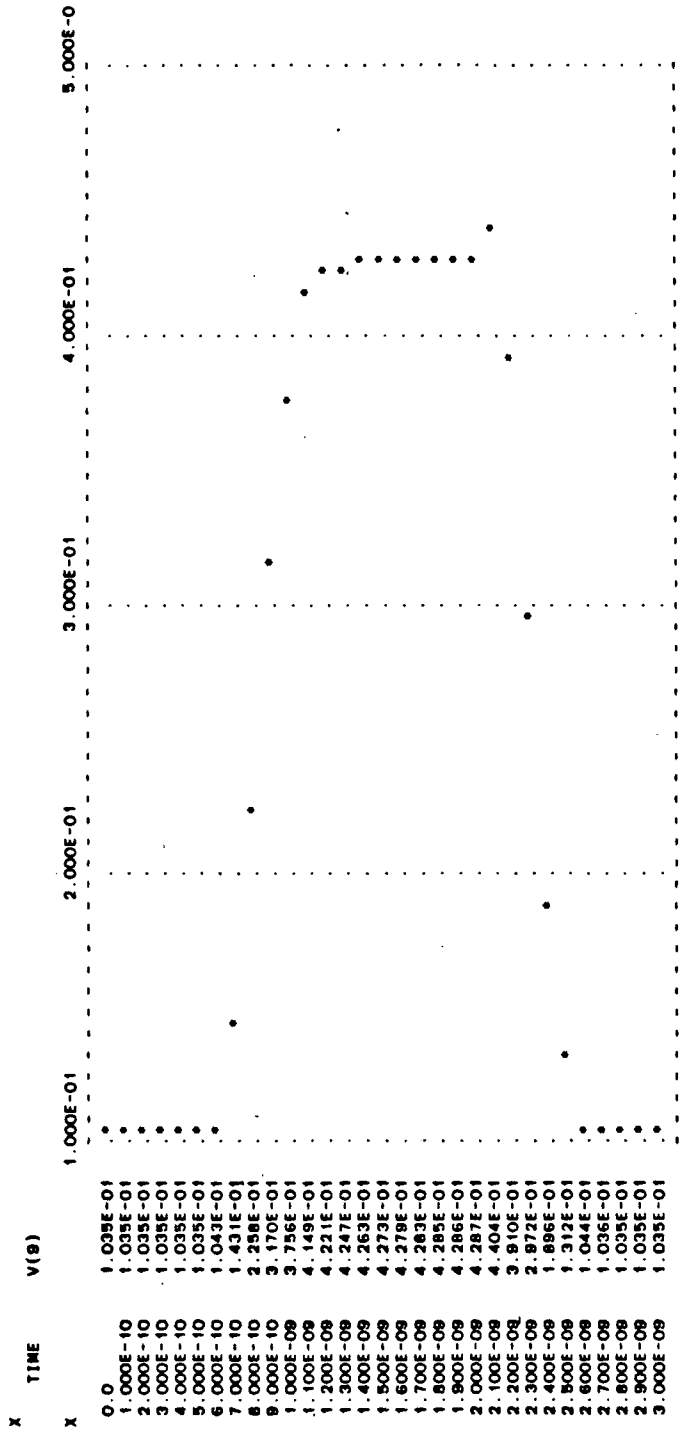


Fig.(7-7) Simulated high frequency response of the DAC.

7-2 Evaluation of the saturated resistor as a load and a current source

The advantages of the saturated resistor are stated in Chapter(2). These advantages can be realized if the saturated resistor is used as a load element for some logic approaches which require large load current such as the SDFL. However, some problems may be faced if it was used as a load element for some other logic approaches, such as the DCFL, or a current source device.

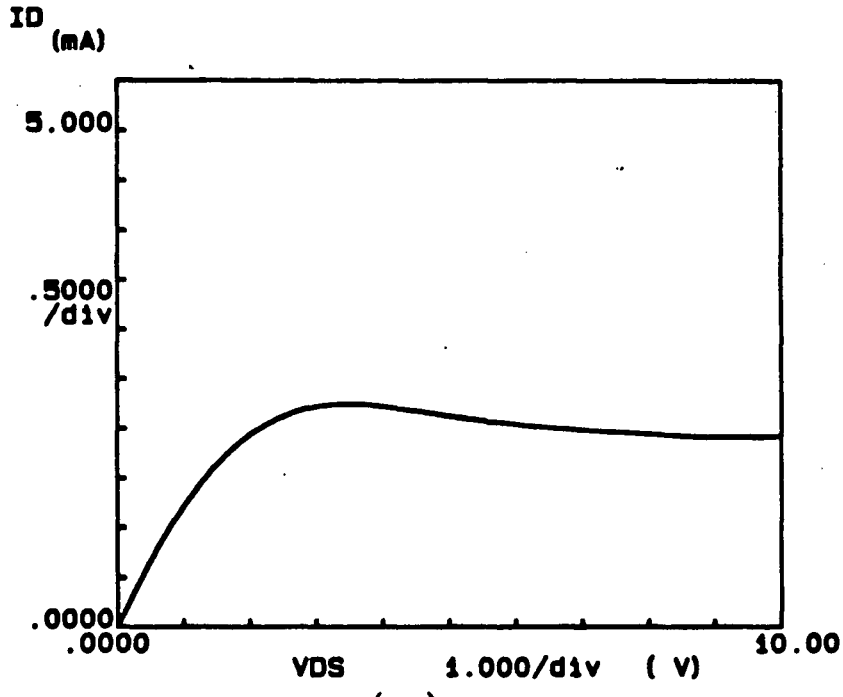
The first problem we have faced with the saturated resistor was that very small dimensions must be used. This is because the saturated resistor conductance is 2.5 times that of a transistor with -1 V threshold voltage, assuming that both have the same channel length. Therefore, the saturated resistor width should be 1/10 that of the switching transistor if the load saturation current is required to be 1/4 that of the switching transistor to obtain an output pulse with equal fall and rise times. Using a switching transistor with a width of 10 μm requires a saturated resistor width of 1 μm. Therefore, an increase of 0.5 μm on both sides of the device due to the photoresist development leads to an increase of 100% in the saturated resistor width compared to only a 10% increase in the switching transistor width. This makes it hard to scale this device.

The insensitivity of the saturation current to the channel length (space between the source and the drain) makes it impossible to scale the current by scaling the channel length to maintain reasonable dimensions. The increase of the channel length leads only to the increase of the saturation voltage which is 0.5V/μm of the channel length (see Chapter(1)).

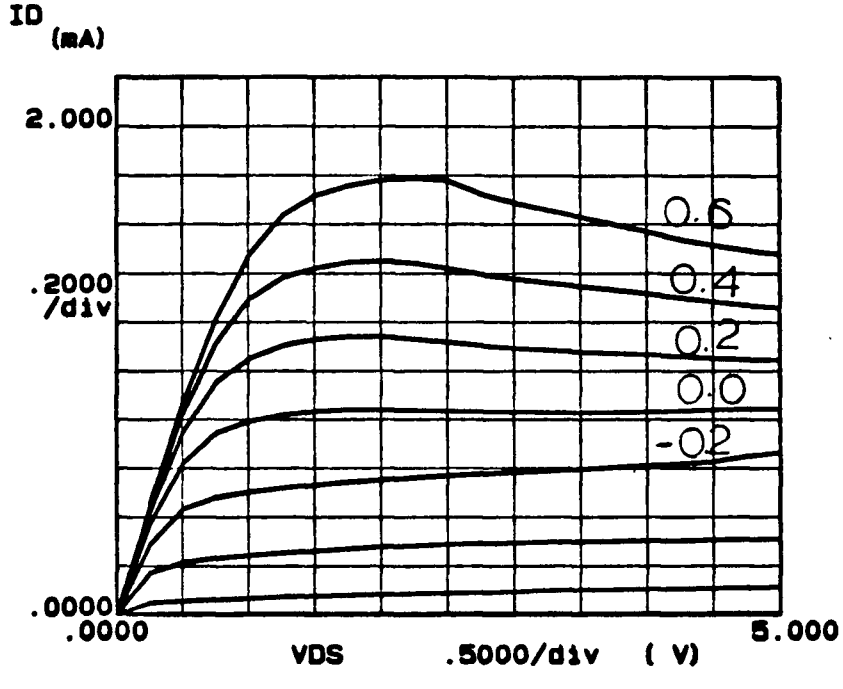
The saturated resistor may not give any advantage when used with the DCFL where the voltage swing is about 0.5V and the saturation voltage is 0.5V/μm, therefore it will act as an ordinary resistor. Reducing the channel width to submicron dimensions will reduce the saturation voltage but the diffusion of the dopant from the highly doped areas may cause a short circuit between the source and the drain if such very small dimensions are used.

The mechanism of current saturation of the saturated resistor is due to the electron velocity saturation. Therefore, the possibility of the effect of the negative conductance appearing is high. Fig.(7-8.a) shows the I-V characteristics of a gateless transistor acting as a saturated resistor where there is an overshoot in the characteristic. Fig.(7-8.b) shows the I-V characteristic of the same device after depositing the gate. From these two Figures one can see that the effect of the negative conductance is nearly unnoticed with V_{gs} = 0 V, while at V_{gs} = 0.6 V, the I-V curve is similar to that of the saturated resistor. This phenomenon can be attributed to the fact that at V_{gs} = 0.6V the depletion region width is nearly zero leading to a channel similar to that of the saturated resistor. The appearance of the negative conductance at the saturation region does not make the saturated resistor an ideal current source element.

The lower sensitivity of the transistor to the negative conductance can be attributed to the nature of current saturation which is due to channel pinch-off or a mix between channel pinch-off and electron velocity saturation. The negative conductivity effect becomes stronger if the channel is uniformly doped. The solution is to implant at lower dose and higher energy



(a)



(b)

Fig.(7-8) (a) I-V characteristics of a transistor without gate metal in place acting as a saturated resistor and (b) same device after putting down the gate metal.

to get a nonuniform (Gaussian) distribution. This method was used with the DAC.

Generally, the saturated resistor has the disadvantages of (a) small diimensions must be used, (b) sensitivity to the surface damage, (c) sensitivity to the negative conductance, and (d) possibility of lateral diffusion if small channel length is used to reduce the saturation voltage value.

CHAPTER(8)

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

The main contributions from this work were as follows.

(1) The fabrication techniques of GaAs MESFETs by ion implantation into SI LEC material were studied. It was found that:

(a) implantation of silicon dopant ions directly into the GaAs substrate results in better parameter uniformity and device quality than implantation through a Si_3N_4 film.

(b) A self aligned gate technique using polyimide (SAGUPI) was developed. It has the advantages of simplicity, high yield and good parameter uniformity.

(c) The temperature-dependence of transistor parameters was investigated. The results imply that the circuit time delay would be nearly constant in the temperature range from -80°C to 80°C.

(2) Ways of implementing logic functions in GaAs were studied. A new logic was proposed (CDFL) which was predicted to offer high speed, low power dissipation, low power-time delay product, and less loading sensitivity.

(3) A need exists for fast digital to analog converters and analog to digital converters. GaAs has the potential to fill this need. Two prototype DACs (one with MESFETs as current sources and the other with saturated resistors) were designed and fabricated. The two converters were tested at low frequencies and the high frequency response was simulated. The simulation has shown that they will be able to operate at frequencies up to 10 GHz.

For future work the following is suggested:

(1) The SAGUPI technique should be applied also to fabricate enhancement mode devices since reduction of series resistance is even more important for

enhancement mode than for depletion mode devices.

(2) Logic should be investigated in which the AND and OR gates are made with CDFL but the inverters (needed to obtain NAND and NOR gates) are made with DCFL. The point here is that the overall number of devices would decrease and this would increase the speed. This combined CDFL-DCFL approach could be realized with GaAs MISFETs as well as MESFETs and also with InP devices.

(3) The CDFL approach was introduced for GaAs but it could also be used with silicon. For example, the CDFL could be used to build AND and OR gates instead of using NAND + inverter and NOR + inverter.

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Appendix(A)

Computer Simulation Programsof the CDFL Approach

Listing of CDFL.S1 at 08:18:53 on SEP 3, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(A) CONT. ############
2     ******* CDFL BUFFER SIMULATION FOR NATCHING WITH
3     ******* THE EXPERIMENTAL RESULTS ******
4     VIN= 3 0 PULSE(3.0V 0.00V 400PS 200PS 200PS 600PS 1800PS)
5     VDD=4 0 DC 3.5
6     VSS=0 1 DC 0.5
7     J2 2 1 1 JM1 1.0 OFF
8     J1 4 3 2 JM1 1.0 OFF
9     *********************************
10    J3 4 2 5 JM1 1.0 OFF
11    J4 5 1 1 JM1 1.0 OFF
12    *********************************
13    .MODEL JM1 NJF VTO=-1.137 RS=170 RD=450 CGS=040FF CGD=040FF
14    +BETA=1.104E-3
15    .PLOT DC V(2)
16    .PLOT TRAN V(2)
17    .DC VIN 0.0 3.0 0.1
18    .TRAN 60PS 1800PS
19    .END
```

Listing of CDFL.S2 at 08:20:47 on SEP 3, 1985 for CCid=NANY Page

```
1     ####### APPENDIX(A) CONT. ##########
2     ******* CDFL INVERTER FOR EXPERIMENTAL RESULTS MATCHING ***
3     VIN= 3 0 PULSE(3.0V 0.00V 0.5NS 0.5NS 0.5NS 1.5NS 4.0NS)
4     VDD=4 0 DC 3.0
5     VSS 0 1 DC 3.0
6     R1 3 2 03K
7     J2 2 1 1 JM2 1.0 OFF
8     J3 4 5 5 JM3 1.0 OFF
9     J4 5 2 0 JM1 OFF
10    J5 4 5 6 JM1 1.0 OFF
11    J6 6 0 0 JM1 1.0 OFF
12    .MODEL JM1 NJF VTO=-1.137 RS=170 RD=450 CGS=40FF CGD=40FF
13    +BETA=1.104E-3
14    .MODEL JM2 NJF VTO=-1.137 RS=243 RD=642 CGS=28FF CGD=28FF
15    +BETA=0.77E-3
16    .MODEL JM3 NJF VTO=-1.137 RS=340 RD=900 CGS=40FF CGD=40FF
17    +BETA=0.276E-3
18    .PLOT DC V(5)
19    .PLOT DC V(2)
20    .PLOT TRAN V(5)
21    .DC VIN 0.0 3.0 0.1
22    .TRAN .1NS 4.0NS
23    .END
```

Appendix(B)

Computer Simulation Programs for GaAs MESFET Logic

```
Listing of CCL.N at 08:09:06 on SEP  3, 1985 for CCid=NANY Page

     1     **********    APPENDIX(B) CONT.    **********
     2     ****     CCL    FAN OUT=3  ****
     3     .WIDTH OUT=80
     4     VIN 4 0 PWL(0 1 0.5NS 1 1.0NS 5 1.5NS 5 2NS 1 2.5NS 1
     5     +3.0NS 5 3.5NS 5 4.0NS 1 4.5NS 1 5NS 5 5.5NS 5 6NS 1 6.5NS 1)
     6     VDD 1 0 DC 5
     7     J1 1 2 2 JM1 0.6 OFF
     8     J2 2 3 0 JM1 1.0 OFF
     9     D1 3 4 DIODE 1.0 OFF
    10     ****************************************
    11     J3 1 5 5 JM1 0.6 OFF
    12     J4 5 6 0 JM1 1.0 OFF
    13     D2 6 2 DIODE 1.0 OFF
    14     ****************************************
    15     J5 1 7 7 JM1 0.6 OFF
    16     J6 7 8 0 JM1 1.0 OFF
    17     D3 8 2 DIODE 1.0 OFF
    18     ****************************************
    19     J7 1 9 9 JM1 0.6 OFF
    20     J8 9 10 0 JM1 1.0 OFF
    21     D4 10 2 DIODE 1.0 OFF
    22     ****************************************
    23     .MODEL JM1 NJF VTO= -2.5 RS=100 RD=100 CGS=5FF CGD=5FF BETA=4.4E-4
    24     .MODEL DIODE D RS=2000 CJO=100FF VJ=0.77 EG=0.77 IS=2.3E-14
    25     .PLOT DC V(2)
    26     .PLOT TRAN V(2)
    27     .DC VIN 0.0 5.0 0.25
    28     .TRAN 50PS 6.5NS
    29     .END
```

Listing of BFL1.N at 08:09:40 on SEP 3, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(B) CONT. #########
2     ***** BFL FAN OUT=4  ****
3     VIN 4 0 PULSE(0.5V -2.5V 0.5NS 0.5NS 0.5NS 0.5NS 2.5NS)
4     VDD 2 0 DC=5.5V
5     VSS 0 1 DC=4.5V
6     J1 2 3 3 JM1 0.6 OFF
7     J2 3 4 0 JM1 1.0 OFF
8     J3 2 3 5 JM1 1.0 OFF
9     J4 7 1 1 JM1 1.0 OFF
10    D1 5 6 DIODE 1.5 OFF
11    D2 6 7 DIODE 1.5 OFF
12    ****************************************
13    J5 2 8 8 JM1 0.6 OFF
14    J6 8 7 0 JM1 1.0 OFF
15    ****************************************
16    J7 2 9 9 JM1 0.6 OFF
17    J8 9 7 0 JM1 1.0 OFF
18    ****************************************
19    J9 2 10 10 JM1 0.6 OFF
20    J10 10 7 0 JM1 1.0 OFF
21    ****************************************
22    J11 2 11 11 JM1 0.6 OFF
23    J12 11 7 0 JM1 1.0 OFF
24    ****************************************
25    .MODEL JM1 NJF VTO=-2.5V RS=100 RD=100 CGS=5FF CGD=5FF BETA=4.4E-4
26    .MODEL DIODE D RS=800 IS=0.58E-14 CJO=5FF VJ=0.77 EG=0.77
27    .PLOT DC V(7)
28    .PLOT DC V(3)
29    .PLOT TRAN V(7)
30    .DC VIN -2.5 0.5 0.1
31    .TRAN 50PS 2.5NS
32    .END
```

Listing of BFL2.N at 08:09:45 on SEP 3, 1985 for CCid=NANY Page

```
1     ######### APPENDIX(B) CONT. #########
2     **** UFL FAN OUT= 3  ******
3     VIN 4 0 PWL(0 -2.5 0.5NS -2.5 1.0NS 0.5 1.5NS 0.5 2NS -2.5 2.5NS
4     +-2.5)
5     VDD 2 0 DC=5.0V
6     VSS 0 1 DC=4V
7     J1 2 3 3 JM1 1.0 OFF
8     J2 3 4 0 JM1 1.8 OFF
9     J3 7 1 1 JM1 0.5 OFF
10    D1 3 5 DIODE 0.8 OFF
11    D2 5 7 DIODE 0.8 OFF
12    ****************************************
13    J4 2 8 8 JM1 1.0 OFF
14    J5 8 7 0 JM1 1.8 OFF
15    ****************************************
16    J6 2 9 9 JM1 1.0 OFF
17    J7 9 7 0 JM1 1.8 OFF
18    ****************************************
19    J8 2 10 10 JM1 1.0 OFF
20    J9 10 7 0 JM1 1.8 OFF
21    ****************************************
22    .MODEL JM1 NJF VTO=-2.5 RS=100 RD=100 CGS=5FF CGD=5FF BETA=4.4E-4
23    .MODEL DIODE D RS=800 CJO=05FF IS=0.58E-14 VJ=0.77 EG=0.77
24    .PLOT DC V(7)
25    .PLOT DC V(3)
26    .PLOT TRAN V(7)
27    .DC VIN -2.5 0.5 0.3
28    .TRAN 50PS 2.5NS
29    .END
```

Listing of CCL at 08:09:56 on SEP 3, 1985 for CCid=NANY Page

```
1     ##### APPENDIX(B) CONT. #####
2     ***** CCL FAN OUT=3  Vth=-1 V  ****
3     VIN 4 0 PWL(0 1 0.5NS 1 1.0NS 5 1.5NS 5 2NS 1 2.5NS 1
4     +3.0NS 5 3.5NS 5 4.0NS 1 4.5NS 1 5NS 5 5.5NS 5 6NS 1 6.5NS 1)
5     VDD 1 0 DC 3
6     J1 1 2 2 JM1 0.6 OFF
7     J2 2 3 0 JM1 1.0 OFF
8     D1 3 4 DIODE 1.0 OFF
9     ****************************************
10    J3 1 5 5 JM1 0.6 OFF
11    J4 5 6 0 JM1 1.0 OFF
12    D2 6 2 DIODE 1.0 OFF
13    ****************************************
14    J5 1 7 7 JM1 0.6 OFF
15    J6 7 8 0 JM1 1.0 OFF
16    D3 8 2 DIODE 1.0 OFF
17    ****************************************
18    J7 1 9 9 JM1 0.6 OFF
19    J8 9 10 0 JM1 1.0 OFF
20    D4 10 2 DIODE 1.0 OFF
21    ****************************************
22    .MODEL JM1 NJF VTO= -1.0 RS=200 RD=200 CGS=5FF CGD=5FF BETA=7.0E-4
23    .MODEL DIODE D RS=2000 CJO=100FF VJ=0.77 EG=0.77 IS=2.3E-14
24    .PLOT DC V(2)
25    .PLOT TRAN V(2)
26    .DC VIN 0.0 5.0 0.25
27    .TRAN 50PS 6.5NS
28    .END
```

Listing of BFL1 at 08:10:06 on SEP 3, 1985 for CCid=NANY Page

```
1     ##### APPENDIX(B) CONT. ######
2     ****** BFL FAN OUT=3 Vth=-1 V ########
3     VIN 4 0 PULSE(0.5V -1.0V 0.5NS 0.5NS 0.5NS 0.5NS 2.5NS)
4     VDD 2 0 DC=3.0V
5     VSS 0 1 DC=1.6V
6     J1 2 3 3 JM1 0.6 OFF
7     J2 3 4 0 JM1 1.0 OFF
8     J3 2 3 5 JM1 1.0 OFF
9     J4 7 1 1 JM1 1.0 OFF
10    D1 5 6 DIODE 1.5 OFF
11    D2 6 7 DIODE 1.5 OFF
12    ****************************************
13    J5 2 8 8 JM1 0.6 OFF
14    J6 8 7 0 JM1 1.0 OFF
15    ****************************************
16    J7 2 9 9 JM1 0.6 OFF
17    J8 9 7 0 JM1 1.0 OFF
18    ****************************************
19    J9 2 10 10 JM1 0.6 OFF
20    J10 10 7 0 JM1 1.0 OFF
21    ****************************************
27    .MODEL JM1 NJF VTO=-1.0V RS=200 RD=200 CGS=5FF CGD=5FF BETA=7.0E-4
28    .MODEL DIODE D RS=800 IS=0.58E-14 CJO=5FF VJ=0.77 EG=0.77
29    .PLOT DC V(7)
30    .PLOT DC V(3)
31    .PLOT TRAN V(7)
32    .DC VIN -1.0 0.5 0.1
33    .TRAN 50PS 2.5NS
34    .END
```

Listing of BFL2 at 08:10:11 on SEP 3, 1985 for CCid=NANY Page -

```
      ####### APPENDIX(B) CONT. ##########
      ******* DFL FAN OUT=3 Vth=-1 V ********
      VIN 4 0 PWL(0 -1.0 0.5NS -1.0 1.0NS 0.5 1.5NS 0.5 2NS -1.0 2.5NS
     +-1.0)
      VDD 2 0 DC=2.8V
      VSS 0 1 DC=1.2V
      J1 2 3 3 JM1 1.0 OFF
      J2 3 4 0 JM1 1.8 OFF
      J3 7 1 1 JM1 0.5 OFF
      D1 3 5 DIODE 0.8 OFF
      D2 5 7 DIODE 0.8 OFF
      ****************************************
      J4 2 8 8 JM1 1.0 OFF
      J5 8 7 0 JM1 1.8 OFF
      ****************************************
      J6 2 9 9 JM1 1.0 OFF
      J7 9 7 0 JM1 1.8 OFF
      ****************************************
      J8 2 10 10 JM1 1.0 OFF
      J9 10 7 0 JM1 1.8 OFF
      ****************************************
      .MODEL JM1 NJF VTO=-1.0 RS=200 RD=200 CGS=5FF CGD=5FF BETA=7.0E-4
      .MODEL DIODE D RS=800 CJO=05FF IS=0.58E-14 VJ=0.77 EG=0.77
      .PLOT DC V(7)
      .PLOT DC V(3)
      .PLOT TRAN V(7)
      .DC VIN -1.0 0.5 0.1
      .TRAN 50PS 2.5NS
      .END
```

Listing of SDFL1 at 08:10:36 on SEP 3, 1985 for CCid=NANY Page

```
      ######## APPENDIX(B) CONT. ##########
      ******* SDFL1 FAN OUT=3 ************
      VIN= 1 0 PULSE(2.6V 0.5V 0.5NS 0.5NS 1.0NS 0.5NS 3.5NS)
      VDD=5 0 DC 2.6
      VSS 0 4 DC 2.0
      D1 1 2 DIODE
      D2 2 3 DIODE 4.5
      J1 3 4 4 JM1 0.70 OFF
      J2 6 3 0 JM1 OFF
      J3 5 6 6 JM1 1.50 OFF
      ************************************************************
      D3 6 7 DIODE
      D4 7 8 DIODE 4.5
      J4 8 4 4 JM1 0.7 OFF
      ************************************************************
      D5 6 9 DIODE
      D6 9 10 DIODE 4.5
      J5 10 4 4 JM1 0.7 OFF
      ************************************************************
      D7 6 11 DIODE
      D8 11 12 DIODE
      J6 12 4 4 JM1 0.7 OFF
      ************************************************************
      .MODEL JM1 NJF VTO=-1.0 RD=200 RS=200 CGS=005FF CGD=005FF BETA=7E-4
      .MODEL DIODE D RS=730 CJO=2FF VJ=0.7 EG=0.7
      .PLOT DC V(6)
      .PLOT TRAN V(6)
      .DC VIN 0.0 2.6 0.25
      .TRAN 50PS 3.5NS
      .END
```

Listing of SDFL2.N at 08:10:44 on SEP 3, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(B) CONT. #########
2     ******** SDFL2 FAN OUT=3  **********
3     VIN 3 0 PULSE(3V 0.5V 0.5NS 0.5NS 0.5NS 0.5NS 2.5NS)
4     VDD 2 0 DC 3.0
5     VSS 0 1 DC 2.0
6     D1 3 4 DIODE 5 OFF
7     D2 4 5 DIODE 5 OFF
8     D3 5 6 DIODE 5 OFF
9     J1 6 1 1 JM1 0.70 OFF
10    J2 7 6 0 JM1 1.4 OFF
11    J3 2 7 7 JM1 1.0 OFF
12    J4 2 7 8 JM1 1.4 OFF
13    J5 8 6 0 JM1 0.5 OFF
14    ****************************************
15    D4 8 9 DIODE 5 OFF
16    D5 9 10 DIODE 5 OFF
17    D6 10 11 DIODE 5 OFF
18    J6 11 1 1 JM1 0.7 OFF
19    ****************************************
20    D7 8 12 DIODE 5.0 OFF
21    D8 12 13 DIODE 5.0 OFF
22    D9 13 14 DIODE 5.0 OFF
23    J7 14 1 1 JM1 0.7 OFF
24    ****************************************
25    D10 8 15 DIODE 5.0 OFF
26    D11 15 16 DIODE 5.0 OFF
27    D12 16 17 DIODE 5.0 OFF
28    J8 17 1 1 JM1 0.7 OFF
29    ****************************************
30    .MODEL JM1 NJF VTO=-1.0 RD=200 RS=200 CGS=005FF CCD=005FF BETA=7E-4
31    .MODEL DIODE D RS=800 CJO=5FF VJ=0.77 EG=0.77  IS=.580E-14
32    .PLOT DC V(6)
33    .PLOT DC V(7)
34    .PLOT TRAN V(7)
35    .PLOT DC V(8)
36    .PLOT TRAN V(8)
37    .DC VIN 0.0 3 0.25
38    .TRAN 50PS 2.5NS
39    .END
```

Listing of CDFL1.N at 07:29:41 on SEP 9, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(B) CONT. #########
2     ****** CDFL.I1 FAN OUT=3 ********
3     VIN= 7 0 PULSE(2.5V 0.0V 0.2NS 0.2NS 0.2NS 0.2NS 1.0NS)
4     VDD=4 0 DC 2.5
5     VSS 0 1 DC 2.0
6     J7 4 7 3 JM2  1.0 OFF
7     J8 3 0 0 JM2  1 OFF
8     R1 3 2 3.0K
9     J2 2 1 1 JM1 0.7 OFF
10    J3 4 5 5 JM1 1.00 OFF
11    J4 5 2 0 JM1 OFF
12    ********************************************
13    J5 4 5 6 JM2  OFF
14    J6 6 0 0 JM2  OFF
15    ************************************************
16    J9 4 5 8 JM2 OFF
17    J10 8 0 0 JM2 OFF
18    ************************************************
19    J11 4 5 9 JM2 OFF
20    J12 9 0 0 JM2 OFF
21    ************************************************
22    .MODEL JM1 NJF VTO=-1.0 RD=200 RS=200 CGS=5FF CGD=5FF BETA=7E-4
23    .MODEL JM2 NJF VTO=-0.5 RS=400  RD=400  CGS=05FF CGD=5FF
24    +BETA=1.0E-3
25    .PLOT DC V(5)
26    .PLOT TRAN V(5)
27    .DC VIN 0.0 2.5 0.1
28    .TRAN 020PS 1.0NS
29    .END
```

```
      ####### APPENDIX(B) CONT. ######
      ******* SCFL FAN OUT=3 *********
      VIN 5 0 PWL(0 -1.2 1.0NS -1.2 2.0NS -2.4 3NS -2.4 4.0NS -1.2 5.0NS
     + -1.2)
      VSS 1 0 DC=-5V
      VREF 8 0 DC= -1.8
      R1 4 1 10K
      R2 0 2 5K
      R3 6 1 10K
      R4 0 7 5K
      R5 10 1 10K
      D1 3 4 DIODE 4.0 OFF
      D2 9 10 DIODE 4.0 OFF
      J1 0 2 3 JM1 1.0 OFF
      J2 2 5 6 JM1 1.0 OFF
      J3 7 8 6 JM1 1.0 OFF
      J4 0 7 9 JM1 1.0 OFF
      ********************************************************
      R6 11 1 10K
      R7 0 14 5K
      R8 0 15 5K
      J5 14 10 11 JM1 1.0 OFF
      J6 15 8 11 JM1 1.0 OFF
      ********************************************************
      R9 0 16 5K
      R10 0 17 5K
      R11 12 1 10K
      J7 16 10 12 JM1 1.0 OFF
      J8 17 8 12 JM1 1.0 OFF
      ********************************************************
      R12 0 18 5K
      R13 0 19 5K
      R14 13 1 10K
      J9 18 10 13 JM1 1.0 OFF
      J10 19 8 13 JM1 1.0 OFF
      ********************************************************
      .MODEL JM1 NJF VTO=-0.1 RS=450 RD=450 CGS=5FF CGD=5FF
     +BETA=1.4E-3
      .MODEL DIODE D RS=80 IS=1.7E-13 CJO=225FF EG=0.77 VJ=0.77
      .PLOT DC V(4)
      .PLOT TRAN V(4)
      .DC VIN -2.4 -1.2 0.1
      .TRAN 50PS 5.0NS
      .END
```



```
      ######## APPENDIX(B) CONT. #######
      ******** DCFL FAN OUT=3 **********
      VIN 4 0 PULSE(0.7V -0.001 0.4NS 0.2NS 0.2NS 0.4NS 1.6NS)
      VDD 2 0 DC=0.8
      J1 2 3 3 JM2 1.6 OFF
      J2 3 4 0 JM1 1.0 OFF
      ************************************
      J3 2 5 5 JM2 1.6 OFF
      J4 5 3 0 JM1 1.0 OFF
      ************************************
      J5 2 6 6 JM2 1.6 OFF
      J6 6 3 0 JM1 1.0 OFF
      ************************************
      J7 2 7 7 JM2 1.6 OFF
      J8 7 3 0 JM1 1.0 OFF
      ************************************
      .MODEL JM1 NJF VTO=0.200 RS=400 RD=400 CGS=5FF CGD=5FF BETA=1.5E-3
      .MODEL JM2 NJF VTO=-0.3   RS=400 RD=400 CGS=5FF CGD=5FF BETA=1.2E-3
      .PLOT DC V(3)
      .PLOT TRAN V(3)
      .DC VIN 0 0.7 0.1
      .TRAN 40PS 1.6NS
      .END
```

Listing of LP1D at 08:11:19 on SEP 3, 1985 for CCid=NANY Page

```
      1     ####### APPENDIX(B) CONT. ########
      2     ********* LP1D FAN OUT=3 ***********
      3     VIN 4 0 PWL(0 0 0.4NS 0 0.6NS 0.85 1NS 0.85 1.2NS 0 1.6NS 0)
      4     VDD 2 0 DC=3.0V
      5     R1 2 3 10K
      6     R2 6 0 3.3K
      7     D1 5 6 DIODE 1.0 OFF
      8     J1 3 4 0 JM1 1.0 OFF
      9     J2 2 3 5 JM1 1.5 OFF
     10     ************************************
     11     R3 2 7 10K
     12     J3 7 6 0 JM1 1.0 OFF
     13     ************************************
     14     R4 2 8 10K
     15     J4 8 6 0 JM1 OFF
     16     ************************************
     17     R5 2 9 10K
     18     J5 9 6 0 JM1 OFF
     19     ************************************
     20     .MODEL JM1 NJF VTO=-.1 RS=450 RD=450 CGS=5FF CGD=5FF BETA=1.4E-3
     21     .MODEL DIODE D RS=400 CJO=10FF IS=1.16E-14 EG=0.77 VJ=0.77
     22     .PLOT DC V(6)
     23     .PLOT DC V(3)
     24     .PLOT TRAN V(6)
     25     .DC VIN 0 0.85 0.05
     26     .TRAN 40PS 1.6NS
     27     .END
```

Listing of LP3D at 08:11:24 on SEP 3, 1985 for CCid=NANY Page

```
      1     ####### APPENDIX(B) CONT. #######
      2     ****** LP3D FAN OUT=3 ***********
      3     VIN 4 0 PWL(0 0 0.5NS 0 0.9NS 0.75 1.5NS 0.75 2.0NS 0 2.5NS 0)
      4     VDD 2 0 DC=3.0V
      5     R1 2 3 06K
      6     R2 6 0 3.3K
      7     D1 3 6 DIODE 2.0 OFF
      8     J1 3 4 0 JM1 1.0 OFF
      9     ************************************
     10     R3 2 5 06K
     11     J3 5 6 0 JM1 1.0 OFF
     12     ************************************
     13     R4 2 7 6K
     14     J4 7 6 0 JM1 1 OFF
     15     ************************************
     16     R5 2 8 6K
     17     J5 8 6 0 JM1 1 OFF
     18     ************************************
     19     .MODEL JM1 NJF VTO=-0.1 RS=450 RD=450 CGS=5FF CGD=5FF BETA=1.4E-3
     20     .MODEL DIODE D RS=400 CJO=10FF IS=1.16E-14 EG=0.77 VJ=0.77
     21     .PLOT DC V(6)
     22     .PLOT DC V(3)
     23     .PLOT TRAN V(6)
     24     .DC VIN 0 0.75 0.05
     25     .TRAN 50PS 2.5NS
     26     .END
```

Listing of CDFL1 at 08:12:11 on SEP 3, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(B) CONT. ########
2     ****** CDFL.B FAN OUT=3 ***********
3     VIN= 3 0 PULSE(2.5V 0.00V 200PS 100PS 100PS 200PS 800PS)
4     VDD=4 0 DC 2.5
5     VSS=0 1 DC 0.50
6     J2 2 1 1 JM1 OFF
7     J1 4 3 2 JM1 OFF
8     *********************************
9     J3 4 2 5 JM1 OFF
10    J4 5 1 1 JM1 OFF
11    *********************************
12    J5 4 2 6 JM1 OFF
13    J6 6 1 1 JM1 OFF
14    *********************************
15    J7 4 2 7 JM1 OFF
16    JM 7 1 1 JM1 OFF
17    *********************************
18    .MODEL JM1 NJF VTO=-0.5 RD=400 RS=400 CGS=05FF CGD=05FF
19    +BETA=1.4E-3
20    .PLOT DC V(2)
21    .PLOT TRAN V(2)
22    .DC VIN 0.0 2.5 0.1
23    .TRAN 20PS 800PS
24    .END
```

Listing of FFL.N at 08:09:25 on SEP 3, 1985 for CCid=NANY Page

```
1     ########  APPENDIX(B) CONT.  ##########
2     ****  FFS  FAN OUT=3  ****
3     VIN 4 0 PULSE(0.5V -2.5V 0.5NS 0.5NS 0.5NS 0.5NS 2.5NS)
4     VDD 2 0 DC=6V
5     VSS 0 1 DC=4V
6     J1 2 3 3 JM1 0.6 OFF
7     J2 3 4 0 JM1 1.0 OFF
8     J3 2 3 5 JM1 0.25 OFF
9     J4 7 1 1 JM1 0.25 OFF
10    D1 5 6 DIODE 0.3 OFF
11    D2 6 7 DIODE 0.3 OFF
12    D3 7 3 DIODE2 1.0 OFF
13    ******************************************
14    J5 2 8 8 JM1 0.6 OFF
15    J6 8 7 0 JM1 1.0 OFF
16    ******************************************
17    J7 2 9 9 JM1 0.6 OFF
18    J8 9 7 0 JM1 1.0 OFF
19    ******************************************
20    J9 2 10 10 JM1 0.6 OFF
21    J10 10 7 0 JM1 1.0 OFF
22    ******************************************
23    J11 2 11 11 JM1 0.6 OFF
24    J12 11 7 0 JM1 1.0 OFF
25    ******************************************
26    ..MODEL JM1 NJF VTO=-2.5V RS=100 RD=100 CGS=5FF CGD=5FF BETA=4.4E-4
27    .MODEL DIODE D RS=800 IS=0.58E-14 CJO=5FF VJ=0.77 EG=0.77
28    .MODEL DIODE2 D RS=2000 CJO=100FF IS=2.3E-14 VJ=0.77 EG=0.77
29    .PLOT DC V(7)
30    .PLOT TRAN V(7)
31    .DC VIN -2.5 0.5 0.1
32    .TRAN 50PS 2.5NS
33    .END
```

Listing of CDFL1 at 08:12:11 on SEP 3, 1985 for CCid=NANY Page

```
1     ######## APPENDIX(B) CONT. ########
2     ****** CDFL.B FAN OUT=3 ***********
3     VIN= 3 0 PULSE(2.5V 0.00V 20OPS 100PS 100PS 200PS 800PS)
4     VDD=4 0 DC 2.5
5     VSS=0 1 DC 0.50
6     J2 2 1 1 JM1 OFF
7     J1 4 3 2 JM1 OFF
8     *********************************
9     J3 4 2 5 JM1 OFF
10    J4 5 1 1 JM1 OFF
11    *********************************
12    J5 4 2 6 JM1 OFF
13    J6 6 1 1 JM1 OFF
14    *********************************
15    J7 4 2 7 JM1 OFF
16    JM 7 1 1 JM1 OFF
17    *********************************
18    .MODEL JM1 NJF VTO=-0.5 RD=400 RS=400 CGS=05FF CGD=05FF
19    +BETA=1.4E-3
20    .PLOT DC V(2)
21    .PLOT TRAN V(2)
22    .DC VIN 0.0 2.5 0.1
23    .TRAN 20PS 800PS
24    .END
```

Listing of FFL.N at 08:09:25 on SEP 3, 1985 for CCid=NANY Page

```
1     ########  APPENDIX(B) CONT.  ##########
2     ****  FFS  FAN OUT=3  ****
3     VIN 4 0 PULSE(0.5V -2.5V 0.5NS 0.5NS 0.5NS 0.5NS 2.5NS)
4     VDD 2 0 DC=6V
5     VSS 0 1 DC=4V
6     J1 2 3 3 JM1 0.6 OFF
7     J2 3 4 0 JM1 1.0 OFF
8     J3 2 3 5 JM1 0.25 OFF
9     J4 7 1 1 JM1 0.25 OFF
10    D1 5 6 DIODE 0.3 OFF
11    D2 6 7 DIODE 0.3 OFF
12    D3 7 3 DIODE2 1.0 OFF
13    ******************************************
14    J5 2 8 8 JM1 0.6 OFF
15    J6 8 7 0 JM1 1.0 OFF
16    ******************************************
17    J7 2 9 9 JM1 0.6 OFF
18    J8 9 7 0 JM1 1.0 OFF
19    ******************************************
20    J9 2 10 10 JM1 0.6 OFF
21    J10 10 7 0 JM1 1.0 OFF
22    ******************************************
23    J11 2 11 11 JM1 0.6 OFF
24    J12 11 7 0 JM1 1.0 OFF
25    ******************************************
26    .MODEL JM1 NJF VTO=-2.5V RS=100 RD=100 CGS=5FF CGD=5FF BETA=4.4E-4
27    .MODEL DIODE D RS=800 IS=0.58E-14 CJO=5FF VJ=0.77 EG=0.77
28    .MODEL DIODE2 D RS=2000 CJO=100FF IS=2.3E-14 VJ=0.77 EG=0.77
29    .PLOT DC V(7)
30    .PLOT TRAN V(7)
31    .DC VIN -2.5 0.5 0.1
32    .TRAN 50PS 2.5NS
33    .END
```

APPENDIX(C)

Recipes for GaAs Fabrication Processes

Appendix(C-1) GaAs PROCESSING TECHNOLOGY

---

1. PRECLEANING

A. Degreasing

a. 5 minutes in boiling trichlorethylene

b. 5 minutes in boiling acetone

c. 5 minutes in boiling 2-propanol

B. Damaged Layer Etch

a. immerse for 2 minutes in $4H_2SO_4$: $1H_2O_2$: $1H_2O$ by volume at room temperature.

b. 3 to 5 minutes in boiling concentrated HCl

2. REGISTRATION MARKS

A. Photo Resist Patterning

a. spin photo resist at 4500 r.p.m. for 20 seconds

b. soft bake at 70°C for 30 minutes

c. expose photo resist (under appropriate mask) for 1.5 minutes at 10 mW/cm^2

d. develop pattern in Shipley MF312 Developer for about 15 seconds

e. hard bake at 125°C for 30 minutes (required only when etching Si_3N_4)

Appendix(C-1) GaAs PROCESSING TECHNOLOGY - cont'd

B. Registration Marks Etch

a. 1 minute immersion in 10% HCl

b. 1 minute rinse in D.I. H_2O

c. 50 seconds immersion in 5% H_3PO_4 : 2.5% H_2O_2 : 92.5% D.I. H_2O

d. 5 minutes rinse in D.I. H_2O

C. Photo Resist Layer Removal

a. immerse in warm acetone

3. n-IMPLANT

A. Photo Resist Patterning

a. repeat 2A above

B. Implant

a. implant using the appropriate dose and energy

C. Photo Resist Removal

a. immerse in warm acetone (this will remove most of the photo resist); to be certain of complete removal of the photo resist

Appendix(C-1) GaAs PROCESSING TECHNOLOGY - cont'd

either of the following is recommended:

i. Oxygen Ashing (see Process(3-2))

ii. Shipley's Microposit Remover 140

- immerse in remover 140 which is heated to about 100°C
- immerse for 15 seconds in buffered H.F.

4. POST-IMPLANT ANNEAL

A. Si_3N_4 Layer (see Process(3-3)

B. Anneal in Mini-Brute

a. anneal at 850°C for 25 minutes

b. the following steps are recommended:

i. place wafer at the edge of furnace for 5 minutes to warm it up

ii. push wafer into the centre of the furnace for 25 minutes

iii. after the required time interval in the furnace, pull wafer out to the edge of the furnace and leave it there for 5 minutes to cool down

C. Si_3N_4 Layer Removal

a. immerse in H.F.

Appendix(C-1) GaAs PROCESSING TECHNOLOGY - cont'd

5. DRAIN AND SOURCE CONTACTS

A. Photo Resist Patterning

a. repeat 2A but this time soak the wafer in chlorobenzene for 2 minutes after developing to obtain "overcharging" resist profile

B. AuGe Deposition

a. lay down 1500Å thick layer of Au-Ge

b. perform single lift-off in warm acetone to remove the unwanted metal

c. if b does not work, do lift-off in resist remover

d. alloy in Mini Brute at 450°C for 2 minutes and check the contact. Alloy further if ohmic contact is not yet achieved

6. GATE METAL

A. repeat 2A

B. immerse the wafer after developing into BHF for 15 seconds and then D.I. water for 15 seconds

C. lay down ~ 2000Å thick layer of Al

D. repeat $4.B_b$

Appendix(C-2) O_2 PLASMA ASHING FOR POLYIMIDE AND PHOTORESIST

1. Flush the system before loading

2. Load the samples

3. Purge the system with N_2 for 3 minutes

4. Pump down the chamber

5. Set the parameters

   O_2 flow = 200

   pressure = 250

   power = 200W

   T = 120°C

   tune = 60

   load = 115

6. Wait 5 minutes for the parameters to stabilize and then apply the power

7. After finishing, turn the power off, the gas valve off, and the pressure valve off.

8. Pump the chamber down and unload the samples

Appendix(C-3) Si_3N_4 DEPOSITION

1. Turn ON the plasma machine and pump down.
2. Flush the system to get rid of any gas residues.
3. Vent the chamber and raise the cover to load the samples.
4. After loading, pump the chamber down again and set the temperature to 310°C
5. When the temperature reaches the set value, flush the chamber prior to the application of any gases.
6. Check the gas, temperature, pressure, power, tune and load setting for ammonia plasma which is used to clean the GaAs surface before Si_3N_4 deposition
7. Ammonia plasma parameters should be:

   Ammonia = 37.6 SCCM

   power = 100W

   pressure = 500 mTorr

   temperature = 310°C

   tune = 69

   load = 110
8. Before applying the plasma wait about 5 minutes for the gases and the pressure to stabilize then turn the power ON
9. After finishing, turn the power off, gas valve off, and pressure valve off

Appendix(C-3) Si_3N_4 DEPOSITION - cont'd.

10. Check the settings for Si_3N_4 deposition. These are:

    Ammonia = 37.6 SCCM

    Helium = 500 SCCM

    Silane = 550 SCCM

    pressure = 1500 mTorr

    power = 100W

    temperature = 310°C

    tune = 86

    load = 103

11. Wait for the gases to stabilize and then apply the plasma, the rate of deposition will be 170Å/minute.

12. When finished, turn the power off, gases valves off, and pressure valve off.

13. Flush the system and unload the samples.

Appendix(C-4) SiO_2 DEPOSITION

1. After loading the sample, pump down the chamber to 1×10^{-6} Torr.

2. Apply Ar only; the pressure should be 3.5×10^{-3} Torr.

3. When the pressure stabilizes, apply the power (100W with reflected power of no more than 10W).

4. When finished, turn off the power and the gas and unload the sample.

Appendix(C-5) Si_3N_4 ETCHING WITH CF_4 PLASMA

1. Repeat steps 1-4 in process(3-2)

2. Set the parameters

   CF_4 flow = 20 SCCM

   pressure = 500 mTorr

   power = 250W

   temperature = 100°C

   load = 79

   tune = 115

3. repeat steps 6-8 in process(3-2)