GALLIUM ARSENIDE MATERIALS AND DEVICE FABRICATIONS

by

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ABSTRACT

The purpose of this work was to study certain aspects of device fabrication and material properties of ion implanted MESFETs in semi-insulating LEC GaAs. The fabrication technology and materials properties of GaAs are presently the chief limitations in the way of application of GaAs ion-implanted devices in high speed circuits. One part of the work involved studies on the effects of etching away the surface layers of the starting semi-insulating LEC GaAs. The point here is that it appears that impurities and other defects can sometimes be concentrated at the surface. A test structure containing MESFETs, Schottky diodes and van der Pauw crosses was fabricated using ion implantation on etched and unetched substrates. Improved activation and device characteristics were found on the etched sample. The second part of the work involved studies of the effects of dislocations on device characteristics. The topic is important because dislocations may give scatter in the threshold voltage of MESFETs which would, naturally, become a problem for large scale integration. Arrays of devices were fabricated and their characteristics measured. The position of dislocations was located by etching in such a way as to leave the ghost of the devices behind. The results were unfortunately not conclusive because of the difficulty in accurately etching the samples. We were subsequently forced to use fewer samples than planned.

Table of Contents

LIST Of FIGURES

LIST OF FIGURES

LIST OF TABLES

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1. INTRODUCTION

Increasing demand for high speed circuits in digital logic and microwave devices; for example, in real-time signal processing, continuous voice recognition and direct satellite broadcasting has stimulated interest in GaAs [1]. GaAs is electronically superior to Si in that [2]:

1. Its 5 to 6 times higher electron mobility than silicon can be exploited for higher speeds.

2. The readily available semi-insulating (SI) GaAs substrate reduces interconnect parasitic capacitances and provide a natural way for isolating devices making device isolation simple.

3. The low field at which the electron drift velocity saturates in GaAs as compared with Si (figure 1.1) allows the high saturation velocity to be reached at lower voltages than for Si. This lowers power dissipation.

4. Other inherent advantages of GaAs over Si include the ability to work at higher temperatures and better resistance to radiation.

However, as with Si technology years ago, GaAs researchers are faced with problems of poor substrate and device uniformity. The fact that GaAs is a compound material makes its processing and synthesis more complicated than those of Si.

Early GaAs devices were fabricated on buffer layers formed using epitaxial techniques. The buffer layer was used to isolate the active layer from the unpredictable substrate. Some problems of the substrate include high residual impurity concentration and surface conversion during thermal treatment [3]. Better control of impurity incorporation during crystal growth has eliminated the need to intentionally dope GaAs with Cr. The Cr compensates shallow donor levels (like that due to Si) rendering the GaAs material SI [4]. The availabilty of purer GaAs wafers has made direct

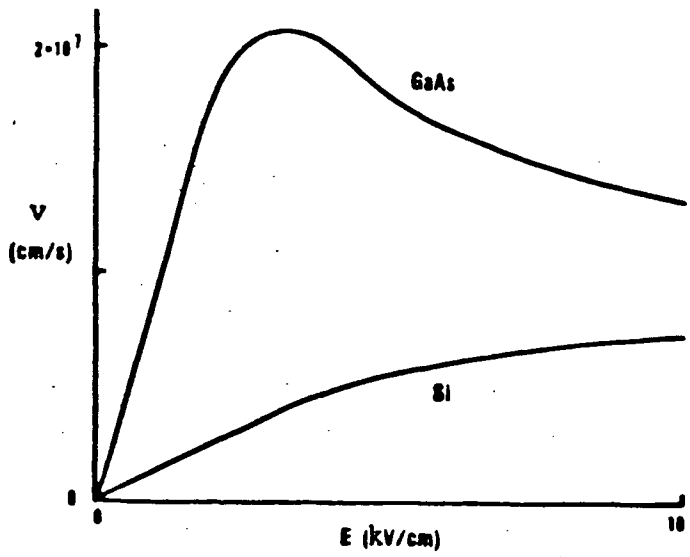


Figure 1.1: Electron Velocity As A Function Of Electric Field In GaAs and Si [5]

implantation for the formation of the active layer feasible.

Although, the purity of the GaAs substrate has been improved, the substrate requirements for direct ion-implantation are very severe. The work performed here is concerned with processing and materials problems of GaAs. Specifically, (1), the activation process is not fully controllable. This is particularly important for enhancement devices used in direct coupled logic which is the key to very large scale integration (VLSI) as opposed to large scale integration (LSI) for GaAs [6]. (2), as circuits become increasingly complex and dense, the non-uniformity of the substrate can be a problem. Some non-uniformity is commonly attributed to dislocations which are known to follow a W-shaped variation across the wafer [7].

In chapter 2, a brief description of GaAs growth and fabrication technology will be given and two problems associated with the development of GaAs integrated circuits will be identified. In chapter 3, the effects of a surface etch will be studied. Chapter 4 will look into the effects of dislocations in the GaAs crystals on discrete metal semiconductor field effect transistor (MESFET) characteristics. Finally, in chapter 5, a summary of the results obtained and some suggestions for future work will be presented.

2. GAAS GROWTH AND FABRICATION TECHNOLOGY

2.1 INTRODUCTION

The first GaAs integrated circuit (IC) was reported by Van Tuyl et al. [8] in 1974. It was made using epitaxial layers on Cr doped SI Bridgman wafers. Since then, GaAs ICs with increasing complexity have been demonstrated. They are based on the availabilty of large undoped SI liquid-encapsulated Czochralski (LEC) GaAs wafers and the change to direct ion-implantation technology requiring no epitaxial buffer layer.

Undoped GaAs wafers of 3 inch diameter can now be routinely produced with LEC pullers. Current improvements in the growth technology include the use of magnetic field during crystal growth [9] and the addition of In to reduce crystal defects [10]. Lower impurity content and the large size and round shape has made undoped LEC GaAs the preferred substrate over Bridgman GaAs.

Ion-implantation directly into the SI substrate provides reasonably good control of the dopant profile. With the aid of an implant mask, good selectivity of the implant area can be achieved. In addition, planar fabrication using ion implantation to form the active layer has a higher throughput and a lower cost. The emergence of rapid thermal annealing techniques make it possible to cure an implant area in seconds. This reduces impurity diffusion which could prevent the control of the doping in the thin active layer of MESFETs to the extent needed for good device threshold voltage uniformity. Most GaAs logic are still based on depletion devices because of the difficulty of making good enhancement transistors with uniform threshold voltage and high transconductance. Depletion devices, for example in buffered field effect transistor logic (BFL) and Schottky

diode field effect transistor logic (SDFL), require level shifting and could cause power dissipation problems in densely packed circuits [2].

In the next section we will discuss the development of GaAs crystal growth.

2.2 CRYSTAL GROWTH

Until recently, most SI GaAs was made by the Bridgman process. In Bridgman growth [11], the polycrystalline GaAs melt is contained in a boat usually made of quartz. To promote crystallisation, the melt is cooled from one end of the crucible to the other. In order to achieve GaAs of a specific orientation, a seed of that orientation is placed at the end of the crucible where the melt is first cooled. Figure 2.1 gives a schematic of the

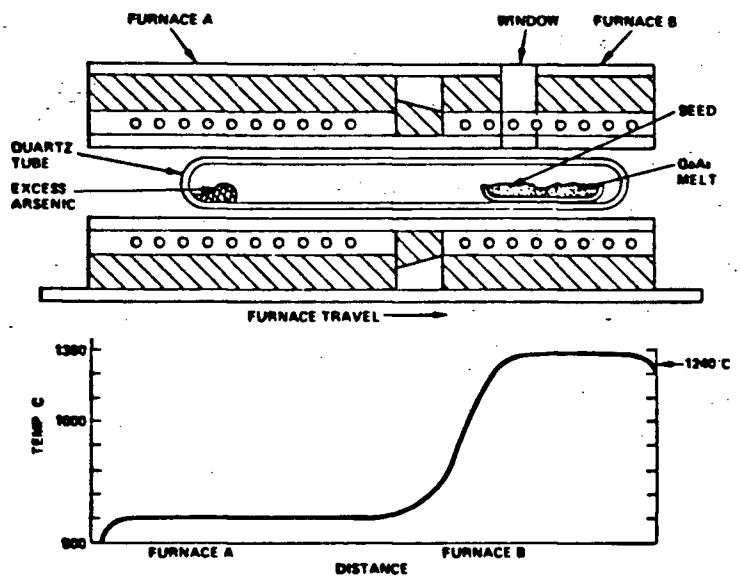


Figure 2.1: Schematic Of Bridgman Growth [11]

Bridgman growth apparatus. Characteristically, D-shaped slices obtained from Bridgman grown GaAs are a deterrent to achieving a cost effective manufacturing technology because much of the standard processing equipment for silicon technology relies on large round substrates [12]. Although it is true that Bridgman wafers generally have lower and more uniform dislocation density because of less stress due to slower cooling they are plagued with the problem of Cr redistribution as Cr is required to compensate shallow donors such as Si [4].

Fused quartz boats that are used to hold the melt tend to dope the GaAs with Si which is a shallow donor when present on a Ga site. As mentioned above, Cr was added to the melt to compensate the shallow donor level created by Si. However the intentionally introduced impurity, Cr, accumulates at the surface when the material is subjected to temperatures of 800°C or higher, for 30 minutes or longer during post implant anneal [13]. As a result, a deficit of Cr is created just beneath the surface, causing the slice to convert to n-type. In addition, Cr also reduces electron mobility in the channel because of increased impurity scattering [14]. Consequently, an epitaxial buffer layer was used. The channel can be formed either by a n-type buffer layer or by direct ion-implantation into Cr-free epitaxial SI GaAs.

The problems associated with Cr are no longer an issue because the SI property of GaAs can now be attained without Cr. The present state of the art LEC pullers grow undoped SI and high purity ingots by using pyrolytic boron nitride (PBN) crucibles and extremely pure Ga and As. In undoped SI substrates, the SI property is believed to be the result of a deep donor known as EL2 compensating shallow acceptors the most abundant of which is carbon [15]. Although the identity of EL2 is not

established, there is evidence from electron spin resonance (ESR) studies that the antisite defect As on a Ga site formed during post-growth annealing is involved [16]. Midgap level EL2 concentration is strongly affected by melt composition [17].

The LEC process is a variation of the Czochralski method used for pulling silicon ingots [18]. Modifications have to be made to the original Czochralski process because GaAs tends to dissociate into its constituent elements when it is heated over 400°C. This is caused by the high vapour pressure of arsenic at temperatures over 400°C. As the the name implies, LEC growth uses an inert molten layer of B_2O_3 to cap the melt. To prevent As from bubbling through the B_2O_3 encapsulant, the growth chamber is pressurised by an inert gas such as Ar or Ne. The B_2O_3 layer has an added advantage in that a film of that liquid remains on the GaAs as it crystalises preventing As loss from the solidified but still hot crystals. The H_2O content of the B_2O_3 encapsulant also has an effect on the purity of resulting ingot. Specifically, the incorporation of C, B and Si can be suppressed by increasing the H_2O content of B_2O_3 [19].

The GaAs charge for LEC growth using the high pressure Melbourn pullers (as used by Cominco) is formed *in situ* because a purer charge is obtained. Essentially, LEC growth involves inserting a GaAs seed of the required orientation through the B_2O_3 layer into the melt which is contained in a graphite or PBN crucible. The seed is then slowly pulled out of the melt, typically at speeds of 10 millimeters per hour. A schematic of GaAs growth by LEC is given in figure 2.2. The crystal grows by progressive freezing at the liquid-solid interface. To minimise thermal forces during freezing, the liquid-solid interface must be kept as flat as possible. This flatness is obtained by spinning the seed as it is pulled out of the melt

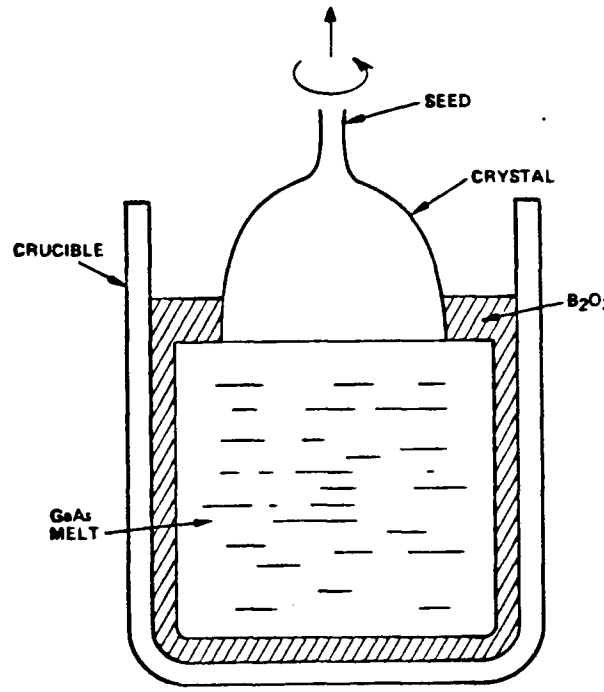


Figure 2.2: Schematic Of LEC GaAs Growth [18]

and often, the crucible is simultaneously counter rotated.

Despite all the recent advances in crystal technology, growth of boules with uniform properties is still not possible. Thomas et al. [20] have found that undoped SI boules grown in PBN crucibles by the high pressure LEC technique exhibit a seed to tail increase in resistivity. Across the wafer, Holmes et al. [21] confirmed the W-shaped of the EL2 profile observed by Martin et al. [22] only at the seed section of the boule. Towards the tail end, the distribution becomes more diffuse and uniform.

2.3 PLANAR FABRICATION TECHNOLOGY

The two GaAs based field effect transistors (FETs) are the MESFET and junction field effect transistor (JFET). The MESFET is by far the dominant GaAs device because its Schottky gate is much easier to fabricate than the PN junction in the JFET. The GaAs MESFET was first proposed by Mead [23] in 1966 and subsequently fabricated by Hooper et al. [24] using a GaAs epitaxial layer. Bipolar transistors on GaAs are also possible. The two types of bipolar transistors demonstrated are homojunction [25] and heterojunction [26] transistor. The former can be fabricated using ion implantation but the latter requires sophisticated molecular beam epitaxy to grow the GaAs-AlGaAs heterojunction needed.

In order to achieve the degree of integration of GaAs ICs demonstrated, for example at a recent conference [27], such as the 1K gate array, 12 bit digital to analog converter and 8:1 multiplexer, among others, a controlled and reproducible fabrication technology must exist. Planar fabrication technology, like the one used at Rockwell meets the requirements of such a process [28]. Direct ion-implantation is the key to a viable planar fabrication technology. It provides better selectivity and higher throughput than earlier epitaxial techniques which help to reduce device fabrication cost.

Planar processes rely on ion implantation for the formation of the active layer and the SI substrate for isolation [28] except that if a blanket implant is used activation is followed by an isolation implant or a 'MESA' etch. H or B ions [29] are used to create a damage layer for isolation. In the Rockwell process illustrated in figure 2.3, the SI is used for isolation. Conventional MESFETs such as those produced by the Rockwell process have high gate to source and gate to drain series resistances which limit

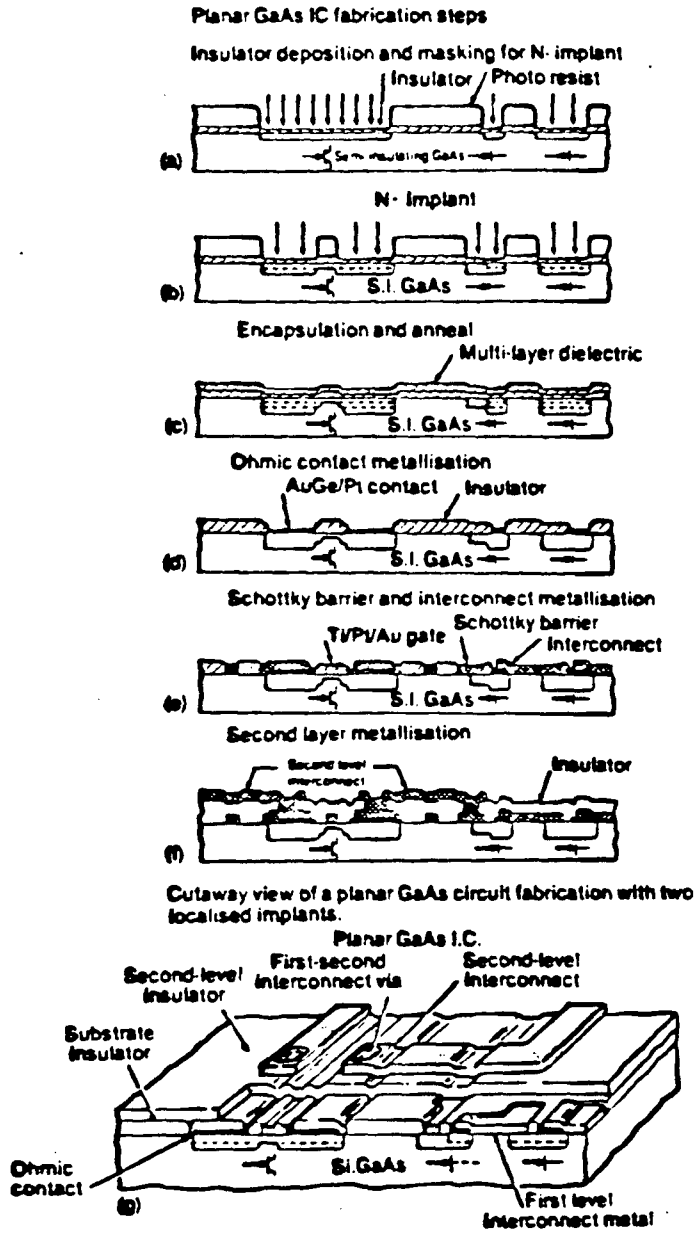


Figure 2.3: Rockwell's Planar Fabrication Process [28]

the speed and the tranconductance [30]. To reduce these parasitic resistances, a high concentration region is placed immediately adjacent to the gate. Self-aligned gate (SAG) techniques are used to fabricate devices with extremely low gate to drain and gate to source resistances. The self-aligned implantation for N^+ layer technology (SAINT) process illustrated in figure 2.4 uses a SiO_2/resist dummy gate to 'align' the gate [31]. Other SAG processes use refractory metal gates because the gate metal, like TiW [32] or PtAu [33], is deposited before annealing.

2.3.1 ION IMPLANTATION

Ion implantation (ie the injection of energetic ions into a substrate) dominates over diffusion for doping GaAs. Si, Se, S and Sn are the most commonly used materials to dope GaAs n-type.

To use ion implantation effectively, it is important to know the distribution of the dopant as a function of depth. This information is given by the LSS theory developed by Lindhard, Scharff and Shiott [34]. It is derived for an amorphous target. The dopant density according to the LSS theory is Gaussian in nature and can be written as,

$$N(x) = \frac{\phi}{\sigma_p\sqrt{(2\pi)}} \exp\left[-\frac{(x - R_p)^2}{2(\sigma_p)^2}\right] \qquad (2.1)$$

where ϕ is the implant dose, x the depth into the surface, R_p the mean projected range, and σ_p the standard deviation in the projected range. Hence, given the dose and the energy of an implant, the resulting implant profile can be calculated with the equation above and range statistics data compiled by Gibbon et al. [35] to obtain R_p and σ_p. Range statistics data for Si into GaAs is given in table 1. This particular set of statistics is

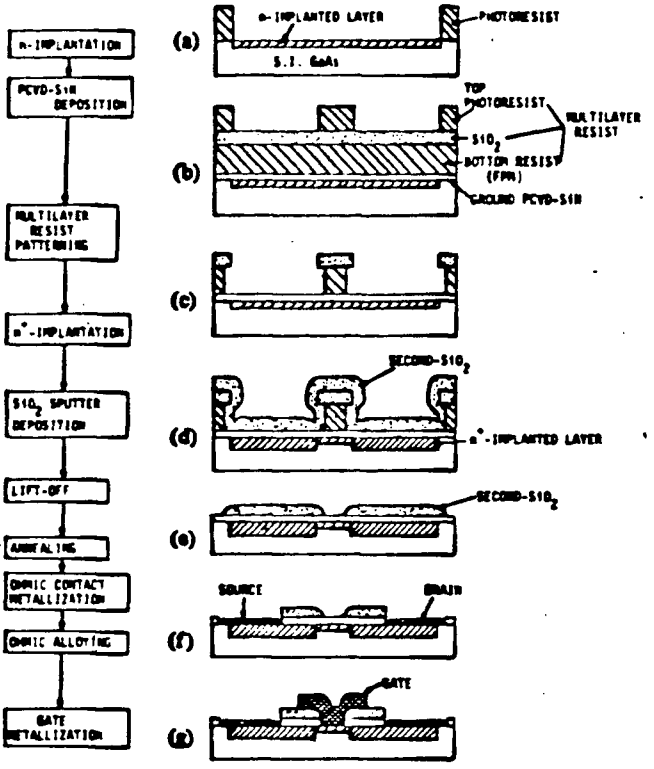


Figure 2.4: SAINT Fabrication Process [31]

given because in the fabrication process used for this thesis, silicon 28 ions are used for the active channel implant.

It has been found that near the edge of the masking material, there is also a lateral dependence to the distribution function. Furukawa et al. [36] have shown that the resulting complex distribution is the product of a Gaussian function and complementary error function. The distribution is represented by the following:

$$N(x) = \frac{\phi}{\sigma_p\sqrt{(2\pi)}} \exp\left[-\frac{(x - R_p)^2}{2(\sigma_p)^2}\right] \frac{1}{\sqrt{\pi}} \operatorname{erfc}\left[\frac{y - a}{\sigma_y\sqrt{2}}\right] \quad (2.2)$$

where y is the lateral distance from the edge of the mask, σ_y its standard deviation and the rest of the variables have the same meaning as above. This lateral diffusion of the implant can increase the gate parasitic capacitance, especially in the case of SAG MESFET. It is speculated that the extent of this lateral diffusion is also orientation dependent [37].

Table 1: Range Statistics Data For Silicon 28 Into GaAs

Energy (keV)	Projected Range (micron)	Projected Standard Deviation (micron)	Lateral Standard Deviation (micron)
60	0.0507	0.0294	0.0399
80	0.0677	0.0370	0.0508
100	0.0850	0.0442	0.0615
120	0.1025	0.0510	0.0717
150	0.1291	0.0607	0.0866

2.3.2 ANNEALING

Annealing is necessary after ion implantation to repair lattice damage and to activate the implant. To keep the surface intact during furnace annealing, which is typically performed at temperatures greater than 800°C one of the following steps can be taken:

1. Encapsulating the surface with a dielectric.
2. As over-pressure.
3. Covering the sample with a slice of GaAs.

The most common dielectric encapsulants on GaAs are SiO_2 and Si_3N_4. Sometimes a combination of both materials has been used to reduce

stress. Stress introduced by encapsulants during annealing has been shown to affect the profile of the dopant [38]. This stress is eliminated in capless annealing where an arsine overpressure is used to minimise arsenic vacancy so that amphoteric Si will activate predominantly on gallium sites. In proximity annealing, the GaAs slice placed on top of the wafer to be annealed presumably supplies the arsine overpressure during annealing to minimise As loss.

In so-called rapid thermal annealing techniques [39], lasers, arc lamps or halogen lamps are used to anneal implants in a few seconds. The short annealing time prevent anomalous impurity and dopant profile diffusion that occur during the longer furnace annealing. Hence, a sharper profile is normally obtained with these newer techniques. What is more, under optimised conditions, the activation efficiency of the newer annealing techniques can be higher than the best figures achieved with the furnace. However, rapid thermal annealing can result in larger DC parameter variations than furnace annealing if uniform heating is not achieved [40].

2.3.3 OHMIC CONTACTS

Achieving a good ohmic contact is important for any fabrication process. A eutectic mixture of 12%Ge:88%Au is the most common ohmic contact system for n-type GaAs. Ni is often evaporated on top of the Au-Ge because a smooth contact is obtained [41].

The three mechanisms responsible for current flow in a metal semiconductor contact are thermionic emission, Schottky field emission and tunneling [42]. The dominant mechanism will depend on the barrier height and doping density. The barrier height observed on n-type GaAs is essentially constant (0.8eV) regardless of the metal used. It is therefore not

possible to reduce the barrier height by proper choice of the metal alone. The normal strategy used to achieve good ohmic contacts to n-type GaAs is to dope the GaAs sufficiently high enough so that tunneling becomes dominant.

During alloying of Au-Ge, Ga diffuses out from the surface and Ge from the eutectic Au-Ge mix diffuses into the GaAs occupying vacant Ga sites [43]. Since Ge acts as a donor on Ga sites, a heavily doped n-type region is formed near the surface. As a result, the width of the potential barrier is decreased making tunneling more probable. Interfacial oxide presents a further barrier to current flow.

2.4 PRESENT PROBLEMS

Two prevalent problems with current MESFET technology are the non-uniformity of the wafer and reproducibility from ingot to ingot in ion implantation and activation. One aspect of the problems is the surface. Residual impurities and defects appear to be concentrated at the surface and they can affect the activation of implanted dopant. It is of interest to device manufacturers to know if the top layer of the starting substrate should be removed. Another aspect of the problems is the dislocations present in the wafer. Dislocations affect device uniformity and will limit the yields of circuits in the VLSI level because MESFETs threshold voltage cannot deviate by more than 5 per cent [44]. Hence, it is vital that the effects of dislocations on device properties be understood and characterised.

3. EFFECTS OF REMOVAL OF SURFACE LAYER ON DEVICE CHARACTERISTICS

3.1 INTRODUCTION

Commercially available GaAs wafers have already been chemically and mechanically polished into a high quality mirror finish. In spite of this, our understanding is that they are frequently subjected by device manufacturers to a surface etch before device fabrication. The reason is presumably that this improves device characteristics but little has been published on this topic. However, recently Dzioba [45] in an abstract of a paper has reported the presence of a subsurface damaged layer of 1-2μm on etch (100) LEC GaAs wafers. He also obtained better activation percentage on etched samples. GaAs wafers are sometimes annealed before an etch is performed. Annealing, in addition to producing a more uniform substrate, also drives impurities like Cu, Mg and Mn to the surface [46] so that they can be subsequently removed by a surface etch.

Surface etching plays an essential role in device fabrication technology. For example, it is widely used for patterning the surface for mask alignment and isolation as in 'MESA' etching. Etching normally proceeds by oxidation-reduction-complexing reactions [47]. The GaAs surface can be etched by a variety of etchants. Some of the common etchants include H_2SO_4:H_2O_2:H_2O, NaOH:H_2O_2 and NH_4OH:H_2O_2:H_2O. The resulting surface has been found to be dependent on the etch rate and the specific etchant used.

Most of the work on the surface treatment of GaAs has concentrated on the effects after the active layer has been formed. For example in Schottky or ohmic contacts, it is well reported that a light

surface etch performed just prior to metal evaporation improves the electrical characteristics of the contacts [48]. In this study the effects of a surface layer removal on the Schottky metallisation, the profile of the Si-implant and device characteristics were investigated. Devices were fabricated on undoped LEC (100) GaAs wafers. The wafers were not annealed before etching.

3.2 DIAGNOSTIC PATTERN

The test pattern was based on that of Immorlica et al. [49]. These test patterns are commonly incorporated into fabrication masks so that important fabrication data on process steps can be collected. A layout of the pattern with important device dimensions is given in figure 3.1. The pattern contains:

1. A Schottky diode, D1, to evaluate the doping profile and gate metallisation.

2. Four different MESFETs, T1-T4, to monitor the effects of the etch on device characteristics.

3. MESFET T3, known as the FATFET, is also used to obtain the drift mobility profile of the active layer [50].

4. A van der Pauw cross to measure the sheet resistance and Hall mobility [51].

3.3 DEVICE FABRICATION AND EXPERIMENTAL PROCEDURE

The devices were fabricated on undoped LEC (100) GaAs wafer supplied by Cominco Ltd. The fabrication steps used are listed in Table 4 on page 55. The wafer was first diced and pre-cleaned to step 1b in the table before etching. The etchant used was $5NH_4OH:2H_2O_2:240H_2O$.

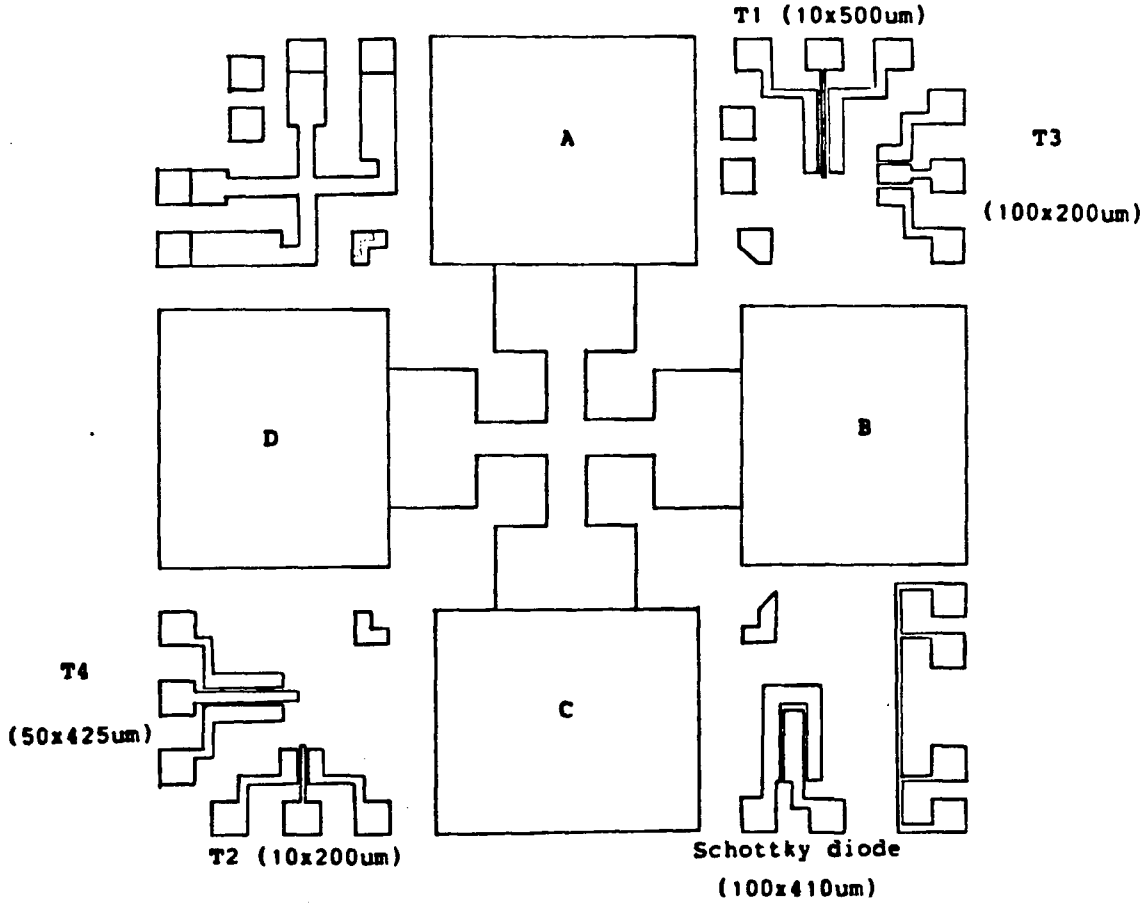


Figure 3.1: Test Mask Layout

Approximately 2μm of GaAs was removed in a fresh mixture of the etchant which has an etch rate of 2000 angstroms per minute. This etch rate was determined with the aid of the Tencor Alpha Step 200 profiler. The rest of the fabrications steps used are as listed in table 4. The implant energy and dose were fixed, they were 80 keV and 3.37 X 10^{12} ions per cm^2 respectively.

Samples 468s126A and 468s126D as depicted in figure 3.2 are made up of two quadrants of slice 468s126. Sample 468s126D has been subjected to a 2μm surface etch using the procedures described in the above paragraph. It retained its mirror-like surface after the etch indicating that no visible surface damage was introduced. There were also no abnormal

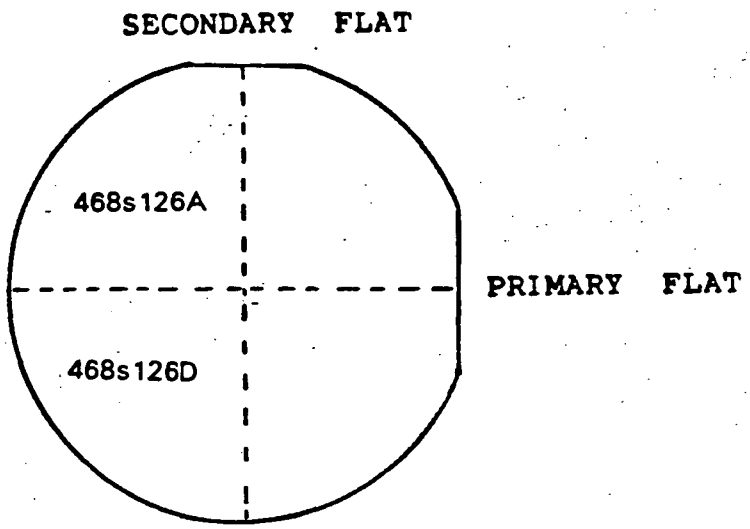


Figure 3.2: Position Of The Samples On The Wafer

features in the dark field image of the surface. Based on experience in the laboratory, samples have to be pre-cleaned to produce a featureless etch. Also, a fresh solution of the etchant was used each time because its etch rate decreases with time.

3.4 SCHOTTKY METAL EVALUATION

The Schottky contact formed between a semiconductor and metal is extremely sensitive to the nature of the interface. Consequently, it has frequently been used to investigate surface damage caused by processing steps. The electrical characteristics of Schottky contacts can be evaluated by measuring their barrier heights, ideality factors, leakage currents or breakdown voltages. Metal or metal systems that have been used to form Schottky barriers for GaAs diodes and MESFET gates include TiW, and Al.

The barrier height (ϕ) and ideality factor (n) were derived by analysing the Schottky diode current in accordance with the thermionic emission model. The model expresses the current, I, as [42]:

$$I = SA^{**}T^{2}\exp\left(-\frac{q\phi}{KT}\right)\left[\exp\frac{qV}{nkT} - 1\right] \qquad (3.1)$$

where V, T, k, S and A^{**} are the voltage applied, the temperature, the Boltzmann's constant, the Schottky contact area and the Richardson constant respectively. If the diode is slightly forward biased, $V > 3kT/q$, equation 3.1 can be rewritten as:

$$I = I_{s}\exp\left(\frac{qV}{nkT}\right) \qquad (3.2)$$

where

$$I_S = SA^{**}T^2 \exp\left(-\frac{q\phi}{kT}\right) \qquad (3.3)$$

I_S is the Schottky diode saturation current. The current voltage (I-V) characteristic of a typical forward biased diode is given in figure 3.3. The ideality factor can be determined using the following relation:

$$n = \frac{q}{\Delta kT} \qquad (3.4)$$

where Δ is the slope of the $\ln(I)$ versus V plot. With the value of the y-intercept, I_S, the barrier height can be evaluated as follows:

$$\phi = -\frac{kT}{q} \ln\left(\frac{I_S}{SA^{**}T^2}\right) \qquad (3.5)$$

The n, ϕ and leakage current (I_L) of all the Schotty contacts on samples 468s126A and 468s126D were measured. The equations used to evaluate n and ϕ are equations 3.4 and 3.5 respectively. The leakage current was defined as the diode current when a voltage of -2.5 volts was applied. A plot of the reverse biased diode current is given in figure 3.4. Table 2 gives a summary of the diode characteristics measured.

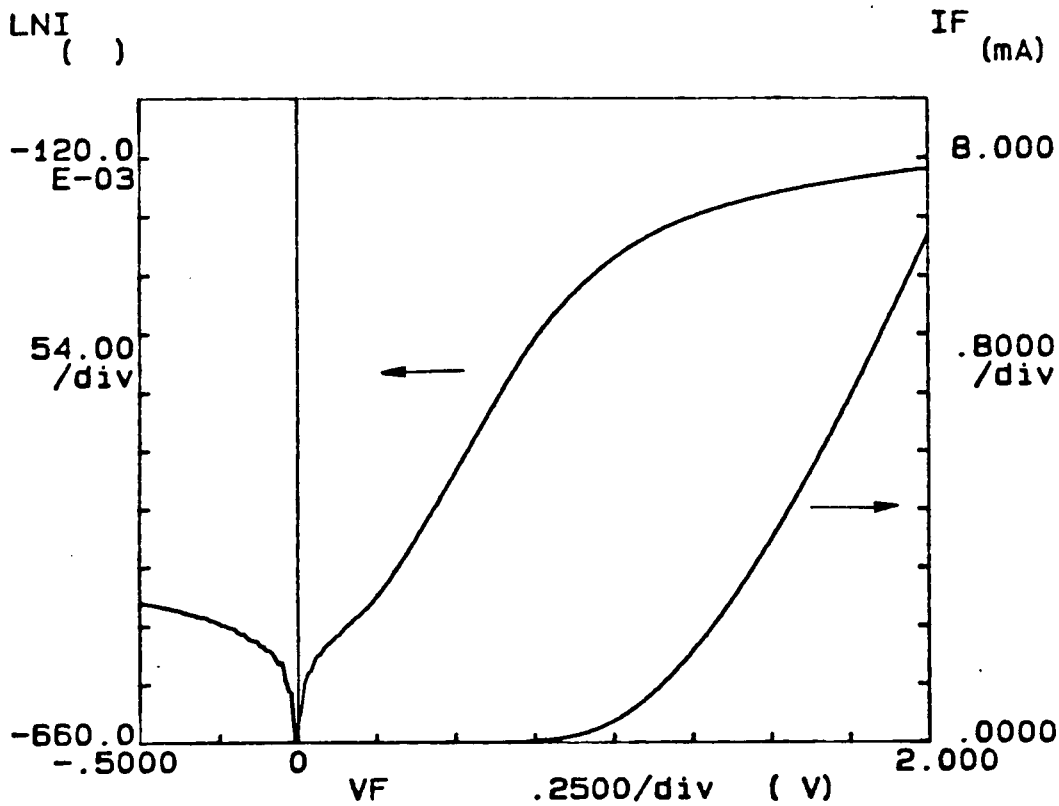


Figure 3.3: Characteristics Of The Forward Diode Current

Table 2: Summary Of Schottky Metallisation And Implanted Layer Characteristics

Sample	468s126A (UNETCHED)	468s126D (ETCHED)
n	1.31	1.79
Scatter in n	0.18	0.28
ϕ (eV)	0.72	0.70
Scatter in ϕ	0.03	0.05
I_L (μA)	10.77	13.71
Scatter in I_L	1.10	1.30
W_o (A)	1957	2160
Scatter in W_o	111	90
W_1 (A)	3406	3623
Scatter in W_1	229	231
μ_{peak} ($cm^2/V-s$)	3886	3627
Scatter in μ_{peak}	165	166
R_S ($k\Omega/\square$)	3.26	2.69
Scatter in R_S	0.42	0.18
μ_H ($cm^2/V-s$)	4349	4406
Scatter in μ_H	204	385
η (%)	12.24	15.86
Scatter in η	1.4	1.1

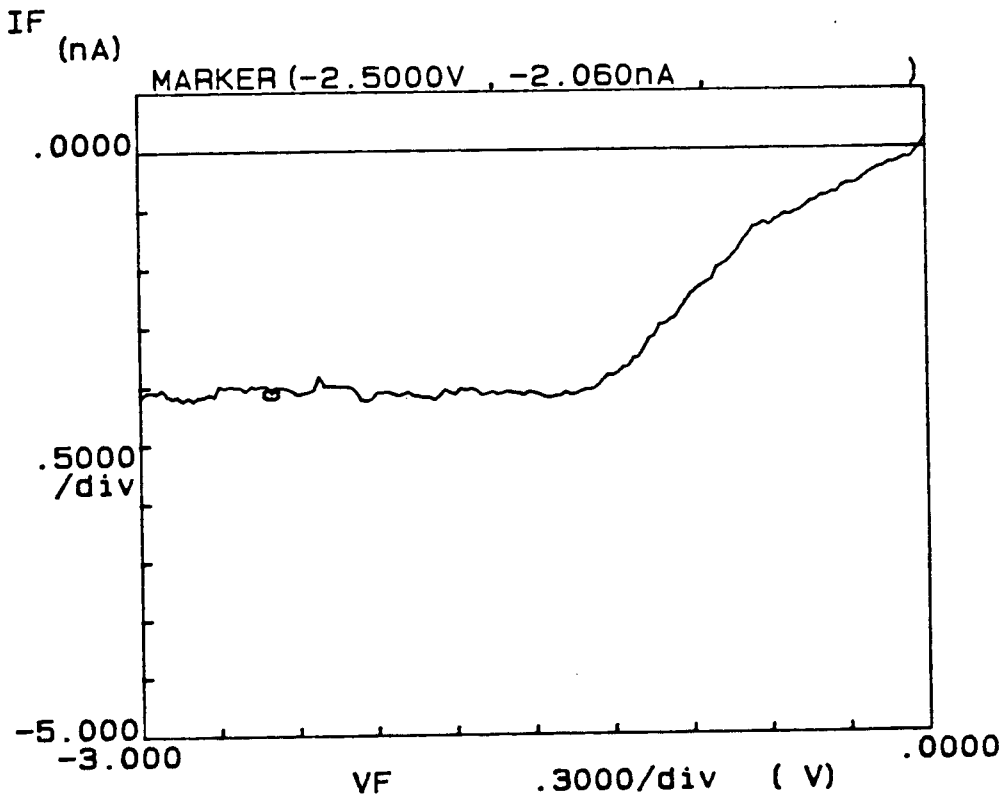


Figure 3.4: Characteristics Of The Reverse Diode Current

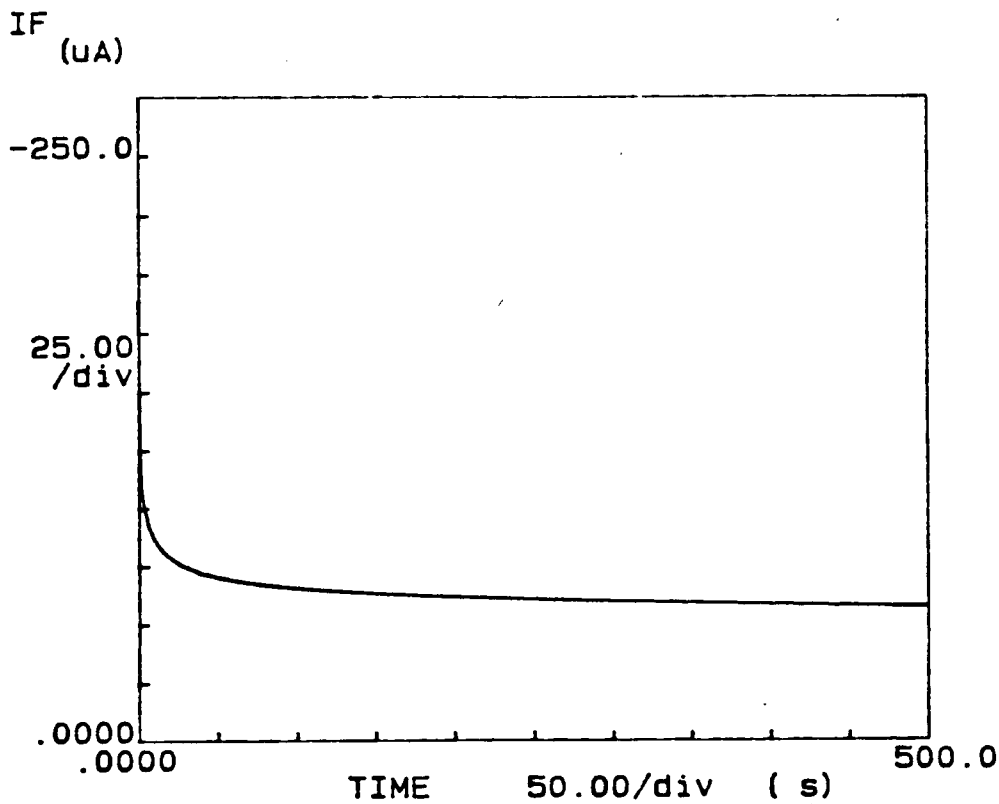


Figure 3.5: Transient In The Reverse Diode Current

A 30 seconds wait time was incorporated into the measurement routines of all the parameters. This was done to avoid the large transient in the current that occured immediately after a measurement was started. The transient was especially evident when measuring the small leakage current as depicted in figure 3.5.

The average value of n and the leakage current was larger while that of ϕ was smaller on the sample that has received a surface etch. Hence, slightly poorer diode characteristics were obtained on the etched sample. This can be ascribed to surface damage caused by the etchant. The nature of the surface damage introduced cannot be detected using Schottky contacts. The uniformity of the diode characteristics also deteriorated after the etch. This is not surprising because chemical etches are not known for their uniformity.

2.5 IMPLANT LAYER CHARACTERISATION

In this section the electrical characteristics of the active layer will be evaluated. They include the doping profile, the sheet resistance, Hall mobility and drift mobility.

2.5.1 DOPING PROFILE

The doping profile was evaluated using the C-V [42] technique which expresses the carrier density, $N(x)$ as,

$$N(x) = -\frac{C^3}{q\epsilon A^2}\frac{\partial V}{\partial C} \qquad (3.6)$$

where C, A, q and ϵ are the capacitance, the Schottky contact area, the electronic charge and the permittivity respectively. C is related to the depth

of the profile, x by,

$$C(x) = \frac{\epsilon A}{x} \qquad (3.7)$$

A depletion layer is present at zero gate voltage because of the work function difference between the semiconductor and the metal and the presence of surface states. To profile very close to the surface, the diode is usually slightly forward biased but the resultant forward current prevents much improvement over scanning from zero volt. This is evident in the doping profiles given in figure 3.6 which were scanned from a gate of 0.25 volt. The profile depth on the other hand is limited by the breakdown voltage of the diode. This constraint is usually not a problem with the implant dose and energy used in active channels of low power MESFETs.

The capacitance of the diode was measured at 1 MHz using a HP 4275A LCR meter. The experimental set up used to obtain the doping profile in addition to the LCR meter included a HP 9816 computer, a Wentworth Labs probe station and an electrically shielded box.

The depth of the peak carrier concentration is directly related to the implant energy used. In all the profiles obtained, the small implant energy, 80 keV, did not allow the peak to be profiled because it lay within the zero gate voltage depletion region. As a result, the depth of the profile when the carrier concentration are 10^{15} and 10^{16} per cm^3 (W_1 and W_0 respectively) were recorded and summarised in Table 2. Compared with the unetched sample, the implant on the etched sample on the average went deeper into the substrate. Figure 3.6 gives the typical profile on samples 468s126A and 468s126D. It can be seen that activation was generally higher on the etched wafer. However, the sheet carrier concentration and

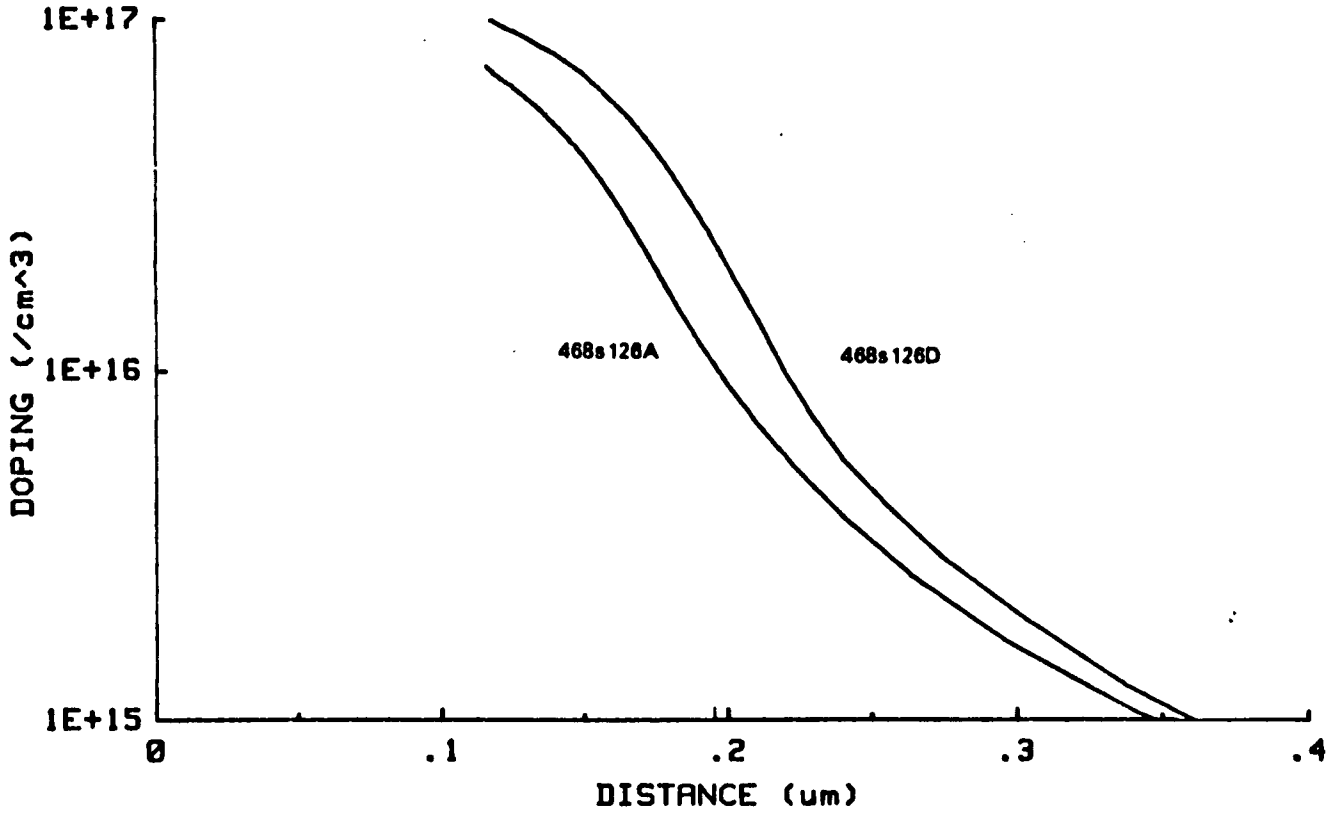


Figure 3.6: Typical Doping Profile Of Samples 468s126A and 468s126D

subsequently the percentage activation cannot be calculated from the profiles because the peak carrier concentration and its depth from the surface cannot be determined. The activation efficiency, can be evaluated using the van der Pauw cross in the next section.

2.5.2 SHEET RESISTANCE

The sheet resistance of the implanted layer was evaluated using van der Pauw's method with the aid of the van der Pauw cross (figure 3.1). The sheet resistance is written as [51],

$$R_S = \frac{\pi V_{CD}}{\ln(2) I_{AB}} \qquad (3.8)$$

where I_{AB} is the current applied between adjacent electrodes, A and B, and V_{CD} the voltage measured at the other pair of electrodes, C and D. The HP 4145A semiconductor parameter analyser (SPA) was used to both measure the voltage and source the current.

A plot of sheet resistance as a function of applied current is given in figure 3.7. The sheet resistance was defined as the value obtained when the current between electrodes A and B of the van der Pauw cross was 500μA. This current was chosen arbitrarily and should not have any bearing on the reading because the sheet resistance is essentially constant as can be seen in figure 3.7.

The sheet resistances of sample 468s126A and 468s126D are given in Table 2. A smaller sheet resistance was obtained for the etched sample. This follows directly from the higher carrier concentration observed in the doping profiles of the etched sample. In addition, the sheet resistance uniformity was also better on the etched substrate.

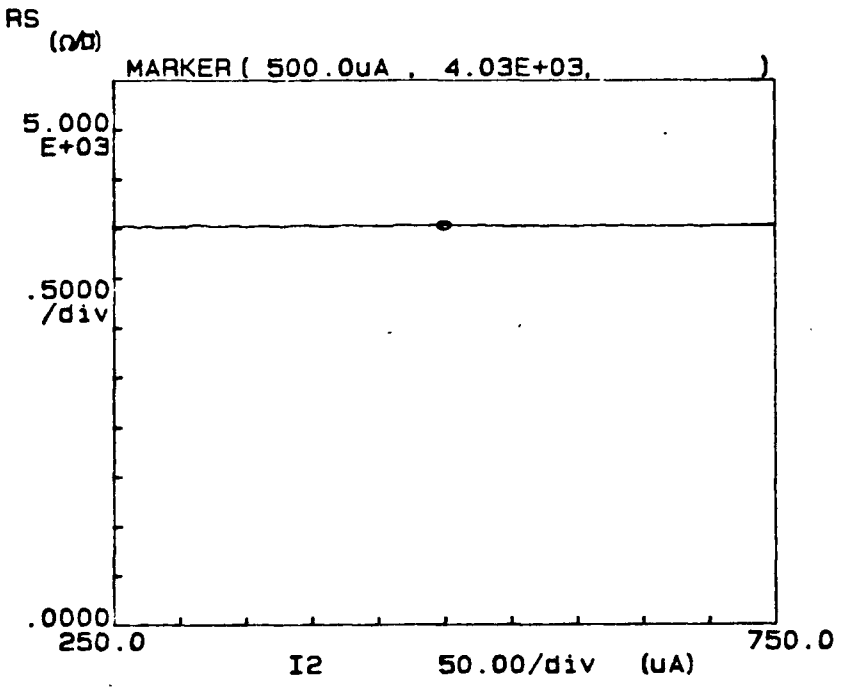


Figure 3.7: Sheet Resistance Of The Implant

The Hall mobility was also measured using the van der Pauw cross. In this case, the sample was placed on a probe holder instead of the probe station. A magnetic field of 0 to 0.2 tesla was applied perpendicular to the sample using an Alpha Scientific Laboratories magnet. A constant current of 250μA was also applied between the opposite ends of the van der Pauw cross while the voltage in the remaining two ends was monitored. The Hall mobility μ_H is given by [60],

$$\mu_H = \frac{V_{BD}}{(R_s B I_{AC})} \tag{3.9}$$

where

I_{AC}, V_{BD}, B and R_S is the current applied between electrodes A and C (figure 3.1), the voltage measured between electrodes B and D, the magnetic field applied and the sheet resistance respectively.

The activation efficiency, η, can be calculated using the R_S and μ_H. η is defined as:

$$\eta = \frac{N}{D} \tag{3.10}$$

where D is the implant dose and N the undepleted sheet carrier concentration which can be evaluated using the following relation,

$$N = \frac{1}{(q\mu_H R_S)} \tag{3.11}$$

As a result, equation 3.10 can be rewritten as,

$$n = \frac{1}{(Dq\mu_H R_S)} \tag{3.12}$$

The Hall mobility and the activation efficiency were determined using equations 3.9 and 3.12 respectively. The average value of both parameters obtained were slightly higher on the etched sample (Table 2), implying that the removal of the surface layer resulted in a marginally better substrate for direct ion implantation.

2.5.3 DRIFT MOBILITY PROFILE

Because the drift mobility (μ) is a function of the traps present in the channel, it can be used to assess the quality of the implanted layer. An approximate μ value can be obtained using the technique invented by

Pucel and Krumn [50] which expresses the μ as:

$$\mu = \frac{g_m L^2}{(C_g V_{ds})} \qquad (3.13)$$

where g_m, L, C_g, and V_{ds} are the transconductance, gate length, gate capacitance and drain source voltage respectively. All the measurements needed to obtain the μ profile were performed on FATFET T3. The C_g was measured using the LCR meter with the drain and source electrodes tied together. To measure the g_m, the SPA was used. Only 50mv was applied across the drain and source electrodes so that the cross-section of the undepleted channel was essentially constant. The g_m at a particular voltage is defined as the slope of I_d as a function of V_g plot at that voltage.

A profile of the μ is given in figure 3.8. On the same figure, the corresponding doping profile is also plotted. The same characteristics μ profile was seen in all the FATFETs tested. The average peak mobility was calculated from the profiles (Table 2).

The μ profile increases to a peak from the surface and decreases from the peak towards the substrate. This agrees with the result of Lee et al. [52]. It has been suggested that the μ profiles decrease towards the substrate because of implant damage at the active layer substrate interface that has not been annealed away [53]. Although, a higher carrier concentration was observed on the etched sample, its average peak mobility was smaller. It is not known for certain at this point why this is the case. This discrepancy could be caused by the inferior Schottky diode characteristics obtained on the etched sample.

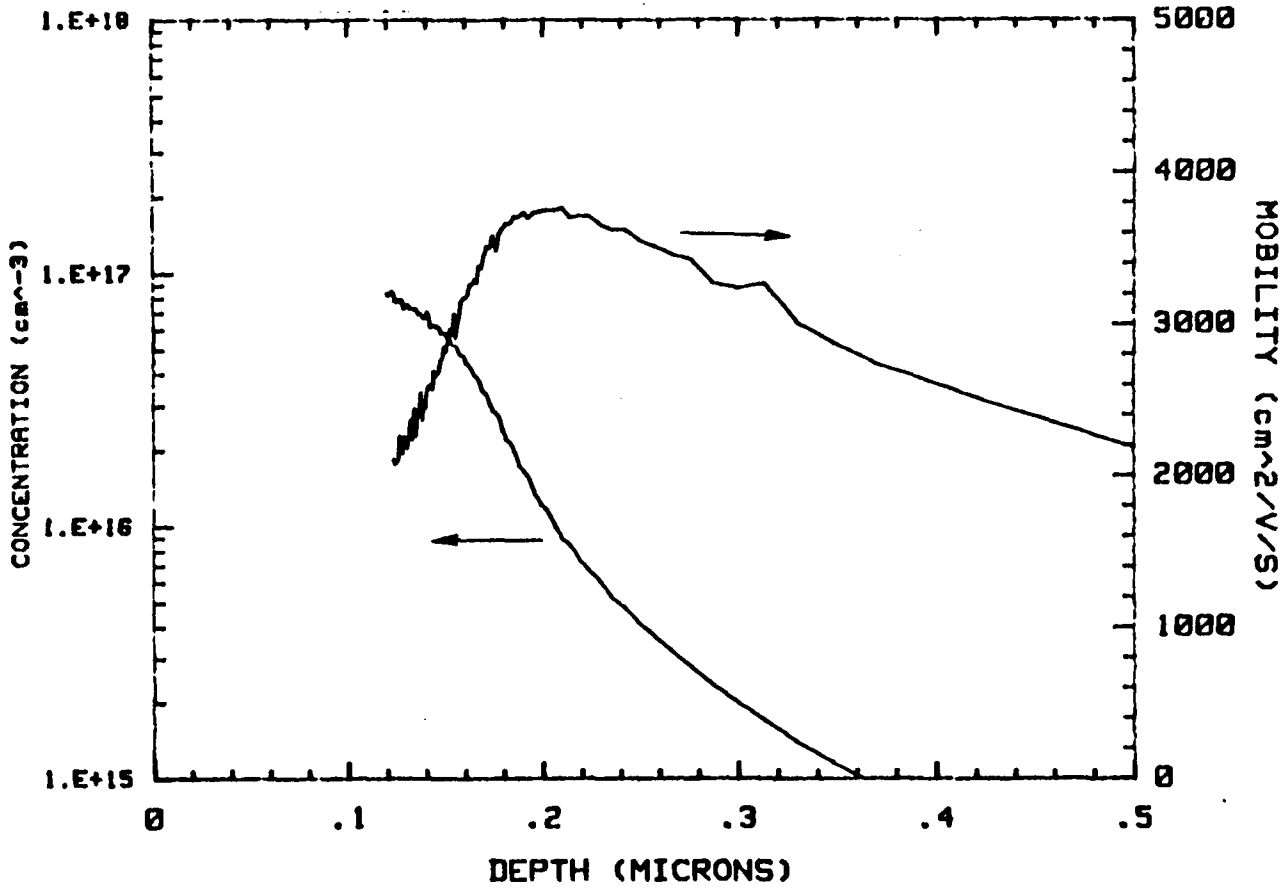


Figure 3.8: Drift Mobility And Doping Profile

3.6 DEVICE PERFORMANCE

In characterising the fabricated MESFETs, we measured the following parameters: V_{th}, K, I_{dss} and g_m. They are the threshold voltage, the K-factor, the saturation drain current with zero applied gate voltage and the transconductance respectively. A listing of the program used for determining the four parameters is given in appendix A.

Above the saturation region, the dependence of drain current of MESFETs on gate voltage is essentially quadratic and can be written as [42]:

$$I_d = K(V_g - V_{th})^2 \qquad (3.14)$$

with the K-factor defined as,

$$K = \frac{\mu \epsilon W}{2aL} \qquad (3.15)$$

where W is the gate width, L the gate length, a the channel thickness μ the drift mobility and ϵ the permittivity.

The I_d-V_g characteristics of all the MESFETs were measured for a drain-source voltage of 2.5 volts. The V_{th} in the program is defined as the gate voltage when the drain current is 5μA. The K-factor is the square of the slope of the $\sqrt{I_d}$ as a function of V_g plot. The g_m is defined as the the slope of I_d versus V_g plot between a gate voltage of 0 and -0.1 volt.

All the DC parameters measured on the MESFETs are listed in table 3. Figure 3.9 gives a plot of the I-V for each of the MESFETs (T1-T4) on the test structure. On all the MESFETs except T3 the following trends were

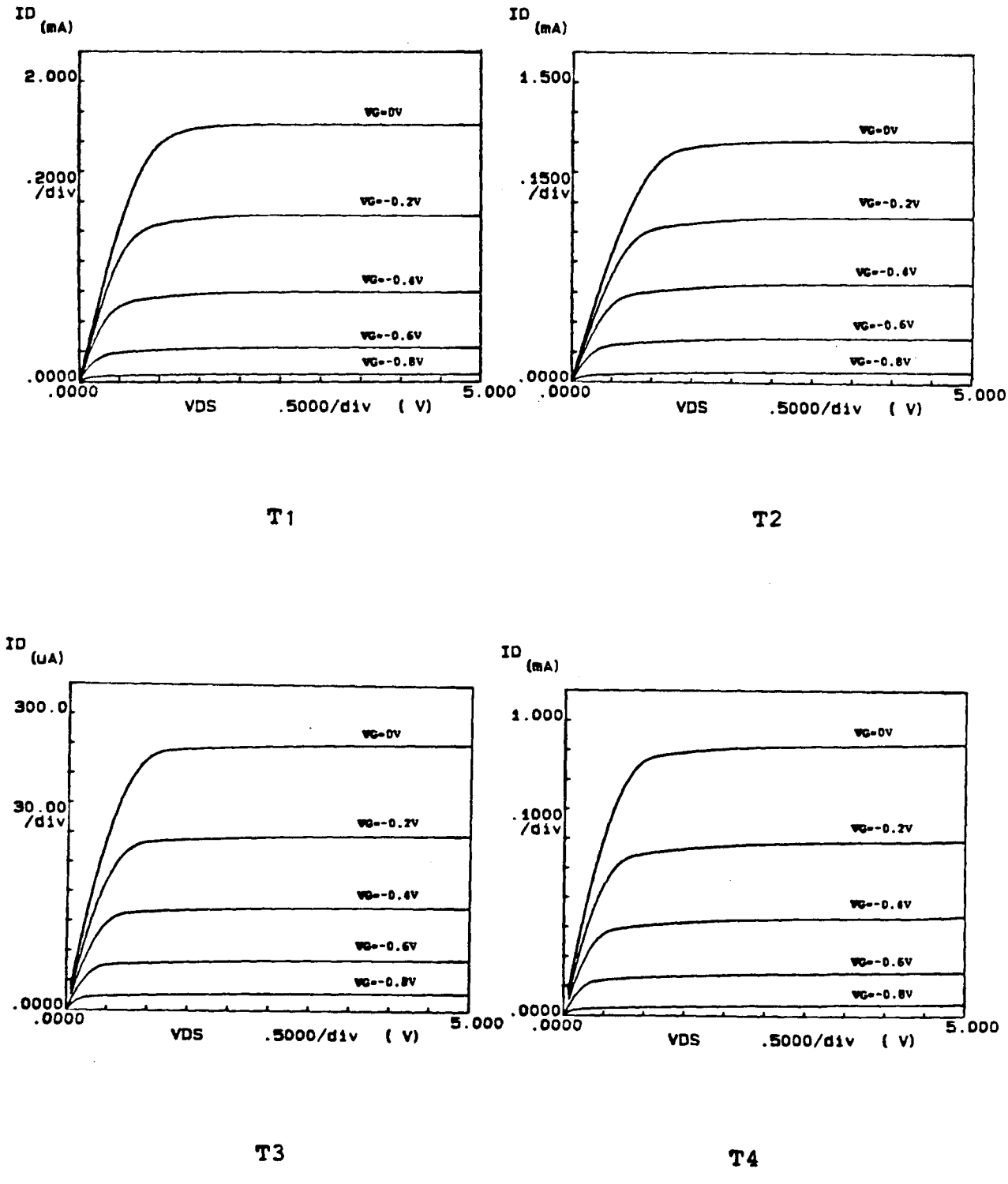


Figure 3.9: Current Voltage Characteristics Of MESFET T1, T2, T3 and T4

observed on the sample that has received a surface removal before device fabrications:

1. V_{th} was more negative
2. I_{dss} became larger
3. g_m became larger
4. K-factor became larger

Although the MESFETs tested were not designed with optimal transistor characteristics, it can still be inferred from the results that the removal of the surface layer just prior to device fabrication improved device characteristics. Since the K-factor is proportional to μ/a (equation 3.15) and the channel was deeper on the etched sample in comparison with the unetched sample (from doping profiles), a higher K-factor obtained on the etched sample implies that the implanted channel also has better transport characteristics.

The I_{dss} of T3 followed the trend of the other transistors but its V_{th} became more negative on the unetched sample despite of the smaller I_{dss} present. This, the smaller K-factor and g_m have prompted us to speculate that the channels of FATFET T3 on 468s126A were not completely covered by the gates. This can result from a slight misalignment. As can be seen in figure 3.1 which gives a layout of the test mask, the gate of T3 does not overlap its channel as much as the gates of the other MESFETs. Hence, a slight misalignment can in fact result in the channel of MESFET T3 not being entirely covered.

Table 3: Summary Of MESFET Characteristics

		Vth (V)	K-factor ($\mu m/V^2$)	Idss (A)	Gm (ms/mm)
MESFET T1					
468s126A	Ave.	-0.82	1.77E3	1.17E-3	3.91
	Sdev.	0.11	0.29E3	0.30E-3	0.75
468s126D	Ave.	-1.21	1.87E3	2.38E-3	5.99
	Sdev.	0.31	0.18E3	0.55E-3	0.56
MESFET T2					
468s126A	Ave.	-0.74	9.89E2	5.36E-4	4.65
	Sdev.	0.13	0.75E2	1.74E-4	1.20
468s126D	Ave.	-0.98	1.07E3	9.93E-4	7.25
	Sdev.	0.17	2.04E2	1.91E-4	6.82
MESFET T3					
468s126A	Ave.	-2.67	23.60	1.23E-4	1.01
	Sdev.	1.25	22.73	0.68E-4	0.45
468s126D	Ave.	-1.12	2.05E2	2.60E-4	1.84
	Sdev.	0.12	0.30E2	0.55E-4	0.25
MESFET T4					
468s126A	Ave.	-0.79	7.20E2	4.68E-4	1.94
	Sdev.	0.14	1.02E2	1.59E-4	0.53
468s126D	Ave.	-1.08	8.10E2	9.09E-4	3.18
	Sdev.	0.19	0.87E2	2.17E-4	0.51

2.7 BACKGATING EFFECTS

Backgating is the effect of a negative voltage applied to a nearby electrode on MESFET characteristics. The backgate voltage modulates the space charge region at the interface between the channel and the substrate which subsequently affects the drain current. With sufficient negative backgate voltage applied, the channel can be completely pinched-off. Backgating can seriously degrade device performance. For instance, the slow drift in I-V characteristics [54] and the frequency dependence of g_m at low frequency have both been attributed to backgating [55].

The possible mechanisms responsible for backgating effects include the traps in the underlying material [56] and the presence of a p-type conversion layer [57]. The threshold voltage, V_{bg}, for backgating is defined as the the backgate voltage at which backgating effects are first observed. In practice, V_{bg} is not always seen. It can be increased by using isolation implants with ions such as H, O and B [58], a p-type guard ring around the device [59] or a negatively biased Schottky contact between the devices [60].

The test structure and measurement set-up for this experiment is shown in figure 3.10. As shown in the figure, the measurements were taken with MESFET T2 using pad C of the van der Pauw structure as the sidegate. The side gate is 400μm away from the MESFET T2.

The backgating effects on both samples were found to vary from region to region. Hence, an overall trend of the effects of the surface etch cannot be detected. But, when devices at approximately the same relative location were compared, those on the etched wafer show less backgating effects. This can clearly be seen in figure 3.11 where the normalised drain current (normalised with I_{dss}) is plotted as a function of the backgate

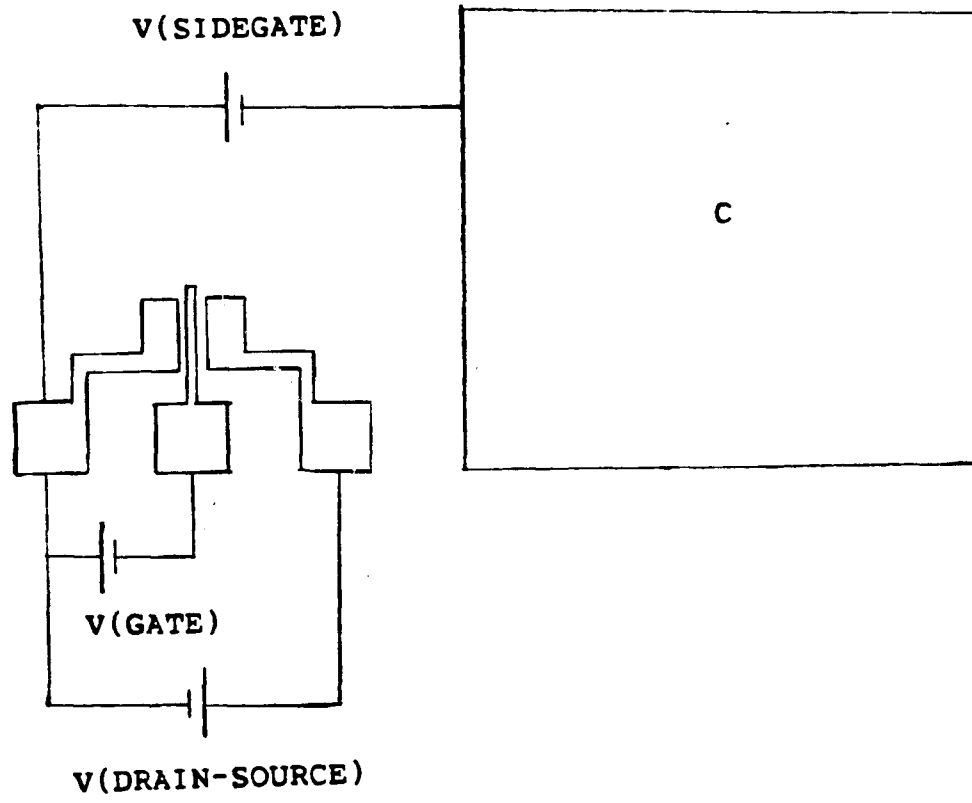


Figure 3.10: Measurement Set-up For The Backgating Experiment

voltage.

From the plot of percent change in I_d versus normalised gate voltage (normalised with V_{th}), given in figure 3.12, the backgate effect becomes more pronounced as the gate voltage approaches the threshold voltage. This evidence supports the claim that the existence of a space charge region at the active layer substrate interface is reponsible for backgating. In undoped LEC GaAs substrate, the width of this depletion layer is dependent on the compensation of the EL2 level and residual impurities like carbon.

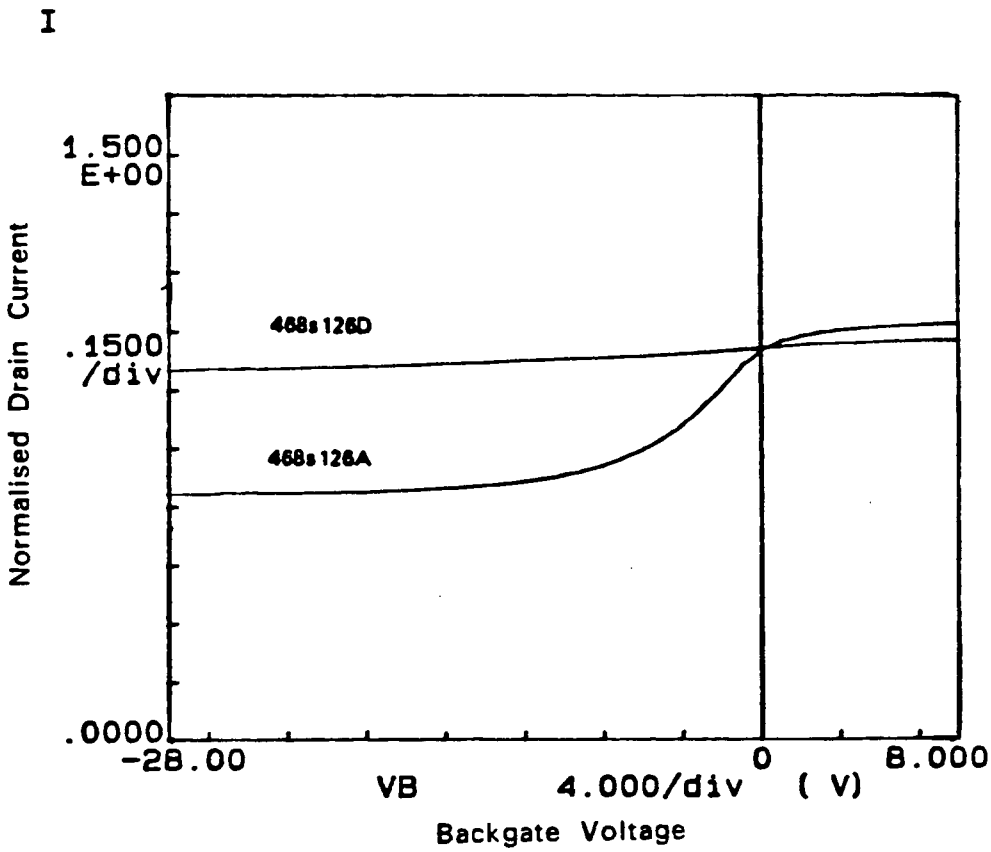


Figure 3.11: Normalised Drain Current Versus Backgate Voltage

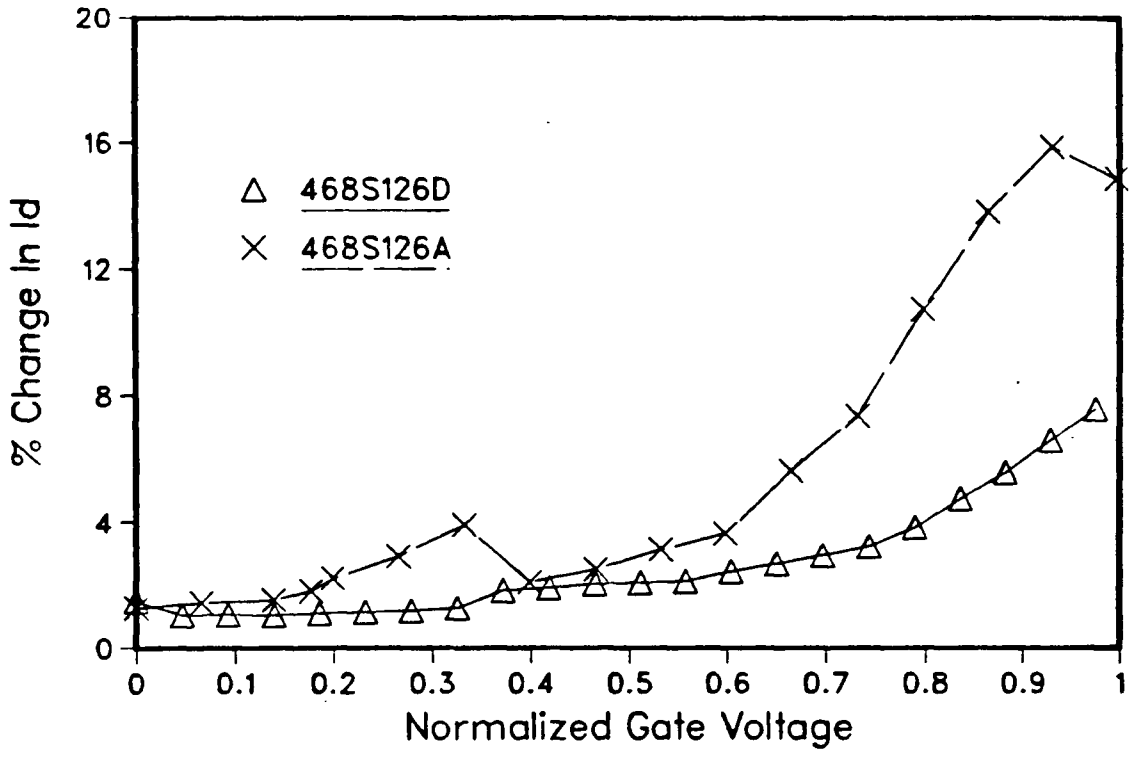


Figure 3.12: Drain Current Versus Normalised Gate Voltage

4. EFFECTS OF DISLOCATION ON DEVICE CHARACTERISTICS

4.1 INTRODUCTION

Non-uniformity of GaAs wafers has been observed using SEM-EBIC [61], cathodoluminescence [62], photoluminescence [63], bulk resistivity variation [64] and infrared photo-absorption [65]. These phenomena have been correlated with dislocation density variation across the wafer. The dislocation density in 2" and 3" GaAs wafers can range from 10^4 to more than 10^5 per cm^2.

As the complexity of GaAs ICs increases, the possible adverse effects of dislocations on device performance and reliability become an important question. It has been known for a long time that dislocations cause the formation of dark-line defects in lasers and light emitting diodes [66]. Work published only recently has shown that the dislocation density of GaAs substrates affects the electrical characteristics of MESFETs [67]. The activation efficiency and thus the channel doping density and the threshold voltage of MESFETs are affected by their local dislocation density. However, studies on the influence of proximity of dislocation on MESFET threshold voltage have not been in agreement [68,69]. In addition, the scatter of threshold voltage has also been found to be dependent on the structure of the dislocation pattern [70]. Clearly, there is an ambiguity as to the origin of the MESFET threshold voltage scatterings.

The generally held opinion now is that dislocations affect device characteristics but the exact origin of the effect is not known. The object of this study was to help determine whether local dislocation density, proximity to a dislocation centre, or the structure of dislocation pattern controls the scatter of threshold voltage. The method used involved the

design, the fabrication and the measurement of a MESFET array of pitch 200μm x 146μm. After measurement, the sample was etched to reveal dislocation centres. Exact local dislocation density and distance to the nearest dislocation centre of MESFETs were obtained with the aid of micro-photographs taken of the sample after the etch.

Following this introduction, a literature survey will be given. In sections 4.3 and 4.4, fabrication procedures and experimental results will be discussed respectively.

2.2 LITERATURE SURVEY

Direct implantation into GaAs for the formation of the active channel places stringent requirements on the substrate quality. One of the requirements is the homogeneity of the substrate. Although it has been well known for some time that there is significant resistivity and dislocation variation along the length of a GaAs boule, it was not until 1982 that the variations of these parameters across a wafer were studied [71]. This is because it was commonly believed then that a dislocation density as high as 3 X 10^4 per cm^2 does not affect device characteristics.

The dislocation variation across a SI GaAs wafer can be obtained by counting the etch pits on it after an A/B [72] or molten KOH [73] etch is done. The etch creates a hexagonal pit on the surface of the wafer at the point where a dislocation line meets it. The dislocation density along the diameter of a GaAs wafer follows a W-shaped variation near the seed end [21]. The dislocation density increases and its W-shaped variation become less pronounced towards the tail end of the ingot. Dislocations are formed as a partial relief to the axial and radial stress which arise during crystal growth. Jordan et al. [74] has theoretically predicted the W-shaped variation

using a thermo-elastic model. Dislocations often appear in cell networks which are typically a few hundred μm in size [70]. The cells contain a dislocation and point defect free region because dislocation centres act as sinks for those defects. This creates what is known as the Cotterell atmosphere around the dislocation centres [75].

Many attempts have been made to reduce the dislocation density and its scatter in SI GaAs wafers. Terashima et al. [9] and Osaka et al. [76] have used a vertical magnetic field during growth to reduce melt temperature fluctuations which produce growth striations. Shimada et al. [77] heated the B_2O_3 encapsulating layer through a window on the susceptor to reduce its temperature gradient. Using this technique, a 2" GaAs wafer with a dislocation density as low as 1000 etched pits per cm^2 was obtained. Impurity hardening using In can also reduce the dislocation density of GaAs wafers [10]. The In atoms increase the crystal's resistance to the generation and propogation of dislocations. Although it is true that very high concentration, 5 to 10 X 10^{19} atoms per cm^3 of In is used, in In-alloyed GaAs, no degradation of Hall mobility is found.

The high resistivity, 10^7 to 10^8 Ω-cm, of SI GaAs is obtained by the compensation of shallow levels, like Si and C, with deep levels, like Cr and EL2 [4,15]. This sensitive balance can be changed by dislocations. Thus it is not surprising that the resistivity variation should closely follow that of the dislocation density. However estimates of the resistivity variation seems to be dependent on the measurement technique used. Brozel et al. [78] using Van der Pauw method found the resistivity variation across a (100) oriented undoped SI GaAs to be M-shaped whereas Blunt et al. [71] found a W-shaped variation on a similarly oriented wafer using the dark spot method. The reason for the different profiles obtained is not known.

Leakage current measured under illumination gave a M-shaped profile in undoped SI GaAs wafers [79]. The same measurement along the diameter of Cr-doped SI GaAs wafers did not result in a similar profile. This is because in Cr-doped substrates, there are still plenty of Cr atoms left to compensate shallow donors after the sinking action of the dislocation centres.

High resolution infrared absorption at 1μm showed that EL2 on SI GaAs wafers also follows the well known W-shaped profile [22]. Tajima et al. [80] using photoluminescence found that two emission bands, one at 0.65eV and the other at 0.8eV, consistently appeared in both undoped and lightly doped SI GaAs. The 0.6eV band coincides with the etch pit density distribution and is believed to be due to the EL2 level. The other band is inversely related to the etch pit density variation and is postulated to be due to microdefects which are generated in regions where the dislocation density is low.

Post growth heat treatment can improve the uniformity of SI LEC GaAs substrates and the same result can be obtained either by annealing individual wafers or the whole ingot. The improvement is brought about through diffusion involving an As-vacancy [81]. Illuminated leakage current, bulk resistivity and cathodoluminescence intensity line variation have all been shown to improve after annealing [82]. HB grown GaAs crystals are generally more uniform in comparision with LEC crystals. For example, HB GaAs shows smaller photoluminescence and cathodoluminescence at a dislocation. This more uniform characteristics of HB crystal is due to the thermal treatment during growth.

The inhomogeneous dislocation density distribution across GaAs wafers affects device characteristics. Nanishi et al. [83] have shown that

MESFETs fabricated on high dislocation regions have higher drain source current and a larger negative threshold voltage than those fabricated on low dislocation regions. Wang et al. [84] showed that mobility and transconductance vary directly with etch pit density. Miyasawa et al. [85] also found that the threshold voltage of MESFETs was influenced by their proximity to a dislocation. MESFETs less than a critical distance of 20-30μm away exhibit a lower threshold voltage than those further away (figure 4.1). Below this critical distance, threshold voltage also shows more scatter. This critical distance is in agreement with the radius of the so-called denuded zone surrounding a dislocation revealed by photoluminescence [63] and cathodoluminescence studies [62]. Recent work

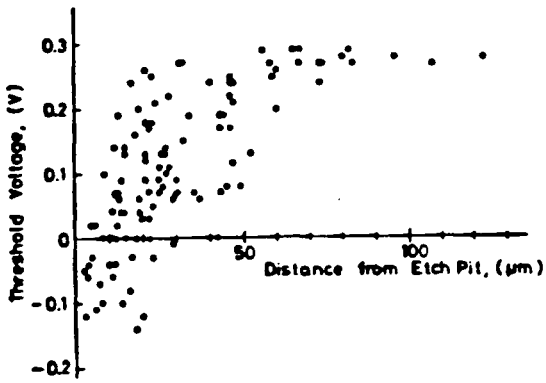


Figure 4.1: Threshold Voltage Versus Distance To Nearest Dislocation Obtained By Miyasawa et al. [85]

by Ishii et al. [72] has shown that threshold voltage scatter is strongly influenced by cell network structure. At a high threshold voltage scatter region, a strongly networked structure was found and threshold voltage scatter was small for randomly networked structure despite its high dislocation density. To complicate matters, the threshold voltage scatter was also found to be dependent on the implant dose and annealing method used [86]. Winston et al. [87] did not find any correlation between the MESFET threshold voltage and its proximity to a dislocation.

Hyuga et al. [88] using completely dislocation free In-alloyed GaAs reported that the sheet carrier concentration of an implanted layer formed by a direct silicon 28 (^{28}Si) implant at 60keV with a dose of 5 x 10^{12} per cm^2 was reduced to one fifth that of conventional GaAs wafers. Dobrilla et al. [89] showed that the local concentration of neutral EL2 in the substrate is a key factor in controlling device properties and suggested that the EL2 concentration uniformity may be more important than the dislocation uniformity. Tamura et al. [90] using wafers from three suppliers showed the existence of two types of undoped SI GaAs crystals. One group showed strong correlation between etch pit density and Hall mobility and resistivity and the other displayed little correlation between these parameters. SEM-EBIC [61] studies showed that two types of dislocation exist and this has been postulated to be due to the temperature at which dislocations were formed. Dislocations formed at high temperature have a Cottrell atmosphere whereas those formed at low temperature do not.

4.3 EXPERIMENT

This experiment involved the fabrication of dense arrays of MESFETs. Invariably, the fabrication process will introduce some inhomogeneity to the device characteristics measured. To study the influence of the substrate inhomogeneity, the process induced scatter must be minimised. With regards to this, we chose a simple four mask fabrication process and 2μm gate length MESFETs. An earlier attempt at this work was performed in this laboratory by W. Tang [91]. In that study, the active channel was formed by implanting through a Si_3N_4 layer which was deposited at the beginning of fabrication to protect the sensitive GaAs surface. This step was avoided in our fabrication procedures because of the difficulty involved in obtaining a uniform Si_3N_4 layer. Short gate length and narrow gate width provide better definition of the active channel position. We decided to use 2μm gates instead of the shorter 1μm ones to achieve better yields. Furthermore, it is impossible to obtain good gate length uniformity for the shorter gates using conventional optical lithography.

4.3.1 MASK DESIGN

In order to look at microscopic effects of dislocation networks a few hundred μm in size, a MESFET array of pitch 200μm x 146μm was used. The bulk of the area is occupied by the three 80μm squares used to probe the transistor. The distance between the drain and source pads is 10μm which gives a nominal spacing of 4μm between the gate and source or gate and drain. This makes alignment of the gate metal mask easier. The designed mask pattern is depicted in Figure 4.2 below. Pattern A is the registration mark, pattern B the channel implant, pattern C the n^+ implant and ohmic contact, and pattern D the gate. For economical reasons,

all the fabrication levels were placed on the same mask.

2.3.2 FABRICATION PROCEDURES

An overview of the fabrication process is schematically illustrated in figure 4.3. The details of the process are listed in Table 4.

Step 1 removes the grease from the samples. The samples were also etched to remove the top 500A of the surface. This ensures the removal of the surface oxide layer and the 'disordered' region right under the surface.

Steps 2 to 7 etch the registration pattern necessary for the higher levels of the mask. To ensure easier alignment in later stages of fabrication, proper resist development must be obtained. It is advisable to repeat steps 2 to 7 till a good resist pattern is obtained. This advice also applies to later resist development.

Steps 8 to 13 involve laying down the resist mask for selective implantation of the channel regions. ^{28}Si ions were used to make the channel n-type. During ion implantation, the (100) orientated sample was tilted 7° away from its <100> axis to any <110> direction. This made the substrate appear amorphous to the incoming ions, preventing axial channeling [92]. To minimise planar channeling and also to increase the uniformity of the implant, the sample was rotated 20° from the fundamental axis. An implant dose of 3.37×10^{12} at 80keV was used.

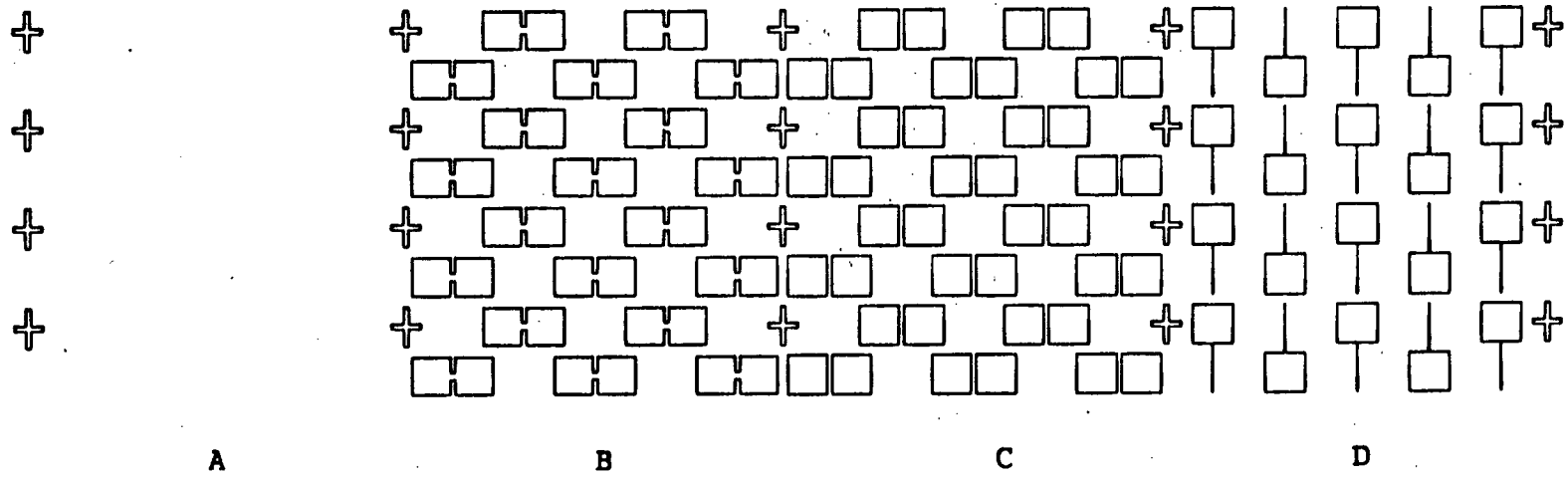


Figure 4.2: MESFET Array

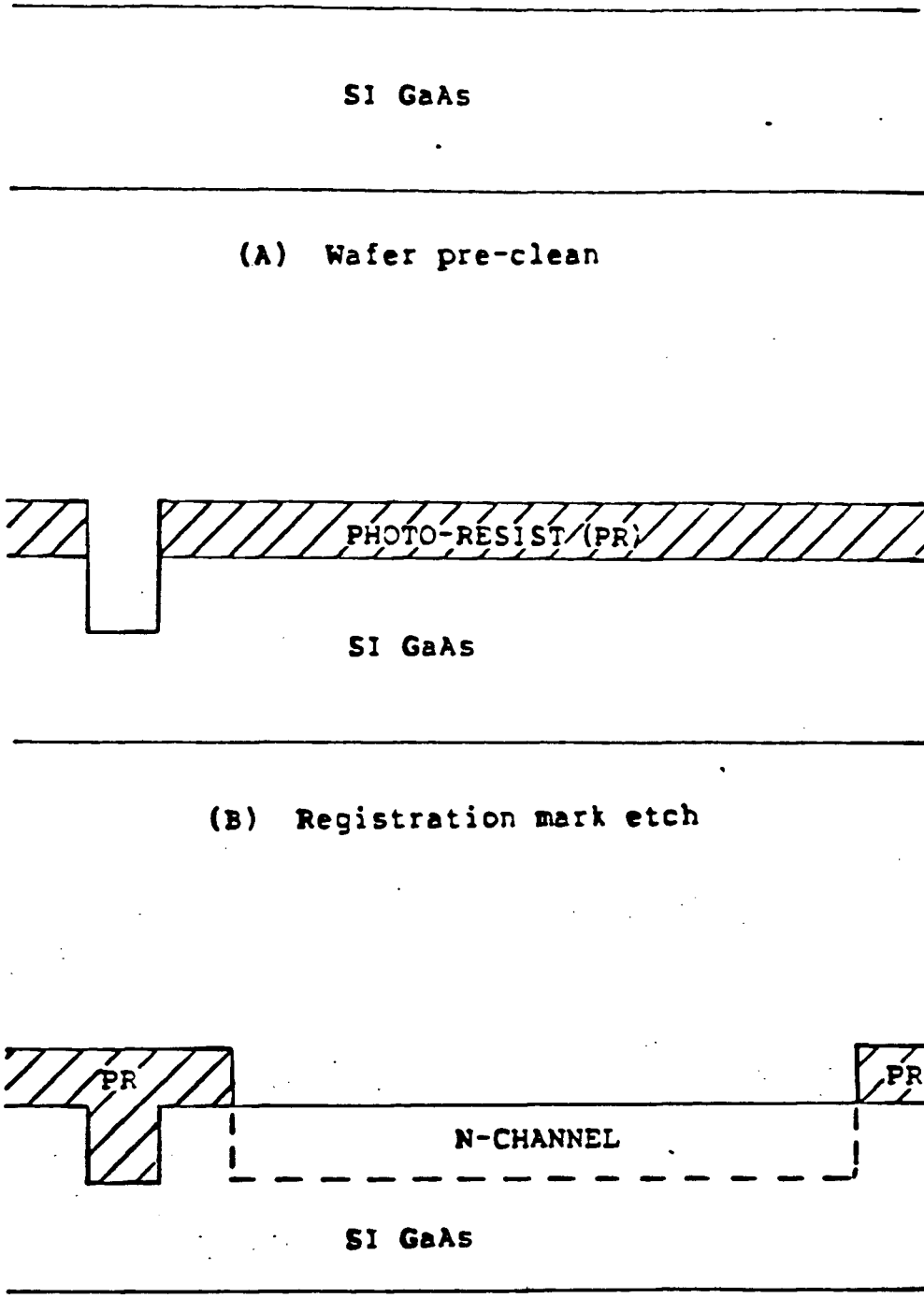
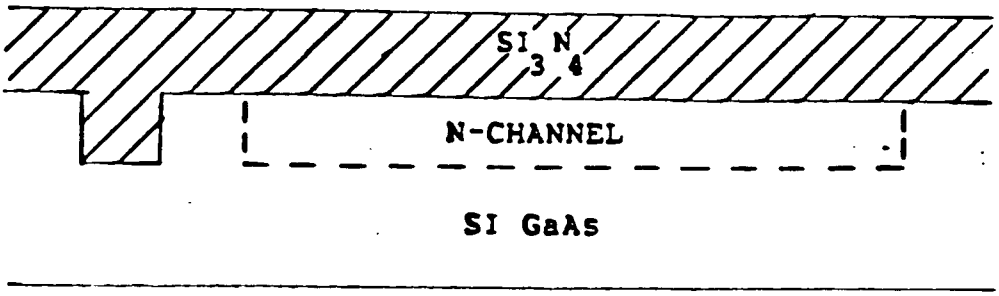
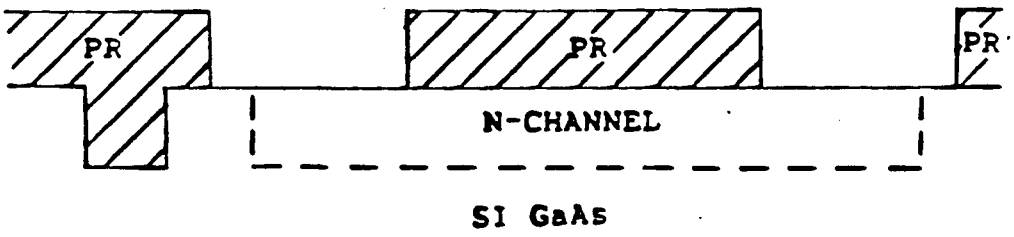


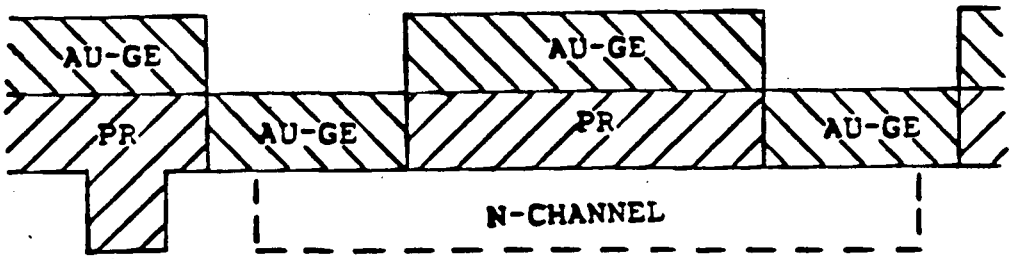
Figure 4.3: Schematics Of The Fabrication Process



(D) Encapsulation and annealing

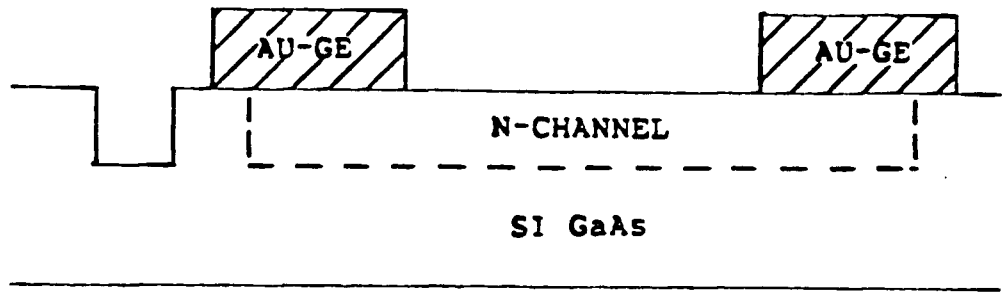


(E) Opening windows for gold-germanium contacts

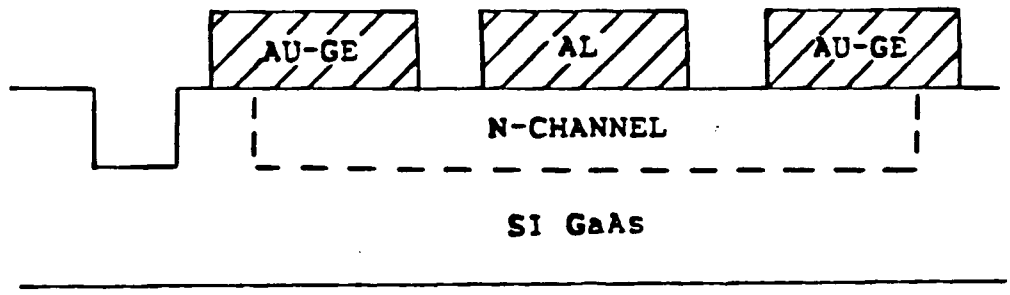


(F) Evaporation of gold germanium

Figure 4.3: Continued



(G) Liftoff of photo-resist, and alloying



(H) evaporation of aluminium.

Figure 4.3: Continued

Table 4: Detailed Fabrication Steps

No	Process Description
1.	<u>Pre-implant cleaning</u> a. Degrease 5 minutes rinse each in warm trichloroethylene, acetone and iso-propanol. b. GaAs etch Soak for 4 minutes in 1% filtered alconox (monosodium dihydrogen phosphate). 15 seconds DI H_2O rinse and N_2 blow dry. c. Oxide etch Immerse for 30 seconds in $1H_2O_2$:$5NH_4OH$:240DI H_2O, 15 seconds DI H_2O rinse and N_2 blow dry.
2.	<u>Clean</u> 2 minutes acetone rinse, 2 minutes iso-propanol rinse and N_2 blow dry.
3.	<u>Resist coat</u> Spin Shipley AZ1400-30 resist at 4500 rotations per minute (RPM) for 20 seconds (approximately 1.7μm thick). Soft bake at 95°C for 25 minutes.
4.	<u>Registration mark level exposure</u> 1 minute under ultra violet (UV) light (Karl-Suss MJB3).

5. Develop

Develop in 50% Shipley Microposit MF312 developer. Developing time is approximately 45 seconds.

6. Registration mark etch

Rinse for 1 minute in 10%HCL, 1 minute in DI H_2O, 50 seconds in 5%H_3PO_4:2.5%H_2O_2:92.5%DI H_2O, 5 minutes in DI H_2O and N_2 blow dry.

7. Resist removal

Soak in warm acetone.

8. Clean

2 minutes warm acetone rinse, 2 minutes iso-propanol rinse and N_2 blow dry.

9. Resist coat

Spin Shipley AZ1400-30 resist at 4500 RPM for 20 seconds. Soft bake at 95°C for 25 minutes.

10. Channel level exposure

1 minute under UV light.

11. Develop

Rinse in 50% Shipley Microposit MF312 developer.

12. Channel implant

^{28}Si at 80keV and dose of 3.37 x 10^{12} per cm^2.

13. Resist removal

Soak in warm acetone. O_2 plasma 200W, 200SCCM of O_2, 120°C, 250mTorr for 25 minutes.

14. Clean

2 minutes warm acetone rinse, 2 minutes iso-propanol rinse and N_2 blow dry.

15. Si_3N_4

Preclean surface with NH_3 plasma at 100W, 37.6SCCM of NH_3, 308°C, 500mTorr for 5 minutes. Without breaking vacuum deposit Si_3N_4 at 100W, 37.6SCCM of NH_3, 500SCCM of He, 550SCCM of 5%SiH_4/He, 308°C, 1500mTorr for 7 minutes (about 800A).

16. Channel implant anneal

825°C for 25 minutes under flowing N_2 gas. Place sample at edge of furnace for 5 minutes. Push sample into the furnace. On the way out, place sample at edge of furnace for 5 minutes before removing from the furnace.

17. Si_3N_4 removal

Freon plasma at 200W, 200SCCM of CF_4, 125°C, 500mTorr for 4 minutes.

18. Clean

2 minutes warm acetone rinse, 2 minutes iso-propanol rinse and N_2 blow dry.

19. Resist coat

Spin Shipley AZ1400-30 at 4500 RPM for 20 seconds. Bake at 95°C for 25 minutes.

20. Ohmic level exposure

1 minute under UV light.

21. Chlorobenzene soak

Soak for 2.5 minutes in chlorobenzene.

22. Develop

Rinse in 50% MF312 developer.

23. Oxide etch

Rinse for 15 seconds in $1NH_4OH:10H_2O_2$, 30 seconds in DI H_2O and N_2 blow dry.

24. Ohmic metal evaporation

1500A of Au-Ge.

25. Liftoff

Soak in warm acetone and agitate.

26. Alloy

2 minutes at 450° in flowing N_2 gas.

27. Ohmic contact

Check drain source current at V_{gs}=2.5 volts.

28. Resist coat

Spin Shipley AZ1400-30 at 4500 RPM. Soft bake at 95°C for 25 minutes.

29. Gate level exposure

1 minute under UV light.

30. Chlorobenzene soak

Soak for 2.5 minutes in chlorobenzene.

31. Develop

Rinse in 50% MF312 developer.

32. Oxide etch

Rinse for 15 seconds in 1NH_4OH:10DI H_2O, 30 seconds in DI H_2O and N_2 blow dry.

33. Gate metal evaporation

2000A of Al.

34. Liftoff

Soak in warm acetone and agitate.

35. DC measurements

The MESFET DC characteristics can now be measured.

To prevent As loss during a high temperature (825°C) anneal (which is required to repair lattice damage as well as to electrically activate the dopants) a Si_3N_4 film of about 800A was used to encapsulate the surface. Si_3N_4 was chosen over SiO_2 because it is more impermeable to gallium atoms [93]. Furthermore, a good quality plasma enhanced chemical vapour deposited (PECVD) Si_3N_4 film can be easily and quickly deposited using the Plasma-Therm.

Early attempts to anneal with Si_3N_4 as the encapsulant resulted in its dissociation. The resulting film was impossible to remove; hence, further work on the sample had to be abandoned. We solved this problem by exposing the implanted sample to 5 minutes of NH_3 plasma before depositing the Si_3N_4 film. The NH_3 plasma removed the surface oxide layer and promoted better adhesion between the film and the GaAs surface [94].

Annealing was performed in the Mini Brute furnace in flowing N_2. The annealing procedure described in step 16 was followed to avoid introducing excessive strain between the Si_3N_4 film and the GaAs surface. Samples were sometimes sandwiched between two pieces of clean silicon wafers to make sure that the Si_3N_4 film did not crack during annealing. After annealing, the Si_3N_4 film was removed by freon plasma. 10% HF solution can also be used.

For ohmic metal (Au-Ge) and gate metal (Al) liftoff, the resist was soaked in chlorobenzene for 2.5 minutes before developing. The chlorobenzene hardened the surface of the resist and upon development, an 'overhang' was produced in the resist which was found to aid the liftoff process [95].

Ohmic metal, Au-Ge, is evaporated in step 24. It is important to soak the sample in $1NH_4OH:10H_20$ mixture prior to evaporation. This mixture

helps remove the surface oxide layer and resist that was not removed during developement. This same soak was also performed prior to gate metal deposition. It has been shown that the $1NH_4OH:10H_2O$ treatment before Schottky contact metal evaporation gave better diode characteristics [47].

Alloying was performed in the Mini Brute furnace in flowing N_2. The alloying temperature was 415°C and the duration was 2 minutes. The SPA was used to check the drain source current. This is a very simple method to determine if there is a channel or not. Further fabrication is futile if there is no channel between the drain and source pads.

The final few fabrication steps, 30 to 36, involve the deposition of the gate metal. Here no alloying is needed to obtain the Schottky characteristics of the gate. After the gate metal deposition, fabrication is complete and the MESFETs are now ready for measurement. A photograph of a fabricated array of MESFETs is given in figure 4.4. The dark region at the top of the photograph is the edge of the wafer. The MESFET array is flanked by regions that are formed because all the fabrication levels are placed on the same mask.

4.3.3 MEASUREMENT

Measurements were performed using a HP9816 computer, a HP 4145A semiconductor parameter analyser and a Wentworth Labs probe station. The probe station was placed in an electrically shielded box which also acted as a light shield. This is important for ensuring reliable measurements because the channel current is extremely sensitive to light. Since an automatic prober is not available, the probes had to be manually moved. Precautions were taken to make sure that the probes were applied with

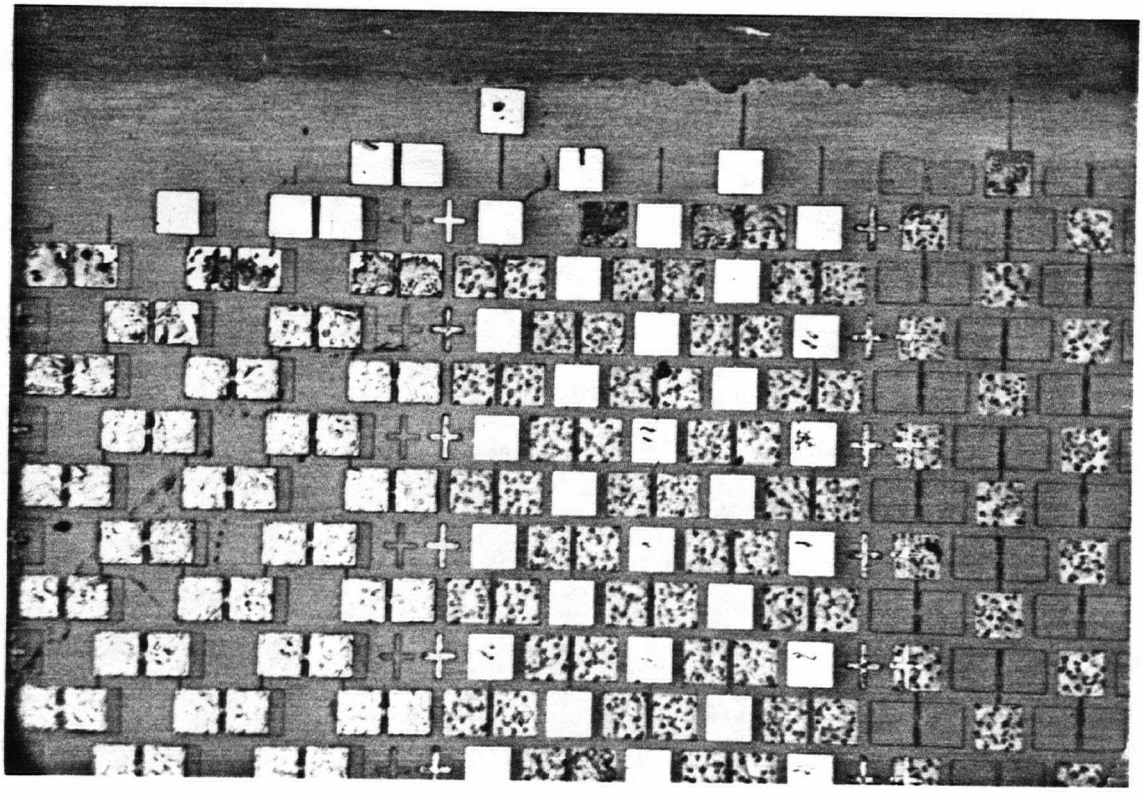


Figure 4.4: Fabricated MESFET Array

light and consistent pressure on each set of pads as the threshold voltage varied as much as 25mv due to pressure.

Only the threshold voltage of the fabricated devices was measured. The threshold voltage was measured with 2.5 volts applied between the drain and source, to ensure that the MESFETs were operating in the saturation region. Two techniques were used to determine the threshold voltage. In the first method, the threshold voltage was defined as the gate voltage at which the drain source current was 5μA with 2.5 volts applied

between the drain and source. In the second method, a square root drain source current versus gate voltage was assumed. The threshold voltage here was defined as the zero current intercept of a line drawn through $\sqrt{I_{dss}}$ at zero gate voltage and $0.1\sqrt{I_{dss}}$ at the appropriate gate voltage (I_{dss} is the drain to source current at zero gate voltage). In the second technique, 2.5 volts was also applied between the drain and source pads. Both the threshold voltage were computed and stored onto the hard disk of the HP9816 before the next transistor was measured. The program used is similar to the one given in appendix A.

To correlate the measured device characteristics with dislocations, the samples have to be etched in molten KOH to reveal etch pits corresponding to the dislocations. The molten KOH etch was done at Cominco in Trail. The sample was first placed in a nickel crucible, then a pre-determined (from trial runs using dummy samples) amount of KOH beads were placed in the crucible before covering it with a lid and placing it in an oven. After an etch time of about 5 minutes, the sample was removed from the oven, cooled and rinsed in DI H_2O.

The MESFET metallisation was removed by the etch but the registration marks and the ohmic and gate pads are still clearly outlined (figure 4.5). These features were used to deduce the location of the MESFETs on micro-photographs taken of the MESFET array. The micro-photographs were taken at 100X magnification. The distance between the MESFET and the nearest dislocation and the etch pit densities were all obtained using the micro-photographs. The etch pit density was calculated from a 200μm x 200μm square area centred on the MESFET.

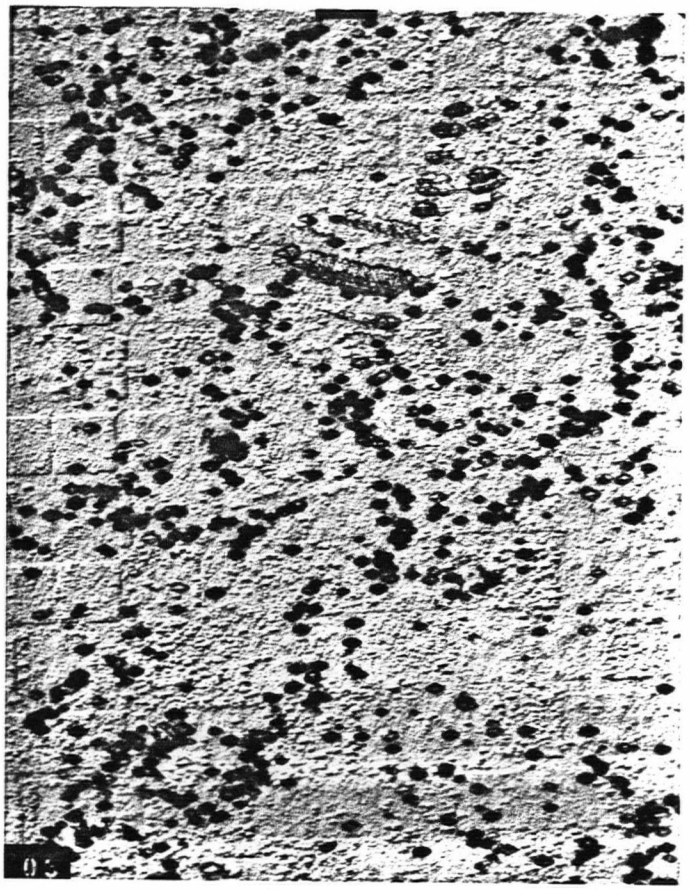


Figure 4.5: Micro-photograph Of Etched Sample With Registration Marks Left Behind

4.4 RESULTS AND DISCUSSIONS

The slice tested, 429s122G, is from wafer 429s122 supplied by Cominco Limited. Its position on the wafer is as depicted in figure 4.6. MESFETs fabricated on the sample, which is roughly the size of a 1.7cm radius quadrant, have gates perpendicular to the major <110> flat. 10 columns of transistors, about 800 in number, were measured. However, only two columns were included in this study because the sample was slightly over-etched by Cominco. Three other samples sent to Cominco were

completely over-etched. The molten KOH etch should ideally reveal hexagonal pits at locations where dislocations meet the surface, and at the same time leave a 'ghost' of the devices behind (figure 4.5). But, when a sample is over-etched, no trace of the original devices is left behind making it impossible to pin point their original position.

Out of the 148 devices used in this study, 141 were functional. The rest of the devices were not tested either because of poor gate definition or a non-existent gate. A typical MESFET I-V characteristic is shown in Figure 4.7. At saturation drain source voltages, the drain current is constant which is ideal in MESFETs. Shown in figure 4.8 are I_d and $\sqrt{I_d}$ versus V_g curves for the same transistor.

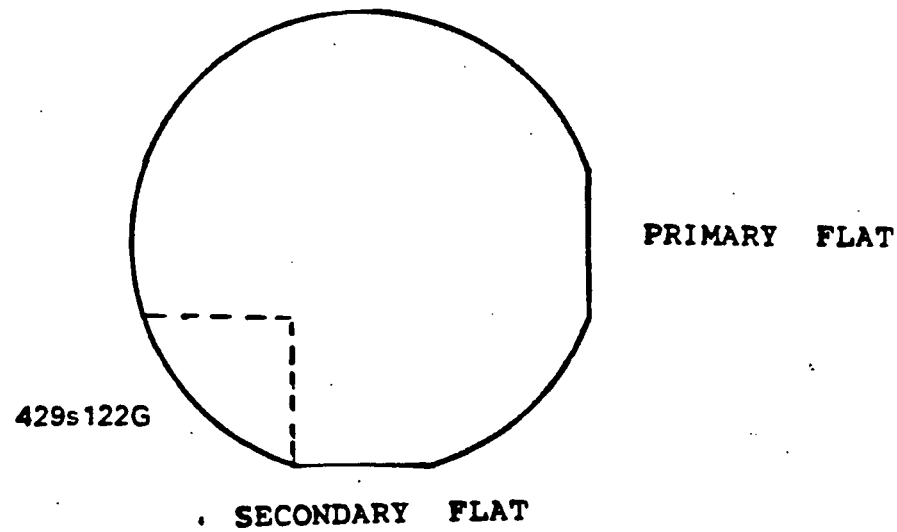


Figure 4.6: Position Of Sample 429s122G On Wafer

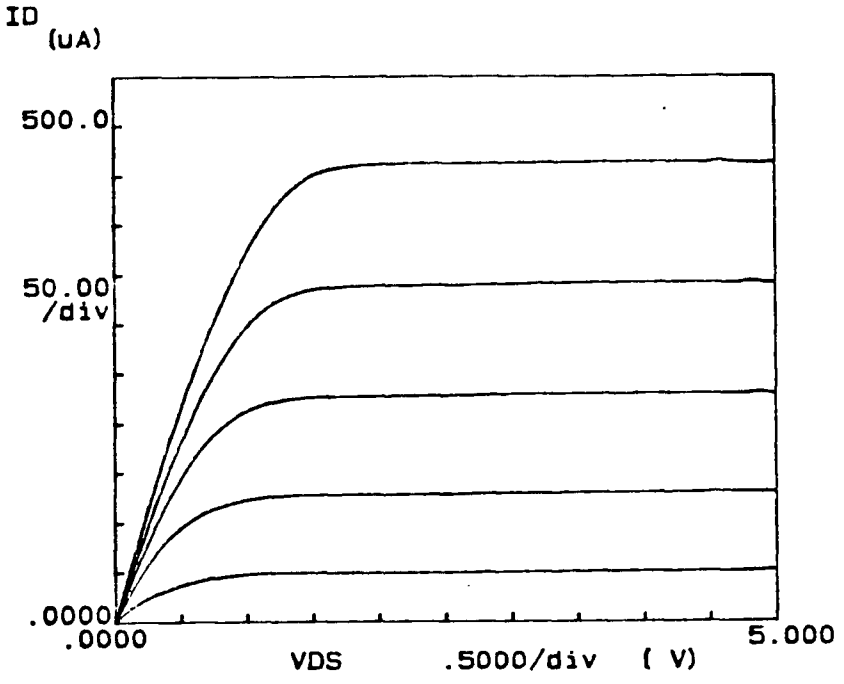


Figure 4.7: Typical MESFET I-V Characteristics

The threshold voltage of transistors can be determined in a number of ways. Two techniques commonly used by experimenters working on the uniformity of V_{th} were investigated. The first, V_{tha}, was based on the I_d versus V_g curve [83], and the second, V_{thb}, was obtained from $\sqrt{I_d}$ versus V_g curves [87]. V_{tha} values were found to be less negative than those of V_{thb}, the average of the former is -1.71 volts and the latter is -1.86 volts. The standard deviations of V_{tha} and V_{thb} are 0.18 volt and 0.19 volt respectively.

In the saturation region, I_d, can be written as:

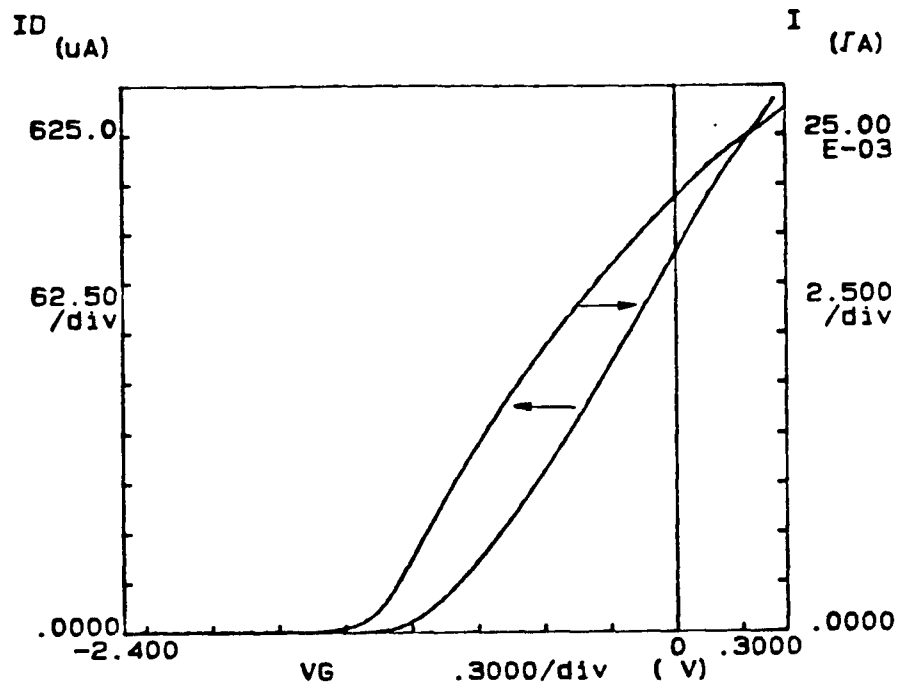


Figure 4.8: I_d and $\sqrt{I_d}$ Versus V_g Of The Same MESFET In Figure 4.7

$$I_d = K(V_g - V_{th})^2 \qquad (4.1)$$

where $K=\mu\epsilon W/(2aL)$ with μ, ϵ, W, L and a as the mobility, the permittivity, the gate width, the gate length and the channel depth respectively. Although, V_{thb} is theoretically correct, V_{tha} values will be used from now on because they gave a good approximation to V_{thb} as can be seen in figure 4.9. Furthermore, V_{tha} is computationally simpler. A histogram of V_{tha} distribution is given in figure 4.10. Good distribution of the threshold voltage was obtained.

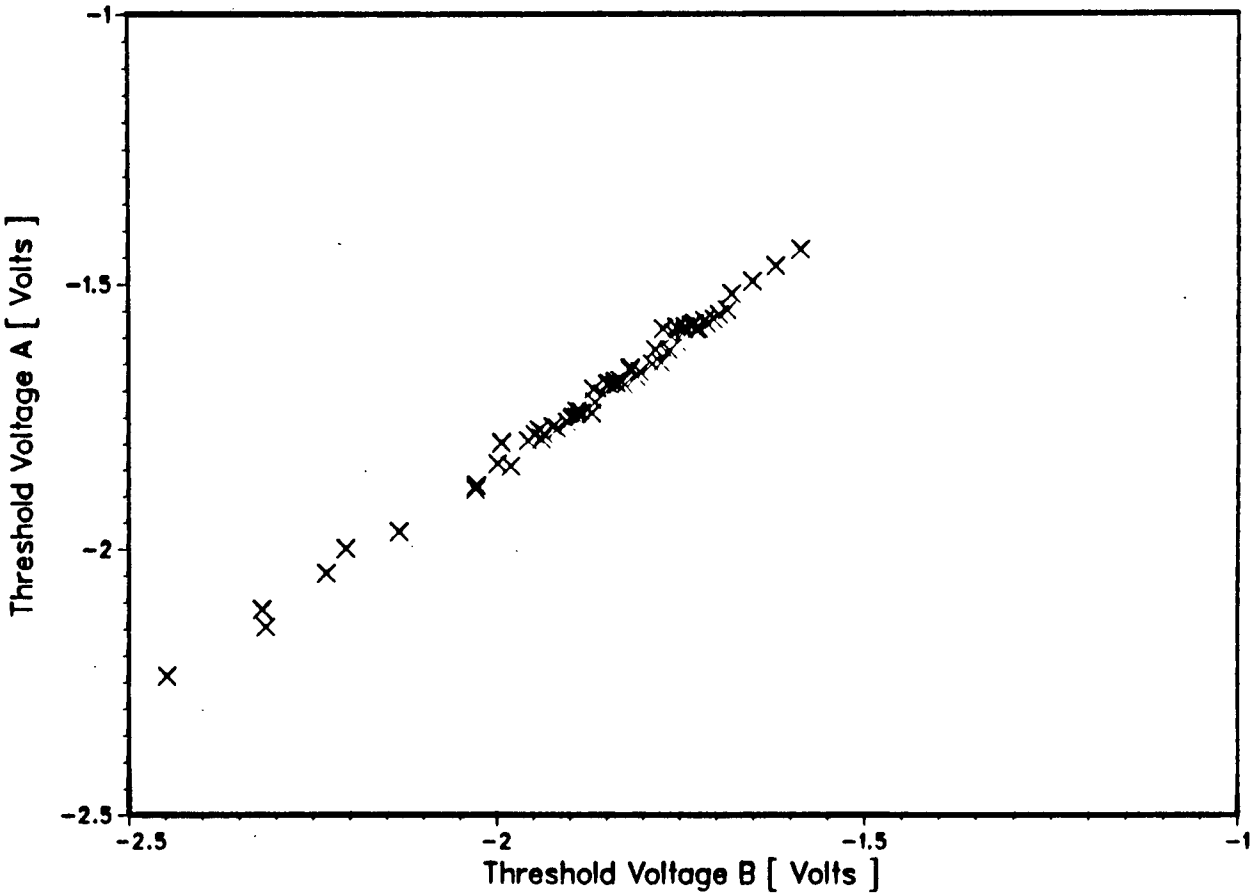


Figure 4.9: Plot Of V_{tha} Versus V_{thb}

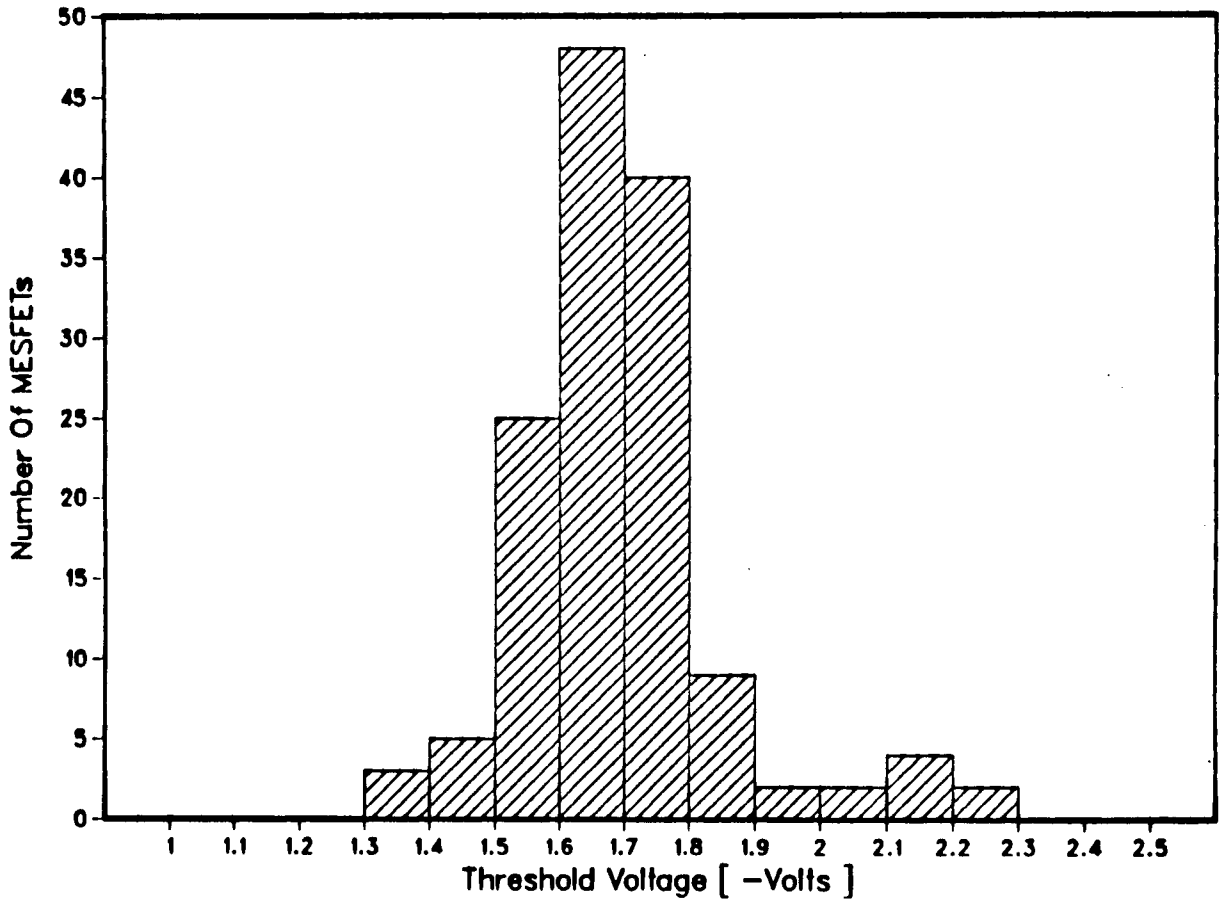


Figure 4.10: Histogram Of Threshold Voltage

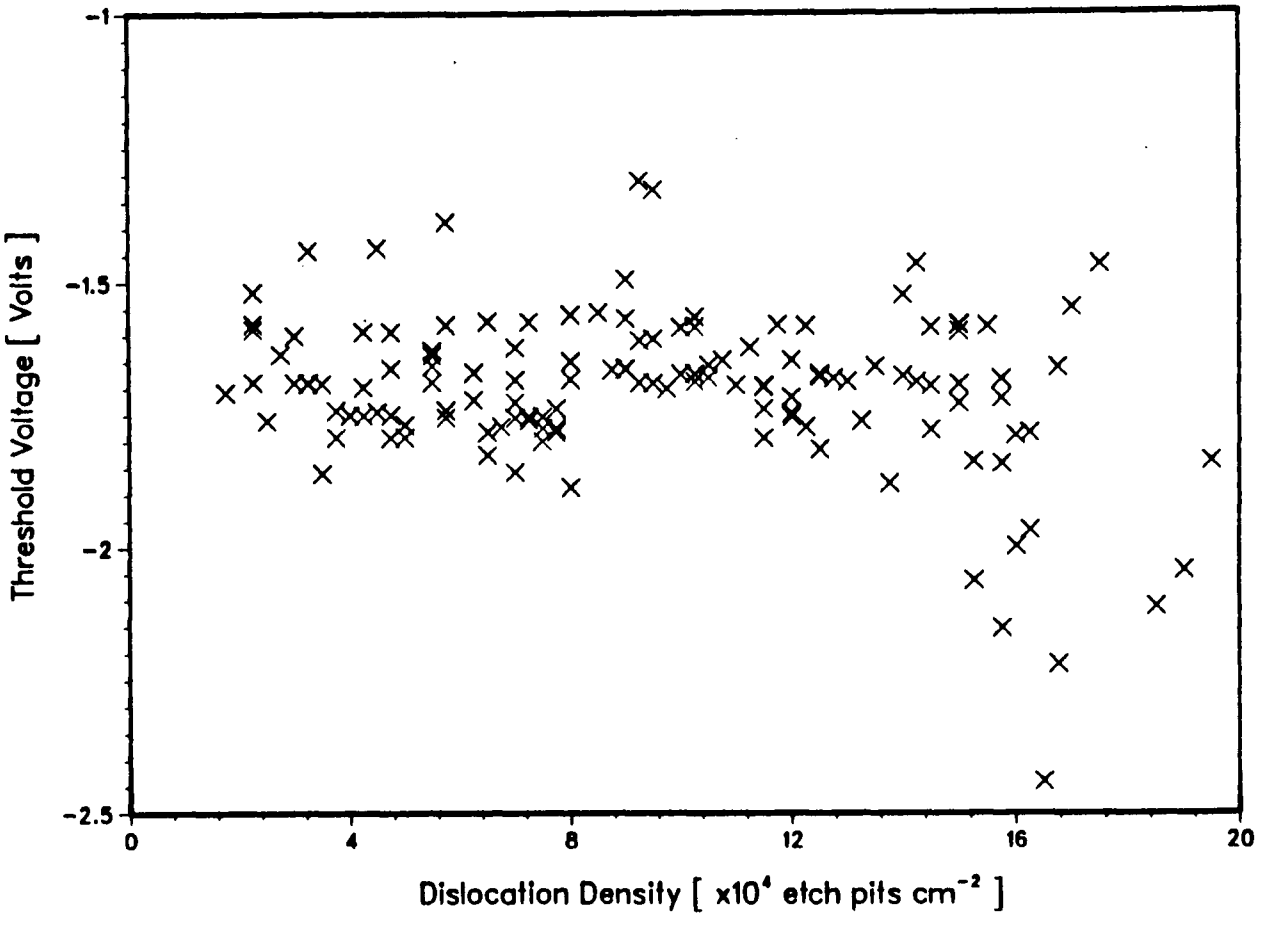


Figure 4.11: Dislocation Density Versus Threshold Voltage

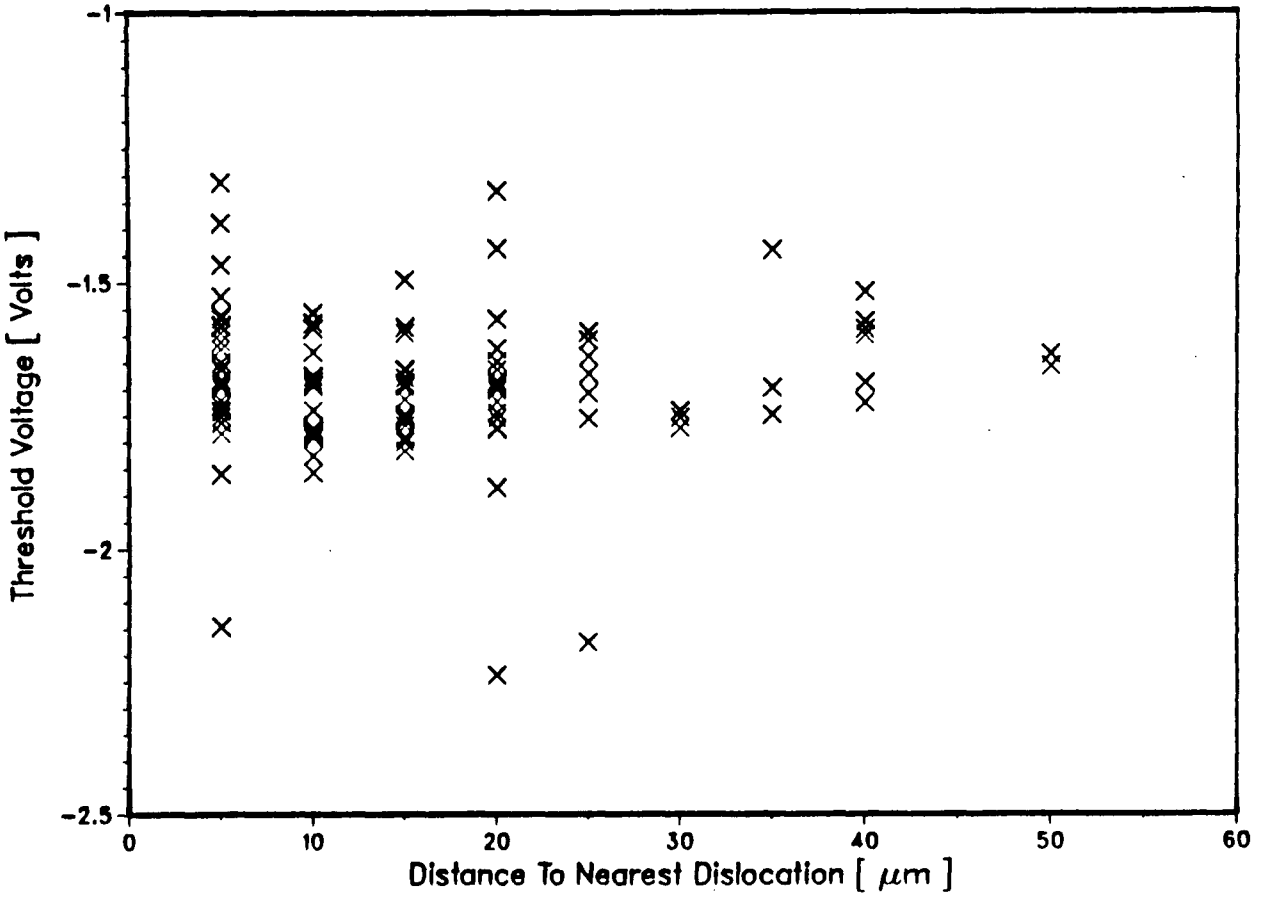


Figure 4.12: Threshold Voltage Versus Nearest Distance To A Dislocation

A plot of dislocation density and V_{th} is shown in figure 4.11. It appears from the plot that V_{th} is lower in regions with dislocation density greater than 1.3 x 10^5 per cm^2. Below this dislocation density no definitive trend can be detected. The abrupt drop in threshold voltage in regions with more than 1.3 x 10^5 etch pits per cm^2 is probably due to the small number of MESFETs available in those regions. From the same set of MESFETs, a plot of distance to the nearest and V_{th} was also obtained and this is depicted in figure 4.12. It shows no evidence of any effect distance from a dislocation has on MESFET V_{th}.

4.5 DISCUSSIONS

Our results on the influence of dislocation density on threshold voltage agree with those of Miyazawa et al. [83] and Winston et al. [87]. As pointed out before, V_{th} was found to be lower in high dislocation regions. Better activation in high dislocation density regions is directly reponsible for the observed V_{th} variation. Since dislocations act as sinks for point defects and impurities, purer regions are obtained in the vicinity of dislocations resulting in the higher activation of implanted dopants.

Winston et al. [87] also found no correlation between MESFET V_{th} and its proximity to a dislocation. The plot of threshold voltage versus nearest distance to a dislocation obtained by Winston et al. [87] is reproduced in figure 4.13. This is in disagreement with the results of Miyazawa et al. [85]. He found the existence of a 20–30μm radius area surrounding etch pits, within which V_{th} is algebraically lower. Such a cylinder of influence, commonly known as the Cottrell atmosphere, was also observed by Chin et al. [62] using cathodoluminescence.

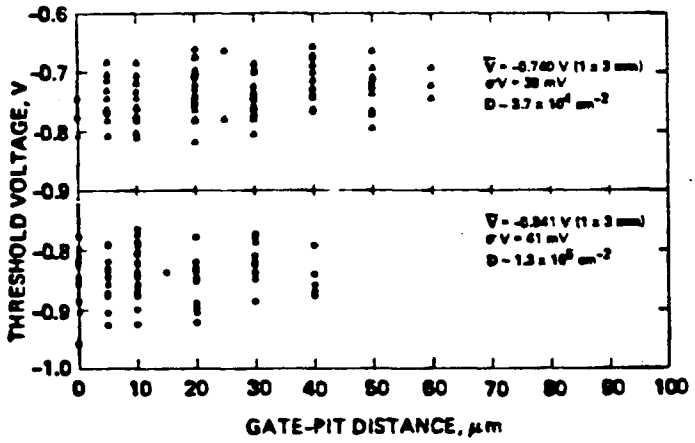


Figure 4.13: Plot Of MESFET Threshold Voltage Proximity To A Dislocation Obtained By Winston et al. [87]

It has been suggested that an erroneous correlation between MESFET V_{th} and its proximity to a dislocation can be obtained when such a plot is obtained for a 2" wafer [87]. Since V_{th} is more negative at high dislocation density regions, it is inevitable that algebraically lower V_{th} will have smaller nearest etch pit distances. This means that when a plot is done for a localised area, such as in the case here, no correlation between MESFET V_{th} and its proximity to a dislocation should be obtained.

To summarise, MESFETs fabricated in regions with dislocation density higher than 1.3×10^5 per cm^2 appear to have lower V_{th}. In a localised area, MESFET proximity to a dislocation was not found to have any effect on its electrical characteristics. Unfortunately, from the data available, no statement can be made on the effects of dislocation networks on MESFETs V_{th}.

5. CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

The aim of this thesis was to study the effects of the removal of the surface layer and also the influence of dislocations on the electrical characteristics of ion implanted GaAs MESFETs.

The first part of this work found that the removal of approximately 2μm of the top layer of the starting substrate supplied by Cominco resulted in:

1. A higher activation efficiency in the implant.

2. Improved transistor characteristics. The zero gate voltage saturation current, transconductance and K-factor all increased in magnitude while the threshold voltage became more negative.

3. An ion implanted layer with better electron transport characteristics. This was concluded from the results of Hall mobility and K-factor measurements. The lower drift mobility obtained from the FATFET measurements was probably due to poor Schottky diode characteristics.

4. Less backgating effect when MESFETs in approximately the same location on the sample were compared.

Clearly, a more suitable substrate for direct ion implantation was obtained after a surface removal. However, the etch left behind less desirable surface (as confirmed by the poor Schottky diode characteristics).

In the second part of this work, the effects of dislocations were investigated and the following findings were made:

1. It appears that dislocation density affects device characteristics. MESFETs in regions with dislocation density larger than 1.3×10^5 per cm^2 have more negative threshold voltage.

2. Proximity to a dislocation centre was not found to have any influence on MESFET threshold voltage.

Unfortunately, it is not known from the results of this section whether dislocation networks have any effect on the scatter of MESFET threshold voltage.

The work done for this thesis suggests that efforts would be best directed in the following areas:

1. Although the removal of approximately 2μm of top layer of Cominco's wafer resulted in a better substrate, wafers from other crystal growers should also be studied because different growth and polishing procedures are used. The possibility exists that such an etch may not be necessary.

2. The surface before and after the etch should be investigated for impurities and surface damage using such techniques as secondary ion mass spectroscopy (SIMS) and Auger electron spectroscopy (AES).

3. To study the effects of dislocation networks, substrates with 1-5 x 10^4 etch pits per cm^2 should be used because dislocation networks are more clearly defined.

4. The effects of dislocations should be investigated with different dose and energy implants.

5. Also, for further work an automatic prober would drastically reduce the time required to measure the MESFETs.

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APPENDIX A

```
10     ! SET MASS STORAGE UNIT TO HARD DISK.
20      MASS STORAGE IS ":HP9133,700"
30      DIM Cur$[25],In$[1],I(31),Isqrt(31),Idss(100),Vtha(100),Vthb(100)
,Gm(100),File1$[10],File2$[10],File3$[10],File4$[10]
40      INTEGER M,J,K
50      REAL V1,V2,I1
60      L_val=-9.9999
70     ! SEMICONDUCTOR PARAMETER ANALYSER IS ON INTERFACE SELECT CODE 7
80     ! AT PRIMARY ADDRESS 17.
90      Spa=717
100     P=31
110     INPUT "ENTER THE DATA FILE NUMBER",M
120     File1$="F_VTHA"&VAL$(M)
130     File2$="F_VTHB"&VAL$(M)
140     File3$="F_IDSS"&VAL$(M)
150     File4$="F_TRAN"&VAL$(M)
160     CREATE BDAT File1$,4
170     CREATE BDAT File2$,4
180     CREATE BDAT File3$,4
190     CREATE BDAT File4$,4
200    ! OPEN DATA PATH TO FILES.
210     ASSIGN @Path_1 TO File1$
220     ASSIGN @Path_2 TO File2$
230     ASSIGN @Path_3 TO File3$
240     ASSIGN @Path_4 TO File4$
250     K=0
260 Measure:J=0
270    ! SET SPA TO USER MODE.
280     OUTPUT Spa;"US"
290    ! SET MEASUREMENT INTEGRATION TIME (IT2), AUTO CALIBRATION (CA1),
300    ! AND BUFFER CLEAR.
310     OUTPUT Spa;"IT2 CA1 BC"
320    ! SCAN GATE VOLTAGE FROM -2.5V TO .5V USING A STEP OF .1V.
330     FOR Vgs=-25 TO 5 STEP 1
340       V1=Vgs/10
350    ! CONNECT SOURCE TO SMU1, DRAIN TO SMU2 AND GATE TO SMU3.
360       OUTPUT Spa;"DV1,1,0,2E-3"
370       OUTPUT Spa;"DV2,1,2.5,2E-2"
380       OUTPUT Spa;"DV3,1,";V1;",1E-3"
390      ! TRIGGER CURRENT MEASUREMENT OF SMU2.
400       OUTPUT Spa;"TI2"
410      ! ENTER MEASUREMENT DATA INTO THE STRING, CUR$.
420       ENTER Spa;Cur$
430       PRINT J,Cur$
440      ! CHECK TO SEE IF THE MEASUREMENT IS NORMAL.
450       IF Cur$[1,1]<>"N" THEN
460         BEEP
470         GOTO Problem
480       ELSE
```

```
490         J=J+1
500        ! TAKE VALUE OF NORMAL STRING.
510         I(J)=VAL(Cur$[4])
520       END IF
530     NEXT Vgs
540    ! CHECK CHANNEL BY MONITORING LAST POINT OF CURRENT ARRAY.
550     IF I(P)<=5.E-6 THEN
560       GOTO Channel
570     END IF
580     ! CHECK GATE BY MONITORING FIRST POINT OF CURRENT ARRAY.
590     IF I(1)>=5.E-6 THEN
600       GOTO Gate
610     ELSE
620       K=K+1
630      ! CALCULATE THE THRESHOLD VOLTAGE USING THE FIRST METHOD. IT IS
640      ! THE GATE VOLTAGE VALUE WHEN THE DRAIN CURRENT IS 5.E-6.
650       FOR J=1 TO P
660         IF I(J)>=5.E-6 THEN
670           GOTO Volt1
680         ELSE
690           GOTO Next1
700         END IF
710 Next1:NEXT J
720 Volt1:Vth(K)=-2.5+.1*(J-1)-.1*((I(J)-5.E-6)/(I(J)-I(J-1)))
730     END IF
740    ! STORE DRAIN CURRENT WHEN GATE VOLTAGE IS 0V.(IDSS)
750     Idss(K)=I(26)
760    ! CALCULATE THE TRANSCONDUCTANCE (ITS UNIT IS IN MS/MM)
770    ! AND STORE INTO ARRAY.
780     Gm(K)=(I(27)-I(26))*7.143E+5
790    ! TAKE THE SQUARE ROOT OF THE DRAIN CURRENT VALUES.
800     FOR J=1 TO P
810       Isqrt(J)=SQR(I(J))
820       PRINT J,Isqrt(J)
830     NEXT J
840   ! CALCULATE THE THRSHOLD VOLTAGE USING THE SECOND METHOD.
850   ! IT IS THE X-INTERCEPT VALUE OF THE LINE PASSING THROUGH
860   ! SQUARE ROOT IDSS AND .1*(SQUARE ROOT IDSS) IN THE SQUARE
870   ! ROOT ID VERSUS VGS PLOT.
880     I1=SQR(Idss(K))
890     FOR J=1 TO P
900       IF Isqrt(J)>=.1*I1 THEN
910         GOTO Volt2
920       ELSE
930         GOTO Next2
940       END IF
950 Next2:NEXT J
960 Volt2:V2=-2.5+.1*(J-1)-.1*((Isqrt(J)-.1*I1))/(Isqrt(J)-Isqrt(J-1))
970     PRINT V2
```

```
980    Vthb(K)=V2/.9
990 Question:DISP "DEVICE # IS",K
1000   PAUSE
1010   LINPUT "ARE THERE ANYMORE MEASUREMENTS TO BE TAKEN? Y OR N",In$
1020   IF In$="Y" THEN
1030     GOTO Measure
1040   ELSE
1050     IF In$="N" THEN
1060       GOTO Finish
1070     ELSE
1080       GOTO Question
1090     END IF
1100   END IF
1110 Channel:DISP "POOR OR NO CHANNEL"
1120   PAUSE
1130   GOTO Large_val
1140 Gate:DISP "POOR GATE OR VTH < -2.5 VOLTS"
1150   PAUSE
1160   GOTO Large_val
1170 Problem:DISP "ERROR IN MEASUREMENT"
1180   PAUSE
1190   ! STORE LARGE VALUES INTO ARRAYS IF MEASUREMENT CANNOT
1200   ! BE DONE.
1210 Large_val:K=K+1
1220   Vtha(K)=L_val
1230   Vthb(K)=L_val
1240   Idss(K)=L_val
1250   Gm(K)=L_val
1260   GOTO Question
1270 Finish:DISP "THE # OF DEVICES MEASURED IS",K
1280   ! STORE ,K, THE # OF DEVICES MEASURED INTO ALL THE
1290   ! FILES.
1300   OUTPUT @Path_1;K
1310   OUTPUT @Path_2;K
1320   OUTPUT @Path_3;K
1330   OUTPUT @Path_4;K
1340   ! STORE DATA ARRAYS INTO THEIR RESPECTIVE FILES.
1350   OUTPUT @Path_1;Vtha(*)
1360   OUTPUT @Path_2;Vthb(*)
1370   OUTPUT @Path_3;Idss(*)
1380   OUTPUT @Path_4;Gm(*)
1390   ! STOP OUTPUT FROM SMU1, SMU2 AND SMU3.
1400   OUTPUT Spe;"DV1;DV2;DV3"
1410   ! CLOSE DATA PATH TO THE FILES.
1420   ASSIGN @Path_1 TO *
1430   ASSIGN @Path_2 TO *
1440   ASSIGN @Path_3 TO *
1450   ASSIGN @Path_4 TO *
1460   END
```