PHOTOVOLTAIC ARRAY SIMULATORS

by

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ABSTRACT

Two basic types of photovoltaic (PV) array simulator have been designed and tested. The first involves the use of a pilot panel and variable light source. It is implemented with analogue circuits. A stability analysis based on Popov's method is presented for this simulator with resistance-inductance (R-L) loads. In the second, characteristic array curves are stored in the memory of a microprocessor-based simulator. The design of both simulators is based on the transfer function method. By using the computing facility available, a stability study for the Type I simulator and some dynamic simulations are carried out. Both simulators are capable of driving a special load, namely, an experimental solar pumping system. The experimental results for both types of simulator are satisfactory in terms of steady state precision and dynamic behaviour when used with this load.

Compared with previously-reported PV array simulator designs [6,7,8,9,18], the two simulators described here have the following distinctive features:

1. A new method of sample curve generation for the Type II simulator results in relatively short sampling period and small memory size.

2. The sample curves of the type II simulator are based directly on the real PV array to be simulated. They are more accurate than the sample curves in references [6,7,9].
3. Different loads (R, R-L and an experimental solar pumping system) have been considered in the design and have been tested in laboratory.

4. A stability analysis and some dynamic simulations are presented for the type I simulator. An analysis of this type has not been reported in previous studies [6,7,8,9,18].
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1. INTRODUCTION

Solar energy is a promising energy source for the future. When other non-renewable energy sources, such as gas, oil and coal, become limited and expensive, electric energy from photovoltaic arrays will be economically competitive. Some experts in this field have given quite optimistic predictions. It has been predicted [1] that in a region with an annual insolation level of 1750 kwh/m² (tropics), the electricity from PV arrays will be cheaper than that from conventional power grid by the year 2000.

1.1 PV ARRAY POWERED SYSTEMS

A sketch showing a typical PV array-powered system is illustrated schematically in Figure 1-1. When the PV array is exposed to sunlight, it becomes a power source with the current/voltage (I/V) characteristics shown in Figure 1-2.

![Solar Cell System Diagram](image)

Figure 1-1. Functional Elements of A Solar Cell System

As can be seen, the I/V characteristics of a PV array vary
with both the light intensity and temperature. For this reason, 'power conditioning' and 'power storage' elements are necessary in most systems. Typical 'electrical loads' in a stand-alone system are light bulbs, electrical appliances in residences, motors in a pumping system or, in interconnected systems, the PV array could feed power into the grid. Taking a residential system as an example [4], the power demand of a residence over a typical 24-hour period during the Spring and the power a PV array may produce are shown in Figure 1-3. As can be seen, from 6 am to 6 pm, the PV array output power exceeds the power needed.

![Figure 1-2 Typical PV Array Characteristics](image-url)
To make good use of this energy, it is stored in batteries. At other times, when the power demand of the residence exceeds the power output of the PV array, the demand can be met by releasing the energy stored in the batteries. These functions are controlled by the power conditioner.

A further function of the power conditioner is to ensure that the total load is matched to the array so that maximum power is always extracted. This corresponds to operation close to the 'knee' of the curves of Figure 1-2. This matching must be done continuously as load and sunlight conditions change.

In some simple systems the power conditioner is eliminated, with the load being connected directly to the array. The overall efficiency of these systems is low since
the maximum power tracking function is not present.

The purpose of the work described in this thesis is to design a circuit which will produce an output characteristic of the type shown in Figure 1-2. This will allow for research on many different types of loads to be performed in the absence of a real array. This will remove any reliance on prevailing weather conditions, and should also provide some cost savings.

Two approaches to the design of a simulator are described in the next section. The emphasis of the work described here is on the circuit design. The stability analysis of the system is complex and is only performed for certain load conditions. The completed simulator is to be used to supply a pumping system. Initial tests with this load have been satisfactory.

1.2 PV ARRAY SIMULATORS

The requirements of a simulator vary according to the load to be tested. For instance, in laboratory testing of a PV array-powered pumping system, one may need the I/V curve of the array to be fixed for a period of time so that measurement and comparisons can be done. It is not possible to count on the natural environment to provide a fixed light intensity and temperature, and it is costly to build up an artificial environment for a large size array. However, it is easy for the PV array simulator to output a fixed I/V characteristic curve.
A PV array simulator is a controlled power source that can produce output characteristics mimicking that of a real PV array. A power converter is usually used, and it can be an ac to dc bridge converter or a dc to dc chopper. Though control schemes may differ very much from each other, they basically consist of sample curve generation and control loops.

1.2.1 PREVIOUS SIMULATOR DESIGNS

In reference [6], sample curves are obtained by calculating a series of formulae. The steady state error is reasonably small. However, due to the relatively long sampling period caused by the formula calculation, the dynamic response is not very fast (0.3 second). In reference [7], the control function is implemented with analogue circuitry. A chopper (switching regulator) is used as the power converter. The sample curve is obtained by physical simulation based on the solar cell equivalent circuit. The step response of this simulator is very fast (about 20 ms). However, the effect of temperature is not considered. A comparison between the I/V curves of the simulator and those of the real array was not reported. Reference [9] describes a low cost simulator. In that report, an I/V curve is divided into two linear sections and one non-linear section (around the maximum power point). The non-linear section is approximated by an exponential curve and is implemented with an analogue exponential multiplier. The steady state
accuracy is not as good as that of reference [6]. The information regarding dynamic response is not provided.

All the simulators mentioned above produce fixed, repeatable I/V curves which are not subject to the influence of the environment. In references [8 & 18], solar cells are used to obtain sample curves. As a result, the output I/V curves of these simulators are subject to the influence of the environment. However, transient response is not discussed in either reference.

1.2.2 SIMULATOR REQUIREMENTS

The overall design of a simulator is governed by the requirements of the application. It may be desirable to reproduce a continuous variation in the I/V characteristics, as might be experienced during a typical operating day, for example, during the field test of PV array-powered systems. The simulators reported in references [8, 18] are suitable for this kind of application. Alternatively, it may be required that a particular, repeatable I/V characteristic should be produced for comparison purposes. In this thesis, two different types of PV array simulators are introduced, which will be referred to as type I and type II. The major difference between these two types of simulators is the way they generate sample curves. A small PV panel is used as a pilot in the type I simulator. The pilot panel can be put outdoors, being influenced by the natural environment, or it can be placed in a light and temperature
controlled environment. The control unit of the type I simulator keeps the simulator output current proportional to the pilot panel current, and the simulator output voltage proportional to the pilot panel voltage. As a result, the I/V curves of the simulator are amplified versions of those of the pilot panel. The steady state error (compared with the pilot panel) is within 1%. More detailed discussion about the steady state error of the type I simulator is given in Chapter 4. The transient state caused by a step change of load from open circuit to maximum power point is about 50 ms. In the type II simulator a pilot panel is not used. Instead, reference I/V curves are stored in the memory of a microprocessor system. In the system described here the sample curve generation and control tasks are implemented using a Motorola 6809 Microprocessor. The method used for sample curve generation is a combination of formula calculation and data storage, which is a trade-off between execution time and memory size. Different curves can be selected by setting a code. Once a curve is selected, the type II simulator can output an I/V characteristic corresponding to this curve for as long as is required.

The load connected to the simulator is an experimental pumping system. The regulator in the pumping system matches the dc motor to the array so that when the I/V curve of the array changes with the light intensity and temperature, the operating point is kept close to the maximum power point. The regulator adjusts the operating point approximately 10
times every second.

Resistive and resistive-inductive loads are also considered in this thesis.

For both types of simulator studied in this work, the power converter is a one quadrant (positive voltage, positive current) power transistor chopper with high switching frequency and low switching losses.

The major contributions of this thesis are:

1. Two new designs of PV array simulator are presented. These simulators can be used with a particular solar pumping system load and some other loads, such as $R$, $R-L$ and dc motor loads.

2. A stability analysis for the type I simulator and some partial dynamic simulations have been carried out. The results of this analysis and simulations help the designer to choose system parameters properly so that instability (oscillation) will not occur, have not been reported previously.

The detailed design of a type I simulator and practical problems encountered during testing of the simulator are presented in Chapter 2. Chapter 3 provides the details of the design and testing of a type II simulator. Some discussion of the two simulators is given in Chapter 4. Finally, conclusions are drawn in Chapter 5.
2. TYPE I SIMULATOR

2.1 DESIGN CONSIDERATIONS FOR TYPE I SIMULATOR

The basic requirements of a type I simulator are listed below:

1. The steady state error must not exceed 5% in order to assure the accuracy of the experiment using this simulator.

2. The transient state caused by a step change of load from open circuit to maximum power point must not exceed 150 ms. Slower response will affect the operation of the pumping system connected to it.

3. The open circuit voltage and short circuit current must be adjustable.

4. The simulator must be capable of driving an experimental solar pumping system load as well as R and R-L loads.

5. The output I/V curve should be capable of smooth adjustment between different insolation conditions.

To meet the requirements listed above, various design features had to be considered. These are described below.

2.1.1 SAMPLE CURVE GENERATION

Sample curve generation is important to the overall performance of the simulator because the output of the simulator is controlled to follow the sample curve. In reference [7], physical simulation is used. The sample curve is based on the equivalent circuit shown in figure 2-1. This
equivalent circuit is implemented using the analogue circuit illustrated in figure 2-2. By varying the base bias of Q1, one can change the value of the current source so that the variation of light intensity is simulated. Rs and Rp can be adjusted easily to simulate PV arrays with different values of Rs and Rp.

![Figure 2-1. Solar Cell Equivalent Circuit](image)

Figure 2-1. Solar Cell Equivalent Circuit

![Figure 2-2. One Way to Generate Sample Curves](image)

Figure 2-2. One Way to Generate Sample Curves

However, the influence of temperature is not simulated
properly in this scheme. Reference [6] uses formulae based on theoretical analyses to produce sample curves. Once the light intensity, temperature and specific array type are given, the formulae can reproduce the I/V curve with satisfactory precision. Moreover, to simulate different types of PV array, one only need adjust certain constants accordingly. This method can reproduce a repeatable sample curve quite well. However, both methods mentioned above are unsuitable for the type I simulator because neither can simulate the influence of the environment easily. As mentioned in Chapter 1, the pilot panel method has been chosen to form the sample curves for the type I simulator. Because the sample is taken from the PV panel, which is a reduced version of the PV array, this method produces sample curves closer to the real array curves than the previously reported methods [6,7,9]. More importantly, the sample curve is affected by the environment in the same manner as the curve from a real array might be.

2.1.2 CONTROL LOOPS

Although digital circuitry can be used, it is more convenient to use analogue circuitry to form the control loops because the sample curves generated with the pilot panel method are analogue signals. A voltage loop and a current loop are considered in the design of type I simulator. The voltage loop keeps the output voltage proportional to that of the pilot panel and the current loop
keeps the current of the pilot panel following the load current. Proportional-integrational (PI) compensators are used in both control loops. With PI compensators, zero steady state error can theoretically be achieved. The parameters can be adjusted to achieve satisfactory dynamic behaviour. Because the sample curves are non-linear and the load parameters may fall within a wide range of values, stability may be a problem. To investigate such problems, a computer program has been developed to assess the stability for a particular load condition. Details of the stability analysis are described in section 2.3. The algorithm of the program is given in Appendix A. The complete program listing is given in Appendix B.

2.1.3 POWER CONVERTER

The power converter used here is a one quadrant power transistor chopper operating at 25 KHz. This is based on the consideration of getting fast response without substantially increasing the switching losses.

The circuit diagram of the chopper is shown in Figure 2-3. The power transistor in Figure 2-3 works as a power switch controlled by the base voltage. If the base voltage is positive 5 volts, the switch is on; if the base voltage is negative 5 volts, the switch is off. By controlling the lengths of the on period and off period, the output average voltage of the chopper can be adjusted. Figure 2-4 shows the base drive signal and the waveform of the corresponding
output voltage of the chopper.

Figure 2-3. Circuit Diagram of the Chopper

The dotted lines in Figure 2-4 represent the average chopper output voltage of each cycle. The average output voltage of the chopper is given by the following relation:

\[
V_{ch} = (\text{d.c. source voltage}) \cdot \delta
\]

where, \( \delta \) is the duty ratio of the chopper. Alternatively, an ac to dc converter can be used where a dc source is unavailable. However, the operating frequency would be limited by the ac source frequency. This may result in a larger filter time constant and slower dynamic response. A resistor, \( R_{18} \) (see Figure 2-6), acting as a current limiter is in series with the chopper output so that there is no
danger of overcurrent when the simulator is short circuited.

Figure 2-4. Waveforms of Chopper Output and Base signal

2.2 DESIGN AND TEST OF TYPE I SIMULATOR

The type I simulator is shown schematically in the block diagram of Figure 2-5, it serves to duplicate the I/V characteristics of a PV panel, but at a higher power rating. It is intended to be used in applications where a single commercial panel is available, and where it is required to simulate a large array of these panels. The panel used in the tests described here is an ARCO G100. It is rated at 5 W (peak power), open circuit voltage 20.8 volts and short
circuit current 435 mA. A transistor is connected in parallel (c-e) with the pilot panel, as shown in the circuit diagram of Figure 2-6. By controlling the base bias of the transistor, the panel current can be varied from nearly zero (limited by $I_{CEO}$), to nearly short circuit current (limited by emitter resistor and saturation voltage of the transistor). The voltage of the panel will vary accordingly. Thus the sample curve is obtained. The voltage of the pilot panel is used as a reference input for the voltage loop.

In addition to the voltage loop there is a current loop, each with a PI compensator. The load current is sensed by a Hall effect sensor and the current signal goes through a 'T' filter and operational amplifier $A1$ before it is sent to the PI compensator. The purpose of the filter is to obtain a relatively 'ripple free' current feedback signal.
Figure 2-6. Circuit Diagram of the Type I Simulator
This is important to the current loop. The operational amplifier A1 is used to adjust the short circuit current of the simulator. The short circuit current can be adjusted to as high as the power converter can tolerate by simply varying potentiometer R3. The PI compensator includes op amps, A2 and A3, transistor T, and some capacitors and resistors. Figure 2-7 shows a transfer function block diagram of the current loop, where:

\[
\begin{align*}
I_p & = \frac{(K_3 h_2)(T_3 R_b)(T_3 + 1)}{S(T_2 + 1)} \\
K_8 & = \frac{R_8}{R_1} \\
T_1 & = R_1 C_1/4 \\
T_2 & = R_4 C_2/4 \\
T_3 & = R_8 C_5 \\
T_8 & = R_1 C_7/4 \\
K_1 & = R_1/R_3 \\
K_3 & = R_8/R_4 \\
K_8 & = R_{12}/R_{11}
\end{align*}
\]
is the conversion ratio of the current sensor and \( \alpha \) is a hybrid parameter of the transistor T.

Figure 2-8 shows how the pilot panel is adjusted by the shunt transistor T. The voltage and current in Figure 2-8 are in per unit values. The current base and the voltage base are the short circuit current and the open circuit voltage respectively.

Figure 2-8. Load Line of the Transistor T

When the output voltage of A2 changes, the base current of T will change, and thus the operating point will move along the pilot panel characteristic curve, producing a reference input for the voltage control loop. Assuming a change in the load current, there will be a difference between the reference input and feedback current signals. The PI compensator then regulates the pilot panel current until the
reference input and feedback current are equal (reaching steady state). The following formulae are used to determine the current loop parameters:

\[ R_b = 12 \cdot h_{21} / I_{psc} \] (2-8)

\[ R_{12} / R_{11} = 10 / (I_{psc} \cdot R_{10}) \] (2-9)

\[ I_{ssc} = 10 \cdot R_1 / (R_{3a}) \] (2-10)

where \( I_{psc} \) is the short circuit current of the pilot panel, \( I_{ssc} \) is the short circuit current of the simulator.

Figure 2-9 is the transfer function block diagram of the voltage loop, where:

\[ T_6 = R_{16} C_6 \] (2-11)

\[ T_5 = R_{21} R_{14} C_6 / (R_{21} + R_{14}) = R_{21} C_6 \] (2-12)

\[ T_7 = R_{15} R_{20} C_{10} / (R_{15} + R_{20}) \] (2-13)

![Voltage Loop Transfer Function Block Diagram](image)

\[ K_5 = R_{16} / (R_{21} + R_{14}) \] (2-14)

\[ K_7 = R_{16} / (R_{15} + R_{20}) \] (2-15)

\[ K_c = (dc \ source \ voltage) / 10 \] (2-16)
\[ T_L = \frac{L}{R_L} \quad (2-17) \]
\[ T_{L1} = \frac{L}{(R_L + R_{18})} \quad (2-18) \]

\( T_c \) is the chopper period. \( R_L \) and \( L \) are the load resistance and inductance respectively (assuming R-L load). \( K_c \) is the chopper voltage gain parameter. The input to the voltage loop is the pilot panel voltage, which is compared with the feedback voltage from the simulator output, forming the error signal. The PI compensator regulates the output of A4 (\( V_c \)) according to the error signal. The chopper output voltage \( V_{ch} \) is related to this by the following form:
\[ V_{ch} = K_c \cdot V_c \quad (2-19) \]

By adjusting \( R_{15} \), the simulator open circuit voltage can be set:
\[ V_{soc} = 0.1 \cdot V_{poc} \left( R_{15} + R_20 \right) / \left( R_{14} + R_{21} \right) \beta \quad (2-20) \]

where \( V_{soc} \) is simulator open circuit voltage, \( V_{poc} \) is the pilot panel open circuit voltage and \( \beta \) is the conversion ratio of the voltage sensor. Within the whole voltage range the chopper should not saturate. To meet this condition, \( I_{ssc} \), \( V_{soc} \), \( R_{18} \) and the source voltage must be chosen properly. Figure 2-10 shows how the I/V curve is achieved at the simulator output terminals (assuming a resistive load for simplicity). In Figure 2-10, suppose the load characteristic changes from \( L_1 \) to \( L_2 \). The chopper output voltage will change from \( V_{sm1} \) to \( V_{sm2} \), the operating point will move from A to B. Thus the output follows the pilot panel. On the other hand, if the chopper voltage saturates before reaching \( V_{sm2} \), the operating point will move to C
instead of B. Consequently, substantial distortion occurs. To avoid this problem, Issc and Vsoc must be limited so that the entire simulator I/V curve (under the highest illumination level)

![Graph showing output characteristic with varying load](image)

Figure 2-10. Output Characteristic with Varying Load

is inside the triangle formed by the two axes and line $P_2$ (Figure 10, assuming $V_{sm_2}$ is the highest chopper output voltage). Figure 2-11 shows the results of a saturated chopper caused by mismatched parameters (Vsoc too high). During the test of the simulator with R-L load, an adjustable light source is used to obtain different light intensity conditions. The output current is adjusted by varying the load resistor. When the simulator is short
circuited, the short circuit current of the simulator is adjusted to 10 amperes. The open circuit voltage of the simulator is adjusted to 50 volts. This setting is chosen arbitrarily to test the steady state error of the system. As the short circuit current and open circuit voltage can be adjusted within a certain range, once the actual short circuit current (Isc) and open circuit voltage (Voc) are given, the short circuit current and the open circuit voltage of the simulator can be set to Isc and Voc respectively. The simulator output voltage and current are monitored by an oscilloscope (in x-y mode) and recorded by an x-y plotter. The I/V characteristics of the simulator and

Figure 2-11. Simulator Output with Mismatched Parameters
the pilot panel are recorded from the x-y plotter and are shown in figure 2-12.

![Figure 2-12. Experimental Output of Correctly Adjusted Simulator](image)

All values are per-unit, for easy comparison. The difference between the simulator I/V curves and the pilot panel I/V curves is within 1%. As there are differences between the pilot panel I/V curves and the array I/V curves (refer to Chapter 4 for details), the steady state error (compared with the array) is larger than 1%. It is assumed that the maximum difference between a pilot panel I/V curve and the corresponding array I/V curve is not more than 4%. Different
resistive load, R-L loads and motor loads have been connected to the simulator and no stability problems (oscillations) were observed.

2.3 STABILITY ANALYSIS WITH R-L LOADS

This section presents a stability analysis for the type I simulator with R-L loads. The results of this analysis provide guidance for the determination of circuit parameters to assure the stability of the whole system.

The transfer function block diagram of the whole system can be obtained by combining the current and voltage loop transfer function block diagrams (Fig. 2-7 and 2-9) as shown in Figure 2-13.

![Figure 2-13. Model of the Whole System](image)

In Figure 2-13,

\[ N_0 = aK_1K_5P_1P_3 \]  \hspace{1cm} (2-21)

\[ N_1 = N_0 (T_3T_6T_7T_8) \] \hspace{1cm} (2-22)

\[ N_2 = N_0 (T_3T_4 + T_7T_8 + T_3T_7 + T_3T_8 + T_4T_7 + T_4T_8) \] \hspace{1cm} (2-23)
\[ N_3 = N_0 \left[ T_3 T_4 (T_7 + T_8) + T_7 T_8 (T_3 + T_4) \right] \quad (2-24) \]

\[ N_8 = N_0 T_3 T_4 T_7 T_8 \quad (2-25) \]

\[ D_0 = C_0 F_0 \quad (2-26) \]

\[ D_1 = C_0 F_1 + C_1 F_0 \quad (2-27) \]

\[ D_2 = C_0 F_2 + C_1 F_1 + C_2 F_0 \quad (2-28) \]

\[ D_3 = C_0 F_3 + C_1 F_2 + C_2 F_1 + C_3 F_0 \quad (2-29) \]

\[ D_4 = C_0 F_4 + C_1 F_3 + C_2 F_2 + C_3 F_1 + C_4 F_0 \quad (2-30) \]

\[ D_5 = C_0 F_5 + C_1 F_4 + C_2 F_3 + C_3 F_2 + C_4 F_1 \quad (2-31) \]

\[ D_6 = C_1 F_5 + C_2 F_4 + C_3 F_3 + C_4 F_2 \quad (2-32) \]

\[ D_7 = C_2 F_5 + C_3 F_4 + C_4 F_3 \quad (2-33) \]

\[ D_8 = C_3 F_5 + C_4 F_4 \quad (2-34) \]

\[ D_9 = C_4 F_5 \quad (2-35) \]

\[ C_0 = P_3 P_4 \quad (2-36) \]

\[ C_1 = P_3 P_4 T_4 + P_3 P_4 T_L + 1 \quad (2-37) \]

\[ C_2 = P_3 P_4 T_4 T_L + T_C + T_L + T_7 \quad (2-38) \]

\[ C_3 = T_C T_L + T_7 \quad (2-39) \]

\[ C_4 = T_C T_L T_7 \quad (2-40) \]

\[ P_1 = K_3 R_{21} T_3 Rb \quad (2-41) \]

\[ P_2 = 10 / l_p \text{sc} \quad (2-42) \]

\[ P_3 = K_c / T_4 \cdot (R_L + R_{18}) \quad (2-43) \]

\[ P_4 = K_7 R_L \beta \quad (2-44) \]

\[ F_0 = b_0 \quad (2-45) \]

\[ F_1 = a_1 b_0 + b_1 \quad (2-46) \]

\[ F_2 = a_2 b_0 + a_1 b_1 + b_2 \quad (2-47) \]

\[ F_3 = a_2 b_1 + a_1 b_2 + b_3 \quad (2-48) \]

\[ F_4 = a_2 b_2 + a_1 b_3 \quad (2-49) \]

\[ F_5 = a_2 b_3 \quad (2-50) \]
From Figure 2-11 we can write the differential equation for the linear part of the simulator as below:

\[
\sum_{i} D_{i} \tilde{v}_{p} + D_{0} I_{0} = N_{0} \tilde{v}_{0} + \sum_{i} N_{i} \tilde{v}_{i}
\]  

If a certain load is given, say \( R_{0} \) and \( L_{0} \), this load will correspond to one operating point on the characteristic I/V curve of the pilot panel. Let us denote this operating point as \( I_{0} \) and \( V_{0} \) and define new variables:

\[
\tilde{I}_{p} = i_{p} - I_{0}
\]

\[
\tilde{V}_{p} = v_{p} - V_{0}
\]

Substitution of eqs. (2-58, 2-59) into eq. (2-57) leads to:

\[
D_{9} \tilde{I}_{p} + D_{8} \tilde{I}_{p} + \ldots + D_{0} I_{0} = N_{0} \tilde{V}_{p} + \ldots + N_{0} \tilde{V}_{p} + N_{0} V_{0}
\]  

Since \((I_{0}, V_{0})\) is an operating point on the curve, we have:

\[
D_{0} I_{0} = N_{0} V_{0}
\]  

Thus, eq. (2-60) becomes:

\[
D_{9} \tilde{I}_{p} + \ldots + D_{0} \tilde{I}_{p} = N_{0} \tilde{V}_{p} + \ldots + N_{0} \tilde{V}_{p}
\]  

It should be noted that all the coefficients \( D_{0}, \ldots, D_{9}, \ldots, N_{0}, \ldots, N_{4} \) are functions of load resistance and inductance. For a given load \((R_{0}, L_{0})\), the system model can be represented as
Figure 2-14. Modified Model of the Whole System

Note that in Figure 2-14, the origin of the non-linear element has been moved to \((I_0, V_0)\) and the \(i_p\) feedback is negative. The voltage and current variables \(\tilde{v}_p\) and \(\tilde{i}_p\) represent deviations from the equilibrium values \(V_0\) and \(I_0\).

Let the linear open loop frequency response be:

\[
G(j\omega) = \frac{A + jB}{C + jD}
\]

where,

\[
A = N_4 \omega^4 - N_2 \omega^2 + N_0
\]

\[
B = N_1 \omega - N_3 \omega^3
\]

\[
C = D_8 \omega^8 - D_6 \omega^6 + D_4 \omega^4 - D_2 \omega^2 + D_0
\]

\[
D = D_5 \omega^5 - D_1 \omega + D_5 \omega^5 - D_3 \omega^3 + D_1 \omega
\] (2-63) (2-64) (2-65) (2-66) (2-67)
\[
\text{Re}[G(j\omega)] = \frac{AC+BD}{C^2+D^2} \quad (2-68)
\]

\[
\text{Im}[G(j\omega)] = \frac{BC-AD}{C^2+D^2} \quad (2-69)
\]

Assuming the illumination and temperature level do not change suddenly, which is the case in practice, stability of the system represented by the modified model of Figure 2-14 can be considered using the method of Popov for a single non-linear element. According to Popov's criterion, the system is Asymptotically Stable In the Large if there exists a scalar \( q \) such that

\[
\frac{1}{k} + \text{Re}[(1+j\omega q)G(j\omega)] > 0 \quad (2-70)
\]

for all \( \omega \).

In our case,

\[
k = \frac{V_0}{I_0 - I_{psc}}, \quad (2-71)
\]

which is the slope of the constraint line, as shown in Figure 2-15. For the system to be ASIL with a particular load, the PV array characteristic must be confined to the
sector bounded by the constraint line.

![Diagram](image)

Figure 2-15. The Equivalent Non-linear Element

The worst situation is when the simulator is short circuited, that is, \( \text{I}_0 = \text{I}_{pc}, \text{V}_0 = 0 \). In this situation, the constraint line has the highest slope \( k \).

Based on Eqs. (2-20 to 2-71), a computer program was written to assess the stability of the system under different load conditions. An summary of the program is given in appendix A. The complete program is given in Appendix B. The program calculates the eigenvalues of the linear transfer function, and data for Nyquist plots as well as for the modified Nyquist plots used to test the stability criterion graphically. Different values of \( R_L \) and \( L \) were tested on the computer. By examining the open loop eigenvalues and the modified Nyquist plot, we can establish stability for a certain load condition by Popov's criterion. After a series of tests on \( R \) and \( R-L \) load (the values of \( R \) and \( L \) are varied), it was found that:
(a). typical Nyquist plots resemble the one shown in Figure 2-16. Since the Nyquist plots were found to be convex, the modified plots are not needed.

![Nyquist Plot](image)

**Figure 2-16. Typical Nyquist Plot of the Simulator**

The critical point $P_c$ moves further away from the origin as $R$ decreases. According to Popov's criterion, the stable value of $k$ decreases accordingly. When the critical point gets too far away from the origin the system becomes unstable. In practice, however, by adjusting the system parameters properly, the critical point can be moved arbitrarily close to the origin. Thus the system is stable for all R-L load conditions.

(b). For a fixed resistance and varying inductance, there is a value of inductance that gives the smallest stable sector. This can be seen from Figure 2-17. The critical value of $k$
decreases as load resistance decreases.

![Diagram of critical value of k with respect to RL; legend showing RL = 100 OHMS, RL = 10 OHMS, RL = 1 OHMS, RL = 0.1 OHMS.]

Figure 2-17. Stable Value of k with Respect to RL, L

The highest slope of the constraint line must not exceed the lowest value of k in Figure 2-17, which is about 50.

(c). The filter time constants T₁, T₅, and T₇ play an important role in stability of the whole system. T₅ and T₇ should be at least a few times smaller than T₁ in order to keep the system stable over the full voltage or current range. Furthermore, in order to obtain quick dynamic response, T₁, T₅, and T₇ should be reasonably small (T₁ is 55 ms in the type I simulator). Unfortunately, their lower bounds are limited by the system noise or chopper frequency, whichever is lower. The chopper output is modelled by an ideal voltage source with a value equal to the average output value. Since it is in fact composed of a train of
pulses, the model is valid only when the output filter has a corner frequency substantially lower than the chopper or noise frequency so that the output voltage ripple is small. This means that $T_5$ and $T_7$ must be substantially larger than the chopper period, $T_C$, which is 40 $\mu$s.

A step change of load from no-load to maximum power point and back to no-load was applied to the system. The response of the type I simulator (R-L load) is shown in Figure 2-18.

![Diagram](image)

Figure 2-18. Type I Simulator Response to Step Change

The fall and rise time is 50 ms and 38 ms respectively. The speed of response is fast enough to meet the requirement of 150 ms.
2.4 APPLICATION TO A PUMPING SYSTEM

The type I simulator has been connected to an experimental solar pumping system. An important requirement of this pumping system is to keep the system operating at the maximum power point of the photovoltaic array so that maximum power is extracted from the given array with changing illumination level and temperature. A schematic diagram of the pumping system is shown in Figure 2-19.

![Schematic Diagram of the Pumping System](image)

Figure 2-19. Schematic Diagram of the Pumping System

The dc motor drives a pump which can be considered as a constant torque load. As illumination level and temperature vary during the day, so does the array I/V characteristic curve. That is, the motor has a constant torque load and a varying power source. The purpose of the regulator in the pumping system is to match the motor to the PV array such
that the array operates at its peak power point regardless of the deviation of the illumination level and temperature, and the motor operates at constant current and varying voltage or speed depending on the environmental condition.

To accommodate this kind of load, the voltage loop described in Section 2.2 has to be modified. As far as the simulator is concerned, the pumping system can be considered as the equivalent circuit shown in Figure 2-20.

![Figure 2-20. Equivalent Circuit of the Pumping System](image)

In Figure 2-20, $E_m$ is a variable voltage source representing the emf of the dc motor. During the operation, $E_m$ is controlled by the regulator in the pumping system.

The transfer function block diagram of the modified voltage loop is shown in Figure 2-21, where,

\[
T = C \cdot R_1 \\
T_4 = C_8 \cdot R_{18} \\
T_5 = R_{21} \cdot C_8
\]
Figure 2-21. Model of the Modified Voltage Loop

\[ K = \frac{R}{R + R_0} \]
\[ K_e = \frac{R_0}{R + R_0} \]
\[ K_5 = \frac{10}{V_{poc}} \]
\[ K_7 = \frac{10}{V_{soc}} \]

Other parameters remain the same as those in Section 2.2.

The transfer function of the modified voltage loop can be written as below:

\[ \frac{V_s(s)}{V_p(s)} = \frac{B_0 + B_1s}{s^3 + A_2s^2 + A_1s + A_0} \]  \hspace{1cm} (2-72)

\[ \frac{V_s(s)}{E_m(s)} = \frac{Q_1s}{s^2 + M_1s + M_0} \]  \hspace{1cm} (2-73)

Where,
\[ B_0 = K \cdot K_c \cdot K_5 / (T_4 T_5 T) \]
\[ B_1 = B_0 T_4 \]
\[ A_2 = (T_4 T_5 + T_4 T + T_4 T_5 K K_7 K_c) / (T \cdot T_4 T_5) \]
\[ A_1 = (T_4 + T_4 K \cdot K_7 K_c + T_5 K \cdot K_7 K_c) / T \cdot T_4 T_5 \]
\[ A_0 = K \cdot K_7 K_c / T \cdot T_4 T_5 \]
\[ Q_1 = K_e / T \]
\[ M_1 = (1 + K \cdot K_c \cdot K_7) / T \]
\[ M_0 = (K \cdot K_c \cdot K_7) / T \cdot T_4 \]

The step and ramp response of the voltage loop have been simulated on the computer (using FORSIM) with the parameters listed below:
\[ T = 0.02 \text{ sec.} \]
\[ T_4 = 5.6 \times 10^{-3} \text{ sec.} \]
\[ T_5 = 10^{-3} \text{ sec.} \]
\[ K = 0.054 \]
\[ K_e = 0.946 \]
\[ K_5 = 0.5 \]
\[ K_7 = 0.5 \]
\[ K_c = 11.5 \]

The unit step response is shown in Figure 2-22, from which it can be seen that the steady state error is zero. A ramp response of the voltage loop is given in Figure 2-23. There is a steady state error which can be determined from the transfer function block diagram of Figure 2-21.
Figure 2-22. Step Response of the Voltage Loop

\[
E(s) = \frac{s(Ts+1)}{V_p(s)(Ts+1)+K_T(Ts+1)}
\]  \hspace{1cm} (2-74)

where,

\[
K_T = \frac{KK_T K_c}{T_s}
\]  \hspace{1cm} (2-75)
Figure 2-23. Ramp response of the Voltage Loop

For a ramp input of \( v_p(t) = K_a t \),

\[ V_p(s) = \frac{K_a}{s^2} \]

The steady state error:

\[ e(\infty) = \lim_{s \to 0} s \cdot \frac{s(T_s + 1)}{s(T_s + 1) + K_T(T_s + 1)} \cdot \frac{K_a}{s^2} = \frac{K_a}{K_T} \]  \hspace{1cm} (2-76)

From eqs. (2-75) & (2-76) it can be seen that the steady state error with ramp input is proportional to \( T_s \). Thus, \( T_s \) should be reasonably small. In the final circuit, \( T_s \) is .0056 second. When \( K_a = 1 \) volt/sec.

\[ e(\infty) = 1/55.4 \text{ (V)} \]
This error is small enough to meet our requirements.

The equivalent load line of the pumping system is shown in Figure 2-24.

![Figure 2-24. Equivalent Load Line of the Pumping System](image)

From eq.(2-73) it can be seen that the step response of the simulator output voltage $v_s$ with respect to the emf of the motor $e_m$ will settle down to zero. That is, when there is a step change in $e_m$, the output of the simulator will settle down to the value determined by the reference input $v_p$. The current loop remains the same as in section 2.2.

The simulator with the pumping system as the load was tested first with a simulated load set up as illustrated in
During the test with the simulated load, the voltage source is adjusted so that the load voltage varies from zero to $V_{soc}$. The voltage and the current of the simulator are monitored by an oscilloscope and recorded by an x-y plotter. It has been observed that the simulator's output voltage and current follow the sample closely while the voltage source is being adjusted. Since the pilot panel is not changed, the I/V curves recorded by the plotter are the same as those in Figure 2-12.
3. TYPE II SIMULATOR

As mentioned in the INTRODUCTION, it is desirable in some experiments of PV array powered system to have repeatable array curves. The type II simulator provides fixed PV array curves under different illumination levels and temperatures. The basic requirements of the type II simulator are listed below:

1. The steady state error must be smaller than 5%. Since the operating points of most loads move along the array curve during operation, for instance, when tracking the maximum power point in the pumping system, the PV array simulator should have output I/V characteristics as close to those of the real array as possible.

2. The transient state due to a step change of load from open circuit to maximum power point must not exceed 150 ms. Like any other dynamic system, the simulator has a transient state when a load disturbance or any other system disturbance occurs. For example, in a solar pumping system, there is a regulator that keeps adjusting the voltage and current of the PV array. If the PV simulator has slow dynamic response, the experiment with this PV array simulator may lead to incorrect results.

3. The short circuit and open circuit voltage must be adjustable so that the simulator can represent arrays of different Isc and Voc ratings.
The next section describes how these requirements can be met.

3.1 DESIGN CONSIDERATIONS

3.1.1 SAMPLE CURVE GENERATION

Among the previously-reported PV array simulators, reference [6] achieves quite precise sample curves. However, the formula calculation method used in reference [6] causes a long execution time and sampling period. As a result, the dynamic response is not very fast. A new method, which combines formula calculation and data storage, is used in the type II simulator. It is a compromise between execution time and memory size.

Suppose the I/V characteristics of the PV array to be simulated are given (usually PV array characteristics are available from manufacturers). The I/V characteristics can be stored in the memory of a microprocessor-based system. Once a certain illumination level and temperature are given, then for every value of output current there is a corresponding value of voltage, which is obtained from the look-up table stored in the memory. As the number of I/V curves increases, the memory size increases linearly. To save some memory space, a formula calculation method is used for the low current half of the I/V curve. This is based on the fact that when the array current is lower than half the short circuit current, the I/V curve is basically a straight
line as shown in Figure 3-1.

![Figure 3-1. One of the I/V curves to Be Simulated](image)

Therefore, a simple straight line formula can represent the lower half of the array I/V curve with sufficient accuracy. In this way, half of the memory size can be saved in comparison to the full memory storage method. Also, relatively short execution time (compared with the full formula calculation method) is achieved, which leads to a higher sampling rate and faster dynamic response.

In Figure 3-1, the I/V curve is based on an ASI 16-2300 panel made by ARCO SOLAR INC.. The I/V curve given by the specification is measured and then plotted using the
computing facility available. The I/V curve in Figure 3-1 is used as a prototype to assess the steady state error. The current and voltage are not represented in actual values, but in scaled variables that can be represented by one byte in the microprocessor.

3.1.2 CONTROL SCHEME OF THE SIMULATOR

As the sample curve generation is implemented in a microprocessor system, it is natural to use a digital control scheme. Special care has been taken to design the voltage loop in order to achieve good dynamic response of the whole system. The idea is to have a fast response voltage loop, fast enough to follow the varying voltage input caused by the relatively slower change of load current. In other words, the speed of response of the voltage loop determines the allowed maximum changing rate of load current. In each cycle, load current is sampled and a corresponding reference voltage is generated by the control program. A current loop is not needed in the type II simulator. Proportional and integrational (PI) control and proportional control (P) schemes have been designed and implemented. By selecting the parameters Q0 and Q1, the PI controller has the same form as a deadbeat controller. However, due to some practical problems that will be explained in section 3.2.2, a deadbeat control is not desirable. According to transfer function analysis, a PI controller gives zero steady state error and good dynamic
response, provided the assumption of linearity is true. Unfortunately, the assumption is not true in this application. One problem encountered in the design of the voltage loop is whether the controller output will exceed the limited range of the system. If it does, the expected result based on transfer function analysis will be wrong. To find out whether the controller saturates, a computer simulation program can be used. Alternatively, the saturation problem can be ignored in the early stage of design. For instance, an oscilloscope can be used to monitor the control output. Any saturation can be easily detected with the oscilloscope.

The sampling frequency is chosen as the highest possible value, which is about 2.5 kHz. This corresponds the execution time of one cycle of the control program.

3.1.3 POWER CONVERTER

As in the type I simulator, a one quadrant transistor chopper is used as the power converter. A current limiter is inserted in the chopper output for the same reason mentioned in section 2.1.3. There are two ways to obtain a pulse width modulated signal for the chopper. One is to use the microprocessor software, the other is to use extra hardware. The first method was used in the preliminary design and the second was adopted in the final design of the simulator. The advantages of the second method are that the execution time of the control program and thus the sampling period can be
shortened. Besides, by using a PWM IC chip (NE5561N), the PWM generating circuit is very simple and the operating frequency can be easily adjusted.

3.2 DESIGN AND TEST OF THE TYPE II SIMULATOR

This section describes the design and test of the type II simulator in full detail. The I/V curves to be simulated are from the specification of an ASI 16-2300 panel made by ARCO SOLAR INC.. One of the I/V curves given by the manufacturer is reproduced and plotted in Figure 3-1. The whole control unit, including sample curve generation and control algorithm, is implemented on a 6809 microprocessor development system. A simplified diagram showing the architecture of the microprocessor development system is given in figure 3-2. Only the MPU, VIA0, VIA1 and some RAM are used directly by the simulator. That is, once the design is complete and ready to put in production, other elements in Figure 3-2 (which are necessary during design and test) can be dispensed with. Other elements required include A/D, D/A converters, a PWM generator and a chopper with its drive circuit.

3.2.1 HARDWARE OF THE TYPE II SIMULATOR

The hardware configuration of the type II simulator is given in Figure 3-3. VIA1 is a versatile interface adaptor which contains two programmable INPUT/OUTPUT ports. Each port can be either an input port or an output port, depending on
the contents of the data direction register DDRA or DDRB. When a '1' is put in bit0 of DDRA, bit0 of port A will become an output bit; when a '0' is put in bit0 of DDRA, bit0 of port A will become an input bit. Other bits work the same way. Making use of this flexible property, one can use one port to take in the feedback signal (input) as well as to send out the control signal (output) — acting like two ports. In the type II simulator, port A of VIA1 is used to input the current feedback signal and to output the control signal Vc, as shown in Figure 3-3. Port A of VIA0 (PA0) is used to select curves corresponding to different illumination levels and temperatures, to input the start signal and to provide enable signals for the A/D and D/A converters. The output voltage signal is picked up by a voltage sensor and is then sent to an A/D converter which is connected to port B of VIA1, as shown in Figure 3-3. Figure 3-4 shows the signal assignment to the INPUT/OUTPUT ports. Bit0 --- bit3 of PA0 are used to select different I/V curves. Thus, a maximum number of 16 curves can be selected. The A/D converter used is an ANALOG DEVICES AD750, with 8-bit data output and 0 --- 10 volts analogue input. When the analogue input is negative, the digital output is 0; when analogue input is higher than 10 volts, the digital output will be locked at 255. Therefore, if the voltage or current feedback signal is beyond the normal range, the data obtained from the
Figure 3-2. Architecture of 6809 Microprocessor Development System
Figure 3-3. Hardware Configuration of the Type II Simulator
A/D converter is not the correct value. A 25 to 40 µs wait time is required after an enable signal is applied to the
A/D converter. The D/A converter is an AD558 IC chip. It has an 8-bit data input and two levels of data output. One is 0 to 2.56V, the other is 0 to 10 volts. The latter is used in the simulator because the PWM chip requires an analogue signal of 2 to 5 volts. As mentioned in section 3.1.3, the pulse width modulated signal can be generated directly from the microprocessor, using software. This was attempted in the preliminary design stage. The frequency of the PWM signal was about 4 kHz. The test of the scheme shows a good steady state accuracy for most of the voltage range. However, the dynamic response was slow. The hardware implementation of the PWM generator is shown in the circuit diagram of Figure 3-5. A 2 to 5 volt signal in the input of the IC chip NE5561N will produce a PWM signal with 5% to 98% duty ratio. When testing the PWM generator, one can remove the resistor \( R_3 \) first and adjust \( R_6 \) so that when \( V_c \) is 10 volts, \( V_{pwm} \) is 3 volts. Then \( R_3 \) is connected and adjusted until \( V_{pwm} \) reaches 5 volts (\( V_c \) remains 10 volts). It has been observed that the relationship between chopper output voltage and the control input is not strictly linear.

3.2.2 TRANSFER FUNCTION ANALYSIS FOR THE PUMPING SYSTEM LOAD

For the pumping system load, the transfer function block diagram of the whole system is shown in Figure 3-6. where,

\[ T \approx 400 \mu s \] (sampling period)
Figure 3-5. Circuit Diagram of the PWM Generator
Inside the dashed frame of Figure 3-6 is the digital part and outside is the analogue part. The circuit diagram of the analogue part is shown in Figure 3-7. Since there is a large capacitor in the pumping system load (it is quite common in practice that a large capacitor is connected in parallel with the PV array), the voltage waveform will be flat and a voltage filter is not necessary. A current filter is used in order to obtain a smooth current feedback signal. The open circuit voltage and short circuit current of the simulator can be adjusted by varying potentiometers $R_2$ and $R_4$ respectively. The Laplace transfer function of $V_f$ with respect to $V_c$ is given by:

$$V_f(s)/V_c(s)=Kck_1K_{fv}/(T_1s+1) \quad (3-1)$$

The transfer function of $V_f$ with respect to $E_m$ is given by:

$$V_f(s)/E_m(s) = K_2K_{fv}/(T_1s+1) \quad (3-2)$$

Converting eqs(3-1,3-2) into z transfer functions [13] and using step response equivalence yields:
Figure 3-6. Transfer Function Block Diagram for Pumping System Load
Figure 3-7. Circuit Diagram of Analogue Part

\[ G_{vc}(z) = (1-z^{-1})Z \left[ \frac{G_{vc}(s)}{s} \right] \]
\[ = \frac{V_f(z)}{V_c(z)} \]
\[ = z^{-1} / (a_0 + a_1 z^{-1}) \]  \hspace{1cm} (3-3)

\[ G_{ve}(z) = \frac{V_f(z)}{E_m(z)} = z^{-1} / (b_0 + b_1 z^{-1}) \]  \hspace{1cm} (3-4)

where,
\[ a_0 = \frac{1}{K_a} (1-e^{-T/T_1}) \]
\[ a_1 = -\frac{e^{-T/T_1}}{K_a} (1-e^{-T/T_1}) \]
\[ b_0 = \frac{1}{K_b} (1-e^{-T/T_1}) \]
\[ b_1 = -\frac{e^{-T/T_1}}{K_b} (1-e^{-T/T_1}) \]
\[ K_a = K_c K_{f_v} \]
\[ K_b = K_2 K_{f_v} \]

From Figure 3-6 we can see that the plant is of first order, with a reference input \( V_p \) and a disturbance \( E_m \). A PI
controller is designed for the voltage loop. The z transfer function of the controller is shown below:

\[ \frac{V_c(z)}{E(z)} = \frac{Q_0 + Q_1 z^{-1}}{1 - z^{-1}} \]  \hspace{1cm} (3-5)

With PI control, the z transfer function of \( V_f \) with respect to \( V_p \) becomes:

\[ \frac{V_f(z)}{V_p(z)} = \frac{Q_0 z^{-1} + Q_1 z^{-2}}{a_0 + (a_1 + Q_0 - a_0)z^{-1} + (Q_1 - a_1)z^{-2}} \]  \hspace{1cm} (3-6)

The z transfer function of \( V_f \) with respect to \( E_m \) is given by:

\[ \frac{V_f(z)}{E_m(z)} = \frac{z^{-1} (1 - z^{-1})}{b_0 + (b_1 - b_0 + Q_0)z^{-1} + (Q_1 - b_1)z^{-2}} \]  \hspace{1cm} (3-7)

From eq(3-6) it can be seen that, if \( Q_0 = a_0 \) and \( Q_1 = a_1 \), the step response of \( V_p \) will have a deadbeat behaviour. However, as the deadbeat control depends on the cancellation of poles and zeros, it is sensitive to the deviation of the system parameters. Since the circuit elements are not ideal, and especially that the chopper is not quite linear, a deadbeat control scheme is not used. Instead, \( Q_0 \) and \( Q_1 \) are selected so that the system poles are at \( z = 0.2 \pm j0.3 \). \( Q_0 \) and \( Q_1 \) can be calculated from the following formulae:

\[ Q_0 = -0.4 \cdot a_0 + a_0 - a_1 \]
\[ Q_1 = 0.13 \cdot a_0 + a_1 \]

During operation, the reference input \( V_p \) is varying due to the change of load or the change of sample curve. Thus, fast dynamic response of the voltage loop is essential to the overall performance of the simulator.

The simulator I/V curves are recorded by an x-y plotter and plotted together with the sample curve, as shown in
Figure 3-8. The scales in Figure 3-8 (also in Figure 3-9) represent the current and voltage values stored in the microprocessor. These values correspond to the actual current and voltage values of the simulator. As an alternative, a proportional controller was also designed and implemented. The advantage of the P control is that the execution time of one cycle of the control program is substantially shorter than that using PI control. The simulator output with P control is plotted together with the sample curve as shown in Figure 3-9. All the values of current and voltage are corresponding values represented by the microprocessor.

3.2.3 SOFTWARE OF THE SYSTEM

The control program is written in assembly language. The basic tasks of the control program are listed below:
1. Select one I/V curve.
2. Sample simulator output voltage and current.
3. Generate reference voltage according to selected I/V curve.
4. Control algorithm.
5. Output the control signal.

The flowcharts of the control program are given in Figure 3-10a and 3-10b. One can see from Figure 3-10a that port A of VIA1 is defined twice, first as an input port to read the current signal and then as an output port to send out the
control signal to the D/A converter.

Figure 3-8. Type II Simulator I/V Curves (PI control)
(scaled in terms of microprocessor bit size)
Figure 3-9. Type II Simulator Output Using P Control (scaled in terms of microprocessor bit size)

The enable signal for the A/D converter is issued 13 instructions earlier than when the microprocessor actually
samples the current and voltage signals from A/D converters. Thus a 40 μs wait time is ensured. From Figure 3-3 one can see that a D/A and an A/D converter are connected together to port A of VIA1. Care must be taken to make sure that the A/D converter and the D/A converter are not enabled at the same time. All additions and subtractions in the control algorithm are carried out with two-byte representation. The dynamic range of the control algorithm is large enough to avoid overflow. However, the control output is represented by only one byte. Therefore, in both control algorithms, $V_c$ is set to zero when the calculated value is negative. When the calculated value is larger than 255, $V_c$ is set to 255. This saturation nature of the controller must be taken into account when analyzing the performance of the simulator.

The full voltage and current ranges are quantized into 256 steps, with one step representing 0.39% of $V_{soc}$ and $I_{ssc}$. This is sufficient for most applications.

A step change of load from open circuit to maximum power point and back to open circuit has been applied to the type II simulator, the system response (simulated pumping system load) is given in Figure 3-11.
Figure 3-10a. Flowchart of Control Program
Figure 3-10b. Flowchart of Subroutines
The speed of response meets our requirement (approximately 120 ms fall time and 80 ms rise time respectively).

Figure 3-11. Step Response of Type II Simulator
4. DISCUSSION

Among the previously-reported PV array simulators, those in references [8,18] can be categorized as type I simulators because the output characteristics are affected by the natural environment. The simulators reported in references [6,7,9] can be categorized as type II simulators since their output characteristics are not affected by the natural environment. The influence of light intensity and temperature is reproduced by manual adjustment.

Actual solar panels are not uniform (even if they are of the same type). Due to the dispersion of panel parameters, mismatch loss exists when many panels are connected to form a large array. The amplitude of the mismatch loss increases with the degree of dispersion. For instance, when two panels with slightly different open circuit voltages are connected in parallel, some current will flow from the panel with higher open circuit voltage to the one with lower open circuit voltage so that the total output power is smaller than the sum of the two separate panel output powers. An example given in reference [20] shows that for the parallel array being studied, the total array output power is 2.25% lower than the sum of the separate cell powers.

Because of the mismatch problem, the I/V curves of the array do not have the same shape as the pilot panel. This is a limitation in assessing the steady state error of the type I simulator introduced in this thesis (this limitation
exists in references [8,18] too).

In references [7,9], the simulator output characteristics are not compared with the real array I/V curves so that the actual steady state error is difficult to assess. The type II simulator described in this thesis uses the object curve (the actual I/V curve to be simulated) as the criterion to assess the steady state error. This provides accurate information about the steady state error of the simulator. The object curves can be the characteristics of a complete array. The type II simulator described here can thus easily simulate a complete array, which is not possible with the type I simulators.

When an array is partially shaded, the output characteristic will change accordingly. As the shading is arbitrary, the simulation of this effect will be complex and is not considered in this thesis.
5. CONCLUSION

Two different types of PV array simulator have been designed and tested. The type I simulator is suitable where a field test of a particular panel type is required. The design of a type I simulator involves stability analysis and partial simulation of dynamic behaviour, which provide guidance in choosing system parameters to assure stability and good dynamic behaviour. The type II simulator is suitable for experiments demanding fixed irradiation and temperature levels for a period of time. A new simulation method, combining formula calculation and data storage is used in the simulator, which leads to a relatively short sampling period and small memory size. The experimental results of these two simulators meet the requirements listed at the beginning of Chapter 2 and Chapter 3.

The simulators designed in this thesis provide convenient replacements for PV arrays used in experiments studying PV array-powered systems. They were originally designed for the use in an experimental solar pumping system which is under study at the Department of Electrical Engineering at U.B.C.. Further work to develop commercial versions of such simulators is worthwhile.
REFERENCES


APPENDIX A: ALGORITHM FOR STABILITY STUDY

Algorithm for stability study program:

1. Set flags: U=FALSE, V=FALSE, WW=POSITIVE
2. Input data (including load data $R_L$ and $L$).
3. Print out load data.
4. Calculate coefficients of denominator $D_0$--$D_9$. Formulae are given in Chapter 2 of this thesis.
5. Calculate coefficients of numerator $N_0$--$N_4$. Formulae are given in Chapter 2.
6. Calculate the eigenvalues of the open loop transfer function.
7. Print out eigenvalues.
8. $\omega=0$
9. If $\omega > 1500$, go to 22.
10. $\text{Re}[G(j\omega)] = \frac{AC+BD}{C^2+D^2}$

$\text{Im}[G(j\omega)] = \frac{BC-AD}{C^2+D^2}$

11. Print out $\text{Re}[G(j\omega)], \text{Im}[G(j\omega)]$ and $\omega \text{Im}[G(j\omega)]$.
12. If WW=0, go to 16
13. If $\text{Re}[G(j\omega)] \leq 0$, set V=TRUE.
14. If $\text{Im}[G(j\omega)] \geq 0$, set U=TRUE.
15. If V.AND. U=TRUE, go to 19.
16. If $\omega > 10$, go to 18.
17. $\omega=\omega+0.1$, go to 9.
18. \( \omega = \omega + 5 \), go to 9.

Comment: print out the critical slope in per-unit value:

19. \( K = \frac{1}{\text{Re}[G(j\omega)]]} \).

20. \( K = 0.43 \cdot K/20.8. \), print \( K \).

21. \( \text{ww} = 0 \), goto 16.

22. stop.
APPENDIX B: PROGRAM LISTING FOR STABILITY STUDY

Listing of THESIS at 22:10:49 on MAY 30, 1985 for CCid=LIU. Page 1

1 C
2 C A PROGRAM TO STUDY THE STABILITY OF TYPE I PV ARRAY SIMULATOR:
3 C
4 C
5 C LOAD DATA AND CORRESPONDING EIGENVALUES ARE OUTPUT TO LOGIC
6 C UNIT 6. NYQUIST PLOT DATA IS OUTPUT TO LOGIC UNIT 7.
7 C
8 C SYSTEM PARAMETERS (INCLUDING LOAD PARAMETERS) ARE INPUT FROM
9 C LOGIC UNIT 5.
10 C
11 C REAL N,K1A,K3,K5,K7,K8,KC,L
12 C LOGICAL V,U
13 C V=(1.LT.O)
14 C U=(1.LT.O)
15 C WW=10.
16 C DIMENSION D(10),N(5)
17 C CALL FREAD(5, '17RM : ' .
18 C &T1,T2,T3,T4,T5,T7,T8,TC,L,K1A,K3,K5,K7,KC,H21.,
19 C &RL,RO)
20 C WRITE(6.8)T1,T2,T3,T4,T5,T7,T8,TC,L,K1A,K3,
21 C WRITE(6.11)K5,K7,KC
22 C WRITE(6.7)H21,RL,RO
23 C
24 C
25 C FORMAT(/, 'H21= ' .F8.3, ' RL= ' .F15.4, ' R0= ' ,F8.3)
26 C
27 C FORMAT(//, 'K5= ' .F8.4, 'KC= ' .F8.4)
28 C
29 C FORMAT(/.'T1=' .F8.4, 'T2=' .F10.6, 'T3=' .F8.4, 'T4=',F10.6, 'T5=',F10.5,
31 C
32 C TL=L/RL
33 C TL1=L/(R0+RL)
34 C WRITE(6,90)TL,TL1
35 C
36 C
37 C
38 C FORMAT(//, 'P1= ' .15X, 'P2=', 15X, 'P3=', 15X, 'P4=',//.4F15.10)
39 C
40 C
41 C
42 C
43 C
44 C
45 C
46 C
CALCULATE NUMERATOR:

\[ D(4) = F_0* C_3 + F_1* C_2 + F_2* C_0 \]

\[ D(5) = F_0* C_4 + F_1* C_2 + F_2* C_0 + F_3* C_1 + F_4* C_0 \]

\[ D(6) = F_1* C_4 + F_2* C_3 + F_3* C_2 + F_4* C_1 + F_5* C_0 \]

\[ D(7) = F_2* C_4 + F_3* C_3 + F_4* C_2 + F_5* C_1 \]

\[ D(8) = F_3* C_4 + F_4* C_3 + F_5* C_2 \]

\[ D(9) = F_4* C_4 + F_5* C_3 \]

\[ D(10) = F_5* C_4 \]

CALCULATE NUMERATOR:

\[ H = K_5* P_1* P_3 \]

\[ N(1) = H* K_1 A \]

\[ N(2) = H* K_1 A* (T_3* T_4 + T_7* T_8) \]

\[ N(3) = H* K_1 A* (T_3* T_4 + T_7* T_8 + (T_3* T_4) * (T_7* T_8)) \]

\[ N(4) = H* K_1 A* (T_3* T_4 + T_7* T_8 + T_3* T_4) \]

\[ N(5) = H* K_1 A* 4* T_7* T_8 \]

PRINT OUT DENOMINATOR:

\[ \text{WRITE}(6,20) \]

\[ \text{CALCULATE DENOMINATOR:} \]

\[ \text{WRITE}(6,30) \]

\[ \text{CALCULATE NL:} \]

\[ \text{IF(WW LT. 0.0) GOTO 33, 33.34} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

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\[ \text{WRITE}(7,66)XR, XI \]

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\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

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\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

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\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

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\[ \text{IF(WW LT. 0.0) GOTO 32} \]

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\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

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\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]

\[ \text{IF(WW LT. 0.0) GOTO 32} \]

\[ \text{IF(WW LT. 0.0) V=(1.GT.0) AND(U LT. 0.0)} \]

\[ \text{WRITE}(7,66)XR, XI \]
34  W=W+500.
35  GOTO 55
36  FORMAT(2X,F15.10,2X,F15.10)
37  RL=1.E-6
38  I=12
39  WRITE(6,98)
40  98  FORMAT(/,7X,'RL','Vph/Iph (PU)',//)
41  99  IF(I)102,103,103
42  103  XK=K7*RL/(K5*.12)
43     XK1=XK/16.7
44  101  WRITE(6,101)RL,XK1
45  101  FORMAT(F15.7,7X,F15.7)
46  102  RL=RL*10.
47  104  Z=-1./XR
48  105  WW=-3.
49  104  FORMAT(/,5X,’dVph/dIph(in p.u.) must be less than’,F15.3)
50  105  STOP
51  END
APPENDIX C

Control Program for Type II Simulator:

* A PROGRAM TO CONTROL THE PV SIMULATOR

* INPUTS:
  1. START SIGNAL FROM BITS OF PA0
  2. CURVE SELECT SIGNAL FROM BIT0 TO BIT3 OF PA0
  3. CURRENT SIGNAL FROM PA10
  4. VOLTAGE SIGNAL FROM PB11

* OUTPUTS:
  1. CONTROL SIGNAL OUTPUT TO PA WHICH IS CONNECTED TO D/A CONVERTER
  2. A/D ENABLE SIGNAL TO BIT4 OF VIA0
  3. D/A ENABLE SIGNAL TO BIT6 OF VIA0

* VIA1 DEFINITIONS:

  CFE0 IRB EQU $CFE0 PORTB OF VIA1
  CFE0 ORB EQU $CFE0 PORTB OF VIA1
  CFE1 IRA EQU $CFE1 PORTA OF VIA1
  CFE2 RRAB EQU $CFE2 PORTA OF VIA1
  CFE3 DRRA EQU $CFE3 DATA DIRECTION REG. B
  CFE3 DDRB EQU $CFE3 DATA DIRECTION REG. A

* VIA0 DEFINITIONS

  CFF1 ORA2 EQU $CFF1 PORTA OF VIA0
  CFF1 IRA2 EQU $CFF1 PORTA OF VIA0
  CFF3 DRRA0 EQU $CFF3 DATA DIRECTION REG. OF VIA0

* OTHER DEFINITIONS

  KPL EQU 0014
  KPH EQU 0014

* PROGRAM STARTS HERE:

* INITIATE VIA'S

  0100 10CE 0100 START
  0104 86 50  LDA #0100000
  0106 B7 CFF3 STA DDRA0 SET PORT A OF VIA0
  0109 CC 00FF LDD #0000FF
  010C FD CFE£ STD DDRB SET PA & PB OF VIA1
  010F 86 50 LDA #0100000
  0111 B7 CFF1 STA ORA0 DISABLE A/D, D/A CONVERTERS
  0114 86 00 LDA #0
  0116 B7 CFE1 STA ORA OUTPUT '0' TO PORT A
  0119 B6 10 LDA #00010000
  011B B7 CFF1 STA ORA0 ENABLE D/A CONVERTER, D/A OUTPUT '0'

  00
  011E 86 00 LDA #0
  0120 B7 0228 STA VC SET CONTROL SIGNAL OUTPUT '0'
  0123 86 50 LDA #01010000
  0125 B7 CFE1 STA ORA0 DISABLE D/A CONVERTER
  0128 86 00 LDA #0
  012A B7 CFF3 STA DDRA SET PORT A OUTPUT PORT

  58
  59
  60

* TO FORM V/I CURVE:
61 012D 8E 0240 L1 LDX #TBB LOAD X WITH BEGINNING OF ADDRESS TABLE
62 0130 56 CFF1 LDA IRA0
63 0133 84 20 ANDA #x00100000 CHECK START SIGNAL
64 0135 26 82 BNE L0 IF STOP, THEN IDLE
65 0137 86 40 LDA #x01000000
66 0139 B7 CFF1 STA ORA0 ENABLE A/D CONVERTER
67 013C 86 CFF1 LDA IRA0 SELECT CURVE
68 013F 84 0F ANDA #FF
69 0141 48 ASLA
70 0142 1A 8E 86 LDY A, X Y=BEGINNING OF DATA TABLE
71 0144 17 008E LBSR ADJ TO SUBROUTINE TO ADJUST PARAMETERS
72 0146 8C CFF9 LDD IRA INPUT I, V SIGNAL
73 0148 B7 0226 STA V STORE V SIGNAL
74 014A 86 50 LDA #x01000000
75 0150 B7 CFF1 STA ORA0 DISABLE A/D CONVERTER
76 0153 86 40 LDA #00000000 CHECK WHETHER I>lbound
77 0156 86 30 LDA #10000000 JUMP TO LOOKUP TABLE IF I>lbound
78 0159 B7 0237 STA KP
79 015D 86 C231 LDA SLO
80 0162 3D MUL
81 0164 40 NEGA
82 0166 8E 0230 ADDA VMA A=VMA-SLO*I, (I>lbound)
83 0168 8E 16 BRA LY
84 016A 8E 03 LT LDA #3 TIME EQUALIZER
85 016C 4A 48 DECA
86 016E 8E 0E30 LDA #KPL
88 016E B7 0237 STA KP
90 0171 F1 022F CMPB IMA
91 0174 82 02 BHI LX
92 0176 20 03 BRA LW
93 0178 F6 022F LX LDB IMA
94 017B 8E 05 LW LDA B, Y LOCKUP VOLTAGE IN DATA TABLE
95 *
96 *
97 *
98 *
99 017D 17 0005 LY LBSR CONT1
100 0180 C6 FF LDB #FF
101 0182 F7 CFE3 STB DDRA SET PORT A OUTPUT PORT
102 0185 B7 CFE1 STA ORA SEND VC TO PORT A
103 0188 C6 10 LDB #x00100000
104 018A F7 CFF1 STB ORA0 ENABLE D/A, VC IS OUTPUT TO D/A
105 018D C6 50 LDB #x01010000
106 018F F7 CFF1 STB ORA0 DISABLE D/A
107 0192 C6 0 LDB #0
108 0194 37 0E PULU A,B
109 0196 A6 FF93 STB DDRA SET PORT A INPUT PORT
110 0197 16 FF93 LERA L1
111 *
112 019A 8E 0E33 ADJ LDX #ADT
113 019D EE 86 LDU A, X
114 019F 37 06 PULU A,B
115 01A1 FD 022F STD IMA
116 01A4 37 0E PULU A,B
117 01A6 FD 0231 STD SLO
118 01A9 39 RTS
119 *
* SUBROUTINE: CONT

*******************************************************************************
* * INPUT: COMMAND VOLTAGE VR (IN REGISTER A) *
*  2. SAMPLED VOLTAGE IN MEMORY V *
* * OUTPUT: CONTROL OUTPUT (IN REGISTER A) *
* * MODIFY: MEMORY VC,E1 *
* *
180 01A1 1F 87  CONT  TFR  A,B
181 01AC 8E 00  LDA  #0
182 01AE 85 0225  SUBB  V0
183 01B1 FD 0229  STD  E
184 01B4 4D  TSTA
185 01B5 2A  0C  BPL  EPL
186 01B7 43  COMA
187 01B8 53  COMB
188 01B9 5C  INCB
189 01BA B6 0223  LDA  A0
190 01BD 3D  MUL
191 01BE 53  COMB
192 01B0 5C  INCB
193 01C1 20  04  BRA  C1
194 01C3 B6 0223  EPL  LDA  A0
195 01C6 3D  MUL
196 01C7 FD 022D  C1  STD  SE0
197 01CA FC 022B  LDD  E1
198 01CD4D  TSTA
199 01CE 2A  09  BPL  EPL1
200 01D0 43  COMA
201 01D1 53  COMB
202 01D2 5C  INCB
203 01D3 B6 0224  LDA  A1
204 01D6 3D  MUL
205 01D7 20  07  BRA  C2
206 01D9 B6 0224  EPL1  LDA  A1
207 01DC 3D  MUL
208 01DD 43  COMA
209 01DE 53  COMB
210 01DF 5C  INCB
211 01E0 F3 022D  C2  ADDD  SE0
212 01E3 F3 0227  ADDD  VC0
213 01E6 4D  TSTA
214 01E7 88  09  BMI  VC0
215 01E9 27  0E  BEG  NORM
216 01E6 C6 FF  LDB  *#FF  REQUIRED CONTROL EXCEEDS MAX. VALU
E
217 01E0 F7 022B  STB  VC
218 01FC 8E 0A  BRA  C3
219 01F3 F3 0228  VCM  LDB  #0
220 01F4 F7 0228  STB  VC  REQUIRED CONTROL IS NEGATIVE, SET
VC=0
221 01F7 20  03  BRA  C3
222 01F9 8E 0A  BMI  VC
223 01FA F7 0228  STB  VC  REQUIRED CONTROL IS NORMAL
224 01FE FD 022B  STD  E1
225 0202 B6 022B  LDA  VC  UPDATE E
226 020E 8E 0A  BRA  C2
227 020F 8E 0A  UPDATE E
228 0212 8E 0A  BRA  C1
229 0213 8E 0A  UPDATE E
230 0214 8E 0A  BRA  C0
231 0215 8E 0A  UPDATE E
232 0216 8E 0A  BRA  C2
233 0217 8E 0A  UPDATE E
234 0218 8E 0A  BRA  C1
235 0219 8E 0A  UPDATE E
236 021A 8E 0A  BRA  C0
237 021B 8E 0A  UPDATE E
238 021C 8E 0A  BRA  C2
239 021D 8E 0A  UPDATE E
240 021E 8E 0A  BRA  C1
241 021F 8E 0A  UPDATE E
242 0220 8E 0A  BRA  C0
243 0221 8E 0A  UPDATE E
244 0222 8E 0A  BRA  C2
245 0223 8E 0A  UPDATE E
246 0224 8E 0A  BRA  C1
247 0225 8E 0A  UPDATE E
248 0226 8E 0A  BRA  C0
249 0227 8E 0A  UPDATE E
250 0228 8E 0A  BRA  C2
251 0229 8E 0A  UPDATE E
252 022A 8E 0A  BRA  C1
253 022B 8E 0A  UPDATE E
254 022C 8E 0A  BRA  C0
255 022D 8E 0A  UPDATE E
256 022E 8E 0A  BRA  C2
257 022F 8E 0A  UPDATE E
258 0230 8E 0A  BRA  C1
259 0231 8E 0A  UPDATE E
260 0232 8E 0A  BRA  C0
261 0233 8E 0A  UPDATE E
262 0234 8E 0A  BRA  C2
263 0235 8E 0A  UPDATE E
264 0236 8E 0A  BRA  C1
265 0237 8E 0A  UPDATE E
266 0238 8E 0A  BRA  C0
267 0239 8E 0A  UPDATE E
268 023A 8E 0A  BRA  C2
269 023B 8E 0A  UPDATE E
270 023C 8E 0A  BRA  C1
271 023D 8E 0A  UPDATE E
272 023E 8E 0A  BRA  C0
273 023F 8E 0A  UPDATE E
274 0240 8E 0A  BRA  C2
275 0241 8E 0A  UPDATE E
276 0242 8E 0A  BRA  C1
277 0243 8E 0A  UPDATE E
278 0244 8E 0A  BRA  C0
279 0245 8E 0A  UPDATE E

SUBROUTINE CONT1:

INPUT:

1. VOLTAGE COMMAND IN REGISTER A

2. SAMPLED VOLTAGE IN MEMORY V

OUTPUT:

CONTROL VC IN REGISTER A

RESERVED MEMORY UNITS:

PV DATA STORAGE:
END