GaAs MATERIAL INVESTIGATION FOR INTEGRATED CIRCUITS FABRICATION

By

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ABSTRACT

The primary objective of the work described in this thesis was to study the influence of undoped LEC GaAs substrate material from various suppliers on the performance of ion implanted and annealed active layers. Optical transient current spectroscopy (OTCS) was investigated as a qualification test for GaAs substrates. Deep level spectra of the substrates before ion implantation were obtained. It was found that while the OTCS spectra of high pressure grown GaAs from two suppliers were similar, that of the low pressure material showed different relative concentration of traps. The use of OTCS was further extended to study trap concentration as a function of surface treatment. It was found that the use of chemical etchants reduces the concentration of some levels, possibly those located on the surface as opposed to bulk traps. Surface damage was found to enhance the negative peak in the OTCS spectrum. The deep levels spectra were found to be affected by the geometry of the device and the type of electrode material.

Channel current deep level transient spectroscopy (DLTS) was used to study both process- and substrate-induced deep levels in ion implanted MESFET channels. The spectra of process-induced traps were found to be different according to the encapsulant used. Silicon dioxide (both RF sputtered and plasma enhanced chemically vapor deposited (PECVD)) was found to induce a variety of process related defects. This is believed to be because silicon dioxide is permeable to gallium and hence does not preserve the stoichiometry

of ion implanted GaAs during high temperature anneals. Deep level spectra of MESFETs annealed using silicon nitride, on the other hand, were found to contain single traps related to the defects in the starting material. For implants through silicon nitride, a high concentration of the main electron trap EL2 was found, whereas implants directly into the surface resulted in the level EL12.

Comparison of the characteristics of the variety of LEC undoped GaAs material show that they differed widely and had inhomogeneous properties. For example, compared to the high pressure grown GaAs, the Litton's low pressure substrate had lower activation, mobility, drain current and threshold voltage, good confinement of the scatter in the same characteristics, low concentration of deep levels, and the least backgating effect which makes it promising for IC fabrication. Comparison of the high pressure grown material from two suppliers showed that Cominco's recent material had good mobility, activation, relatively high scatter of threshold voltage, high concentration of deep levels, and was affected by backgating. In comparison, Sumitomo's material showed thermal instability, less scatter of threshold voltage, less mobility and deep level concentrations, and similar backgating characteristics. Substrate grown three years earlier showed higher diffusion of dopant, different deep levels, and better backgating characteristics. Finally, a substrate which had failed the qualification test by a device manufacturer showed minimal diffusion tails and threshold voltage scatter, the highest concentration of deep levels, and substantial backgating.

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CHAPTER 1

INTRODUCTION

Formation of uniformly doped impurity layers in bulk grown GaAs substrates for integrated circuit (IC) fabrication by ion implantation offers more advantages than the use of doped epitaxial grown layers because of the ease, precise control and reproducibility of the implantation process. Of the two available bulk crystal growth methods, Horizontal Bridgman (HB) and Liquid-Encapsulated Czochralski (LEC), the former has found decreasing applications in IC fabrication because of the limitation of the size and shape of HB substrates, and because of low device yield. LEC grown GaAs, on the other hand, is becoming the dominant choice for IC fabrication because two to four inch diameter wafers can be grown, and because semi-insulating (SI) GaAs can be made without intentional addition of impurities.

The objectives of this thesis are to investigate undoped LEC GaAs substrates for IC fabrication. GaAs wafers from different vendors were obtained. The deep trapping levels in SI GaAs wafers were investigated using Optical Transient Current Spectroscopy (OTCS). Deep levels in ion implanted MESFETs fabricated using several different processing techniques were investigated by channel current Deep Level Transient Spectroscopy (DLTS). The processing techniques applied for MESFET fabrication included: (1) ion implantation directly into GaAs; and (2) ion implantation through Plasma Enhanced Chemically Vapor Deposited (PECVD) silicon nitride film. Several dielectric capping materials for high temperature anneals were used: (1) RF

sputtered silicon dixoide; (2) PECVD silicon dioxide; and (3) PECVD silicon nitride. Active layer parameters of various ion implanted substrates were investigated and compared. The measurements used to assess the MESFETs were: (1) threshold voltage and drain current magnitudes and scatter; (2) sheet resistance, Hall mobility and undepleted carrier concentration; (3) carrier and drift mobility profiling, and (4) backgating.

The contents of the thesis are as follows: Chapter 2 gives an overview of SI GaAs crystal growth techniques with particular emphasis on undoped LEC GaAs technology. In Chapter 2, a review is presented on deep levels in the starting SI GaAs materials, and a comparison is made of the OTCS spectra of GaAs substrates from different suppliers. Influence of surface treatment on the OTCS spectra is also investigated. Chapter 4 details the results of deep level investigation in the MESFETs fabricated by the four different processing techniques described above. The objective being to find and compare process-induced deep levels. Chapter 5 contains a comparison of MESFETs made by the same process at the same time on GaAs wafers from three suppliers, including: (1) low and high pressure grown substrates; (2) high pressure grown substrates from two suppliers; and (3) two high pressure grown substrates from the same supplier which were grown at two different time periods. In addition, a substrate is investigated which did not pass qualification tests by a device manufacturer. Finally, Chapter 6 gives conclusions and suggestions for future work.

CHAPTER 2

GROWTH AND PROPERTIES OF SEMI-INSULATING GALLIUM ARSENIDE

2.1 Introduction

Semi-insulating GaAs is used for the production of high performance electronic devices such as high speed digital integrated circuits, field effect transistors, charge coupled devices and monolithic microwave integrated circuits. For large scale integrated circuit GaAs technology to develop reliably many problems related to the reproducible growth of high quality crystals remain to be solved. To achieve high electrical yields of GaAs ICs [1] it is essential to develop GaAs subtrates with low density of dislocations and impurities, high resistivity and good thermal stability, high activation of the implanted species, and homogeneous doping profiles.

2.2 GaAs Crystal Growth Techniques

There are two main GaAs crystal growth techniques: the Horizontal Bridgman (HB) and the Liquid-Encapsulated Czochralski (LEC) [2,3,4]. In the former, a quartz boat which contains gallium is sealed inside a quartz ampoule filled with an inert gas. Arsenic is placed at the neck of the ampoule, and a temperature gradient is established such that the arsenic starts to sublimate (614°C) and the temperature of gallium is held at 1235°C, the melting point of GaAs. After the arsenic evaporates and reacts with gallium to form a GaAs melt, either the ampoule or the heaters are slowly moved so that the GaAs is cooled at one end as the temperature gradient moves

along the boat; the growth then proceeds in the <111> direction. The resulting ingot takes the shape of the boat truncated by the liquid surface i.e., it is D shaped. The wafers have to be cut at an angle to yield <100> material. A variety of impurities are introduced into the ingots in the quartz silica boat container. The predominant type of impurity is silicon, usually in the 10^{16} - 10^{17} cm^{-3} range [5]. To make the HB GaAs semi-insulating, a deep acceptor impurity, usually chromium, has to be incorporated into the melt at approximately 10^{17} cm^{-3} so as to balance the donor impurity level. Problems arise because of inhomogeneous FET performance in HB GaAs because of the nonuniformity in the chromium concentration resulting from the disagreement between the cutting plane and the growth plane [6]. As an alternative to quartz boats, Pyrolitic Boron Nitride (PBN) boats have been used in an attempt to achieve higher purity GaAs [5], somewhat better performance was reported, but nevertheless, the resulting electrical yields for ion implantation remain generally low [1].

The LEC technique [7] is used for the growth of III-V compounds with one volatile constituent. In this method, the melt is prepared by a compounding process [3] where gallium and arsenic are placed below a boric oxide (B_2O_3) encapsulant and the entire assembly is heated. The temperature is held at the melting point of GaAs, and the seed is lowered through the molten encapsulant into the GaAs melt. In addition, an overpressure of an inert gas, typically argon, is applied to prevent the arsenic from bubbling through the boric oxide. Both the seed and the crucible are rotated slowly in the opposite directions at predetermined rotational speeds so as to reduce radial and slice-to-slice nonuniformities [8]. A slow pull rate is applied

to the seed and <100> GaAs round ingots 2-4 inches in diameter are grown.

To reduce contamination of GaAs with silicon, PBN rather than quartz crucibles are used [9]. The resulting silicon concentration is reduced from 10^{16} to 10^{15} cm^{-3}. Another reason for not using quartz is that the boric oxide reacts with silicon resulting in losing the clear visibility through the encapsulant which is an essential requirement in GaAs melt growth. With a quartz crucible, the boric oxide turns grey, opaque, and becomes full of bubbles [9], evidence of undesirable reaction of the melt with the surroundings. With a PBN crucible, the boric oxide remains clear and scum free. Growth of highly resistive GaAs depends directly on the boric oxide preparation before growth; the encapsulant has to be heat treated and vacuum baked to reduce the water content and prevent contamination of the melt with oxygen.

Unlike HB GaAs ingots, LEC GaAs ingots are round, cylindrical and can be semi-insulating without intentional doping. Though it is necessary to add chromium to the GaAs melt when grown with quartz crucibles, the same material grown with PBN crucibles is sufficiently high in resistivity to make it acceptable for device fabrication. The major advantages of undoped over chromium doped LEC GaAs are the following: (1) the lower concentration of the ionized impurities leads to higher electron mobilities in the ion implanted region; and (2) the absence of large resistivity changes which are typically caused by the redistribution of chromium during high temperature annealing. Undoped LEC GaAs is gradually emerging as a high quality and reproducible material for fabrication of ion implanted active layers.

2.3 Impurities and Their Role in Undoped LEC GaAs

The principal source of residual impurities in undoped LEC GaAs is the interaction of the melt with the crucible and the boric oxide encapsulant [10]. Investigation of the various impurities using spectroscopic techniques [1,11,12] revealed the existence of contaminants in undoped LEC GaAs grown with PBN crucibles, and substrate-to-substrate as well as ingot-to-ingot variations in concentration. Table 2.1 shows the order of magnitude of some of the impurities.

Boron, which is believed to be inactive in GaAs [11], is introduced into the melt through reaction with the boric oxide. Oxygen is believed to be substitional in the arsenic sublattice giving rise to a deep donor level. Its origin is traced to the water levels ("wetness") of the boric oxide. It was only recently concluded [13] that oxygen is not associated with the main electron trap EL2 which is responsible for the semi-insulating property of GaAs. Chromium, an unintentional impurity, creates a deep acceptor level [4] when it occupies substitutional sites in the gallium sublattice. Silicon is a shallow donor and has consistently lower concentration when a PBN rather than a quartz crucible is used. Carbon is observed at high concentrations in GaAs, and is believed to arise from the PBN crucible and from the close proximity of the melt to the hot graphite furnace parts [10]. This impurity forms a shallow acceptor and together with the deep donor antisite defect [14] tends to compensate the GaAs. Sulfur arises from the arsenic source element [1] and forms a shallow donor. Magnesium and manganese are shallow acceptors introduced from the silicon nitride coracle [1] and the bulk material [2] respectively. Iron and copper impurities are deep acceptors

Table 2.1. Order of magnitudes of some common impurities found in SI, undoped, LEC GaAs

Impurity	Log (concentration/cm^3)
Boron	15
Oxygen	16
Chromium	14
Silicon	15
Carbon	16
Sulfur	15
Magnesium	15
Manganese	15
Iron	15
Copper	15
Selenium	15
Tellurium	15

with potentially degrading effects on the ion implanted layer. The former has been demonstrated to cause interface traps between the active layer and the substrate [15] whereas the latter moves rapidly at low temperatures causing effective reduction of the diffusion length of n-type GaAs [4]. Copper contamination of GaAs takes place during crystal growth as a result of contact with the puller's brass material [5].

2.4 Relation of the Melt Stoichiometry to Compensation and Thermal Stability of GaAs

GaAs melt composition is an important growth parameter which affects both resistivity [10,16] and the concentration of the midgap level EL2 [16] which is now believed to be the antisite defect arsenic on gallium site [14]. Stoichiometry variations in GaAs substrates generate various native defects which recently have been found to influence the ion implanted carrier concentration profiles and electrical activation [17]. Recent results on resistivity data [16] have shown that using dry boric oxide (500 ppm H_2O), and above a critical arsenic concentration of 0.48 atom fraction of the melt, the GaAs material is semi-insulating and thermally stable up to about 0.53 (As atomic fraction). For compositions where the arsenic atom fraction is above 0.53, the resistivity drops due to increase in the free electron concentration. On the other hand, below the critical arsenic concentration, GaAs turns p-type. This can be explained by reasoning that the EL2 concentration increases with increasing As/Ga and V_{GA}/V_{AS} ratios [14], and a balance is made with the residual carbon acceptors [18] so as to make the material semi-insulating. The material becomes p-type below the critical composition because the EL2 concentration becomes lower than that of the

shallow acceptors, and becomes n-type for compositions above 0.53 As atom fraction because the EL2 concentration is higher than the shallow acceptors concentration.

Significantly different results are obtained when using wet boric oxide (2000 ppm H_2O). Recent results [19] have shown that in this case above a critical arsenic concentration of 0.42 atom fraction of the melt, the GaAs material remains semi-insulating up to an arsenic atom fraction of 0.48. The impurities concentration in the melt for boron, oxygen, and carbon are different from typical levels obtained with dry boric oxide. Lower concentration for both boron and carbon were found, but the concentration of oxygen predictably was larger. The compensation in this case is expected to be different because of the lowering in the concentration of both EL2 (due to different melt composition) and carbon and the increase in the density of oxygen donors.

The thermal stability of undoped SI GaAs is also strongly influenced by the stoichiometry of the melt. Conversion of the thin surface layer of GaAs to a conducting state, believed to be p-type, after thermal treatment was previously attributed to out-diffusion and pileup of residual acceptors, such as, manganese [20], and an increase in carbon levels due to solvents used during substrate preparation [12]. Recent results indicate that high thermal stability for undoped LEC GaAs can only be achieved with stoichiometric or arsenic rich compositions [10]. For gallium rich melts and dry boric oxide, the sheet resistance is observed to decrease rapidly following high temperature anneal. Surface conversion results when the EL2 concentration at the surface falls below the residual acceptor concentration,

and the surface becomes p-type. This mechanism is probably enhanced by the outdiffusion of gallium and/or arsenic defects to the surface.

2.5 Recent Advances in the Growth of Undoped LEC GaAs

Major efforts in the past few years have been concentrated on developing a controlled and reproducible growth technique of high quality undoped LEC GaAs crystals. One such effort aims at purifying the material using a special computer controlled distillation process [21]. In this technique, the arsenic pressure inside the growth chamber is abruptly decreased to near one atmospheric pressure; this creates bubbling in the boric oxide encapsulant as gases which include water, compounds of carbon and water, compounds of silicon and water, and excess arsenic are released from the melt. This bubbling process is repeated until the electrical conductivity of the melt is appreciably decreased. GaAs crystals are grown at low pressure (6 atm), and low temperature gradient in the melt (50°C/cm) is achieved by using thermal reflectors. With both silicon dioxide and PBN crucibles, highly homogeneous and highly resistive (1×10^{8} ohm-cm) ingots were obtained. The wafers are characterized with low dislocation density (8×10^{3} -1×10^{4} cm^{-2}) with a U-shaped distribution.

An alternative to the high pressure growth synthesis which is in common use is a recent low pressure growth technique which is said by its advocates to be more efficient [22]. The advantages of low pressure growth techniques are that the cycle times are significantly shorter, the maximum crucible temperature is lower, the melt capacity is larger, and the melt stoichiometry can be better controlled. Though the quality of the material

has not been fully proven, recent results of GaAs grown using quartz crucibles indicate similar thermal stability for arsenic rich melts (As/Ga = 1.02~1.04 atomic) and dry boric oxide (500 ppm water). The activation and mobility of silicon implanted material indicates similar results compared to the high pressure grown GaAs. The work for this thesis includes tests on a GaAs wafer grown at low pressure.

More recently, attempts were made to reduce the dislocation density in semi-insulating GaAs crystals [23,24]. The principle involved is to grow the crystal under a low temperature gradient and under a low pressure (5 atm), as this further lowers the temperature gradient by decreasing the convection heat transfer. The improvements made are found in: (1) reducing the arsenic escape by increasing the thickness of the boric oxide encapsulant; (2) reducing the temperature gradient at the boric oxide and the GaAs melt interface; (3) reducing the temperature gradient of the boric oxide itself by opening windows bored in the susceptor cylinder to directly heat this layer [24], and by setting a thermal baffle above the crucible [23]. As a result of those improvements, very low dislocation densities of approximately $1000/cm^2$ with uniform distribution, and homogeneous high resistivities (10^8 ohm-cm) were obtained for two inch diameter wafers.

Another technique which is successfully applied to obtain dislocation free crystals is based on adding large amounts of indium or indium arsenide (0.1 mol% - 0.4 mol%) to the GaAs melt [12]. Those additions are found to be effective in suppressing the generation of microdefects which are responsible for the formation of dislocations. This improvement, along with reducing the temperature gradient at the solid/liquid interface, is necessary to prevent

the generation and multiplication of dislocations from localized thermal stresses. The resulting quality of the ion implanted layers' uniformity indicate better homogeneity than conventional undoped LEC GaAs crystals.

Finally, the application of a vertical magnetic field [25,26] has been attempted recently to enhance the uniformity and to reduce the dislocation density of high pressure LEC PBN grown GaAs. The effect of the magnetic field, which is supplied by a super-conducting coil, is to suppress the temperature fluctuations through the molten GaAs. More importantly, laminar thermal convection which degrades both the microscopic and macroscopic homogeneity of crystals has been reduced. Uniformity in the GaAs melt is enhanced by optimizing the seed rotation as this adds forced convection to the melt. It is expected that those improvements can enhance the quality of the GaAs substrates for ion implantation.

CHAPTER 3

OPTICAL TRANSIENT CURRENT SPECTROSCOPY INVESTIGATION OF VARIOUS GaAs SUBSTRATES

3.1 Introduction to Optical Transient Current Spectroscopy

Optical Transient Current Spectroscopy (OTCS), often referred to as Photo Induced Transient Spectroscopy (PITS) [27], is a member of the class of Deep Level Transient Spectroscopy (DLTS) techniques. Its advantage is that it can be applied to semi-insulating GaAs (which is the starting material for integrated circuit (IC) fabrication). The aim is to obtain information on deep trapping levels which may be of fundamental interest and would certainly be of practical interest if it could help in diagnosing the suitability of the material for IC fabrication.

The OTCS method was introduced by Hurtes, Boulou, Mitonneau, and Bois [28], by Fairman, Morin and Oliver [29], and by Martin and Bois [30]. This method is suitable for the investigation of deep trapping levels in high resistivity epitaxial layers and semi-insulating GaAs substrates to which other deep trapping level spectroscopy methods [31] are not applicable. Several GaAs materials have been investigated using OTCS; for example, chromium doped Bridgman GaAs was investigated by Hurtes [28], Devaeaud [32], Fairman [1,29,33], and Martin [30], Chromium doped LEC GaAs was investigated by Fairman [1,29,33], whereas undoped LEC GaAs was examined by Oliver [34], K. Lowe [35], and W. Tang [36]. GaAs grown by Vapor Phase Epitaxy (VPE) on chromium doped substrates was investigated by Itoh [37], Fairman [1,29,33],

and Hurtes [28]. OTCS was further used to search for deep levels in other materials such as, indium phosphide (InP) [27], and lead iodide (PbI_2) [38] which is an insulator.

As a result of the application of OTCS to the study of GaAs substrate material, several significant deep levels were observed. For example, the deep level EL2 [39,40] has been observed by Martin [30], and Tang [36]. Chromium related deep levels which are responsible for the semi-insulating behaviour of chromium doped GaAs were detected (as HL1) by several investigators [1,28,29,32,33,37,41]. Other deep levels due to impurities or native defects [42] (and with distribution affected by dislocations [43]) were also detected, and are believed to cause problems of variable threshold voltage [44], hysteresis [45], frequency dependent transconductance [46], and noise [47] in GaAs ICs.

3.2 Theory of Optical Transient Current Spectroscopy

The theory of OTCS was proposed by Hurtes et al. [28] and then developed by Martin et al. [30]. It is based on a depletion layer model where the current is determined by the charge transport across a depletion layer by electrons or holes released from traps. Thus an electron trap (i.e. a centre which communicates only with the conduction band) may capture an electron during illumination and lose it afterwards. The contribution which the electron makes to the terminal current as it crosses the depletion layer is as if this layer acted as an insulator separating the conducting (or semi-conducting region) from the electrodes. A hole trap behaves similarly. Once gone the carriers are not replaced because the concentration of

electrons and holes in the reverse biased junction depletion region are low. Assuming that the probability f that a trap is occupied by an electron, the following rate equations are defined [48]:

$$\text{rate of electron capture} = r_a = n\, N_T\, (1-f)\, V_n \sigma_n$$

$$\text{rate of electron emission} = r_b = N_T f\, e_n$$

$$\text{rate of hole capture} = r_c = p\, N_T\, f\, V_p \sigma_p$$

$$\text{rate of hole emission} = r_d = N_T (1-f)\, e_p$$

where n(p) is the density of electrons (holes), $V_n(V_p)$ is the thermal velocity of electrons (holes), $\sigma_n(\sigma_p)$ is the electron (hole) capture cross section, and N_T is the total population of the trap. Imposing the steady state condition that $r_a - r_b = r_c - r_d$ yields:

$$f_{ss} = \left(1 + \frac{e_n + \sigma_p V_p p}{e_p + \sigma_n V_n n}\right)^{-1}$$

Given that the current during illumination has reached a steady value and that at time t=0 the illumination is removed one finds:

$$f(0) = \left(1 + \frac{e_n + \sigma_p V_p\, (p_\infty + \delta_p)}{e_p + \sigma_n V_n\, (n_\infty + \sigma_n)}\right)^{-1} \approx \left(1 + \frac{\sigma_p V_p}{\sigma_n V_n}\right)^{-1}, \text{ for } \delta_n = \delta_p \text{ large enough}$$

$$f(\infty) = \left(1 + \frac{e_n + \delta_p V_p p}{e_p + \sigma_n V_n n}\right)^{-1} \approx \left(1 + \frac{e_n}{e_p}\right)^{-1}, \text{ for no recapture in the dark.}$$

where n(p) is the equilibrium concentration in the dark of electrons (holes) and $\delta_n \approx \delta_p$ is the excess number of electrons and holes generated by the light.

The current i(t) is given by r_b and r_d,

$$i(t) = \frac{q\ A\ W}{2} N_T \left(e_n f(t) + e_p(1-f(t))\right)$$

where A is the area of the contact and W is the width of the layer. So

$$\Delta i(t) = i(t) - i(\infty) = \frac{q\ A\ W}{2} N_T\left(e_n(f(t) - f(\infty))\right) + e_p\left((1-f(t))-(1-f(\infty))\right)$$

From $\frac{df}{dt} = -fe_n + (1-f)e_p$ with solution

$$f(t) = f(\infty) + \left(f(0) - f(\infty)\right) \exp -t/\tau$$

where $1/\tau = e_n + e_p$, we obtain:

$$\Delta i(t) = \frac{q\ A\ W}{2} N_T(e_n - e_p) \left(1 + \frac{e_n + \sigma_p V_p (p+\delta_p)}{e_p + \sigma_n V_n (n+\delta_n)}\right)^{-1}$$

$$- \left(1 + \frac{e_n + \sigma_p V_p P_\infty}{e_p + \sigma_n V_n n_\infty}\right)^{-1} \exp\ (-t/\tau)$$

Hurtes et al. treated the case of large $\delta_n = \delta_p$ during illumination and no recapture in the dark to obtain:

$$\Delta i(t) = \frac{q\ A\ W}{2} N_T (e_n - e_p) \left[\left(1 + \frac{\sigma_p V_p}{\sigma_n V_p} \right)^{-1} - \left(1 + \frac{e_n}{e_p} \right)^{-1} \right] \exp\ (-t/\tau)$$

For electron traps where $\sigma_n/\sigma_p >> 1$ and $e_n >> e_p$, and for hole traps where $\sigma_p/\sigma_n >> 1$ and $e_p >> e_n$, then the current reduces to:

$$\Delta i(t) = \frac{q\ A\ W}{2} N_T\ \tau^{-1}\ \exp(-t/\tau)$$

where $\tau = 1/e_n$ for electron traps, and $\tau = 1/e_p$ for hole trap. For the case of a boxcar's sampling whose output is

$$\Delta i(t) = A_B \left(i(t_1) - i(t_2) \right)$$

where A_B is the boxcar's amplification, the current difference is:

$$i(t) = A_B \frac{q\ A\ W}{2} N_T\ \tau^{-1}\ \left(\exp(-t_1/\tau) - \exp(-t_2/\tau) \right)$$

By differentiating the current difference with respect to τ and setting the result to zero, the value of maximum τ_m can be solved:

$$\frac{\delta \Delta i(t)}{\delta(\tau)} = 0 = (1-t_1/\tau_m)\exp(-t_1/\tau_m) - (1-t_2/\tau_m)\exp(-t_2/\tau_m)$$

can be solved for once t_1 and t_2 are set; and when the boxcar's time constant is set to this value, a maximum $\Delta i(t)$ is registered at a characteristic temperature T_m. Data on the activation energy ΔE and capture cross section σ can be obtained by inserting the sets of characteristic temperatures for each time constant into the equation defining the time constant of traps:

$$\tau = (\sigma \gamma T)^{-1} \exp(\Delta E/kT)$$

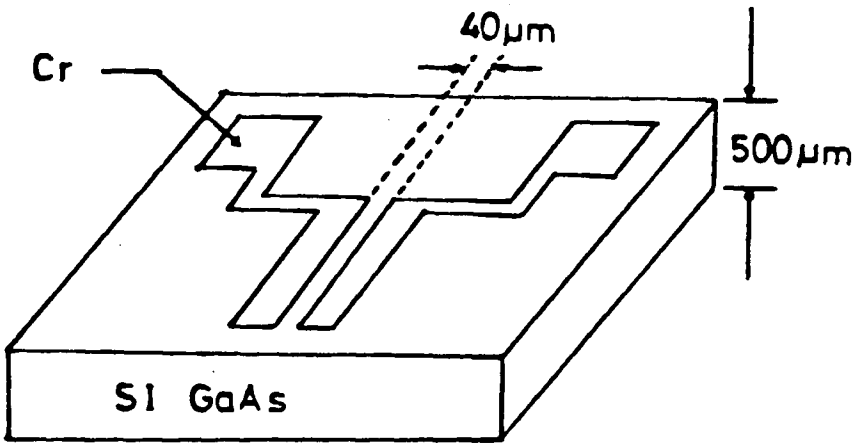
where ΔE is the difference from the conduction band to the trapping level energy for electron traps, and is the difference between the trapping level and the valence band for hole traps. γ is a constant defined as 2.28×10^{20} cm^{-2} S^{-1} k^{-2} for electron traps and 1.70×10^{21} cm^{-2} S^{-1} k^{-2} for hole traps.

While electron and hole traps give rise to positive peaks as the boxcar's output is swept through a temperature range of 150K to 400K, nevertheless, negative peaks are seen in various undoped LEC GaAs samples. They are obtained if $e_n > e_p$ and $(\sigma_p V_p/\sigma_n V_n) > (e_n/e_p)$, or if both inequalities are reversed. The possible mechanism [49,50] is that a centre which gives a negative peak gives a steady state dark current due to its pumping out first an electron then a hole. When the illumination ceases, one of these events occurs more slowly, and if the traps are left in the condition which requires the slow process as the next step, the current will initially be low i.e. a negative peak is produced.

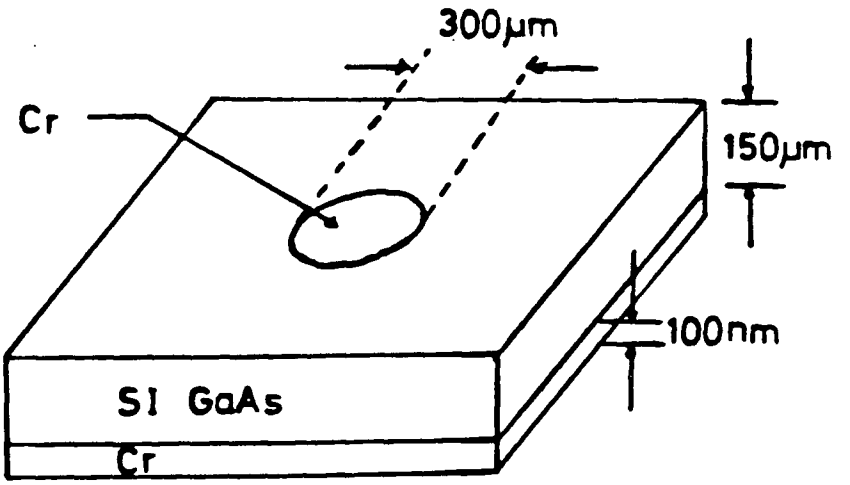
3.3 Experimental Procedure

Semi-insulating GaAs starting substrate materials investigated in this work were obtained from Cominco Ltd. and Bell Northern Research (BNR). All the substrates were LEC undoped wafers grown in the <100> direction. Three wafers labelled 344S10 (sheet resistivity = 2.8×10^8 ohms/square, mobility = 6700 cm^2/v sec, etch pits = 27000/cm^2), 453S74 and 453S75 (sheet resistivity = 3.1×10^8 ohms/square, mobility = 6100 cm^2/v sec, etch pits = 39000/cm^2) were obtained from Cominco. The first number in the label represents the ingot number, and the letter S (for seed) indicates that the last number stands for the slice number in the ingot counted from the seed end. Wafer #453S74 was reported (by BNR) to have been etched about 10 um using the following chemical etch: $H_2SO_4:H_2O_2:H_2O$ (4:1:1 by volume). A single wafer from Sumitomo was obtained which was grown at high pressure the same way as those from Cominco. The wafer was labelled 400600-1, and resistivity > 10^7 ohm.cm. No data were obtained for mobility and etch pit density. A single wafer from Litton was obtained. This was grown at low pressure. The wafer was taken from boule 2052, slice 2-9, and had the following specifications: resistivity = 1.37×10^8 ohm.cm, mobility = 2810 cm^2/v sec, and etch pit density = 30000/cm^2. All wafers were 2 inches in diameter.

Two types of test devices for OTCS were used. These were the planar and the sandwich type (figure 3.1). In the planar type the electrodes were evaporated side by side on one surface, and in the sandwich type they were evaporated on opposite surfaces. The electrodes were [3] either chromium or gold-germanium (Ge = 12%wt + Au=88%wt) unalloyed or alloyed at 450°C in flowing nitrogen. The chromium and unalloyed Au/Ge form a Schottky barrier.



(a)



(b)

Fig. 3.1 Geometry of (a) planar and (b) sandwich structures used in OTCS

The alloyed Au/Ge produces an n+ layer just under the contact (due to Ge). Some samples were thinned by grinding them in a silicon carbide slurry on a glass plate followed by a chemical etch in a solution of $H_2SO_4+H_2O_2+H_2O$ (4:1:1 by volume) for two minutes.

The block diagram of the experimental setup is shown in figure 3.2. The samples were mounted on a liquid nitrogen cooled finger (KRYOSTIK model 1320H) in an evacuated light-tight chamber as shown in figure 3.3 with contact probes for electrical connections. A power transistor was used to heat the samples. A copper-constantan thermocouple for temperature measurement was mounted on the sample holder close to the device. Light pulses were provided by a GaAsP 670 nm LED. A fixed voltage bias (typically ±7 VDC) was applied to the sample, and the current was amplified with an EG&G 181 current sensitive amplifier followed by an EG&G dual gate boxcar. The output of the boxcar and of the thermocouple (through an amplifier) were recorded on an X-Y recorder.

3.4 Results

The main practical question about the OTCS technique is whether it can usefully be employed to test the suitability of a particular batch of material for device fabrication. In addition to obtaining information about deep trapping levels, the use of OTCS here is further extended to investigate several effects on the DLTS spectrum, such as, the effects of chemical etch, surface damage, different test structures, varying contact geometry, and choice of electrode material.

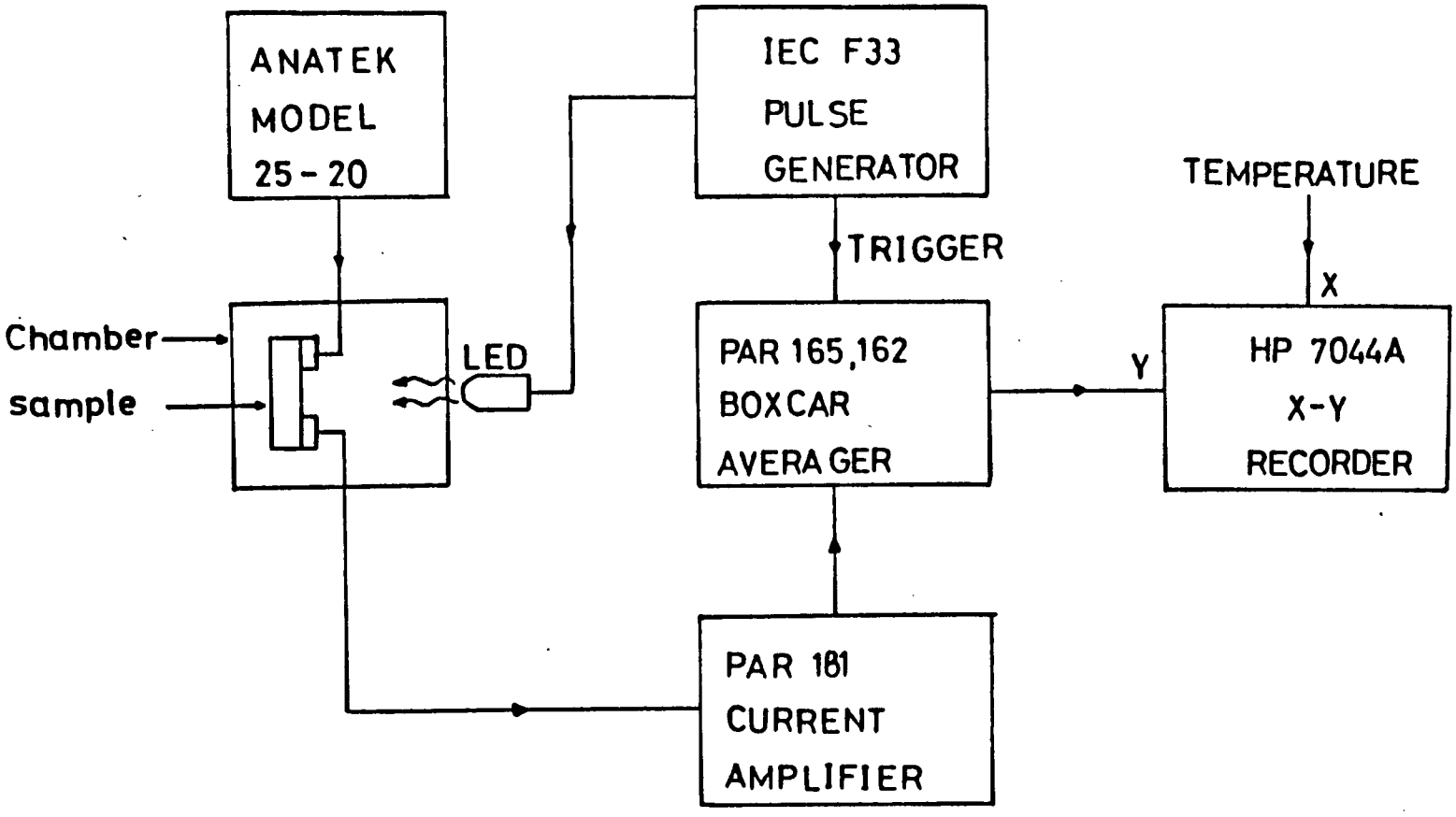


Fig. 3.2 Block diagram of the OTCS setup

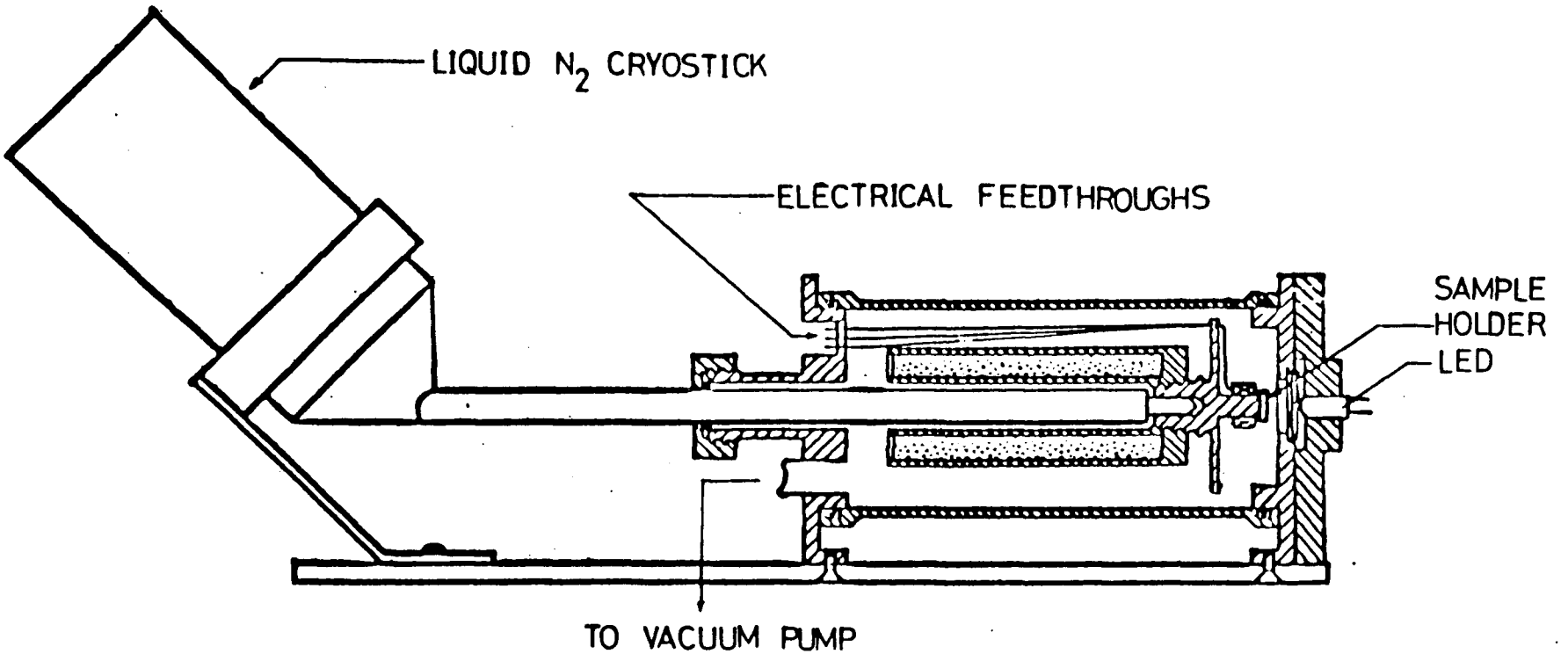


Fig. 3.3 Vacuum chamber used in the OTCS experiment

3.4.1 OTCS Spectra of GaAs Substrates From Three Vendors

Figure 3.4(a,b,c) shows the OTCS spectra of devices made on slices of Cominco's, Sumitomo's, and Litton's GaAs respectively. The test samples used here were the planar type with chromium electrodes (length = 30 um, width = 600 um). The spectrum of Cominco's GaAs was similar to test devices tested earlier [36] except in the high temperature range where the magnitude of the negative peak was larger, and peak 1 appears much smaller in magnitude. No information on how typical the GaAs substrates from Sumitomo and Litton is known. The OTCS spectra of Cominco and Sumitomo GaAs substrates show the same traps and with similar relative heights. Both substrates were high pressure LEC material. The OTCS spectrum of the Litton substrate, low pressure grown LEC, was considerably different in that although it shows a similar set of peaks, the relative peak heights are different. Figures 3.5(a,b) show the DLTS spectra of samples of both Cominco and Sumitomo before and after chemical etch in a mixture of sulfuric acid, water, and hydrogen peroxide (4:1:1 by volume). Though peaks 1 to 4 are unaffected by the surface etch, peaks 5 to 8 were considerably reduced in amplitude. This indicates that the unaffected peaks were due to deep levels present in the bulk of the substrates, whereas the affected defects were enhanced by surface conditions such as damage, oxides, and chemical treatment. These results demonstrate that the OTCS technique is useful in the investigation of surface etching treatments much as are used in the fabrication of devices to remove damage or contaminated surfaces.

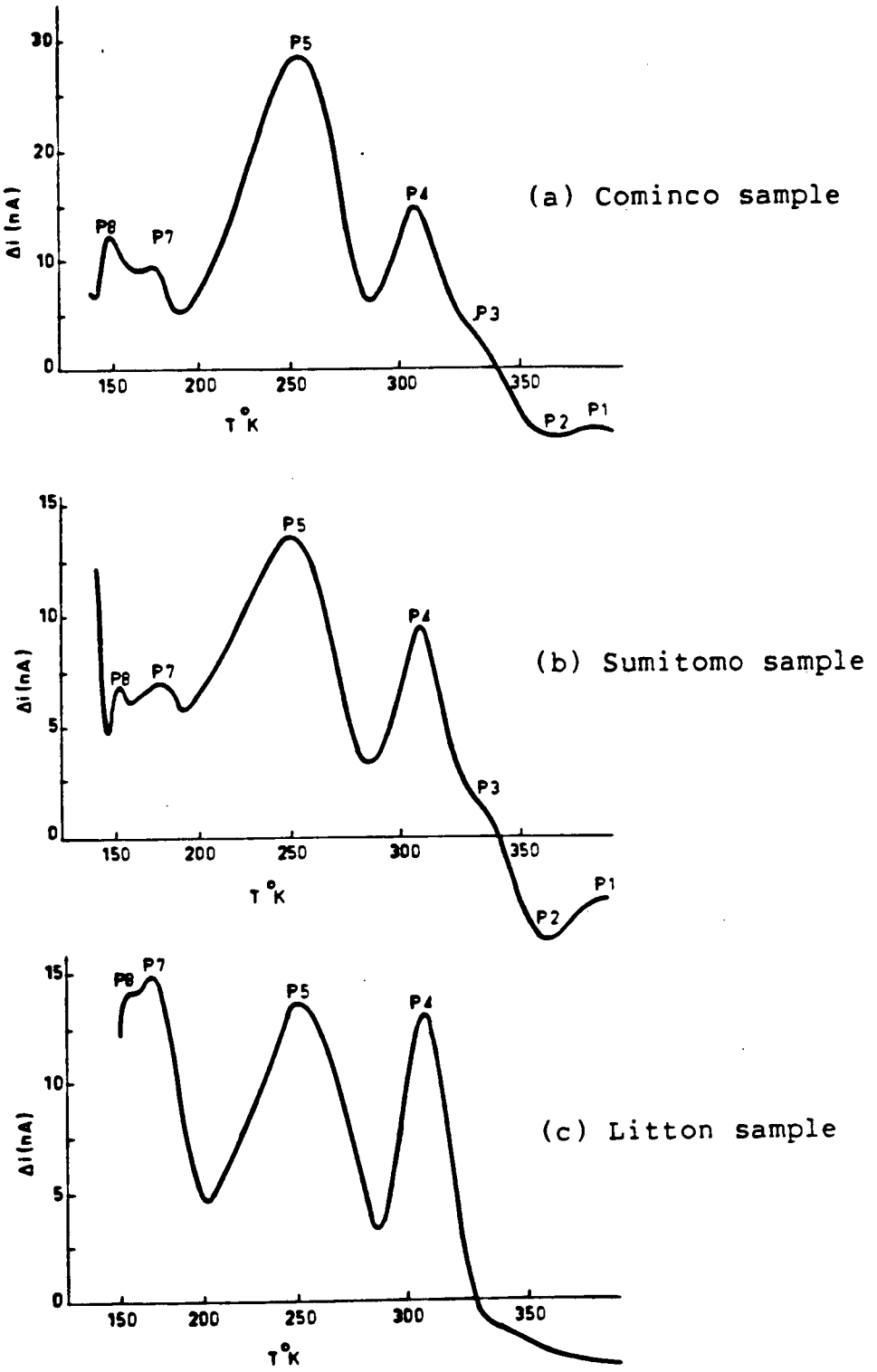
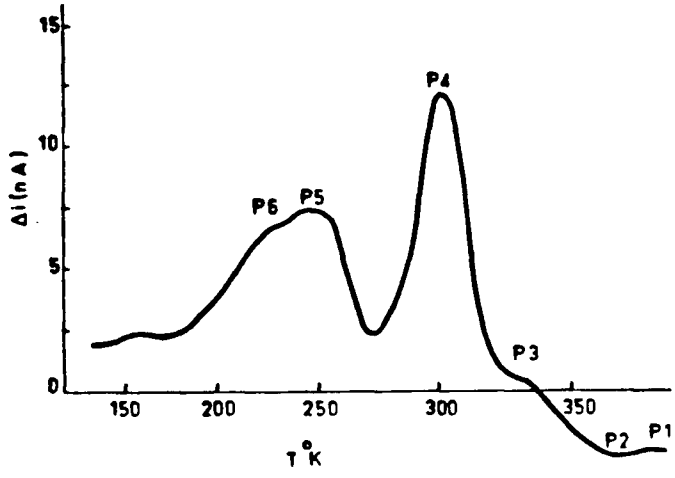
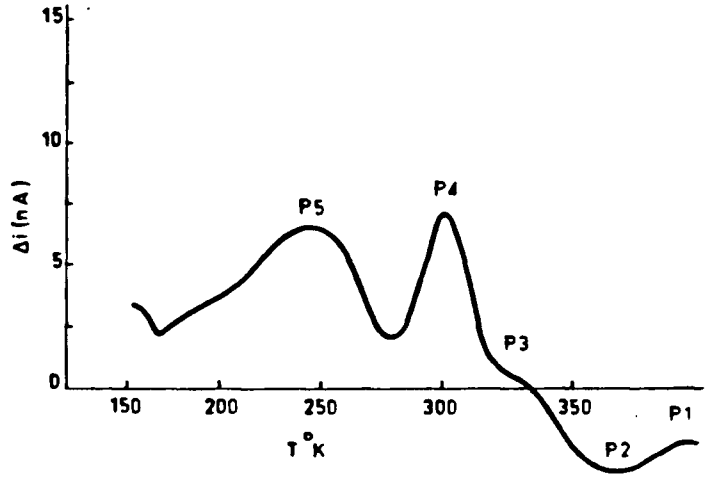


Fig. 3.4 OTCS spectra of SI undoped LEC GaAs from three vendors (Rate Window = 8.5msec)



(a) Cominco sample



(b) Sumitomo sample

Fig. 3.5 OTCS spectra of SI undoped LEC GaAs substrates from two vendors subjected to chemical etch (Rate Window = 8.5msec)

3.4.2 Identification of the Peaks

Table 3.1 shows activation energies and capture cross sections of all the OTCS peaks found in this work. Figure 3.6 shows the signature lines of the OTCS peaks. Table 3.2 shows the data on traps found by previous investigators. The peak labelled 1 was identified from its signature line in figure 3.6 by comparison with the well known compilation of data given by Martin et al. [51] as being due to the main electron trap EL2. This peak has been reported many times using various forms of DLTS on conducting material but curiously not too often for semi-insulating material. This is presumably because most authors have used Au+Ge electrodes and these, as opposed to chromium, give inconveniently high dark currents at the temperatures necessary to observe EL2.

Peak 3 and the broad peak 4 have signature lines on either side of Martin et al.'s EL12. According to Martin, Lang et al. [52] have also observed this level which is probably due to an impurity. Polarity change on the sandwich type specimen [36] gave a greater peak for negative voltage on the illuminated electrode indicating an electron trap.

The broad peak 5 is often found with another peak 6 (for example figure 3.5a). Those two peaks are closest to EL3 and EL4 respectively in Martin et al.'s DLTS data. They used capacitance DLTS [48] on conducting as-grown MBE (molecular beam epitaxy) material to obtain the level EL4. Fairman et al. [33] identified as EL4 a centre which gave one of the two negative OTCS peaks which they observed in Cr-doped semi-insulating Bridgman slices. Peak 7 is found to closely resemble Martin et al.'s EL6, while peak 8 is found to be a hole trap from polarity measurement on thin samples [36].

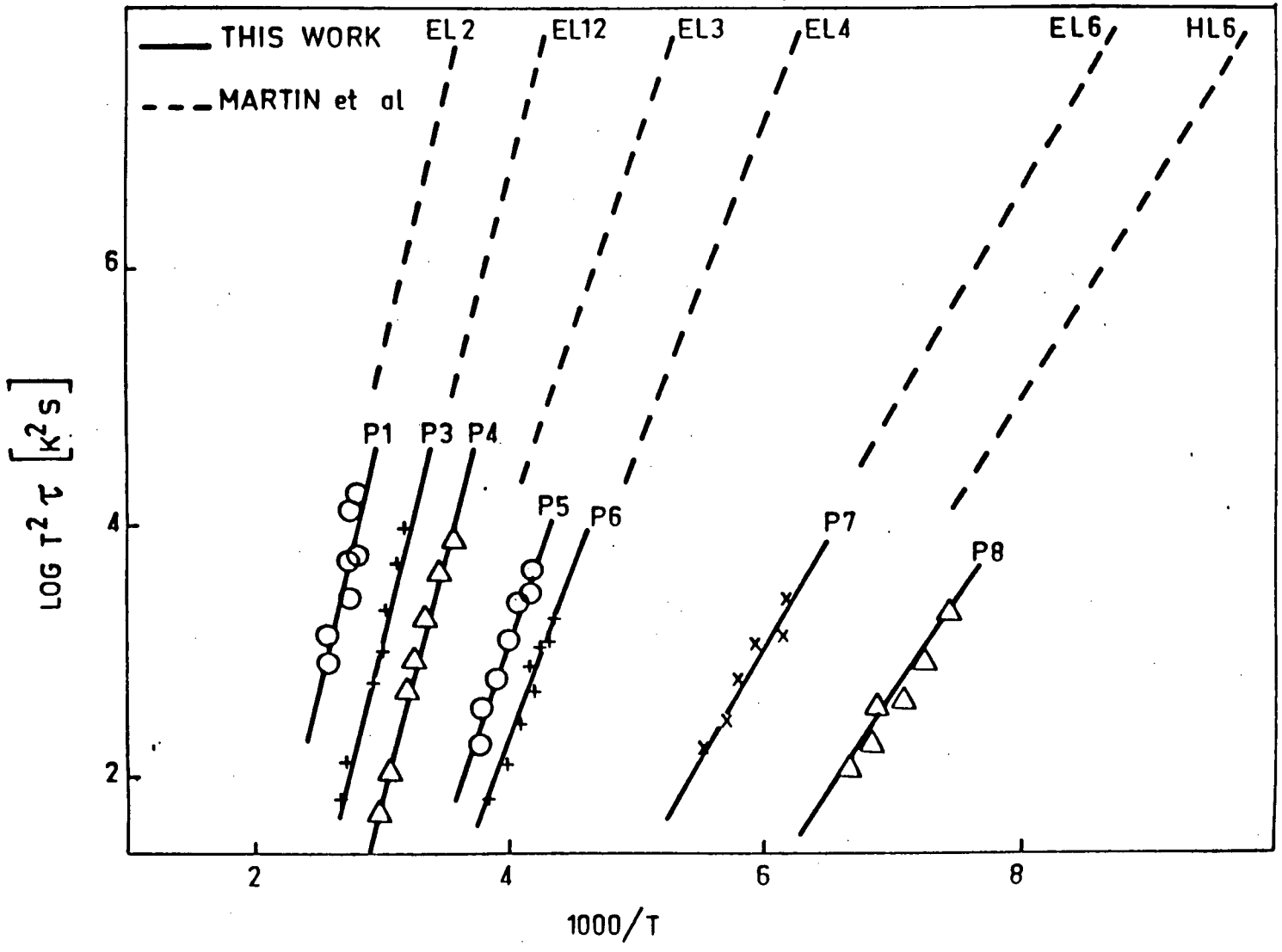


Fig. 3.6 Activation energy plots for traps detected using OTCS

Table 3.1 Activation energies, capture cross sections, and possible identities of the deep levels found using OTCS (P1-8) in semi-insulating, undoped, LEC GaAs.

label	activation energy (ev)	capture cross section (cm^2)	possible identity
P1	0.87	1.05×10^{-12}	EL2
P2	0.65	3.00×10^{-12}	negative peak
P3	0.79	3.69×10^{-12}	EL12 ?
P4	0.76	2.12×10^{-12}	EL12 ?
P5	0.59	3.46×10^{-12}	EL3 ?
P6	0.52	2.90×10^{-13}	EL4
P7	0.38	3.20×10^{-14}	EL6
P8	0.32	2.50×10^{-13}	HL6

Table 3.2 Deep levels in SI GaAs reported in the literature (as detected by OTCS (PITS)). VPE = vapour phase expitaxial layer.

Authors	W_0	$\sigma(cm^2)$	Identi-fication	Materials
Martin et al.	0.9	2.2×10^{-14}	HL1	Cr-doped Bridgman GaAs
[30]	0.74	6.3×10^{-15}	EL2	
	0.57	5.4×10^{-13}	EL3	
	0.35	5.5×10^{-15}	EL5	
	0.34	2.7×10^{-14}	EL6	
	0.27	2.05×10^{-14}	EL12	
Fairman et al.	0.9	2×10^{-14}	HL1	All*
[1,29,33]	0.83	2×10^{-13}	HL10	Cr-doped LEC GaAs
	0.65(N)**	1×10^{-13}		All*
	0.60	1×10^{-12}	EL3	Cr-doped LEC GaAs
	0.51(n)**	1×10^{-12}	EL4	Cr-doped Bridgman GaAs
	0.34	4×10^{-14}	EL6	All*
	0.34	6×10^{-13}		VPE layer on Cr-doped GaAs
	0.30	7×10^{-14}	HL12	Cr-doped LEC & Bridgman GaAs

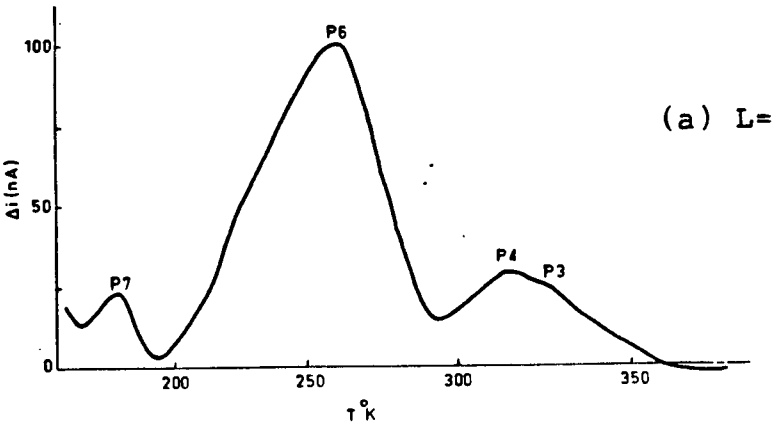
	0.26	2×10^{-12}		Cr-doped Bridgman GaAs
	0.15	8×10^{-14}		Cr-doped LEC GaAs
	0.14	1×10^{-16}		VPE layer on Cr-doped GaAs
	**negative peak			*Cr-doped LEC & Bridgman GaAs and VPE layer on Cr-doped GaAs
Deveaud et al. [32]	0.87	1.3×10^{-17}	HL1	Cr-doped Bridgman GaAs
	0.5	3×10^{-19}		
Itoh et al. [37]	0.98	1.3×10^{-13}	HL1	VPE(n-)
	0.89	1.8×10^{-14}	HL1	
	0.75	2.7×10^{-14}	EL2	
	0.62	1.5×10^{-14}	HL3	
	0.60	8.6×10^{-13}	EL3	
	0.42	Not Given		
	0.41	1.4×10^{-15}	HL4	
Rhee et al. [27]	0.90	2.1×10^{-12}		Cr-doped GaAs
	0.85	1.3×10^{-13}	HL1	
	0.73	1.3×10^{-17}		
	0.17	3.9×10^{-22}		
Oliver et al. [34]	0.83	Not Given	HL10	undoped LEC GaAs grown with dry B_2O_3

	0.65(N)			undoped LEC GaAs grown with wet B_2O_3
	0.57			undoped LEC GaAs
	0.34			
	0.28			
	0.15			
Hurtes et al. [28]	0.90	Not Given	HL1	high resistivity VPE layer on Cr-doped Bridgman
	0.81		EL2	n-VPE layer with high Cr-doped Bridgman
	0.56		HL8	high resistivity VPE buffer layer on Cr-doped Bridgman
	0.54		EL3	n-VPE layer with high resistivity buffer layer on Cr-doped Bridgman
	0.41		HL4	n-VPE layer with high resistivity buffer layer on Cr-doped Bridgman
	0.32		EL6	both type of samples

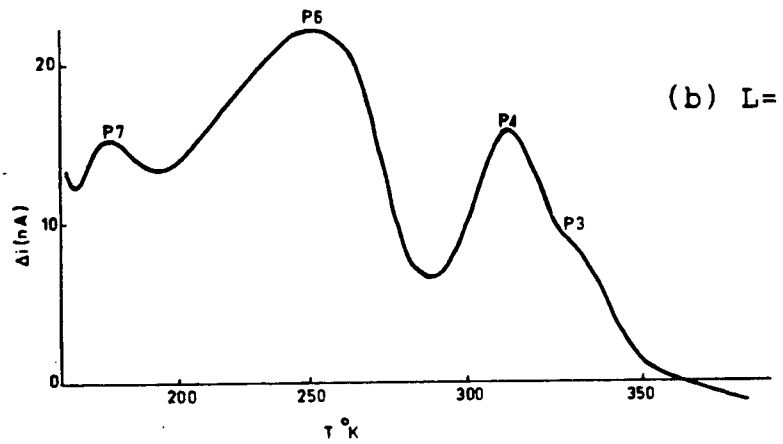
The peak labelled 2 is the negative peak and uncritical application of the equations for positive peaks gave activation energy 0.65 eV and capture cross section of 3×10^{-15} cm^2. Oliver et al. [34] found using OTCS (their PITS) a strong negative peak with planar specimens made from undoped LEC GaAs grown with wet boric oxide, but not in slices grown with dry boric oxide. They found ΔE = 0.65 eV and suggested that this level was related to oxygen impurity and was partly responsible for the semi-insulating condition (since this was enhanced when wet boric oxide was used). Fairman et al. [33] using vapor phase epitaxial layers and Cr-doped Horizontal Bridgman crystals obtained similar results with ΔE = 0.65 eV and $\sigma = 3\times10^{-13}$ cm^2. Ogawa et al. [49] also using OTCS found a minor negative peak in samples of unstated geometry using undoped LEC. In the previous paper by Itoh et al. [37] using OTCS on Cr-doped Horizontal Bridgman slices no such negative peak or even low valley is seen (their figure 4) using an ungated FET with one Au+Ge contact on n+ gate pad and the other on semi-insulating sustrate with or without a semi-insulating buffer layer.

3.4.3 Effects of Varying Sample Geometry on OTCS Spectra

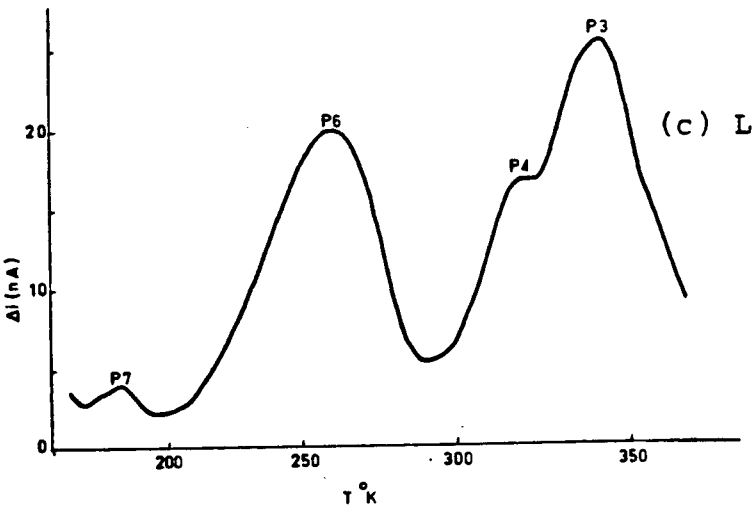
The effect of varying the contact spacing and width of the planar samples was investigated. Other authors have used varying spacings e.g. 500 um (Hurtes et al. [53]), 5 um (Fairman et al. [33]), 20 um (Itoh et al. [37]) and a little over 10 um (Rhee et al. [41]). Results of OTCS spectra for two different widths W = 300 and 600 μm and two different spacings L = 30 and 60 μm are shown in figures 3.7(a,b,c). With L = 60 μm (Figure 3.7c) the right hand peak is very pronounced where it was a mere shoulder with L = 30 um.



(a) L=30um, W=300um



(b) L=30um, W=600um



(c) L=60um, W=600um

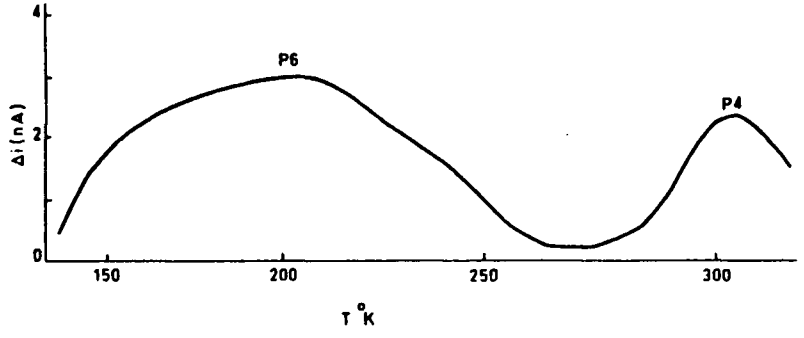
Fig. 3.7 OTCS spectra of different planar sample geometries (Rate Window = 18.9msec)

(It lies between peak 1 (not appearing at higher temperature) and peak 4.) The negative peak was even less pronounced for L = 60 um than for L = 30 um, perhaps because the positive peak which was more pronounced is close enough to interfere by giving a reduction in the net increase in current with time after illumination. Peak 4 which is the prominent peak on the two L = 30 devices, is now a mere shoulder on the 60 um device. The difference in the spectra for different geometries can be associated with the different sampling regions due to the different geometry.

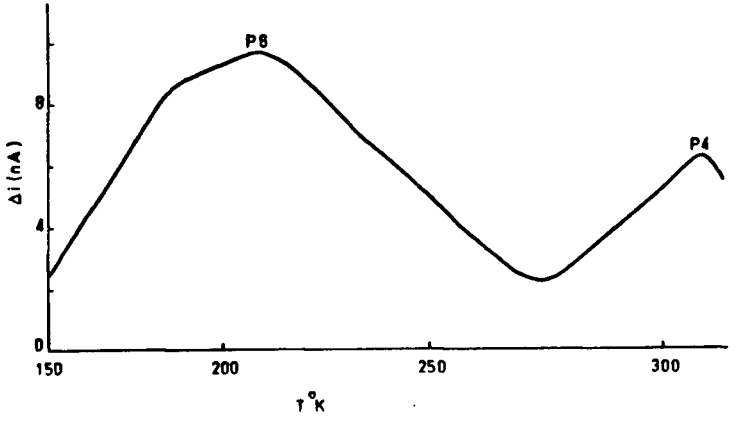
3.4.4 Effect of Varying the Electrode Material

In the first work by Hurtes et al. [28], alloyed Au+Ge electrodes were used, whereas Martin et al. [30] used chromium electrodes for his sandwich sample structures because they noted that gold-germanium electrodes gave more complicated results. In earlier work [35] in this laboratory, alloyed gold-germanium electrodes were used, and they were found to result in too large dark currents which made OTCS measurements above room temperature very difficult. In later work [36], chromium electrodes were used and resulted in reduced leakage currents.

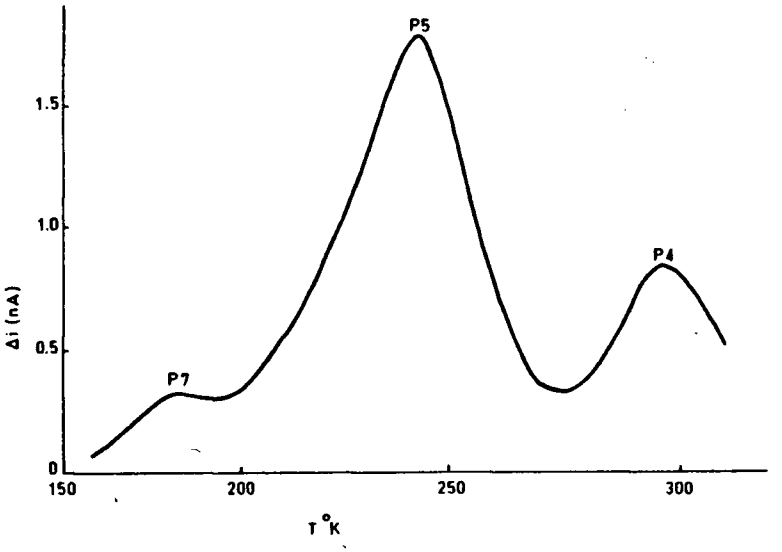
To investigate the difference in electrode material and preparation on the OTCS spectrum, four samples were prepared with two types of electrode material, Cr and Au+Ge. All devices were of planar type using a gateless MESFET structure with L = 30 um, and W = 600 um. Two samples with Cr and Au+Ge contacts were alloyed for ten minutes at 450°C. The OTCS spectra of the four devices which were made from Cominco's GaAs material are shown in Figure 3.8(a,b,c,d). The range of the OTCS scans were limited to those



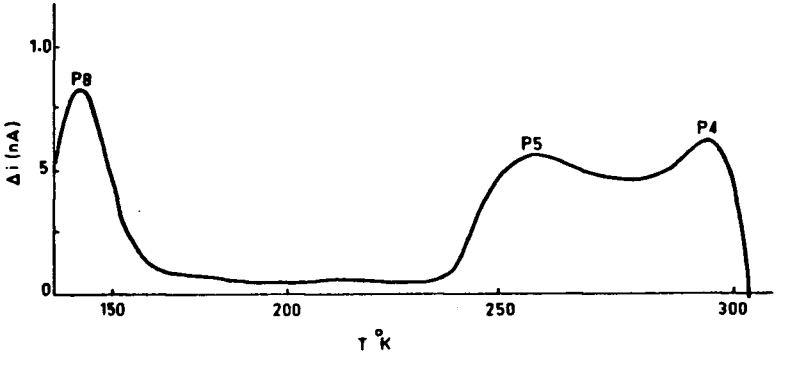
(a) Cr unalloyed electrodes



(b) Au+Ge unalloyed electrodes



(c) Cr alloyed electrodes



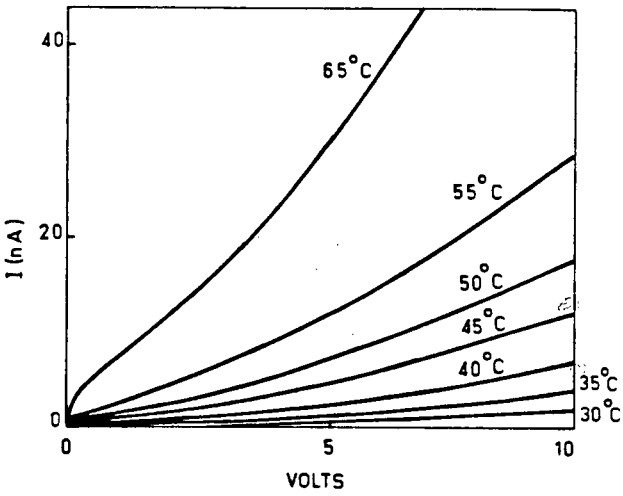
(d) Au+Ge alloyed electrodes

Fig. 3.8 OTCS spectra of samples prepared with different electrodes
(Rate Window = 38.8msec)

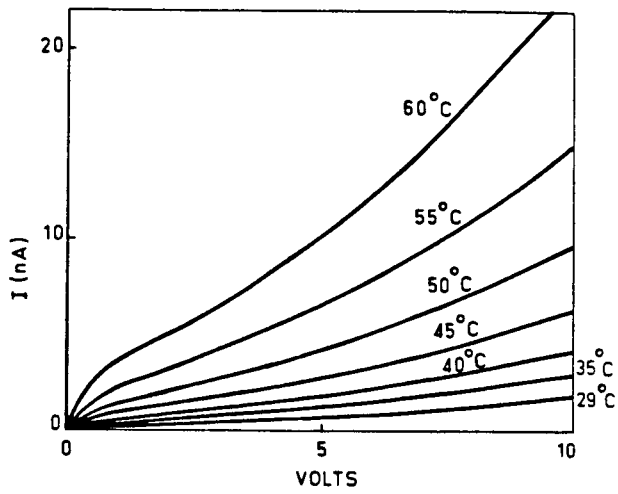
obtained for Au+Ge scans. The unalloyed Cr and Au+Ge electrodes gave the same two broad peaks but with different amplitudes. On alloying the Cr sample, the peak heights were all reduced, and the broad peak (combination of peaks 5 and 6) on the unalloyed sample, has now become distinct with peak 5 dominating. The Au+Ge specimen on alloying gave also an OTCS spectrum with some of the peaks such as, peak 6, reduced much in amplitude. In addition, the two low temperature peaks 7 and 8 amplitudes were different in both types of alloyed samples: whereas peak 7 (electron trap) remained in the Cr alloyed sample, peak 8 (hole trap) remained in the AuGe alloyed samples.

The results indicate that the deep levels are affected by the high temperature treatment upon alloying, and that the type of electrode seems to influence the results. One might also expect unalloyed Au+Ge and chromium to behave similarly, both acting as Schottky diodes. Au electrodes, used by some authors [41] would presumably be similar. On alloying the Au+Ge, the n+ layer due to Ge doping may be presumed to act as an efficient source of electrons. The heat treatment of the chromium electrodes was done for completeness and because chromium or related metal gates on MESFETs would quite normally receive the heat treatment applied to the Au+Ge source and drain electrodes.

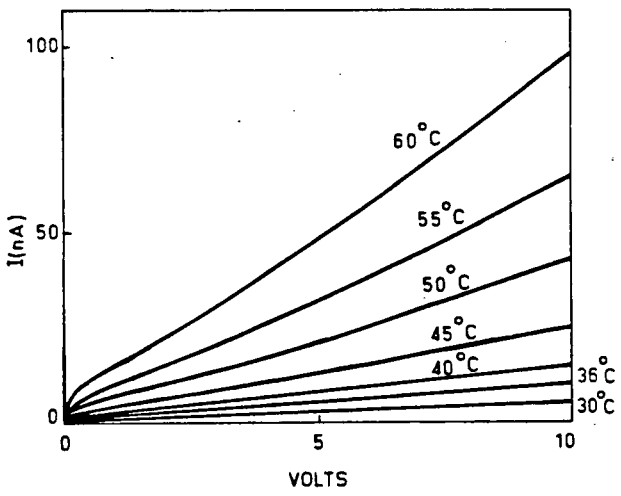
To help elucidate the effects of the nature of the contacts on the spectrum observed by OTCS, dark current vs. voltage curves were obtained using an HP 4145A semiconductor parameter analyzer. Data for Au+Ge and Cr electrodes before and after heat treatment at 450°C for 10 minutes are given in figures 3.9(a,b,c,d) for various temperatures. The current voltage curves for Cr (fig. 3.9a and 3.9c) are consistent with back to back diodes with



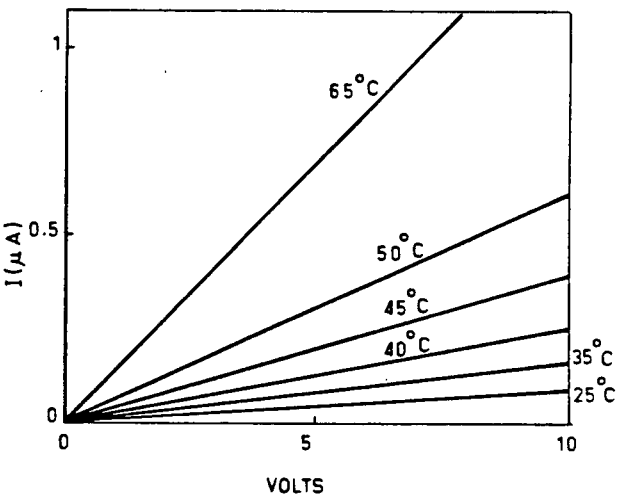
(a) Cr unalloyed electrodes



(c) Cr alloyed electrodes



(b) Au+Ge unalloyed electrodes



(d) Au+Ge alloyed electrodes

Fig. 3.9 Current vs. voltage for planar specimens with different electrodes

poorly saturating reverse current. On heat treatment the current decreased considerably. Those for Au+Ge (figure 3.9b and 3.9d) before heat treatment also appeared consistent with back to back poorly saturating diodes but still giving more current than Cr. After heat treatment the Au+Ge, the current voltage curves were fairly linear up to 0.5 uA with 10 volts between electrodes separated by 60 um. Arrhenius plots of log I_{dark} at 7 volts (as used in OTCS) vs. 1/T in figure 3.10 show the relative values of the currents and the activation energies. The slope of the data for Au+Ge changed slightly on alloying giving apparent activation energies of about 0.76 eV and 0.8 eV before and after. With chromium the slope changed from a value corresonding to 0.84 eV to one giving 0.72 eV.

3.4.5 Effect of GaAs Surface Damage on the OTCS Spectrum

Previous work by Tang [36] has revealed that the relative peak heights changed for sandwich specimens than from planar ones. In particular, he found that the negative peak was much more accentuated for the sandwich than the planar sample. The question that arises then is whether the difference between sandwich and planar specimens were due to the geometry or whether the fabrication process affected the results (since Tang prepared his thin samples by abrading it so that the surface was damaged). To investigate these factors, thin sandwich samples were prepared by mounting the wafer fragment on a silicon slice with black wax and then abrading with a slurry of 400 grade carborundum. The specimens were then removed from the silicon with hot trichloroethylene and etched briefly in the sulfuric acid and hydrogen peroxide mixture used previously. Two such thin sandwich samples were

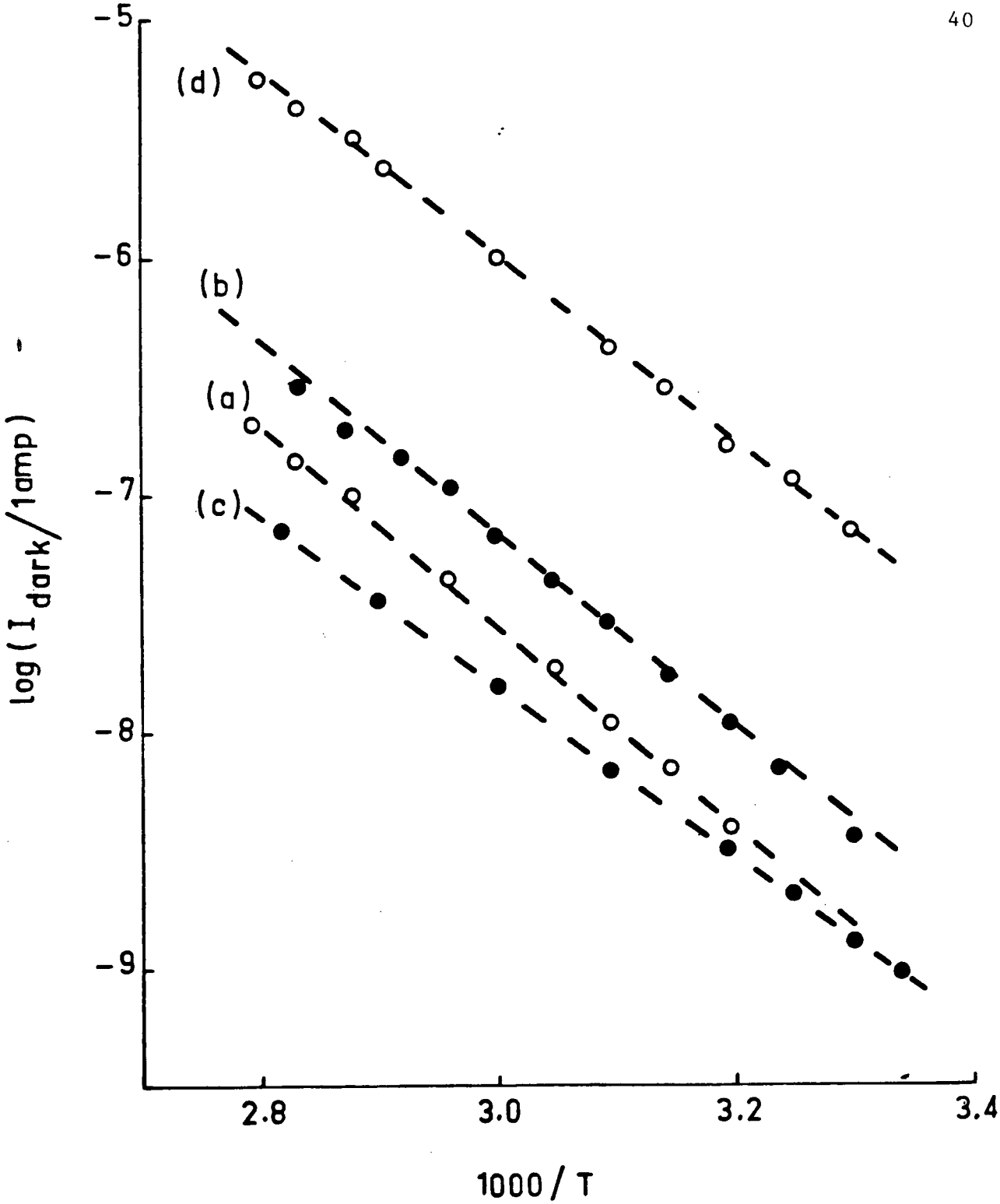
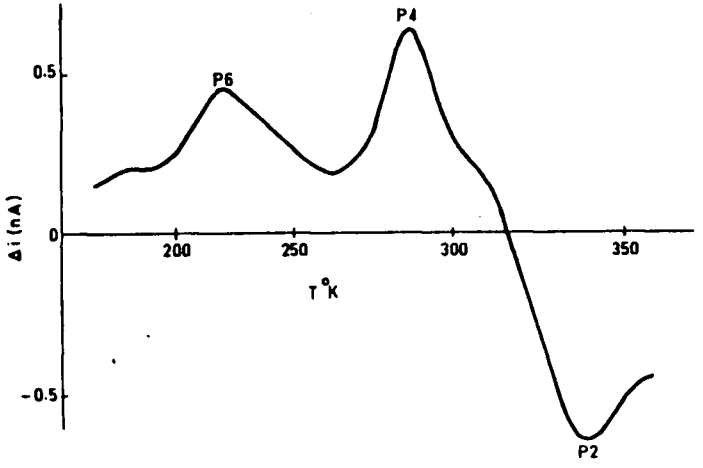
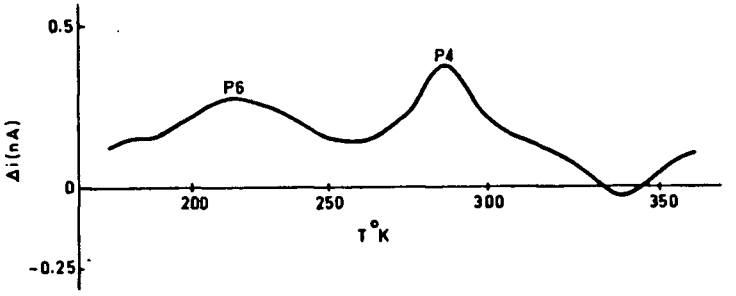


Fig. 3.10 Signature line plots for the data of figure 3.9 (Labels same as in figure 3.9)

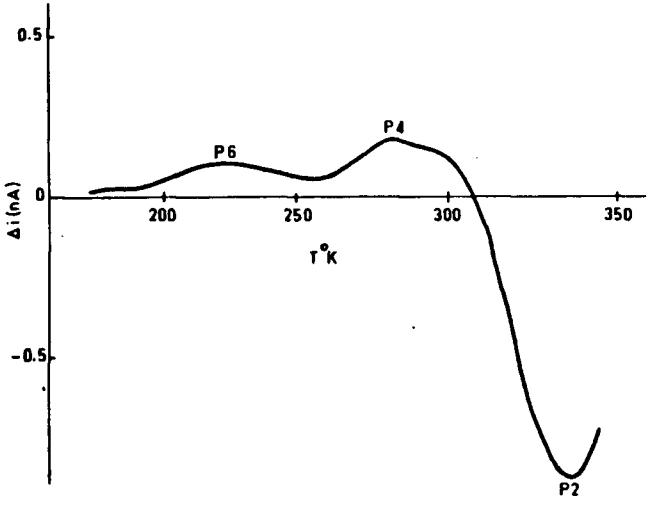
prepared with the top electrode in each case either on the abraded side or the polished side. In additon, another two thick sandwich sructures (i.e. starting wafer thickness = 450 um) were prepared where one of them was given a token grind, while the other merely degreased. The results of the OTCS spectra are shown in figure 3.11(a,b,c,d) for each of the above stated cases. In the case of the thin sandwich structures (figure 3.11a and 3.11b), for the sample where the abraded side was on top, the positive peaks were somewhat attenuated whereas the negative peak increased somewhat in amplitude compared to the sample with the polished side on top. This effect is attributed to grinding which was followed by surface etch. To demonstrate the effect of surface abrasion only (no etch), figure 3.11d shows the spectrum of the thick sandwich sample which was given a token grind. Compared to the thick sandwich structure which was merely degreased (figure 3.11c), the positive peaks were slightly attenuated whereas the negative peak has increased significantly in magnitude. To verify that the negative peak was affected by surface damage, and to investigate separately the effect of surface etch on the negative peak, a planar specimen was prepared this time. To start with, the spectrum of the sample, as is, (i.e. with no etching or grinding) was recorded as shown in figure 3.12a. The same sample was then etched by about 1 um using a mixture of sulfuric acid, hydrogen peroxide, and water (4:1:1) by volume). The OTCS spectrum indicated no difference (shown in circles in figure 3.12a). The sample was then lightly abraded using a carborundum slurry. The negative peak, figure 3.12b, was significantly accentuated. The sample showed almost the same starting OTCS spectrum, figure 3.12c, after the sample was etched. From these findings it can be concluded that the negative



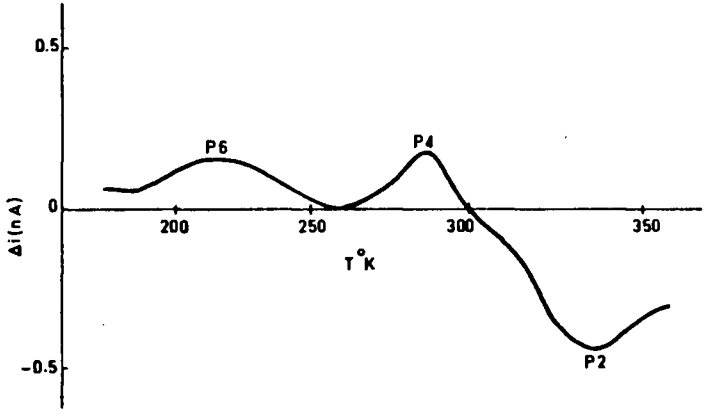
(a) unabraded side on top, thickness = 120um



(c) unabraded side on top, thickness = 500um



(b) abraded side on top, thickness = 120um



(d) abraded side on top, thickness = 500um

Fig. 3.11 OTCS spectra of sandwich structures with a negative bias on the top illuminated electrode (Rate Window = 75.5msec)

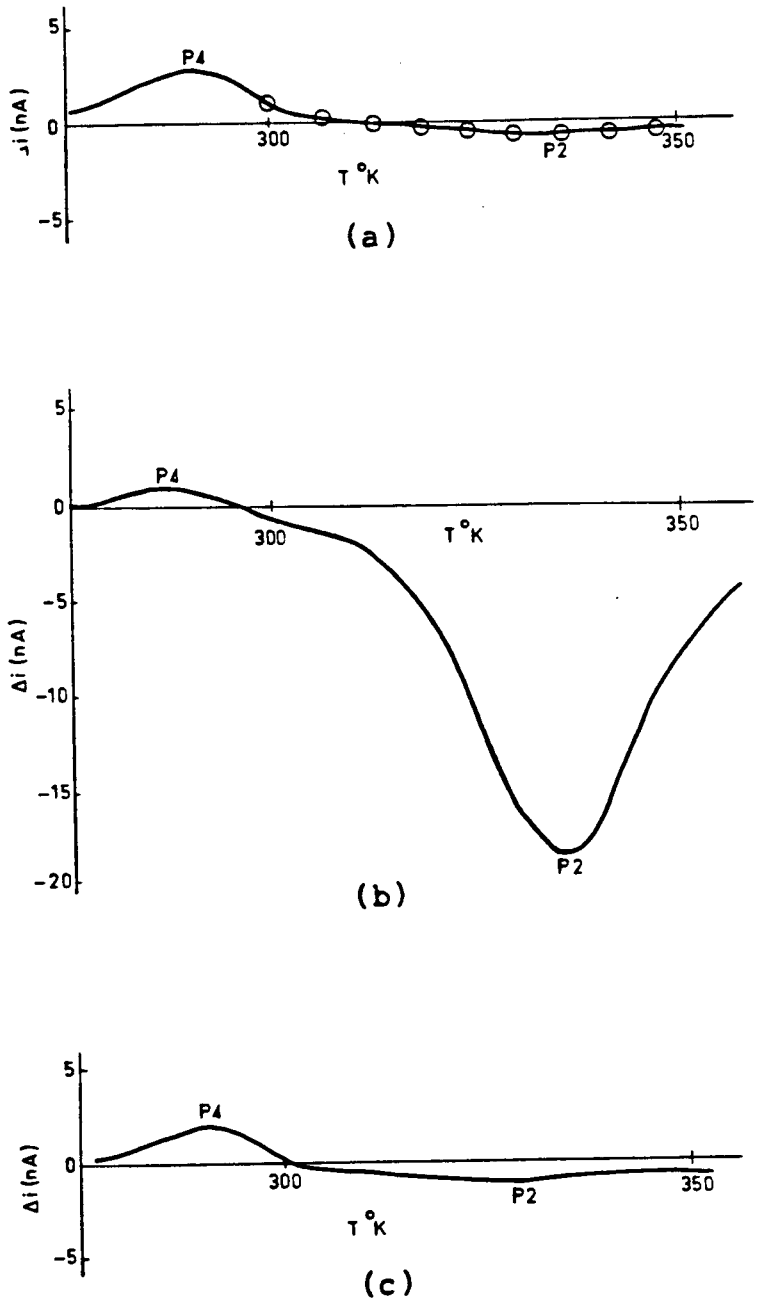


Fig. 3.12 OTCS spectra of a planar structure (a) before and after chemical etch (b) after light abrasion (c) after chemical etch (Rate Window = 75.5msec)

peak is associated with the damage done to GaAs by the abrasion process.

3.5 Summary

From the above study, it was shown that the OTCS technique is a useful tool for the evaluation of GaAs material. The OTCS spectra were shown to be different for high and low pressure LEC grown GaAs. Some of the peaks were found to be dependent on the surface condition, as it was shown that the concentration of some of the deep levels were attenuated after the top surface layer was removed. The nature of the OTCS spectrum was found to be influenced by the electrodes, sample geometry, and fabrication method. Finally, surface damage was shown to affect the negative peak.

Before this chapter is concluded, it is useful to point out that the theory of OTCS based on the depletion layer model of Hurtes [28] (described in section 3.2) may not be totally applicable for the study of transients. For example in the case of transients resulting from a sandwich structure, the depletion layer will be confined to a small depth below the surface, while the bulk remains undepleted. Other models are now available [50] which provide for possible alternative description of the observed transients.

CHAPTER 4

INVESTIGATION OF PROCESS-INDUCED DEEP LEVELS IN ION IMPLANTED MESFETs

4.1 Introduction

Despite the recent advances which have been made in the field of MESFETs IC technology, there are still many problems concerning the stability of such devices due to the presence of deep level defects and impurities both those initially present in the substrate material and those induced by the fabrication process. It has been widely reported [5,54-59] that traps in the MESFET channel and in particular those at the interface of the channel and the semi-insulating substrate can cause such effects as looping in the drain I-V characteristics, low transconductance at saturation, low drain-source breakdown, low power gain, and large noise figures. Those effects were found in particular for active layers made by epitaxial growth over chromium doped gallium arsenide substrates because chromium tended to react with the active layer and form hole traps which contribute to the formation of an interface space charge region which in turn affect the channel width [59]. To isolate the active layer from the substrate, high purity epitaxial buffer layers were used to keep the deep levels in the substrate from diffusing into the MESFET channel. However, it was found [60] that for all buffer layer thicknesses (1-3 μm), chromium, copper, and iron still were able to diffuse and resulted in a large number of deep levels at the active layer and buffer (A/B) interface.

Some of the problems with deep trapping levels in epitaxial layers and

at the A/B interface are no longer present in the case of ion implantation in undoped LEC GaAs substrates. Nevertheless, the problems of the newer technology still include those due to the presence of the many impurities [33,8] in undoped LEC GaAs substrates, and due to defects either present in the starting material or induced by the process steps. Process-induced defects in MESFET channels arise from several factors: (1) irradiation damage due to silicon ion implantation (used as n-type dopants), and whether the implantation was done directly into the surface or through a thin dielectric film; (2) the high temperature annealing stage required to remove the implantation damage and allow silicon to reach vacant gallium sites; (3) the type of encapsulant used; and (4) the chemical treatment of the surface. Of those factors, the first factor is important, since implants through silicon dioxide or silicon nitride can introduce unwanted atoms such as oxygen and nitrogen into the active layer by knock-on mechanisms [61] inducing serious defects. Also, the type of encapsulant which is used to preserve the GaAs stoichiometry during high temperature anneal is important. Studies have shown [62] that the implanted atoms redistribute by diffusion more with a silicon dioxide than a silicon nitride cap. Also, the silicon dioxide encapsulant does not preserve the substrates stoichiometry as well as silicon nitride since it is known that gallium can diffuse through the silicon dioxide. Problems of enhanced diffusion of defects are also caused by the encapsulants as a result of stresses due to thermal expansion mismatch between the dielectric cap and GaAs.

There is an extensive literature on electron and hole deep levels in GaAs [63] and on their effects on device characteristics. Recent papers

specifically on deep levels in ion implanted undoped semi-insulating GaAs include Sriram et al. [64,65], Rhee et al. [41,66] and Hickmott [45]. In this chapter, deep levels in silicon implanted MESFETS fabricated by four procedures are investigated by channel current DLTS. The four cases include effects of implants directly into GaAs and through silicon nitrde film, and also effects of three types of encapsulants.

4.2 Principle of Channel Current DLTS

Channel current DLTS is a technique which allows the investigation of the deep level traps in ion implanted MESFET channels. The principle is illustrated in figure 4.1. A small bias (50 mV DC) is applied between the drain and source so that the FET operates in the linear region. A reverse bias voltage is placed on the gate such that the channel is nearly pinched off. Pulses of voltage taking the gate to near zero bias are applied. The basic idea is that majority carrier traps are filled by carriers which are allowed to enter the previously depleted channel during the positive going voltage pulse. When the gate voltage returns to its more negative value the negative charge due to the trapped electrons partially compensates the positive space charge density in the depleted region. To maintain the fixed voltage drop across the region it must therefore become initially wider than before. The channel is therefore narrowed and the drain current is less. As the occupancy returns to normal the drain current increases (with the time constant depopulation emission process) as illustrated in figure 4.2. Hole traps give the reverse sign of effect (the hole trap occupancy can be changed because the quasi Fermi level for holes communicates with the gate Fermi

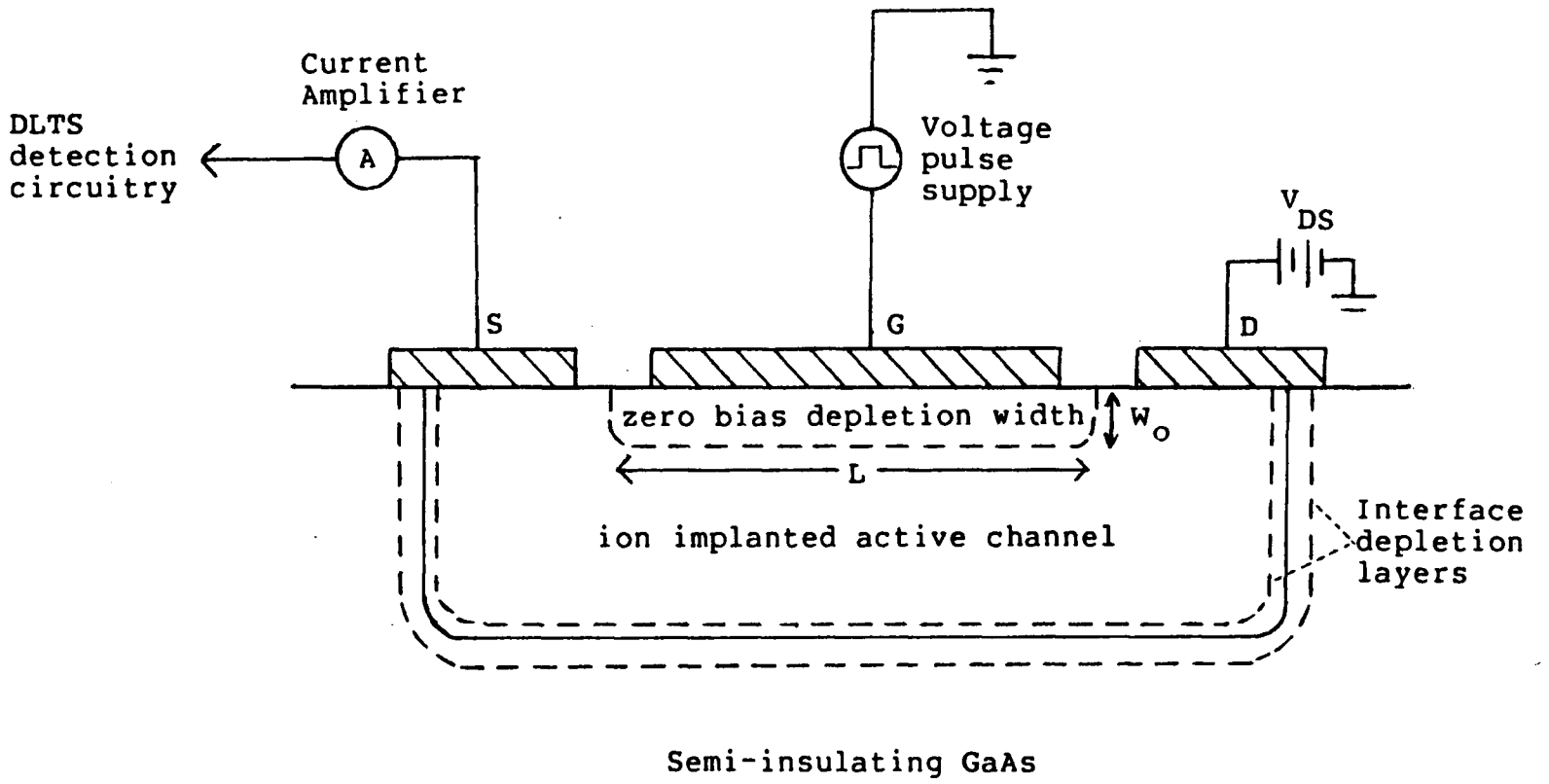


Fig. 4.1 Schematic diagram showing the channel current DLTS measurement system

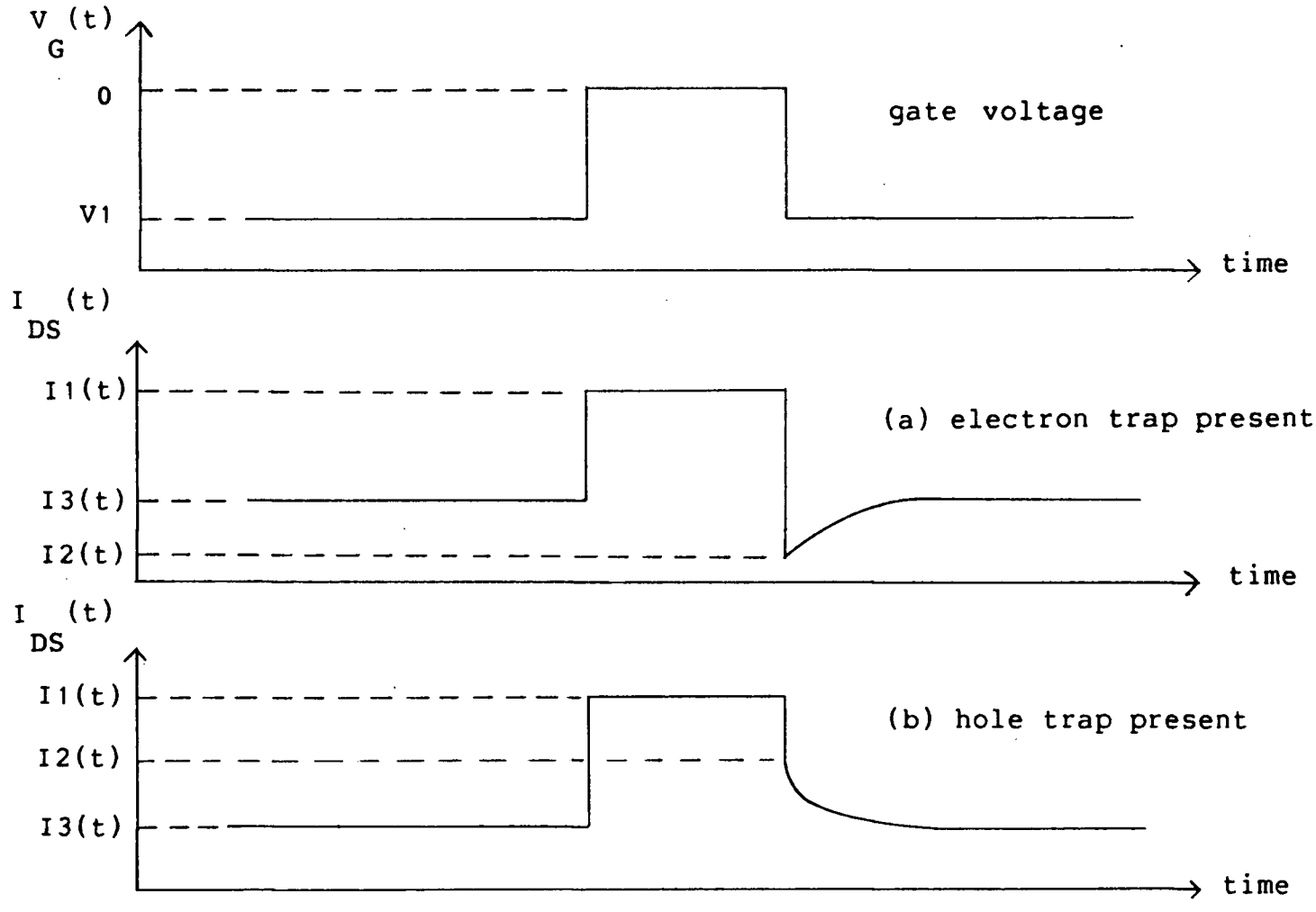


Fig. 4.2 Transient responses of the drain current to an applied gate voltage

level).

The depletion width which is modulated by the traps is obtained for any time t after the lapse of the zero bias pulse [64] as:

$$\Delta W(t) = W_\infty - W(t)$$

$$\Delta W(t) = \frac{- N_T}{2 W_\infty N_D|_\infty} \left(W^2_\infty - W^2_o\right) \exp(-e_n t) \qquad (4.1A)$$

for an electron trap. The corresponding expression for a hole trap:

$$\Delta W(t) = \frac{+ N_T}{2 W_\infty N_D|_\infty} \left(W^2_\infty - W^2_o\right) \exp(-e_p t) \qquad (4.1B)$$

where N_T is the total concentration of the trap, $N_D|_\infty$ is the donor level density at steady state depletion width, W_o and W_∞ are the depletion widths at zero gate and steady state depletion widths respectively.

The channel current for an arbitrary doping profile is:

$$I_{DS} = \int_{w_0}^{k} \left(q\ u(x)\ n(x)\right) \left(Z/L\right) V_{DS}\ dx \qquad (4.2)$$

where u(x) is the drift mobility in the channel, n(x) is the free carrier concentration, Z is the channel width, L is the effective channel length, and k is the channel thickness. For a small change in depletion width, (4.2)

becomes:

$$\Delta I_{DS} = (q\ u(x)\ n(x))\ (Z/L)V_{DS}\ \Delta W \tag{4.3}$$

This expression can be combined with (4.1A) to obtain the transient current equation for an electron trap:

$$\Delta I_{DS} = \frac{-(q\ u(x))|_{W_\infty}}{2W_\infty} (Z/L)V_{DS}\ N_T\ (W_\infty - W_o^2)\ \exp(-e_n t) \tag{4.4A}$$

The corresponding expression for a hole trap:

$$\Delta I_{DS} = \frac{(q\ u(x))|_{W_\infty}}{2W_\infty} (Z/L)V_{DS}\ N_T\ (W_\infty - W_o^2)\ \exp(-e_p t) \tag{4.4B}$$

The current is sampled at two time instants, t_1 and t_2 by the boxcar averager which gives an output:

$$v_0(t) = A_B R\ (I_{DS}(t_1) - I_{DS}(t_2)) \tag{4.5}$$

where A_B is the amplification of the boxcar, and R is the current to voltage conversion factor in the current amplifier. Utilizing the expressions in equation (4.4A), the output current becomes:

$$v_0(t) = - A_B R \frac{(q\ u(x))|w_\infty}{2W_\infty} (Z/L) V_{DS}\ N_T\ (W_\infty^2 - W_o^2) \cdot$$
$$(\exp(-t_1/\tau) - \exp(-t_2/\tau) \qquad (4.6)$$

The information about the traps is obtained by the DLTS circuitry as in section 3.2. The trap activation energy and capture cross section are obtained by plotting $(T^2_m \tau)$ vs. $(1000/T_m)$, where T_m is the characteristic temperature of the peak in the DLTS spectrum. The boxcar rate window in the case of channel current DLTS is obtained by differentiating (4.6) with respect to τ, setting the result to zero, and solving for τ_m:

$$\tau_m = 1/e_n = (t_1 - t_2) \ / \ \ln(t_1/t_2) \qquad (4.7)$$

Unlike OTCS, positive peaks in channel DLTS correspond to hole traps, while negative peaks indicate electron traps. This technique is therefore unambiguous with respect to the type of the deep level. Also, in contrast to OTCS where the concentration of the traps are difficult to obtain because not all the levels are occupied during optical excitation, the concentration of traps in channel current DLTS can be estimated since during electrical excitation all the deep levels in the sampled region undergo periodical filling and emptying. The concentration can be estimated by solving for N_T in equation (4.6).

4.3 Experimental Procedure

Four sets of long channel devices ("Fat FETs") were used for channel

current DLTS, each fabricated using a different procedure. Substrates from the following ingots of Cominco were used: #43, #51, #123, #175 and #344. The first set of fat FETs were fabricated by Lowe [35] with a gate length of 100 um and a gate width of 200 um. The channel was implated with 3×10^{12} cm^{-3} ^{28}Si at 100 keV directly into the GaAs surface. A 600 nm RF sputtered silicon dioxide mask was used to block the silicon implant where isolation was needed. The implant damage was furnace annealed at 850°C for 20 minutes using a 170 nm RF sputtered silicon dioxide as an encapsulant.

The second set of fat FET's (L = 120 um, W = 180 um) were implanted with 3.38×10^{12} cm^{-2} using ^{28}Si at 125 keV through a 40 nm layer of PECVD silicon nitride film. A Photoresist mask was used for selective ion implantation. The dielectric film was laid down in a Plasmatherm Inc. Multiversion machine with NH_3 and SiH_4 in He. The film was thickened to 80 nm before furnace anneal at 850°C for 25 minutes.

The third set of MESFETs had identical geometry to that of set 2. The channel was implanted with ^{28}Si directly into the GaAs surface at 100 keV with a dose of 2.25×10^{12} cm^{-2}. The devices were annealed identically to set 2, using an 80 nm PECVD silicon nitride films.

The fourth and final set of devices were supplied by Allied Bendix Aerospace Corporation. The fat FETs (L = 200 um, W = 200 um) were implanted with 3×10^{12} cm^{-2} of ^{29}Si at 60 keV directly into the GaAs surface. The wafer was furnace annealed at 850°C for 15 minutes under 250 nm PECVD silicon dioxide. The GaAs was reported to have been obtained from Cominco Ltd.

The source and drain of the all the devices were Au+Ge alloyed at 450°C, while the gates were aluminum. The experimental setup for channel

current DLTS shown in figure 4.3 is similar to the OTCS setup described previously.

4.4 Results

Channel current DLTS spectra are given in figures 4.4-4.7 for MESFETs made using the four processes described above. Arrhenius plots are given in figures 4.8 and 4.9 for the channel current DLTS peaks. Table 4.1 summarizes the DLTS data.

The two sets of devices made with RF sputtered and PECVD silicon dioxide cap (processes I and IV respectively) each gave four peaks corresponding to four defects. The resulting traps were different. In process IV, two of the peaks were hole traps (T2 and T4), while the other two were electron traps (T1 and T3). Since none of them were found in the starting material by OTCS (table 3.1) the four traps were thus likely to be process induced. The two hole traps may have originated from metal impurity diffusion from the substrate into the active layer during high temperature anneal.

In process I, with an RF sputtered silicon dioxide cap, the peaks were all electron traps. Two of these peaks, Q1 and Q2 are the same as the two peaks P4 and P5 found in the starting material by OTCS (table 3.1), and they are probably to be identified on the basis of activation energy with EL12 and EL3 respectively found by Martin et al. [48]. The other two peaks Q3 and Q4 were not observed in the starting material and are, therefore, process-induced defects.

For devices implanted directly into GaAs and annealed under PECVD

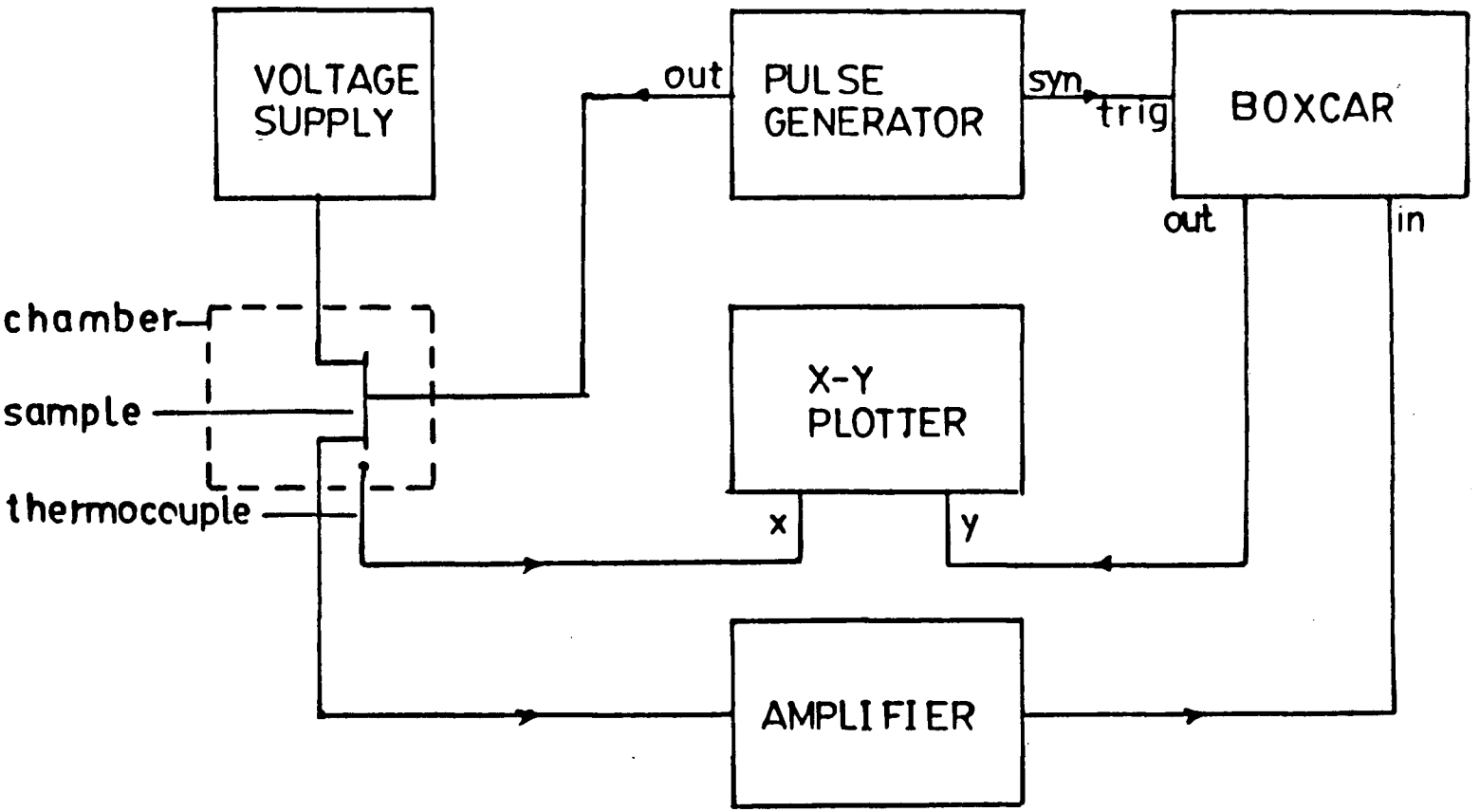


Fig. 4.3 Block diagram of channel current DLTS system

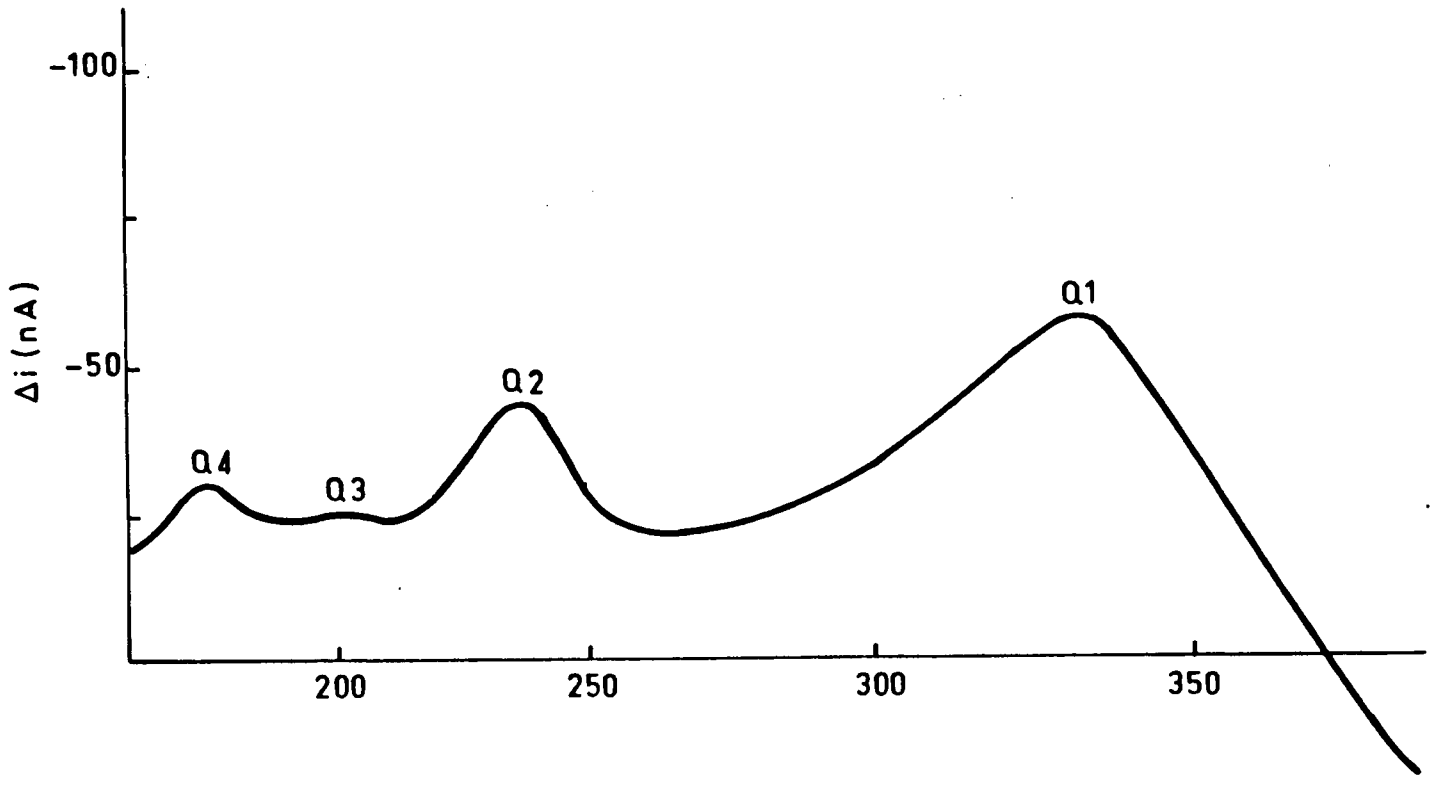


Fig. 4.4 Channel current DLTS spectrum for MESFETs prepared using process I

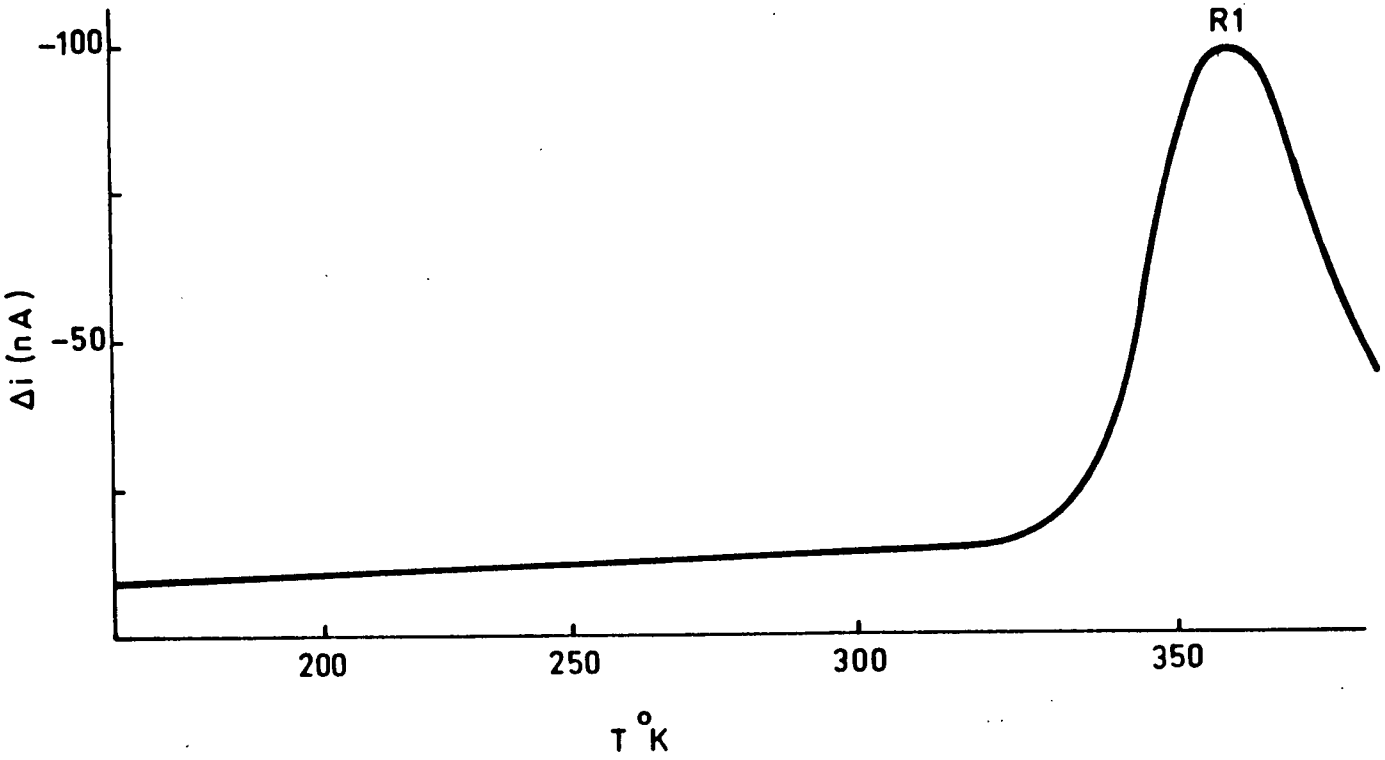


Fig. 4.5 Channel current DLTS spectrum for MESFETs prepared using process II

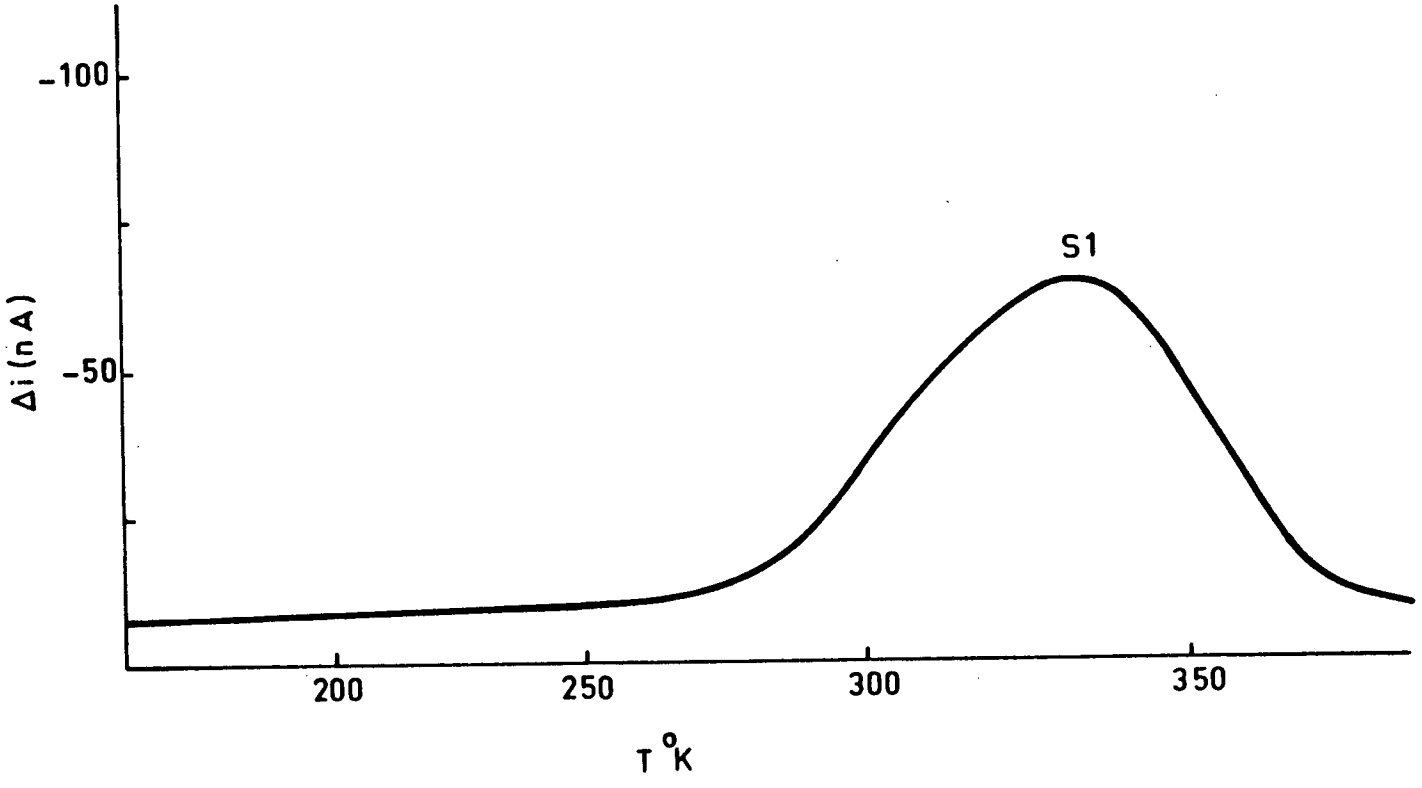


Fig. 4.6 Channel current DLTS spectrum for MESFETs prepared using process III

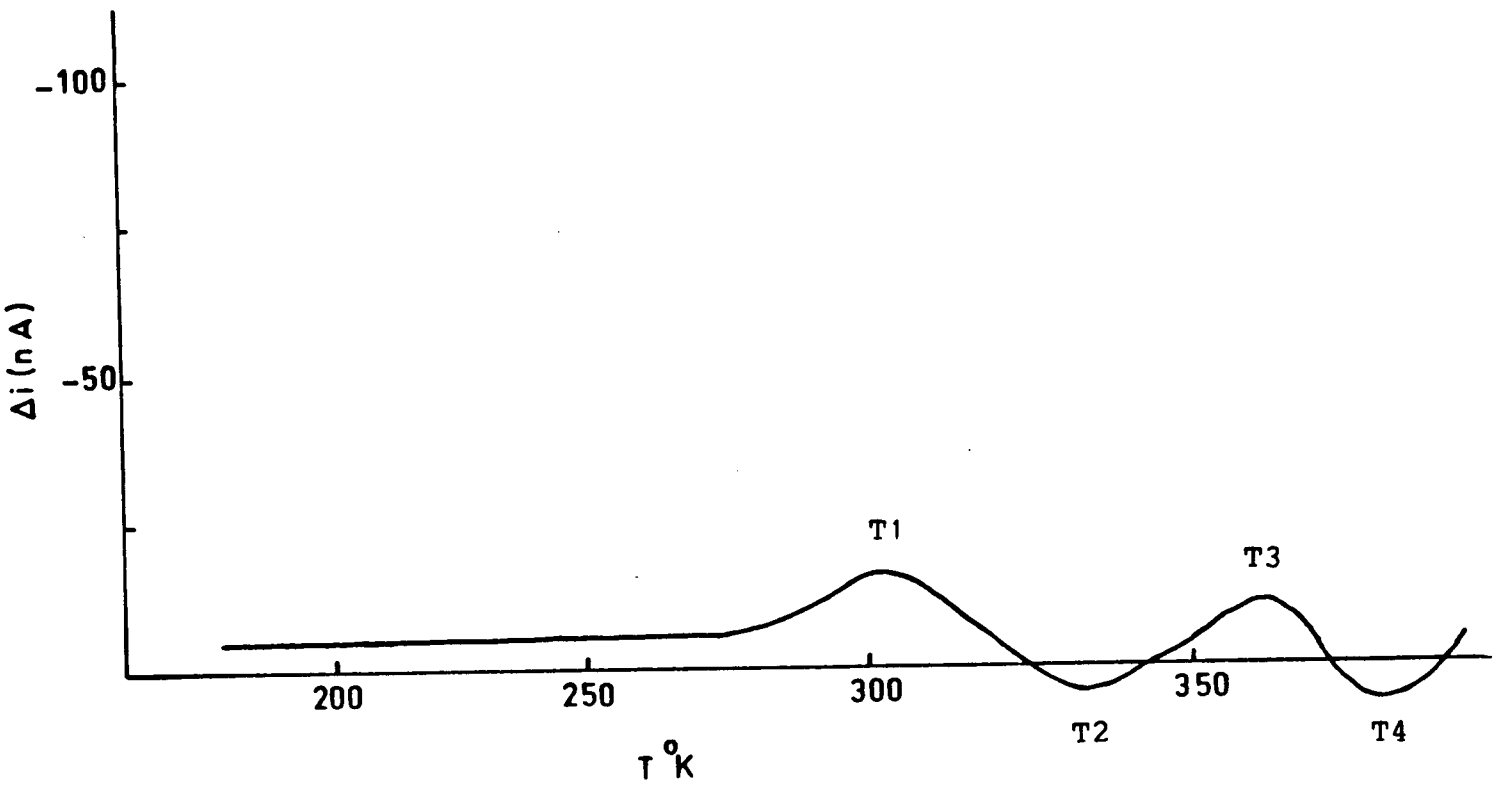


Fig. 4.7 Channel current DLTS spectrum for MESFETs prepared using process IV

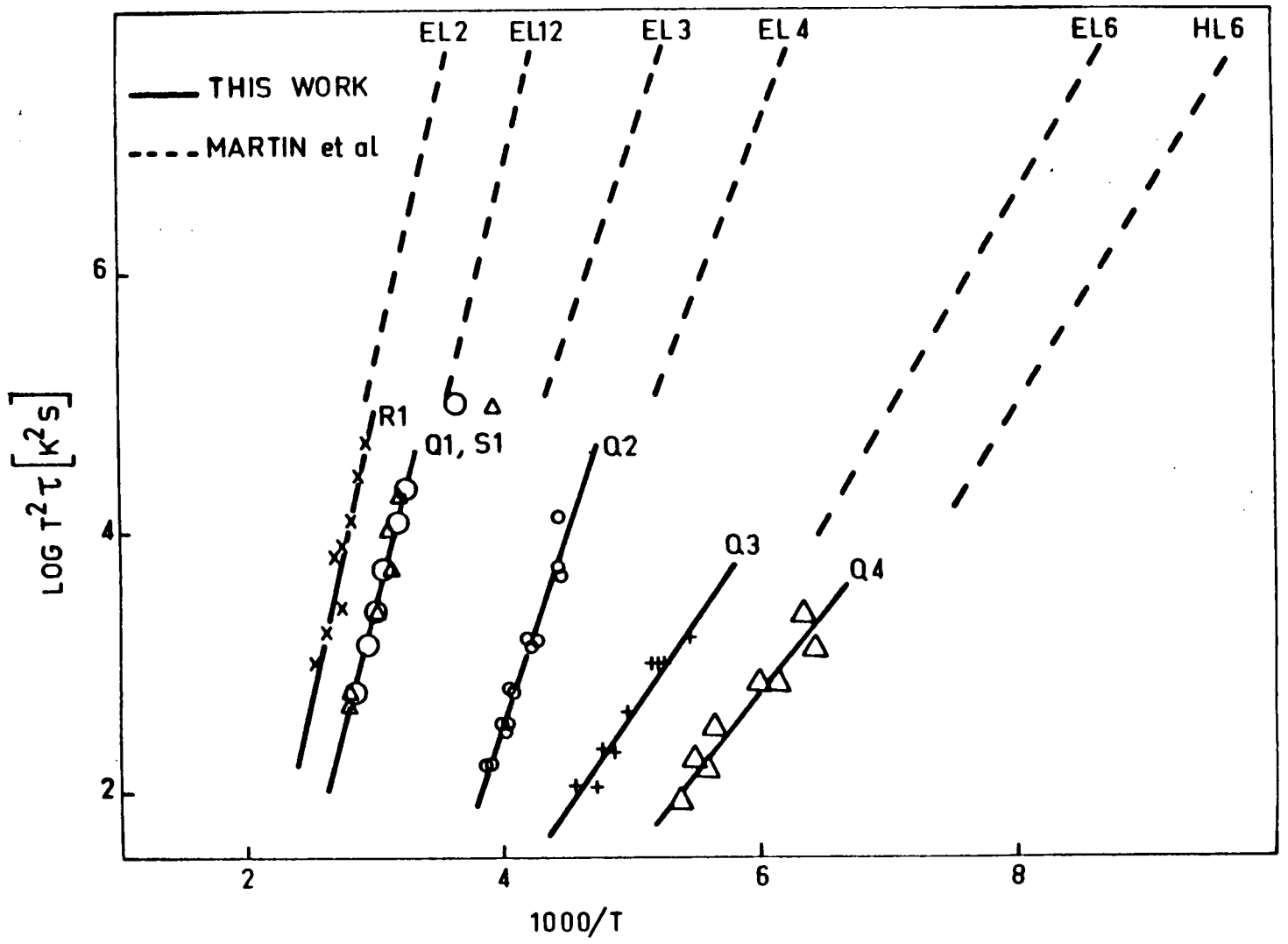


Fig. 4.8 Signature line plots for DLTS data of processes I-III

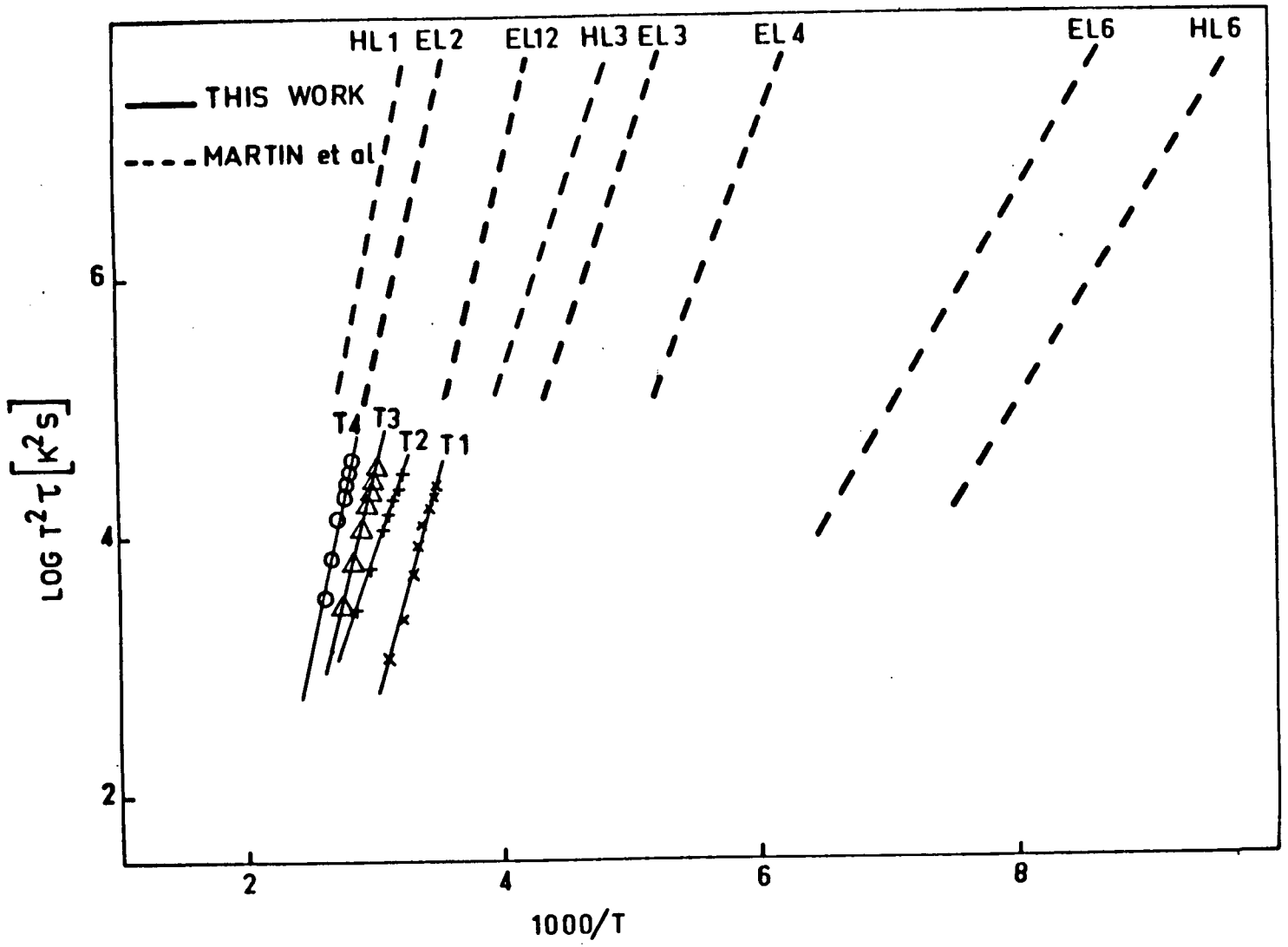


Fig. 4.9 Signature line plots for DLTS data of process IV

Table 4.1 Activation energies, capture cross sections, and possible identities of the deep levels found by channel current DLTS in MESFETs fabricated by four processes (Q1-4,R1,S1,T1-T4).

label	activation energy (ev)	capture cross section (cm^2)	possible identity
Q1	0.74	2.67×10^{-13}	P4 and EL12
Q2	0.57	4.47×10^{-12}	P5 and EL3
Q3	0.28	1.66×10^{-16}	-
Q4	0.24	1.45×10^{-16}	-
R1	0.85	4.30×10^{-13}	P1 and EL2
S1	0.74	2.10×10^{-13}	
T1	0.69	2.3×10^{-12}	electron trap
T2	0.57	3.44×10^{-17}	hole trap
T3	0.78	1.015×10^{-13}	electron trap
T4	0.911	1.55×10^{-13}	hole trap

silicon nitride cap (process III) only one peak, S1 (ΔE = 0.74 eV), was found. This peak was observed in the starting material by OTCS as P4 and is believed to be EL12. For devices implanted through PECVD silicon nitride (process II) only R1 (ΔE = 0.85 eV) was observed. This peak was found by OTCS as P1 and is Martin et al.'s [48] EL2.

Relating these results to previous work (table 4.2), Sriram et al. [64,65] used devices with silicon implanted directly into semi-insulating undoped LEC GaAs at doses of 2 to 5.5×10^{12} cm^{-2} at 100 to 325 keV and annealed at 860°C under "phosphorus silicate" glass. Using channel current DLTS, they found six levels of which three were process-induced. Their defect A is probably our level Q4. Rhee and Bhattacharya [41] implanted silicon directly into Cr-doped semi-insulating LEC GaAs at does of 10^{12} and 10^{13} cm^{-2} at 100 keV and annealed under silox cap. They found three electron traps of which one was present in their starting material. In a further paper [66] they found two dominant levels (0.52 eV electron trap and an 0.15 eV hole trap) in directly implanted material, these centres being absent on implantation through Silox. Jervis et al. [67] compared the traps produced by implantation (a) direct and (b) through silicon nitride into epitaxial and chromium doped semi-insulating wafers (probably Bridgman). They annealed under silicon nitride. Using capacitance DLTS with both electrical and optical excitation, they found an increase in EL2 on implanting through silicon nitride.

As regards a mechanism to account for the extra EL2 found in devices made by process II, it is suggested that when implantation is done through silicon nitride, knocked-on nitrogen atoms [68] compete with displaced

Table 4.2 Some deep levels in silicon implanted GaAs reported in the literature.

label	activation energy (ev)	capture cross section (cm^2)	possible identity (reference)
A	0.23	1.90×10^{-17}	unknown [64]
B	0.22	1.17×10^{-15}	EL14
C	0.53	1.60×10^{-12}	EL4
D	0.85	1.00×10^{-9}	New
E	0.64	5.90×10^{-14}	Cr complex
F	0.75	1.50×10^{-14}	EL2
A	0.52 ± 0.01	$(1.20\text{-}1.60) \times 10^{-18}$	[41]
B	0.17 ± 0.01	$(5.20\text{-}5.50) \times 10^{-23}$	
C	0.21	3.10×10^{-21}	
EB2	0.83	2.20×10^{-13}	EL2 [67]
EB3	0.90	3.00×10^{-11}	
EB4	0.71	8.30×10^{-13}	
EB7	0.30	1.70×10^{-14}	
EB6	0.41	2.60×10^{-13}	

arsenic atoms for vacant arsenic sites (since both nitrogen and arsenic belong to group 5 elements). The pre-empted arsenic atoms could adopt vacant arsenic sites to produce As which is, or is associated with, EL2.

With silicon dioxide as encapsulant, the loss of gallium is to be expected to have some effect on the type of defects produced. Perhaps occupation of the vacant gallium sites by impurities from the silicon dioxide film or from metal traces in the substrate is responsible for the process-induced hole and electron traps. One of the traps, P4 or EL12, is probably associated to gallium vacancy concentration since it was present in processes I and III (under silicon dioxide and silicon nitrde caps) but not in process II (implanted through silicon nitride) where gallium vacancy was reduced due to the formation of the anti-site defect.

To summarize the main results:

1. The number and nature of deep levels are influenced by the type of the annealing cap. Annealing with a silicon nitride cap is observed to remove all but one defect in the starting substrate and does not cause process-induced levels. Annealing under a silicon dioxide cap leads to the formation of several process-induced traps which give detrimental effects on the devices characteristics.

2. For a different encapsulant, for example, RF sputtered and PECVD silicon dioxide, the resulting number and nature of deep levels are different.

3. For implantation through silicon nitride, the channel was found to contain a larger concentration of EL2. This trap is undesirable in MESFETs since it can cause drift in the DC characteristics.

CHAPTER 5

INFLUENCE OF VARIOUS LEC UNDOPED GaAs SUBSTRATES ON THE CHARACTERISTICS OF ION IMPLANTED AND ANNEALED ACTIVE LAYERS

5.1 Introduction

With the emergence of advanced GaAs integrated circuit technologies, stringent demands are placed on the GaAs material in order to make high quality devices reproducibly. The advantages of ion implantation into bulk material over the use of epitaxial technology lie in the ability to form planar device structures easily by selective doping [69], precise tailoring of the implant profile [70], and cost effectiveness. However, the influence of the bulk grown substrate material on the properties and characteristics of the ion implanted and annealed active layers remains a major concern.

It is known that GaAs substrates can influence the active layer performance in several ways, such as: (1) variations in activation efficiency, mobility, and doping profiles which in turn produce variations in pinchoff voltage and drain current [71-75]; (2) degraded drift mobility at the active layer-substrate interface due to traps caused by impurities [15] has adverse effects on transconductance and noise figure; (3) backgating (and sidegating) effect [72,76] can severely limit circuit performance; (4) problems with surface conversion and thermal instability of GaAs are due to improper compensation [77]. These substrate-related problems have prompted the use of qualification tests or pre-screening of substrates for ion implantation.

Suppliers of substrate materials check their material through measurement of substrate resistivity, Hall mobility, and thermal stability, and quality control checks involving device fabrication for GaAs substrates are largely performed by the device manufacturers [78]. Typical qualification tests of GaAs substrates require [33] (1) reproducibly high resistance substrates which can withstand high temperature (850°C) anneal without surface conversion; (2) low background doping compared to shallow donor and acceptor impurities; (3) high electrical activation and carrier mobility with abrupt doping profiles for bare surface n-type implants; and (4) low dislocation and defect densities. One test [70] which has been used to qualify substrates involves ion implantation with an inert gas such as argon to simulate damage caused by n-type implants, followed by high temperature capped anneal; the substrate qualifies if it remains semi-insulating. Other tests involve measurement of the electron concentration profile after ion implantation and annealing of silicon and checking that the doping profile is similar to that of a control sample. These tests aim at reproducibly obtaining high quality active layers with the following properties [79,15]:

1. reproducible and well controlled carrier profiles,
2. high undepleted carrier concentration,
3. high drift mobility (> 4500 cm^2/v sec) which stays constant or rises through the channel-substrate interface,
4. controlled drain currents and pinchoff voltages with minimal nonuniformities, and
5. stable and high resistance substrates after high temperature

processing.

Undoped LEC bulk grown GaAs substrates are preferred for fabrication over Bridgman or Cr-doped material because the latter tends to exhibit poor performance in active layer properties such as lower activation and mobility, drain current and threshold voltage nonuniformity, and thermal conversion associated with chromium in the substrates [72,74,77,79]. With LEC undoped GaAs substrates, improvement of reproducibility of active layer properties compared to chromium doped LEC GaAs has been reported [71] as uniformity from ingot to ingot has been markedly improved and the problem of surface conversion has been eliminated. However, it is expected that undoped LEC GaAs material from different sources should exhibit differences in quality and performance. Also some suppliers may change their growth procedures to obtain semi-insulating wafers and to pass qualifying tests.

It is the objective of this chapter to investigate undoped LEC GaAs substrates: (1) from different suppliers; (2) for differences between low pressure and high pressure grown material; and (3) from recent and earlier eras from one supplier. In addition, a substrate is also analyzed which did not pass the qualification tests of a device manufactuer, but did pass the screening test of the supplier. The following parameters are sought to charcterize GaAs substrates for this investigation:

1. sheet resistance, Hall mobility, activation,
2. doping profile, undepleted carrier concentration, and zero gate bias depletion width,
3. drift mobility,
4. deep levels in MESFETs channel, and

5. backgating effect.

5.2 Description of the Diagnostic Test Pattern

The test pattern which is shown in figure 5.1 was developed by N.G. Tarr [80] based on that reported by Immorlica [81]. Occupying the centre of the pattern is a Van der Pauw cross used for measuring the n-implant sheet resistance, Hall mobility, and undepleted carrier concentration. A similar cross is provided in the top left hand side to allow similar measurements for the heavily doped n^+-implant used for ohmic contacts. A Schottky diode on the lower right hand corner is used to measure implant profiles. There are also four MESFETs with different dimensions, labelled T1-T4. MESFET T3 is a fat FET with a gate length far greater than source-gate and drain-gate spacings; it is used to profile the drift mobility in the ion implanted channel. MESFET T4 is used for investigating deep levels by channel current DLTS. Finally, MESFETs T1 and T2 are used primarily to determine the drain current and threshold voltage variations.

5.3 Diagnostic Pattern Fabrication

Fabrication was carried out on five substrate slices of undoped LEC GaAs. Two of the slices B, and C from Sumitomo (high pressure LEC GaAs) and Litton (low pressure LEC GaAs) respectively were obtained from 2" wafers. The remaining three slices were obtained from 3" wafers supplied by Cominco (high pressure grown): Substrate A-686 is a recent wafer grown in 1985, substrate B-727 is also a recent wafer which failed the screening tests of a device manufacturer, and finally substrate A-184 is from an earlier era grown

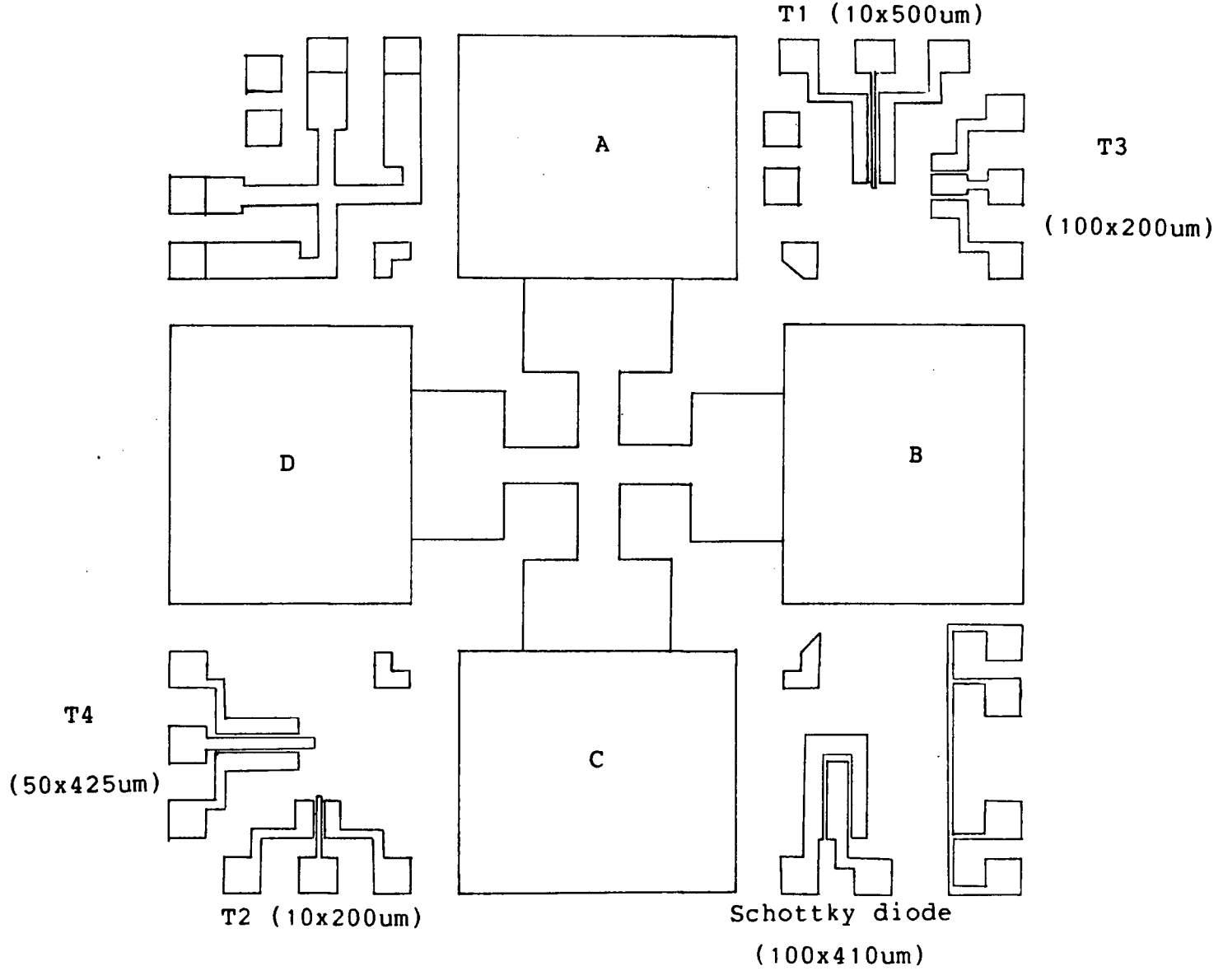
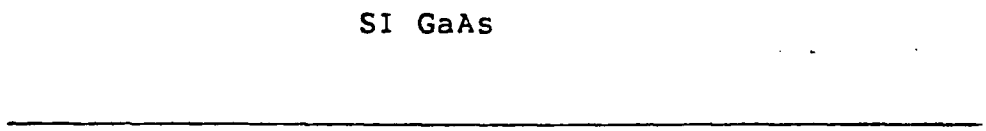


Fig. 5.1 The diagnostic test pattern

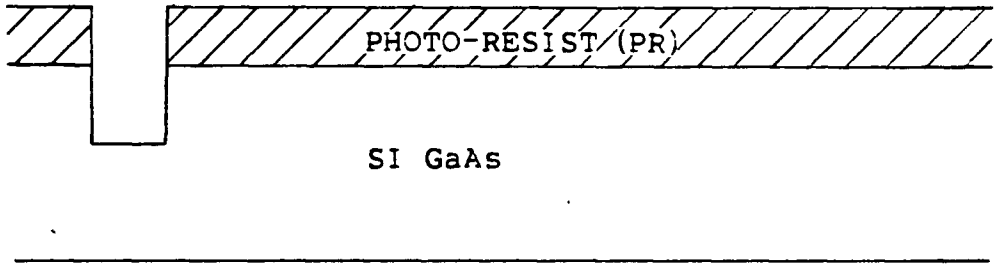
in 1982. All slices were fabricated identically so that different substrate effects can be observed. Ten to twelve test patterns (each 5 mm × 5 mm) are fabricated on each slice (20 mm × 15 mm) to average the various measurements.

The first step in fabrication was to degrease for five minutes in boiling trichloroethylene, acetone, and isopropanol. This was followed with four minutes cleaning in a 1% Alconox solution (monosodium dihydrogen phosphate). Afterwards the slices were rinsed for 15 seconds in de-ionized (DI) water. The surface was then etched one micron by dipping in a mixture of ammonium hydroxide, hydrogen perioxide, DI water (5:2:240 by volume) for five minutes. After rinsing the slices for 15 seconds in DI water, the slices were bathed for two minutes in boiling isopropanol. At this stage (figure 5.2a), the slices were all ready for processing.

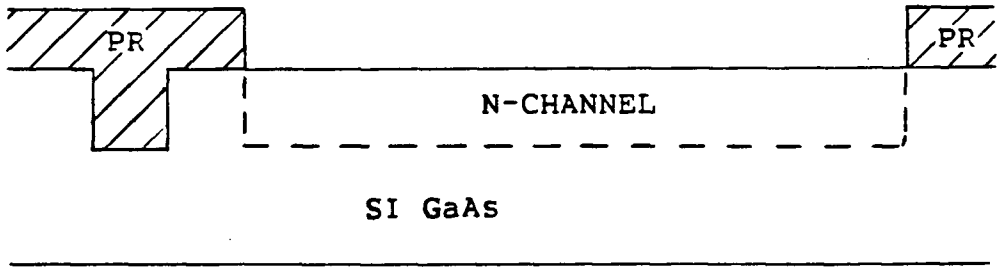
In the next fabrication stage, registration marks were opened in the slices, Photoresist (Shipley AZ1450J) was spun to a uniform thickness of 1.5 microns, baked for 30 minutes at 65°C, and exposed to UV light through the appropriate mask for 1.5 minutes. The registration marks were then etched 1000Å with the ammonium hydroxide solution used above for 30 seconds (figure 5.2b). With the photoresist removed by boiling acetone, the slices were similarly patterned using an n-implant mask. Windows were opened through the photoresist to allow ion implantation directly into the GaAs surface (figure 5.2c). The samples were then all ion implanted with ^{28}Si using a dose of $2.2\times10^{12}/cm^2$ at 100 keV. Afterwards, the photoresist was removed by dipping the slices in acetone; the stubborn remainder was removed by oxygen plasma in the Plasmtherm system. Preparing the samples for high temperature anneal



(A) Wafer pre-clean

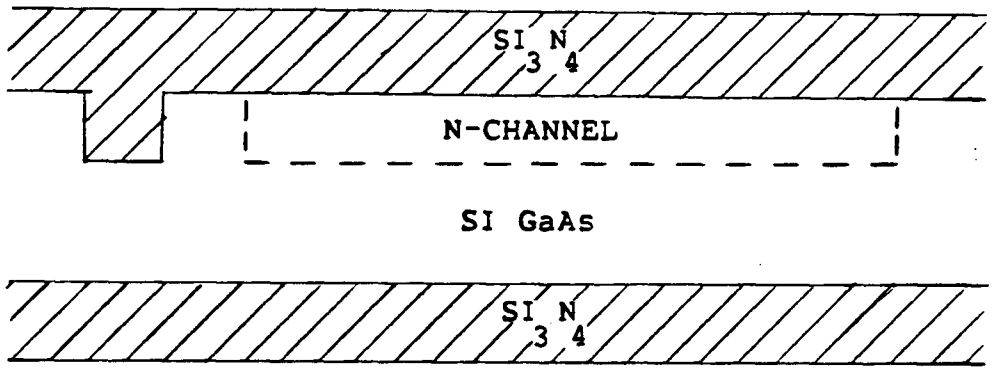


(B) Registration mark etch

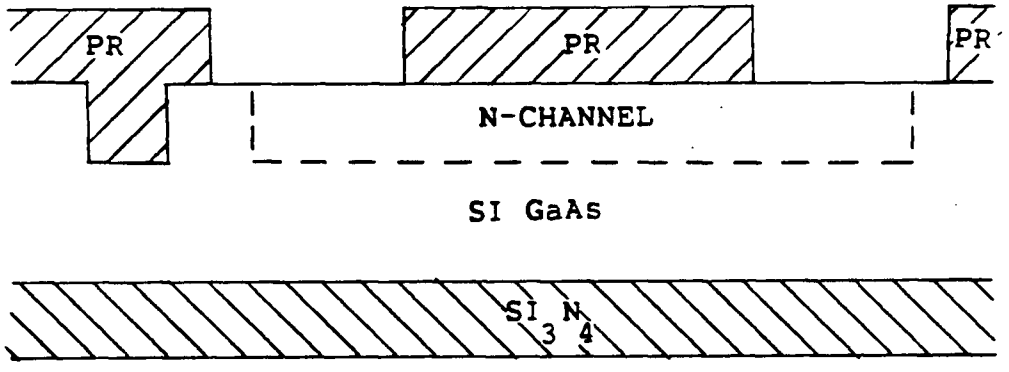


(C) Opening windows for ion-implantation

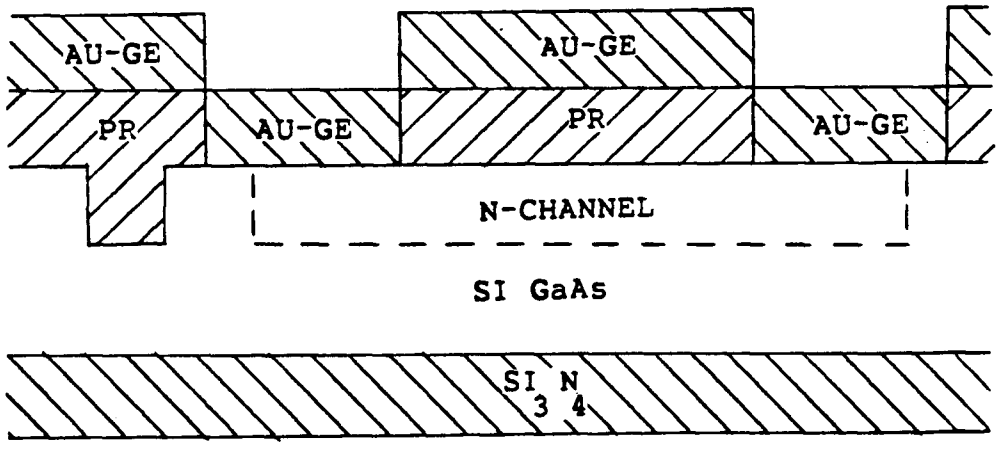
Fig. 5.2 Fabrication sequence for the diagnostic test pattern



(D) Encapsulation and annealing

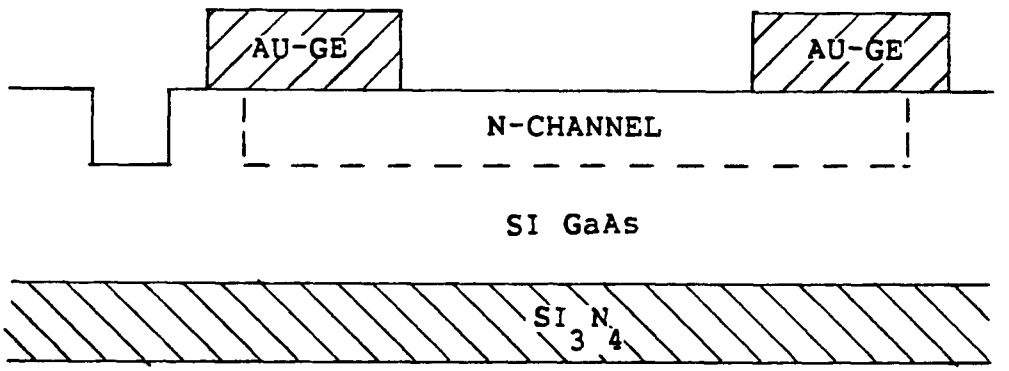


(E) Opening windows for gold-germanium contacts

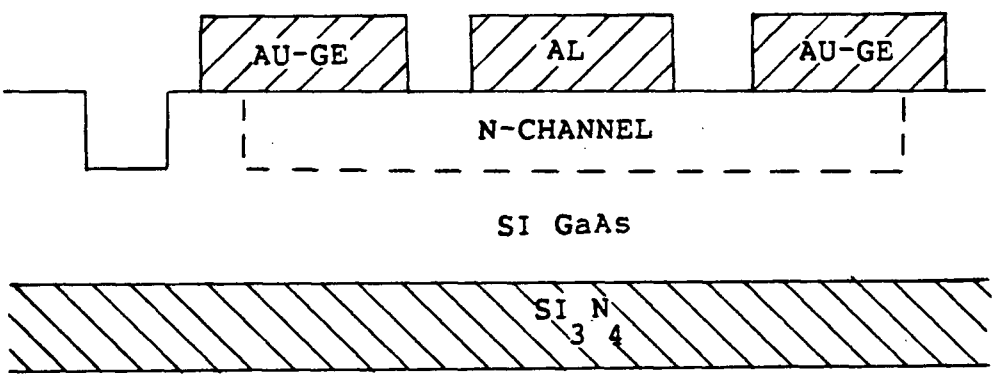


(F) Evaporation of gold germanium

Fig. 5.2 cont'd



(G) Liftoff of photo-resist, and alloying



(H) evaporation of aluminium.

Fig. 5.2 cont'd

consisted of degreasing the slices, laying down a 900Å to 1000Å film of PECVD silicon nitride on both surfaces of the wafer (figure 5.2d) and annealing in a Mini Brute silica tube furnace at 825°C for 25 minutes. After the anneal, the top silicon nitride film was removed by freon plasma in the Plasmatherm system. The n^+-implant was here foregone to simplify the processing steps.

In the next step (figure 5.2e), the slices were degreased and patterned with the ohmic contacts mask. Au+Ge (88%Au+12%Ge) was evaporated to a thickness of 2000Å (figure 5.2f). This was followed with boiling in acetone to get metal liftoff (figure 5.2g) and alloying for two minutes at 435°C in the Mini Brute furnace. In the final step (figure 5.2h), the slices were patterned with the Schottky gate metal mask, and 2000Å of aluminum was evaporated into the slices and then followed by liftoff to form Schottky gate contacts.

5.4 Measurements on the Diagnostic Test Pattern

All the measurements carried out here were non-destructive and meant to give information on the properties of the ion implanted and annealed active layers. A useful tool that facilitated a number of measurements is the HP 4145A Semiconductor Parameter Analyzer. Measurements of MESFETs characteristics were programmed into the internal computer. In this manner, measurement of I_{dss}, or drain current at zero gate voltage was obtained from I_{DS} vs. V_{GS}. Measurement of the threshold voltage was accomplished by measuring the gate voltage at which the drain current was roughly 5 ua. Measurement of the transconductance was obtained by plotting the drain current versus gate voltage and determining the slope at each point.

Measurement of the sheet resistance was made using the central Van der Pauw cross of figure 5.1 with the technique in [82]. A current (1 ma) was passed between two adjacent terminals such as A and B using an HP 6186A DC current source, while the voltage between the other adjacent terminals C and D was measured by a sensitive (Fluke 8050) voltmeter. The active layer sheet resistance, R_S, was obtained by solving:

$$R_S = (\pi/\ln 2)\ (V_{CD}/I_{AB})$$

The Hall mobility of the active layer was measured by using the same Van der Pauw cross structure. The sample was placed in a miniature probe holder and placed in a magnet (Alpha Scientific Laboratories) such that a magnetic field, B, (0-.2 Tesla) was applied normally to the sample. A constant current (100 ua) was applied between two opposite terminals, such as A and C, while the voltage was monitored at the remaining opposite terminals B and D. The average Hall mobility was obtained by solving:

$$U_H = (V_{BD}/R_S B\ I_{AC})$$

The undepleted carrier concentration N_{UC} was then calculated from the sheet resistance and Hall mobility:

$$N_{UC} = (1/q\ U_H R_S)$$

The doping profile was obtained by using the Schottky diode in figure

5.1 and performing gate capacitance versus reverse bias voltage measurement and calculating the electron concentration n(x) versus depth x (e.g. [83]):

$$n(x) = (C^3/q\varepsilon A^2)\ (dV/dC)$$

where ε is the permittivity of GaAs, A is the area of the diode, and C is the gate capacitance. This capacitance was measured by a HP 4275A Multi-Frequency LCR Meter which is interfaced to a HP 9812 computer, and the doping was profiled by two software routines, HFCVN and NWALLN, supplied by HP.

The drift mobility profile was measured using the fat FET (T3) following the method of Pucel and Krumm [84]. With the FET biased in the linear mode such that it is well below saturation (V_{DS} = 50 mV), the transconductance, dI_{DS}/dV_{GS}, was recorded by the HP 4145A Semiconductor Parameter Analyzer, the gate capacitance vesus reverse bias voltage was recorded by the HP 4275 LCR Meter, and with the doping profile obtained above, the drift mobility $\mu(x)$ was given by:

$$\mu(x) = (L/C\ V_{DS})\ (dI_{DS}/dV_{GS})$$

where L is the gate length. For the particular FET geometry used, the channel resistance was much greater than the contact resistances associated with the drain and source, and those factors were thus ignored in the mobility measurement.

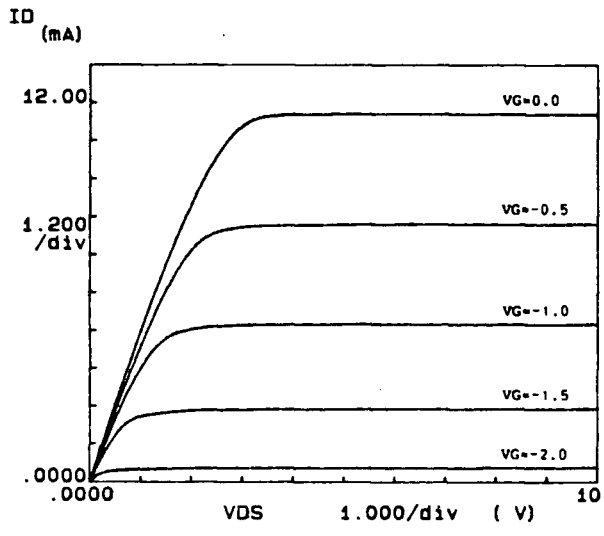
The backgating measurements were accomplished using the HP 4145A

Semiconductor Parametric Analyzer. MESFET T1 was used as the active device, and the adjacent pad A of the Van der Pauw cross (500 um separation) was used as the sidegate electrode. The Parameter Analyzer was programmed to plot the drain current with both the gate and source grounded versus the backgating voltage as it was swept from +20 V to -30 V. The data were stored and replotted on the HP 9816 computer so that the drain current was normalized to I_{dss} with the backgating electrode disconnected.

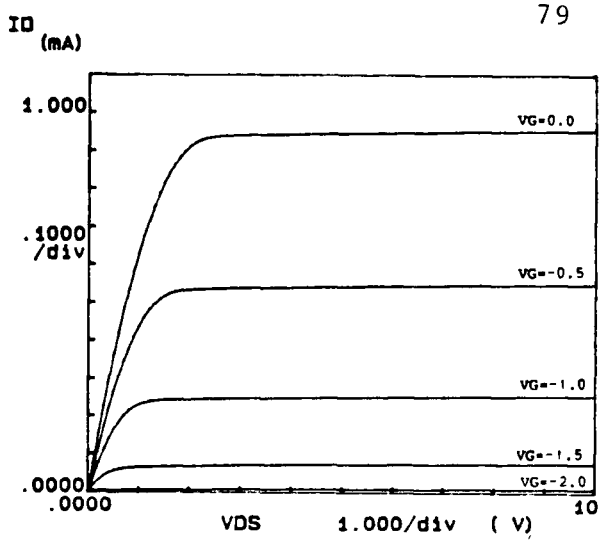
The last measurement was the deep levels in the MESFET channels. That was performed using the channel current DLTS technique described in the last Chapter.

5.5 Results of Active Layer Evaluation

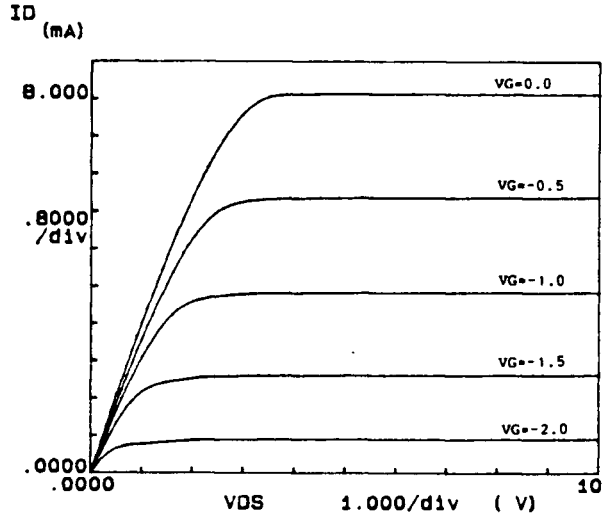
Typical I_{DS}-V_{DS} characteristics of the four MESFETs in each test pattern are shown in figure 5.3. I_{dSS} is not the same in the four transistors because of the different gate lengths and widths in each device. The linear region of the characteristics does not have a steep slope which is a consequence of not using an n^+-implant to reduce the source and drain contact resistances. The drain current at saturation is almost constant with increasing drain voltage which is desirable in MESFETs. Because of the light doping of the channel, no breakdown in the drain current occurs for drain voltages below 10 volts. Table 5.1 presents results on the average drain current and threshold voltage and their scatter for MESFET T1 (L = 10 μm, W = 500 μm). The averaging was done over 10 to 12 devices which are spaced horizontally and vertically by 5 mm, and so the scatter reflects macroscopic (as opposed to microscopic) inhomogeneity in the slices. The table also



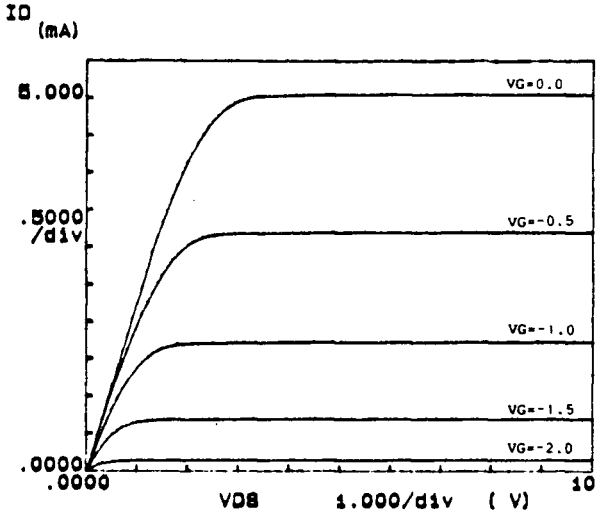
(a) MESFET T1



(c) MESFET T3



(b) MESFET T2



(d) MESFET T4

Fig. 5.3 Typical I_{DS} - V_{DS} characteristics of MESFETs in the diagnostic test pattern

Table 5.1 Comparison of the active ion implanted layers parameters of five GaAs samples.

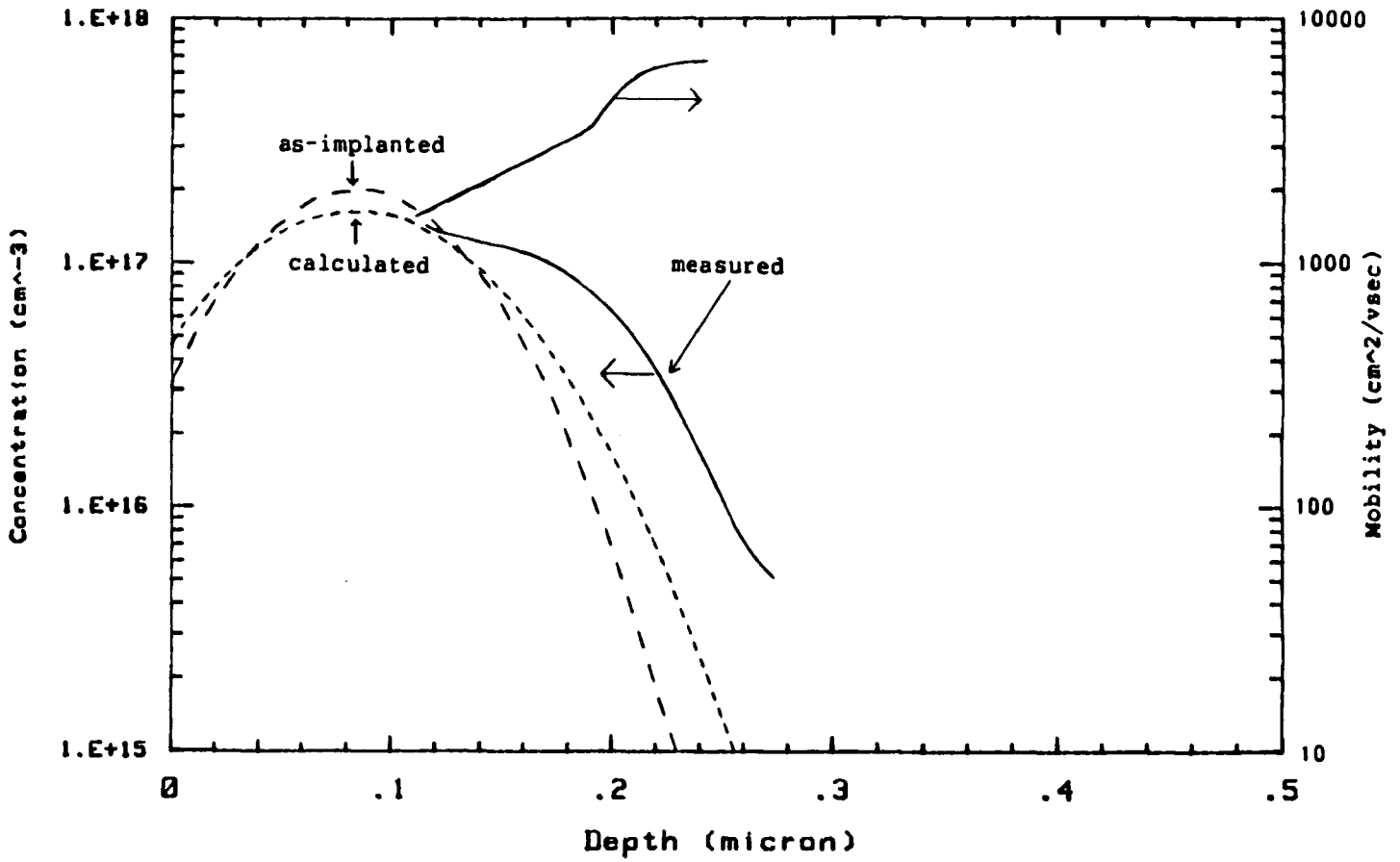
Parameter	A-686	A-727	A-184	B	C
I_{dss} (Tl)	9.25 ma	7.82 ma	11.21 ma	9.58 ma	7.73 ma
Scatter (I_{dss})	1.25 ma	0.61 ma	1.46 ma	1.00 ma	0.94 ma
Vth (Tl)	-2.00 V	-1.71 V	-2.21 V	-1.74 V	-1.50 V
Scatter (Vth)	170 mV	66 mV	130 mV	94 mV	90 mV
Rs	1584	1672	1370	1282	1553
Scatter (Rs)	125	76	82	85	132
U_H	4542	4693	4530	4751	4683
N_{uc}	8.7E11	8.0E11	1.0E12	1.0E12	8.6E11
W_0	1186 Å	1107 Å	1215 Å	949 Å	1065 Å
W_1	2478 Å	2389 Å	2700 Å	2501 Å	2383 Å
N_{max}	1.32E17	1.22E17	1.26E16	1.36E17	1.12E17
Activation	66.2 %	61.5 %	63.0 %	68.4 %	56.1 %

shows the average sheet resistance (R_S) and its scatter, Hall mobility (U_H), undepleted carrier concentration (N_{UC}), zero gate bias depletion width (W_0), the doping profile depth at a doping level of 10^{16} (W_1), the peak carrier concentration N_{max}, and activation of the 5 samples. The information of the last four entries in table 5.1 were obtained from the doping profiles of the five samples determined by C-V carrier profiling. The doping profiles of the five substrates and the drift mobilities are shown in figures 5.4(a-e). The as-implanted profile was calculated knowing that the implant depth R_p is 850Å and the standard deviation ΔR_p is 442Å for an energy of 100 keV, and a dose, Ds, of 2.2×10^{12} cm^{-2}; n(x) is (e.g. [4]):

$$n(x) = \frac{Ds}{(2\pi)^{1/2}\,\Delta R_p}\,EXP\left\{-\frac{(x-R_p)^2}{2(\Delta R_p)^2}\right\} \qquad (5.1)$$

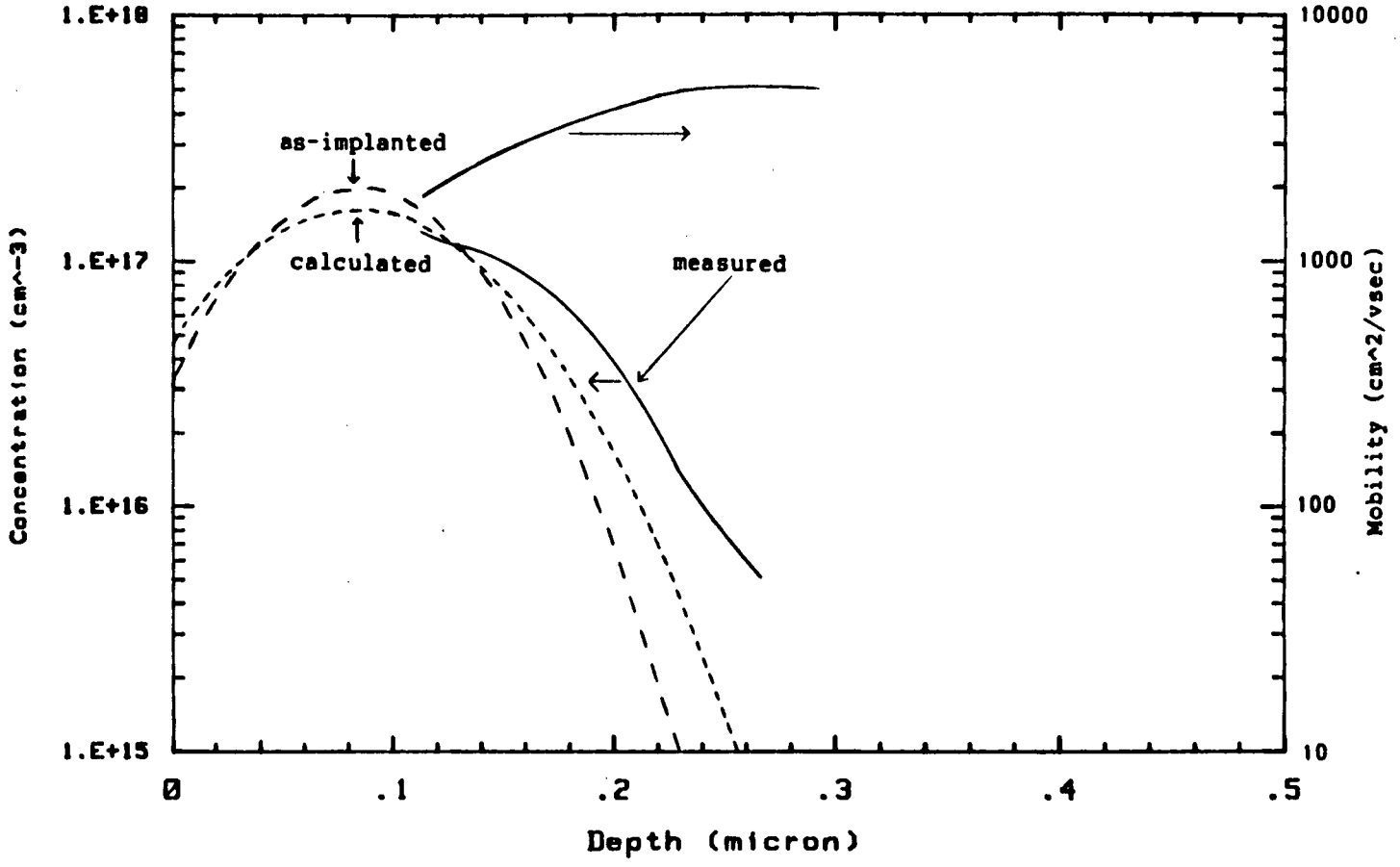
The theoretical peak carrier concentration is the factor multiplying the exponential in equation (5.1). The measured peak carrier concentration (from C-V measurements) can then be divided by that obtained for the as-implanted profile to obtain activation in table 5.1. The calculated doping profile, on the other hand, was estimated by including the effects of the time, t, of the anneal and also be taking into account the diffusion coefficient, D, of silicon in GaAs (Yamazaki et al. [85]). The effective straggle is increased by diffusion at high temperatures and becomes [85,86]:

$$\Delta R_p' = \left((\Delta R_p)^2 + 2\,D\,t\right)^{1/2}$$



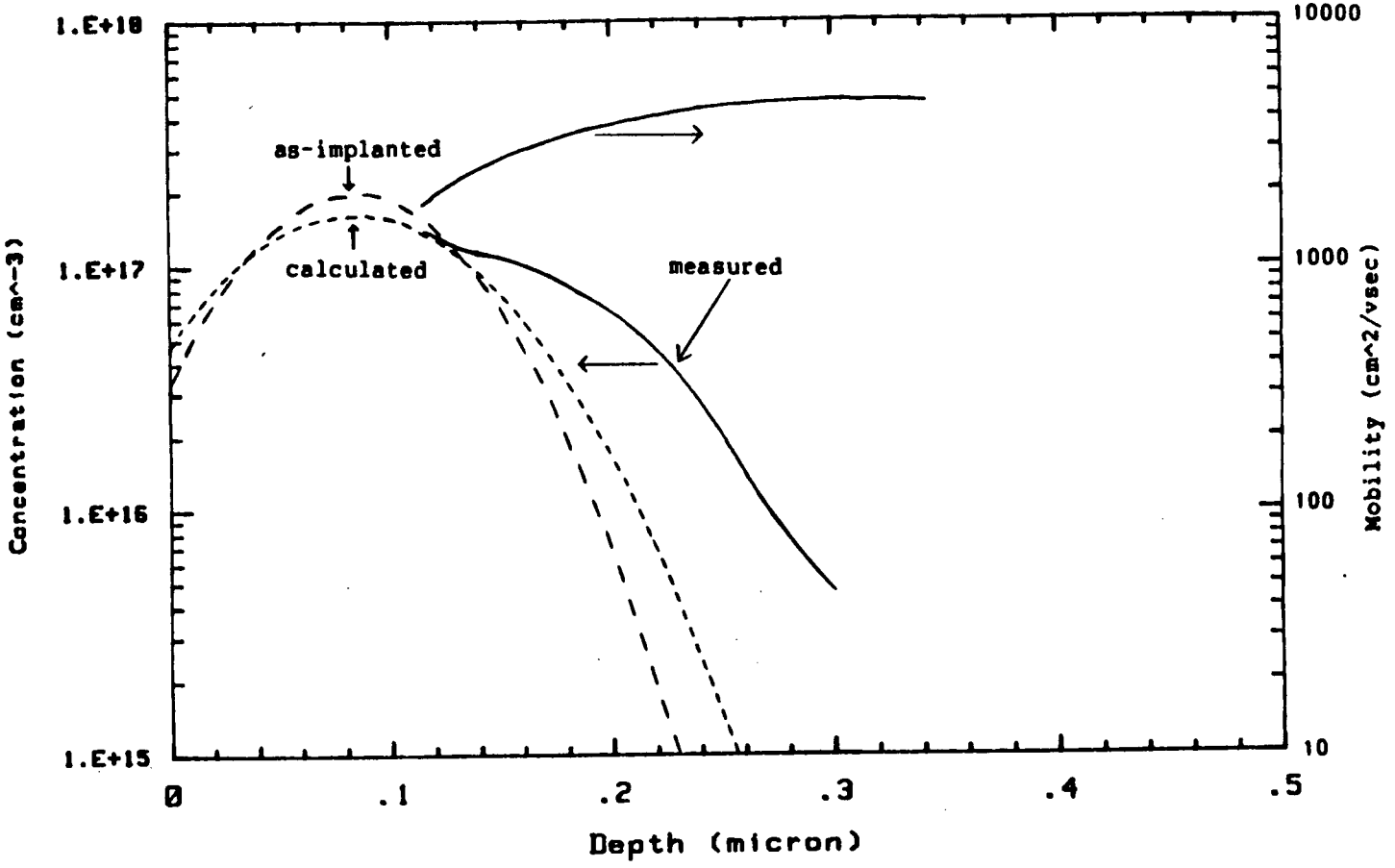
(a) A-686 (Cominco)

Fig. 5.4 As-implanted, calculated, and measured carrier density profiles and drift mobility profiles



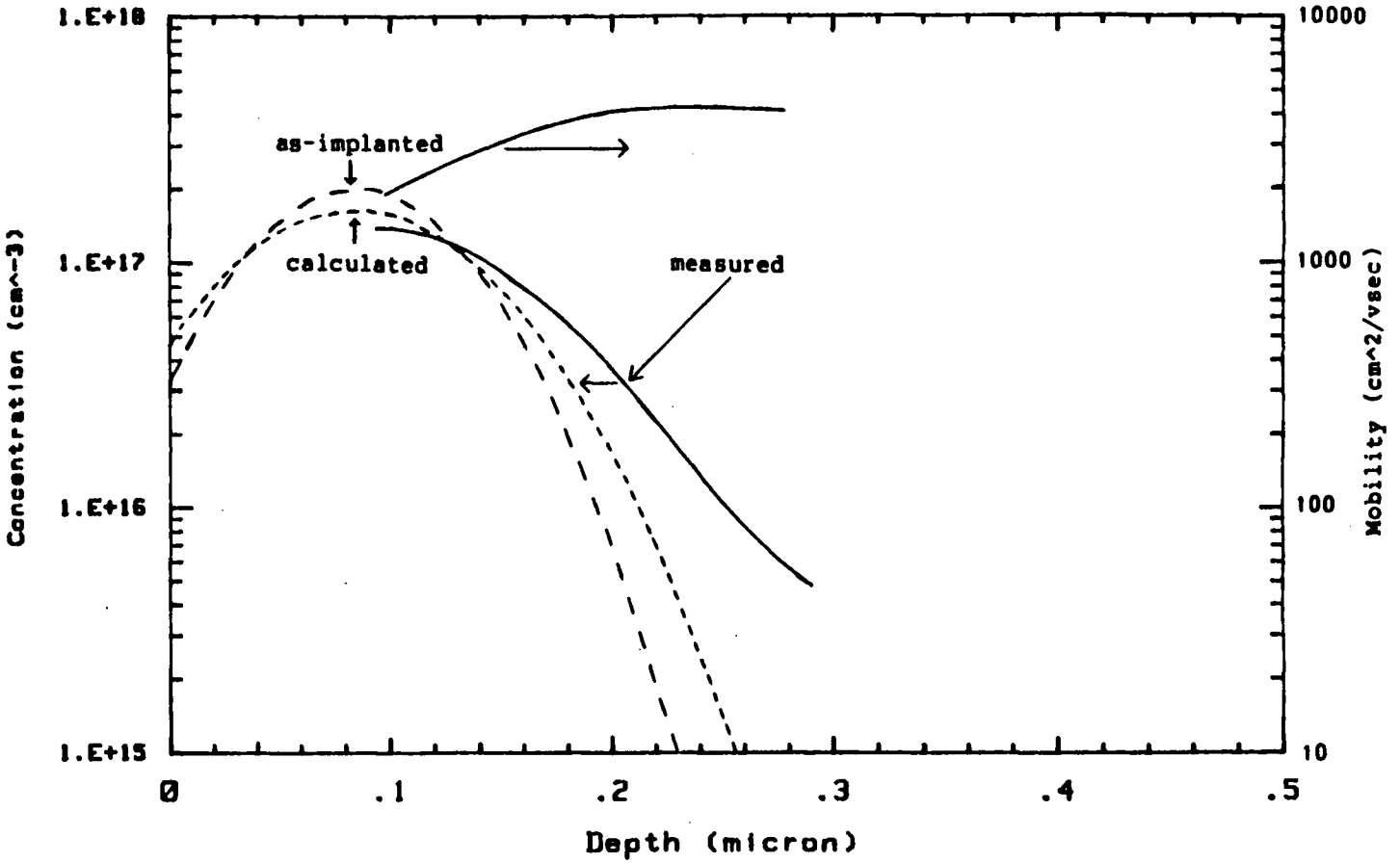
(b) A-727 (Cominco)

Fig. 5.4 cont'd



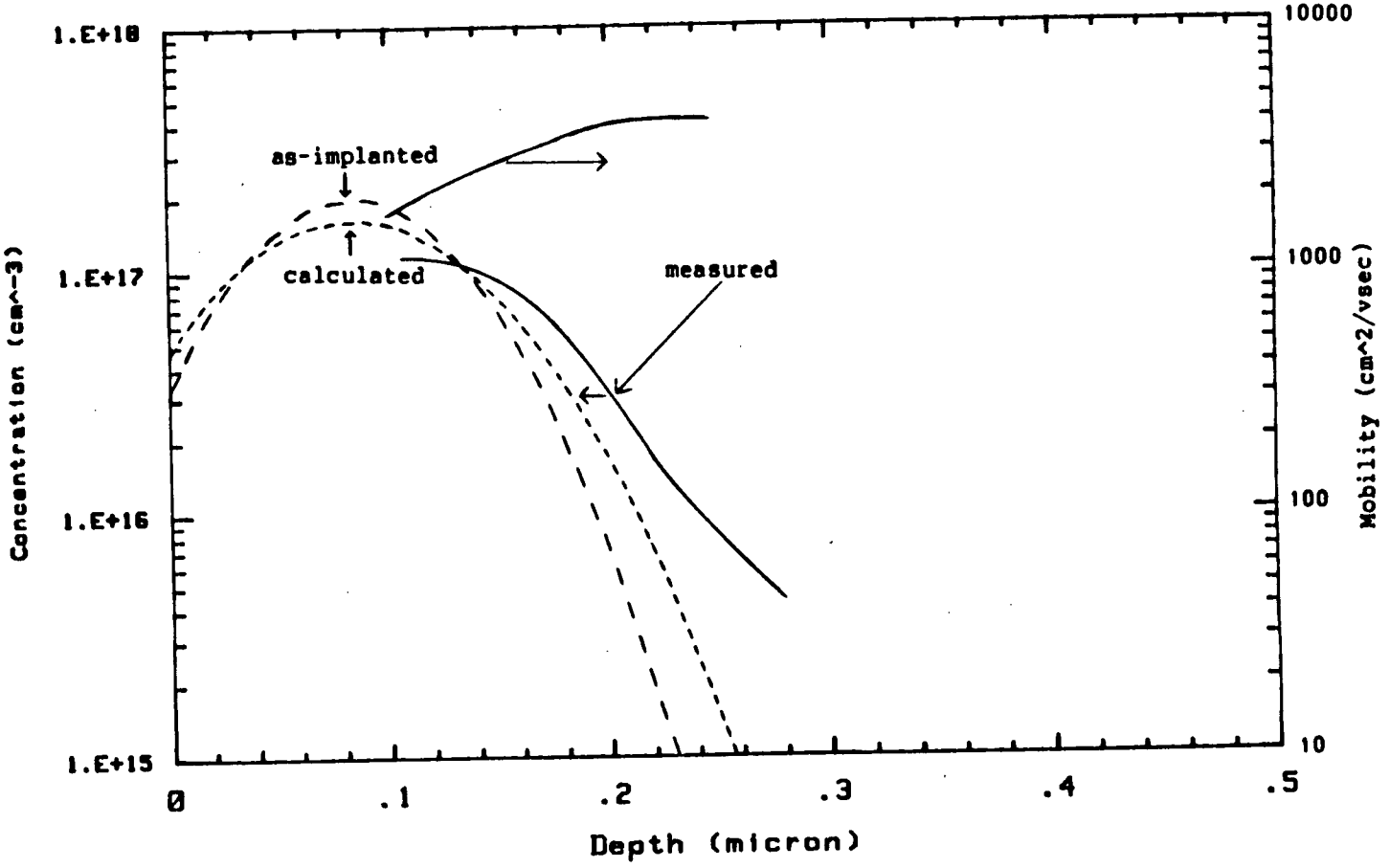
(c) A-184 (Cominco)

Fig. 5.4 cont'd



(d) B (Sumitomo)

Fig. 5.4 cont'd



(e) C (Litton)

Fig. 5.4 cont'd

where t is 1500 sec and D = 3×10^{-15} cm^2/sec. This effective straggle replaces ΔR_p in equation (5.1) and the resulting calculated profile is generally flatter than the as-implanted profile.

Examination of the parameters in table 5.1 and the doping profiles reveals wide variations between the substrates. Concentrating first on Cominco's material, it is seen that their most recent wafer A-727 has the least scatter in the threshold voltage, drain current and sheet resistance among all the samples. This makes it desirable. The fact that the drain current measured was one of the lowest is explained by the doping profile (figure 5.4b) which shows that the electron density as a function of depth is the closest to the calculated doping profile and therefore the channel is narrower. An interesting feature of this sample is the fact that the dip in the peak carrier concentration, N_{max}, was not accompanied with a long diffusion tail as compared to other samples from the same vendor. This may be caused by substantial compensation of silicon in the channel. Nevertheless, the drift mobility of this substrate can be seen in figure 5.4b to be rising towards the interface, reaching 5100 cm^2/v sec near the semi-insulating substrate. On the other hand, comparison of Cominco's samples from different eras, A-686 (1985) and A-184 (1982), both of which were qualified for fabrication, show differences with respect to the drain current magnitude and the threshold voltage which are evident by examining table 5.1. The differences can be explained by comparing the doping profiles of the samples in figures 5.4a and 5.4c where it can be seen that extensive diffusion has taken place for sample A-184 making its channel the widest, and

as a consequence, the drain current and threshold voltage of A-184 is the highest of all the five samples. Unlike A-727, there is substantially higher scattering of the threshold voltage, drain current, and sheet resistance in both A-686 and A-727. The drift mobility profile for A-686 can be seen in figure 5.4a to be rising to a value fo 6200 cm^2/v sec towards the interface, while for A-184 the drift mobility shown in figure 5.4c is constant (5000 cm^2/v sec) towards the interface. The better mobility, better activation, and smaller diffusion tail of the recent sample, A-686 shows that the vendor has changed the growth conditions to improve his material. A-727 which is rather different from A-686 though they were both grown at close periods of time indicate that one or more growth parameters were not adequately controlled.

Sample B from Sumitomo showed substantially different charcteristics. Compared to Cominco's recent material (A-686) it had similar drain currents, and similarly controlled diffusion tails in the doping profile. However, high activation is obtained as indicated by the better peak carrier concentration. Also, substantially less depletion width under the gate is observed (949Å compared to 1186Å for A-686). The scatter in the drain current and of the threshold voltage was better controlled, perhaps as a result of a lower dislocation density in this 2" wafer than Cominco's 3" wafers. However, the drift mobility of this sample (figure 5.4d) was constant (4300 cm^2/v sec) toward the interface, which was far lower than any of Cominco's material.

Sample C from Litton had the lowest percentage activation, drain current, and threshold voltage in comparison to Cominco's and Sumitomo's high

pressure grown substrates. The scatter of the threshold voltage and drain current, however, was confined to reasonably good values similar to sample B. The depletion width under the gate and the diffusion of the carriers were adequately controlled as in A-727. However, as a consequence of lower activation, the threshold voltage was lower than A-727. The drift mobility profile shown in figure 5.4e reaches a value of 4200 cm^2/v sec which is the lowest amongst the five samples.

5.6 Results on Deep Levels

The MESFETs used for this test were made essentially following process III described in the previous chapter i.e. direct implantation into GaAs and annealing under PECVD silicon nitride cap. Another refinement was now introduced in that capping was done also on the back side so as to prevent As loss on this surface. It was found in the previous chapter that only a single level, S1, was present in the MESFET channels prepared by process III. In addition, it was found using OTCS that this trap was present in the starting material as EL12, and hence was not process-induced.

In this experiment, all processing steps are identical and hence deep levels other than S1 present in the five GaAs MESFET channels may be concluded to be substrate-induced. Results of channel current DLTS spectra on MESFET T4 (L = 50 um, W = 425 um) for the five samples from three vendors are shown in figures 5.5a to 5.5e. Arrhenius plots of the traps obtained are shown in figure 5.6. Tables 5.2 and 5.3 provide the DLTS data and concentration of the traps. Examination of the DLTS spectra of the five substrates reveal a number of substrate-induced defects. Focussing first on

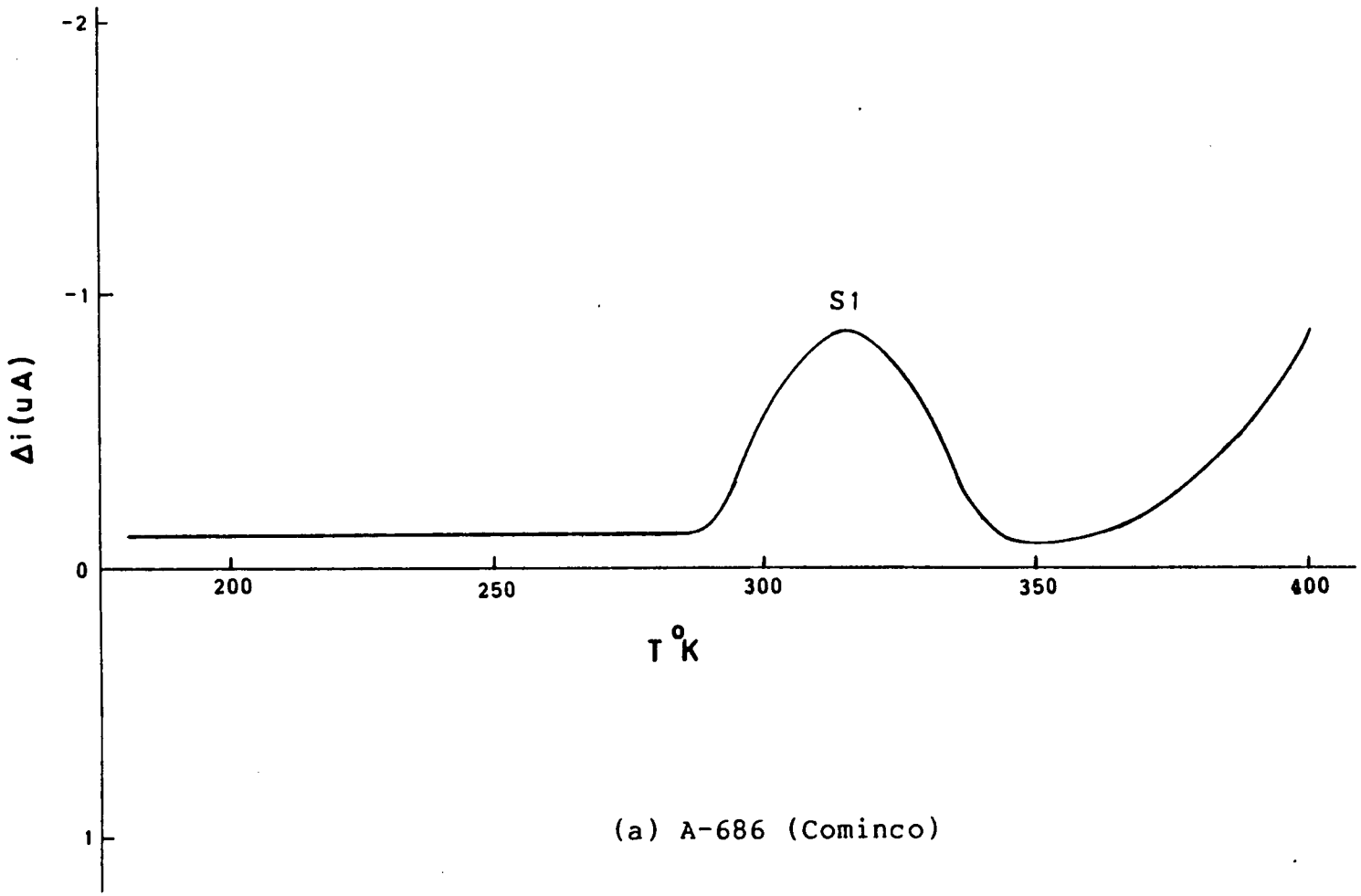
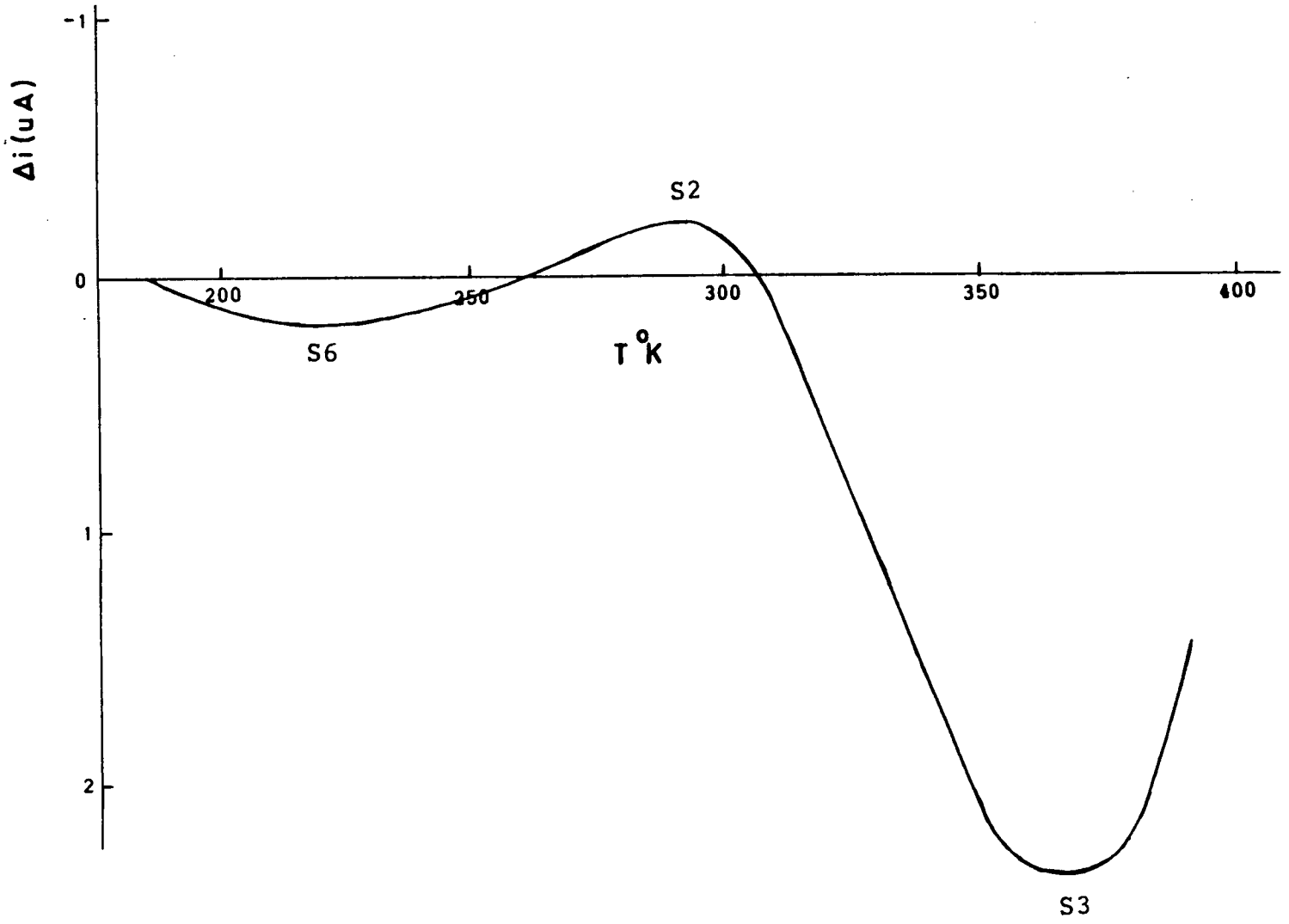
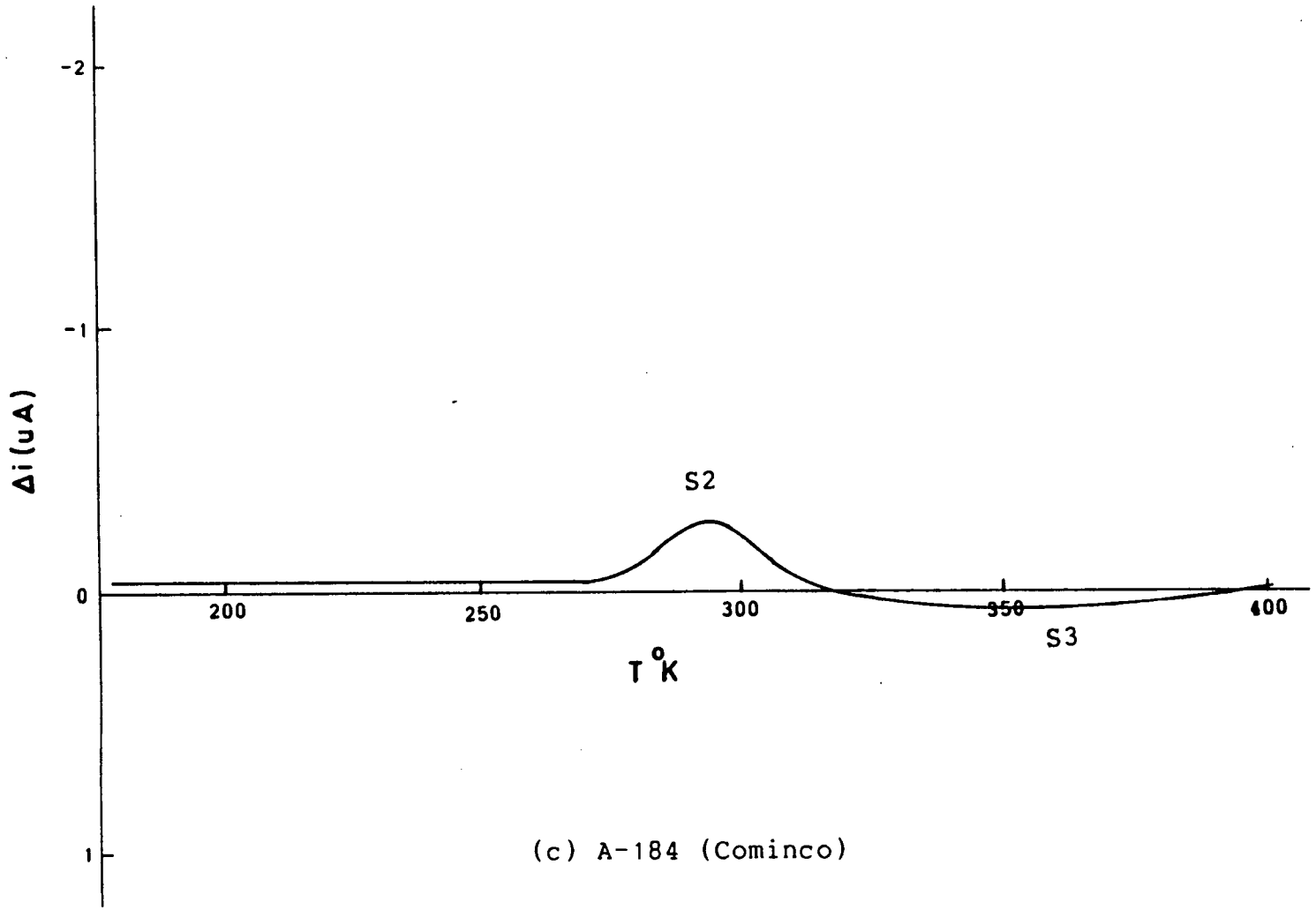


Fig. 5.5 Channel current DLTS spectra for MESFETs fabricated on five substrates (Rate Window = 49.7msec)



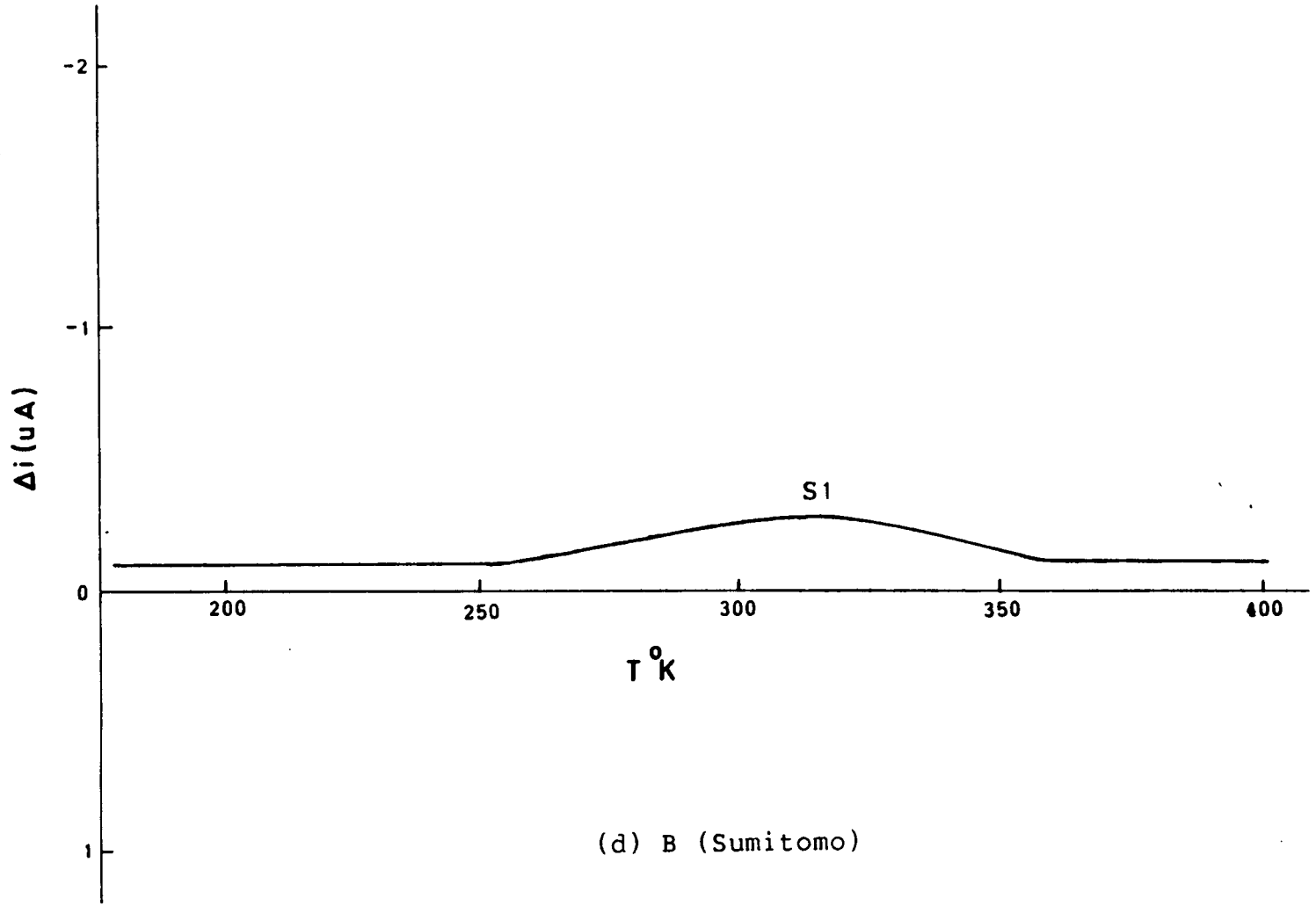
(b) A-727 (Cominco)

Fig. 5.5 cont'd



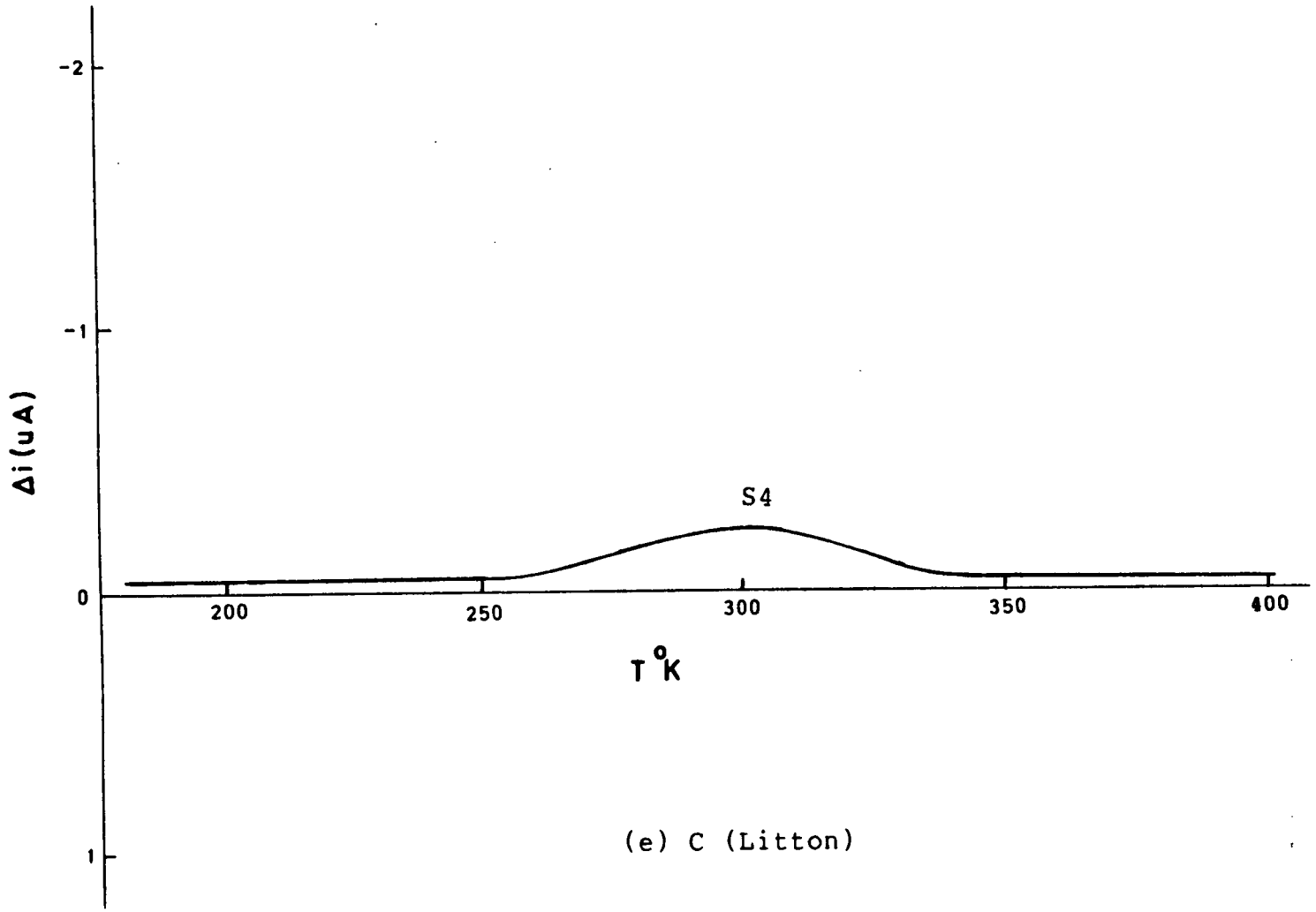
(c) A-184 (Cominco)

Fig. 5.5 cont'd



(d) B (Sumitomo)

Fig. 5.5 cont'd



(e) C (Litton)

Fig. 5.5 cont'd

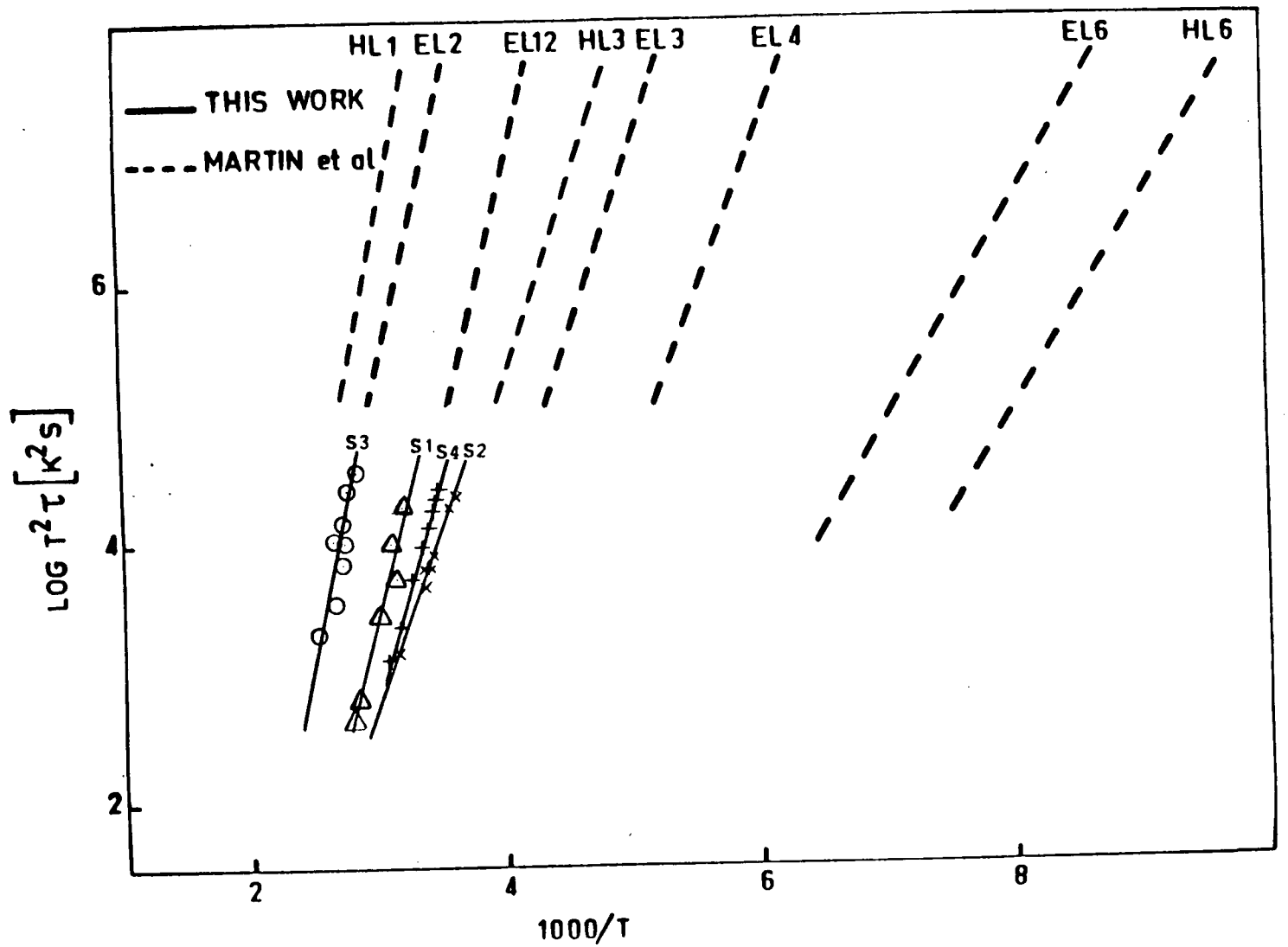


Fig. 5.6 Signature line plots of the channel current DLTS data

Table 5.2 DLTS data on the traps found by channel current DLTS.

Trap Level	Activation Energy	Capture Cross Section	Type	Identity
S1	0.74 eV	2.1×10^{-13} cm^2	electron	EL12
S2	0.52 eV	3.62×10^{-16} cm^2	electron	
S3	0.87 eV	5×10^{-14} cm^2	hole trap	Cr ?
S4	0.69 eV	2.3×10^{-12} cm^2	electron	
S5	?	?	hole trap	

Table 5.3 Concentration of the traps found by channel current DLTS.

	concentration of traps (cm^{-3})				
Substrate Type	S1	S2	S3	S4	S5
A-686	8.7×10^{14}	-	-	-	-
A-727	-	1.98×10^{14}	2.13×10^{15}	-	1.7×10^{14}
A-184	-	1.89×10^{14}	5.32×10^{13}	-	-
B	1.90×10^{14}	-	-	-	-
C	-	-	-	2.17×10^{14}	0

Cominco's material, the DLTS spectrum of sample A-686 reveal that there are two traps one of which is S1 (EL12) at a relatively high concentration ($8.7E14cm^{-3}$). The second trap is substrate-induced and occurs at a high temperature (T > 400 K) beyond the range of the experimental setup, and therefore information about the activation energy, capture cross section and possible identification of the peak could not be obtained. However, it can be seen that the concentration of that level is high and in addition, at that temperature, it was observed that there was substantial lagging of the rise time of the drain current in response to changes in the gate voltage. The above traps are expected to be in the channel region and not at the interface since the drift mobility was high toward the interface with the semi-insulating substrate.

A rather different spectrum was observed for sample A-727 in figure 5.5b. Three substrate-induced defects were found, two of which were hole traps. The level S1 was not found but instead, another electron trap, S2, occurs in the vicinity with much smaller capture cross section and closer to the conduction band as seen in table 5.2. The main feature of the spectrum is the dominant hole trap S3 with an activation energy of 0.87 eV. This could be due to an impurity, possibly chromium, and occurred at a relatively high concentration ($2.13E15\ cm^{-3}$). Another hole trap S6 was found with a much smaller concentration ($1.9E14\ cm^{-3}$) but could not be identified since the peak was too broad for its characteristic temperature to be obtained accurately. It is possible that the limited diffusion of the ion implanted silicon found in this sample in comparison to other samples from this vendor was due to the high concentration of the hole trap S3 which acts as an

acceptor and compensates donors in the channel. The hole traps appearing in this sample, but which were not observed in A-686 although both substrates were recent indicates possible contamination during growth.

The DLTS spectrum of sample A-184, the substrate which was grown three years earlier displayed similar traps to A-727. Two traps were found, S2 and S3, the second of which showed smaller concentration (5.32E13 cm^{-3}). These findings indicate again that vendor A has changed some of the growth parameters over the three year period, as the DLTS spectra of A-686 and A-184 are entirely different. While he succeeded in reducing the impurities of his undoped substrate material (evidenced by the absence of hole traps in A-686), the control of the growth environment was apparently inadvertently lost during the growth of his recent substrate A-727.

Sample B of Sumitomo displayed a DLTS spectrum similar to the material investigated in the previous chapter for process III. The level S1 was found with a small concentration (1.9E14 cm^{-3}) and no substrate induced defects were found. Sample C of Litton did not show the level S1, but another electron level appeared in the vicinity, S4, at a small concentration, (1.90E14 cm^{-3}), which was not present in the starting material.

5.7 Results on Backgating

Backgating is the phenomenon where the drain current of a MESFET is modified by the application of a bias voltage to a nearby electrode separated from the active device by the semi-insulating substrate. This phenomenon occurs when the channel interface with the bulk is modulated in thickness as a result of backgating bias with the semi-insulating separating layer acting

as a dielectric [87]. The severity of the backgating effect is dictated by the separation of the nearby devices, thermal stability of the substrate, the degree of isolation between devices, and the material properties of the semi-insulating substrate. Lee et al. [88] and Miers et al. [76] found a backgating voltage threshold which coincided with a trap filled limit voltage where carriers injected from the backgating voltage fill the traps in the substrate. Beyond the threshold, substrate conduction causes cross-talk between devices. However, agreement between the backgating threshold and the trap filled limit voltage is not conclusive in the literature as the results of Blum and Fleshner [89], and Tang [36] found little or no threshold for capless annealed and silicon dioxide cap annealed devices respectively; both suggest p-type surface conversion caused by the outdiffusion of EL2 as a probable cause of surface conduction giving rise to backgating. Ogawa and Kamiya [90] studied both HB (chromium compensated) and undoped LEC substrates and found gradual reduction in drain current as soon as backgating potential is applied for HB substrates; a threshold was however found in undoped LEC GaAs.

In this study, backgating (sidegating) due to bias on a contact 500 um away from an active device, Tl, was investigated for the undoped LEC GaAs from different vendors. Results of normalized drain current (with respect to I_{dss}) as a function of sidegating bias from +20 V to -30 V for the 5 substrate materials are shown in figure 5.7. As all processing steps are the same, expected variations in the sidegating behaviour are attributed to material differences. It can be seen from figure 5.7 that three substrates, A-727, A-686, and sample B were affected by backgating bias at +5 V, with

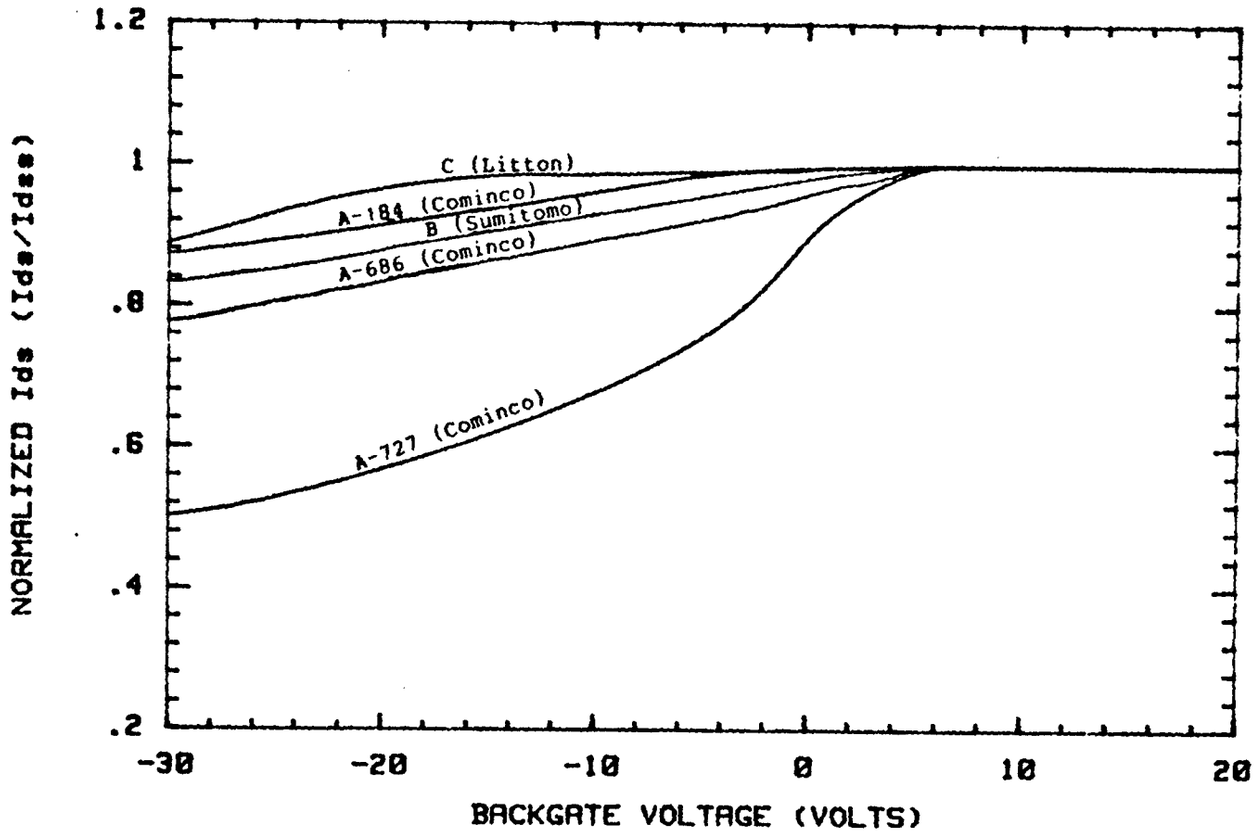


Fig. 5.7 Comparison of normalized drain current versus backgating voltage for five GaAs samples

sample A-727 showing considerable backgating effect as the drain current reduce to half at V_{bg} of -30 V; this makes it unqualified for active device fabrication. It is likely that the dominant hole trap S3 found in A-727 which behaves as an acceptor could form a p-type layer on the surface in addition to the outdiffusion of EL2 reasoned by [89,36] and therefore enhancing substrate conduction. On the other hand, Cominco's earlier sample, A-184, was affected differently by backgating, and the threshold of backgating is found to be -5 V, which agrees with Lee et al. [88]. The low pressure grown sample C, appears in this experiment to have the best backgating characteristics, the backgating voltage threshold for this sample is -16 V, which makes it attractive for high density fabrication. This study shows that the backgating effect is very much material dependent which can explain the disagreement in the experimental findings of backgating in the literature.

5.8 Discussion of the Results

Comparison of various undoped LEC GaAs material has shown that the electrical characteristics of ion implanted active layers, such as, activation efficiency, mobility, doping profile control, and uniformity is a function of the starting material. One of the main differences in the active layer characteristics of the five substrates studied here was shown to be the carrier concentration profiles. Deviations from the calculated doping profiles occur as a result of variations in the depletion width under the gate, the doping efficiency, and the diffusion tails. The depletion width under the gate is [91]:

$$W_0 = \left(\frac{2 \varepsilon V_{bi}}{q(N_D + N_T)}\right)^{1/2}$$

where V_{bi} is the built-in potential (0.8 V for GaAs), N_D is the doping concentration and N_T is the total concentration of traps, and ε is the permittivity of GaAs. Changes in the depletion width can occur as a result of variations in doping efficiency and residual defects just under the surface. Doping efficiency is the ratio of the net donor concentration from the implanted silicon dose. The net donor concentration in undoped GaAs is the amount of the silicon which is electrically active plus the number of shallow donors N_{sd} minus the amount of both shallow and deep acceptors (N_{sa}, N_{da}). Deep donors do not affect activation since they are electrically neutral in the undepleted channel [71]. The extent of diffusion tails are affected by [92] the annealing temperature, stresses caused by the annealing cap, implant dose, and stoichiometry of the substrate. With all parameters the same, different extents of dopant diffusion in the five substrates examined were caused by stoichiometry differences affected by the varying concentration of impurities, defects, and vacancies.

It has been reported that inhomogeneity in the doping profiles, which in turn produces variations in threshold voltages and drain currents, may be caused by the dislocations in the substrates. For example, Nanishi et al. [93] reported that high dislocation density increases the drain current and reduces the threshold voltage in undoped LEC GaAs. Ishii et al. [94] focussed on the effect of dislocation networks on the active layer parameters

and found that the threshold voltage scatter was correlated with dislocation cell networks and not with dislocation density. In the central part of the dislocation network the drain current was decreased whereas the threshold voltage increased. More recently, however, Winston et al. [95] found no correlation between threshold voltage and the active layer vicinity to the nearest dislocation for both conventional LEC GaAs and indium alloyed GaAs substrates. They reported however more uniform threshold voltages for lower dislocation density In-alloyed GaAs than the higher dislocation density LEC GaAs.

The extent of diffusion of the implanted species, the pinch-off voltages, and threshold voltages were calculated from the measured capacitance-voltage profiling to determine the extent of variations in the substrates investigated. The effective straggle, $\Delta R_p''$, was calculated from both N_{max} and the diffusion depths at a doping concentration of 10^{16}, W_1, which were tabulated in table 5.1 and solved for in the following equation:

$$10^{16} = N_{max} \, Exp\left(- \frac{(W_1 - R_p)^2}{2(\Delta R_p'')^2} \right)$$

The value of the corresponding diffusion coefficient, D', was then calculated from the effective straggle:

$$\Delta R_p'' = \left(\Delta R_p^2 + 2\, D' t\right)^{1/2}$$

The pinchoff voltage was calculated by integrating the charges under the gate

that had to be depleted numerically [91]:

$$V_p = \frac{q}{\varepsilon} \int_0^{\infty} n(x)' x dx$$

where n(x)' is the Gaussian profile fitted to the capacitance-voltage (C-V) profile obtained for each substrate. Finally, the threshold voltage was calculated by subtracting the built-in potential from the pinchoff voltage. The results are given in table 5.4 where the calculated pinchoff voltage and threshold voltages of the calculated and as-implanted profiles are also given. The calculated threshold voltages can be seen to approximately match those experimentally derived in table 5.1 with the exception of sample B where the experimental threshold voltage was lower. This indicates that the C-V profile when integrated over the channel length gives more charges in the depletion region than there actually are. This discrepancy must be caused by a degree of n-type surface conversion. For the other samples, the slight difference in threshold voltage is due to variations in the depletion width at zero gate voltage under the gate as indicated in table 5.1.

From the circuit design stand-point, control of the threshold voltage is required for the Schottky Diode Field Effect Logic (SDFL) should be within ±200 mV. This allows thickness variations only in the order of 80Å-100Å [71]. This means for the samples studied that the measured straggle has to be within that thickness variation from the design or control sample. All the samples investigated here had a threshold voltage scatter within the required limit for the SDFL circuit. For LSI circuits, however, considerably

Table 5.4 Comparison of the calculated values of effective straggle ($\Delta R_p''$), diffusion coefficient (D'), pinchoff voltage (V_p), and threshold voltage (V_{th}) of five GaAs samples.

Profile	$\Delta R_p''$ Å	N_{max} cm^{-3}	D' $cm^2 sec^{-1}$	V_p volts	V_{th} volts
A-686	717	1.32×10^{17}	10.6×10^{-15}	-2.91	-2.11
A-727	688	1.22×10^{17}	9.24×10^{-15}	-2.58	-1.78
A-184	822	1.26×10^{17}	16×10^{-15}	-3.18	-2.38
B	723	1.36×10^{17}	10.9×10^{-15}	-3.03	-2.23
C	699	1.12×10^{17}	9.72×10^{-15}	-2.39	-1.59
LSS	442	2.00×10^{17}	0	-2.61	-1.81
Calculated	534	1.64×10^{17}	3×10^{-15}	-2.63	-1.83

more stringent demands are placed on the threshold voltage so that standard deviation must remain within ±50 mV [71]. This requires better substrate quality and reproducibility than presently available.

5.9 Summary

Undoped LEC GaAs was investigated for suitability of IC applications. The following results were obtained:

1. Comparison of the low pressure and high pressure growth materials showed that while the active layer properties of the low pressure grown GaAs was poorer in mobility and activation compared to the high pressure material, it nevertheless had good homogeneity, low deep level concentrations, and excellent backgating characteristics.

2. Comparison of the high pressure grown GaAs from different suppliers showed that there are differences in the material which resulted in differences in doping profiles, mobilities, deep levels, backgating characteristics, and surface conversion.

3. Comparison of the substrates grown at different times from one supplier revealed that the vendor had changed the 'recipe' over the time period examined as the latest material showed worse backgating characteristics, lower diffusion, and entirely different substrate-induced deep levels.

4. Examination of the substrate which was rejected by a device manufacturer revealed that while it showed better controlled doping profiles and homogeneity, the sample had low electrical activation, high concentration of undesirable deep levels, and substantial backgating.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

In the work reported in this thesis a wide range of diagnostic tools including carrier concentration and drift mobility profiling in MESFETs, backgating, and deep level spectroscopic techniques were used to characterize commerically available undoped LEC GaAs. The following observations can be made:

1. Investigation of various GaAs substrates by OTCS revealed that eight traps, P1-P8, were present with P2 being a negative peak. The relative concentration of traps in high and low pressure grown GaAs were found to be different. The OTCS technique was found to be sensitive to GaAs surface treatment, for example, some peaks were attenuated in amplitude following surface etch, whereas the amplitude of the negative peak was increased after surface grinding. The OTCS spectra were affected by the sample geometry and type of electrodes. For future work, it is suggested that the amplitudes of the eight traps found here should be obtained as a function of position in a GaAs substrate with a scanning OTCS system now under construction in our laboratory. The results of this study can then be correlated with the dislocation density distribution.

2. Investigation of deep levels after silicon ion implantation by channel current DLTS revealed that process-induced defects appear in MESFETs furnace annealed with silicon dioxide encapsulant. Furnace annealing with PECVD silicon nitride cap, however, did not cause process-induced defects.

For future work it is suggested that deep levels in MESFETs annealed with and without cap using rapid thermal annealing (RTA) should be investigated. The results can shed light into the role of heating and cooling rates of the two annealing processes on defect generation.

3. Investigation of MESFETs fabricated identically on various LEC undoped GaAs revealed that some of them had defects which were not present in the starting material and may therefore be concluded to be substrate-induced. It is believed that stoichiometry differences in various substrates play a role in inducing defects after ion implantation and annealing. For future study it is suggested that surface analysis by Secondary Ion Mass Spectroscopy (SIMS) for example should be carried out in various substrates to investigate the relation between stoichiometry and substrate-induced defects.

4. It was concluded in chapter 5 that backgating is dependent on the type of GaAs material used. One of the samples which showed substantial backgating had a dominant hole trap which could have played a role. Other samples had different deep level compositions and showed different extents of backgating severity. To investigate whether backgating is influenced by traps, it is suggested for future work that the technique of channel current DLTS be modified to investigate deep levels at the interface of the channel and the semi-insulating substrate. The modification requires that a constant negative bias be applied to the gate of a MESFET so that the channel is nearly pinched off while electrical pulses are applied to the backgating electrode. The sampled region will thus include both sides of the channel substrate interface. The results of deep level spectra should clarify the

influence of traps on backgating.

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