C.1

ION IMPLANTED GaAs MESFET TECHNOLOGY

by

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ABSTRACT

The availability of high quality semi-insulating GaAs substrates is essential to the development of GaAs metal semiconductor field effect transistor (MESFET) integrated circuits. Problems have been encountered with horizontal Bridgman grown substrates since, for example, these must be doped with Cr to make then semi-insulating and the Cr tends to diffuse during device processing. Undoped semi-insulating GaAs substrates can be grown by the Liquid Encapsulated Czochralski (LEC) technique and allow the possibility of forming active regions by the process of implanting dopants directly into the substrate.

The purpose of this thesis was to develop at the University of British Columbia a GaAs MESFET technology based on direct ion implantation and to develop methods to assess undoped LEC substrates for Cominco Limited, Trail, B.C. A test device array consisting of structures for process, material, and device characterization was designed and then fabricated on Cominco wafers by a direct implantation process. Measurements on the test device array elements showed that this initial process could be used to produce MESFET's operational up to 3 GHz and that the test device array will be useful for monitoring future process developments and improvements. In addition, a channel conductance deep level transient spectroscopy system, a photocurrent deep level transient spectroscopy system, and a novel MESFET drain current hysteresis analysis system were developed to examine deep levels in GaAs and deep level trapping effects in GaAs MESFET's.

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1. INTRODUCTION

Gallium arsenide metal semiconductor field effect transistors (GaAs MESFET's) have shown considerable potential for use in high speed digital and monolithic microwave integrated circuits (IC's). For example, 8-12 GHz three and four stage amplifiers have been integrated (Wisseman et al., 1983) and large scale ($> 10^3$ gates) digital circuits realized (Eden, 1981), but before such IC's can become commercially viable and others of greater complexity developed, improved substrate growth and device fabrication techniques are required. One GaAs MESFET process technology (others are dicussed in Chapter 2) that appears very promising involves the use of multiple selective ion implantation directly into undoped semi-insulating GaAs substrates grown by the Liquid Encapsulated Czochralski (LEC) method.

The objectives of this thesis were to develop at the University of British Columbia a GaAs MESFET technology based on direct ion implantation and in conjunction with Cominco Limited, Trail, B.C. (a supplier of undoped LEC substrates) to develop methods to assess their GaAs for suitability in device fabrication. A test device array consisting of structures for process, material, and device characterization was designed. Undoped LEC substrates were obtained from Cominco and used to fabricate the array by a direct ion implantation process. Measurements were then performed on the array elements to assess the fabrications.

To further assist in material and process development three techniques for characterizing deep levels in GaAs were investigated as deep levels play an important role in substrate compensation (Appendix A) and can also cause

degraded device behaviour. The three techniques were channel conductance deep level transient spectroscopy for characterizing deep levels in implanted material, photocurrent deep level transient spectroscopy for characterizing deep levels in semi-insulating material and a novel technique for characterizing deep levels which cause the commonly observed effect of hysteresis (looping) in GaAs MESFET I-V characteristics.

Chapter 2 gives a brief overview of GaAs MESFET technology. Chapter 3 describes the test device array and the direct implantation process used in its fabrication while Chapter 4 describes the measurements performed to assess the fabrications. Chapter 5 describes the operation of and measurements performed with the DLTS systems and Chapter 6 the operation of and measurements performed with the hysteresis analysis system. Chapter 7 gives the summary and conclusions of this thesis.

2. OVERVIEW OF GaAs MESFET TECHNOLOGY

2.1 Introduction

Integrated circuits capable of operating at speeds in excess of 1 GHz are needed in microwave communication systems, high speed computers, optical fibre systems, and high speed test equipment. It is becoming increasingly difficult to extract more speed from Si devices and it is doubtful whether Si IC's can satisfy these needs. GaAs IC's have a two to six times potential speed advantage over Si IC's due in part to GaAs's higher electron mobility. Furthermore, since GaAs substrates may be grown in a semi-insulating state with resistivity near 10^8 Ωcm (compared with a theoretical 10^5 Ωcm for Si) and the GaAs retains its high resistivity after device processing, GaAs IC's can have low inter-device parasitic capacitances and simple inter-device isolation structure.

2.2 Device Considerations

GaAs MESFET's were proposed by Mead (1966) and first realized by Hooper and Lehrer (1967). They are the most widely used transistor in GaAs IC's. (Other choices include junction field effect transistors (JFET's) and metal insulator field effect transistors (MISFET's)). The basic structure of a GaAs MESFET consists of an n-type channel on a semi-insulating GaAs substrate, source and drain ohmic contacts and a metal gate contact which forms a Schottky junction with the channel (Fig. 2.1). The gate to source voltage governs the depth of the gate depletion region and hence the conductance of the channel. As the gate voltage is decreased, the depletion

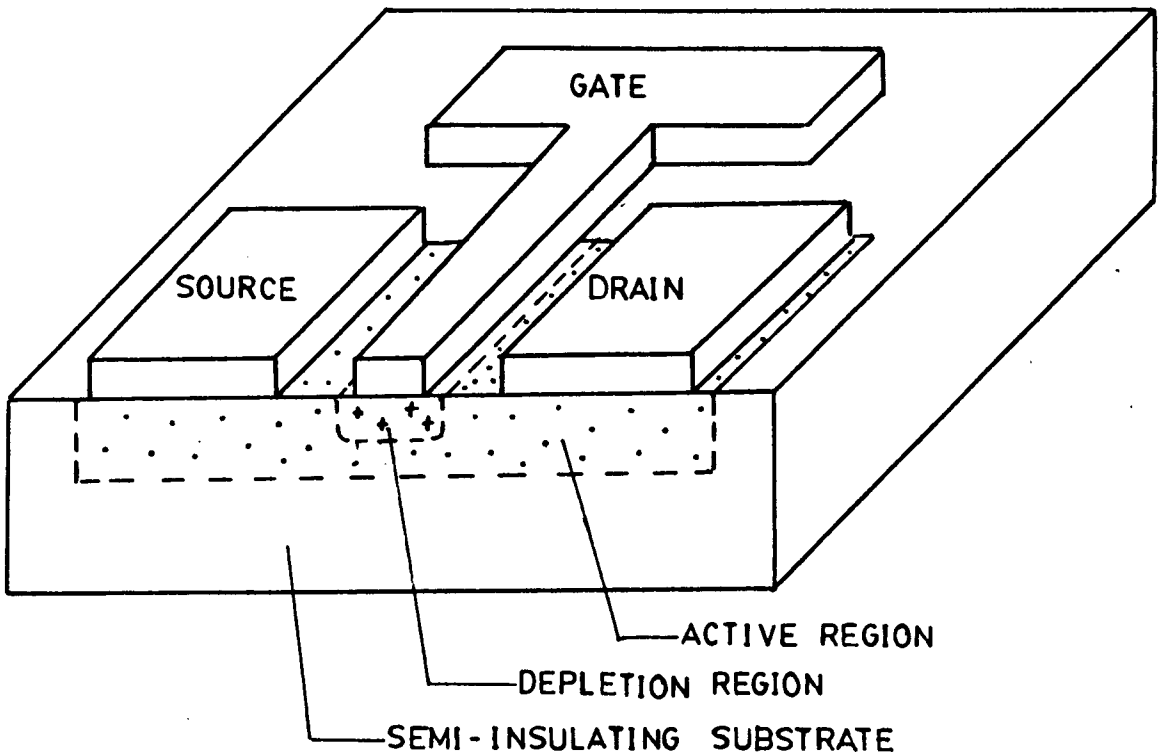


Fig. 2.1 GaAs MESFET

region expands and the channel conductance is reduced until eventually the channel becomes pinched-off. The maximum voltage on the gate (with respect to the source) required to cause pinch-off is called the threshold voltage V_T and is negative for a depletion (normally on) MESFET and positive for an enhancement (normally off) MESFET.

The first GaAs MESFET IC was reported by Van Tuyl and Liechti (1974). The circuit was a NAND/NOR logic gate and it operated three times faster than the fastest Si logic gate (at that time) thus demonstrating the high speed potential of GaAs IC's.

The structure and operation of a GaAs JFET is similar to that of the MESFET except that in a JFET a p^+n junction gate is used. MESFET's have been preferred over JFET's because JFET's have a larger gate sheet resistance and are more difficult to fabricate. Since the first GaAs JFET IC was reported by Notthoff and Zuleeg (1975), only relatively coarse gate length JFET IC's have been reported (i.e. 1.3 μm by Kato et al., 1981) while 0.5 μm gate length MESFET IC's have been fabricated (Barna and Liechti, 1979, Yamasaki et al., 1982). JFET's have a higher gate to channel built-in voltage than MESFET's (typically 1.4 V for JFET's to 0.8 V for MESFET's) and so (Lehovec and Zuleeg, 1980) can accommodate a larger forward bias and thus in digital circuits permit a larger logic voltage swing and noise margin, but again as pointed out by Lehovec and Zuleeg (1980) this advantage of JFET's over MESFET's will disappear if power supply levels in digital circuits are below 0.7 V as will be required for ultra-large scale ($>10^5$ gates) circuits. GaAs MISFET's have an insulating film between the gate and channel. The insulator must give good isolation, low surface state density, and long term device

stability. Several dielectrics have been tried, as reviewed by Boyd (1981), but a satisfactory insulator has not been found.

2.3 Substrate Considerations

Semi-insulating GaAs substrates have been grown by the horizontal Bridgman technique since the early 1960's. GaAs is synthesized in a quartz boat with elemental Ga and As vapour inside a furnace. The GaAs melt is then cooled by slowly moving the boat away from the furnace. Prior to cooling Cr is added to the melt. The Cr introduces a deep level in GaAs which compensates the shallow impurities found to contaminate the melt (Martin et al., 1980).

In the LEC substrate growth technique a GaAs melt is contained in a quartz or pyrolitic boron nitride (PBN) crucible. The melt is encapsulated with B_2O_3. To grow a GaAs ingot a seed is immersed into and then slowly pulled from the melt. The LEC technique was used more than twenty years ago by Metz et al. (1962) but commercial LEC crystal growth equipment has only recently been available (1979).

An attractive feature of the LEC method is that round wafers are produced compared to the D shaped wafers produced by the Bridgman method. A second feature of the LEC method is that semi-insulating wafers may be reproducibly attained without the need for intentional Cr doping as shallow impurities in this material are compensated via an intrinsic deep level formed during crystal growth (Appendix A).

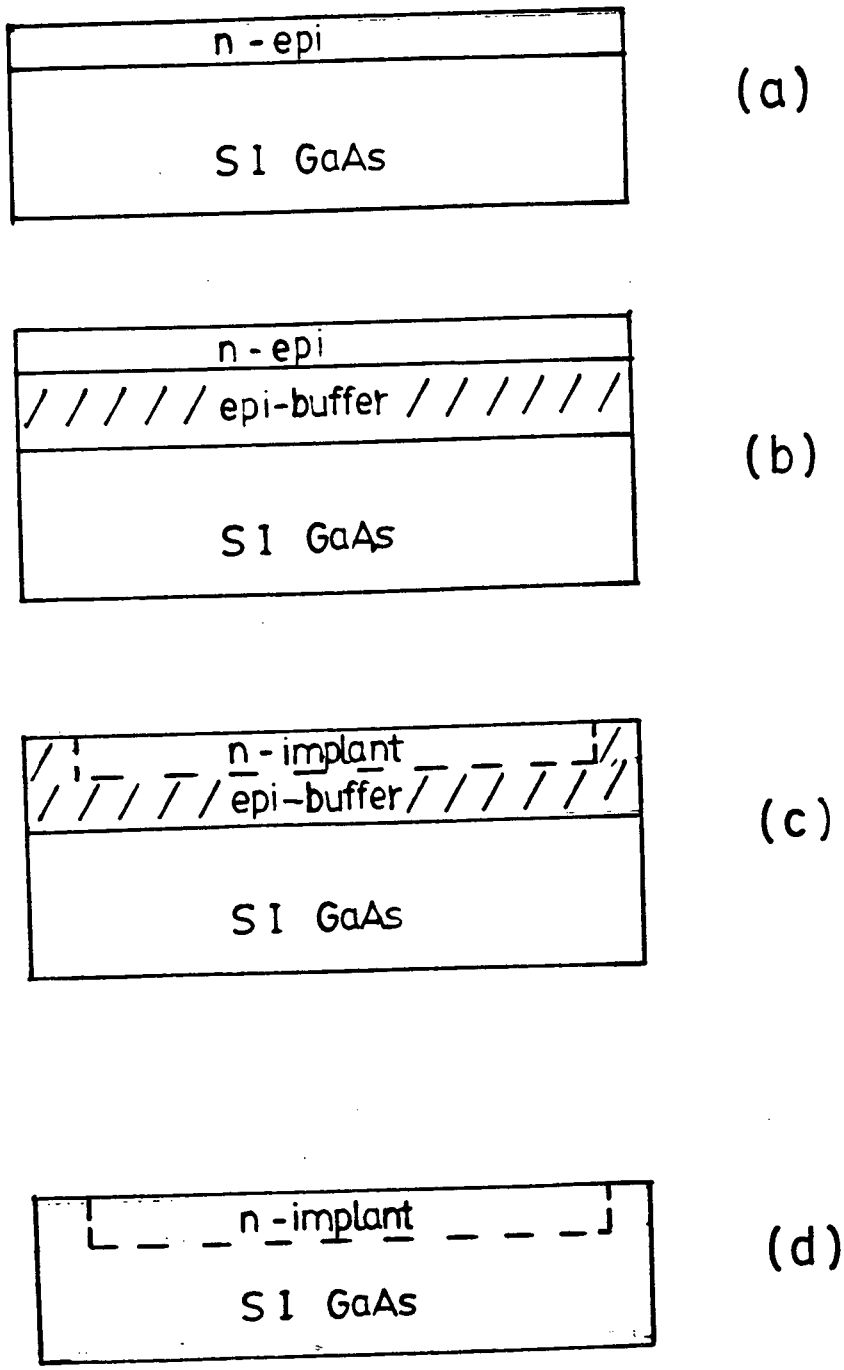


Fig. 2.2 Comparison of active layer formation processes (a) Epitaxial growth (b) Epitaxial growth on buffer layer (c) Implantation into buffer layer (d) Direct ion implantation

2.4 Process Considerations

Difficulties encountered with Bridgman substrates (such as the degradation of active layer properties due to Cr impurity diffusion, Udagawa et al., 1980) lead to the development of GaAs MESFET fabrication processes in which high resistivity epitaxial buffer layers are grown on a substrate and active layers formed by a second epitaxial growth (Fig. 2.2b) or by ion implantation into the buffer layer (Fig. 2.2c). With LEC substrates, however, active layer formation by direct ion implantation (Fig. 2.2c) appears possible (Welch et al., 1980).

Attractive features of direct ion implantation include: high throughput (no epitaxial growth required), the fact that selective implantation may be performed (in which only certain parts of a wafer are implanted) alleviating the need for inter-device isolation procedures ("planar" technology), and the fact that multiple and multiple selective implantations may be performed. Recently reported direct implantation processes are summarized in Appendix B.

3. THE TEST DEVICE ARRAY

3.1 Description

A test device array designed for use in evaluating GaAs integrated circuit processing and material properties is illustrated in Fig. 3.1. Included in the array, which is partly based on that of Immorlica et al. (1980), are a Schottky diode for carrier density profiling, van der Pauw cross structures for use in Hall effect measurements, (David and Buehler, 1977), a long gate MESFET ("fat FET") for drift mobility profiling, pads for checking substrate isolation and ohmic contact resistance, a structure for measuring gate metal resistance, and a set of narrow gate length MESFET's (1-10 μm) for use in device characterization (Table 3.1).

Table 3.1 - Test Device Array Structures

STRUCTURE	NAME	PURPOSE	DESCRIPTION
1	Schottky diode	n-implant carrier density profiling	Gate dimension=100x200 μm
2	Substrate isolation pads	Test of substrate isolation	(Ohmic) metal pads on SI substrate Pad dimension=100x100 μm Pad separations=40,20,10 μm
3	van der Pauw cross	Measurement of Hall mobility and sheet resistance of n-implant	Length of cross=200 μm Width of cross=40 μm
4	van der Pauw cross	Measurement of Hall mobility and sheet resistance of n^+-implant	Length of cross=250 μm Width of cross=40 μm

...continued

STRUCTURE	NAME	PURPOSE	DESCRIPTION
5	Ohmic contact pads	Measurement of ohmic contact resistance	Ohmic metal pads on implanted layer Pad dimension=100x100 μm Pad separations=40,20,10,5 μm
6	Gate metal structure	Measurement of gate metal sheet resistance	Number of squares=50
7	Split gate MESFET	Device Characterization	Gate length=4 μm
8	Fat FET	Drift mobility profiling	Long gate MESFET Gate dimension=100x200 μm
9	1 μm MESFET	Device characterization	Gate width=200 μm
10	2 μm "	" "	" " "
11	3 μm "	" "	" " "
12	4 μm "	" "	" " "
13	4 μm "	" "	" " "
14	6 μm "	" "	" " "
15	8 μm "	" "	" " "
16	10 μm "	" "	" " "
17	Dual gate MESFET	" "	Gate length=4 μm
18	MIM capacitor	Test of dielectric properties	
19	Coarse registration mark	Mask alignment aid	

Six masks were designed for use in fabricating the array via a multiple direct selective ion implantation approach (registration etch mask,

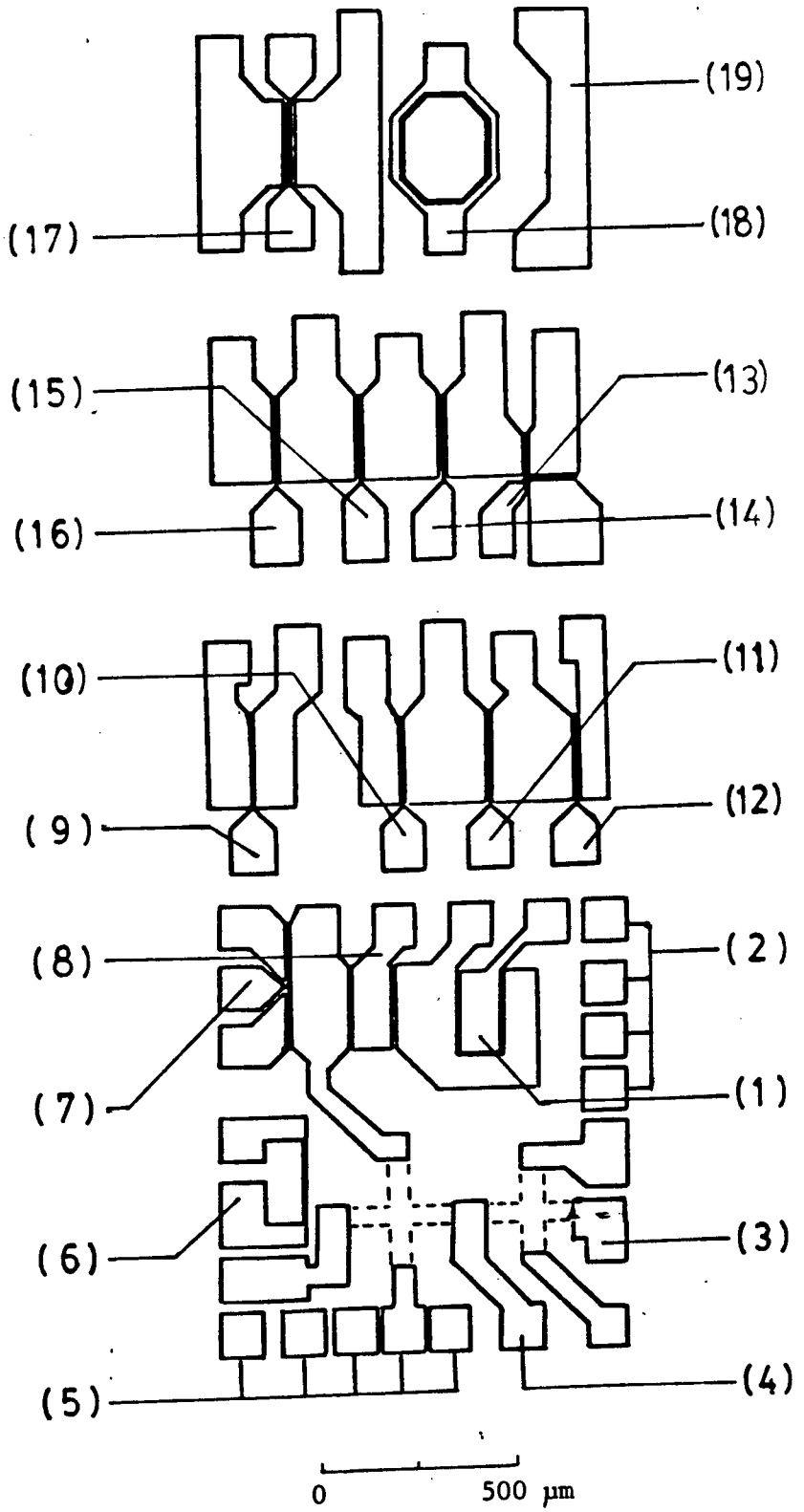


Fig. 3.1 Layout of the test device array

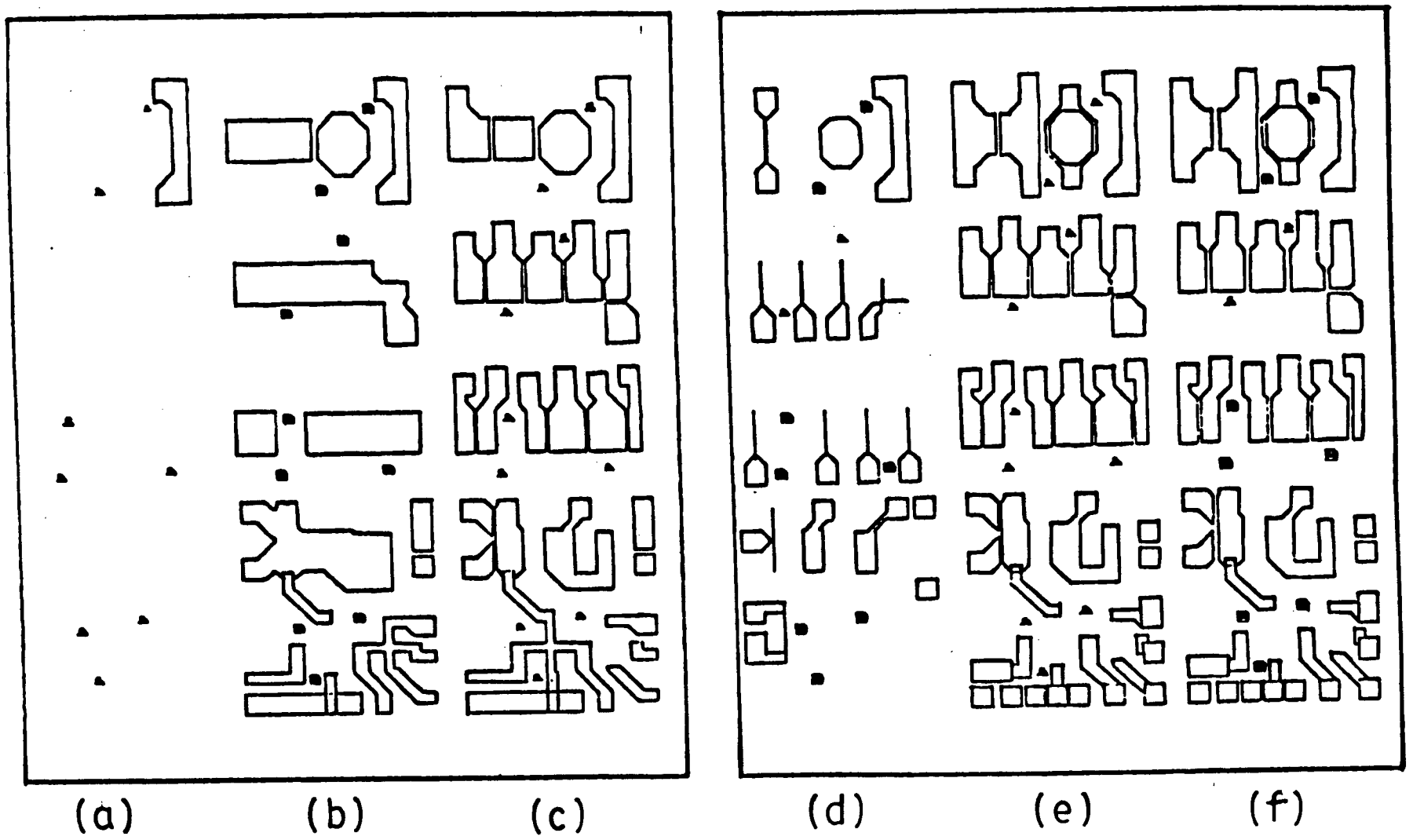


Fig. 3.2 The masks for the test device array (a) Registration marks (b) n-implant (c) n^+-implant (d) Gate metal (e) Ohmic contacts (f) 2nd layer metal

n-implant mask, n^+implant mask, ohmic contact metallization mask, gate metallization mask, and second level metallization mask). To prepare the masks, designs were entered into the U.B.C. Computing Centre's Amdahl using a program written by G. Cheng. The files were then downlinked to a PDP8e in the Electrical Engineering Department and a rubylith master cut under control of this program. The rubylith was sent to Precision Photomask, Quebec, for fabrication of the photographic (stepped and repeated) masks. To reduce production costs the required six pattern were grouped into two masks as shown in Fig. 3.2. With this arrangement about 150 replications of the 1.0 x 3.3 mm array can be made on a 50 mm diameter wafer.

3.2 Fabrication

3.2.1 Substrate Preparation

Semi-insulating GaAs wafers were obtained from Cominco Limited in order to carry out an initial fabrication run of the test device array. The wafers were LEC grown and undoped. The diameter of each wafer was 50 mm, the thickness 0.50 mm, and the crystal orientation (100).

The process used to fabricate the wafers began with the following precleaning procedure (Fig. 3.3a).

1. A three part degreasing consisting of a 5 minute trichlorethylene bath, a 5 minute boiling acetone bath, and finally a 5 minute boiling isopropanol bath.
2. An etch to remove any work damage introduced during wafer sawing and polishing. The etch consisted of a 3 minute immersion in $4H_2SO_4:1H_2O_2:1H_2O$ followed by a 10 minute DI water rinse.

3. A native oxide etch consisting of a 10 minute immersion in boiling concentrated HCl followed by a 10 minute DI water rinse.

3.2.2 Selective Ion Implantation

Following cleaning, an SiO_2 film of 0.6 μm thickness was deposited on the wafers to serve as a mask in the selective ion implantation process (Fig. 3.3b). A Perkin-Elmer 3140 RF sputtering system was used with an SiO_2 target. The sputtering gases were Ar, 34 millitorr, and O_2, 4 millitorr. (O_2 helps preserve the stoichiometry of the films). For a forward power of 150 W the deposition rate was found to be about 0.15 μm/hr.

In the next process step, windows were opened in the SiO_2 to permit the etching of registration marks in the substrates (Fig. 3.3c). These marks are necessary in order to locate those regions of the wafer which have been implanted. The following procedure was used:

1. A photoresist procedure (using the registration mark mask) consisting of photoresist deposition (Shipley AZ1350J), a 30 minute 70° bake, mask alignment and exposure using a Kasper aligner, photoresist development, a 10 minute DI water rinse, and finally a 60 minute 120°C bake.
2. An SiO_2 etch consisting of a 5 minute immersion in a buffered oxide etch (NH_4+HF) and an immersion in acetone to remove the photoresist.
3. A substrate etch consisting of a 1 minute immersion in 10% HCl, a 1 minute DI water rinse, a 50 s immersion in 5% H_3PO_4 2.5% H_2O_2 (to remove approximately 0.1 μm of the substrate), and a 5 minute DI water rinse.

Next, a second set of windows were opened in the SiO_2 to define the regions of the wafers to be implanted (Fig. 3.3d). This was accomplished

using the photoresist procedure (with the n-implant mask) and the SiO_2 etch procedure described above. ^{29}Si was implanted at an energy of 100 keV to a dose of $3x10^{12}cm^{-2}$ (Fig. 3.3e). The implantations were done by Optotek Limited, Ottawa, using an Extrion 200 (since facilities were not yet available at U.B.C). To reduce fabrication time and complexity n^+ implantations and second level metallization were not done. (n^+ implantation is used to reduce ohmic contact resistance. Second level metallization is used to achieve low resistance interconnects).

3.2.3 Post-Implant Anneal

Following implantation the implant mask was stripped using a 10 minute buffered oxide etch. An SiO_2 layer, 0.17 μm thick, was then deposited (by RF sputtering) to serve as an anneal cap (Fig. 3.3f). Annealing was done in a Mini Brute furnace in the following manner:

1. The furnace temperature was set to 850° and gas flow 14 liter/minute N_2 and 1 liter/minute H_2 established.
2. The wafers were placed at the front of the furnace for 5 minutes.
3. The wafers were placed at center of the furnace for 20 minutes.
4. The wafers were placed at the front of the furnace for 5 minutes to complete the anneal.

The encapsulant was then stripped using buffered oxide etch (Fig. 3.3g).

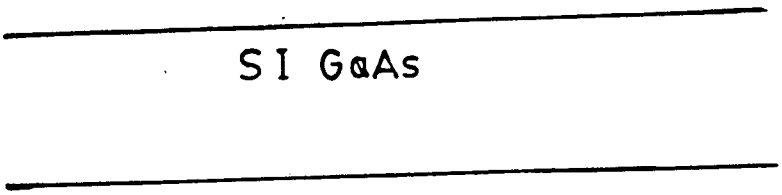
3.2.4 Metallization

In the next stage, ohmic metallization, the single step liftoff technique of Hatzakis (1980) was used. The following steps were performed:

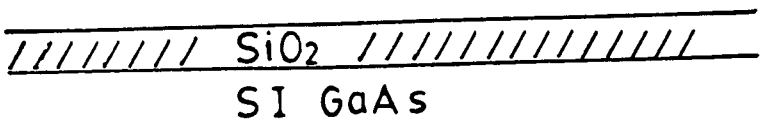
1. Degreasing (as described in Section 3.2.1),
2. Photoresist deposition, Shipley AZ1350J, (Fig. 3.3h),
3. A prebaking at 70°C for 30 minutes,
4. Ohmic contact mask alignment and exposure (Fig. 3.3i),
5. A soaking in 26.0°C chlorobenzene for 2 minutes followed by photoresist development. (The chlorobenzene increases the strength of the top layer (Fig. 3.3j) to the developer so that an undercut edge profile (Fig. 3.3k) results upon photoresist development.)
6. Thermal evaporation of AuGe (88% Au, 12% Ge) to thickness of 300 nm using VEECO VE400 (Fig. 3.3l).
7. Removal of unnecessary metal by immersion in acetone, liftoff, (Fig. 3.3m).

The ohmic contacts were then alloyed for 1 minute in a Mini Brute furnace preheated to 450°C (to create an n^+ region beneath the contacts).

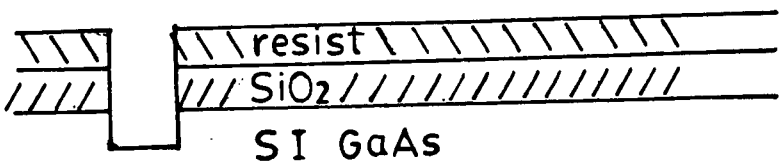
In the final process step, gate metallization, the liftoff procedure was used with the gate metal mask. In this process Al was deposted to 0.5 μm thickness by thermal evaporation using a VEECO VE400 (Fig. 3.3n).



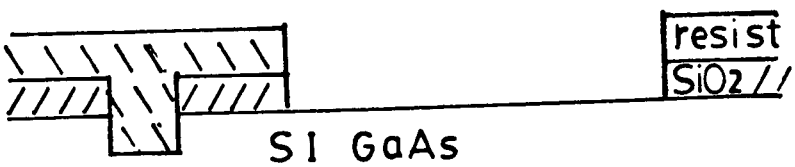
(a) Wafer preclean



(b) Implant mask deposition

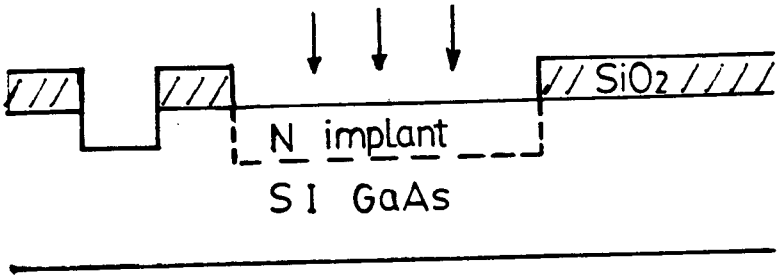


(c) Etch of registration marks

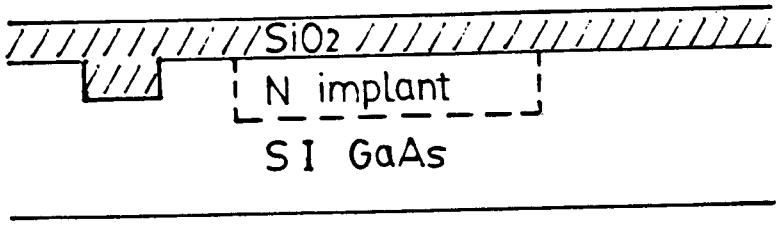


(d) Opening of windows for implant

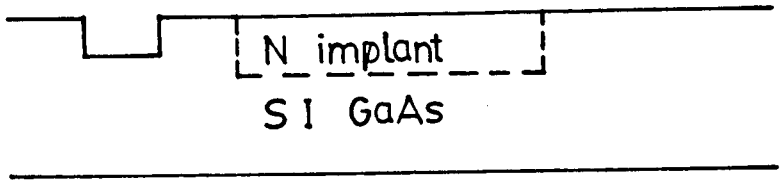
Fig. 3.3 Fabrication sequence for the test device array



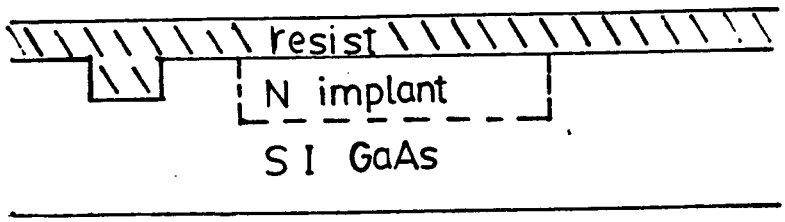
(e) Implantation



(f) Encapsulation and annealing

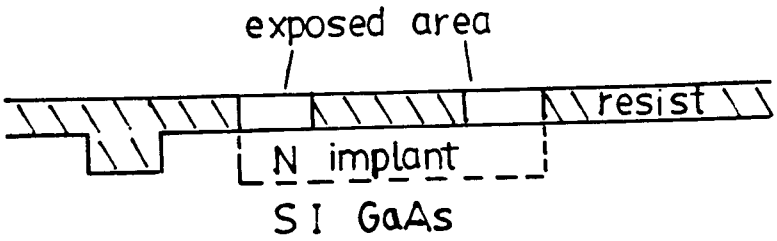


(g) Wafer clean

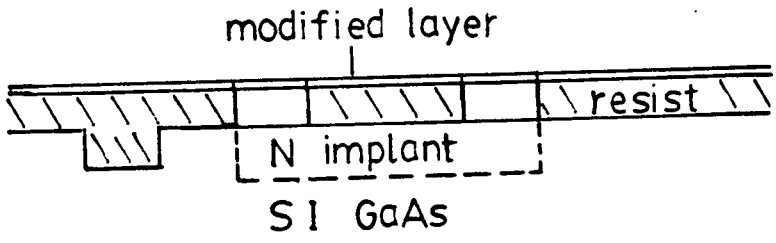


(h) Photoresist deposition

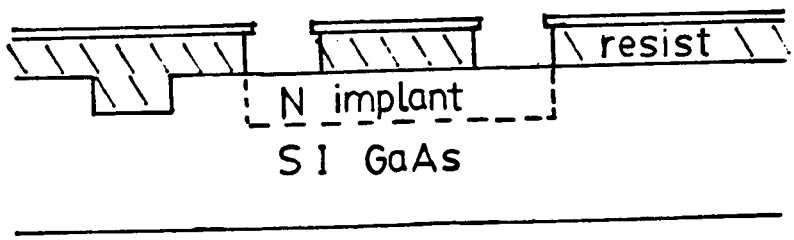
Fig. 3.3 cont'd.



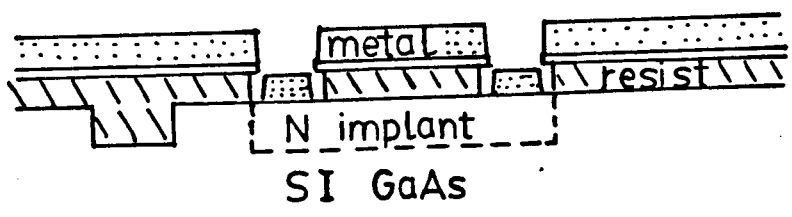
(i) Photoresist exposure



(j) Chlorobenzene soak

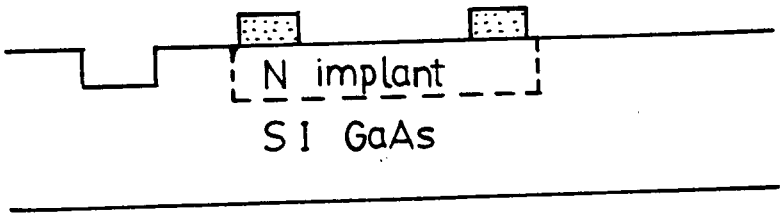


(k) Photoresist development

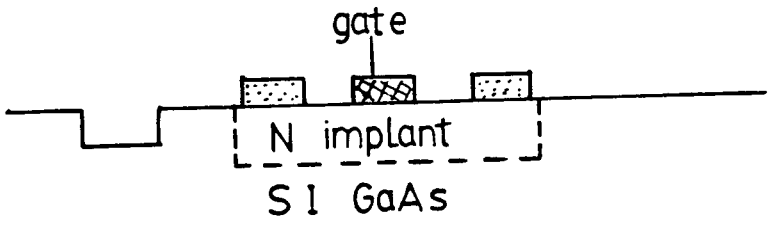


(l) Source-drain metallization

Fig. 3.3 cont'd.



(m) Removal of photoresist



(n) Gate metallization

Fig. 3.3 cont'd.

4. MEASUREMENTS ON THE TEST DEVICE ARRAY

4.1 Active Layer Evaluation

To assess the direct implantation and annealing process described in Sections 3.2.2 and 3.2.3 the following properties of the implanted regions were examined: sheet resistance, Hall mobility, activation, carrier density profile, and drift mobility profile.

Sheet resistance, Hall mobility, and activation measurements were made using the van der Pauw cross (structure #3, Fig. 3.1). Samples were placed in a magnetic field B (0.2T) directed normal to the cross (Fig. 4.1a). An Alpha Scientific 7500-W magnet and power supply were used. A current I (200 μA) was established between opposite terminals of the cross (i.e. between terminals B and D, Fig. 4.1b) using a HP 6186B current source and the Hall voltage V_H across the other terminals (i.e. between terminals A and C) measured (with a Fluke 8050 voltmeter). Average Hall mobility μ_H was then calculated using

$$\mu_H \approx \left| \frac{V_H}{R_s B I} \right| \tag{4.1}$$

where R_s is the active layer sheet resistance (van der Pauw, 1958). To determine R_s a current I' (0-1 mA) was established across adjacent terminals (A and D) (with no applied magnetic field) and the voltage V' across the other terminals (B and C) measured. R_s was then calculated using (van der Pauw, 1958)

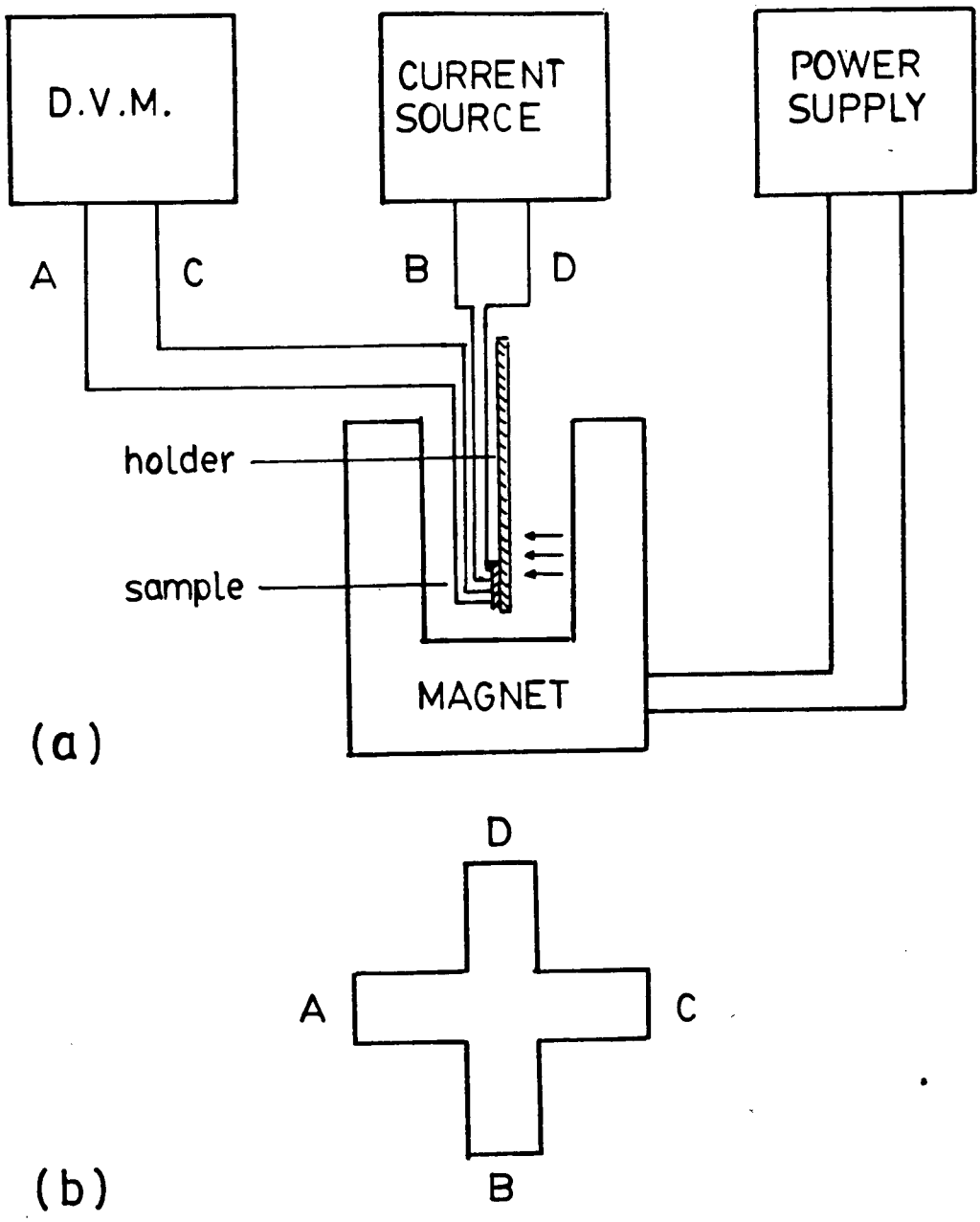


Fig. 4.1 Experimental arrangement used for van der Pauw measurements (a) Apparatus (b) van der Pauw cross

$$R_s \simeq \left| \frac{\pi}{\ell n 2} \frac{V'}{I'} \right| . \qquad (4.2)$$

Activation, η, was estimated using

$$\eta = \frac{\text{measured sheet electron concentration}}{\text{implanted dose}} = \frac{1}{Dq\mu_H R_s} \qquad (4.3)$$

where q is the elementary charge and D the implanted dose.

Carrier density profiles were determined by the capacitance-voltage technique in which the capacitance of a Schottky diode (structure #1, Fig. 3.1) was measured as a function of reverse bias, V, and the profile, N(x), then given by (e.g. Sze, 1981)

$$N(x) = \frac{2}{q\varepsilon A^2} \left[\frac{d(1/C^2)}{dV}\right]^{-1} \qquad (4.4)$$

where ε is the permittivity of GaAs ($\sim 1.16 \times 10^{-10}$ F/m), A the diode area and x the depth below the surface ($x = \varepsilon A/C$). C which was measured with a 1 MHz capacitance meter (Boonton 71A) was recorded under PDP8e computer control using the system of Boyd (1980) and program MESCV written by Ji Lijiu. The arrangement used to perform the profilings is shown in Fig. 4.2.

Drift mobility profiles were measured with the fat FET's (structure #8, Fig. 3.1) using the method of Pucel and Krumm (1976). A fat FET was biased in its linear region (V_{DS} = 50 mV) and the modulation i_d in its drain current resulting from the application of a small-signal gate-source voltage

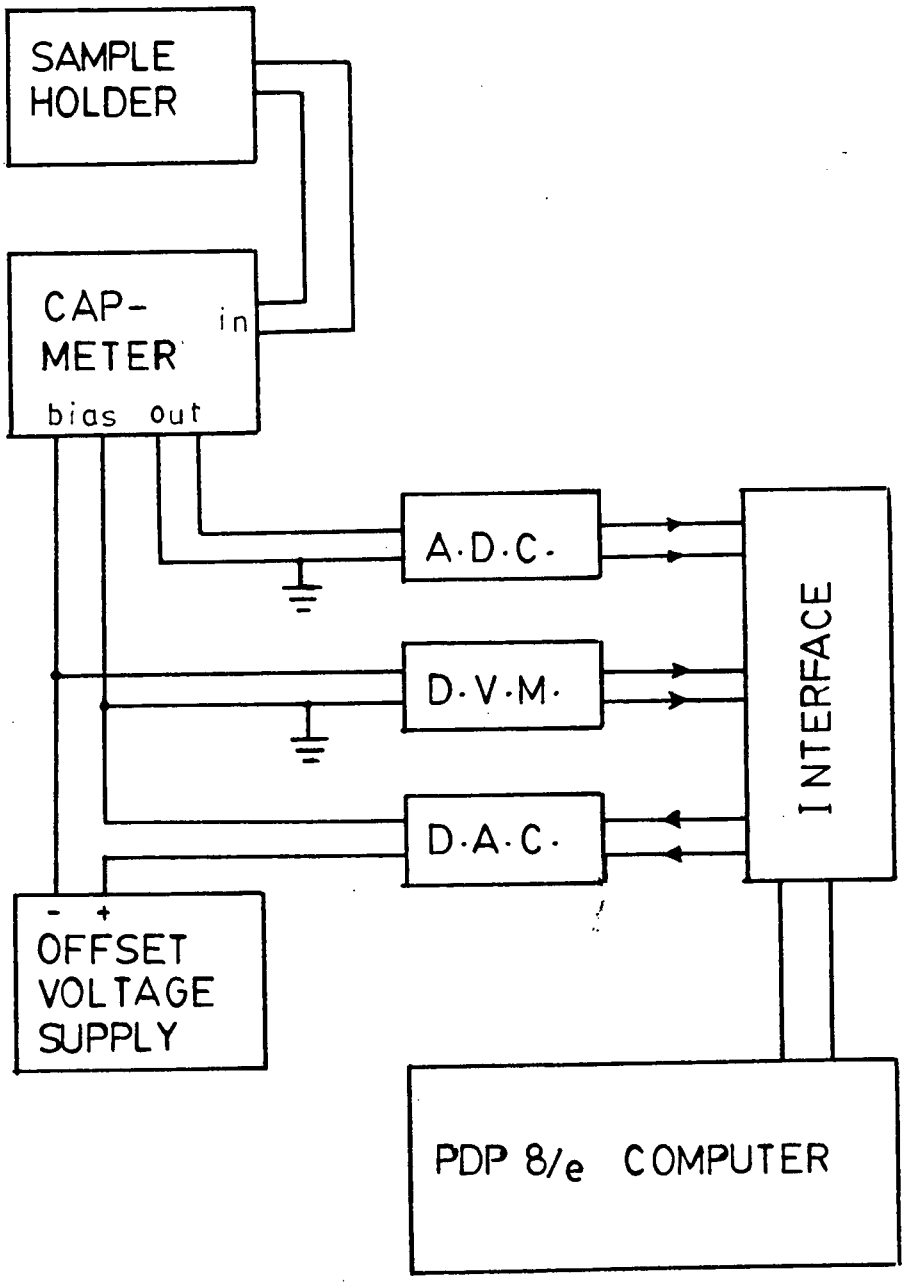


Fig. 4.2 Experimental arrangement used for C-V measurements

v_{gs} (20 mV_{RMS}) recorded as a function of the DC gate-source bias V_{GS}. Drift mobilities $\mu_n(x)$ were then calculated using

$$\mu_n(x) = \frac{L^2 i_d}{CV_{DS} v_{gs}} \tag{4.5}$$

where L is the gate length and C the gate capacitance (determined by C-V measurements). v_{gs} was derived from a sine wave generator (IEC F63) while a lock-in amplifier (PAR 5204) was used to provide an output proportional to i_d/v_{gs}. The apparatus used to implement the profilings is shown in Fig. 4.3.

Sheet resistance values are tabulated in Fig. 4.4. A typical C-V plot is shown in Fig. 4.5 and carrier density and drift mobility profile in Fig. 4.6. Table 4.1 summarizes the active layer parameters. From the results the following comments can be made:

1. Drift mobility is seen to increase towards the substrate. This behaviour has been shown by Immorlica et al. (1981) to correlate with good RF performance in their ion implanted GaAs power MESFET's while devices which displayed a decreasing drift mobility profile were found to exhibit slow pulse response of drain current to applied gate voltage and premature saturation of output power.
2. Liu et al. (1980) have calculated the theoretical implant range R_p and straggle ΔR_p for 100 KeV Si implantation into GaAs to be 86 nm and 38 nm respectively, so that it appears that broadening has occurred during annealing.

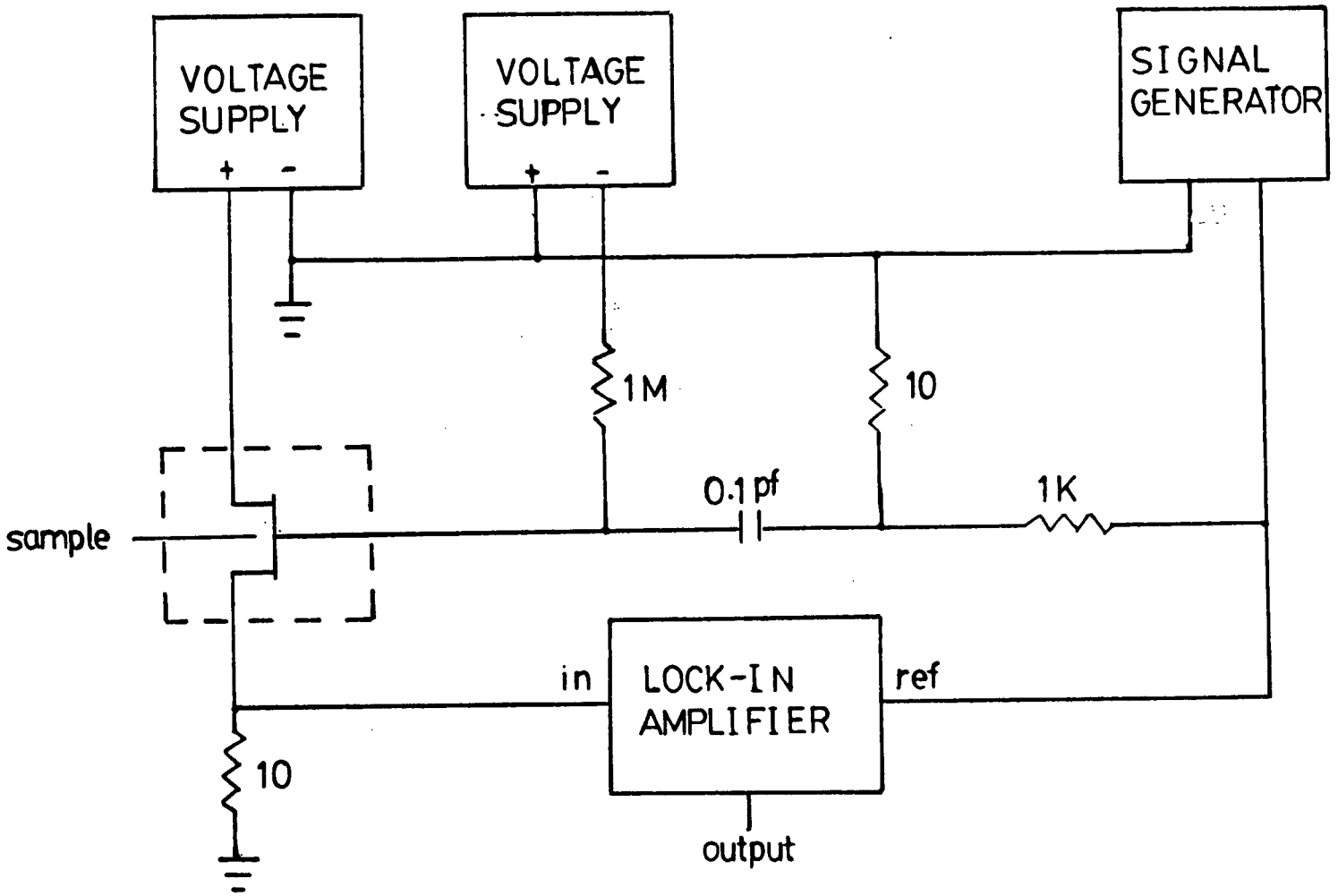


Fig. 4.3 Experimental arrangement used for drift mobility profiling

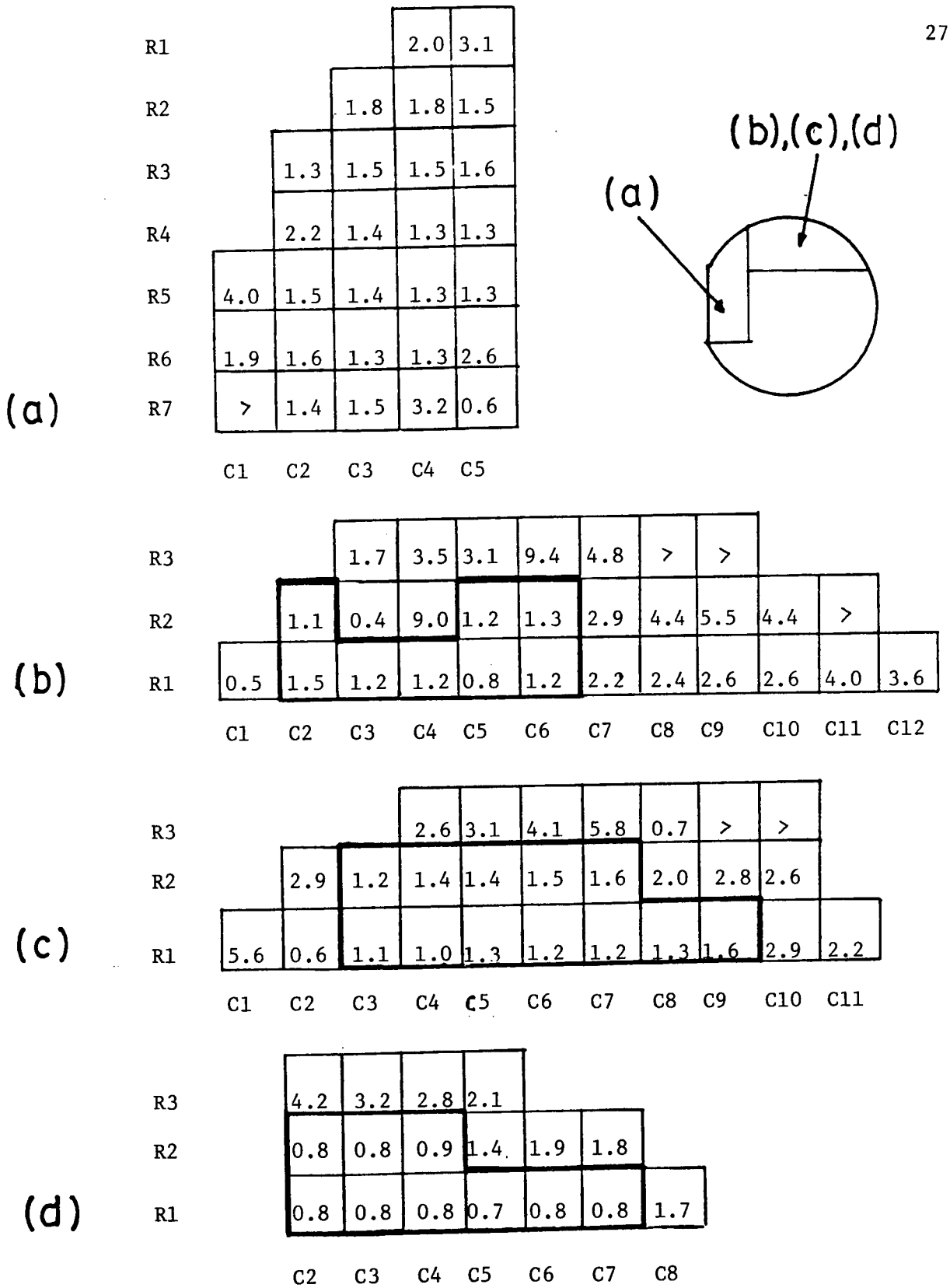


Fig. 4.4 Active layer sheet resistance values for wafer sections fabricated (in kΩ/□ , > =R >10 kΩ/□) (a) Wafer 94-S13 (b) Wafer 43-S10 (c) Wafer 123-S131^{S} (d) Wafer 51-T132

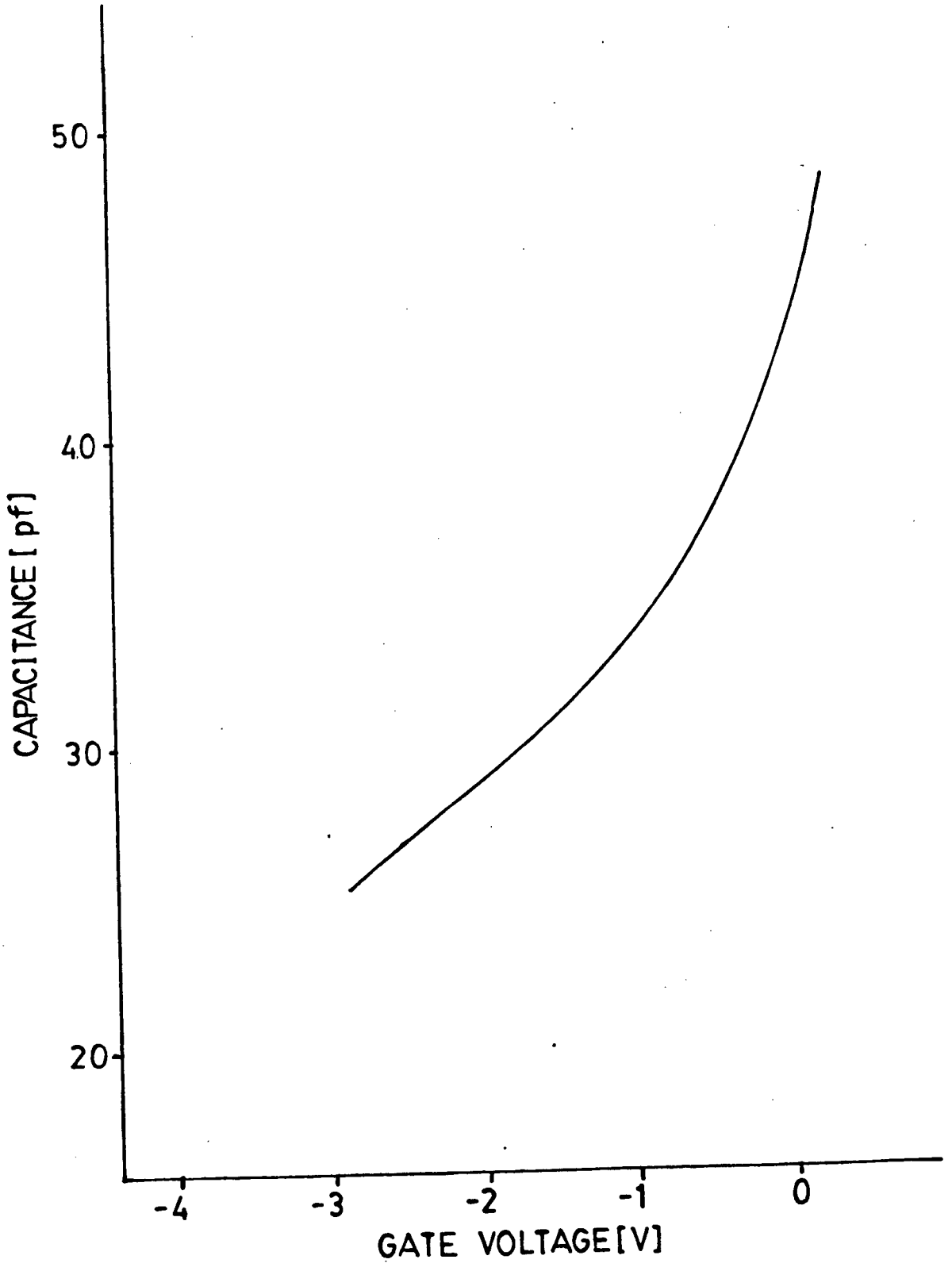


Fig. 4.5 C-V plot for sample 123-S131 (R1-C5)

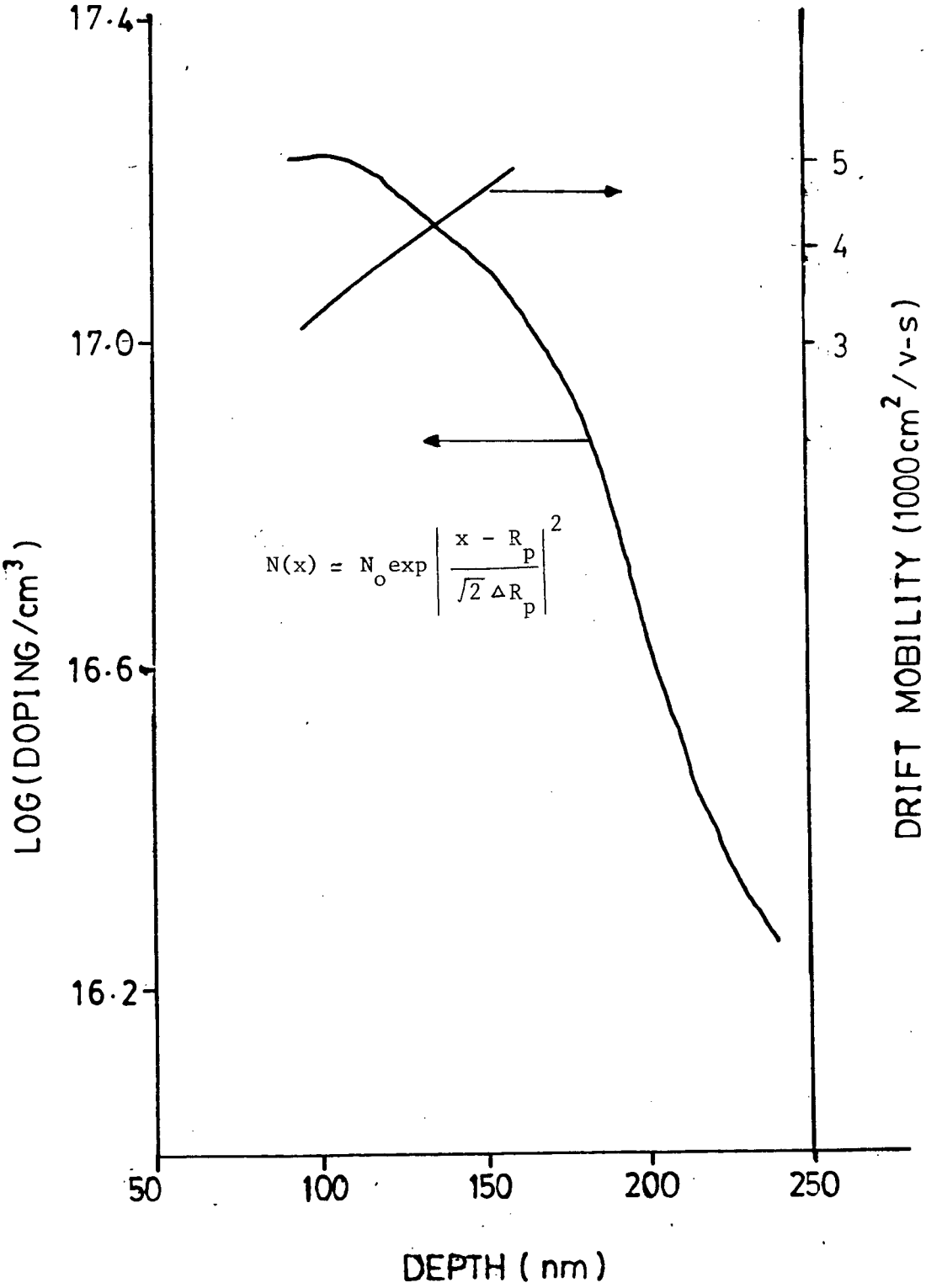


Fig. 4.6 Carrier density and drift mobility profile for sample 123-S131 (R1-C5)

Table 4.1 - Active Layer Properties

Sample		43-S10 (R2-C6)	123-S131 (R1-C5)	51-T132 (R1-C3)
Sheet Resistance, R_s	[kΩ/□]	1.3	1.3	0.8
Hall Mobility, μ_H	[cm^2/Vs]	$3.3x10^3$	$3.3x10^3$	$3.6x10^3$
Percent Activation, η	[%]	49	50	74
Peak Doping, N_o	[cm^{-3}]	$1.5x10^{17}$	$1.6x10^{17}$	$1.9x10^{17}$
Implant Range, R_p	[nm]	102	100	107
Implant Staggle, ΔR_p	[nm]	69	54	69

3. Activations obtained can be compared to those of Immorlica et al. (1980) for $3x10^{12}cm^{-2}$ Si implants who report η's from 67-74%.
4. The average R_s for wafer 51-T132 is lower than of wafers 43-S10 and 123-S131. (The first number in the wafer designation specifies the ingot from which the wafer was cut while the second number specifies the wafer position with respect to either the seed S or tail T of the ingot). This result may reflect the fact that ingot 51 was found by Cominco to be thermally unstable showing a resistivity drop from $1.8x10^8$ Ωcm to $1.1x10^4$ Ωcm following a 30 minute 850°C anneal.

4.2 Gate Metallization Evaluation

To assess the gate metallization process described in Section 3.2.4 the following properties were examinated: current-voltage characteristics, barrier height, ideality factor, (gate metal) sheet resistance, lithographic definition.

Schottky diode current-voltage characteristics were measured on a Tektronix 577 curve tracer. Barrier heights ϕ_B and ideality factors n were then derived from the forward characteristics since for V>3kT/q Schottky diode current density J is approximated by:

$$J = A^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \exp\left(\frac{qV}{nkT}\right) \tag{4.6}$$

where A* is an effective Richardson constant ($A^*=8.7\ Acm^{-2}K^{-2}$ for n type GaAs, Crowell et al., 1965) T the diode temperature, and k Boltzmann's constant so that

$$\phi_B = \frac{2.30\ kT}{q} \log \frac{A^*T^2}{J_s} \tag{4.7}$$

and

$$n = \frac{q}{2.30\ kT} \cdot \frac{dV}{d(\log J)} \tag{4.8}$$

where J_s is an extrapolated current density at zero bias (Fig. 4.7). Gate

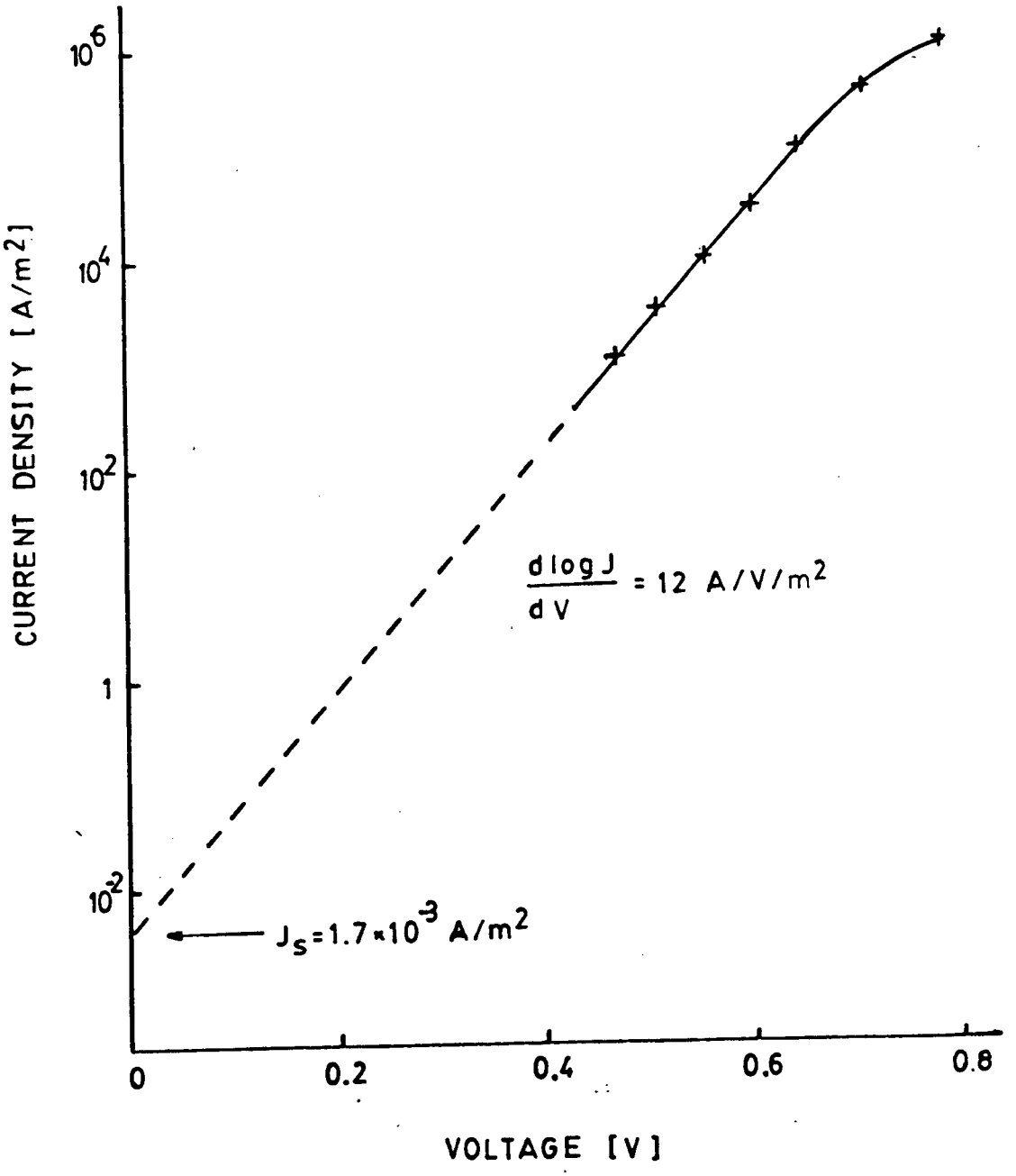


Fig. 4.7 Schottky diode current-voltage plot for sample 123-S131 (R1-C5).

metal sheet resistances R_{SG} were estimated by measuring the resistance between the terminals of the gate metal structure (structure #6, Fig. 3.1) (by a current voltage technique). Photolithographic definition of the gate metallization was checked using a scanning electron microscope (SEM).

Table 4.2 lists values of barrier height, ideality factor and sheet resistance. An SEM photograph of a 3 μm MESFET (structure #11, Fig. 3.1) is shown in Fig. 4.9. The following comments can be made:

1. The high ideality factors obtained may be a result of improper cleaning prior to metallization as Miers (1982) has found that ideality factors varied from 1.08 to 1.33 depending on surface treatment.
2. Barrier heights obtained are consistent with the commonly accepted values for metals on n-type GaAs (see, for example, Sze, 1981).
3. The gate length of the 3 μm MESFET is close to 4 μm and the gate definition is poor indicating the need for an improved mask alignment technique.

Table 4.2 - Metallization Properties

Sample		43-S10 (R2-C6)	123-S131 (R1-C5)	51-T132 (R1-C3)
Schottky Barrier Height, ϕ_B	[eV]	0.74	0.73	0.73
Schottky Barrier Ideality Factor, n		1.3	1.4	1.3
Gate Metal Sheet Resistance, R_{SG}	[Ω/□]	0.2	0.2	0.2
Ohmic Contact Resistance, R_c	[mΩcm^2]	0.27	0.32	0.22

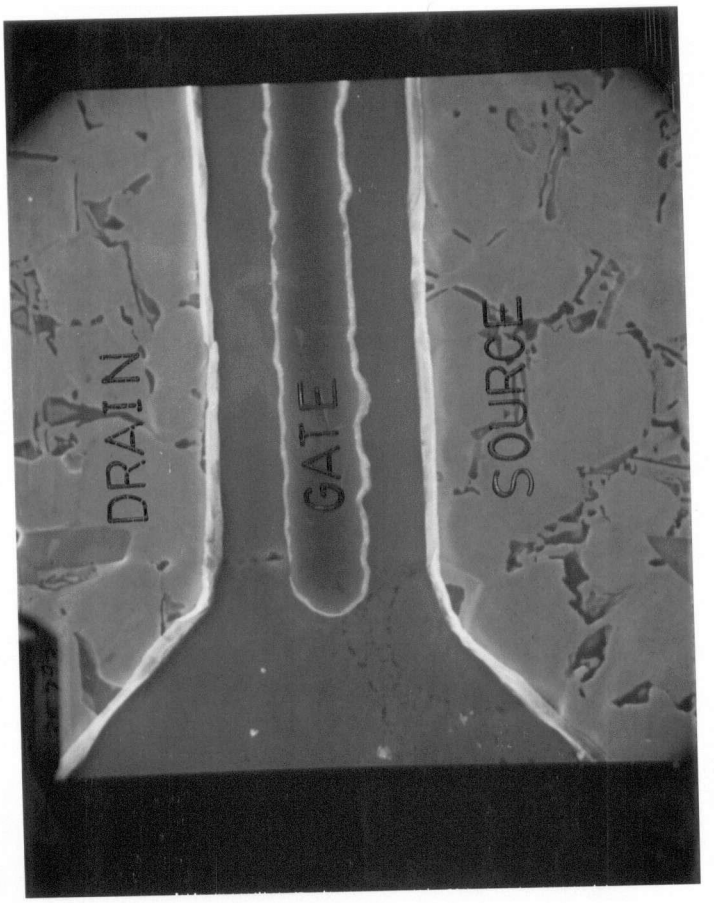


Fig. 4.8 SEM photograph (2000X mag.) for 3μm MESFET sample 123-S131 (R2-C5)

4.3 Ohmic Contact Metallization Evaluation

To assess the ohmic contact metallization process described in Section 3.2.4 measurements were made of specific ohmic contact resistance by the method of Berger (1972). The resistance r_{ij} between adjacent ohmic contact pads i and j (structure #5, Fig. 3.1) was measured and R_c (the contact resistance of a pad) determined by a linear regression of

$$r_{ij} = 2R_c + \frac{R_s}{w} \ell_{ij} \tag{4.9}$$

where ℓ_{ij} is the separation between pads i and j and w is the width of the pads.

Values obtained for specific contact resistance are listed in Table 4.2. Since for microwave FET's specific contact resistances of 10^{-5} Ωcm^2 or less are desirable (Gupta et al. 1983) ohmic contacts of lower resistance are required. Use of the high dose n^+ implant under source and drain regions (i.e. mask C Fig. 3.2) should rectify the situation.

4.4 MESFET Evaluation

To test the operation of the devices produced in the fabrications, characteristics of the narrow gate MESFET's (structure #9-12, 14-16, Fig. 3.1) were checked on a Tektronix 577 curve tracer. From these measurements it was found that operational 2-10 μm devices can be produced but that improved photolithographic tools are required to produce the 1 μm devices (Table 4.3). (A device was deemed operational if it showed I_{DS} saturation

and could be pinched-off to 100 μA). Fig. 4.9 shows a typical I_{DS}-V_{DS} characteristic and Fig. 4.10 a I_{GS} -V_{GS} characteristic.

Table 4.3 - MESFET Yield

Wafer	94-S13	43-S10	123-S131	51-T132	Total
# Devices	27	26	25	17	95
10 μm Gate	.70	.50	.84	.88	.72
8 " "	.52	.38	.76	.94	.62
6 " "	.48	.23	.80	.76	.54
4 " "	.59	.50	.72	.71	.62
3 " "	.59	.46	.76	.76	.63
2 " "	.48	.35	.64	.76	.54
1 " "	0	0	0	.12	.02
TOTAL	.48	.35	.65	.71	.53

Table 4.4 lists the DC characteristics of various 3 μm MESFET's. The AC behaviour of three of these devices (123-S131 R1-C8, 51-T132 R1-C6, and 43-S10 R2-C5) were checked over the frequency range 2-5 GHz on a HP8409 network analyzer (at Microtel Pacific Research, Burnaby, B.C.) and found to have a cutoff frequency of about 3 GHz. This result is reasonable considering the high ohmic contact resistance and large gate-source separation ($\sim$ 4 μm) in the devices. The theoretical cutoff frequency for an intrinsic 3 μm MESFET having no parasitic components is about 10 GHz (Pucel et al., 1975).

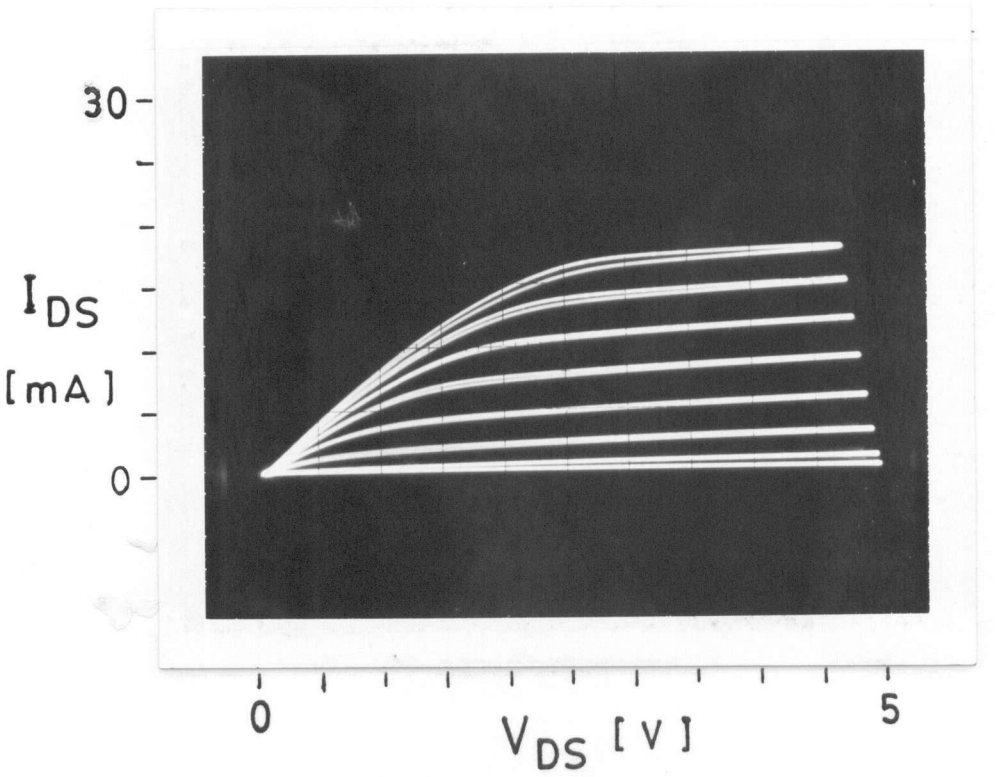


Fig. 4.9 I_{DS}-V_{DS} characteristics for 3 μm MESFET sample 123-S131 (R1-C5). V_{GS} bias step =-0.5 V

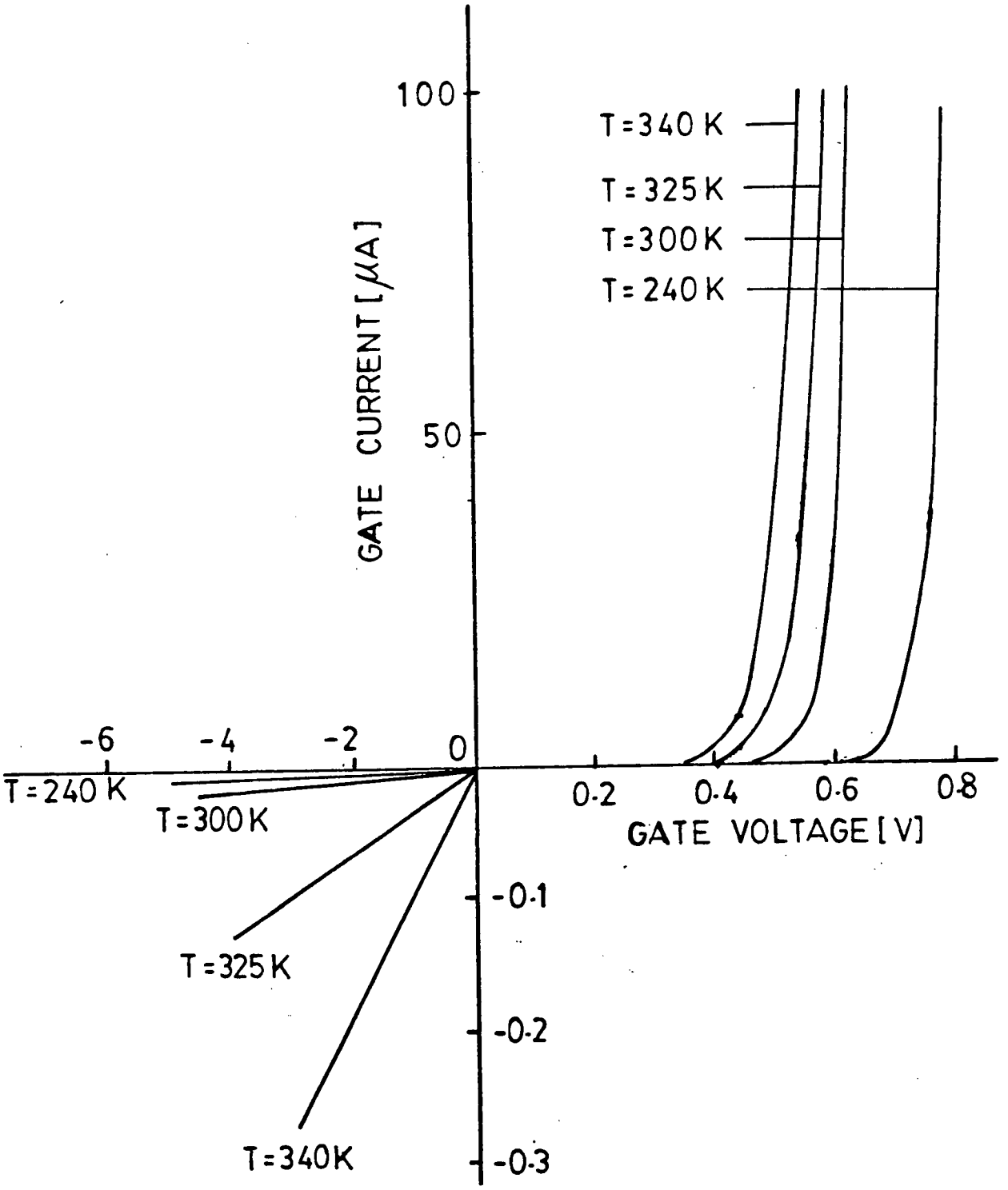


Fig. 4.10 I_{GS}-V_{GS} characteristics for 3 μm MESFET sample 123-S131 (R1-C5)

Table 4.4 - Device Parameters of 3 μm MESFET's

Sample	43-S10 (R2-C5)	43-S10 (R2-C6)	123-S131 (R1-C5)	123-S131 (R1-C8)	51-T132 (R1-C6)	51-T132 (R1-C3)
I_{DSAT} @ V_{DS}=4V [mA]	13	13	16	15	19	19
V_{GS} @ I_{DS}=100 μA [-V]	2.74	-	2.97	2.54	3.10	3.12
V_{GS} @ I_{DS}=10 μA [-V]	3.14	2.82	3.19	2.74	3.30	3.34
V_{GS} @ I_{DS}=1 μA [-V]	-	3.55	3.35	2.91	3.44	3.48
G_m @ V_{DS}=4V [mA/V]	5	6	5	6	8	8

To check MESFET drain current stability 3 μm device 123-S131 (R1-C5) was biased at V_{DS}=1V and a gate voltage applied of sufficient magnitude ($V_{GS}\approx$-3V) to reduce I_{DS} to 100 μA. I_{DS}, following the application of the gate voltage, was then monitored on a chart recorder. I_{DS} was found to be stable to within ±5% of 100 μA over a period of 30 minutes a result that differs from those Itoh and Yanai (1980) and Itoh et al. (1981) who reported drain current drifts of 20-40% (attributed to Cr trapping levels) for MESFET's formed by epitaxy on Bridgman substrates.

5. DEEP LEVEL TRANSIENT SPECTROSCOPY

5.1 Basic Principles

Since its introduction by Lang (1974), deep level transient spectroscopy (DLTS) has proven a very useful technique for investigating deep levels in semiconductor devices. It enables a non-destructive evaluation of the energy level E_T and electron (hole) capture cross section $\sigma_n(\sigma_p)$ of the major deep states in a sample. Deep level concentrations may also be determined.

DLTS is based on the modulation and measurement of the depletion region capacitance C(t) of a pn junction or Schottky diode. To analyze, for example, a p^+n diode for majority carrier traps in the n region, sample temperature T is varied and a voltage V(t) applied (Fig. 5.1). During period t_B-t_A traps in the undepleted n region are filled with electrons. When the bias is changed from V_1 to V_2 the depletion region width expands from W_1 to W_3 while the capacitance drops from C_1 to C_3. Traps at a depth between W_3 and W_1 which were filled are now emptied at a rate dependent on the trap's energy level and electron capture cross section. The release of trapped carriers results in a relaxation of the depletion width from W_3 to the steady state value W_2 and hence a relaxation of the capacitance from C_3 to C_2.

The transient signal S(t) is processed with a dual channel boxcar averager. The choice of boxcar sampling times t_1 and t_2 fixes the so called rate window RC of the system (Eq. 5.12). When the decay constant τ of S(t) is equal to the rate window, the output of the boxcar registers a maximum. As the sample temperature is scanned, a DLTS spectrum of $S(t_1)-S(t_2)$ versus T is obtained (Fig. 5.2). If more than one type of deep level is present in

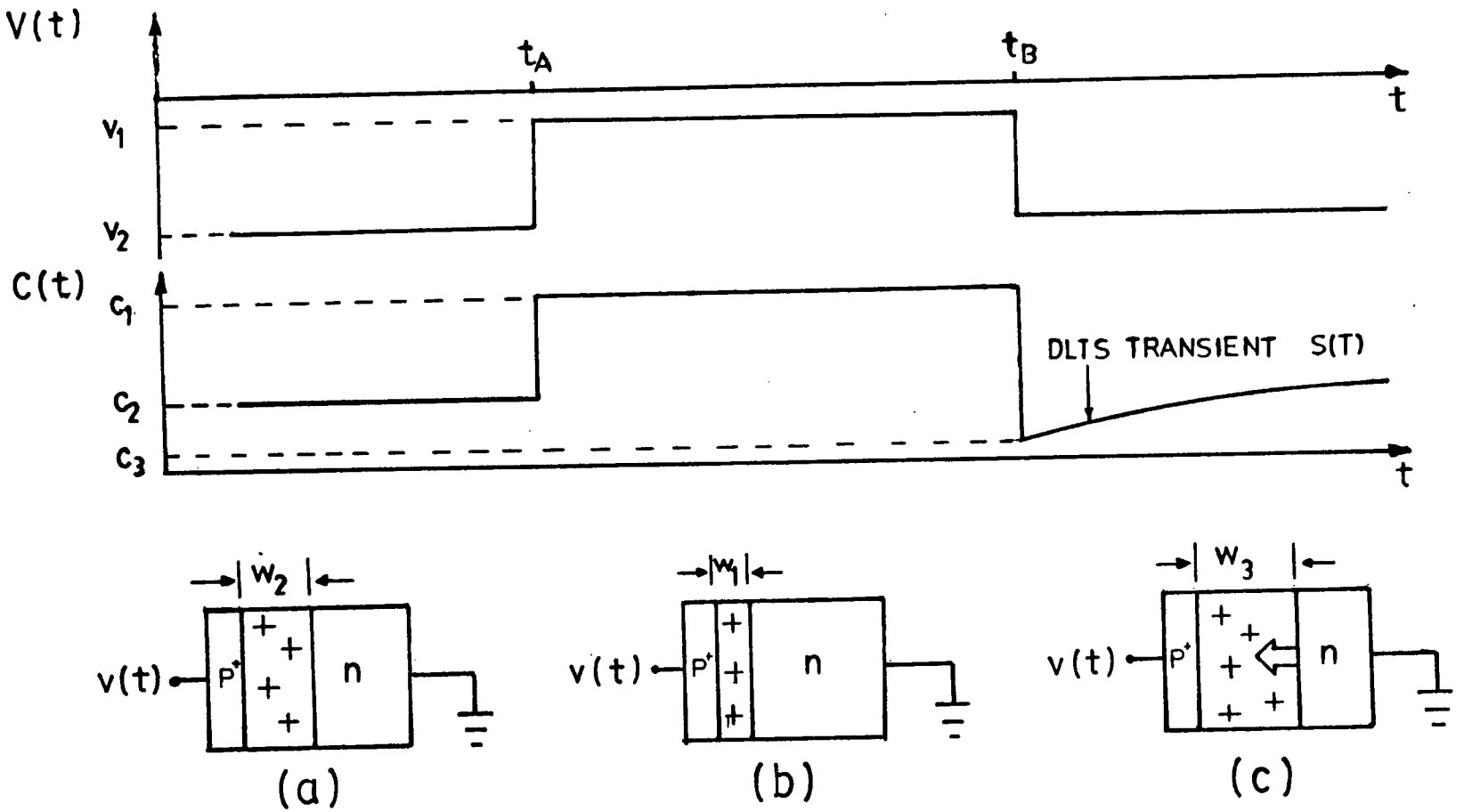


Fig. 5.1 Basic principle of DLTS generation (a) Steady state (b) Trap filling (c) Trap emptying

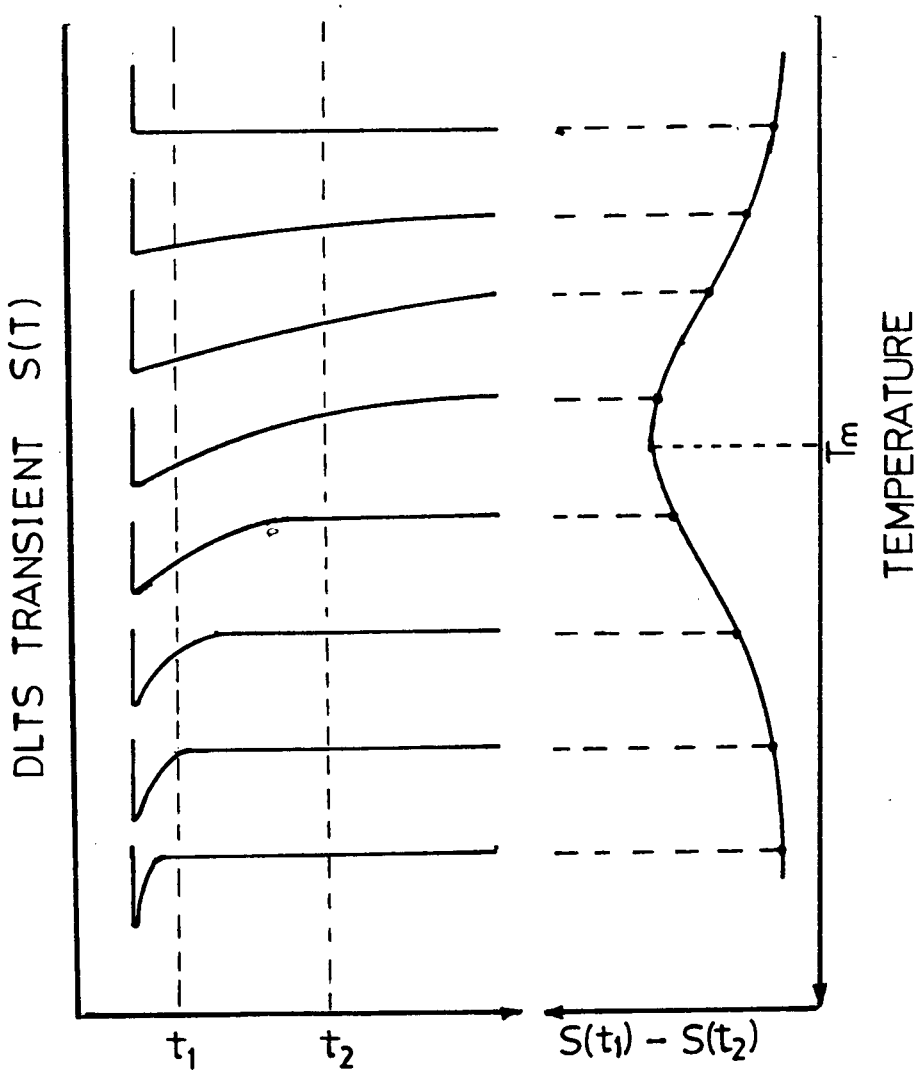


Fig. 5.2 Basic principle of dual channel boxcar sampling of DLTS transient

the sample, several peaks will appear in the spectrum. By selecting various rate windows and repeating the temperature scan a family of DLTS spectra are obtained from which trap data may be calculated (as described in Section 5.2).

5.2 Channel Conductance DLTS

Channel conductance DLTS (CDLTS) is a useful technique to assess the deep levels in the channel of a MESFET (Alderstein, 1976). A small drain to source voltage ($V_{DS} \approx 50$ mV) is applied. V_{GS} is set to zero to allow electron traps in the channel to be filled. V_{GS} is then stepped to V_G ($V_T < V_G < 0$). The gate depletion region widens and a transient channel current develops due to the release of electrons from the expanded depletion region.

An expression for the channel conductance transient may be derived for a MESFET of gate length L, gate width Z, and zero gate voltage channel depth a. It is assumed that a uniform active layer shallow donor density N_D exists and that a single electron trap of density N_T is present. Neglecting the resistance of the unmodulated channel regions, the conductance of the MESFET G(t) is

$$G(t) = \frac{Z\sigma[a-X_d(t)]}{L} \tag{5.1}$$

where σ is the conductivity of the active layer and $X_d(t)$ is the gate depletion region depth measured from the zero gate bias value. If at time t=0 the gate bias is stepped from 0 to V_G and the steady state conductance for large

t is G_0 (with a corresponding depletion depth of X_{do}), then the conductance difference signal $\Delta G(t)$ $\left(\Delta G(t) = G_0 - G(t)\right)$ is

$$\Delta G(t) = \frac{Z\sigma[X_d(t) - X_{do}]}{L} \quad . \tag{5.2}$$

Since $X_d(t)$ can be assumed to be given by

$$X_d(t) = \left\{ \frac{2\varepsilon V_G}{q[N_D + N_T(1 - \exp -t/\tau)]} \right\}^{1/2} \tag{5.3}$$

where τ is a time constant, one finds that

$$\frac{X_d(t)}{X_{do}} = \left[\frac{1}{1 - \frac{N_T}{N_D + N_T} \exp(-t/\tau)} \right]^{1/2} \quad . \tag{5.4}$$

Now if $N_T << N_D$ Eq. (5.4) becomes

$$\frac{X_d(t)}{X_{do}} \approx 1 + \frac{N_T \exp(-t/\tau)}{2N_D} \tag{5.5}$$

so Eq. (5.2) can be written as

$$\Delta G(t) = \frac{Z\sigma X_{do} N_T}{2LN_D} \exp(-t/\tau) \tag{5.6}$$

which is the desired expression for the channel conductance transient.

A block diagram of the CDLTS system of this thesis is shown in Fig. 5.3. The drain voltage to the FET is derived from a regulated power supply while the periodic gate bias is supplied by an IEC F33 pulse generator. A small resistor R (10 Ω) converts the channel current into a voltage signal which is subsequently amplified by a PAR 113 amplifier. The output from the amplifier goes to the input of a PAR 162/165 dual channel boxcar arrangement. The boxcar output goes to the Y channel of an HP 7044A X-Y plotter. The X channel of the plotter records the thermocouple voltage of the sample.

The sample is housed in a light tight chamber. The chamber, which was adapted for use from a previous study (Lester, 1982) is illustrated in Fig. 5.4. After the chamber is evacuated to a pressure of less than 10 torr, sample temperature is lowered to 100 K via liquid nitrogen cooling. A power transistor is used to heat the sample. A copper-constantan thermocouple, soldered to the device package, is used to monitor the temperature.

The input signal transient $V_i(t)$ to the boxcar is given by

$$V_i(t) = A_A R G(t) V_{DS} \tag{5.7}$$

where A_A is the amplifier gain and where it is assumed that $R \ll [G(t)]^{-1}$. The output of the boxcar V_0 (as a function of temperature T) can then be expressed as

$$V_0(T) = A_B[V_i(t_1) - V_i(t_2)] \tag{5.8}$$

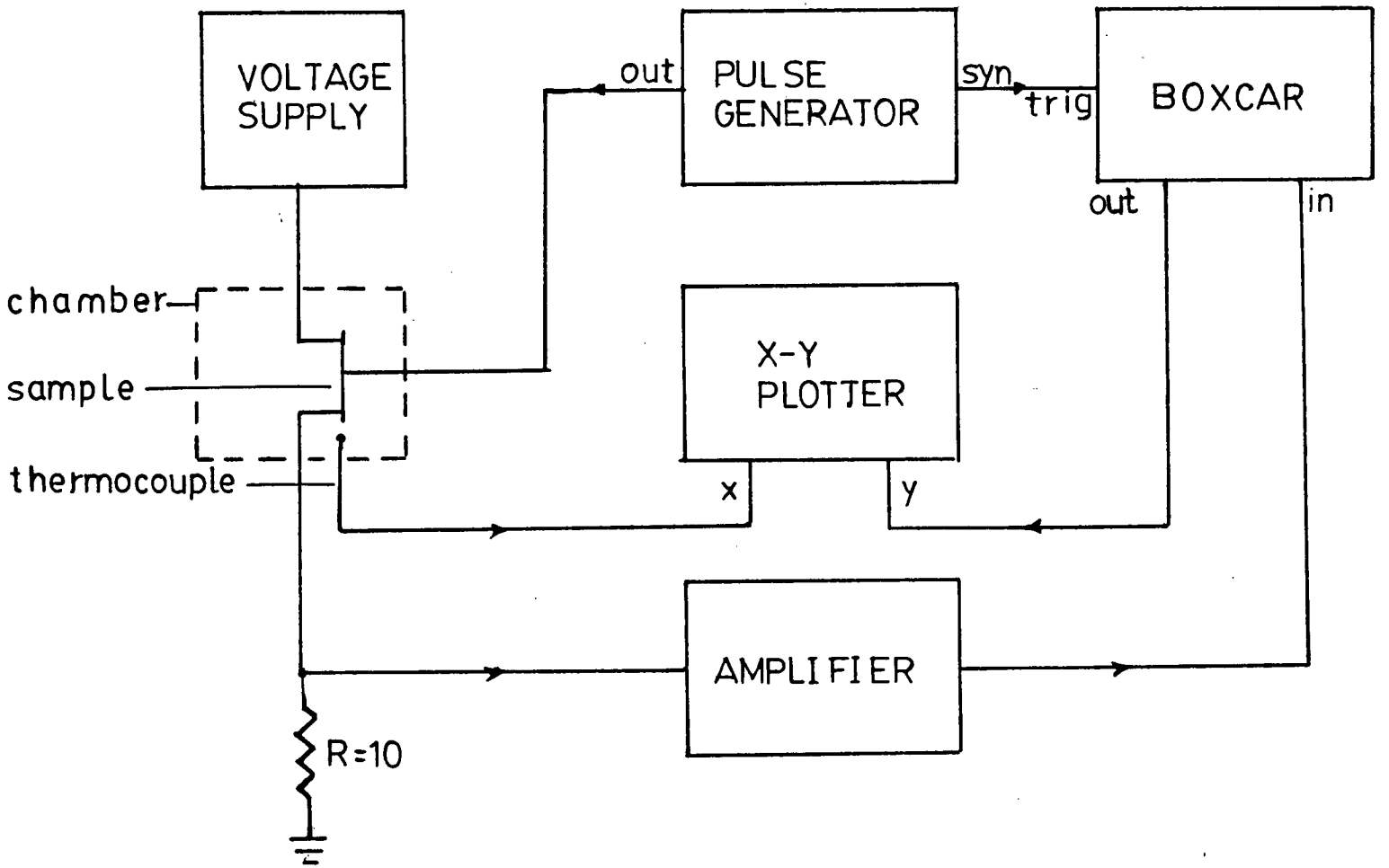


Fig. 5.3 Block diagram of channel conductance DLTS arrangement

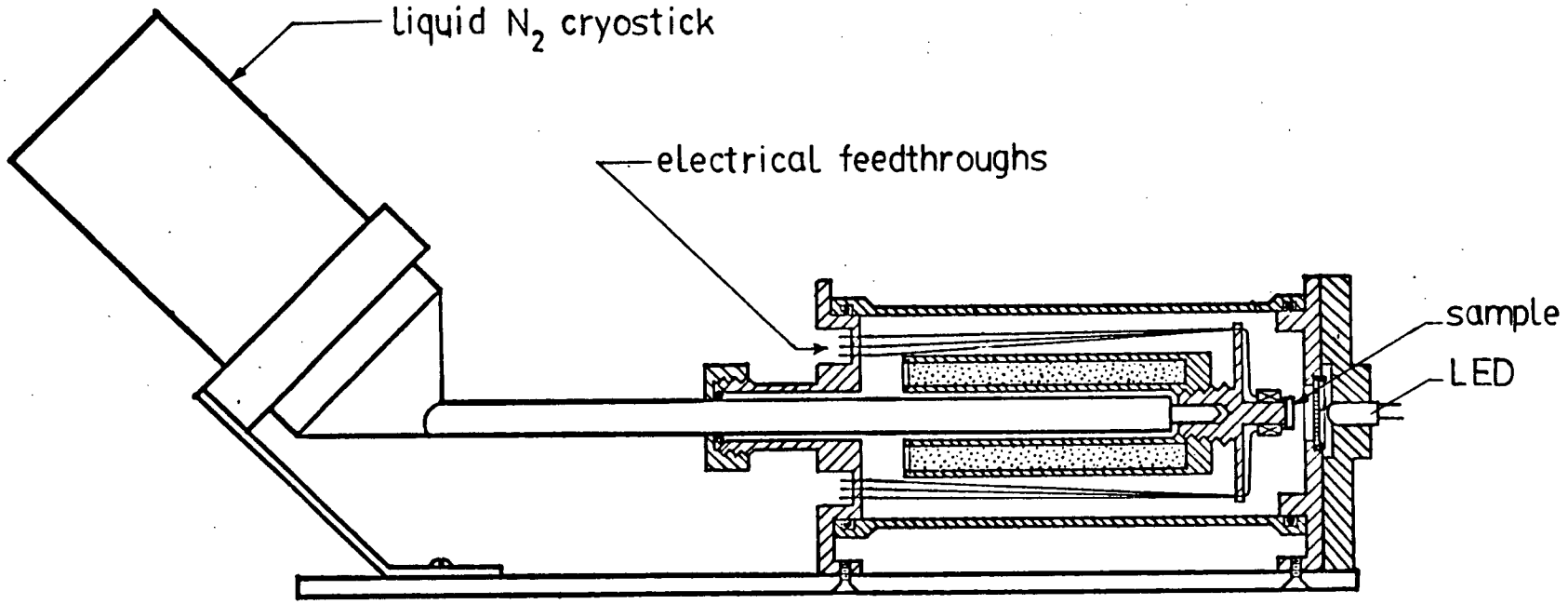


Fig. 5.4 Sample holder used for DLTS measurements

where A_B is the voltage gain of the boxcar. Then from Eq.'s (5.6) and (5.7) Eq. (5.8) can be rewritten as

$$V_o(T) = \frac{A_A A_B RZ \sigma V_{DS} N_T X_{do}}{2LN_D} \left[\exp(-t_2/\tau) - \exp(-t_1/\tau)\right] \tag{5.9}$$

The temperature dependence of V_0 in Eq. (5.9) can be derived from the temperature dependence of τ. From the principle of detailed balance the time constant (reciprocal emission rate) for an electron trap can be shown to be

$$\tau = (\sigma_n v_n N_c)^{-1} \exp\left[\frac{E_c - E_T}{kT}\right] \tag{5.10}$$

where σ_n is the capture cross section, v_n the thermal velocity of electrons, E_c the conduction band energy, and N_c the conduction band density of states. A trap level of single degeneracy is assumed. Since v_{th} and N_c vary markedly with T, Eq. (5.10) is more appropriately expressed as

$$\tau = (\sigma_n \gamma T^2)^{-1} \exp\left(\frac{E_c - E_T}{kT}\right) \tag{5.11}$$

where γ is equal to $2.28 \times 10^{20} cm^{-2} s^{-1} K^{-2}$ for electron traps in GaAs and to $1.7 \times 10^{21} cm^{-2} s^{-1} k^{-2}$ for hole traps in GaAs (Martin et al., 1977, Mitonneau et al., 1977).

For a certain value of τ, called τ_m, V_o peaks. By differentiating Eq. (5.9) with respect to τ and setting the result equal to zero one finds that

$$\tau_m = \frac{t_1 - t_2}{\ln t_1/t_2} \tag{5.12}$$

which is defined as the rate window RC of the CDLTS scan. Since the temperature T_m corresponding to the peak in V_o is obtained from the DLTS spectrum (Fig. 5.2) and t_1 and t_2 are known, one may write

$$\tau_m = (\sigma_n \gamma T_m^2)^{-1} \exp\left(\frac{E_c - E_T}{kT_m}\right) \tag{5.13}$$

If a second spectrum is obtained for a different rate window, σ_n and $E_c - E_T$ are uniquely determined. Usually several scans are made and a plot of $\log T^2\tau$ versus 1/T (activation energy plot) made. Trap parameters are then given by

$$E_c - E_T = 2.30\ km \tag{5.14}$$

and

$$\sigma_n = (\gamma\ 10^b)^{-1} \tag{5.15}$$

where m and b are the slope and intercept, respectively, of the best linear fit to the above plot.

The concentration of a trap is derived from the height $V_o(T_m)$ of the CDLTS peak. From Eq. (5.9) N_T can be calculated as

$$N_T = \frac{2LN_D V_o(T_m)}{A_A A_B RZ \sigma V_{DS} X_{do}} \left[\exp\left(\frac{-t_2}{\tau_m}\right) - \exp\left(\frac{-t_1}{\tau_m}\right)\right] \tag{5.16}$$

where τ_m is given by (5.12).

If the active region of a MESFET is formed by ion implantation the assumption of a uniformly doped channel region is violated. Nevertheless, Eq.'s (5.14) and (5.15) can still be expected to give a reasonable estimate of E_c-E_T and σ_n in most cases. Since the conductivity of an implanted channel can be taken to be proportional to an average N_D it is interesting to note that Eq. (5.16) reveals that N_T may be calculated simply from a knowledge of X_{do} (which can be deduced from a capacitance voltage measurement).

5.3 Photocurrent DLTS

Photocurrent DLTS (PDLTS) is a useful technique to assess the deep levels in a semi-insulating sample (Fairman et al., 1979, Hurtes et al., 1978). The device structure that is used in PDLTS consists of two closely spaced ohmic contact pads. A bias V is established between the pads and the sample is illuminated with bandgap light. Electron/hole pairs are generated which populate traps in the sample. If the sample is illuminated for a sufficient length of time the current flow between the pads approaches a steady state value i_s. If the sample contains a trap of density N_T, the occupation of the trap n_{T_s} during steady state is given by

$$n_{T_s} = N_T \left(1 + \frac{e_n+\sigma_p v_p p}{e_p+\sigma_n v_n n}\right)^{-1} \tag{5.17}$$

where e_n/e_p, σ_n/σ_p, v_n/v_p, and n/p are the electron/hole rate constant, capture cross section, thermal velocity and concentration, respectively

(Hurtes et al., 1978).

When the light is removed (at t=0) the current does not immediately fall to i_L (the leakage flow) but instead gradually decays to this level due to the slow release of trapped carriers. The decay current $i_p(t)$ is given by

$$i_p(t) = C\{e_n n_T(t) + e_p[N_T - n_T(t)]\} \tag{5.18}$$

where n_T is the density of occupied traps, C is a constant dependent on contact geometry (Martin and Bois, 1978) and where i_L has been neglected. If it is assumed that $i_p(t)$ decays exponentially with time constant τ and that $n_T(0)$ is equal to n_{T_s} Eq. (5.18) becomes

$$i_p(t) = Ce_n N_T\left[\left(1 + \frac{\sigma_p v_p}{\sigma_n v_n}\right)^{-1} - \left(1 + \frac{e_n}{e_p}\right)^{-1}\right]\exp\left(\frac{-t}{\tau}\right). \tag{5.19}$$

For an electron trap $\sigma_n >> \sigma_p$ and $\tau^{-1} = e_n >> e_p$ so that

$$i_p(t) = C\tau^{-1}N_T\exp\left(\frac{-t}{\tau}\right). \tag{5.20}$$

A block diagram of the photoconductance DLTS (PDLTS) system of this thesis is shown in Fig. 5.5. The system utilizes the same apparatus as the CDLTS arrangement of Fig. 5.3 except that a type ME7021IR light emitting diode (900 nm, 1.0 mW @100 mA) mounted on the sample chamber is used to

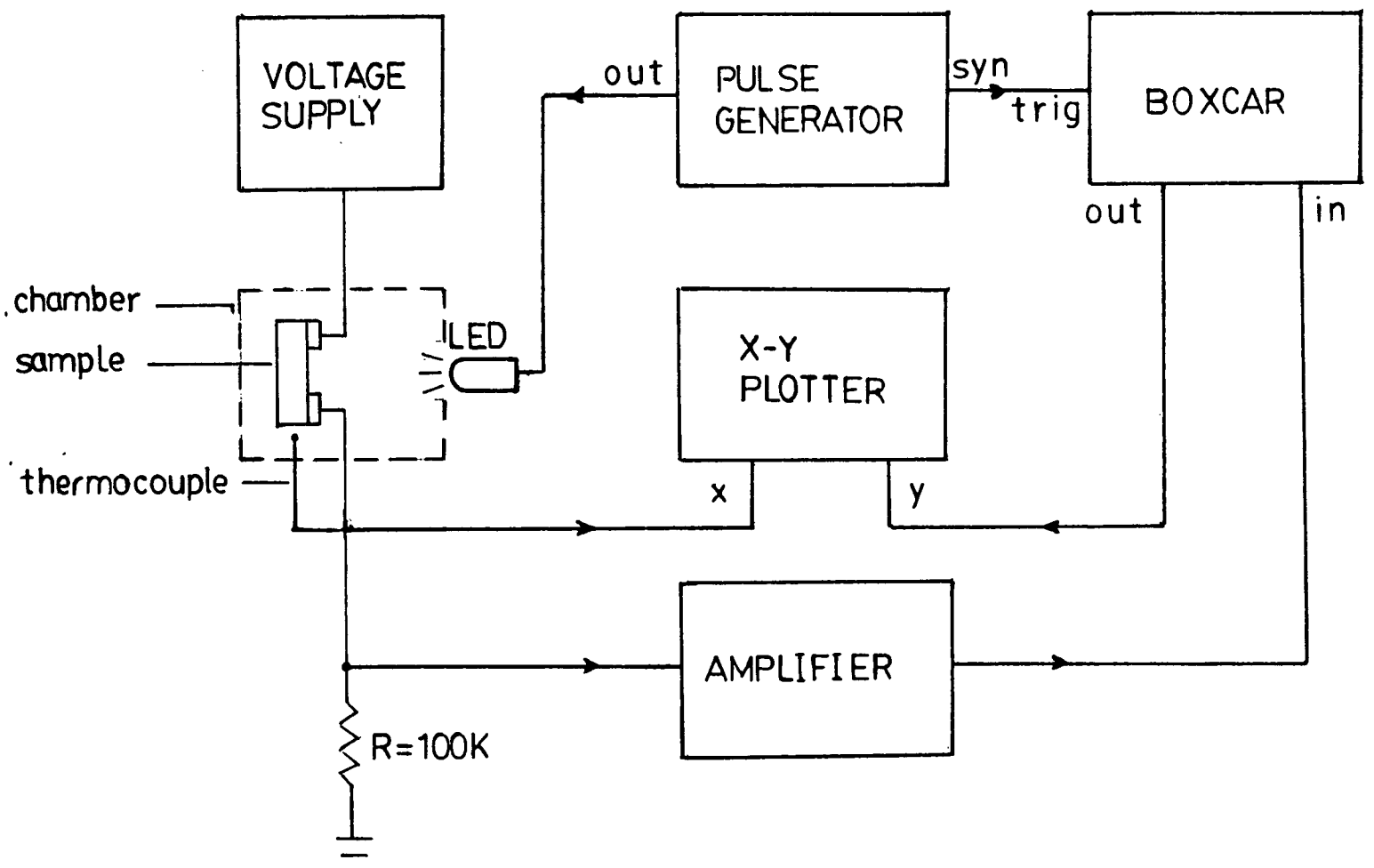


Fig. 5.5 Block diagram of photocurrent DLTS arrangement

illuminate the sample through a window (Fig. 5.4). The transient signal input $V_i(t)$ to the boxcar is

$$V_i(t) = A_A R\, i_p(t) \tag{5.21}$$

while the boxcar output $V_o(T)$ derived from Eq. (5.20) is

$$V_o(T) = A_A A_B RC\tau^{-1} N_T \left[\exp\left(\frac{-t_1}{\tau}\right) - \exp\left(\frac{-t_2}{\tau}\right)\right] \tag{5.22}$$

where A_A, A_B and R are as defined previously. If $V_o(T)$ is differentiated with respect to τ and the result set equal to zero τ_m is found to satisfy (Itoh and Yanai, 1981)

$$\left(1 - \frac{t_1}{\tau_m}\right)\exp\left(\frac{-t_1}{\tau_m}\right) = \left(1 - \frac{t_2}{\tau_m}\right)\exp\left(\frac{-t_2}{\tau_m}\right). \tag{5.23}$$

Once τ_m is calculated, σ_n and $E_c - E_T$ can be determined from Eq. (5.13) as in CDLTS.

5.4 Measurements

CDLTS measurements were made with the system described in Section 5.2 to obtain information on the deep levels in the channel region of the MESFET's fabricated in Chapter 3. 3 μm MESFET's were examined over the temperature range 100-350 K with rate windows 1-100 ms.

CDLTS spectra for devices 123-S131 (R1-C5), 43-S10 (R2-C6), and 51-T132 (R1-C3) are shown in Fig.'s 5.6-5.8. Three electron traps, labelled CE1, CE2, and CE3 are resolved in each sample. The activation energy plot (or DLTS "signature", Martin et al., 1977) of each trap is shown in Fig. 5.9. Table 5.1 lists data on trap energy, cross section, and concentration calculated via Eq.'s 5.14-16. Trap concentrations in 51-T132 (R1-C3) (especially CE1) are lower than in the other two devices. In addition the I-V characteristics of 51-T132 (R1-C3) show less hysteresis than that of 123-S131 (R1-C5) (or 43-S10 R2-C6) (compare Fig. 4.9 with Fig. 5.10) suggesting that one or more of these traps are responsible for hysteresis.

Table 5.1 - Deep Levels Detected by CDLTS

Label	Activation Energy [eV]	Log (σ_n[cm^2])	τ @ 300 K [μs]	N_T [10^{16}cm^{-3}]		
				43-S10 (R2-C6)	123-S131 (R1-C5)	51-T132 (R1-C3)
CE1	0.50 ±0.01	-12.8	77	2.5	2.5	0.5
CE2	0.27 ±0.02	-16.3	27	1.0	0.5	0.3
CE3	0.20 ±0.01	-17.2	13	0.5	0.4	0.3

To investigate semi-insulating properties, substrate samples were prepared so that PDLTS measurements could be made. On each sample AuGe ohmic contact pads were defined. The separation of the pads was 50 μm and the width of each pad 250 μm.

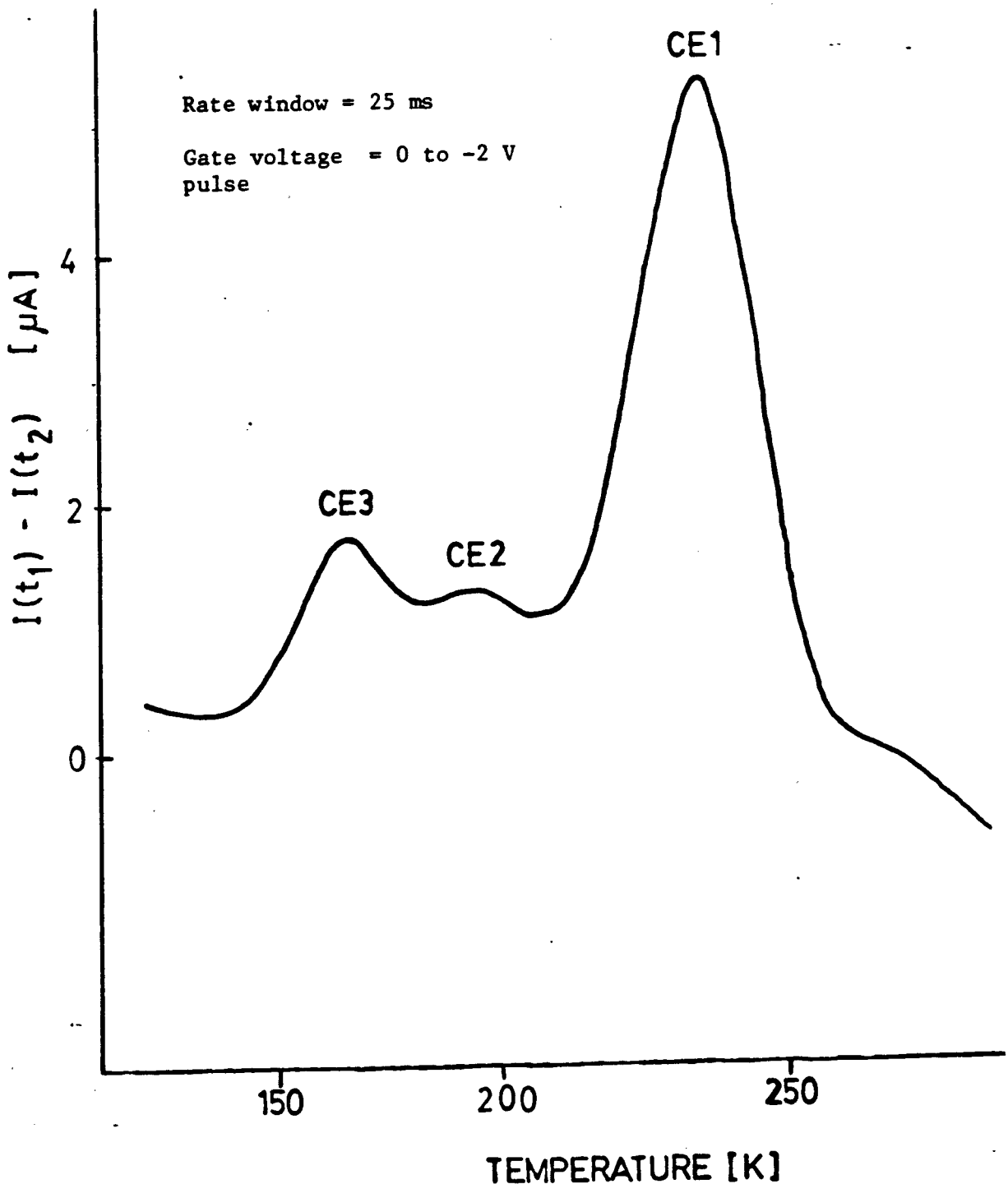


Fig. 5.6 A CDLTS spectrum for 3 μm MESFET sample 123-S131 (R1-C5)

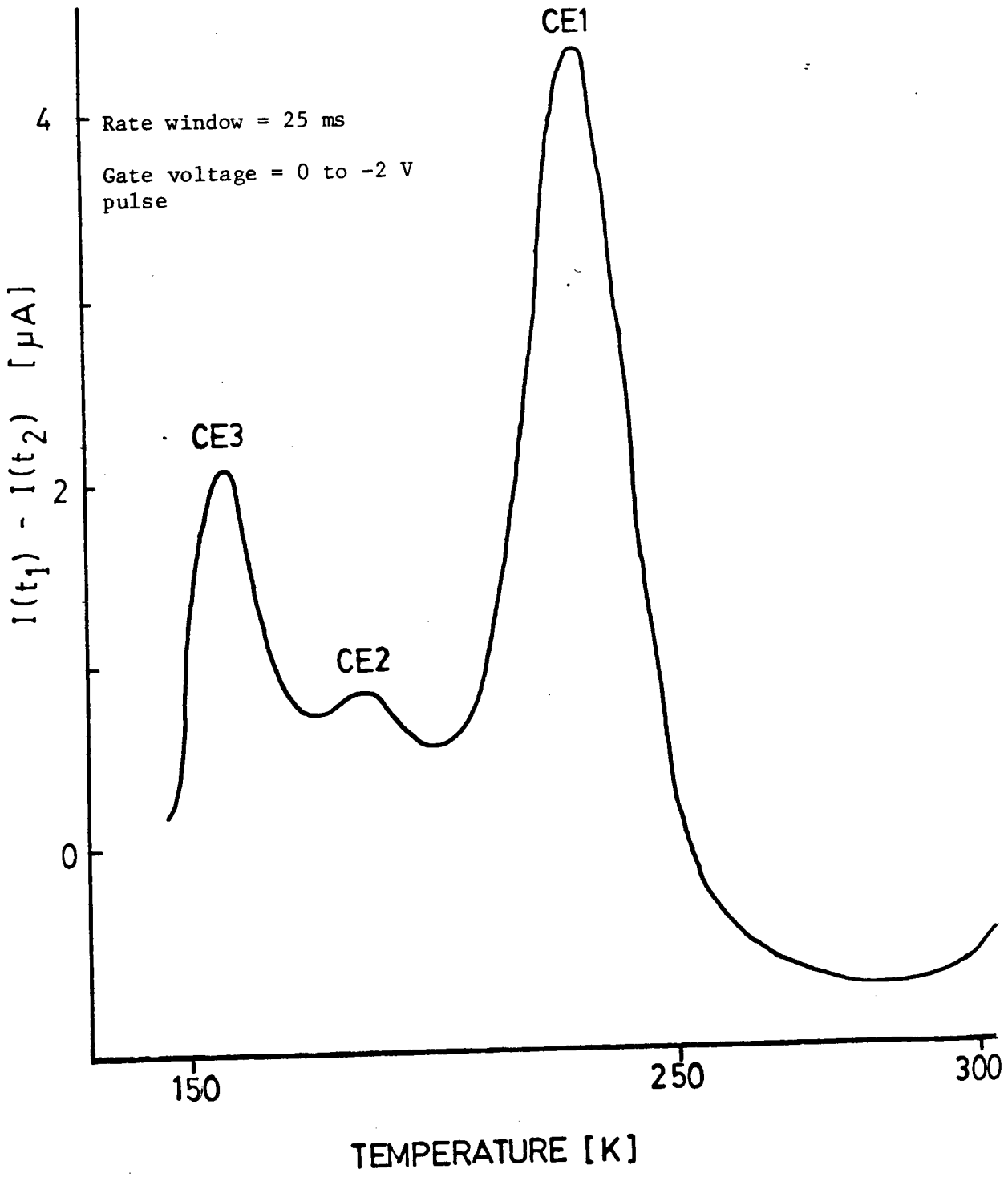


Fig. 5.7 A CDLTS spectrum for 3 μm MESFET sample 43-S10 (R2-C6)

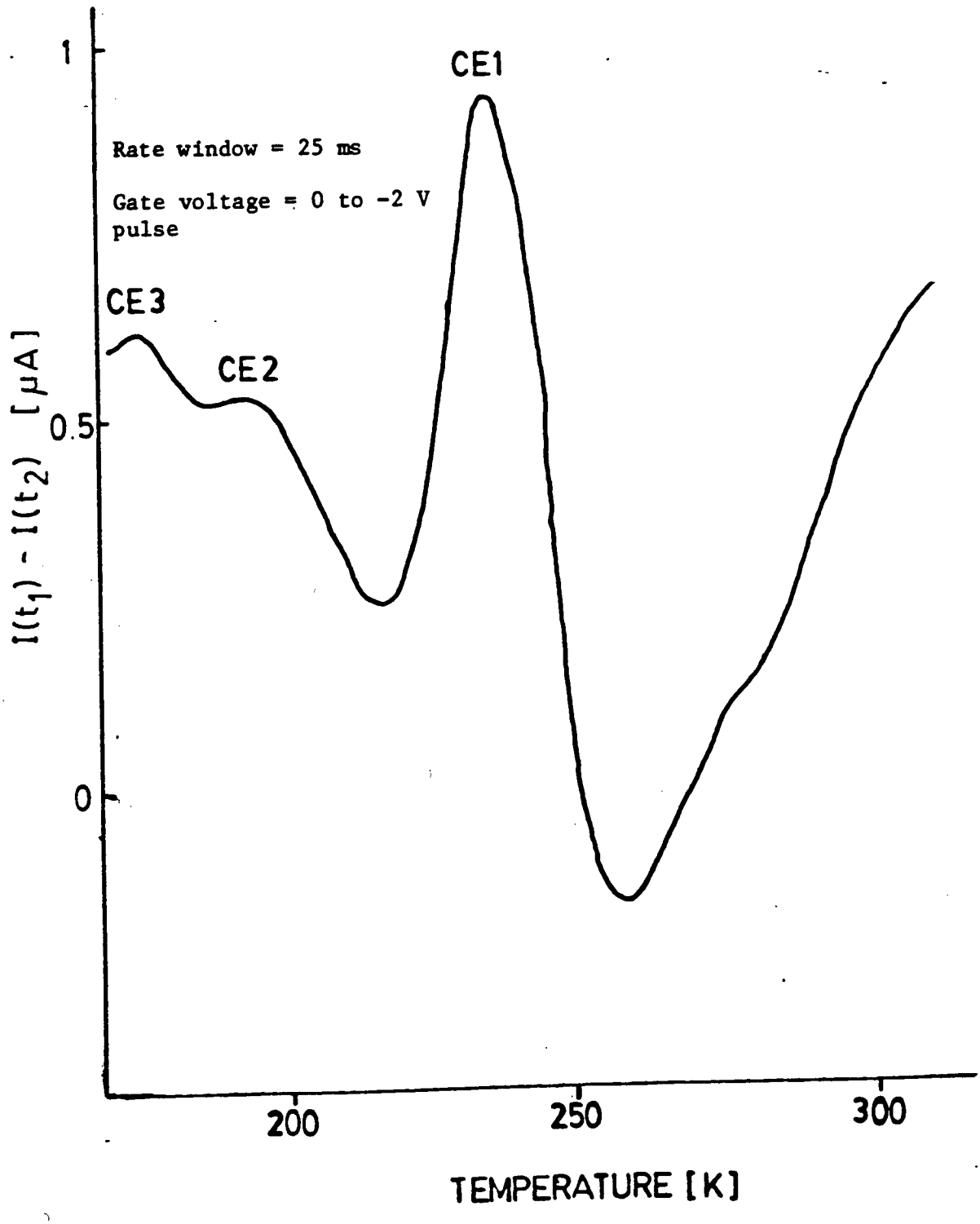


Fig. 5.8 A CDLTS spectrum for 3 μm MESFET sample 51-T132 (R1-C3)

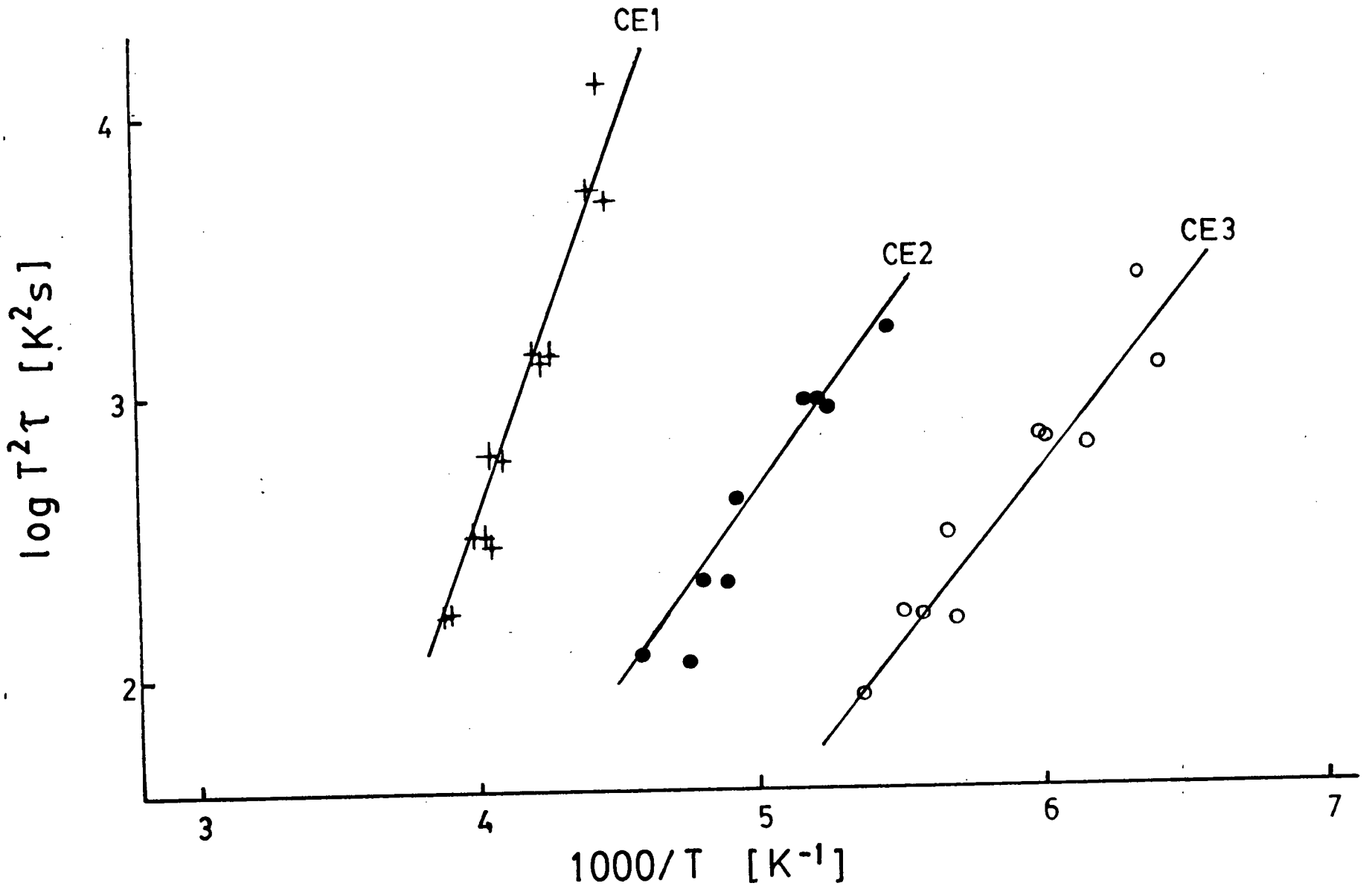


Fig. 5.9 Activation energy plot for traps detected by CDLTS

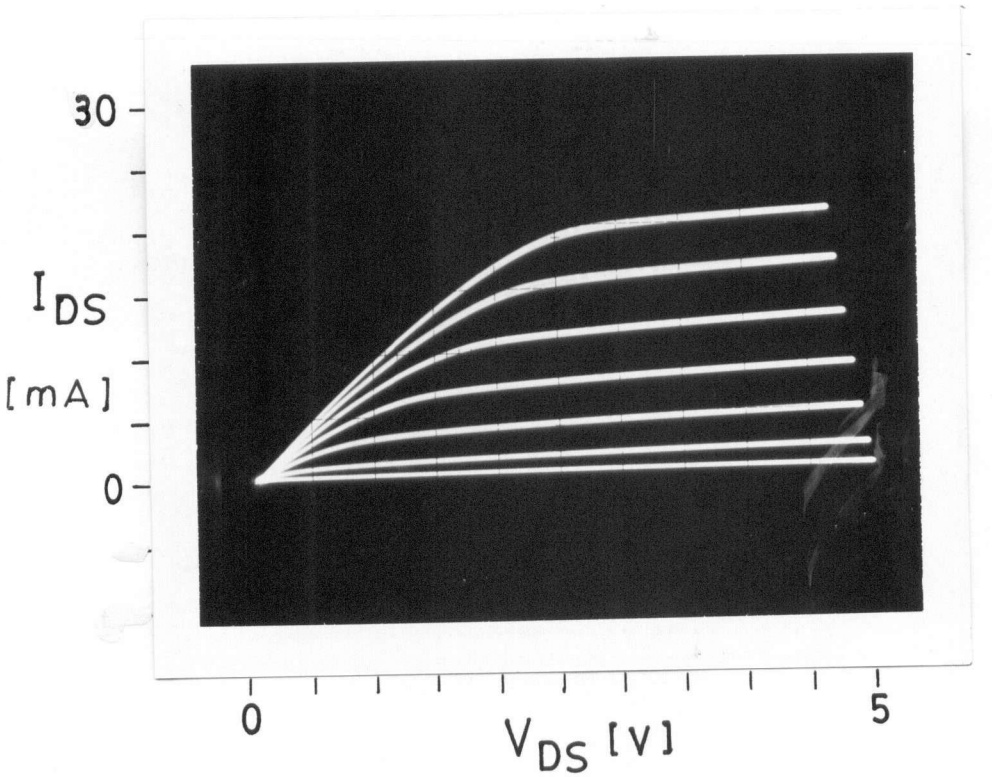


Fig. 5.10 I_{DS}-V_{DS} characteristics for 3 μm MESFET sample 51-T132 (R1-C3). V_{GS} bias step = -0.5 V

PDLTS measurements were conducted using the system described in Section 5.3. The temperature range investigated was 100-330K. Rate windows were varied from 1 ms to 50 ms. An inter-pad bias of 4V and a light intensity sufficient to give a peak photocurrent of 500 nA (at room temperature) were used.

A PDLTS spectrum for sample 63-T42(A) is shown in Fig. 5.11. Five deep levels labelled P1 to P5 are resolved. The PDLTS spectrum for sample 82-S14(A) shown in Fig. 5.12 shows the same five levels but the relative concentration (peak height) of the P1 to P2 level in this sample is apparently higher. Of note is the fact that ingot 82 (like 51) was found by Cominco to be thermally unstable upon 850°C anneal (Table 5.2). Trap signatures are shown in Fig. 5.13 and trap data listed in Table 5.3.

Table 5.2 - Properties of Cominco GaAs

Wafer Obtained From Cominco	Wafer Assessed By Cominco	Resistivity Before Anneal [Ωcm]	Resistivity After Anneal [Ωcm]
43-S10	43-S7	9.6×10^7	$1.8 - 2.1 \times 10^7$
45-S93	45-S96	3.9×10^7	1×10^7
69-T42	63-T27	1.2×10^7	$8 - 9 \times 10^6$
94-S13	94-S22	2.0×10^5	1.9×10^7
123-S131	123-S195	-	2.8×10^7
51-T132	51-T181	1.8×10^8	1.1×10^4
82-S14	82-S11	4.3×10^8	$6.1 \times 7.1 \times 10^3$

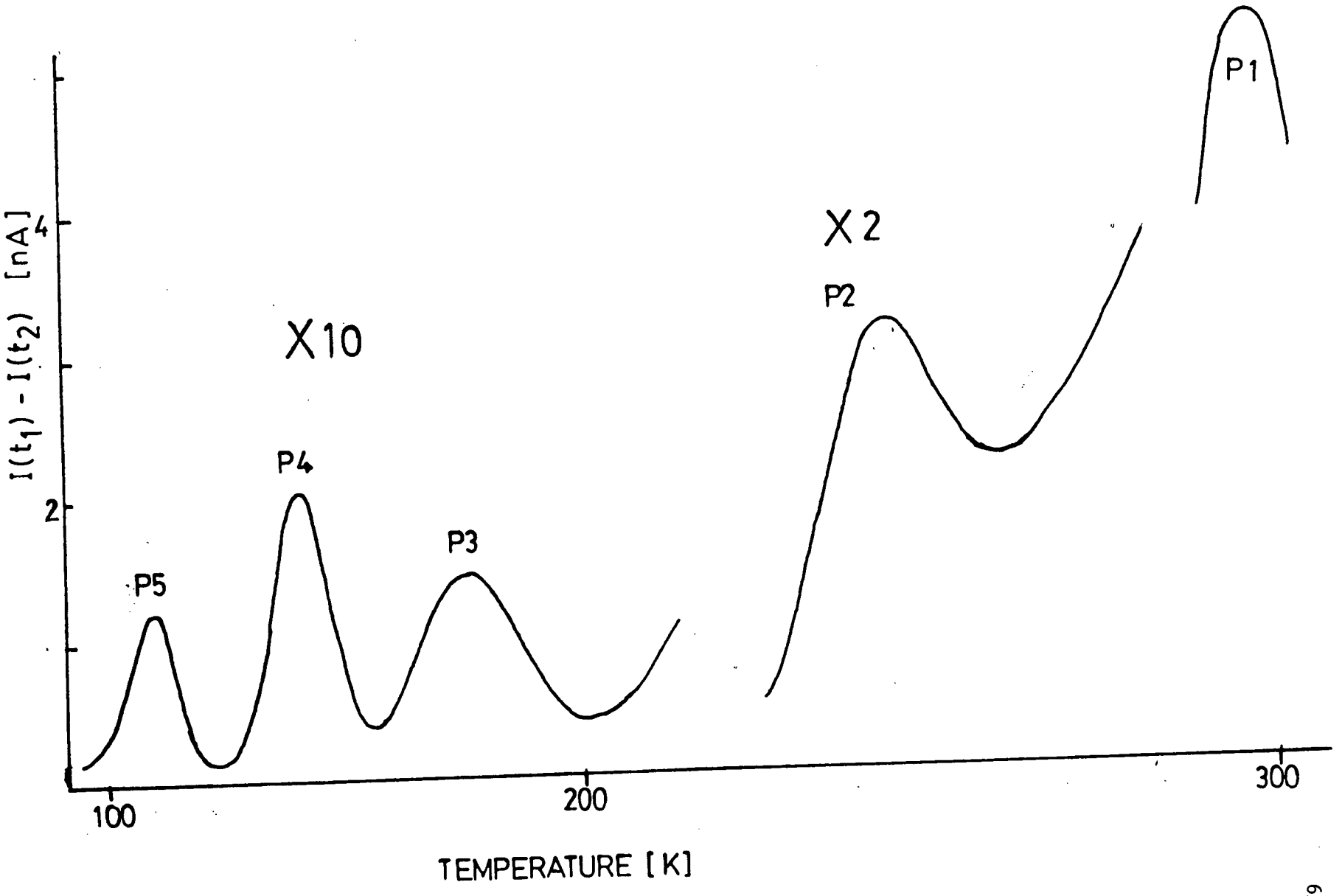


Fig. 5.11 A PDLTS spectrum for sample 63-T42(A) (Rate window = 10 ms)

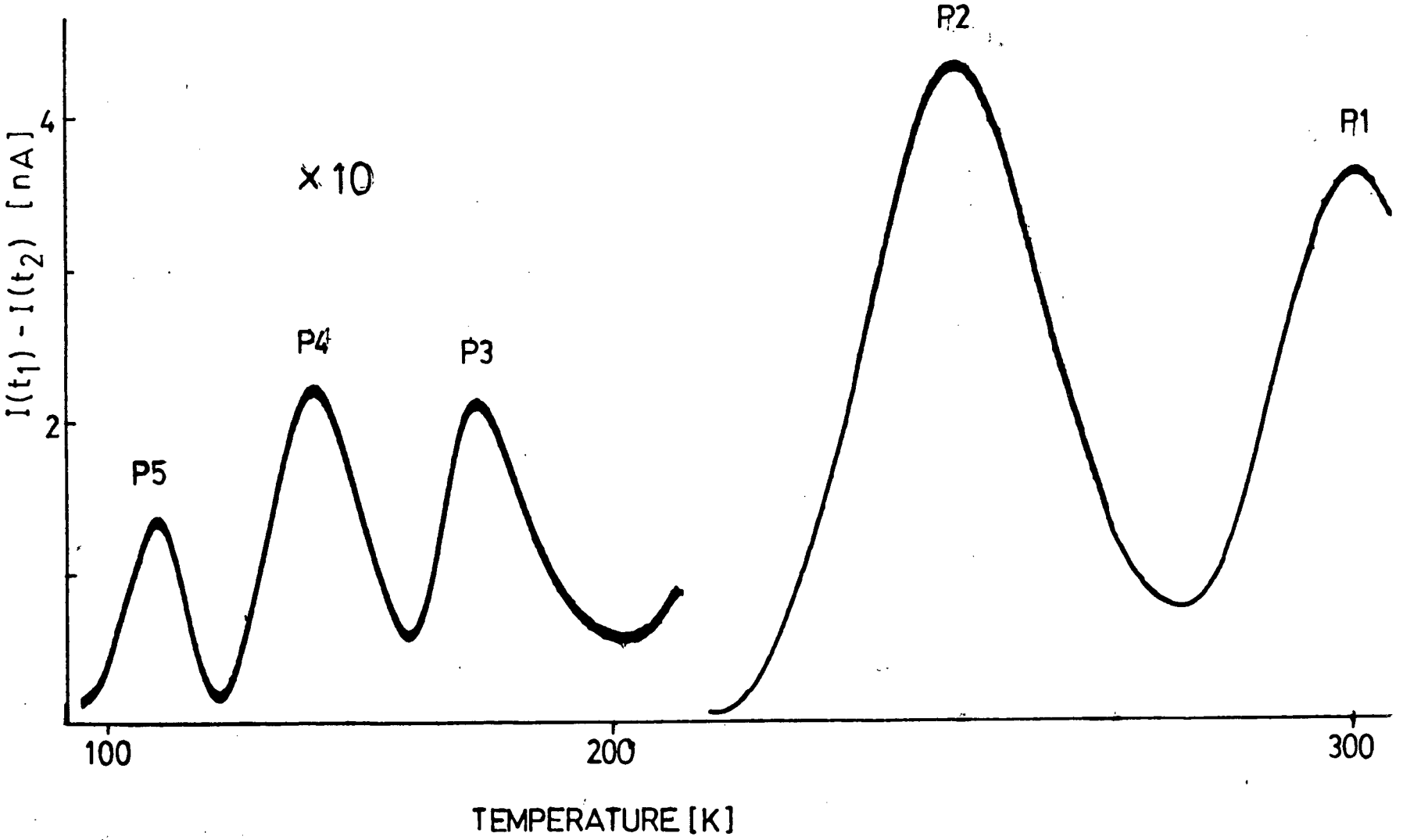


Fig. 5.12 A PDLTS spectrum for sample 82-S14(A) (Rate window = 10 ms)

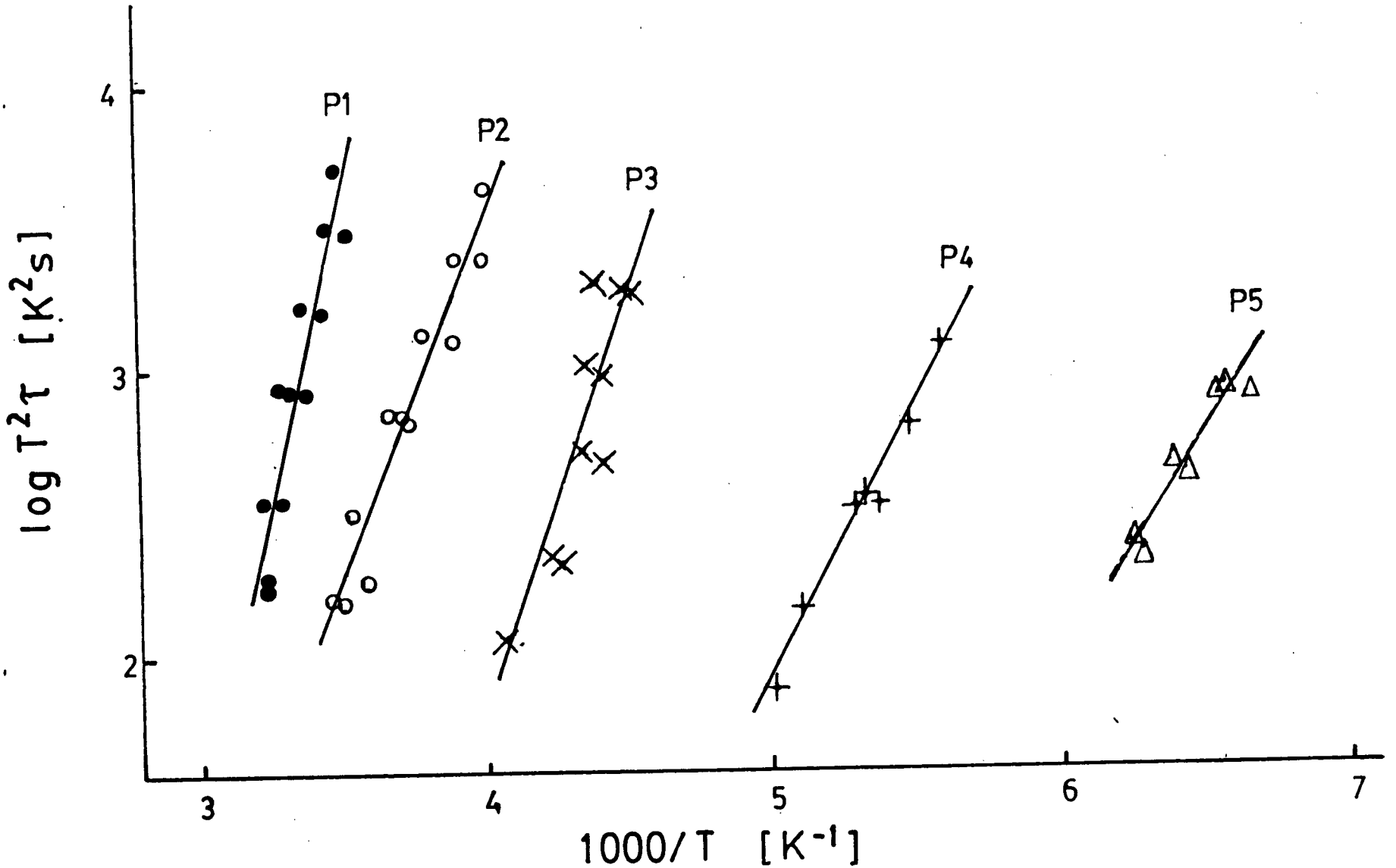


Fig. 5.13 Activation energy plot for traps detected by PDLTS

Table 5.3 - Deep Levels Detected By PDLTS

Label	Activation Energy [eV]	τ @ 300 K [s]	Log(σ_n[cm^2])	Log(σ_p[cm^2])
P1	0.87	7.5×10^{-3}	-8.6	-9.5
P2	0.50	7.3×10^{-3}	-13.8	-14.6
P3	0.59	6.1×10^{-6}	-10.3	-11.1
P4	0.38	5.3×10^{-6}	-12.7	-13.5
P5	0.32	4.6×10^{-9}	-12.6	-13.5

PDLTS and CDLTS trap signatures are compared in Fig. 5.14 along with various levels from the review of Martin et al. (1977) and Mitonneau et al. (1977). Possible associations are P1 with EL12, P2 with EL3, P3 with EL4, P4 with HL6 and P5 with EL8. EL2, a very commonly reported trap in bulk GaAs (Appendix A) was not detected in this work. CE1, CE2, and CE3 could not be identified with any of the levels from the reviews (which report on traps detected by DLTS in bulk and/or epitaxial GaAs) or with any of the PDLTS levels suggesting that the CDLTS levels are introduced during the implantation annealing process. (A similar conclusion has been made by Rhee et al., (1982) who detected a 0.52 eV electron trap in Si implanted GaAs not detected in the substrate). The complete list of traps of Martin and Mitonneau is given in Appendix C along with the results of subsequent DLTS studies reviewed by this author.

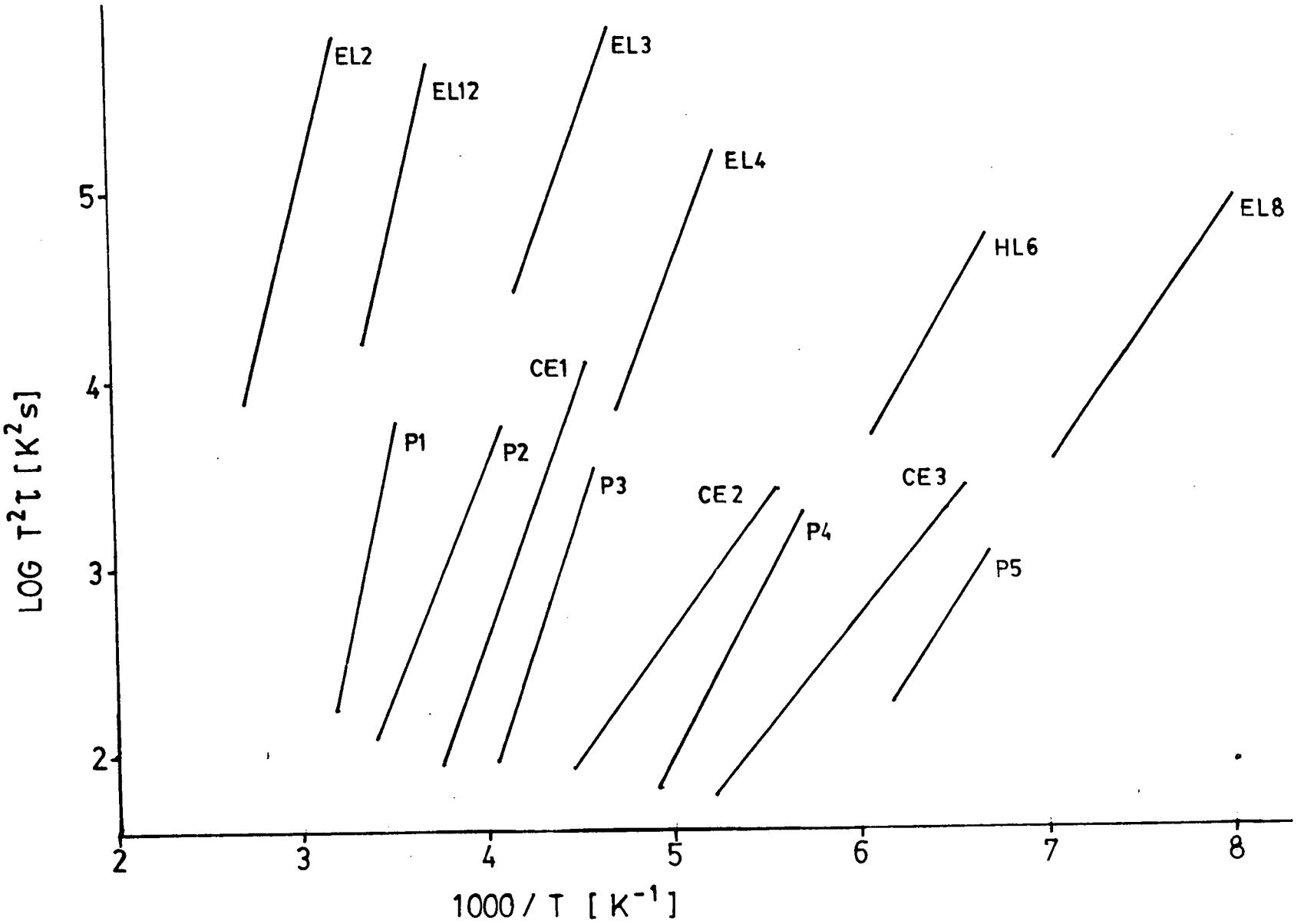


Fig. 5.14 Comparison of trap signatures

6. HYSTERESIS-FREQUENCY SPECTROSCOPY

6.1 Theory

A useful procedure to study the hysteresis effect seen in the I-V characteristics of GaAs MESFET's is to vary the voltage sweep frequency. For sweep frequencies $f \gg \tau^{-1}$ (where τ is the time constant of the traps causing hysteresis) traps cannot respond to the change in voltage so current looping can be expected to be negligible. For sweep frequencies $f \ll \tau^{-1}$ traps can completely follow the change in voltage so current looping can again be expected to be negligible. Therefore, for a sweep frequency $f_m \approx \tau^{-1}$ current looping should be a maximum.

Hysteresis in MESFET drain current vs. gate voltage (I_D-V_G) characteristics is analyzed with the following approximations and assumptions.

We assume that there is only one donor-electron trapping level in the active region of the transistor. Its concentration is N_T, where $N_T \ll N_D$ (N_D is the shallow donor concentration of the n-type active region). Both traps and doping are taken to be uniform. When the depletion region is expanded to include occupied and, hence, neutral traps, their concentration is assumed to start decaying exponentially (as electrons leave them).

As shown in Fig. 6.1(a), a saw-tooth waveform is used to sweep V_G linearly from zero to $-V_m$, i.e., $V_G = -V_m\, t/t_m$, where V_m is the amplitude and t_m is the period of the saw-tooth waveform. V_G is assumed to return to zero so rapidly that the occupation of the traps in the depletion region is frozen during this process.

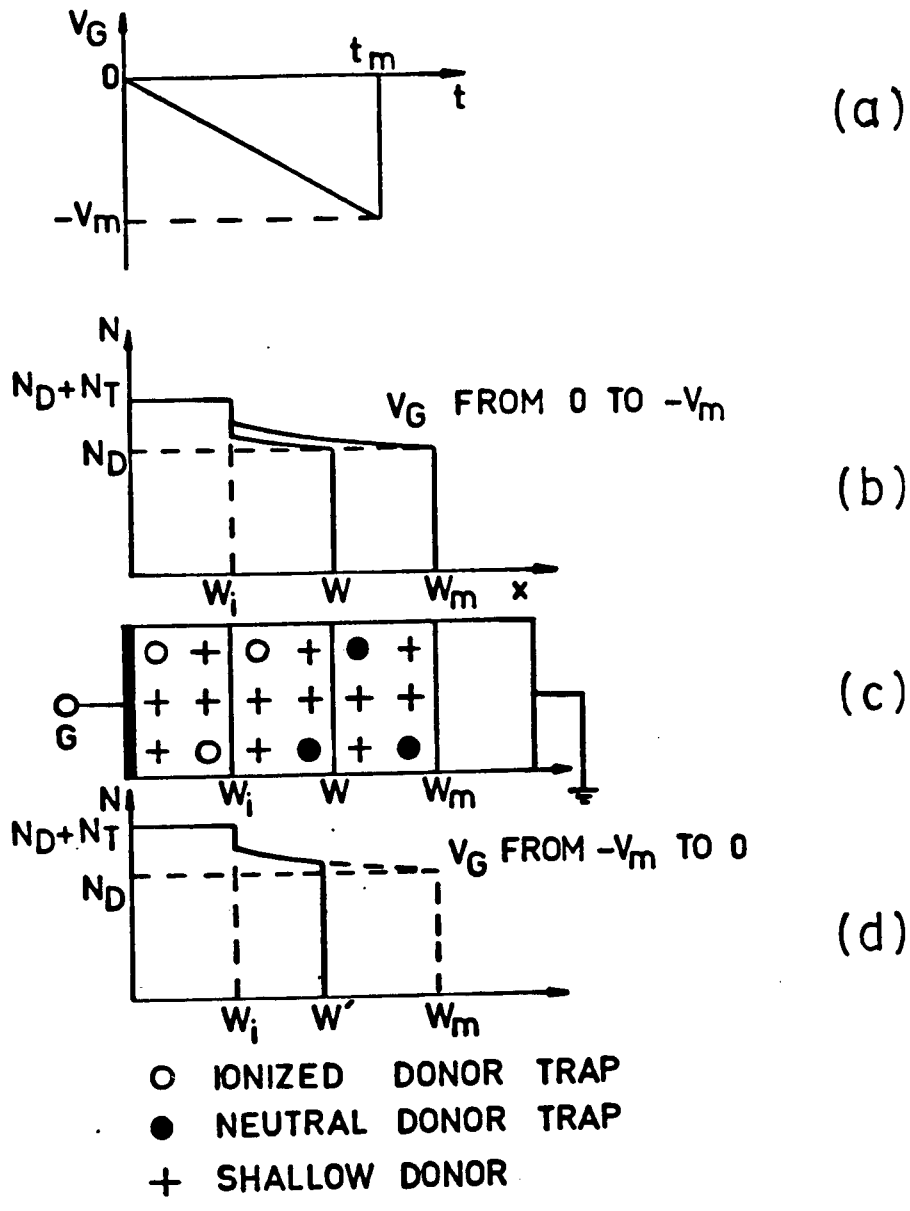


Fig. 6.1 Ionization of traps in the depletion region due to the sweep of gate voltage with a saw-tooth waveform (a) Saw-tooth waveform (b) Concentration of ionized donors for V_G from 0 to $-V_m$ (c) Ionization in Schottky gate depletion region (d) Concentration of ionized donors for V_G from $-V_m$ to 0.

The depletion width at zero gate bias, W_i, corresponds to the built-in voltage V_{bi}. For negative gate biases, the depletion width is always greater than W_i and the traps inside W_i can hence be considered to be completely ionized, so that

$$W_i = \left(\frac{2\varepsilon V_{bi}}{q(N_D+N_T)} \right)^{1/2} , \tag{6.1}$$

where ε is the permittivity of the semiconductor. As the gate voltage changes from zero to V_G, the depletion width increases to W (Fig. 6.1b). The space charge concentration N(x) in the region $W_i < x < W$ can be expressed as

$$N(x) = N_D + \delta(x) , \tag{6.2}$$

where $\delta(x)$ is the ionized trap concentration within this depletion region.

The relation between the depletion width W and the gate voltage V_G can be found by solving

$$\int_{W_i}^{W} N(x)\, x dx = -\int_{o}^{V_G} \frac{\varepsilon}{q}\, dV . \tag{6.3}$$

Since $N_T << N_D$, $\delta(x)$ in Eq.(6.2) will be much smaller than N_D. Hence an iterative method can be used. At first, the ionized traps in the depletion region $W_i < x < W$ are ignored, i.e., the second term of Eq. (6.2) is neglected. From Eq. (6.3).

$$W = \left(\left(\frac{2\varepsilon V_m}{qN_D}\right)\left(\frac{V_{bi}}{V_m}\ \frac{N_D}{N_D+N_T} - \frac{V_G}{V_m}\right)\right)^{1/2} \quad . \tag{6.4}$$

Eq. (6.4) is a first approximation to the relation between W and V_G.

The moment t at which position W starts to deplete can be obtained from Eq. (6.4)

$$t = \left(\frac{W^2}{\frac{2\varepsilon V_m}{qN_D}} - \frac{V_{bi}}{V_m}\frac{N_D}{N_D+N_T}\right) t_m \quad . \tag{6.5}$$

A better approximation of N(x) at V_G in the region $W_i < x < W$ can then be made. Since the concentration of the neutral traps in this region is considered to be decaying exponentially, $\delta(x)$ of Eq. (6.2) can be expressed as

$$\delta(x) = N_T\left(1-\exp\left(-\left(-\frac{V_G}{V_m}t_m - \left(\frac{x^2}{\frac{2\varepsilon V_m}{qN_D}} - \frac{V_{bi}}{V_m}\frac{N_D}{N_D+N_T}\right)t_m\right)/\tau\right)\right) \quad . \tag{6.6}$$

The time when the gate voltage changes to V_G is $-V_G t_m/V_m$ and the moment when position x depleted is estimated with Eq. (6.5). Hence, N(x) can be obtained by substituting Eq. (6.6) into Eq. (6.2). This new N(x) is substituted into Eq. (6.3) the solution of which is a closer approximation of the relation between the depletion width W and the gate voltage V_G and can be written as

$$W^2\frac{qN_D}{2\varepsilon V_m} - \frac{V_{bi}}{V_m}\frac{N_D}{N_D+N_T} - \frac{N_T}{N_D+N_T}\left(\exp\left(\frac{V_G}{V_m}\frac{t_m}{\tau}\right)\right)\left(\exp\left(\frac{t_m}{\tau}\left(W^2\frac{qN_D}{2\varepsilon V_m} - \frac{V_{bi}}{V_m}\frac{N_D}{N_D+N_T}\right)\right)-1\right)\frac{\tau}{t_m}$$

$$= -\frac{V_G}{V_m}\left(1-\frac{N_T}{N_D+N_T}\right) \quad . \tag{6.7}$$

By setting $L = W\left(\frac{qN_D}{2\varepsilon V_m}\right)^{1/2}$, $\alpha = \frac{N_T}{N_D+N_T}$ and $\beta = \frac{V_{bi}}{V_m}\frac{N_D}{N_D+N_T}$, Eq. (6.7) can be simplified to

$$L^2 - \beta - \alpha\left(\exp\left(\frac{V_G}{V_m}\frac{t_m}{\tau}\right)\right)\left(\exp\left(\frac{t_m}{\tau}\left(L^2-\beta\right)\right)-1\right)\frac{\tau}{t_m} = -\frac{V_G}{V_m}\left(1-\alpha\right) \quad . \tag{6.8}$$

L, which is referred as the normalized depletion width later, can be estimated as a function of V_G/V_m and t_m/τ by using Newton-Raphson iteration.

When the gate voltage reaches $-V_m$, the depletion width is defined as W_m which can be obtained by substituting $-V_m$ to V_G in Eq. (6.7).

We now consider the return of the gate voltage from $-V_m$ to zero (Fig. 6.1d). The relation between the depletion width W' and the gate voltage V_G can be obtained similarly by solving

$$\int_{W_m}^{W'} N(x)\, x\,dx = -\int_{-V_m}^{V_G} \frac{\varepsilon}{q}\, dV \quad . \tag{6.9}$$

Since the trap occupancy is assumed to be frozen during this process, N(x) can be obtained by substituting Eq. (6.6) to Eq. (6.2) with $V_G = -V_m$. The solution of Eq. (6.9) is

$$L_m^2 - L'^2 - \alpha\left(\exp\left(-\frac{t_m}{\tau}\right)\right)\left(\exp\left(\frac{t_m}{\tau}\left(L_m^2-\beta\right)\right)-\exp\left(\frac{t_m}{\tau}\left(L'^2-\beta\right)\right)\right)\frac{\tau}{t_m} = \left(1+\frac{V_G}{V_m}\right)(1-\alpha) \tag{6.10}$$

where

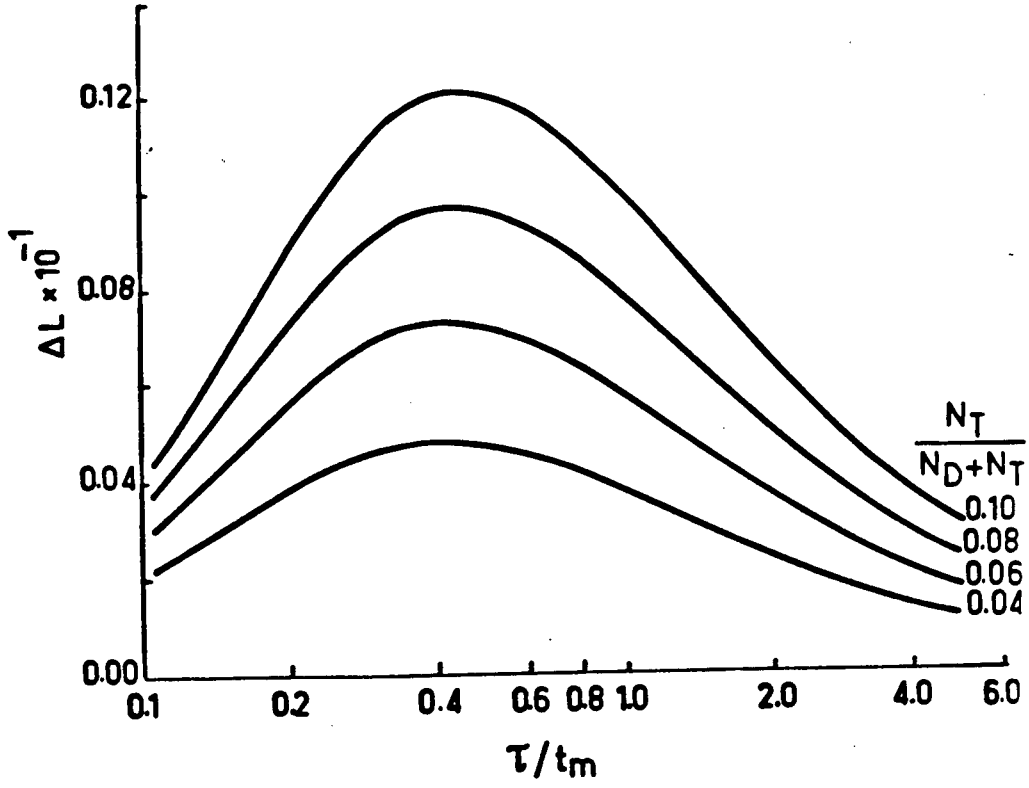
$$L_m = W_m \left(\frac{qN_D}{2\varepsilon V_m}\right)^{1/2}$$

and

$$L' = W' \left(\frac{qN_D}{2\varepsilon V_m}\right)^{1/2} .$$

L' can then be calculated as a function of V_G/V_m and t_m/τ.

The extent of hysteresis observed in the I_D-V_G characteristics is defined as the difference (ΔI_D) between the current I_D (when the gate voltage changes from zero to V_G) and I_D' (when the voltage returns to this V_G after reaching $-V_m$). With the preceding formulation, the hysteresis can be interpreted as a consequence of the inequality of L and L' at the same gate voltage because since I_D is considered to be proportional to the channel width, ΔI_D is proportional to $\Delta L = L-L'$. ΔL at $V_G = -\frac{1}{2} V_m$ has been calculated as a function of τ/t_m for different concentrations of deep level traps (Fig. 6.2a). Fig. 6.2b shows five more curves of ΔL (at $V_G = -\frac{1}{2} V_m$) vs. τ/t_m with different V_m values. These results suggest that the position of the maximum of the curve, ΔL vs. τ/t_m, does not depend significantly on the values of N_T and V_m in the indicated range. The maxima of these curves which correspond to the maximum extent of hysteresis at the indicated conditions always occur at $\tau/t_m \simeq 0.4$. The occurrence of a maximum logically follows the two qualitative considerations: (1) if $t_m^{-1} \ll \tau$ the traps in the



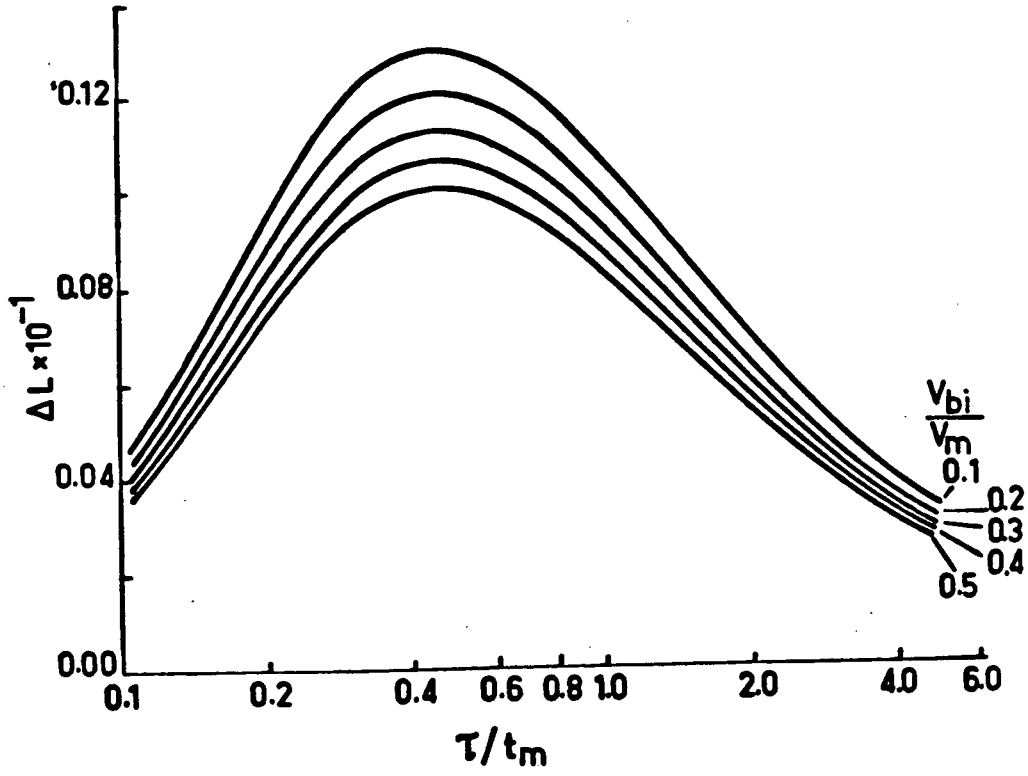


Fig. 6.2 The difference (L) between the normalized depletion width when V_G changes from zero to $-V_m/2$ as a function of normalized sweep frequency (a) for different N_T (b) for different V_m

depletion region can completely ionize and (2) if $t_m^{-1} \gg \tau$ the traps cannot respond to the sweep in voltage and remain neutral. In both cases no hysteresis results.

ΔI_D can be measured experimentally by sampling and comparing the current I_D and I_D' at the same V_G. The resultant plot of ΔI_D vs. sweep frequency ($1/t_m$) will be referred to as an I-V hysteresis spectrum (IVHS) by analogy with DLTS. Since ΔI is proportional to ΔL, the frequency at which the spectrum peaks gives the time constant of the traps

$$\tau \simeq 0.4\ t_m = (2.5 f_m)^{-1} \qquad (6.11)$$

In addition, the energy level of the traps can be estimated by measuring time constants at different temperatures and using Eq. (5.11).

6.2 Apparatus

The system shown in Fig. 6.3 was assembled to record the frequency behaviour of MESFET I_D-V_G hysteresis. Waveform generator 1 (Servomex LF51) generates a voltage ramp to control the frequency of the (saw-tooth) waveform generated by waveform generator 2 (IEC F63) and also drives the X-axis of a X-Y plotter (Moseley 135). The saw -tooth waveform is input to the gate of the MESFET sample and a comparator. The other input of the comparator is connected to a DC supply used to adjust the V_G at which drain current is sampled. Two pulses are derived from the output of the monostable multivibrators (MC 74121) and used to trigger the two LF398 sample and holds. Hence I_D and I_D' are measured at a desired V_G and input to a differential

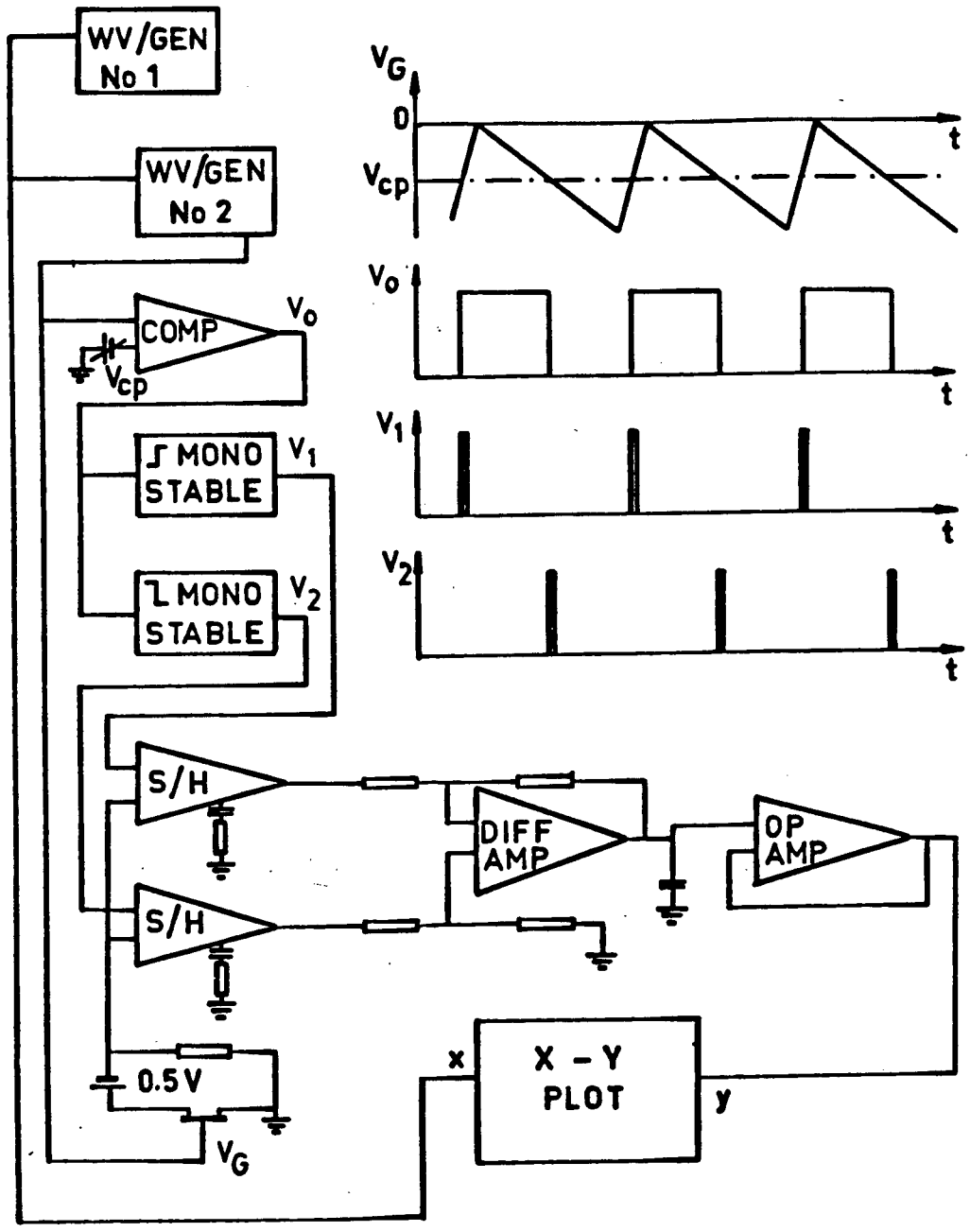


Fig. 6.3 Experimental arrangement for hysteresis measurements

amplifier. The output, a voltage proportional to ΔI_D is sent to the Y-axis of the plotter.

6.3 Measurements

To test the hysteresis model and apparatus, measurements were conducted on 30 μm MESFET 45-S93 R4-C3 as this device (which was processed by Tektronix Corp., Beaverton, Oregon) displayed prominent hysteresis (Fig. 6.4). A V_m of 1V, V_{DS} of 0.5V and sweep frequency range of 0-1 KHz were used. Sample temperature was varied from 300-350 K (using a Stratham SD6 oven).

IVHS spectra are shown in Fig. 6.5 revealing that ΔI_D does indeed peak at a certain frequency. The activation plot obtained from the IVHS spectra (calculated via Eq.'s 6.11, 5.11) is shown in Fig. 6.6. Also shown in Fig. 6.6 is the activation plot for the sample determined by CDLTS measurements. It is evident that the IVHS and CDLTS data agree (i.e. both reveal the presence of a 0.4 eV (electron) trap) thus showing the usefulness of the IVHS method for studying hysteresis in GaAs MESFET's.

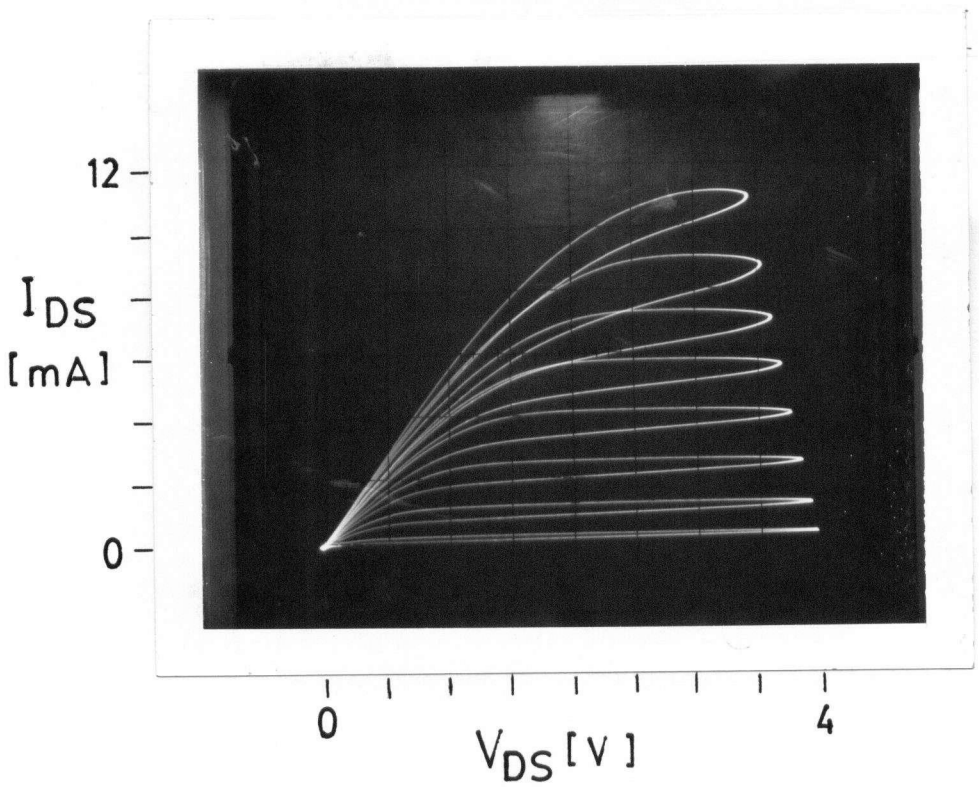


Fig. 6.4 I_{DS}-V_{DS} characteristics for MESFET 45-S93 (R4-C3). Gate bias step = -0.5 V

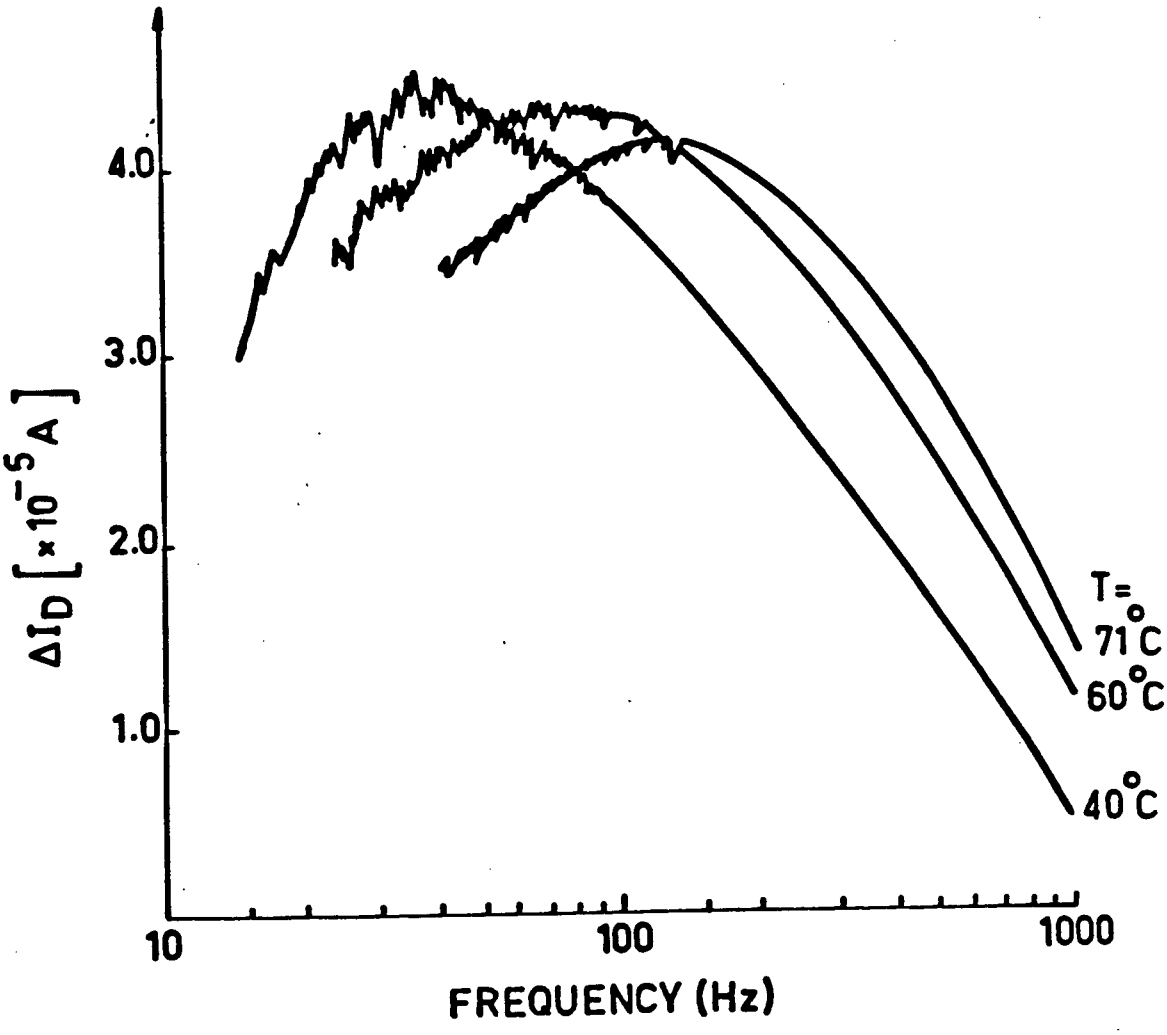


Fig. 6.5 Hysteresis spectra for MESFET 45-S93 (R4-C3)

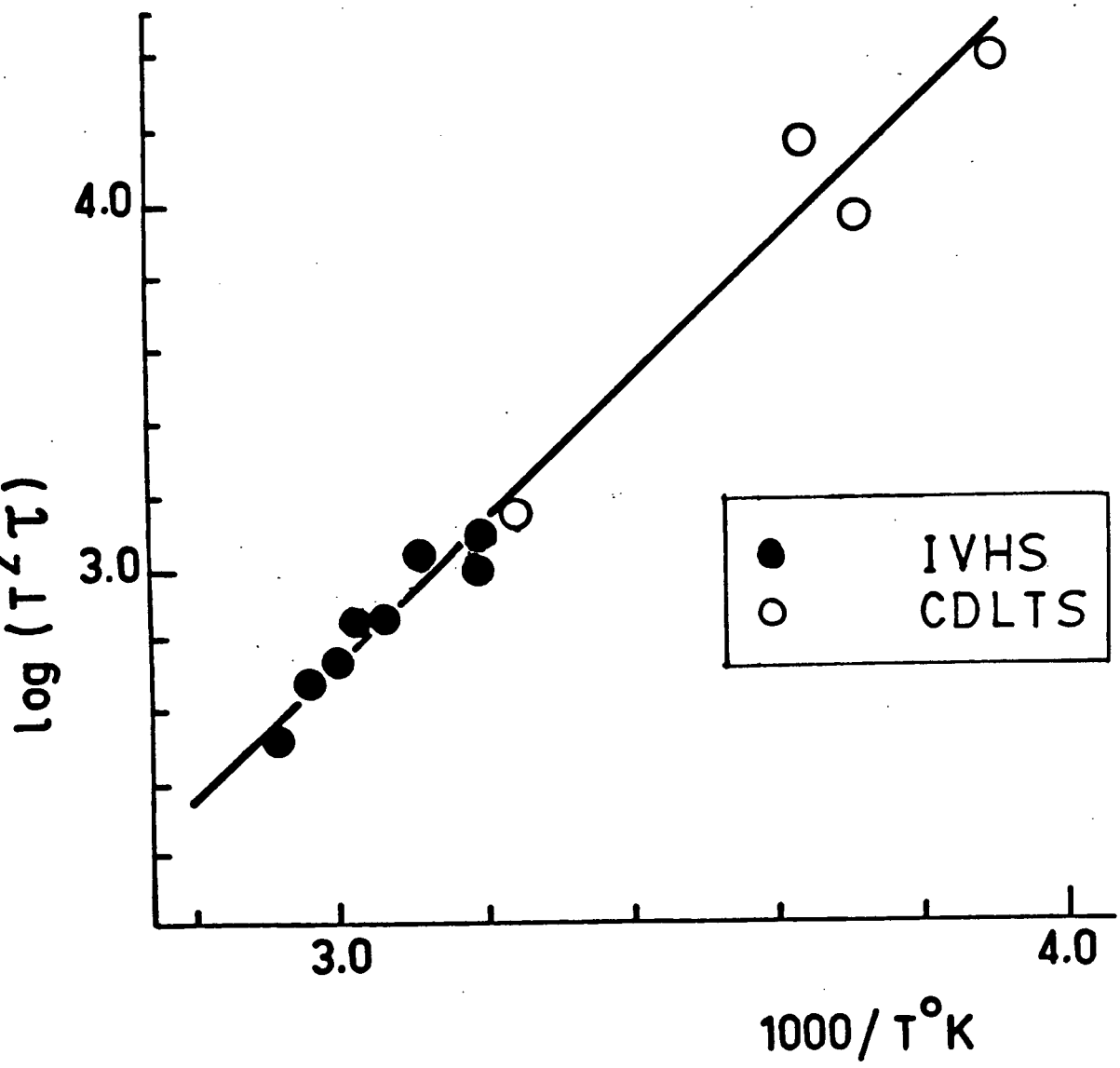


Fig. 6.6 Activation energy plot for MESFET 45-S93 (R4-C3) as obtained by hysteresis and CDLTS measurements

7. SUMMARY AND CONCLUSION

The purpose of this thesis was to develop a GaAs MESFET process technology and tools to assess GaAs and in this respect the following contributions have been made:

1. A GaAs MESFET fabrication process based on direct selective ion implantation into undoped LEC GaAs was developed which is capable of producing 2-10 μm MESFET's operational to 3 GHz.
2. A test device array was designed for use in process, material, and device characterization and techniques for using the array demonstrated. The array should be useful for future process development at U.B.C. and once a suitable process has been established for routine substrate monitoring by Cominco.
3. A channel conductance DLTS system was constructed and its use in assessing active layer quality shown.
4. A photocurrent DLTS system was constructed and its use in monitoring substrate quality demonstrated.
5. A technique for determining the deep levels responsible for hysteresis in GaAs MESFET's was developed.

Several suggestions for further work are made:

1. Although the process developed was shown to be capable of producing operational MESFET's improvements are required before GaAs MESFET IC's can be successfully produced. In particular it is suggested that for future GaAs MESFET fabrications that n^+ source-drain implants be used, that improved photolithographic equipment be obtained, and that

gate-source and drain-source spacings be minimized. The use of Si_3N_4 for the encapsulant (now possible with the recent acquisition of a Plasmatherm PK1250) may improve activation as Eisen et al. (1982) claims that Si_3N_4 is superior to SiO_2 in preventing Ga outdiffusion during annealing.

2. Further investigations on the deep levels detected by CDLTS are required. In particular since these levels appear to be process induced CDLTS spectra should be obtained for regions implanted with different doses, energies, species, and annealed with different times and temperatures.
3. Finally, since the usefulness of the techniques have been demonstrated, it is recommended that the DLTS systems be automated to allow routine material analysis and across wafer scans to be conveniently made.

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APPENDIX A - Substrate Compensation Considerations

The deep level believed to be responsible for compensating undoped LEC GaAs is the so called EL2 level (Martin et al., 1977). This level which is commonly detected in GaAs is a deep donor with a thermal activation energy E_T of 0.75 eV below E_c or more precisely (Martin et al., 1980)

$$E_c - E_T(EL2) = 0.759 - [2.37 \times 10^{-4} K^{-1}]T \text{ eV} .$$

If EL2 does govern the compensation in undoped LEC GaAs one may write from charge neutrality

$$p + N_d^+ + N_{dd}^+ = n + N_a^- \tag{A.1}$$

where n, p, N_d^+, N_{dd}^+ and N_a^- are the densities of electrons, holes, ionized shallow donors, ionized deep EL2 donors, and ionized shallow acceptors, respectively. To solve this equation for n at room temperature one may assume that $N_d^+ \approx N_d$ and $N_a^- \approx N_a$. N_{dd}^+ is calculated from

$$N_{dd}^+ = \frac{N_{dd}}{1 + \exp[(E_F - E_T)/kT]} \tag{A.2}$$

where E_F is the Fermi energy while n and p are governed by

$$n = N_c \exp[-(E_c - E_F)/kT] \tag{A.3}$$

$$p = N_v \exp[-(E_F-E_v)/kT] \qquad (A.4)$$

where N_c, N_v is the effective density of states in the conduction, valence band. ($N_c=4.7\times10^{17}cm^{-3}$ and $N_v=7.0\times10^{18}cm^{-3}$, Sze, 1981). Substitution of (A.2) to (A.4) into (A.1) yields

$$\frac{n^2 + n(N_a-N_d) - n_i^2}{n^2 + n(N_a-N_d-N_{dd})-n_i^2} = -\frac{N_c}{n}\exp[(E_T-E_c)/kT] \qquad (A.5)$$

Eq. (A.5) can then be solved for n (and p found from $n_i^2=pn$) and the conditions to achieve semi-insulating behaviour determined. Johnson et al. (1983), for example, have considered the case where $N_a-N_d=10^{15}cm^{-3}$ and $E_c-E_T=E_g/2$ and found that semi-insulating behaviour (i.e. $10^6cm^{-3}<n,p<10^8cm^{-3}$) is obtained when N_{dd} is between $1.5\times10^{15}cm^{-3}$ and $5\times10^{16}cm^{-3}$ which agrees with the EL2 concentrations measured by optical absorption by Martin et al.(1981).

The origin and chemical nature of the EL2 level is a subject of current debate. A Ga defect is believed to be involved but it is not clear whether the defect consists of a single Ga vacancy, a complex, or an antisite defect but the association of the level to oxygen (a long held belief) has recently been disproved by Huber et al. (1979). The prevading belief is that EL2 is an arsenic antisite defect, As_{Ga} (Lagowski et al. 1982).

It has been found that the resistivity of LEC GaAs depends critically on melt composition (Holmes et al., 1982). If an arsenic fraction of 0.48 to 0.51 is used, n type wafers of resistivity above $10^7\Omega cm$ result. If, however, the arsenic fraction drops below 0.475 p type substrates of much lower

resistivity emerge. These results are consistent with the theory that in a As rich melt a large number of Ga vacancies will be present tending to favour EL2 formation. At high arsenic fractions, >0.52, a large concentration of EL2 can be expected thus causing a drop in resistivity which was another observed result.

APPENDIX B - Some Ion Implantation Processes Used For GaAs MESFET Fabrication

Organization/ Reference	Active Layer Implant			Anneal			Comments
	Species	Energy	Dose	Temp.	Time	Cap	
Fujitsu Kitahara et al. (1980)	^{28}Si	250	4.5×10^{12}	850	15		
Hewlett-Packard Hornbuckle and Van Tuyl (1981)	^{29}Si	230	5.5×10^{12}	850	30	SiO_2	
Hughes Maki et al. (1981)	^{28}Si	100	5×10^{12}	850	30	SiO_2	
NEC Furutsuka et al. (1981)	^{30}Si	50	2.3×10^{12}	800	20	SiO_2	-$1.6 \times 10^{12} cm^2$ dose is used to achieve enchance- ment devices.
Rockwell Welch et al. (1980)	Si	400	2.2×10^{12}	850	30	Si_3N_4	-implant is done through 1100 Å Si_3N_4 layer. -S 350KeV $10^{13} cm^{-2}$ n+ implant used also.
Texas Instr. Tserng et al. (1981)	^{28}Si			850	30		-capless proximity anneal done.
Westinghouse Driver et al. (1981)	^{29}Si ^{29}Si	125 325	2×10^{12} 5×10^{12}	860		Si_3N_4	-implants done through 1000 Å Si_3N_4 layer.

APPENDIX C - Some Deep Levels in GaAs Detected by DLTS

Reference	Label	Electron/ Hole	E_T [eV]	log σ [cm^2]	Association	Material
Lang and Logan (1975)		E	0.86	-13.5	-	Epi (LPE) Cr level
		E	0.89	-12.7	EL2	Epi (VPE)
		H	0.78	-15.3	HL1	Epi (LPE) Cr level
	B	H	0.71	-13.9	HL2	Epi (LPE)
		H	0.52	-15.5	HL3	Epi (LPE) Fe level
		H	0.44	-13.5	HL4	Epi (LPE) Cu level
	A	H	0.40	-12.7	HL5	Epi (LPE)
Hasegawa et al. (1975)		H	0.58	-18.7	HL1	Epi (LPE)
		H	0.64	-15.4	HL2	Epi (LPE)
		H	0.44	-17.3	-	EPI (LPE)
Lang et al. (1976)	M4	E	0.48	-12.6	EL4	Epi (MBE)
	M3	E	0.30	-13.8	EL7	Epi (MBE)
	M1	E	0.19	-13.3	EL10	Epi (MBE)
Martin et al. (1977)	EL1	E	0.78	-14.0		Bulk
	EL2	E	0.825	-12.9		Epi (VPE)
	EL3	E	0.575	-12.9		Epi (VPE)
	EL4	E	0.51	-12.0		Epi (MBE)
	EL5	E	0.42	-12.9		Epi (VPE)
	EL6	E	0.35	-12.8		Bulk
	EL7	E	0.30	-14.1		Epi (MBE)
	EL8	E	0.275	-14.1		Epi (VPE)
	EL9	E	0.225	-14.2		Epi (VPE)
	EL10	E	0.17	-14.7		Epi (MBE)
	EL11	E	0.17	-15.5		Epi (VPE)
	EL12	E	0.78	-11.3		Epi (VPE)
	EL14	E	0.215	-15.3		Bulk
	EL15	E	0.15	-12.2		Epi
	EL16	E	0.37	-17.4		Epi (VPE)
Mitonneau et al. (1977)	HL1	H	0.94	-13.4		Epi (VPE) Cr level
	HL2	H	0.73	-13.7		Epi (LPE)
	HL3	H	0.59	-14.5		Epi (VPE) Fe level
	HL4	H	0.42	-14.5		Epi (VPE) Cu level
	HL5	H	0.41	-13.0		Epi (LPE)
	HL6	H	0.32	-13.3		Epi (VPE)
	HL7	H	0.35	-14.2		Epi (MBE)
	HL8	H	0.52	-15.5		Epi (MBE)

Reference	Label	Electron/ Hole	E_T [eV]	log σ [cm^2]	Association	Material
Mitonneau et al. (1977) cont'd	HL9	H	0.69	-13.0		Epi (VPE)
	HL10	H	0.83	-12.8		Epi (VPE)
	HL11	H	0.35	-14.9		Bulk
	HL12	H	0.27	-13.9		Epi (LPE)
Martin et al. (1978)	S2		0.74	-14.2	EL2	Bulk (HB)
	S3		0.57	-12.3	EL3	Bulk (HB)
	S4		0.35	-14.3	EL5	Bulk (HB)
	S5		0.34	-13.6	EL6	Bulk (HB)
	S1		0.80	-13.7	HL1	Bulk (HB)
	S6		0.27	-13.7	HL12	Bulk (HB)
Fairman et al. (1979)			0.48	-13.2		Bulk (HB)
			0.48	-11.2		Bulk (HB)
			0.35	-13.0		Bulk (HB)
			0.22	-14.7		Bulk (HB)
			0.75	-10.9		Epi (VPE)
			0.55	-14.2		Epi (VPE)
			0.55	-13.0	EL3	Epi (VPE)
			0.46	-12.7		Epi (VPE)
			0.34	-12.5		Epi (VPE)
Zylbersztejn et al. (1979)		H	0.96	-12.8	HL1	Epi (VPE)
		H	0.71	-14.2	HL2	Epi (VPE)
Jervis et al. (1979)					EL2	Epi (LPE)
					HL2	Epi (LPE)
					HL5	Epi (LPE)
					EL2	Epi (implanted)
					HL2	Epi (implanted)
					HL3	Epi (implanted)
					HL4	Epi (implanted)
					HL5	Epi (implanted)
					HL7	Epi (implanted)
					EL7	Bulk (implanted)
					HL1	Bulk (implanted)
					HL3	Bulk (implanted)
					HL5	Bulk (implanted)
Itoh and Yanai (1981)			0.75	-13.6	EL2	Epi (VPE)
			0.61	-11.8	EL3	Epi (VPE)
			0.94	-13.3	HL1	Epi (VPE)
			0.62	-14.1	HL3	Epi (VPE)
			0.41	-14.9	HL4	Epi (VPE)

Reference	Label	Electron/ Hole	E_T [eV]	log σ [cm^2]	Association	Material
Fairman et al. (1981)		E	0.26	-11.7		Bulk (HB)
		H	0.30	-13.2	HL12	Bulk (HB)
		E	0.34	-13.4	EL6	Bulk (HB)
		E	0.51	-12.0	EL4	Bulk (HB)
		E	0.65	-13.0		Bulk (HB)
		H	0.90	-13.7	HL1	Bulk (HB)
		E	0.15	-13.1		Bulk (LEC)
		H	0.30	-13.2	HL12	Bulk (LEC)
		E	0.34	-13.4	EL6	Bulk (LEC)
		E	0.60	-12.0	EL3	Bulk (LEC)
		E	0.65	-13.0		Bulk (LEC)
		H	0.90	-13.7	HL1	Bulk (LEC)
Yuba et al. (1982)			0.88	-12.3	EL1	Bulk (HB)
			0.54	-12.9	EL3	Bulk (HB)
			0.48	-13.2	HL4	Bulk (HB)
			0.34	-12.4	EL6	Bulk (HB)
Rhee et al. (1982)		E	0.90	-11.7		Bulk
		H	0.85	-12.9		Bulk
		H	0.73	-16.3		Bulk
		H	0.17	-21.4		Bulk
		E	0.52	-17.9		Bulk (implanted)
		E	0.17	-22.3		Bulk (implanted)
		E	0.21	-20.5		Bulk (implanted)
		H	0.84	-12.9		Bulk (implanted)
		H	0.15	-22.2		Bulk (implanted)