A new DSP controlled bi-directional DC/DC converter system for inverter/charger applications

by

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Abstract

As prices fall and performance increases DSP controllers are becoming increasingly attractive for use within switch mode power supply applications. However, due to the relative infancy of the technology questions remain concerning the practical implementation of DSP controlled power converters. This work is concerned with the application of current DSP hardware technology within a novel power electronic voltage converter system for combination inverter/chargers. Power circuit design, dynamic modeling, digital control and large signal computer simulation of a select 12:200 Volt, 400 Watt bi-directional dc/dc battery charge/discharge power-circuit are considered.

Initially, a novel DSP interfaced bi-directional dc/dc power circuit for the selected inverter/charger application is proposed. The proposed power-circuit is novel in its seamless two-quadrant bilateral charge/discharge operation based on a single duty cycle control input and fixed pattern DSP derived synchronously rectified PWM switching. A prototype power-circuit is designed and evaluated experimentally with various semi-conductor switch technologies. Ultimately the proposed concept is successfully proven using a combination of FET and IGBT high speed switching devices.

To control the power-circuit a tri-mode digital control system is further developed to regulate the power-circuit in three modes of operation: bus voltage regulation, constant current charge regulation and constant battery voltage charge regulation. Small-signal plant models are derived from the non-linear power-circuit using a novel combination of state-space averaging and MATLAB analysis. To facilitate closed loop feedback controller design digitized both proportional integral (PI) and pure integral (I) feedback control compensators are derived using "worst-case operating point" plant models and frequency domain stability analysis. The pure I controller technique is ultimately adopted due to its proven performance and implementation ease as compared to the PI controller designs.

To verify conceptually the system operation a novel MATLAB/SIMULINK based simulation method is developed to model the transient large signal behavior of the non-linear power-circuit. This reliable simulation tool is shown to model the numerical effects of the DSP, confirm closed loop stability to large-signal changes in operating point and generally verify successful operation of the proposed tri-mode control approach.

Finally, a prototype converter under closed loop DSP control is evaluated experimentally and its performance compared to the predicted results.

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Finally, this work is dedicated to my parents. Without their consistent motivation and support none of this would have been possible.

Chapter 1 - Overview

An inverter is a unidirectional power electronic device designed to convert direct current (dc) electrical power into an alternating current (ac) form in order to power a wide range of commonly available "household" ac loads. Inverters also make it possible to convert any environmentally benign dc power generation source such as solar, wind (non-synchronous generators), and fuel cells into usable ac power. Inverters are capable of providing stable ac power anywhere, especially in locations where dc generation is more available than ac mains power. Additionally, dc power generation from intermittent energy sources is often attractive because surplus generated energy can be stored and easily recovered using storage batteries. Similar energy storage and recovery is not as easily achievable with ac sources since storage batteries are dc by nature. However, there remain significant applications where ac energy storage and recovery are required.

Marine power systems (sailboats etc.) and un-interruptible power supplies (UPS) are primary examples of applications requiring stored ac power. In these applications an inverter produces ac power from a storage battery when grid power is unavailable. Upon the return of grid power the batteries are re-charged and maintained by an ac/dc power converter commonly known as a battery charger. When a single power electronic device can function as both an inverter and a battery charger it is known as a combination inverter/charger.

A bi-directional inverter/charger power converter has the ability to transfer and control power flow in both directions. In one direction the converter behaves as in inverter taking energy from the dc source and regulating the ac output to the load. In the other direction of operation the converter behaves as a battery charger, taking energy form the ac source and regulating the voltage and current returned to the battery. Appendix D presents various example inverter/charger configurations and applications.

A desired feature of a combination inverter/charger unit is to combine or share power components into a single bi-directional circuit topology. The combined topology is inherently reduced in size, component count, complexity and price [1,2]. Another desired feature is to implement centralized digital signal processor (DSP) based control. DSP control can drastically reduce component count, add flexibility and increase reliability

[3,4]. Today's motor controller DSPs have achieved a combination of computational performance, peripheral modules (ADCs, PWMs etc.) and cost allowing for their candidacy as practical and versatile full function switched mode power supply (SMPS) controllers. Traditionally, analog controller circuitry has been widely used to perform the control functions of SMPS circuits. Controller designs are developed using ubiquitous frequency-domain techniques and implemented with high performance, low cost yet inflexible analog-based controllers and PWM generators. However, for multifunction applications digital control design is difficult to ignore as full function programmable DSP processors allow for versatile power circuit control along with supervisory functions all on a single integrated circuit.

Relatively low cost bi-directional inverter/chargers (designed for common battery voltages <48V and conversion power <2KW) in the market today come in one of two main topological varieties: low frequency and high frequency.

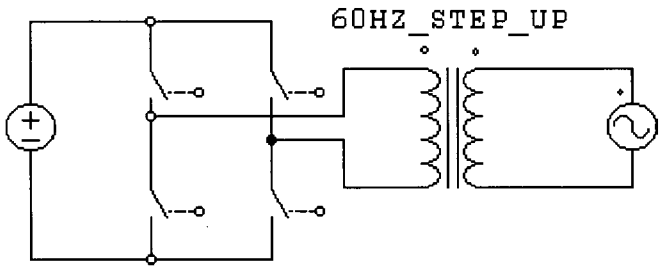


Figure 1: Example topology: Single stage inverter/charger with low frequency transformer

Low frequency designs typically utilize a single 50-60Hz transformer stage. During operation the dc source is actively switched across the appropriate primary taps to create the required ac output. The main distinguishing feature of the low frequency design concept is the resulting large size to power ratio of the 60 Hz transformer stage. Low frequency inverter and inverter/charger designs inevitably end up physically large, heavy and transformer dominated. A summary of advantages and disadvanages is presented in Table 1.

Advantage	Disadvantage
simple, robust, mature technology	noise - 120Hz buzz
no line voltage semi-conductors required - isolation	heavy and therefore expensive
may use low switching frequency - reduced EMI	large magnetics manufacturing
large electrical surge capability due to thermal mass	unattractive power density

Table 1: Low frequency topology advantages and disadvantages

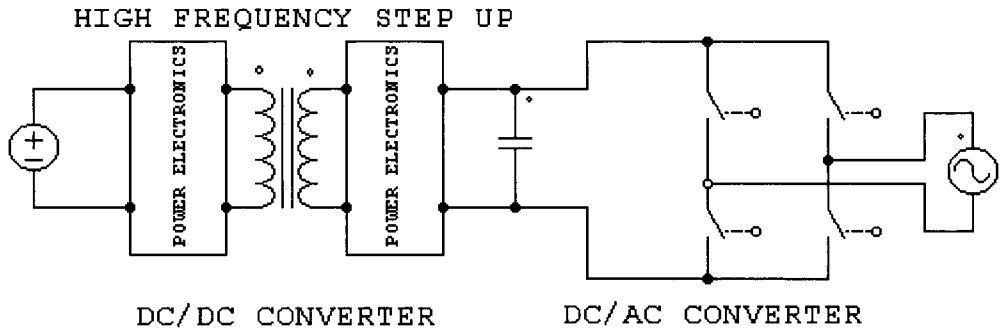


Figure 2: Example topology: Dual stage inverter/charger with high frequency DC/DC

High frequency designs rely on a switch mode dc/dc converter to convert the dc voltage potential between the dc voltage and a dc bus voltage higher than the peak voltage of the required ac. The dc bus is then inverted or rectified by an H-bridge of power switches to create the desired low frequency ac output. This concept eliminates the large low frequency transformer as the main voltage conversion device and replaces it with a compact high frequency dc/dc converter. The dc/dc converter's transformer stage often operates at frequencies in the tens of kilohertz, resulting in small magnetics, reduced mass and invariably lower cost. As with the low frequency designs, the high frequency designs also have advantages and disadvantages as found in Table 2.

Advantage	Disadvantage
high power density	line voltage semi-conductors prone to abuse
relatively inexpensive to manufacture	poor surge capabilities
compact	more difficult to engineer
silent operation	Increased switching losses
	high frequency EMI generation

Table 2: High frequency topology advantages and disadvantages

One school of thought espouses low frequency designs as superior because they are physically robust, simple and the design techniques are mature. However, overall cost is invariably the determining factor when considering any mass produced design. High volume production of high frequency power converters will ultimately be cheaper than low frequency designs because of their inherient increased power density and lower costs of production and distribution. In addition, high frequency magnetics, switches and controllers are constantly reducing in price whereas the bulky iron and copper required to produce low frequency devices are relatively fixed in price. The promise of a more cost effective technology continues to motivate research and development of smaller and lower cost high frequency based power electronic conversion technologies.

To further research in this area a novel 12V to 200V, 400W bi-directional prototype dc/dc converter system with a direct commercial application has been proposed, designed and constructed. The prototype converter has been specifically designed to meet the electrical specification of Xantrex Technology Corporation's RVSINE400 unidirectional inverter product. The fundamental commercial motivation of this industrial / academic collaboration is to evolve Xantrex's existing high frequency RVSINE400 inverter technology towards functioning as an inverter/charger with minimal additions of cost and components.

1.1 Problem Statement

Many high frequency or double stage inverter/charger technologies require a bi-directional 12V to 200V switched mode dc/dc converter to transform the battery voltage to a suitable and much higher dc link voltage. This thesis examines the problem of implementing modern low cost DSP processor technology as a versatile and adaptive single IC controller solution within an appropriate two quadrant bi-directional power circuit-topology. The initial challenges and questions faced for this industrially focused work were as follows: 1a) What is a reduced component count and cost effective dc/dc power circuit topology suitable for the application and also suitable for interface to the DSP controller? 1b) Is it possible to evolve an existing and proven industrial power circuit topology for seamless bi-directional operation to capitalize on existing industrial development? 1c) How is it possible to address the potential issue of magnetic flux imbalance? 2) How is it possible to propose and implement an adaptive digital control system approach to regulate the dc/dc power converter system autonomously in its three necessary modes of operation? 3) In order to perform the feedback controller designs how is it possible to accurately characterize or model the power circuit topology? Specifically, how is it possible to produce, refine and verify accurate state-space averaged models suitable for plant transfer function extraction? 4) Once the power circuit has been characterized, what is an appropriate digital control compensator design? 5) Is it possible to conveniently and accurately simulate the time domain behavior of the power circuit within MATLAB using the state-space-averaged model of the power circuit and a numerically accurate representation of the digital controller?

In this thesis the specific development of a novel digitally controlled and seamlessly bi-directional high frequency switch mode 400W dc/dc converter for battery charge and discharge regulation is explored and the above questions addressed. A novel dc/dc power processing system is ultimately derived by answering the above questions, solving practical design issues and by confirming performance experimentally.

1.2 Current state of the art / literature review

From its origins in the early 60's, the field of Power Processing or Power Electronics has been concerned with solving the challenges pertaining to the processing of electrical power from one form to another while striving for efficiencies approaching 100%. Specifically, Power Electronics is concerned with converting electrical power between and within the four electrical quadrants as defined in [5]. Although the standard ac transformer functions as an almost ideal power processor, it is fundamentally limited to single frequency ac operation. The field of Power Electronics is therefore concerned with developing regulated and efficient power processors that can transform voltage and current over a range of frequencies and within the four electrical quadrants. In particular, advances in power electronics have made it possible to produce efficient dc transformers or dc/dc converters.

The work contained within this thesis is specifically concerned with developing a DSP regulated dc/dc converter system suitable for two-quadrant battery charge and discharge regulation. In order to review the literature, an overview of the existing and current state of the art for two quadrant battery charge discharge technologies can be can further be broken down into three sections, namely: power circuit topologies modeling and control and circuit simulation.

Power circuit topologies

To achieve Power Processing efficiencies approaching 100%, lightweight switched-mode dc/dc power circuit topologies have been developed. A good description of the original and fundamental buck (step down), boost (step up) and buck-boost (step up-down) switched-mode dc/dc converter topologies appears in [6]. Also in [6] the concept of the two quadrant bilateral converter is introduced and its suitability to battery charging / discharging is discussed.

Enroute to developing an optimum topology dc-dc converter the Cuk converter topology is described in [7]. This reduced input and output current ripple converter features capacitive energy transfer and buck-boost voltage conversion. It also features a

distinct inverted voltage output. Significant to this work, this adjustable voltage ratio buck and boost Cuk converter is ultimately featured in a novel battery charge/discharge converter in [8] where the advantages of seamless bi-directional two quadrant operation are first described. In [8] the advantages of utilizing a single bi-directional topology are also highlighted. These advantages include: the elimination of discontinuous inductor current mode, prevention of circulating charge and discharge currents, and of course an inherent reduction in parts count. Unfortunately, the Cuk derived battery regulator application is non-isolated and limited to a relatively small potential difference between the battery and dc link voltages.

A further evolution of the bi-directional dc/dc regulator is presented in [9] where a larger conversion ratio two stage (buck and push-pull) SMART cell is presented. Although functional, the SMART cell is inherently two stage and utilizes three switching devices as opposed to a more attractive two device system. Additionally the spacecraft destined SMART cell is not developed as a galvanically isolated converter. That being said, successful operational results are presented with efficiencies recorded at 92%. Also in [9] the practical issue of switch synchronization is discussed and a hardware timing strategy to prevent switch overlap is presented.

An elegant seamlessly bi-directional single stage bilateral boost converter to convert between 100V and 200V is presented by Chang [10] and again in by Harachi [11]. This converter offers single stage adjustable voltage conversion yet lacks the range to convert between 12V and 200V as required for practical converter considered within this thesis. This same topology is used in [12,13] as a bilateral dc/dc conversion stage for a dc/ac inverter system. Although a unidirectional inverter, the bilateral dc/dc stage is necessary for producing distortion free full wave rectified sinusoids that are then inverted by a slow speed dc/ac H-bridge. Again, the practical application of this circuit is hindered by its lack of galvanic isolation and unsuitable voltage conversion ratio. However, the concept of forming distortion free full wave rectified sinusoids using the bilateral nature of the converter is successfully demonstrated.

Harachi, in a later development, adapts the elegant single stage approach for a wider voltage conversion ratio in [14]. The only modification is the addition of a single strategically placed coupled inductor. The results include improved current stress, wider

voltage conversion and significantly increased efficiency. In fact, if it were not for the lack of galvanic isolation the improved converter would serve as an ideal candidate for this thesis application. As is stands, it still has a strong practical potential for non-isolated bi-directional battery regulators converting between ubiquitous 12V batteries and the 200V bus voltage necessary to form standard 120VAC.

Another novel idea attempted recently is the utilization of switched capacitors to create a two-quadrant bilateral dc/dc converter [15]. This method uses a string of cascaded bi-directional capacitor converter cells. The interesting feature of this type of converter is the complete absence of inductors leading to the potential development of monolithic integrated converters. However, the converter of [15] has only been demonstrated using a two cell string, converting between only 5V and 12V. Even with the short two-cell string the efficiencies were measured to only be approximately 80%.

Of the converter topologies appearing in the literature, the most relevant to this thesis appears in [1]. The converter presented therein is specifically designed for galvanically isolated battery charge discharge regulation with a large conversion ratio of 48V to 350V. To minimize pulsating battery currents and associated EMI, the converter features a current fed push-pull battery interface topology. The isolated high voltage side features a half bridge of switching devices and double transformer winding. It is argued that a benefit of the proposed current fed push-pull to half bridge design is the reduction of switch stress. It is also stated that although efficient soft switching technologies have been reported in the literature they often lead to increased complexity, higher conduction losses when resonating and narrow regions of soft switching operation. In the proposed design the off switch stress of the high side devices is limited to the value of the dc source rather double the voltage as found with traditional push-pull and single ended forward converters. It is also argued that for the low power application (<500W) the two switch half bridge is preferable over the four switch full bridge. However the application of the half bridge design presented requires the addition of two additional capacitors and two diodes resulting in a fundamentally higher component count. In [1] it is also noted that the current fed battery side is appropriate as the current is shared equally between the switches, reducing not only the RMS switch current but also the RMS winding current. However, the power-circuit as presented is not configured to operate in a seamless

bilateral manner. There are two distinct modes of operation: forward and reverse and the power is not free to flow in the counter direction unless the switching pattern is changed accordingly.

The Clarke converter topology as described in [16] is very similar to the topology presented in [1]. Using the Clarke topology one can retain all the benefits of the current fed push-pull low voltage battery side and also capitalize on a reduced component count two switch push-pull high voltage side. The main, albeit minor, disadvantage is the double high side voltage switch stress. This is of little concern with the thesis converter as suitable high side IGBT switch components are rated for at least 600V, which is much more than the double the 200V experienced with the thesis converter. In fact, the Clarke converter is a proven topology and is used extensively in industry as the unidirectional dc/dc convert stage for many current high frequency inverter products - although not yet in a seamless two quadrant manner.

Converter modeling and control

From the very early stages of Power Processing, one of the main challenges was in the area of producing suitable circuit models for the highly non-linear and discontinuous switched-mode circuit topologies. To complement the largely empirically designed ("guess and check") early regulators, work was performed to develop a suitable modeling approach from which the describing functions of the power-circuit plant could be obtained - and to which established control theory could be applied. This work culminated with the versatile and widely adopted state-space averaging technique presented in [17]. The state-space averaging method allows for the input to output and duty-cycle to output small signal transfer functions to be derived. It is reported that the transfer functions are accurate to within $1/10^{th}$ of the fundamental switching frequency. This is more than adequate for most control bandwidth requirements. In [18] it is shown that the parasitic circuit resistances play a significant role in obtaining an accurate state-space averaged model of the switching converter. Generally, omitting the parasitic resistances leads to less than accurate predictions of conversion efficiency, static dc

operation point, and most significantly an erroneous ac small-signal system response. It is therefore important to consider and account for this effect.

In [5] it is pointed out that ease of understanding, design and analysis are crucial for accepted application of the switching converter technology. While the static or dc large signal properties of the converter are easy to understand, the non-linear ac subsystem characteristics present a significant challenge to the designer and often result in overly cautious closed loop regulator designs. From this one can surmise that simplifications in the closed loop regulator analysis and design procedure are of distinct value. In [19] simplified methods for obtaining the crucial system transfer functions are presented. Specifically, the concept of using the state-space averaged model and a 'small computer' to compute the system describing functions is introduced. This special purpose computerized analysis is referred to as the switching converter analysis program or SCAP. Comparing the SCAP results to the measured magnitude and phase response of the converter can then further refine the derived state-space model in a fast iterative fashion. However, obtaining the measured frequency domain information remains not a trivial operation. One needs to either manually inject a small ac perturbation and measure point by point the frequency response (tedious) or utilize a very expensive automated frequency sweeper. Additionally, even through the frequency sweeper may be automated, one will still need to evaluate manually the pertinent range of dc operating points. Furthermore, these techniques of measuring the response of a small superimposed ac component lose relevance once the duty-cycle becomes significantly quantized and immune to the injected perturbation – as with a digitally derived duty-cycle control output.

As mentioned previously, the describing functions can be used in combination with closed-loop control theory to create stable closed-loop regulators that are carefully designed for maximum control response speed. To further complement these feedback regulator designs, a constant-frequency current programmed control is introduced in [20]. Current mode control relies on programming the current rather than the duty-cycle directly. Instead of the feedback control signal directly controlling the switch duty-cycle, the control signal programs another controlled stage that fundamentally limits the current by switching off the switch once the programmed current is achieved. It turns out that

this relatively simple current programming technique has a number of distinct advantages. These include, inherent current limiting, easy paralleling and current sharing due to a common programming signal and a net one pole control signal to output transfer function that can lead to a significant increase in control bandwidth. Current mode control is not without its share of caveats. Specifically, constant frequency peak current mode controlled converters are open loop unstable for duty-cycles exceeding 50% [20]. Also current mode control is more difficult to implement using a single IC controller unless the controller has been specifically designed to do so.

To compensate for the inherent operating point dependent plant models of SMPS converter an adaptive controller technique has been developed in [4,21,22,23] and later implemented with a DSP in [24]. The premise of the control approach is to adjust the feedback controller coefficients as a function of the circuit operation point. In the proposed approach the feedback coefficients are designed to maintain a prescribed dynamic response regardless of the operating point of the circuit using a pole-placement technique. The DSP implementation of this technique took advantage of the processor's ability to actively compute the control gains in real time according to the measured operating conditions of the circuit. Although the technique offered some increase in performance it is not thought dramatic enough to benefit the application this work relative to the required increase in control complexity. Additionally, the state-feedback pole-placement technique presented is fundamentally not attractive for a set-point regulating system requiring minimum steady-sate error. A regulating push-pull dc-dc converter with linear state feedback and steady state error reducing integral control is presented in [25]. Also in [25] it is argued that by synchronously rectifying the switches bi-directional inductor current flow can be achieved. Incidentally, it is demonstrated that the bi-directional current allows a smaller inductor to be used while still maintaining continuous inductor current operating conditions. The direct benefit of this is an increase in the dynamic response of the circuit and faster control action.

Another adaptive controller for boost converter control is found in [26]. A gain scheduled PI controller is presented for controlling a boost converter over a wide range of output voltage and loading. It is demonstrated that a controller designed with a linear PI regulator must be designed at the highest current and lowest voltage of the converter's

operating envelope. It is shown that the performance of PI the control can be further improved by gain scheduling the proportional and integral coefficients as functions of the output voltage and current of the boost converter. While some improvement is shown in simulation results, the overall improvement over the worst case linear design does not appear worth the added complexity and computational effort.

In [27] various digital control strategies are compared for implementation within a two wheeler forward converter. Controllers are designed using a discretization of the analog controller, direct digital PID design and a dead beat controller design. The results indicate that the PID controller yields the best combination of control bandwidth, phase margin and 10Hz gain. However, the exact performance criteria to which the each of the controllers are designed remains unclear. The same converter is later explored in [28] where a DSP based fuzzy controller is proposed and implemented. The premise of this paper is to create a controller that offers high performance while controlling through the cross-operation of both continuous and discontinuous inductor current modes of operation. Again, the flexibility of the DSP is used to implement the fuzzy rule look-up tables used to create a non-linear fuzzy controller. The results show the controller as capable of managing the two operational modes with good dynamic response. The authors argue that an advantage of the fuzzy control is lack of a required mathematical model. However, the lack of both mathematical model and defined design procedure results in a time consuming educated guess and check approach to defining the fuzzy membership functions. The fuzzy controller idea is improved upon in [29] where a digital integrator is used in parallel with the proportional derivative based fuzzy rule table. In this paper it is argued that the digital integrator and direct fuzzy duty cycle output can provide improved steady state error and faster response time as compared to the traditional incremental fuzzy output due to the improved resolution of the independent digital integrator.

Another interesting comparison of digital controller design techniques is presented in [30]. In this work five digital control design approaches are evaluated for realizing the useful digital PI controller. Of the five approaches one is direct PI digital design while the remaining four are common digital emulations of the s-domain PI transfer function. The results indicate that given a control design specification the resulting performance is

clearly superior from a control bandwidth, percent overshoot and phase margin point of view using the direct digital design. This suggests that there is some benefit to creating an initial z-domain model of the plant and directly designing the z-domain PI controller transfer function as opposed to designing completely in the s-domain and creating a z-domain controller by emulation.

Another consideration when implementing digital control is that of analog to digital converter (ADC) input and duty-cycle output quantization. The bit resolution of the ADC input can limit precision to which the controller can regulate. A lack of bit resolution in the duty-cycle PWM can lead to limit cycle oscillation where the duty-cycle oscillates between two outputs while trying to regulate an in-between value. Design guidelines to insure adequate bit resolution are presented in [31]. The necessary condition required to avoid limit cycle oscillation is to have the change in the output by a LSB change of the duty-cycle result in a less than LSB change in the measured output's ADC value. This is of course not very practical as may ADC converters have resolutions of 10 bits or more and this type of duty-cycle resolution is simply not achievable with today's DSP processors and their relatively slow count up count down PWM generation. In [31] the 1 Mhz switching frequency for the example converter is created with an external PWM IC that is simply fed with an appropriate resolution duty-cycle integer value from the DSP. The future evolution of DSP controllers with built in fast and high-resolution duty-cycle outputs is also discussed. Another technique for increasing the effective PWM resolution is by using a doubling technique as presented in [32]. The doubling technique requires the timer limited PWM to be sub-modulated. For example, a periodic 10 pulse train at a duty-cycle of (34/64)% five of them can be made (35/64)% to get an quasi-intermediate (34.5/64)%. Although the doubling effect also introduces extra harmonics to the system, overall effects are reported to be as follows. Increase in the modulating accuracy of the high-frequency PWM with finite timer resolution. A reduction of control over-shoot and an improvement in the control performance without increasing the processor operating frequency.

For applications that are cost-driven, low-power and high-frequency a look-up table PID controller approach is proposed in [33]. The concept is to utilize small look-up tables to calculate the difference equation rather than to multiply the present error and historical

terms with the controller coefficients. For a small range of errors and historical terms the controller coefficient products are stored in a look-up table. This allows for a very low-performance and low-cost processor (without a hardware multiplier) to quickly perform the duty-cycle calculation. The high-speed external PWM IC, as presented in [31], then further provides the high-frequency PWM. It is demonstrated how a buck converter can be PID controlled using only 255 bits of look-up table memory and no multiplications.

Circuit Simulation

A good discussion of available simulation approaches and simulation tools is described in [34]. The long computational efforts and non-convergence pitfalls associated with simulating detailed power circuit models are highlighted. A new non-linear switched state-space technique implemented in the MATLAB/SIMULINK environment is proposed to increase simulation reliability and capitalize on widely available software. However, as compared to other large-signal switched models where components are inserted and system directly simulated, the proposed technique requires some somewhat tedious algebraic work to generate the switched state-space model.

A closed loop digital simulation model using a state-space averaged power-circuit representation has been presented in [35]. However, the model is linear and not valid for changes in circuit operating conditions - a feature that is necessary for simulating the behavior of the power circuit to external plant perturbations. A similar approach is also demonstrated in [36] where a linear model of the buck converter is utilized. Ultimately the experimental results differ significantly from the simulated results under varying operating points because of the crude model approximation. However, the numerical effects of the practical 8-bit digital controller are considered. Results are presented for an idealized digital controller with no numerical considerations and compared to simulation results that include numerical effect such as integer quantization, ADC resolution, saturation, computational delays etc. The non-ideal SIMULINK controller model provided results in closer agreement to the experimental results.

1.3 Summary of contributions

The overall contribution of this thesis is the presentation of a new single IC DSP controlled dc/dc converter system for inverter charger applications. Specific contributions contained within the overall autonomous "high voltage regulated battery" power converter system are summarized in the following paragraphs.

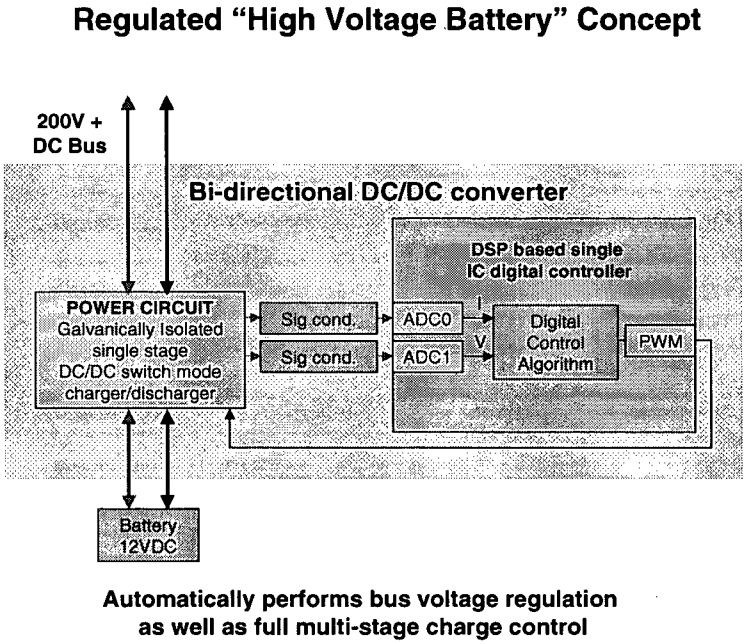


Figure 3: Proposed high frequency DC/DC converter system

It is shown that the traditional unidirectional Clarke topology power-circuit featured in existing commercial products can be modified to operate in an efficient and seamlessly bi-directional manner by the addition of active high side switching devices and direct DSP PWM. A low cost method for providing necessary switch timing adjustment via simple charge resistor and discharge diode has been verified. For the given application, the use of a high side IGBT device was determined to be superior as compared to a FET device due to the faster reverse body diode characteristics of the former. Perhaps most significantly, the proposed synchronously rectified design also

eliminates the discontinuous inductor current mode of operation, which allows for simplified control design and analysis. Additionally, the seamlessly bilateral inductor current is critical for implementation of the state-space averaged circuit model based simulation technique presented within this thesis.

A second contribution is the automatic multi-mode adaptive control approach used to control the dc/dc converter in its three distinct modes of operation. The control system designed allows the converter to essentially function as an autonomous yet regulated high voltage battery. Most notably, the digital control system automatically adapts to the appropriate regulatory control mode based on measured voltage and current from the converter's high voltage side only. This is made possible by implementing a proposed *control mode decision making algorithm* within which the low side battery voltage and current information are calculated from high side voltage and current measurements.

Another contribution offers an improvement in the area of characterizing the dynamic properties of the power-circuit plant. In order to obtain small signal plant transfer functions the power-circuit is modeled using the well-developed state-space averaging technique – specifically including parasitic resistive elements to represent the dissipative effects of the power switches. A MATLAB simulation algorithm is developed from the state-space representation to perform a discrete time-domain simulation of the power-circuit with respect to large-signal changes in switch duty-cycle. In this way large-signal simulated results can be compared to easily obtainable experimental results within the time-domain. This allows for the power-circuit model to be refined in a single step using only a simple oscilloscope rather than the traditional point by point frequency-domain approaches that use a small injected ac signal. The result is an easily refined and accurate state-space model from which the small-signal plant transfer functions can be derived with confidence.

As a final contribution, a technique for simulating the entire closed loop DSP controlled power conversion system is presented. Using this convenient MATLAB-based simulation tool the closed loop performance of the power-circuit can be verified including, specifically, the numerical effects of the DSP.

Chapter 2 - Bi-directional power-circuit

In this chapter a novel seamlessly bi-directional FET and IGBT based power circuit for the high frequency dc/dc converter is proposed. Initially, the basic switched mode power-supply forms are introduced and a suitable power circuit topology is derived. The power circuit is then analyzed, designed, constructed and evaluated by experiment. This chapter also explores the concept of active transformer flux balancing. Efficient, balanced and seamless operation of a proposed power circuit, in both directions, is demonstrated. Ultimately, the question of defining an appropriate power circuit for DSP integration is answered.

2.1 Bi-directional DC/DC converter power-circuit topology

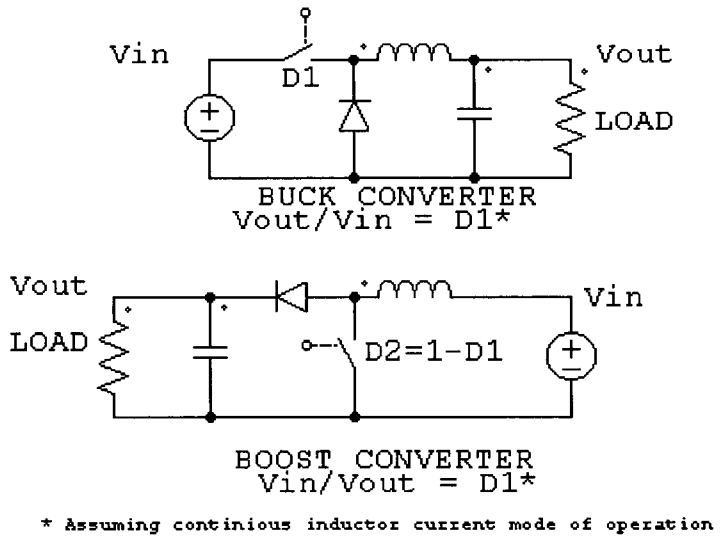


Figure 4: Buck and boost converters

All voltage converting dc/dc switch mode power supply (SMPS) circuit topologies are variations of the standard buck and boost converters shown in figure 4 [16]. The power electronic switch devices operate at switching frequency, f_s, and with duty cycle, D to achieve a dc voltage conversion. A basic seamless bi-directional converter is shown in figure 5. It is a synchronously rectified combination of the two converters appearing in figure 4 where two switching devices are alternately gated. The

diodes in the figure 4 have been replaced with switches that are actively gated, or synchronously rectified, when the diodes would ordinarily be forward biased. Synchronous rectification is an increasingly common technique used to improve the efficiency of low voltage, high current power supplies as the ~1V forward voltage diode drop can be replaced with the lower power dissipation on characteristics of the device.

As can been seen in figure 5, synchronous rectification also creates an inherently bi-directional power circuit that functions as a boost converter in one direction and a buck converter in the other [8]. The duty cycle simply governs the voltage conversion ratio between the input and output of the converter. Current flows according to the voltage and series impedance of the source/sinks. Also, with this type of circuit, discontinuous inductor current mode of operation is eliminated as power and current are free to flow in either direction at all times through the inductor. It is this concept of seamless power flow that we wish to apply to the power circuit of the thesis converter. However, the circuit of figure 5 is not suitable for the inverter/charger application. It is not capable of efficiently providing the large voltage conversion ratios required. For example, a voltage conversion ratio of 200V:10V requires a duty cycle of 5 percent. Generally, duty cycles of less than 10 percent are inefficient and undesirable. Also, as a practical caveat, the example requires uneconomical switches that must operate at both high peak voltage and high peak current.

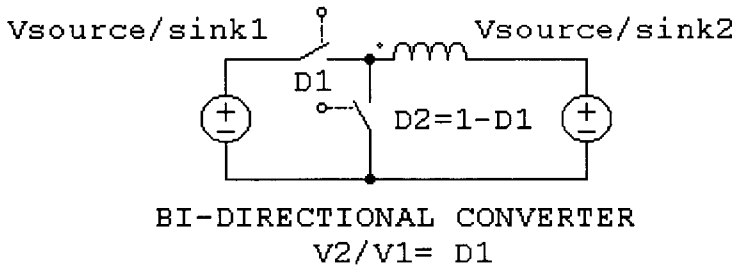


Figure 5: Bi-directional buck boost converter

The addition of an ideal transformer in figure 6 proposes a solution to the above problems and provides the galvanic isolation between the converter's input and output required for regulatory approvals. With the transformer the duty cycle can be increased, the low voltage switch can have a reduced voltage rating and the high side switch can

have a reduced current rating. However, while acceptable to many computer simulators, this circuit also does not work in the real world because of constantly increasing dc magnetic flux within the transformer core. To keep the core out of saturation the magnetic flux must alternate directions while keeping within saturation limits. To this end, the integrated volt-seconds impressed on the windings must equal zero requiring a slightly more complicated approach.

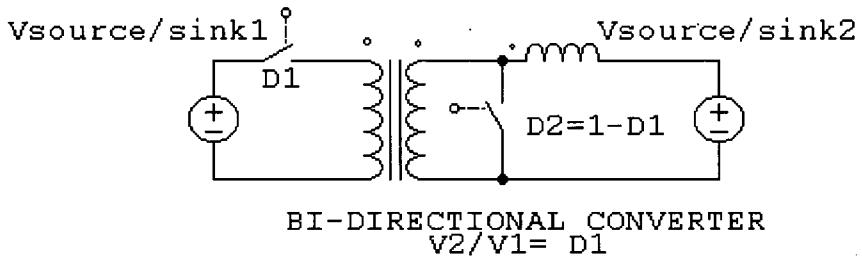


Figure 6: Transformer coupled bi-directional converter

Over the years, many transformer coupled bi-directional dc/dc converter topologies designed for power conversion between battery voltages and higher bus voltages have appeared in the literature [1,8,9]. Early lightweight, switched-mode topologies were originally developed for use in space exploration while later evolutions are more specific to UPS and telecom applications. The dc/dc converter required for this work's inverter/charger application has a number of specific practical requirements including: 1) galvanic isolation between the low voltage and high voltage terminals, 2) current fed topology to reduce large pulsating battery currents, 3) voltage conversion range from a nominal 12V (10V-15V) battery to a 200V+ DC bus, 4) ability to be controlled in constant current and constant voltage modes for battery charging and 5) ability to operate in constant voltage mode for regulating the DC bus while in an invert or battery discharge mode.

Of the converters appearing in the literature, Jian [1] proposes an almost ideal current fed, push-pull design from a topological point of view while Middlebrook [8] proposes a non-isolated, synchronously rectified Cuk converter that is entirely suitable from an operational point of view. Jian's converter is designed to operate in one of two

modes of operation: forward or reverse. In each direction of operation, one side acts as a freewheeling rectifier while the other actively switches the power. The power is not free to flow in either direction unless the appropriate switches are actively gated. In Middlebrook's approach the switches are gated as opposite pairs and power is free to flow in both directions. Discontinuous inductor current mode is completely avoided eliminating the changes in dynamic circuit behavior when operating in the discontinuous mode [8,16]. Additionally, the complications of unknown circuit dynamics during direction change are avoided as only one continuous nonlinear model governs circuit dynamics for both directions of operation. Although the previous two circuit topologies are different, it is later observed in this thesis that the possibility of applying Middlebrook's synchronously rectified approach to a topology similar to Jian's exists. A similar but even more optimized circuit to Jian's is presented later in this chapter.

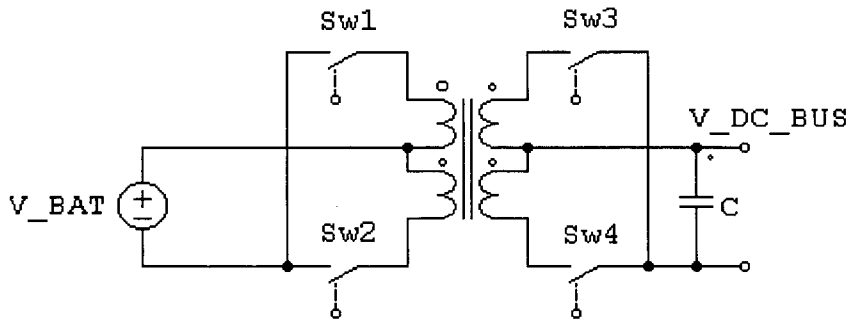


Figure 7: Example topology: voltage fed bi-directional DC/DC

As mentioned previously, the battery charge/discharge power-circuit required for this thesis work must operate over a wide range of voltage conversion ratios. According to the electrical specification of appendix A, the battery may vary from 10-15V while the dc bus can vary from 200 – 250V. The power circuit must efficiently perform over this range of voltages. To satisfy the requirements of appendix A, achieve efficient performance and keep magnetic flux within limits a transformer coupled push-pull type dc/dc converter is required. The two fundamental types of transformer coupled push-pull dc/dc converters appearing in the literature are referred to as voltage fed and current fed.

Figure 7 displays the basic topology of a bi-directional voltage fed inductor-less converter topology. The distinguishing feature of this bi-directional converter, as

compared to a unidirectional converter, is that either Sw1 & Sw2 or Sw3 & Sw4 can be gated as pairs to control power flow. The converter operates under the same principle in either direction. In one direction, invert mode or forward mode, Sw1 and Sw2 alternate to switch ac power into the transformer keeping the core flux alternating. Sw3 and Sw4 act as rectifier diodes allowing power to flow onto the higher voltage dc bus. In the other direction Sw3 and Sw4 switch power into the transformer while Sw1 and Sw2 act as rectifier diodes allowing power to flow from the higher voltage dc bus to the lower voltage battery. However, the main drawback with this type of converter is the voltage conversion ratio is not a function of the switch duty cycle. The duty cycle of the switches can be adjusted but the voltage pulses on either side of the transformer are fixed by the transformer turns-ratio. Ultimately, this type of converter is not suitable for applications requiring a variable voltage conversion ratio and especially not suitable for controlling battery charge currents.

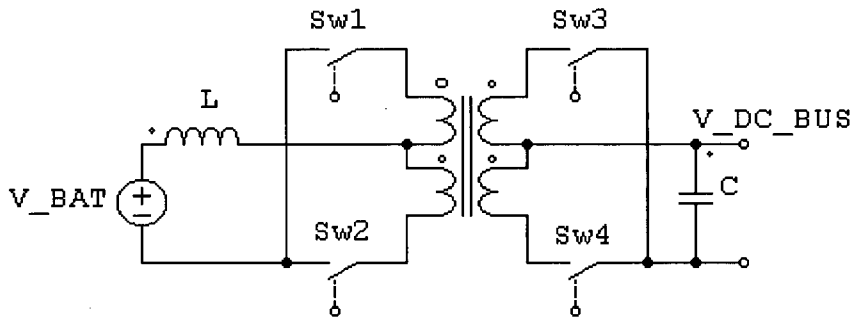


Figure 8: Example topology: current fed bi-directional "Clarke" DC/DC [16]

Current fed converters, on the other hand, feature a current sustaining and energy storing inductance located on one side of the transformer. The side of the converter featuring the current sustaining inductance experiences near constant dc current (in the time scale of the switching frequency) while the other side experiences pulsating currents. Adding an energy storing inductance on the battery side of figure 7 creates the current fed converter seen in figure 8. Specifically, the addition of the energy storage inductance allows the voltage conversion ratio of the converter to become a function of the switch duty cycle creating a converter suitable for this application of this thesis. In the case of an inverter/charger application, it is beneficial to locate the inductance on the

lower voltage and higher current battery side. Two benefits are reduced RMS power circuit currents and reduced EMI radiation.

This popular primary centre taped transformer topology of figure 8 is named after Clarke who patented the Sw1 and Sw2 'boost' overlap technique in 1976 (US Patent 3938024 to Clarke). The defining characteristic of the *Clarke* converter is that in forward mode both control switches are overlapped for a period of time to store energy in the inductor. This stored energy is then released to the secondary when either of the switches is opened. The following analysis discusses how the current fed Clarke topology operates in forward mode to provide the relatively wide range of voltage ratios required for the thesis converter application.

When in forward or invert mode the converter must take power from the approximately 12V battery and convert it to the much higher dc bus voltage. Sw1 and Sw2 are used as the control switches while Sw3 and Sw4 act as rectifiers. Table 3 describes the three states of switch operation and the switching patterns required.

Switch Pattern, (state)	**Action**
Sw1 & Sw2 closed (1)	Current in the inductor, L, ramps up
Sw1 closed, Sw2 open (2)	Current in the inductor ramps down, power transferred to dc bus.
Sw1 & Sw2 closed (1)	Current in the inductor, L, ramps up
Sw1 open, Sw2 closed (3)	Current in the inductor ramps down, power transferred to dc bus.

Table 3: Clarke converter forward (battery discharge) switch pattern

While operating with continuous positive inductor current and when both switches are closed, the primary of the transformer is effectively short circuited and the current ramps up in L according to:

$$\frac{di_L}{dt} = \frac{V_{BAT}}{L} \qquad (2.1.1)$$

When only one switch is closed the current ramps down in L according to (2.1.2) where N is the transformer turns-ratio.

$$\frac{di_L}{dt} = \frac{V_{BAT} - \left(\frac{V_{BUS}}{N}\right)}{L}$$

(2.1.2)

Using (2.1.1) and (2.1.2) the steady state voltage relationship can be described by (2.1.3) as a function of the switching duty cycle where D is the switch duty cycle and represents the time of switch overlap as a percentage of the overall switching period.

$$VBUS(D) = \frac{V_{BAT} \cdot N}{1 - D}$$

(2.1.3)

Here it is noted that (2.1.3) is the same the general boost equation of (2.1.4)

$$V_{out}(D) = \frac{Vin}{1 - D}$$

(2.1.4)

and conclude that the transformer coupled push pull Clarke converter fundamentally behaves as a boost converter. This allows the battery voltage to vary while regulating the dc bus voltage by adjustment of the switch duty cycle. Converter waveforms generated by the PSIM circuit simulation software can be seen in figure 9 where

D=0.33
VBAT=12V
VBUS=180V
N=10
L=10uH
fs=80KHz
DC Bus load=150W.

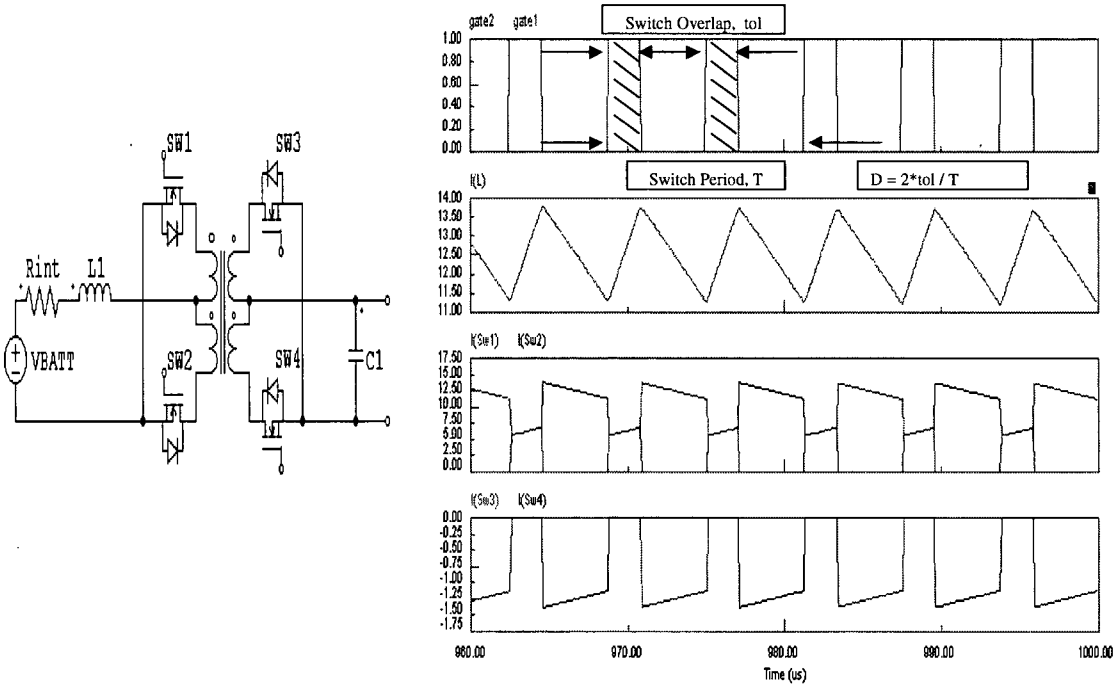


Figure 9: **Clarke converter forward (battery discharge) operation waveforms**

To operate the Clarke converter in reverse mode, Sw3 and Sw4 must be actively switched while Sw1 and Sw2 act as rectifiers. For reverse operation is critical that Sw3 and Sw4 do not overlap. Overlapping Sw3 and Sw4 creates a short circuit across the dc bus and will result in destructive fault currents. The duty cycle, D, is now defined as the two times the switch off time of Sw3 or Sw4 as a percentage of the switching period. The reverse operation of the converter also has three switching states as described in table 4.

	Action
Sw3 & Sw4 open (1)	Current in the inductor, L, ramps up from a negative value to a less negative value.
Sw3 closed, Sw4 open (2)	Current in 'pushed' through the transformer and the inductor current ramps down to a larger negative value.
Sw3 & Sw4 open (1)	Current in the inductor, L, ramps up from a negative value to a less negative value.
Sw3 open, Sw4 closed (3)	Current in 'pushed' through the transformer and the inductor current ramps down to a larger negative value.

Table 4: Clarke converter reverse (battery charge) switch pattern

Assuming continuous negative inductor current, when Sw3 and Sw4 are both open the low voltage side inductance provides the battery with a negative current ramping up, again, according to (2.1.1). When either Sw3 or Sw4 is closed the current ramps down in the inductor, again according to (2.1.2),. and the voltage conversion can be described, again as a function of duty cycle, D, by (2.1.3)

$$V_{BUS}(D) = \frac{V_{BAT} \cdot N}{1 - D} \qquad (2.1.3)$$

The duality between the two converter directions is now apparent. The converter current waveforms are the same for either direction of operation with the only difference being direction. If the converter is transferring a specific power at a specific voltage

conversion ratio, the switches experience the same magnitudes of current independent of the direction of operation. The confirming PSIM generated waveforms for the reverse direction are presented in figure 10.

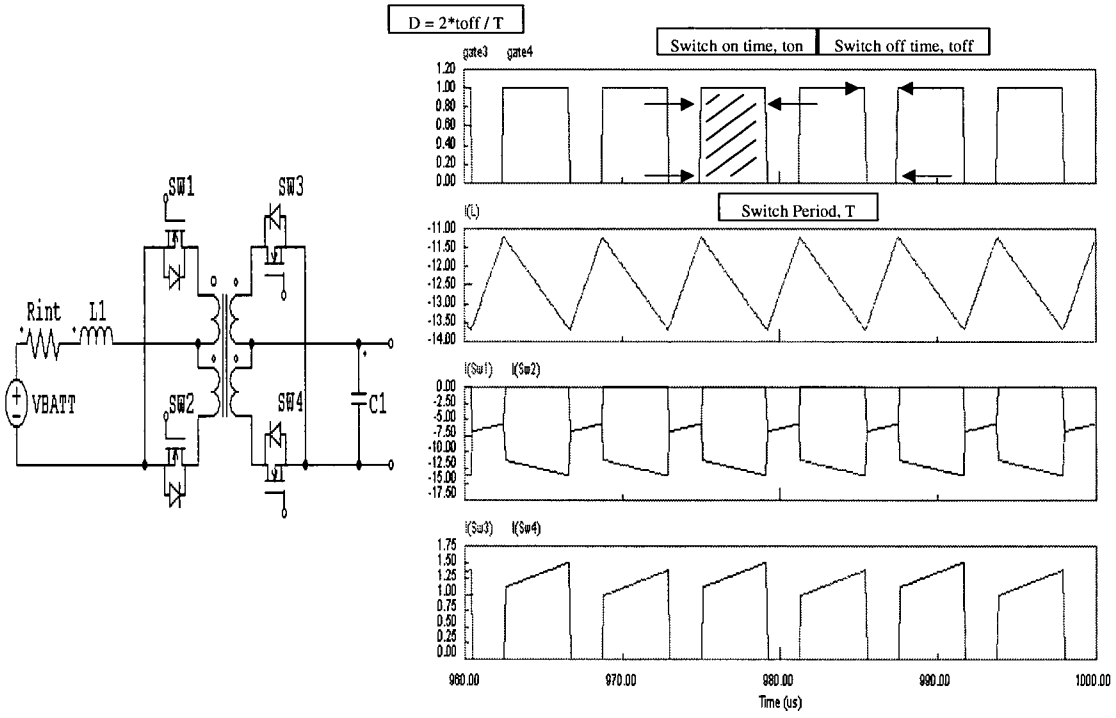


Figure 10: Clarke converter reverse (battery charge) operation waveforms

The Clarke converter as presented in figure 8 can satisfy the electrical specification of appendix A, requires a minimum of components as compared to [1] utilizes the transformer materials efficiently and can share the components to function in both directions. Although not particularly novel in its own right, the Clarke topology qualifies as a suitable power circuit foundation upon which this thesis is evolved. In the next section of this thesis four active switch devices are implemented within the Clarke converter to achieve a more efficient bi-directional synchronously rectified converter.

2.2 Switch power dissipation and synchronous rectification analysis

As mentioned in the prior section, synchronous rectification can be achieved within the Clarke converter by using four appropriately gated switching devices. While the elimination of discontinuous inductor current mode advantage due to the allowance of seamless power flow maybe intuitively clear, there are also inherent efficiency gains resulting from synchronous rectification. In this section the Clarke converter switch currents are discussed and the theoretical efficiency gains of synchronous rectification are analyzed and determined using a MATLAB model. The overall goal is to model the losses as a function of duty-cycle, in either direction, and compare between synchronous rectification and non-synchronous rectification modes of operation. The somewhat non-intuitive optimal transformer turns ratio is also determined as part of the process.

Referencing the balanced waveforms and duality conclusion from the previous section the following can be observed:

ISw1(rms) = ISw2(rms) for forward or reverse operation
ISw3(rms) = ISw4(rms) for forward or reverse operation
ISw1(ave) = ISw2(ave) for forward or reverse operation
ISw3(ave) = ISw4(ave) for forward or reverse operation

Table 5: Symmetrical switch currents

To simplify the analysis the following assumptions applicable to the thesis converter are made:

1) Assume constant, ripple free current in the inductor
2) Assume FET Rds_{on} = .008 ohm for Sw1 & Sw2 (IRF3205, 110A, 55V)
   Assume IGBT Vce_{on} = 2V for Sw3 & Sw4 (12N60B3D, 27A 600V)
3) For non synchronous rectification assume device body diode drop of 1V
4) For synchronous rectification assume forward ISw*Rds_{on}, or 1V for the reverse direction, whichever is less.
5) Actual hard switching transitional losses neglected
6) Assume worst case bus voltage of 250V

The following equations can be used to calculate switch power dissipation:

$$Pswitch = Irms^2 \cdot Rdson \tag{2.2.1}$$

where (2.2.1) is for active FET switches and synchronously rectifying FET switches where ISw*Rds_{on} is less than the 1V forward biased body diode drop.

$$Pswitch = Iave \cdot Vf \tag{2.2.2}$$

(2.2.2) is used for non gated rectifying switches where Vf is the 1V diode forward voltage drop. (2.2.2) is also for synchronously rectified devices and active IGBTs where Vf is less than Isw*Rds_{on} or Vce and (2.2.2b) is used forward active IGBT devices.

$$Pswitch = Iave \cdot Vce \tag{2.2.2b}$$

It is also necessary to limit the low side switch stress voltage to less than 50V to allow for practical usage of an efficient low Rds_{on}, high current FET. This immediately puts a constraint on the transformer turns ratio. The low side switches experience a stress voltage of:

$$Vsw1, sw2pk = \frac{(V_{BUS}) \cdot 2}{N} \tag{2.2.3}$$

$$N = \frac{V_{BUS} \cdot (1 - D)}{V_{BAT}}$$

where N is the transformer turns ratio given D (2.2.4)

when they are in the off state. To limit this voltage to 50V for a worst case bus voltage of 250V the turns ratio has to be greater than or equal to 10. Still, it is not intuitively clear exactly how much greater than 10, if any, the turns ratio must be to insure optimal

efficiency. To investigate this MATLAB code (Appendix C) was written to calculate the switch power losses and required turns ratio over a range of duty cycles to determine optimal efficiency turns ratio. Figure 11 shows the switch currents and equations. Figure 12 displays the resultant plots of both switch power loss and turns ratio as a function of switch duty cycle for four modes of operation: discharge, charge, synchronous rectification discharge and synchronous rectification charge. In the synchronous rectification modes the switches are gated at the times when they would ordinarily be forward biased diodes. This fundamentally avoids any extra power loss associated with the forward voltage drop of the diode and replaces it with the $I*Rds_{on}$ or V_{ce} voltage drop if it is less than the forward diode drop. Results are summarized in table 6.

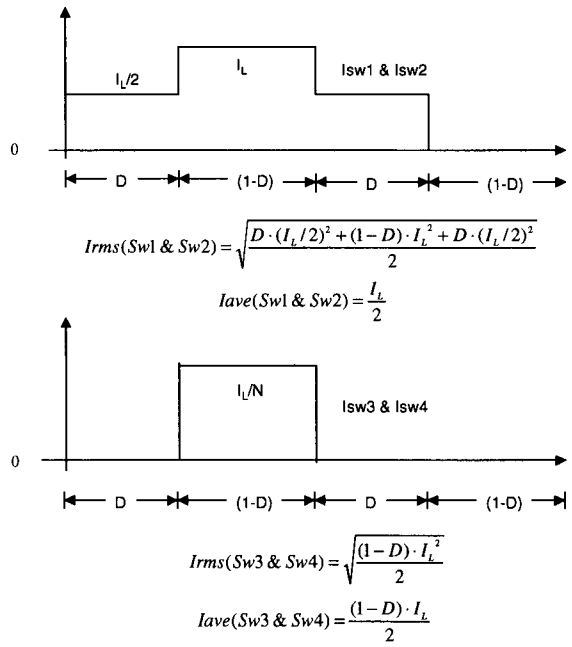


Figure 11: Switch currents equations

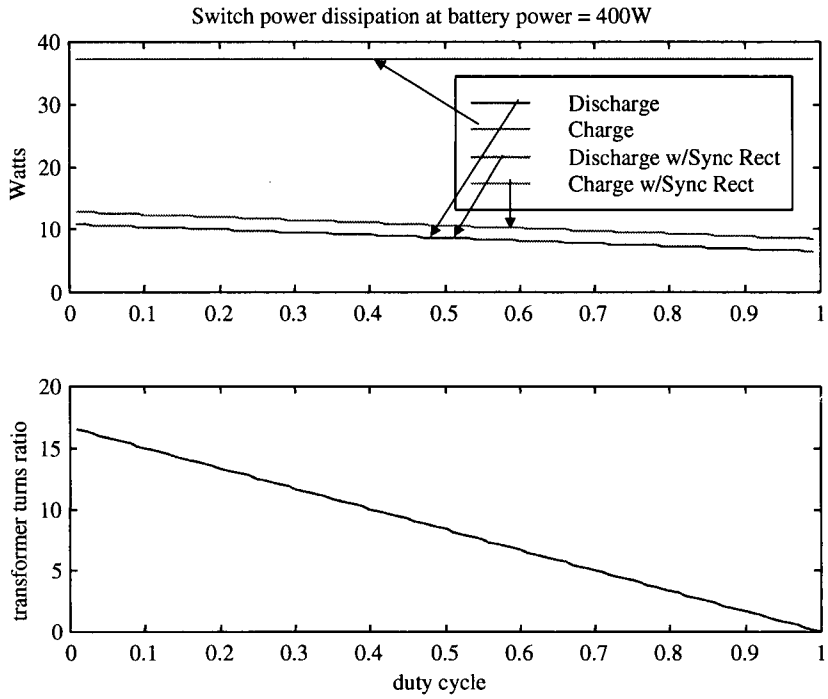


Figure 12: **Switch power dissipation and required transformer turns ratio as a function of duty cycle. Voltage conversion fixed at 12V:200V**

400W Battery Power Transfer Voltage conversion ratio = 12V:200V	Switch Loss @ N=10 & D=0.4	Efficiency @ N=10 & D =0 .4
Discharge (forward)	9.1 W	97.7%
Charge (reverse)	37.3 W	91.5%
Discharge with synchronous rectification	9.1 W	97.7%
Charge with synchronous rectification	11.1 W	97.3%

Table 6: **Theoretical switch conduction losses**

Figure 12 shows that as the transformer turns ratio increases the system efficiency decreases. For this reason and also because it is attractive to maintain as much adjustable dynamic range in the duty cycle as possible, it is beneficial to choose the turns ratio as the

minimum 10. The resulting duty-cycle with which to perform the baseline efficiency comparison is therefore 0.4 and the appropriate results are summarized in table 6.

The proposed Clarke current fed converter has a high switch conduction loss in charge mode due to the large rectifier currents coupled with the 1V rectifier voltage drop. The 37.3W conduction loss can be reduced by over 70% to 11.1W by implementing synchronous rectification while charging. The addition of synchronous rectification while discharging results in no improvement of switch conduction losses. Charger efficiency may not appear critically important as the plentiful ac mains (grid power) is usually used as the source rather than a finite energy battery. However, by reducing the converter's heat dissipation while charging to a power level similar to that of inverting (discharge), additional packaging and cooling costs can be avoided and physical size minimized.

Due to the duality between the two directions of power flow there is also no difference between the switching pattern required bi-directional synchronous rectification. This means that when the switch devices are synchronously rectified, the switching pattern does not have to change according to the converter direction of operation. When synchronously rectified the duty cycle effectively fixes the converter's voltage conversion ratio. Power flow through the converter is determined by where the source and load appear and is independent of the switching pattern. If a load is on the bus power will flow from the battery, onto the bus and into the load. If the bus voltage is increased power will flow seamlessly backwards from the bus into the battery without having to adjust switching pattern. In this way the synchronous rectification also eliminates the complications of non-continuous inductor current as the inductor is free, at all times, to operate with negative or positive current.

It is concluded that implementing synchronous rectification benefits two significant areas: 1) heat generation due to switch conduction losses and 2) simplification of switch control allowing for seamless bi-directional power flow. Additionally, the hardware costs incurred with a move to synchronous rectification are, in theory, zero since all four switches must already be actively controlled. For these reasons it is also concluded that the new, synchronously rectified *Clarke* converter circuit is to be further developed as the power-circuit topology for the thesis converter application.

2.3 Component specification and design

To build a working model of the power circuit the key power components need to be specified. The key components of the proposed thesis converter consist of the four power switch devices, the *Clarke* inductor, dc bus capacitor and a four winding high frequency transformer. The magnetic components are both specified and designed as it is common to custom wind the inductor and transformers for each individual application.

2.3.1 Power switch devices

In today's era of semi-conducting power switch technology the two candidate switch types are the field effect transistor (FET) and the insulated gate bipolar transistor (IGBT). The original bipolar power switch transistors of the '70s were base current controlled devices characterized with relatively slow switch on and switch off times. Today's FET and IGBT are voltage controlled devices with improved dynamic response and in many cases integrated reverse body or *anti- parallel* diodes .

Field effect transistors are a *Gate Drain Source* device characterized by having a fixed on resistance characteristic, Rds_{on}, which tends to increase as the voltage blocking rating of the switch increases. To minimize heating effects, it is advantageous to specify FET(s) devices with as low Rds_{on} as possible. FETs can also be effectively paralleled due to their positive Rds_{on} temperature coefficient. Insulated gate bipolar transistors are a *Gate Collector Emitter* device characterized by having a consistent Vce_{on} voltage drop typically around 1.5 volts. Generally FETs are clearly suitable for lower voltage applications of less than 50 volts where the low Rds_{on} yields high efficiency. Conversely, IGBTs are generally suitable for higher voltage applications where the Vce_{on} voltage drop of the device is fixed. For applications above 600V the power dissipated by an IGBT will usually be less that that of a FET with similar voltage and current ratings. This leaves a gray area between 50V and 600V where either a FET or an IGBT device could be effectively utilized. Of the four switch devices required for the thesis converter, two can be considered low side devices and two can be considered high side devices. The low side devices, Sw1 and Sw2, will clearly require a FET device while the high side devices, Sw3 and Sw4 may be FET or IGBT based.

With the transformer turns ratio set at 10 and a maximum dc Bus voltage of 250V, Sw1 and Sw2 will be faced with a maximum blocking voltage of 50V each. Taking into consideration transient currents and the actual lower RMS value of the switch current relative to the battery current, it is safe to specify a device with a continuous current rating in the 100A range. The selected IRF3205 MOSFET, found in Appendix G, is a 55V device rated for a maximum continuous current of 110A @ 25C and a pulsed drain current of 390A. Rds_{on} is a low 8mΩ and the body diode has a maximum reverse recovery time of 100ns. This is a low-cost common part with alternative suppliers producing similar components.

Sw3 and Sw4 may experience normal operational blocking voltages of 500V, average currents up to 2A and regular pulsed currents of up to 8A. To this end two high side components are specified, both a FET and an IGBT. The IRF840 MOSFET, found in Appendix H, is a 500V device rated for a maximum continuous current of 8A @ 25C and a pulsed drain current of 32A. Rds_{on} is a significant 850mΩ and the body diode has a significant maximum reverse recovery time of 900ns. This FET is also a common part with alternative suppliers. The selected 12N60B3D IGBT, found in Appendix I, is a 600V device with a continuous collector current of 27A and a pulsed collector current of 110A. The Vce_{on} is typically 1.6V and the fast anti-parallel diode's maximum recovery time is a maximum of 40ns. The two devices are identical packages and similar in price and in static losses and at this point it appears that possibly either could be utilized. In a later section the operational performance of the two devices are compared and it is concluded that the IGBT is superior for the thesis converter application due to its much faster reverse body diode operation and lower switching losses.

2.3.2 Clarke inductor

In addition to functioning as the main magnetic energy storage component of the converter, the Clarke inductor is responsible for smoothing out the current flowing both to and from the battery. From a theoretical point of view it is attractive to make the energy storing inductance as large as possible. A larger inductance reduces current ripple, reduces edge of continuous inductor current mode and reduces RMS switch currents. Unfortunately as inductance increases both cost and physical size also increase. To minimize costs, the Clarke inductor in the project dc/dc converter must be designed as small as possible while still satisfying the project's electrical specification of Appendix A. Using the worst case battery voltage and the maximum allowable peak to peak battery current from the electrical specification, the minimum inductance can be calculated according to (2.3.1).

$$L(\min) = \frac{Vbat \cdot dt}{di(\max)} = 19uH$$

where di(max) = 4A, Vbat = 10V and dt = 7.6uS

(2.3.1)

A value of 20uH is chosen instead to help compensate for the fact that the inductance will decrease slightly as the dc current increases, especially when the core usage is maximized. The inductor must also function with an average dc current of 40A at full load. Due to potential sinusoidal loading of the dc/dc converter by a dc/ac converter the inductor current may actually experiences a 120Hz ripple with a maximum current of 80A. A 20uH inductor that can function without becoming overly saturated at 80A is required for use as the thesis converter's Clarke inductor.

The maximum energy stored in the core is described by (2.3.2) and occurs when the inductor current is 80A:

$$J = \frac{1}{2} \cdot L \cdot I^2 = 64mJ$$

(2.3.2)

The inductor core must be able to store 64mJ of energy without significant saturation.

Using the core selector chart in Magnetics Corporation's Kool Mu Powered Core Catalog it can be determined that the A-7-77259 core is of sufficient characteristics to support the 64mJ energy requirements. The core selector chart quickly yields optimum permeability and smallest core size for a given dc bias current. The A-7-77259 core features a permeability of $75u_o$ and an inductance, Al, of 101mH/1000 turns. The number of turns required to form a 20μH inductor is determined by (2.3.3) where Ln = 0.020mH and Al = 101.

$$Nturns = \sqrt{\frac{Ln(mH)\cdot 10^6}{Al}} = 15 \qquad (2.3.3)$$

The core selector chart used above allows for a permeability reduction of no more than 50% at maximum dc bias. This means that at 80A the inductance will be no less than 10μH. The exact inductance value at 80A can be calculated by first calculating the magnetic field intensity as in (2.3.4).

$$H = \frac{N \cdot I}{\lambda_e} = 122000 AT/m$$

where *le* is the magnetic path length = .0984 m

(2.3.4)

According to Magnetics Corporation's Permeability –vs- dc Bias curves, a dc magnetizing force of 122000 AT/m and an initial core permeability of $75\mu_o$, results in a reduced permeability to approximately $37\mu_o$. The reduced inductance can now be calculated by (2.3.5)

$$L = \frac{u_o \cdot u_r \cdot N^2 \cdot A_e}{\lambda_e} = 10.7 uH$$

where
L = inductance
μ_o= permeability of space = 4π*10-7
μ_r = reduced core permeability = 35
N = Number of Turns = 15
A_e = core cross section (cm^2) = .0001072 m^2
l_e = core magnetic path length (m) = .0984 m

(2.3.5)

When winding high frequency inductors and transformers it is beneficial to use many strands of a thinner wire rather than a single thick wire of equivalent resistance for two main reasons. The first and predominant reason is because of the skin effect associated with high frequency operation. During high frequency operation many strands of thinner wire have a larger effective cross sectional area as compared to a solid conductor of equivalent area. The second reason for using stranded wire is because it is physically easier to manipulate when winding the inductor or transformer. The project Clarke inductor features 15 turns of twenty strands of 0.5mm diameter wire resulting in a total cross sectional area of $40*10^{-3}$ cm^2 and a total resistance of 1.1 mΩ. This corresponds to copper losses of approximately two watts at 40A RMS.

2.3.3 High frequency transformer

The objective of the transformer design process is to realize a combination of transformer core and conductive winding material that results in maximum power conversion performance while minimizing both cost and volume.

The area product method is an effective tool for transformer design. The area product is determined by multiplying the required transformer core area (A_c) by the required winding window area (A_w). Note (2.3.6) is void of terms that are core dependent, eg. number of turns, and can be used to determine an appropriate fit core.

$$Ap = \frac{Vpri \cdot tpri \cdot Ipri \cdot (1+x)}{Bm \cdot Kw \cdot J} \qquad (2.3.6)$$

where (including project converter values):
Ap = area product = 1.5 cm^4
Vpri = maximum normal primary voltage = 20V
tpri = maximum elapsed time primary voltage is applied = 9μs
Ipri = maximum primary current = 40A
x = area occupied by sec / area occupied by pri = 1
Bm = maximum flux density swing = 500 mT (conservative)
Kw = winding fill factor = 0.25 (conservative)
J = maximum allowable current density = 5A/mm^2

The transformer core selected must at a minimum satisfy the Ap requirement to ensure a combination of enough effective core and window areas. Samwha Corporation's EI4035S ferrite core features an A_c of 122 mm^2, an A_w of 166 mm^2 and a resulting A_p of 2.44 cm^4. Although the chosen core exceeds the A_p requirement by almost a factor of two, it is readily available, low cost. and is therefore selected as the thesis converter's core.

The next consideration is the number of turns required on the primary of the transformer.

$$Npri = \frac{Vpri \cdot tpri}{Bm \cdot Ac} = 1.25 \qquad (2.3.7)$$

use Npri = 2 and flux density swing is reduced to an acceptable 318mT

$$Bm = \frac{Vpri \cdot tpri}{Npri \cdot Ac} = 318mT$$

(2.3.8)

Using 2 turns on the primary requires 20 turns on the secondary to achieve the 1:10 turns ratio.

The required primary winding current density of 5A/mm^2 can be achieved by using 6 wires each of 0.9 mm diameter.

$$J = \frac{.5 \cdot I}{N \cdot (D/2)^2 \cdot \pi} = 5.2A/mm^2$$

(2.3.9)

where:
J = current density
I = 40 A
N = 6
D = 0.9 mm
.5 = duty cycle for each primary winding

The diameter in millimeters required for the secondary windings to achieve the same current density is calculated in eq. 2.3.10:

$$D = \sqrt{\frac{I}{\pi \cdot J \cdot .5}} = 0.7$$

(2.3.10)

where:

I = maximum secondary current = 4 A
J = maximum current density = 5 A
0.5 = duty cycle for each secondary winding

The four winding transformer is created by using two primary and two secondary windings of the above specification wound in a bifilar fashion to minimize leakage inductance.

2.3.4 DC bus capacitor

In principle the dc bus capacitance determines the output voltage ripple appearing on the dc bus. A larger capacitance reduces voltage ripple but also slows system control response to a change in output voltage. A smaller capacitance increases ripple but also allows for faster system response. For the thesis converter application maximizing control response is of more interest rather than minimizing bus voltage ripple. To this end, the maximum acceptable bus voltage ripple specified for the thesis converter application is 2% pk-pk or 4V pk-pk at 200V. A simplified approach to sizing the capacitor is as follows.

The worst case load current occours when the inverter is at the peak of its sinusoidal current for a 400WRMS load. At this point the Vdc bus is 200V and the load current is 4A. Assuming a low end duty cycle of 0.33, the current into the capacitor will be 2A when the current is injected from the secondary (*Sw3* or *Sw4* conducting) and -4A when supplying the bus load alone or 2.8A RMS. Since the switching frequency and duty cycle are known, it is possible to determine the minimum capacitor required to acheive the maximum specified pk-pk voltage ripple according to equation (1.5.11).

$$C = \cdot \frac{IL * DC}{Vpp \cdot fs \cdot (1 - DC)} \qquad (1.5.11)$$

where DC = the duty cycle (0.33)
Vpp = the peak to peak voltage ripple (4 V)
fs = effective switching frequency (80KHz)
IL = the dc load current (4 A)

The minimum capacitance calculates to be 6.15μF.

Traditionally, the dc bus capacitor will be of the electrolytic type, however, for the case of the thesis converter a small 6.8μF 350V electrolytic capacitor rated for approximately 2.8A RMS ripple current is simply not produced. In practice capacitors have a dissipative equivalent series resistance (ESR). The ESR of an electrolytic capacitor in the above voltage and capacitence specification is in the region of ohms. This creates power disupation problems and also has the effect of increasing the actual voltage ripple due to the ESR voltage drop. In design practice the electrolytic dc bus

capacitance is usually increased until a suitable low cost and high energy density electrolytic capacitor(s) can be specified.

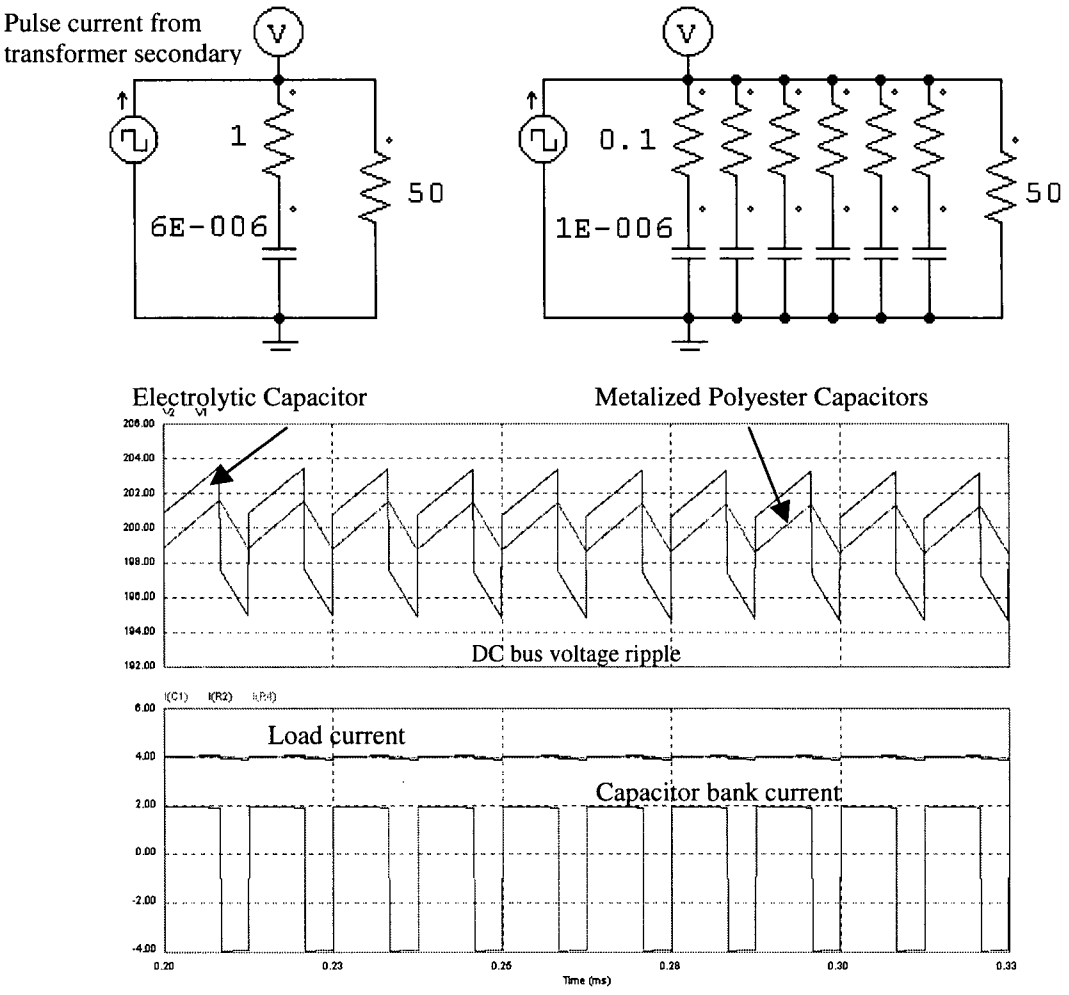


Figure 13: Voltage ripple –vs- capacitor technology

In the case of the thesis converter the goal is to minimize the bus capacatence to increase control bandwidth. An alternative capacitor technology proposed to accomplish this is the metalized polyester capacitor. A common 1μF 400V metalized polyester capacitor has a power dissipation factor of less than 1% at 20KHz. This means the ESR of the capacitor is less than $1/100^{th}$ of the capacitors reactance at 20Kz. For the 1μF capacitor the frequency dependent ESR can be considered a nominal 0.1 Ohms. Six 1μF

capacitors can be used in paralled to create the approximately required 6μF. Figure 13 compares the waveforms of the 6uF electrolytic capacitor with an ESR of 1 Ohm to six 1μF polyester capacitors in parallel, each with an ESR modeled as 0.1 Ohm. The waveforms are generated by PSIM and represent the thesis converter at the 800W full load.

Figure 13 shows the increased voltage ripple resulting from the electrolytic capacitor and accompanying ESR. More significantly, the power dissipation of the electrolytic capacitor is $2.8A^2$*1 Ohm or 7.8 Watts (well out of its design range). The power dissipation of the parallel polyester capacitors is $0.47A^2$*0.1*6 or a reasonable 1/8W total. Moreover, the ESR of six metalized polyester capacitors does not significantly increase the output voltage ripple. This extra proformance does however come at a cost. The six metalized poylester capacitors cost appriximately five times more than the same value of the unsuitable electrolytic capacitor.

It is concluded that six 1μF metalized polyester capacitors in parallel are suitable choice. The polyester units, traditionally used as line filter capacitors, selected for use as the dc bus storage capacitance for the Thesis converter application.

2.4 PWM signal generation from a TMS320F243 DSP controller

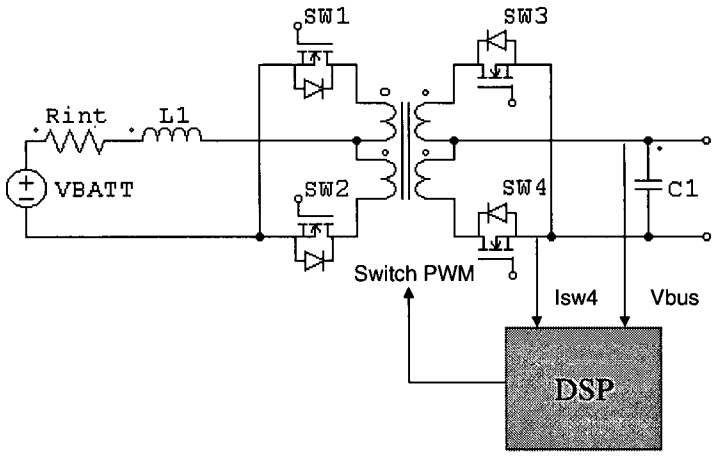


Figure 14: DSP Derived PWM Switch Gating

The intention of this section is to solve the problem of obtaining the required PWM switch gating signals for the bi-directional Clarke converter from the DSP controller. It was originally thought that an onboard adjustable dead time feature could be used to for precicely compensate switch timing for opto-isolator propogation delays. This proved to be false. Within this section the technical limitations of the DSP derived PWM for the thesis dc/dc converter applicaion are considered.

The Texas Instruments TMS320F243 DSP controller used within the thesis dc/dc converter is one of today's new breed of DSP controllers designed specifically for three phase motor control. These controllers inherently feature on board peripheral PWM generation, high computational speed and on board analog to digital sampling circuitry. Today's new range of PWM equipped motor controller DSPs all feature at least six PWM outputs, one for each device of a three phase ac inverter bridge. However, for the six PWM outputs there are usually only three independent hardware comparators where each comparator governs the operation of a pair of PWM outputs. Within each pair of outputs

one will be a high side bridge device and the other will be a low side device – each device operating inversely with respect to the other. Most motor control DSPs will also feature some sort of programmable dead time parameter where both switches in the pair are held off for certain period of time. This prevents current shooting through both bridge devices during the transition time when one device is switching off and the other is switching on.

In keeping with the above explanation, there are only three completely independent PWM outputs within the six advertised PWM channels on the TI TMS320F243 DSP. This is a significant point when using the PWM channels for purposes other than three phase motor control. Such an example is within the thesis dc/dc converter itself. The TMS320F243 DSP used in the thesis converter utilizes three dedicated hardware based PWM comparators to create six PWM outputs as discussed above. In addition to these, two more independent PWM outputs can be generated using two more on onboard hardware comparitors. This results in a total of five independent high speed, peripheral hardware derived, PWM signals available for use. Of course more PWM signals can be obtained using standard I/O pins and software algorithms but this may come at a significant expense of processor time and hardware resourses since they are not perhipherally located. A summary of the PWM outputs available on the TMS320C243 DSP is found in table 7. A description of the timer, compare operation and PWM output generation is described in figure 15.

PWM(x)	DSP timer used	Comments
PWW(1 and 2)	must use GP1 timer/counter	PWM 1 and 2 use a common compare match value to set duty cycle
PWM (3 and 4)	must use GP1 timer/counter	PWM 3 and 4 use a common compare match value to set duty cycle
PWM (5 and 6)	must use GP1 timer/counter	PWM 3 and 4 use a common compare match value to set duty cycle
PWM 7	must use GP1 timer/counter	PWM 7 uses independent compare match to set duty cycle
PWM 8	must use GP2 timer/counter	PWM 8 uses independent compare match and can feature a different switch period than the previous 7

Table 7: PWM Outputs on the TMS320F243 DSP

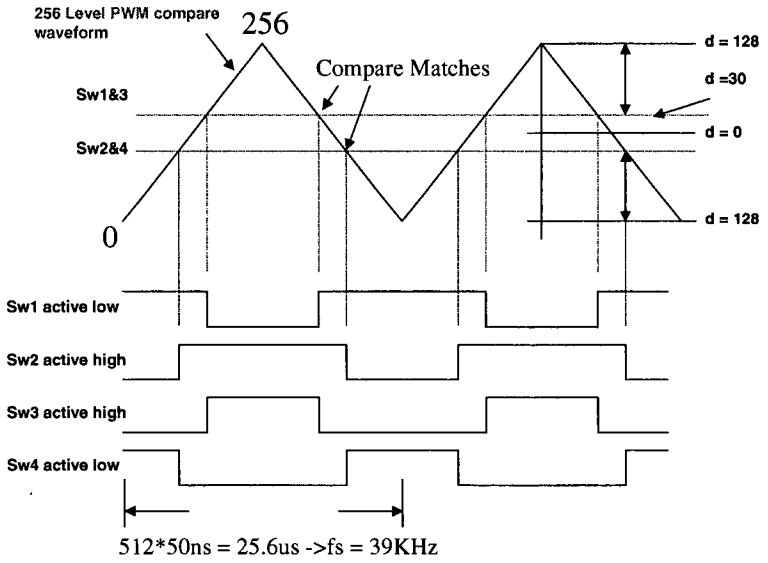


Figure 15: PWM Generation for the bi-directional Clarke Converter.

Figure 15 demonstrates how the Clarke converter switching pattern is generated from the DSP's PWM outputs using only two of the five independent PWM comparators. The key to the PWM generation is the *x* level count up count down *compare* waveform. For the Texas Instruments F243 DSP utilized the *compare* waveform is generated by general purpose timer/counter 1 (GP1 in Table 6) set to count up/down mode with a period set to *x*. This creates the approximately 39kHz triangular *compare* waveform presented in figure 15 given the 50ns timer increment of the 20MIPS processor. By setting the PWM compare matches to the appropriate number within the integer range 0 to *x* and by setting the appropriate outputs to *active high* or *active low* the resulting PWM signals of figure 15 are achieved. In figure 20 $PWM_{1,2}$ map to Sw1,3 where PWM1 is configured *active low,* or on, when the compare waveform is less than the $PWM_{1,2}$ compare match value. Conversely, PWM2 is configured *active high,* or on, when the compare waveform value is above the compare match value. Independently, $PWM_{3,4}$ map to Sw2,4 where in this case PWM3 is configured *active high* and PWM4 is configured *active low*. In this way the required synchronously rectified Clarke switching pattern is generated using only two of the five PWM compares. The duty cycle, *D*, of the

waveform can be controlled by the value of the compare matches according to (2.4.1) where x represents the levels of the compare waveform.

$$D = \frac{2d}{x}$$

$$d = PWMCompareMatch_1 - x/2 = -(PWMCompareMatch_2 - x/2) \quad (2.4.1)$$

Adjusting the duty cycle within the DSP results in an unavoidable quantization effect. This is because the PWM_compare_matches and x have to be fixed point integer values. The number of quantized duty cycle steps, DQ, between 0 and 1 is a function of the required switching frequency, *fs*, and the CPU clock speed of the processor, *fcpu*. This relationship can be expressed by (2.4.2) where *fs* must be chosen to result in an integer *DQ*.

$$DQ = \frac{fcpu}{4 \cdot fs} = \frac{x}{2} \quad (2.4.2)$$

The TMS320F243 DSP used is a 20MIPS (million instructions per second) device meaning *fcpu* is 20MHz. Figure 19 demonstrates that for a switching frequency of ~39Khz a DQ of 128 steps is obtained. This switching frequency is chosen for the thesis converter to match the current technology utilized within the Xantrex RVSINE400 inverter.

In reality, the two low voltage switches, Sw1 and Sw2, of the thesis converter must be driven via a combination opto-coupler/FET driver circuit in order to maintain the galvanic electrical isolation between the low voltage and high voltage sides of the converter. This opto-coupler/driver stage introduces a significant propagation delay, *tp* (possibly 500ns), from the time the DSP signals the switch until the time the switch responds. The high voltage switches, Sw3 and Sw4, are not subject to this opto-coupler propagation delay. If the PWM signals of figure 15 are applied directly to the power-circuit through the low side opto-couplers the results would be catastrophic. Current shoot-through due to switch overlap would cause certain switch failure. With the synchronously rectified approach the precise timing of the switch pulses are extremely important. It is therefore necessary to retard switch pulses appearing at Sw3 and Sw4 by *tp* as seen in figure 16. Originally it was thought that by adjusting the appropriate internal

PWM *dead time* setting of the DSP, the two high side gating signals, Sw3 and Sw4, could be retarded by *tp* or, alternatively, Sw1 and Sw2 could be advanced by *tp*. It is possible to achieve this but it requires the use of four of the five independent *PWM comparators* and additional compare set point calculations to create, in effect, four independent PWM waveforms. This is not a viable option as the other three *PWM compares* must be reserved for the dc/ac inverter section of the complete inverter/charger device. The technical details of the dead band generation can found in [37] beginning on page 2-55.

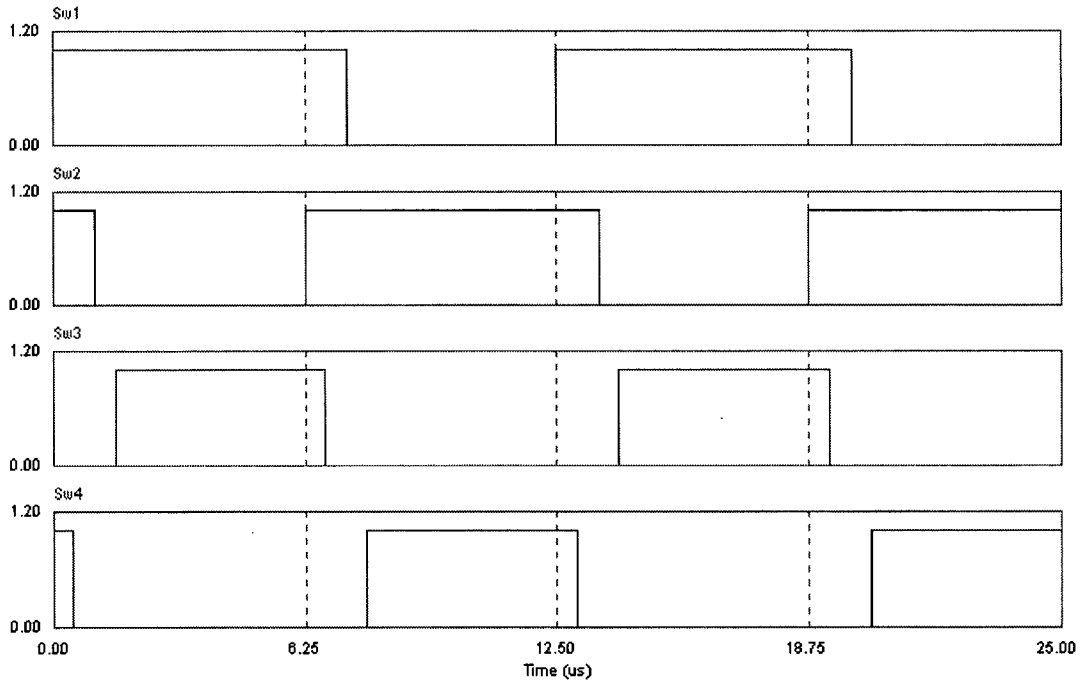


Figure 16: Adjusted switch timing required

A simpler solution is to delay the gating signals to Sw3 and Sw4 by *tp* by a means external to the DSP. This method satisfies the requirement of using only two *PWM comparators* while keeping the other three free. It should be noted that with the implementation of the four comparator PWM, switch timings can independently controlled in 50ns increments and precisely adjusted in software for possibly more efficient converter operation.

Separate from the larger scale timing issue of the opto-isolator delay is the need for some small actual dead time where Sw1,3 and Sw2,4 are both held off for a period of time during their state transition. This 'off time' is required to prevent switch overlap and current shoot through during the finite time required for the switches to turn on and off.

One would intuitively suspect that the *dead time* feature on the DSP could be utilized to achieve this goal. This is, in fact, literally only one half true. With PWM1 active high and PWM2 active low the addition of a dead band time via the dead band control register creates the desired effect. However, with PWM3 active low and PWM4 active high, as required, the addition of dead band time actually has the counter effect of overlapping the switches. This is because PWM_{odd} must be configured active high and PWM_{even} must be configured active low to create the required *dead time* where both outputs are low or zero. With the switching pattern required for the Clarke converter this is simply not achievable. Again, it would be possible to achieve full software switch timing control if four independent PWM compares were implemented. Using two PWM compares forces the use of a hardware compensation for both the opto-isolator propagation delay, *tp,* and the additional required transitional *dead time.* A hardware compensation solution is presented in section 2.4.

2.5 As built power-circuit

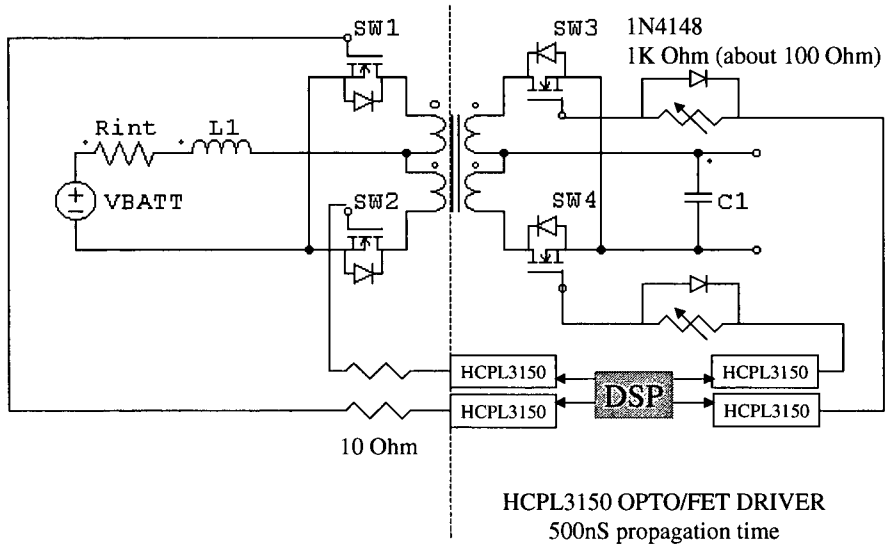


Figure 17: Switch Timing Strategy

Figure 17 shows the isolated drivers and the basic diode and resistor configuration used to prevent switch overlap and current shoot through. Sw1 and Sw2 require the use of the opto-isolator/driver to satisfy the fundamental isolation requirement. However, as mentioned in the previous section, the isolated driver introduces a *tp* of 500nS. To keep Sw3 and Sw4 synchronized the PWM signals are also propagated through two additional opto-isolator/drivers. This has the effect of synchronizing the switch signals as well as provides additional isolation and protection to the DSP. A variable resistance is used to increase the switch on time by slowing the gate charge to prevent switch overlap and catastrophic current shoot through. The diode is implemented to increase switch off time by quickly removing the gate charge thus creating an appropriate dead time between Sw1,2 and Sw3,4.

2.6 Measured Performance

This section presents and discusses the measured results from three tested variations of power-circuit. Initially the power circuit is tested in a discharge mode only with rectifier diodes implemented as Sw3 and Sw4. The purpose of this test is to produce a baseline result to which the synchronously rectified approaches can be compared. Next, IRF840 FET switches are installed as Sw3 and Sw4. They are synchronously rectified and their bi-directional performance is studied. Finally, 12N60B3D IGBTs are implemented as Sw3 and Sw4 and the bi-directional power flow is recorded and analyzed. In both the latter experiments the concept of the seamless bi-directional power flow is proven. It is concluded that the IGBT based power circuit produces superior results as compared to the FET based circuit.

2.6.1 Power circuit operation with MUR860 Diodes

As a first step to qualifying the power circuit MUR860 fast recovery rectifier diodes were implemented as Sw3 and Sw4. The DSP was used to gate the IRF3205 low side FETs and a 100Ω load was placed on the dc bus. The duty-cycle was fixed at 0.33 to create approximately 180V on the dc bus from a 12VDC source. Measured waveforms of this circuit are found in figure 18. Figure 18a shows the expected inductor current waveform as well as the drain source voltage across Sw1. Channel one of figure 18c shows the forward voltage across Sw3, the rectifier diode. A ringing voltage is present when both Sw1 and Sw2 are overlapped. The voltage is trying to settle at the dc bus voltage but the combination of transformer leakage inductance and snubber capacitance leads to this harmless initial transient response. Channel two of 18b shows the current though the naturally commutating diode. Figure 18c is actually a zoom of 18b with the inclusion of V_{gs1}. This plot shows in detail the recovery characteristic of the fast MUR860 diode. It is observed that the conducting diode takes about 50ns to return to 0A at which point the current proceeds to conduct past zero in the reverse direction as the reverse voltage of the diode also increases. The current takes another 50ns to return to zero again during which time the voltage is high. The instantaneous power dissipated by the diode is equal to its current multiplied by its voltage. During this 50ns of recovery

time the negative current and the voltage are both high and produce a large power dissipation. Fundamentally, the faster the recovery time the less power is dissipated. In switching power supplies where the diode has to recover often this power can dissipation can become very significant. The 50ns recovery time of the MUR860 diode in figure 18c is fast enough to not cause significant efficiency loss. While operating in this fashion the converter was measured to achieve a battery discharge efficiency of 93%. Of course with the rectifier diodes it is not possible to achieve power flow in the charge direction.

2.6.2 Power circuit operation with IRF840 FETs

After proving operation of the circuit with the MUR 860 rectifier diodes the next step was to implement the IRF840 FETs as the high side switching device. As an initial experiment the FETs were installed but not gated by the DSP. In this way they were simply to act as rectifiers. Figure 18a displays the measured result. The slow recovery time of the recovering diode is about 500ns. Also note the reduced supply voltage in the figure. The components would actually fail when subjected to the full 100Ω loading with a full supply voltage of 12V.

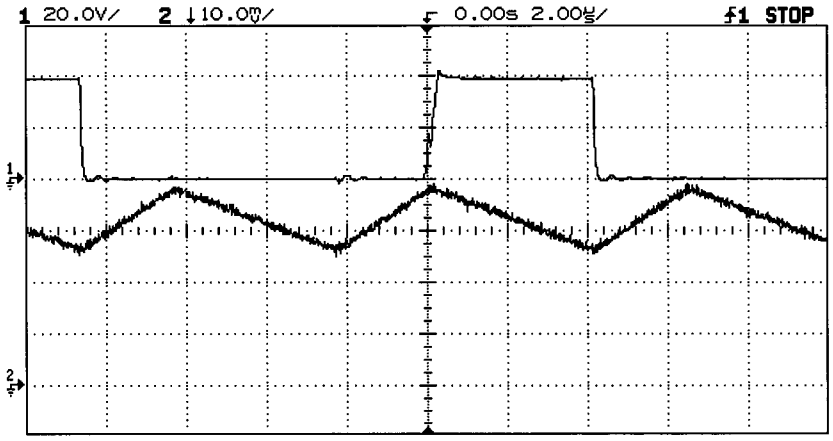
When synchronous rectification was initially applied the gate drive resistance was simply 100Ω, identical to the low voltage side. Unfortunately this resulted in current shoot though as indicated in figure 19b. The switch overlap and corresponding shoot through caused component failure at supply voltages above 2V. This result reinforced the need for some dead time between the low side and high side devices. To reduce switch overlap the high side gate drive resistance was raised to 400Ω to slow the switch turn on time. This prevented the high side switch from conducting while the low side switch was turning off. IN4148 diodes were next added in parallel to the increased resistance to remove the gate charge and turn the device off more quickly. The goal being to turn the high side device off faster than the low side device would turn on. This technique actually worked quite well. Figure 19c shows the successful synchronous rectification under load. The circuit was now free to conduct power in both directions - and it did. When the bus voltage was increased via an external power supply, power began to flow back into the battery. Efficiency in the discharge direction was measured to

be 88%. Efficiency in the charge direction was measured to be 83%. These results were encouraging but it was felt that some improvement was needed to approach the 93% benchmark set for the same circuit by the MUR860 diodes.

2.6.3 Power circuit operation with 12N60B3D IGBTs

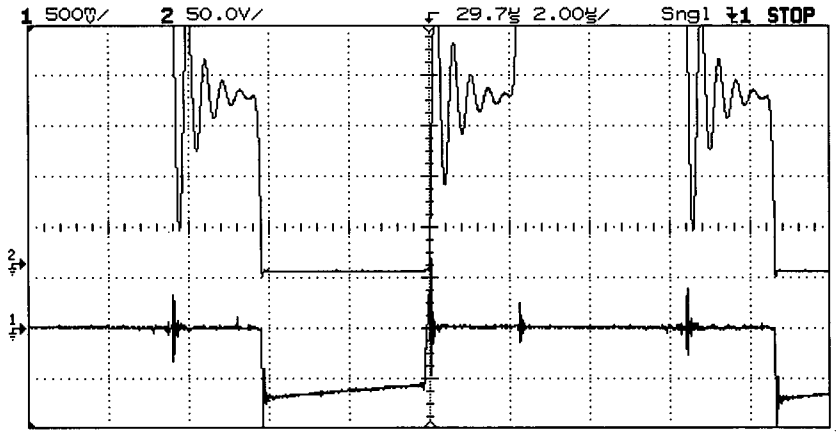
It was felt that the higher performance *anti-parallel* diode and low Vce_{on} drop of the IGBT may lead to more efficient circuit operation. This was confirmed when the IGBTs were installed and tested. Figure 20a shows ungated devices simply acting as rectifiers. The diode recovery time is fast and efficiency in this battery discharge mode was measured to be 91%. When the gating signals where applied and the devices synchronously rectified the efficiency fell by 2% to 89%. The largest gains were made when the bus voltage was increased and power flowed into the battery. Efficiency of 91% was measured in this charge mode - a significant increase from the 83% measured with the FET devices. Figure 21 shows in detail the switch timing of the IGBT devices. It can be seen with some accuracy that the effective switch on dead time is 50ns and the effective switch off dead time is 150ns. During testing the on time was adjusted and it was concluded that 50ns *on dead time* resulting from a 220Ω gate drive resistance was optimal. However, it was not possible to adjust the off dead time as the diode responsible for removing the gate charge remained fixed. It is not known if adjusting the off dead time could offer any increase in efficiency.

Figure 22 shows the bi-directional currents of the IGBT based converter. In figure 22a the dc bus is loaded, the battery is discharging and the inductor current is negative. In 22b the bus voltage has been raised to 212V, the inductor current is positive and the battery is being charged. Finally in 22c the dc bus in unloaded and the inductor current oscillates around zero. This figure epitomizes the true seamless bi-directional nature of the synchronously rectified circuit. Discontinuous inductor current mode is eliminated and power is flow in either direction. Additionally the charge pumping and uncontrolled voltage output voltage creeping effect of the unloaded boost converter is avoided.



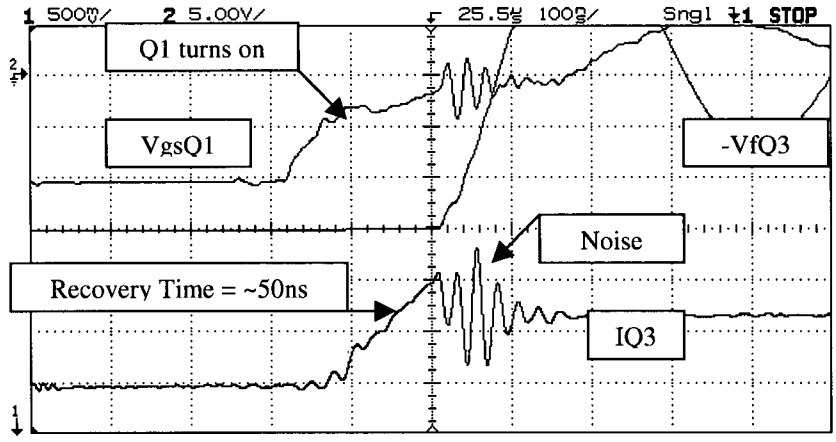
a) discharge operation with MUR860 fast recovery rectifier diodes

Ch1 = VdsQ1, Ch2 = Il(5A/div), Vin =12.0V, Iin = 25.1A, Vo = 166.7V, Io=1.64



b) discharge operation with MUR860 fast recovery rectifier diodes

Ch1 = VfQ3, Ch2 = -IQ3, Vin =12.0V, Iin = 30.8A, Vo = 166.7V



c) discharge operation with MUR860 fast recovery rectifier diodes

Diode recovery characteristics

Figure 18: Power circuit operation with MUR860 rectifier diodes

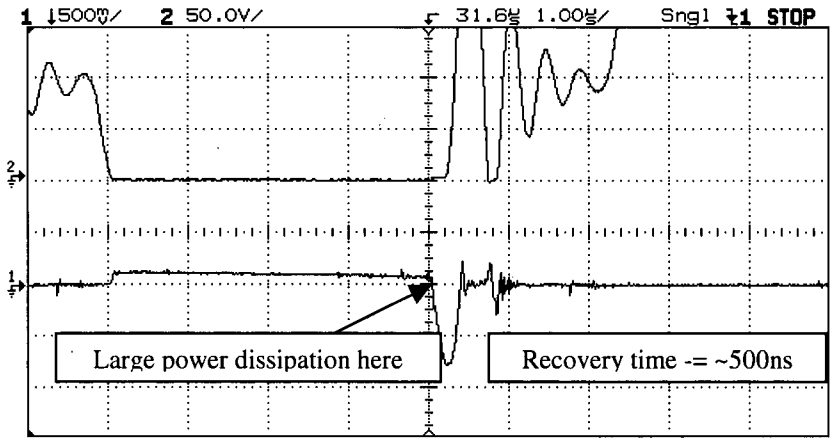
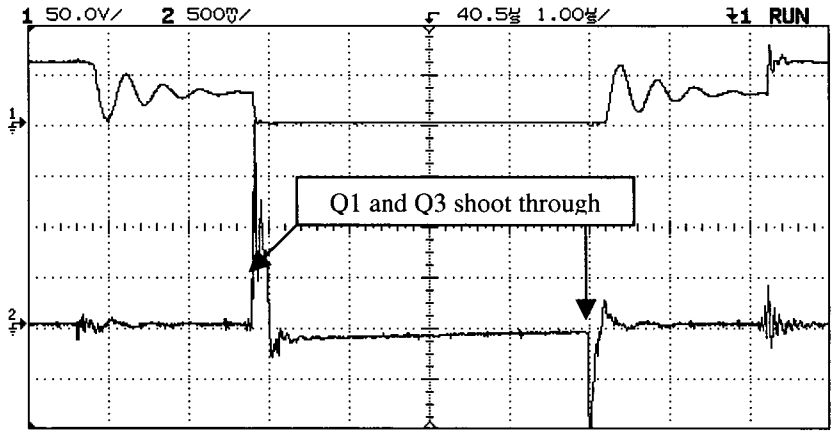


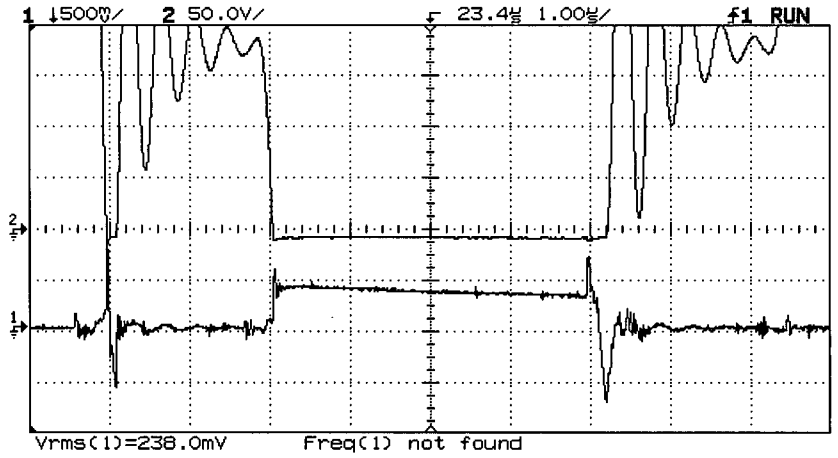
Figure a) discharge operation with IRF840 FETs. Not synchronously rectified.

Ch1 = -VdsQ3, Ch2 = IQ3, Vin =6.0V, Iin = 4.6A, Vo = 90.2, Io = .17A



b) discharge operation with IRF840 FETs. Synchronously Rectified

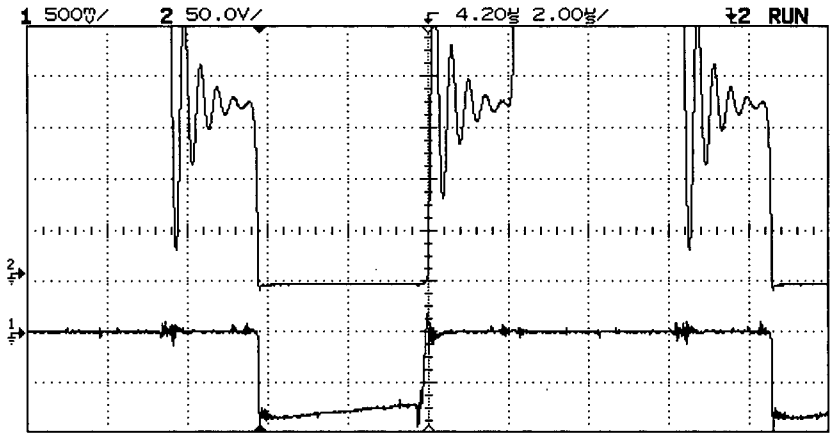
Ch1 = -VdsQ3, Ch2 = IQ3, Vin =2.0V, Iin = 1.1, Vo = 28.7V



c) discharge operation with IRF840 FETs. Synchronously rectified and switch timing adjusted to prevent shoot through.

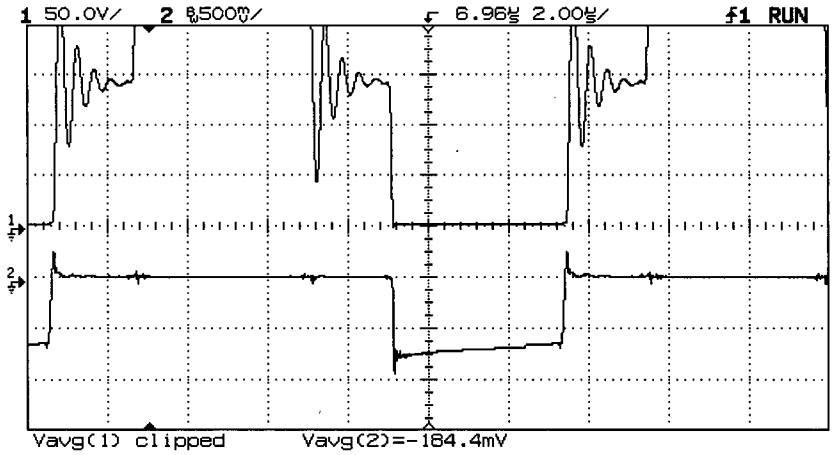
Ch1 = -VdsQ3, Ch2 = IQ3(2A/div), Vin =11.9V, Iin = 29.2, Vo 168

Figure 19: Power Circuit operation with IRF840 FETs



a) discharge operation with 12N60B3D IGBTs. Not synchronously rectified

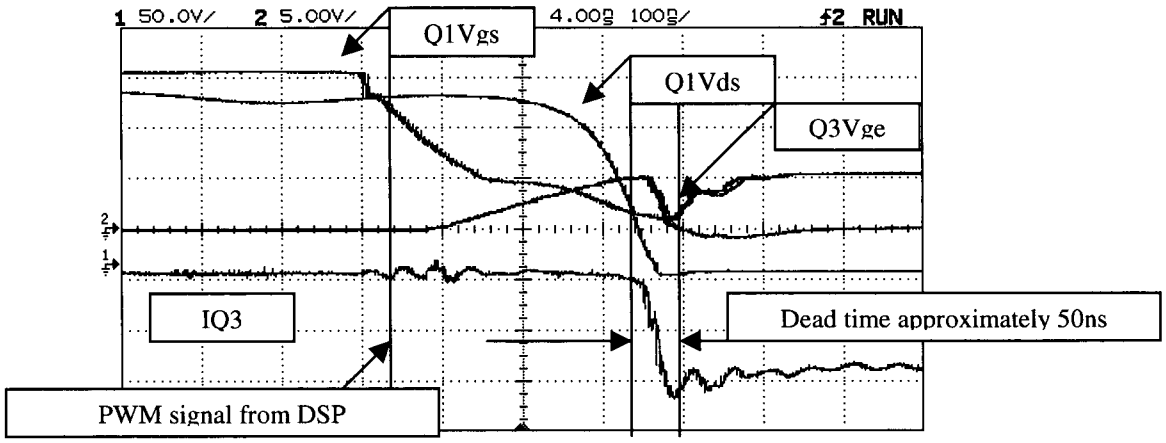
Ch1 = -VceQ3, Ch2 = -IQ3, Vin =12V, Iin = 29.2, Vo = 168V



b) discharge operation with 12N60B3D IGBTs. Synchronously rectified and switch timing adjusted to prevent shoot through

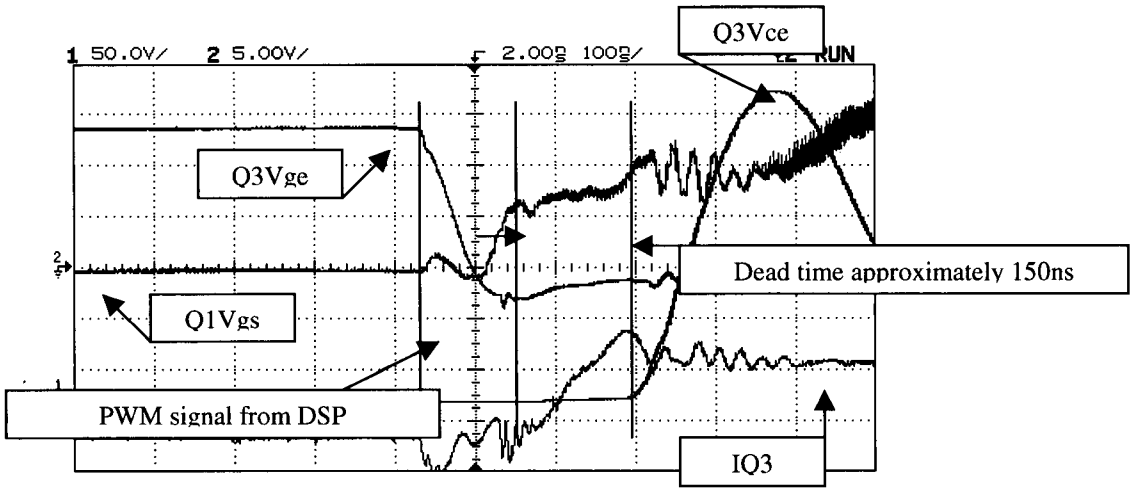
Ch1 = VceQ3, Ch2 = IQ3, Vin =12.0V, Iin = 31.7, Vo = 166.0V

Figure 20: Power Circuit Operation with 12N60B3D IGBTs



a) Forward operation IGBT switch on. Synchronously rectified and switch timing adjusted to prevent cross-over

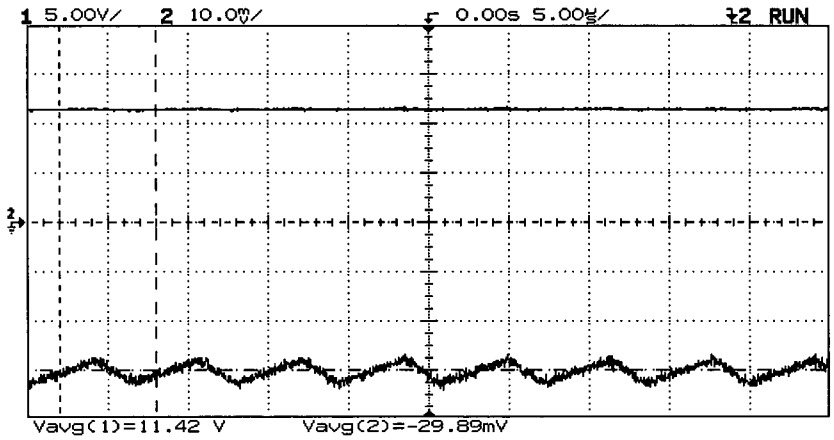
Vin =12.0V, Iin = 31.7, Vo = 166.0V



b) Forward operation IGBT switch off. Synchronously rectified and switch timing adjusted to prevent cross-over

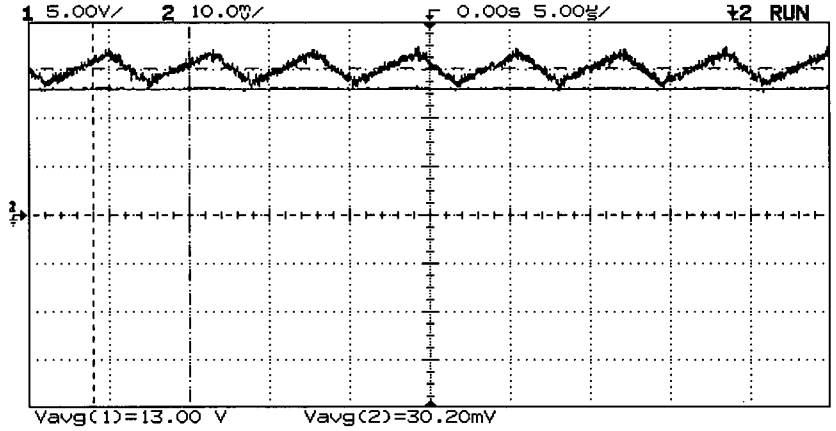
Vin =12.0V, Iin = 31.7, Vo = 166.0V

Figure 21: Detailed IGBT switch timing



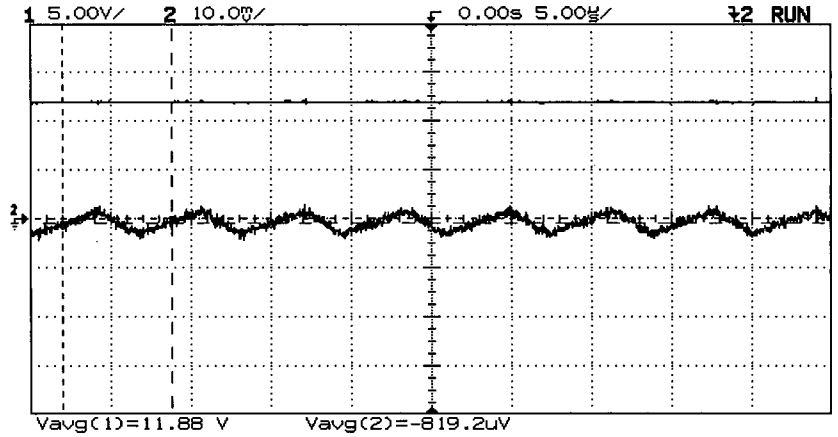
a) Bi-directional converter discharge operation

Ch1 = Battery Voltage Ch2 = IL(5A/div), Vo = 166.7, Io = 0.90A



b) Bi-directional converter charge operation

Ch1 = Battery Voltage Ch2 = IL(5A/div), Vo = 212.7, Io = 1.03A



c) Bi-directional converter no load operation

Ch1 = Battery Voltage Ch2 = IL(5A/div), Vo = 184.5, Io = 0.0A

Figure 22: Seamless bi-directional current

2.6.4 Summary of performance

The following table summarizes the experimental results. It is concluded that the converter with the low side FET and high side IGBT combination provides the most efficient operation.

Synchronously Rectified Test Data	**Mode**	**Vbatt**	**Ibatt**	***Vdcbus***	***Idcbus***	***Eff. @~250W***	***Notes***
Low Side 3205 FETs and High Side MUR860 rectifier diodes	discharge / invert	11.1V	19A	156V	1.26A	93%	
	charge	n/a	n/a	n/a	n/a	n/a	unidirectional only
Low Side 3205 FETs and High Side IRF840 FETs	discharge/ invert	11.4V	20.3A	153V	1.28A	88%	Q3, Q4 rgate = 400 ohm
	charge	14.3V	16.0A	234V	1.18A	83%	
Low Side 3205 FETs and High Side 12N60B3D IGBTs	discharge / invert	10.9V	18.7A	154V	1.23A	92%	Q3, Q4 rgate = 220 ohm
	charge	13V	15.1A	212.7V	1.03A	90%	

Table 8: Synchronously rectified performance results

Summary of dc-dc converter operational efficiencies @~250W	**Discharge Efficiency**	**Discharge (invert mode) Efficiency Synchronously Rectified**	**Charge Efficiency Synchronously Rechified**
Low side 3205 FETs and high side MUR860 rectifier diodes	93%	N/A	N/A
Low side 2305 FETs and High side IRF840 FETs	failed	88%	83%
Low Side 3205 FETs and High Side 12N60B3D IGBTs	91%	89%	92%

Table 9: Summary of operational efficiencies

Chapter 3 - Discrete time feedback control of the power-circuit

The proposed DSP based digital control system developed in this chapter regulates the energy flow into and out of the battery via a single integrated circuit (IC) digital controller. The DSP controller processes the bus voltage and switch current input signals, computes a single control output and generates the four PWM output signals required to gate the power switching devices. The proposed centralized digital control approach reduces the hardware requirements significantly as compared to an analog controller based approach, especially given the multi control mode requirements of the bi-directional converter. The digital controller also offers manufacturing advantages, is inherently more reliable, insensitive to temperature and age drift and may well reduce the overall converter cost [3].

As stated above, the synchronously rectified bi-directional converter developed in chapter one requires a single duty cycle control output to regulate all modes of regulation. To change from battery charge to discharge, for example, requires adjustment of only the switch duty cycle. No adjustment of the switch gating pattern is required. Similar circuits in the literature tend to have separate charge and discharge switching patterns due to their non-synchronously rectified topologies. The control system design of the proposed bi-directional converter is therefore conceptually simplified as the number of controlled outputs is reduced to one.

This chapter primarily discusses the development of a multi mode digital closed loop control system for the thesis converter. In particular, the non-linear dynamics of the power circuit are considered with respect to developing the single input single output plant models for use in the control system design process. Numerous papers appear in the literature discussing both analog and digital control of SMPS dc-dc converter circuit topologies. The majority of these discussions focus on deriving a small signal linearized model of the non-linear SMPS circuit topologies using time-domain circuit averaging techniques. However, it is not clear which operating point should be used to form the small signal models as the linearized models clearly vary with the power-circuit operating point. This question will be investigated with respect to the thesis converter application.

Ultimately three closed loop controllers representing the three control modes of operation and their discrete time control calculations are derived. A decision-making algorithm to cycle between the control modes is also presented.

3.1 Automatic tri-mode bilateral control strategy

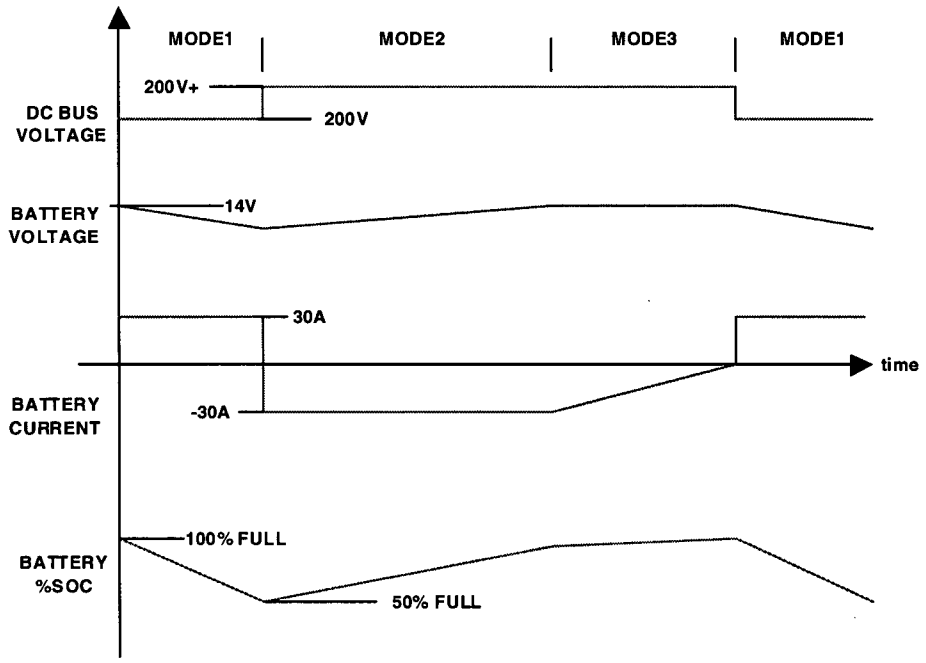


Figure 23: Bi-directional converter charge/discharge operation

Figure 23 presents the required charge/discharge operation of the thesis converter. The converter must be capable of regulating and automatically switching between the following closed loop control modes of operation: 1) Regulate the dc bus voltage at 200V for *"invert"* mode discharge operation. 2) Regulate the charge current at -30A for constant current *"bulk charge"* operation. 3) Regulate the battery voltage at 14V for constant voltage *"absorption charge"* mode operation. Modes two and three represent the standard bulk charge and absorption battery charging stages while mode one regulates the dc bus whenever there is no charge energy available.

To achieve tri-mode control three individual closed loop digital controllers are proposed in block diagram form within figure 24. In each case the digital controller samples the appropriate output of the power converter, compares it to a reference and the resultant error is input to a digital compensator. The output of the digital compensator is a discrete duty cycle value, which is then zero order held and then fed back into the power

circuit in a switch duty cycle form. Note the s-domain power circuit transfer functions are functions of the operating point duty cycle, *D*, and output state values, *X*. This will be discussed in more detail in a later section 3.2. The three digital compensators must be designed to regulate the output at a reference set point with fast response and zero steady state error.

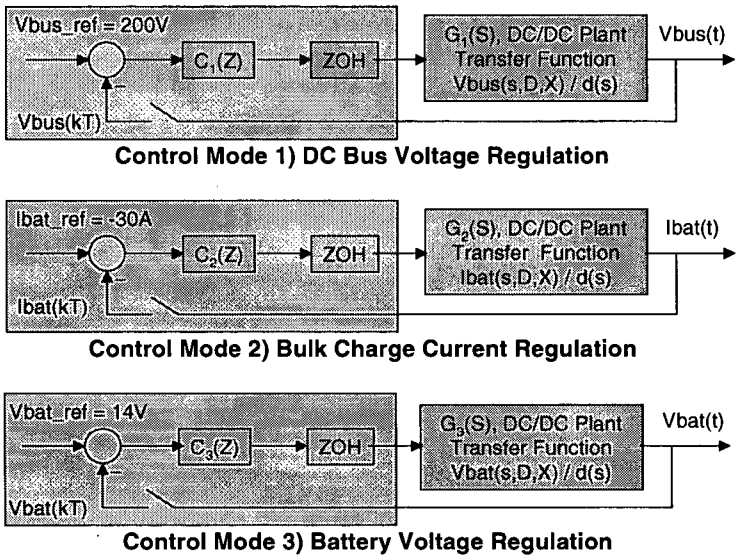
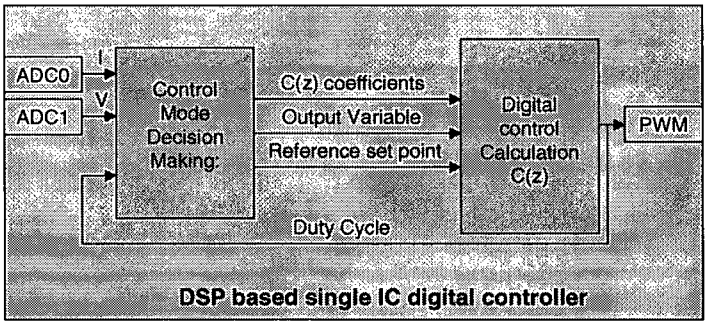


Figure 24: Three closed loop digital controllers

The fundamental design objective of the closed loop control systems design is to specify the digital compensator transfer functions $C_1(Z)$, $C_2(Z)$ and $C_3(Z)$ to yield fast and stable closed loop control performance. In order to utilize any of the well established frequency domain compensator design techniques it is necessary to obtain a linear dynamic model describing the input to output characteristics of the plant to be controlled. This model is usually expressed in a convenient s-domain transfer function form. In the case of the thesis converter it is necessary to obtain the three unique linear transfer function models of the power circuit appearing in figure 24. This is where the complications begin, as the switching power circuit is inherently not a linear system. It is actually two alternating linear systems whose appearances are controlled by the on or off

state of the switch duty cycle. This problem has been addressed in the literature and methods have been developed to produce linearized plant models valid for small-signal linearizarion around a fixed duty-cycle operating point. To further complicate things the dynamic behavior of the power circuit is also a function of the circuit loading. It is therefore a combination of duty cycle and circuit loading that defines the operating point. Section 3.2 of this thesis develops the appropriate linear plant model for compensator design based on the determination of the worst case operating points.



Control Mode Decision Algorithm - once per sample:

If Vbus < 200V then Mode 1) Bus Voltage Regulation
else
If Ibat < -30A then Mode 2) "Bulk Charge" Current Regulation
else
If Vbat > 14V then Mode 3) "Absorption" Battery Voltage Regulation
else
use previous control mode

Figure 25: Control Mode decision Algorithm

Figure 25 presents the proposed automatic digital control strategy. This novel digital control strategy uses a single control output computational stage combined with a control mode decision making stage. Every sample period a control mode decision is made according to the algorithm of figure 25. The decision, based solely on measurements of the bus voltage and *Sw4* current, simply selects the output variable, reference set point and compensator coefficients to be sent to the control calculation stage. The single control calculation stage determines the set point error and calculates a

duty cycle control output via the control equation defined by *C(Z)*. In this way the bi-directional converter is completely automatic and autonomous.

The three controllers of figure 23 require bus voltage, battery current and battery voltage information yet only direct information regarding the bus voltage and current through *Sw4* is available to the DSP. The decision making stage internally computes the required output variables *Vbus, Ibat* and *Vbat* from the measured voltage, *V*, and current, *I*, and internal duty cycle, *dc*, according to the following equations:

The bus voltage of course is simply equal to the measured voltage as shown in equation 3.1.1.

$$Vbus(V, I, D) = V \tag{3.1.1}$$

Since only the current through *Sw4* is measured and input to the controller, the actual battery current needs to be calculated by the DSP. Initially it was thought that the voltage developed across a current sense resistor could be used directly as the input to the DSP. In this way a voltage signal directly proportional to the average battery current would be available to the DSP's analog to digital converter (ADC) input by synchronizing the sampling instant to the middle of the *Sw4* current pulse. In actuality this is not possible as the bi-directional converter current produces both positive and negative voltages on the sense resistor and the ADC of the DSP accepts only positive voltages. This necessitates the use of a level shift circuit to represent the entire range of bi-directional output currents as positive voltages input to the ADC. In practice it proved difficult to implement a level shift circuit with enough bandwidth to accurately recreate the square voltage pulse. A level shifted and time averaged value of *ISw4* proved much easier to obtain. However, the battery current is no longer directly proportional to the time averaged current. Using the time averaged current through *Sw4* the battery current can be calculated as a function of the duty cycle as shown in equation 3.1.2.

$$Ibat(V, I, D) = \frac{2 \cdot N \cdot I}{1 - D} \tag{3.1.2}$$

where I is the time averaged current flowing through *Sw4*. This equation also calls for the computation of *1/(1-D)* which is difficult to implement in the fixed point DSP as it does

not divide in factors other than 2^{-n}. In practice it proved necessary to implement the *1/(1-D)* with a duty cycle look up table consisting of *DQ* entries *(2.5.2)*.

Calculating the voltage conversion ratio of the converter can obtain the battery voltage as shown in equation 3.1.3.

$$Vbat(V, I, D) = \frac{V \cdot (1 - D)}{N} \qquad (3.1.3)$$

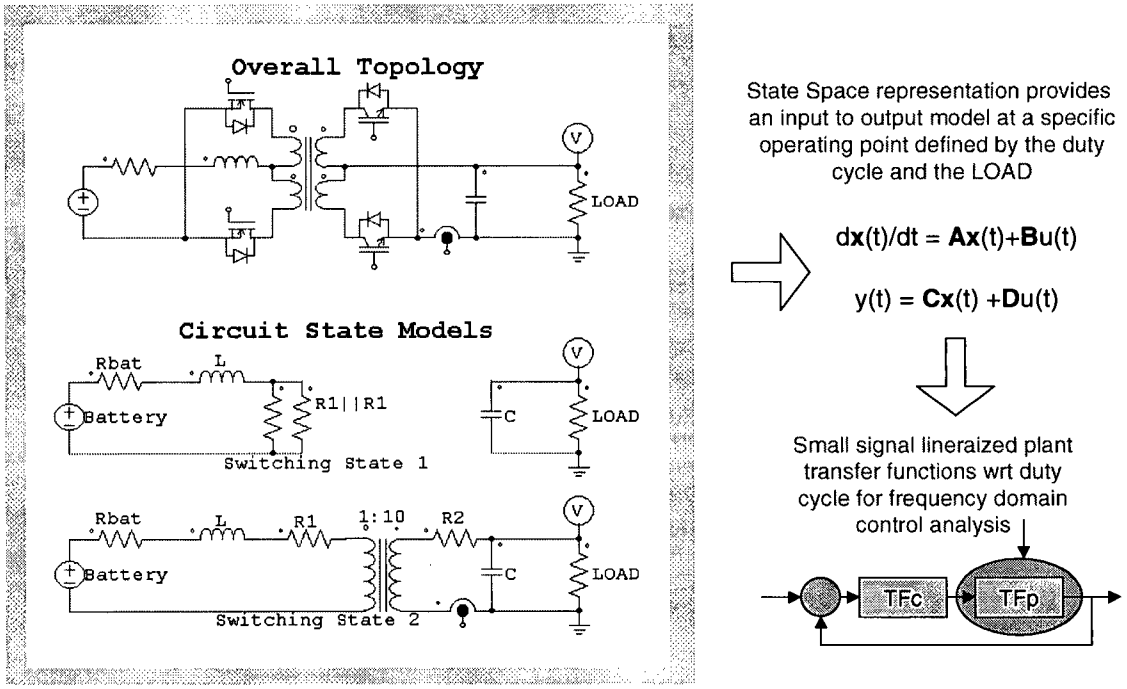
An automatic digital control strategy using only V and I to control the converter in the three modes of operation has now been defined. To design the closed loop compensators $C_1(Z)$, $C_2(Z)$ and $C_3(Z)$ suitable plant models of the power stage are required. The power circuit plant models are developed in the next section.

3.2 Small-signal plant modeling and large-signal operation

The two main switched mode power circuit modeling techniques appearing in the literature are the circuit averaging approach and the state space averaging based modeling approach. A good overview of these two techniques is presented in the well-referenced paper [17]. The circuit averaging approach uses duty cycle averaged voltage and current sources with which a continuous circuit model consisting of only sources and passive components is created. Traditional circuit analysis techniques can then be used to derive linearized input output type transfer functions. In continuous inductor current mode the state-space averaged method uses two individual state space representations of circuit in differential equation form; one circuit representation for each state of the duty cycle. The two models are then averaged together by a duty cycle weighting factor to create a single state-space averaged model. Traditional state-space analysis techniques can then be used to create input output transfer function relationships. The state space based approach has been selected for thesis converter application because, as it will be shown, MATLAB software contains tools that can be conveniently used to compute the state equations and develop the s-domain plant models. It will also be shown that the MATLAB software package can be used as a very powerful design tool for digital SMPS control loop design and circuit simulation.

Figure 26 shows the fundamental flow of the state space modeling approach for the thesis converter. The circuit of the synchronously rectified Clarke converter is broken down into two continuous circuit representations - one for each switching state. Although the transformer coupled Clarke converter actually has four individual switch states the inherent symmetry allows the converter to be modeled as the two individual states shown in figure 26. An averaged state time-domain representation of the circuit is then derived from the state space representations for the individual circuits. From the averaged state model a small signal lineraized plant transfer function is derived for use in the closed loop controller design. Note that the proposed Clarke converter topology never operates in the discontinuous inductor current mode as the inductor current is always free to operate in either direction.

Of specific interest are the three distinct linearized dynamic plant relationships outlined in figure 24. To reiterate, these plant transfer function relationships are: 1) Duty cycle to output voltage during bus voltage regulation. 2) Duty cycle to battery current for during constant current charging. 3) Duty cycle to battery voltage during battery voltage regulation



R.D. Middlebrook: A general unified approach to modeling switching converter power stages, PESC '76

Figure 26: General state space approach to obtain the power circuit plant model.

Traditionally an analog network analyzer is used to obtain the plant model directly from a prototype power circuit. A small ac perturbation is superimposed on the duty-cycle and the specific output response is measured over a spectrum of useful frequencies. The plant characteristics can then be used design stable feedback compensation loops. This approach is difficult to implement with the DSP driven power circuit as it is very inconvenient to inject the analog modulation signal. The duty cycle is internal to the DSP and physically unavailable as an analog signal to modulate. Additionally the duty cycle quantized and sinusoidal modulation is inherently difficult. A

detailed state-space modeling approach can avoid the complications of prototyping and injecting the modulating signal into the DSP.

The following sections describe in detail how the state averaging technique has been adapted to create accurate small signal linearized plant transfer function models of the thesis Clarke converter in its three distinct modes of operation and without the need for the network analyzer. Of note is the implementation of an ideal transfer representation in the circuit model. Due to the relatively slow circuit dynamics vis-à-vis the transformer parasitic effects and the operation of the conservatively designed transformer in its linear region, the ideal transformer is all that is required to form an accurate dynamic power circuit model. This model is observed to be valid within the bandwidth of interest via successful simulation results as compared to measured data.

3.2.1 Dynamic plant model for control mode 1: discharge voltage regulation

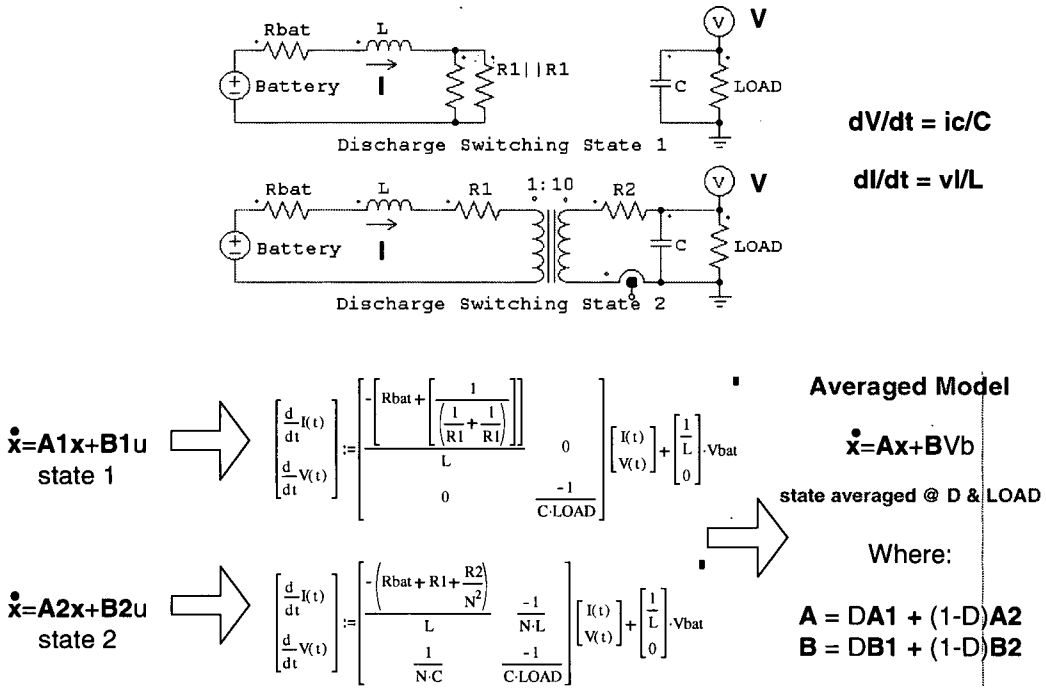


Figure 27: Bus Voltage Regulation Plant model

The process of obtaining the state space averaged plant model of the power circuit in dc bus voltage regulation mode is presented in figure 27. The state matrix based differential equations can be written as shown with inductor current and output voltage selected as the two state variables *I(t)* and *V(t)*. Note the output voltage state variable *V* is the output of specific interest. The internal battery voltage, *Vbat*, is conveniently defined as the input parameter, *u*, of the state space representation. In figure 27 the two individual 2nd order state space representations have been developed in sufficient detail to include the effects of the switch resistances as well as the internal resistance of the battery. This level of detail is, in many cases, omitted as it is time consuming to develop the equations

accurately. However, it is the intention of this thesis to model the converter as accurately as possible and later investigate if the same model can be used as the core of an accurate simulation algorithm.

Weighting the two models together based on a duty cycle weighting factor, D, forms the single state space averaged model also shown in figure 27. Within the averaged model the steady state voltage conversion ratio is ultimately controlled by the duty cycle, D, while the *LOAD*, defined here now as R, determines the steady state inductor current. It is now clear to see that the averaged model is a function of the duty cycle and the load resistance as the state space averaged model is formed at a specific duty cycle, D, with a specific value of load resistance, R.

To develop a suitable plant model the duty cycle and load dependent state space averaged model can be initially written in the form of equation (3.2.1)

$$[\dot{x}] = [A(D,R)]\cdot[x] + [B(D)]\cdot u \qquad (3.2.1)$$

which is a linear system for fixed values of D and R.

The *linear* system of equation (3.2.1) can be perturbed with variations in the input by representing the input as a dc component, U, with a superimposed dynamic ac component, $\hat{u}$, as presented in equation (3.2.2)

$$[\dot{x}] = [A(D,R)]\cdot[X] + [B(D)]\cdot[U] + [A(D,R)]\cdot[\hat{x}] + [B(D)]\cdot\hat{u} \qquad (3.2.2)$$

where U is the dc component and $\hat{u}$ is ac component of the perturbed input battery voltage and $[X]$ and $[\hat{x}]$ are the dc and ac components of the state vector respectively. There is no dc $[\dot{x}]$ and by definition $[A]\cdot[X] + [B]\cdot U$ must equal zero. The dc operating point, X, of the state variables I and V can therefore be calculated as a function of U, D and R according to equation (3.2.3).

$$[X] = -[A(D,R)]^{-1}\cdot[B(D)]\cdot U \qquad (3.2.3)$$

The linear transfer functions describing the state output responses to the input, u(s), can be derived according to the well know state space process of equation (3.2.4) [38]

$$\frac{[x(s)]}{u(s)} = (s[I] - [A(D,R)])^{-1} \cdot [B(D)] \qquad (3.2.4)$$

where $[x(s)]$is a vector of $V(s)$ and $I(s)$ and $[I]$ is a 2 by 2 unit matrix. Unfortunately, although straightforward to obtain, these transfer functions are not of much use for the controller design as only the controller output duty cycle perturbations to state output transfer functions are of practical interest.

Perturbations to the duty cycle can be included in the above analysis by further defining the duty cycle as a dc component, D, plus a superimposed ac component, $\hat{d}$. Equation (3.2.2) can be expanded to include the time variation of the duty cycle resulting in equation (3.2.5).

$$[\dot{x}] = [A(D,R)] \cdot [X] + [B(D)] \cdot U + [A(D,R)] \cdot [\hat{x}] + [B(D)] \cdot \hat{u} + [([A1] - [A2]) \cdot [X] + ([B1] - [B2]) \cdot U] \cdot \hat{d} + [([A1] - [A2]) \cdot [\hat{x}] + ([B1] - [B2]) \cdot \hat{u}] \cdot \hat{d} \qquad (3.2.5)$$

Equation (3.2.5) is non-linear as the last term contains the multiplication of the time dependant variables $[\hat{x}], \hat{u}$ and $\hat{d}$. Assuming the ac variations are much less than the dc components the last term of equation (3.2.5) can be neglected due to the relative reduction effect of multiplying the ac components. Furthermore the first two terms can also be eliminated because they add to zero. The resulting dynamic equation of (3.2.6) is therefore linearized for changes in u and d around a fixed operating point defined by $[A(D,R)]$ and $[X(D,R,U)]$. Or, in words, around an operating point defined by a fixed duty cycle, load resistance and input voltage.

$$[\dot{x}] = [A(D,R)] \cdot [\hat{x}] + [B(D)] \cdot \hat{u} + [(A1 - A2) \cdot [X] + (B1 - B2) \cdot U] \cdot \hat{d} \qquad (3.2.6)$$

Equation (3.2.6) describes the small signal dynamic behavior of the two output state variables as a function of two input variables. The transfer function relationship can now be expressed as

$$[x(s)] = [G_{ux}(s)] \cdot u(s) + [G_{dx}(s)] \cdot d(s) \qquad 3.2.7)$$

where $G_{ux}(s)$ is equal to equation (3.2.4) and the small signal valid $G_{dx}(s)$ is calculated as

$$[G_{dx}(s)] = \frac{[x(s)]}{d(s)} = (s[I] - [A(D,R)])^{-1} \cdot [([A1] - [A2]) \cdot [X] + ([B1] - [B2]) \cdot U] \qquad (3.2.8)$$

Equation 3.2.8 yields the crucial duty cycle to output voltage transfer function equation required for the control loop design in $[G_{dx}(s)]_{2,1}$. It is also observed that $[G_{dx}(s)]$is dependant on the operating point in $[X]$, in $[A(D,R)]$ and also in U.

As mentioned previously, the MATLAB (matrix laboratory) software package can be used as an effective tool for calculating plant model transfer functions. Initially, the state matrices can be defined directly from figure 27 as:

```
% DEFINE STATE MATRICIES
A1 =    [ -( (1/((1/R1)+(1/R1)))+Rbat)/L1     0;
          0                                   -1/(R*C1)];

A2 =    [ -(Rbat+R2+(R2/N^2))/L1     -1/(N*L1);
        1/(N*C1)                     -1/(R*C1)];

B1 =    [1/L1;
         0 ];

B2 =    [1/L1;
         0];
```

(3.2.9)

Then duty cycle averaged state matrices calculated as:

```
% AVERAGED STATE MATRICIES
A  =    D*A1 + (1-D)*A2
B  =    D*B1 + (1-D)*B2
C  =    [0 1]                    % SELECTS VOLTAGE STATE OUTPUT
D  =    [0];                     % NO FEEDFOWARD EFFECTS
```

(3.2.10)

Then the dc operating point can be calculated as:

```
% DC LARGE SIGNAL OPERATING POINT
X = -(inv(A))*B*VBAT
```

Eq. 3.2.11

And finally the duty cycle to voltage transfer function can be calculated in one simple step as:

```
% DUTY CYCLE TO VOLTAGE STATE OUTPUT SMALL SIGNAL TRANSFER FUNCTION
[NUM,DEN] = SS2TF(A,((A1-A2)*X + (B1-B2)*VBAT),C,D);
```

Eq. 3.2.12

where NUM and DEN are vectors containing the transfer function coefficients in descending powers of s. Once more, note the resulting transfer function's large signal dependence on the variables load, *R*, duty cycle, *D* and internal battery voltage, *Vbat*.

3.2.2 Dynamic plant model for control modes 2 & 3: charge regulation

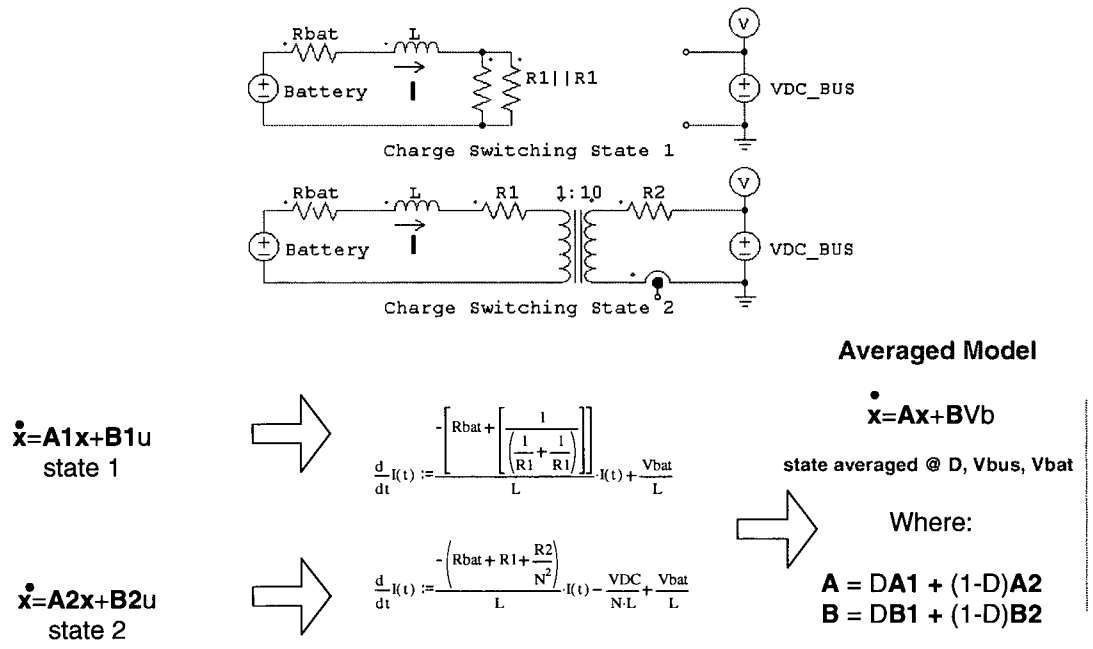


Figure 28: Battery Charging Plant Model

Figure 28 details the battery charging power circuit model. The proposed state space approach uses the same state space averaged framework as used generating the mode 1 bus voltage regulation plant model of the previous section. The main difference being there is now only one state variable to consider; the inductor current. The second order effects of output capacitor disappear as the dc bus must now be modeled as a 200 to 250 volt source. It is no longer a dynamic state output. The battery's internal voltage, *Vbat*, is again defined as the system input parameter, *u*. The bus voltage level, *VDC*, and also *Vbat* now must appear within the *B2* matrix to complete the state space representation. At this point it becomes apparent that the averaged model is now going to be large signal dependent on both the duty cycle and the difference between the bus and internal battery voltages.

The first order dynamic plant transfer function is formed according to the same procedure of the previous section. In fact this is the reason to use the same state space averaged modeling as used in the previous section with the mode 1 plant model. The linearized plant model of the modes 2 and 3 charging power circuit can now be described by

$$G_{dx}(s) = \frac{x(s)}{d(s)} = (s[I] - [A(D,R)])^{-1} \cdot [([A1] - [A2]) \cdot [X] + ([B1] - [B2(VDC,VBAT)]) \cdot U]$$

(3.2.13)

where the single state $x(s)$ is the inductor current, $I(s)$, and $G_{dx}(s)$ is the small signal duty cycle to inductor current transfer function. This is the specific plant model required for the constant current charge controller. MATLAB can again be used to easily compute the transfer function equation according to the following. Initially the state matrices can be defined as:

```
% DEFINE STATE MATRICIES
A1 =    [ -( (1/((1/R1)+(1/R1)))+Rbat)/L1];
A2 =    [ -(Rbat+R2+(R2/N^2))/L1];

B1  =   [1/L1];
B2  =   [ (1 - ( VDC/(N*VBAT) ) ) * (1/L1)];
```

(3.2.14)

Then duty cycle averaged state matrices calculated as:

```
% AVERAGED STATE MATRICIES
A   =       d*A1 + (1-d)*A2;
B   =       d*B1 + (1-d)*B2;
C   =       [1];                    % INDUCTOR CURRENT IS THE ONLY STATE
D   =       [0];                    % NO FEEDFOWARD EFFECTS
```

(3.2.15)

Then the dc operating point can be calculated as:

```
% DC LARGE SIGNAL OPERATING POINT
X = -(inv(A))*B*VBAT
```

(3.2.16)

And finally the duty cycle to voltage transfer function can be calculated in one simple step as:

```
% DUTY CYCLE TO INDUCTOR CURRENT STATE OUTPUT SMALL SIGNAL TRANSFER FUNCTION
[NUM,DEN] = SS2TF(A,((A1-A2)*X + (B1-B2(VDC,VBAT))*VBAT),C,D);
```

(3.2.17)

where the small signal transfer function is large signal dependent on the duty cycle, *D*, the bus voltage, *VDC,* and the internal battery voltage, *Vbat.*

The battery terminal voltage is directly related to the inductor current according to

$$Vterm = Vbat - I \cdot Rbat \tag{3.2.18}$$

which means the small signal duty cycle to battery terminal voltage transfer function can be defined as

```
% DUTY CYCLE TO BATTERY TERMINAL VOLTAGE SMALL SIGNAL TRANSFER FUNCTION
[NUM,DEN] = -Rbat*[SS2TF(A,((A1-A2)*X + (B1-B2(VDC,VBAT))*VBAT),C,D)];
```

(3.2.17)

where the small signal duty cycle to inductor current transfer function is simply multiplied by the negative of the battery internal resistance, *-Rbat.*

3.3 Digital compensator design

The objective of this section of to explore the design and development of the three digital single loop feedback compensators defined in section 3.1. Initially, a brief overview of voltage mode and current mode control will be discussed to give the reader some background into the sometimes confusing nomenclature of switch mode power supply (SMPS) field. Next, for each mode of operation a digital controller will be designed using standard frequency domain phase and gain margin stability indicators. To allow for open loop analysis small-signal power-circuit plant models are derived for each control mode of operation. The digital compensator is then deigned around the small-signal model.

Numerous papers appear in the literature discussing both analog and digital control of SMPS dc/dc converter circuit topologies. The majority the controller designs focus on deriving a small-signal linearized model of the non-linear SMPS circuit topologies using time domain circuit averaging techniques. However, selecting the large-signal operating point is seldom discussed. During the design approach proposed within this chapter special attention is paid to the operating point dependency of the small-signal models. Conclusions will be made regarding the appropriate worst case design points used to insure stability. Finally both proportional integral (PI) and integral (I) z-domain transfer functions are developed and presented for each operational control mode of the thesis converter. The I controller form is proven to be the most suitable candidate.

3.3.1 Overview of voltage mode and current mode control

There are two common types of closed loop control approaches for boost and buck LC filter based switching power converters appearing in the literature: *voltage mode* control and *current mode* control. Voltage mode control uses output voltage feedback compared with a reference voltage to program (adjust) the duty cycle to acheive output voltage regulation. Current mode control uses feedback information from both the inductor current and the output voltage to achieve similar output voltage regulation. Examples of the two types of output voltage regulation control schemes can be found in figures 29 & 30.

Many control techniques for boost and buck type converters have been proposed in the literature with well developed *current mode* control techniques offering distinct advantages over *voltage mode* control configurations. Current mode controllers can use either peak or average inductor current feedback on a cycle by cycle basis to control the inductor in the power circuit as a current source. Voltage feedback is then used to program the current reference, *iref* in figure 30, according to the error between the output voltage and an output voltage reference. Although not intuitive, current mode control voltage regulation techniques offer a few important advantages over solely voltage mode control.

A primary advantage is the inductor current can be actively limited by clamping the signal allowed to appear at *iref* thereby providing inherent over current protection. Secondly, due to the effective inductor current source, the control output, *iref*, to output voltage transfer function has a first order response rather than second order. The greater the bandwidth of the inner current loop compared to the outer voltage loop the more pronounced this effect is. Ultimately the single poll roll off response is easier to control as compared to the oscillatory second order response experienced with voltage mode control. In fact with boost converters there can be an order of magnitude increase in the control bandwidth by implementing current mode control over voltage mode control [39]. A third advantage is the automatic feed forward of perturbations in the supply voltage.

Current mode control also has its share of complications. There are practical difficulties involved with measuring the current with enough bandwidth and issues with

stability - eg. operating at duty cycles above 50% with peak current control may require the use of ramp compensation techniques [39]. Designing circuits with current mode controllers has become very popular due to the availability of low cost dedicated controller ICs that perform onboard PWM generation and the double loop control. Aiding in their popularity, the ICs are very simple to implement with the aid of manufacturers application notes.

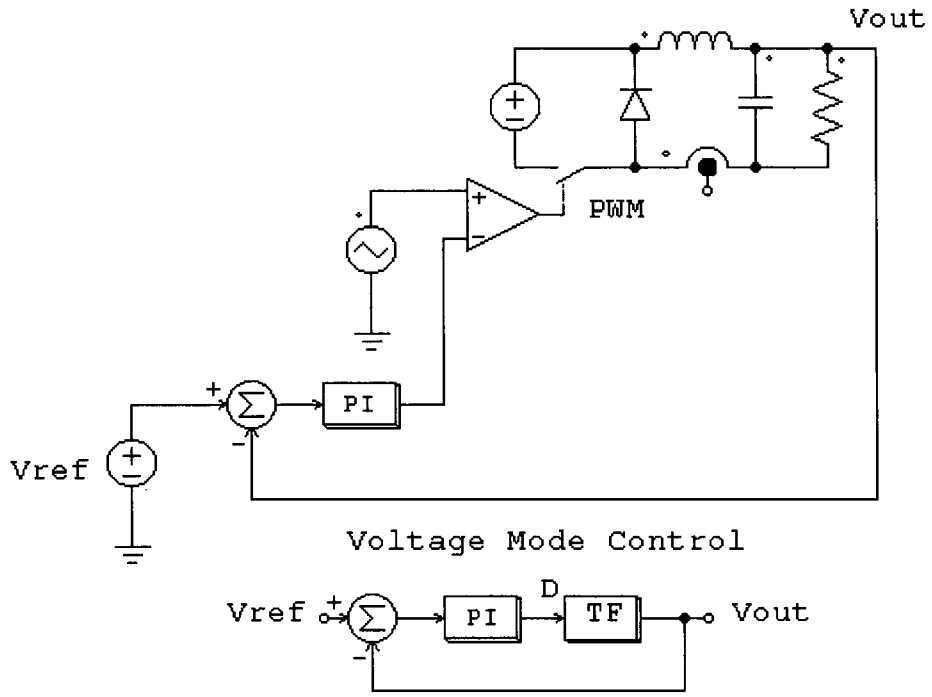


Figure 29: Voltage Mode Control: Buck Converter Voltage Regulator Example

Two of the single loop voltage regulators used for the thesis application, mode 1 and mode 3, are clearly voltage mode control in nature. The remaining battery current regulation loop, mode 2, is a constant current controller but is not a *current mode voltage controller* as defined above. It is very possible that the thesis controller could be designed with double loop current mode controllers for modes 1 and 3 since the power circuit current and voltages are always available. It is also likely that the control bandwidth of especially the mode 1 controller could be dramatically increased. However, the analysis and design processes covered in this thesis are limited to the more straightforward single

loop controller approach. Exploring the potential benefits of implementing double loop digital controllers may make for an interesting future work.

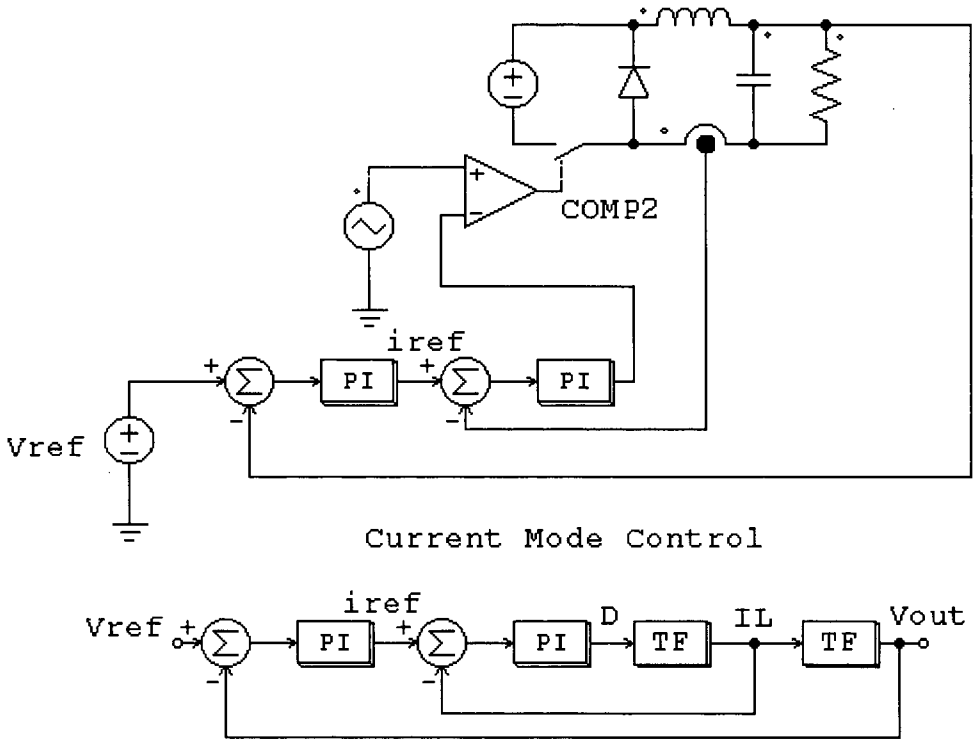


Figure 30: Current Mode Control: Buck Converter Example

3.3.2 Open loop dynamic compensation for control mode 1

The objective of this section is to determine a suitable closed loop digital compensator for the thesis converter operating in dc bus voltage regulation mode while also accounting for the large signal operating point dependence of the plant model. To aid in the controller development process, frequency response design methods are utilized because of their suitability to stable open loop systems and robustness to plant variations.

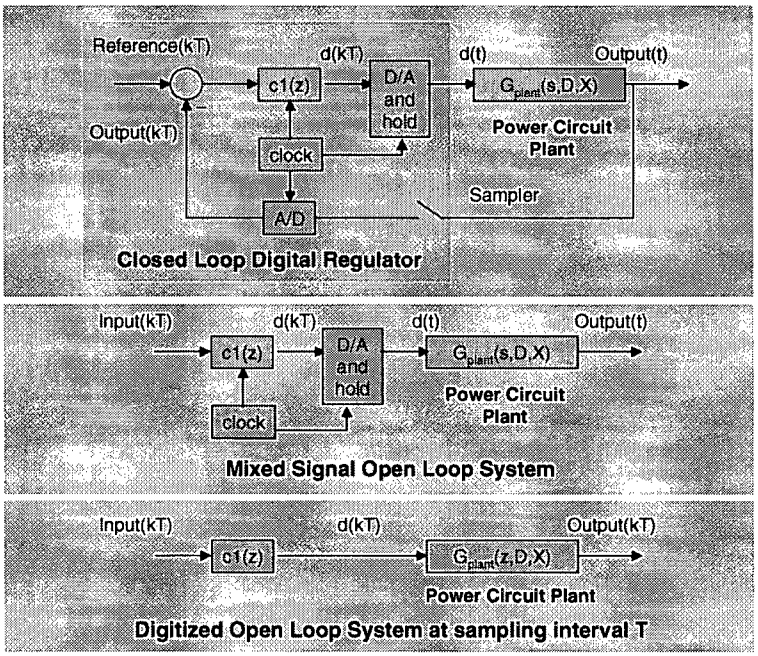


Figure 31: Single loop digital controller with large signal dependent plant

The proposed single loop controller design strategy determines the z-domain digital compensator transfer function based on manipulating the open loop system gain and phase margins according to some well established engineering rules of thumb. These rules are namely that the gain margins should be at least 6dB and the phase margins should be at least 60 degrees for assured stable closed loop operation. The open loop system transfer function is defined as the multiplication of the control compensator transfer function with the plant transfer function. The gain margin is defined as the attenuating gain response, $\left|G_{openloop}(j\omega)\right|_{dB}$, of the cascaded open loop system when the

phase response, $\angle G_{openloop}(j\omega)$, crosses -180 degrees. A gain of above 0dB at this point results in clear unstable closed loop operation. The gain margin fundamentally describes the gain factor by which the entire system can be multiplied before this closed loop instability results. The phase margin is the phase response of the open loop system that exceeds -180 degrees when the gain response crosses unity. The frequency at which this occurs is also known as the unity gain crossover frequency and can be used to describe the control bandwidth of the system. The higher this frequency can be manipulated by the compensator the faster the system will respond. Both the gain margin and phase margin can be easily determined analyzing a bode plot of the open loop system.

The following procedure proposes how MATLAB can be used to determine the open loop response of the digitally compensated system:

1) Obtain the small signal plant transfer function at some operating point from the state-space representation:

```
% DUTY CYCLE TO VOLTAGE STATE OUTPUT SMALL SIGNAL TRANSFER FUNCTION
[NUM,DEN] = SS2TF(A,((A1-A2)*X + (B1-B2)*VBAT),C,D);
G_S = TF(NUM,DEN);
```

(3.3.1)

where *G_S* is the plant model in s domain transfer function form.

2) Digitize the plant model including the D/A and hold - or zero order hold (ZOH) effect on the input duty cycle

```
G_Z = c2d(G_S,Ts,'zoh');
```

(3.3.2)

where Ts is the sampling interval of the digital controller. The 40kHz switching frequency of the converter is also the maximum frequency at which the duty cycle can be updated. It is also, therefore, the uppermost valid sampling frequency. Since it is desirable to push the control bandwidths as high as possible a 40kHz sampling frequency is selected for the thesis converter application. This is actually convenient for two reasons. Generally it is possible to achieve control bandwidths of 1/10 sampling frequency and secondly, the state space averaged model is considered valid only for frequencies below 1/10 the switching frequency [17]. Utilizing 40kKz sampling

frequency, therefore, allows accurate control system development with control bandwidths up to a maximum of approximately 4kHz. Sampling at 40kHz with the 20 MIPS TMS320F243 DSP yields an adequate 500 intermediate instruction cycles to perform the control calculation and associated computational overhead before the updated duty cycle is required at the next sample interval. Sampling at a lesser frequency will have the effect of reducing the control bandwidth of the digital controller. However, sampling at the switching frequency is not usually an *expensive* proposition when using a DSP as the processor always has be about 500 times faster to support the PWM duty cycle generation with adequate *DQ* or duty cycle resolution (equation 2.5.2).

3) Define the compensator transfer function using numerator and denominator polynomials in descending powers of s.

```
C_S = TF([0 Ki],[1 0])
% integrator example C_S = Ki/S
```

(3.3.3)

In this way it is possible to specify compensator with any combination of poles and zeros for manipulating the open loop response.

4) Discreteize the compensator into a z domain transfer function. That transfer function will eventually be used as the basis for the duty cycle output calculation performed within the digital controller.

```
C_Z = c2d(C_S,Ts,'zoh')
% C_Z = integrator example Ki*(Ts/2)*(Z+1)/(Z-1)
```

(3.3.4)

There are a number of emulation methods available for digitizing an analog transfer function including: the bi-linear transform or tustin method, tustin method with prewarping, matched pole zero method and a few others [40]. The digital approximation of the continuous system differs slightly between the methods with reducing discrepancy as the sampling frequency is increased. For the thesis converter application the 40kHz sampling frequency is one or two orders of magnitude higher than the critical frequency of the open loop making the choice of emulation techniques is virtually arbitrary from an

error point of view. The ZOH method is chosen as it is the defacto method within MATLAB and many application examples.

5) Consult the open loop bode plots for control bandwidth and the gain/phase margin stability indicators.

```
LTIVIEW('bode',C_Z*G_Z)
```

(3.3.5)

The MATLAB LTIVIEW command is a very powerful tool for designing the control compensator. It launches a viewer that contains a Bode representation, among others, of system in question. On the Bode plot the phase margin and gain margin indicators can be automatically displayed for easy interpretation.

6) If necessary adjust the compensator in either step three or directly in step four to improve control performance. This iterative process combines a basic understanding of the open loop response by adding transfer function poles and zeros with an immediate graphical display of the resulting open loop system response. This leads to easy visual examination and iterative manipulation of the stability indicators.

3.3.2.1 Control mode 1: small signal plant representations

The component values used for the actual thesis converter in discharge mode are as follows:

```
% GIVEN POWER CIRCUIT INFORMATION

Ts =    .000025;        %sampling interval for digital emulation
L1=     20e-6;          %inductor value in Henrys
C1=     6e-6;           %dc bus capacitor in Farads
Rbat =  .0025;          %Battery Internal Resistance
R1 =    .040;           %RDSon of the low voltage switches and board copper
R2  =   .050;           %RDSon of the high voltage switches and board copper
N =     10;             %transformer turns ratio
```

(3.3.6)

Even though it is possible to calculate the small signal transfer function using equations 3.2.9 through 3.2.11 the worst case large signal operating point around which to design compensator remains unknown. This thesis proposes to determine the worst case operating point by analyzing the open loop system responses at various operating points and observing the worst case phase and gain margin indicators. The worst case operating point will, of course, have the weakest stability indicators.

As a first step in the process the uncompensated plant transfer function can be observed at various operating points. Three reference points are used for the analysis: no load, 400W loading and 800W loading where in all three cases the bus is regulated at 200V and the load, *R*, determines the power output. In each case the corresponding duty cycle required to support the 200V bus in association with the load resistance, *R*, and battery voltage, *VBAT*, define the particular large signal operating point. In addition to the information in equation 3.3.6 the following plant information can be derived for each operating point.

For no load operation:

```
% 0W LOAD LARGE SIGNAL PARAMETERS
R =     10e8;       %Load Resistance
VBAT =  14;         %Battery Voltage
D =     .30;        %Duty Cycle required for 200V Bus

Small Signal Transfer function:
-0.05556 s + 1e010                  POLES = 1.0e+003 *          ZEROS =
-------------------------          -1.3230 + 5.3150i           1.8000e+011
s^2 + 2646 s + 3e007                -1.3230 - 5.3150i

Large Signal Operating Point = 0.0000 A , 200.0000 V
```

(3.3.7)

For 400W bus load:

```
% 400W LARGE SIGNAL PARAMETERS
R =      100;          %Load Resistance
VBAT = 12;             %Battery Voltage
D =     .44            %Duty Cycle required for 200V Bus

Small Signal Transfer function:
-6.715e005 s + 7.638e009          POLES =1.0e+003 *          ZEROS =
------------------------          -2.0296 + 4.5499i          1.1375e+004
s^2 + 4059 s + 2.482e007          -2.0296 - 4.5499i

Large Signal Operating Point = 40.2887 A , 200.0000 V
```

(3.3.8)

For 800W bus load:

```
% 800W LARGE SIGNAL PARAMETERS
 R =50;            %Load Resistance
VBAT = 12;             %Battery Voltage
d =      .62           %Duty Cycle required for 200V bus

Small Signal Transfer function:
-1.755e006 s + 4.361e009          POLES =  1.0e+003 *        ZEROS =
------------------------          -2.7108 + 3.4126i          2.4850e+003
s^2 + 5422 s + 1.899e007          -2.7108 - 3.4126i

Large Signal Operating Point = 105.2946 A , 200.0597 V
```

(3.3.9)

The bode plot of the three mode 1 small signal state space derived plant transfer functions and their digitized counterparts can be found in figure 32. MATLAB automatically inserts the vertical line at the 20 kHz Nyquist frequency of the 40 kHz sampling rate after which there is no defined response for the digitized representation. The analog and their respective digital responses have been plotted on top of each other to visually indicate the digitization effects. The gain responses are within 3dB until about 80,000 rad/s or 12.5 kHz and the phase responses are within 10 degrees until 10,000 rad/s or 1.6 kHz where the digitized phase then tends indicate lower than actual.

As discussed previously, the three different large signal operating points result in unique small signal plant dynamics. All three plants feature a stable denominator characteristic equation, negative overall gain and a non-minimum-phase zero in the numerator. At no load the plant has the most un-damped second order response with the minimum phase zero far in the right hand plane. With increased loading and resulting duty cycle increase the response becomes increasingly damped and the right hand plane zero moves left and starts to play an increasing role in driving the phase down through 180 degrees. It is this non-minimum phase right hand plane zero that has the effect of significantly restricting the control bandwidth.

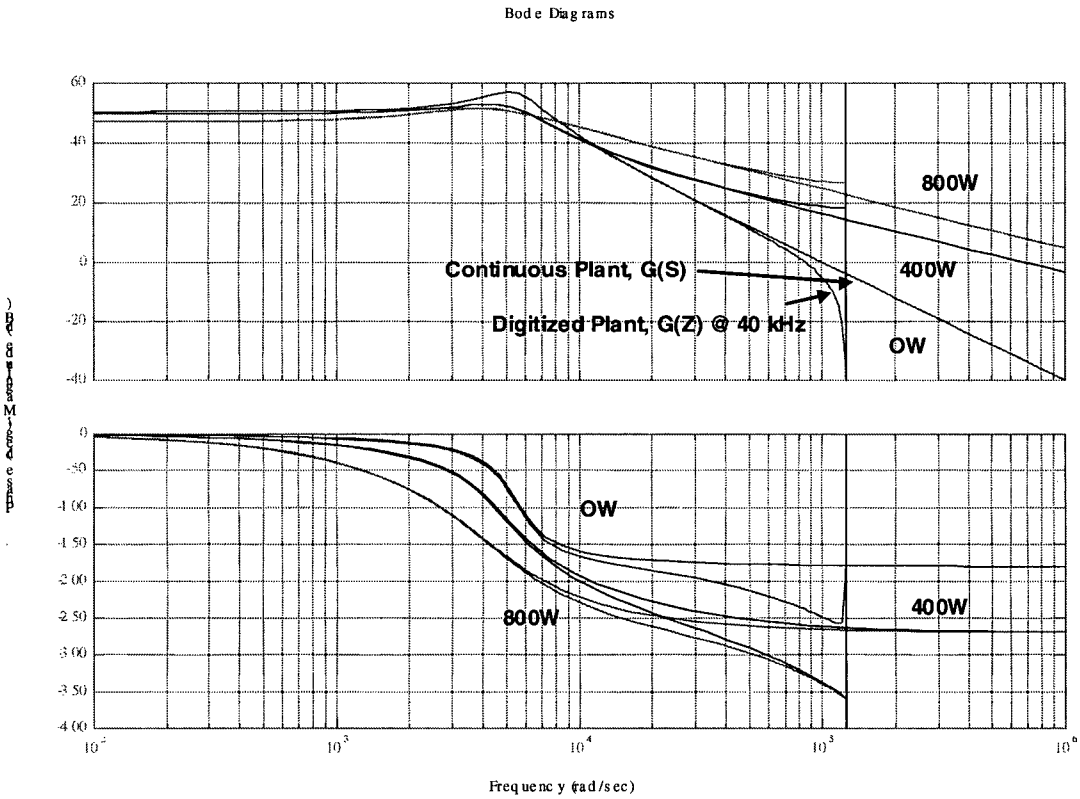


Figure 32: **Duty Cycle to Bus Voltage Small Signal Transfer Functions, $G_1(s)$, $G_1(z)$**

3.3.2.2 Control mode 1: PI compensation

The object of the dynamic compensation is to modify the open loop response of the plant to provide stable closed loop response with zero steady-state error and maximum control bandwidth. Ideally this can be achieved by creating a large open loop dc gain and manipulating system response to result in acceptable phase margin at as high a frequency as possible. Traditionally, a *proportional-integral* (PI) or similar *lag* type compensation is used to increase the dc gain and provide zero steady state error while leaving the phase margin unaffected. *Proportional-derivative* (PD) or *lead* type compensation can then be used to increase the gain at elevated frequencies while introducing a phase increase, or lead, to push the gain margin thereby increasing the control bandwidth. In addition to introducing noise sensitivity issues, derivative type compensation is not suitable for the systems of figure 31 as the control bandwidth cannot be pushed much further than the natural frequency of the plant where there is already adequate phase. In fact efforts were made to carefully manipulate the open loop system's response by the addition of multiple strategically placed poles and zeros in the compensator. However, the resultant performance increases were minimal and not considered worth the extra design and computational effort. The initial conclusion was that PI or possibly I type compensation is all that is required.

In the analog control world lag compensators have to be used to approximate the 1/s integration effect of the PI type control response. However, in the digital world PI type controllers can be emulated directly based on the PI equation of (3.3.10).

$$C(s) = \frac{K}{s}(s + \omega_b)$$

(3.3.10)

An elegant approach for compensating the plants of figure 32 is to first reduce the overall gain of the open loop system via K to yield 6dB of gain margin at the highest resonant peak, a frequency near to where the phase tends to cross 180 degrees. In the case of figure 31 this occurs with the unloaded loaded small signal plant model operating its natural frequency. The natural frequency can then also be selected as the break point, ω_b, to yield high dc gain, minimum overall gain margin of about 6dB and near maximum

phase margin for the entire range of large signal operation. The design process can be calculated in MATLAB according to (3.3.11).

```
eig_0W=eig(A_0W); %OBTAIN EIGENVALUES FROM STATE SPACE AVERAGED SYSTEM
characteristic_poly = poly(eig_0W); %OBTAIN SYSTEM CHARACTERISTIC POLYNOMIAL
undampednaturalfrequency = sqrt(characteristic_poly(3)); %CALCULATED NATURAL FREQ
G_dB = 20*log10(bode(G_S_0W,(undampednaturalfrequency))); %SOLVE FOR GAIN IN dB
K = 10^(-(G_dB+6)/20); %CALCULATE REQUIRED GAIN COMPENSATION
C_S = K*tf([1 undampednaturalfrequency],[1 0]); %DEFINE PI TRANSFER FUNCTNION
C_Z = c2d(C_S,Ts,'zoh') *TF([1],[1 0],Ts); %DISCRITIZE WITH 1/Z COMPUTATIONAL DELAY
K = .00726 and wb = 5477
```

(3.3.11)

The resulting s domain PI transfer function for the thesis converter is shown in equation 3.3.11.

$$C(S)=\frac{U(S)}{E(S)}=\frac{0.000726}{s}(s+5477)$$

(3.3.12)

and converted into the z domain using zero order hold emulation and the computational delay in equation 3.3.12

$$C(Z)=\frac{U(Z)}{E(Z)}=\frac{0.0007264\cdot z-0.0006269}{z-1}\cdot\frac{1}{z}$$

(3.3.13)

and further converted into the difference equation form suitable for direct digital control calculations in equation 3.3.14.

$$u([k+1]T)=u(kT)+0.0007264\cdot e(kT)-0.0006269\cdot e([k-1]T)$$

(3.3.14)

The addition of the *1/Z* computational delay in the digital emulation process allows for the time it takes the controller to sample the data, compute the control output and update the duty cycle. The compensated open loop analysis must include this delay effect. In the resulting difference equation the actual control output is not needed until the next iteration. If the computational delay is not included the result of the difference equation and the duty cycle update is required immediately. This is simply not possible. Note that controller memory is also required to store the single historical error term.

Even though the PI transfer function has been designed solely with the characteristics of the unloaded plant the actual worst case phase and gain margin situations occur with the fully loaded plant. For this reason it is necessary analyze the

open loop Bode plot of the system at maximum load to insure adequate stability margins. For the application of the thesis converter the large signal results using the PI compensator of equation 3.2.13 are listed in table 10.

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Watts	96, 1464	10
400 Watts	83, 1329	9
800 Watts	60, 1014	6

Table 10: Mode 1 PI Control: Large Signal Dependant Gain and Phase Margin

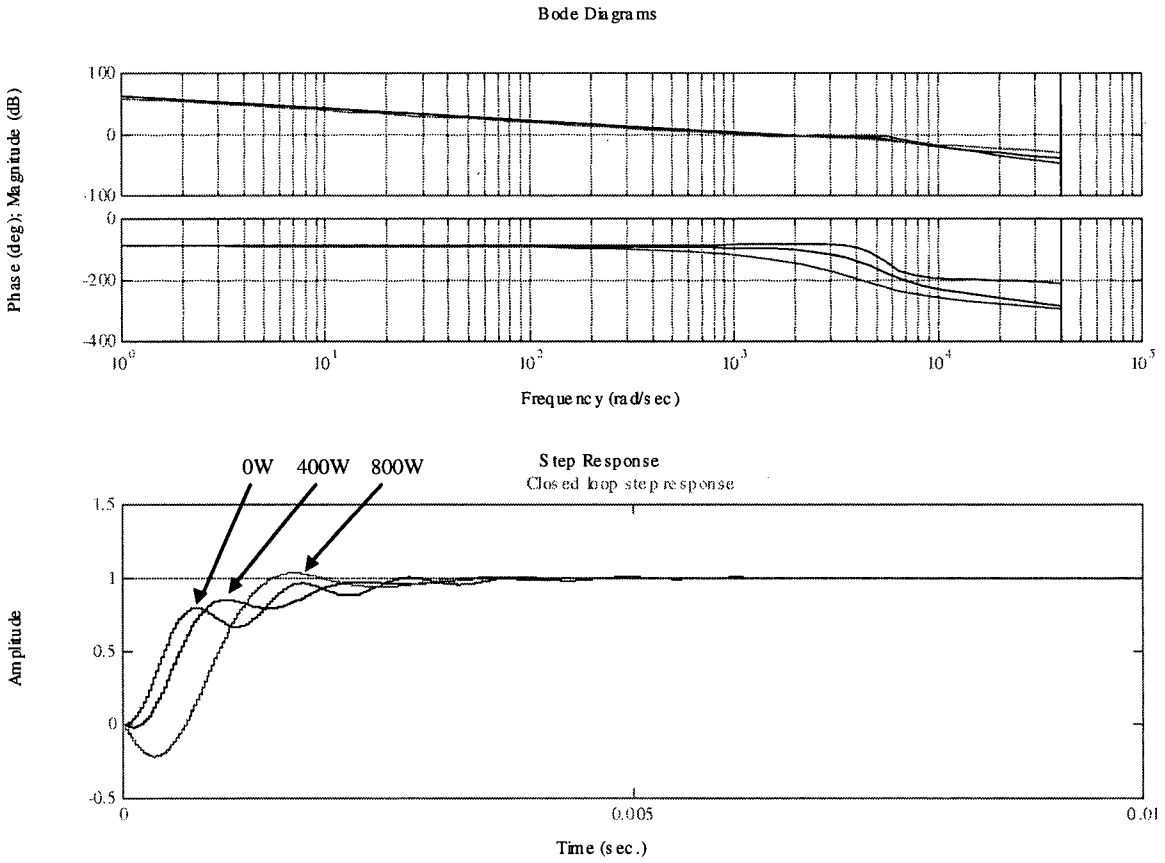


Figure 33: Control mode 1 PI control: open loop Bode and closed loop transient responses, $G_1(z)C_1(z)$

3.3.2.3 Control mode 1: I compensation

While studying the details of the PI compensator it became apparent that an even simpler control scheme was possible. The small signal plant transfer functions are inherently high gain in nature at dc and as a result no further dc gain is required. For this reason a simple integrator, I-type compensation of equation 3.3.15 can be implemented with gain selected to provide satisfactory open loop stability margin. When examined for use in thesis converter application the resulting phase margins and control bandwidth prove to be comparable to the PI control described above.

$$C(s) = \frac{K}{s}$$

Eq. 3.3.15

To select the gain coefficient, K, a similar process as described for the PI design can be utilized. The idea is to bring the natural frequency peak response of the purely integrated compensated system to 6 dB below unity gain to insure satisfactory control response. To do this the response of the integrated unloaded plant at its natural frequency is determined. The gain, K, is then calculated to position the entire response down to the appropriate level. The design approach is, again, outlined in the following MATLAB procedure of equation 3.3.16. It is similar to the PI approach but note the multiplication of the plant with the integrator before the gain is calculated. The performance results are displayed in table 11 and figure 34.

```
integrator = tf([1],[1 0]);  %DEFINE THE INTEGRATOR AS 1/S
characteristic_poly = poly(eig_0W);  %OBTAIN SYSTEM CHARACTERISTIC POLYNOMIAL
undampednaturalfrequency = sqrt(characteristic_poly(3)); %CALCULATED NATURAL FREQ
G_dB = 20*log10(bode(G_S_0W*integrator,(undampednaturalfrequency))); %EVALUATE-
THE INTEGRATED PLANT RESPONSE
K = 10^(-(G_dB+6)/20); %SOLVE FOR GAIN TO ACHEIVE -6dB AT THE NATURAL FREQUENCY
C_S = K*integrator;          %FORM THE OVERALL COMPENSATOR
C_Z = c2d(C_S,Ts,'zoh')

K = 3.978
```

(3.3.16)

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Watts	81, 1407	6
400 Watts	70, 1288	8
800 Watts	51, 994	5

Table 11: Mode 1 I Control: Large Signal Dependant Gain and Phase Margin

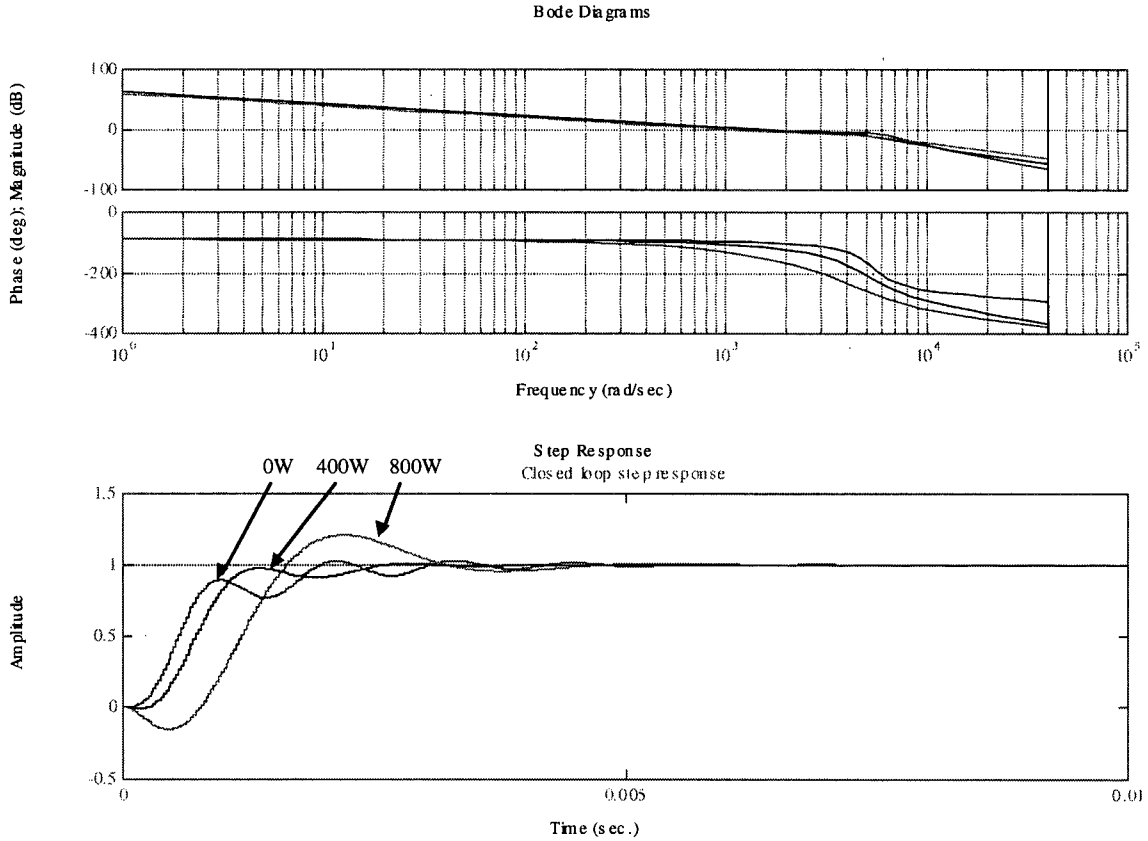


Figure 34: Control mode 1 I control: open loop Bode and closed loop transient responses, $G_1(z)C_1(z)$

Again, it is observed that the 800W loading produces the most marginal stability and conclude that the open loop system response analysis should be performed at full loading to insure complete operating range stability.

Note the absence of the 1/Z control delay in discrete emulation of the compensator in equation 3.3.16. The s domain integral only compensator function of equation 3.2.15 can be converted to its z domain digital counterpart but the following intuitive zero order hold integration process. At each sample instant the error input to the

compensator is known. The zero order hold process assumes the same error, *e(kT)*, for the duration sample interval and where the iterative process of calculating the new total integrated error is shown in equation 3.3.16 where T is the sampling interval and u is the control output and e is the error. The additional computational delay in this case is not required.

$$C(S) = \frac{U(S)}{E(S)} = \frac{K}{s} = \frac{3.978}{s} \tag{3.3.17}$$

$$u([k+1]T) = u(kT) + KTe(kT) \tag{3.3.18}$$

Specifically using the zero order hold integrator emulation strategy in this case over other methods is advantageous because it makes for a difference equation requiring no future terms or stored historical elements to calculate the output. This allows for a full sample period of computational time before the new integrated error control output, *u([k+1]T)*, is required and the resulting difference equation 3.3.18 is optimally simplified. Equation 3.3.18 can be converted into 3.3.19 via z transform and as a final check equation 3.3.19 yields the same results as the c2d MATLAB function of equation 3.3.20.

$$C(z) = \frac{U(Z)}{E(Z)} = \frac{KT}{z-1} = \frac{0.00009946}{z-1} \tag{3.3.19}$$

c2d(C_S,Ts,'zoh') =
Transfer function:
9.946e-005
----
z - 1
sample interval = 25us

(3.3.20)

In this section the development of a digital control system for regulating the dc bus has been developed. Initially the feedback control system configuration was specified and a design process outlined. As part of the controller development the large signal variation in the small signal plant model was examined. A PI type open-loop compensation was then derived and further simplified into pure integral control. In both cases the proposed designs used solely information from the unloaded plant model to

blindly calculate a suitable compensator transfer function. However, when implemented across the range of large signal operation the fully loaded plant was found to be the least stable. For this type of variable load voltage regulation control the fully loaded small signal model should be used when evaluating the open loop Bode plot for gain and phase margin stability indicators. Alternatively, the gains, K, can be determined graphically using the small signal plant corresponding with the maximum load and by vertically positioning the open loop gain to achieve the minimum gain or phase margin. The simplified integrator control approach was lastly converted into a discrete version suitable for computation by a DSP based control system.

3.3.3 Open loop dynamic compensation for control mode 2

For constant current charge mode 2 operation a similar approach to the one outlined in section 3.3.2 is used to analyze the closed loop stability of the power circuit. First the large signal varying small signal plant models are presented and analyzed. Next a dynamic compensator to insure closed loop stability over the large signal operation is derived. It is shown that the large signal variation does not pose as significant of a concern as for the bus voltage regulation of control mode 1.

3.3.3.1 Control mode 2: small signal plant representations

The component values used for the actual thesis converter in charge mode are again as follows:

```
% GIVEN POWER CIRCUIT INFORMATION
clear;
Ts =    .000025;    %sampling interval for digital emulation
L1=     20e-6;      %inductor value in Henerys
C1=     6e-6;       %dc bus capacitor in Farads
Rbat =  .0025;      %Battery Internal Resistance
R1 =    .040;       %RDSon of the low voltage switches and board copper
R2  =   .050;       %RDSon of the high voltage switches and board copper
N =     10;         %transformer turns ratio
```

(3.3.21)

Again, the small-signal transfer functions can be calculated using equations 3.2.9 through 3.2.11. Three small signal models are again derived around three large signal operating points to investigate the large signal behavior. Three large signal reference points are used for the charge control analysis: no load, 30A and 60A charge currents. In each of the three cases the difference between the bus voltage and internal battery voltage determines the large signal operating point.

For no load operation:

```
% 0A LOAD LARGE SIGNAL PARAMETERS
VDC =       250;        %Load Resistance
VBAT =      14;         %Battery Voltage
D =         .44;        %Duty Cycle required for OA Charge

Large Signal Operating Point  =-5.9955e-014 A

 Transfer function:
1.25e006                          POLES =
--------                          -1699
s + 1699
```

(3.3.22)

For 30A charge operation:

```
% 30A CHARGE LARGE SIGNAL PARAMETERS
VDC =      250;      %Load Resistance
VBAT =     12;       %Battery Voltage
D =        .50;      %Duty Cycle required for 200V Bus

Large Signal Operating Point =-30.1568 A

 Transfer function:                    POLES =
1.25e006                               -1658
--------
s + 1658
```

(3.3.23)

For 60A charge operation:

```
% 60A CHARGE LARGE SIGNAL PARAMETERS
VDC =      250;      %Load Resistance
VBAT =     10;       %Battery Voltage
D =        .52;      %Duty Cycle required for 200V Bus

Large Signal Operating Point = -61.8429 A

 Transfer function:                    POLES =
1.25e006                               -1617
--------
s + 1617
```

(3.3.24)

The Bode plot of the three plant transfer functions and their digitized counterparts can be found in figure 35. The analog and digital systems have again been plotted on top of each other to visually indicate the digitization effects.

During charge current regulation the effects of large signal variation in the plant model are not as significant as compared to mode 1 discharge bus regulation. This is mainly due to the following facts: the duty cycle is not required to vary as much and the system is now only first order and there is no non minimum phase zero. The duty cycle variation is minimized because of the high gain duty cycle to charge current relationship.

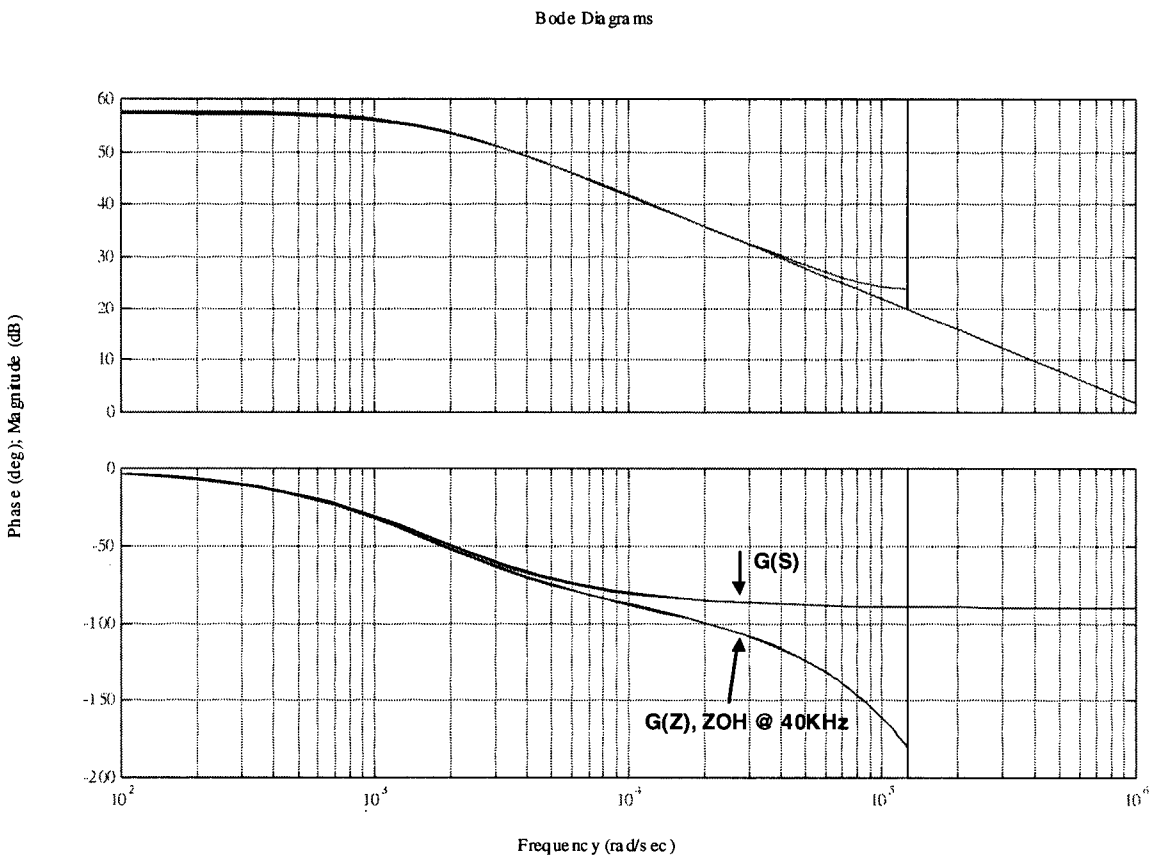


Figure 35: Duty Cycle to Charge Current Small Signal Transfer Functions, $G_2(s)$, $G_2(z)$

3.3.3.2 Control mode 2: PI compensation

It can be seen in figure 35 that the closed loop control bandwidth of this plant can be made much faster than that of the discharge regulator. However, it is important to keep in mind that the control bandwidth must be kept to at least an order of magnitude lower than the sampling and switching frequencies – which, in case of the thesis converter, are one and the same at 40kHz. The dynamic compensator must again provide zero steady state error while also maximizing, as much as practically allowed, the control bandwidth. To accomplish this, the break point of a PI controller can be set to the corner frequency of the plant response. In the case of figure 34 this is closely 1K rad/s. This has the effect of virtually flattening out the phase to -90 degrees across the entire spectrum and also provides a virtually linear first order open loop gain attenuation of 20dB per decade. In this way gain margin is not an issue as the phase never crosses 180 degrees. As a result the unity gain cross-over point and associated phase margin could be pushed infinitely high in frequency by increasing the overall system gain. Of course with the practical system there is a constraint to keep the unity gain crossover point to less than, say, a twentieth of the sampling or switching frequency which, in the case of the thesis converter, is close to 10K rad/s. The proposed design procedure is to specify the break point frequency of equation 3.3.23 as 1K rad/s and solve for K by making the unity gain cross over at 10K rad/s.

The following MATLAB sequence can be used to accomplish this:

```
G_dB = 20*log10(bode(G_S_0W,(10000))); %FIND GAIN OF PLANT AT 1/20 Fs
K = 10^(-(G_dB)/20); %FIND K TO ACHEIVE UNITY GAIN AT 1/20 Fs
C_S = K*tf([1 1000],[1 0])%SPECIFY PI COMPENSATOR WITH 1000 rad/s BREAK POINT
C_Z = c2d(C_S,Ts,'zoh') *TF([1],[1 0],Ts);  %DISCRITIZE WITH 1/Z COMPUTATIONAL DELAY
K = 0.0081
```

(3.3.23)

The resulting s domain compensator is found in equation 3.3.24.

$$C(S) = \frac{U(S)}{E(S)} = \frac{K}{s}(s+\omega_b) = \frac{0.0081}{s}(s+1000)$$

(3.3.24)

The zero order held discrete emulation including computational delay is found in equation 3.3.25

$$C(Z) = \frac{U(Z)}{E(Z)} = \frac{0.008115 \cdot z - 0.007912}{z - 1} \cdot \frac{1}{z}$$

(3.3.25)

And finally the difference equation is formed in equation 3.3.26.

$$u([k+1]T) = u(kT) + 0.008115 \cdot e(kT) - 0.007912 \cdot e([k-1]T)$$

(3.3.26)

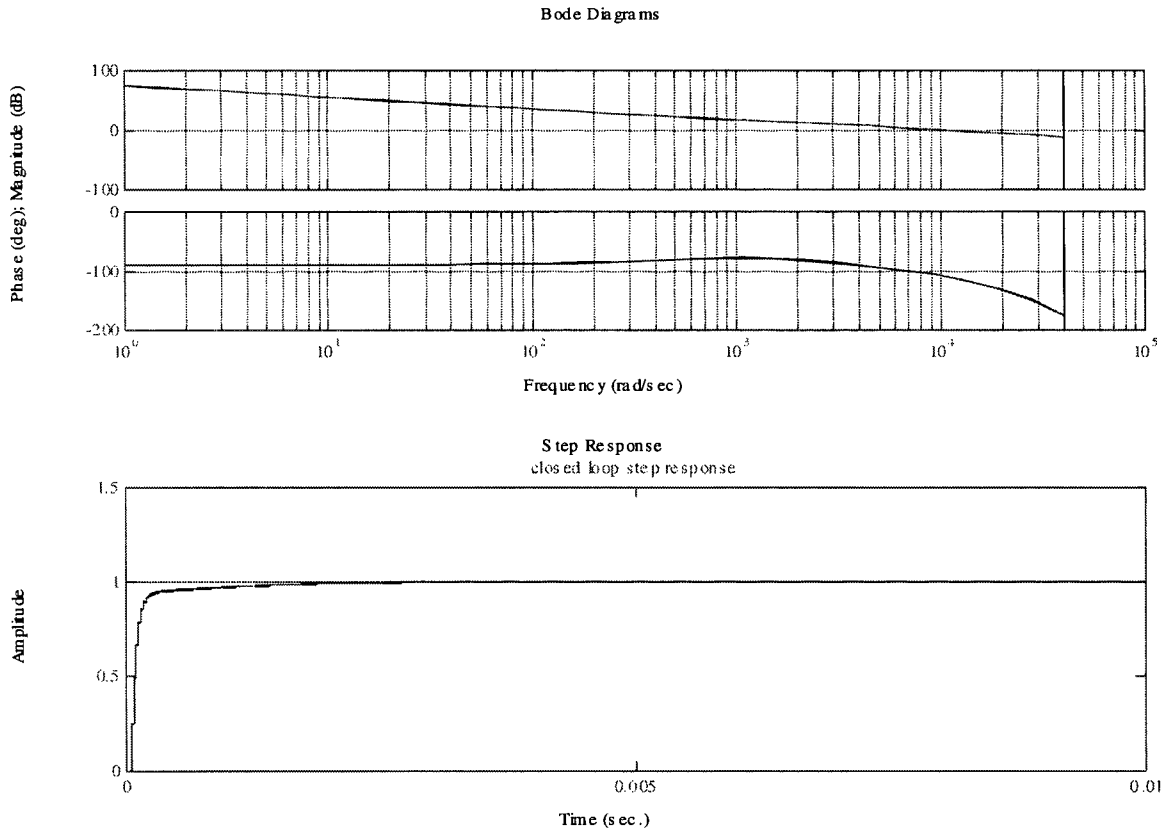


Figure 36: Control mode 2, PI compensation: open loop Bode and closed loop transient responses, $G_2(z)C_2(z)$

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Amps	73, 10064	12
30 Amps	73, 10064	12
60 Amps	73, 10064	12

Table 12: Mode 2 PI control: Large Signal Dependant Gain and Phase Margin

3.3.3.3 Control mode 2: I compensation

It is also possible to perform mode 2 control with a pure integral controller. The control bandwidth is significantly reduced but nonetheless a functional controller with zero steady state error is achieved. The same approach developed in section 3.3.2.3 is used to calculate the integral gain coefficient.

Again, MATLAB can be used calculate the mode 2 integral gain.

```
integrator = tf([1],[1 0]); %DEFINE THE INTEGRATOR AS 1/S
G_dB = 20*log10(bode(G_S_0W*integrator,(1500)));
K = 10^(-(G_dB+6)/20);
C_S = K*integrator
C_Z = c2d(C_S,Ts,'zoh');

K = 1.63
```

(3.3.27)

In equation 3.3.27 the gain was calculated to give -6bB at 1500 rad/s. This was manually found to be the frequency that provided the largest control bandwidth while maintaining the stability margins. It also represents approximately 1.5 times the break point frequency of the 1st order small signal plant model. The resulting s-domain compensator appears in equation 3.3.28

$$C(S) = \frac{U(S)}{E(S)} = \frac{K}{s} = \frac{1.363}{s}$$

(3.3.28)

and converted into z-domain using ZOH at 40kHz in equation 3.3.29

$$C(z) = \frac{U(Z)}{E(Z)} = \frac{KT}{z-1} = \frac{0.00003408}{z-1}$$

(3.3.29)

and finally converted into difference equation form in equation 3.3.30. Note the computational delay is not required.

$$u([k+1]T) = u(kT) + 0.00003408e(kT)$$

(3.3.30)

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Amps charging	61, 897	32
30 Amps charging	61, 897	32
60 Amps charging	61, 897	32

Table 13: Mode 2 I Control: Large Signal Dependant Gain and Phase Margin

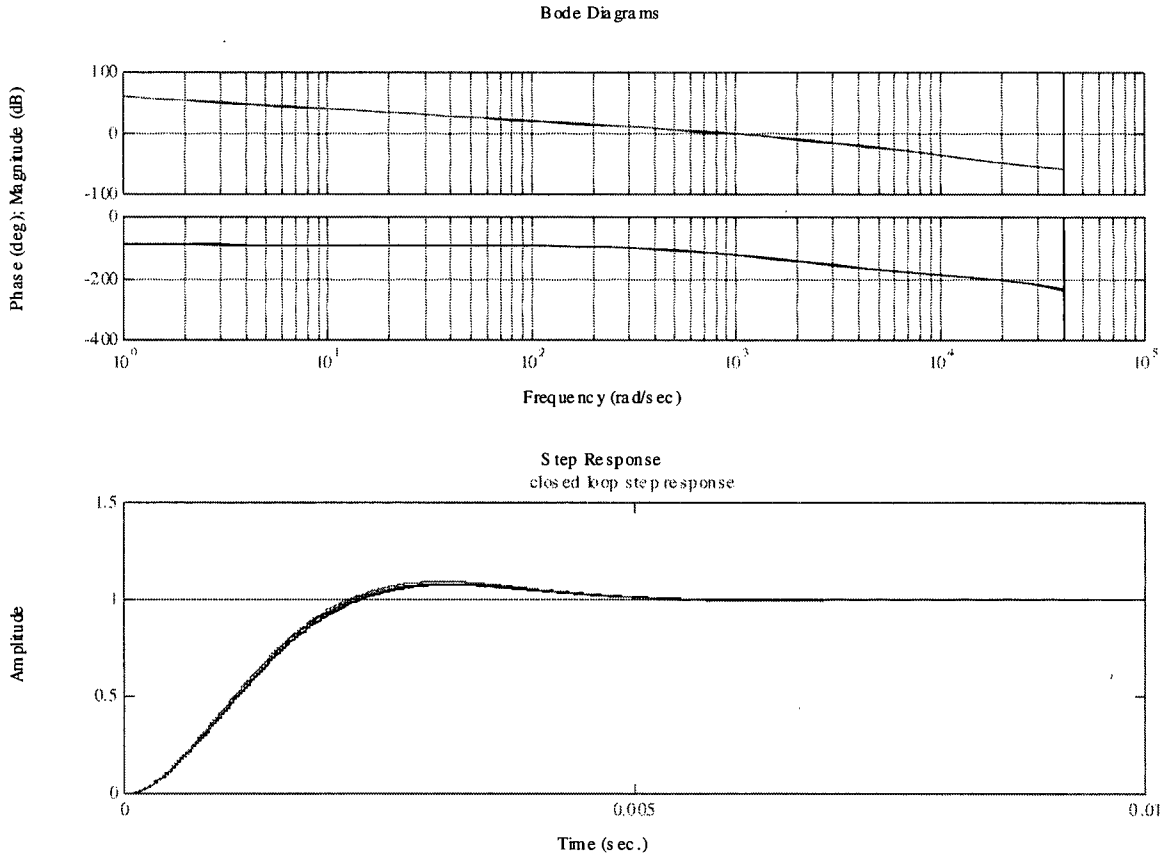


Figure 37: Control mode 2 I control: open loop Bode and closed loop transient responses, $G_2(z)C_2(z)$

3.3.4 Open loop dynamic compensation for control mode 3

For constant voltage charge operation a similar approach to the ones previously outlined in sections 3.2.2 and 3.2.3 is used to analyze the closed loop stability of the power circuit. First the large signal varying small signal plant models are presented and analyzed. Next a dynamic compensator to insure closed loop stability over the large signal operation is derived. It is shown that the large signal variation does not pose a significant concern in constant voltage charge mode 3 as the duty cycle variation is virtually non-existent.

3.3.4.1 Control mode 3: small signal plant representations

The component values used for the actual thesis converter in charge mode are again as follows:

```
% GIVEN POWER CIRCUIT INFORMATION
clear;
Ts =    .000025;    %sampling interval for digital emulation
L1=     20e-6;      %inductor value in Henerys
C1=     6e-6;       %dc bus capacitor in Farads
Rbat =  .0025;      %Battery Internal Resistance
R1 =    .040;       %RDSon of the low voltage switches and board copper
R2  =   .050;       %RDSon of the high voltage switches and board copper
N =     10;         %transformer turns ratio
```

(3.3.31)

Again, it is possible to calculate the small signal transfer function using equations 3.2.9 through 3.2.11. Three small signal models are again derived to around three large signal operating points to investigate the large signal behavior. Three large signal reference points are used for the constant voltage charge control analysis: no load, 15A and 30A charge currents. In each of the three cases the difference between the bus voltage and internal battery voltage determines the large signal operating point. It is important to make the distinction at this point that the object is to control the terminal voltage of the battery and not the internal voltage. The terminal voltage is calculated as *Vbat - IRbat.* The highest dc bus voltage is used in the analysis as it produces the largest and therefore worst case small signal gains.

<u>For no load operation:</u>

```
% 0A LOAD LARGE SIGNAL PARAMETERS
```

```
VDC =      250;      %Load Resistance
VBAT =     14;       %Battery Voltage
D =        .44;      %Duty Cycle required for OA Charge

Large Signal Operating Point  =-5.9955e-014 A

 Transfer function:
-3125                          POLES =
--------                             -1699
s + 1699
```

(3.3.32)

For 15A charge operation:

```
% 15A CHARGE LARGE SIGNAL PARAMETERS
VDC =      250;      %Load Resistance
VBAT =     13.5;     %Battery Voltage
D =        .44;      %Duty Cycle required for 200V Bus

Large Signal Operating Point =-14.7145 A

 Transfer function:                  POLES =
-3087                                -1699
--------
s + 1699
```

(3.3.33)

For 30A charge operation:

```
% 30A CHARGE LARGE SIGNAL PARAMETERS
VDC =      250;      %Load Resistance
VBAT =     13;       %Battery Voltage
D =        .44;      %Duty Cycle required for 200V Bus

Large Signal Operating Point = -29.4291 A

 Transfer function:                  POLES =
-3050                                -1699
--------
s + 1699
```

(3.3.34)

The Bode plot of the three plant transfer functions and their digitized counterparts is found in figure 38. Again, the analog and digital systems have again been plotted on top of each other to visually indicate the digitization effects. During battery terminal voltage regulation the effects of large signal variation in the plant model are not as significant as compared to voltage discharge mode 1 regulation. This is mainly due to the following facts: the duty cycle is not required to vary, the system is now only first order and the non minimum phase zero is absent. The duty cycle variation is of course minimized because of the constant voltage conversion ratio of the power circuit. This can be seen by the fixed pole locations for the variation in charge currents. The voltage control mode 3 plant of figure 37 shows a dramatic reduction in gain response and a phase shift of 180 degrees due to the effect of the voltage drop across *Rbat* in turn due to

the in phase battery current to duty cycle relationship. This will of course be accounted for in the compensator design.

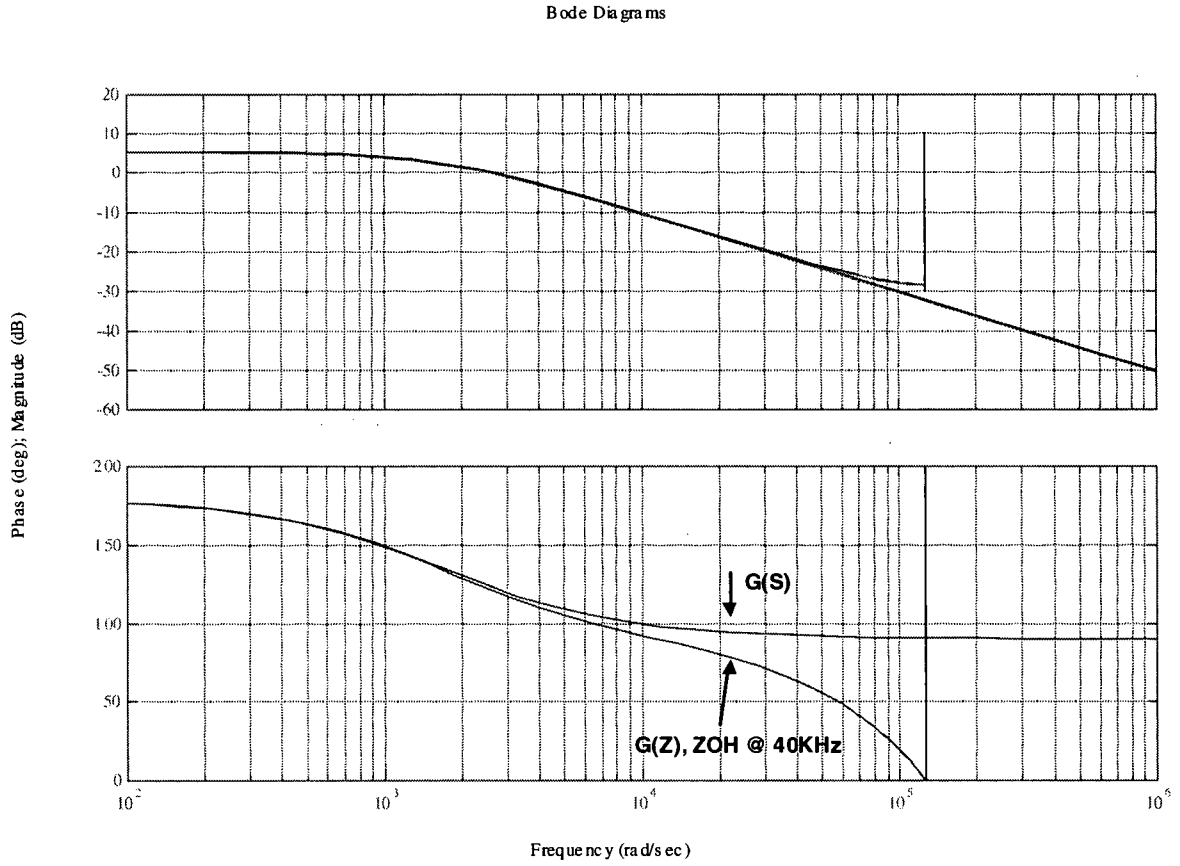


Figure 38: Duty Cycle to Charge Current Small Signal Transfer Functions, $G_3(s)$, $G_3(z)$

3.3.4.2 Control mode 3: PI compensation

Again it can be seen in figure 38 that due to the -180 degree maximum phase the closed loop control bandwidth of the mode three plant can be made much faster than that of the mode 1 discharge voltage regulator. However, it is important to keep in mind that the control bandwidth must be set at least an order of magnitude lower than the sampling and switching frequencies – which, in the case of the thesis converter, are one and the same at 40kHz. As with control modes 1&2 the dynamic compensator must again provide zero steady state error while also maximizing, as much as practically allowed, the control bandwidth. For mode 3 the suitable PI control design process is the same procedure as developed for the mode 2 controller. This procedure has been previously described in detail in section 3.3.3.2. However, it has been modified slightly to compensate for the negative gain effect of the duty cycle to terminal voltage small-signal transfer function, $G_3(S)$.

The following MATLAB sequence is used to determine the compensator characteristics

```
G_dB = 20*log10(bode(G_S_0W,(10000)));%FIND GAIN OF PLANT AT 1/20 Fs
K = -10^(-(G_dB)/20);%FIND K AND NEGATE TO ACHEIVE UNITY GAIN AT 1/20 Fs and 180 DEG SHIFT
C_S =K*tf([1 1000],[1 0])%SPECIFY PI COMPENSATOR WITH 1000 rad/s BREAK POINT
C_Z = c2d(C_S,Ts,'zoh') *TF([1],[1 0],Ts);  %DISCRITIZE WITH 1/Z COMPUTATIONAL DELAY
K = -3.2459
```

(3.3.35)

The resulting s domain compensator is found in equation 3.3.24.

$$C(S)=\frac{U(S)}{E(S)}=\frac{K}{s}(s+\omega_b)=\frac{-3.2459}{s}(s+1000)$$

(3.3.36)

The zero order held discrete emulation including computational delay is found in equation 3.3.25

$$C(Z)=\frac{U(Z)}{E(Z)}=\frac{-3.246\cdot z+3.165}{z-1}\cdot\frac{1}{z}$$

(3.3.37)

And finally the difference equation is formed in equation 3.3.26.

$$u([k+1]T) = u(kT) - 3.246 \cdot e(kT) + 3.165 \cdot e([k-1]T)$$

(3.3.38)

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Amps charging	73, 9800	12
15 Amps charging	73, 9800	12
30 Amps charging	73, 9800	12

Table 14: Mode 3 PI control: Large Signal Dependant Gain and Phase Margin

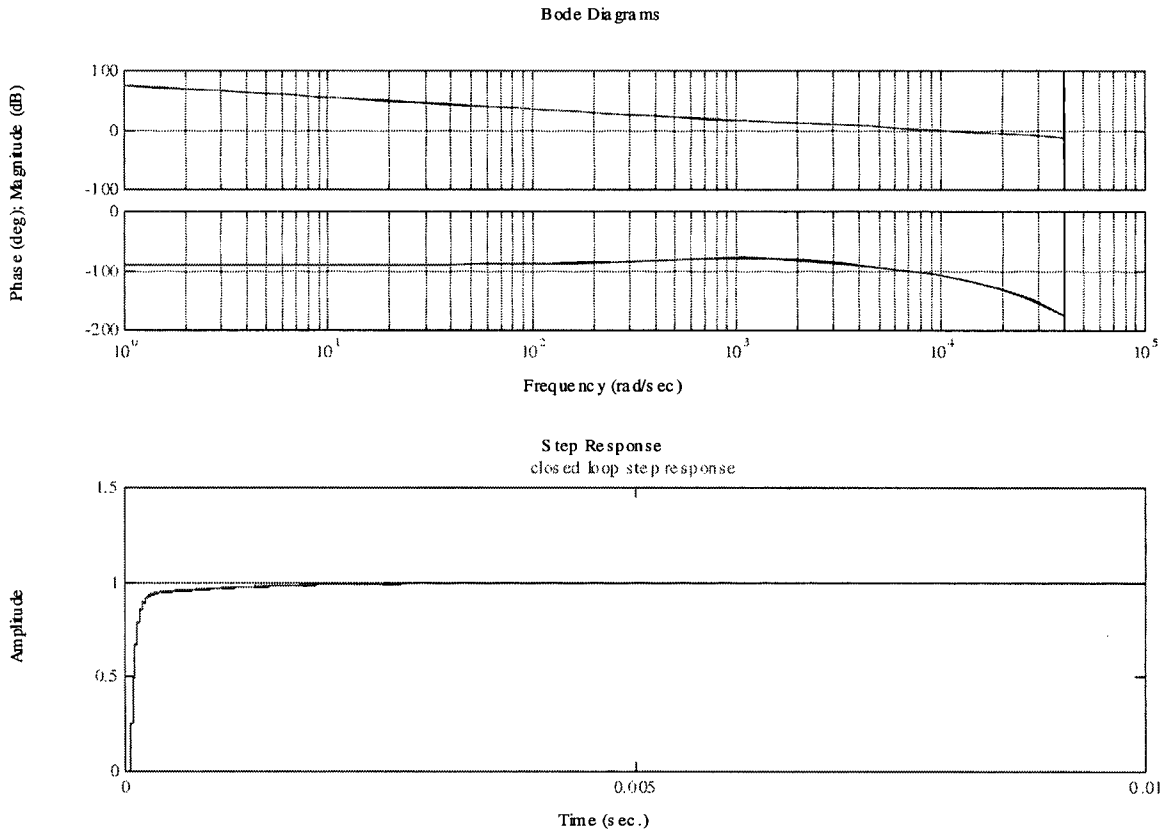


Figure 39: Control mode 3, PI compensation: open loop Bode and closed loop transient responses, $G_3(z)C_3(z)$

3.3.4.3 Control mode 3: I compensation

It is also possible to perform mode 3 control with a pure integral controller. The control bandwidth is significantly reduced but nonetheless a functional controller with zero steady state error is achieved. The same approach developed in section 3.3.2.3 is used to calculate the integral gain coefficient.

Again, MATLAB can be used calculate the mode 3 integral gain:

```
integrator = tf([1],[1 0]); %DEFINE THE INTEGRATOR AS 1/S
G_dB = 20*log10(bode(G_S_0W*integrator,(1500)));
K = 10^(-(G_dB+6)/20);
C_S = K*integrator
C_Z = c2d(C_S,Ts,'zoh');

K = -545.2
```

(3.3.39)

In equation 3.3.27 the gain was calculated to give -6bB at 1500 rad/s. This was manually found to be the frequency that provided the largest control bandwidth while maintaining the stability margins. It also represents approximately 1.5 times the break point frequency of the 1st order small-signal plant model. The resulting s-domain compensator appears in equation 3.3.40

$$C(S) = \frac{U(S)}{E(S)} = \frac{K}{s} = \frac{-545.2}{s}$$

(3.3.40)

and converted into z-doman using ZOH at 40kHz in equation 3.3.41

$$C(z) = \frac{U(Z)}{E(Z)} = \frac{KT}{z-1} = \frac{-0.01363}{z-1}$$

(3.3.41)

and finally converted into difference equation form in equation 3.3.42. Note the computational delay is not required.

$$u([k+1]T) = u(kT) - 0.01363e(kT)$$

(3.3.42)

Large Signal Loading	Phase Margin (deg, rad/s)	Gain Margin (dB)
0 Amps charging	63,870	32
15 Amps charging	63,870	32
30 Amps charging	63,870	32

Table 15: Mode 3 I Control: Large Signal Dependant Gain and Phase Margin

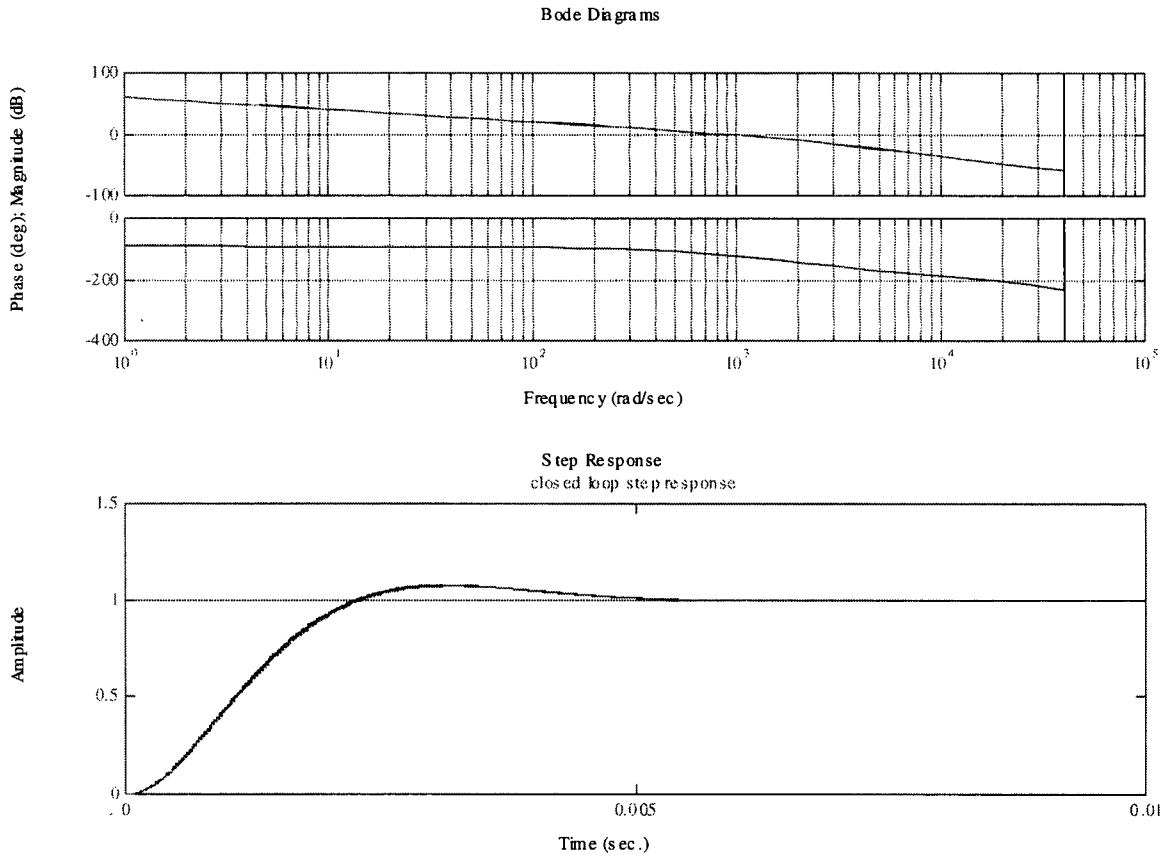


Figure 40: Control mode 3 I control: open loop Bode and closed loop transient responses, $G_3(z)C_3(z)$

3.3.5 Digital control compensator summary

Chapter three has explored the design of three separate closed loop discrete time controllers for the three individual control modes of the power circuit. In section 3.3.2, while developing the initial mode 1 controller, the application of PI compensation was explored with respect to the power circuit models. A digital PI control scheme suitable for the power circuit was justified and developed using small signal plant models at varying operating points. The fully loaded plant was determined to be the hardest to stabilize. To insure stability the fully loaded small signal model should be used for the compensator design. Additionally, while designing a suitable PI controller it was determined that a single I controller could achieve similar results with less computational effort. Similar analysis was performed to develop additional PI and I conpensators for control modes 2 and 3. However, for modes 2 and 3 implementing the I control resulted in a significant decrease in control bandwidth as compared to the PI control. The resulting compensator designs suitable for the three digital controllers outlined in figure 24 can be found in tables 16 and 17.

The computationally less intensive but slower charge mode response I compensation was used within the DSP based thesis converter experimental prototype. The I controller's ease of implementation is felt to be more significant than the response speed of the PI controller for the thesis charger/discharger application. The I controller has a response time of about 5ms in both charge modes which is felt to be acceptable.

Control Mode	**Z-domain PI compensators including 1/Z computational delay Ts = 25us**	**Worst Case Phase Margin Degrees, Radians/s**	**Worst Case Gain Margin dB**
Mode 1 $C_1(Z)$	$C(Z)=\frac{U(Z)}{E(Z)}=\frac{0.0007264\cdot z-0.0006269}{z-1}\cdot\frac{1}{z}$	51, 1014	5
Mode 2 $C_2(Z)$	$C(Z)=\frac{U(Z)}{E(Z)}=\frac{0.008115\cdot z-0.007912}{z-1}\cdot\frac{1}{z}$	73, 10000	12
Mode 3 $C_3(Z)$	$C(Z)=\frac{U(Z)}{E(Z)}=\frac{-3.246\cdot z+3.165}{z-1}\cdot\frac{1}{z}$	73, 9800	12

Table 16: Digital PI compensator summary

Control Mode	Z-domain I compensators computational delay not required Ts = 25us	Worst Case Phase Margin Degrees, Radians/s	Worst Case Gain Margin dB
Mode 1 $C_1(Z)$	$C(z)=\frac{U(Z)}{E(Z)}=\frac{0.00009946}{z-1}$	51, 994	5
Mode 2 $C_2(Z)$	$C(z)=\frac{U(Z)}{E(Z)}=\frac{0.00003408}{z-1}$	61, 897	32
Mode 3 $C_3(Z)$	$C(z)=\frac{U(Z)}{E(Z)}=\frac{-0.01363}{z-1}$	63,870	32

Table 17: Digital I compensator summary

Chapter 4 - Large-signal simulation of the controlled system

Chapter three of this thesis discusses the small-signal behavior of the power circuit at various large-signal operating points. As a result of the discussion there, digital feedback controllers have been designed to insure small signal stability at the worst case large-signal operating points - one feedback controller for each of the three modes of operation. However, the large-signal transient behavior of the DSP controlled system remains somewhat a mystery. The controller designs and frequency domain stability analysis of chapter three were performed with respect to small-signal variations in a reference set point only. Although this insures small-signal closed loop stability the large-signal transient responses to real life changes in circuit operating conditions (loading, duty cycle etc.) require further investigation to insure acceptable transient response and stability.

In addition to investigating large-signal transient behavior of the power circuit, the numerical effects of the digital controller also need to be considered. The resolution of the A/D converters, the number of quantized duty cycle steps between 0 and 1 and the computational bus width of the controller all affect the ability of the DSP to smoothly regulate and control the power circuit.

To ensure large-signal stability and to investigate the numerical effects of the DSP it is of interest to develop a detailed simulation model of the controlled power circuit. A discrete-time computer-based transient time simulator can quickly explore large-signal power circuit operation, investigate sampling rates, model duty cycle quantization effects and confirm proposed controller algorithms all before the power circuit is physically constructed. While transient time electric circuit simulators are nothing new, most are unsuitable for modeling digitally controlled switch mode power supply circuits. This is mainly because traditional circuit simulators such as PSpice and PSIM require cumbersome small time step intervals to model the highly discontinuous switching power circuit operation. Additionally, traditional circuit simulators are not designed to easily model the numerical considerations of sampling digital controllers.

To address the issues described above a proposed bilateral simulation system model is presented in figure 41. To efficiently model the power-circuit the non-linear

state-space averaged model previously developed in section 3.2.1 is utilized. This averaged model can be simulated at a much lower sampling rate as compared to the multiple switching state power circuit. To control the duty cycle the power circuit model is fed by separate model of the DSP controller that includes the numerical considerations described above. Computer simulation of this system can be iterated at the controller sampling frequency rather than approximately 100 times the switching frequency as would be required by a cycle by cycle simulation of the switching power circuit. The fundamental advantages of the proposed method as compared to traditional circuit simulators are faster simulation times and a significantly reduced chance of experiencing the non-convergence simulation errors common to non averaged simulation of switching power circuits. The proposed model is also valid for complete non-linear bilateral operation. All possible input parameter variations directly alter the state matrices of the system providing a constantly evolving plant model that includes the large-signal effects of changes in load, R, duty-cycle, D, and other plant variations.

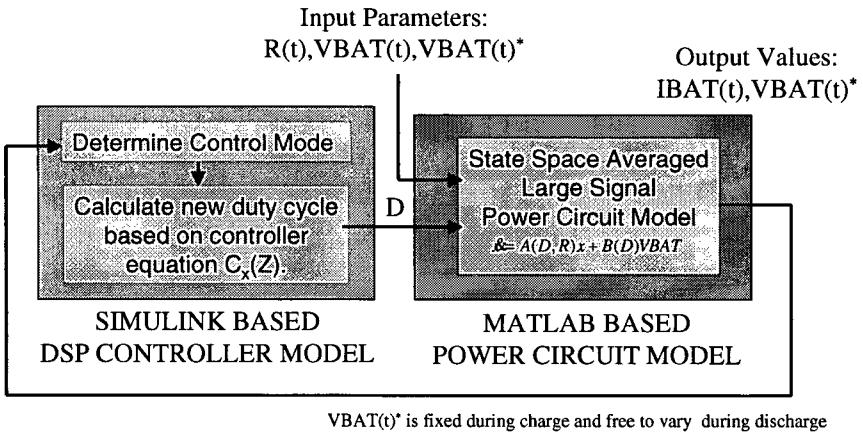


Figure 41: Proposed power circuit modeling approach

This chapter will show how the MATLAB environment can be conveniently used as a stable simulation platform for modeling transient circuit behavior as proposed by figure 41. Initially it will be shown how the state-space averaged power circuit model can be digitized for discrete time simulation. The graphical programming arm of MATLAB, SIMULINK, will then be used as a platform to model and develop the DSP controller specifically including its numerical limitations. Finally, the closed loop transient circuit operation will be simulated within MATLAB to investigate large signal behavior, the effects of digital control on the converter's ability to regulate the appropriate output and to generally validate the proposed multi-mode control concept.

4.1 Discrete time state space power-circuit model for large signal bilateral operation

To perform a discrete-time computer simulation with the state-space averaged plant model it is necessary to first have the model in a discrete time form. This section outlines the process used to generate the discrete time plant model from the continuous time state space averaged model developed chapter 3. In the next section MATLAB will be used as a simulation environment to validate the derived large signal simulation model against some acquired large signal experimental test data. Upon comparison the simulated results generally prove to be in very close agreement with the experimental data.

The continuous time state space averaged representation of the power circuit is again presented in (4.1.1).

$$[\dot{x}] = [A(D,R)]\cdot[x] + [B(D)]\cdot u \tag{4.1.1}$$

The system of (4.1.1) can be discretized according to (4.1.2) where T is the sampling frequency and the sampled input, u_i, is constant or zero order held from each sampling instance [38].

$$[x]_{i+1} = e^{[A(D,R)]T}\cdot[x]_i + [A(D,R)]^{-1}\left[e^{[A(D,R)]T} - I\right]\cdot[B(D)]\cdot u_i \tag{4.1.2}$$

and for simplicity (4.1.2) can be represented as (4.1.3) where ***Ad*** and ***Bd*** can be described as the discrete time state matrices.

$$[x]_{i+1} = [Ad][x]_i + [Bd]\cdot u_i \tag{4.1.3}$$

Equation (4.1.3) is an easy to compute iterative equation that provides the next state values of the output voltage and inductor current based on the current values and the digital state matrices ***Ad*** and ***Bd***. The complicated matrix exponential dependent equation of (4.1.2) can be conveniently computed in MATLAB by the single line command of (4.1.4) to yield the discrete time matrices required for (4.1.3)

```
[Ad,Bd,Cd,Dd] = c2dm(A,B,C,D,T,'zoh');
```

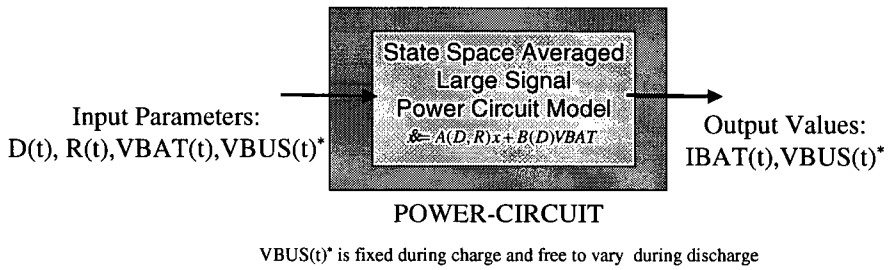
(4.1.4)

where T in (4.1.2) and (4.1.4) is the sampling interval and where the next iteration of state values can be calculated according to (4.1.5).

```
x(i+1) = Ad*x(i) + Bd*u(i)
```

(4.1.5)

4.1.1 Large signal power-circuit simulation algorithm using MATLAB



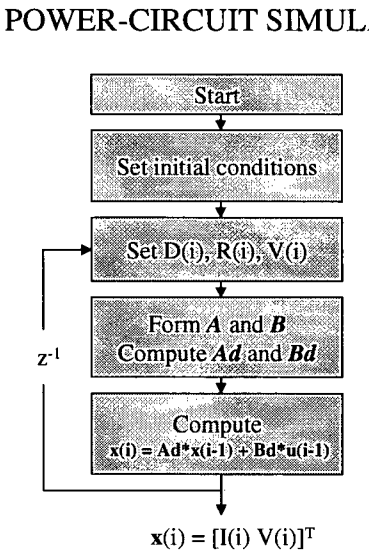


Figure 42: MATLAB based discrete time large signal open loop simulation of the power circuit

As mentioned in the previous section, MATLAB can be utilized to conveniently compute the discrete time transient response. To ensure the validity of the discrete time model the results of the proposed MATLAB based transient simulation algorithm based on figure 42 are compared to experimental results measured directly from the thesis

converter. The object of this experiment is to observe and compare the simulated and measured transient responses of the power circuit to step changes in duty-cycle under various loading conditions. These dynamic responses are of particular interest because the power circuit response is non-linear with respect to changes in duty cycle and load. It is clear from the A matrix of the plant model that the eigenvalues and hence the dynamic response of the converter circuit are non-linear and functions of D and R e.g. A(D,R).

MATLAB can be used to model the power-circuit complete with step changes in the load or duty cycle by implementing the following simulation algorithm which is also described by figure 42.

1. **Set initial conditions for x,**
2. **Update D to reflect change in duty cycle**
3. **Update R to reflect change in load**
4. **Update V if necessary**
5. **Calculate Ad(D,R,T) and Bd(D,R,T)**
6. **Compute x_{i+1} using (3.1.5)**
7. **Branch to 2 for (Simulation-Length/T) iterations**

The simulated responses of figure 43 were produced using the following simulation parameters derived from the prototype converter. A full MATLAB program listing is found in Appendix K.

N=10
Vbatt = 12
Rint = 2.5 mOhm
L1=13uH
C1=1uF
R1= 40 mOhm
R2= 120 mOh

It can be clearly observed in the simulated results of figure 43 that the 2nd order dynamic response of both output voltage and inductor current increases significantly in frequency with a decrease in duty cycle thus confirming the non-linear plant variation of the power circuit. Furthermore the response becomes increasingly damped with an increase in load. It is worth noting here that without the damping effects of the battery internal resistance and the switching device losses (and the other power circuit losses

included in R1 and R2) the states would oscillate indefinitely with a step change in duty cycle. More significantly, it is not the battery internal resistance that provides the majority of the damping – it is actually R1 and R2. This suggests that more attention may be required of these values as they are often neglected in the state-space averaged switching models although they appear important to the system response.

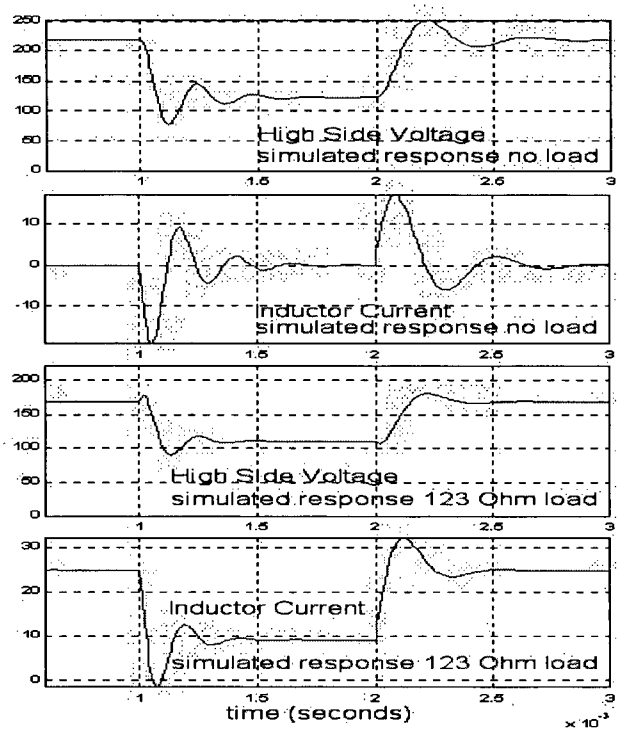


Figure 43: **MATLAB Simulated dynamic response to step change in duty cycle from D=0.45 to D=0.03 to D=0.45**

Figure 44 confirms experimentally the validity of the simulation model at the simulated conditions. The experimental results are extremely similar to the simulation results confirming the accuracy of the large-signal discrete simulation model. The experimental results yield the same response characteristics for oscillation frequency and dampening predicted by the MATLAB simulation. Given the close agreement between the measured and simulated results it is possible to proceed further with confidence that the MATLAB based converter model is valid for large signal operation. The measured results of figure 44 also confirm the true seamless bi-directionality of the converter as the inductor current is again observed to pass freely through zero.

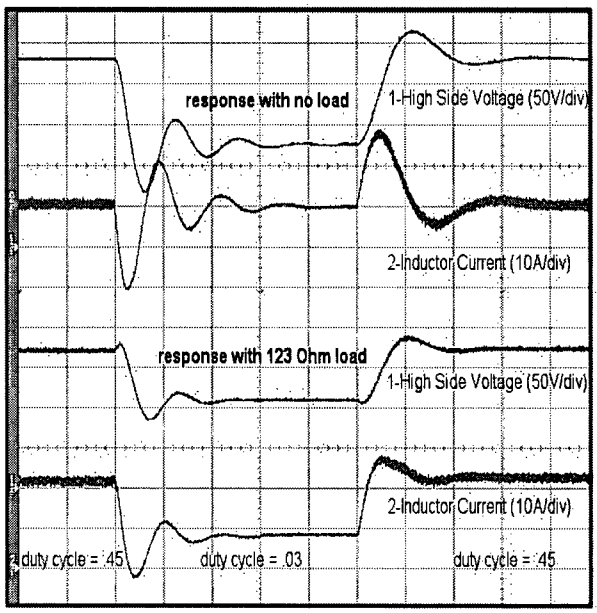


Figure 44: Measured dynamic response to step change in duty cycle from D=0.45 to D=0.03 to D=0.45 (200us/div)

Within the simulation model the battery discharge current and large-signal circuit operating point are determined by the duty cycle and load resistance when no external voltage source influences the dc bus voltage. To model and simulate the reverse power flow battery charging current the dc bus voltage state must be manually clamped higher than the natural dc bus voltage determined by the duty-cycle and battery voltage. Although not shown in the prior simulation example, this has the effect of impressing a higher voltage on the battery and thus creates the desired reverse current flow charging effect. This also describes what physically happens within the prototype bi-directional thesis converter when a stiff external dc charge source above the voltage bus voltage set-point is impressed on the dc bus.

Although the 1uF output capacitor used in this experiment may appear unusually small and the dynamic response may appear uncharacteristically rapid this is actually done on purpose. Part of the experiment was to prove the use of a very small bus capacitance. Also, in keeping with the cost reduction theme, the smaller the components are the less they cost. Additionally, it is beneficial to have the circuit respond as quickly

as possible while still filtering the high frequency ripple. Upon closer inspection one can also note that the lack of input capacitor and small 1uF output capacitor leads to very small startup inrush currents. However, although the use of the 1uF capacitor was successful, upon further consideration a 6uF capacitor has been selected for the finalized design to minimize voltage ripple for reasons outlined in section 2.5.4. The smaller 1uF capacitor used in this comparison nonetheless serves to illustrate and verify the proposed MATLAB- based simulation process.

4.2 Modeling the DSP controller in SIMULINK/MATLAB

In the previous section power-circuit simulation algorithm and a MATLAB based simulation program were proposed. The MATLAB based power-circuit simulation proved to be effective at representing the dynamic behavior of the power circuit to large-signal step changes in the duty-cycle. This section presents a SIMULINK/MATLAB based model of the DSP feedback controller. When used in conjunction with the power-circuit simulator the resulting simulation system is hypothesized to accurately predict the response of the power circuit under closed-loop digital control.

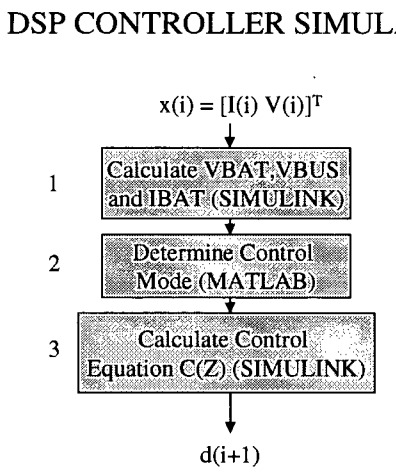


Figure 45: SIMULINK/MATLAB based DSP controller simulation

SIMULINK is simply an extension of the MATLAB programming environment that allows MATLAB based subroutines to be programmed graphically. Once developed the SIMULINK subroutines can be called the main MATLAB program. SIMULINK has been selected as the preferred environment to develop the DSP simulator mainly because of its easy to interpret graphical programming environment. However, it will be shown

that the digital controller simulator presented still depends on the direct MATLAB programming environment to calculate a portion of the controller procedure.

Although SIMULINK is traditionally used as a complete environment for performing transient time simulations of dynamic systems, there is no easy way to represent the constantly evolving non-linear model of the power circuit within the SIMULINK transient time environment. For this reason the SIMULINK models proposed are single iteration only and are deigned be called once per time step from within the main MATLAB based power-circuit simulation program developed in the previous section.

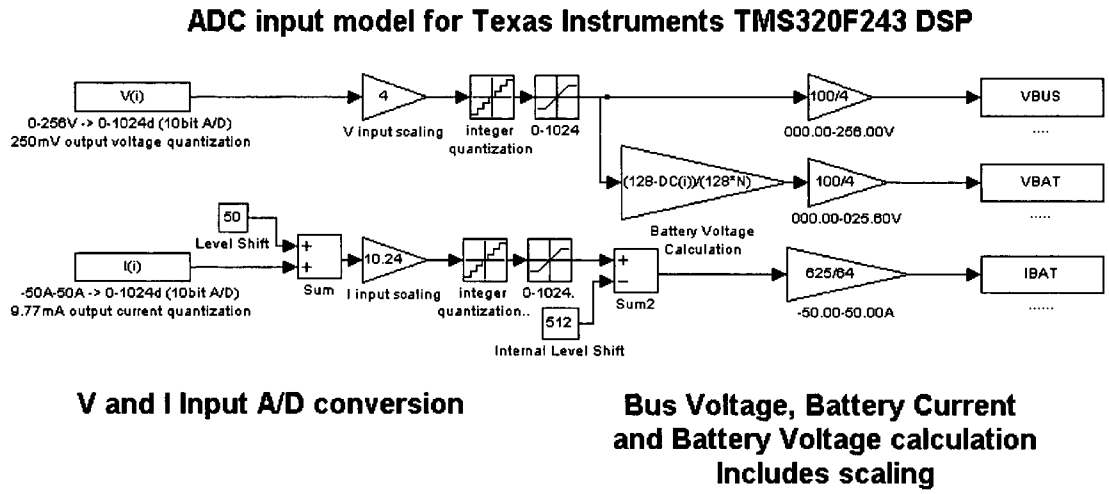


Figure 46: SIMULINK based ADC input model

A block diagram overview of the proposed DSP controller simulation model only is shown in figure 45. The first block of the controller model is displayed in detail in figure 46. This SIMULINK based model represents the portion of the DSP controller that inputs the voltage and current information from power-circuit. For the prototype thesis converter the inputs are the dc bus voltage and the time averaged current through *Sw4* as outlined in section 3.1. However, within the controller simulator it is necessary to utilize the battery current directly, as this is the current provided by the state space averaged model of the power-circuit.

The SIMULINK model of figure 46 initially scales the inputs to take maximum advantage of the TI DSP's 10 bit ADC. The inputs are then integer quantized and subject to the 0-1024 saturation limits of the ADC. In this way the numerical effects of the analog to digital conversion are accounted for. The bus voltage, battery voltage and battery current required for the three control modes are then calculated from power-circuit outputs, *V* and *I*, according to the process of section 2.1. Again, careful attention is paid to scaling the results to take maximum advantage of the 16 bit fixed point DSP processor.

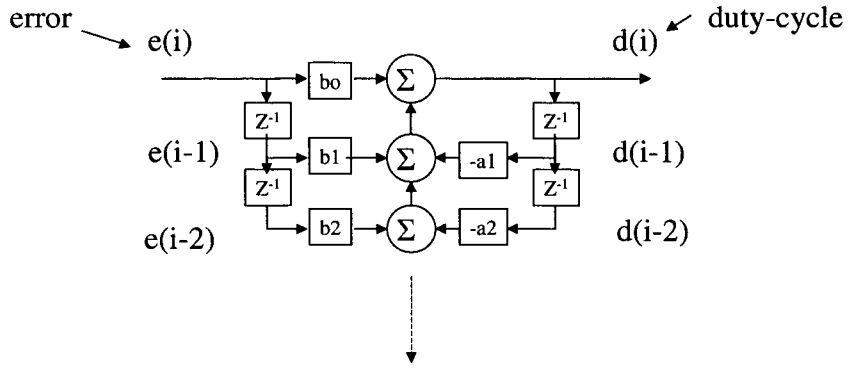
The second block of the controller simulation process takes *VBUS, VBAT* and *IBAT* from the previous SIMULINK block and calculates the control mode of the converter according to the control mode decision making algorithm derived in section 3.1. This section is modeled in straight MATLAB code as SIMULINK is not as suitable for executing the decision-making algorithm. The MATLAB code appears as follows:

```
%*******MATLAB BASED Control Mode Decision Making Algorithm - Follows ADC input model*****
if VBUS < 20000
M = 1;
elseif IBAT<-3000
M = 2;
elseif VBAT>1400
M = 3;
end
if M == 1
B0=round(0.00009946*2^16)
output = VBUS;
setpoint = 20000; %200.00 Volts
elseif M == 2
B0=round(.0003408*2^16);
output = IBAT;
setpoint = -3000; %-30.00 Amps
elseif M == 3
B0=round(-.01363*2^16);
output = VBAT;
setpoint = 1400; %14.00 Volt
end
%******* Data then fed into the Digital controller model *********
```

The MATLAB code determines the control mode, *M*, and then outputs the appropriate output value, setpoint value and C(Z) coefficients to be used within the final closed loop digital feedback controller section. Again, careful attention has been paid to scaling the single C(Z) coefficient, *B0*, required for each of the three I (integral) controllers as summarized in section 3.3.5. Due to the 16 bit fixed point nature of the DSP and 40KHz sampling frequency it is necessary to scale the derived *B0* coefficients

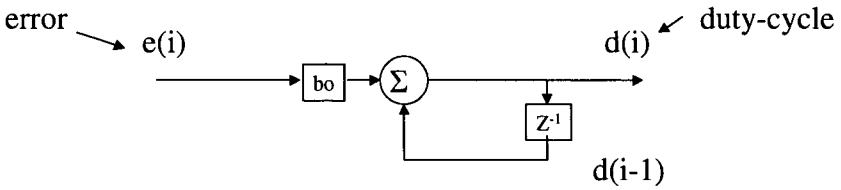
by 2^{16} and round to integer values for use in the final 32 bit double word control calculation.

$$C(Z) = \frac{D(Z)}{E(Z)} = \frac{b_0 z^m + b_1 z^{m-1} \ldots b_m}{z^n + a_1 z^{n-1} \ldots a_n} * \frac{z^{-n}}{z^{-n}}$$



A) Universal C(Z) controller form

$$C(Z) = \frac{D(Z)}{E(Z)} = \frac{b_0}{a_0 z - a_1 1}$$



B) I (integral) controller

Figure 47: Controller Transfer function to discrete time control calculation

Any z-domain C(Z) controller transfer function can be converted to discrete time difference equation form and implemented in a digital controller as outlined in figure 47a.

However, figure 47b shows the reduced form required to implement the I controllers as developed in chapter 3. Note only a single *B0* coefficient is necessary as *A0* and *A1* are unity - as confirmed by the I compensator transfer functions appearing in Table 16. It is the digital controller form of figure 47b that is used within the final simulation section to calculate the required duty-cycle output value.

The third and final section of the controller simulation model consists of the digital control calculation required for the I controller. The SIMULINK model of figure 48 takes the information produced by the MATLAB code of section two and computes the next duty-cycle. Special attention has been taken to account for the 16 bit fixed point computational limits of the DSP controller. The error is effectively right shifted 16 bits to create a two word 32 bit environment that allows the use of the scaled integer *B0* gain calculated in the previous section. The 32 bit duty-cycle calculation is fundamentally necessary to accumulate the very small error integrated over each 25us cycle resulting from the small original *B0* coefficients of table 16. The model is organized so the 0-1 duty cycle appears in integer form between 0 and 128. In doing so the high 16 bits are used for the integer duty-cycle and the low 16 bits are used as the necessary fractional component of the duty-cycle calculation. The SIMULINK based controller model also provides mechanisms to prevent integrator windup and represent the critical 128 point quantization of the duty-cycle.

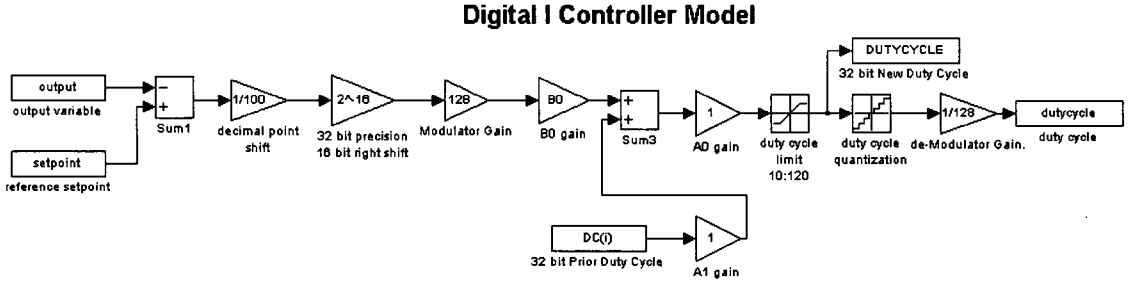


Figure 48: SIMULINK based I control calculation

4.3 Simulation of the DSP controlled non-linear power circuit

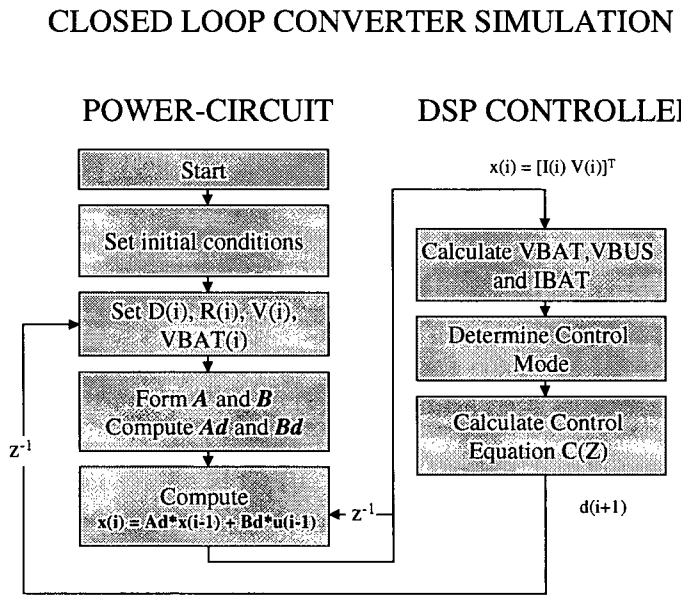


Figure 49: Complete Closed Loop Large-Signal Simulation model

The two models of the power-circuit and DSP controller previously developed can now be integrated to form the complete closed loop system as presented in figure 49. A variable internal battery voltage, *VBAT*, has been introduced in the power-circuit model to include the variance of the internal battery voltage as energy is added and removed. The idea is to start with an initial internal battery voltage and reduce it as amp-hours are removed during discharge and increase the internal voltage as amp hours-are added during charge. In this way the variable battery voltage can be included and the constant voltage mode 3 of the control process can be validated. A MATLAB program has been developed simulate this closed loop system and appears in appendix L.

The simulation results displayed in figures 50 through 53 indicate the transient behavior of the output voltage, battery terminal voltage, battery current and controller duty-cycle output. Initially the dc bus of converter is unloaded and the controller adjusts the duty cycle to regulate at 205V. The battery current remains at virtually zero and the

battery terminal voltage remains, as expected, at its initial 12V. Notably, the simulation results indicate the effect the quantized duty-cycle has on regulating the output voltage. A significant output voltage oscillation is observed as the quantized duty-cycle struggles to maintain the voltage set-point.

At 15ms a 200 ohm resistive load is placed on the dc bus to represent inverter loading. The battery discharge current increases accordingly and the controller responds by increasing the duty-cycle to compensate for the reduced terminal voltage of the battery and internal power-circuit voltage drops. Additionally, the internal battery voltage starts to decline due to the amp-hours removed from the battery (Note that simulation has been adjusted to rapidly reduce the battery voltage to better display this effect). Again, the quantized effect of the duty-cycle on the output voltage regulation can be observed. Most importantly the transient response from no load to fully loaded is observed to be stable.

At 33ms a 225V dc source appears on the dc bus. Given the current duty-cycle, this has the effect raising the terminal voltage of the battery and charge current is driven into the battery. Observing the bus voltage is above 205V, the battery current is below -30A the controller responds and switches to control mode two. The controller, as designed, then adjusts the duty-cycle to regulate the charge current at -30A. As the battery charges the battery voltage also increases due to the accumulating amp-hours.

At about 45ms the battery terminal voltage is deemed to be 14V. At this point the controller automatically switches to control mode three and the duty cycle is adjusted by the controller to provide a constant 205V:14V conversion ratio. The charge current is then observed to taper towards zero due to the increasing internal voltage.

The results of the closed loop simulation example have proven the proposed control approach as well as ensured acceptable dynamic performance and large signal stability of the digitally controlled power circuit. Furthermore, by investing time developing the simulation model for the digital controller the majority of the conceptual DSP controller programming work is complete. Further programming of the actual DSP controller simply requires transferring the information of the proven controller model into a programming language suitable applicable to the particular DSP utilized.

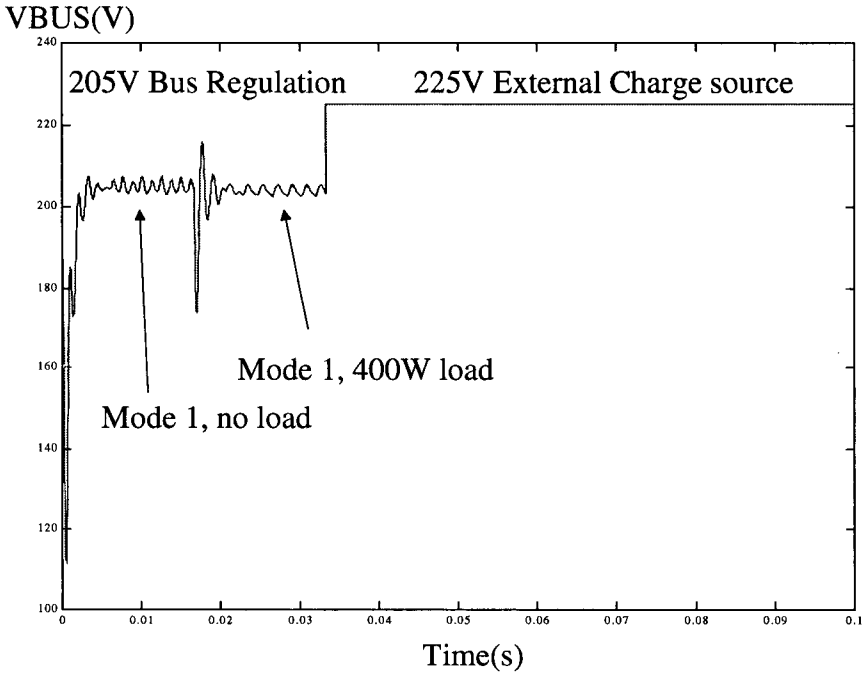


Figure 50 : Simulated Bus Voltage

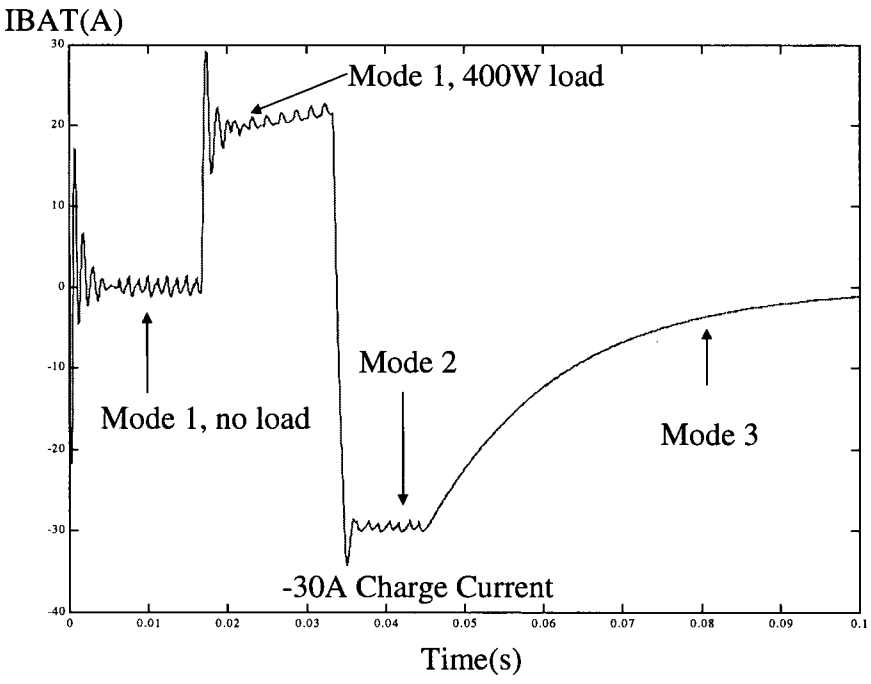


Figure 51: Simulated Battery Current

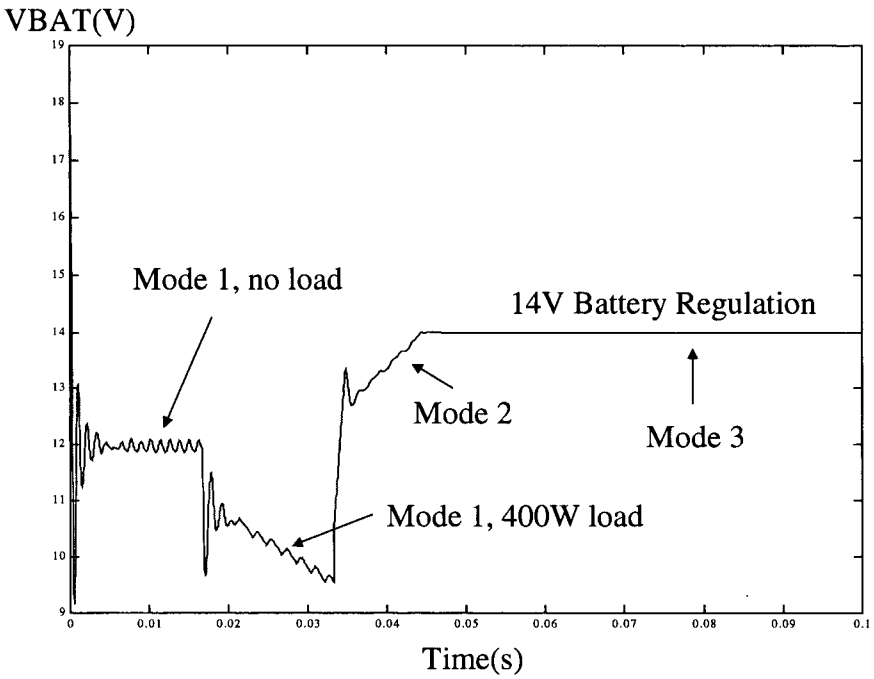


Figure 52: Simulated Battery Voltage

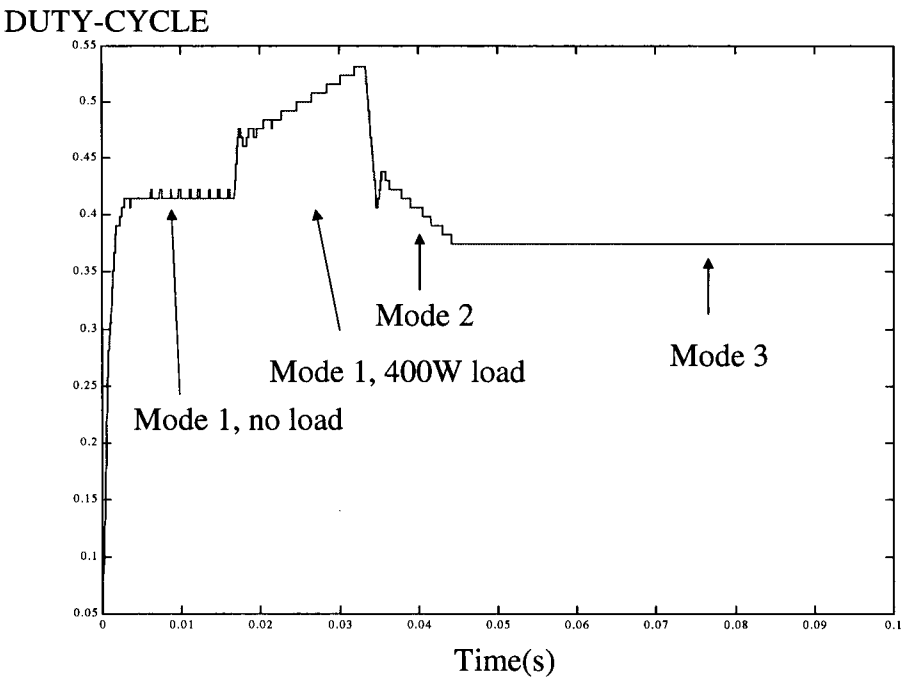


Figure 53: Simulated Controller Output: Duty-Cycle

Chapter 5 - Prototype power-circuit under closed loop digital control

As a final step in the thesis converter development it is necessary to measure and acquire real-life data from the DSP controlled prototype power-circuit. The measured data is necessary to validate experimentally the concepts proposed within the prior chapters. Measured results can be obtained by programming the DSP with the program algorithm proposed in chapter three and then subjecting the converter to various large-signal step changes in operating conditions. The two primary goals of the evaluation are: 1) confirm stable and automatic multi-mode operation of the prototyped system when interfaced with real-life components, e.g. storage battery and dc bus charging source, 2) measure the transient performance of the controlled converter and compare to predictions made by the simulation algorithm developed in chapter 3.

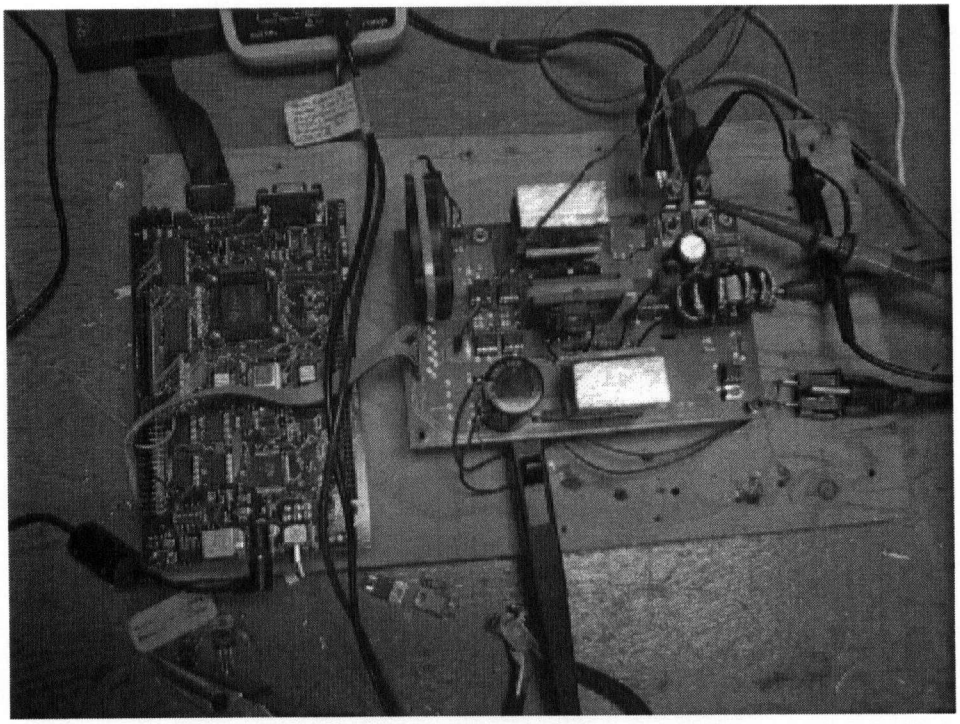


Figure 54: DSP controller interfaced to the prototype power circuit

5.1 DSP controller programming

To facilitate a performance evaluation the 16 bit fixed point DSP processor was programmed in assembly language according to the controller design outlined in chapter three. Complete program code can be viewed in appendix L. The bus voltage and Sw4 current were conditioned and interfaced to the ADC module on the DSP.

Two caveats discovered during the programming process are the need for greater than 16-bit precision when performing the mathematics of the controller difference equation and the inability of the processor to divide by non-radix 2 numbers. Scaling the control equation coefficients to integer values and manually implementing double word 32-bit math solved the extended precision issue. Implementing a lookup table to represent the 128 possible 1/(1-D) divisions required when calculating the battery current solved the division limitation.

Once programmed, debugged and tested, the measured time required to service the 40KHz sampling interrupt, calculate the duty-cycle then return to the main program was 15us. This represents approximately 60% of the total time available between the sample interrupts. A detailed breakdown of the DSP controller timings can be found in table 18. It is shown that the control equation calculation requires 2.2us of the total 15us required for sampling and updating the duty-cycle. This represents relatively little computational time with respect to the other components of the duty-cycle update routine. There is certainly room for computing a more complex control equation if required. In fact, for the prototype power-circuit design, processor speed will most likely cause limitations in the duty-cycle quantization effect before causing a limitation of CPU cycles available to calculate a suitable control equation. Assuming a maximum sampling rate where $f_{sample} = f_{switch}$ there will always be a fixed number of CPU cycles available for any *DQ* (3.5.2). In the case of the thesis converter application it is shown that even at the maximum sampling rate there are a more than adequate 511 CPU cycles available for the duty-cycle update computations.

Code Function	Measured Time Required
Sample and store I and V	3.5us
Calculate VBAT, IBAT & VBUS	4.5us
Control mode decision making	1.7us
Control equation calculation	2.2us
Overhead (LEDs, context save etc.)	3.1us
TOTAL/AVAILABLE	**15us/25us**

Table 18: Measured duty-cycle update timings

5.3 Measured closed loop performance

The evaluation of the closed loop power circuit performance is broken down into three sections. Initially, the overall functional performance of the converter is evaluated by performing a full battery discharge/charge cycle. Next, the controlled transient behavior of the circuit in mode 1 is examined and compared to the predicted results from the power-circuit simulator developed in chapter three. In this experiment the converter is subjected to large-signal changes in operating point while controller stability and simulation accuracy are observed. Finally, the transient response into and out of mode 2 operation is measured and compared to results predicted by the simulator.

5.3.1 Full battery discharge/charge cycle

The first test serves to confirm the automatic tri-mode operation of the digitally controlled power-circuit by performing a complete charge/discharge cycle on a popular Optima "Yellow Top" 65 Amp-Hour absorbed glass mat lead acid battery. The purpose of this test is to confirm that the converter fundamentally works as designed. No detailed attention is paid to controller transient performance at this point.

The test commenced with a 125 Ohm resistive load placed on the regulated 200V bus to facilitate mode 1 of operation. Over time the 320W load dissipated the energy from within the battery resulting in a steady decrease of the battery terminal voltage. The DSP duty-cycle steadily increased to compensate for the battery voltage while regulating the bus at 200V. VBAT, IBAT, VBUS and dc are all measured values logged from within the DSP memory. A number of individual samples were recorded and the average value calculated. This was necessary as the values were constantly changing due to the variation in the result due to the duty-cycle oscillation.

Once the battery voltage fell below to 10 volts it was deemed discharged and 35 minutes into the test a stiff 225V dc source power supply was added to the bus. The converter reacted and automatically switched to mode two of operation and began regulating a stable 20A of charge current into the battery. As energy was returned to the battery the terminal voltage, as expected, steadily increased. The converter automatically

switched to mode three of operation and began regulating the DSP calculated battery voltage at 14V once the 14V set point was initially exceeded. Results of the converter evaluation are summarized in table 19.

	MEASURED		DSP INTERNAL DATA				
TIME	VBUS (V)	VBAT (V)	VBUS (V)	VBAT (V)	IBAT (A)	DUTY CYCLE	MODE
2:25	Start test with a 125 Ohm load on the DC BUS (320W)					(0-128)	
2:27	200.4	11.56	200*	10.3*	33*	62*	1
2:37	200.4	11.31	200*	10.0*	35*	64*	1
2:48	200.4	10.94	200*	9.5*	37*	67*	1
2:58	200.4	9.90	200*	8.5*	41*	77*	1
3:00	225 VDC voltage source added onto the DC BUS						
3:02	225.0	11.79	225*	13.0*	(-20)*	53*	2
3:09	225.0	12.56	225*	13.5*	(-20)*	51*	2
3:15	225.0	12.70	225*	13.8*	(-20)*	50*	2
3:23	225.0	12.81	225*	13.8*	(-20)*	49*	2
3:32	225.0	12.90	225*	13.9*	(-20)*	49*	2
3:42	225.0	12.96	225*	14.0*	(-20)*	48*	3
3:53	225.0	13.04	225*	14.1*	(-18)*	49*	3
4:23	225.0	13.22	225*	14.0*	(-15)*	49*	3
4:44	225.0	13.37	225*	14.0*	(-11)*	48*	3
5:02	225.0	13.55	225*	14.0*	(-8)*	48*	3
5:26	225.0	13.66	225*	14.0*	(-5)*	48*	3
5:30	225 VDC voltage source removed from the DC BUS						
5:31	200.4	12.01	200*	10.9*	31*	58*	1
6:07	200.4	9.24	200*	8.2*	44*	79*	1
6:08	End of test						
Mode 1 = 200V bus voltage regulation / battery discharge							
Mode 2 = -20 Amp constant current battery charge regulation							
Mode 3 = 14V constant battery voltage charge regulation							
* approximate time average of instantaneous sampled DSP data points							

Table 19: Measured Automatic operation of the DSP controlled converter

It is worth noting here that there is some significant discrepancy between the DSP calculated battery voltage and the actual measured voltage. During discharge the DSP calculated voltage is lower than the actual measured voltage and during charge the DSP measured voltage is higher than the DSP calculated voltage. This is because the equation used to calculate the battery voltage within the DSP (3.1.3) does not take into consideration the I*R voltage drops within the power circuit. Therefore, when current is

flowing, there is some inaccuracy with the calculated value. This does not cause any serious practical concern and the only arguable negative side effect is that the charge algorithm begins to taper off the charge current prematurely. It is only crucial for the controller to accurately regulate the voltage of the battery at a preset level when the battery is fully charged to prevent overcharging or boiling of the battery. At this point the battery current is inherently zero and the DSP calculated voltage matches the actual battery voltage with an acceptable degree of accuracy. Table 19 shows that as the current is reduced so is the discrepancy. A current dependent correction factor could be easily implemented to compensate for the error but in the interest of increased simplicity it was omitted.

One hour and five minutes into the test, once the charge current had tapered to 5A, the charging source was removed and the battery was forced to discharge again. The converter successfully reverted back to mode 1 and began to regulate the dc bus at 200V.

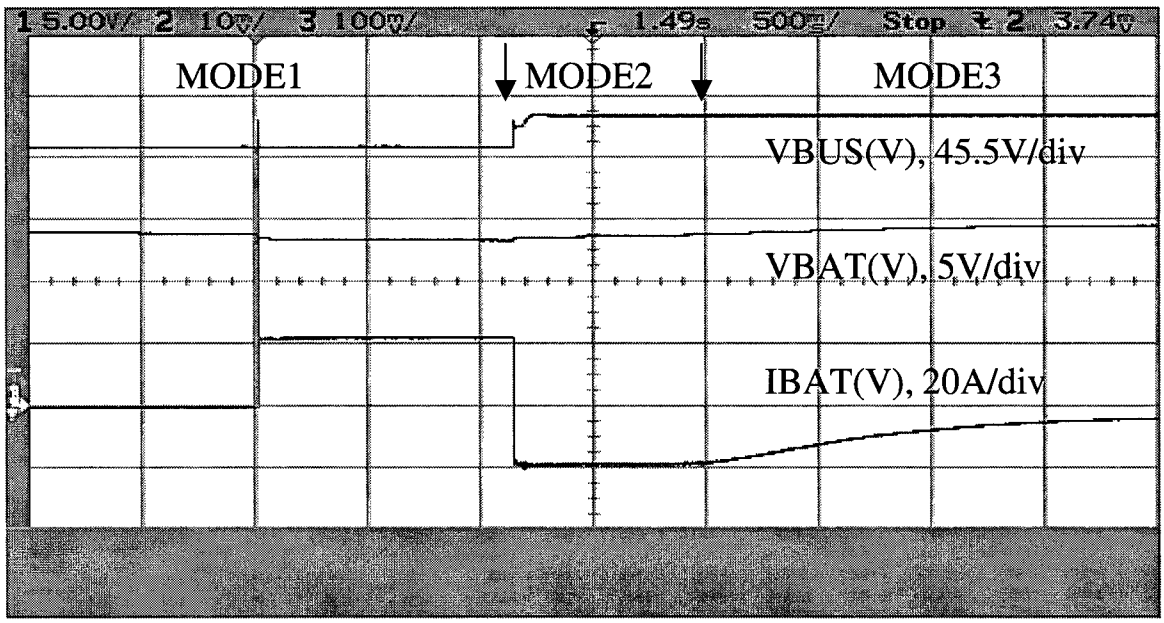


Figure 55: Measured automatic discharge / charge operation

To confirm clean mode changing operation it is of interest to have a graphical representation of the converter automatically cycling between modes of operation. Figure

55 shows a low-resolution time scale, seconds not milliseconds, oscilloscope plot of the converter's multi-mode transient time response to changes in operating conditions. Unlike the results of table 19 the results of figure 55 were obtained using a battery at close to a 100% state of charge (SOC). With the battery at 100% SOC it is possible to quickly discharge some energy and observe the multi-mode response once a charge source is placed on the dc bus. In figure 55 all three modes of operation are achieved within 5 seconds. Initially the converter is unloaded and operating in mode 1. A resistive solid state load is then added to cause a battery discharge current of approximately 20A. 1.2 seconds later a 225V dc bus source is introduced to recharge the already very full battery. The battery voltage rises quickly and the time spent in mode two is minimal due to the full state of charge of the battery. The thesis converter then switches to mode three, constant voltage charge, hence the resultant tapering current. Figure 55 shows graphically the stable transient time response to the changing operating modes described in Table 19.

5.3.2 Mode 1 transient response to step changes in load

The purpose of this examination is to observe the behavior of the converter to large-signal changes in operating point while in mode 1 of operation and to compare the response to results generated by the converter simulator developed in chapter three. To accomplish this a solid state resistive bus load was set up to oscillate between a load condition of 85 ohms and 1750 ohms, 470W and 23W respectively, at a frequency of nearly 30Hz. Figures 57 and 57 display the results and clearly demonstrate a strong correlation. Both the measured and simulated results yield virtually the same result, including the magnitude and frequency of the ripple effect influenced by the quantized duty cycle. Additionally, the stable response time for both transitions is sub 5ms, which is what was designed for in Chapter 2.

Figures 56 and 57 confirm two important things: 1) the DSP controlled power-circuit is closed loop stable for large-signal changes in bus loading and 2) the proposed simulation results accurately predict the converter performance. This means that the MATLAB simulator can be used to further investigate the effects of implementing controllers with different numerical characteristics. It can now be said with some degree of confidence that, for example, one can accurately observe the results of using a faster DSP capable of providing an increased *DQ*, or a slower DSP capable of providing more coarse *DQ*, by simply adjusting the SIMULINK DSP model. Results can be quickly simulated without actually implementing the changes in hardware.

Using a *DQ* of 128 yields a maximum 5V peak to peak ripple in the 200V regulated output. Further simulation tests proved this ripple to increase with a decrease in *DQ* and decrease with an increase in *DQ*. However, the difference was subtle over a practical region of interest. For example, a *DQ* of 256 yielded a simulated ripple of 3V peak to peak while a *DQ* of 64 yielded a simulated ripple of 7V peak to peak. In each case the ripple frequency appears to occur at the duty-cycle dependant natural frequency of the converter.

At this point one may wonder about utilizing a larger capacitor on the dc bus to reduce the ripple and voltage transients. This is certainly a possibility but along with possibly being more expensive the larger capacitor will also result in a slower reacting

voltage regulator when used in the single feedback loop voltage control mode. The larger bus capacitance may also introduce some additional inrush current control complications when first starting the power-circuit. It is therefore concluded that using a minimum bus capacitance serves to successfully reduce the number of additional control complications, optimize control response time albeit at the expense of increased quantized duty-cycle ripple and voltage transients.

In this section the stable operation of the DSP controlled power circuit in control mode one has been proven. The results predicted be the proposed simulation approach closely match the measured results effectively model the numerical effects of the DSP.

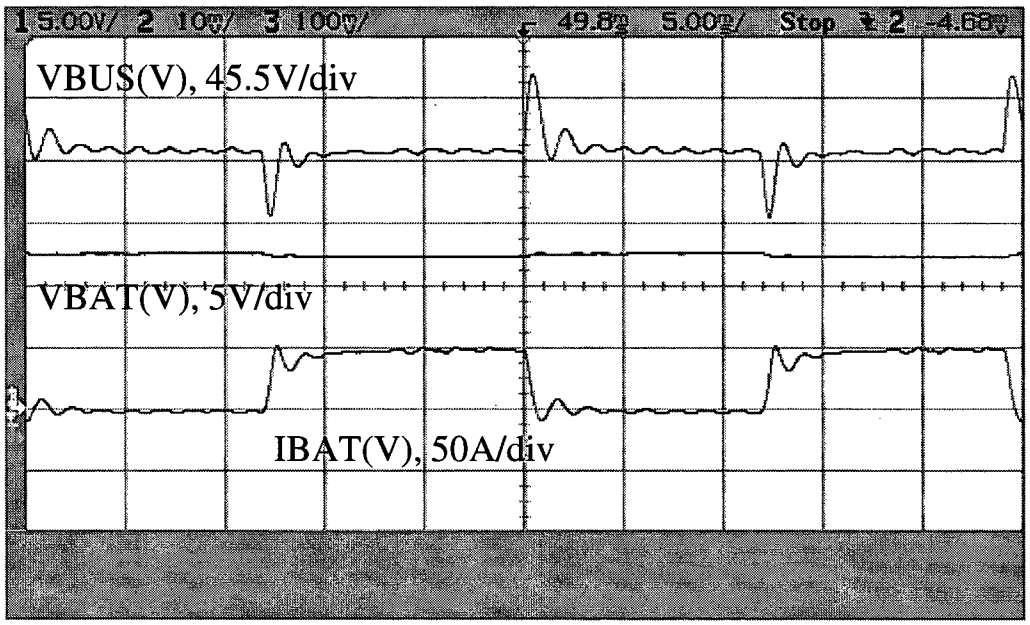


Figure 56: **Measured Mode 1 regulation to a step change in resistive load (1750 to 85 Ohm)**

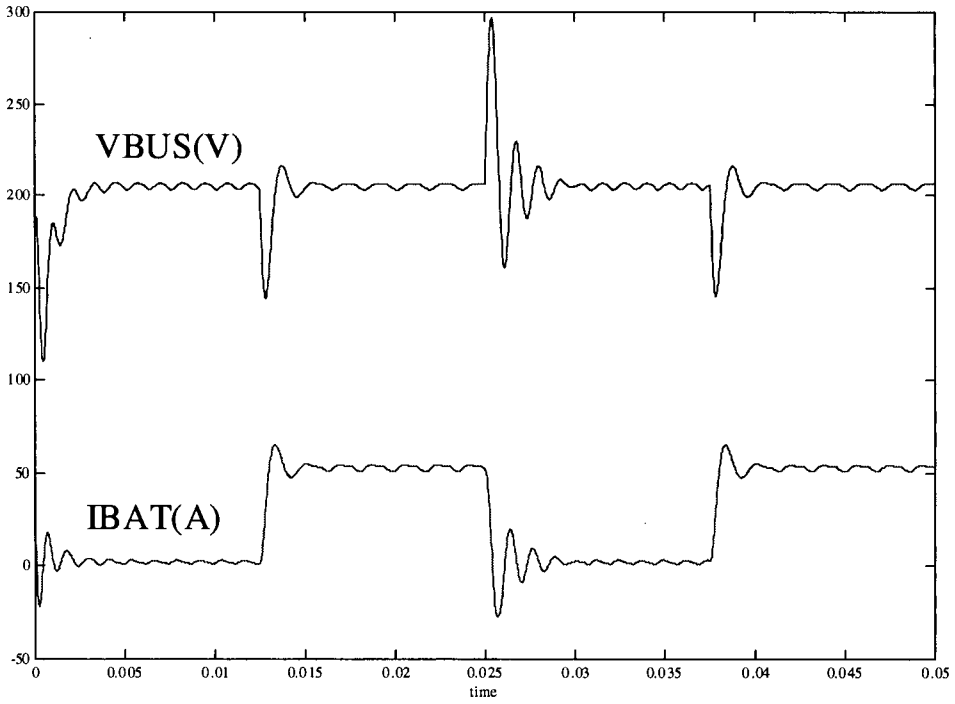


Figure 57: **Simulated Mode 1 regulation to a step change in resistive load (1750 to 85 Ohm)**

5.3.3 Mode 1-2-1 transient response to the appearance of a charging source

In this section the transient performance of the DSP controlled power-circuit is evaluated when faced with the appearance of a charging source on the dc bus. The measured results of the experiment are compared to results predicted by the proposed power converter simulator.

To measure the transient performance a stiff 225V dc source was applied and then quickly removed from the dc bus. This resulted in a transition from mode 1 to mode 2 and back to mode one within a 100 ms time span and provided an appropriate window for measuring the transient response The measured and simulated results appear in figures 58 and 59. Again, the measured and simulated results agree with a high degree of accuracy. In the measured result one can observe the dynamic response of the 225V source. The real life source is not as stiff as the simulated source. In any case the both sets of results confirm an acceptable level of performance. Stable operation is observed and the settling response time is again within 5ms as predicted in chapter 2. The proposed automatic switching concept and simulation technique are again successfully proven.

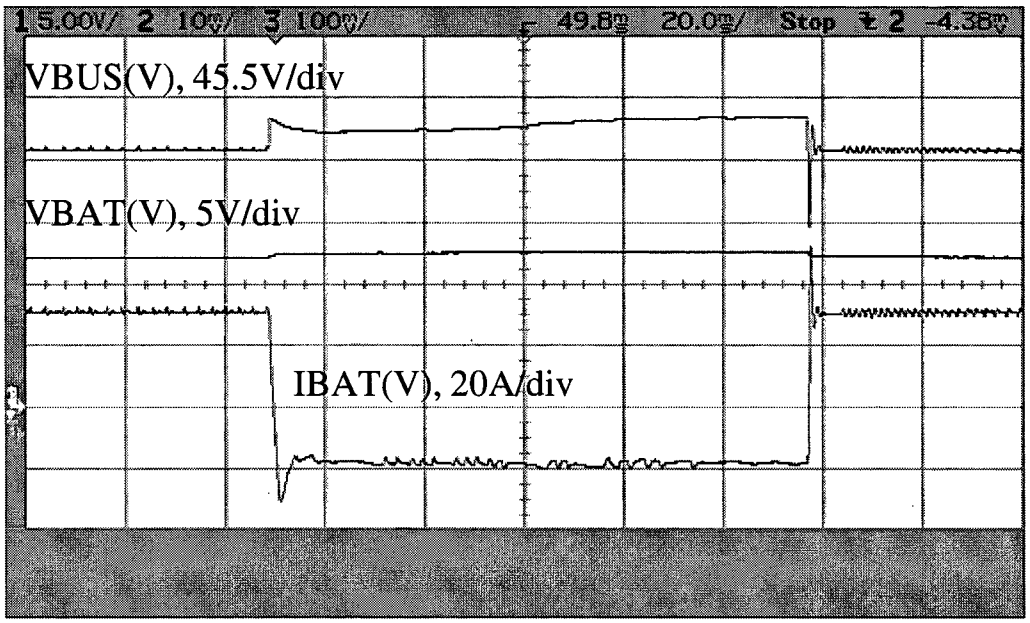


Figure 58: **Measured Mode 1 Bus Voltage regulation to Mode 2 Constant Charge Current Regulation**

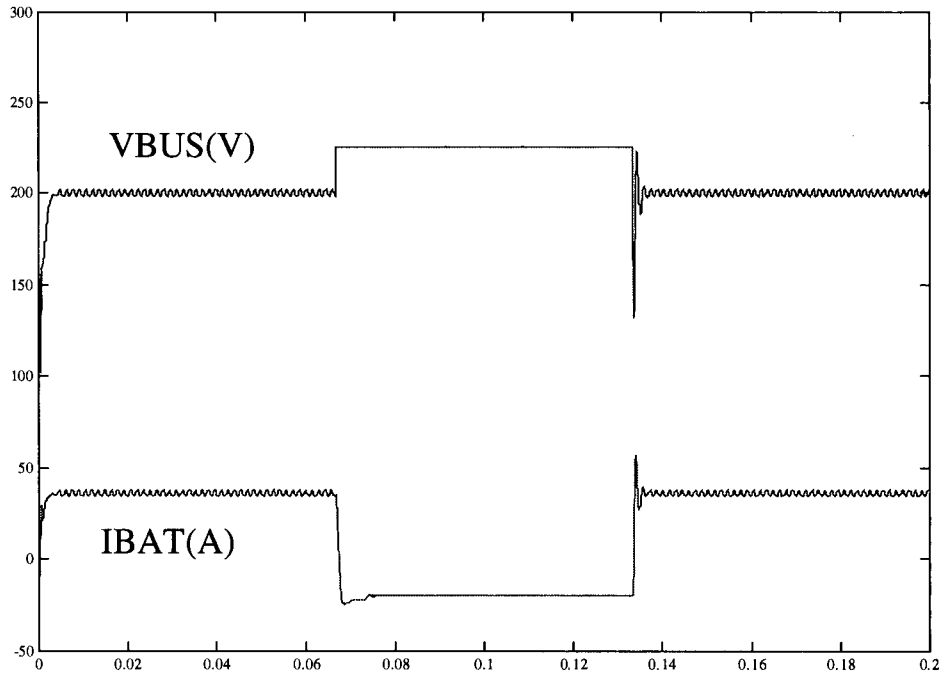


Figure 59: **Simulated Mode 1 Bus Voltage regulation to Mode 2 Constant Charge Current Regulation**

Chapter 6 - Conclusions

In this thesis the development of a novel DSP controlled bi-directional power converter has been considered. A power-circuit design, digital-control design approach and MATLAB simulation procedure have been proposed, analyzed and validated experimentally.

In the second chapter a suitable DSP driven and synchronously rectified bi-directional power circuit was proposed. Along with providing an inherently seamless bi-directional power flow the synchronously rectified approach significantly increases the overall efficiency of the power circuit when transferring energy into the battery. A MATLAB based analysis was performed to quantify the efficiency gains associated with synchronous rectification of the switching devices. The analysis proved that synchronous rectification yields a theoretical 70% increase in charge mode efficiency and a negligible increase in discharge efficiency. The synchronous rectification approach also serves to eliminate the discontinuous inductor current mode of operation and thus further reduces controller design considerations.

Similar transformer coupled push-pull power circuits in the field have experienced performance problems due to transformer magnetic flux imbalance. For this reason transformer flux balancing was also studied in the first chapter. A four winding transformer model and MATLAB based simulation were developed to model the reduction in performance attributed to the magnetic flux imbalance. The tools developed were to aid in developing an active flux balancing control system for the proposed converter. However, when the proposed DSP gated power-circuit was evaluated experimentally transformer flux imbalance proved to be a non-issue. It is thought that the precise symmetrical switch gating signals provided by the DSP reduced the transformer volt second imbalance to a point that resulted in a negligible dc flux component. Another contributing factor may be the conservative design of the transformer core that fundamentally allows for some dc flux offset while still operating in the linear region.

Also in chapter two the practical issues of constructing an efficient power-circuit were addressed. A design was proposed to efficiently switch the four power-circuit switches in an appropriately synchronized manner and with the appropriate delay timings.

Finally, an experiment was performed to compare two high side switch technologies: FET and IGBT. Ultimately the IGBT devices provided the most efficient operation with measured efficiencies of 89% and 92% in discharge and charge directions respectively. The difference between the measured results and 97% idealized efficiency of table 6 can be attributed to switching losses and also the losses of the other non-ideal components.

In chapter 3 a tri-mode digital control system was proposed and developed. The proposed digital control system consists of three feedback control systems designed to regulate the power converter automatically in three separate modes of operation: 1) bus voltage regulation, 2) constant current charge regulation and 3) constant voltage charge regulation. A control design was developed where the DSP automatically selects the control mode according to a proposed control mode decision-making algorithm. It is also determined how to calculate the bus voltage, battery voltage and battery current within the DSP when only the bus voltage and current through a high side switch are sampled.

Also in chapter 3 the crucial small-signal power-circuit plant models are derived to represent the three plants to be controlled. A state space averaging modeling approach of the power-circuit topology is interfaced with MATLAB to conveniently produce duty-cycle to output small-signal valid transfer functions at a given large-signal operating point. The proposed approach is applied to all three plant models. However, the question of which operating point to design for remained. To investigate this question the control compensator design analysis were all performed at three distinct large-signal operating points.

A MATLAB based design procedure was further proposed to conveniently calculate both PI and I compensators for each of the three controllers and at three separate large-signal operating points for each controller. In this way the worst case small-signal plant model could be identified for each controller implementation. For mode 1 operation the fully loaded plant model proved to clearly be the "worst case" or most difficult plant to stabilize and therefore was the appropriate worst case plant model to design for. For control modes 2 and 3 there was little large-signal variation within the small-signal plant models.

For each of the three control modes both PI and I control compensators were derived using frequency domain open loop stability analysis. For control mode 1 there

was little control performance to be gained by implementing PI control over I control. However, for control modes 2 and 3 the PI control offered and order of magnitude increase in terms of control bandwidth over I control. Ultimately the straightforward I control approach offered an acceptable combination of 900 rad/s control bandwidth and ease of implementation and was therefore selected for use within the DSP controlled thesis converter.

In chapter four a large-signal valid power-circuit simulation algorithm was presented. The state-space model of the power circuit developed in chapter three was digitized for iterative computation by MATLAB. The proposed MATLAB simulation procedure proved valid for both bi-directional and large-signal power-circuit operation. To complement the power-circuit simulation model the DSP controller was represented using a combination of SIMULINK and MATLAB. This allowed the closed loop performance of the converter to be simulated while including the numerical effects of the DSP - especially the effects resulting from the 128 point quantized duty-cycle provided by the DSP.

The complete power-circuit simulation model provided an environment in which to develop and test the DSP control algorithm. Ultimately the simulator was used to confirm the automatic multi-mode operation of the proposed converter.

Chapter five experimentally validates the converter and proposed simulation technique. The measured bi-directional performance of the converter agrees strongly with the simulations - including the effects caused by the quantized duty-cycle. The tri-mode concept, digital I controller design approach and simulation tool were proven to function as designed.

The power circuit design, controller design procedure and simulation algorithm approach are transferable to other SMPS applications. The discrete plant simulation algorithm, specifically, will be applicable to various power circuit configurations provided the state equations can be derived in the form of (3.2.1). The digital controller representation is, of course, virtually universal in its application.

Of specific interest to researchers in this field may be the development of the power-circuit model refinement based on a single measurement made purely in the time domain. The illusive dissipative component, R1 and R2 in the case of the demonstrated

converter can be determined by simple comparison of the simulated large-signal duty-cycle step response to the actual measured response. Another contribution that may prove useful is the technique presented for simulating the closed loop behavior of the digitally controlled power circuit. This relatively simple simulation technique run in the ubiquitous MATLAB environment serves to accurately model the true behavior of the power converter while allowing for the comparative study of system component changes. It was in fact during this simulation process when it became apparent that at 16 bit word length was inappropriate for performing the digital control calculations at 40KHz and further attention was warranted.

As a continuation to this work it would be interesting to look at applying current mode control within the tri-mode control scheme. Work could also be performed to increase the overall efficiency of the power-circuit. From a complete inverter/charger system point of view, it would be interesting to look at designing and controlling a bi-directional dc/ac stage to function in combination with the DSP controller and dc/dc stage as presented within this thesis.

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Appendix A: Electrical Specifications

The overall goal of this thesis is to perform research into low cost "consumer market" bi-directional inverter/charger technology and not necessarily to determine the exact market specifications for a new product. However, it is very difficult to consider a design without a functional electrical specification to work within. The power converter considered during this thesis is based on a modification of Xantrex Corporation's new consumer market, DSP based, RVSINE400 sinewave inverter. For this reason the core electrical specifications of the RVSINE400 inverter are combined with electrical specifications of Xantrex's low cost TC10 battery charger to create an approximate consumer market electrical specification within which the project converter is designed Table A.

Specification	Inverting Mode	Charging Mode
Nominal Operating Temp	25C	
Operating Temp Range (power departed above nominal temperature)	0-50C	
Nominal Input Voltage	12 VDC	225 VDC
Operating Input Voltage	10.0-16.0 VDC	200-250 VDC
Safe Input Voltage	0 – 15.0 VDC	0-250 VDC
Nominal Input Current @ full load	40 A	1.8 A
Peak Output Power	700 W	
5 minute Output Power	450 W	
Continuous Power	400 W	
Nominal Output Voltage	200 VAC	14V DC
Line/Load Regulation (0 – full power) (%VDC)	-5 to +5	-5 to +5
Output Frequency (Hz)	DC	DC
Maximum Charge Current	N/A	25A (Bulk Charge)
Maximum Charge Output Voltage	N/A	16V
Minimum Charge Output Voltage	N/A	0V
Battery Ripple Current	< 4A pk-pk	
Charge Profile	N/A	Multi Stage
Charging Input Power Factor	N/A	consumer product, not required
Minimum Efficiency	90%	
Safety	UL458- 4th Edition – Power Converters...For Land Vehicles and Marine Crafts	
Safety	CSA 107.1- 95 – General Use Power Supplies	
EMC	FCC Part 15, Class A – radiated and conducted emissions	
Parts Cost	<$45	

Table A: DC/DC converter electrical specification

Appendix B: Converter Costs

The component costs of a switch mode power converter can be divided up into five main areas:

1) *Packaging*: mainly consisting of the printed circuit board, enclosure, connectors and switches.
2) *Capacitors / Magnetics*: high frequency transformers, inductors and capacitors
3) *High Speed Switches*: diodes, semiconductor switches (FETs, IGBTs).
4) *Control*: micro-controllers, DSPs, control ICs
5) *Cooling*: fans, heatsinks.

Based on the above criteria the two figures in Appendix A show the cost breakdowns of two Xantrex products; the 10 year old TC-10, 10A (120W) battery charger and the new RVSINE 400, 400W inverter. These two products share the same parts cost at ~$35 but the new inverter converts more than twice the power. The power densities and costs per Watt of the two converters are compared in table B.1.

Model	**$/W**	**W/cm^3**
TC-10, 120W charger	~0.292	~0.093
RVSINE 400W inverter	~0.100	~0.391

Table B.1

Fundamentally, the cost of a power converter is a function of its power handling capabilities. A converter's power density and cost per watt should be similar regardless of its function. That is to say if a 400W inverter costs $35 there is no reason why a 400W battery charger should cost much more or less if it is of the same quality and has comparable features. One of the goals when designing the project inverter/charger is to far exceed the $/W and W/m^3 characteristics of the TC10 charger.

Some comments can made regarding the five main cost areas by comparing the two power converters. Most noticeably the TC10 has a large packaging cost component. Although the enclosure is mostly a low cost Aluminum extrusion, by today's technology (based on the RVSINE costs) it is large and expensive for a 120W converter. The TC10 also uses the Aluminum enclosure extrusion as its heat sink for the switching devices but contains no cooling fan resulting in a larger heat sink requirement. In the case of the fan

equipped RVSINE 350 the packaging and cooling represent 40% ($14) of the total cost where as in the TC10 packaging alone represents 52% ($18) of the costs for a much lower power converter. The RVSINE is far superior in terms of packaging performance.

The converter switching frequency affects the size and therefore costs of the magnetic and energy storage components. Figure B.1 shows for both converters magnetic and capacitive energy storage devices represent about 20% of the overall costs. Increasing the switching frequency decreases the size of all switching magnetics and some capacitors. Unfortunately increasing the switching frequency also results in increased switching losses (heat) requiring more packaging and or larger cooling components and a lower overall efficiency. Both example converters utilize a switching frequency of ~80KHz.

In both example converters, switch costs range from 9% to 25% with the charger requiring fewer switching devices in general. The switches are a significant cost of the overall converter design and reducing the number of switches can decrease switching losses as well as switch costs.

Control components for both converters consume 16% of the total costs. However, the RVSINE utilizes a very powerful, low cost digital signal processor (DSP) to perform all of the inverter control functions. Although the TC10 uses a micro-controller of about the same price as the DSP, the micro-controller is far less powerful.

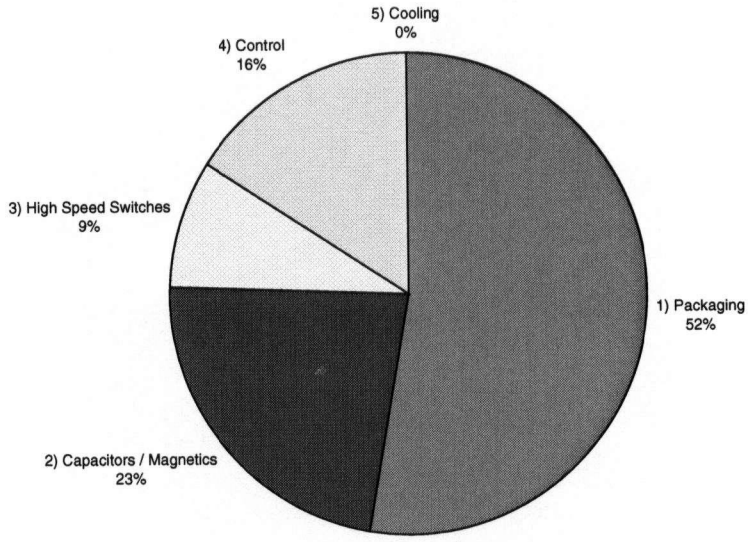
Only the RVSINE incurs costs in the heat sink and fan category. For regulatory approval reasons the RVSINE does not use the Aluminum extrusion enclosure as a heat sink for the switches. The RVSINE features a separate internal aluminum heat sink over which air is moved by the cooling fan. Still, it has attractive power density (W/m^3) and lower costs per watt ($/W) than the TC10.

One of the objects of this thesis work is to aim towards modifying the RVSINE inverter with the minimum amount of additional hardware to produce a low cost, low component count, inverter charger unit. Given that the TC10 charger parts costs are $35 and the RVSINE 400 parts costs are $35, the lowest cost Xantrex sinewave inverter/charger combination presently adds up to $70. Modifying the RVSINE inverter to perform both inverting and charging functions has an attractive cost benefit because the components representing all five main cost areas can be shared for each mode of

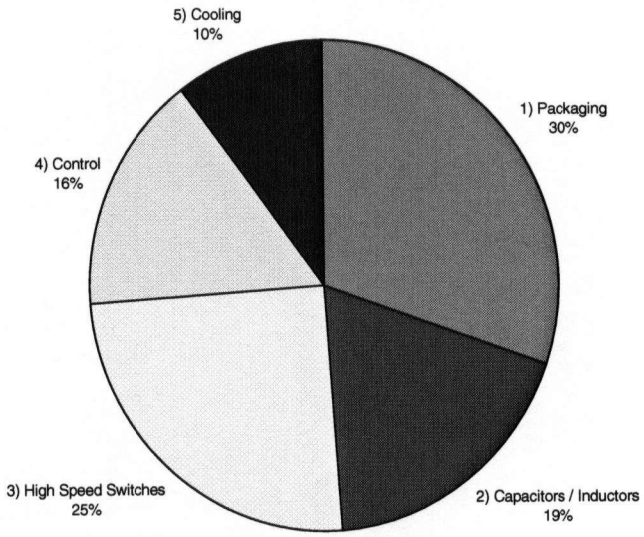
operation. By sharing the packaging, magnetics, switches, control and cooling the incremental cost to go from inverter to inverter / charger are minimal. The cost target is to go from 400W sinewave inverter to 350W combination inverter charger with only a 15% size increase and a 25% cost increase.

Converter Type	**$/W (total parts cost)**		**W/m^3**
RVSINE 400 Inverter	0.10	$35	0.093
400W Inverter / Charger	0.125	$43	0.079

Table B.2: Cost targets and power densities



TC10 battery charger, total parts cost = $35



RVSINE 400, total parts cost = $34

Figure B.1 **Converter costs based on components as listed in the bill of materials.**

Appendix C: MATLAB CODE - Switch Conduction Losses

```
%***Switch Power Dissipation Analysis*****
%***Andrew Swingler - rev. DEC 3, 2002****
clear;
Vbat = 12;
Vbus = 200;
P = 400;
IL = P/12;
Rds = 0.008;
Vce = 2;
Vf = 1;

for i=1:100
   D(i) = i/100;

   N(i) = Vbus*(1-D(i))/Vbat;

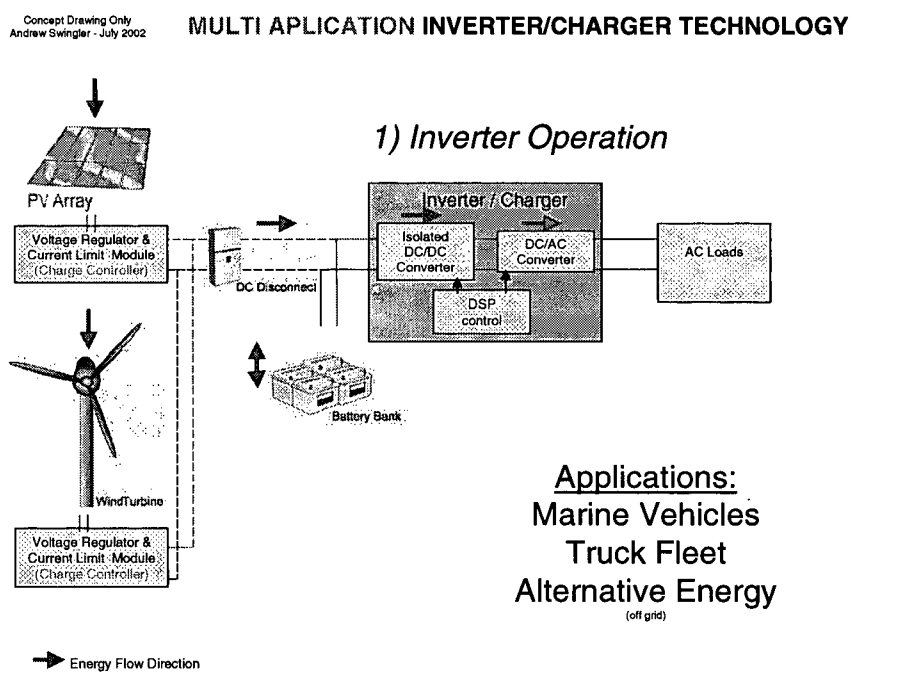
   Irms12 = sqrt( ( (D(i)*(IL/2)^2) + (1-D(i))*IL^2 +(D(i)*(IL/2)^2))/2
);
   Iave12 = IL/2;
   Irms34 = sqrt( ((1-D(i))*(IL/N(i))^2)/2  );
   Iave34 = (1-D(i))*IL/(2*N(i));
   %FORWARD/INVERT/DISCHARGE NON SYNCHRONOUS RECTIFICATION
   P12 = 2*Irms12^2*Rds;
   P34 = 2*Iave34*Vf;
   PF(i) = P12+P34;
   %REVERSE/CHARGE NON SCNCHRONOUS RECTIFICATION
   P12 = 2*Iave12*Vf;
   P34 = 2*Iave34*Vce;
   PR(i) = P12+P34;
   %FORWARD WITH SYNCHROUNOUS RECTIFICATION
   P12 =  2*Irms12^2*Rds;
   P34 =  2*Iave34*min([Vf   Vce]);
   PFS(i) = P12+P34;
   %REVERSE WITH SYNCHROUNOUS RECTIFICATION
   P12 = 2*( (IL/2)*min([IL/2*Rds  Vf])*D(i) + IL*min([IL*Rds  Vf])*(1-
D(i))/2) ;
   P34 = 2*Iave34*Vce;
   PRS(i) = P12+P34;

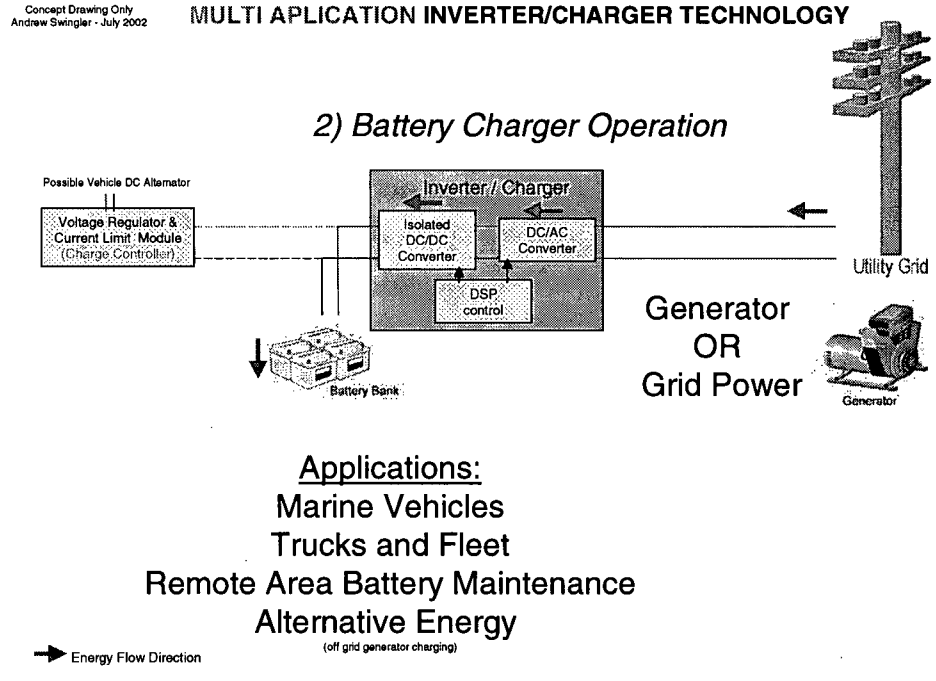
end

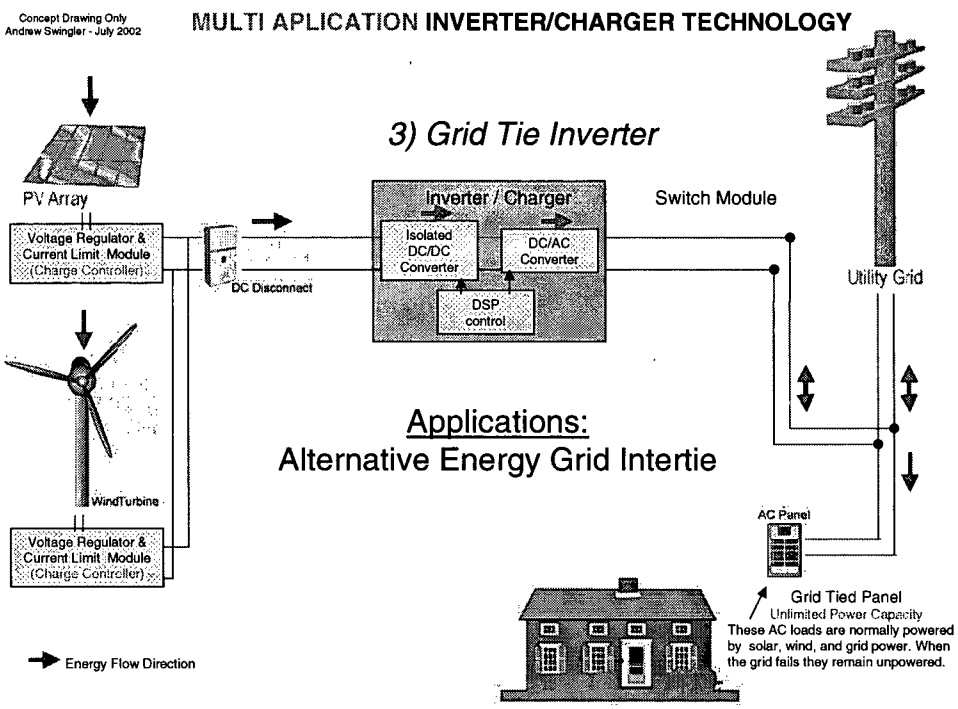
subplot(2,1,1),plot(D,PF,D,PR,D,PFS,D,PRS);
legend('Discharge','Charge','Discharge w/Sync Rect','Charge w/Sync
Rect');
Title('Switch power dissipation at battery power = 400W'),
ylabel('Watts'),

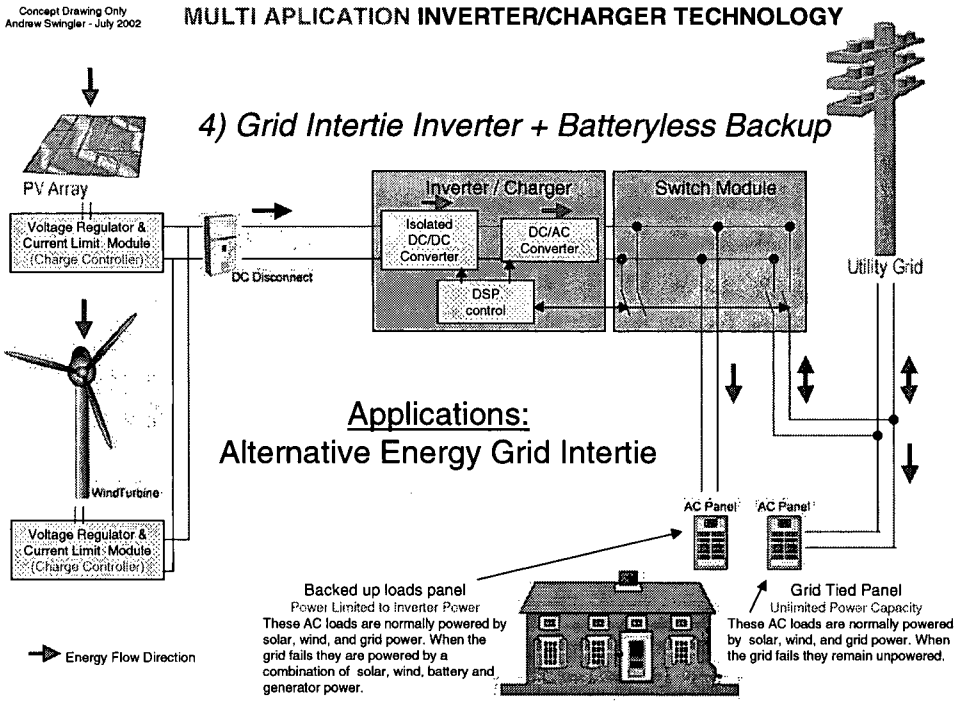
subplot(2,1,2),plot(D,N);
xlabel('duty cycle'),
                  ylabel('transformer turns ratio'),
```

Appendix D: Inverter/Charger applications





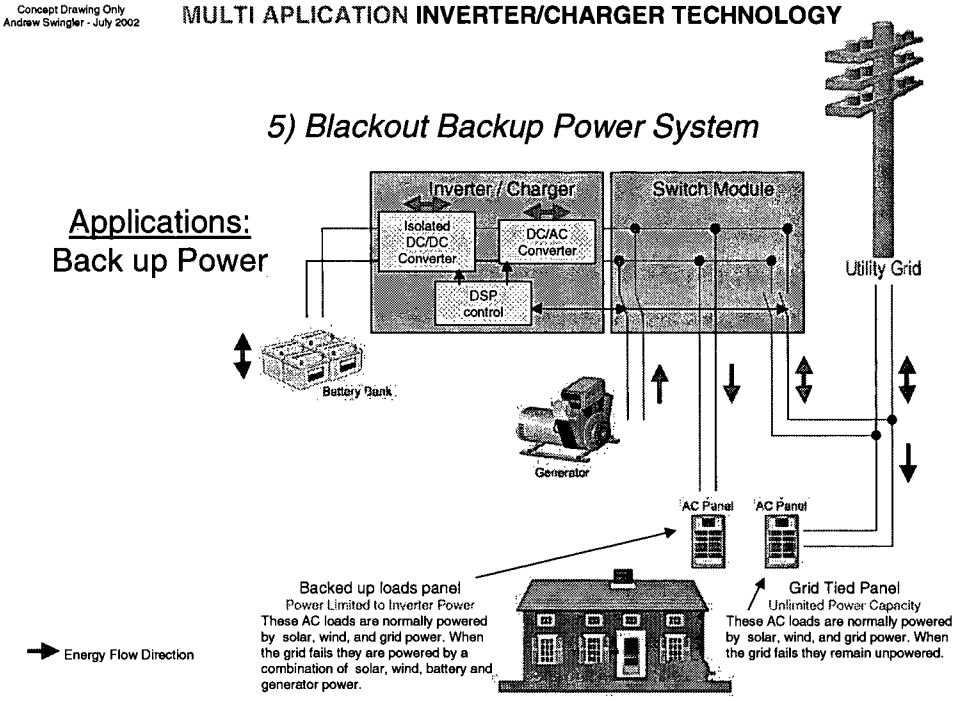

Concept Drawing Only
Andrew Swingler - July 2002
MULTI APLICATION INVERTER/CHARGER TECHNOLOGY
3) Grid Tie Inverter
PV Array
Voltage Regulator & Current Limit Module (Charge Controller)
DC Disconnect
Inverter / Charger
Isolated DC/DC Converter
DC/AC Converter
DSP control
Switch Module
Utility Grid
WindTurbine
Voltage Regulator & Current Limit Module (Charge Controller)
Applications:
Alternative Energy Grid Intertie
AC Panel
Grid Tied Panel
Unlimited Power Capacity
These AC loads are normally powered by solar, wind, and grid power. When the grid fails they remain unpowered.
Energy Flow Direction


Concept Drawing Only
Andrew Swingler - July 2002
MULTI APLICATION INVERTER/CHARGER TECHNOLOGY
4) Grid Intertie Inverter + Batteryless Backup
PV Array
Voltage Regulator & Current Limit Module (Charge Controller)
DC Disconnect
Inverter / Charger
Isolated DC/DC Converter
DC/AC Converter
DSP control
Switch Module
Utility Grid
WindTurbine
Voltage Regulator & Current Limit Module (Charge Controller)
Applications:
Alternative Energy Grid Intertie
AC Panel
AC Panel
Backed up loads panel
Power Limited to Inverter Power
These AC loads are normally powered by solar, wind, and grid power. When the grid fails they are powered by a combination of solar, wind, battery and generator power.
Grid Tied Panel
Unlimited Power Capacity
These AC loads are normally powered by solar, wind, and grid power. When the grid fails they remain unpowered.
Energy Flow Direction

Concept Drawing Only
Andrew Swingler - July 2002

MULTI APLICATION **INVERTER/CHARGER TECHNOLOGY**

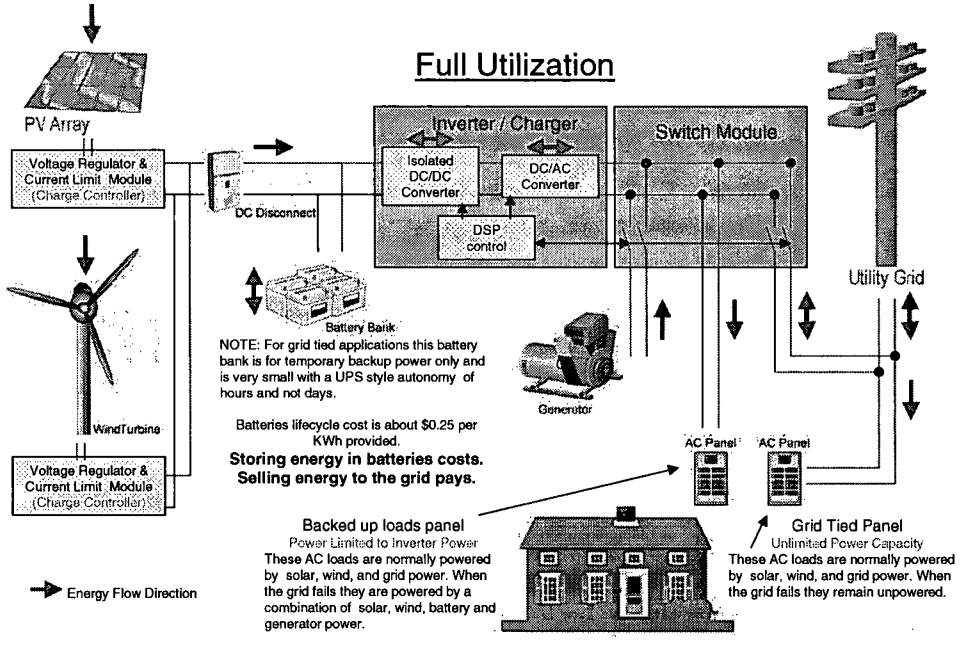
5) Blackout Backup Power System



Concept Drawing Only
Andrew Swingler - July 2002

MULTI APLICATION **INVERTER/CHARGER TECHNOLOGY**

Full Utilization



Appendix E: Transformer magnetic flux balancing discussion

The prior analysis of the proposed Clarke converter topology neglects to point out that the transformer is not an ideal power conversion device. A necessary transformer characteristic to consider is the changing magnetic flux required inside the transformer core to support the induced winding voltages. In actuality the physical core can only operate usefully within a limited range of core flux variation. Outside of this range the core becomes magnetically saturated. During saturation large magnetizing currents are required to support the induced winding voltages. In a push-pull transformer configuration such as the Clarke converter it is important to keep this alternating magnetic flux out of saturation and with zero dc component. This is known as flux balancing. Flux balance is necessary to insure a balanced distribution of switch currents and therefore balanced switch heating effects.

Firstly, a review of basic magnetic concepts is required to properly discuss transformer magnetic flux and flux balance. The fundamental relationship of inductor voltage to inductor current rate of change is found in (E.1).

$$v = L \cdot \frac{di}{dt} \tag{E.1}$$

According to Faraday's law of magnetic induction, (E.1) can be rewritten as (E.2) when the inductor is a uniform single coil of wire with T turns

$$v = -T \cdot \frac{d\phi}{dt} \tag{E.2}$$

and where ϕ is the magnetic flux linked or encircled by the coil winding.

Any transformer winding, when considered alone, is simply an inductor. It consists of a winding of wire wrapped around a ferromagnetic core and behaves in accordance with the above magnetic equations. A transformer exists if more than one winding encircles a common core. In a transformer separate windings are magnetically coupled by the flux that flows within the common core. For a voltage to appear across any transformer winding there has to be an associated magnetic flux rate of change within

the transformer core. This is described by (E.2). To support flux in the transformer core, at least one of the windings must provide the current required for generating the magneto-motive force (MMF), F. This is described by Ampere's Law, (E.3)

$$F = T \cdot i \tag{E.3}$$

where i is defined as the magnetizing current and F is units of Ampere Turns.

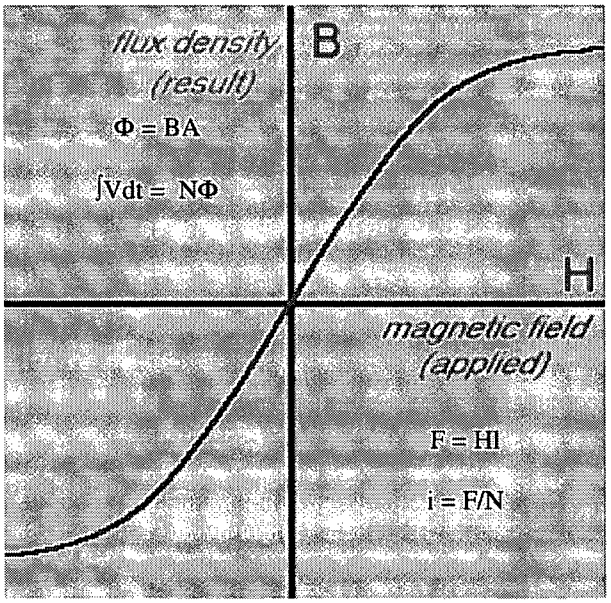


Figure E1: BH Characteristic

The magnetic flux generated within the transformer core by the MMF is a function of the BH properties of the core material, the physical dimensions of the core and the applied magneto-motive force. Figure E1 describes this relationship where B is the flux density and H is the magnetic field intensity. The slope of the B vs. H characteristic describes the permeability of a specific core material. The same BH curve can also represent Φ vs. F, by transforming the B and H scale factors as indicated in figure E1. The slope of this scaled curve describes the permeance of a specific core with defined area, A, and length, l. Yet another scaled BH curve can used to represent ∫Vdt vs. i. The slope of this curve describes the inductance of the core winding. Incidentally, the inverse of permeance is known as reluctance, $\Re$.

Ultimately it is important to operate the transformer core within the linear region of the BH curve. Operating outside the linear region requires a disproportionately large magnetizing current to support the changing flux requirement demanded by the impressed/induced winding voltages. As will be seen later, the large magnetizing current due to an unbalanced and saturated core creates excessive switch currents and switch heating effects.

In a multi-winding transformer the magnetic energy or flux stored within the transformer core is accessible by all the windings. The current component of any winding that supports the core flux is known as a magnetizing current. A transformer magnetizing current is often modeled as flowing through a separate and hypothetical flux generating magnetizing inductance appearing in parallel with a transformer winding. The value of this magnetizing inductance for any independent transformer winding is simply equal to the inductance of the winding itself with all other windings open circuited. (E.4) indicates how this inductance is proportional to the square of the winding turns and the reluctance of the core.

$$L = \frac{T^2}{\Re} \qquad (E.4)$$

A multi-winding transformer can be considered as a black box with ports for the winding conductors. Transformer operation, including core magnetization effects, can be explained with the simplified standard transformer model found in figure E2. The magnetizing inductance can be arbitrarily modeled on either the primary or secondary of the transformer. In actuality it could be anywhere in the middle, eg. 55% primary, 45% secondary but modeling it on one side only greatly simplifies the analysis. In the end it is only the total winding currents entering the black box that can ever be measured. The current through the magnetizing inductance can be calculated using standard circuit analysis techniques. The magnetic flux in the core of the transformer is a function of the current flowing through the magnetizing inductance as previously seen in figure 13. When the core is operating in the linear region of the ϕ/F curve the transformer flux can be modeled as (E.5):

$$\phi = \frac{Ni}{\Re} = \frac{F}{\Re} \tag{E.5}$$

where F is magneto motive force and i is the current flowing through the magnetizing inductance and $\Re$ is a constant linear region reluctance. Outside the linear region the core becomes magnetically saturated.

From figure E2 it can be determined that:

$$Ipri - ILm_p = N \cdot I\,\text{sec} \tag{E.6}$$

or

$$Ipri / N = I\,\text{sec} + ILm_s \tag{E.7}$$

where Lm_s reflected on the secondary is N^2Lm_p.

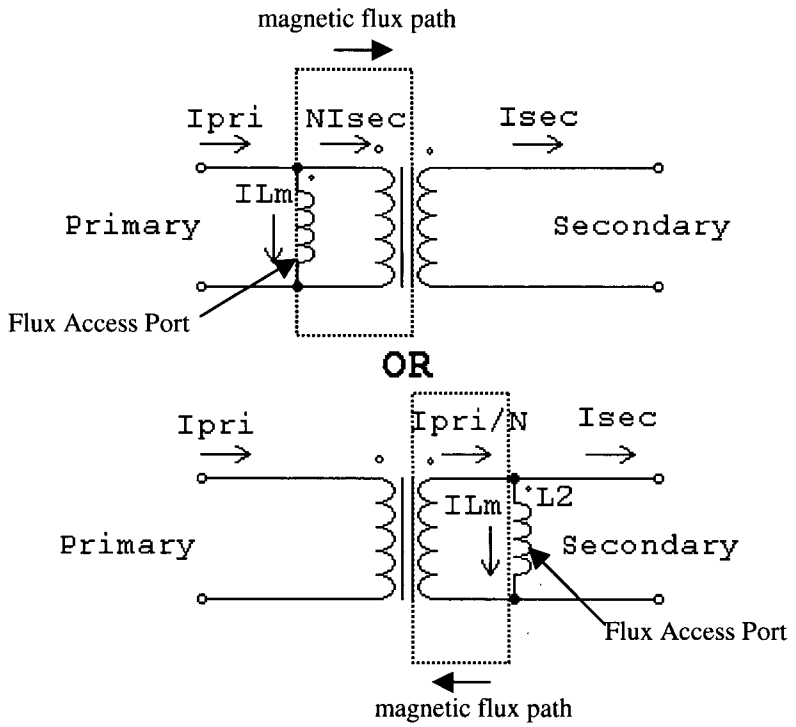


Figure E2: Two winding transformer model

(E.6) and (E.7) are essentially identical proving the magnetizing inductance can be modeled on either side of the transformer. The single, yet movable, magnetizing

inductance can be considered as an access port for manipulating the transformer core flux. For the two winding transformer model in figure E2 a single magnetic flux access port or magnetizing inductance is sufficient. It can be modeled on either on the secondary or primary. The choice is arbitrary.

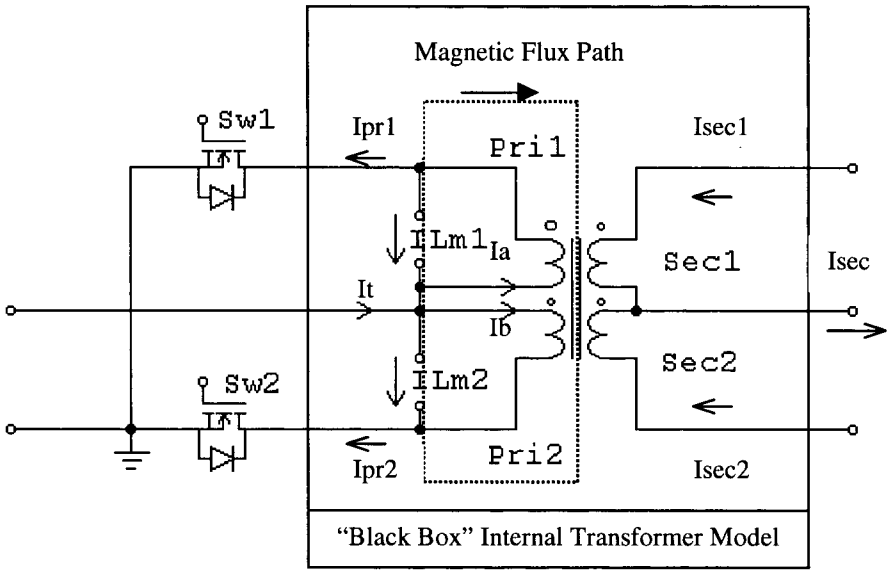


Figure E3: Proposed four winding Clarke converter transformer model

Modeling the magnetization of the thesis converter's four winding transformer becomes slightly more complex. In the two winding transformer model the magnetizing inductance, or magnetic flux access port, can be permanently modeled in a single location. When modeling the four winding transformer, the magnetic flux access can also be defined as exclusive to either the primary or secondary side. However, there are now two potential *port* locations per side to consider. For the purposes of this discussion only the primary side locations will be considered, although the overall results will be the same for a model with magnetization access on secondary. Figure E3 proposes a circuit to model the core magnetization properties of the four winding Clarke converter transformer. As will be seen, the location of where the magnetizing inductance appears depends on the switching state.

Equations can be written to explain the operation of the transformer model. With both switches closed:

$$VLm1 = VLm2 = Vpri1 = Vpri2 = 0 \tag{E.8}$$

$$\frac{d\phi}{dt} = 0 \tag{E.9}$$

$$\frac{diLm1}{dt} = \frac{diLm2}{dt} = 0 \tag{E.10}$$

$$ia = ib \tag{E.11}$$

$$it = ipr1 + ipr2 \tag{E.12}$$

And the relationship between ipr1 and ipr2 is described as:

$$im = ipri2 - ipri1 \tag{E.13}$$

where *im* is the equivalent magnetizing inductor current required to sustain the existing magnetic core flux, ϕ.

(E.13) can be derived by modeling *im* flowing through port *Lm1 or Lm2* or with any proportional split in between. This is an arbitrary split with no defined value. *ILm1* and *ILm2* can never really be known nor does it need to be. In any case (E.13) applies.

When *Sw1* is open and *Sw2* is closed the magnetizing inductance port, *Lm1*, is effectively removed from the circuit as no current flows through the primary winding, *Pri1*. Only *Lm2* remains as a flux access port to perform the circuit analysis with. For this open switch condition the following equations apply:

$$Vpri1 = Vpri2 = \frac{V\sec 1}{N} = \frac{V\sec 2}{N}$$

(E.14)

$$-\frac{d\phi}{dt} \propto Vpri2 = \frac{V\sec 1,2}{N}$$

(E.15)

$$\frac{\dim}{dt} = \frac{d\phi}{dt} \cdot \frac{l}{A \cdot \mu_r(H) \cdot T}$$

where μ_r is the relative permeability of the core and T is the core turns

(E.16)

$$\frac{diLm2}{dt} = \frac{\dim}{dt}$$

(E.17)

Flux access port, *Lm2,* is now where the full magnetizing inductance appears.

$$i\sec 2 = \frac{it - iLm2}{N}$$

(E.18)

When *Sw2* is open and *Sw1* is closed only magnetizing inductance port *Lm1* remains. Now only *Lm1* is available to perform the circuit analysis with. The following equations apply:

$$-Vpri1 = -Vpri2 = -\frac{V\sec 1}{N} = -\frac{V\sec 2}{N}$$

(E.19)

$$\frac{d\phi}{dt} \propto Vpri1 = \frac{V\sec 1,2}{N}$$

(E.20)

$$\frac{\dim}{dt} = \frac{d\phi}{dt} \cdot \frac{l}{A \cdot \mu_r(H) \cdot T}$$

(E.21)

where again μ_r is the relative permeability of the core and T is the core turns

$$\frac{diLm2}{dt} = \frac{\dim}{dt}$$

(E.22)

$$i\sec 2 = \frac{it + iLm1}{N}$$

(E.23)

Using a combination of the above equations and by manually defining the magnetic flux current, *im*, the effects of various magnetizing effects can be observed on the switching devices. The results of a MATLAB based analysis are presented in figures E4 and E5. The results demonstrate a Clarke converter under balanced conditions and the same Clarke converter with non-balanced flux and saturated transformer core. Inherently, at the time scale of switching periods, the Clarke converter demonstrates a near constant input current provided by the Clarke inductor. The near constant inductor current, *it*, and magnetizing current, *im*, are pre-defined and used as a base for the MATLAB waveform generation.

In figure E4 the converter is operating in a balanced and unsaturated condition. The magnetizing current, *im,* has zero dc offset and is relatively linear. There is some curvature of *im* to simulate the general BH characteristics of the core but it is nowhere near saturation. The waveforms are similar to the PSIM waveforms of the previous section. In figure E5 the magnetic flux is now unbalanced with a dc offset and has become saturated resulting in a large *im* saturation current. The following two significant points can be made about this condition:

1) one of the primary switches supports a larger RMS current and therefore more losses
2) one of the secondary switches experiences saturation current spikes, more RMS current and higher losses

In order to actively balance the core flux it is necessary to have some indication of when the core is unbalanced. The resultant MATLAB waveforms illustrate what happens when the flux is unbalanced and shows where the magnetizing current manifests itself vis-a-vis the switch currents. Evidently the magnetizing current required to support magnetic flux within the transformer core can be measured directly during the time that both switches are overlapped according to (E.13). A saturated core during this time produces a large magnetizing current. The large magnetizing current upsets the balance

of switch currents and may cause excessive heating. Additionally, if the reluctance –vs-magnetizing current property of the core is available the flux can be determined. The degree of flux balance can be easily determined by measuring and comparing the currents for each alternating switch overlap period. However, this would be practically difficult for the project converter as the all the sensor circuitry is required on the high voltage side of the transformer isolation.

The two waveform plots also indicate how to gauge transformer flux balance with sensor information from the secondary side only. In figure E5 the two different secondary current pulse shapes represent the currents through the two secondary switches. The pulse shapes have different areas depending on the balance of the flux. When the transformer core saturates the peak currents can become quite large. Flux balance can be achieved by controlling the switch timing to keep the current pulse areas equal. This is an attractive option for the thesis converter because the secondary current needs to be measured anyway to determine battery current. Although not discussed, an example of unbalanced flux can be found within the measured results of [1].

In this section the appearance of magnetizing current with respect to circuit operation has been described with the aid of a four winding transformer model. It can be concluded that operating the transformer with a dc offset in the magnetic flux produces unbalanced RMS currents in both the primary and secondary switching devices. This results in extra switch stressing and increased losses in general. The transformer flux can be actively balanced by controlling and equating the volt seconds impressed on the windings via switch timing adjustments. Measurement of the transformer secondary currents can provide the necessary control feedback signals.

However, this analysis of the magnetic flux balance and proposed control approach later proves unnecessary for implementation within the thesis converter since the measured flux appears to be naturally balanced. It is suspected that this is a result of the precise and symmetrical switch timing provided by the DSP combined with conservative core utilization. This section is nonetheless included here as the analysis and modeling tools may prove valuable for other transformer coupled dc/dc converter applications.

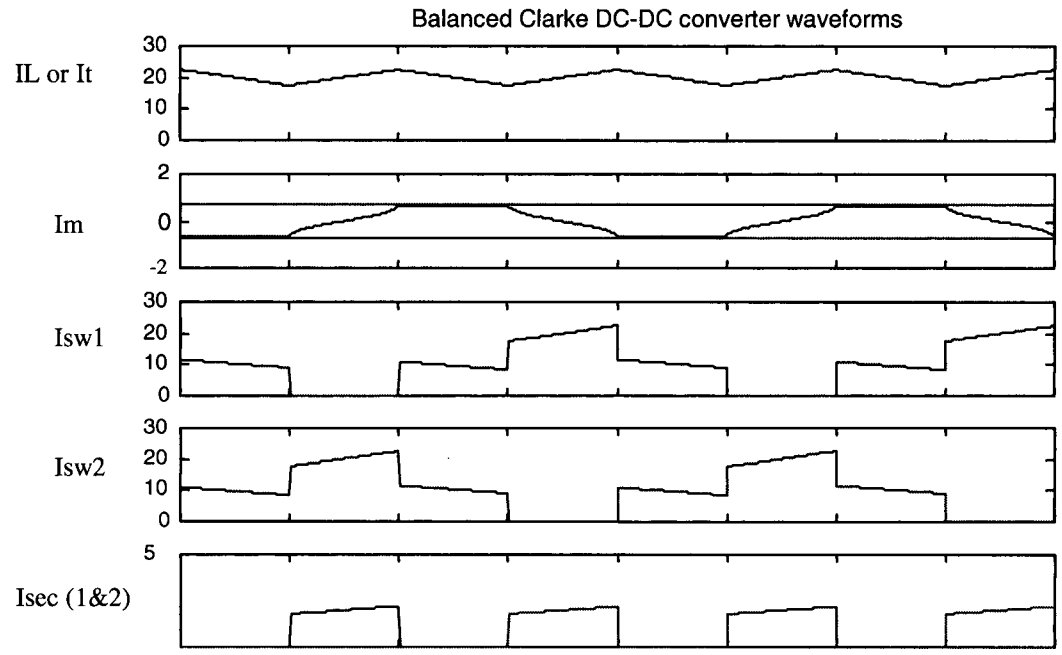


Figure E4: Clarke converter with unbalanced flux

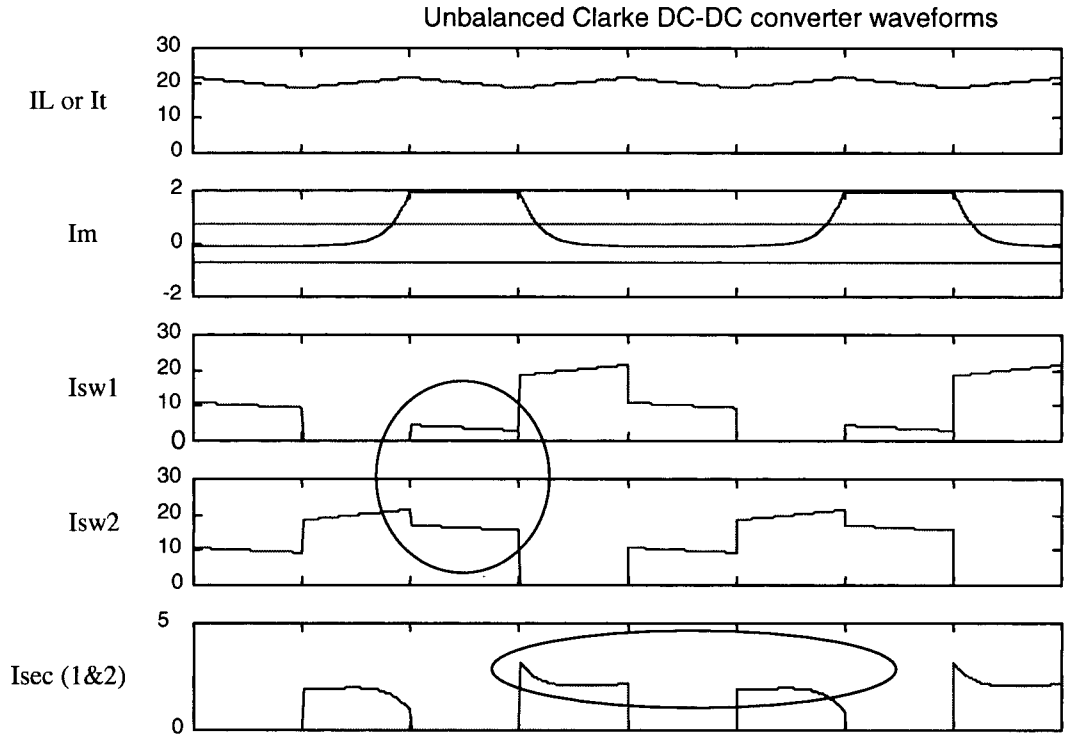


Figure E5: Clarke converter with unbalanced flux

Appendix F: MATLAB CODE - Power-Circuit Simulation

```
%******************   plant_simulation.m  *********************
%***Program Simulates Power Circuit Dynamic Operation**********
%*************** Andrew D Swingler, April 2003 ***************
% GIVEN POWER CIRCUIT INFORMATION
clear;
L =       .003;        %simulation time
Ts =      .000025;     %sample interval in seconds
L1=       13e-6;       %inductor value in Henerys
C1=       1e-6;        %dc bus capacitor in Farads
Rbat =    .0025;       %Battery Internal Resistance
R1 =      .040;        %RDSon of the low voltage switches
R2 =      .12;         %RDSon of the high voltage switches
N =       10;          %transformer turns ratio
R =       123;         %bus load resistance
x =       [25 ; 175]; %initial value state vector [I;V]
Vbat =    12;          %battery voltage
%************************************************************
% DEFINE STATE MATRICIES
A1 =      [ -( (1/((1/R1)+(1/R1)))+Rbat)/L1          0;
          0                                  -1/(R*C1)];

A2 =      [ -(Rbat+R2+(R2/N^2))/L1        -1/(N*L1);
          1/(N*C1)                  -1/(R*C1)];

B1 =      [1/L1;
           0 ];

B2 =      [1/L1;
           0];

for i = 1:(L/Ts)
   if i>(2*L)/(Ts*3)
       d = 0.45;
   elseif i>L/(Ts*3)
       d = 0.03;
   else
       d = 0.45;
   end

% AVERAGED STATE MATRICIES
A  =      d*A1 + (1-d)*A2;
B  =      d*B1 + (1-d)*B2;
C  =      [0 1];
D  =      [0];

[Ad,Bd,Cd,Dd] = c2dm(A,B,C,D,Ts,'zoh');
x = Ad*x + Bd*Vbat;
Time(i) = i*Ts;
x1(i) = x(1,1);
x2(i) = x(2,1);
end
plot(Time,x1,Time,x2)
```

Appendix G: MATLAB CODE - Closed Loop System Simulation

```
%********   CLOSED LOOP CONVERTER SIMULATION  *****************
%***Program Simulates Power Circuit Dynamic Operation**********
%*************** Andrew D Swingler, April 2003 ***************

% GIVEN POWER CIRCUIT INFORMATION
clear;
L =       .1;          %simulation time
Ts =      .000025;     %sample interval in seconds
L1=       20e-6;       %inductor value in Henerys
C1=       6e-6;        %dc bus capacitor in Farads
Rbat =    .0025;       %Battery Internal Resistance
R1 =      .040;        %RDSon of the low voltage switches
R2 =      .080;        %RDSon of the high voltage switches
N =       10;          %transformer turns ratio
R =       10e6;        %initial bus load resistance
x =       [25 ; 175]; %initial value state vector [I;V]
Vbatinternal = 12;     %initial battery internal voltage
d    =    0;           %initial duty cycle (0-1)
DC(1) =   0;           %initial 32bit duty cycle (0-128)
%************************************************************

for i = 1:(L/Ts)

% DEFINE STATE MATRICIES
A1 =      [ -( (1/((1/R1)+(1/R1)))+Rbat)/L1          0;
          0                                  -1/(R*C1)];

A2 =      [ -(Rbat+R2+(R2/N^2))/L1        -1/(N*L1);
          1/(N*C1)                  -1/(R*C1)];

B1 =      [1/L1;
           0 ];

B2 =      [1/L1;
           0];

Vbatinternal = Vbatinternal - (x(1,1)*.0001);

% AVERAGED STATE MATRICIES
A  =      d*A1 + (1-d)*A2;
B  =      d*B1 + (1-d)*B2;
C  =      [0 1];
D  =      [0];

[Ad,Bd,Cd,Dd] = c2dm(A,B,C,D,Ts,'zoh');

x = Ad*x + Bd*Vbatinternal; % Power Circuit Calculation

Time(i) = i*Ts;

%************TRANSIENT TIME CIRCUIT VARIATIONS*************
if i < L/(6*Ts) %Step Change From No Load to Full Load
   R=10E6;
```

```
else
   R=200;
end

if i > L/(3*Ts)
   x(2,1) = 225; %225V appears on the bus to Charge the battery.
end
%*******RUN input signal conditioning SIMULINK model**********
I(i) = x(1,1);
V(i) = x(2,1);

sim('adc_model',0.000025);

VBUSdata(i) = VBUS; % STORE DATA
IBATdata(i) = IBAT;
VBATdata(i) = VBAT;
%*******Control Mode Decision Making Algorithm***************
if VBUS < 20000
   M = 1;
elseif IBAT<-3000
   M = 2;
elseif VBAT>1400
   M = 3;
end
if M == 1
      B0=round(0.00009946*2^16);
      output = VBUS;
      setpoint = 20500; %200.00 Volts
elseif M == 2
      B0=round(.0003408*2^16);
      output = IBAT;
      setpoint = -3000; %-30.00 Amps
elseif M == 3
      B0=round(-.01363*2^16);
      output = VBAT;
      setpoint = 1400; %14.00 Volts
end

%*******RUN SIMULINK CONTROL CALCULATION***************
sim('controller_model',0.000025);
d = dutycycle;          %update quantized 0-1 dutycycle for the plant
model
DUTY(i) = dutycycle;    %store quantized 0-1 dutycyle for plotting
DC(i+1) = DUTYCYCLE;    %update 32 bit dutycycle for the SIMULINK
controller
end
figure(1),plot(Time,VBUSdata/100,Time,V), xlabel('time'),ylabel('BUS
VOLTAGE');
figure(2),plot(Time,VBATdata/100), xlabel('time'),ylabel('BATTERY
TERMINAL VOLTAGE');
figure(3),plot(Time,IBATdata/100,Time,I),
xlabel('time'),ylabel('BATTERY CURRENT');
figure(4),plot(Time,DUTY), xlabel('time'),ylabel('QUANTIZED DUTY
CYCLE');
```

Appendix H: DSP CODE – Assembly programming

```
*************************************************************************
* Filename: i_control.asm                                               *
* Requires: vectors.asm and x24x.h                                      *
*                                                                       *
* Author: Andrew Swingler                                               *
*                                                                       *
* Last Modified: 04/17/03                                               *
*                                                                       *
*                                                                       *
*************************************************************************

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Global symbol declarations
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
                .def start
                .def timer2_isr
                .def lookup_table
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Address definitions
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
                .include x24x.h

                  .bss  LEDS_ON,1
                  .bss  DC,1              ;Duty Cycle: 0 to 128
                  .bss  V,1
                  .bss  I,1
                  .bss  IBAT,1
                  .bss  VBUS,1
                  .bss  VBAT,1
                  .bss  DC_COMP,1
                  .bss  TEMP,1
                  .bss  MODE,1
                  .bss  REF,1
                  .bss  OUT,1
                  .bss  E,1
                  .bss  GAIN,1
                  .bss  GEL,1
                  .bss  GEH,1
                  .bss  D1L,1
                  .bss  D1H,1
                  .bss  DL,1
                  .bss  DH,1


DAC0            .set    0000h       ;EVM DAC register 0 (I/O space)
DAC1            .set    0001h       ;EVM DAC register 1 (I/O space)
DAC2            .set    0002h       ;EVM DAC register 2 (I/O space)
DAC3            .set    0003h       ;EVM DAC register 3 (I/O space)
DACUD           .set    0004h       ;EVM DAC update register (I/O space)
DIPSWCH         .set    0008h       ;EVM DIP switch (I/O space)
LED             .set    000Ch       ;EVM LED bank (I/O space)

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
;Constant definitions
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

DC_MDPT         .set    0080h
DC_ADJ_MAX      .set    0050h
DC_ADJ_MIN      .set    0002h


;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Uninitialized global variable definitions
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
         .bss   TEMP1,1
         .bss   LED_index,1     ;LED index

                        .data
lookup_table:     ;lookup table = 16*128/[128-DC] to achieve correct
resolution
        .word   16,16,16,16,16,16,16,17,17,17,17,17,17,17,18,18
        .word   18,18,18,18,19,19,19,19,19,20,20,20,20,20,21,21
        .word   21,21,22,22,22,22,23,23,23,23,24,24,24,24,25,25
        .word   25,26,26,26,27,27,28,28,28,29,29,30,30,31,31,32
        .word   32,33,33,34,34,35,35,36,37,37,38,39,40,40,41,42
        .word   43,44,45,46,47,48,49,51,52,53,55,56,58,60,62,64
        .word   66,68,70,73,75,78,81,85,89,93,97,102,107,113,120,128
        .word
136,146,157,170,186,204,227,256,292,341,409,512,682,1024,2048


*************************************************************************
*                       M A I N   R O U T I N E                         *
*************************************************************************

                .text
start:

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Initialize Variables
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
      LDP   #LEDS_ON
      SPLK  #0,LEDS_ON
      SPLK  #0,DC
      SPLK  #0,DC_COMP
      SPLK  #0,IBAT
      SPLK  #0,VBUS
      SPLK  #0,VBAT
      SPLK  #0,TEMP
      SPLK  #0,e
      SPLK  #0,GEL
      SPLK  #0,GEH
      SPLK  #0,D1L
      SPLK  #0,D1H
      SPLK  #0,DL
      SPLK  #0,DH
      SPLK  #0,MODE
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Configure the System Control and Status Registers
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

```
        LDP   #DP_PF1          ;set data page

        SETC  OVM               ;set overflow mode.

         ;SPLK    #0000000000000001b, SCSR
*                  ||||||||||||||||
*                  FEDCBA9876543210
* bit 15          0:      reserved
* bit 14          0:      CLKOUT = CPUCLK
* bit 13-12       00:     IDLE1 selected for low-power mode
* bit 11-9        000:    reserved
* bit 8           0:      reserved
* bit 7           0:      reserved
* bit 6           0:      reserved
* bit 5           0:      reserved
* bit 4           0:      reserved
* bit 3           0:      reserved
* bit 2           0:      reserved
* bit 1           0:      reserved
* bit 0           1:      clear the ILLADR bit


;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Disable the watchdog timer
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        LDP     #DP_PF1                 ;set data page

        SPLK    #0000000011101000b, WDCR
*                  ||||||||||||||||
*                  FEDCBA9876543210
* bits 15-8       0's     reserved
* bit 7           1:      clear WD flag
* bit 6           1:      disable the dog
* bit 5-3         101:    must be written as 101
* bit 2-0         000:    WDCLK divider = 1

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Setup external memory interface for LF2407 EVM
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        LDP     #temp1                  ;set data page

        SPLK    #0000000001000000b, temp1
*                  ||||||||||||||||
*                  FEDCBA9876543210
* bit 15-11       0's:    reserved
* bit 10-9        00:     bus visibility off
* bit 8-6         001:    1 wait-state for I/O space
* bit 5-3         000:    0 wait-state for data space
* bit 2-0         000:    0 wait state for program space

        OUT     temp1, WSGR

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Setup shared I/O pins
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        LDP     #DP_PF2                 ;set data page
```

```
        SPLK    #00000001111000000b,OCRA ;group A pins
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15        0:      0=IOPB7,      1=TCLKIN
* bit 14        0:      0=IOPB6,      1=TDIR
* bit 13        0:      0=IOPB5,      1=T2PWM/T2CMP
* bit 12        0:      0=IOPB4,      1=T1PWM/T1CMP
* bit 11        0:      0=IOPB3,      1=PWM6
* bit 10        0:      0=IOPB2,      1=PWM5
* bit 9         0:      0=IOPB1,      1=PWM4
* bit 8         0:      0=IOPB0,      1=PWM3
* bit 7         0:      0=IOPA7,      1=PWM2
* bit 6         1:      0=IOPA6,      1=PWM1
* bit 5         0:      0=IOPA5,      1=CAP3
* bit 4         0:      0=IOPA4,      1=CAP2/QEP2
* bit 3         0:      0=IOPA3,      1=CAP1/QEP1
* bit 2         0:      0=IOPA2,      1=XINT1
* bit 1         0:      0=IOPA1,      1=SCIRXD
* bit 0         0:      0=IOPA0,      1=SCITXD

        SPLK    #1111111000000011b,OCRB ;group B pins
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15        1:      0=reserved,  1=TMS2 (always write as 1)
* bit 14        1:      0=reserved,  1=TMS  (always write as 1)
* bit 13        1:      0=reserved,  1=TD0  (always write as 1)
* bit 12        1:      0=reserved,  1=TDI  (always write as 1)
* bit 11        1:      0=reserved,  1=TCK  (always write as 1)
* bit 10        1:      0=reserved,  1=EMU1 (always write as 1)
* bit 9         1:      0=reserved,  1=EMU0 (always write as 1)
* bit 8         0:      0=IOPD0,      1=XINT2/ADCSOC
* bit 7         0:      0=IOPC7,      1=CANRX
* bit 6         0:      0=IOPC6,      1=CANTX
* bit 5         0:      0=IOPC5,      1=SPISTE
* bit 4         0:      0=IOPC4,      1=SPICLK
* bit 3         0:      0=IOPC3,      1=SPISOMI
* bit 2         0:      0=IOPC2,      1=SPISIMO
* bit 1         0:      1=IOPC1,      0=BIO*
* bit 0         0:      1=IOPC0,      0=XF



;-------------------------------------------------------------------------
;Setup the software stack
;-------------------------------------------------------------------------
stk_len         .set    100             ;stack length
stk             .usect  "my_stack",stk_len  ;reserve space for stack

        LAR     AR1, #stk               ;AR1 is the stack pointer

;-------------------------------------------------------------------------
;Setup timers 1 and 2, and the PWM configuration
;-------------------------------------------------------------------------
        LDP     #DP_EVA                 ;set data page
        SPLK    #0000h, T1CON           ;disable timer 1
```

```
        SPLK    #0000h, T2CON           ;disable timer 2

        SPLK    #000000000000000b, GPTCON
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15         0:      reserved
* bit 14         0:      T2STAT, read-only
* bit 13         0:      T1STAT, read-only
* bit 12-11      00:     reserved
* bit 10-9       00:     T2TOADC, 00 = no timer2 event starts ADC
* bit 8-7        00:     T1TOADC, 00 = no timer1 event starts ADC
* bit 6          0:      TCOMPOE, 0 = Hi-z all timer compare outputs
* bit 5-4        00:     reserved
* bit 3-2        00:     T2PIN, 00 = forced low
* bit 1-0        00:     T1PIN, 00 = forced low

;Timer 1: Configure to clock the PWMs
;Symmetric PWM, 40KHz carrier frequency
        SPLK    #0000h, T1CNT           ;clear timer counter
        SPLK    #0100h, T1PR            ;set timer period
        SPLK    #0000h, DBTCON          ;deadband units off
        SPLK    #DC_MDPT, CMPR1         ;set PWM duty cycle
        SPLK    #DC_MDPT, CMPR2         ;set PWM duty cycle

        SPLK    #0000000010010110b, ACTR
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15         0:      space vector dir is CCW (don't care)
* bit 14-12      000:    basic space vector is 000 (dont' care)
* bit 11-10      00:     PWM6/IOPB3 pin forced low
* bit 9-8        00:     PWM5/IOPB2 pin forced low
* bit 7-6        10:     PWM4/IOPB1 pin active high
* bit 5-4        01:     PWM3/IOPB0 pin active low
* bit 3-2        01:     PWM2/IOPA7 pin active low
* bit 1-0        10:     PWM1/IOPA6 pin active high

        SPLK    #1100001000000000b, COMCON
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15         1:      1 = enable compare operation
* bit 14-13      00:     00 = reload CMPRx regs on timer 1 underflow
* bit 12         0:      0 = space vector disabled
* bit 11-10      00:     00 = reload ACTR on timer 1 underflow
* bit 9          1:      1 = enable PWM pins
* bit 8          0:      PDPINTB STATUS in F2407A: reserved in F2407
* bit 7-0        0's:    reserved

        SPLK    #1110100001000000b, T1CON
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 15-14      00:     stop immediately on emulator suspend
* bit 13         0:      reserved
* bit 12-11      01:     01 = continous-up/down count mode
* bit 10-8       000:    000 = x/1 prescaler
* bit 7          0:      reserved in T1CON
* bit 6          1:      TENABLE, 1 = enable timer
* bit 5-4        00:     00 = CPUCLK is clock source
```

```
* bit 3-2        00:     00 = reload compare reg on underflow
* bit 1          0:      0 = disable timer compare
* bit 0          0:      reserved in T1CON

;Timer 2: configure to generate a ~25us periodic interrupt
        SPLK    #0000h, T2CNT           ;clear timer counter
        SPLK    #01FFh, T2PR              ;set timer period

        SPLK    #1101000001000000b, T2CON
*                |||||||||||||||
*                FEDCBA9876543210
* bit 15-14      11:     stop immediately on emulator suspend
* bit 13         0:      reserved
* bit 12-11      10:     10 = continous-up count mode
* bit 10-8       111:    111 = x/128 prescaler
* bit 7          0:      T2SWT1, 0 = use own TENABLE bit
* bit 6          1:      TENABLE, 1 = enable timer
* bit 5-4        00:     00 = CPUCLK is clock source
* bit 3-2        00:     00 = reload compare reg on underflow
* bit 1          0:      0 = disable timer compare
* bit 0          0:      SELT1PR, 0 = use own period register

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;PWM setup
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;LED index initialization
        LDP     #LED_index              ;set data page
        SPLK    #1h, LED_index          ;initialize the LED index

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Setup the core interrupts
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        LDP     #0                      ;set data page
        SPLK    #0h,IMR                 ;clear the IMR register
        SPLK    #111111b,IFR            ;clear any pending core
interrupts
        SPLK    #000100b,IMR            ;enable desired core interrupts

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Setup the event manager interrupts
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        LDP     #DP_EVA         ;set data page
        SPLK    #0FFFFh, EVIFR  ;clear all EVA group A interrupts
        SPLK    #0FFFFh, EVIFRB ;clear all EVA group B interrupts
        SPLK    #0FFFFh, EVIFRC ;clear all EVA group C interrupts
        SPLK    #00000h, EVIMRA ;enabled desired EVA group A interrupts
        SPLK    #00001h, EVIMRB ;enabled desired EVA group B interrupts
        SPLK    #00000h, EVIMRC ;enabled desired EVA group C interrupts

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Setup ADC
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

ADC_INIT

      LDP   #224
```

```
      SPLK  #0000000000000000b, ADCTRL2
*                ||||||||||||||||
*                FEDCBA9876543210
* bit 2-0       three bit ADC clock prescaler


;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Enable global interrupts
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        CLRC    INTM                    ;enable global interrupts

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;Main loop
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

loop:
         NOP
         B      loop                    ;branch to loop


*************************************************************************
*  I N T E R R U P T  S E R V I C E  R O U T I N E                      *
*************************************************************************

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
;GP Timer 2 period interrupt (core interrupt INT3)
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

timer2_isr:

;toggle the IOPC0 pin for control loop time observation
        LDP     #DP_PF2                 ;set data page
        LACC    #0101h                  ;ACC = 0001h
        SACL    PCDATDIR                ;store result to PCDATDIR
;Context save to the software stack
        MAR     *,AR1                   ;ARP=stack pointer
        MAR     *+                      ;skip one stack location
(required)
        SST     #1,*+                  ;save ST1
        SST     #0,*+                  ;save ST0
        SACH    *+                     ;save ACCH
        SACL    *+                     ;save ACCL

;Clear the T2PINT interrupt flag
        LDP     #DP_EVA                 ;set data page
        SPLK    #00001h, EVIFRB         ;clear T2PINT flag

SAMPLE_I_and_V:

      LDP   #224
      SPLK  #0101100000110101b, ADCTRL1   ;reconfigure the control regs
*             ||||||||||||||||
*             FEDCBA9876543210

      RPT   #50               ;wait for ADC conversion
      NOP
      CLRC  SXM          ;or FIFO high goes all ones after 512
```

```
      LACC  ADCFIFO1,10
      LDP   #V
      SACH  V
      LDP   #224
      LACC  ADCFIFO2,10
      LDP   #I
      SACH  I

*****************************************************************

* UPDATE THE PWM DUTYCYCLE
*
*****************************************************************

DUTY_CYCLE_UPDATE:
      LDP     #DC
      LACL    #DC_MDPT
      ADD     DC
      LDP     #DP_EVA
      SACL    CMPR2     ;adjust compare 1 point
      LDP     #DC
      LACC    #DC_MDPT
      SUB     DC
      LDP     #DP_EVA
      SACL    CMPR1       ;adjust compare 2 point

*****************************************************************
*   DUTY CYCLE NON-NONEAR COMPENSATION FACTOR TABLE LOOKUP      *
*   uses lookup table to perform 1/[1-D] resulting in           *
*     DC_COMP = 16*[1/[1-DC_ADJ/128]]                          *
*****************************************************************

      MAR   *,AR0  ;load address register pointer with 0 (?)
      LDP   #DC    ;load datapage for DC
      LAR   AR0,DC ;load auxreg 0 with the duty cycle offset (0 to 128)
      MAR   *,AR6  ;load address register pointer with 6
      LDP   #lookup_table ;load datapage for lookup_table (?)
      LAR   AR6,#lookup_table ;load auxreg 6 with lookup_table address
      LACC  *0+   ;add dutycycle offset in AR0 to contents of AR6
      LACC  *    ;load acc with contents of address referenced by AR6
      LDP   #DC_COMP                ;
      SACL  DC_COMP ;store the contents of the lookuptable in DC_COMP

*****************************************************************
*   BATTERY CURRENT CALCULATION                                 *
*   USING LEVEL SHIFT AND NON-LINEAR SCALING                    *
*     calculates IBAT = IaveSw4*2*N/[1-D]  (equation 2.1.2) using *
*     IBAT = [DC_COMP/16] * [625/64] * [CURRENT-512]            *
*     where
                *
*   -512 to +512 = -5000 to 5000 or -50.00A to 50.00A @ DC = 1  *
*   condition input signal to acheive -2.5A to 2.5A = 0-5V      *
*****************************************************************

        SETC      SXM    ;set sign extension mode
        LDP #I
        LACL      I      ;load CURRENT into the lower accumulator
```

```
        SUB   #512       ;ZERO BIAS level shift
        SACL      I
        LT    I
        LDP   #DC_COMP
        MPY   DC_COMP
        PAC         ;put the product register in the accumulator
        SFR         ;shift the acc right four times to divide by 16
        SFR
        SFR
        SFR
        SACL  TEMP
        LT    TEMP
        MPY   #625
        PAC
        SFR       ;shift the acc right six times to divide by 64
        SFR
        SFR
        SFR
        SFR
        SFR
        LDP   #IBAT
        SACL  IBAT

*****************************************************************

* BATTERY VOLTAGE AND BUS VOLTAGE CALCULATIONS                   *
*                                                                *
* VBUS = V*100/4    -> 0-1023 = 000.00V - 265.00V                *
*                                                                *
* VBAT = V*(1-D)/N    (equation 2.1.3)                           *
* VBAT = V*[[128-DC]/128]*[10/4] -> 0-1023 = 000.00V - 026.50V   *
*                                                                *
*****************************************************************

 ;scale V to result in VBUS XXX.XX volts
      SETC  SXM
      LDP   #V
      LACL  V
      LT    V
      MPY   #100
      PAC
      SFR
      SFR
      LDP   #VBUS
      SACL  VBUS

 ;calculate battery voltage from V to result in VBAT XXX.XX volts;
      LACL  #128
      LDP   #DC
      SUB   DC
      LDP   #TEMP      ;TEMP = 128-DC
      SACL  TEMP
      LT    TEMP
      LDP   #V
      MPY   V          ; = V*[128-DC]
      PA
      SFR
```

```
        SFR
        SFR
        SFR
        SFR
        SFR
        SFR
        LDP   #TEMP
        SACL  TEMP
        LT    TEMP     ; = V*[[128-DC]/128
        MPY   #10
        PAC
        SFR
        SFR
        SACL      VBAT     ; = V*[[128-DC]/128]*[10/4]

*********************************************************************

* CONTROL MODE DECISION MAKING ALGORITHM
*
*********************************************************************

CONTROL_MODE_DECISION:
      SETC  SXM

      ;branch to new control mode
      LDP   #VBUS
      LACL  VBUS
      SUB   #20000
      BCND  BUS_VOLTAGE_REGULATION,LT

      LDP   #IBAT
      LACC  IBAT
      ADD   #2000
      BCND  CHARGE_CURRENT_REGULATION,LEQ

      LDP   #VBAT
      LACC  VBAT
      SUB   #1400
      BCND  CHARGE_VOLTAGE_REGULATION,GT


      ; if there is no mode change then use previous mode
      LDP   #MODE
      LACL  MODE
      SUB   #1
      BCND  BUS_VOLTAGE_REGULATION,EQ
      SUB   #1
      BCND  CHARGE_CURRENT_REGULATION,EQ
      SUB   #1
      BCND  CHARGE_VOLTAGE_REGULATION,EQ
      B     CONTROL_CALCULATION

BUS_VOLTAGE_REGULATION:
      LDP   #GAIN
      SPLK  #8 ,GAIN  ;GAIN = B0*1.28 = .00009946*2^16*1.28 = 8.34
      LDP   #REF
      SPLK  #20000,REF
```

```
        LDP   #VBUS
        LACL  VBUS
        LDP   #OUT
        SACL  OUT
        LDP   #MODE
        SPLK  #1,MODE
        B     CONTROL_CALCULATION

CHARGE_CURRENT_REGULATION:
        LDP   #GAIN
        SPLK  #3,GAIN  ;GAIN = B0*1.28 = .00003408*2^16*1.28 = 2.858
        LDP   #REF
        SPLK  #-2000,REF
        LDP   #IBAT
        LACL  IBAT
        LDP   #OUT
        SACL  OUT
        SPLK  #2,MODE
        B     CONTROL_CALCULATION

CHARGE_VOLTAGE_REGULATION:
        LDP   #GAIN
        SPLK  #-1143,GAIN  ; GAIN = B0*1.28 =-.01363*2^16*1.28 = -1143.36
        LDP   #REF
        SPLK  #1400,REF
        LDP   #VBAT
        LACL  VBAT
        LDP   #OUT
        SACL  OUT
        SPLK  #3,MODE
        B     CONTROL_CALCULATION



*****************************************************************

* CONTROL CALCULATION                                           *
*                                                               *
* from the SIMULINK model: 2^-16*128*B0/100 = 1.28*B0*2^-16     *
*
* where REF = SETPOINT, OUT = OUTPUT, GAIN = B0*1.28            *
*                                                               *
*****************************************************************

CONTROL_CALCULATION:
        SETC  SXM
        SETC  OVM
        LDP   #REF
        LACL  REF
        LDP   #OUT
        SUB   OUT   ;16 bit error XXX.XX
        LDP   #E
        SACL  E
        LT    E     ;put error into TREG
        LDP   #GAIN
        MPY   GAIN  ;32 bit gain*error: GE
        LDP   #GEH
```

```
        SPH  GEH      ;store the integer part in GEH
        LDP  #GEL
        SPL  GEL      ;store the fractional part in GEL
        PAC           ;ACC now holds 32 bit GE

        LDP  #DL      ;D1 is the 32 bit historical duty cycle
        LT   DL
        MPY  #1       ;D1L now in low product reg
        LDP  #DH
        LPH  DH       ;D1H n0w in high product reg
        APAC          ;ACC = GE + D1 (32BIT) addition
        LDP  #DC
        SACH DC       ;store the high accumulator as the duty cycle
        LDP  #DL      ;update the duty-cycle
        SACL DL
        LDP  #DH
        SACH DH

*****************************************************************

* SET DUTY CYCLE SATURATION LIMITS AND PREVENT INTEGRATOR WINDUP  *
*****************************************************************

DC_LIMITS:
       SETC  SXM
       LDP   #DC
       LACC  DC
       SUB   #DC_ADJ_MIN
       BCND  SET_MIN_DC,LT
       LACC  DC
       SUB   #DC_ADJ_MAX
       BCND  SET_MAX_DC,GT
       B     LED_DC_METER
SET_MIN_DC:
       LDP   #DC
       LACC  #DC_ADJ_MIN
       SACL  DC
       LDP   #DH    ;anti integrator windup
       SACL  DH
       B     LED_DC_METER
SET_MAX_DC:
       LDP   #DC
       LACC  #DC_ADJ_MAX
       SACL  DC
       LDP   #DH     ;anti integrator windup
       SACL  DH
       B     LED_DC_METER

*****************************************************************

* SET EVM LEDS TO INDICATE THE DUTY CYCLE

*****************************************************************

LED_DC_METER:                              ;DUTY CYCLE IS 0-128 -> 0-1
       CLRC  SXM
       LACL  DC
```

```
      SUB   #26
      BCND  DC_LT2,LT          ;DUTY CYCLE IS 0 - 0.2
      LACL  DC
      SUB   #38
      BCND  DC_LT3,LT         ;DUTY CYCLE IS 0.2 - 0.3
      LACL  DC
      SUB   #51
      BCND  DC_LT4,LT         ;DUTY CYCLE IS 0.3 - 0.4
      LACL  DC
      SUB   #64
      BCND  DC_LT5,LT         ;DUTY CYCLE IS 0.4 - 0.5
      LACL  DC
      SUB   #77
      BCND  DC_LT6,LT         ;DUTY CYCLE IS 0.5 - 0.6
      SPLK  #000Ah,LEDS_ON
      OUT   LEDS_ON,000Ch     ;DUTY CYCLE IS 0.6 - 1.0
      B           CONTROL_CALC_COMPLETE
DC_LT2:
      SPLK  #0005h,LEDS_ON
      OUT   LEDS_ON,000Ch
      B           CONTROL_CALC_COMPLETE
DC_LT3:
      SPLK  #0001h,LEDS_ON
      OUT   LEDS_ON,000Ch
      B     CONTROL_CALC_COMPLETE
DC_LT4:
      SPLK  #0002h,LEDS_ON
      OUT   LEDS_ON,000Ch
      B     CONTROL_CALC_COMPLETE
DC_LT5:
      SPLK  #0004h,LEDS_ON
      OUT   LEDS_ON,000Ch
      B     CONTROL_CALC_COMPLETE
DC_LT6:
      SPLK  #0008h,LEDS_ON
      OUT   LEDS_ON,000Ch
      B     CONTROL_CALC_COMPLETE

CONTROL_CALC_COMPLETE:

      ;toggle the IOPC0 pin down for control loop timing observation
      LDP   #DP_PF2             ;set data page
      LACC  #0100h              ;ACC = 0001h
      SACL  PCDATDIR            ;store result to PCDATDIR

      ;context restore from the software stack
      MAR   *, AR1              ;ARP = AR1
      MAR   *-                  ;SP points to last entry
      LACL  *-                  ;restore ACCL
      ADD   *-,16               ;restore ACCH
      LST   #0,*-               ;restore ST0
      LST   #1,*-               ;restore ST1, unskip one stack l
      CLRC  INTM                ;re-enable interrupts


    RET                         ;return from the interrupt
```

```
;*************************************************************************
;* Filename: vectors.asm                                                 *
;*                                                                       *
;* Author: David M. Alter, Texas Instruments Inc.                        *
;*                                                                       *
;* Last Modified: 03/14/01                                               *
;*                                                                       *
;* Description: Interrupt vector table for '240x DSP core                *
;* for use with assembly language programs.                              *
;*                                                                       *
;*************************************************************************

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***********************************************************************


      .ref start, timer2_isr

.sect    "vectors"
reset:   B       start          ;00h reset
int1:    B       int1           ;02h INT1
int2:    B       int2           ;04h INT2
int3:    B       timer2_isr     ;06h INT3
int4:    B       int4           ;08h INT4
int5:    B       int5           ;0Ah INT5
int6:    B       int6           ;0Ch INT6
int7:    B       int7           ;0Eh reserved
int8:    B       int8           ;10h INT8  (software)
int9:    B       int9           ;12h INT9  (software)
int10:   B       int10          ;14h INT10 (software)
int11:   B       int11          ;16h INT11 (software)
int12:   B       int12          ;18h INT12 (software)
int13:   B       int13          ;1Ah INT13 (software)
int14:   B       int14          ;1Ch INT14 (software)
int15:   B       int15          ;1Eh INT15 (software)
int16:   B       int16          ;20h INT16 (software)
int17:   B       int17          ;22h TRAP
int18:   B       int18          ;24h NMI
int19:   B       int19          ;26h reserved
int20:   B       int20          ;28h INT20 (software)
int21:   B       int21          ;2Ah INT21 (software)
int22:   B       int22          ;2Ch INT22 (software)
int23:   B       int23          ;2Eh INT23 (software)
int24:   B       int24          ;30h INT24 (software)
int25:   B       int25          ;32h INT25 (software)
int26:   B       int26          ;34h INT26 (software)
int27:   B       int27          ;36h INT27 (software)
int28:   B       int28          ;38h INT28 (software)
int29:   B       int29          ;3Ah INT29 (software)
int30:   B       int30          ;3Ch INT30 (software)
int31:   B       int31          ;3Eh INT31 (software)
```

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;***********************************************************************
; File name:       X24x.h
; Project:         F241/243 silicon functional test
; Originator:      DSP Digital Control Systems (DCS) Group (Houston)
;
; Description:     F240-3/C240-3 register definitions.
;_____________________________________________________________________
;Date of Mod       |                  Description
;---------------------------------------------------------------------
; Jan. 15, 1998    | Created from header file used by design
;---------------------------------------------------------------------
; Data memory mapped registers
;---------------------------------------------------------------------

; C2xx core registers
IMR          .set 0004h          ; Interrupt Mask Register
GREG         .set 0005h          ; Global memory allocation Register
IFR          .set 0006h          ; Interrupt Flag Register

; System configuration and interrupt registers
SYSCR        .set 7018h          ; System Module Control Register. X240
only.
SYSSR        .set 701Ah          ; System Module Status Register. X240
only.
SYSIVR       .set 701Eh          ; System Interrupt Vector Register. X240
only.

SCSR         .set 7018h          ; System Control & System Status Reg.
X241/2/3 only.
DIN          .set 701Ch          ; Device Identification Register.
PIVR         .set 701Eh          ; Peripheral Interrupt Vector Reg.
X241/2/3 only.
PIRQR0       .set 7010h          ; Peripheral Interrupt Request Reg 0.
X241/2/3 only.
PIRQR1       .set 7011h          ; Peripheral Interrupt Request Reg 1.
X241/2/3 only.

; PLL configuration registers
CKCR0        .set 702ah          ; PLL Clock Control Register 0. X240
only.
CKCR1        .set 702ch          ; PLL Clock Control Register 1. X240
only.

; External interrupt configuration registers
XINT1CR      .set 7070h          ; Int1 (type A) Control reg for X240
only.
                                 ; External interrupt 1 config reg for
X241/2/3 only.
NMICR        .set 7072h          ; Non maskable Int (type A) Control reg.
X240 only.
XINT2CR240   .set 7078h          ; Int2 (type C) Control reg. X240 only.
XINT2CR241   .set 7071h          ; External interrupt 2 config. X241/2/3
only.
XINT3CR      .set 707Ah          ; Int3 (type C) Control reg. X240 only.

; Digital I/O registers
OCRA         .set 7090h          ; Output Control Reg A
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OCRB        .set 7092h        ; Output Control Reg B
ISRA        .set  7094h ;Input Status Reg A. X240 only
ISRB        .set  7096h ;Input Status Reg B. X240 only
PADATDIR    .set 7098h        ; I/O port A Data & Direction reg.
PBDATDIR    .set 709Ah        ; I/O port B Data & Direction reg.
PCDATDIR    .set 709Ch        ; I/O port C Data & Direction reg.
PDDATDIR    .set 709Eh        ; I/O port D Data & Direction reg.

; Watchdog (WD) registers
WDCNTR      .set 7023h        ; WD Counter reg
WDKEY       .set 7025h        ; WD Key reg
WDCR        .set 7029h        ; WD Control reg

; Real Time Interrupt registers
RTICNTR     .set 7021h        ; RTI counter reg. X240 only.
RTICR       .set 7027h        ; RTI control reg. X240 only.

; ADC registers
ADCTRL1     .set 7032h        ; ADC Control Reg1
ADCTRL2     .set 7034h        ; ADC Control Reg2
ADCFIFO1    .set 7036h        ; ADC DATA REG FIFO for ADC1
ADCFIFO2    .set 7038h        ; ADC DATA REG FIFO for ADC2

; SPI registers
SPICCR      .set 7040h        ; SPI Config Control Reg
SPICTL      .set 7041h        ; SPI Operation Control Reg
SPISTS      .set 7042h        ; SPI Status Reg
SPIBRR      .set 7044h        ; SPI Baud rate control reg
SPIRXEMU    .set 7046h        ; SPI Emulation buffer reg
SPIRXBUF    .set 7047h        ; SPI Serial receive buffer reg
SPITXBUF    .set 7048h        ; SPI Serial transmit buffer reg
SPIDAT      .set 7049h        ; SPI Serial data reg
SPIPC1      .set 704Dh        ; SPI Port Control Register 1. X240 only.
SPIPC2      .set 704Eh        ; SPI Port Control Register 2. X240 only.
SPIPRI      .set 704Fh        ; SPI Priority control reg

; SCI registers
SCICCR      .set 7050h        ; SCI Communication control reg
SCICTL1     .set 7051h        ; SCI Control reg1
SCIHBAUD    .set 7052h        ; SCI Baud Rate MSbyte reg
SCILBAUD    .set 7053h        ; SCI Baud Rate LSbyte reg
SCICTL2     .set 7054h        ; SCI Control reg2
SCIRXST     .set 7055h        ; SCI Receiver Status reg
SCIRXEMU    .set 7056h        ; SCI Emulation Data Buffer reg
SCIRXBUF    .set 7057h        ; SCI Receiver Data buffer reg
SCITXBUF    .set 7059h        ; SCI Transmit Data buffer reg
SCIPC2      .set 705Eh        ; SCI Port Control reg2 (X240 only)
SCIPRI      .set 705Fh        ; SCI Priority control reg

; Event Manager (EV) registers
GPTCON      .set 7400h        ; GP Timer control register.
T1CNT       .set 7401h        ; GP Timer 1 counter register.
T1CMPR      .set 7402h        ; GP Timer 1 compare register.
T1PR        .set 7403h        ; GP Timer 1 period register.
T1CON       .set 7404h        ; GP Timer 1 control register.
T2CNT       .set 7405h        ; GP Timer 2 counter register.
T2CMPR      .set 7406h        ; GP Timer 2 compare register.
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T2PR        .set 7407h        ; GP Timer 2 period register.
T2CON       .set 7408h        ; GP Timer 2 control register.
T3CNT       .set 7409h        ; GP Timer 3 counter register. X240 only.
T3CMPR      .set 740Ah        ; GP Timer 3 compare register.  X240
only.
T3PR        .set 740Bh        ; GP Timer 3 period register.  X240 only.
T3CON       .set 740Ch        ; GP Timer 3 control register. X240 only.

COMCON      .set 7411h        ; Compare control register.
ACTR        .set 7413h        ; Full compare action control register.
SACTR       .set 7414h        ; Simple compare action control register.
DBTCON      .set 7415h        ; Dead-band timer control register.

CMPR1       .set 7417h        ; Full compare unit compare register1.
CMPR2       .set 7418h        ; Full compare unit compare register2.
CMPR3       .set 7419h        ; Full compare unit compare register3.

SCMPR1      .set 741Ah        ; Single compare unit compare register1.
X240 only.
SCMPR2      .set 741Bh        ; Single compare unit compare register2.
X240 only.
SCMPR3      .set 741Ch        ; Single compare unit compare register3.
X240 only.

CAPCON      .set 7420h        ; Capture control register.
CAPFIFO     .set 7422h        ; Capture FIFO status register.

CAP1FIFO    .set 7423h        ; Capture Channel 1 FIFO Top
CAP2FIFO    .set 7424h        ; Capture Channel 2 FIFO Top
CAP3FIFO    .set 7425h        ; Capture Channel 3 FIFO Top
CAP4FIFO    .set 7426h        ; Capture Channel 4 FIFO Top. X240 only.

EVIMRA      .set 742Ch        ; Group A Interrupt Mask Register
EVIMRB      .set 742Dh        ; Group B Interrupt Mask Register
EVIMRC      .set 742Eh        ; Group C Interrupt Mask Register

EVIFRA      .set 742Fh        ; Group A Interrupt Flag Register
EVIFRB      .set 7430h        ; Group B Interrupt Flag Register
EVIFRC      .set 7431h        ; Group C Interrupt Flag Register

EVIVRA      .set 7432h        ; Group A Int. Vector Register. X240
only.
EVIVRB      .set 7433h        ; Group B Int. Vector Register. X240
only.
EVIVRC      .set 7434h        ; Group C Int. Vector Register. X240
only.

; CAN(SCC) registers. X241/2/3 only.
CANMDER     .set 7100h        ; CAN Mailbox Direction/Enable reg
CANTCR      .set 7101h        ; CAN Transmission Control Reg
CANRCR      .set 7102h        ; CAN Recieve COntrol Reg
CANMCR      .set 7103h        ; CAN Master Control Reg
CANBCR2     .set 7104h        ; CAN Bit COnfig Reg 2
CANBCR1     .set 7105h        ; CAN Bit Config Reg 1
CANESR      .set 7106h        ; CAN Error Status Reg
CANGSR      .set 7107h        ; CAN Global Status Reg
CANCEC      .set 7108h        ; CAN Trans and Rcv Err counters
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CANIFR      .set 7109h        ; CAN Interrupt Flag Registers
CANIMR      .set 710ah        ; CAN Interrupt Mask Registers
CANLAM0H    .set 710bh        ; CAN Local Acceptance Mask MBx0/1
CANLAM0L    .set 710ch        ; CAN Local Acceptance Mask MBx0/1
CANLAM1H    .set 710dh        ; CAN Local Acceptance Mask MBx2/3
CANLAM1L    .set 710eh        ; CAN Local Acceptance Mask MBx2/3

CANMSGID0L  .set 7200h        ; CAN Message ID for mailbox 0 (lower 16
bits)
CANMSGID0H  .set 7201h        ; CAN Message ID for mailbox 0 (upper 16
bits)
CANMSGCTRL0 .set 7202h        ; CAN RTR and DLC
CANMBX0A    .set 7204h        ; CAN 2 of 8 bytes of Mailbox 0
CANMBX0B    .set 7205h        ; CAN 2 of 8 bytes of Mailbox 0
CANMBX0C    .set 7206h        ; CAN 2 of 8 bytes of Mailbox 0
CANMBX0D    .set 7207h        ; CAN 2 of 8 bytes of Mailbox 0
CANMSGID1L  .set 7208h        ; CAN Message ID for mailbox 1 (lower 16
bits)
CANMSGID1H  .set 7209h        ; CAN Message ID for mailbox 1 (upper 16
bits)
CANMSGCTRL1 .set 720Ah        ; CAN RTR and DLC
CANMBX1A    .set 720Ch        ; CAN 2 of 8 bytes of Mailbox 1
CANMBX1B    .set 720Dh        ; CAN 2 of 8 bytes of Mailbox 1
CANMBX1C    .set 720Eh        ; CAN 2 of 8 bytes of Mailbox 1
CANMBX1D    .set 720Fh        ; CAN 2 of 8 bytes of Mailbox 1
CANMSGID2L  .set 7210h        ; CAN Message ID for mailbox 2 (lower 16
bits)
CANMSGID2H  .set 7211h        ; CAN Message ID for mailbox 2 (upper 16
bits)
CANMSGCTRL2 .set 7212h        ; CAN RTR and DLC
CANMBX2A    .set 7214h        ; CAN 2 of 8 bytes of Mailbox 2
CANMBX2B    .set 7215h        ; CAN 2 of 8 bytes of Mailbox 2
CANMBX2C    .set 7216h        ; CAN 2 of 8 bytes of Mailbox 2
CANMBX2D    .set 7217h        ; CAN 2 of 8 bytes of Mailbox 2
CANMSGID3L  .set 7218h        ; CAN Message ID for mailbox 3 (lower 16
bits)
CANMSGID3H  .set 7219h        ; CAN Message ID for mailbox 3 (upper 16
bits)
CANMSGCTRL3 .set 721Ah        ; CAN RTR and DLC
CANMBX3A    .set 721Ch        ; CAN 2 of 8 bytes of Mailbox 3
CANMBX3B    .set 721Dh        ; CAN 2 of 8 bytes of Mailbox 3
CANMBX3C    .set 721Eh        ; CAN 2 of 8 bytes of Mailbox 3
CANMBX3D    .set 721Fh        ; CAN 2 of 8 bytes of Mailbox 3
CANMSGID4L  .set 7220h        ; CAN Message ID for mailbox 4 (lower 16
bits)
CANMSGID4H  .set 7221h        ; CAN Message ID for mailbox 4 (upper 16
bits)
CANMSGCTRL4 .set 7222h        ; CAN RTR and DLC
CANMBX4A    .set 7224h        ; CAN 2 of 8 bytes of Mailbox 4
CANMBX4B    .set 7225h        ; CAN 2 of 8 bytes of Mailbox 4
CANMBX4C    .set 7226h        ; CAN 2 of 8 bytes of Mailbox 4
CANMBX4D    .set 7227h        ; CAN 2 of 8 bytes of Mailbox 4
CANMSGID5L  .set 7228h        ; CAN Message ID for mailbox 5 (lower 16
bits)
CANMSGID5H  .set 7229h        ; CAN Message ID for mailbox 5 (upper 16
bits)
CANMSGCTRL5 .set 722Ah        ; CAN RTR and DLC
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CANMBX5A    .set 722Ch        ; CAN 2 of 8 bytes of Mailbox 5
CANMBX5B    .set 722Dh        ; CAN 2 of 8 bytes of Mailbox 5
CANMBX5C    .set 722Eh        ; CAN 2 of 8 bytes of Mailbox 5

;-------------------------------------------------------------------------
----
; I/O space mapped registers
;-------------------------------------------------------------------------
----
WSGR        .set  0FFFFh      ; Wait-State Generator Control Reg

;-------------------------------------------------------------------------
----
; Bit codes for Test bit instruction (BIT) (15 Loads bit 0 into TC)
;-------------------------------------------------------------------------
----
BIT15       .set 0000h        ; Bit Code for 15
BIT14       .set 0001h        ; Bit Code for 14
BIT13       .set 0002h        ; Bit Code for 13
BIT12       .set 0003h        ; Bit Code for 12
BIT11       .set 0004h        ; Bit Code for 11
BIT10       .set 0005h        ; Bit Code for 10
BIT9        .set 0006h        ; Bit Code for 9
BIT8        .set 0007h        ; Bit Code for 8
BIT7        .set 0008h        ; Bit Code for 7
BIT6        .set 0009h        ; Bit Code for 6
BIT5        .set 000Ah        ; Bit Code for 5
BIT4        .set 000Bh        ; Bit Code for 4
BIT3        .set 000Ch        ; Bit Code for 3
BIT2        .set 000Dh        ; Bit Code for 2
BIT1        .set 000Eh        ; Bit Code for 1
BIT0        .set 000Fh        ; Bit Code for 0

;-------------------------------------------------------------------------
----
;Test mode on and off constants;-------------------------------------
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ABRPT       .set    01fh      ; Analysis BreakPoint Register
PSA_ON      .set    03A1h     ; Turn PSA and FEEDB on
PSA_FB_OFF  .set    0121h      ; Turn PSA and FEEDB off

;Data page definitions for LDP instruction
DP_PF1      .set 224    ;sys regs, WD, SPI, SCI, (0x7000 - 0x707F)
DP_PF2      .set 225    ;ADC, GPIO (0x7080 - 0x70FF)
DP_CAN1     .set 226    ;CAN control regs (0x7100 - 0x717F)
DP_CAN2     .set 228    ;CAN mailboxes 1-5 (0x7200 - 0x727F)
DP_EVA      .set 232    ;Event manager A (0x7400 - 0x747F)
```