A PRECISELY ALIGNED CCD MOSAIC FOR ASTRONOMY

By

SCOTT CHRISTOPHER CHAPMAN

B. Sc. (Honours Physics and Mathematics) University of British Columbia, 1995

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE

in

THE FACULTY OF GRADUATE STUDIES ASTRONOMY

We accept this thesis as conforming to the required standard

THE UNIVERSITY OF BRITISH COLUMBIA March 1800 © SCOTT CHRISTOPHER CHAPMAN, 1996 In presenting this thesis in partial fulfilment of the requirements for an advanced degree at the University of British Columbia, I agree that the Library shall make it freely available for reference and study. I further agree that permission for extensive copying of this thesis for scholarly purposes may be granted by the head of my department or by his or her representatives. It is understood that copying or publication of this thesis for financial gain shall not be allowed without my written permission.

Department of Physics & Astronomy

The University of British Columbia Vancouver, Canada

Date April 25/96

STS PLOT - CONTRACTOR
 CONTRACTOR - CONTRACTOR

Abstract

By relying on semiconductor lithography and processing techniques, I have fabricated a flat, precision aligned CCD mosaic for astronomical uses, and other imaging applications where large, flat focal planes are important. Modifications to the lithographic techniques used in micromachining lead to a significant reduction in various residue deposits, allowing a smooth surface suitable for CCD alignment. Details of the technique and the fabrication of a prototype mosaic are described. The composite device is flat to within $\pm 5 \,\mu$ m, with rows/columns oriented to within 20 ppm. The use of an existing technology with built in precision reduces many of the difficulties and expenses typically encountered with mosaic detector construction. Imaging with a prototype camera confirms the accuracy of alignment. Applications for the 5 meter liquid mirror telescope (LMT) are considered, using the mosaic in time-delay and integrate (TDI) mode.

Table of Contents

Ał	ostra	ct	ii
Li	st of	Tables	v
Li	st of	Figures	vi
Ac	knov	vledgement	viii
1	Intr	oduction	1
2	Tec	nniques for CCD Mosaics	2
	2.1	Standard technique for mosaic cameras	2
	2.2	Alternative techniques	4
	2.3	A new approach to mosaics	7
3	Ove	rview of Etch-Alignment Technique	9
4	Fab	rication of Substrate	14
5	Ass	embly of prototype	20
	5.1	Mounting to Invar	23
	5.2	Align and bond detectors	24
	5.3	Wirebonding	25
	5.4	Dewar and controller	27
6	Me	asures of Precision	29

.

	6.1	Direct Measurements	29
	6.2	Test pattern imaging	30
	6.3	Limited CCD characterization	35
7	Lim	its of Technique	40
8	Ast	ronomy Advantages	42
	8.1	Time-delay and integrate readout (TDI)	42
	8.2	Liquid Mirror Telescope (LMT)	43
9	Con	clusions	46
A	open	dices	47
A	Stej	ps involved in Lithography	47
в	Gri	nding and Mounting INVAR	53
С	Cal	culation of thermal resistance	54
Re	efere	nces	55

List of Tables

ţ

٤

ł

3.1	Material Parameters	13
6.1	Three CCD Mosaic Measurements	31

List of Figures

.

2.1	Modular bracket mosaic technique	3
2.2	Alignment Setup	6
2.3	Photograph of a three socket, etched silicon substrate with one CCD in	
	place	8
3.1	Cross-section of the mosaic substrate. Preferential etching along the $\{111\}$	
	crystal plane yields an $80\mu\mathrm{m}$ deep socket with a 54.7° angled edge. The	
	substrate is $550\mu m$ thick. The CCD is butted against the socket edge	
	during the alignment process	9
3.2	Photograph of the mosaic socket corner showing the clean edges and flat	
	bottom of the socket. The edge is straight to within the most accurate	
	measurement available to us. The bottom can be dimpled on a $\pm 2\mu$ m scale.	11
4.1	Socket mask for a three element prototype	14
4.2	Interconnect masks for a three element prototype	15
4.3	Silicon crystal structure	16
4.4	Anisotropic Etch	17
4.5	A more isotropic etch due to lower etch ratios	17
5.1	Photograph of two socket prototype mosaic. The CCDs are wire- bonded	
	to a circuit board which is fastened to the Invar plate. The CCD is a 3K	
	$ imes$ 1.5K 15 μ m pixel detector, with the serial register along the long axis	21

5.2	Close-up photograph of the prototype mosaic. The CCD detectors are	
	mounted on the substrate and directly wire-bonded to a circuit board.	
	Interior bond pads are wire-bonded to the interconnect traces printed on	
	the substrate.	22
5.3	Outgassing Measurements	26
5.4	Photograph of the assembled prototype mosaic, mounted inside the dewar.	27
6.1	Geometry for the Two-CCD angular displacement	32
6.2	reduced test pattern 1	33
6.3	reduced test pattern 2	34
6.4	reduced test pattern 3	34
6.5	test pattern 1, upper CCD	35
6.6	test pattern 1, lower CCD	35
6.7	test pattern 2, upper CCD	36
6.8	test pattern 2, lower CCD	36
6.9	test pattern 3, upper CCD	37
6.10	test pattern 3, lower CCD	37
6.11	M13, lower CCD \ldots	38
6.12	star field, upper CCD	39
8.1	Three-element prototype with CCDs angled towards the North Celestial	
	Pole. Readout is east to west along the short axis of the CCDs	45
A.1	CCD dimensions and bond pad spacings	48
A.2	mask contact printing	51

;

Acknowledgement

· !

Greg Burley provided an invaluable experiential resource for discussing ideas, and made significant suggestions leading to the realization of this new mosaic technique. Ron Johnson made possible all the imaging tests by converting his controller and dewar to the purpose of a two-CCD mosaic. With pleasure, I also acknowledge the assistance and suggestions of Mike Jackson, Paul Hickson, and Ash Parameswaren.

This research is partially supported by operating grants from the Natural Sciences and Engineering Research Council of Canada.

ì

Chapter 1

:1

Introduction

Against the trend to smaller semiconductor die and feature size, astronomers prefer electronic detectors which are as large as possible to fill the focal planes of large telescopes and mimic photographic plates. Scientific grade charge-coupled devices (CCDs) are the most widely used electronic detectors [1]. However, defect free devices are limited in size by the yield of the semiconductor fabrication process. After over 20 years, CCDs remain poor competitors to photographic plates in terms of spatial resolution and format size.

With larger CCD arrays it is more difficult to maintain a near perfect charge transfer efficiency. Defects and traps occurring in a single pixel can corrupt entire columns. Other defects such as substrate shorts and cosmetic blemishes result in marginal devices or temperature dependent behavior. The likelihood of such defects occurring increases with the area of the array due to difficulty of wafer processing and maintaining high purity in large Si wafers. The present device size limit is about $4K \times 4K 15 \ \mu m$ pixels or less.

For larger format detectors, it becomes essential to assemble high quality individual CCDs in a mosaic arrangement. While there is the disadvantage that gaps will inevitably exist between CCDs, the individual devices can be pretested and preselected to minimize any defects in the composite device. The end result is a large-scale device, with relatively high yield if the mosaic technique is reliable. The main challenge in constructing the mosaic is then to precisely align the columns and/or rows of the individual CCDs and to ensure that the resulting device is coplanar.

Chapter 2

Techniques for CCD Mosaics

2.1 Standard technique for mosaic cameras

The largest existing CCD mosaics have been fabricated using a combination of precision machining and delicate assembly steps involving micromanipulation of the detectors under high power microscopes. One such camera was constructed by Luppino et al. [2] and is in use on the University of Hawaii 2m telescope. Another built by Christopher Stubbs [3] is in use for the MACHO dark matter survey. With this method, mounting brackets are constructed for each CCD from a low expansion alloy such as Kovar or Invar, using wire electric discharge machining (EDM) (tolerance of $\pm 3 \ \mu$ m). Alignment screws are used to connect the brackets to an EDM machined mounting block. Figure 2.1 illustrates the technique where the mounting brackets are shown empty and with a CCD in place.



Figure 2.1: Modular bracket mosaic technique

Luppino et al report a flatness of ± 0.5 mil over the entire array with the edges of the packages aligned and straight to within ± 0.5 mil (1 mil = 25μ m) The resulting assembled mosaic can have pixels along rows and columns aligned to within one pixel width (15 μ m). In practice, the four element MOCAM detector fabricated by this method for the Canada-France-Hawaii telescope has angular misalignments between CCDs of as much as 3 pixels (Greg Fahlman, UBC, private communication).

The main advantage of the technique is the ease with which faulty CCDs may be replaced. The modular mounting brackets make it a relatively simple operation to remove a single CCD without disturbing the remaining ones. The compromise is in the precision of alignment. Mechanical creep with time can be problematic with the use of alignment screws and different types of metals and interfaces. Where temperature gradients are present, differential stresses will cause misalignment.

2.2 Alternative techniques

An alternative to this modular bracket approach is to position and bond CCDs directly on a flat substrate such as a polished slab of aluminum or Kovar. Using this technique, it is easier to achieve a more precise alignment, but it becomes difficult or impossible to replace faulty devices. One such technique involves the use of an alignment mask, as described by Chen et al. [4]. Sekiguchi et al. have successfully aligned 14 CCDs in two columns using elaborate micropositioning stages [5].

An attempt was made to use a variation of these techniques to produce a mosaic suitable for use on the UBC 5 meter liquid-mirror telescope (LMT) [6], emphasizing

ł

1 h

relatively low cost and ease of fabrication compared to previous attempts. The proposed technique¹ involved micropositioning of the CCDs under a microscope using precisely defined alignment marks printed on the substrate to position and align the CCDs. Precedents in fiber-optic laser experiments (Mike Jackson, UBC, private communication) suggested that our tolerances for alignment precision could be met through such manual positioning. Standard photo-lithographic techniques used in the semiconductor processing industry are well suited to creating such alignment marks over a large wafer size. Glass and silicon wafers polished flat are commonly used in industry, such as the nearby micromachining lab at Simon Fraser University².

In order to overcome the problem with modularity, various bonding agents were investigated [6]. Desirable characteristics included bond strength, low temperature behaviour, degree of permanence, lubrication and ease of handling for alignment given the degree to which the CCDs must be positioned manually to align with the reference marks. Paraffin wax was chosen as the most favorable material for bonding, satisfying our constraints for all of these qualities.

This visual alignment technique is described using a glass substrate and $3K \times 1.5K$ 15μ m pixel CCDs. The wax is first precisely measured out:

$$\left\{ egin{array}{l} CCD\\ area \end{array}
ight\} imes \left\{ egin{array}{l} wax \ layer\\ thickness \end{array}
ight\} imes \left\{ egin{array}{l} wax\\ density \end{array}
ight\}$$
$$= 11.52 \, cm^2 imes 10 \, \mu m imes 0.87 \, rac{gm}{cm^3} = 10.02 \, mg \, wax \, per \, CCD.$$

The temperature is monitored and maintained at $50^{\circ}C$. It is then possible to essentially 'drop' each CCD roughly in place, placing one end of the CCD on the alignment marks and then dropping it from a low height. The transparent glass substrate revealed that the

¹The idea was originally suggested by Greg Burley and Mike Jackson

²Ash Parameswaran, assistant professor, engineering science Simon Fraser University, Burnaby, BC, V5A 1S6

Chapter 2. Techniques for CCD Mosaics

CCD's didn't have full wax contact from simply being placed on the substrate. In order to get an uniform coverage, a slight pressure needs to be applied to the CCD. Flatness will result from the equalization of the wax flow under the CCD, verified to within $\pm 2\mu m$ by microscope measurement of the CCD height above the substrate.

Positioning each CCD is quite smooth on the liquid wax interface, with the glass firmly anchored to the aluminum heating base. Low power magnification is used while roughly aligning the CCDs within the pattern by manually maneuvering the probes. More precise positioning requires higher magnification and use of an x,y,z-stage to move the probes. Simultaneous alignment of several CCDs is non-trivial as aligning one CCD can disturb the position of another, given that all CCDs are 'floating' on the substrate until the wax has cooled. The setup for manual alignment is shown in figure 2.2.



Figure 2.2: Alignment Setup

Numerous problems prevent this technique from achieving the required alignment or the reliability in replacing damaged CCDs for the LMT without extensive time and money. A fundamental limitation seems to be that the thickness of the CCD ($500 \mu m$) makes it difficult to see the alignment marks at close distance. Further work with a more sophisticated microscope setup (one which could rotate around the CCD alignment stage for instance) might overcome this difficulty. The precision of movement on the smallest scale is also hard to achieve. Very precise positioners would have to be developed or purchased. The manipulation of CCDs required over an extended period of time at 50°C might damage CCDs. Finally, the difficulty in aligning all three devices at the same time before allowing the wax to cool means that replacing a CCD may require re-aligning all CCDs in the mosaic.

2.3 A new approach to mosaics

I have developed a technique in which many of the constraints of alignment are reduced by taking advantage of the inherent precision of established semiconductor lithography technology³. Detailed submicron patterns are routinely created on large, flat silicon wafers. These same techniques and equipment can be used to create a mosaic substrate with built-in alignment guides (sockets) for each detector. Fabrication of the substrate and mounting, aligning and replacement of the CCDs is straightforward, with a final composite device that is expected to be flat, aligned, and mechanically stable with time and temperature. Alignment screws are eliminated, reducing the potential for mechanical creep. Figure 2.3 shows a photograph of a three socket, etched silicon substrate with one CCD in place.

³Initial idea developed by Scott Chapman, Greg Burley and Ash Parameswaren



Figure 2.3: Photograph of a three socket, etched silicon substrate with one CCD in place.

Chapter 3

Overview of Etch-Alignment Technique

The mosaic assembly is essentially a "silicon motherboard" variation in which the individual CCD detectors are positioned by alignment guides (sockets) preferentially etched into the mosaic substrate. Since the lithographic process is highly accurate over the entire area of the silicon wafer, the alignment of the socket edges with respect to one another can be made very precise. During the mounting process, each CCD is butted against the socket edge(s) in a self-alignment process. To electrically connect the CCD detectors, bond pads and traces are etched into an aluminum interconnect layer. Figure 3.1 illustrates the concept.



Figure 3.1: Cross-section of the mosaic substrate. Preferential etching along the $\{111\}$ crystal plane yields an 80μ m deep socket with a 54.7° angled edge. The substrate is 550μ m thick. The CCD is butted against the socket edge during the alignment process.

Anisotropic etching favours certain crystal lattice directions. In silicon, the etch rates can vary by a factor of 20 to 600 in the different crystal orientations [6,7]. Using this process, a uniform, flat-bottomed socket with edges angled at 54.7 degrees from the horizontal can be produced. The etching process can be accomplished without measurable degradation in the precision of the lithography. Trial runs have shown that the etch process produces high quality edges and polished flat bottoms suitable for aligning the detector elements, as shown in Figure 3.2.

Figure 3.2: Photograph of the mosaic socket corner showing the clean edges and flat bottom of the socket. The edge is straight to within the most accurate measurement available to us. The bottom can be dimpled on a $\pm 2\mu$ m scale.



The design of the pattern of sockets, bond pads and interconnect traces depends upon the bond pad arrangement of the individual devices. Some astronomical CCDs are now being fabricated with the bond pads restricted to less than four sides, allowing the imaging areas to be butted against each other. For the prototype, the non-buttable devices required individual sockets and more extensive interconnect than would be necessary for the newer, three-side buttable CCD detectors. Careful design of the socket depth (60 to 80μ m) and dimensions is necessary to minimize the dead space between devices, while maintaining sufficient depth to ensure alignment. Where possible, the sockets can be designed to be slightly oversized to ease alignment by allowing more freedom of movement and avoid overconstraining the CCD due to contact with more than two alignment edges. Sockets with vertical walls can be fabricated using a silicon wafer with $\{110\}$ crystal orientation [6], however an angled edge is suitable for excellent alignment and also appears to act as a 'well' for the excess wax to flow into. The electrical traces for the prototype were designed 100 μ m wide with 75 μ m spacing, but could have a reduced width without compromising electrical performance. The bond pads can be made oversized $(300\mu m \times 1000\mu m)$ to permit the repeated wirebonding involved when faulty CCDs are replaced.

Each CCD may be held in place on the substrate with a permanent epoxy bond, or with a non-permanent wax bond. In either case, the bond layer is thin (about 10μ m) to ensure the device remains flat and to minimize any degradation in thermal conductivity. Faulty or damaged CCDs may be removed and replaced from the etched substrate relatively easily if a wax bond is used. None of the other CCDs needs to be handled directly. The old wire-bonds are first removed under a microscope. The substrate can then be heated to ~ 50°C and the problem CCD replaced. Alignment and re-wirebonding are again straightforward as described above. Even before the wax has cooled, the CCDs are essentially fixed in place once aligned in the socket, and it is clear that the other CCDs in the substrate are not at all disturbed by the removal and replacement of a damaged one. In practice, it has taken as little as two hours to completely change two CCDs and have the mosaic detector operational again.

The flexible silicon substrate is bonded to a polished INVAR¹ plate to maintain flatness and prevent breakage. The Invar mounting plate is stress-relief annealed after machining to minimize extraneous shape changes over time or temperature. The combination of bond layers, substrate and Invar plate add a thermal resistance of approximately $0.1 \circ C/W$ (appendix C). The devices, substrate and mounting plate are bonded evenly over their entire area to form a solid structure. To minimize thermal expansion mismatch stresses, the CTE of the substrate matches that of the detectors (both silicon), and is close to that of the Invar mounting plate (Table 3.1). At an operating temperature of -90°C, we estimate the Invar-silicon thermal expansion mismatch to be about $3\mu m$ over the 7.5cm substrate length; this should not lead to measurable displacement in the imaging surface.

Table 3.1: Material Parameter	s
-------------------------------	---

Material	Thickness	Conductivity $\frac{W}{m \cdot K}$	CTE $\frac{ppm}{K}$
Paraffin wax	$10 \mu { m m}$	0.25	6.7
Silicon	$550 \mu { m m}$	270 to 170 °	1.4 to 2.5 *
Invar	$2.5 \mathrm{mm}$	10.5	2.0 to 1.3 ^a
Epoxy	$50 \mu { m m}$	300	4.2
	1		

¹INVAR is an acronym for Invariant, implying close to zero thermal expansion.

Chapter 4

Fabrication of Substrate

The equipment required for substrate fabrication includes a photoresist spinner, a mask aligner and exposer, wafer baking ovens, SiO_2 deposition ovens, etching fume hoods, and a variety of etchants and solvents. The substrate consists of a silicon {100} wafer, 10cm diameter $\times 550\mu$ m thick. Out of the box, the polished wafer was flat to better than a micron. The pattern of sockets, bond pads and interconnect traces are created by a CAD system and contact printed on photosensitive plastic plates from simple postscript files. One mask defines the sockets to hold the CCDs, while the second details the interconnect metalization. The masks for a three element prototype are shown in Figures 4.1, and 4.2. Actual lithography lab procedures are described in appendix A.



1

Figure 4.1: Socket mask for a three element prototype.

To understand anisotropic etching, consider the silicon crystal lattice (identical to



Figure 4.2: Interconnect masks for a three element prototype.

that of diamond). The Miller indices, showing the various planes in a cubic crystal, are portrayed in figure 4.3 along with the crystal structure of silicon - two interpenetrating face-centered cubic lattices. The atomic packing density in the $\{100\}$ plane is considerably less than in the $\{111\}$ plane. This results in a 20 to 100 times faster etch in the $\{100\}$ plane, with an angled edge of 54.7° with the horizontal (the angular difference between the $\{100\}$ and $\{111\}$ planes).

For controlled preferential etching of silicon, EDP (ethylene diamene pyrocatechol) is generally the best etchant [9]. EDP supports the high contrast in etch rates for the different silicon crystal orientations which is necessary for producing the long, straight reference edges for aligning the CCDs (figure 4.4). This also allows the accurate reproduction of the etch mask without undercutting of the SiO₂ layer. Figure 4.5 reveals the lower quality socket and undercut edges that can result with other etchants. The uniformity of the process leaves flat surfaces, free from large scale irregularities that could



Figure 4.3: Silicon crystal structure

5

tilt or misalign the CCDs. For the prototype, the sockets were etched 80μ m deep, using a variation of EDP chemical etching developed for this application with the addition of pyrazine to act as a catalyst.



Figure 4.4: Anisotropic Etch



Figure 4.5: A more isotropic etch due to lower etch ratios

Before etching, the silicon wafer is first thoroughly cleaned. A $1\mu m \operatorname{SiO}_2$ layer is then deposited on both sides of the wafer. The first mask is used to lithographically define the etch socket and the SiO₂ is etched away in the socket region using Hydrogen Fluoride. As the ratio of EDP etch rates for Si and SiO₂ can be as high as 5000:1, the remaining SiO₂ effectively acts as an etch stop while the sockets are etched 60 to $80\mu m$ into the Si wafer. Other chemical etchants (such as KOH) can have much lower etch ratios (400:1) and are more difficult to implement for this application [9].

EDP etching is not without its own problems, which can include residue formation, non-linear etch rates, and hillocks. Non-linear etch rates can cause the sockets to be etched to the wrong depth. An over-etched socket could have a bottom area smaller than the CCD itself, since the socket edges are angled and the design tolerances are small (appendix A). Ideally, the bottom surface of the socket should have the minimum excess area necessary for alignment to occur reliably. Residue and hillock formation can be substantial enough to lead to misaligned or tilted devices.

Several factors can lead to non-homogeneous residue formation on the edges and bottom surface [9]. The primary reason appears to be over-saturated EDP solutions, occurring when large quantities of silicon are being dissolved. Depositing a sufficiently thick back-side layer of SiO_2 eliminates back-side etching that would perturb the smooth surface and saturate the EDP solution. Residue formation from material contaminants can be largely suppressed with a 15 second acetone bath prior to etching. We noticed that UV light leads to residue, and a light blocking foil should surround the etch vessel.

The etch rate obtained with EDP can be severely non-linear [8]. Pyrazine has successfully been incorporated as a catalyst providing a much faster and more efficient etch [8]. Residue also tends not to be observed with its use. In addition, a linear, repeatable etch rate $(1.5\mu m/min)$ can be achieved for the time frame involved (1 hour) in making the $80\mu m$ sockets. That is, the etch rate is more controlled so that it is not necessary to continually remove the wafer from the etchant to check the etch depth, risking contamination and residue formation.

Hillocks consist of silicon pyramids of up to 40 μ m height formed on the etched surface. The hillocks can be sizable and abundant enough to raise or tilt the CCD. Details of the hillock problem are not fully understood [8], however we found a significant reduction in formation to be associated with an increased pyrocatechol concentration in the EDP. We were able to consistently produce substrates with Hillock size less than 5μ m. In many cases, there were no Hillocks present.

Lithographic processing steps are interconnected, and the entire process will be altered by adjusting any particular parameter. Carefully matched processing times and concentrations are required. The concentrations of pyrocatechol and pyrazine were adjusted until the best possible surface quality was achieved (Figure 3.2) with 6g crystalline pyrazine, 40g solid pyrocatechol, 1000 mL ethylenediamene. The resulting etched surface was flat to within $\pm 2\mu$ m, observed by bringing the highest and lowest features into focus with a calibrated microscope.

Once the sockets have been etched, the bond pads and interconnect traces are patterned on the wafer. First aluminum is sputtered evenly onto the wafer to a thickness of $1\mu m$. The metalization pattern is then transferred from the mask to the wafer by lithography. Photoresist is used as the etch stop for the aluminum etch. Spinning photoresist onto the wafer with the required uniformity becomes difficult as the corners of the etched sockets tend to funnel the photoresist. The resulting streaks are excessively thick and can cause incomplete or inaccurate exposure of the metal etch pattern, leading to shorted bond pads near the socket corners. To overcome this problem, the spinning speed is increased (5400 rpm) for an extended time (35 seconds). This ensures that excess photoresist deposited on the wafer is kept to a minimum. The mask exposure time is also increased from 40 to 50 seconds to expose the thicker layer of photoresist near the problem corners. The aluminum etch must then be terminated at the initial realization of the pattern to avoid etching the patterned areas to any degree (leaving an unusably thin layer of aluminum for bond pads). Fortunately, the main criterion for the metalization is that none of the traces or bond pads become shorted, and we can overlook slight imperfections in the pattern.

The completed substrate is then diced from the round wafer using a manual diamond scriber. The precision $(\pm 10\mu m)$ and reliability of the scriber are not crucial here as one millimeter is left on all four sides of the substrate, and there is no danger of damaging the sockets.

Chapter 5

Assembly of prototype

Once the substrate has been fabricated and diced from the wafer, the steps to assemble the mosaic are: (1) Bond the silicon substrate to the Invar mounting plate with thermally conductive epoxy. During the process the substrate surface is pressed against an optical flat to ensure the bonded substrate remains flat. (2) Heat the substrate, apply bonding wax and align the individual CCD detectors. (3) Wire-bond the detectors to the substrate, or external circuit board. Figure 5.1 shows a photograph of the completed two-socket prototype mosaic. The CCDs are wire-bonded to a circuit board which is fastened to an Invar plate. The CCDs are $3K \times 1.5K 15\mu$ m pixel detectors, with the serial register along the long axis. A close-up photograph of the CCDs aligned in the sockets and wirebonded is shown in figure 5.2. Figure 5.1: Photograph of two socket prototype mosaic. The CCDs are wire-bonded to a circuit board which is fastened to the Invar plate. The CCD is a $3K \times 1.5K \ 15\mu m$ pixel detector, with the serial register along the long axis.



Figure 5.2: Close-up photograph of the prototype mosaic. The CCD detectors are mounted on the substrate and directly wire-bonded to a circuit board. Interior bond pads are wire-bonded to the interconnect traces printed on the substrate.



Chapter 5. Assembly of prototype

5.1 Mounting to Invar

In order to assure the overall flatness of the assembled mosaic, the Invar mounting plate must be polished as flat as possible. High temperature ovens are first used for annealing and stress relief procedures¹. The plate is then ground on both sides, with subsequent polishing steps achieving an overall flatness of $\pm 5\mu$ m with a local variation of $\pm 10\mu$ m. Thermal modelling performed by Luppino et al. [1] and private communication with Mike Lesser (Steward Labs, University of Arizona) indicate that the INVAR36 can maintain its shape over time and temperature if it is properly stress-relieved. They also confirm that INVAR36 has adequate thermal conductivity for cooling to the typical operating temperatures of astronomical CCDs (-90°C).

The epoxy² used for bonding the etched silicon substrate to the Invar is electrically conductive to keep the substrate at ground potential and thermally conductive for cooling through the composite mount. To mount the silicon substrate to the Invar, a pressure of $\sim 230 \text{ g/cm}^2$ is applied with weights on an optical flat, acting as a uniform plunger. Slight imperfections in the Invar surface will have little effect, as the overall flatness is sufficient/within our tolerance. Angular alignment of the substrate with respect to the Invar is not crucial, as the position of the camera can be rotated once mounted on the telescope. Details of these mounting procedures are described in appendix B.

Alternatives to Invar were also considered. Kovar has similar properties [2] but is not quite as good a match to silicon for thermal expansion. It does however possess better thermal conductivity, perhaps making it an option for limited cooling systems. Thick silicon was also considered, but its high thermal resistance and difficulty to work with made it unfeasible. Ceramics are also not as good as Invar as far as machinability and other mechanical, thermal, and electrical properties [2, UBC metalurgy - S.Cocroft,

¹Scientific Alloys, technical data sheet for INVAR36FM - UNS-K93602

²Tracon: Tra-duct2902, conductive silver epoxy adhesive

private communication].

5.2 Align and bond detectors

To bond the detectors to the substrate, paraffin wax was chosen over other waxes and epoxies [6]. Non-functional CCDs are bonded to a glass wafer to study the bonding properties of wax. As well as providing a reversible bond, the wax flows well and results in a very even layer, which tends to act as a lubricant during the alignment process. The wax has a reasonably low melting temperature (50°C) making it easy to handle and allowing an unlimited time for positioning of CCDs. At low operating temperatures (-90°C), the wax continues to act as an adhesive and does not become brittle. Sharp impacts to an aluminum testblock at operating and room temperatures did not dislodge the CCDs. For the size of the devices, about 1.5mg of wax (density 0.9 g/cm^3) results in a $10\mu\text{m}$ thick bond layer. Excess wax can be wiped away with acetone or dissolved with benzene or ether chloroform.

Each of the devices essentially "snaps" into its socket, and is easily aligned against the reference edge(s). The alignment procedure can be carried out without micromanipulation under a high power microscope since the positive contact of CCD with the socket edge ensures that the CCD is in place. Trial runs have shown that alignment with a 60 to 80μ m socket depth is not a difficult task. Two orthogonal sides of the socket are used for alignment, where the CCD is first pushed against one edge and then butted up to the other. The smooth surface finish of the socket allowed the detectors to be mounted without flatness problems, and no weighted optical flat is required. In the case of a pebbled (hillock) socket surface, alignment and coplanarity are not compromised if the surface is still uniform overall (no localized hillocks). If the hillock size is less than the wax depth, no effect will be noticed. This is important as a hillock-free surface is not easy to achieve.

.

It was initially a concern that the wax bond of the CCDs might lead to outgassing. As the CCD has very little freedom of movement in the socket, it is possible for air bubbles to be trapped underneath (as revealed by the glass wafer testing). Since the mosaic detector is required to operate at low temperature in an evacuated housing, excessive outgassing from the wax would be a problem. Vacuum waxes were considered as a bonding alternative, but they do not have the lubricant properties that paraffin has, and the CCDs cannot be subjected to the high melting temperatures (100°C).

The assembled mosaic was placed in its dewar and pumped down to operating pressure of 10mTorr. Figure 5.3 shows the variation in dewar pressure with time for the cases of an empty dewar and the detector mounted inside the dewar. Subsequent pump-downs have increasingly better hold times as contaminants continue to be evacuated. There is a slight indication of increased outgassing for the detector in dewar test with the smallest initial slope (marked A in figure 5.3), where the slope increases after about 12 hours. However, in all other cases the pressure rises about equally fast with and without the detector in the dewar, and there is likely very little increased outgassing from the wax bond.

5.3 Wirebonding

For the non-buttable CCDs, the bond pads along the channel separating two CCDs must be wirebonded to the traces leading to the substrate edge. The bond pads on the periphery of the mosaic must then be wirebonded to an external printed circuit board (PCB) in order to connect the CCDs to the control electronics. The melting temperature of paraffin wax places a constraint on the types of wirebonding that can be done. Thermo-sonic bonders cannot be used, despite their ease of bonding different



Figure 5.3: Outgassing Measurements

materials. An ultrasonic wedge bonder without heating is thus used with aluminum wire for the aluminum bond pads on CCD and substrate. The resulting cold weld is difficult to achieve and the samples must be thoroughly cleaned of oils and oxides prior to bonding. We gold electro-plated the tin PCB in order to bond to it with aluminum wire.

The wirebonding also places some design constraints on the mosaic. The wedge bonder foot size, wire clamp height, and the height differences on the mosaic all lead to limits on socket closeness. It is possible to circumvent some of these difficulties by designing bond pads diagonally away from the corresponding CCD bond pads along the narrow channels between CCDs. This allows the bonding to proceed along the length of the channels rather than orthogonal to them.

.1

5.4 Dewar and controller

The mosaic detector is mounted to a teflon 'spider' and bolted to aluminum brackets in the detector head. Wiring for this prototype is done directly from PCB to the dewar outputs. Figure 5.4 shows the assembled prototype mosaic, mounted inside the dewar.

Figure 5.4: Photograph of the assembled prototype mosaic, mounted inside the dewar.



Cooling is achieved with a cold finger attached to a liquid nitrogen (LN_2) tank. The cold finger quickly cools an aluminum disk, which in turn cools the Invar mounting plate. As the thermal conductivity of the Invar is not high, less robust cooling schemes (such as thermo-electric) may require a more complete Invar surface contact with the cold finger to achieve the -90°C operating temperatures.

In order to make use of an existing controller for initial test purposes³, all clock lines were hardwired in parallel on the PCB. Thus both CCDs are clocked together from the single timing board signals. Two preamplifier boards are switched between externally to readout one or the other CCD. Readout is destructive for both CCDs, so a complete mosaic image requires two integrations on the same field. Scientific imaging will require the development or purchase of a high readout speed, multi-channel controller.

³An2910A processor-based, built by Ron Johnson, UBC

Chapter 6

Measures of Precision

6.1 Direct Measurements

The mechanical accuracy of the technique was verified with a number of measurements which are detailed in Table 6.1 for a three element prototype. Height measurements were made under a microscope with a calibrated z stage, accurate to within $\pm 2\mu$ m. Planer (x,y) measurements of the mosaic substrate were made using a photographic plate comparator. At low magnification, these were repeatable to about a micron. Measurements of the alignment between the detectors and the substrate sockets were made with a high magnification microscope, using a digitally-metered movable eyepiece crosshair, accurate to within 0.5μ m.

The etched socket edges were straight and aligned beyond our ability to measure them $(\pm 1\mu m)$. The angular misalignment of the CCD rows and columns with respect to the socket edge was measured to be less than $1\mu m$ along the 5cm long axis of each detector (20 parts per million). In order to assess the die cut precision, seven Loral CCDs were measured from bond pad to the cut edge. Four of the CCDs were consistently cut at the same distance to within $\pm 1\mu m$. The worst case deviation from this distance among the seven devices was $6\mu m$. The angular displacement of the cut (distance from bond pad to CCD edge) for these same four CCDs was less than $1\mu m$ along the 5cm long axis of each detector (20 ppm). The largest angular displacement found for this die cut among the seven CCDs was less than 60 ppm. By choosing two suitable CCDs for the prototype,

with edges cut a consistent distance from the imaging area, registration of the columns to within $\pm 1\mu$ m was possible.

Height measurements at the four corners of each device indicate a slight tilt to some of the devices along the long axis of the CCDs, resulting in a $\pm 5\mu$ m overall flatness variation. This is likely due to excessive butting against the angled socket edge, as initial testing of the wax bond on glass did not reveal any flatness variations. It therefore may be possible to improve the overall flatness by refining the CCD alignment procedure. When CCDs did not ride up the socket edge, they were found to have a variation from flatness of $\pm 2\mu$ m from a reference plane. There was no measurable tip to the CCDs along the short axis of the CCDs. Since this tip degree of freedom does not seem to be a factor, the mosaic flatness variation would be comparable to our measurement error and restricted to one axis (tilt) only.

6.2 Test pattern imaging

Imaging of test patterns with the two-element prototype mosaic camera was performed under laboratory conditions with a bench setup where the camera dewar was fitted with a short focal length lens capable of imaging a target a few feet away. The test patterns provide a means of assessing the quality of the CCDs and measuring the precision of the alignment. As a test of alignment, the data has certain limitations: lens aberrations, non-flat test pattern, and non-aligned test pattern. The lens gives a vignetted field, only part of which is distortion free.

The data is reduced using IRAF and SuperMongo scripts (appendix B). The test pattern line to be reduced is scanned along each row for a drop-off point in pixel intensity. An initial analysis of the images show that this drop-off is well defined. A linear least squares fit is then performed on the central region of the test pattern line for each CCD,

Table 0.1: Three CCD Mosaic Measurements			
Parameter		Value	Units
Device thickness *	Α	550 ± 1	μ m
	В	552	
	\mathbf{C}	551	
Substrate thickness	SS	550	$\mu \mathrm{m}$
Socket depth		80	μ m
Socket flatness		± 2	μ m
Composite device	flatness ^{b,c}	± 5	μ m
Device tilt ^{c,d}	Α	6 ± 2	μ m
	В	10	,
	Ċ	0	
Device tip •	A,B,C	0 ± 2	μ m
Angular alignment	f,g	20	ppm
Column registratio	on ^g	± 1.5	μm

Table 6.1: Three CCD Mosaic Measurements

^adevices are labelled A,B,C

^bmeasured with respect to the substrate

^cderived from height measurements at the corners of each device

^dmeasured along the serial register direction

^emeasured orthogonal to the serial register direction

^fdeviation of less than 1μ m over the 5cm long axis of each device

^gmeasured from detector feature to socket edge

where the lens gives aberration free images:

Figures 6.2, 6.3, and 6.4 show the reduced test pattern data (corresponding to Figures 6.5, 6.6, 6.7, 6.8, 6.9, and 6.10). The results of each linear fit are shown on the graph for each CCD. The coefficients correspond to the formula y = Bx + A and r is the correlation. The two sloped lines on each graph map the column and row of the test pattern on each CCD. Subtraction of the slope parameters, B, gives the angular misalignment of the two CCDs in the small angle approximation, as shown in figure 6.1.



Figure 6.1: Geometry for the Two-CCD angular displacement

The results are as follows: test1 - 40ppm, test2 - 100ppm, test3 - 80ppm (20ppm corresponds to 1μ m displacement along the 5cm substrate). There are two points to

consider here. Firstly, the test pattern results all indicate a greater angular misalignment than the 3-element prototype. This is certainly understandable since greater care was taken in the later assembly of the 3-element prototype. Secondly, the spread in values for the 3 tests are more likely an indication of the tests themselves rather than of the actual misalignment. The test patterns are all different and reduction of the data may not provide the same degree of accuracy in all cases. Also, lens aberrations and image flatness may vary between the 3 tests.



Figure 6.2: reduced test pattern 1



Figure 6.3: reduced test pattern 2



Figure 6.4: reduced test pattern 3



Figure 6.5: test pattern 1, upper CCD



Figure 6.6: test pattern 1, lower CCD

6.3 Limited CCD characterization

It can be seen in the images taken with the prototype that the cosmetics of the devices are not very good (figures 6.11, and 6.12 as well as test pattern images). Numerous dead regions, blocked columns, and hot pixels abound. Nonetheless, these CCDs provide a very



Figure 6.7: test pattern 2, upper CCD



Figure 6.8: test pattern 2, lower CCD



Figure 6.9: test pattern 3, upper CCD



Figure 6.10: test pattern 3, lower CCD

adequate proof of concept and allowed precise measurement of the degree of alignment possible.

Out of the seven Loral CCDs tested only 4 had even an engineering grade performance. Most had nonfunctional output amplifiers or substrate shorts. The top CCD in the functional prototype had one dead amplifier, however, the remaining one proved adequate for test purposes. None of the CCDs will be suitable for scientific use with the liquid mirror telescope.



Figure 6.11: M13, lower CCD



Figure 6.12: star field, upper CCD

Chapter 7

Limits of Technique

The wafer dicing process sets the limit to the precision of alignment. Each CCD must be diced so that the physical device edges are parallel to the rows and columns of the imaging area. Since the device is butted against the socket edge, any angular misalignment of the device edge will show up as misalignment of the imaging area. As well, the registration of rows/columns between the detectors depends on the consistency of dicing each detector edge a fixed distance from the imaging area. If the cut edges are not smooth, or if the cuts are not lined up properly, then the precision of the mosaic is compromised. Private communication with SITe (Scientific Imaging Technologies) confirmed that the CCD dies can be reliably cut for this purpose. Thick saw blades with high diamond impregnation are used to achieve micron accuracy and repeatability.

Height variations of the individual CCD devices will show up as height variations of the composite mosaic. It is conceivable that single devices which originate from different wafers could be lapped to the same thickness to minimize this effect. However, the most realistic solution is to ensure from the manufacturer that the CCDs destined for a mosaic all come from the same thickness wafer.

There are several aspects of the lithography processing that could lead to misalignment if not done properly. The printing of mask transparencies from the CAD postscript files must be done at a very high resolution and level of control. With some printers, two lines may deviate from parallel enough to distort the mosaic geometry on the scale of a fraction of a pixel. There must be perfect contact between layers in contact exposure of

Chapter 7. Limits of Technique

mask plates from the transparencies, and contact printing the photoresist wafer patterns from the mask plates.

The etch pattern realization can certainly lead to displacement of the aligned CCD position if it is not carried out with exacting care. Although it is possible to achieve precision edges through etching, problems such as undercutting of the SiO_2 layer and hillocks can lead to misalignment.

There may be some complications in using buttable CCDs. Modularity may not be an easy task, unless additional wasted space is inserted between CCDs. Thinned CCDs could conceivably work with the technique, although then there is more than just the dicing of the CCD to consider as a precision constraint. The alignment of the thinned device on the package will affect the overall alignment, as will the precision of the package itself.

Chapter 8

Astronomy Advantages

Correct angular alignment and pixel registration could be advantageous for use in astronomy. In general, software corrections can be worked into the data reduction once the misalignment is known. However, the cost in time, difficulty of application, and degree of correction must be weighed against the efficacy with which mechanical alignment can be performed. Some examples include astrometry applications over large scales which may be very sensitive to misalignment of rows and columns. Gravitational lens experiments require precise image reconstruction [10], and the misalignment of the CCDs can lead to difficult software reductions. Also, with the successful use of field flattening correcter lenses in telescopes such as the Sloan Digital Sky Survey (SDSS), the CCDs of a mosaic must be as coplanar as possible.

Specific projects which can take full advantage of the improved accuracy obtained with etched alignment are driftscanning surveys such as the 5 meter liquid mirror telescope (LMT).

8.1 Time-delay and integrate readout (TDI)

TDI or driftscanning is a CCD readout technique whereby the telescope is kept stationary while the Earth's motion moves celestial objects across the field of view of the telescope [11]. A one-to-one correspondence of sky and image is maintained by moving charge on the CCD (which corresponds to fixed point in the sky) at the sidereal rate (15"/s at celestial equator). TDI provides distinct scientific advantages, especially for larger detectors. Superior flat-fielding and image uniformity are obtained as the effects of pixelto-pixel variations are minimized in a scanned image due to the averaging of signal over an entire column of pixels. There is an efficiency advantage where less overhead is associated with telescope positioning and CCD readout. Data is always being integrated and read out without interruption. Although one is limited to a specific integration time dictated by the detector size, observations can be co-added over successive nights.

There are certain intrinsic problems in TDI imaging that must be overcome [11]. Objects at different declinations (even as little as one CCD field of view) have noticeably different linear drift velocities. This leads to a blurring along CCD columns since the readout rate is only matched to objects on the central column. There are discrete shifting and sampling elongations. Finally the apparent paths of stars are perfectly straight only on celestial equator. Images are then blurred along CCD rows in any non-equatorial scan as the stars trace an arc across the CCD. Tracking along great circles in the sky will compensate for star-trail curvature, effectively giving the same performance as TDI on the equator. This tracking can be accomplished with a motorized stage for the detector or with the telescope itself. A properly aligned rectilinear geometry for the mosaic detector is then crucial to avoid further blurring of images.

8.2 Liquid Mirror Telescope (LMT)

A specific application of the etch alignment mosaic is the 5 meter liquid mirror telescope (LMT) to be constructed for operation at latitude 49.04° for faint object survey work [12]. The telescope achieves its primary mirror by uniformly rotating liquid mercury to form a parabola. This forces the telescope to be strictly zenith pointing and conventional staring imaging techniques cannot be used. TDI readout is the obvious solution, in addition to providing the optimal data acquisition technique for surveys. However, tracking with the telescope along a great circle is not an option.

An offset angle between the detectors could be designed into the lithography to compensate for the curved star trails encountered. Alignment is still assured by the lithographic placement of the sockets, which are easily calculated and introduced in the layout design. Figure 8.1 demonstrates how this could be implemented for the three-element prototype. The substrate with this geometry were fabricated and measurement of the aligned CCDs indicates that measured distances correspond to design. With certain CCDs (SITe, three-side buttable 2k X 4k CCD), this angling is not possible due to the readout direction. The main problem with angling the CCDs is that the mosaic is then optimized for one particular latitude, and even so, still has TDI error associated with one CCD.

The favored solution to the TDI error is to construct a distortion correcting lens to ensure linear star trails across the CCD and compensate for differential drift velocities. This then places a stringent constraint on the mosaic to keep misalignments less than 0.8" corresponding to 4μ m (with a plate scale of 0.3" per 15 μ m pixel). As the results in table 6.1 indicate, careful implementation of the technique should be able to achieve this.



Figure 8.1: Three-element prototype with CCDs angled towards the North Celestial Pole. Readout is east to west along the short axis of the CCDs.

Chapter 9

Conclusions

Use of the precision inherent in the lithography and etching processes allows the fabrication of precisely aligned mosaics suitable for many applications in astronomy. The fabrication process is relatively simple and economical using standard lithography laboratory equipment. It appears to be scalable up to the largest silicon wafer sizes.

Replacement of faulty CCDs is fast and straightforward. The resulting composite device is flat and mechanically stable. As far as we are aware, no other existing mosaic technique is comparable in terms of alignment achieved. If the CCDs can be diced accurately enough, then by the proper use of the technique there will be correct registration between pixels and no angular displacement between CCDs.

Time delay and integrate readout (drift-scanning) is certainly an application that benefits greatly from the increased alignment precision attained with etched sockets. Although the full generality of the technique is not yet known, the prospects are promising for use of etch alignment in mosaic applications other than TDI. Three edge buttable and thinned CCDs may be incorporated into direct imaging mosaics with a common socket for alignment. Other imaging applications where large, flat focal planes are important, such as remote sensing, may make use of this technique.

For some astronomical applications, the improved alignment of the mosaic may still not be adequate to eliminate all software data correction. However, the ease of the technique and low cost in addition to reduced software data manipulation still merit its use over existing machined techniques.

Appendix A

Steps involved in Lithography

Designing lithography masks

CAD design of the masks entails certain limitations. The public domain software package 'XKic', for the X-windows platform, was used to design all masks for use in the photo-lithographic processes. It is a fairly standard CAD (computer aided design) package, which implements a multi-level environment for design of minute detail over a fairly large surface area. The reason for the use of this particular package was that it is currently the software used by the micro-machining group at SFU, and thus is already configured for their 4" wafers.

The lithography pattern and it's dimensions are shown in the figure A.1. This was used as the starting point for design of the metalization and etch masks. The lithography process used in fabricating the CCD's is extremely precise, however the way in which a CCD is cut from the wafer is not necessarily in complete accord with the lithography design. (As we shall see, this is especially true in the case of the diamond scribed CCD's that we cut ourselves.) Thus the CCD's were measured under the microscope from the bond pad edge to the cut edge. For the pre-cut CCD's available, the lithography marked edge was $10\mu m$ greater than the the actual cut edge.

The main considerations for the metalization mask were: the CCD position, alignment marks to get the CCD in place, the bond pad spacing, and the trace positions connecting the bond pads. Ideally, one would like the CCD's on the mosaic to be as close together as



Figure A.1: CCD dimensions and bond pad spacings

possible to eliminate 'dead' space on the device. The CCD positioning on the substrate was dictated by the amount of space taken up by the bond pads and traces between each device. The trace width and spacing were taken as $75\mu m$ and $100\mu m$ respectively to allow proper electronic functioning (ie: avoidance of cross-talk etc.). This resulted in approximately 2 mm separation between the CCD's.

The bond pad spacings could be taken directly from the design parameters. The pads were lined up exactly with the CCD bond pads, except near the spacing between the CCD's where the quantity of pads brought to the outside edge dictated that some of the side bond pads be offset.

For the etch alignment technique, another mask had to be made specifically to control the etching area on the wafer. Additional mask alignment marks were added to the metalization mask so that the metalization could be matched up precisely with the etched sockets. Also, the metalized alignment outline described above was removed as it would just appear at the bottom of the socket, and would have no used for alignment.

The main question arising for the size of the etched sockets concerns the etched area needed to get the CCD into the socket and be able to position it without too much difficulty. If we want an extra $40\mu m$ on each side of the CCD on the bottom, this translates to a larger area in the mask design (on top) due to the 54.7° angle of the etched edge (see section 2.5). If the etched edge is to be used as the alignment reference, we need to decide what etch depth will be felt in aligning the CCD. We chose 10% of the CCD height (roughly $50\mu m$) as a figure which should be adequate.

$$\left\{\begin{array}{l} lost space \\ on pit \\ surface \end{array}\right\} = \frac{\{etch \, depth\}}{\tan 54.7^{\circ}} = \frac{50 \, \mu m}{1.412} = 35.41 \mu m$$

Of course we will end up with slightly more space to work with because of the thickness of the wax layer ($\sim 10 \mu m$).

Oxidizing the Silicon wafer

The wafer first needs to be thoroughly cleaned before a SiO_2 layer can be put onto it. Three solutions are used to rid the wafer of any ions or SiO_2 . The first is Ammonium Hydroxide-1 part, H_2O - 8 parts, H_2O_2 - 2 parts. We boil the wafer in the solution at 80 deg C for about 10 minutes. The wafer is rinsed and put into a Hydrofluoric acid (HF) bath for 30 seconds to get rid of any SiO_2 (1 -100, HF - H_2O). The wafer is again rinsed and put in a HCl, water, H_2O_2 , solution (same ratios as1st solution) at 80 deg C for another 10 minutes. After rinsing and drying, the wafer is ready for oxidation in the furnace.

The wafer is inserted in the furnace in a holder at 750 deg C. The temperature of the oven is then increased to 1100 deg C. We can then introduce first dry oxygen gas, followed by wet oxygen gas for a time depending on the layer thickness desired, and number of wafers in the furnace. For a $1\mu m$ layer on 6 wafers, we use 30 minutes of dry oxygen and 2 hours of wet oxygen. Then the furnace temperature can be reduced to 750 deg C and the wafers removed to cool.

Mask Making

The masks are made from the emulsion pattern on a overhead-type plastic page using a contact printing method. The following setup is used:

The photosensitive mask plate is inserted with the emulsion page in the black box with glass window on top. It is illuminated for 40 seconds. The mask is then put in appropriate developer for 5 minutes, followed by the fixing solution for another 5 minutes. Then it is transferred to a water wash for roughly 15 minutes, and finally photo-flo is used to avoid streaking. The mask is then ready to be used for photo-lithography.

Etching

The essential process consists of opening a hole in the SiO_2 so the etchant can act on



Figure A.2: mask contact printing

the bare silicon. The following procedures and times were found to give good results:

The wafer is first hard baked for 30 min. to drive off moisture. This will allow the photoresist to adhere to the wafer. Photoresist is then spun on at 4000 rpm, for 30 seconds. A soft bake follows for 30 minutes to harden the photoresist.

The mask aligner can then be set up to expose the etch pattern on the wafer. All surfaces are thoroughly cleaned. The mask is inserted emulsion side down (with the word ETCH readable) for contact printing. We use a coarse alignment of the edges of the Si wafer with the mask edges. This will make a good reference point when the metalization mask needs to be precisely aligned under the microscope. Then contact is made between the wafer and the mask, and we expose with UV light for 45 seconds.

A one minute developing time followed by a rinse in DI water gets rid of the photoresist in the exposed areas. The photoresist, once hardened will resist the BOE (buffered oxide etch, 1 part HF to 10 parts ammonium fluoride), thus the wafer is hard baked for another 30 minutes. Then 5 minutes in the BOE solution will open the desired hole(s) in the SiO_2 layer. (Note that the BOE will etch away at metal handling devices, such as tweezers, so plastic should be used.) A good test for when the BOE has etched through the SiO_2 is the hydrophobicity of silicon - water will shoot off bare silicon, while it will bead on the SiO_2 . Finally the remaining photoresist can be removed by an acetone bath.

The wafer is then ready for the etchant bath. In this case, 20 minutes submerged in EDP with pyrazine added.

Photo-lithography on aluminized wafer

First a $1\mu m$ aluminum layer is sputtered onto the cleaned wafer surface. The resulting wafer can then be contact printed as in the etching procedure above. When developed and hardened, the photoresist will stop the aluminum from being washed away by the aluminum etch solution maintained at 50°C. Acetone is then used to get rid of the remaining photoresist over the resulting aluminum pattern.

Appendix B

Grinding and Mounting INVAR

The Invar plate is first machined to size from the rough slab. The annealing process then requires an oven temperature of 350°C for one hour followed by some lower temperature cycling. The stress relief will cause some warpage to the Invar plate. Both sides are initially ground on a magnetic chuck with a random motion wheel grinder. The backside must also be flat for thermal contact with the aluminum cooling plate. Three stages of polishing using finer grit paper in a figure eight pattern then bring the plate to within $\pm 5\mu$ flatness overall. The plate should be relatively stress insensitive to temperature changes at this point.

The Si substrate is then mounted on Invar. The steps are: (1) plug up screw holes with blanks to prevent epoxying them in (2) clean both surfaces with propanol (3) apply epoxy glob in center of Invar (4) press plastic wrap over epoxy and work out air bubbles. The optical flat can aid in this process. (5) peel off plastic wrap to leave thin film of epoxy. Successive peel-offs may be necessary to get the desired layer thickness. (6) gently place substrate on the epoxy layer and use probes to align it in place using the screw holes and corners as markers (7) use the PCB as a visual template to ensure the placement is correct. (8) apply even pressure on substrate using weights and the optical flat: kimwipe, optical flat, lead weights (9) carefully remove the weights and inspect and leave to cure.

Appendix C

Calculation of thermal resistance

As we are only concerned with the steady state heat flow solution, we do not need to consider any heat flow differential equation with complicated boundary conditions. We take the sum of the heat flow mechanisms and equate them with the average heat generated by the CCD, $\sim 200 mW$.

$$200mW = \frac{dQ}{dt} = \sum_{i} \frac{dQ_{i}}{dt} = A_{rad} \epsilon \sigma T_{H}^{4} + A_{cond} k \frac{T_{H} - T_{C}}{L} + \frac{dQ_{conv}}{dt}$$

A - area, ϵ - emmisivity, σ - Stephan-Boltzman constant, k - thermal conductivity, L - slab thickness. The three contributors to heat flow are: radiation, conduction and convection. The convection term can be ignored, as we are essentially operating the device in a vacuum. The radiative term is negligible, thus we need only calculate the conduction term. The T_C temperature is generated by a thermoelectric cooler or liquid nitrogen tank. We take the cooler to be operating at ~ 193K.

$$200mW = \frac{(19.35cm^2)(1.09)[\frac{W}{mK}]}{(750\mu m)}(T_1 - 193K)$$
$$T_1 = 193 + 0.071 K$$

The materials are thus feasible for cooling. The temperature rise due to the CCD operation is very small.

References

- C.D.Mackay, CCDs for astronomy, AAAR (Astronomy and Astrophysics Annual Review) 24, pp255 (1986).
- [2] G.Luppino and K.Miller, A modular dewar design and detector mounting strategy for large format astronomical CCD mosaics, PASP (Publications of Astronomy Society of Pacific) 104, pp215-222 (1992).
- [3] C.W. Stubbs et al (19 authors), A 32 megapixel dual color CCD imaging system, Proceedings of SPIE Vol. 1900, p192-204 (1992).
- [4] C.L.Chen, R.W.Johnson, R.C.Jaeger, M.B.Cornelius, W.A.Foster, Multichip thinfilm technology for low temperature packaging, IEEE 40th Electronic Components and Technology Conference, pp571-579, Las Vegas (1990).
- [5] M.Sekiguchi et al., Development of a 2k X 8k Mosaic CCD Camera, PASP 104, pp704-751 (1992).
- [6] S.C. Chapman, CCD Mosaic for possible use with 5m LMT, Undergrad Thesis (Astronomy), UBC (1995).
- [7] K.E.Bean, Anisotropic etching of silicon, IEEE Transactions on Electron Devices
 25, pp1185-1193 (1978).
- [8] A.Reisman, M.Berkenblit, S.A.Chan, F.B.Kaufman, D.C.Green, Controlled etching of silicon in catalyzed EDP solutions, Journal of Electrochemical Society 126, pp1406-1415 (1979).

- [9] X.Wu, Q.Wu and W.Ko, Deep etching of Si using EDP, 3rd Int.Conf on Solid State Sensors, pp333-343, Philadelphia (1986).
- [10] G.Luppino et al., Design of an 8k X 8k pixel CCD mosaic, SPIE 2198, pp 810 (1994).
- [11] B.K.Gibson and P.Hickson, Time-delay integration CCD read-out techniques: image degradation, MNRAS (Monthly Notices of Royal Astronomical Society) 258, pp 543-551 (1992).
- [12] P.Hickson et al., UBC/LAVAL 2.7 Meter Liquid Mirror Telescope, ApJ (Astrophysical Journal) 436, pp L201–L204 (1994).