FABRICATING SILICON MESH BOLOMETERS FOR BAM

By

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Abstract

Silicon membranes have been fabricated and etched into mesh structures using both wet and Cl_2 plasma etching. The most repeatable process involoved wet etching triple bonded wafers with a buried oxide layer. A recipe to build Si meshes, with a grid spacing of 375 μm and leg cross-sections of 5 μm by 30 μm, from 5 μm thick membranes is described. The meshes are supported by 4 legs that are each 30 μm wide and 1 mm long. Also, the resistivity of thin gold films was measured for temperatures ranging from 4.2 K to 300 K. It was found that the ideal thickness, that leads to a sheet resistance of 188 $\Omega/\square$ at 300 mK for of 5 μm by 385 μm gold lines, was 150 Å. A bolometer building process that incorporates the gold evaporations with the mesh building procedure is given, although preliminary attempts to produce bolometers have been unsuccessful.

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Chapter 1

Introduction

The Balloon-borne Anisotropy Measurement (BAM) is designed to measure the temperature fluctuations, or anisotropies, in the cosmic microwave background (CMB) at medium angular scales. Such measurements can provide information about the basic nature of our universe, including its age, density and geometry. Unfortunately, these anisotropies from the CMB mean temperature of 2.7286 K are small; the signal level is a mere $\frac{\Delta T}{T} \approx 10^{-5}$. To be able to detect such small differences in temperature across the sky, any experiment must have very sensitive detectors. What makes BAM unique from other balloon-borne CMB experiments is the sensitive differential Fourier transform spectrometer (FTS), previously used to measure the CMB intensity spectrum from a sounding rocket [1, 2]. Housed within a cryostat at $\sim$2 K so that there are no warm moving parts, the FTS measures the difference in intensity between two 0.7° regions of the sky separated by 3.6°. Each optical output of the spectrometer is independently coupled to a bolometric detector, held at 0.27 K, that measures the total power, incident on it. Thus, each bolometer returns an interferogram proportional to the brightness difference between the two input beams [3].

This thesis describes a program to build novel detectors sensitive enough for the BAM experiment which are less sensitive to cosmic rays and could be frequency tunable. By using common micromachining methods many bolometers of this type could be made in one production cycle. The rest of this chapter is devoted to a brief discussion of bolometer theory and design. Chapter 2 describes the micromachining techniques that

were used in the fabrication process. Chapters 3 and 4 describe experiments to construct the substrate and absorption layer components of the bolometer while the final chapter describes a possible process to build a fully functional bolometer.

1.1 Bolometers

Bolometers are broadband thermal radiation detectors commonly used in astronomical applications to detect far infrared and millimeter wavelength radiation. They can be placed at the receiving end of a horn as the BAM experiment does, or at the end of a waveguide or in a focal plane, where the incident radiation will be absorbed. The detection is made by measuring the the temperature changes in the absorbing material. They are different from other thermal radiation detectors in that they rely on a thermistor whose electrical resistance is heavily dependent on temperature. Once the incident power is absorbed, the temperature of the detector element rises causing a change in the thermistor resistance R. If a constant current or voltage is applied, the change in R can be measured (since it is easier to amplify small voltages, the BAM experiment uses the constant current configuration). Thus, the output of the detector is directly proportional to the bolometric intensity of the radiation incident on it. Some examples of thermistors include carbon resistors, heavily doped Ge and ion implanted Si [4]. For semi-conductor materials and superconducting films near T_c, $dR/dT < 0$, while for metals, $dR/dT > 0$.

Composite bolometers are composed of several key components that can be individually tailored to provide optimal performance for various applications. In contrast, in monolithic bolometers, all the components are integrated into one structure so that the thermistor element is part of the substrate structure [4]. Those previously used on BAM, as shown in Figure 1.1, are composite bolometers consisting of a radiation absorbing bismuth layer on a sapphire support structure and a neutron transmutation doped (NTD)

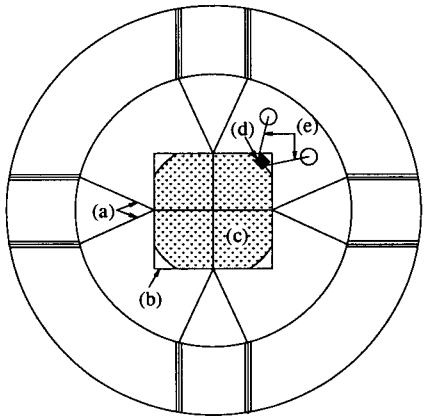

Figure 1.1: A schematic drawing (not to scale) of the 1998 BAM composite bolometer, suspended inside a copper ring: a) nylon support legs b) sapphire substrate, c) thin bismuth film, d) NTD Ge thermistor, and e) brass electrical leads.

germanium thermistor [5]. The bolometer is suspended within a copper ring by 4 twisted pairs of nylon surgical threads. For an effective bolometer, the radiation absorber should have a large absorptivity over the desired frequency range and be of an appropriate size for the optical system. As well, the thermistor's electrical resistance should have an strong temperature dependence and have low electrical noise. The supporting substrate should not only be mechanically rigid and have a large thermal conductivity so that it remains isothermal during operation, but also, it should be thermally isolated from its surroundings. The mechanical support for the device should have low thermal conductivity and provide a weak link to the heat sink. All of the above components should have a low heat capacity to reduce the thermal time constant of the device.

The next four sections will briefly describe how the bolometer responds to incident electromagnetic waves.

1.2 Impedance Matching to Free Space

When radiation is incident on the bolometer, its initial function is to absorb as much power as it can and dissipate it thermally. Since the absorber is typically a thin metallic film, whose thickness is much thinner than a mm wavelength, deposited on a dielectric substrate, the optical properties of this system are easily described by comparing the bolometer to a resistive short in a transmission line. The reader is directed to Ulrich's article on the far infrared properties of metallic mesh structures [6] for greater detail.

Imagine a transmission line composed of two slightly separated parallel conductors along the z-direction connected by an AC source. There is a capacitance C and inductance L per unit length of the wires. As the circuit is driven by an AC signal, the time varying current produces a counter emf dV proportional to the inductance, which in turn produces a current dI since the wires are also coupled by their capacitance. That is,

$$dV = \frac{\partial V}{\partial z}dz = -Ldz\frac{\partial I}{\partial t}, \tag{1.1}$$

$$dI = \frac{\partial I}{\partial z}dz = -Cdz\frac{\partial V}{\partial t}. \tag{1.2}$$

These two equations lead to the following coupled differential equations,

$$\frac{\partial V}{\partial z} = -L\frac{\partial I}{\partial t}, \tag{1.3}$$

$$\frac{\partial I}{\partial z} = -C\frac{\partial V}{\partial t}. \tag{1.4}$$

Differentiating (1.3) with respect to z and (1.4) with respect to t gives,

$$\frac{\partial^2 V}{\partial z^2} = -L\frac{\partial^2 I}{\partial t \partial z}, \tag{1.5}$$

and

$$\frac{\partial^2 I}{\partial z \partial t} = -C\frac{\partial^2 V}{\partial t^2}. \tag{1.6}$$

Substitution of (1.5) into (1.6), or vice versa leads to two second order differential equations that are easily recognized as one dimensional wave equations for the voltage and the current:

$$\frac{\partial^2 V}{\partial z^2} = LC\frac{\partial^2 V}{\partial t^2}, \tag{1.7}$$

$$\frac{\partial^2 I}{\partial z^2} = LC\frac{\partial^2 I}{\partial t^2}. \tag{1.8}$$

The propagation speed of the current and voltage down the line is just $v^2 = 1/LC$ or,

$$v = \frac{1}{\sqrt{LC}}. \tag{1.9}$$

The solution to (1.7) is a superposition of two traveling waves,

$$V(z,t) = V_- + V_+, \tag{1.10}$$

where $V_- = V_-(t + z/v)$ describes a wave moving to the left and $V_+ = V_+(t - z/v)$ describes a wave moving to the right. To find $I(z,t)$, use (1.3) and differentiate $V(z,t)$ with respect to z, then integrate with respect to t. This gives

$$I(z,t) = \frac{1}{vL}(V_+ - V_-). \tag{1.11}$$

In order to get the characteristic impedance of the transmission line Z_ℓ, one only needs to take the ratio between V and I for either of the traveling waves. Then,

$$Z_\ell = \frac{V}{I} = \sqrt{\frac{L}{C}}. \tag{1.12}$$

If the line is terminated by a load whose impedance matches Z_ℓ, then the signal will not be reflected by the load, but instead, all the power will be transferred to the load.

Now consider a resistive load with impedance Z_L *shorting* an infinite transmission line as in Figure 1.2. Since the load acts like an impedance in parallel with the line, the equivalent impedance Z_T of the circuit becomes,

$$Z_T = \frac{Z_L Z_\ell}{Z_L + Z_\ell}. \tag{1.13}$$

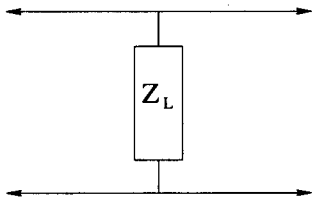

Figure 1.2: Infinite transmission line with a resistive short.

A signal, $I_\circ$ traveling down the line, once encountering the short, will be partially reflected, I_r, and partially transmitted, I_t past the load to the remainder of the line. The voltage $V_\circ$, is the sum of the reflected and transmitted waves, that is,

$$V_\circ = V_t - V_r. \tag{1.14}$$

What is of interest is the power dissipated in the load. The current through the load I_L is given by:

$$I_L = \frac{V_L}{Z_L}, \tag{1.15}$$

$$I_L = I_\circ + I_r - I_t \tag{1.16}$$

$$= \frac{V_\circ}{Z_\ell} - \frac{V_r + V_t}{Z_\ell}, \tag{1.17}$$

where V_L=V_t since the drop across the load is the same as the drop across the rest of the line. Substituting (1.14) into (1.15) and (1.17) leads to,

$$\frac{V_\circ}{Z_L} = -V_r \frac{2Z_L + Z_\ell}{Z_L Z_\ell} \tag{1.18}$$

The ratios $V_r/V_\circ$ and $V_t/V_\circ$ are useful quantities called the reflection and transmission coefficients ρ and τ respectively and $\tau - \rho = 1$. From (1.18),

$$\rho = -\frac{Z_\ell}{2Z_L + Z_\ell}. \tag{1.19}$$

$$\tau = \frac{2Z_L}{2Z_L + Z_\ell}. \tag{1.20}$$

The fractional reflected power is the ratio $P_R = P_r/P_\circ$, where $P_r = V_r^2/Z_\ell$ is the power in the reflected wave and $P_\circ = V_\circ^2/Z_\ell$ is the power in the source signal. It can be immediately seen that

$$P_R = \frac{V_r^2}{V_\circ^2} = \rho^2. \tag{1.21}$$

Similarly, the fractional transmitted power $P_T = \tau^2$. From conservation of energy, the power dissipated through the load, P_L is

$$P_L = 1 - \rho^2 - \tau^2 \tag{1.22}$$

Combining (1.19), (1.20) and (1.22) lead to the following equation for P_L in terms of Z_L and Z_ℓ,

$$P_L = 1 - \frac{Z_\ell^2 + 4Z_L^2}{(2Z_L + Z_\ell)^2} \tag{1.23}$$

The value of Z_L which maximizes (1.23) can be found with first year calculus,

$$\frac{dP_L}{dZ_L} = Z_\ell(Z_\ell - 2Z_L) = 0. \tag{1.24}$$

Thus,

$$Z_L = \frac{Z_\ell}{2}, 0. \tag{1.25}$$

A quick check with the second derivative shows that $Z_L = Z_\ell/2$ is in fact the maximum. Clearly, to maximize the power dissipated in the load, its impedance should be half the transmission line impedance. Returning to (1.19), (1.20) and (1.22), one finds that half of the signal power is dissipated in the load, while a quarter is reflected and the remaining quarter is in the rest of the line.

Electromagnetic waves traveling through free space and encountering the absorbing layer of the bolometer at normal incidence can be thought of as signals encountering parallel admittances on a transmission line. In fact, this optics system is completely analogous to the shorted transmission line described above, and one only has to replace V with the electric field E_x, I with the magnetic field B_y, L with $\mu_\circ$ and finally C with $\varepsilon_\circ$.

Then, the wave equations for the optics case is just the results of Maxwell's equations for the electric and magnetic fields traveling through free space:

$$\frac{\partial^2 E_x}{\partial z^2} = \varepsilon_\circ \mu_\circ \frac{\partial^2 E_x}{\partial t^2}, \tag{1.26}$$

$$\frac{\partial^2 B_y}{\partial z^2} = \varepsilon_\circ \mu_\circ \frac{\partial^2 B_y}{\partial t^2}. \tag{1.27}$$

The propagation speed is just $v = 1/\sqrt{\varepsilon_\circ \mu_\circ} = c$ which is the speed of light in a vacuum. The impedance of free space, $Z_\circ$ is given by (1.12) with the proper substitutions, giving

$$\begin{aligned} Z_\circ &= \sqrt{\frac{\mu_\circ}{\varepsilon_\circ}} \\ &= 377\,\Omega. \end{aligned} \tag{1.28}$$

So, for the bolometer to absorb the maximum amount of power, its absorbing medium should have an impedance of $Z_{bolo} = Z_\circ/2 = 188.5\,\Omega$. If the absorbing medium consists of a metallized mesh made up of $N \times N$ leg segments with each leg having an impedance Z_l, the impedance of the entire mesh, Z_{mesh}, can be calculated. If a voltage is applied from one side of the mesh to the other, there are N legs in series and N legs in parallel so that

$$Z_{mesh} = (N \times \frac{1}{NZ_l})^{-1} \tag{1.29}$$

$$= Z_l. \tag{1.30}$$

Therefore, each metallized leg of the absorbing grid in our bolometer should have an impedance of $188.5\,\Omega$. The above works well for meshes with a grid spacing much less than the wavelengths being detected and so it is possible to build frequency tuned bolometers [16].

1.3 Thermal Properties of the Bolometer

As the bolometer absorbs power from some radiant source $P_\gamma = P_\circ + P_1(t)$, where $P_\circ$ is time independent and $P_1(t)$ is the time dependent part, the temperature of the bolometer

will vary, $T_B = T_\circ + T_1(t)$. The electrical power input to the constant current biased thermistor varies since the resistance depends on T_B. To first order, $P_R = I^2R(T_\circ) + I^2\,(dR/dT)\,T_1(t)$. Some power will be stored in the heat capacity, $P_C = C\,dT_B/dt = C\,dT_1/dt$ while the rest flows through a thermal link with conductance, $G(T)$, to the heat sink held at temperature T_S. To first order, $P_G = G(T)(T_\circ - T_S) + \frac{dP}{dT}T_1$. The thermal circuit is sketched in Figure 1.3 and can be written as:

$$\begin{aligned} \sum P_i &= C\frac{dT_1}{dt} \\ P_\circ + P_1(t) + I^2(R(T_\circ) + \frac{dR}{dT}T_1) &= G(T_\circ)(T_\circ - T_S) + G_D T_1 + C\frac{dT_1}{dt}. \end{aligned} \tag{1.31}$$

$G_D = dP/dT$ is the dynamical thermal conductance which arises since the thermal conductivity changes rapidly with T at low temperatures. From the time independent terms of (1.31) one arrives at the steady state heat flow equation where the bolometer is in thermal equilibrium with the heat sink and a constant background power loading $P_\circ$.

$$P_\circ + I^2R(T_\circ) = G(T_\circ)(T_\circ - T_S) \tag{1.32}$$

The time dependent terms give

$$P_1(t) - C\frac{dT_1}{dt} = T_1(t)(G_D - I^2\frac{dR}{dT}). \tag{1.33}$$

Thus, the temperature change T_1 is influenced by the thermal feedback from the thermistor element. Defining

$$\alpha = \frac{1}{R}\frac{dR}{dT}, \tag{1.34}$$

(1.33) can be rewritten as

$$P_1(t) - C\frac{dT_1}{dt} = T_1(t)(G_D - \alpha P_\circ). \tag{1.35}$$

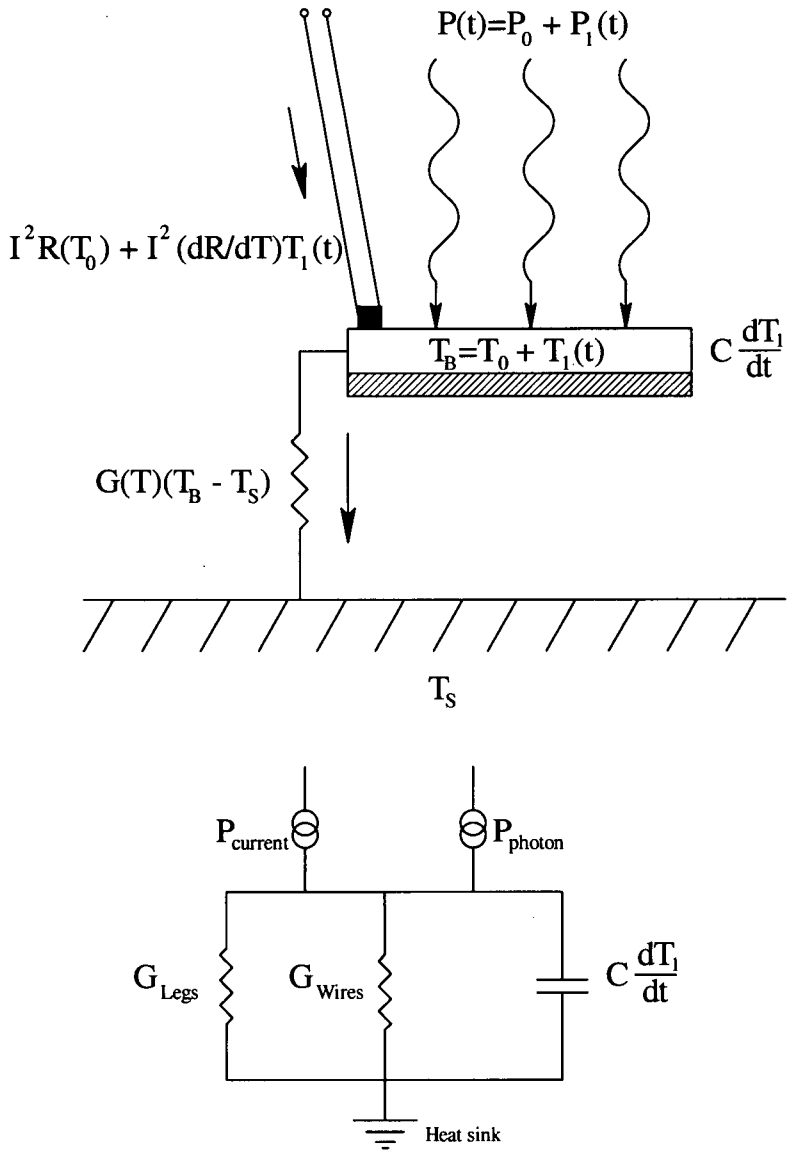

Figure 1.3: A schematic diagram of the bolometer and the equivalent thermal circuit.

The quantity $G_D - \alpha P_\circ$ is sometimes called the effective thermal conductance G_e. For neutron transmutation doped (NTD) germanium thermistors, $\alpha < 0$ and so $G_e > G_D$. Rewriting (1.33), the resulting first order differential equation is just,

$$C\frac{dT_1}{dt} + G_e T_1(t) = P_1(t). \tag{1.36}$$

If the radiant power is constant, $P_1(t) = 0$, with the initial condition $T_1(0) = T'$, $T' > T_\circ$, then the solution to (1.36) is simply $T_1(t) = T'e^{-\frac{G_e}{C}t}$. The time it takes for the bolometer temperature to decay to $1/e$ of its peak value is $\tau = C/G_e$. This quantity is called the characteristic thermal time constant of the device.

For a sinusoidal power input $P_1(t) = pe^{i\omega t}$, the solution to (1.36) is

$$T_1(t) = \frac{p}{G_e + i\omega C}e^{i\omega t}. \tag{1.37}$$

Both C and G depend on the physical properties of the material and its temperature. The heat capacity is a product of the body's mass m and the specific heat $\kappa(T)$, where $\kappa(T) = \gamma T + \beta T^3$ for metals and $\kappa(T) = \beta T^3$ for insulators. Here, γ is the electronic contribution to the material's heat capacity and β is the lattice contribution due to phonons. Table 1.1 shows estimated specific heats for materials typically used in bolometer construction.

The thermal conductance is proportional to the cross-sectional area A through which the heat flows, and inversely proportional to the length l, so that $G = k(T)A/l$, where $k(T)$ is the thermal conductivity of the material. However, since for some materials $k(T)$ depends rapidly on T, especially at low T, it is common to define and use the *average* thermal conductance,

$$\bar{G} = \frac{A}{l}\frac{1}{T_S - T_\circ}\int_{T_\circ}^{T_S} k(T)dT \tag{1.38}$$

Material	γ ($J/cm^3\,K^2$)	β ($J/cm^3\,K^4$)	$\kappa(0.270)$ ($J/cm^3\,K$)
Pd	1.1×10^{-3}	1.1×10^{-5}	2.97×10^{-4}
Au	6.8×10^{-5}	4.5×10^{-5}	1.92×10^{-5}
Ge	2.0×10^{-9}	3.0×10^{-6}	2.93×10^{-7}
Brass	9.7×10^{-5}	7.9×10^{-6}	2.63×10^{-5}
Bi	3.8×10^{-7}	5.3×10^{-5}	1.15×10^{-6}
Ti [7]	1.6×10^{-5}	1.2×10^{-7}	4.32×10^{-6}
Si [8]	2.1×10^{-5}	6.8×10^{-6}	8.78×10^{-8}
SiO_2 [9]	-	3.7×10^{-5}	7.28×10^{-7}

Table 1.1: Estimated specific heats for materials commonly used in bolometers. $\kappa(T) = \gamma T + \beta T^3$ (from [10] unless otherwise noted.)

At cryogenic temperatures, most of the thermal transport in insulators is carried by phonons and $k(T) \propto T^3$. On the other hand, in pure metals, electrons carry most of the heat current and $k(T) \propto T$. In this last proportionality there is a nearly universal value for how the proportionality constant scales with electrical conduction given by the Wiedemann-Franz law,

$$\begin{aligned} k(T) &= \frac{\pi^2 k_B^2}{3e^2}\sigma T \\ &= \mathcal{L}\sigma T. \end{aligned} \tag{1.39}$$

$\mathcal{L} = 25\ \mathrm{nW\Omega/K^2}$ is the Lorentz constant and $\sigma = \sigma(T)$ is the electrical conductivity. This relation allows one to calculate the thermal conductivity of a metal after measuring its electrical conductivity at temperature T.

1.4 Responsivity

The absorbed power responsivity of a bolometer is defined to be the change in voltage per watt of absorbed signal power, i.e., $S_A = V_1/P_1$. Since $V_1 = I(dR/dT)T_1$ and given

(1.36), one can write

$$S_A = \frac{\alpha T_1 V}{G_e T_1 + C\frac{dT_1}{dt}}. \tag{1.40}$$

Another useful quantity that is more easily measurable is the electrical responsivity, $S_E = V/P_E$, which characterizes how the bolometer responds to changes in the electrical power dissipated in the thermistor. Rewriting (1.40) in terms of the voltage V across the resistor,

$$S_E = \frac{\alpha V}{G_D - \alpha P}. \tag{1.41}$$

Assuming there is no radiant power on the bolometer (although the result is valid if there is a constant background power loading $P_\circ$ [11]) and using $dV = d(IR) = RdI + IdR$ and $dP = d(IV) = 2VdI + P\alpha dT = GdT$, one can solve for dV and dI.

$$dV = RdI + V\alpha dT \tag{1.42}$$

$$dI = \frac{(G - \alpha P)dT}{2V}. \tag{1.43}$$

Letting $Z = dV/dI$,

$$Z = R\frac{G + \alpha P}{G - \alpha P}. \tag{1.44}$$

Solving for G,

$$G = \alpha P\frac{Z + R}{Z - R} \tag{1.45}$$

$$= I^2\frac{dR}{dT}\frac{Z + R}{Z - R}, \tag{1.46}$$

and substituting (1.45) into (1.41),

$$S_E = \frac{Z - R}{2IR}. \tag{1.47}$$

I–V curves for one of the composite sapphire chip bolometers we made for the 1998 BAM flight are graphed in Figure 1.4. The resistance $R = V/I$ depends on the temperature (as can be seen from the upper two curves of the bolometer held at slightly different temperatures.) and on the radiative load (comparing the lower two curves for the bolometer held at the same temperature). Thus, if the bolometer is cooled to its operating temperature and one measures its I–V curve, S_E can be determined for various bias currents. As well, once $R(T)$ is known, $G(T)$ can be calculated from (1.46).

By changing the bias current with a large step function and observing the resulting voltage change, one can measure τ and hence arrive at a value for C. To determine the time constant of the same bolometer used in the 1998 BAM flight, we examined the detector response to 3 normalized cosmic rays hits. The optical system and electronics of the experiment was modeled and fitted to the 3 cosmic rays. The solid line in Figure 1.5 is the model with a time constant of $\sim$5.5 ms, which seems to fit the detector response fairly well. The tail end of the response is set by filters in the electronics which were not included in the model.

1.5 Noise

It is useful to scale the various noise sources in a bolometer by the appropriate sensitivity and express the quadrature sum as the noise equivalent power, or NEP. This is the incident power which produces a signal equal to the noise in a one Hz bandwidth. The dominant sources of noise in bolometers, as shown in in Figure 1.6, include Johnson noise, amplifier noise, and phonon or thermal fluctuation noise. For greater detail on the noise terms presented here, the reader is directed to Mather's articles [12, 13]. Other

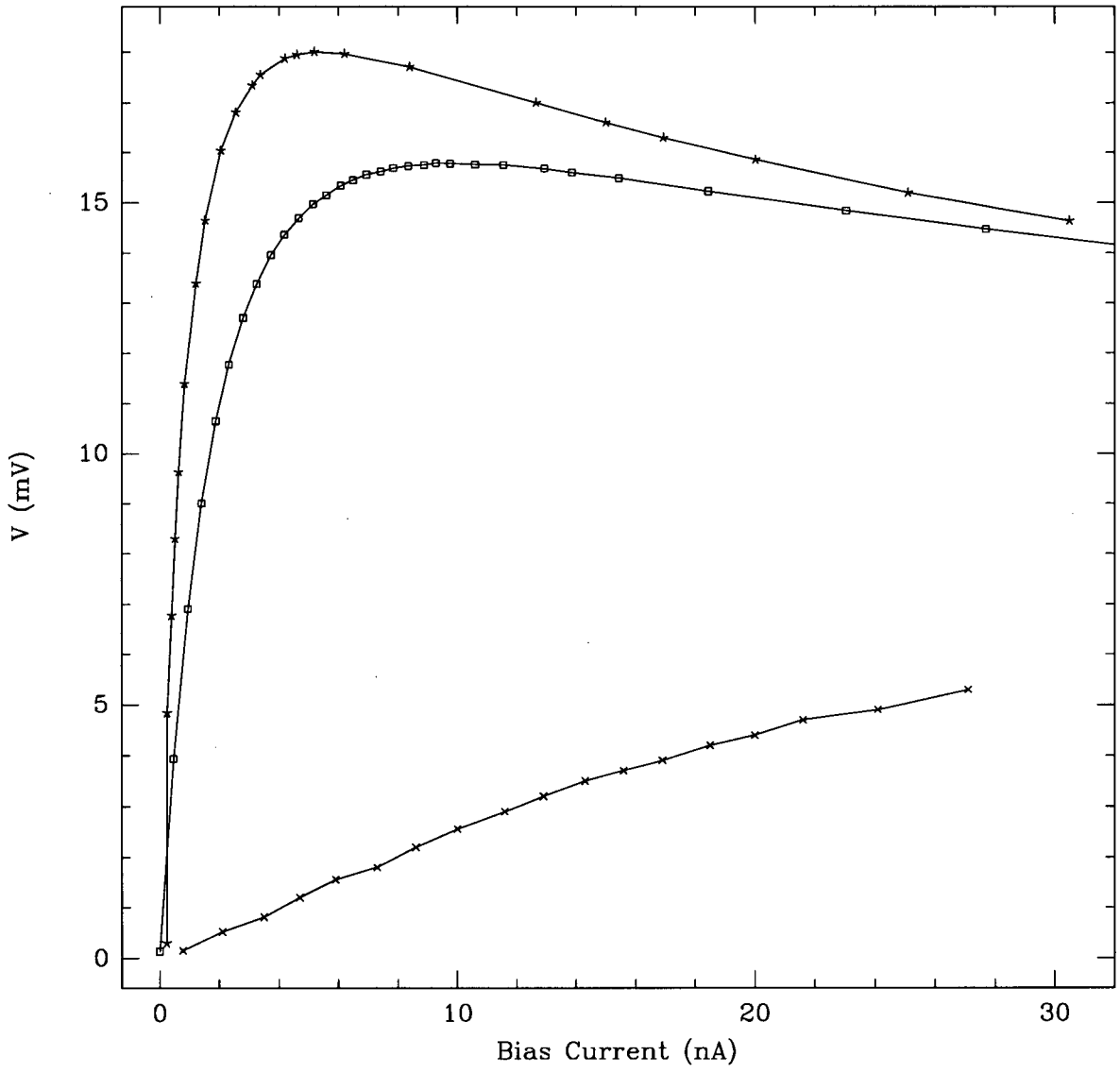

Figure 1.4: I–V curves for one of the sapphire and NTD Ge chip bolometers used in the 1998 BAM flight. Bolometer cooled to T=0.263 K and looking at a cold load calibrator ($\star$), bolometer cooled to T=0.269 K and looking at the same cold load ($\square$), bolometer cooled to T=0.269 K looking at the room ($\times$). Solid lines are not fits but are just to lead the eye.

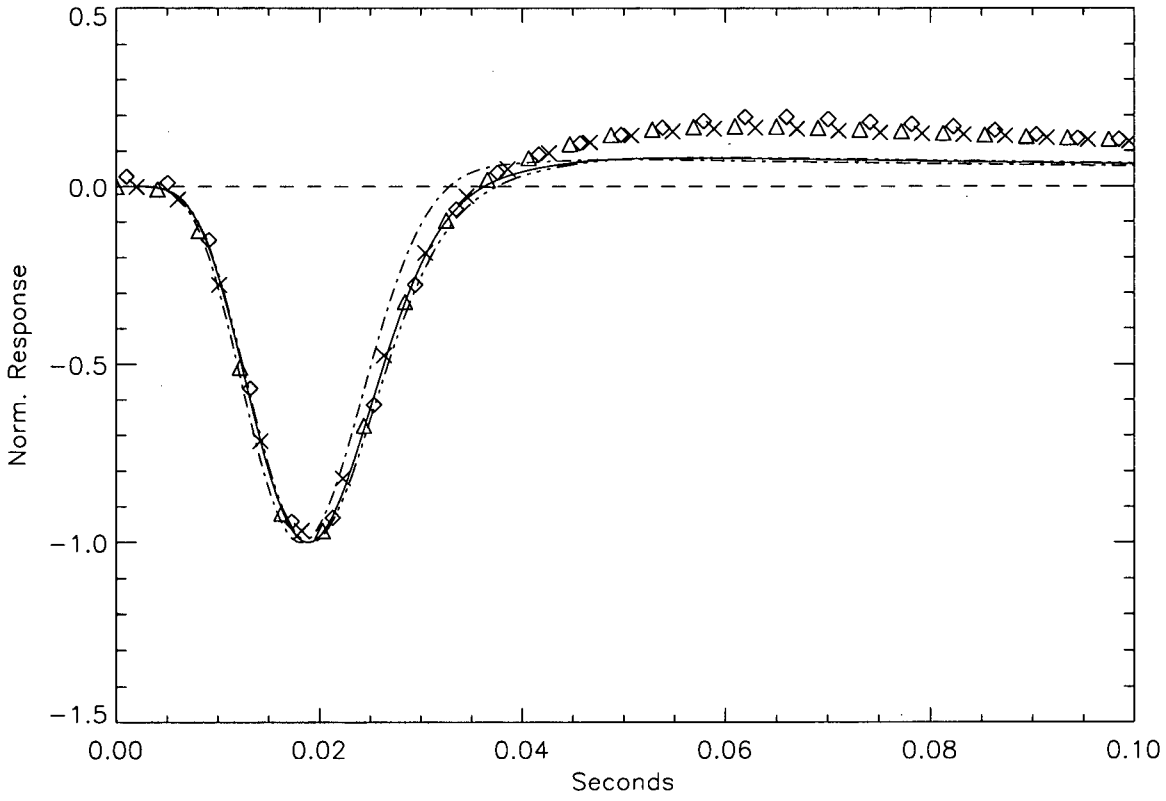

Figure 1.5: Modeling the 1998 flight bolometer's response to cosmic ray hits to determine the thermal time constant. The lines are for the model with $\tau = 4\,\text{ms}(-\cdot-)$, $\tau = 5.5\,\text{ms}(—)$, $\tau = 6\,\text{ms}$ $(-\cdot\cdot\cdot)$ and three different cosmic ray hits ($\triangle$,$\diamond$,$\times$) occurring at $t = 0$.

contributions to the noise include cosmic rays and microphonics.

In simple bolometer theory, the Johnson noise, from voltage fluctuations in the resistive thermistor element arises in the form $NEP_J^2 = V_J/S^2 = 4k_BTR/S^2$. However, this ignores the electrothermal feedback since the bias current does work on the Johnson noise source. Since any increase in V_J increases the temperature of the bolometer, which lowers the resistance and decreases the output voltage, the Johnson noise is actually reduced by as much as 60% [12]. This can be described by the equivalent Johnson noise source, $V_J' = V_J(Z+R)/2R = \sqrt{4k_BTR}(Z+R)/2R$. Thus, combined with (1.47),

$$NEP_J^2 = 4k_BTP\left(\frac{Z+R}{Z-R}\right)^2. \tag{1.48}$$

The noise in the first stage of amplification, at the amplifier input, is described by $NEP_a^2 = (V_a^2 + (I_aR)^2)/S^2$. In order for the noise in the amplifier to be unimportant, the temperature T_N at which the $NEP_a = NEP_J$ should be less than the operating temperature of the bolometer.

Because the bolometer is connected to a heat sink at temperature T_S via an average thermal conductance $\bar{G}$, there are energy fluctuations in the bolometer caused by traveling phonons or electrons. When the system is in thermal equilibrium, the noise fluctuations are described by,

$$NEP_{phonon}^2 = 4k_BT^2\bar{G}. \tag{1.49}$$

If there is a large responsivity S, then both NEP_J and NEP_a become negligible, and the phonon noise term dominates the total NEP of the bolometer.

Another concern in balloon borne CMB experiments is the bolometer's sensitivity to cosmic ray hits in the upper atmosphere. These hits leave power spikes in the data and are a major source of noise. Figure 1.7 shows the number of cosmic ray hits during the

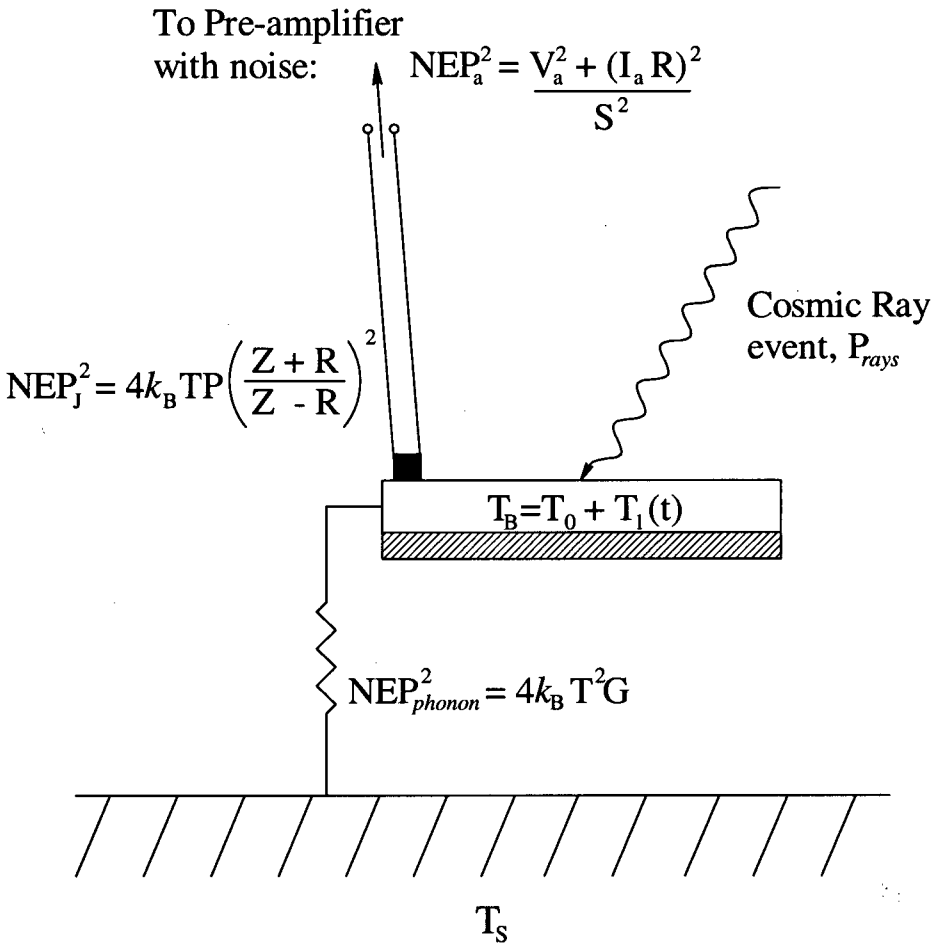

Figure 1.6: Block drawing of bolometer noise sources.

1995 BAM flight. The float altitude was 41.5 km and remained at that position for 4 hours, for which 8.7% of the data was lost due to cosmic rays. Notice that there are many cosmic ray hits in every minute of the flight, posing a large data editing problem. An improvement then would be to reduce the geometric cross-section (also lowering the total heat capacity) of the radiation absorber without compromising the sensitivity of the device.

1.6 Bolometer Design and Constraints

On its previous two flights, BAM used bolometers that were individually hand-made (see Figure 1.1) with a 200 Å layer of evaporated bismuth on a solid sapphire chip suspended by surgical nylon threads. The thermistor element was a 250 μm cube of neutron transmutation doped (NTD) germanium whose resistance near 0.3 K is heavily dependent on temperature. This was glued to the non-metallized side of the sapphire with a trace amount of epoxy. The electrical connection consisted of 0.0003″ diameter brass leads which were indium soldered to gold pads on opposing sides of the NTD Ge chip.

Several improvements can be made to this bolometer design. As previously mentioned, these detectors are subject to cosmic ray hits whose effects can be reduced by decreasing the geometric cross-section of the device. This can be achieved by fabricating web or mesh structures that have grid spacings suitable to the appropriate wavelengths to be measured. Previously, the BAM bolometers used solid sapphire chips and NTD Ge thermistors which have volumes of 3.1×10^8 μm^3 and 1.7×10^7 μm^3 respectively. A 16 mm^2 mesh with 40 μm wide and 5 μm thick lines effectively reduces the cosmic ray cross-section by a factor of $\sim$20. Reducing the volume of the mesh further does not significantly reduce the cross-section to cosmic rays due to the presence of the thermistor.

Also, the current composite bolometers are individually hand-made, leading to devices

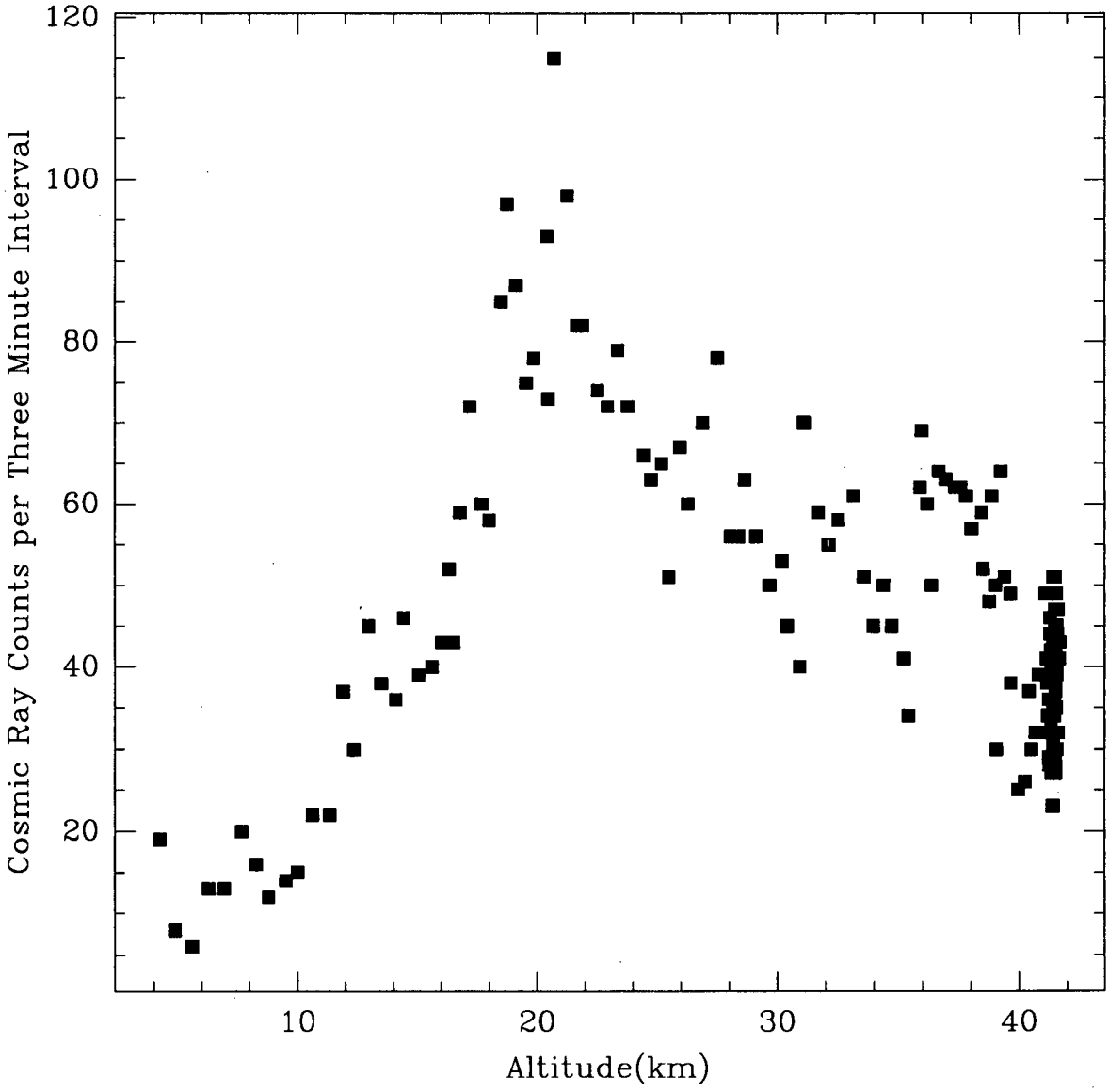

Figure 1.7: The number of cosmic ray hits during the 1995 flight. [14]

with slightly different characteristics depending on the craftsmanship, and having a longer production time. It would be preferable to build many bolometers, all with identical characteristics, in one production cycle. This is possible if one applies micromachining techniques to bolometer construction.

Such improvements have already been made by Mauskopf et al. using a Si_3N_4 membrane 1 μm thick etched into a spiderweb pattern [15]. Generally, however, Si_3N_4 processing capabilities are less accessible whereas most cleanrooms support basic silicon processing techniques. If Si wafers are used, one could also develop tuned bolometers that are frequency selective [16]. Thus, it is of interest to build micromesh bolometers from easily obtainable silicon wafers.

The proposed design is shown in Figure 1.8. The center grid will be patterned from a free-standing silicon membrane held in place to a surrounding silicon frame (the heat sink) by four silicon legs. A thin ($\sim$200 Å) metal layer will be evaporated onto the grid area to act as the radiation absorber, while the NTD Ge thermistor is glued to the center of the mesh on the side opposite the gold layer. Two brass electrical leads will run from the thermistor to gold contact pads located on the Si frame.

From the previous noise and responsivity discussions, one can design a bolometer optimized for the BAM experiment. The maximum noise at the bolometer input is $NEP_{max} = 10^{-16}\,\mathrm{W/Hz^{\frac{1}{2}}}$. Since this quantity is dominated by the phonon noise, (1.49) gives an upper limit for the thermal conductance to the heat sink, held at 0.27 K, to be $G = 2.48\times10^{-9}\,\mathrm{W/K}$. The thermal conductivities of brass and silicon are $2\times10^{-3}\,\mathrm{W/cmK}$ [9] and $2.4\times10^{-5}\,\mathrm{W/cmK}$ [17] respectively (see Table 1.2). If the same NTD Ge thermistors are used on the mesh bolometers, then the two 4 mm long, 0.0003″ diameter brass leads dominate the thermal conductance with $G_{Brass} = 4.5\times10^{-9}\,\mathrm{W/K}$. This exceeds the noise budget and leads to a total $NEP_{Brass} = 1.4\times10^{-16}\,\mathrm{W/Hz^{\frac{1}{2}}}$. A similar calculation for 4, 1 mm long Si support legs does not add significantly to the total

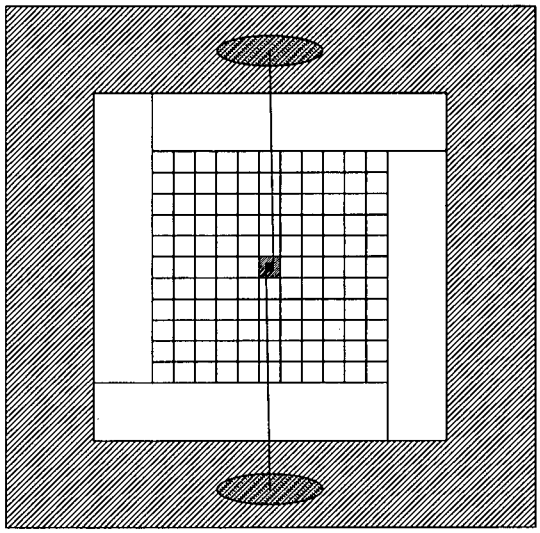

Figure 1.8: The proposed Si micromesh bolometer design to detect the CMB. The entire device is $10\,\mathrm{mm}^2$. The bolometer element is an NTD Ge thermistor with $\sim$4 mm long brass electrical leads while the absorbing layer consists of a Au grid with $R = 188\,\Omega/\square$.

thermal noise if the cross-sectional area of each leg does not exceed $150\,\mu m^2$. This upper limit contributes $G_{legs} = 1.44 \times 10^{-9}\,W/K$ and brings the phonon noise total to $NEP_{phonon} = 1.55 \times 10^{-16}\,W/Hz^{\frac{1}{2}}$ at 270 mK. The value of k for thin legs of Si is less than the bulk value since the mean free path of the phonons is greater than the leg dimensions [17]. If this was not the case then the Si support legs would have to undergo ion bombardment to destroy the crystal structure. It is possible to reduce the total phonon noise by increasing the length of the brass wires or by forming gold contact lines on the substrate to which the thermistor could be attached.

Material	$k(0.27)$ (W/cm K)	Dimensions (cm)			A/ℓ (cm)	#	G_{270mK} (W/K)
		w or r	t	ℓ			
Brass	$2.0 \cdot 10^{-3}$	$3.8 \cdot 10^{-4}$	–	0.4	$1.1 \cdot 10^{-6}$	2	$4.5 \cdot 10^{-9}$
$Si_{support\ leg}$	$2.4 \cdot 10^{-5}$[17]	$3.0 \cdot 10^{-3}$	$5.0 \cdot 10^{-4}$	0.1	$1.5 \cdot 10^{-5}$	4	$1.4 \cdot 10^{-9}$
Si_{bulk}	$\sim 4 \cdot 10^{-4}$	$3.0 \cdot 10^{-3}$	$5.0 \cdot 10^{-4}$	0.1	$1.5 \cdot 10^{-5}$	4	$\sim 2 \cdot 10^{-8}$
$Si_{mesh\ leg}$	$2.4 \cdot 10^{-5}$[17]	$3.0 \cdot 10^{-3}$	$5.0 \cdot 10^{-4}$	0.4	$3.75 \cdot 10^{-6}$	1	$9.0 \cdot 10^{-11}$
$Au_{mesh\ leg}$	$1.8 \cdot 10^{-3}$	$5.0 \cdot 10^{-4}$	$1.5 \cdot 10^{-6}$	0.4	$1.9 \cdot 10^{-9}$	1	$3.4 \cdot 10^{-12}$

Table 1.2: Estimated thermal conductance at 270 mK, for bolometer components with the listed dimensions. Values of k from [9] unless otherwise noted.

To keep the thermal time constant lower than $\tau = 5.5$ ms, the total heat capacity of the bolometer cannot exceed $C_{max} = 0.0055 \times 6.0 \times 10^{-9}\,J/K = 3.3 \times 10^{-11}\,J/K$. Using the data in Table 1.1, one can estimate the heat capacity of each bolometer component, at 270 mK as shown in Table 1.3. Clearly the thermistor and brass leads dominate the heat capacity of the entire device, however the total heat capacity is well below C_{max} and $\tau \approx 2$ ms.

When determining the particular dimensions of the remaining bolometer components, the only constraint is to keep the cross section of the support legs under $150\,\mu m^2$. From researching micromachining techniques, fabricating Si membranes with thicknesses of the

order of a few microns seemed fairly common. So, the initial thickness of the support legs was taken to be 5 μm, leading to a width of 30 μm.

Material	κ (J/cc K)	Dimensions (cm)			Volume (cc)	#	C_{270mK} (J/K)
		w or r	ℓ	t			
Pd	$2.97 \cdot 10^{-4}$	0.025	0.025	$2.0 \cdot 10^{-6}$	$1.25 \cdot 10^{-9}$	2	$7.43 \cdot 10^{-13}$
Au	$1.92 \cdot 10^{-5}$	0.025	0.025	$2.5 \cdot 10^{-5}$	$1.56 \cdot 10^{-8}$	2	$6.00 \cdot 10^{-13}$
NTD Ge	$2.93 \cdot 10^{-7}$	0.025	0.025	0.0275	$1.72 \cdot 10^{-5}$	1	$5.03 \cdot 10^{-12}$
Brass	$2.63 \cdot 10^{-5}$	$3.8 \cdot 10^{-4}$	0.4	–	$1.82 \cdot 10^{-7}/2$	2	$4.80 \cdot 10^{-12}$
Bi *	$1.15 \cdot 10^{-6}$	$3.0 \cdot 10^{-3}$	0.4	$2 \cdot 10^{-6}$	$2.9 \cdot 10^{-9}$	22	$6.07 \cdot 10^{-14}$
Au	$1.92 \cdot 10^{-5}$	$5.0 \cdot 10^{-4}$	0.4	$2 \cdot 10^{-6}$	$4.0 \cdot 10^{-10}$	22	$1.69 \cdot 10^{-13}$
Ti *	$4.32 \cdot 10^{-6}$	$5.0 \cdot 10^{-4}$	0.4	$5 \cdot 10^{-7}$	$1.0 \cdot 10^{-10}$	22	$9.50 \cdot 10^{-15}$
$Si_{support}$	$8.78 \cdot 10^{-8}$	$3.0 \cdot 10^{-3}$	0.1	$5.0 \cdot 10^{-4}$	$1.5 \cdot 10^{-7}$	4	$5.27 \cdot 10^{-14}$
$Si_{mesh\ leg}$	$8.78 \cdot 10^{-8}$	$3.0 \cdot 10^{-3}$	0.4	$5.0 \cdot 10^{-4}$	$6.0 \cdot 10^{-7}$	22	$1.16 \cdot 10^{-12}$
SiO_2 *	$7.28 \cdot 10^{-7}$	$3.0 \cdot 10^{-3}$	0.4	$3.0 \cdot 10^{-5}$	$3.6 \cdot 10^{-8}$	22	$5.77 \cdot 10^{-13}$

Table 1.3: Estimated heat capacities of bolometer components at 270 mK with the listed dimensions. The first three materials form the thermistor element. Materials marked with * are not used in the final bolometer design.

Several constraints were considered in the initial mesh structure design. The overall size of the mesh needs to be at least the area of the optical output of the Winston cones (9.6 mm^2) and have a suitable grid spacing to absorb millimeter wavelengths. The mesh was chosen to be a square with 16 mm^2 and a grid spacing of 385 μm. The widths of the mesh legs were kept at 30 μm, to remain consistent with the width of the support legs. The thickness of the mesh should be the same as that of the support legs. These dimensions are not at all engraved in stone and, as will be seen in later chapters, the structural dimensions were varied, but kept within the noise parameters, as different micromachining processes were performed. The dimensions of the Au absorbing layer are addressed in Chapter 4 as is the question of whether or not to include an insulating SiO_2 layer and a Ti adhesion layer.

Chapter 2

Silicon Micromachining Basics

Micromachining techniques provide a reproducible process for fabricating three dimensional microstructures from single crystal silicon wafers (SCS). Here the basic processes involve photolithography, anisotropic etching and metallisation.

Note that all process parameters and recipes used in this thesis are included in more detail in Appendix A.

2.1 Photolithography

Photolithography uses photoemulsion techniques to create three dimensional structures from a substrate. A masking layer of light sensitive photoresist is exposed with UV light to a particular pattern from which structures can be defined. These structures are commonly formed by subtractive or additive pattern transfers as illustrated by Figure 2.1. In the subtractive method, the film to be patterned is first grown or deposited onto the SCS. Then, the pattern is etched into the film using photolithograpy. The additive process involves the same lithographic steps, but in the reverse order; that is, the masking resist layer is first patterned on the SCS followed by the film deposition. Afterwards, the photoresist layer is stripped, lifting off the undesired film deposits and leaving the desired pattern behind. The two processes could be used to reach identical final states, but more often, they lead to two different final states as in Figure 2.1. Generally, the subtractive method is used more often in SCS processing, but in both cases, photolithography defines the shape and the precision of the final structure.

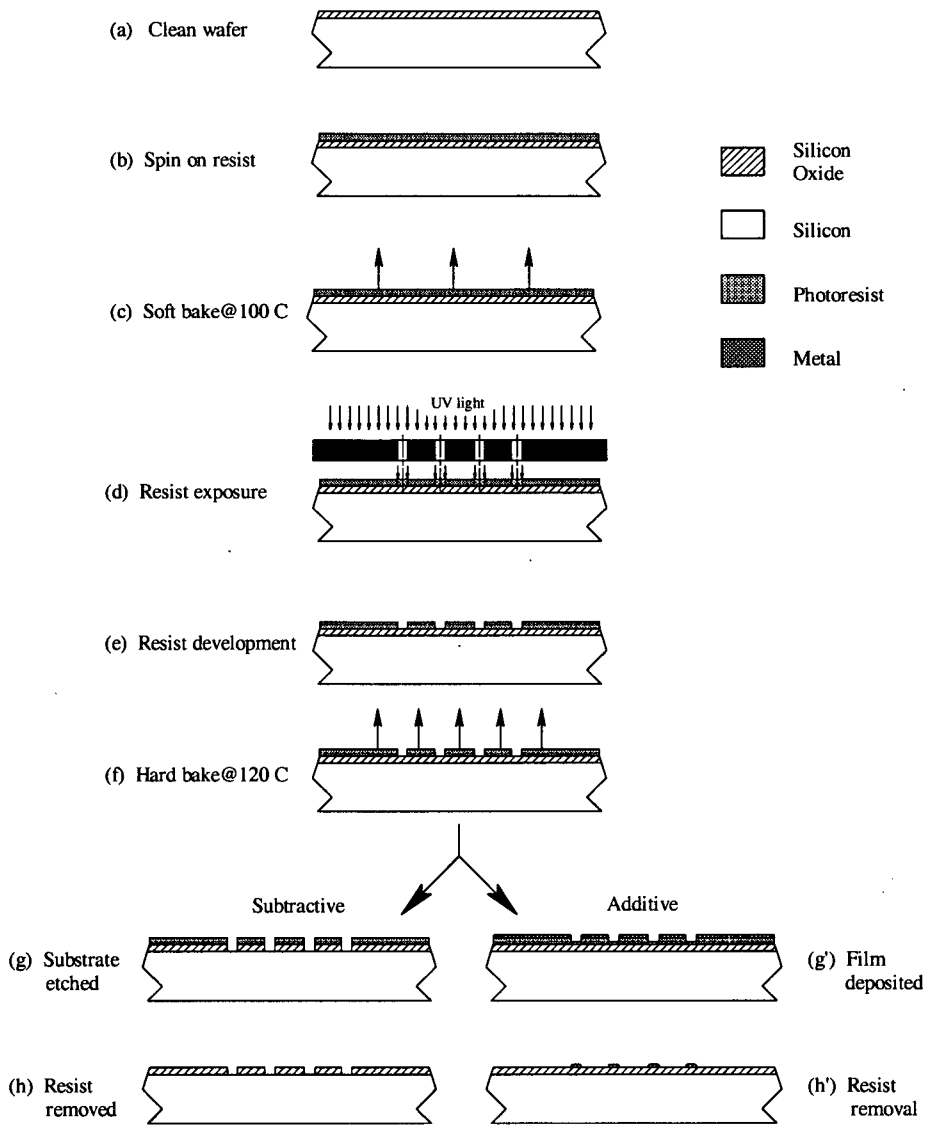

Figure 2.1: Basic steps to additive or subtractive photolithography. (a)Grow or deposit the film to be patterned. (b)Apply photoresist. (c)Soft bake. (d)The mask is aligned and exposed. (e)The exposed resist is removed. (f)Hard bake. (g)The exposed film is etched or (g′) another layer is deposited. (h)Photoresist removal.

Figure 2.1 shows the cross-section of a wafer during the basic eight steps of photolithography when used as either part of a subtractive or additive pattern transfer process. Step (a) shows a SCS wafer with a thermally grown layer of SiO_2 that is ready to be patterned. First, a thin layer of photoresist, a few microns thick, is spun unto the wafer as in (b). The resulting resist thickness depends on the type of resist, time and rotational speed. After the wafer is lightly baked at 100°C (c) to promote resist adhesion and to remove solvents in the resist, a mask (analogous to a negative in photography) is precisely aligned to the wafer. The wafer is then exposed to ultraviolet light through the mask as in (d). The resist which is exposed to the UV light is polymerised and then removed in the developer (e), while the unexposed portions remain. Then in (f), the wafer is baked again, this time at 120°C to harden the remaining resist. The exposed areas are then inspected under the microscope. If there are resist residues on the oxide or other resist defects, then the photoresist is stripped in acetone, and steps (a) through (f) are repeated. Once it is determined that the pattern is correctly masked into the resist layer, step (g) is performed. (g) shows the result of a subtractive process where the wafer is placed into a wet or dry etch process so that the exposed areas of the oxide are etched. On the other hand, an additive process, such as metallisation, is shown in (g′) where a metal has been deposited over the entire surface. The remainder of the photoresist is then removed in acetone leaving the desired pattern etched *into* the oxide (h) or patterned *onto* it with another material (h′). Depending on the purpose of the etched layer the patterned film could be the final structure desired, or it could act as a mask for additional processes such as doping or etching of the silicon substrate.

During the photolithography process the mask and wafer must remain dust free. If either have defects such as dirt or cracks, then the photoresist exposure will be compromised. Unwanted pinholes in the photoresist layer will be transferred to other layers in subsequent processes. As a preventive measure, all procedures are performed in a Class

100 cleanroom, on wafers and samples that have been cleaned first with acetone, then deionized water and finally, methanol. Before certain processes such as oxidation and doping, wafers must been cleansed thoroughly with an RCA clean. The RCA cleaning procedure removes trace metals, organics and surface oxides from the wafer, as described in Appendix A.

2.1.1 A Note on Mask Making

Each layer of patterning requires a mask (analogous to a negative in photography) that will expose the photoresist to UV light in the regions to be removed. These high resolution masks, drawn with the computer design tool *XKic*, define the device onto the wafer. *XKic* allows all the different masks, or layers, of the design to be drawn on the same layout and can distinguish between each layer so that if desired, any number of layers can be shown. From the *XKic* designs, either a *.CIF* file or individual postscript files of each layer are created. *.CIF* files can be professionally transfered to 5″ chrome emulsion masks, while postscript files are printed onto linotronic films which are usually used in printing companies as proofs. The linotronic films are then used as a negative to transfer the pattern onto 5″ *Kodak* photographic emulsion plates.

Two important aspects arise when making masks. First, the final mask image can be either a positive or a negative of the design. Secondly, one must note which way the emulsion is facing so that the proper image, not a mirrored one, is patterned on the wafer at the end. The image should be such that the emulsion is face down on the wafer when exposing the photoresist.

Theoretically, the highest resolution of the linotronic film output is 5080 dpi or 5 μm resolution. Unfortunately, 10 μm lines on the linotronic films are actually bloated as in Figure 2.2. As a result, darkened areas of the mask are generally bloated by $\sim$10 μm on each side. Thus if greater resolution is desired, laser or E-Beam written chrome masks

are used. The choice to use emulsion masks at all is because they are at least 30 times cheaper in cost to purchase.

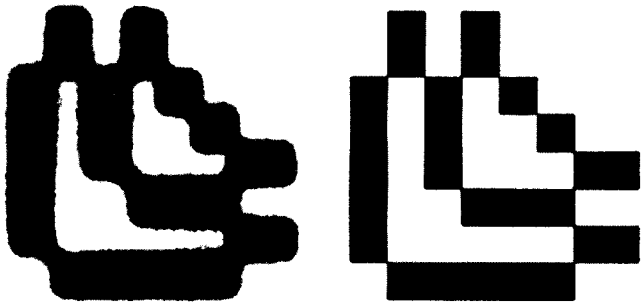

Figure 2.2: Dark lines appear bloated on the printed masks as can be seen from the resolution marks. The left resolution mark ($\sim$50 μm wide) is a scanned image of the printed mask, while the right is a scaled image of the original mark (30 μm wide) from the postscript file of the computer design. Note that the edges of the marks are actually sharp and the fuzziness in the right hand pattern is a result of the bitmap graphics on this page.

2.2 Wet Si Etchants

Once the photolithographic steps are completed, the silicon wafer is ready for further processing. For example, the wafer can be etched to create 3D structures. Silicon may be etched either isotropically or anisotropically with various wet etchants. The degree of etch selectivity for an etchant to etch silicon over other materials, determines the appropriate masking material. Figure 2.3 shows various hole geometries common to silicon etches. Isotropic etches, in c), produce holes which drastically undercut the masking material since the etch proceeds in all directions. On the other hand, anisotropic etches proceed along silicon's crystalline planes, for example, etching $<100>$ and $<110>$ planes much faster then the $<111>$ plane. In this case, as shown in a), $<100>$ wafers will have etched grooves with sloped walls bounded by the $<111>$ plane, inclined at 54.75°, with a minimal amount of mask undercutting.

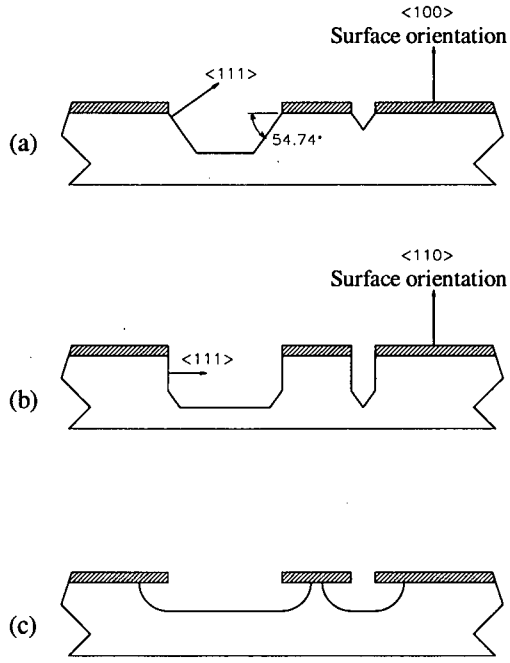

Figure 2.3: Etched hole geometries commonly used in micromechanical devices. The shaded regions indicate the masking material. a) Anisotropic etching on $<100>$ surfaces. b) Anisotropic etching on $<110>$ surfaces. c) Isotropic etching.

A common anisotropic etchant is Ethylene diamine pyrocatecol (EDP) diluted with water. This etchant is highly selective and attacks silicon but not SiO_2, Al, Au or heavily boron doped Si. Thus any of these materials may be used either as a masking layer or an etch stop layer. When comparing selectivities, SiO_2 is the safer choice as a masking layer during long duration etches in EDP.

Previous tests [18] on SCS have shown that the EDP etch rate of the $<100>$ plane varies from 61 μm/hr to 100 μm/hr over the surface of the wafer during a long (>6 hours) etch. The etch rate depends heavily on fluid flow, temperature and etchant freshness. The fluid flow over a wafer in the EDP reactor varies from top to bottom, and left to right, hence etch rates across the wafer also vary. This is problem when one is timing the etch in order to reach a specific etch depth. Preferably, an etch stop layer is used so that it is unnecessary to monitor the progress of the etch. If the wafer is constantly pulled from the EDP reactor in order to check the etch depth, the repeated temperature change between the EDP and the deionized water rinse tends to crystallize a white Si based substance onto the etched areas. It is thought that the dissociated pyrocatecol molecules form bonds with excess Si atoms and subsequently crystallize into the white compound at room temperature [19]. Although these white deposits are removable with buffered HF, their presence interferes with subsequent etches and leaves the underside of the Si membrane roughened and uneven. Therefore when using EDP the micromachine 3D structures, it is important to employ some sort of etch stop layer such as heavily boron doped Si or SiO_2.

Another anisotropic silicon wet etchant is tetramethylammonium hydroxide (TMAH), which has a slower etch rate (see Table 2.1) when compared to EDP. However, TMAH does etch heavily doped Si so that doped areas can also be micromachined. A detailed review of these and other anisotropic and isotropic etchants may be found in [20].

Silicon Etchant Temperature (°C)	TMAH 80	TMAH 90	EDP 95
Etch rate of < 100 > Si (μm/hr)	40	65	60–100
Selectivity ratios			
Si: SiO_2	1190:1	800:1	>2000:1
Si: B doped Si (10^{20} atoms/cc)	27:1	20:1	>500:1
Si: B doped Si (10^{21} atoms/cc)	100:1	92:1	>500:1

Table 2.1: Estimated etch rates and selectivity ratios for TMAH and EDP[21].

2.3 Plasma Etching

Dry or plasma etching is a common alternative to etch silicon selectively over other materials. In plasma etching, corrosive liquids are replaced with plasmas that can etch via three processes: sputtering, chemical reaction and ion-enhanced etching. In sputtering, substrate atoms are forcibly ejected from the surface by the impinging ions, while chemical reactions rely on the reactivity of the surface atoms to those in the plasma. Both these processes are relatively slow when performed separately, but increased etch rates are observed when performed together [22]. This latter is the condition for ion-enhanced etching. The most widely accepted model for this phenomenon is that the slow chemical reactions at the surface provide a larger sputtering yield to impacting ions. The energy provided by the impacting ions subsequently goes into the reaction layer and increases the formation of volatile products which desorb from the surface.

Anisotropic etching of silicon is possible with Cl plasmas. Although the etch rate is faster, the more common fluorine based chemistries are typically isotropic, unless cryogenically cooled or side-wall passivation polymers are introduced into the system [23]. Successful anisotropic etching of Si with Cl has been performed by Juan and Pang [23, 24]. The typical dry etching recipe requires high microwave and RF power coupled with high chamber pressure and a reasonable high flow of pure Cl gas.

In this work, all attempts to plasma etch silicon were with a *PlasmaQuest* electron cyclotron resonance (ECR) source coupled with an RF field through chlorine gas. The ECR source couples a 2.45 GHz microwave power source with electrons accelerated by a magnetic field to large velocities. The Lorentz force causes the electrons to circulate around the magnetic field lines with the cyclotron frequency given by $w = eB/m_e$. For a magnetic field strength of 875 gauss, $w = 2.45\,\text{GHz}$. As the energy coupling becomes resonant, the electrons ionize the gases present in the chamber. In the process chamber, the wafer is RF biased to control the energy of the the impinging ions across the plasma sheath.

The etchant gases are continuously fed into the chamber through mass flow controllers while a turbo pump regulates the chamber pressure. The wafer is cooled to process temperatures with a back flow of He and water cooling lines. These process parameters as well as the microwave and RF power are controlled via computer.

2.4 Metallization

Thin metal films can be grown onto a substrate with a variety of methods. Common procedures include thermal evaporation and electron beam (E-Beam) evaporation. The former process involves heating and melting the metal on a resistance heater so that the evaporated atoms collect on the surface of the substrate. The metal source is usually placed into a tungsten boat or wrapped around a tungsten wire filament. A current is passed through the boat or wire, heating it and the source until the source begins to evaporate. The rate at which the metal condenses on the substrate depends on the amount of current passing through the boat and on the height above the boat at which the substrate is placed.

E-beam evaporations involve a similar process except the source is heated via a beam

of electrons. Here, the current is passed through an isolated filament and the ejected electrons are directed, with magnetic fields, towards the metal contained in a crucible. This deposition method is useful for materials with higher boiling points, like platinum (3800 °C) and titanium (3260 °C) that cannot be evaporated in tungsten resistance heaters, but require crucible s. Again, the rate of deposition depends on the location of the substrate, the current flowing through the tungsten wire, and the resulting energy in the E-beam.

The deposition takes place within an evacuated bell jar, typically at pressures $<$ 3 μtorr. The substrate is cleaned inside the chamber during evacuation with a plasma discharge. A high voltage rod in the chamber discharges electrically, ionizing all the gases in the chamber. The walls and substrate are bombarded by the highly ionized air and all excess materials are ejected off their surfaces. Usually, the evacuated chamber is backfilled with Argon gas and subsequently ionized. Because Ar is a noble gas and the atoms are heavier, the plasma scrubs the substrate more efficiently and leaves a cleaner surface. If only air is present during the discharge in the chamber, hydrogen or oxygen atoms can still cling or bond to stray molecules (eg. hydrocarbons) on the substrate without removing them from the surface.

The easiest method to measure the deposition rate as well as the thickness of the metal film is with a crystal thickness monitor. This device measures the frequency of oscillation of a quartz crystal which is placed as close to the substrate as possible. As materials are deposited onto the crystal, the frequency of oscillation changes slightly depending on the thickness of the film. Using this device during deposition, it is possible to monitor the deposition rate (and to control the rate by adjusting the current through the boat or wire) and measure the thickness of film to within a few angstroms. Once the desired thickness is achieved, the evaporation can be stopped immediately with a manually controlled mechanical shutter that is moved in front of the substrate.

2.4.1 Metal Lift-off Process

To metallize detailed structures onto the substrate, slightly modified additive photolithography, sometimes called the metal lift-off process, is used. The changes to the lithography process (as shown in Figure 2.4) occur during the photoresist exposure and development stages, before the metal is deposited.

Prior to the soft bake and exposure to UV light, the wafer can be soaked in a hardening solution so that the upper portion of the photoresist layer becomes more resistive to the developer as indicated by the heavier crosshatch in (b). Once baked and exposed (c), the polymerised regions are removed in the developer (d). Letting the wafer soak in the developer (e) for an extra 2-3 minutes overdevelops the lower unhardened portions of the resist, leaving the upper portions to form a small overhang. The opening remains the same thickness as what was on the mask, but the overdevelopment ensures that the final metallized pattern (f) is not in physical contact with the resist layer. This allows an easy removal of the resist (g) in acetone. Note that in Figure 2.4, the photoresist layer has been drawn thicker for clarity and is not drawn to scale. In fact, we do not always overdevelop the resist so that we can strip out the SiO_2 layer and deposit the metal directly onto the Si.

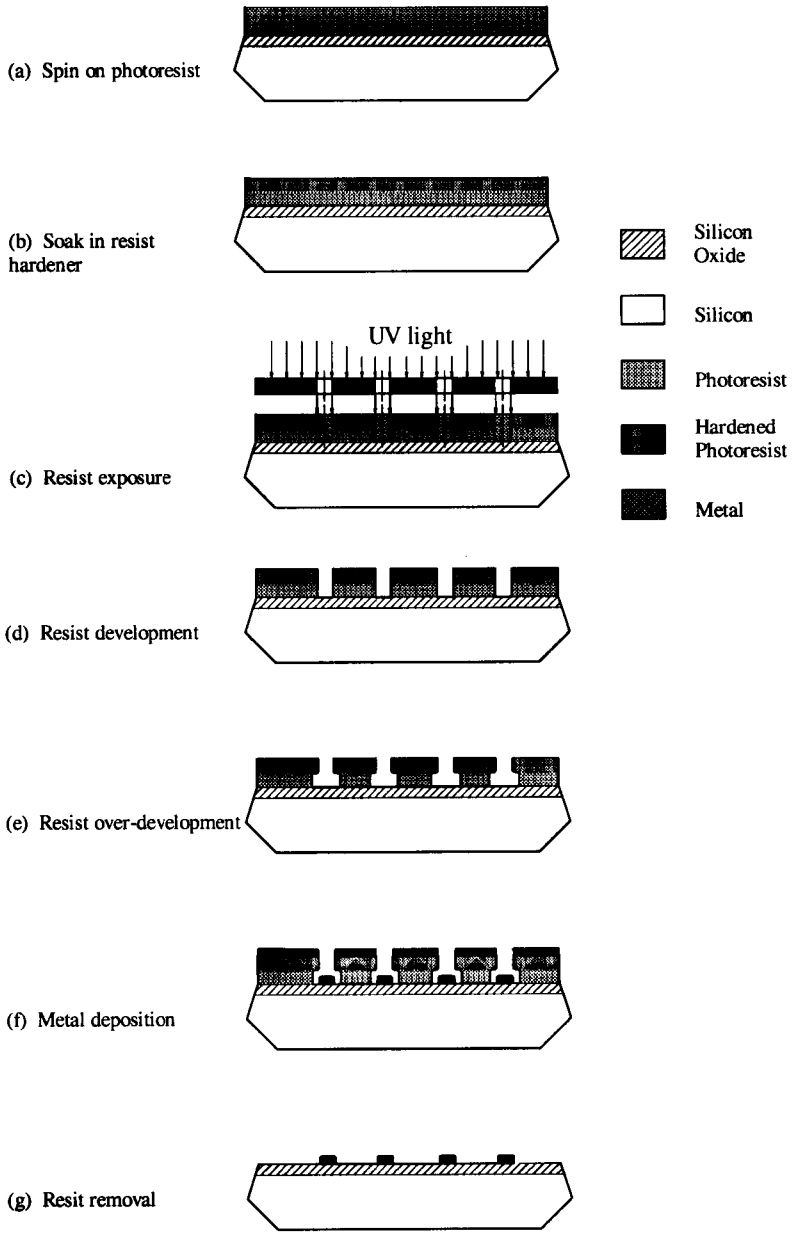

Figure 2.4: Modified additive photolithography for a metal lift-off process. See text for details. (Not drawn to scale)

Chapter 3

Fabricating the Mesh Structure

The main goal of this work is to produce bolometers that would be less susceptible to cosmic ray hits, but remain as sensitive to microwaves as the BAM sapphire chip bolometers. Consequently, a large part of this work involves investigating micromachining techniques which would lead to a thin free standing mesh held in place by a few supports with low thermal conductance. While it is possible to obtain whole Si wafers of thicknesses down to $2\,\mu$m, it is much easier and cheaper to work with regular wafers (with thicknesses $\sim 450\,\mu$m) that are less fragile. In this case, it is necessary to remove the majority of the wafer thickness over a small area to leave a thin membrane, surrounded by a thicker frame for handling. From the suspended thin membrane, the bolometer substrate can be defined into a mesh structure like that of Figure 1.8.

This chapter details various attempts, via wet etching, to construct suspended membranes ranging in thickness from $2\,\mu$m to $\sim 100\,\mu$m. The subsequent steps to micromachine the mesh structures via wet etching and plasma etching are also examined for meshes of various dimensions. The suppliers from whom the wafers were purchased are listed in Appendix B.

3.1 Using Etch Stop Layers to Form Thin Membranes and Meshes

It is easiest to thin the wafer in small areas with an anisotropic wet etch. Square openings made into one side of a $<100>$ wafer will etch into the wafer leaving straight but sloped side walls and will only stop at the etch-stop layer if one is present as a part of the wafer.

The result is a thin square membrane with a frame which is as thick as the original wafer.

One possible method to stop the wet etch is to have the membrane layer be of material that will not be etched. This can be achieved by depositing the bolometer substrate material directly onto the Si wafer as Mauskopf et. al. do by depositing a uniform layer of Si_3N_4 to a specific thickness [15]. Due to a lack of facilities, this was not an option for us. One could however, heavily dope the wafer with boron atoms prior to back-etching. Since heavily doped Si is not etched by EDP, but can be etched with TMAH, the membranes can be defined with an EDP etch, and the square grid structures with the TMAH.

A different approach to the problem involves processing a triple-layered wafer rather than a simple double-side polished wafer. Commercially available triple-layered wafers have an additional layer of oxide between the bulk (handle) wafer and the membrane (device) layer. Thus, the thin membrane is already present and the bulk wafer may be removed in EDP with the intermediate oxide layer acting as the etch-stop layer which can be removed at a later step.

While these processes seems fairly straight-forward, the question of how to regulate the thickness of the membrane remains unresolved. Boron doping generally penetrates the wafer to a depth of 5 μm, but the concentration of the doping drops off with the depth, so the thickness is variable. The second method involving a buried intermediate layer is more promising as the device layer thickness can be specified to the wafer manufacturer. The following sections describe the experiments performed to evaluate both methods.

3.1.1 Heavily Boron Doped Si

Silicon wafers can be doped by baking them in a furnace at high temperatures next to an activated boron source. The source ejects boron atoms which lodge themselves into the silicon crystal structure. A subsequent oxidation step drives the boron atoms into

the wafer and also forms protective oxide layers for the later EDP and TMAH etches.

Initially, 3 single side polished (SS) wafers and 3 double side polished (DS) wafers were cleaned in a series of hot baths containing hydrogen peroxide with ammonium hydroxide, buffered hydrofluoric acid, and finally hydrogen peroxide with hydrochloric acid. This cleaning procedure removes organic materials, native oxides and metals from the surfaces of the wafers and should be performed immediately prior to placing the wafers in the furnace for doping and oxidation.

Once cleaned, the wafers were loaded into a furnace boat, containing boron sources. Two wafers were placed on either side of each source with the the polished surfaces facing the source. Dummy scrap wafers were placed in the unused boat slots next to the extra boron sources. The boat was slowly pushed into the furnace after which the furnace was ramped to an operating temperature of 975 °C. The boron diffusion was stopped 40 minutes after the temperature stabilized. The furnace temperature was then ramped down to 750°C and the boat slowly pulled out. The target doping concentration was 10^{19} atoms/cc, but the actual average concentration for the six wafers was determined from 4-probe resistance measurements to be $\sim 10^{18}$ atoms/cc. This was thought to be an acceptable doping level to act as an etch stop layer so the wafers were removed from the boron furnace boat and placed into the oxidation boat. The boat was then slowly pushed into the furnace and oxidized in a wet oxygen environment. A 0.3 μm layer was grown onto the wafers.

Each wafer was then processed individually with various micromachining steps in order to find a repeatable process that would lead to the desired free standing grid structure (with a grid spacing of 385 μm and 35 μm wide lines) held to the support frame by 4 legs, 1 mm long, running diagonally from the outside corners of the mesh to the frame.

For the first SS wafer, large open areas were patterned and etched into the unpolished

side for 6.75 hours in EDP. It was believed that the etch would proceed through the wafer, forming sloped sidewalls until it encountered the heavily boron doped Si where the EDP would cease etching. When the wafer was pulled from the solution, it was observed that for the majority of the open areas, there was a thin membrane of uneven thickness that transmitted reddish wavelengths. However in some locations, the membranes had either been etched through or had many tiny pinholes. This was attributed to uneven doping levels across the wafer. Next, the polished side of the wafer was patterned to create the mesh structure. Since EDP does not etch the doped membrane, the wafer was placed in a hot bath of TMAH instead. Due to lack of foresight, the TMAH proceeded to etch the membrane from both sides and as a result, the membranes were eaten through before the mesh was well defined.

The second SS wafer was patterned to open up the back windows but for unknown reasons, the doped layer was insufficient as an etch stop layer and the etch ate through the entire wafer after 6.5 hours. It was suspected that the boron source was the culprit because the DS wafer on the other side of the same source also exhibited strange reactions to conventional etches. With this DS wafer, the oxide on the doped side of the wafer would not etch in HF (possibly some kind of borosilicate glass was formed) so the mesh pattern could not be defined into the membrane. This was not investigated further and we proceeded with the second DS wafer.

It was thought that the middle oxidation step could be skipped if the mesh was first patterned, and then the backside opened up and etched. In this manner, the EDP would only attack the open areas from the back, and would not laterally etch the mesh legs. The boron doped side of the second DS wafer was successfully patterned and etched in TMAH however the back side was not etched in EDP. It was unclear how it would be known when the meshes were released from the back silicon because the etch could not be monitored. Also, because the support legs of the mesh were diagonal, they would be

etched away by the EDP. So this step-saving idea was abandoned and we returned to the original plan. The last DS wafer was opened up in the back and etched for 6.75 hours. Some membranes were etched through, but the majority were intact and transmitted red light evenly. The wafer was cleaned, reoxidized and the doped side patterned for the mesh. After 42 minutes in the TMAH, a few grids were defined and held in place by the support legs and the back oxide. The wafer was pulled from the bath and the oxides removed with a 10 minute dip in HF.

Of the 54 devices patterned into it, only 2 membranes led to free standing meshes. The rest of the devices were either under etched or over etched. Figure 3.1 is a scanned photo of one of the meshes. Clearly, these were not entirely etched to completion and there is still residual Si to be removed from the backside of the mesh. However, the result seemed promising. One reason that more than half the grids were lost was due to the fact that the 4 mesh support legs were patterned to be diagonal instead of square and so were being laterally etched by the TMAH. This could be remedied by remaking masks with a grid design like that of Figure 1.8.

A new mask was made and printed on linotronic film. The mesh consisted of 35 μm wide lines with a 385 μm grid spacing and four, 1 mm long, square support legs arranged as in Figure 1.8. The unpolished side of the wafer was patterned and etched in EDP, for 6.75 hours, to open up large square windows as before. However, in this instance, the membranes seemed rather thick and did not transmit red light. The second oxidation step used before to protect the back side of the membrane was skipped so that the membrane could be thinned out as the mesh was defined.

Once the polished side had been patterned for the mesh structure, the wafer was placed in TMAH for a total of 3.25 hours. Because the TMAH etchant is clear, the progress of the etch could be monitored without pulling the wafer from the bath. After the first 2.5 hours, the etch seemed to be progressing unevenly across the entire wafer and

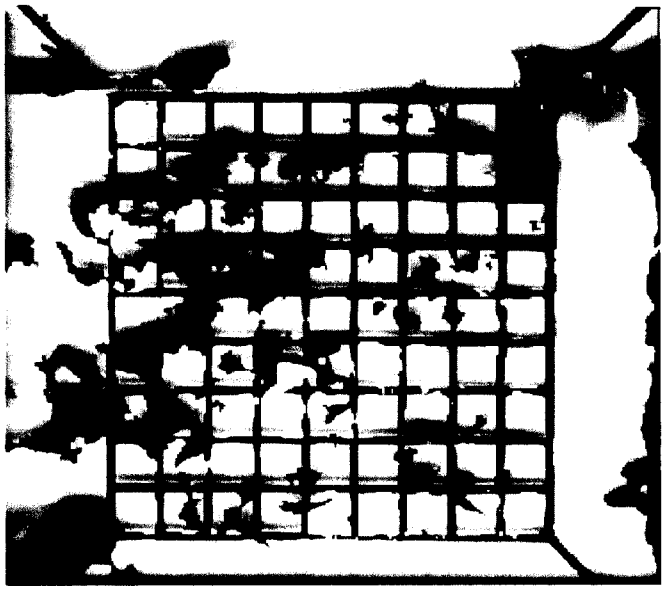

Figure 3.1: First free-standing Si mesh made by back etching a wafer to a heavily boron doped Si etch stop layer. The mesh defining etch was not quite complete as there is still some leftover Si on the backside of the grid area. The outside Si frame is not shown.

even across individual membranes. Approximately 1/3 of the devices located randomly across the wafer, had already etched completely through from the back side, while the remaining membranes were wholly intact, that is, the mesh structures could be seen etched into the membrane, but the backside was not yet cleared out. When the etch was stopped, there were 2 fully intact and free-standing meshes, while 12 other devices required a longer etching period. The wafer was diced and the other chips were etched individually in the TMAH, until their grids were fully released from the back silicon.

Pictures were taken of some of these free standing meshes. While the etched membrane appears cleaner than those in Figure 3.2, the uneven etch from one side of the membrane to the other cannot be ignored. The wider legs in the lower left hand side are a result of an uneven membrane thickness. The mask that defined the lines were all 35 μm wide, but since the etch progresses at a sloped angle, the backside of the legs are much wider. Thus the difference in width is an indication of a difference in the membrane

thickness from the lower left hand side to the upper right hand side of the mesh. When examined with a profilometer, the thickness of the membranes were close to 90 μm at the thickest regions. Clearly this is not a repeatable nor controllable process. The thickness of the membrane cannot be predetermined and the quality of the resulting grids are variable. This method of mesh fabrication is not at all useful for building bolometers with controlled dimensions and so it was abandoned.

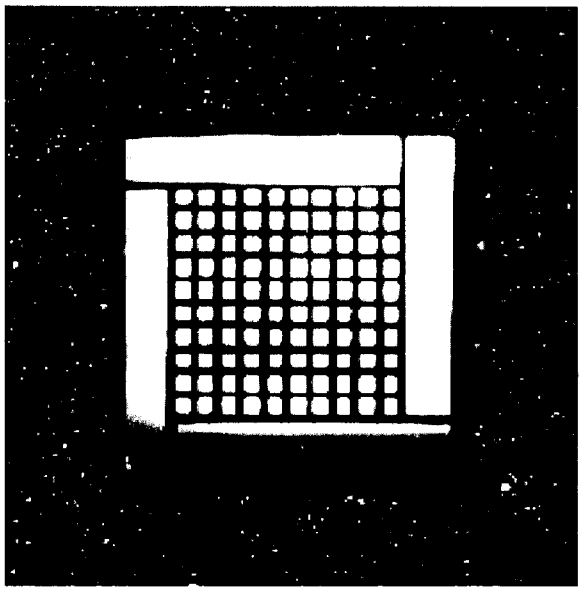

Figure 3.2: A mesh and it surrounding Si frame from the second successful attempt to make free standing meshes from a doped Si membrane. The uneven etching is apparent from the wider legs in the lower left hand corner as compared to the upper right hand corner. The membrane was measured to be as thick as ~90 μm.

3.1.2 Buried Oxide Layer

Because of the demands of the silicon integrated circuits technology, newer wafers are now available which have insulator layers sandwiched between two single crystal silicon layers. Such wafers consist of a regular handle wafer 450-500 μm thick, bonded to an insulating material such as silicon nitride or silicon dioxide. A second Si wafer is bonded to the

insulator and polished down to the desired device layer thickness. These wafers can be purchased with a variety of specifications including handle and device layer thicknesses, crystal orientations and resistivities, as well as the type of insulator material and its thickness.

We were able to acquire three types of these triple layer wafers that had buried oxide (BOX) layers. Their specifications are given in Table 3.1. Because we were ordering in small quantities, we purchased $< 100 >$ wafers that had appropriate device layer thicknesses and that were readily available from stock inventory.

Device Layer		Handle Wafer		BOX
thickness (μm)	ρ (Ω cm)	thickness (μm)	ρ (Ω cm)	thickness (μm)
2.25	10–20	381	10–20	0.2
6.5	20–30	375	10–20	0.2
5.0	150–250	525	2–30	1.0

Table 3.1: Relevant specifications for the three BOX wafers used in this work.

Initially, only the BOX wafers with 6.5 μm thick device layers were cleaned and oxidized. Then, while protecting the topside of the wafer, square openings were etched into the backside for 7 hours in EDP. Because of the buried oxide layer, there was no worry of over etching. Once the etch was complete, the BOX layer was protected with photoresist while the front side was patterned and etched into a mesh. The mask used was identical to that used in the previous runs with the boron doped wafers. The grid was made up of lines 35 μm by 375 μm, supported by 4 legs 35 μm wide and 1 mm long. After ten minutes in EDP, the etch was complete and the wafer was pulled from the etchant and rinsed with DI water. Immediately after the rinse, the wafer was placed into HF to remove all the oxides to free the mesh. After 10 minutes in HF, the wafer was dipped vertically into beakers of DI water as a rinse. Finally, the wafer was heat dried in an open oven since

the N_2 air gun would likely blow the meshes out. Water spots were minimal, but these could be avoided in later runs with an isopropanol rinse and letting the wafer air dry. With this process, 15 free standing Si meshes were successfully fabricated from a single wafer that had been patterned for 42 individual devices.

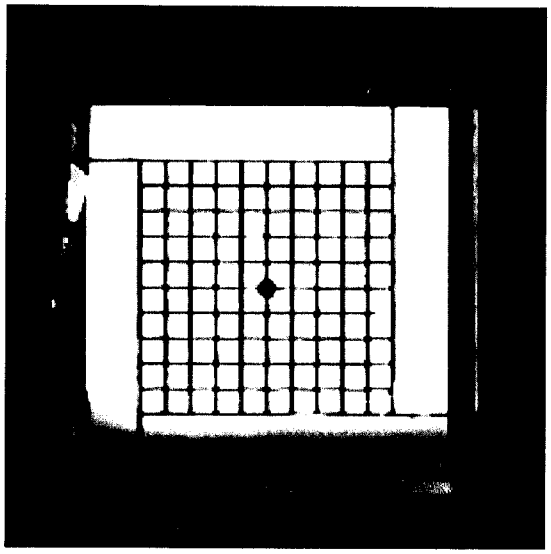

Figure 3.3: Free standing mesh made from a BOX wafer with a device layer 6.5 μm thick.

The low yield was mostly due to two problems. First, the surface tension on the BOX layer as the wafer was removed from the DI water rinse popped many meshes free. The thin oxide membrane is quite stressed when it is stretched out over large open areas and cracks and buckles in many places. The surface tension of the DI water rinse increases the stresses and occasionally breaks one of the corner support legs so that the oxide can curl and relieve the stresses. There was no obvious solution to this problem except to keep the wafer vertical when removing it from liquids and to remove the oxide layer as quickly as possible. The second problem occurred while the wafer was being diced. Merely scribing the wafer with a diamond tip did not provide an adequate fault line to break the wafer along the desired paths. Instead, the wafer tended to crack at the boundaries of the

etched windows where the wafer had been entirely etched through. This problem can be easily solved by patterning and etching dicing grooves into the backside during the etch to open up the back windows.

As a test of the robustness of the meshes, a 0.001″ brass wire was glued with epoxy to the central pad region meant for the NTD Ge thermistor. A light tap of the wire into a tiny ball of *Miller-Stevenson 907* epoxy was all that was required to attach the wire. Once the wire was glued down, it was possible to pick up the entire chip, mesh and frame, by the wire. Presumably, attaching a NTD Ge thermistor would be equally as easy.

Next we moved to the BOX wafers with 2.25 μm membranes since thinner support legs would provide lower thermal conductance to the heat sink and reduce the thermal noise. Unfortunately the previously described surface tension problems increased once the membrane was etched. We then investigated the possibility of using the 6.5 μm membranes and designing the mesh to have 8 support legs with reduced widths of 5 μm. This also did not have the structural support necessary to withstand the surface tension of liquids prior to oxide removal. This whole problem can be avoided by using plasma etching to micromachine the mesh structure. This possibility is examined in the next section.

3.2 Forming Mesh Structures via Plasma Etching

In order for plasma etching to be an improvement over wet etching, both the Si etch as well as the masking material removal must be performed in dry environments. Once the mesh is etched the membrane cannot ever be immersed in any liquids. Prior to the Si etch though, when the full membrane is still intact, the chip can still be immersed so that patterning of the membrane is possible.

Valid masking materials for a Cl based plasma etch include SiO_2, metals and photoresist. While the removal of most metals requires soaking the sample in some solvent, photoresist can be ashed away with an oxygen plasma. Clearly, this was the simplest choice to mask with, given the current UBC cleanroom facilities. Cl based plasma etching could take place in the *PlasmaQuest* ECR etcher while the resist could be ashed off using the *Technics Plasma Etch II* etcher.

3.2.1 Etching Mesh Structures

Several attempts to plasma etch mesh structures from a 2.25 μm membrane showed some promising results. Unfortunately, there was not enough time to pursue this further. A brief description of the attempts to etch Si with a Cl_2 plasma is described here.

The handle portion of a BOX wafer with a 2.25 μm device layer, was patterned and etched to open up the back windows. Before the etch reached the etch stop layer, the wafer was removed and diced so that the chips could be etched individually. Once the etch reached the BOX layer for all the chips, all the oxides were immediately stripped in an HF bath to reduce the stress on the Si membranes. Then, photoresist was spun onto the topside of 5 free standing membranes and which were subsequently patterned with a mesh structure with 8 support legs, 5 μm wide.

One chip was then placed into the *PlasmaQuest* ECR etcher. Following the recipe in Juan and Pang's article, the chip was etched with the following process parameters for 10 minutes:

Microwave power:	1000 W
RF power:	100 W
DC bias:	72 V
Pressure:	15.3 mTorr

Cl_2 flow rate: 8.7 sccm

BCl_3 flow rate: 2.1 sccm

The result is shown in Figure 3.4. The etch appeared to have proceeded from the center of the membrane outwards and the mesh was not fully released. Only the central portion of the membrane had been fully etched through so that the mesh was supported by a frame formed by the remaining outer portions of the membrane. The masked area of the sample was entirely blackened. The blackened portions could not be removed in solvents, but could be easily scratched off with tweezers. It was unclear whether the black material was burnt photoresist, or the "black grass" of etched Si pillars [22]. It is possible that the photoresist layer was sputtered off during the etch and the underlying Si was being etched in those areas. The support wafer on which the sample had been placed in the chamber had turned cloudy gray and it was assumed that some sort of oxide had been deposited onto the wafer. This deposit could be wiped off with a little DI water and alcohol. The area of the support wafer that was under the sample remained shiny and clean.

An exact repeat of the above process on a second sample had slightly different results. The membrane was not etched through in the center although it appeared from the coloured fringes that the etch was progressing from the center outwards. The masked areas were a cloudy gray colour while the support wafer was now blackened.

A third membrane was etched for twice the length of time, under the same conditions. When removed from the chamber, the mesh was nearly fully defined in all areas. However, when the mesh was placed into a *Flouroware* chip holder, the mesh was pulled out of the frame due to static between the Si and the plastic holder. Clearly the thinner support legs were quite fragile and it would be quite difficult to attach a thermistor to the mesh.

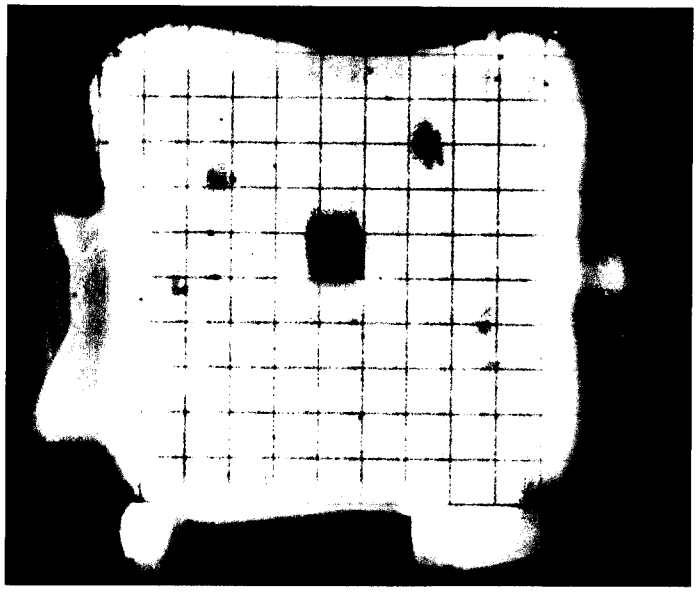

Figure 3.4: Free standing mesh plasma etched from a BOX wafer with a device layer 2.2 μm thick and legs 5 μm wide.

Although the first and third result seemed promising, the unknown properties of the black material and the unpredictable appearances of the cloudy gray deposits remain problematic. However, plasma etching remains an attractive option if these problems could be resolved, either by turning to fluorine based plasmas or by finding an alternate masking layer. It was decided that wide-legged meshes were acceptable and would not compromise our noise budgets. So, the meshes would be fabricated from the thicker 5.0 μm membranes, using wet etching as in Section 3.1.2.

Chapter 4

Resistivity Measurements of Thin Gold Films

As described in Chapter 1, the absorbing layer of the bolometer should have a resistance of 188.5 Ω per leg at the operating temperature of 270 mK. Any metal film deposited to this sheet resistance will work as an absorbing film. However, it is also desirable to select a metal that has a low heat capacity as compared to the other bolometer components. At 270 mK, recalling Table 1.1, both gold and bismuth are good candidates as absorbers. While bismuth begins to exhibit excess heat capacity at slightly lower temperatures due to nuclear quadrapole moments, and has a tendency to oxidize when exposed to air and humidity, the resistivity of gold is much lower than that of the semi-metal and so requires a thinner film. If the gold film is too thin (<100 Å), it may be discontinuous since the gold atoms tend to clump together to form island structures as the film is grown.

The basic theory on the resistivity of thin metal films, and how the appropriate film thickness for our bolometers can be determined is outlined in this chapter.

4.1 The Resistivity of Thin Metal Films

The electrical resistivity of bulk materials arises due to electron-phonon collisions and electrons scattering off of lattice impurities and dislocations. Because phonons are thermal excitations in the crystal lattice, the phonon scattering component of the resistivity. ρ_p is temperature dependent and dominates at temperatures > 4 K. On the other hand, the resistivity due to electron-impurity and dislocations scattering, ρ_i is temperature independent and can be considered a rough measurement of the material's purity. Because

these two components are independent of each other, the total resistivity ρ can be written as their sum.

$$\rho = \rho_p + \rho_i \tag{4.1}$$

The electrical properties of thin metal films are slightly different from those of the bulk metal. Once the film thickness, t, becomes much smaller than the bulk mean free path of the electrons, other scattering effects like surface scattering and grain boundary scattering must be considered. Generally, one observes that $\rho_i \propto 1/t$ [25].

Surface scattering is due to the scattering of the electrons off of the film's surfaces. Consequently, when the bulk electron mean free path, λ_o is much larger than the film thickness, the resistivity-temperature dependence is a strong function of the film thickness. On the other hand, in the grain scattering model, electrons scatter off of grain boundaries. Grain boundaries can be thought of as parallel partially reflecting planes randomly distributed throughout the film. The average grain diameter, d, is the average distance between planes and is usually taken to be equal to the film thickness. Here, the scattering mechanism is temperature independent and only adds a constant offset to the temperature-resistivity curve. This offset is called the residual resistivity $\rho(0)$ of the film, and is an indication of defect density and sample purity. Studies on a variety of metals including aluminum and gold, by De Vries [26, 27] and van Attekum [25], have shown that the latter process is likely the dominating contribution to the residual resistivity at temperatures $< 4.2\,\mathrm{K}$.

De Vries found that the resistivity could be described by the following simplified equation, derived from grain scattering theory.

$$\rho_{film} = (1.39\alpha + 1)\rho_{bulk} \tag{4.2}$$

where $\alpha = (\lambda_o/d)(R/1-R)$. Here R is the grain boundary reflection coefficient.

Since the phonon contribution to the resistivity can be measured and found from the Bloch-Gruneisen relation $\rho_p \propto T^5/\Theta_D^6$, (for gold, $\Theta_D = 171\,\mathrm{K}$) and the quantity $\rho\lambda_o$ is considered a constant for all temperatures with the generally accepted value $9.6 \times 10^{-12}\,\Omega\,\mathrm{cm}^2$ [26], one can calculate λ_o for a given gold film and fit for a value of R.

4.2 Preparation of Thin Gold Films

Evaporating gold directly onto glass-like substrates usually produces films that are flaky and do not adhere well to the substrate. However, a thin intermediate layer ($\sim 50\,\text{Å}$) of chromium or titanium usually forms a good adhesion layer for gold. This is possibly because chrome and titanium both form thin oxide layers which stick to the insulator, while the upper metallic layer forms a good bonding surface for the gold. For our purposes, titanium is favoured over chromium because Ti has a lower magnetic contribution to the heat capacity. The magnetic contribution remains constant at low temperatures and therefore remains large, dominating the heat capacity at low T.

However, if gold is evaporated directly onto a very clean Si substrate without oxides, the gold film adheres quite well. In this case one must worry about whether the Si will "freeze out" electrically at 300 mK or remain electrically conductive. Previous measurements [18] showed that for doping concentrations under 10^{18} atoms/cc, Si does in fact freeze out below 4.2 K.

To ensure that the correct resistance was evaporated onto the membrane, various film thicknesses of gold were evaporated onto Si substrates in a known pattern and 4 wire DC resistance measurements from 4.2 K to 300 K were made. As test samples, thin lines of titanium and gold were deposited, Figure 4.1, onto spare individual Si chips (some with oxide overlayers, some without) using metal lift-off techniques and an E-beam evaporator

as described in Chapter 2 and Appendix A. The geometry of the lines were defined by a mask design such as that in Figure 4.1. The electrical connections, for 4-wire resistance measurements, were made to the outer rectangular pads by attaching electrical leads with conductive silver epoxy.

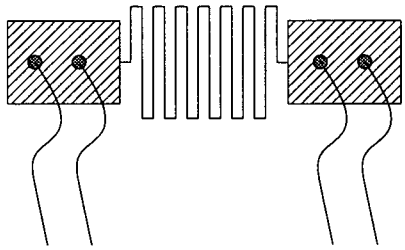

Figure 4.1: Gold meander path used for thin film resistivity tests.

Once the metals were deposited to the desired thickness and outfitted with leads, individual samples were attached to a probe and slowly lowered into a liquid ^{4}He dewar and cooled to 4.2 K. During the cooling, the resistance was measured with an *HP 34401A* multimeter while the temperature was measured with a calibrated diode. The diode, supplied with a constant current source of 50 μA, has a linear voltage-temperature relation given by

$$T = \frac{V_{Diode} - 1.1938}{-0.00245} \tag{4.3}$$

in the temperature range $40\,K \leq T \leq 300\,K$.

The samples are mounted onto the probe with *Emerson Cumming 2580FT Stycast*

which has a smaller thermal expansion coefficient than silicon. Thus only a little stycast should be used to bond the silicon to the probe, otherwise the silicon may crack once cooled.

4.2.1 Preliminary Test Runs

The first Si chips used were from two different cleaned wafers with SiO_2 overlayers 0.3 μm and 0.5 μm thick respectively. Two different substrates were used to test whether the thin film resistivity would depend on the underlying surface. Oxides grown under slightly different conditions may have differing surface roughness. The surface roughness will directly affect how the gold film forms as it is evaporated onto the surface.

Photoresist was spun onto all the samples and patterned using the metal lift-off technique. The test path, similar in geometry to Figure 4.1 was 3.115 cm long and 50 μm wide. For the titanium evaporation, all the samples were mounted on the stationary stage in the *Balzers* E-Beam evaporator. Unfortunately, the crystal monitor is mounted at the very top of the chamber, while the stationary stage holding the samples is at the midpoint. This discrepancy in height can be accomadated for by setting the tooling factor on the thickness monitor controller to $\sim$ 150 %. Once $\sim$60 Å of Ti was deposited, the samples were removed.

The gold evaporations were carried out in a thermal evaporator where the crystal monitor could be placed directly beside the samples for a more accurate thickness measurement. One sample of each type of wafer was mounted into the chamber. The bell jar was evacuated and the air was ionized by a high voltage discharge. Once the chamber pressure was at 2.9 μTorr, 50 Å of gold was evaporated onto the samples. This was repeated for the other samples so that there were gold films 150 Å, 200 Å, and 250 Å thick on both types of substrates.

Once the photoresist was removed in an ultrasonic bath of acetone, electrical leads

were attached to the contact pads under microscope. Initial 4-wire measurements of the room temperature resistance showed that indeed the quality of the underlying layer partly determined the resistivity of the film. Two of the samples had open paths, because the lines had been accidentally scratched while the electrical leads were being attached.

Au thickness (Å) ±2 Å	Resistance (Ω) of film on substrate	
	0.3 μm SiO_2	0.5 μm SiO_2
50	–	10150
150	4060	–
200	2136	1235
250	1596	1036

Table 4.1: Room temperature resistance of thin gold films on two different substrates. (–) indicates the gold paths that were open.

The resistivity of the thicker films at lower temperatures is plotted in Figure 4.2. Though the thickness of the film did not seem to affect the resistivity of gold for the substrate with the thicker oxide, the effect of the substrate is quite apparent. The $\star$ and $\triangle$ points correspond to the 0.3 μm SiO_2 substrate samples with 200 Å and 250 Å thick gold films respectively, while the $\times$ and $\square$ points correspond to the 0.5 μm SiO_2 substrate samples with 200 Å and 250 Å thick gold films respectively. The residual resistivity is much higher for the films on the thinner oxide. From this, it was concluded that to get the correct absorber sheet resistance, resistivity measurements would have to be performed for each wafer immediately prior to the absorber deposition.

By using the 200 Å Au on 0.3 μm SiO_2 data as a rough estimate of the thin film resistivity and extrapolating to $T = 300\,\text{mK}$, the sheet resistance is only $2\,\Omega/\square$. So, a 375 μm long leg, 50 μm wide (the size of the mesh legs) would only have a resistance of $\sim 16\,\Omega$. To increase the resistance to 188.5 Ω, the thickness of the gold film would

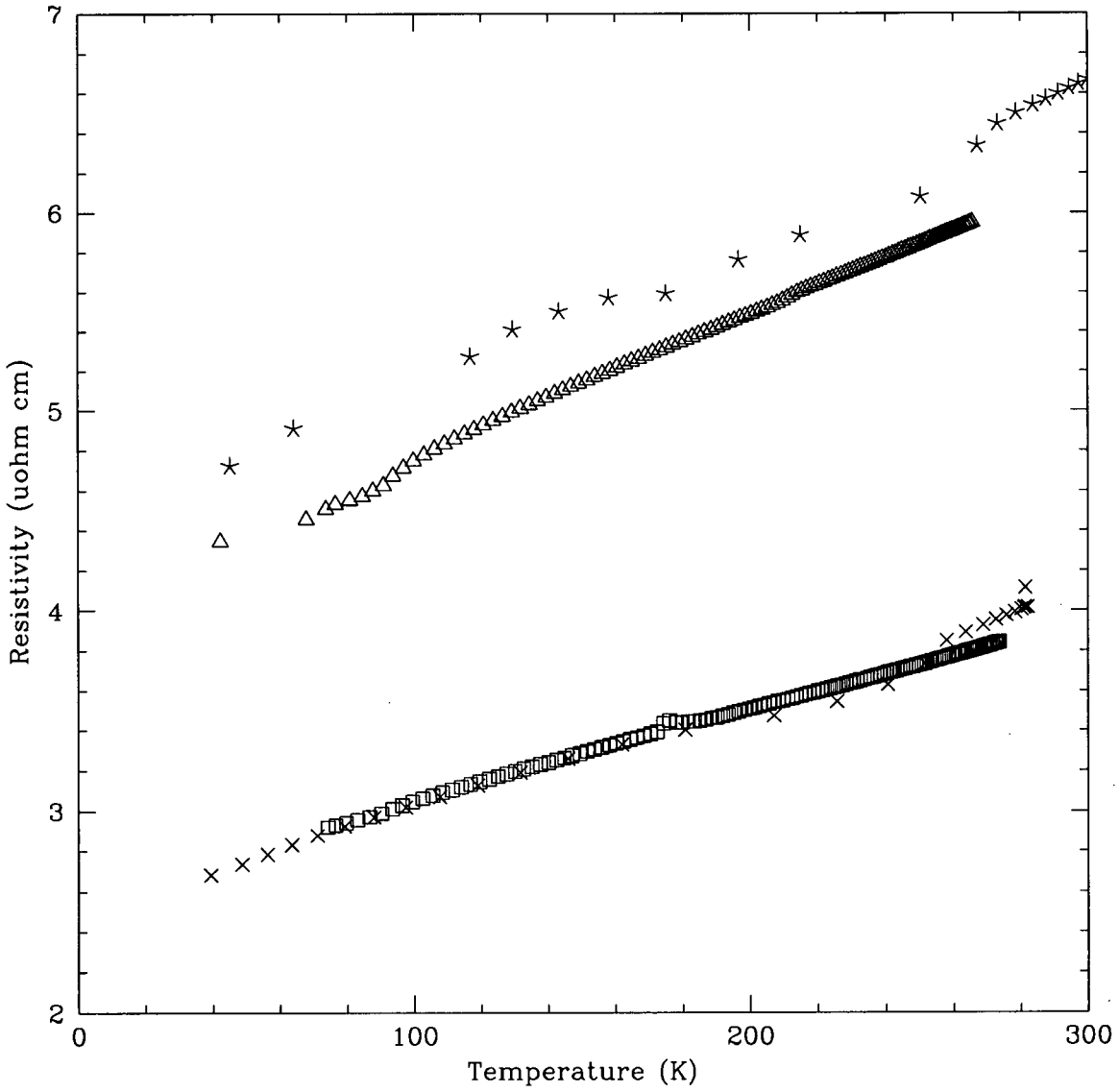

Figure 4.2: Resistivity vs temperature for gold films with thicknesses: 200 Å (×,⋆) and 250 Å (□, △) on 2 different substrates. See text for details.

have to be a mere 17 Å thick. Such a thin film is likely to be discontinuous. A better alternative is to decrease the width of the path from 50 μm to 5 μm.

Another important test for these films is to examine how well they hold up in a hot EDP bath. Although EDP does not etch gold, it will slowly etch titanium. Another Si chip (with a 0.3 μm layer of SiO_2, cut from the same wafer used for the resistivity measurements) was coated with 60 Å of Ti and 200 Å of Au. It was then placed in a bath of EDP held at 95 °C for 10 minutes. When the sample was removed and rinsed, the metal layers were gone and flakes of the gold film could be seen floating in the EDP solution. The gold would have to be evaporated directly onto the Si.

4.3 Au on Si

Anticipating the complete bolometer fabrication process, it is necessary to evaporate 5 μm wide lines onto 30 μm wide legs, which is a little tricky. The Si mesh cannot be defined prior to the gold mesh deposition because photolithography must be used to pattern the gold mesh and it is difficult to spin an even photoresist layer onto an already defined Si mesh structure. Furthermore, since the gold must be evaporated directly onto the Si, the SiO_2 must be removed from the topside of the membrane for the Au path. Only enough of the protective oxide is removed to define the Au pattern, so that the remaining oxide can be patterned to define the Si mesh. In this case, the metal lift-off technique cannot be used. If there is an overhang in the resist layer, than the oxide etch will be too wide. That is, the gold layer will be the correct width, but the subsequent patterning of the oxide layer to define the mesh structure would be compromised. Therefore, only standard photolithography can be used.

A BOX wafer with a 5 μm device layer was oxidized and etched to open up the back windows. After 6 hours, the wafer was removed, and the unetched outside edges of the

wafer were trimmed and diced into 1 cm^2 samples. Each of these was patterned with a new meander path design that was 3.390 cm long and 5 μm wide. After the photoresist was exposed and developed, the samples were placed into HF for 3 minutes to etch away the oxide. The resist layer was left intact on the samples which were now ready for the gold evaporation.

Before gold was deposited onto the samples, two cleaned pieces of Si, cut from the same wafer as the samples, were placed into the bell jar to test the adhesion of gold to Si. Once the chamber was evacuated to 8 μTorr, it was back filled with Ar gas and ionized with the discharge rod. The Si pieces were subjected to the plasma scrubber for 15 minutes, after which the chamber was evacuated once more. Once the pressure reached 2.8 μTorr, a 200 Å layer of gold was deposited onto the samples. The adhesion was quite good as the gold film could not be lifted off with scotch tape. However, the film could still be easily scratched off with tweezers. One of the samples was then placed in hot EDP for 10 minutes. The gold film did in fact protect the Si from the etchant.

The meander path samples were subsequently placed in the evaporator and gold was evaporated under the same above conditions. Three samples had complete gold lines, and had films with thicknesses of 152 Å, 173 Å, and 202 Å. These 3 samples were mounted onto the probe and lowered into the ^{4}He dewar for resistance measurements. Unfortunately, the 173 Å sample cracked as it was being cooled in the dewar. The data is graphed in Figure 4.3 which includes the resistivity of bulk gold (solid line) [28] for reference.

One can also see that the resistivity of thin gold films at absolute zero is not in fact zero, but there is a residual resistivity. In Figure 4.4 the resistivity is graphed against the inverse of the film thickness and shows that $\rho_i \propto 1/t$ with a non-zero intercept. We do not believe that $\rho = 0$ at finite thicknesses. Perhaps the steep slope of ρ vs $1/t$ for thin films can be attributed to grain boundary scattering since the films may be slightly discontinuous. Once the film thickness is greater than 250 Å, the film becomes continuous

and the film behaves like the bulk material.

For one gold mesh leg 375 μm long, 5 μm wide to have the desired resistance of 188.5 Ω, $R_\square = 188.5\,\Omega(5/375) = 2.5\,\Omega/\square$. From Figure 4.4, this corresponds to a thickness of $t = 152$ Å. This is the thickness of gold that should be deposited onto the Si membrane.

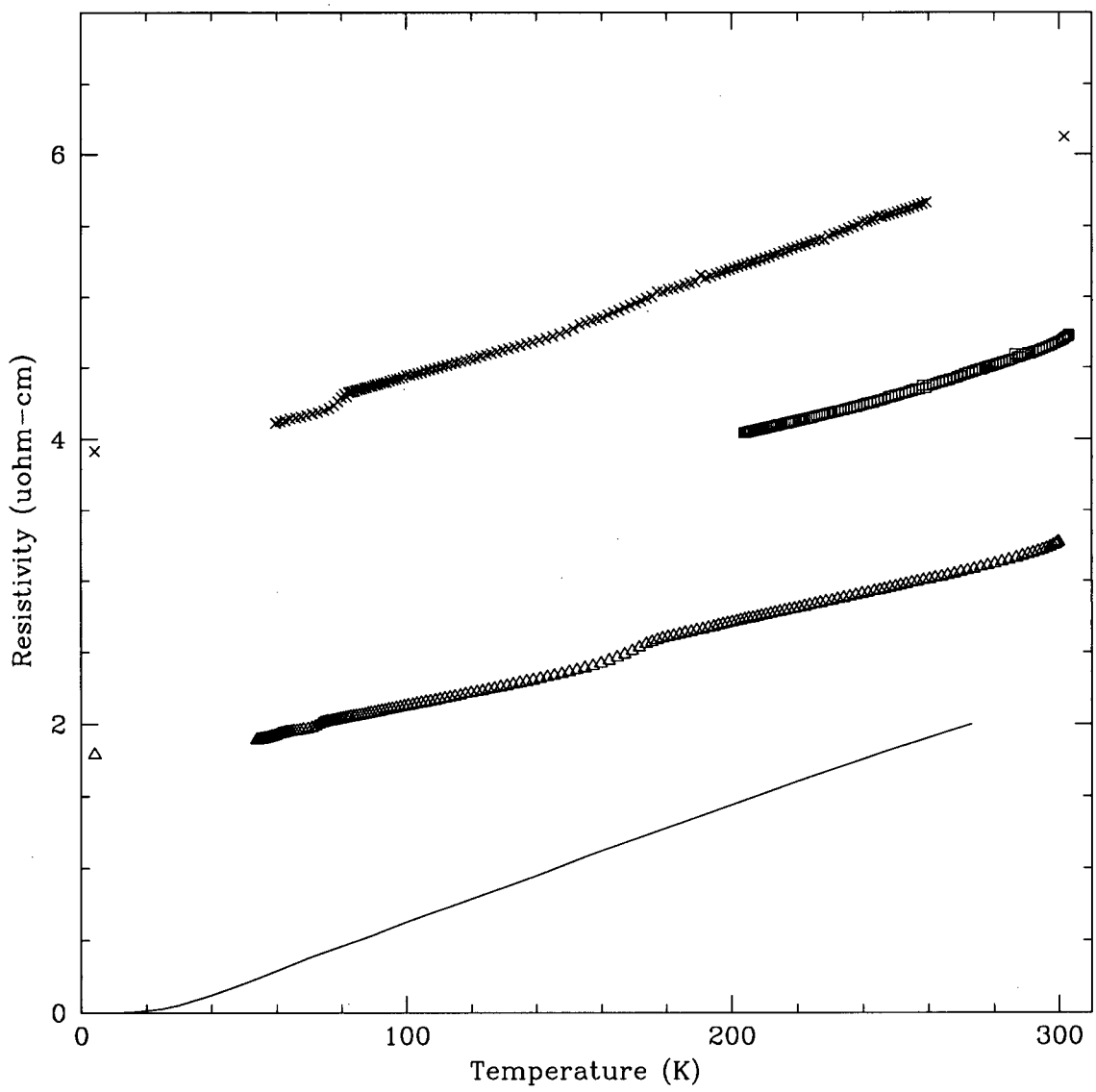

Figure 4.3: Resistivity vs temperature for gold films with thicknesses: 152 Å (△) (closest to target resistivity), 173 Å (□) and 202 Å (×). The solid line is the bulk resistivity of gold [28].

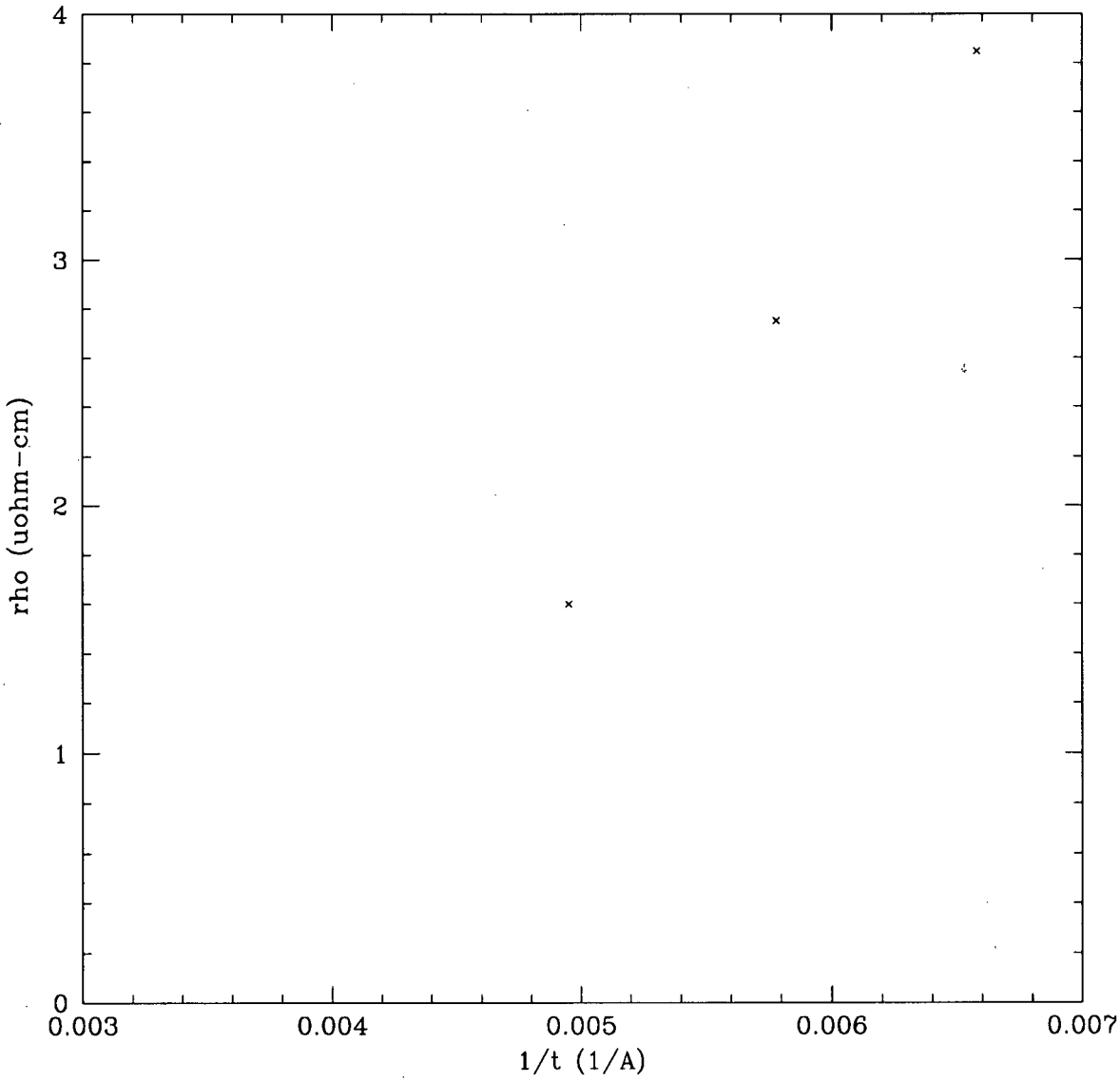

Figure 4.4: Resistivity vs. inverse film thickness at T=0 K.

Chapter 5

Conclusions

With the micromachining techniques developed in the earlier chapters, one is now in a position to combine the successful processes into a bolometer fabrication procedure. In particular, it is possible to etch the support structures and deposit the desired absorbing layers. The recommended process is presented here.

A silicon mesh, as in Figure 1.8 with a thin gold absorption layer, could be fabricated following the steps in Figure 5.1. First, a custom ordered buried oxide (BOX) silicon wafer, which consists of a 1 μm silicon oxide layer sandwiched between a 5 μm thick silicon layer and a 525 μm silicon handle wafer, is cleaned and thermally oxidized (a). Next, a 1 cm square opening is removed from the handle wafer in EDP (b). Before the etch reaches the BOX layer, the etch is stopped and gold is evaporated onto both sides of the wafer. A gold mesh is patterned on top and gold contact pads, 2 mm$\times$3 mm, on the bottom for the thermistor electrical leads (c). The rest of the opening in the handle wafer is then etched to completion (d). The top oxide layer is then patterned to reveal the final mesh pattern (e), after which, the mesh is patterned into the thin silicon layer, (f). The mesh is then released when all the oxides are removed in HF (g). Finally, a prepared NTD Ge thermistor is glued onto the mesh while the brass leads are glued to the gold contact pads on the outer silicon frame (h).

There are two logistical reasons to stop the back etch before the EDP reaches the etch stop layer (steps (b) to (d)). Firstly, it is easier to work with the whole wafer when the membrane area is still thick. The photolithography steps to define the gold

mesh pattern can be performed without worrying about membranes popping out due to surface tension. The second reason deals with timing and the juggling act of working at two cleanroom facilities. It takes roughly 1.5 hours to pattern the oxide on the wafer to open up the back windows, while the etch itself takes a little more than 7 hours to proceed through the full thickness of the handle wafer. The subsequent photolithography process to define the gold mesh pattern takes another 1.5 hours. However, the photolithography processes for both the back window and gold mesh patterning must be performed in the SFU cleanroom since their mask aligner can handle 4″ wafers and has double side alignment capabilities. The latter is very important since it ensures that the gold mesh pattern is properly centered over the membrane and will subsequently be properly aligned with the Si mesh. So, in theory, one could do all three process in a 10 hour workday at SFU without stopping the etch midway as previously described. However, one must remember that at the end of the 7+ hour EDP etch, the membranes will be very delicate and fragile during the subsequent patterning process and one will most likely be too fatigued to perform the delicate work involved in the next patterning step. This is not the best working combination and nothing is gained by it. Stopping the etch midway allows one to work with a more robust wafer and with a more alert frame of mind.

Although Figure 5.1 only shows the cross section of one device on the wafer, each 4″ wafer can hold at least 40 individual detectors, leaving ample room for alignment marks and wafer dicing lines. Clearly, many bolometer designs of differing dimensions can be made on one wafer at once.

Once the thermistor is attached and the leads soldered to the gold contact pads, the bolometer can be mounted into modified copper holders which are compatible with the BAM dewar coldstage. The Si frame can be soldered to a flexible support made from gold plated 0.005″ copper sheet metal bent as in Figure 5.2. The sheet metal provides rigid support but allows for thermal contraction of the bolometer during cooling. The

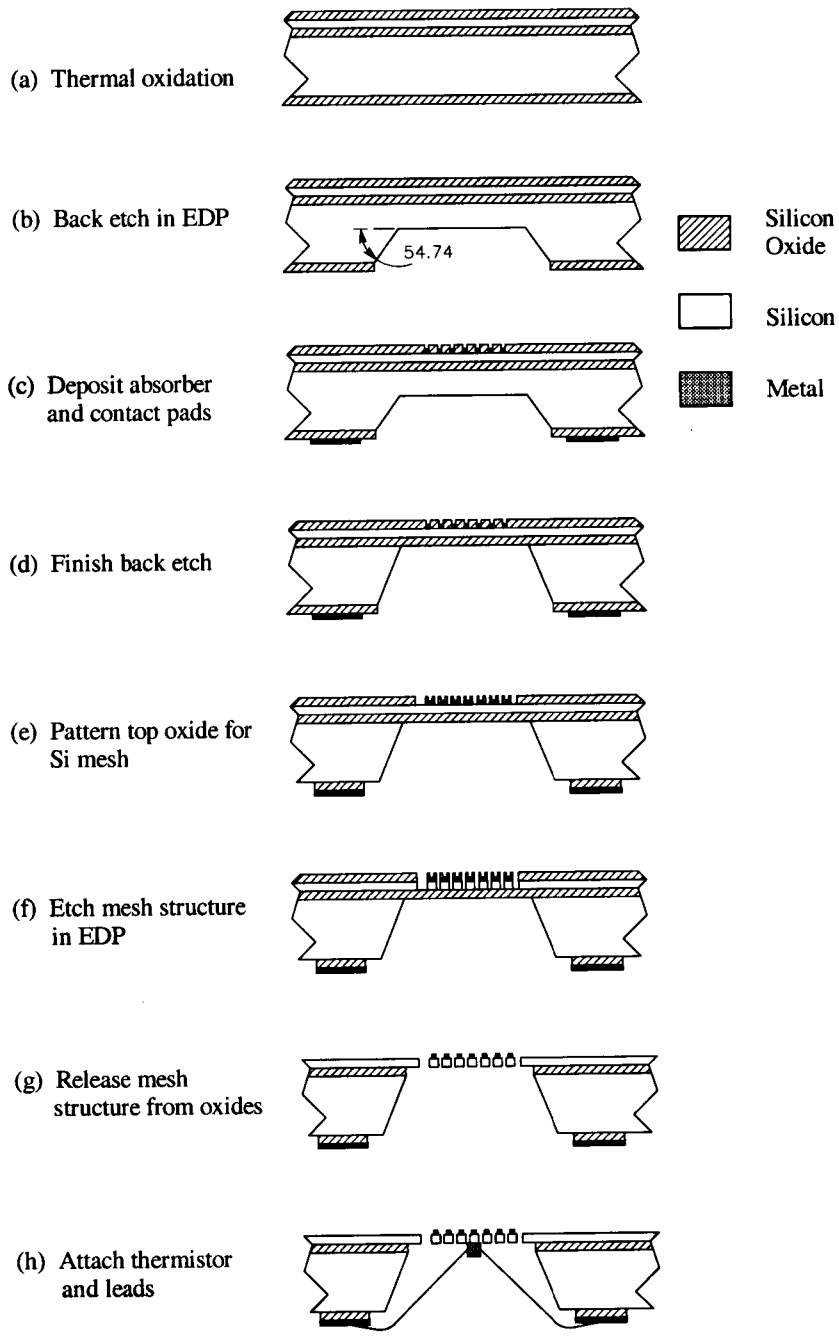

Figure 5.1: Basic steps to building a micromesh bolometer (not to scale). See text for details.

support is soldered to a ring against which the Winston cone is mounted (see Figure 5.3).

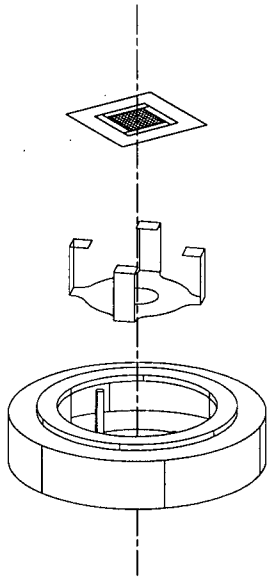

Figure 5.2: Bolometer holder assembly. The bolometer (top piece) is soldered to a flexible copper support (center) that is mounted to the copper ring (bottom) which is compatible with the dewar coldstage.

5.1 First Attempt at Using This Recipe to Build Bolometers

The above recipe was tried on one wafer. As before, a BOX wafer was first cleaned in a series of hot baths containing hydrogen peroxide with ammonium hydroxide, buffered hydrofluoric acid, and finally hydrogen peroxide with hydrochloric acid. This cleaning procedure removes organic materials, native oxides and metals from the surfaces of the wafers and thus should be performed immediately prior to being place in the furnace for oxidation.

Once clean, the wafers are thermally oxidized at 1100 °C as in Appendix A.2. First in a thin dense oxide is grown in a dry oxygen environment. Subsequently, the bulk of

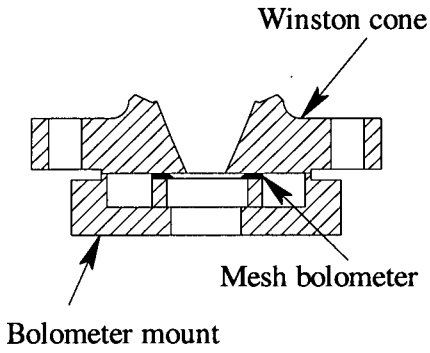

Figure 5.3: The bolometer is placed at the output of a Winston cone. The raised central portion of the bolometer is the radiation absorbing region.

the oxide is grown in a wet oxygen environment where water vapour is present. Then, a secondary thin layer of dry oxide is grown on top. This dry-wet-dry oxide sandwich is more chemically resistant to the silicon etchants and ensures that there are no pinholes in the oxide. Because oxides grown in a wet atmosphere tend to be less dense, defects and pinholes are more likely to appear unless thicker oxides are grown. On the other hand, wet oxides grow much faster than dry oxides. It takes 40 minutes to grow $0.3\,\mu$m in a "wet" furnace and 3 hours in a "dry" furnace. The dry-wet-dry sandwich cuts down on the growth time and produces oxide films adequate for protection against the EDP etchant. The baking temperatures and growth times given in the appendix form an oxide layer $\sim 0.3\,\mu$m thick.

Note in Figure 5.1 that the oxide layers on both sides of the wafer are the protective masking layers for all subsequent silicon etching steps. As a result, both sides of the

wafer must be protected during all photolithography processes, either with photoresist, or by floating the wafer on the buffered HF etchant so that only one side is etched at a time.

Since the bolometer will be fabricated from the 5 μm device layer on the wafer, an appropriately sized portion of the handle wafer must be removed. Square windows, 7 mm×7 mm, are patterned, via photolithography, into the oxide on the backside of the wafer. Because the Si etchant is anisotropic, the resulting sloped walls will form a smaller square opening at the membrane, 6 mm×6 mm in size. At the same time that the windows are pattered, 50 μm wide scribe lines which traverse the length of the wafer are also patterned into the photoresist. These scribe lines provide defined fault lines along which the wafer can be broken to isolate individual devices. It was found previously that without etched scribe lines, the wafer tended to crack at the boundaries of the etched windows instead of cracking along the surface scribe lines made with a diamond tipped scriber. Also, alignment marks on the mask, under each square opening, provide easy alignment for subsequent masks. Note however, this requires a mask aligner with back side alignment capabilities.

Once the oxide has been patterned, the exposed silicon is etched in a hot bath of ethylene diamine pyrocatecol (EDP). The etch is allowed to proceed for 6 hours and is subsequently stopped before the etch is allowed to reach the etch stop layer. The remaining layer of Si ($\sim$ 150 μm thick) can be removed at a later time after most of the other processes are completed.

The radiation absorbing gold layer should be deposited in a grid pattern which will lie directly on top of the Si mesh. In order for the film to be of a reasonable thickness, the grid is made up of 5 μm wide lines, 150 Å thick. The grid spacing is 0.375 mm. Ideally, the supporting Si would also have 5 μm wide legs, but because of the fragility of the mesh as discussed in Chapter 3, this proved infeasible. Instead, the design uses

30 μm wide legs since they are mechanically stronger and robust once the buried oxide layer has been removed. As a result, the thinner gold lines must be defined first with photolithography. The gold mesh cannot be deposited after the Si mesh has been etched into a free standing mesh because the mesh does not provide an adequate solid surface to spin on an even film of photoresist.

Because of the decision to evaporate gold directly onto Si described in Chapter 4, the metal lift-off technique was not used, and the standard additive photolithography technique was used instead. In this work, this step was only performed on two individual devices instead of the whole wafer, although presumably in practice, one would use the entire wafer. Photoresist was spun only onto the topside of the wafer (leaving the backside clean for the second Au deposition). After exposure and development, they are floated on buffered HF for 3.5 minutes to etch away the exposed oxide on the topside. The chips were not immersed as there was no protective resist coating on the backside. The resist on the topside is left on to await the Au deposition.

The two devices were then placed in the thermal evaporator and Au was deposited to a thickness of 150 Å. After the evaporation, the chamber was vented and the devices were turned over and placed onto a premade aluminum support. The support design was precisely made so that gold would be evaporated only onto two ellipsoidal areas to form two gold pads on the backside of the Si frame. Because the size and orientation of the gold contact pads is noncritical, this simpler method of deposition was preferred over going through the more time-consuming photolithographic method. The contact pads consisted of 500 Å Cr adhesion layer with $\sim$ 1000 Å Au. This double layer typically forms robust pads that can be easily soldered to and are more resistant to light scratches. Note that the total heat capacity of the outer frame is not an issue so evaporating Cr as part of the contact pads is likewise not an issue.

After all the depositions, the photoresist on the topside was lifted off in acetone with

an ultrasonic cleaner. After a rinse in DI water, the Au mesh structures were examined under a high power microscope and found to be intact. Unfortunately, a meander path was not included in the mesh deposition run, so we were unable to measure the resistance of the gold mesh. A meander path should be included in future gold evaporations.

At this point, the remaining portions of the handle thickness in the back windows can be removed in EDP. The chips were held on edge in a custom built teflon chip holder and immersed in EDP for approximately 2.5 hours. Unfortunately, the area between the gold mesh lines and the surrounding oxides were not completely sealed. There were gaps in some areas between the gold film and the oxide well walls (the area in the dashed circles in Figure 5.4). As a result, the EDP managed to reach the Si membrane through these joints and undercut the protective oxide layer. After the 2.5 hour etch, all that remained of the membrane layer were small squares so that it was impossible to define the mesh structure.

This problem could be avoided in the future by depositing a layer of evaporated SiO_2 over the gold mesh and the existing oxide as a protective layer. This oxide coating would then be removed in the final HF etch when the Si mesh is released from the BOX layer.

In conclusion, we have determined a repeatable process to construct Si meshes from from BOX wafers with 5 μm device layers and have developed a process to determine the necessary film thickness for a gold absorber. A recipe has been developed from which bolometers can be made.

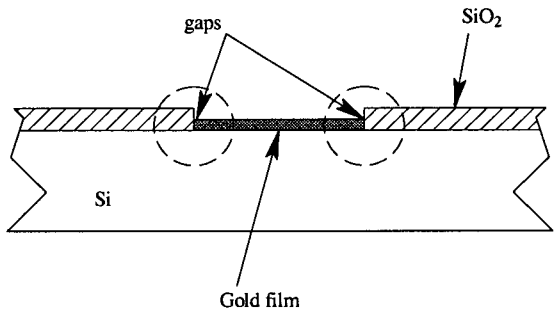

Figure 5.4: Gold film evaporated onto Si with surrounding silicon dioxide walls. The film does not seal with the oxide walls (region indicated by the dashed circles) and there are gaps between the gold film and oxide.

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Appendix A

Cleanroom Process Recipes

** Recipes adapted from Bill Woods' "Process Batch Sheets" [29].*

*** Recipes adapted from Al Schmalz's "Cleanroom Standard Operating Procedures" [30].*

A.1 RCA Clean *

1. **Organics clean:** In a clean beaker, heat to 80 °C: 1000 mL deionized (DI) water, 150 mL NH_4OH and 150 mL H_2O_2.
2. When temperature is stabilized, soak wafers for 10 minutes.
3. Rinse in DI water for >3 minutes.
4. **Native oxide strip:** Place wafers in room temperature container with 1500 mL DI water and 150 mL buffered HF for 30 seconds.
5. Rinse in DI water for >3 minutes.
6. **Metals:** In a clean beaker, heat to 80 °C: 1050 mL DI water, 175 mL HCl and 175 mL H_2O_2.
7. When the temperature is stabilized, soak wafers for 10 minutes.
8. Rinse in DI water for >15 minutes.
9. Spin dry the wafer or use a N_2 air gun.

A.2 Oxidation Recipe for a 0.3 μm Oxide Layer *

1. *Prior to oxidation, all wafers must be RCA cleaned.*
2. Ramp the furnace temperature to 800 °C. There should be a 4 scfh flow of N_2 gas through the furnace.
3. Load wafers into proper boat and push the boat into the furnace at <4″/min.
4. Ramp the temperature up to the desired oxidizing temperature (usually 1100 °C).
5. **Dry oxidation:** Once the temperature is stabilized proceed with a dry oxidation for 10 minutes. N_2 flow rate: 0 scfh, O_2 flow rate: 4 scfh.
6. **Wet oxidation:** Proceed with wet oxidation for 30 minutes. O_2 gas is bubbled through boiling water at ~0.5 scfh with the N_2 flow rate of 4 scfh.
7. **Dry oxidation:** Repeat the dry oxidation step.
8. Shut off the oxygen flow, the nitrogen flow rate remains at 4 scfh. Ramp down the temperature to 400 °C.
9. When the furnace temperature is <800 °C, pull the boat from the furnace at <4″/min.
10. Once wafers are cool, compare their colour to an oxide colour chart. A blue to blue-green colour when looked face on indicates a thickness ~0.3–0.325 μm.

A.3 Boron Diffusion *

1. *Prior to oxidation, all wafers must be RCA cleaned.*

2. Ramp the furnace to 800 °C. N_2 flow rate: 10 scfh. and O_2 flow rate: 0.

3. Load the wafers into the boat so that there are 2 wafers per boron source with the polished side facing the source. Place dummy wafers in unused slots. Push the boat into the furnace at <4″/min. N_2 flow rate: 5 scfh. and O_2 flow rate: 5 scfh.

4. Ramp furnace to operating temperature of 975 °C. N_2 flow rate: 10 scfh. and O_2 flow rate: 0.

5. **Diffusion** Leave at operating temperature for desired time. 40 minutes produces a doping concentration of $\sim 10^{18}$ atoms/cc. N_2 flow rate: 10 scfh. and O_2 flow rate: 0.

6. Ramp down the furnace temperature to 400 °C. Once all the furnace zones are < 800 °C, the boat can be removed at <4″/min. N_2 flow rate: 5 scfh. and O_2 flow rate: 5 scfh.

7. Return furnace to idle. N_2 flow rate: 0.5-1.0 scfh. and O_2 flow rate: 0 scfh.

A.4 General Photolithography *

1. On the less critical side of a clean wafer, spin SC??? photoresist for 30 sec at 4000 rpm. (*If this side does not need protection, skip this step and proceed to step 3.*
2. Soft bake at 100 °C for 5 minutes.
3. Spin photoresist onto the other side of the wafer for 30 sec at 4000 rpm.
4. **Soft bake:** Soft bake at 100 °C for 25 minutes.
5. **Alignment and exposure:** *Exposure times may vary depending on the type of mask being used and on the underlying substrate. If exposure times are unknown, perform exposure tests on scrap wafers.*

   Align the wafer to the mask. For *Kodak* photoemulsion masking plates and thermally grown silicon oxide, expose the resist with 10 mW/cm^2 of UV light for 20 seconds. For chrome on soda lime glass masks, the exposure time is ~8 seconds.
6. **Develop:** Develop the wafer in *Shipleys MF 319* developer for 35–45 seconds.
7. Rinse in DI water for >3 minutes and dry with N_2 gun.
8. **Hard bake:** Bake for 20 minutes at 120 °C.
9. Inspect for resist defects or mask misalignments. If there are no problems, proceed with subsequent process (eg. oxide etch and doping). Otherwise, strip the resist with acetone and repeat the above steps.

A.5 Metal Lift-off **

1. Spin *AZ4210* photoresist onto wafer for 40 seconds at 4000 rpm. This should produce a film ~2.1 μm thick.

2. **Soft bake:** Soft bake the wafer on a temperature controlled hotplate for 1 minute at 100°C.

3. Soak the sample in *AZ300MIF* developer for 2 minutes. The goal here is to harden the top portion of the photoresist layer so that the unexposed areas are less susceptible to the *AZ400K* developer. Rinse in DI water and dry with N^2 gun.

4. **Exposure:** Expose the resist for 50 seconds to UV light through a chrome on sodalime mask at an intensity of 4 mW/cm^2 *(The exposure time may vary depending on mask type, if unsure, run a few exposure tests.)*

5. **Create overhang:** Develop in 1:3, *AZ400K*:DI water for 2 minutes. The goal here is to slightly overdevelop the resist so that the hardened top layer of the resist is slightly undercut. Rinse in DI water and dry.

6. Inspect the resist for defects. If all is well, metallize the sample to the desired thickness.

7. **Lift-off** Strip the photoresist in straight *AZ400K* or acetone in an ultrasonic cleaner.

A.6 The ECR PlasmaQuest System *

Refer to Standard Operating Procedure (SOP) for detailed instructions for this system.

1. Open the appropriate gas cylinders located in or beside the gas cabinets.
2. Open the mass flow controller valves and turn on the water chiller, RF supply and microwave power switches.
3. Login to computer and set up the appropriate recipe for etch times, chamber pressure, gas flow rates and microwave power.
4. Load samples into load lock and begin the recipe.
5. Once the microwave power is on, manually turn on the RF power, and set it to the desired DC bias. Turn it off when the microwave power switches off.
6. When the recipe is complete, and the samples have returned to the load lock, vent the chamber and remove the samples.
7. Repeat for other samples. When finished, pump out the load lock and log off the computer.
8. Follow the steps outlined in the SOP to close and vent the gas lines.

A.7 Ashing Photoresist with the Technics Plasma Etch II

1. Close chamber valve on front of etcher and ensure all gas lines are closed.
2. Vent the chamber (with the vent switch) and load samples.
3. Close lid and open chamber valve to pump down the chamber to <20 mTorr.
4. Set temperature controller to 50°C.
5. Open the oxygen gas line and adjust the flow meter until the pressure reaches $\sim$ 250 mTorr.
6. When the pressure is stable, ignite the plasma.
7. Turn on RF power to 150 W for 10 minutes.
8. Turn off RF power, close oxygen line and chamber valve. Vent chamber to remove samples.

A.8 E-Beam Evaporation Using the *Balzers* Evaporator **

1. Vent chamber and load samples onto stand, directly above the source.

2. Pump down chamber with roughing pump until the pressure is below 7×10^{-3} Torr.

3. Close the valve to the roughing pump and open the valve to the cryopump. *Note: the cryopump must be cooled to ~12–13 K beforehand.*

4. Turn on the high voltage power supply and water flow to the electron guns 15 minutes prior to evaporation. Set the crystal growth monitor settings for density and z-factor. The tooling should be set to 150 % since the crystal is mounted on the bell jar ceiling, above the sample stage.

5. Once the pressure is below 3×10^{-6} Torr, evaporation may begin. Ensure that all emission dials are set to zero and turn on the electron guns. Slowly ramp up the emission current until the beam visibly melts the surface of the source. Align the beam to the centre of the source. Typically, an emission current of 0.4 A and 0.7 A will melt Au and Ti sources respectively and produce film growth rates of 1.2 Å/s. Use the shutter to start and finish the evaporation.

6. Once the evaporation is complete, slowly turn down the emission current, then turn off the electron guns. Allow the source and samples to cool for 30 minutes before venting the chamber.

A.9 Thermal Evaporation in the BAM Lab Bell Jar

1. Vent chamber and load samples onto stand, directly above the source. Move the crystal growth monitor as close to the samples as possible.

2. Pump down the chamber and turn on the high voltage glow discharge rod. Once the pressure is $< 3 \times 10^{-2}$ Torr, turn on the diffusion pump heater. Be sure that there is water flowing through the cooling lines to the diffusion pump and the crystal growth monitor.

3. When the pressure is $< 7 \times 10^{-3}$ Torr, close the roughing pump line and begin pumping on the diffusion pump. When the thermocouple on the heater reads ≥ 2.5 mV and the diffusion pump pressure is $\sim 10^{-3}$ Torr, open the gate valve to the chamber.

4. Backfill the chamber with Argon gas once the pressure has dropped to 10^{-5} Torr. Run the discharge again, maintaining the pressure at $\sim 3.5 \times 10^{-2}$ Torr and leaving the Argon plasma on for $\sim$15 minutes. Pump out the chamber again as before.

5. When the pressure is below 3×10^{-6} Torr, the evaporation may begin. Turn on the filament and ramp up the current until the source begins to melt. Use the shutter to control the film thickness.

6. Once the evaporation is complete, turn down the filament current and wait for the source and sample to cool.

7. Close the chamber gate valve. Turn off the diffusion pump heater but continue to pump on the oil until cool. At this point, the chamber may be vented and the samples removed.

A.10 Anisotropic Si Etch: EDP or TMAH *

1. Heat fresh etchant in a beaker with a reflux condenser to operating temperature. EDP: 95 °C, TMAH: 85 °C.

2. Ensure that the wafer is appropriately masked with a material that is not etched in by the etchant (SiO_2 or gold are good masking materials).

3. Once the etchant temperature is stable, place the wafer into solution. The EDP etch rate is on average $\sim$70 μm/hour, while TMAH etches at $\sim$40 μm/hour, so time the etch accordingly. Do not remove the wafer until etch is complete.

4. Remove the wafer and immediately rinse with DI water for >5 minutes.

5. Dry with N_2 gun or rinse with isopropanol and heat dry in oven.

A.11 Oxide Etch: HF *

1. The sample is first patterned with photoresist using photolithography.

2. After the hardbake and inspection, place the sample in *Transene* buffered HF solution. This solution etches thermally grown oxide at $\sim$0.1 μm/min. Time the etch accordingly to avoid undercutting the photoresist. *Note: Since Si is hydrophobic, one can tell by eye when the etch is complete since the etched areas will "dewet" once the HF reaches the underlying Si.*

3. Rinse the sample for 5 minutes in running DI water, and dry with N_2 gas.

Appendix B

Si Wafers and Processing Chemicals Suppliers

- **Single side and double side polished wafers:**

  Silicon Sense

  #217-110 Daniel Webster Hwy

  Nashua, New Hampshire 03060-5252

- **BOX wafers:**

  SiBond L.L.C. (no longer in business)

  501 Pearl Dr.

  P.O. Box 8

  St. Peters, Mo 63376

  SEH America

  4111 N.E. 112th Ave.

  Vancouver, Wa 98682-6776

- **Processing Chemicals:**

  Transene Co. Inc.

  10 Electronics Ave

  Davers, Ma 01923

Appendix C

NTD Ge Thermistors

The detector response to temperature changes depends entirely on how the thermistor's resistance responds to temperature changes. A steep resistance-temperature function over the operating temperature range is most desirable. Typically, doped semiconductors, such as Si or Ge, exhibit this electrical behaviour. The type of dopant and doping concentration determine the useful operating range for bolometers. For example, silicon chips doped with arsenic and phosphorous and metallized with bismuth, have been used as monolithic bolometers [4].

The thermistors used in this project are ultra pure germanium chips that have been neutron transmutation doped (NTD) to a doping concentration suitable for use at 300 mK by Haller et al. [5]. After the NTD process, the Ge crystals were thermally annealed at 400 °C to remove crystal lattice damage from the energetic neutrons, and to move dopant atoms to crystal lattice sites. Finally, to form electrical contacts, the two opposing surfaces are highly doped with boron and subsequently metallized with 100 Å Pd and 4000 Å Au.

Previously, the Haller thermistor chips that are currently being used as part of the BAM bolometers, have been characterized and found empirically to have a resistance that is described by

$$R(T) = R_{\circ} e^{\sqrt{\frac{T_{\circ}}{T}}}, \tag{C.1}$$

where $R_{\circ}$ and $T_{\circ}$ are constants with values of 200 Ω and 49 K respectively.

Because the thermistor elements are individually diced from a large sample their physical dimension vary to within tens of microns and hence $R_\circ$ may vary from element to element. This effect is probably insignificant and characterizing one thermistor should indicate how the rest will operate.

Electrical connections were made to one thermistor element with indium solder and 0.0003″ diameter brass wires. The wires were then soldered to posts and the chip was glued to a fiberglass base with epoxy. To test the feasibility of using our bolometers in quantum well experiments, one thermistor was sent to Daniel Tsui's lab in Princeton University where several tests were performed by Noh to characterize the thermistor response to temperature changes and to applied magnetic fields [31]. The results are graphed in Figures C.1–C.5.

By fitting the slopes of the curves in Figure C.3 at zero bias current for the different temperatures, one can deduce a resistance-temperature relationship using (C.1). The fitted slopes are given in Table C.1.

Temp (mK)	R (MΩ)
23	7637
64	7138
93	4879
152	2729
202	860
297	80

Table C.1: Fitted values of R at $I = 0$ and $V = 0$.

In Figure C.2, we fit the last three data points to (C.1) (assuming the thermistor freezes out below 150 mK) and calculate the values for the coefficients $R_\circ$ and $T_\circ$ to be, $R_\circ = 2300$ and $T_\circ = 32.8$. The value of R is roughly an order of magnitude larger than expected. This could be due to the experimental setup, but the matter was not pursued.

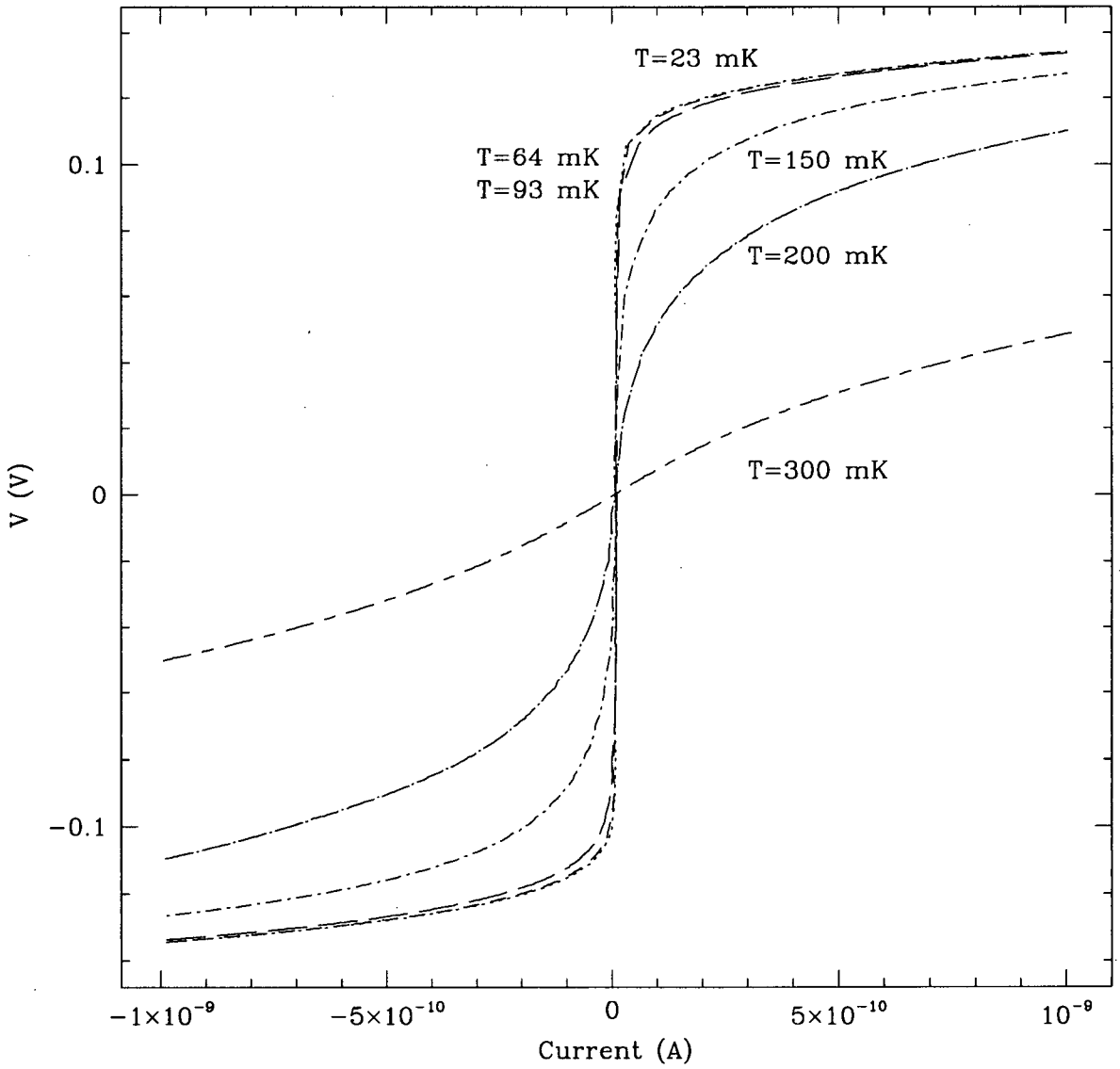

Figure C.1: *I–V* curves for NTD Ge thermistors at various temperatures [31].

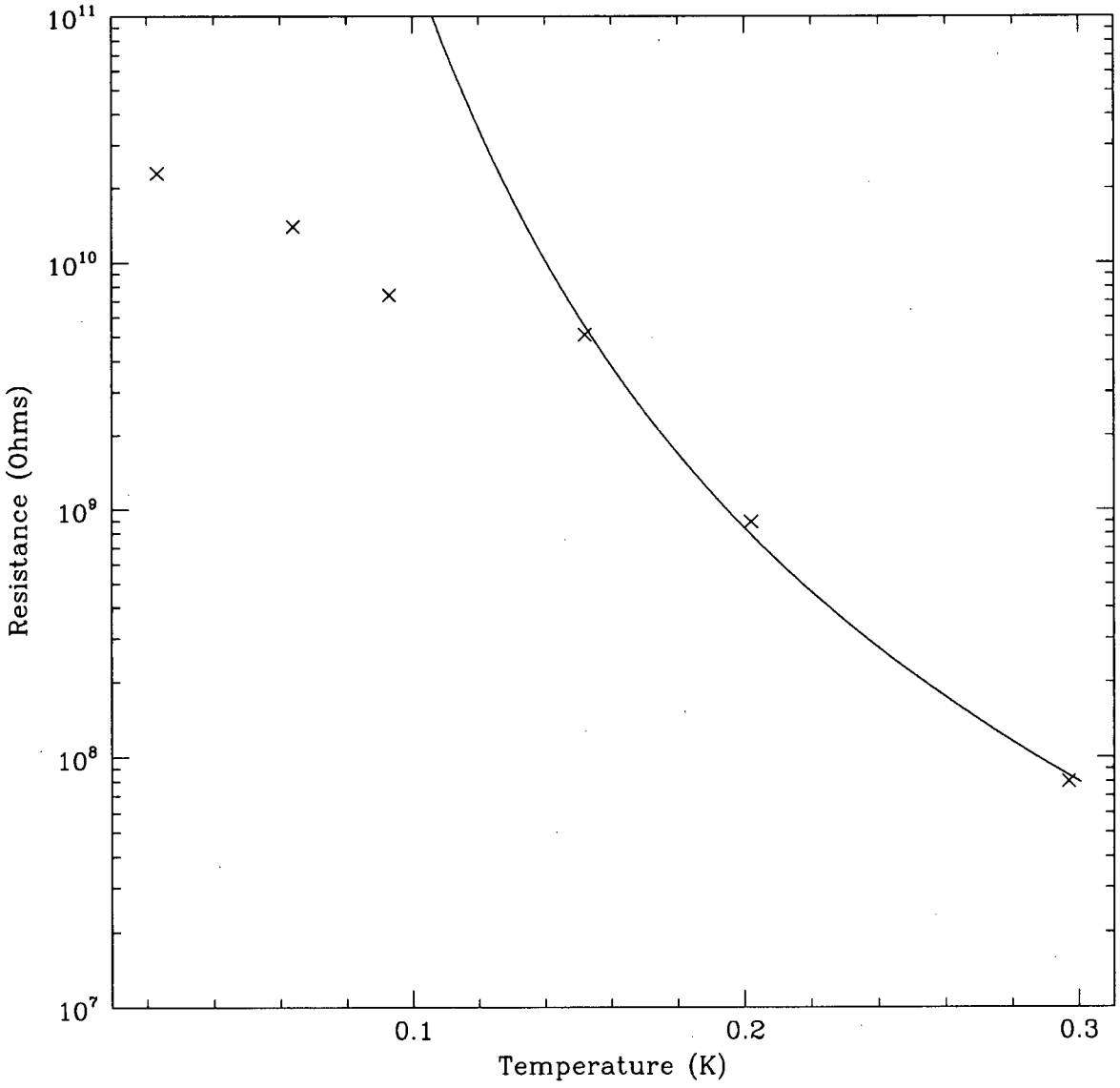

Figure C.2: $R(T)$ calculated from the last 3 data points in Table C.1. (×) Data, (–) Fit.

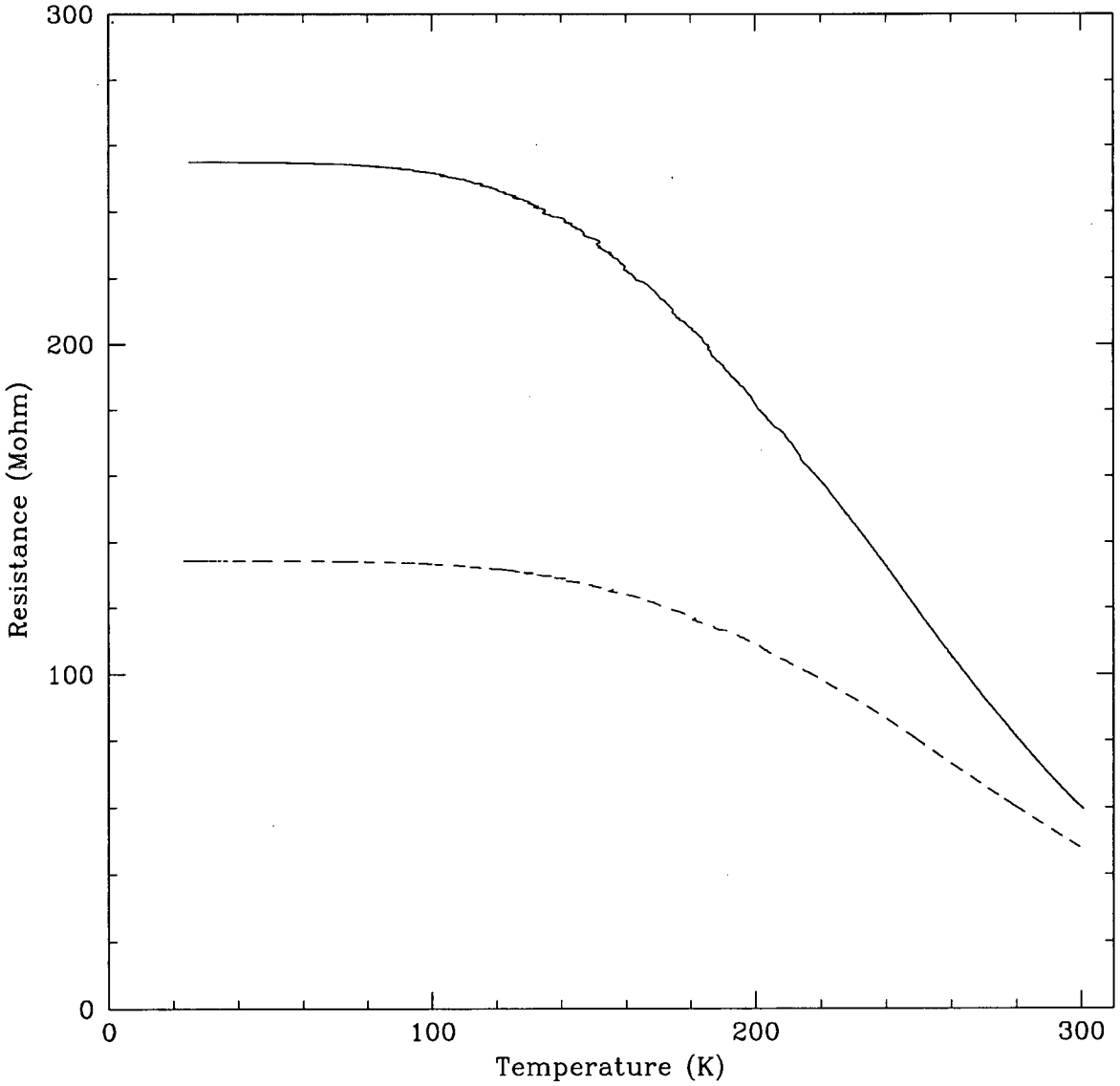

Figure C.3: Temperature sweep of a thermistor biased with a constant current of 0.5 nA (–) and 1.0 nA (- -) with no applied magnetic field.[31]

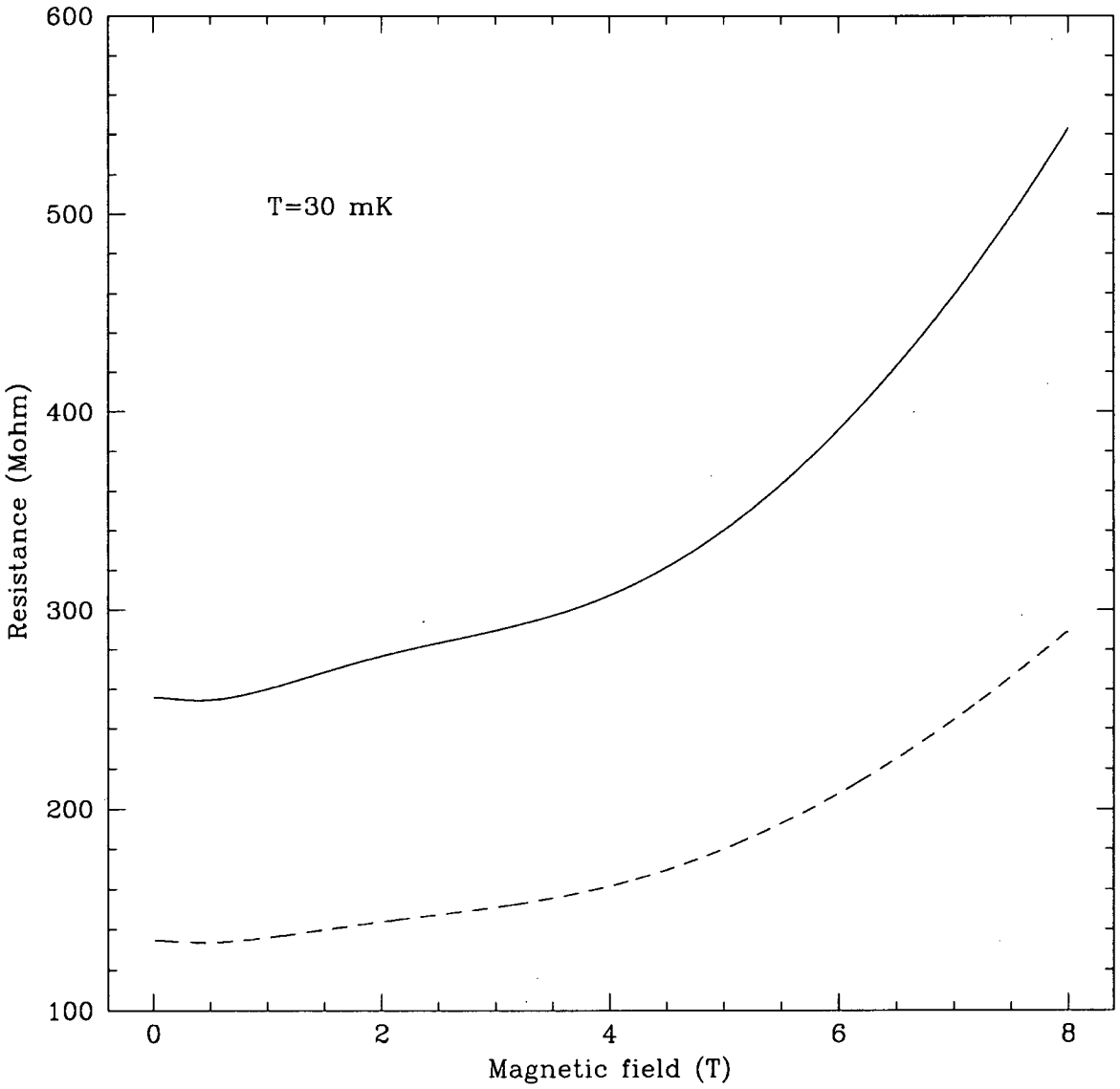

Figure C.4: Thermistor resistance vs applied magnetic field strength at T=30 mK. The thermistor is biased with a constant current of 0.5 nA (–) and 1.0 nA (- -). [31]

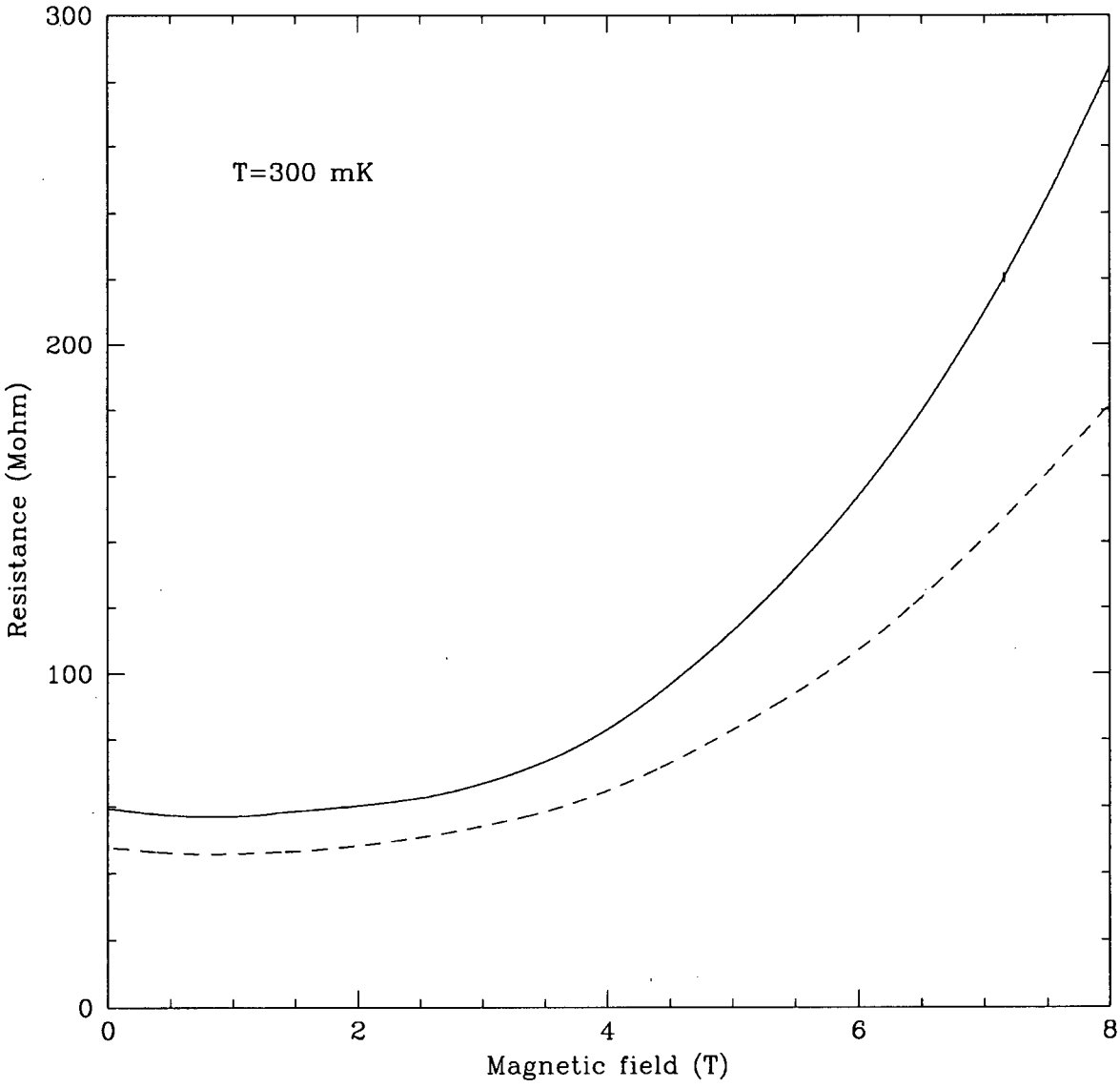

Figure C.5: Thermistor resistance vs applied magnetic field strength at T=300 mK. The thermistor is biased with a constant current of 0.5 nA (–) and 1.0 nA (- -). [31]