A SINGLE PHASE Al$_{0.3}$Ga$_{0.7}$As/GaAs HETEROJUNCTION
RESISTIVE-GATE CHARGE-COUPLED DEVICE

by

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We accept this thesis as conforming
to the required standard

THE UNIVERSITY OF BRITISH COLUMBIA
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Date **OCT. 5 / 92**
Abstract

The design, fabrication, and evaluation of a 128 pixel, single phase Al$_{0.3}$Ga$_{0.7}$As/GaAs heterojunction resistive-gate charge-coupled device (HRGCCD) is described. The HRGCCD has a higher operating speed and a larger charge handling capacity in comparison to the conventional buried channel, resistive-gate GaAs charge-coupled device (GaAs RGCCD). The higher operating speed of HRGCCDs is due to the higher electron mobility and velocity in an AlGaAs/GaAs heterojunction in contrast to a GaAs homojunction. In addition, the HRGCCDs can be integrated with high-speed on-chip high electron mobility transistors (HEMTs). The larger charge handling capacity of a HRGCCD is the direct result of the higher electron density in a HRGCCD in comparison to a GaAs RGCCD. A quantum mechanical model is used to calculate the carrier density in a triangular potential well formed at the interface between an undoped AlGaAs layer and an undoped GaAs layer. This model is coupled to a solution of Poisson's equation in bulk AlGaAs to determine the total carrier density in a HRGCCD for different layer and material specifications. This model is used to aid in the design of the HRGCCD. The fabrication of the HRGCCD required six mask levels employing 405 nm contact photolithography with a 1.0 μm design rule. Developments in the process technology previously employed at TRIUMF were required to create the HRGCCDs. These developments included a standard chlorobenzene-aided photoresist lift-off process to delineate r.f. magnetron sputtered Cr:SiO islands and a dry etch process to create
interconnect vias. Two process runs of HRGCCDs, with differing layer parameters, were fabricated and evaluated at 4.33 MHz and at 50 MHz. The HRGCCDs tested at 50 MHz exhibited a charge transfer efficiency in excess of 0.99, and a dynamic range in excess of 50 dB with a linear response over a 40 dB input signal range.
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All energies are referenced to the Fermi level energy unless otherwise stated.

A - area of a Schottky-barrier contact pad
B - insertion loss
B_0 - insertion loss normalization factor
C_t - capacitance of a Schottky-barrier diode
d - thickness of the undoped AlGaAs layer
D - 2-dimensional density of states
E_0 - first energy level in the 2-dimensional electron gas, referenced to the bottom of the potential well at the AlGaAs/GaAs interface
E_1 - second energy level in the 2-dimensional electron gas, referenced to the bottom of the potential well at the AlGaAs/GaAs interface
E_c - conduction band energy
E_a - conduction band energy at the doped/undoped AlGaAs interface, referenced to the bottom of the potential well at the GaAs/AlGaAs interface
E_f - Fermi level energy
E_{fi} - Fermi level energy, referenced to the bottom of the potential well at the AlGaAs/GaAs interface
E_g - band gap energy
E_{min} - minimum conduction band energy
E_v - valence band energy
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_q$</td>
<td>conduction band energy at an arbitrary point along the $x$-axis</td>
</tr>
<tr>
<td>$f$</td>
<td>input signal frequency</td>
</tr>
<tr>
<td>$f_c$</td>
<td>operating frequency of the HRGCCDs</td>
</tr>
<tr>
<td>$F_s$</td>
<td>surface electric field</td>
</tr>
<tr>
<td>$i$</td>
<td>integer index</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann’s constant</td>
</tr>
<tr>
<td>$m^*$</td>
<td>effective mass of electrons in GaAs</td>
</tr>
<tr>
<td>$n_d$</td>
<td>density of ionized donors in the depletion region underneath a Schottky-barrier electrode</td>
</tr>
<tr>
<td>$n_f$</td>
<td>density of free carriers in the doped AlGaAs</td>
</tr>
<tr>
<td>$n_m$</td>
<td>maximum density of carriers in the 2-dimensional electron gas</td>
</tr>
<tr>
<td>$n_s$</td>
<td>density of carriers in the 2-dimensional electron gas</td>
</tr>
<tr>
<td>$N_e$</td>
<td>effective density of states in the conduction band</td>
</tr>
<tr>
<td>$N_d$</td>
<td>density of donor impurities in the doped AlGaAs</td>
</tr>
<tr>
<td>$N_{d^+}$</td>
<td>density of ionized donor impurities in the doped AlGaAs</td>
</tr>
<tr>
<td>$N_i$</td>
<td>number of single electrode transfers in the HRGCCD</td>
</tr>
<tr>
<td>$q$</td>
<td>electronic charge</td>
</tr>
<tr>
<td>$Q$</td>
<td>total charge</td>
</tr>
<tr>
<td>$t$</td>
<td>thickness of the doped AlGaAs layer</td>
</tr>
<tr>
<td>$T$</td>
<td>absolute temperature</td>
</tr>
<tr>
<td>$V_g$</td>
<td>applied bias to a Schottky-barrier electrode</td>
</tr>
<tr>
<td>$V_{off}$</td>
<td>pinch-off voltage of the HRGCCD</td>
</tr>
<tr>
<td>$V_t$</td>
<td>thermal voltage, $kT$</td>
</tr>
</tbody>
</table>
\( x \) - depth in the HRGCCD

\( x_{\text{min}} \) - location of the minimum in the conduction band energy

\( y \) - a dummy variable for integration

\( \gamma_0, \gamma_1 \) - Shubnikov-de Haas constants

\( \Delta E_c \) - conduction band discontinuity

\( \Delta E_d \) - donor level energy referenced from the conduction band energy

\( \Delta E_v \) - valence band discontinuity

\( \varepsilon_{\text{AlGaAs}} \) - permittivity of AlGaAs

\( \varepsilon_{\text{GaAs}} \) - permittivity of GaAs

\( \eta \) - efficiency

\( \xi \) - an arbitrary point along the x-axis

\( \rho \) - space charge density

\( \phi_b \) - Schottky-barrier height

\( \chi_{\text{AlGaAs}} \) - electron affinity of AlGaAs

\( \chi_{\text{GaAs}} \) - electron affinity of GaAs

\( \hbar \) - reduced Planck's constant
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1. INTRODUCTION

The gallium arsenide charge-coupled device (GaAs CCD) was originally proposed by Schuermeyer et al. in 1972[1], and consists of an array of metal-GaAs Schottky-barrier electrodes separated by small, dielectric filled gaps. This structure is known as a capacitive-gate CCD (CGCCD). A GaAs CGCCD was first demonstrated by Kellner et al. in 1977[2], with a charge transfer efficiency (CTE) of 0.98 at frequencies between 5 kHz and 1 MHz[2]. Since then, attempts have been made to increase the CTE and the operating frequency of a GaAs CGCCD for the purpose of ultra-high frequency signal processing[3,4]. In 1981, Cohen et al.[3] demonstrated the operation of a GaAs CGCCD at a frequency of 1 GHz with a CTE of 0.994, and in 1984, Sovero et al.[5] reported a GaAs CGCCD with a CTE of 0.999 at 1 GHz.

Potential wells, also termed energy troughs, may form within the GaAs CGCCD active layer, underneath the gaps, due to a non-monotonically varying potential along the dielectric/GaAs interface[6,7]. The energy troughs capture a small quantity of charge from a passing charge packet. The trapped charge may be released from the energy troughs after a period of time or may be lost through recombination, resulting in greater charge transfer inefficiency and subsequent CCD performance loss[7,8].
A schematic illustration of a portion of the transport region of a GaAs CGCCD is shown in Figure 1.1(a). The GaAs CGCCD active layer thickness is typically greater than 1 μm and the active layer doping density is usually between $10^{15}$ to $10^{16}$ cm$^{-3}$[9]. The electrodes are separated by gaps approximately 1 μm long. The transport electrodes are identified as $\Phi_1$, $\Phi_1A$, $\Phi_2$, and $\Phi_2A$. A non-monotonic potential distribution along the channel of a GaAs CGCCD, in single phase operation, is shown in Figures 1.1(b) and 1.1(c), to demonstrate charge trapping by energy troughs. Initially, a charge packet is shown to reside underneath the $\Phi_1A$ electrode when the voltage signals applied to the transport electrodes are such that $\Phi_1A > \Phi_1 \geq \Phi_2A > \Phi_2$, as displayed in Figure 1.1(b). In Figure 1.1(c), the signals applied to the electrodes change, from their initial values to $\Phi_2A > \Phi_2 > \Phi_1A > \Phi_1$, by the application of a clock pulse to the $\Phi_1$ and $\Phi_1A$ electrodes. The charge packet will be transferred to the potential well formed underneath the $\Phi_2A$ electrode, as shown in Figure 1.1(c). Some of the charge from the charge packet is trapped in the energy troughs formed between the $\Phi_1$ and $\Phi_1A$, and the $\Phi_1A$ and $\Phi_2$ electrodes resulting in decreased charge transfer efficiency.

Deyhimy et al.[7] developed a two-dimensional electrical analogue of a GaAs CGCCD to investigate the relationship between the spacing of the CGCCD Schottky-barrier electrodes and the relative magnitude of the energy trough. They found that the relative magnitude of the energy trough was reduced as the gap length was reduced[7]. Colbeth et al.[9] showed that the magnitude of the energy troughs in a GaAs CGCCD is proportional to the active layer doping density and inversely proportional to the active layer thickness[9].
Figure 1.1: The potential distribution along the channel of a GaAs CGCCD.

They found that a GaAs CGCCD with an electrode spacing of 1 μm, an active layer doping density of 7.0×10^{15} cm^{-3}, and an active layer thickness of 0.90 μm possessed a CTE in excess of 0.999[9]. Colbeth et al. demonstrated that the doping density of the active layer of a GaAs CGCCD should be between 10^{15} - 10^{16} cm^{-3}, for an active layer thickness ranging from 0.35 μm to 0.90 μm, to achieve CTEs greater than 0.99[9]. Metal-semiconductor field-effect
transistors (MESFETs), which are monolithically integrated with the GaAs CGCCD, typically require thin, highly doped active layers for optimal performance\cite{10,11,12}. Since the GaAs CGCCD requires relatively low doping levels and a thick active layer in comparison to conventional GaAs MESFETs, the performance of the on-chip MESFETs will be compromised\cite{13}.

Song et al.\cite{14} proposed a recessed gap GaAs CGCCD in 1989. They found that by recessing the gaps, the effect of energy troughs on GaAs CGCCD performance is reduced and the compatibility of the GaAs CGCCD with on-chip MESFETs is increased, because a recessed gap GaAs CGCCD can be fabricated on thin, highly doped active layers\cite{14}. Song et al.\cite{14} fabricated recessed gap GaAs CGCCDs with a GaAs active layer thickness between 0.135 and 0.285 \(\mu\)m, a GaAs active layer doping density between 1.2 and 2.0\(\times10^{17}\) cm\(^{-3}\), and recessed gaps between 0.05 and 0.13 \(\mu\)m deep. These devices were operated at a clock frequency of 12 MHz, demonstrating CTEs approaching 0.9999\cite{14}. Difficulties in fabrication of recessed gaps, uniformity of the etch across the wafer, and reduced fringing fields in the gap region were identified as the main problems with this design\cite{14}.

An increased compatibility with on-chip MESFETs and an elimination of energy troughs is obtained from the GaAs resistive-gate CCD (RGCCD). The first GaAs RGCCD was demonstrated by Higgins et al. in 1982\cite{10}. In 1984, Sovero et al.\cite{15} operated a GaAs RGCCD at frequencies ranging from 1 MHz to 4 GHz with a CTE of 0.99 at 2.5 GHz\cite{15}.
The GaAs RGCCD has short transport electrodes separated by wide gaps. The electrodes are usually placed on top of a thin layer of conductive cermet material that covers the surface of the GaAs active layer in the transport region of the GaAs RGCCD[16,17]. The cermet material used for a GaAs RGCCD is a metal-insulator composite[10,16,18]. A cermet film can be modelled as a distributed resistance/capacitance structure[19]. LeNoble et al.[18] developed a transmission line model of the cermet/GaAs interface to investigate the surface potential variation in the gaps of a GaAs RGCCD. They showed that the surface potential distribution in the gaps of a GaAs RGCCD is monotonic for all frequencies. The formation of energy troughs between the electrodes is suppressed because the surface potential variation is monotonic. Due to the suppression of energy troughs in GaAs RGCCDs, these devices can be fabricated on thin, highly doped active layers enabling compatibility with a MESFET process[10].

A schematic illustration of a portion of the transport region of a GaAs RGCCD is shown in Figure 1.2(a). The GaAs active layer thickness is typically less than 1 μm, and the active layer doping density is usually $10^{17}$ cm$^{-3}$[9,16,18]. The resistive-gate electrodes are separated by gaps greater than 1 μm long[9,18]. A monotonic potential distribution along the channel of a GaAs RGCCD, in single phase operation, is shown in Figures 1.2(b) and 1.2(c), to demonstrate the suppression of energy troughs. Initially, a charge packet is shown to reside underneath the $\Phi_{1A}$ electrode when the voltage signals applied to the transport electrodes are such that $\Phi_{1A} > \Phi_{1} \geq \Phi_{2A} > \Phi_{2}$, as displayed in Figure 1.2(b). In Figure 1.2(c), the signals applied to the electrodes change, from their initial values to $\Phi_{2A} > \Phi_{2}$.
> Φ1A > Φ1, by the application of a clock pulse to the Φ1 and Φ1A electrodes. The charge packet will be transferred to the potential well formed underneath the Φ2A electrode, as shown in Figure 1.1(c). The monotonic surface potential variation in the gaps suppresses the formation of energy troughs, resulting in low charge loss.

![Diagram](image)

Figure 1.2: The potential distribution along the channel of a GaAs RGCCD.
Improvements in AlGaAs/GaAs heterojunction fabrication technology have enabled the realization of heterojunction AlGaAs/GaAs CCDs. These devices have two significant operational advantages over GaAs CCDs. The main advantages are: increased operating speed and increased dynamic range. The increased device speed is a result of two primary factors. Heterojunction AlGaAs/GaAs CCDs can be monolithically integrated with high electron mobility transistors (HEMTs). HEMTs have superior transport characteristics compared to conventional MESFETs due to higher electron mobility and higher electron velocity in AlGaAs/GaAs heterojunctions than in GaAs homojunctions[20,21]. The increased dynamic range of a heterojunction AlGaAs/GaAs CCD is a result of higher carrier densities. The carrier density in an AlGaAs/GaAs CCD can be up to 2.0\times10^{12} \text{ cm}^{-2}[22], while the highest carrier density in a GaAs CCD is approximately 2.0\times10^{11} \text{ cm}^{-2}[9,18].

Liu et al.[23] fabricated the first heterojunction CGCCD (HCGCCD) in 1979. The device used a layer of Al_{0.22}Ga_{0.78}As placed on top of a semi-insulating GaAs substrate. Milano et al.[24,25] created a modified AlGaAs/GaAs HCGCCD in 1982, that exhibited a CTE of 0.98 at 6 kHz and 0.9 at 100 kHz.

The extension of the GaAs RGCCD to heterojunction materials was suggested by Milano et al. in 1983[25], but not realized. Song et al.[26] demonstrated the operation of the first AlGaAs/GaAs heterojunction RGCCD (HRGCCD) in 1991. The device exhibited a CTE of 0.999 for frequencies between 10 MHz and 1 GHz[26].
Figure 1.3(a) displays a schematic representation of a HRGCCD. The input and output ohmic contacts of the HRGCCD are labelled I/O and O/P, and the Schottky-barrier electrodes, which control charge injection and charge extraction in the HRGCCD, are labelled G1, G2, and G3. The on-chip HEMT circuitry which senses the presence of a charge packet at the O/P node of the HRGCCD is comprised of a reset HEMT and a HEMT amplifier. R/G is the gate electrode and R/D is the drain electrode of the reset HEMT. B/D is the drain electrode, B/S is the source electrode, and B/O is the output electrode of the HEMT amplifier. A schematic diagram of the on-chip HEMT circuit is given in Figure 1.3(b).

The different CCDs described in this chapter are summarized in Table I. The active layer thickness, the active layer charge density, the electrode spacing and the on-chip transistor technology are listed for each of the CCDs.

<table>
<thead>
<tr>
<th>Device</th>
<th>Thickness</th>
<th>Charge Density</th>
<th>Electrode Spacing</th>
<th>Transistor technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>CGCCD</td>
<td>&gt; 1 µm</td>
<td>1 (-3\times10^{10}) cm(^{-2})</td>
<td>≤ 1 µm</td>
<td>MESFET</td>
</tr>
<tr>
<td>recessed gap CGCCD</td>
<td>&lt; 0.3 µm</td>
<td>2\times10^{11} cm(^{-2})</td>
<td>≤ 1 µm</td>
<td>MESFET</td>
</tr>
<tr>
<td>RGCCD</td>
<td>&lt; 1 µm</td>
<td>2\times10^{11} cm(^{-2})</td>
<td>&gt; 1 µm</td>
<td>MESFET</td>
</tr>
<tr>
<td>HCGCCD</td>
<td>&lt; 0.2 µm</td>
<td>10^{12} cm(^{-2})</td>
<td>≤ 1 µm</td>
<td>HEMT</td>
</tr>
<tr>
<td>HRGCCD</td>
<td>&lt; 0.2 µm</td>
<td>10^{12} cm(^{-2})</td>
<td>&gt; 1 µm</td>
<td>HEMT</td>
</tr>
</tbody>
</table>

Table I: A summary of different GaAs based CCDs.
Figure 1.3: A schematic diagram of, (a) a HRG CCD, (b) the on-chip HEMT circuit.
There are a variety of applications that can employ HRGCCDs. These applications include: electrooptical signal processing for spectrum analyzers[27], optical matrix multipliers[28,29], video signal processing[30,31,32], optical imaging systems[9,33,34], and beam forming systems for radar and sonar systems[35].

A 128 pixel, single phase HRGCCD was fabricated at the Tri-University Meson Facility (TRIUMF, Vancouver, Canada) for application in a 500 MHz transient digitizer system[36,37,38]. This system will become part of the rare kaon decay spectrometer for Experiment number 787 at Brookhaven National Laboratories (BNL, New York, U.S.A)[39,40,41].

The design, fabrication, and evaluation of HRGCCDs fabricated at TRIUMF will be presented. A description of the AlGaAs/GaAs heterojunction and the design of a HRGCCD will be given in Chapter 2. A self-consistent solution of Schrodinger’s and Poisson’s equations aided in the design of the HRGCCD. The technique used to inject and sense charge in the HRGCCD, and the clocking scheme applied to the transport electrodes of the HRGCCD, will also be detailed in Chapter 2. In chapter 3, the fabrication of a HRGCCD and the modifications of the process technology previously employed at TRIUMF will be presented. The modifications included: the development of a chlorobenzene-aided photoresist lift-off process to reduce the formation of wings in a r.f. magnetron sputtered cermet film, and the development of a reactive ion etch process to obtain a high degree of etch anisotropy for the purpose of forming interconnect vias.
Device performance measurements and tests will be described in Chapter 4. The tests were used to characterize the HRGCCD die, and the measurements were used to determine the CTE, the dynamic range, and the linearity of the response of the devices. A summary and considerations for future work will be presented in Chapter 5.
2. DEVICE THEORY AND OPERATION

A quantum mechanical model will be developed in section 2.1. to calculate the carrier density in the triangular, quantum mechanical, potential well. In section 2.2, the quantum mechanical model will be coupled to a solution of Poisson's equation in the bulk AlGaAs to determine the capacitance-voltage (C-V) profile of a Schottky-barrier. The theoretical C-V profile will be compared to measured C-V profiles of Schottky-barrier diodes fabricated with the HRGCCDs. The injection, transport and detection of charge in a HRGCCD will be described in section 2.3.

2.1. AlGaAs/GaAs Heterojunctions

A triangular, quantum mechanical, potential well is formed when a doped AlGaAs layer is grown on top of an undoped GaAs layer, due to the different electron affinities of GaAs and AlGaAs[22]. The well extends from the AlGaAs/GaAs interface into the undoped GaAs layer. The energy band diagram of an n-AlGaAs layer and an undoped GaAs layer is displayed in Figure 2.1, $E_c$ is the conduction band energy, $E_v$ is the valence band energy, $E_f$ is the Fermi level energy, $E_{fl}$ is the Fermi level energy referenced to the bottom of the potential well, $E_g$ is the energy band gap, $\Delta E_c$ is the conduction band discontinuity, $\Delta E_v$ is the valence band discontinuity, $\chi_{AlGaAs}$ is the electron affinity of AlGaAs, and $\chi_{GaAs}$ is the electron affinity of GaAs.
Free electrons in the doped AlGaAs layer diffuse into the lower energy GaAs layer and become trapped in the potential well. Electron motion in the well is quantized in the z-direction, defined in Figure 2.1, because the de Broglie wavelength of the electrons in the well is larger than the width of the well[22,42]. The quantization of electron motion results in the formation of a two-dimensional electron gas (2DEG) within the potential well. The existence of a 2DEG at the AlGaAs/GaAs interface has been experimentally verified using Shubnikov-de Haas magnetoresistance oscillation measurements, and cyclotron resonance

Figure 2.1: The energy band diagram of an n-AlGaAs layer and an undoped GaAs layer; (a) not in contact, with the vacuum level chosen as the point of reference, (b) in contact, under zero bias conditions.
Stern et al. [44] have calculated the discrete energy levels in the 2DEG by solving Schrodinger's wave equation for a triangular potential well. The energy levels are given by

$$E_i = \left[ \frac{\hbar^2}{2m^*} \right]^{1/3} \left[ \frac{3\pi}{2} q F_s (i + \frac{3}{4}) \right]^{2/3} \quad i = 0,1,2,... \quad (1)$$

Here, $\hbar$ is the reduced Planck constant, $m^*$ is the effective mass of the electrons in GaAs, and $F_s$ is the surface electric field. $F_s$ is related to the carrier density ($n_s$) in the 2DEG by Gauss's law [22]

$$\epsilon_{GaAs} F_s = q n_s \quad (2)$$

where $\epsilon_{GaAs}$ is the permittivity of GaAs. By substituting the surface electric field, from equation (2) into equation (1), the energy levels in the 2DEG can be written as

$$E_i = \gamma_i n_s^{2/3} \quad i = 0,1,2,... \quad (3)$$

The Shubnikov-de Haas constants, $\gamma_0$ and $\gamma_1$, have been approximated by Linh et al. [45] to be $1.16 \times 10^{-9} \text{ eV} \cdot \text{cm}^{4/3}$ and $1.49 \times 10^{-9} \text{ eV} \cdot \text{cm}^{4/3}$ respectively.
The carrier density in the 2DEG can be expressed as

\[ n_s = D \int_{E_0}^{E_1} \frac{dE}{1 + e^{\frac{q(E-E_{fl})}{kT}}} + 2D \int_{E_1}^{\infty} \frac{dE}{1 + e^{\frac{q(E-E_{fl})}{kT}}} \]  (4)

using Fermi-Dirac statistics and assuming that only the first two energy levels in the potential well are populated with electrons. Here, \( E_{fl} \) is the Fermi level energy referenced to the bottom of the potential well, \( k \) is Boltzmann’s constant, \( T \) is absolute temperature, and \( D \) is the two-dimensional density of states of the electron gas which is

\[ D = \frac{q m^*}{\pi \hbar^2} = 3.24 \cdot 10^{13} \text{ cm}^{-2} \text{ V}^{-1} \]  (5)

Applying the identity

\[ \int \frac{dy}{1 + e^y} = -\ln(1 + e^{-y}) \]  (6)

to equation (4), \( n_s \) can be written as

\[ n_s = D \frac{kT}{q} \ln \left[ \left( 1 + e^{\frac{q(E_{fl}-E_0)}{kT}} \right) \left( 1 + e^{\frac{q(E_{fl}-E_1)}{kT}} \right) \right] \]  (7)

Substituting \( E_0 \) and \( E_1 \) from equation (3) into equation (7) yields

\[ n_s = D \frac{kT}{q} \ln \left[ \left( 1 + e^{\frac{q(E_{fl}-\gamma_0 n_s^{2/3})}{kT}} \right) \left( 1 + e^{\frac{q(E_{fl}-\gamma_1 n_s^{2/3})}{kT}} \right) \right] \]  (8)

This equation establishes a relationship between \( E_{fl} \) and \( n_s \) which will be used in the
development of a theoretical model of the C-V profiles of Schottky-barrier diodes fabricated with the HRGCCDs.

2.2. Design of the HRGCCD's Active Layers

The design of the active layers for the HRGCCDs and the development of a theoretical model to determine the C-V profile of a Schottky-barrier diode is presented in this section. The theoretical C-V model was developed by solving Poisson’s equation in the bulk AlGaAs, to find the conduction band energy and the carrier density as a function of the bias applied to a gate electrode, and coupling this solution to the equation for the carrier density in the 2DEG, equation (8), developed in the previous section. The HRGCCDs consist of, from bottom to top: an undoped, liquid-encapsulated Czochralski grown, semi-insulating <100> GaAs substrate, a 1 μm undoped GaAs buffer layer, a 40 Å undoped Al$_{0.3}$Ga$_{0.7}$As spacer layer, a uniformly doped n-Al$_{0.3}$Ga$_{0.7}$As active layer designed to produce a pinch-off voltage of -1.4 V, and a 100 Å, 1×10$^{18}$ cm$^{-3}$, uniformly doped n$^+$-GaAs cap layer.

The 100 Å GaAs cap layer is used to aid in the formation of ohmic contacts for the HRGCCD. This layer is removed after the ohmic contacts have been formed and therefore will not be considered in the solution of Poisson’s equation.
An undoped AlGaAs spacer layer is commonly placed in between the doped AlGaAs and the GaAs buffer layer to spatially separate the impurities in the doped AlGaAs layer from the 2DEG. This layer reduces impurity scattering of electrons in the 2DEG[46], and lessens the probability of electron tunnelling from the 2DEG to the doped AlGaAs layer. Shur found that the optimal spacer layer thickness is between 40 and 100 Å[46].

The thickness of the uniformly doped n-Al_{0.3}Ga_{0.7}As layer was calculated to produce a pinch-off voltage ($V_{\text{off}}$) of -1.4 V for different active layer doping densities. $V_{\text{off}}$ can be found from the following relationship[47]

$$V_{\text{off}} = \phi_b - \frac{\Delta E_c}{q} - \frac{qN_d t^2}{2\varepsilon_{\text{AlGaAs}}}$$

(9)

where $\phi_b$ is the Schottky-barrier height, $N_d$ is the doping density of the n-Al_{0.3}Ga_{0.7}As layer, $t$ is the thickness of the n-Al_{0.3}Ga_{0.7}As layer, and $\varepsilon_{\text{AlGaAs}}$ is the permittivity of Al_{0.3}Ga_{0.7}As. The terms $\phi_b$, $\Delta E_c$, and $\varepsilon_{\text{AlGaAs}}$ were taken to be 0.7 V, 0.241 eV, and 1.06•10^{-12} F/cm²[48], respectively, in the calculations. The n-Al_{0.3}Ga_{0.7}As layer parameters for the two HRGCCD runs, A07 and A08 described in this work, are summarized in Table II. The Schottky-barrier height was determined to be 0.85 volts for the A07 devices and 0.92 volts for the A08 devices by using the Richardson-Dushman equation[49,50] for charge transport across a Schottky-barrier junction and neglecting series and contact resistances.
<table>
<thead>
<tr>
<th>Process Run</th>
<th>Layer Thickness (Å)</th>
<th>Doping Density (cm$^{-3}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A08</td>
<td>1100</td>
<td>$2 \times 10^{17}$</td>
</tr>
<tr>
<td>A07</td>
<td>800</td>
<td>$4 \times 10^{17}$</td>
</tr>
</tbody>
</table>

Table II: The n-$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer parameters for the HRGCCDs.

Delagebeaudéuf and Linh modelled the transport characteristics of an AlGaAs/GaAs heterojunction[45]. Their model assumed that all of the donor atoms in the doped AlGaAs layer were ionized and free electrons did not exist in the doped AlGaAs layer. Lee et al.[51] showed that these assumptions are invalid. They produced a model of an AlGaAs/GaAs heterojunction which took into account the incomplete ionization of electrons in the doped AlGaAs layer and the existence of free electrons in the doped AlGaAs layer. However, in their approach the carrier density in equation (8) was linearized with respect to the Fermi level energy. Their model does not accurately predict the experimentally observed capacitance-voltage characteristics of a Schottky-barrier diode when the applied bias approaches zero[52,53]. Eskandarian[54] developed a mixed quantum mechanical and classical model of the transport characteristics of an AlGaAs/GaAs heterojunction which models the experimentally observed capacitance-voltage characteristics of a Schottky-barrier diode reasonably well over a wide range of applied biases. This model couples the quantum mechanical model of the AlGaAs/GaAs interface developed by Stern et al.[44] to a solution of Poisson’s equation in the AlGaAs layers. Eskandarian’s model is used in this work to determine the density of electrons in a HRGCCD as a function of the bias applied to a Schottky-barrier electrode.
The one-dimensional Poisson equation in the bulk AlGaAs is

$$\frac{d^2 (E_c - E_p)}{dx^2} = \frac{\rho}{\varepsilon_{AlGaAs}} = \frac{q(N_d^+ - n_i)}{\varepsilon_{AlGaAs}}$$  \hspace{1cm} (10)

where $\rho$ is the space charge density in the AlGaAs layers, $N_d^+$ is the ionized donor density in the doped AlGaAs layer, $n_i$ is the free electron density in the doped AlGaAs layer, and $x$ refers to depth in the HRGCCD, as shown in Figure 2.2. The density of ionized donors in AlGaAs is given by[54]

$$N_d^+ = \frac{N_d}{1 + 2e \left(\frac{E_c - E_f - \Delta E_d}{kT}\right)}$$  \hspace{1cm} (11)

through the application of Fermi-Dirac statistics and assuming that there is only one donor level in Al$_{0.3}$Ga$_{0.7}$As, 0.006 eV below the conduction band edge[55]. This assumption is valid for an Al content in AlGaAs of less than 0.22[55]. For Al contents in excess of 0.22, a second donor level exists between 0.05 and 0.100 eV below the conduction band edge[55]. This second donor level was neglected in this work to simplify the solution of Poisson’s equation. In equation (11), $E_c$ is the conduction band energy referenced to the Fermi level energy $E_f$, and $\Delta E_d$ is the donor level energy referenced from the conduction band energy. A closed form approximation for $n_i$ is[56]

$$n_i = \frac{4N_c}{\left(E_c - E_p\right)} \frac{(\varepsilon_{AlGaAs})}{1 + 4e \frac{\left(E_c - E_p\right)}{kT}}$$  \hspace{1cm} (12)
where \( N_c \) is the effective density of states in the conduction band of AlGaAs and is taken to be \( 6.988 \times 10^{17} \, \text{cm}^{-3} \)[57].

Figure 2.2: The energy band diagram of a HRGCCD.
Equation (10) can be integrated analytically by multiplying both sides of the equation by
\[
2 \left( \frac{d(E_c - E_p)}{dx} \right)
\]
and integrating with respect to \(x\) from the undoped AlGaAs/GaAs interface to a point \((\xi)\) in the doped AlGaAs layer
\[
2 \int_{-d}^{\xi} \frac{d^2(E_c - E_p)}{dx^2} \frac{d(E_c - E_p)}{dx} dx = \int_{E_c}^{E_{\xi}} \frac{2\rho}{e_{AlGaAs}} d(E_c - E_p) + \int_{E_{cs}}^{E_{\xi}} \frac{2\rho}{e_{AlGaAs}} d(E_c - E_p). \tag{14}
\]
Here, \(d\) is the thickness of the undoped AlGaAs spacer layer, \(E_{\xi}\) is the conduction band energy at \(x = \xi\), and \(E_{cs}\) is the conduction band energy at the doped/undoped AlGaAs interface
\[
E_{cs} = \Delta E_c - E_f - \frac{q_n d}{e_{AlGaAs}} . \tag{15}
\]
Since the doping density of the undoped AlGaAs layer is small in comparison to the doped AlGaAs layer, the electric field at the undoped/doped AlGaAs interface is approximately the same as the electric field at the undoped AlGaAs/GaAs interface and is given by[54]
\[
\int_{\Delta E_c - E_f}^{E_c} \frac{2\rho}{e_{AlGaAs}} d(E_c - E_p) = \left[ \frac{q_n d}{e_{AlGaAs}} \right]^2 . \tag{16}
\]
Substituting equations (11) and (12) into equation (10) and integrating with respect to \(x\) yields the following equation

21
The conduction band energy \((E_c-E_f)\) in the bulk AlGaAs is found as a function of the 2DEG carrier density \(n_s\). When charge neutrality exists within the bulk AlGaAs \((N_d^+ = n_i)\), the 2DEG carrier density is a maximum[54]. The maximum 2DEG carrier density \(n_m\) is found by calculating the conduction band energy under charge neutrality conditions and substituting the conduction band energy into equation (8). An arbitrary value between 0 and \(n_m\) is chosen for \(n_s\). Equation (8) is used to find \(E_{fi}\) which is substituted into equation (15) to find \(E_m\). The minimum conduction band energy \((E_{min})\) is found by setting the left hand side of equation (17) to zero, substituting \(E_m\) into equation (17) and solving for \((E_c-E_f)\). Equation (17) is rewritten in terms of \(dx\) and numerically integrated to find the location of the minimum \((x_{min})\) in the conduction band energy. Knowledge of the location and value of the minimum in conduction band energy enables the conduction band energy \((\phi_b - V_s)\) at the Schottky-barrier metal/doped AlGaAs interface \((x=t)\) to be found by integrating equation (17) with respect to \(x\) from \(x=x_{min}\) to \(x=t\) and solving for \((E_c-E_f)\) at \(x=t\).
The ionized donor density \( n_d \) in the depletion region below a Schottky-barrier gate electrode, is calculated by integrating \( N_d^+ \) with respect to \( x \) from the edge of the depletion region \( (x=x_{\text{min}}) \) to the Schottky-barrier electrode/doped AlGaAs interface \( (x=t) \)

\[
n_d = \int_{x_{\text{min}}}^{t} N_d^+ \, dx
\]

(18)

This equation was integrated numerically by substituting equations (11) and (17) into equation (18). The solution of equation (18) establishes a relationship between \( n_d \) and \( V_g \) which was used to find the theoretical capacitance of the Ti-Pt-Au Schottky-barrier diodes fabricated with the HRGCCDs. The program used to find the conduction band energy and the ionized donor density as a function of the bias applied to a Schottky-barrier gate electrode is given in Appendix A.

The electrons in the 2DEG are screened from the gate electrode by the space charge in the region extending from \( x=0 \) to \( x=x_{\text{min}} \) as a result of charge neutrality

\[
n_s - \int_{0}^{x_{\text{min}}} N_d^+ \, dx = 0
\]

(19)

The charge in the GaAs buffer layer and in the semi-insulating GaAs substrate has been neglected in equation (19). Consequently, the total gate capacitance \( (C_t) \) of a Schottky-barrier diode is
\[ C_f(V_g) = \frac{\partial Q}{\partial V_g} = qA\frac{\partial n_d}{\partial V_g} \]  

(20)

where \( Q \) is the total gate charge of the diode and \( A \) is the gate area taken to be \( 10^{-4} \text{ cm}^2 \).

The theoretical and measured capacitances of the Ti-Pt-Au Schottky-barrier diodes associated with the A07 and A08 process runs are shown in Figure 2.3. The agreement between measurement and theory is reasonable for the A07 and A08 devices except for an apparent voltage displacement between the measured and the theoretical curves for the A08 devices. The displacement is a result of a thinner active layer supplied by the vendor (1000 Å instead of 1100 Å) which has caused the measured C-V profile to shift.
Figure 2.3: The measured and theoretical capacitances of Schottky-barrier diodes from the A07 and A08 process runs.
2.3. Operation of the HRGCCD

For the HRGCCD to operate successfully the following sequence of events must occur: (1) charge injection, (2) charge transport, and (3) charge detection. An analog signal applied to the input of the HRGCCD is transformed into a series of discrete charge packets within the HRGCCD. The charge packets are subsequently transferred through the HRGCCD using a single phase clocking scheme applied to the transport electrodes \( \Phi 1A \), \( \Phi 1A \), \( \Phi A \), and \( \Phi 2A \). The charge packets arriving at the output of the HRGCCD are transformed into analog voltages by the on-chip HEMTs.

The input stage of the HRGCCD consists of an input ohmic contact (I/O) and two Schottky-barrier control electrodes (G1 and G2). G1 is a.c. coupled to the \( \Phi 1 \) clock which varies from -5.0 to 0.0 V, and G2 is held constant at 0.0 V. A schematic representation of the input stage of the HRGCCD, and an illustration of the charge injection process is presented in Figure 2.4. An analog input signal ranging from 0.0 to 0.3 V is applied to the I/O node of the HRGCCD. Charge is injected into the potential well formed underneath the \( \Phi 1A \) electrode when the bias applied to the G1 electrode and the \( \Phi 1 \) clock is 0.0 V, as shown in Figure 2.4(b). When the \( \Phi 1 \) clock swings negatively, the charge under the \( \Phi 1A \) electrode is transferred into the potential well formed underneath the \( \Phi 2A \) electrode, creating a discrete charge packet in the first pixel of the HRGCCD, as displayed in Figure 2.4(c). The magnitude of the charge packet injected into the transport region of the HRGCCD is a function of the analog input signal. The nominal voltages applied to the
input stage of the HRGCCD are listed in Table III, on page 31.

Figure 2.4: (a) The input stage of a HRGCCD. The surface potential distribution when the $\Phi_1$ clock is at: (b) 0.0 V, (c) -4.0 V.

An illustration of the charge transport process is shown in Figure 2.5. The charge packets are transferred from the input stage to the output stage of the HRGCCD by the application of a single phase clock, as shown in Figure 2.5(e). Initially, at time $t=t_0$, a charge packet resides underneath the $\Phi_2A$ electrode when the voltages applied to the transport electrodes are such that $\Phi_2A > \Phi_2 \geq \Phi_1A > \Phi_1$. The discrete charge packet is transferred to the potential well formed underneath the $\Phi_1A$ electrode, at time $t=t_1$. 


Figure 2.5: (a) A portion of the transport region of a HRGCCD. The surface potential distribution at time: (b) $t = t_0$, (c) $t = t_1$, and (d) $t = t_2$. (e) The voltages applied to the transport electrodes.
when the voltages applied to the transport electrodes change from their initial values to \( \Phi_1 A > \Phi_1 \geq \Phi_2 A > \Phi_2 \). The charge packet is transferred to the next \( \Phi_2 A \) electrode, at time \( t = t_2 \), when the voltages applied to the transport electrodes return to their initial values. The nominal voltages applied to the transport electrodes of the HRGCCDs are presented in Table III, on page 31.

The output stage of the HRGCCD consists of a Schottky-barrier control electrode G3, an output ohmic contact O/P, a reset HEMT, and a HEMT amplifier as shown in Figure 2.6. The O/P node is connected to the source contact of a reset HEMT and the input gate of a HEMT amplifier. The O/P node is precharged to the drain voltage of the reset HEMT by applying a positive voltage pulse to the reset gate (R/G) on the rising edge of the \( \Phi_1 \) clock. The pulse turns the reset HEMT on, causing the O/P node to precharge. The reset HEMT is turned off when the reset gate returns to its minimum value, causing the O/P node to float at its precharged value. When a charge packet arrives at the final \( \Phi_2 A \) electrode of the HRGCCD, it passes through the potential well formed underneath the G3 control electrode on the negative transition of the \( \Phi_1 \) clock. The electrons in the charge packet accumulate on the parasitic capacitance \( (C_{O/P}) \) on the O/P node causing a negative voltage displacement to occur at the output node (B/O) of the HEMT amplifier. The voltage at the B/O node contains feedthrough components of the reset gate pulse and the clock, as displayed in Figure 2.6. A summary of the voltages applied to the output stage of the HRGCCD is presented in Table III.
Figure 2.6: A diagram of the output stage of a HRGCCD, and the on-chip HEMTs.
<table>
<thead>
<tr>
<th>Applied Signals</th>
<th>Voltage Level(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O</td>
<td>0.0 to 0.3</td>
</tr>
<tr>
<td>G1</td>
<td>-5.0 to 0.0</td>
</tr>
<tr>
<td>G2</td>
<td>0.0</td>
</tr>
<tr>
<td>Φ1</td>
<td>-5.0 to 0.0</td>
</tr>
<tr>
<td>Φ1A</td>
<td>-4.0 to 1.0</td>
</tr>
<tr>
<td>Φ2</td>
<td>-2.0</td>
</tr>
<tr>
<td>Φ2A</td>
<td>0.0</td>
</tr>
<tr>
<td>G3</td>
<td>0.0</td>
</tr>
<tr>
<td>R/D</td>
<td>5.0</td>
</tr>
<tr>
<td>R/G</td>
<td>0.0 to 3.0</td>
</tr>
<tr>
<td>B/D</td>
<td>12.0</td>
</tr>
<tr>
<td>B/S</td>
<td>0.0</td>
</tr>
</tbody>
</table>

Table III: The signals applied to the HRGCCD and their corresponding voltage levels.
3. DEVICE FABRICATION

The fabrication of the HRGCCD required six mask levels employing a 1.0 micron design rule. The masks provided the patterns for the fabrication of the ohmic contacts, the proton isolation implants, the cermet deposition, the gate and transport electrode metallizations, the interconnect vias, and the second level metallization. Conventional 405 nm contact photolithography was used to transfer the mask patterns to the photoresist on the wafer. An overview of the HRGCCD fabrication procedure is presented in Figure 3.1.

3.1. Ohmic Contact Formation

The formation of the ohmic contacts, to the HRGCCD and the supporting HEMT circuit, was the first step in the HRGCCD fabrication procedure. The wafer was initially cleaned and degreased using a series of solvent solutions which included acetone, trichloroethylene and isopropanol. A nominal 1.1 μm thick film of Hoechst Celanese AZ4110, positive photoresist, was patterned on the wafer using the ohmic contact mask. Ohmic contacts were formed by alloying the deposited...
Figure 3.1: An overview of the HRGCCD fabrication procedure.
metals to the doped GaAs and AlGaAs layers following the photoresist lift-off procedure. The alloy was performed at 395°C for 10 seconds with a Heatpulse 2210 rapid thermal anneal (RTA) system. The doped GaAs cap layer was removed by the developer solution, AZ400K:H₂O (1:4 vol.). The etch rate of GaAs exposed to AZ400K:H₂O was found to be 70 ± 20 Å per minute.

3.2. Device Isolation

Multiple energy proton isolation implants were used to isolate the active region of the HRGCCD[59]. Ion implantation damages the crystal lattice, creating electron trapping centres which renders the damaged regions insulating[59]. Isolation using mesa etching was not employed because the surface profile of the wafer would be non-planar, making subsequent contact photolithography difficult. A nominal 6.2 μm thick film of Hoechst Celanese AZ4620, positive photoresist, was used to protect the active regions of the device during the implantation process. A postbake was performed after the photoresist was developed to further harden the photoresist, providing extra protection of the active regions during the implantation process. Two sequential proton implants of 1) 35 keV and 2) 200 keV, at fluences of 1•10¹³ cm² were used to isolate the active region of the HRGCCD. The photoresist was stripped off in 1-methyl-2-pyrrolidone (1M2P), with the aid of ultrasonic agitation, after the isolation implants were completed.
3.3. Cermet Deposition

A nominal 2.1 μm thick film of Hoechst Celanese AZ4210, positive photoresist, was patterned on the wafer using the cermet mask. The transport region of the HRGCCDs was covered with a nominal 2000 Å Cr:SiO (45:55 at. wt. %) cermet film. A 500 Å Ti:W (30:70 at. wt. %) layer was placed on top of the cermet to provide adhesion and to form an ohmic contact to the gate metal electrodes. The Cr:SiO and Ti:W films were r.f. magnetron sputtered from four inch composite targets at a pressure of 5 mTorr. The unwanted cermet was removed using the photoresist lift-off method in acetone with the aid of ultrasonic agitation.

A chlorobenzene-aided photoresist process was employed to achieve an overhang profile in the AZ4210 photoresist[60]. This process was utilized to reduce the formation of 'wings' in the cermet film. The term 'wings' usually refers to material protruding from the edges of a deposited film, as shown in Figure 3.2(a). In the unaided photoresist lift-off process, a cermet film deposited on photoresist is typically continuous, because the deposition coats the photoresist sidewalls. During the lift-off process, the cermet film coating the sidewalls breaks in an irregular manner resulting in the formation of wings. Subsequent metallizations which are required to step over the irregular cermet edge profile may fail, causing the device to be inoperable. Figure 3.3 illustrates the failure of the metal electrodes to step over a cermet film which has wings. This failure can be avoided by soaking the photoresist covered wafer in chlorobenzene, which causes the removal of low
Figure 3.2: Deposition of the cermet and gate metal using, (a) the unaided, and (b) the chlorobenzene-aided photoresist lift-off process.

molecular weight resin and residual solvents from the upper layers of the photoresist[60]. The action of the developer on these upper layers is retarded, resulting in the formation of an undercut sidewall profile in the photoresist[60], as shown in Figure 3.2(b). In the chlorobenzene-aided photoresist process, the deposited cermet film will typically be discontinuous because the undercut photoresist sidewall profile shadows the deposition.
A chlorobenzene-aided photoresist process was developed for the AZ4210 photoresist. It was found, through experimentation, that a 20 minute, room temperature, chlorobenzene soak following a 30 minute, 70°C softbake produced a suitable overhang profile for the AZ4210 photoresist. The sidewall profiles of AZ4210 photoresist employing the unaided and chlorobenzene-aided photoresist lift-off processes are displayed in Figure 3.4. The photoresist islands are 4 μm wide and the overhang of the chlorobenzene-aided photoresist is between 0.25 and 0.5 μm. Interference fringes can be seen in the sidewall.
profile of the unaided photoresist, as displayed in Figure 3.4(a).

Figure 3.4: A photograph of the sidewall profile of AZ4210, 2.1 μm photoresist employing, (a) the unaided, and (b) the chlorobenzene-aided photoresist lift-off process.
The interference fringes are standing waves patterns in the photoresist caused by diffraction and reflection of the imaging beam used to transfer the mask pattern to the photoresist[61]. Standing wave patterns also cause notches to form in the edges of the photoresist, as displayed in Figure 3.5. Interference fringes and notches are less pronounced in the chlorobenzene-aided photoresist process because the upper layers of the photoresist have been modified[60].

![Figure 3.5: A photograph of the sidewall profile of overexposed AZ4210, 2.1 μm photoresist.](image)

The optimum exposure and develop times of the photoresist were different for the unaided and the chlorobenzene-aided photoresist processes, due to the effect of chlorobenzene on the upper layers of photoresist. The optimum exposure and develop times were found, through experimentation, to be 25 seconds and 130 seconds, respectively, for an imaging wavelength of 405 nm and a power density of 5.0 mW/cm².
3.4. Gate Metal Deposition

The Schottky-barrier gates and transport electrodes were deposited after the cermet islands were formed. A nominal 1.1 \( \mu \)m thick film of AZ4110 was patterned on the wafer using the gate metal mask. The gate metal deposition was accomplished by sequentially e-beam evaporating a nominal 500 Å thick layer of Ti, a 100 Å thick layer of Pt and a 3000 Å thick layer of Au at a pressure of 8\( \cdot 10^{-6} \) Torr. The unwanted metal was removed using the photoresist lift-off method in 1M2P with the aid of ultrasonic agitation. After the lift-off process, a CF\(_4\):O\(_2\) reactive ion etch (RIE) was used to remove the Ti:W in between the transport electrodes.

3.5. Interlayer Dielectric and Via Formation

A 1 \( \mu \)m thick film of Du Pont PYRALIN PI2556 polyimide was used as the interlayer dielectric[62]. The polyimide was imidized in a temperature controlled convection oven. The oven temperature was initially held at 100°C for 15 minutes, it was then ramped up to and held at 250°C for 90 minutes, and subsequently ramped down to a temperature of less than 100°C over a period of an hour. The 250°C maximum temperature of the oven, in this process, was below the 360°C eutectic temperature of the ohmic contacts[63], and the 500°C anneal temperature of the proton isolation implants[64].
The interconnect vias between the first and second level metallization were formed by using a multilevel patterning process. A thin, 500 Å thick layer of Ti was deposited on the polyimide using e-beam evaporation at a pressure of \(8 \times 10^{-6}\) Torr. A 1.1 μm thick photoresist film was subsequently patterned on the Ti layer. The vias were formed by using a three-step reactive ion etch process shown in Figure 3.6.

A CF\(_4\):O\(_2\) etch was used to remove the Ti in the photoresist openings, transferring the via mask in the photoresist to the underlying Ti. The polyimide in the openings of the Ti layer and the photoresist was etched with O\(_2\). Finally, a CF\(_4\):O\(_2\) etch was performed to remove the remaining Ti, completing the formation of the interconnect vias in the polyimide. Figure 3.7 shows a photograph of completed interconnect vias.

A conventional plasma etch chamber, a Technics Planar Etch plasma etching system, was originally used at TRIUMF to form interconnect vias for earlier devices. It was found that greater etch anisotropy was required to minimize lateral etching of the 512, 4 μm square vias needed for the HRGCCDs. To accomplish this a reactive ion etching process was developed using a 13.56 MHz Plasma-Therm 2406 reactive ion etch system. Reactive ion etching offers substantial etch anisotropy since the etch proceeds more rapidly in the direction of the applied electric field[65]. Experiments were done to determine the effect of the flow rates of CF\(_4\) and O\(_2\), the power density, the chamber pressure, duration of the etch, temperature of the substrate holder, and ratios of CF\(_4\) to O\(_2\) on the different RIEs. A summary of the RIE parameters used to fabricate the HRGCCDs is given in Table IV.
Figure 3.6: The three-step reactive ion etch process used to form the interconnect vias.

Legend:
- \(\square\) - PI2556 Polyimide
- \(\square\) - First Level Metal
- \(\square\) - Titanium
- \(\square\) - AZ4110 Photoresist
Figure 3.7: A photograph of completed interconnect vias. The vias are approximately 4 \( \mu \text{m} \) square separated by a gap approximately 4 \( \mu \text{m} \) long.

<table>
<thead>
<tr>
<th>Plasma Parameters</th>
<th>Settings</th>
</tr>
</thead>
<tbody>
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<td>power density</td>
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</tr>
<tr>
<td>temperature</td>
<td>30°C</td>
</tr>
<tr>
<td>CF(_4) flow rate (CF(_4):O(_2))</td>
<td>100 sccm</td>
</tr>
<tr>
<td>O(_2) flow rate (CF(_4):O(_2))</td>
<td>10 sccm</td>
</tr>
<tr>
<td>O(_2) flow rate (O(_2))</td>
<td>100 sccm</td>
</tr>
<tr>
<td>pressure (CF(_4):O(_2))</td>
<td>150 mTorr</td>
</tr>
<tr>
<td>pressure (O(_2))</td>
<td>50 mTorr</td>
</tr>
<tr>
<td>base pressure</td>
<td>&lt; 2 mTorr</td>
</tr>
</tbody>
</table>

Table IV: The settings used for the CF\(_4\):O\(_2\) and O\(_2\) reactive ion etches.
3.6. Second Level Metallization

The second level metallization was the final step in the HRGCCD fabrication procedure. A 2.1 μm thick film of AZ4210 photoresist was patterned on the wafer using the second level metal mask. The second level metallization was formed by sequentially depositing a nominal 1000 Å thick layer of Ti and a nominal 5000 Å thick layer of Au using e-beam evaporation at a pressure of 8×10^{-6} Torr. The Ti layer was used to provide adhesion between the first and second level layers of Au. The unwanted metal was removed using the photoresist lift-off method in acetone with the aid of ultrasonic agitation.

Photographs of a completed HRGCCD fabricated at TRIUMF are displayed in Figures 3.8, 3.9, 3.10, and 3.11. A photograph of the entire HRGCCD is displayed in Figure 3.8. The active region of the HRGCCD is 50 μm wide by 2584 μm long. The entire HRGCCD die is 950 μm by 3340 μm. A photograph of the input section of the HRGCCD is displayed in Figure 3.9. The I/O contact pad is 20 μm long, the G1 electrode is 2 μm long, the G2 electrode is 10 μm long and the Φ1 electrode is 2 μm long. The separation between I/O and G1 is 2 μm. The G1 to G2 and G2 to Φ1 gaps are both 1 μm long. A portion of the transport region of a HRGCCD is displayed in Figure 3.10. The transport electrodes are 2 μm long and approximately 100 μm wide. The interelectrode gaps are 3 μm long. The output stage of a HRGCCD is displayed in Figure 3.11. The G3 electrode is 2 μm long. All of the on-chip HEMTs employ 2 μm technology. The detailed HRGCCD fabrication procedure is given in Appendix B.
Figure 3.8: A photograph of the entire HRGCCD. The bonding pads are 96 μm square.

Figure 3.9: A photograph of the input section of the HRGCCD.
Figure 3.10: A photograph of a portion of the transport region of a HRGCCD.

Figure 3.11: A photograph of the output section of a HRGCCD.
4. DEVICE CHARACTERIZATION

The HRGCCD die from the A07 and A08 process runs were characterized using automated d.c. and a.c. tests. The operation of a HRGCCD is demonstrated at a frequency of 4.33 MHz. Insertion loss measurements were performed to find the CTE, the dynamic range, and the linearity of the HRGCCD response at an operating frequency of 50 MHz.

The HRGCCD die were d.c. and a.c. probed on an Electroglass 1304X, automated probe station to find the functional devices. These devices were then bonded in a 0.45 inch square, 28 pin, 28LCC package, as shown in Appendix C, and prepared for further evaluation.

A qualitative demonstration of a HRGCCD operating at 4.33 MHz, is shown in Figures 4.1 and 4.2. The input (upper) and output waveforms (lower) are displayed in Figure 4.1. In 128 clock cycles, the charge packet is transferred from the input to the output stage of the HRGCCD resulting in the 30 μS delay between the input and output waveforms. The output waveform shows little dispersion indicating near unity CTE. A detailed illustration of the HRGCCD output waveform is shown in Figure 4.2. The feedthrough of the reset and clock pulses are evident in the output waveform.
Figure 4.1: A photograph of the input and output waveforms of a HRGCCD operated at 4.33 MHz.

Figure 4.2: A photograph of the output waveform of a HRGCCD operated at 4.33 MHz. There are 100 nS per division on the horizontal scale and 200 mV per division on the vertical scale.
The CTE of the HRGCCDs fabricated at TRIUMF was determined using the insertion loss technique[66,67]. A Hewlett Packard HP-8753A network analyzer and a HP-85046 s-parameter test set were used for these measurements. The CTE was calculated by fitting the equation[66],

\[
B = 20 \log \left( B_0 \exp \left[ -N_t (1 - \eta) \left( 1 - \cos \left( \frac{f}{f_c} \right) \right) \right] \right)
\]  

(21)
to the measured insertion loss. A is the insertion loss in decibels, \(B_0\) is a normalization factor, \(N_t\) is the number of single electrode transfers through the HRGCCD (256 for the 128 pixel HRGCCD in single phase operation), \(\eta\) is the charge transfer efficiency, \(f\) is the input signal frequency, and \(f_c\) is the HRGCCD clock frequency. The measurements were performed using an input signal ranging from 300 kHz to 25 MHz and a HRGCCD clock frequency of 50 MHz. The calculated CTE of five HRGCCDs from the A07 and A08 runs are listed in Table V.

<table>
<thead>
<tr>
<th>Process Run</th>
<th>CTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A07</td>
<td>0.998</td>
</tr>
<tr>
<td>A07</td>
<td>0.991</td>
</tr>
<tr>
<td>A07</td>
<td>0.999</td>
</tr>
<tr>
<td>A08</td>
<td>0.995</td>
</tr>
<tr>
<td>A08</td>
<td>0.990</td>
</tr>
</tbody>
</table>

Table V: The charge transfer efficiency of HRGCCDs from runs A07 and A08.
Figure 4.3 displays the measured and theoretically calculated insertion loss, for the HRGCCD from the A07 process run which exhibited a CTE of approximately 0.999. The CTE of this HRGCCD is in agreement with the results previously obtained by Song et al.[26].

![Insertion Loss Measurements](image)

**Figure 4.3:** The measured and theoretically calculated frequency response of a HRGCCD operated at 50 MHz.

The measured dynamic range of the HRGCCD from process run A07 that exhibited a CTE of 0.999, is shown in Figure 4.4. This device exhibited a dynamic range in excess of 50 dB with an essentially linear response over a 40 dB input signal range, as shown in Figure 4.5. The observed deviation from linearity is attributed to the nonlinear relationship between the injected signal charge and the input signal amplitude. This is caused by the voltage dependence of the input capacitance between the control electrodes (G1 and G2).
and the input ohmic contact (I/O)[68].

**Figure 4.4:** The frequency response of a HRGCCD operated at 50 MHz with the input signal attenuated in steps of 10 dB.

**Figure 4.5:** The linearity of the HRGCCD response for a 12.5 MHz input signal.
5. SUMMARY AND PROSPECTS FOR FUTURE WORK

The design, fabrication and evaluation of a 128 pixel, single phase HRGCCD was described in this work, and is summarized in section 5.1. Proposals for the continuing development of these devices are given in section 5.2.

5.1. Summary

The design and operation of a 128 pixel, single phase HRGCCD was explained in Chapter 2. A quantum mechanical model of the triangular potential well formed at an undoped AlGaAs/GaAs interface was developed and coupled to a solution of Poisson’s equation in the bulk AlGaAs to determine the carrier densities in a HRGCCD as a function of the active layer parameters and the applied bias. The carrier densities in the HRGCCD were used to calculate the capacitance-voltage profile of a Schottky-barrier diode fabricated along with the HRGCCD. The theoretical capacitance-voltage profile was compared with measured capacitance-voltage profiles of Schottky-barrier diodes fabricated with the HRGCCDs. The agreement between the measured and theoretically computed capacitance-voltage profiles are reasonable. The difference between measurement and theory for the A08 devices is caused by variations in the active layer thickness of the wafers supplied by the vendor.
The charge injection, transport, and detection processes in a HRGCCD were also
described in Chapter 2. An analog input signal, applied to the input ohmic contact of the
HRGCCD, causes a discrete charge packet to form within the input stage of the HRGCCD.
A single phase clock, applied to the transport electrodes of the HRGCCD, is used to
transfer the charge packet from the input stage to the output stage of the HRGCCD. The
charge packet is sensed at the output stage of the HRGCCD by a HEMT amplifier, which
converts the charge into an analog voltage signal.

The fabrication of the HRGCCD was presented in Chapter 3. Six mask levels,
employing a 1 µm design rule, were used in the fabrication procedure. The mask patterns
were transferred to photoresist placed on the wafer with conventional 405 nm contact
photolithography. The six mask steps in the fabrication procedure consist of; the formation
of Au/Ge-Ni-Au ohmic contacts, the proton isolation implants, the Cr:SiO cermet film
deposition, the Ti-Pt-Au gate metal deposition, the interlayer dielectric and via formation,
and the Ti-Au second level metallization. The development of a chlorobenzene-aided
photoresist process for Hoechst Celanese AZ4210 photoresist, and a three-step reactive ion
etch process to form interconnect vias were also described in this chapter. The
chlorobenzene-aided photoresist process was developed to reduce the formation of wings
in the cermet film. The reactive ion etch process was developed to obtain an anisotropic
and uniform etch across the wafer, enabling the interconnect vias to be precisely formed.
The fabricated HRGCCDs were characterized in Chapter 4. Measurements were performed on packaged HRGCCDs to find the CTE, the dynamic range, and the linearity of the response of the HRGCCDs operated at 50 MHz. The CTE was in excess of 0.99 for all of the devices tested, the dynamic range was in excess of 50 dB, and a linear response over a 40 dB input signal range was obtained.

5.2. Considerations for Future Work

Improvements to the HRGCCDs considered in this work can be obtained by using different active layer profiles and materials. The layer structure of the HRGCCD can be modified to reduce the number of defects in the wafer and to increase the operating speed and dynamic range of the HRGCCDs. Defects in the wafers can be reduced by incorporating a superlattice of alternating AlGaAs and GaAs layers between the substrate and the GaAs buffer layer[69]. Different layer profiles and different materials can be used to increase the operating speed and the dynamic range of HRGCCDs. The carrier densities and the mobility of the HRGCCD can be enhanced by planar doping[17,70] or delta doping[71,72] the doped AlGaAs layer, or using indium phosphide based materials. The conduction band discontinuity of InAlAs/InGaAs is larger than that of AlGaAs/GaAs, resulting in better confinement of the carriers in the 2DEG of a InAlAs/InGaAs/InP system[73,74]. The superior confinement properties of InAlAs/InGaAs/InP systems enable the 2DEG to have higher carrier densities and mobilities than AlGaAs/GaAs systems.
BIBLIOGRAPHY


[26]. J-I. Song, D.V. Rossi, S. Xin, W.I. Wang and E.R. Fossum, A Resistive-Gate Al_{0.3}Ga_{0.7}As/GaAs 2DEG CCD with High Charge Transfer Efficiency at 1 GHz, *IEEE Transactions on Electron Devices*, vol. 38, #4, April 1991, p.930-931.


[73]. Y-C. Pao, C. Nisimoto, M. Riaziat, R. Majidi-Ahy, N.G. Bechtel and J.S. Harris Jr., Impact of Surface Layer on In_{0.52}Al_{0.48}As/In_{0.55}Ga_{0.47}As/InP High Electron Mobility Transistors, *IEEE Electron Device Letters*, vol.11, #7, July 1990, p.312-314.

APPENDIX A: Program Listing for the Carrier Density Calculations

This is the MATHCAD, version 3.1 for Windows, file used to calculate the carrier densities in the HRGCCDs as a function of the bias applied to a Schottky-barrier diode. The carrier densities were found by using a quantum mechanical model of the triangular potential well at the AlGaAs/GaAs interface coupled to a solution of Poisson's equation in the bulk AlGaAs.

All references to equations in this file are directed to the work done by Eskandarian[54].

1. Defining the constants:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>doping density</td>
<td>(Nd := 2 \cdot 10^{17}) cm(^{-3})</td>
</tr>
<tr>
<td>doped AlGaAs layer thickness</td>
<td>(d := 1100 \cdot 10^{-8}) cm</td>
</tr>
<tr>
<td>undoped AlGaAs layer thickness</td>
<td>(t := 40 \cdot 10^{-8}) cm</td>
</tr>
<tr>
<td>Schottky-barrier height</td>
<td>(\Phi_b := .92) V</td>
</tr>
<tr>
<td>permittivity of the AlGaAs</td>
<td>(\varepsilon := 1.06 \cdot 10^{-12}) F/cm</td>
</tr>
<tr>
<td>conduction band discontinuity</td>
<td>(\Delta E_C := 0.28) eV</td>
</tr>
<tr>
<td>donor level energy</td>
<td>(\Delta E_d := 0.006) eV</td>
</tr>
<tr>
<td>electronic charge</td>
<td>(q := 1.602 \cdot 10^{-19}) C</td>
</tr>
<tr>
<td>thermal voltage, kT/q</td>
<td>(V_t := 0.0259) eV</td>
</tr>
<tr>
<td>effective density of states</td>
<td>(N_e := 6.988 \cdot 10^{17}) cm(^{-3})</td>
</tr>
<tr>
<td>two-dimensional density of states</td>
<td>(D := 3.24 \cdot 10^{13}) eV(^{-1})cm(^{-2})</td>
</tr>
<tr>
<td>Shubnikov-de Haas constant</td>
<td>(\gamma_0 := 1.16 \cdot 10^{-9}) eV(\cdot)cm(^{4/3})</td>
</tr>
<tr>
<td>Shubnikov-de Haas constant</td>
<td>(\gamma_1 := 1.49 \cdot 10^{-9}) eV(\cdot)cm(^{4/3})</td>
</tr>
</tbody>
</table>
2. Defining the variables:

All energies are referenced to the Fermi level unless otherwise stated.

- \( E_0 \): the first energy level in the 2DEG referenced to the bottom of the triangular potential well.
- \( E_1 \): the second energy level in the 2DEG referenced to the bottom of the triangular potential well.
- \( E_C \): the conduction band energy.
- \( E_{Cg} \): the conduction band energy at the Schottky metal/AlGaAs interface.
- \( E_{Ct}, E_g, E_{Cgate} \): dummy variables used to find \( E_{Cg} \).
- \( E_{Ci} \): the conduction band energy at the GaAs/AlGaAs interface referenced to the bottom of the triangular potential well.
- \( E_{Cm} \): the minimum conduction band energy in the bulk AlGaAs.
- \( E_{Cm1}, E_{Cm2}, E_m, E_{Croot} \): dummy variables used to find \( E_{Cm} \).
- \( E_{Cs} \): the conduction band energy at the doped/undoped AlGaAs interface.
- \( E_s \): a dummy variable used to find \( E_{Cs} \).
- \( E_{Cmax} \): the conduction band energy at the AlGaAs/GaAs interface when the 2DEG carrier density is a maximum.
- \( E_{Cmax0} \): the conduction band energy at the AlGaAs/GaAs interface, referenced to the bottom of the triangular potential well, when the 2DEG carrier density is a maximum.
- \( F \): a dummy variable for integration.
- \( Q_t \): the charge within the bulk AlGaAs.
- \( n_s \): the carrier density in the 2DEG.
- \( n_b \): the carrier density in the bulk AlGaAs.
- \( x_m \): the distance between the minimum conduction band energy in the bulk AlGaAs and the doped/undoped AlGaAs interface.
- \( \rho \): the space charge density in the bulk AlGaAs.
- \( t \): a dummy variable for integration.
3. Determining the maximum 2DEG carrier density:

The maximum 2DEG carrier density (nm) is found by assuming that the minimum conduction band energy (ECm) is equal to the conduction band energy of the bulk AlGaAs. The conduction band energy of the bulk AlGaAs is obtained by assuming that charge neutrality exists within the bulk AlGaAs. Therefore, Poisson's equation in the bulk AlGaAs can be written as;

\[ \rho = 0 = N_{d^+} - n_f \]

where \( N_{d^+} \) is the ionized donor density and \( n_f \) is the free electron density. By solving Poisson's equation for \( EC_{max} \) the following expression is obtained:

\[ EC_{max} = 0.0417072 \text{ eV} \]

The conduction band energy is assumed to be constant in the bulk AlGaAs therefore, the derivative of the conduction band energy with respect to the depth in the bulk AlGaAs is zero \( (d(\text{EC})/dx = 0) \) and the left hand side of equation (4) is zero. The maximum carrier density in the AlGaAs is found by numerically solving equations (4) and (5) simultaneously.

\[ a := \sqrt{\frac{2 \cdot e \cdot N_d \cdot V_t}{q}} \]

\[ b := 4 \cdot \frac{N_c}{N_d} \]

\[ c := \ln \left( \frac{2 + \exp \left( \frac{EC_{max} - A_{Ed}}{V_t} \right)}{4 + \exp \left( \frac{-EC_{max}}{V_t} \right)} \right)^b \]

An initial guess of the carrier density in the 2DEG (ns) and the conduction band energy (ECmax) is required to solve equations (4) and (5) simultaneously.

\[ ns = 1 \cdot 10^{11} \text{ cm}^{-2} \]  \[ EC_{max} = .2 \text{ eV} \]

Note: the variable \( EC_{max} \) is not the same as \( EC_{max} \).

Given

\[ \ln \left( \frac{1 + \exp \left( \frac{EC_{max} - \gamma_0 \cdot ns}{V_t} \right)}{1 + \exp \left( \frac{EC_{max} - \gamma_1 \cdot ns}{V_t} \right)} \right) \]  \[ = \frac{ns}{V_t \cdot D} \]
ECmax0 + \eta - t - AEC \rightarrow \frac{\exp{\Delta EC - \Delta Ed - ECmax0 - q\eta ns}}{Vt} \cdot \frac{4 + \exp{\frac{ECmax0 + q\eta ns}{\epsilon}}}{Vt} \cdot ns = 0

nm := \text{Find}(ns, ECmax0)

nm = 5.49914583 \cdot 10^{11} \text{ cm}^{-2}

4. Calculating the conduction band energy (Ecs) at the undoped/doped AlGaAs interface for a given 2DEG carrier density (ns)

Ecs is found by subtracting the conduction band energy at the GaAs/AlGaAs interface (ECi) and the linear drop in the conduction band energy across the undoped AlGaAs layer (q*ns*Vt/\epsilon) from the conduction band discontinuity.

Before Ecs can be found ECi must be found as a function of ns. This is done by calculating E0 and E1 as a function of ns and then solving equation (5) numerically to find ECi.

maxi := 100

i := 1.. maxi

EC0 := .5 \text{ eV}

Given

\ln\left(\frac{1 + \exp{\frac{EC0 - E0}{Vt}}}{1 + \exp{\frac{EC0 - E1}{Vt}}}\right) \cdot \frac{ns}{Vt D}

EC0(E0, E1, ns) := \text{Find}(EC0)

ns_{i} := \text{nm} \cdot \text{tanh}\left(\frac{3i}{\text{maxi}}\right)

E0_{i} := \gamma_{0} (ns_{i})^{2}

E1_{i} := \gamma_{1} (ns_{i})^{2}

66
EC_{i} := EC_{0}(E_{0}, E_{1}, n_{s})

EC_s := \Delta E - EC_{i} - \frac{q \cdot n_{s}}{\epsilon}

5. Calculating the minimum conduction band energy (ECm) in the bulk AlGaAs.

ECm is calculated for a given ns by setting the left hand side of equation (4) to zero, and then numerically solving the resultant equation for ECm.

The solution of equation (4) produces two roots ECm1 and ECm2.

Finding the first root of equation (4).

\[
\Gamma_{i} := 2 \cdot \frac{q \cdot N_{d} \cdot V_{t}}{\varepsilon}
\]

EC := 0.5 \text{ eV}

Given

\[
1 + \frac{\Gamma_{i}}{e_{2}} \ln \left[ \frac{2 + \exp \left( \frac{EC - \Delta Ed}{V_{t}} \right)}{1 + \exp \left( \frac{EC}{V_{t}} \right)} \right] = 0
\]

ECmin1(e_{2}, \Gamma_{0}) := \text{Find(EC)}

\[
e_{2} := \left( \frac{q \cdot n_{s}}{\epsilon} \right)^{2}
\]

\[
\Gamma_{0} := 2 + \exp \left( \frac{EC_{s} - \Delta Ed}{V_{t}} \right) \cdot \exp \left( \frac{-EC_{s}}{V_{t}} \right)
\]

ECm1 := ECmin1(e_{2}, \Gamma_{0})

Finding the second root of equation (4).

EC := 0.01 \text{ eV}
Given

\[
1 + \frac{\Gamma_1}{e^2} \left[ \frac{\left( 2 + \exp\left(\frac{EC - \Delta Ed}{Vt}\right)\right) \cdot \left( 4 + \exp\left(\frac{-EC}{Vt}\right)\right)}{\Gamma_0} \right] = 0
\]

\[EC_{min2}(e^2, \Gamma_0, EC_{root1}) := \text{Find}(EC)\]

\[EC_{m2_i} := EC_{min2}(e^2, \Gamma_0, EC_{m1_i})\]

Choosing the correct root.

\[EC_{m_i} := \max\left( EC_{m1_i} \right) \cdot EC_{m2_i} \]

6. Calculating the distance \((x_m)\) from the point in the bulk AlGaAs where the conduction band energy is a minimum to the undoped/doped AlGaAs interface.

Equation (4) is integrated from \(EC_s\) to \(EC_m\) to find \(x_m\).

\[F(EC, e^2, \Gamma_0) := 1 + \frac{\Gamma_1}{e^2} \left[ \frac{\left( 2 + \exp\left(\frac{EC - \Delta Ed}{Vt}\right)\right) \cdot \left( 4 + \exp\left(\frac{-EC}{Vt}\right)\right)}{\Gamma_0} \right] \]

\[x_m := \frac{1}{\sqrt{e^2}} \int_0^{\sqrt{EC_s - EC_{m_i}}} \frac{2 \cdot \tau}{\sqrt{F\left( (EC_{m_i} + \tau^2), e^2, \Gamma_0 \right)}} \, d\tau\]

7. Calculating the applied bias \((V_g)\) for a given \(n_s\):

Equation (4) is used to find the conduction band energy \((EC_g)\) at the Schottky metal/AlGaAs interface.

\[EC_t := 2 \quad \text{eV}\]
Given

\[ \int_{0}^{\sqrt{E_{Ct} - E_{Cm}}} \frac{2 \cdot \tau}{\sqrt{F(E_{Cm} + \tau^2, e2, \Gamma_0)}} \, d\tau - (d - x_m) \sqrt{e2 = 0} \]

\[ E_{C\text{gate}}(E_{Cm}, e2, \Gamma_0, d, x_m) := \text{Find}(E_{Ct}) \]

\[ E_{Cg_i} := E_{C\text{gate}}(E_{Cm_i}, e2_i, \Gamma_0_i, d, x_m_i) \]

\[ V_{g_i} \text{ is found from the relationship:} \]

\[ V_{g_i} := \phi_b - E_{Cg_i} \]

8. Calculating the ionized donor density \( n_b \) caused by the bias \( V_g \) applied to a Schottky-barrier diode.

\[ n_b \] is calculated by integrating the space charge density \( \rho \) in the doped AIGaAs from the edge of the depletion region to the AIGaAs/metal interface.

\[ \rho(E_C) := q \left[ \frac{\exp \left( \frac{E_C - \Delta \Phi d}{V_t} \right)}{2 + \exp \left( \frac{E_C - \Delta \Phi d}{V_t} \right)} \right] \]

\[ Q_t(E_m, E_g, e22, \Gamma_00) := \int_{0}^{\sqrt{E_g - E_m}} \frac{2 \cdot \tau \rho(E_m + \tau^2)}{\sqrt{e22 \cdot F(E_m + \tau^2, e22, \Gamma_00)}} \, d\tau \]

\[ n_{b_i} := \frac{1}{q} \int_{0}^{Q_t(E_{Cm_i}, E_{Cg_i}, e2_i, \Gamma_0_i)} \]
APPENDIX B: The HRGCCD Fabrication Procedure

Ohmic Contact Formation

1. General Clean-up

   3 min. in warm acetone, immersed in an ultrasonic(U/S) bath
   3 min. in hot clean trichloroethylene
   3 min. in hot clean acetone
   3 min. in hot clean iso-propanol
   dry wafer with $N_2$

2. Photolithography

   dispense AZ4110, 1.1 µm, positive photoresist, onto wafer
   spin wafer at 4000 rpm for 20 sec.
   softbake wafer at 90°C for 30 min.
   allow wafer to cool for 3 min.
   align wafer with 'ohmic contact' mask
   expose wafer with 405 nm, 5 mW/cm² light for 16 sec.
   spray develop photoresist using AZ400K:H₂O (1:4), for 90 sec.
   rinse wafer in deionized H₂O for 1 min.

3. Evaporation

   thermal evaporate:
   550 Å of Au-Ge (12% weight Ge)
   at a pressure of 8*10⁻⁶ Torr

   sequentially e-beam evaporate:
   200 Å of Ni
   1500 Å of Au
   at a pressure of 8*10⁻⁶ Torr
4. Photoresist Lift-off and Cleaning

10 min. in hot lift-off acetone
3 min. in hot, new lift-off acetone immersed in an U/S bath
3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean trichloroethylene
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with N₂

5. Inspect pre-RTA current voltage characteristics of the contacts

6. Rapid Thermal Anneal

10 sec. RTA at 395°C in a N₂ ambient

7. Inspect current-voltage characteristics of the contacts

Device Isolation

1. General Clean-up

3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean trichloroethylene
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with N₂

2. Photolithography

dispense AZ4620, 6.2 µm, positive photoresist, onto wafer
spin wafer at 4000 rpm for 20 sec.
softbake wafer at 90°C for 30 min.
allow wafer to cool for 3 min.
align wafer with 'isolation' mask
expose wafer with 405 nm, 5 mW/cm² light for 60 sec.
spray develop photoresist using AZ400K:H₂O (1:4), for 90 sec.
rinse wafer in deionized H₂O for 1 min.
postbake wafer at 120°C for 15 min.
allow wafer to cool for a minimum of 3 min.
3. Isolation Implants

implant $H^+$ atoms at 200 keV, $1 \times 10^{13}$ cm$^{-2}$
implant $H^+$ atoms at 35 keV, $1 \times 10^{13}$ cm$^{-2}$

4. Photoresist stripping and cleaning

15 min. in hot lift-off 1-methyl 2-pyrrolidone (1M2P)
5 min. in hot, new lift-off 1M2P immersed in an U/S bath
5 min. in hot lift-off acetone immersed in an U/S bath
3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean trichloroethylene
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with $N_2$

5. Inspect current-voltage characteristics of isolated and unisolated regions

**Cermet Deposition**

1. General Clean-up

3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean trichloroethylene
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with $N_2$

2. Photolithography

dispense AZ4210, 2.1 μm, positive photoresist, onto wafer
spin wafer at 4000 rpm for 20 sec.
softbake wafer at 70°C for 30 min.
allow wafer to cool for 3 min.
soak wafer in chlorobenzene for 20 min.
dry wafer with $N_2$
align wafer with 'cermet' mask
expose wafer with 405 nm, 5 mW/cm$^2$ light for 25 sec.
spray develop photoresist using AZ400K:H$_2$O (1:4), for 90 sec.
rinse wafer in deionized H$_2$O for 1 min.
dry wafer with $N_2$
3. Sputter

   r.f. magnetron sputter 2000 Å Cr:SiO (45:55 at. wt %)
   set:
   - argon flow rate: 50 sccm
   - base pressure: 5 mTorr
   - input power to target: 200 Watts
   - d.c. target bias: -230 V

   r.f. magnetron sputter 500 Å Ti:W (30:70 at. wt %)
   set:
   - argon flow rate: 50 sccm
   - base pressure: 5 mTorr
   - input power to target: 100 Watts
   - d.c. target bias: -140 V

4. Photoresist stripping and cleaning

   10 min. in hot lift-off acetone
   5 min. in hot, new lift-off acetone immersed in an U/S bath
   3 min. in warm acetone immersed in an U/S bath
   3 min. in hot clean trichloroethylene
   3 min. in hot clean acetone
   3 min. in hot clean iso-propanol
   dry wafer with N₂

5. Measure cermet height and inspect current-voltage and capacitance-voltage characteristics of the cermet diode structures

Gate Metal Deposition

1. General Clean-up

   3 min. in warm acetone immersed in an U/S bath
   3 min. in hot clean trichloroethylene
   3 min. in hot clean acetone
   3 min. in hot clean iso-propanol
   dry wafer with N₂
2. Photolithography

dispense AZ4110, 1.1 μm, positive photoresist, onto wafer
spin wafer at 4000 rpm for 20 sec.
softbake wafer at 90°C for 30 min.
allow wafer to cool for 3 min.
align wafer with 'gate metal' mask
expose wafer with 405 nm, 5 mW/cm² light for 16 sec.
spray develop photoresist using AZ400K:H₂O (1:4), for 90 sec.
rinse wafer in deionized H₂O for 1 min.
dry wafer with N₂

3. Evaporation

sequentially e-beam evaporate:
500 Å of Ti
100 Å of Pt
3000 Å of Au
at a pressure of 8×10⁻⁶ Torr

4. Photoresist Stripping and cleaning

15 min. in hot lift-off 1M2P
5 min. in hot, new lift-off 1M2P in an U/S bath
5 min. in hot lift-off acetone immersed in an U/S bath
3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean trichloroethylene
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with N₂

5. Reactive Ion Etch

precondition plasma chamber with a CF₄:O₂ plasma for 20 min.
reactive ion etch unwanted Ti:W with CF₄:O₂ for 2 min.

set:
CF₄:O₂ flow rate: 100:10 sccm
base pressure < 2 mTorr
pressure: 150 mTorr
power density: 400 mW/cm²
temperature: 30°C
6. Measure cermet height, inspect current-voltage and capacitance-voltage characteristics of FETs and check the quality of the gates with a scanning electron microscope (SEM).

**Interlayer Dielectric and Via Formation**

1. **General Clean-up**
   - 3 min. in warm acetone immersed in an U/S bath
   - 3 min. in hot clean trichloroethylene
   - 3 min. in hot clean acetone
   - 3 min. in hot clean iso-propanol
   - dry wafer with $N_2$

2. **Deposit and cure polyimide**
   - dispense Du Pont PI-2556 polyimide onto wafer
   - spin wafer at 4000 rpm for 60 sec.
   - softbake wafer at 105°C for 15 min. in a forced air oven
   - ramp up and hold the oven temperature at 250°C for 90 min.
   - ramp down the oven temperature to below 100°C
   - allow wafer to cool for 3 min.

3. **Evaporation**
   - e-beam evaporate:
     - 500 Å of Ti
     - at a pressure of $8 \times 10^{-6}$ Torr

4. **Photolithography**
   - dispense AZ4110, 1.1 μm, positive photoresist, onto wafer
   - spin wafer at 4000 rpm for 20 sec.
   - softbake wafer at 90°C for 30 min.
   - allow wafer to cool for a minimum of 3 min.
   - align wafer with 'interlayer dielectric' mask
   - expose wafer with 405 nm, 5 mW/cm² light for 16 sec.
   - spray develop photoresist using AZ400K:H₂O (1:4), for 90 sec.
   - rinse wafer in deionized H₂O for 1 min.
5. Reactive Ion Etch

precondition plasma chamber with a CF$_4$:O$_2$ plasma for 20 min.
reactive ion etch exposed Ti with CF$_4$:O$_2$ for 3 min.

set:
- flow rates of CF$_4$:O$_2$: 100:10 sccm
- base pressure < 2 mTorr
- pressure: 150 mTorr
- power density: 400 mW/cm$^2$
- temperature: 30°C

reactive ion etch exposed polyimide and photoresist with O$_2$ for 8 min.
set:
- flow rate of O$_2$ to 100 sccm
- base pressure < 2 mTorr
- pressure: 50 mTorr
- power density: 400 mW/cm$^2$
- temperature: 30°C

reactive ion etch remaining Ti with CF$_4$:O$_2$ for 4 min.
set:
- flow rate of CF$_4$:O$_2$ to 100:10 sccm
- base pressure < 2 mTorr
- pressure: 150 mTorr
- power density: 400 mW/cm$^2$
- temperature: 30°C

6. Measure polyimide height and check the quality of the vias with a SEM

Second Level Metallization

1. General Clean-up

3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with N$_2$
2. Photolithography

dispense AZ4210, 2.1 μm, positive photoresist, onto wafer
spin wafer at 4000 rpm for 20 sec.
softbake wafer at 90°C for 30 min.
allow wafer to cool for a minimum of 3 min.
align wafer with 'second level metal' mask
expose wafer with 405 nm, 5 mW/cm² light for 16 sec.
spray develop photoresist using AZ400K:H₂O (1:4), for 90 sec.
rinse wafer in deionized H₂O for 1 min.

3. Evaporation

sequentially e-beam evaporate:
1000 Å of Ti
5000 Å of Au
at a pressure of 8×10⁻⁶ Torr

4. Photoresist Stripping and cleaning

15 min. in hot lift-off acetone
5 min. in hot, new lift-off acetone immersed in an U/S bath
3 min. in warm acetone immersed in an U/S bath
3 min. in hot clean acetone
3 min. in hot clean iso-propanol
dry wafer with N₂
APPENDIX C: HRGCCD Bonding Configuration
HRGCCD Die

1 - No Connection
2 - 1p1A
3 - No Connection
4 - 1p1
5 - No Connection
6 - G2
7 - Input Ohmic
8 - G1
9 - No Connection
10 - No Connection
11 - No Connection
12 - No Connection
13 - No Connection
14 - No Connection
15 - Ground
16 - No Connection
17 - No Connection
18 - No Connection
19 - No Connection
20 - Amplifier Drain
21 - Amplifier Output
22 - Amplifier Source
23 - Reset Drain
24 - Reset Gate
25 - G3
26 - 1p2
27 - No Connection
28 - 1p2A

Ribbon Size: 0.0005" x 0.003"
Gate Wires: 0.0008"

TRIUMF

HRGCCD Bonding Configuration