A Low-Swing, Wide-Tuning-Range CMOS Phase-Locked Loop

by

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Abstract

Increasing demand for affordable high performance communication devices, in particular in mobile systems, is the driving force behind the development of high-speed, low cost, and low power circuits in CMOS technology. This is mainly due to the fact that CMOS process facilitates the integration of analog and digital circuits on the same chip. A major technique to reduce the power consumption in a CMOS chip is the use of low-swing signaling. Integrated phase-locked loops (PLLs) are versatile components used in many communication and control applications.

In this thesis, the design of a low-swing, wide tuning range charge-pump PLL is presented. PLLs are the integral part of many communication and computing applications. The PLL is designed and simulated in a 0.18μm standard CMOS technology. Its frequency range of operation is from 1.14GHz to 2.25GHz. Almost all of the PLL internal signals are fully differential and low swing (1V peak-to-peak differential swing). To further reduce the power consumption of the PLL, the charge pump current of 15μA is used. The PLL operates from a single 1.8V supply while consuming 14.5mW. It remains functional if the supply voltage changes by ±10%. Due to the low-swing nature of the internal PLL signals, the magnitude of the induced noise on the power supply is small, less than 0.8mV.
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<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
</tr>
<tr>
<td>LF</td>
<td>Loop Filter</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector</td>
</tr>
<tr>
<td>PFD</td>
<td>Phase/Frequency Detector</td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump</td>
</tr>
<tr>
<td>CMFB</td>
<td>Common-Mode Feedback</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Silicon</td>
</tr>
<tr>
<td>CML</td>
<td>Current Mode Logic</td>
</tr>
<tr>
<td>SCL</td>
<td>Source-Coupled Logic</td>
</tr>
<tr>
<td>FF</td>
<td>Flip-Flop</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very Large Scale Integration</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital Subscriber Line</td>
</tr>
<tr>
<td>LTI</td>
<td>Linear Time Invariant</td>
</tr>
<tr>
<td>CM</td>
<td>Common-Mode</td>
</tr>
<tr>
<td>PM</td>
<td>Phase Margin</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
</tbody>
</table>
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Dedicated to those who had the talent but never got a chance
Chapter 1

Introduction

1.1. Motivation

The concept of phase locking was invented in the 1930s [1]. Phase locking is a powerful technique that have become ubiquitous in many communication and computing applications. Phase-locked loops (PLLs) are widely used in a variety of applications, including clock generation and skew compensations in microprocessors, clock and data recovery systems, and synchronization. For example, in fiber optic data transceivers [2], disk drive read channels [3], local area network transceivers [4], and DSL transceivers [5], PLLs are used as clock and data recovery systems. In some other applications such as the Internet, de-skewing PLL clock generators for microprocessors, DRAMs [6, 7, 8], and clock generators for network routers [9], the PLL-based circuits are used as the clock synthesis blocks. In addition to the above applications, PLL-based frequency synthesizers are used in local oscillators for RF or microwave transceivers [10].

In recent years, increasing demands for affordable high performance communication devices, in particular in mobile systems, have driven the development of high-speed, low cost,
and low-power circuits in CMOS technology. This is mainly due to the fact that CMOS process facilitates the integration of analog and digital circuits on the same chip. A major technique to reduce the power consumption of a CMOS chip is the use of low-swing signaling [11, 12, 13].

This thesis focuses on the design and simulation of a low-swing wide tuning range charge-pump PLL. Among different PLL topologies, charge-pump PLLs are more commonly used due to their advantages over other approaches. These advantages include a wide capture range, small static phase error, amenability to integration, and higher accuracy [14]. To improve the power consumption and speed of operation of this PLL, fully differential low-swing architecture is used. The PLL is designed and simulated in a 0.18μm CMOS technology.

The differential structure further improves the robustness of the circuit in the presence of the power supply and common-mode noise. In addition, due to the low-swing nature of the internal PLL signals, the magnitude of the induced noise on the power supply is small.

In order to minimize the area (and consequently the size) of the design, it is decided to avoid using any inductors. Therefore, a non-LC ring oscillator is used. Another benefit of using ring oscillators (as compared to LC oscillators) is their wider tuning range which has been taken advantage of in this design. In this thesis, the design of a low-swing, wide tuning range charge-pump PLL is presented.

1.2. Overview of Previous Designs

Table 1 summarizes the performance of the previously published works in full swing PLL design in different CMOS technologies. As Table 1 shows, integrated PLLs with LC oscillators typically require a larger area. They also have a smaller frequency tuning range and a better jitter
performance. On the other hand, PLLs with ring oscillators occupy smaller area and have a wider tuning range at the expense of a poor jitter performance.

Table 1. Performance comparison of the proposed PLL with other designs

<table>
<thead>
<tr>
<th>Reference Number</th>
<th>VCO type</th>
<th>Technology (µm)</th>
<th>Operating Frequency Range (GHz)</th>
<th>Power Consumption (mW)</th>
<th>Supply Voltage (V)</th>
<th>Phase Noise/Jitter</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15]</td>
<td>LC</td>
<td>0.18</td>
<td>4.7-5.3</td>
<td>29.9</td>
<td>1</td>
<td>-96.3dB @10MHz</td>
<td>NA</td>
</tr>
<tr>
<td>[16]</td>
<td>LC</td>
<td>0.12</td>
<td>2.1-2.7</td>
<td>32</td>
<td>1.2</td>
<td>0.74ps @2.7GHz</td>
<td>0.7</td>
</tr>
<tr>
<td>[17]</td>
<td>LC</td>
<td>0.25</td>
<td>5.35-5.64</td>
<td>23</td>
<td>1.5</td>
<td>-88dB @40kHz</td>
<td>NA</td>
</tr>
<tr>
<td>[18]</td>
<td>Ring</td>
<td>0.13</td>
<td>0.03-0.65</td>
<td>7</td>
<td>1.5</td>
<td>1.7% of the Period</td>
<td>0.182</td>
</tr>
<tr>
<td>[19]</td>
<td>Ring</td>
<td>0.25</td>
<td>0.2-2</td>
<td>10</td>
<td>2.5</td>
<td>28.89ps @2GHz</td>
<td>0.028</td>
</tr>
<tr>
<td>[20]</td>
<td>Ring</td>
<td>0.35</td>
<td>0.13-1.02</td>
<td>4.59</td>
<td>1.8</td>
<td>110ps @1.02GHz</td>
<td>0.16</td>
</tr>
<tr>
<td>[21]</td>
<td>LC (CML)</td>
<td>0.18</td>
<td>2.4-2.4835</td>
<td>22</td>
<td>1.8</td>
<td>-125dBc @1MHz</td>
<td>NA</td>
</tr>
<tr>
<td>The Proposed Design</td>
<td>Ring (CML)</td>
<td>0.18</td>
<td>1.14-2.25</td>
<td>14.5</td>
<td>1.8</td>
<td>14ps @2.25GHz</td>
<td>0.023</td>
</tr>
</tbody>
</table>

1.3. The Proposed PLL Design Overview

The proposed PLL is a charge-pump PLL that is intended for low-cost low-power high-speed applications. The PLL uses an input frequency reference of 35MHz (although it remains operational if the reference frequency is chosen between 25 and 40MHz). The PLL uses a divide ratio in a range of 32 to 63 with a five-bit control. A tri-state phase-frequency detector in current-mode logic is designed. A differential charge pump topology is used to compensate for any signal variations. The VCO is a ring oscillator with a frequency range of 700MHz to 4 GHz. All
Chapter 1. Introduction

of the internal signals of the PLL, with the exception of the VCO control voltage, are low swing and differential with about 1V peak-to-peak differential voltage swing. The PLL operates from a 1.8V supply and consumes less than 14.5mW. The complete PLL including its loop filter occupies 0.023mm$^2$ of which loop filter capacitors account for 76% of the total area. To analyze the transient time behavior, the PLL circuit is simulated at its two extreme frequencies, the maximum frequency of 2.25GHz, and the minimum of 1.14GHz.

This thesis is organized in five chapters. Phase-locked loop fundamentals are described in Chapter 2, including the basic concepts of charge-pump PLLs, the loop dynamic, and a general description of PLL building blocks. Chapter 3 presents the design of the entire PLL, including all of its internal components. Chapter 4 and Chapter 5 explain the simulation results of the VCO and PLL and the conclusion and future work, respectively.
Chapter 2

Phase-Locked Loop Fundamentals

Phase-locked loops are an integrated block of many communication and computing applications. A generic block diagram of a PLL is illustrated in Figure 2-1. A PLL is essentially a feedback system that synchronizes its output signal with its input reference signal by minimizing the phase difference between these two signals. In general, PLLs consist of a phase detector\(^1\) (PD), a loop filter (LF), a voltage-controlled oscillator (VCO), and two optional dividers, one in the feedback path and the other in the input path as an input divider. Although, the entire PLL or each component can be implemented in the digital domain, but analog PLLs are preferred in high frequency applications.

\[ f_{in} \xrightarrow{\div M} f_{ref} \xrightarrow{PD} LF \xrightarrow{VCO} f_{out} \]

\[ f_{in} \xrightarrow{\div N} \]

Figure 2-1. Block diagram of a generic PLL

\(^1\) Some applications use phase frequency detectors (PFDs).
Chapter 2. Phase-Locked Loop Fundamentals

The reference signal is generally produced by a crystal oscillator due to its low phase noise and high accuracy. A phase detector compares the phases of the reference signal \( V_{in} \) and the feedback signal \( V_{fb} \) (Figure 2-1) in order to generate an error signal that is used to adjust the frequency of the VCO until the phases are aligned. To suppress the high-frequency components of the PD output and prepare the control voltage of the VCO, the PD output must be filtered through a LF. The output frequency of the VCO is then adjusted based on the value of its input control voltage. The output frequency may be divided down by a frequency divider in the feedback path. The frequency divider in the feedback path is usually a programmable divider that allows the output frequency to fall within the reference frequency. The division ratio of this divider can be either an integer or a fractional number. As illustrated in Figure 2-1, there could be another divider (with divide ratio of \( M \)) at the input of the PLL to set the reference frequency as \( f_{ref} = f_{input} / M \) [22, 23].

When a PLL is in lock, the negative feedback adjusts the average value of the VCO control voltage so that the two inputs of the PD have a constant, ideally zero, phase difference, i.e., they have the same frequency [24].

A popular class of PLLs, particularly in integrated applications, is the charge-pump PLL. In these PLLs, a charge-pump is included in the forward path of the PLL, as illustrated in Figure 2-2. This class of PLLs is capable of accurately tracking the input phase [25]. A charge-pump PLL is typically composed of a PD or phase-frequency detector (PFD), a charge-pump (CP), a LF, a VCO, and a frequency divider.
In this chapter the building blocks of a PLL and the basic PLL dynamics are briefly reviewed. The following sections explain the different building blocks of the charge-pump PLL, followed by the loop characteristic explanation of a CP PLL. Section 2.1 explains the building blocks of the phase or phase/frequency detector. Section 2.2 presents the general overview of the charge-pump, the common-mode feedback, and the loop filter. Sections 2.3 and 2.4 describe the voltage-controlled oscillator operation and the frequency divider building block, respectively. Section 2.5 describes the charge-pump loop characteristic. Finally, jitter in PLLs is briefly reviewed in Section 2.6.

2.1. Phase or Phase/Frequency Detector

A phase detector compares the phase of its two input signals and generates an output signal whose average value is proportional to the phase difference between the two inputs \( V_{out} \propto \Delta \phi \). In the ideal case, the relationship between \( V_{out} \) and \( \Delta \phi \) is linear, and the constant of proportionality, \( K_{PD} \), is referred to as the gain of the PD (Figure 2-3).
One of the most common phase detectors is the XOR detector, which is not suitable for this application. An XOR PD has the disadvantage of possible locking on the harmonics of the reference signal because its output frequency can vary by a factor of more than two. To avoid this, the VCO must not send any harmonics of the chosen operating frequency, and its two inputs should be close enough. Additionally, the XOR phase detector is fairly insensitive to frequency differences of its inputs, and in the presence of a large frequency difference between its two inputs, it cannot generate the proper output, and so the PLL could fail to lock. This problem is called an inadequate acquisition range of the PLL [24] and can be ameliorated by using a PFD instead of a PD. Furthermore, XOR PD circuits produce error pulses on both edges (rising and falling), but other types of PDs may generate a pulse error only on one of the edges, which means that a 50% duty cycle is not necessary.

The PFD circuit generates three states according to its response to the rising or the falling edges of its two inputs. Consider that both outputs, Out1 and Out2, are low (Figure 2-4), and are called UP and DN respectively in a PFD. A rising edge on IN1 leads to Out1=1, and Out2=0. The circuit will keep this state until a rising edge occurs on IN2, and consequently it forces the Out1 to become low. The same procedure is considered for IN2.
In Figure 2-4 (a), the frequencies of the two inputs are equal, but IN1 leads IN2. The PFD produces a series of pulses on Out1 that is proportional to $\phi_{IN1} - \phi_{IN2}$, and Out2 remains zero. In Figure 2-4 (b), the two inputs have unequal frequencies, and IN1 has a higher frequency than IN2, and Out1 generates pulses when Out2 is zero. The dc value of the outputs provides information about the phase difference or the frequency difference between the two inputs.

A tri-state PFD is a good choice, because it locks only at the fundamental frequencies of its input. Figure 2-5 depicts a simplified implementation of a standard tri-state PFD consisting of two edge-triggered and resettable D-flipflops (D-FF1 and D-FF2). The inputs of both D-FFs are connected to $V_{DD}$. The reference clock (CKref) and the feedback clock (CK_fb) act as two inputs (the same as IN1 and IN2 in Figure 2-4) for the PFD.
The state diagram of the tri-state PFD is shown in Figure 2-6. Initially PFD is in “State-II”. On the rising edge of reference clock (Clk_ref), UP becomes one and PFD goes to State-I. The PFD remains in this state until another edge occurs on the feedback signal (Clk_fb) and causes a transaction to State-II and therefore, forcing the UP signal to return to zero and takes PFD to “State-II.” In this diagram, it is important to consider the frequency difference between the reference and feedback signals. The final state of the operation of the PFD is toggling between “State-II” and “State-I.” To clarify, consider the case that the feedback frequency is smaller than the reference frequency, then there is a time interval during which two edges of Clk_ref take place between two edges of Clk_fb. Figure 2-6 shows that PFD leaves “State-III” and toggles between “State-I” and “State-II” [26, 27].

Figure 2-6. Tri-state PFD state diagram
Chapter 2. Phase-Locked Loop Fundamentals

When both UP and DN signals are high, both registers will be reset through the AND gate. The reset signal stays high until both UP and DN have gone low again. If a simple AND gate is used to produce the reset signal, sufficient delay should be added in the reset path to make sure that the reset signal stays high long enough to satisfy the hold time requirements of both D-FFs.

2.2. Charge-Pump and Loop Filter

The charge-pump circuit consists of two switches driven with UP and DN signals that are produced by the PFD (Figure 2-7). The charge pump draws the current into or out of the loop filter. At the rising edge of the UP signal, the charge-pump forces a current into the loop filter. Similarly, when the reference signal operates at a lower frequency than the feedback signal, DN rises. At the rising edge of DN, the charge pump sinks the current out of the loop filter. The combination of the charge pump and the loop filter generates the average output of the PFD (UP – DN) that is used to adjust the frequency of the VCO oscillation.

Figure 2-7. Simplistic charge-pump circuit
Chapter 2. Phase-Locked Loop Fundamentals

One major drawback in a single-ended charge pump structure is the leakage problem [28]. When a pulse from the PFD turns one of the switches OFF from its ON position, the charge stored in the channel of the switch transistor escapes to its nearby nodes, shown by the dashed lines in Figure 2-7. Consider the PMOS switch (UP) in Figure 2-7, half of the charge is injected to the parasitic capacitor at the source of the switch, and the other half is injected to the loop filter. When UP forces the PMOS switch to be OFF, this additional charge is added to the loop capacitor (C), which is an undesirable effect. Differential charge pump topology is used to provide an additional path for this extra charge, as shown in Figure 2-8, by adding the complementary inputs. When the UP switch is closed, the current path exists for the extra charge between the current source ($I_C$) and the charge pump to function exactly like a normal charge pump.

![Figure 2-8. Differential charge pump with a loop filter](image)

A PFD, a single-ended CP, and a loop filter (Figure 2-9) are modeled as a linear continuous time system. In a real system, a PFD acts as a pulse modulator and drives the charge pump for the duration of a pulse width, which is related to the PFD input phase difference (Figure 2-10). The output of the PFD, named UP, forces the current into the loop filter and causes the VCO control voltage to rise. As illustrated in Figure 2-10, when UP and DN are equal
to zero, $S_1$ and $S_2$ are off, and $V_{out}$ remains constant. If UP is high and DN is low, then $I_1$ charges the $C_p$. On the other hand, if UP is low and DN is high, $I_2$ discharges $C_p$.

![Figure 2-9. The PFD/CP/LF](image)

The time during which the UP or DN signals are high determines the amount of current that gets delivered to the loop filter. The difference between the reference and the feedback signal phases can be shown as:

$$\Delta \phi = \phi_{ref} - \phi_{fo} \quad (2-1)$$
The PFD outputs go high on the leading edge of their related clock inputs and remain high until the reset signal makes them low. The time during which the outputs are high, \( t_{\text{high}} \), which is related to the phase error, \( \Delta \phi \), can be shown as \[29\]:

\[
t_{\text{high}} = \frac{\Delta \phi}{\omega_{\text{ref}}} \quad (2-2)
\]

The open loop transfer function of the PFD/CP/LF combination, illustrated in Figure 2-10, can be expressed as:

\[
\frac{V_{\text{ctrl}}(s)}{\Delta \phi} = K_{\text{PFD}} \cdot I_{\text{CP}} \cdot F(s) \quad (2-3)
\]

where \( K_{\text{PFD}} \) is the PFD gain, \( I_{\text{CP}} \) is the charge pump current, and \( F(s) \) is the transfer function of the loop filter.

2.3. Voltage-Controlled Oscillator

An oscillator is a system that generates a periodic output signal without any input. Voltage-controlled oscillators (VCOs) are tunable oscillators that are widely used in PLLs. Their output frequency is a function of their input control voltage, as depicted in Figure 2-11, and can be expressed as:

\[
\omega_{\text{out}} = \omega_0 + K_{\text{VCO}} V_{\text{ctrl}} \quad (2-4)
\]

where \( \omega_0 \) represents the centre frequency of the VCO and \( K_{\text{VCO}} \) denotes the conversion gain of the oscillator that is the slope of the linear region [24]. Ideally, for a linear analysis, \( K_{\text{VCO}} \) should be constant. \( K_{\text{VCO}} \) and the achievable frequency range, \( \omega_2 - \omega_1 \), is called the VCO tuning range, as shown in Figure 2-11.
Chapter 2. Phase-Locked Loop Fundamentals

The VCO has a fundamental role in defining the desired range of operation of a PLL because all of the PLL building blocks, except VCO, are operating over a wide frequency range, and the VCO is the only limiting block. A VCO is usually considered as a linear time-invariant system, with the control voltage as the input of the system and the excess phase of the output signal as the output of the system. This output phase can be written as:

\[
\phi_{out}(t) = K_{VCO} \int V_{ctrl} dt \tag{2-5}
\]

The VCO input/output transfer function is:

\[
\frac{\phi_{out}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \tag{2-6}
\]

Equation (2-5) shows that to change the output phase, we must first change the frequency, which lets the integration take place. The above equations reveal that the output phase of the VCO cannot be determined only from the present value of the control voltage, but that is also depends on the history of \( V_{ctrl} \).

Two chief topologies are used in the design of VCOs: LC-Oscillator and the ring oscillator. LC-oscillators oscillate at the resonant frequency \( (\omega_0) \) of the inductor and the capacitor, given by \( \omega_0 = \frac{1}{\sqrt{LC}} \). An LC tank filters out frequencies away from the resonant peak, which improves the phase noise performance, particularly with a high-Q tank (Figure...
The advantage of the LC-oscillator is its good phase noise performance because of the energy storage nature of the inductor and the capacitor, which greatly limits the amount of energy added by other active devices. In spite of their good phase noise response, their tuning range is very limited. Also, the LC-oscillator topologies do not provide quadrature outputs by nature. Quadrature outputs are four output signals with four different phases that are apart of each other by 45° as shown in Figure 2-14.

The second topology is the ring oscillator, which contains a ring of inverters with a net inversion in the feedback path, as illustrated in Figure 2-13. The frequency of the ring oscillator VCO is inversely proportional to the propagation delay of each inverter \( t_d \) and the number of the inverters \( N \) can be written as \( f_0 = 1/(2Nt_d) \). To tune the VCO frequency, the propagation delay of each inverter can be adjusted. The propagation delay of each inverter is small, which increases the maximum output frequency of the ring oscillator. The other reason for their wide tuning range is that the current through each stage can be varied in several orders. In the single-ended ring oscillator topology, there are an odd number of inverters.
With differential signaling, a ring oscillator can be built with an even number of inverters by flipping the output of the last stage, which is fed back to the input of the first stage. Ring oscillators can produce quadrature outputs by their nature. For example, by using four stages as a ring oscillator, quadrature outputs can be produced (Figure 2-14).

Although they have a good tuning range, their phase noise is poor. As described in [30], in a ring oscillator, the transistors have to provide all the energy that is necessary to charge and discharge the node capacitances in each cycle because there is no storage element in a ring oscillator. Therefore, ring oscillators can improve phase noise performance by consuming more power.

Compared to LC-oscillators, ring oscillators have a very wide tuning range determined by current variation, an inherent ability to produce quadrature outputs, poor phase noise, and their power, which can vary greatly due to the trade-offs between the power and the phase noise. LC-oscillators have a narrow tuning range and a very good phase noise. They consume too much power and do not have the inherent ability to produce quadrature output [30]. In this thesis, a ring oscillator has been chosen because of its wide tuning range. Generally, they also occupy a smaller chip area compared to integrated LC oscillators [31].
2.4. Frequency Divider

The PLL reference signal is produced by a crystal that operates from between tens of kHz to a few hundred MHz. The PLL output signal generated by the VCO operates at a few GHz. To compare the reference signal with the VCO output signal, a frequency divider is necessary in the feedback path from VCO output to the PFD input in order to produce a low frequency programmable signal from a high frequency signal. This frequency division can be done using an analog frequency divider [32] or a digital counter [33, 34]. Due to the resonant nature of the analog dividers, they are less noisy than the digital ones. However, digital dividers are capable of providing large and programmable division ratios. In this work, a digital divider has been chosen for this reason. Chapter 3 provides a detailed description of the divider design.

2.5. Charge-Pump Loop Characteristics

This section deals with the dynamic behavior of a low-swing charge-pump PLL. A PLL is a system with a memory that requires a finite time to respond to its input changes. In addition, the dimensions of the variable of interest change around the loop. Furthermore, under the lock condition, the output frequency is equal to the input frequency, regardless of magnitude of the loop filter [24].

It is a common practice to analyze the behavior of the PLL near its lock condition by using a linear time invariant (LTI) model, as shown in Figure 2-15. The transfer function of this linearized PLL model can be expressed as:
Chapter 2. Phase-Locked Loop Fundamentals

Figure 2-15. The equivalent phase domain LTI model for the generic PLL

\[
H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PFD} K_{VCO} F(s)}{s + \frac{K_{PFD} K_{VCO} F(s)}{N}} = \frac{N/M}{\frac{1}{\omega_{LPF}} + \frac{s}{\omega_{z}}} \quad (2-7)
\]

where \(K_{PFD}\) is the gain of the PFD, \(K_{VCO}\) is the VCO gain, and \(F(s)\) is the loop filter transfer function. The exact nature of the transfer function in Equation (2-7) is determined by the loop filter transfer function. The order of the loop filter determines the speed and the transient behavior of the PLL response.

In its simplest form, \(F(s)\) could be a constant, representing gain or attenuation. In that case the loop is a first-order system. In a first-order loop, to have a lower steady-state phase error, the loop bandwidth should be increased. High-order loops are more common because they are not limited by this strong coupling between the bandwidth and the steady-state phase error of the first-order loop, as shown in (2-7) [25]. Many applications use a low-pass filter for \(F(s)\) to add another pole to the system. This extra pole allows more flexibility in the design of the PLL.

One capacitor \((F(s) = 1/\omega_{s})\) is not a good choice as a LF. It adds one pole in origin, which makes the PLL unstable. To guarantee system stability, a compensating network that is typically a zero should be added to the filter. One of the most common loop filters has a pole at the origin and a zero at a frequency, \(\omega_{z}\), just below the unity gain frequency of the PLL loop (Figure 2-17).

In this case the transfer function of the loop filter can be written as:
Chapter 2. Phase-Locked Loop Fundamentals

\[ F(s) = \frac{1 + \tau_s s}{s} \quad (2-8) \]

Consider:

\[ K = K_{VCO} K_{PF} \quad (2-9) \]

By substituting \( F(s) \) (2-8) in (2-7), the new transfer function is achieved as:

\[ H(s) = \frac{(\tau_s s + 1)(K/M)}{s^2 + (K\tau_s /N)s + (K/N)} \quad (2-10) \]

The resulting PLL transfer function in (2-10) is a second-order system that is characterized by its natural frequency, \( \omega_n \), and its damping factor, \( \xi \). A second-order transfer function can be rewritten with its natural frequency and damping factor as:

\[ H(s) = \frac{2\xi \omega_n s + \omega_n^2}{s^2 + 2\xi \omega_n s + \omega_n^2} \quad (2-11) \]

A comparison of the resulting transfer function with (2-11) shows that the natural frequency and the damping factor can be expressed as:

\[ \omega_n = \sqrt{K/N} \quad (2-12) \]

\[ \xi = \frac{\tau_s}{2} \sqrt{K/N} \quad (2-13) \]

The loop filter is used to set the appropriate unity gain frequency and guarantee stability when the other important parameters such as the gain of the PFD, the VCO gain, and divider ratio have been chosen. The open loop gain of the LF should be kept as small as possible to reject the noise that is added within the loop. It can be achieved by a second-order filter with a pole at DC, a zero before the unity gain frequency, to provide an adequate phase margin, which is one of the key parameters for measuring the stability, and a second pole after the unity gain frequency to help improve the high frequency rejection. Figure 2-16 and Figure 2-17 show the
loop filter schematics and the magnitude and the phase of the open-loop transfer function, respectively.

![Second-order loop filter schematic](image)

**Figure 2-16. Second-order loop filter schematic**

The damping factor is a measure of stability. An increase in the damping factor of the PLL allows both poles of the PLL to move into the left-hand plane to make sure that the PLL is stable. For optimum settling time and no peaking in the frequency response, $\zeta$, damping factor is chosen as 0.7 [24]. Noise can be filtered by adjusting the loop bandwidth and peaking in the frequency response based on the dominant noise source [35]. Because of the direct relation between the “zero” time constant and the loop damping factor, adjusting one of them will adjust the other.
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The transfer function of the loop filter in Figure 2-16 can be written as:

\[ Z(s) = \frac{(RCs + I)}{(C + C')s(R(C||C')s + I)} \]  
\[ (2-14) \]

In a charge-pump PLL (Figure 2-18), the open-loop transfer function \( H'(s) \) is:

\[ H'(s) = K_{PFD} \cdot \frac{I_{CP}}{(C + C')s} (I + RCs) \cdot \frac{K_{VCO}}{s^2 \cdot [I + R(C||C')s]} \]  
\[ (2-15) \]

Figure 2-17. Magnitude and phase of the open-loop transfer function for a third-order PLL

Figure 2-18. Charge-pump PLL
Chapter 2. Phase-Locked Loop Fundamentals

where \( \omega_z = \frac{1}{RC}, \omega_{p3} = \frac{1}{R(C||C')}, \) and \( \omega_c \) are zero frequency, third pole frequency, and the open-loop unity gain frequency, respectively. The resistor and the capacitors of the loop filter should be chosen carefully so that they can filter the high-frequency portion of the signal, maintain the stability of the loop, and not produce extra noise. Another major parameter for stability measurement is phase margin. For phase margin calculation, the Equation (2-14) can be rewritten as:

\[
Z(s) = \left( \frac{m}{m+1} \right) \frac{\tau s + 1}{sC \left( \frac{\tau s}{m+1} + 1 \right)} \quad (2-16)
\]

where \( \tau = RC, \) and \( m = C/C' \). Also:

\[
H'(s) = K_{VCO} I_{CP} K_{PFD} \left( \frac{m}{m+1} \right) \frac{\tau s + 1}{s^2 C \left( \frac{\tau s}{m+1} + 1 \right)} \quad (2-17)
\]

The phase margin (PM) for a third-order PLL can be approximated with [36, 37]:

\[
PM = \tan^{-1} \left( \frac{\tau \omega_c}{m+1} \right) - \tan^{-1} \left( \frac{\tau \omega_c}{m+1} \right) \quad (2-18)
\]

where \( \omega_c \) is the crossover frequency shown in Figure 2-17. The maximum phase margin is only a fraction of the loop filter capacitors (C and C'). The ‘m’ value greater than one is desirable in order to have a stable loop, which forces the phase margin to be greater than 20. Typically ‘m’ is considered around 10 or 20 to achieve a stable loop [24].
2.6. Jitter in PLLs

Jitter is defined as the deviation of the significant instances of a signal from its ideal location in time. The significant instances in a signal are typically chosen to be the transition points (zero crossing of the signal). In other words, jitter shows how early or late a signal transition happens with respect to the expected transition time [52]. Jitter can be specified in a time unit (e.g., picoseconds) or a percentage of the time period.

There are three main measures for the jitter: long-term jitter, cycle jitter, and cycle-to-cycle jitter [38]. Long-term jitter is the maximum change in a clock's output transition from its ideal position, over many cycles. In other words, the long-term jitter is the accumulated jitter over time, as shown in Figure 2-19. The time point of the nth negative-to-positive zero crossing of the output of the PLL in the steady state is referred to as tn, and the nth period is defined as Tn = tn+1-tn. For an ideal PLL, this time difference is independent of n. But in reality, it varies with n as a result of jitter in the circuit. This variation results in a deviation ΔTn = Tn- T from the mean value of the period, T [43, 52, 38]. Long-term jitter is the accumulated value of ΔTn over time, which can be expressed as:

Long-term jitter = \sum_{n=1}^{N} ΔT_n (2-19)

Figure 2-19. Long-term jitter
Chapter 2. Phase-Locked Loop Fundamentals

A better measure of jitter for the PLL and especially for the VCO is the cycle jitter, which is defined as the rms value of the timing error $\Delta T_n$. Cycle jitter describes the magnitude of the period fluctuations and is written as (2-20). Figure 2-20 illustrates the cycle jitter diagram.

$$\Delta T_c = \lim \sqrt{\frac{1}{N} \sum_{n=1}^{N} \Delta T_n^2}$$  \hspace{1cm} (2-20)

![Figure 2-20. Cycle jitter](image)

The third type of jitter considered here is the cycle-to-cycle jitter, which represents the rms value of the difference between the two consecutive periods, as shown in Figure 2-21. In other words, the cycle-to-cycle jitter is the change in a signal transition time compared to its corresponding position in the previous cycle. This jitter is expressed as:

$$\Delta T_{cc} = \lim \sqrt{\frac{1}{N} \sum_{n=1}^{N} (T_{n+1} - T_n)^2}$$  \hspace{1cm} (2-21)

![Figure 2-21. Cycle-to-cycle jitter](image)
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The cycle jitter compares each period with the mean value of the periods, while the cycle-to-cycle jitter compares each period with the preceding one. Therefore, cycle-to-cycle jitter describes the short-term dynamics of the time period [43].
Chapter 3

Phase-Locked Loop Design Procedure

The block diagram of the proposed PLL that is intended for high-speed low-power application is shown in Figure 3-1. A 35MHz crystal produces the input reference frequency. A programmable divider in the feedback path produces the 32 to 63 division range through a 5-bit control inputs. The resolution step size is around 30MHz, controlled by a divider in the feedback path. This PLL has been designed and simulated in a 0.18μm CMOS technology with a 1.8V supply. The total power consumption is less than 14.5mW, and it takes less than 700ns for the PLL to lock to the desired frequency. Table 2 summarizes design specifications.

![Figure 3-1. The proposed PLL building blocks](image-url)
Table 2. Design specifications

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input reference frequency</td>
<td>35MHz</td>
</tr>
<tr>
<td>Output frequency</td>
<td>1.14GHz-2.25GHz (31 steps)</td>
</tr>
<tr>
<td>Lock time</td>
<td>&lt;700ns</td>
</tr>
<tr>
<td>Power consumption</td>
<td>14.5mW</td>
</tr>
<tr>
<td>Process technology</td>
<td>TSMC 0.18μm CMOS</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 ± 0.18 V</td>
</tr>
</tbody>
</table>

Low-swing signaling is used through the PLL to enhance its speed as well as the power consumption. The designed voltage-controlled ring oscillator (VCO) is operational in the frequency range from 700MHz to 4GHz. Due to the CML implementation of the low-swing PLL; at the frequency range of PLL operation (1.14GHz to 2.25GHz) the static power consumption of the PLL is lower than the standard CMOS implementation. In lower frequencies, the CML, which has a constant power that is relatively independent of its frequency of operation, may consume more power than standard CMOS. But at higher frequencies, the power consumption of the standard CMOS will also increase.

In CML logic circuits, a constant current passes through the cells, which produce less noise on the power supply. On the other hand, the CMOS standard circuits work on the basis of the current switching. In the same coupling situation, the low-swing CML logic circuits produce a smaller amount of noise on the power supply. This noise contribution can be measured by the IR drop technique.

This chapter discusses the building blocks of this fully differential PLL. Section 3.1 explains the design of the phase-frequency detector. Section 3.2 discusses the design of the
Chapter 3. Phase-Locked Loop Design Procedure

charge-pump circuit, including common-mode feedback along with the loop filter implementation. Sections 3.3 and 3.4 present the VCO and the divider, respectively.

3.1. Phase/Frequency Detector Circuit

Figure 3-2 depicts a simplified schematic of the PFD. As mentioned before, the rising edge of the reference voltage \( V_{\text{ref}} \) sets the output to UP, and the rising edge of the feedback signal \( V_{\text{fb}} \) (output of the divider) sets the output to DN. Phase error is obtained by comparing the widths of the UP and DN pulses. Once both UP and DN are high, the "Reset" signal through the delay path resets both registers. The reset stays high until both outputs of the registers go low again.

![Figure 3-2. Simplified tri-state PFD schematic](image)

The error signal is the difference of the averages of the UP and DN signals. If the reference input is ahead of the feedback signal, the frequency of the VCO will increase to reduce the phase error between the two signals. Therefore, when the reference phase \( \phi_{\text{ref}} \) is ahead of
Chapter 3. Phase-Locked Loop Design Procedure

the feedback phase ($\phi_{fb}$), the width of the UP pulse increases, given that $|\phi_{ref} - \phi_{fb}| < 2\pi$. Also, when $\phi_{ref} = \phi_{fb}$ (neglecting the narrow pulses in Figure 2-4(b)), the output is low [31].

Figure 3-3 illustrates the transfer characteristic of the PFD. It shows that the output varies symmetrically as the phase difference changes around zero. The slope of this transfer function represents the PFD gain that is $V_o/2\pi$.

![Figure 3-3. Phase-frequency detector transfer curve](image)

As shown in Figure 3-2, the main building blocks in a PFD are two D-flip flops (D-FFs) and the AND gate. Combined with the charge pump, the PFD potentially suffers from a dead zone in its transfer characteristic, as shown with the solid line in Figure 3-4. If the phase difference between the input and the output varies within the dead zone area, the dc output of the charge pump does not change significantly and the loop fails to correct the resulting error; therefore, a peak-to-peak jitter equal to the dead zone width arises in the output [31]. The dead zone, which is due to the inherent delay in turning on charge pump currents, directly translates to a peak-to-peak phase jitter in the PLL [39]. In other words, if the delay through the reset path is shorter than the delay to the charge pump, which the PFD is driving, then the charge pump will not get switched even though there is a phase error present. To eliminate the dead zone, the delay of the reset path of the PFD should be increased. Including the proper amount of delay results in
Chapter 3. Phase-Locked Loop Design Procedure

the dashed line in Figure 3-4. Subsection 3.1.1 and 3.1.2 explain the design of the D-FF and the design of the CML AND gate.

Figure 3-4. PFD output characteristic versus input phase error

3.1.1. D-Flip Flop Circuit

Figure 3-5 shows the basic structure of a D-FF, which consists of two cascaded latches. The clock input for the second latch is the inverse of the clock input for the first one.

Figure 3-5. Basic structure of a D-FF

The building blocks of the PFD are designed using differential CML, also known as source-coupled logic (SCL), blocks. This logic family of circuits is fully differential and has two main benefits over other logic families such as the standard static or dynamic CMOS logic. First, CML can be used at high speed partly because only NMOS devices are used. Second, the current
through the logic gates is constantly dictated by the constant tail current, even when the differential output is switching, leading to less noise on both the power supply and the substrate [31, 40]. In addition, for high operating frequencies, CML has lower power dissipation than rail-to-rail logic [41]. One disadvantage of the CML circuit is its static current, which causes higher power consumption. In this work, at low frequencies, the number of the CML gates used in low frequency blocks (e.g., PFD) has been minimized to limit their power consumption.

Figure 3-6 shows the differential CML latch structure. This kind of structure employs positive feedback, which is realized using a cross-coupled NMOS differential pair. The latch consists of an input pair (M1-M2) for sensing (tracking) the input and a regenerative pair (M3-M4), for storing the state. The track and store modes are established by the clocked transistor pair, M5-M6. When CLK is high, the tail current is steered to the input pair, allowing the output voltage to track the input voltage, while M3 and M4 are turned off. When CLK is low, in the transition to the store mode, M1 and M2 are off, and the cross-coupled pair can store the output levels on the output nodes [37]. Reset signal is connected to the outputs through M7 and M8.

![Figure 3-6. Schematic of a CML latch](image-url)
Chapter 3. Phase-Locked Loop Design Procedure

There are three steps in designing such a latch. First, the tracking amplifier should be designed to have a moderate gain of around 2. Second, for simplicity, cross-coupled devices should be sized the same as the transistor sizes in the tracking stage. Third, the clock transistors should be chosen roughly 20% larger in width compared to the other transistors because they will be in the triode region of operation and have a lower drive capability [37].

There are several options for the load of the CML logic, including resistors, diode connected PMOS or NMOS transistors, and PMOS transistors biased in the triode region. Resistors are used for high-speed applications, but they occupy a larger area. Diode connected PMOS or NMOS transistors are usually used in applications where the area is an important issue, but their speed of operation is low. The other choice for the load is PMOS transistor operating in the triode region. This type of load can be used in high speed applications, but it is nonlinear, and the designer has to make sure that they stay in the triode region. In this work, resistors have been used as the loads. Table 3 shows transistor sizes in the PFD. The resistor loads are 6KΩ each.

<table>
<thead>
<tr>
<th>(W/L)_{1,2}</th>
<th>(W/L)_{3,4}</th>
<th>(W/L)_{5,6}</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8µm/0.18µm</td>
<td>1.8µm/0.18µm</td>
<td>3µm/0.18µm</td>
</tr>
</tbody>
</table>

An important design issue in the low-swing design is the value of the output swing. In particular, when one differential stage drives another one, the second differential stage requires a large enough $V_{DS}$ to stay in the saturation region. The output voltage levels should be carefully chosen such that they can fully switch the subsequent differential stage.
3.1.2. AND-Gate Circuit

Figure 3-7 illustrates the basic schematic of CML logic AND gate. Depending on the input and output signal configuration, this structure can be used as an AND/NAND and OR/NOR gate. The chosen arrangement of the input and the output signals in Figure 3-7 is AND/NAND operation such that the gate would perform. When A and B are high, the current flows through \( R_1 \) and causes the NAND output to become \( V_{DD} - R_1 I_{bias} \), while the other output, which represents the AND operation, goes to \( V_{DD} \). The output voltage swing cannot be too large because \( M_1 \) and \( M_2 \) are in the triode region and the drain-source voltage of the \( M_1 \) and \( M_2 \) should be enough to keep them in that region. To achieve a symmetric output waveform in the AND gate, an NMOS transistor, \( M_5 \), is added, as shown in Figure 3-7 [41].

![Figure 3-7. Current mode logic AND/NAND gate with differential inputs and output](image)

Sufficient delay should be added in the reset path of the PFD to make sure that the reset signal stays high long enough to satisfy the hold times of both D-FFs and therefore to minimize the dead zone. Two NOT gates (Figure 3-2) has been used in the reset path to provide this delay. Table 4 shows the transistor sizes in the PFD. The resistive loads are equal to 6kΩ.
3.2. Charge Pump Circuit

The charge pump circuit uses the UP and DN signals as its inputs and controls the amount of current that should be sources or sunk from the loop filter. Figure 3-8 depicts the fully integrated charge pump designed in this system. Since inputs of the charge pump circuit are low-swing signals as opposed to the rail-to-rail, the sizing of the transistors M1 to M4 are carefully chosen so that they can properly be turned off.

This charge pump consists of two current mirrors. The PMOS one (M5, M6, and M10) mirrors $I_{bias}$ through the UP current ($I_{UP}$) into the charge-pump (CP). Similarly, there is an NMOS current mirror (M7 and M8) to mirror the current bias ($I_{bias}$) through the DN current ($I_{DN}$).
Chapter 3. Phase-Locked Loop Design Procedure

into the charge pump. Depending on the value of the input signals at the gates of transistors \( M_1 \) to \( M_4 \), the charge pump current is sunk to or sourced from its differential output. \( I_{UP} \) and \( I_{DN} \) of the charge pump must be equal to ensure a constant value for the \( K_{PFD} \). The bias circuit shown in Figure 3-8 is used to produce equal UP and DN currents.

In a differential charge-pump, the paths for the UP and DN signals should be symmetric. In the PLL’s lock mode, the UP and DN signals have narrow pulses. In this case, if the UP and DN paths are not symmetric, the charge pump’s net output current will be non-zero. This non-zero current would generate a drifting ripple on the control voltage and consequently result in a phase error. Even with a perfect adjustment of the UP and DN signals, the net current produced by the charge pump can be nonzero because of the mismatch between the drain currents of \( M_5 \) and \( M_8 \) (Figure 3-8).

The charge-pump UP and DN currents are chosen to be 15\( \mu \)A. Special care has been given to the sizing of \( M_5 \) and \( M_8 \) to make sure that these devices stay in the saturation region. The proper \( V_{SAT} \) allows a possible 0.45V drop across the switches. Initially the transistor sizes can be chosen using the following equation. Table 5 shows the transistor sizes in the charge-pump, which are optimized through simulation in Cadence.

\[
\left( \frac{W}{L} \right) > \frac{2I_D}{\mu_n C_{ox} V_{SAT}^2} \quad (3-1)
\]

<table>
<thead>
<tr>
<th>( (W/L)_{1,2} )</th>
<th>( (W/L)_{3,4} )</th>
<th>( (W/L)_{5,6,10} )</th>
<th>( (W/L)_{7,8} )</th>
<th>( (W/L)_{9,11} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5( \mu )m/0.18( \mu )m</td>
<td>0.8( \mu )m/0.18( \mu )m</td>
<td>8( \mu )m/0.27( \mu )m</td>
<td>7( \mu )m/0.36( \mu )m</td>
<td>7( \mu )m/0.36( \mu )m</td>
</tr>
</tbody>
</table>

Table 5. The charge pump transistor sizes
3.3. Common-Mode Feedback (CMFB) Circuit

To set the output common-mode voltage of the differential charge pump to the desired dc voltage, a common-mode feedback circuit is used, as illustrated in Figure 3-9 [42]. The output common-mode (CM) level of a differential structure is sensitive to device properties and mismatches. Basically, the common-mode feedback (CMFB) circuit senses the CM level of the outputs, then compares it with a reference and returns the error signal to the charge pump circuit.

![Figure 3-9. Common-mode feedback and the loop filter](image)

Out1 and out2 are the two outputs of the charge pump circuit. M_{8-10} and M_{1-3} are NMOS and PMOS current sources, respectively. The reference voltage is equal to twice that of the \( V_{GS} \) of the NMOS transistors. If the CM level of the CP output increases, the gate-source voltage of the current source transistors will be increased and, consequently, their current is increased. As a result, the voltage of the out1 and out2 nodes drops. Table 6 shows the transistor sizes in the CMFB circuit. A differential to single-ended voltage converter is used at the output of the loop.
Chapter 3. Phase-Locked Loop Design Procedure

filter to generate the control voltage for the VCO because the designed VCO works with a single-ended control voltage.

Table 6. The sizes of the CMFB transistors

<table>
<thead>
<tr>
<th>(W/L)_{1,2,3}</th>
<th>(W/L)_{4,5}</th>
<th>(W/L)_{6,7}</th>
<th>(W/L)_{8,9,10}</th>
</tr>
</thead>
<tbody>
<tr>
<td>4\mu m/0.18\mu m</td>
<td>4\mu m/0.18\mu m</td>
<td>3\mu m/0.27\mu m</td>
<td>3\mu m/0.36\mu m</td>
</tr>
</tbody>
</table>

3.4. Loop Filter Circuit

Basically, the loop filter circuit attenuates the high frequency components of the charge pump’s output. To have a stable loop filter, special attention is given to choosing the loop filter type, as explained and illustrated in Figure 2-16. To have a symmetrical layout topology for the differential low pass filter, the loop filter’s resistor is broken into two equal parts (Figure 3-9) each connected to one terminal of C.

The resistor R, in series with capacitor C of the loop filter, produces some ripple at the output of the loop filter (i.e., the control voltage of the VCO) that can cause cycle-to-cycle jitter. As a common practice to reduce this effect [42], the capacitor C’ is added in parallel with the RC filter. For C’\ll C, the additional pole due to C’ is large, and its effect can be neglected. The loop filter’s cut-off frequency is usually chosen to be about one tenth or one twentieth of the maximum operation frequency of the PLL. For this loop filter design, one tenth of the reference frequency is used. As mentioned in [36] the phase margin, PM, and crossover frequency, \omega_c, are where m=C/C’.
Chapter 3. Phase-Locked Loop Design Procedure

\[ PM = \tan^{-1}(\tau \omega_c) - \tan^{-1}\left(\frac{\tau \omega_c}{m+1}\right) \] (3-2)

Differentiating (3-2) with respect to \( \omega_c \) achieves the maximum phase margin:

\[ \omega_c = \sqrt{m+1}/\tau \] (3-3)

If we force the crossover frequency to be exactly equal to (3-3), then we get:

\[ K_{VCO} I_{CP} K_{FFD} \left( \frac{m}{m+1} \right) = C \frac{\tau^2}{\sqrt{m+1}} \] (3-4)

The loop filter can be designed as follows: first, the VCO gain should be set. After setting \( K_{VCO} \), the desired PM should be chosen and from (3-2) \('m'\) can be calculated. Then from (3-3), \( \tau \) should be chosen. \( C \) and \( I_{CP} \) can be selected such that they satisfy (3-4). The noise contribution of \( R \) is calculated. If the calculated value is negligible the design is complete; otherwise, the \( C \) value should be changed [36]. In this design \( C=15\text{pF}, \ C'=3\text{pF}, \) and \( R=10\text{k}\Omega \) have been chosen.

3.5. VCO Circuit

One of the challenging building blocks of a fully integrated PLL is the VCO. A major design challenge for integrated VCOs is to have a large tuning range to compensate for temperature and process variations. Ring oscillators are among the popular structures for VCOs due to their wide tuning range and amenability to integration. Despite the fact that they have a relatively poor phase noise performance (as mentioned in Chapter 2), ring oscillators are commonly used in many PLL applications, including wire-line communication, microprocessor clock generation, and wireless systems [43, 44].

In this work, a three-stage differential ring oscillator (Figure 3-10) is used for the VCO. The differential structure of the VCO reduces the common-mode noise effect, which improves
Chapter 3. Phase-Locked Loop Design Procedure

the system's overall jitter performance. Jitter (phase noise) increases as the number of stages of the VCO increases. The lower the number of stages, the higher the free running frequency of the VCO. The number of stages is typically chosen to be three or four [49]. By dissipating the same total power of the large number of stages in a smaller number of stages, one can achieve a better jitter/phase noise [49]. Hence, three stages are chosen for this design.

This VCO has a single control voltage that is used to set the desired output frequency. Figure 3-11 depicts the schematic of each stage of the VCO [45]. To have a high differential gain, a cross coupled PMOS pair is used as the active load of the differential stage [46].
Equation (3-5) shows the phase shift of each stage in an N-stage ring oscillator. In this design, N is equal to three. This means that the phase shift of each stage is 60°.

\[ 2N\Delta\phi = 360^\circ \Rightarrow \Delta\phi = \frac{180^\circ}{N} \]  

(3-5)

To the first-order approximation, the transfer function of each stage is:

\[ H_i(j\omega) = \frac{-A_0}{1 + \frac{s}{\omega_0}} \]  

(3-6)

Therefore, the overall transfer function is:

\[ L(j\omega) = \frac{-A_0^3}{\left(1 + \frac{s}{\omega_0}\right)^3} \]  

(3-7)

The circuit oscillates if the phase shift of each stage equals 60°. The frequency at which this occurs is given by (3-8). \( \omega_0 \) and \( \omega_{osc} \) are the 3-dB bandwidth of each stage and the VCO oscillation frequency, respectively. A low-frequency gain of 2 is needed per stage.

\[ \tan^{-1}\left(\frac{\omega_{osc}}{\omega_0}\right) = 60^\circ \]  

(3-8)

\[ \omega_{osc} = \omega_0\sqrt{3} \Rightarrow A_0 = 2 \]  

(3-9)

The time constant on each node is calculated in (3-10). \( C_L \) is the total capacitance at the output node of each stage that includes the drain parasitic capacitances of all of the transistors connected to the output node. The total resistance on each output node is calculated in (3-11).
Chapter 3. Phase-Locked Loop Design Procedure

\[ \tau = R_{on3,4,6} C_L \quad (3-10) \]

\[ R_{on} = \frac{V_{swing}}{I_D} \quad (3-11) \]

To improve the speed, low-swing architecture is chosen for the VCO. The choice of the output swing is influenced by several factors. There is a trade-off between speed and noise margins. A higher speed needs a lower output swing, while a better noise margin requires a higher swing [47]. In a simple differential pair with resistive PMOS loads shown in Figure 3-11, the gain of the stage is approximately equal to the product of \( g_m \) and \( R_L \), which has an inverse relation with \( (V_{GS} - V_{THN}) \). According to Equation (3-12), a low swing will require a low \( (V_{GS} - V_{THN}) \) bias voltage.

\[ \text{gain} = g_m R_L = \frac{I_{bias}}{V_{GS} - V_{THN}} \cdot \frac{V_{swing}}{I_{bias}} = \frac{V_{swing}}{V_{GS} - V_{THN}} \quad (3-12) \]

Some considerations limit the size of this output signal. First of all, the PMOS load transistors should stay in the triode region of operation, which needs a drain-to-source voltage \( (V_{DS}) \) that is kept below the \( V_{GS} - V_{THP} \) bias point of the PMOS transistors [47].

\[ V_{swing} < |V_{GS} - V_{THP}| \quad (3-13) \]

It is usually preferable to keep the load devices deep in the triode region over the entire range of the output voltage swing. This provides a more linear output resistance, which helps with the shape of the output waveforms, including the matching between the rising and falling shape of the output waveforms. It also guarantees a good performance over process variation. For this reason a smaller output swing is desired [47].

In addition to the above considerations, the output swing of each stage should be in the input voltage range of the next stage in the ring oscillator. This is required since the tail current
source of the next differential stage should remain in the saturation region. Typically, the output swing is considered larger than this value so that the transistor maintains in the desired region of operation. The tuning range of VCO defines the frequency range of the PLL.

\[ VCO \text{ Tuning Range} \geq 1.11 \text{ GHz} \quad (3-14) \]

The conversion gain of the VCO depends on two factors: the tuning range of the VCO and the range of the VCO control voltage. The VCO conversion gain can be obtained by:

\[
K_{vco} = \frac{2\pi(Frequency - tuning - range) \text{ rad}}{(Control - voltage - range) V} \quad (3-15)
\]

The calculated transistor widths were optimized by using the Cadence simulations. Table 7 summarizes the transistor sizes.

<table>
<thead>
<tr>
<th>Table 7. The transistor sizes in the VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>(W/L)_{1,4}</td>
</tr>
<tr>
<td>1.8\mu m/0.18\mu m</td>
</tr>
</tbody>
</table>

3.6. Divider Circuit

A programmable divider is needed for a wide tuning range as shown in Figure 3-1. Dividers are necessary to keep the VCO output frequency down to about the reference frequency at the input of the phase frequency detector. For this PLL, a divider with a division range of 32 to 63 is needed to produce the desired range of output frequencies. To achieve this division range, a number of 2/3 dividers are needed. A 2/3 divider circuit is a circuit that divides by 2 or 3, depending on a control input signal. These types of dividers are widely used in programmable
dividers to achieve a range of division ratios. First the divide-by-two circuit and then the 2/3 divider circuit will be discussed. Finally, the timing diagram of each circuit along with its schematic is presented.

As the divider has to operate at the VCO frequency, its power dissipation is of major concern. In this design, CML flip-flop topology is used. There are other topologies such as [22, 34]. However, CML circuits with resistor loads have higher speeds. Also, they require a low-swing clock, which is much easier to satisfy at higher frequencies. Additional speedup can be obtained by using inductor peaking. However, in this work, resistors are preferred because of the area constraint. Section 3.6.1 expresses the divide-by-2 schematic and timing diagram. Section 3.6.2 explains the circuit of the 2/3 divider and the schematic and operation of the chosen programmable divider used in this work.

3.6.1. Divide-by-2 Circuit

A divide-by-2 block is implemented using a toggle flip-flop, as shown in Figure 3-12. Frequency division by two is achieved by clocking these two latches. Figure 3-13 and Figure 3-14 show the schematic transistor level and the timing diagram of the flip-flop-based divide-by-2 circuit.

Figure 3-12. Architecture of a divide-by-2 circuit
The circuit operates as follows. The cycle starts when the clock signal is rising, \( \phi_2 \) is low, and its complement \( \phi_4 \) is high. These are the input signals of the left latch in Figure 3-13. In the first step, in the left latch, a current is directed into the latch’s differential amplifier portion to follow the input, i.e., \( \phi_1 \) rises to high and \( \phi_3 \) falls to low. At the same time, in the right latch, in order to hold the output of the latch, the current is directed into the latch’s cross-coupled pair portion. In the second step, in a similar process, the left latch goes to the hold mode while the right latch enters the track mode, and the process continues. In the third step, the same process repeats on the left side, but the voltage polarity is now reversed [37].
3.6.2. Divide-by-2/3 Circuit and the Programmable Divider Circuit

As stated before, for 32 to 63 division ratios, 2/3 divider cells are required. A 2/3 divider circuit is shown in Figure 3-15 [37].

![Figure 3-15. The schematic of a divide-by-2/3 circuit](image)

The function of the circuit is determined by the control bit 'CON*'. When CON*=0, the input signal frequency is divided by 2, while a CON*=1 causes a division ration of 3. To use the divider in a divider chain, the CON* input signal is generated by the output signals of the next cells in the chain. For this purpose, an end-of-cycle logic circuit is used. This logic circuit activates the CON* signal once in a division period [37, 41]. To further investigate this concept and to provide an example of a divider chain, an 8/9 divider is designed using a 2/3 divider followed by two dividers by 2, as shown in Figure 3-16, the end-of-logic circuit.

![Figure 3-16. Divider-by-8/9 schematic](image)
In this figure, there is an external input ‘CON’ to determine the division ratio, i.e., 8 or 9. Figure 3-17 shows the timing diagram for this divider. When the CON input is zero, the end-of-cycle logic circuit is disabled and no CON* pulse is generated. As a result, the 2/3 divider works as a divider by 2, and the complete circuit divides the input by 8. When the CON input is one, the end-of-logic circuit is enabled to find the end of a cycle; that is, when all the dividers’ outputs are zero, the CON* will be one. Thus, once in a division cycle the 2/3 works as a divide by 3. This results in a division by 9. In other words, we can say that when the CON input is one, one extra period of the input clock is ‘swallowed’ in the divider. Note that to achieve a divide by 9, the functionality of the end-of-logic circuit is important. By cascading a number of ‘n’ 2/3 division cells a division range of $2^n$ to $2^n+1-1$ can be achieved. Figure 3-18 shows the divider circuit for n=5 [23, 41].

![Figure 3-17. The signal diagram of dividing by 8/9 divider](image)

As Figure 3-16 shows if we replace the two dividers by 2 with two dividers by 2/3, we will get an 8 to 15 divider. This is because each divider can swallow ‘up to one’ clock period (depending on its CON input). Note that one clock period in the inputs of the second and the third dividers correspond to 2 and 4 input clock periods, respectively, because of the division function. Therefore, the combination of these 3 cascaded dividers can swallow up to $1 + 2 + 4$ or...
7 clock periods. This means that we have an 8 to 15 divider. Figure 3-18 shows the divider circuit for \( n=5 \) to achieve the desired range of 32 to 63.

![Figure 3-18. A 32 to 63 divider](image)

Generalizing this idea to a number of 'n' cascaded 2/3 division cells yields a division range of \( 2^n \) to \( 2^{n+1} - 1 \). The division ratio, \( N \), can be formulated as:

\[
N = 2^n + 2^{n-1}.CON_{n-1} + \ldots + 2^1.CON_i + 2^0.CON_0 \quad (3-16)
\]

The output signal period can be depicted as:

\[
T_{out} = N.T_{in} \quad (3-17)
\]

In (3-16) and (3-17), \( T_{in} \) is the period of the input signal, and \( CON_0, CON_1, \ldots, CON_{n-1} \) are the binary control voltages of the cells 0 to \( n-1 \), respectively. A division ratio of \( 2^n \) is achieved by an all-zero input, while an all-one input results in a division by \( 2^{n+1} - 1 \).

An example operation of the circuit in is shown in Figure 3-20, for \( N=42 \) (42 = 10101B). As a result, the 2\textsuperscript{nd} and the 4\textsuperscript{th} dividers ('B' and 'D' outputs) operate as divide by 2, while the other dividers operate as 2/3 dividers, depending on their control inputs.

The divider's power consumption can be reduced by combining the two circuits of the CML AND gate and the CML latch to achieve a CML latch-AND gate, as shown in Figure 3-19 [41]. The 2/3 divider can be modified by these combined circuits to achieve a faster speed and lower power consumption. One of the drawbacks of this circuit is the use of stacked NMOS
transistors. Because of the relatively low swing supply voltage, this circuit can be used in higher supply voltages.

Figure 3-19. The implementation of a Latch-AND gate
Figure 3-20. Divider output timing diagram for $N = 42$
Chapter 4

Simulation Results

This chapter presents the simulation results for the PLL and its building blocks. These simulations are performed using Cadence environment and Matlab tools. Table 8 summarizes the loop parameters of the PLL. The PLL system level phase noise is simulated using the “PLL Design Assistant” program [48]. Section 4.1 presents the correspondingly system level simulation results. Section 4.2 shows the PFD simulation results, including the transient behavior and the transfer characteristic. Section 4.3 reviews the VCO simulation results, including the tuning range and the transient waveforms for the VCO output and control voltage. Also, the transient response of the VCO control voltage is shown in this section. Section 4.4 shows the simulation results of the complete PLL for different division factors corresponding to the maximum and minimum operating frequencies of the PLL. Finally, Section 4.5 explains the different jitter measures along with the jitter measurements in the PLL by Matlab.
Table 8. Main parameters in the PLL design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CP}$</td>
<td>15$\mu$A</td>
</tr>
<tr>
<td>$K_{VCO}$</td>
<td>3.2e6</td>
</tr>
<tr>
<td>$C$</td>
<td>15pF</td>
</tr>
<tr>
<td>$C'$</td>
<td>3pF</td>
</tr>
<tr>
<td>$R$</td>
<td>10k$\Omega$</td>
</tr>
<tr>
<td>$K_{PFD}$</td>
<td>$1/2\pi$</td>
</tr>
<tr>
<td>PM</td>
<td>44.6°</td>
</tr>
</tbody>
</table>

4.1. General PLL Design

A systematic simulation of the PLL in Matlab provides the phase and gain margins of the PLL. Figure 4-1 illustrates the results. The magnitude diagram of the PLL transfer function shows two poles in the origin, which cause the phase diagram to start from -180°. The diagrams also represent a zero in the middle of the frequency range. This zero improves the stability of the system. Simulations show a phase margin (PM) of 42°, which meets the system’s stability requirements. The PLL loop’s phase margin and gain margin are obtained by examining the PLL transfer function using Matlab, as illustrated in Figure 4-1.
Chapter 4. Simulation Results

The “PLL Design Assistant Program” is provided as a self-extracting executable file that provides a graphical user interface for designing PLLs. This design is at the transfer function level. This program takes a desired closed-loop transfer function description as the input and calculates the open-loop parameters that must be chosen in the design. The other feature of this package is its ability to estimate the PLL noise performance by entering the noise parameters and observing the phase noise and the jitter of the PLL [48].

Figure 4-2 and Figure 4-3 show the step response and the phase noise simulation results, respectively. As Figure 4-3 shows the main contributor to the PLL phase noise is the VCO [49].
Chapter 4. Simulation Results

Also shown in the figure, PFD is the other building block, which has a considerable contribution in the phase noise. The measured rms jitter by this package is 13.7ps, which is within 10% of that of the simulation result in Cadence.

**Figure 4-2. Closed loop step response of the PLL**

**Figure 4-3. Output phase noise of the PLL**
4.2. PFD Simulation Results

PFD compares its two input signals and generates the UP and DN outputs based on the phase difference between its two inputs. Figure 4-4 shows the waveforms of the PFD signals in the closed loop PLL for an operating frequency of 2.25GHz. As illustrated in this figure, the rising edges of the reference and feedback signals generate the UP and DN signals, respectively.

As stated in Section 3.1, adding enough delay to the reset path of the PFD removes the dead zone in the PFD transfer characteristic, which is shown in Figure 4-5. This figure depicts...
Chapter 4. Simulation Results

the difference between the average values of UP and DN signals versus the phase difference between the two inputs.

Figure 4-5. PFD transfer characteristic

4.3. VCO Simulation Result

The VCO's tuning range is calculated by running a parametric simulation over the entire range of the VCO control voltage. Simulations show that a range of 0.4 to 1.4V for the control voltage results in a tuning range of 750MHz to 4GHz for the VCO. However, in this design a smaller frequency range of 1.14GHz to 2.25GHz is used, which corresponds to the 0.68V to 1.03V control voltage. Figure 4-6 illustrates the VCO frequency-voltage conversion curve. The gain of the VCO in the desired frequency range is 3.2GHz/V.
Figure 4-6. VCO tuning range

Figure 4-7 and Figure 4-8 show the transient output signal of the VCO at both ends of the frequency range, i.e., 1.14GHz and 2.25GHz. Simulations over a number of control voltages in this range show that the output amplitude of the PLL is almost constant. This is confirmed by the waveforms in Figure 4-7 and Figure 4-8.
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Figure 4-7. The transient response of the VCO at 1.14GHz

Figure 4-8. The transient response of the VCO at 2.25GHz
Chapter 4. Simulation Results

One of the noisy signals in the PLL is the VCO control voltage. Figure 4-9 shows the VCO control voltage under the lock condition. The ripples on the waveform are due mainly to the switching behavior of the charge pump. However, the UP and DN current mismatch could also increase the ripples. These ripples are attenuated (smoothed) by the loop filter. The amplitude of the ripples on the control voltage in the steady state is 28mV. As shown in Figure 4-9, the lock-in time for the control voltage is less than 700ns.

![Figure 4-9. Lock-in time transient of the VCO control voltage](image)

Figure 4-9 illustrates the waveforms of UP and control voltage signals. This figure shows how the control voltage of the VCO, which is the LF’s output, responds to the UP signal, which is the input signal of the charge pump. When the UP signal is high, the capacitor in the LF is charged to a higher voltage. This capacitor is discharged when the UP signal is low.
Finally, a phase noise measurement is performed on the circuit. For this purpose, the VCO is simulated in free running mode in a centre frequency of 1.53GHz, which corresponds to a 0.9V control voltage. Figure 4-11 represents the simulation results. The measured phase noise of the VCO is around -62.75dBc/Hz @1MHz.
4.4. PLL Simulation Results

The complete circuit of the PLL, including the divider, is simulated for N=63. Figure 4-12 shows the PLL internal waveforms, including UP, DN, and the output and control voltage of the VCO. To analyze the transient behavior when the divider's division ratio changes, a simulation is performed with N=32 and N=63. Figure 4-12 shows changes in the control voltage due to the switching in the divider's division ratio. As illustrated in the figure, the lock time of the PLL in the switching from N=63 to N=32 is less than 700ns.

Figure 4-11. Phase noise of a free running VCO
Chapter 4. Simulation Results

Figure 4-12. The transient response of the major signals in the PLL

Figure 4-13. The response of the control voltage of the VCO to the divider control bit switching
Chapter 4. Simulation Results

As a complementary step in the design of the PLL, the circuit must be tested in process, temperature, and supply voltage variations. Table 9 gives the results of the PLL simulation in four process corners and three different temperatures. The process corners are SS (slow PMOS/slow NMOS), FF (fast PMOS/fast NMOS), FS (fast PMOS/slow NMOS), SF (slow PMOS/fast NMOS). Also, Table 9 shows the simulation results for a typical (T) process.

Table 9. Impact of process and temperature variations on PLL output frequency

<table>
<thead>
<tr>
<th>PMOS</th>
<th>NMOS</th>
<th>Temperature</th>
<th>Minimum Frequency (GHz)</th>
<th>Maximum Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>T</td>
<td>0</td>
<td>1.161</td>
<td>2.29</td>
</tr>
<tr>
<td>T</td>
<td>T</td>
<td>27</td>
<td>1.14</td>
<td>2.25</td>
</tr>
<tr>
<td>T</td>
<td>T</td>
<td>70</td>
<td>1.118</td>
<td>2.205</td>
</tr>
<tr>
<td>S</td>
<td>S</td>
<td>0</td>
<td>1.087</td>
<td>2.251</td>
</tr>
<tr>
<td>S</td>
<td>S</td>
<td>27</td>
<td>1.077</td>
<td>2.23</td>
</tr>
<tr>
<td>S</td>
<td>S</td>
<td>70</td>
<td>1.066</td>
<td>2.209</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>0</td>
<td>1.256</td>
<td>2.358</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>27</td>
<td>1.205</td>
<td>2.262</td>
</tr>
<tr>
<td>F</td>
<td>F</td>
<td>70</td>
<td>1.154</td>
<td>2.167</td>
</tr>
<tr>
<td>S</td>
<td>F</td>
<td>0</td>
<td>1.1084</td>
<td>2.32</td>
</tr>
<tr>
<td>S</td>
<td>F</td>
<td>27</td>
<td>1.1064</td>
<td>2.316</td>
</tr>
<tr>
<td>S</td>
<td>F</td>
<td>70</td>
<td>1.1044</td>
<td>2.27</td>
</tr>
<tr>
<td>F</td>
<td>S</td>
<td>0</td>
<td>1.188</td>
<td>2.205</td>
</tr>
<tr>
<td>F</td>
<td>S</td>
<td>27</td>
<td>1.175</td>
<td>2.181</td>
</tr>
<tr>
<td>F</td>
<td>S</td>
<td>70</td>
<td>1.161</td>
<td>2.157</td>
</tr>
</tbody>
</table>
To find the sensitivity of the circuit to supply variation, a ±10% change in the power supply voltage is applied to the circuit. Figure 4-14 and Figure 4-15 show the related waveforms. The simulation results show that the output frequency is almost independent of the supply voltage, when the change in supply is within 10%. In fact, supply variations are compensated by the changes in the VCO control voltage. Table 10 tabulates the changes in the range of VCO control voltages due to the supply variations.

Figure 4-14. The effect of a 10% increase in supply voltage on the PLL transient response (VDD=1.98V)
Chapter 4. Simulation Results

Figure 4-15. The effect of a 10% decrease in supply voltage on the PLL transient response (VDD=1.62V)

Table 10. Simulation results for 10% variation in supply voltage

<table>
<thead>
<tr>
<th>Power Supply Voltage (V)</th>
<th>VCO Voltage Control Range (V)</th>
<th>Frequency Range (GHz)</th>
<th>Output Amplitude Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.98</td>
<td>0.73 - 1.15</td>
<td>1.139-2.267</td>
<td>1.1</td>
</tr>
<tr>
<td>1.8</td>
<td>0.67 - 1.05</td>
<td>1.14-2.25</td>
<td>1</td>
</tr>
<tr>
<td>1.62</td>
<td>0.525 - 0.871</td>
<td>1.14-2.248</td>
<td>0.977</td>
</tr>
</tbody>
</table>
Chapter 4. Simulation Results

4.5. Jitter Measurement

Timing jitter has been the subject of many studies. Different models exist that predict the jitter of the PLL based on the internal circuit blocks of the PLL. Several circuit blocks are typically fabricated on the same substrate. PLL operates from the global supply voltage and ground, experiencing both substrate and supply noise. This noise reveals itself as jitter in the output of the PLL. The building blocks of the PLL contribute different amounts of noise to the output, but VCO plays the dominant role in the amount of the jitter. Ring oscillators are increasingly being used in jitter sensitive applications because of their speed, ease of integration, and wide tuning range. Several studies have been done specifically on jitter and phase noise in ring oscillators [50, 51, 52]. Cycle-to-cycle jitter, cycle jitter, and long-term jitters, explained in Chapter 2, have been measured for both ends of the PLL tuning range in Matlab. Table 11 presents the results.

<table>
<thead>
<tr>
<th>Jitters (ps)</th>
<th>Output Frequency =1.14GHz</th>
<th>Output Frequency =2.25GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle-to-cycle</td>
<td>2.38</td>
<td>3.02</td>
</tr>
<tr>
<td>Long-term</td>
<td>6.35</td>
<td>7.06</td>
</tr>
<tr>
<td>Cycle</td>
<td>12.77</td>
<td>14</td>
</tr>
<tr>
<td>Peak-to-peak</td>
<td>22.7</td>
<td>24.2</td>
</tr>
</tbody>
</table>

One of the most popular and efficient representations of the jitter is the eye diagram, which is a composite view of several periods of a captured waveform. Based on time domain jitter analysis (eye diagram), deterministic jitter can be calculated. Deterministic jitter can be defined as the worst-case difference between a determined crossing point and a rising (or falling)
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This eye diagram shows a non-symmetric waveform that has different falling and rising edges, which indicates the presence of deterministic jitter. Figure 4-16 illustrates the eye diagram for the PLL output. In this figure, the outer distance of the rising and falling edges represents the total deterministic jitter. As measured in this eye diagram, the mean value of the deterministic jitter is 25ps, which is compatible through the related formulas, with the measured result in Table 11. Figure 4-17 illustrates the magnified eye diagram of the output of this work, which is the cross point of the differential outputs.

![Eye Diagram](image)

**Figure 4-16. Eye diagram for the designed PLL**

**Figure 4-17. The magnified eye diagram**

4.6. Post-Layout Simulations

The PLL is designed and laid out in a 0.18µm CMOS technology. The layout of the entire PLL including the loop filter is shown in Figure 4-18. The overall die area of the PLL is 0.023mm².
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Figure 4-18. Layout of the entire PLL including the LF

The extracted view of the layout has been also simulated and in general the post-layout simulations are in a good agreement with the corresponding pre-layout ones. For example, Figure 4-19 shows the post-layout simulation results for the VCO control voltage. In this simulation, the divider ratio is changed between its two extreme values, 32 and 63. As shown in Figure 4-19, the PLL can follow this frequency change and the lock-in time is less than 700ns, which is very close to the pre-layout simulation results. It should be mentioned that the voltage ripple on the control voltage is slightly bigger than that of the pre-layout simulation results (by 2.5%). Figure 4-20 shows the post-layout simulation results for the PFD signals, UP and DN.
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Figure 4-19. Post-layout simulation result for the VCO control voltage

Figure 4-20. Post-layout simulation results for PFD signals
Chapter 5

Conclusion and Future Work

This thesis presents the design of a fully differential low-swing charge pump phase-locked loop that operates in the frequency range of 1.14GHz to 2.25GHz. The target technology for this design is 0.18μm CMOS. Fully differential low-swing design structure improves the system immunity to common-mode noise (power supply noise), while facilitating high speed of operation. To operate with low-swing signals, most of the building blocks of the PLL are designed in CML. Although at low frequencies, CMOS CML circuits usually suffer from high power consumption in comparison with the standard CMOS gates, as the CML's power consumption remains relatively constant with increasing frequency. Therefore, at high frequencies CML circuits demonstrate a better performance as compared to the standard CMOS gates.

Voltage-controlled oscillator is one of the key elements in the PLL design. LC-oscillators show a very good phase noise performance, while they occupy a large space and also, their tuning range is limited. Therefore, non-LC based ring oscillator is chosen for the VCO. To reduce the power and noise contribution of the VCO, three stages are used in the ring oscillator.

To make sure that the PLL locks only to the fundamental component of its input frequency, a tri-state PFD implemented in CML is used in this design. Since this PLL is intended
for a wide tuning range application, a divider with variable division ratio is required. To address this, a 5-bit programmable divider is designed to be used in the feedback path of the PLL.

The PLL is simulated with an input reference frequency of 35MHz. With a division ratio of 32 to 63, an output frequency of 1.14 to 2.25GHz is achieved. Simulations show an approximately constant power consumption of 14.5mW over the entire tuning range. The phase noise of the free running VCO is -62dBc/Hz @ 1MHz. The deterministic jitter for the output of the PLL is 25ps. The worst-case locking time in the complete frequency range is 700ns.

Low-swing design in all the building blocks of the PLL results in higher-speed of operation. Simulation results show a maximum operating frequency of 4GHz for the designed VCO of the PLL. Thus, with some modifications, the entire PLL circuit can operate in the frequencies up to 4GHz. By changing the divider to one that is capable of larger division increments, this PLL can have higher output frequencies.

Experimental test and verification of the proposed PLL should also be performed. In addition, the sensitivity of the PLL to power supply and substrate noise should be verified in practice. It should be noted that testing of PLL circuits, at both prototyping and production stages, is a challenging task and is an active area of research [53, 54, 55, 56, 57].

Another possible extension to this work is to reduce the power consumption in the divider; using techniques that can decrease the current through biasing resistors in the low-frequency stages of the divider can make an immediate impact.
Bibliography


Bibliography


