REPRESENTATION OF MULTIVARIABLE-CONTROLLED MOSFET NONLINEARITIES IN TRANSIENT ANALYSIS PROGRAMS

By

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We accept this thesis as conforming to the required standard

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Abstract

This thesis deals with the modelling and circuit simulation problems of nonlinear electronic devices. Emphasis has been aimed at MOSFET devices.

A Piecewise Linear (PWL) modelling scheme has been proposed for a general four-terminal nonlinear charge device. The charge functions are all nonlinear and are approximated by PWL functions. If analytical expressions for the nonlinear functions are not available, PWL function approximations can be built from a data table in which discrete data points are recorded.

In the time domain, the critical-damping-adjustment (CDA) scheme is used as the integration rule in the discretization of dynamic charge devices.

Piecewise linear modelling combined with the CDA integration scheme gives a fast yet adequately accurate simulation algorithm. The algorithm is based on linear analysis because the entire circuit becomes linear with PWL modelling of nonlinear elements. In order to avoid an iterative solution, PWL region extrapolation is permitted when the circuit solution switches PWL regions. The extrapolation approximation will generate an overshoot error in the solution vector. However, with caution in the selection of the integration step size, the error can be limited to an acceptable range.

Two types of MOSFETs have been modelled and simulated with the algorithm introduced in this thesis, and satisfactory results have been obtained as compared to Newton's iteration solutions.
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Direct time domain nonlinear dynamic circuit simulation involves two aspects: one is the time domain discretization of the differential equations which model the dynamic devices; the other is the solution of nonlinear algebraic circuit equations.

Generally, one can first formulate the circuit by a set of differential-algebraic equations by any one of the circuit analysis approaches\(^1\), then use the above two steps to compute time domain solutions. But a practical and convenient way is to discretize and linearize each nonlinear device model itself. After discretization and linearization, each nonlinear dynamic component can be modelled by a linear companion circuit; thus, the entire circuit can be formulated by a set of linear algebraic equations. Therefore linear analysis techniques can be applied directly to compute the time domain solutions of the nonlinear circuits and systems.

1.1 Time domain discretization

Most dynamic devices in today's electronic circuits can be described by first-order differential equations. For example, a two-terminal linear inductor can be described by

\[
v_L(t) = L \frac{di_L(t)}{dt}
\]  

(1.1.1)

and a two-terminal linear capacitor can be described by

\[
i_C(t) = C \frac{dv_C(t)}{dt},
\]  

(1.1.2)

where L and C are a constant inductance and a constant capacitance. If the inductor and capacitor

\(^1\) Nodal analysis approach will be used throughout the entire thesis.
are nonlinear devices, the differential relations above have to be changed to the following:

\[ v_L(t) = \frac{d\phi_L(t)}{dt} \]  \hspace{1cm} (1.1.3)

for the nonlinear inductor, and

\[ i_C(t) = \frac{dq_C(t)}{dt} \]  \hspace{1cm} (1.1.4)

for the nonlinear capacitor. In these equations, \( \phi_L = \phi_L(i_L(t)) \) and \( q_C = q_C(v_C(t)) \) are nonlinear functions.

In a time domain step-by-step digital computer solution, the differential equations have to be approximated by finite difference formulas, namely, numerical integration rules. This transformation of device models from continuous differential form into approximated discrete form is time domain discretization.

The trapezoidal integration rule and the Backward Euler (BE) integration rule are the two most often used discretization rules in today's popular circuit simulators. They are implicit and easy to implement. More importantly, they are A-stable [4]. According to [15][33], the trapezoidal rule exhibits overall better numerical properties than BE rule both in the time domain and the frequency domain. But a major shortcoming of the trapezoidal rule is its lack of numerical oscillation damping capability. High frequency artificial numerical oscillation, which can be superimposed on the normal solution waveform, will occur whenever there is a discontinuity of the circuit variables during the simulation. In [33], the critical-damping-adjustment (CDA) scheme, a combination of trapezoidal rule and BE rule, was proposed to suppress such numerical oscillations. In piecewise linear circuit simulation, the CDA scheme suppresses artificial numerical oscillations in two consecutive BE steps by exploiting the strong damping capability of the BE integration rule. This technique maintains the computational accuracy of the trapezoidal rule within linear regions. BE integration is only invoked at the moment when the solution vectors of the circuit are found to have switched from one linear
Chapter 1. Introduction

region into another. In this thesis, the CDA scheme will be used as the integration rule for the discretization of a Piecewise Linear (PWL) multi-terminal multi-voltage controlled charge device model.

To illustrate the discretization process, we can take the linear capacitor as an example. Integrating equation (1.1.2) from \( t-\Delta t \) to \( t \), we get

\[
\int_{t-\Delta t}^{t} i_C(t) dt = C \int_{t-\Delta t}^{t} \frac{dv_C(t)}{dt} dt.
\]  

(1.1.5)

Applying the trapezoidal rule to approximate the integral into a finite difference relation yields

\[
\frac{i_C(t) + i_C(t-\Delta t)}{2} \Delta t = C[v_C(t) - v_C(t-\Delta t)].
\]  

(1.1.6)

If the BE rule is applied, we then get

\[
i_C(t)\Delta t = C[v_C(t) - v_C(t-\Delta t)].
\]  

(1.1.7)

Since the circuit variables at \( t-\Delta t \) are known during the solution at time \( t \), the above approximate difference equations can be rewritten into a more compact form:

\[
i_C(t) = a_C v_C(t) + b_C.
\]  

(1.1.8)

A companion equivalent circuit can be set up for this linear capacitor according to equation (1.1.8), as shown in Figure 1.1.1.
Chapter 1. Introduction

Figure 1.1.1 Companion circuit for a linear capacitor

where the constants $a_C$ and $b_C$ are given by:

For the trapezoidal rule

\[
    a_C = \frac{2C}{\Delta t} \\
    b_C = -\frac{2C}{\Delta t} v_C(t - \Delta t) - i_C(t - \Delta t) ;
\]

For the BE rule

\[
    a_C = \frac{C}{\Delta t} \\
    b_C = -\frac{C}{\Delta t} v_C(t - \Delta t) .
\]

However, if the capacitor is a nonlinear one, the discretization of equation (1.1.4) leads to the following compact form:

\[
    i_C(t) = a'_C q(t) + b'_C
\]

where the constants $a'_C$ and $b'_C$ are given by:
Chapter 1. Introduction

For the trapezoidal rule

\[ a'_C = \frac{2}{\Delta t} \]
\[ b'_C = -\frac{2}{\Delta t} q_C(t - \Delta t) - i_C(t - \Delta t) \]  

(1.1.12)

For the BE rule

\[ a'_C = \frac{1}{\Delta t} \]
\[ b'_C = -\frac{1}{\Delta t} q_C(t - \Delta t) \]  

(1.1.13)

Since \( q_C(t) \) is a nonlinear function of \( v_C(t) \), the voltage across the capacitor, the companion equivalent circuit will not be as simple as the one shown in Figure 1.1.1. The linear conductor in Figure 1.1.1 has to be replaced by a nonlinear conductor which has an i-v characteristic of \( a'_C q_C(t)/v_C(t) \) or replaced by a voltage controlled current source with a nonlinear amplitude of \( a'_C q_C(t) \).

At each time point \( t \), after each dynamic device (linear or nonlinear) has been discretized, the entire circuit becomes a resistive circuit represented by a set of algebraic equations,

\[ F[v(t)] = u(t) \]  

(1.1.14)

where \( F \) is a matrix function, \( v(t) \) is the node voltage vector, \( u(t) \) is the source vector. \( F \) could be linear or nonlinear. It depends on the characteristics of the devices in the circuit. If one or more devices are nonlinear (static or dynamic), then \( F \) would be nonlinear.

To make use of the linear analysis techniques, or to make \( F \) become a linear matrix function, linearization procedures have to be applied to the nonlinear characteristics of the devices.

1.2 Linearization

The most widely used local linearization technique in solving nonlinear problems is Newton's iteration. Take the nonlinear capacitor as an example. Apply Taylor's expansion to equation
Chapter 1. Introduction

(1.1.11) at time point \( t \) and discard the higher order terms. We can then get the locally linearized approximation to the original nonlinear function \( i_C(t) \) at an initial or intermediate iterative voltage point \( v_C^0(t) \):

\[
i_C^1(t) = i_C^0(t) + \left[ \frac{d i_C(t)}{d v_C(t)} \right]^0 [v_C^1(t) - v_C^0(t)] ,
\]

(1.2.15)

where the superscript "0" represents the circuit variables at the previous iterative step, and "1" represents the circuit variables at the current iterative step which are to be solved for. \( v_C^0(t) \) can be found by substituting \( v_C^0(t) \) into equation (1.1.11):

\[
i_C^0(t) = a'_C q_C(v_C^0(t)) + b'_C
\]

(1.2.16)

where \( a'_C \) and \( b'_C \) are related to time discretization step size \( \Delta t \) and the circuit variables at the last time point \( t-\Delta t \), these values are known at time point \( t \). Since \( i_C(t) \) is a nonlinear function of \( v_C(t) \) through the representation of charge \( q_C(t) \), the derivative of \( i_C(t) \) with respect to the controlling variable \( v_C(t) \) in equation (1.2.15) can be found as follows:

\[
\left[ \frac{d i_C(t)}{d v_C(t)} \right]^0 = a'_C \left[ \frac{d q_C(t)}{d v_C(t)} \right]^0
\]

(1.2.17)

Then the locally linearized equation (1.2.15) can be further written into a compact form,

\[
i_C^1(t) = a''_C v_C^1(t) + b''_C
\]

(1.2.18)

where \( a''_C \) and \( b''_C \) are given by

\[
a''_C = a'_C \left[ \frac{d q_C(t)}{d v_C(t)} \right]^0
\]

\[
b''_C = \left[ a'_C q_C(v_C^0(t)) + b'_C \right] - a''_C v_C^0(t).
\]

(1.2.19)
After each nonlinear device is linearized, the matrix function $F(t)$ of the entire discretized circuit becomes linear. *Newton's iteration* solution will be successfully completed at each time point when a convergence is reached. The criteria for the convergence usually takes the following form

$$\| v^1(t) - v^0(t) \| < \epsilon ,$$

(1.2.20)

where $\epsilon$ is a pre-defined small positive number.

Two factors are crucial for *Newton's iteration* to be successful in reaching a convergence quickly. One factor is the initial guess of node voltage $v(t)$; the other is the existence of derivatives of nonlinear functions of the discretized current with respect to the controlling voltages. The second factor requires that the nonlinear charge functions be smooth along each dimension of the controlling voltages in the nonlinear device model. Many simulators employing *Newton's iteration* require the nonlinear functions to be $C^1$ smooth [35]. If the initial guess of $v(t)$ is far off from the real solution, or if the nonlinear characteristics of the devices are not smooth enough, *Newton's iteration* may not converge, in the sense that the criteria in (1.2.20) will never be satisfied within a certain amount of iteration steps. In practice, it is not uncommon that a nonlinear circuit simulation session will fail to converge due to the above reasons.

Furthermore, even with well-constructed analytical models for the nonlinear devices, *Newton's iteration* still needs three to four steps to converge. These extra computation steps slow down the speed of simulators which employ *Newton iteration* as their nonlinear solution algorithms.

Finally, since our concern is in the time domain analysis of nonlinear circuits, the time step size plays an important role in the solutions. As can be seen from discretized equation (1.2.11), the nonlinear characteristics of the devices are related to the time step size as well as to the integration rule used. Generally, a small time step size will help the convergence of the *Newton's iteration* algorithm.
Chapter 1. Introduction

1.3 Objectives

The objective of this work is to find a modelling and solution method for nonlinear electronic devices in time domain simulations.

Realizing the disadvantages of using Newton's iteration as the linearization tool in time domain nonlinear circuit analysis modelling, we will use instead a PWL approximation technique. We will apply this technique to the modelling of a four-terminal multi-voltage controlled nonlinear charge device in time domain circuit simulation. Since PWL modelling of the charge device for time domain solutions will cause abrupt changes of the capacitive parameters when switching PWL regions, the CDA scheme is adopted as the integration technique to suppress the numerical oscillations when this happens. The immediate application of the proposed PWL modelling and time domain solution algorithm is to the MOSFET intrinsic device and its circuit simulation.

In the latter part of the thesis, the PWL approximation technique is also applied to the modelling of power MOSFETs (VDMOSTs).

1.4 Organization of this thesis

In chapter 2, a PWL model is presented for a four-terminal multi-voltage controlled charge device based on the simplicial division [7][6] of the controlling voltage space.

PWL modelling and solution algorithm is proposed in chapter 3 for the nonlinear charge device defined in chapter 2 in time domain circuit simulation.

In chapter 4, we first give a brief review of the modelling of the MOSFET intrinsic device, then the algorithm proposed in chapter 3 is applied to MOSFETs in simulation examples. Comparison simulation examples with the Newton's iteration solution are also given in this chapter.

VDMOST PWL modelling and simulation examples are discussed in chapter 5.

Finally, chapter 6 concludes the thesis.
Chapter 2

PWL Modelling of A Four-Terminal Nonlinear Charge Device

PWL modelling of nonlinear functions has been studied for many years. Since PWL modelling is an interpolation approximation technique, it only needs discrete data points on which the PWL functions are interpolated to approximate the original nonlinear functions. The data points can be obtained by physical measurement of the device or by theoretical calculations from the nonlinear analytical expressions describing the physics of the device or by numerical simulations of the device. The resolution of PWL approximations can be freely controlled by the designer so that a good compromise between computational speed and solution accuracy are attained.

2.1 Definition of a four-terminal nonlinear charge device

A four-terminal multi-voltage controlled charge device is shown in figure 2.1.1.

![Figure 2.1.1 A four-terminal charge device](image)
Chapter 2. *PWL Modelling of A Four-Terminal Nonlinear Charge Device*

In this Figure $v_a$, $v_b$, $v_c$ and $v_d$ are terminal voltages with respect to a datum point in the circuit. $i_a$, $i_b$, $i_c$ and $i_d$ are terminal currents. The directions of the terminal currents are assumed as indicated in the Figure. These voltages and currents are governed by KVL and KCL as follows:

**KVL:**

\[ v_{ab} + v_{bc} + v_{cd} + v_{da} = 0 ; \]  

\[(2.1.1)\]

**KCL:**

\[ i_a + i_b + i_c + i_d = 0 . \]  

\[(2.1.2)\]

There are only three independent terminal voltage drops and three independent terminal currents because of KVL and KCL. We also assume that the terminal currents are generated by the corresponding device charges attached to each terminal. Furthermore, we assume that all terminal charges are multi-voltage controlled nonlinear functions of three terminal voltage drops. Selecting terminal $a$ as the positive reference terminal for the controlling voltage variables, the nonlinear charge functions are generally assumed in the following form:

\[ Q_a = Q_a(v_{ab}, v_{ac}, v_{ad}) \]
\[ Q_b = Q_b(v_{ab}, v_{ac}, v_{ad}) \]
\[ Q_c = Q_c(v_{ab}, v_{ac}, v_{ad}) \]
\[ Q_d = Q_d(v_{ab}, v_{ac}, v_{ad}) . \]  

\[(2.1.3)\]

Since we have assumed that the individual terminal currents are generated by their own charges, from KCL equation (2.1.2), we can get the charge neutral equation

\[ Q_a + Q_b + Q_c + Q_d = 0 \]  

\[(2.1.4)\]
Chapter 2. PWL Modelling of A Four-Terminal Nonlinear Charge Device

The major task in this chapter is to approximate these nonlinear charges by PWL models.

### 2.2 Simplicial partitioning of the voltage space

The basis of the PWL approximation to an arbitrary monotonic continuous nonlinear function is the partitioning of the multidimensional controlling voltage space.

First the three dimensional controlling voltage space \([v_{ab}, v_{ac}, v_{ad}]\) is partitioned into cubes. Then each cube is partitioned into six polyhedral simplices which are defined by the vertices and hyperplanes of the polyhedrons.

These polyhedral PWL regions are not overlapping within the entire range of controlling voltage space considered. Figure 2.2.2 shows the partitioning of the voltage space in three dimensions.

![Simplicial partitioning of controlling voltage space](image)

Figure 2.2.2 Simplicial partitioning of controlling voltage space

Suppose an equal resolution partitioning scheme for each voltage dimension is employed. A
PWL voltage cube is defined by

\[(n_i - 1)\Delta V_{ab} \leq v_{ab} \leq n_i \Delta V_{ab}\]
\[(n_j - 1)\Delta V_{ac} \leq v_{ac} \leq n_j \Delta V_{ac}\]  \hspace{1cm} (2.2.5)
\[(n_k - 1)\Delta V_{ad} \leq v_{ad} \leq n_k \Delta V_{ad}\]

where \(n_i, n_j, n_k\) are the cube numbers in voltage dimensions \(v_{ab}, v_{ac}\) and \(v_{ad}\), respectively. \(\Delta V_{ab}, \Delta V_{ac}\) and \(\Delta V_{ad}\) are the partitioning resolutions in each voltage dimension. The resolutions may be different from each other and can be decided based on the characteristics of the actual devices considered. For simplicity, equal voltage partitioning resolution for all the dimensions is used in the simulations in this thesis. Total PWL Cube numbers can be easily determined after having chosen \(\Delta V_{ab}, \Delta V_{ac}\) and \(\Delta V_{ad}\)

\[N_i = \frac{V_{abmax} - V_{abmin}}{\Delta V_{ab}}\]
\[N_j = \frac{V_{acmax} - V_{acmin}}{\Delta V_{ac}}\]  \hspace{1cm} (2.2.6)
\[N_k = \frac{V_{admax} - V_{admin}}{\Delta V_{ad}}\]

where \(V_{abmax} (t = b, c, d)\) are higher ends of the voltage dimensions; while \(V_{abmin} (t = b, c, d)\) are lower ends of the voltage dimensions. It must be pointed out that if a non-equal partitioning scheme on each voltage dimension is used, a multidimensional data table should be set up to store the voltages and nonlinear charge function values (experimental results or device numerical simulation results) at these data points. The higher the resolution, the larger the data-table. Equal size partitioning of voltage space is used without explicit mentioning in the explanations that follow.

In each cube, there can be six non-overlapping polyhedral regions as shown in Figure 2.2.2. Each of them is delimited and designated by four vertices as follows:

R1: vertex[7651]
R2: vertex[7261]
R3: vertex[7321]
R4: vertex[7581]
R5: vertex[7841]
R6: vertex[7341]

PWL regions obtained as above are said to be proper since the vertex matrix of each PWL polyhedron

$$[V] = \begin{bmatrix} V_1 & V_2 & V_3 & V_4 \\ 1 & 1 & 1 & 1 \end{bmatrix}$$

(2.2.7)

is non-singular. In this matrix $V_i$'s ($i = 1,2,3,4$) are the coordinate vectors of the four vertices of one PWL polyhedron [6]. This property of non-singularity ensures the success of PWL interpolation over the polyhedrons.

### 2.3 Charge representation in PWL regions

After having partitioned the voltage space into polyhedral PWL regions, in each PWL region, the original nonlinear charge functions can be approximated by linearly interpolated functions as follows:

$$Q_j^{PWL} = C_{j1}v_{ab} + C_{j2}v_{ac} + C_{j3}v_{ad} + Q_{jo}$$

(2.3.8)

where $Q_j^{PWL} = Q_j$ at the vertices of a PWL region. Nonlinear terminal charge functions are thus linearized by interpolation within each PWL region. Compared to the small-signal linearization during Newton's iteration solutions, this is a large-signal linearization of nonlinear functions. The parameters, $C_j$, and $Q_{jo}$, in the linear expressions of charge functions have to be identified in their residing PWL region by data at the four vertices that form the PWL region. Since

$$Q_j = Q_j(v_{ab}, v_{ac}, v_{ad})$$

(2.3.9)
The four vertices are

\[ Q^i_j = Q^i_j(v^i_{ab}, v^i_{ac}, v^i_{ad}) \]

\[ i = 1, 2, 3, 4 \]

\[ j = a, b, c, d . \] (2.3.10)

Substituting into equation (2.3.8), we can identify the linear coefficients for each terminal charge function. We need to solve a set of linear equations

\[
[Q] = [V][C] \tag{2.3.11}
\]

where \([Q]\) is the charge vector on the four vertices, \([C]\) is the linear coefficients to be identified, and \([V]\) is the vertex matrix mentioned in equation (2.2.7). Since matrix \([V]\) is non-singular, \([C]\) can be found from

\[
[C] = [V]^{-1}[Q] . \tag{2.3.12}
\]

If the original nonlinear charge functions are continuous over the entire voltage space considered, then the PWL charge approximations obtained as above have the following properties [6]:

1. For any given small number \(\epsilon > 0\), a PWL cube division can be chosen such that

\[
\left\| Q_j - Q_j^{PWL} \right\| \leq \epsilon \tag{2.3.13}
\]

exists in the entire region.

2. The PWL charge functions \(Q_j^{PWL}\) are continuous over the entire voltage space considered.
Property 1 assures that if the voltage partitioning resolution is small enough, the PWL function approximation will be close enough to the original nonlinear function. Hence, the PWL solution will approach the actual solution of the circuit.

By approximating nonlinear charge devices with PWL functions, the nonlinear analysis problem is transformed into a linear analysis problem in the large-signal sense within each PWL region. This transformation greatly simplifies the time domain solution of a circuit which involves such devices. This aspect will be shown in the next chapter.
Chapter 3

Time Domain Solution Algorithm of PWL Circuits

Time domain solution of nonlinear circuits involves discretization and linearization. For PWL systems, since the characteristics of the nonlinear devices have been modelled by linear functions within each PWL region, the solution process at each time point is a straight-forward linear analysis. To ensure the proper representation of PWL models of nonlinear devices, the crucial point is to check the position of the solution vectors.

3.1 Time domain solution of PWL models

In time domain circuit simulation, discretized i-v relationships for each PWL device have to be found in order to form circuit equations. The terminal currents for the charge device are given by the definition

\[ i_j(t) = \frac{dQ_j^{PWL}(t)}{dt} \quad j = a, b, c, d \]

(3.1.1)

All the terminal charges are nonlinear functions of controlling voltages \( v_{ab}(t) \), \( v_{ac}(t) \) and \( v_{ad}(t) \). Note that although the nonlinear charges have been linearized by PWL functions, the PWL linear expressions of the charges can’t be substituted into the differential relations above because the PWL functions are not purely linear functions over the entire range of the voltage space. During the solution process, the linear capacitive coefficients are changing from one PWL region to another. This fact has to be included in the time domain discretization process by using the charge variable directly instead of its linear expression.

Applying the trapezoidal integration rule to directly discretize the first-order differential equations in (3.1.1), we get
Chapter 3. Time Domain Solution Algorithm of PWL Circuits

\[
\begin{align*}
    i_j(t) &= \frac{2}{\Delta t} Q_j^{PWL}(t) - \frac{2}{\Delta t} Q_j^{PWL}(t - \Delta t) - i_j(t - \Delta t) \\
    j &= a, b, c, d .
\end{align*}
\tag{3.1.2}
\]

Rewriting into a compact form, we obtain

\[
\begin{align*}
    i_j(t) &= \frac{2}{\Delta t} Q_j^{PWL}(t) + I_{hj} \\
    j &= a, b, c, d ,
\end{align*}
\tag{3.1.3}
\]

where \( I_{hj} \) represents the last two terms in equation (3.1.2). Substituting \( Q_j^{PWL}, j=a,b,c,d, \) into equation (3.1.3), we get linear relationships between terminal currents \( i_j \) and terminal voltages \( v_j \).

\[
\begin{align*}
    i_j(t) &= G_{j1}v_a(t) + G_{j2}v_b(t) + G_{j3}v_c(t) + G_{j4}v_d(t) + I_j \\
    j &= a, b, c, d ,
\end{align*}
\tag{3.1.4}
\]

where the linear coefficients are provided by the following relations:

\[
\begin{align*}
    G_{j1} &= \frac{2}{\Delta t} (C_{j1} + C_{j2} + C_{j3}) \\
    G_{j2} &= - \frac{2}{\Delta t} C_{j1} \\
    G_{j3} &= - \frac{2}{\Delta t} C_{j2} \\
    G_{j4} &= - \frac{2}{\Delta t} C_{j3} \\
    I_j &= \frac{2}{\Delta t} Q_{jo} + I_{hj} \\
    j &= a, b, c, d .
\end{align*}
\tag{3.1.5}
\]

Note that since \( i_a + i_b + i_c + i_d = 0 \), we only need to obtain the coefficients for three of the four terminal currents. The linear coefficients of the other terminal current, say \( i_d \), can be obtained by the following relations:
Chapter 3.  Time Domain Solution Algorithm of PWL Circuits

\[ G_{d1} = -(G_{a1} + G_{b1} + G_{c1}) \]
\[ G_{d2} = -(G_{a2} + G_{b2} + G_{c2}) \]
\[ G_{d3} = -(G_{a3} + G_{b3} + G_{c3}) \]
\[ G_{d4} = -(G_{a4} + G_{b4} + G_{c4}) \]
\[ I_d = -(I_a + I_b + I_c) . \]  

(3.1.6)

Next, before presenting the PWL solution algorithm, we first review the commonly used Newton's iteration solution algorithm for nonlinear circuit simulations.

3.2 Newton's iteration solution algorithm

Assume the nonlinear terminal charges have not been linearized by PWL functions. Applying Taylor's expansion to the discretized terminal current equation (3.1.3) and discarding the higher-order terms, we get

\[ i_j^1(t) = i_j^0(t) + \frac{2}{\Delta t} \sum_{v_k} \left[ \frac{\partial Q_j(t)}{\partial v_k(t)} \right]^0 \left[ v_k^1(t) - v_k^0(t) \right] \]

\[ v_k(t) = v_{ab}(t), v_{ac}(t), v_{ad}(t) \]

\[ j = a, b, c, d , \]  

(3.2.7)

where superscript “0” represents previous iterative values; and “1” represents the current iterative variables to be found by solving the circuit equations. \( i_j^0(t) \), \( j = a, b, c, d \), can be obtained by inserting \( v_k^0(t) \), \( k = ab, ac, ad \), into the discretized terminal current expressions as follows:

\[ i_j^0(t) = \frac{2}{\Delta t} Q_j(v_{ab}^0(t), v_{ac}^0(t), v_{ad}^0(t)) + I_{hj} \]

\[ j = a, b, c, d . \]  

(3.2.8)

Equation (3.2.7) can be rewritten into a more compact form as follows:
\[ i_j^1(t) = P_{j1}v_a^1(t) + P_{j2}v_b^1(t) + P_{j3}v_c^1(t) + P_{j4}v_d^1(t) + IN_j \]
\[ j = a, b, c, d \]  

(3.2.9)

where the linear parameters are provided from

\[ P_{j1} = \frac{2}{\Delta t} \sum_{v_k} \left[ \frac{\partial Q_j(t)}{\partial v_k(t)} \right]^0 \]

\[ P_{j2} = -\frac{2}{\Delta t} \left[ \frac{\partial Q_j(t)}{\partial v_{ab}(t)} \right]^0 \]

\[ P_{j3} = -\frac{2}{\Delta t} \left[ \frac{\partial Q_j(t)}{\partial v_{ac}(t)} \right]^0 \]

\[ P_{j4} = -\frac{2}{\Delta t} \left[ \frac{\partial Q_j(t)}{\partial v_{ad}(t)} \right]^0 \]  

(3.2.10)

\[ IN_j = i_j^0(t) - \frac{2}{\Delta t} \sum_{v_k} \left[ \frac{\partial Q_j(t)}{\partial v_k(t)} \right]^0 v_k^0(t) \]

\[ v_k(t) = v_{ab}(t), v_{ac}(t), v_{ad}(t) \]

\[ j = a, b, c, d \]  

Comparing equation (3.2.10) with equation (3.1.5), we can see that the Newton's iteration expressions have a similar form to i-v relations such as the PWL i-v relations. The difference is in the linear parameters. In Newton's iteration, the parameters are obtained from local derivatives of the nonlinear charge functions, while in the PWL method, the parameters are obtained from interpolation on the vertices of the PWL region. Intuitively, when the PWL voltage space partitioning resolutions tend to be infinitively high, the differences between the two methods disappear.

Assume now that the only type of nonlinear device in the circuit is the charge device we discussed above. The time domain solution algorithm using Newton's iteration as nonlinear equation solver proceeds as follows:
Chapter 3. Time Domain Solution Algorithm of PWL Circuits

Newton's iteration time domain solution algorithm

Step 1) Assign initial values for node voltages and currents. These values are usually taken from those at last time point.

Step 2) Replace nonlinear terminal currents by linear equation (3.2.9), form circuit equations by nodal analysis approach.

Step 3) Solve the circuit's linear equations.

Step 4) Check the convergence of the solution. If converged, go to step 5; if not, update voltages, go to step 2.

Step 5) Increase time $t$ by a step $\Delta t$. Go to step 1.

These steps continue until the pre-specified simulation time is reached. Two factors are essential for Newton's iteration to achieve quadratic convergence rate [32][36][33][4]. The first one is that the initial values of the node voltages should be close enough to the real solution. In the DC operating point analysis of an arbitrary circuit, it is difficult to assign initial node voltages close enough to the real solution for the nonlinear devices in a computer-aided solution. In time domain analysis, the initial guess voltages can be taken as the solutions at the last time step, and therefore, it is generally possible to achieve a good closeness of the initial voltages by reducing the discretization time step size.

The other factor relates to the nonlinear charge functions themselves. Good models are at least continuous as a function of each of the controlling voltage variables. Usually the continuity of the derivatives of the nonlinear charge functions is required for the entire working voltage space, since the circuit variables may stray into every possible voltage areas during Newton's iteration. Hence, nonlinear charge functions should be smoothly continuous over the entire considered voltage space. This requirement limits the applicability of analytical modelling of modern electronic devices, such as MOSFET, in circuit transient analysis because these devices are intrinsically nonlinear in both of their DC and AC aspects.
There have been many published works dealing with techniques in multidimensional space for surface smoothing of nonlinear functions. These techniques can be applied to the nonlinear functions and the smoothed functions used in the Newton's iteration. In general, however, without proper conditioning, simulations using Newton's iteration may take a relatively long time to achieve a reasonable convergence, or may even fail to converge.

An alternative to using nonlinear analytical charge functions in time domain simulations is to use PWL approximations to represent the nonlinear characteristics of the charge device. Since only linear algebraic analysis techniques are involved in a PWL circuit simulation, the simulation speed is expected to improve rapidly as compared to Newton's iteration algorithm.

3.3 PWL solution algorithm

In the DC analysis of a resistive circuit, two PWL modelling and solution algorithms have been widely used. One is the Katzenelson's method [6][7][31], and the other is the Newton-like iteration method [8]. Both of them are iterative solution methods.

Katzenelson's method makes extensive searches through the whole range of the concerned voltage space. It is an iterative algorithm, and although it always can find a solution, the searching for this solution may take a long time. Also it is tedious in determining the parameter $\lambda$ [31] used to force the next iterative guess point to be exactly on the PWL region's boundary.

Newton-like iteration faces similar problems of failing to converge to the real PWL solution as the Newton's iteration does [8]. In the method of PWL Newton's iteration solution, the criteria for convergence is judged by the fact that the iterative solution is falling within the same PWL region of the last iterative solution. If the iterative solution cannot fall within the PWL region of the last iterative solution, the divergence form will be such that the iterative solutions are cyclic through a series of identical PWL regions [8].

Unlike the iterative PWL solutions, we expand the single dimension PWL direct solution method of [33] into a multidimensional PWL solution scheme.
Chapter 3. Time Domain Solution Algorithm of PWL Circuits

**PWL direct solution algorithm**

Step 1) Assign initial node voltages and currents for the dynamic elements.

Step 2) Determine the PWL regions for each nonlinear device and get the linear parameters of the PWL models.

Step 3) Form the circuit equations and solve for the node voltages.

Step 4) Check if all the PWL devices stay in their previous regions. If all the PWL devices stay in their previous regions, increase time \( t \) by \( \Delta t \), go to step 3; if there is a PWL region change of any PWL devices, go to step 5.

Step 5) Switch integration rule to BE rule. Carry out two steps of BE integration.

5.1) Increase time \( t \) by \( \Delta t / 2 \). Use the BE integration rule to discretize the PWL charge device. Repeat step 2 and step 3.

5.2) Check the PWL regions for each PWL charge device.

5.3) Repeat steps 5.1 and 5.2. If there is any change of PWL regions during the two steps of BE integration, repeat step 5; if there is no PWL region change, switch back to normal trapezoidal integration rule and go to step 3.

The algorithm continues until the pre-specified simulation time is reached.

Remarks on PWL direct algorithm: 1) The solution is accurate if PWL devices stay in the same region in two consecutive solution steps. 2) There is no iteration in finding the solution if the current solution reaches out of the present PWL region. Instead, a linear extrapolation of the present PWL region is employed to find an approximate solution. Hence, caution should be taken in choosing the integration time step size in order to minimize the overshoot error incurred by the extrapolation approximation. 3) Two consecutive BE integration rules are introduced if there is a switch of PWL regions in order to suppress the numerical oscillations that occur in the trapezoidal integration solutions. 4) PWL modelling and direct solution algorithm translates a nonlinear problem into a linear one by piecewise linearization of nonlinear device functions. There is no need to require the original nonlinear device functions to be smoothly continuous.
Chapter 3. Time Domain Solution Algorithm of PWL Circuits

over the entire voltage space. A compromise between solution speed and accuracy can be freely determined by the user. 5) This algorithm is compatible with the electric circuits simulation program EMTP [13], which is a fixed time step size simulator. The device models can be directly implemented into the EMTP.

In the following chapters, we will use this algorithm to model and simulate intrinsic MOSFET devices in a circuit environment and to compare the results with those obtained by a Newton's iteration algorithm.

3.4 Location of PWL regions during the transient solution

As has been noted, the three-dimensional voltage space is partitioned into a bulk of PWL regions which are non-overlapping polyhedrons. If at the present solution point \( t \), the controlling voltage vector of a nonlinear device is found outside the current PWL region, the location of the new PWL region has to be identified. Here we illustrate this in a two-dimensional plane because it is cumbersome to graphically describe it in the three-dimensional space. The procedure of locating PWL regions in the three-dimensional space is similar to that in the two-dimensional plane.

Figure 3.4.1 shows a two-dimensional voltage plane. The plane has been partitioned into rectangles. Each rectangular area is divided into two triangles. A single triangle area, including the boundaries, is a PWL region. Assume the present controlling voltage vector is located in one of the triangles as shown by a dot at the starting point of the arrows. Referring to Figure 3.4.1, the following situations can happen:

Case 1) If the voltage vector is shifting to positions 5, 6 and 7, the voltage vector is still in the same PWL region.

Case 2) If the voltage vector is shifting to positions 1, 3 and 4, the voltage vector then belongs to the upper triangle PWL region in the same rectangle.

Case 3) If the voltage vector is shifting onto any triangular area of a rectangle other than that of itself, the new PWL region is assigned to be the lower triangle.
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In the three-dimensional space, we can similarly deal with the cube and the six PWL polyhedral regions as shown in figure 2.2.2.

Figure 3.4.1 Location of PWL regions on a plane
Chapter 4.  

Intrinsic MOSFET PWL Modelling and Circuit Simulation

There has been a lot of literature published presenting intrinsic MOSFET models. There are two directions in this area. One is to model the device physics and use numerical methods to solve the nonlinear physical equations directly. This branch is usually branded as device simulation. The other modelling methodology of MOSFET devices, which has been used in almost all of the popular circuit simulators, is based on building an equivalent circuit for the device. Device simulation can accurately represent the physical process happening in the device, but it is hard to couple the representation with the external circuit equations. Equivalent circuit methods have been used widely in the past years to simulate the circuit behaviors of MOSFETs in ICs. Intrinsic MOSFETs are modelled by a DC channel current and a set of dynamic capacitive charge components. They are all nonlinear functions.

4.1 Intrinsic MOSFET devices

Intrinsic MOSFET devices are composed of four terminals and a conducting channel. Each terminal is associated with a part of the device area. The surface state of the channel is controlled by the voltages applied on the terminals. The channel current is a nonlinear function of the terminal voltages characterized by the square-law. It can be modelled by a voltage-controlled current source under the quasi-static assumption. A cross sectional view of an n-type MOSFET device is shown in Figure 4.1.1.

In Figure 4.1.1, g,s,d,b represent the each device’s terminal. Qg, Qs and Qb are three space-distributed charges inside the device. They are responsible for the transient charging currents on the terminals. Apart from these capacitive charging currents, the channel current i_d, plays the most important role for transient analysis under several assumptions. One of the major assumptions is the quasi-static assumption, which means that the channel current and all the space charges are instantaneously reacting to the variation of terminal voltages. Obviously this assumption implies that the variation rate of the applied external terminal voltages should be in the low range of
Chapter 4. *Intrinsic MOSFET PWL Modelling and Circuit Simulation*

frequencies. If the working frequency of the MOSFET is too high, a modified model for the charges and currents should be pursued without the quasi-static assumption. Our modelling and solution method is concerned mostly about the numerical solution of nonlinear models rather than the physical details of the device. Once the analytical form of a nonlinear model of charges and currents can be found by non quasi-static approaches, our solution method will still be applicable.

![Figure 4.1.1 A cross sectional view of the intrinsic NMOSFET](image)

Another point we would like to mention refers to the charge conservation problem during transient simulation of MOSFET circuits. This problem, as indicated in [8], arises from the mistreatment of the nonlinearity of small-signal MOSFET mutual terminal capacitances in Meyer’s capacitance model [33]. Since we are using a nonlinear charge model directly before the time domain discretization of terminal current, this problem does not arise in our model.

Before using the PWL technique to model the nonlinear analytical functions of the device, we first look at the equations of the MOSFET’s intrinsic nonlinear charges and channel current.
4.2 Review of modelling of MOSFET device

A first-order MOSFET model from [25] is presented below. The channel charge density $q_c(x)$ is given by Poisson's equation

$$q_c(x) = C_{ox} \left[ v_{cs}(x) - v_g + V_{FB} + 2\phi_F + \gamma \sqrt{v_{cs}(x) - v_b + 2\phi_F} \right] \quad (4.2.1)$$

under the following assumptions:

1. quasi-static assumption
2. uniform channel approximation
3. one dimensional depletion approximation
4. strong inversion approximation
5. electron mobility is constant along the channel
6. electron current is in the x dimension only
7. hole current is negligible
8. substrate is uniformly doped
9. recombination is negligible.

The channel transport current is given as follows under the same assumptions,

$$I_{ds}(x) = -\mu W q_c(x) \frac{dv_{cs}}{dx}, \quad (4.2.2)$$

where $C_{ox}$ is the oxide linear capacitance per unit area; $v_{cs}(x)$ is the channel to source terminal voltage drop; $V_{FB}$ is the device flat band voltage; $\phi_F$ is the Fermi level of the semiconductor surface; $\gamma$ is the body effect factor; and $W$ is the width of the channel.

The charge continuity assumption in the channel leads to the following charge partitioning equations

$$q_s(x) = \left(1 - \frac{x}{L}\right) q_c(x) \quad (4.2.3)$$

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Chapter 4. Intrinsic MOSFET PWL Modelling and Circuit Simulation

\[ q_{d}(x) = \frac{x}{L} q_{c}(x) \]  \hspace{1cm} (4.2.4)

where \( L \) is the length of the channel. Note that \( q_{c} = q_{s} + q_{d} \). Choosing the gate terminal as the positive reference terminal,

\[ v_{cs}(x) = v_{c}(x) - v_{s} = -v_{gc}(x) + v_{gs} \]  \hspace{1cm} (4.2.5)

Changing variables in the channel charge equation (4.2.1) and transport current equation (4.2.2), we get

\[ I_{ds}(x) = -\mu W q_{c}(x) \frac{dv_{gc}}{dx} \]
\[ q_{c}(x) = -C_{ox} [v_{gc}(x) - (V_{FB} + 2\phi_{F}) - \gamma \sqrt{2\phi_{F} + v_{gb} - v_{gc}(x)}] \]  \hspace{1cm} (4.2.6)

\( q_{c} \) contains two distinctive parts, \( q_{g} \) and \( q_{b} \). These charges satisfy the charge neutral condition of the device

\[ q_{c} + q_{g} + q_{b} = 0 \]  \hspace{1cm} (4.2.7)

where \( q_{g} \) and \( q_{b} \) are gate charge density and substrate charge density, respectively,

\[ q_{g}(x) = C_{ox} [v_{gc}(x) - (V_{FB} + 2\phi_{F})] \]
\[ q_{b}(x) = -\gamma C_{ox} \sqrt{2\phi_{F} + v_{gb} - v_{gc}(x)} \]  \hspace{1cm} (4.2.8)

The further assumption of constant substrate charge density eliminates variable \( x \) out of \( v_{gc}(x) \) in \( q_{b}(x) \) and \( v_{gc}(x) \) can be replaced by \( v_{gs} \). The device threshold voltage is defined as follows

\[ V_{t}(v_{gs}, v_{gb}) = V_{FB} + 2\phi_{F} + \gamma \sqrt{2\phi_{F} + v_{gb} - v_{gs}} \]  \hspace{1cm} (4.2.9)
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and denote

\[ v_{gct} = v_{gc} - V_t \]
\[ v_{gst} = v_{gs} - V_t \]
\[ v_{gdt} = v_{gd} - V_t \]
\[ v_{gbt} = v_{gb} - V_t \]  

(4.2.10)

Finally, we can get the needed terminal charge densities for the calculation of the terminal charges,

\[ q_c(x) = -C_{ox} v_{gct}(x) \]
\[ q_s(x) = \left(1 - \frac{x}{L}\right) q_c(x) \]
\[ q_d(x) = \frac{x}{L} q_c(x) \]
\[ q_b(x) = C_{ox} \left[ v_{gct}(x) + \gamma \sqrt{2 \phi_F + v_{gbt} - v_{gst}} \right] \]
\[ q_b = -C_{ox} \gamma \sqrt{2 \phi_F + v_{gbt} - v_{gst}} \]  

(4.2.11)

and the channel transport current

\[ I_{ds} = \mu W q_c(x) \frac{dv_{gct}(x)}{dx} \]  

(4.2.12)

Integrating the charge densities and channel current along the channel dimension from \( x = 0 \) to \( x = L \), we can get the total terminal charges and the channel current (see appendix A). Note that the charge densities above are obtained under the assumption that the device is working in the linear region. When the device works in other operational regions, such as the cut-off region or the pinch-off region, those charge densities will be different. In appendix A, the total terminal charges are given for all the operational regions of the device.

An equivalent circuit can now be built for transients analysis of the MOSFET’s intrinsic device charges and current. This circuit is shown in Figure 4.2.2.
In the circuit of figure 4.2.2 the nonlinear capacitors are represented by charges $Q_{gs} = -Q_s$, $Q_{gd} = -Q_d$, and $Q_{gb} = -Q_b$. The capacitors in dotted lines represent the parasitic capacitive elements in the device. The nonlinear capacitances in the equivalent circuit model the space charge effects of the device. The voltage-controlled current source models the channel transport current. Notice that the nonlinear capacitances are modelled by charges directly and that the sum of the three charges on the nonlinear capacitors equals the gate charge with opposite polarity. Therefore, the charge conservation law still holds.

4.3 PWL representations of MOSFET terminal currents

The PWL modelling and solution algorithm introduced in chapter 3 can be applied directly to the four-terminal nonlinear charges and channel current of the MOSFET intrinsic device. The terminal currents are the sum of charging currents and transport currents.
Chapter 4.  Intrinsic MOSFET PWL Modelling and Circuit Simulation

For the source terminal current $i_s(t)$,

$$i_s(t) = -i_{gs}(t) - I_{ds}(t) - i_{cgs0}(t) + i_{sb}(t), \quad (4.3.13)$$

where

$$i_{gs}(t) = \frac{dQ_{gs}(t)}{dt} \quad (4.3.14)$$

$$i_{cgs0}(t) = C_{gs0} \frac{dv_{gs}(t)}{dt} \quad (4.3.15)$$

$$i_{sb}(t) = C_{sb} \frac{dv_{sb}(t)}{dt}. \quad (4.3.16)$$

Both $Q_{gs}(t)$ and $I_{ds}(t)$ are nonlinear functions of $v_{gs}(t)$, $v_{gd}(t)$ and $v_{gb}(t)$.

Applying the trapezoidal rule to discretize the differential equations, we get

$$i_{gs}(t) = \frac{2}{\Delta t} (Q_{gs}(t) - Q_{gs}(t - \Delta t)) - i_{gs}(t - \Delta t) \quad (4.3.17)$$

$$i_{cgs0}(t) = \frac{2C_{gs0}}{\Delta t} (v_{gs}(t) - v_{gs}(t - \Delta t)) - i_{cgs0}(t - \Delta t) \quad (4.3.18)$$

$$i_{sb}(t) = \frac{2C_{sb}}{\Delta t} (v_{sb}(t) - v_{sb}(t - \Delta t)) - i_{sb}(t - \Delta t). \quad (4.3.19)$$

Substituting the discretized currents into $i_s(t)$,

$$i_s(t) = -\frac{2}{\Delta t} [Q_{gs}(t) + C_{cgs0}v_{gs}(t) - C_{sb}(t)v_{sb}(t)] + IH_s - I_{ds}(t), \quad (4.3.20)$$

where $IH_s$ is called the "history term" and it is given by the values of circuit variables at previous time point $t-\Delta t$.  

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\[ I_{H_s} = \frac{2}{\Delta t} Q_{gs}(t - \Delta t) + i_{gs}(t - \Delta t) + \frac{2C_{gso}}{\Delta t} v_{gs}(t - \Delta t) + i_{cgs}(t - \Delta t) - \frac{2C_{sb}}{\Delta t} v_{sb}(t - \Delta t) - i_{sb}(t - \Delta t) \]  \hspace{1cm} (4.3.21)

For PWL modelling, the nonlinear charge \( Q_{gs} \) and the nonlinear current \( I_{ds} \) are approximated by PWL functions as follows

\[ I_{ds}^{PWL}(t) = G_{gs} v_{gs}(t) + G_{gd} v_{gd}(t) + G_{gb} v_{gb}(t) + I_{dso} \]  \hspace{1cm} (4.3.22)
\[ Q_{gs}^{PWL} = C_{s1} v_{gs}(t) + C_{s2} v_{gd}(t) + C_{s3} v_{gb}(t) + Q_{gso} \]  \hspace{1cm} (4.3.23)

Substituting these PWL functions into equation (4.3.20), we get the expression for the linearized source terminal current as follows:

\[ i_s(t) = h_{s1} v_g(t) + h_{s2} v_s(t) + h_{s3} v_d(t) + h_{s4} v_b(t) + I_s \]  \hspace{1cm} (4.3.24)

where the linear coefficients are given by

\[ h_{s1} = - \frac{2}{\Delta t} (C_{s1} + C_{s2} + C_{s3}) - \frac{2}{\Delta t} C_{gso} \]
\[ - (G_{gs} + G_{gd} + G_{gb}) \]
\[ h_{s2} = \frac{2}{\Delta t} C_{s1} + \frac{2}{\Delta t} C_{gso} + \frac{2}{\Delta t} C_{sb} + G_{gs} \]
\[ h_{s3} = \frac{2}{\Delta t} C_{s2} + G_{gd} \]
\[ h_{s4} = \frac{2}{\Delta t} C_{s3} - \frac{2}{\Delta t} C_{sb} + G_{gb} \]
\[ I_s = \frac{2}{\Delta t} Q_{gso} - I_{dso} + I_{H_s} \]  \hspace{1cm} (4.3.25)

The discretized and linearized expressions for the currents in the other three terminals can be obtained similarly to the source terminal current \( i_s(t) \) presented above. Now, since,
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\[ i_d(t) = -i_{gd}(t) + I_{ds}(t) - i_{cgo}(t) + i_{db}(t) \]  \hspace{1cm} (4.3.26)

\[ i_b(t) = -i_{gb}(t) - i_{cgo}(t) - i_{sb}(t) - i_{db}(t) \]  \hspace{1cm} (4.3.27)

\[ i_g(t) = -(i_s(t) + i_d(t) + i_b(t)) \]  \hspace{1cm} (4.3.28)

After discretization with the trapezoidal rule and linearization by PWL function approximations, the terminal currents can also be expressed as:

\[ i_d(t) = h_{d1}v_g(t) + h_{d2}v_s(t) + h_{d3}v_d(t) + h_{d4}v_b(t) + I_d \]  \hspace{1cm} (4.3.29)

\[ i_b(t) = h_{b1}v_g(t) + h_{b2}v_s(t) + h_{b3}v_d(t) + h_{b4}v_b(t) + I_b \]  \hspace{1cm} (4.3.30)

\[ i_g(t) = h_{g1}v_g(t) + h_{g2}v_s(t) + h_{g3}v_d(t) + h_{g4}v_b(t) + I_g \]  \hspace{1cm} (4.3.31)

The linear coefficients for the above terminal current equations are given in appendix B.

4.4 Circuit simulation experiments

A simulation program has been written to test the MOSFET equivalent circuit model in nodal analysis approach using both the Newton's iteration and the PWL modelling solutions. The input format of the simulation is similar to that used by SPICE2 [2] for the description of the connection of circuit components. The CDA [34] integration scheme is used for time domain discretization in the PWL solution algorithm. The advantage of this scheme is its capability to dampen numerical oscillations when the controlling voltage variables in the MOSFET device switch from one PWL region into another. For comparison, the trapezoidal integration rule is used with the Newton's iteration nonlinear solution algorithm to simulate the same circuits.

The derivative elements in the Jacobian matrix of Newton's iteration are obtained from the central difference formula as follows:

\[ \frac{dq}{dv} = \frac{q(v + \Delta v_{io}) - q(v - \Delta v_{io})}{2\Delta v_{io}} \]  \hspace{1cm} (4.4.32)
where $\Delta V_{io}$ is a small positive number representing increment of the voltage vector in the $v_i$ dimension. *Newton's iteration* in which Jacobian matrix is calculated by the central difference formula is called *discrete Newton's iteration*. The convergence criteria in the simulations is set to be

$$|v_j^1 - v_j^0|_{max} < 10^{-5}$$

(4.4.33)

where subscript $j$ indicates one of the controlling voltage variables of the nonlinear MOSFET charge functions. The subscript "max" represents the largest difference value between two consecutive iterations.

Circuit 1 is a single MOSFET inverter as shown in figure 4.4.3.

![Circuit Diagram](image)

Figure 4.4.3 A single MOSFET inverter

To emphasize the effects of nonlinearity and the numerical properties of the CDA scheme and the trapezoidal rule, only the MOSFET equivalent circuit of the intrinsic device, as shown in figure 4.2.2 with solid lines, is used in this simulation.
Figure 4.4.4 shows the output voltage and MOSFET source terminal current waveforms using Newton's iteration solution when the input signal is a sinusoidal waveform. The simulation integration time step is $\Delta t=1\mu s$. Numerical oscillations appear in the output voltage and in the source terminal current. The oscillations are superimposed on the correct solutions with the frequency of the sampling rate (inverse of integration time step size). The oscillation amplitudes are accumulating along the cycles of the input waveform. Since there is no linear capacitor in the circuit, and the input is a continuous sinusoidal waveform, the cause of these oscillations must be due to the discretization of nonlinear charges by the trapezoidal integration rule. Every time the input waveform changes from a level of 0 volt to 5 volts, the controlling voltages of the MOSFET nonlinear charges sweep through all the operational regions of the device from cut-off region to linear region until pinch-off region. The nonlinear capacitive effects lead to the numerical oscillations when the trapezoidal integration rule is used to approximate the differential equations.

We decrease the time step size $\Delta t$ to simulate the circuit again. It was found, however, that as the time step size $\Delta t$ decreases, the amplitudes of the oscillations also decreases. This effect is shown in Figure 4.4.5 and Figure 4.4.6 (scale changed) where $\Delta t=0.5\mu s$ and $\Delta t=0.1\mu s$.

It is therefore important in this solution method to make a proper choice of the time step size because of the truncation error imposed by the approximation of the differential equations by the trapezoidal integration rule. Generally, the smaller the time step, the smaller the truncation error.

In the solution with the PWL algorithm presented in Figures 4.4.7 to 4.4.9, the partitioning resolution plays an important role in determining time step size. If the resolution is high enough, the PWL approximation will be in good agreement with the original nonlinear charge functions.

Figures 4.4.7 to 4.4.9 shows the results of simulating the same MOSFET inverter using PWL algorithm presented in this chapter.

As shown in the simulation results using the PWL algorithm, numerical oscillations are completely suppressed. This is due to the CDA procedure which introduces two half-size BE integration steps when the controlling voltage vectors change PWL regions. But as can be seen from these results, the overshoot error of PWL algorithm is also reduced with the decreasing
time step size.

The PWL algorithm also gives much faster computational times than Newton's iteration. Table 1 lists the computation times for the simulation of circuit 1 on a SUN SPARC station. The simulations were run from \( t = 0 \) to \( t = T_{\text{max}} \) with the indicated time step size. The last column in the table is the total CPU computer time.

---

2 The simulation program is written in Fortran and is by no means optimal. These times include output time at each time step point.
Figure 4.4.4 trapezoidal rule, Newton iteration, ∆t=1μs. *above*)

Input and output voltages; *below*) Source terminal current
Figure 4.4.5 trapezoidal rule, Newton iteration, $\Delta t=0.5\mu s$. above)

Input and output voltages; below) Source terminal current

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Figure 4.4.6 trapezoidal rule, Newton iteration, \( \Delta t = 0.1 \mu s. \) above)

Input and output voltages; below) Source terminal current
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Figure 4.4.7 PWL algorithm, $\Delta t=1 \mu s$. 

*above*) Input and output voltages; *below*) Source terminal current
Figure 4.4.8 PWL algorithm, $\Delta t=0.5\mu s$. above) Input
and output voltages; below) Source terminal current
Figure 4.4.9 PWL algorithm, $\Delta t=0.1\mu s$. *above*) Input and output voltages; *below*) Source terminal current
Table 1 Computation Times for Circuit 1

<table>
<thead>
<tr>
<th>Scheme</th>
<th>$\textit{Step size } \Delta t \text{ (µs)}$</th>
<th>$T_{\text{max}} \text{ (µs)}$</th>
<th>CPU time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWL</td>
<td>1</td>
<td>400</td>
<td>2.6</td>
</tr>
<tr>
<td>Newton</td>
<td>1</td>
<td>400</td>
<td>21.25</td>
</tr>
<tr>
<td>PWL</td>
<td>0.5</td>
<td>400</td>
<td>4.74</td>
</tr>
<tr>
<td>Newton</td>
<td>0.5</td>
<td>400</td>
<td>37.77</td>
</tr>
<tr>
<td>PWL</td>
<td>0.1</td>
<td>100</td>
<td>4.4</td>
</tr>
<tr>
<td>Newton</td>
<td>0.1</td>
<td>100</td>
<td>41.55</td>
</tr>
</tbody>
</table>

Circuit 2 is a MOSFET charging circuit, shown in figure 4.4.10, which has been used by many authors to check the charge conservation problem of the MOSFET device equivalent circuit.

![MOSFET charging circuit](image)

Figure 4.4.10 MOSFET charging circuit

We use the same intrinsic MOSFET equivalent circuit in the simulations described previously. Figures 4.4.11 shows the Newton's iteration solution for the voltage on capacitors $C_1$ and $C_2$ and for the source terminal current. Figure 4.4.12 shows the results obtained with the proposed PWL algorithm.
Figure 4.4.11 trapezoidal rule, Newton iteration, $\Delta t=0.1\mu s$. above) Voltages on capacitors $C_1$ and $C_2$ (they are identical); below) Source terminal current.
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Figure 4.4.12 PWL algorithm, $\Delta t=0.1\mu s$. Above) Voltages on capacitors $C_1$ and $C_2$; below) Source terminal current.

The simulations were repeated with a larger time step size of $0.2\mu s$ with similar results. The
computation time comparisons are listed in table 2 below.

Table 2 Computation Times for Circuit 2

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Time step $\Delta t$ ($\mu$s)</th>
<th>$T_{max}$ ($\mu$s)</th>
<th>CPU time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWL</td>
<td>0.1</td>
<td>400</td>
<td>16.16</td>
</tr>
<tr>
<td>Newton</td>
<td>0.1</td>
<td>400</td>
<td>107.31</td>
</tr>
<tr>
<td>PWL</td>
<td>0.2</td>
<td>400</td>
<td>8.98</td>
</tr>
<tr>
<td>Newton</td>
<td>0.2</td>
<td>400</td>
<td>67.46</td>
</tr>
</tbody>
</table>

Circuit 3 is a MOSFET switched capacitor network as shown in figure 4.4.13.

![MOSFET switched capacitor network](image)

Figure 4.4.13 MOSFET switched capacitor

An integration time step of $\Delta t = 0.2 \mu s$ is used. Figure 4.4.14 shows the voltages on capacitors $C_1$ and $C_2$ simulated by the *Newton's iteration* algorithm. Figure 4.4.15 shows the results obtained with PWL algorithm.
The simulations were repeated with a reduced time step size of $\Delta t = 0.1\mu s$. The results are shown in figures 4.4.16 and 4.4.17. Note in figure 4.4.16, the voltages on $C_1$ and $C_2$ are shown in the upper plot with solid line and dotted line, respectively. In the lower plot the source terminal currents of both MOSFETs are shown with severe numerical oscillations. The same arrangement of simulation results using the PWL algorithm is shown in figure 4.4.17. In figure 4.4.17, the simulated voltage results are very close to those of Newton's iteration algorithm while the numerical oscillations in the source terminal currents are totally suppressed.

It was also found that the time step size has non-trivial influence on the simulated waveforms. Referring to figure 4.4.14 and figure 4.4.16, both of them are simulation results with the Newton's iteration algorithm. But the voltage waveforms are different. We may speculate that the reason for this is that the Newton's iteration converges to the different solution points since the discretized finite difference equation of the original differential device equation is a function of time step size $\Delta t$.

Table 3 lists computation time comparisons between Newton's iteration and PWL solutions.

<table>
<thead>
<tr>
<th>Scheme</th>
<th>$\Delta t$ ($\mu s$)</th>
<th>$T_{max}$ ($\mu s$)</th>
<th>CPU time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWL</td>
<td>0.1</td>
<td>800</td>
<td>70.77</td>
</tr>
<tr>
<td>Newton</td>
<td>0.1</td>
<td>800</td>
<td>265.74</td>
</tr>
<tr>
<td>PWL</td>
<td>0.2</td>
<td>800</td>
<td>37.02</td>
</tr>
<tr>
<td>Newton</td>
<td>0.2</td>
<td>800</td>
<td>161.56</td>
</tr>
</tbody>
</table>
Figure 4.4.14 trapezoidal rule, Newton iteration, \( \Delta t=0.2 \mu s \).

voltages on capacitors \( C_2(\text{above}) \) and \( C_1(\text{below}) \).
Figure 4.4.15 PWL algorithm, $\Delta t=0.2\mu s$.

voltage on capacitors $C_2(above)$ and $C_1(below)$.
Figure 4.4.16 trapezoidal rule, Newton iteration, $\Delta t=0.1\mu s$. (above)
Voltages on capacitors $C_1$ and $C_2$; (below) Source terminal currents.
Figure 4.4.17 PWL algorithm, \( \Delta t=0.1\mu s \). (above) Voltages on capacitors \( C_1 \) and \( C_2 \); (below) Source terminal currents.
In chapter 4, an equivalent circuit was presented to model MOSFET devices in circuit transients analysis. In this chapter, a model is presented for power MOSFETs.

In general, in dealing with the transient behavior of solid state electronic devices, it is not always possible to find a suitable equivalent circuit representation for the device and it becomes necessary to solve the device physical equations and couple the solution with the circuit equation [29]. In the case of power MOSFETs, the circuit where these devices are used and the device parameters usually limit the operation to well below microwave frequencies [19]. One can then assume that at any moment the device charge densities and channel current are determined by the instantaneous values of the terminal voltages (quasi-static assumption).

5.1 VDMOST equivalent circuit for transient analysis

The power MOSFET is different from the general small-size MOSFET device in large-scale integrated circuits in terms of both physical structure and analytical characteristics. Some of the main differences are related to the variation property of gate-drain capacitance and of the body-drain diode in the power device. These differences are important in determining the response of the device in the circuit.

Figure 5.1.1 shows a cross sectional structure of a vertical double diffused power MOSFET (VDMOST) device. The VDMOST is a three terminal device. There is no substrate. Under normal voltage bias, $v_d > v_s$, the channel current flows from drain to source (in fact, the minority carrier in the inversion layer flows from source to drain in the channel). The transient behavior of the VDMOST is also largely determined by the parasitic capacitances and the packaging inductances. Figure 5.1.2 shows a large-signal equivalent circuit model for this device which includes 11 linear and nonlinear elements. This equivalent circuit has most of the critical parasitic elements in it [19][39].
Figure 5.1.1 A cross sectional view of a double diffused vertical power MOST. It has a symmetrical structure. The elements of the equivalent circuit are shown on the right half of the device.

We will discuss each component in the following.

**Channel current** $I_{ds}$ The VDMOST channel DC characteristic is modelled by the nonlinear channel current $I_{ds}$ and resistances $R_s$ and $R_d$. Based on *quasi-static assumption*, the channel current is controlled by the terminal voltages instantaneously. $I_{ds}$ is governed by the following *square-law* characteristics [19][39]:

i) $v_{gsi} < V_T$

$$I_{ds} = 0$$  \hspace{1cm} (5.1.1)
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Figure 5.1.2 Equivalent circuit model of VDMOST for large signal analysis

ii) $0 < v_{dsi} < v_{gsi} - V_T$

\[ I_{ds} = \beta \left[ 2v_{dsi}(v_{gsi} - V_T) - v_{dsi}^2 \right] \]  \hspace{1cm} (5.1.2)

iii) $0 < v_{gsi} - V_T < v_{dsi}$

\[ I_{ds} = \beta (v_{gsi} - V_T)^2 \] \hspace{1cm} (5.1.3)

The channel current $I_{ds}$ is a nonlinear function of two controlling voltage variables, the internal terminal voltages $v_{dsi}$ and $v_{gsi}$:
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\[ v_{gsi} = v_{gi} - v_{si} \]
\[ v_{dsi} = v_{di} - v_{si} \]  

Those voltages are related to the external terminal voltages by

\[ v_{gi} = v_{g} - r_g i_g \]
\[ v_{si} = v_{s} - r_s i_s \]
\[ v_{di} = v_{d} - r_d i_d \]  

where \( r_s \) and \( r_d \) are two portions of channel resistance residing in source terminal and drain terminal. \( r_g \) is the gate access resistance. In DC state, \( i_g = 0, i_s = -i_d \).

There are four model parameters to determine for channel current \( I_{ds} \). They are the threshold voltage \( V_T \), and \( \beta \), \( r_s \) and \( r_d \).

1. Determination of \( V_T \) and \( \beta \)

There exist analytical formulas to compute these parameters [18] and their values could be obtained from the data in the data-sheets of VDMOST product. Another way is to measure the device channel characteristics of \( v_{gs} \) versus \( I_{ds} \) in the pinch-off region and deduce the parameters from the analytical equation (5.1.3) and the measurement curve as shown in [38]. In the pinch-off region, the terminal current is \( i_s = -I_{ds} \) and the drain current is given by

\[ I_{ds} = \beta (v_{gsi} - V_T)^2 \]
\[ = \beta (v_{gs} - r_s I_{ds} - V_T)^2 \]  

For small \( r_s \) and \( I_{ds} \) we can get the following approximate linear relation from equation (5.1.3)

\[ v_{gs} \approx \frac{1}{\sqrt{\beta}} \sqrt{I_{ds} + V_T} \]  

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Then $V_T$ and $\beta$ can be deduced from the measurement plot in the lower range of the channel current.

2. **Determination of $r_s$**
   Again, in the pinch-off region, from equation (5.1.3), we have
   \[
   r_s = \frac{v_{gs} - V_T}{I_{ds}} - \frac{1}{\sqrt{\beta I_{ds}}}
   \]  
   (5.1.8)

   After obtaining $V_T$ and $\beta$, we need only substitute one set of data $(v_{gs}, V_T)$ to determine this parameter. However, this set of data should be taken at an appropriate measurement point where the $I_{ds}, r_s$ drop is significant. The authors of [12] neglected this parameter since it is primarily due to the bonding wire and the metallization and the diffusion layers of the device chip. In the actual device, it may be reduced to the Ohm range.

3. **Determination of $r_d$**
   In the device data-sheets, the static drain-to-source on-state resistance $R_{ds(on)}$ is provided.
   In the linear region $R_{ds(on)} = r_d + r_{ch} + r_s$, where $r_{ch}$ is the channel resistance in the linear operating region. For small $v_{ds}$, equation (5.1.2) approximates the channel resistance
   \[
   r_{ch} = \frac{1}{2\beta(v_{gs} - V_T)}
   \]  
   (5.1.9)

   where $v_{gsi}$ has been approximated by $v_{gs}$ under the condition of large $v_{gs}$. Notice that $r_{ch}$ is a nonlinear function of $v_{gs}$. It is therefore suggested that to more accurately model channel resistances, a more elegant nonlinear function may be used.

**Dynamic components** There are six dynamic components in this model. They are the gate-source capacitance $C_{gs}$, the gate-drain capacitance $C_{gd}$, the drain-source capacitance $C_{ds}$, and the three terminal inductances. Device data-sheets will give typical parameter values and measured voltage-capacitance curves of three capacitances $C_{iss}$, $C_{oss}$ and $C_{rss}$, known as input capacitance,
output capacitance and reverse transfer capacitance, respectively. To model the device, we need to know the analytical models of the nonlinear capacitances, $C_{gs}$, $C_{gd}$ and $C_{ds}$ which will be used in the equivalent circuit model.\(^3\) The author of [38] measured the small-signal characteristics of a VDMOST of the International Rectifier type IRF130 to deduce the relations between terminal bias voltages and capacitances across the terminals. Since those capacitances are obtained based on small-signal measurements, the actual nonlinear charges on these capacitors have to be found in order to be used in the time domain discretization of the charge differential equations.

1. Determination of the drain-gate capacitance $C_{dg}$

The measured drain-to-gate capacitance curve in [38] shows that this capacitance depends on only one controlling voltage $v_{dg}$ and it can be approximated by a polynomial function. We should mention here that since voltage controlled nonlinear capacitances are usually described as small-signal capacitances, from the definition of small signal capacitance, $C_{dg}$ is

$$C_{dg} = \frac{dQ_{dg}}{dv_{dg}}. \quad (5.1.10)$$

To calculate the current in a nonlinear capacitor, we can no longer use the small-signal capacitance directly in the discretization of the differential equation without considering the nonlinearity of the small-signal capacitance. Instead, charges on the nonlinear capacitor should be integrated out and used in the time domain discretization\(^4\).

$$Q_{dg} = \int C_{dg} dv_{dg} \quad (5.1.11)$$

Here for VDMOST, $C_{dg}$ is approximated by a polynomial function

\(^3\) The relation among these capacitances are: $C_{rss} = C_{gs} + C_{gd}$, $C_{oss} = C_{gd} + C_{ds}$, $C_{rss} = C_{gd}$

\(^4\) Of course it is better if the nonlinear charge can be found directly without resort to the integration from the small-signal capacitance.
where the $C_{dgn}$ are constant capacitive parameters. They are obtained by fitting the measurement data with the polynomial function by least-square method. Then the nonlinear charge would be

$$Q_{dg} = \sum_{0}^{n} \frac{1}{n+1} C_{dgn} v_{dg}^{n+1}.$$  

(5.1.13)

The constant of integration $C_{dg}(0)$ is set to be zero. Note, however, that since the measured data are only obtained within a certain range of voltage spans, the application of these data are limited to the corresponding ranges and the specific device measured.

2. Determination of the drain-source capacitance $C_{ds}$

This small-signal capacitance is largely due to the nonlinear depletion and diffusion capacitances presented by the channel diode. The equivalent circuit for this part in figure 5.1.2 is modelled as shown in figure 5.1.3.

![Diagram](image_url)
In the circuit of Figure 5.1.3, the diode is modelled by a current source, diode capacitance and internal resistance, \( C_p \) is the parasitic capacitance. The diode capacitance is given by

\[
C_d = \frac{\tau}{k} e^{v_{\text{diode}}/k} + C_{do} \left( 1 - \frac{v_{\text{diode}}}{\phi} \right)^{-m} \quad (5.1.14)
\]

where the first term is the diffusion capacitance, the second term is the depletion capacitance, and \( v_{\text{diode}} \) is the junction voltage of the diode. Under normal operation, \( v_{\text{diode}} < 0 \) and the diode is turned off. \( C_d \) is dominated by the depletion capacitance:

\[
C_d = C_{do} \left( 1 - \frac{v_{\text{diode}}}{\phi} \right)^{-m} \quad (5.1.15)
\]

When \( v_{\text{diode}} > 0 \), the diode is working under forward bias, and the second term in equation (5.1.14) is no longer valid. The diffusion capacitance will dominate \( C_d \) and

\[
C_d = \frac{\tau}{k} e^{v_{\text{diode}}/k} \quad . (5.1.16)
\]

The charge on the nonlinear diode capacitance can now be obtained by integrating the small-signal capacitance. In order to get a continuous charge function, the condition \( Q_d(0) = 0 \) has been set in the following integrations.

For \( v_{\text{diode}} < 0 \)

\[
Q_d = -\frac{1}{1-m} C_{do} \phi \left[ \left( 1 - \frac{v_{\text{diode}}}{\phi} \right)^{1-m} - 1 \right] \quad (5.1.17)
\]

For \( v_{\text{diode}} \geq 0 \)

\[
Q_d = \tau \left( e^{v_{\text{diode}}/k} - 1 \right) \quad . (5.1.18)
\]
3. **Determination of the gate-source capacitance** $C_{gs}$

Physically, the gate-source capacitance comprises the overlap capacitance, the gate-channel capacitance, and the capacitance through the field oxide of the source overlay. It is largely independent of bias and is treated as a linear constant. Hence the charge on it is simply obtained from

$$Q_{gs} = C_{gs}v_{gs}. \quad (5.1.19)$$

4. **Determination of the terminal inductances** $L_g$, $L_s$ and $L_d$

These parasitic inductances originate from the device bonding and packaging. They can all be treated as linear components and are given in the device data-sheets for each specific VDMOST.

**Other components** The last two elements, the gate access resistance $r_g$ and channel diode current $i_{diode}$, need to be modelled.

1. **Determination of the gate access resistance** $r_g$

This resistance is very small, but making this parameter zero would affect the delay times, especially when the transistor is driven by a very low impedance circuit. The value of this resistance can be obtained by measuring the time constant of the step response of the gate voltage when the device is operating in the cut-off region [38].

2. **Modelling of the channel diode current** $i_{diode}$

The channel diode current is given by

$$i_{diode} = I_o \left( e^{\frac{v_{diode}}{k}} - 1 \right) \quad (5.1.20)$$

where $v_{diode}$ is the diode junction voltage. When the VDMOST works in the reverse mode, i.e., when $v_{ds} < 0$, the channel current will be less significant as compared to the channel...
diode current which is forward biased\(^5\). \(v_{\text{diode}}\) and \(v_{\text{dsi}}\) have the following relation,

\[
v_{\text{dsi}} = -\left[ v_{\text{diode}} + \left( i_{\text{diode}} + \frac{dQ_d}{dt} \right) r_{\text{diode}} \right]
\]  \hspace{1cm} (5.1.21)

where \(r_{\text{diode}}\) is the internal resistance of the diode. The current originated from the diode nonlinear capacitance, \(dQ_d/dt\), can be discretized with the trapezoidal integration rule and expressed as

\[
i_{Q_d}(t) = \frac{dQ_d}{dt} = \frac{2}{\Delta t} Q_d(t) + I_{dh}
\]  \hspace{1cm} (5.1.22)

where \(I_{dh}\) denotes the history term. \(Q_d\) is a nonlinear function of \(v_{\text{diode}}\) as shown in equations (5.1.17) and (5.1.18). However, after linearization by PWL functions, \(Q_d\) can be expressed as

\[
Q_d = C_{\text{diode}} v_{\text{diode}} + Q_{do}
\]  \hspace{1cm} (5.1.23)

Substituting the PWL \(Q_d\) into equation (5.1.22), \(i_{Q_d}(t)\) can be expressed as a linear relationship

\[
i_{Q_d}^{\text{PWL}}(t) = gQ_d v_{\text{diode}}(t) + I'_{dh}
\]  \hspace{1cm} (5.1.24)

where the linear coefficients are given by

\[
gQ_d = \frac{2C_{\text{diode}}}{\Delta t}
\]

\[
I'_{dh} = I_{dh} + \frac{2Q_{do}}{\Delta t}
\]  \hspace{1cm} (5.1.25)

---

\(^5\) In fact, almost all of the VDMOST models published did not discuss the channel current under reverse bias mode.
Hence equation (5.1.21) can be expressed as

\[ v_{dsi} = -(1 + gQ_d r_{diode}) v_{diode} - (i_{diode} + I'_{dh}) r_{diode} \]  

(5.1.26)

Note that the diode current \( i_{diode} \) is also a nonlinear function of \( v_{diode} \), but it can also be linearized by a PWL function as well. After linearization, \( v_{diode} \) can be found once \( v_{dsi} \) has been determined.

Table 4 lists all the coefficients used in the VDMOST equivalent model [38][18] studied here.

<table>
<thead>
<tr>
<th>Elements</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_s )</td>
<td>0.005( \Omega )</td>
</tr>
<tr>
<td>( R_d )</td>
<td>0.07( \Omega )</td>
</tr>
<tr>
<td>( R_g )</td>
<td>4.5( \Omega )</td>
</tr>
<tr>
<td>( C_{dgj} (pF) )</td>
<td>( C_{dgj} ), ( j = 0 ) to ( 5 )</td>
</tr>
<tr>
<td></td>
<td>600, -98.3, 2.7624, 0.51193,</td>
</tr>
<tr>
<td></td>
<td>-0.036845, 0.00067881</td>
</tr>
<tr>
<td>( C_{ds0} )</td>
<td>1100pF</td>
</tr>
<tr>
<td>( k )</td>
<td>0.0259</td>
</tr>
<tr>
<td>( \phi )</td>
<td>0.7 ( \nu )</td>
</tr>
<tr>
<td>( \tau )</td>
<td>200ns</td>
</tr>
<tr>
<td>( C_{gs} )</td>
<td>550pF</td>
</tr>
<tr>
<td>( C_p )</td>
<td>80pF</td>
</tr>
</tbody>
</table>
Table 4 (Continued) VDMOST equivalent model parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_0$</td>
<td>$1.1 \times 10^{-10}$ amp</td>
</tr>
<tr>
<td>$I_{diode}$</td>
<td>0.05Ω</td>
</tr>
<tr>
<td>$L, L_d, L_g$</td>
<td>5.5nH, 40nH, 40nH</td>
</tr>
</tbody>
</table>

5.2 PWL modelling and simulation

In this section, the nonlinear elements in the VDMOST equivalent circuit will be modelled by PWL function approximations.

5.2.1 PWL modelling of the channel current $I_d$s

The channel current $I_d$s is a nonlinear function of two internal node voltages, $v_{dsi}$ and $v_{gsi}$

$$I_{ds} = I_{ds}(v_{dsi}, v_{gsi})$$  \hspace{1cm} (5.2.27)

Compared to the three-dimensional case discussed in the last chapter for a small size MOSFET device, the VDMOST device is much simpler to approximate by PWL functions. Two-dimensional PWL partitioning should be applied to the channel current. Figure 5.2.4 shows the triangular partitioning of a two-dimensional voltage plane. The plane is divided into rectangular areas and each rectangle is then divided into two triangular PWL regions.
Chapter 5.  Power MOSFET modelling and simulation

In each PWL region, the following form of linear expression of $I_{ds}$ is obtained by interpolating the nonlinear channel current on three vertices of the triangle,

$$I_{ds}^{PWL} = g_1 v_{dsi} + g_2 v_{gsi} + I_{dso}.$$  \hspace{1cm} (5.2.28)

5.2.2 PWL modelling of the nonlinear capacitances $Q_{dg}$ and $Q_d$

$Q_{dg}$ and $Q_d$ are both nonlinear capacitors and are single variable controlled. Their PWL modelling is thus straight forward. For these one-dimensional charges, the PWL linear expressions are

$$Q_{dg}^{PWL} = C_{dg} v_{dg} + Q_{dgo}$$
$$Q_d^{PWL} = C_{diode} v_{diode} + Q_{do}$$  \hspace{1cm} (5.2.29)

where the capacitive parameters and charge constants are to be obtained by PWL function interpolation over the two end points of each PWL voltage segment.
5.2.3 PWL modelling of the diode current

The diode current can be expressed in exponential form as in equation (5.1.20)

\[ i_{\text{diode}} = I_0 \left( e^{v_{\text{diode}}/k} - 1 \right) \text{.} \]  

(5.2.30)

Figure 5.2.5 shows this voltage-current curve. Note that the control variable is the junction voltage \( v_{\text{diode}} \).

The diode current is a highly nonlinear function of the junction voltage. Under forward bias, it increases exponentially, while under reverse bias, it stays near the value of saturation \( I_0 \) in opposite direction. At \( T=300 \) K, the thermal parameter \( k \) is about 0.0259, and a small forward junction voltage will produce quite a large current. Overflow problem may be encountered using iterative solution since the iteration solutions may stray into a large forward bias.

Due to the heavy nonlinearity of the diode current characteristics, under forward bias \( v_{\text{diode}} > 0 \), we divide the voltage dimension into segments with a resolution of \( \delta v \) smaller than the resolution used in reverse bias. The nonlinear characteristic of the diode is linearized in
Chapter 5. Power MOSFET modelling and simulation

each PWL segment by interpolation at the two ends of the segment

\[ i_{\text{diode}}^{\text{PWL}} = g_{\text{diode}}v_{\text{diode}} + I_{\text{diode}} \]  \hspace{1cm} (5.2.31)

If the forward voltage is over the pre-specified value \( v_{do} \) (we choose \( v_{do} = 1 \) volt and \( \delta v = 0.1 \) volt), the linearized expression for \( i_{\text{diode}} \) is used as follows:

\[ g_{\text{diode}} = \left( \frac{d i_{\text{diode}}}{d v_{\text{diode}}} \right) v_{do} \]  \hspace{1cm} (5.2.32)

\[ I_{\text{diode}} = \left( i_{\text{diode}} \right)_{v_{do}} - \left( \frac{d i_{\text{diode}}}{d v_{\text{diode}}} \right)_{v_{do}} v_{do} \]  \hspace{1cm} (5.2.32)

Under reverse bias, a larger PWL division resolution can be chosen since the reverse current is almost constant at the value of saturation current \( I_{ss} \).

The relation between \( v_{\text{diode}} \) and \( v_{\text{dsi}} \) is described by equation (5.1.26). Substituting \( i_{\text{diode}}^{\text{PWL}} \) into equation (5.1.26), we obtain the following equation

\[ v_{\text{dsi}} = -(1 + Q_{d} r_{\text{diode}}) v_{\text{diode}} - \left( g_{\text{diode}} v_{\text{diode}} + I_{\text{diode}} + I'_{dh} \right) r_{\text{diode}} \]  \hspace{1cm} (5.2.33)

therefore,

\[ v_{\text{diode}} = -\frac{v_{\text{dsi}} + \left( I_{\text{diode}} + I'_{dh} \right) r_{\text{diode}}}{1 + \left( Q_{d} + g_{\text{diode}} \right) r_{\text{diode}}} \]  \hspace{1cm} (5.2.34)

The above equation can be rewritten into compact form

\[ v_{\text{diode}} = \alpha v_{\text{dsi}} + \eta \]  \hspace{1cm} (5.2.35)

---

\(^{6}\) Reverse break down of diode is not considered since the reverse voltage is normally within the rated break down voltage of the device.
where \( \alpha \) and \( \eta \) are given by

\[
\alpha = -\frac{1}{1 + (gQ_d + g_{diode})r_{diode}} \quad (5.2.36)
\]

\[
\eta = -\frac{(I_{diode} + I_{rh})r_{diode}}{1 + (gQ_d + g_{diode})r_{diode}}
\]

### 5.2.4 VDMOST PWL terminal currents

Referring to the equivalent circuit in Figure 5.1.2, the terminal currents of the VDMOST in the time domain are provided by the following relations

\[
i_g = -\frac{dQ_{di}}{dt} + C_{gs} \frac{dv_{gsi}}{dt}
\]

\[
i_d = C_p \frac{dv_{dsi}}{dt} + I_{ds} - \frac{-v_{dsi} - v_{diode}}{r_{diode}} + \frac{dQ_{di}}{dt}
\]

\[
i_s = -C_p \frac{dv_{dsi}}{dt} - I_{ds} + \frac{-v_{dsi} - v_{diode}}{r_{diode}} - C_{gs} \frac{dv_{gsi}}{dt}
\]

They satisfy KCL

\[
i_g + i_s + i_d = 0 \quad (5.2.38)
\]

We now apply the trapezoidal rule to equation (5.2.37) to discretize the terminal currents.

For \( i_g \),

\[
i_g(t) = -\frac{2}{\Delta t} Q_{dg}(t) + \frac{2}{\Delta t} Q_{dg}(t - \Delta t) + i_{dg}(t - \Delta t)
\]

\[
+ \frac{2}{\Delta t} C_{gs} [v_{gsi}(t) - v_{gsi}(t - \Delta t)] - i_{gs}(t - \Delta t) \quad (5.2.39)
\]
Substituting the PWL approximation of $Q_{dg}$ into the discretized equation, we can get the following circuit equation for the gate terminal current

$$i_g(t) = a_{g1}v_{gi}(t) + a_{g2}v_{si}(t) + a_{g3}v_{di}(t) + I_g , \quad (5.2.40)$$

where the parameters are provided by the following relations:

$$a_{g1} = \frac{2C_{dg}}{\Delta t} + \frac{2C_{gs}}{\Delta t}$$

$$a_{g2} = -\frac{2C_{gs}}{\Delta t}$$

$$a_{g3} = -\frac{2C_{dg}}{\Delta t}$$

$$I_g = -\frac{2}{\Delta t}Q_{dgo} + \frac{2}{\Delta t}Q_{dg}(t - \Delta t) + i_{dg}(t - \Delta t) - \frac{2C_{gs}}{\Delta t}v_{gsi}(t - \Delta t) - i_{gs}(t - \Delta t) . \quad (5.2.41)$$

For $i_d$,

$$i_d(t) = \frac{2C_p}{\Delta t} [v_{dsi}(t) - v_{dsi}(t - \Delta t)] - i_{ds}(t - \Delta t)$$

$$+ I_{ds}(t) + \frac{(1 + \alpha)v_{dsi} + \eta}{r_{d} + \Delta t} + \frac{2}{\Delta t}Q_{dg}(t) - \frac{2}{\Delta t}Q_{dg}(t - \Delta t) - i_{dg}(t - \Delta t) . \quad (5.2.42)$$

Substituting the linearized expressions of $Q_{ds}$, $Q_{dg}$, $I_{ds}$ into this equation, the following relation can be obtained

$$i_d(t) = \left( \frac{2C_p}{\Delta t} + g_1 + \frac{1 + \alpha}{r_{d}} \right)v_{dsi}(t) + g_2v_{gsi}(t) + \frac{2C_{dg}}{\Delta t}v_{dgi}(t) + I_d , \quad (5.2.43)$$

where $I_d$ is as follows
Chapter 5.  Power MOSFET modelling and simulation

\[ I_d = -\frac{2C_p v_{dsi}(t - \Delta t) - i_{ds}(t - \Delta t)}{\Delta t} + I_{dso} + \frac{\eta}{r_{diode}} + \frac{2}{\Delta t} Q_{dgo} - \frac{2}{\Delta t} Q_{dg}(t - \Delta t) - i_{dg}(t - \Delta t) \]  

Equation (5.2.43) can be rewritten as a linear combination of node voltages

\[ i_d(t) = a_{d1} v_{gi}(t) + a_{d2} v_{si}(t) + a_{d3} v_{di}(t) + I_d \]  

where

\[ a_{d1} = g_2 - \frac{2C_{dg}}{\Delta t} \]
\[ a_{d2} = -\left(\frac{2C_p}{\Delta t} + g_1 + \frac{1 + \alpha}{r_{diode}}\right) - g_2 \]  
\[ a_{d3} = \left(\frac{2C_p}{\Delta t} + g_1 + \frac{1 + \alpha}{r_{diode}}\right) + \frac{2C_{dg}}{\Delta t} \]  

In a similar way we obtain the source terminal current \( i_s \). But since the terminal currents are related by KCL, we can simply find the linear parameters for \( i_s \) from

\[ i_s(t) = a_{s1} v_g(t) + a_{s2} v_s(t) + a_{s3} v_d(t) + I_s \]

where the parameters are provided by the following equations

\[ a_{s1} = -(a_{g1} + a_{d1}) \]
\[ a_{s2} = -(a_{g2} + a_{d2}) \]
\[ a_{s3} = -(a_{g3} + a_{d3}) \]
\[ I_s = -(I_g + I_d) \]  

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Chapter 5.  *Power MOSFET modelling and simulation*

Equations (5.2.47), (5.2.45) and (5.2.40) give the complete PWL forms for the implementation of the internal terminal currents of the VDMOST for nodal analysis. To simulate a complete VDMOST, the terminal resistances $R_s$, $R_d$ and $R_g$, as well as terminal linear inductances $L_s$, $L_d$ and $L_g$ have to be added to the internal equivalent circuit.

### 5.3 Power MOSFET circuit simulation

The simulation circuit is shown in figure 5.3.6. It is a VDMOST drive circuit with resistive load.

![VDMOST with resistive load](image)

*Figure 5.3.6 VDMOST with resistive load*

Figure 5.3.7 shows the simulation results of the VDMOST terminal voltages and currents.
Figure 5.3.7 Simulated switching waveforms, from top to bottom: input voltage on gate; output voltage on drain terminal; source terminal current; drain terminal current. Δt=200ns
Chapter 6. Discussions and Conclusion

In this thesis, a PWL modelling method has been combined with the very effective CDA integration scheme to simulate the time domain response of nonlinear voltage controlled charge and current devices and circuits. Very good simulation results have been obtained in several MOSFET circuit examples using the PWL direct solution algorithm. Very few works are found in the literature dealing with PWL modelling and simulation of MOSFET devices in which both nonlinear charges and currents are all multidimensional voltage-controlled functions. The proposed PWL solution scheme constitutes a new and effective transient analysis algorithm for nonlinear devices and circuits.

In comparison with the conventional Newton's iteration solution algorithms, our approach possesses the following advantages:

- No $C^1$ smooth requirement on the nonlinear analytical device model.
- No convergence problem since there is no iteration.
- Much faster solution speed.
- Suppression of numerical oscillation while keeping the computational accuracy of the trapezoidal integration.
- A high freedom of choosing modelling resolution to get the best compromise between the modelling accuracy and the simulation speed.

Since we have inserted two consecutive steps of BE integration rule for the suppression of numerical oscillations, the simulation is slowed down when the circuit solution switches from one PWL segment combination to another. When the solution stays within the same PWL segment, the integration rule is the trapezoidal rule which is much more accurate than the BE rule.

In the linearization aspect of PWL modelling, PWL region extrapolation is employed at the moment of switching regions. This can cause overshoot errors, even though the computational speed is much faster than that of the iterative solution method. Caution should be paid, however,
Chapter 6. Discussions and Conclusion

to the selection of the size of integration step in order to minimize the overshoot error. To get a more accurate circuit solution while maintaining a fast solution speed, future work may have to concentrate on searching for an effective iterative solution method.

As for the analytical modelling of MOSFET devices, since all the device models are based on the quasi-static assumption, they are valid only in the lower range of operational frequencies. To simulate higher frequency effects in MOSFET devices and circuits, non-quasi-static device models should be pursued.

In spite of the advantages of the proposed PWL algorithm, several important issues remain future researches:

• The effects of overshoot error and its influence on the solutions.
• The methodology in selecting a proper integration time step which can minimize the overshoot error while maintain a high simulation speed.
• The study of relations among discretization error, time step size and overshoot errors.
A First-Order MOSFET Charge Model

A first-order charge analytical model and channel current model are provided by the following piecewise equations [25]:

Normal mode $v_d \geq v_s$

1. When $v_{gb} \leq V_{FB}$

   $$Q_g = C_o (v_{gb} - V_{FB})$$
   $$Q_b = -C_o (v_{gb} - V_{FB})$$
   $$Q_s = 0$$
   $$Q_d = 0$$
   $$I_{ds} = 0$$  \hspace{1cm} (A.1)

2. When $v_{gb} > V_{FB}$ and $v_{gdt} \leq v_{gst} \leq 0$

   $$Q_g = C_o \gamma \left[ \sqrt{\left(\frac{\gamma}{2}\right)^2 + v_{gb} - V_{FB} - \frac{\gamma}{2}} \right]$$
   $$Q_b = -C_o \gamma \left[ \sqrt{\left(\frac{\gamma}{2}\right)^2 + v_{gb} - V_{FB} - \frac{\gamma}{2}} \right]$$
   $$Q_s = 0$$
   $$Q_d = 0$$
   $$I_{ds} = 0$$  \hspace{1cm} (A.2)
3. When $v_{gb} > V_{FB}$ and $v_{gdt} \leq 0 \leq v_{gst} \leq v_{gbt}$

\[
Q_g = C_o \left\{ \frac{2}{3} v_{gst} + V_t - (V_{FB} + 2\phi_F) \right\}
\]
\[
Q_b = -C_o \left\{ \frac{2}{3} v_{gst} + V_t - (V_{FB} + 2\phi_F) \right\}
\]
\[
Q_s = -\frac{2}{5} C_o v_{gst}
\]
\[
Q_d = -\frac{4}{15} C_o v_{gst}
\]
\[
I_{ds} = \frac{\mu W C_{ox}}{2L} v_{gst}^2
\] (A.3)

4. When $v_{gb} > V_{FB}$ and $0 < v_{gdt} \leq v_{gst} < v_{gbt}$

\[
Q_g = C_o \left\{ [V_t - (V_{FB} + 2\phi_F)] + \frac{2}{3} \left[ v_{gst} + v_{gdt} - \frac{v_{gst} v_{gdt}}{v_{gst} + v_{gdt}} \right] \right\}
\] (A.4)
\[
Q_b = -C_o \gamma \sqrt{2\phi_F} + v_{gbt} - v_{gst}
\] (A.5)
\[
Q_s = -\frac{C_o}{3} \left[ \frac{1}{5} v_{gst} + \frac{4}{5} v_{gdt} + \frac{v_{gst}^2}{v_{gst} + v_{gdt}} + \frac{1}{5} v_{gst} v_{gdt} (v_{gst} - v_{gdt}) \right]
\] (A.6)
\[
Q_d = -\frac{C_o}{3} \left[ \frac{1}{5} v_{gdt} + \frac{4}{5} v_{gst} + \frac{v_{gdt}^2}{v_{gst} + v_{gdt}} + \frac{1}{5} v_{gdt} v_{gst} (v_{gdt} - v_{gst}) \right]
\] (A.7)
\[
I_{ds} = \frac{\mu W C_{ox}}{2L} (v_{gst}^2 - v_{gdt}^2)
\] (A.8)
**Appendix. A**

**Reverse mode** $v_d < v_s$

Since the MOSFET is a symmetric device, the roles of the source terminal and drain terminal will be reversed under such bias. The charge and channel current equations of the normal operation model are all valid simply by swapping the voltage variable $v_{gst}$ to $v_{gds}$, and vice versa. Note, however, that the physical terminals remain the same.

The physical constants used in the calculations are

\[
\begin{align*}
W &= 50 \times 10^{-6} \text{ m} \\
L &= 50 \times 10^{-6} \text{ m} \\
\phi_T &= 0.33 \text{ volt} \\
V_{FB} &= -1.18 \text{ volt} \\
\gamma &= 1.03 \text{ volt}^{1/2} \\
\mu &= 700 \times 10^{-4} \text{ m}^2/\text{s} \\
T_{ox} &= 10^{-9} \text{ m} \\
K_{ox} &= 3.9 \\
\epsilon_0 &= 8.86 \times 10^{-14} \text{ Farad/m} \\
\epsilon_{ox} &= K_{ox} \times \epsilon_0 \text{ Farad/m} \\
C_{ox} &= \epsilon_{ox}/T_{ox} \text{ Farad/m}^2 \\
C_0 &= W \times L \times C_{ox} \text{ Farad}
\end{align*}
\]

Figures A.1 to A.4 show the surface shape of three nonlinear charges and the nonlinear channel current under the condition of $v_{gs} = 0$ volts.
Appendix A

Charge on Cgs

\[ V_{gb}=0, \; DV=2v, \; Q_{gs} \text{ vs. } V_{gs}(-20v,20v), V_{gd}(-20v,20v) \]

Figure A.1 Source terminal charge Qs

Charge on Cgd

\[ V_{gb}=0, \; DV=2v, \; Q_{gd} \text{ vs. } V_{gs}(-20v,20v), V_{gd}(-20v,20v) \]

Figure A.2 Drain terminal charge Qd

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Appendix A

Charge on Cgb

\[ V_{gb}=0, \Delta V=2V, Q_{gb} \text{ vs. } V_{gs}(-20V,20V), V_{gd}(-20V,20V) \]

Figure A.3 Substrate terminal charge Qb

Channel current Ids

\[ V_{gb}=0, \Delta V=2V, \text{Ids vs. } V_{gs}(-20V,20V), V_{gd}(-20V,20V) \]

Figure A.4 Channel current Ids

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Appendix B

PWL Coefficients for MOSFET Terminal Currents

The linear coefficients of the drain, substrate and gate currents for time domain analysis using the trapezoidal integration rule are given below.

Drain terminal $i_d$

$$h_{d1} = -\frac{2}{\Delta t} (C_{d1} + C_{d2} + C_{d3}) - \frac{2}{\Delta t} C_{gdo} + (G_{gs} + G_{gd} + G_{gb})$$

$$h_{d2} = \frac{2}{\Delta t} C_{d1} - G_{gs}$$

$$h_{d3} = \frac{2}{\Delta t} C_{d2} + \frac{2}{\Delta t} C_{gdo} + \frac{2}{\Delta t} C_{db} - G_{gd}$$

$$h_{d4} = \frac{2}{\Delta t} C_{d3} - \frac{2}{\Delta t} C_{db} - G_{gb}$$

$$I_d = -\frac{2}{\Delta t} Q_{gdo} + I_{dso} + IH_d$$

Substrate terminal $i_b$

$$h_{b1} = -\frac{2}{\Delta t} (C_{b1} + C_{b2} + C_{b3}) - \frac{2}{\Delta t} C_{gbo}$$

$$h_{b2} = \frac{2}{\Delta t} C_{b1} - \frac{2}{\Delta t} C_{sb}$$

$$h_{b3} = \frac{2}{\Delta t} C_{b2} - \frac{2}{\Delta t} C_{db}$$

$$h_{b4} = \frac{2}{\Delta t} C_{b3} + \frac{2}{\Delta t} (C_{gbo} + C_{sb} + C_{db})$$

$$I_b = -\frac{2}{\Delta t} Q_{gbo} + IH_b$$

Gate terminal $i_g$

$$h_{g1} = -(h_{s1} + h_{d1} + h_{b1})$$

$$h_{g2} = -(h_{s2} + h_{d2} + h_{b2})$$

$$h_{g3} = -(h_{s3} + h_{d3} + h_{b3})$$

$$h_{g4} = -(h_{s4} + h_{d4} + h_{b4})$$

$$I_g = -(I_s + I_d + I_b)$$

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References


