GALLIUM ARSENIDE INTEGRATED CIRCUIT MODELING, LAYOUT AND FABRICATION

by

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ABSTRACT

The object of the work described in this thesis was to develop GaAs integrated circuit modeling techniques based on a modified version of SPICE 2, then layout, fabricate, model and test ion implanted GaAs MESFET integrated sample and hold circuits.

A large signal GaAs MESFET model was used in SPICE to evaluate the relative performance of inverted common drain logic (ICDL) digital integrated circuits compared to other circuit configurations.

The integrated sample and hold subsequently referred to as an integrated sampling amplifier block(ISAB), uses a MESFET switch with either one or two guard gates to suppress strobe feedthrough.

Performance guidelines suggested by the project sponsor indicate an optimal switch sampling pulse width capability of 25 ps with 5 ps rise and fall time. Guard gates are included in the switch layout to evaluate pulse feedthrough minimization. The project sponsor suggested -20 dB pulse feedthrough isolation and minimum sampling switch off isolation of -20 dB at 10 GHz as project guidelines.

Simulations indicate that a 0.5 μm gate length process approaches the suggested performance guidelines. A mask layout was designed and modeled including both selective implant and refractory self aligned gate processes. The refractory self aligned gate process plasma etched t-gate

structure produces a sub 0.5 μm gate length.

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Symbol Definitions

Symbol	Units	Description
δ_I	μm	mask intra layer skew
δ_L	μm	mask inter layer skew
δ_A	μm	mask alignment skew
δ_{LA}	μm	lateral alloy movement
ϵ	F/cm	free space permittivity
ϵ_{GaAs}	F/cm	permittivity of GaAs, taken as 12.9ϵ
μ_H	$cm^2/V\text{-}s$	Hall mobility
μ_o	$cm^2/V\text{-}s$	electron low field drift mobility
μ_n	$cm^2/V\text{-}s$	electron drift mobility
ρ	Ω/cm	specific resistivity
ρ_{Cn}	$\Omega/\mu m^2$	contact specific resistance, C1 = N^+ GaAs to AuGe, C2 = AuGe to TiW.
ΔR_p		standard deviation of the implant
τ	ps	channel transit time = L/v_{dr}
v_s	cm/s	saturated electron drift velocity $=\mu_n E_s$
ϕ_{Bn}	V	Schottky barrier height on n-GaAs
Θ_G	$rad/\mu m$	gate phase shift
β	A/V^2	MESFET model current gain factor
λ	V^{-1}	channel length modulation parameter
α	V^{-1}	hyperbolic tangent function parameter
E_s	V/cm	velocity saturation field $=v_s/\mu_n$
L	μm	channel length

t	μm	apparent channel thickness
A	μm	effective uniform profile channel thickness
L_G	μm	metallurgical gate length
L_{gap}	μm	effective MESFET source or drain to gate gap or diode Schottky metal to ohmic gap.
Z	μm	gate width dimension
C_{GD}	$fF/\mu m$	gate to drain capacitance
C_{GS}	$fF/\mu m$	gate to source capacitance
C_{DS}	$fF/\mu m$	drain to source capacitance
C_{SC}	$fF/\mu m$	space charge capacitance
R_{ps}	$\Omega/\mu m$	Schottky diode parasitic series resistance
R_G	Ω	gate series resistance
R_S	Ω	source series resistance
R_D	Ω	drain series resistance
R_{si}	$\Omega/\square$	LEC GaAs semi-insulating sheet resistivity
R_{SH}	Ω	drain to source shunt resistance
g_m	mA/V	$\partial I_{DS}/\partial V_{GS}$
I_{DS}	$mA/\mu m$	drain to source current
I_{DSS}	$mA/\mu m$	saturated drain to source current at stated V_{GS} and V_{DS}

V_{gs}	V	internal gate to source voltage
V_{GS}	V	external gate to source voltage
V_{ds}	V	internal drain to source voltage
V_{DS}	V	external drain to source voltage
V_{bs}	V	substrate bias voltage
f_T	Hz	cutoff frequency = $1/(2\pi\tau)$
V_{bi}	V	(positive) built-in voltage at the gate
V_P	V	pinchoff voltage $=q/\epsilon_{GaAs}\int_0^t N(x)xdx$
V_T	V	threshold voltage $V_T=V_P+V_{bi}$
W_0	μm	zero gate bias depletion width
W_1	μm	the doping profile depth at a doping level of 10^{16}
n		diode ideality factor
N(x)	ions/cm^3	activated ion implanted doping profile
N_a	ions/cm^3	effective p-doping substrate concentration
N_D	ions/cm^3	effective uniform profile channel doping density
N_{max}	ions/cm^3	peak value of doping profile
q	C	electron charge
n	e/cm^3	free electron concentration
n_i	e/cm^3	intrinsic free electron concentration
N_C	s/cm^3	effective density of states in conduction band

N_T	s/cm^3	total concentration of traps
Q_1	$ions/cm^2$	total N^- dose
Q_2	$ions/cm^2$	total N^+ dose
Q_a	ions/cm	available dose $=\int_0^t N(x)dx$
Φ_1	keV	N^- implant energy
Φ_2	keV	N^+ implant energy
R_{PO}	cm	projected range of the implantation
R_P	cm	effective projected range $R_{PO}-\Delta R_p$

List of Acronyms

Acronym	Meaning
BFL	buffered FET logic
CAD	computer aided design
EBL	electron beam lithography
ID	interdigitated
MBE	molecular beam epitaxy
MESFET	metal semiconductor field effect transistor
MIM	metal insulator metal
PR	positive photoresist
RD	refractory diode
RIE	reactive ion etch
RSAG	refractory self aligned gate
ISAB	integrated sampling amplifier block
SD	selective implant diode
SEM	scanning electron microscope
SI	selective implant
SPICE	simulation program with integrated circuit emphasis
TD	two implant diode, SD on N^+

1. INTRODUCTION

The purpose of this work was to investigate the design, simulation and fabrication of GaAs devices and in particular of a GaAs sample and hold device. The work was sponsored by the Defense Research Establishment Ottawa.

1.1 INTEGRATED SAMPLING AMPLIFIER OVERVIEW

One of the target applications for integrated GaAs sample and holds is a microwave acquisition system or digital radio frequency memory(DRFM)[1.1]. This involves sampling a microwave frequency signal on an input delay line at regular distributed points. Ideally the entire unit would be constructed on a single chip, complete with microstrip delay line, pulse generator, controller circuits, and analog to digital conversion.

The primary purpose of the simulation, layout and fabrication is to investigate and optimize, as far as possible within the confines of the available process parameters, the performance of the integrated sampling amplifier (ISAB). The most important aspects of the ISAB are a low input time constant, ideally less than 25ps, combined with minimal strobe "blow-by".

In previous published work Saul[1.2] demonstrated a MESFET switch ring approach with greater than 40dB of "OFF" isolation and an acquisition time of 2ns suggesting operation up to 250MHz. Sample pulse "blow-by" or feedthrough was minimized by careful chip and circuit layout

to minimize capacitive coupling. Sample strobe feedthrough ranged from a worst case of about 80mV to an average of about 20 to 30 mV on a 2.5V signal corresponding to about 40dB of strobe isolation from the sampled signal.

A 1μm SI triple gate MESFET switch ISAB with a 65ps input time constant was built and tested to 500 Megasamples per second, using a 36MHz sine-wave input by G.S. Barta and A.G. Rode[1.3]. Isolation in the "OFF" state was about 40dB with a MHz band input. Sample strobe blow-by was -35mV on a 300 mV signal, corresponding to 18.6dB of strobe isolation. The test equipment was considered inadequate for the full capability of the device. If the MIM capacitor was omitted an input time constant of about 33ps would result, close to the desired specification. However absence of the MIM capacitor would likely result in a reduction of strobe isolation below the already marginal specification.

Work at U.B.C. by Durtler attempted to extend the results of Barta and Rode using a single and dual gate switch configuration[1.4].

The ISAB configuration, shown in figure 1.1, consists of either a single, dual or triple gate sampling switch followed by a MIM or interdigitated hold capacitor and an amplifier. Due to the low acquisition time, switch configuration variations are designed to investigate the relative merit of MESFET "guard gates" (BSG1 and BSG2 in Fig. 1.1) in suppressing sampling strobe feedthrough to the signal path.

The amplifier is, in its open loop form, essentially a BFL inverter, shown with the ICDL modeling section of Appendix A. Feedback is achieved by adding another MESFET(BFB) with source and drain, in parallel with the input MESFET as shown in Fig. 1.1. The amplifier was developed to enable cascading and is treated extensively by D.P. Hornbuckle, R.L. Van Tuyl and D.B. Estreich [1.5,1.6,1.7,1.8].

The MESFET integrated sampling switch and amplifier built and tested by G. S. Barta and A. G. Rode[1.3], was fabricated in SI process technology, with the Nminus channel implant through a 100nm silox film yielding V_P=-1.5 V or V_T≃-0.8 V. The lithographic resolution was 1μm lines and 1μm gaps for the triple gate structure resulting in an "ON"

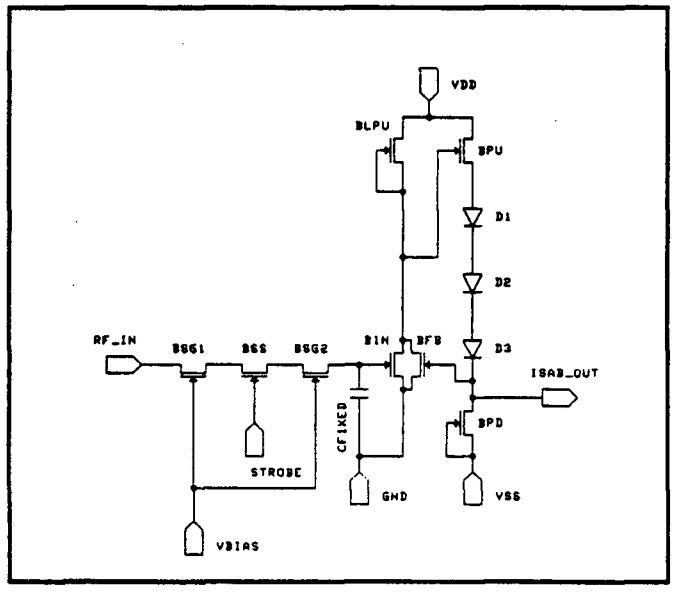


Fig. 1.1 Integrated Sampling Amplifier Block configuration.

resistance of 120Ω at V_{gs}=0 V for a 100μm width, or 12000Ω/μm. The base RC input time constant calculated from this is 36ps as compared to the 65ps input time constant arrived at with 90% sampling efficiency with a 150ps strobe. If the system is considered as a simple RC network with a switch input step height V_i and the capacitor initially at V_{h0} such that $\delta V=V_i-V_{h0}$ then $V_h(t)=V_i-\delta Ve^{-t/\tau}$ and 90% of δV is lost in $t=2.3\tau$. This would imply an input time constant of 83ps for the switch, as compared to the measured 65ps. However the MESFET I_{ds} is not linear with V_{ds} and the strobe can be driven to 0.5+ V providing more node charging current.

The amplifier output stage diode stack employs diodes fabricated using gate metal on N+ GaAs, reducing the series resistance(R_{ps}) per unit width of the forward biased stack diodes. A 150fF MIM capacitor was formed by using 100 nm of sputtered silicon nitride over an AuGe base plate resulting in a total of about 300fF sample node capacitance and a droop rate of 4 mV/μs. The use of external capacitors induces excessive ringing due to lead inductance[1.2]. The amplifier had a measured 3dB bandwidth of 1.1GHz with unity gain feedback and a measured system slew rate of 800 V/μs.

The aim of the present project was to extend the work of Barta and Rode by modeling and implementing an ISAB in refractory self aligned gate(RSAG) technology using lithographic resolution of 1μm line and 2μm gaps as shown in figure 1.2. As the RSAG process is a t-gate technology the

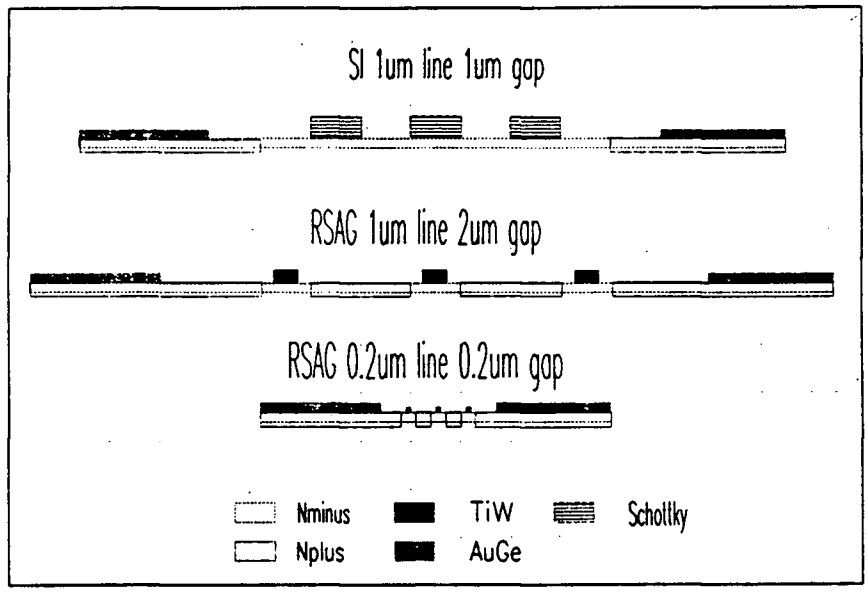


Fig. 1.2 Triple Gate Switch Cross Sections.

resulting submicrometer gate will exhibit a reduced C_{gs} which should reduce the displaced charge during strobe operation and increase the strobe isolation to over 20dB. The input time constant should be reduced by decreasing the "ON" resistance per μm with the self aligned intergate Nplus implant. Considering the triple gate structures of figure 1.2 four series parasitic resistance regions will have a sheet resistance reduction of about 5 times which should reduce "ON" resistance by 15 to 20% compared to Barta and Rode. Thus the same width switch RSAG version of the SI triple gate ISAB should have a 55ps input time constant with about 25dB of strobe isolation. Strobe isolation could then be sacrificed by reducing the node capacitance to bring the input time constant into the 25ps range. This implies that

operation up to 20GHz would be possible with the triple gate configuration. Dual and single gate configurations would have lower input time constants, which is the main priority of the work.

The RSAG process has been demonstrated for digital integrated circuits[1.9,1.10,1.11] of short gate width(10μm) and gate length down to less than 0.1μm using electron beam lithography(EBL). Devices with 0.5μm gate length are obtainable with 300nm optical lithography capable of 1μm linewidths[1.4]. Considering the 0.2μm EBL triple gate of figure 1.2, "ON" resistance would be reduced by about ten times and C_{gs} about 5 times compared to the other RSAG cross section. This implies that operation up to several hundred GHz would be possible with good strobe isolation.

As the RSAG TiW or tungsten silicide gate metalization is more resistive than SI gate metalizations RSAG switch gates should be driven at one or more t-junctions, similar to power MESFETs.

In order to fabricate RSAG MESFET ISABs with low R_{ps} Schottky diodes for the amplifier output stage and MIM capacitors, eight mask layers were necessary. Interdigitated hold capacitors were used in the ISAB layouts as an alternative to the MIM type and if successful will result in the elimination of one mask layer and an increase in yield, which would be significant for the single chip acquisition system. Only the refractory and Schottky metalizations are shown in figure 1.3 for clarity.

Lithographic plate process related layout variations are designed to enable fabrication of high performance working devices, with manufacturable tolerances. As such SI layouts with 1μm gate lengths and 2, 3, or 4μm source and drain to gate gaps are combined with six RSAG layouts with 1 or 2μm gate mask lengths and 2, 3, or 4 μm source and drain

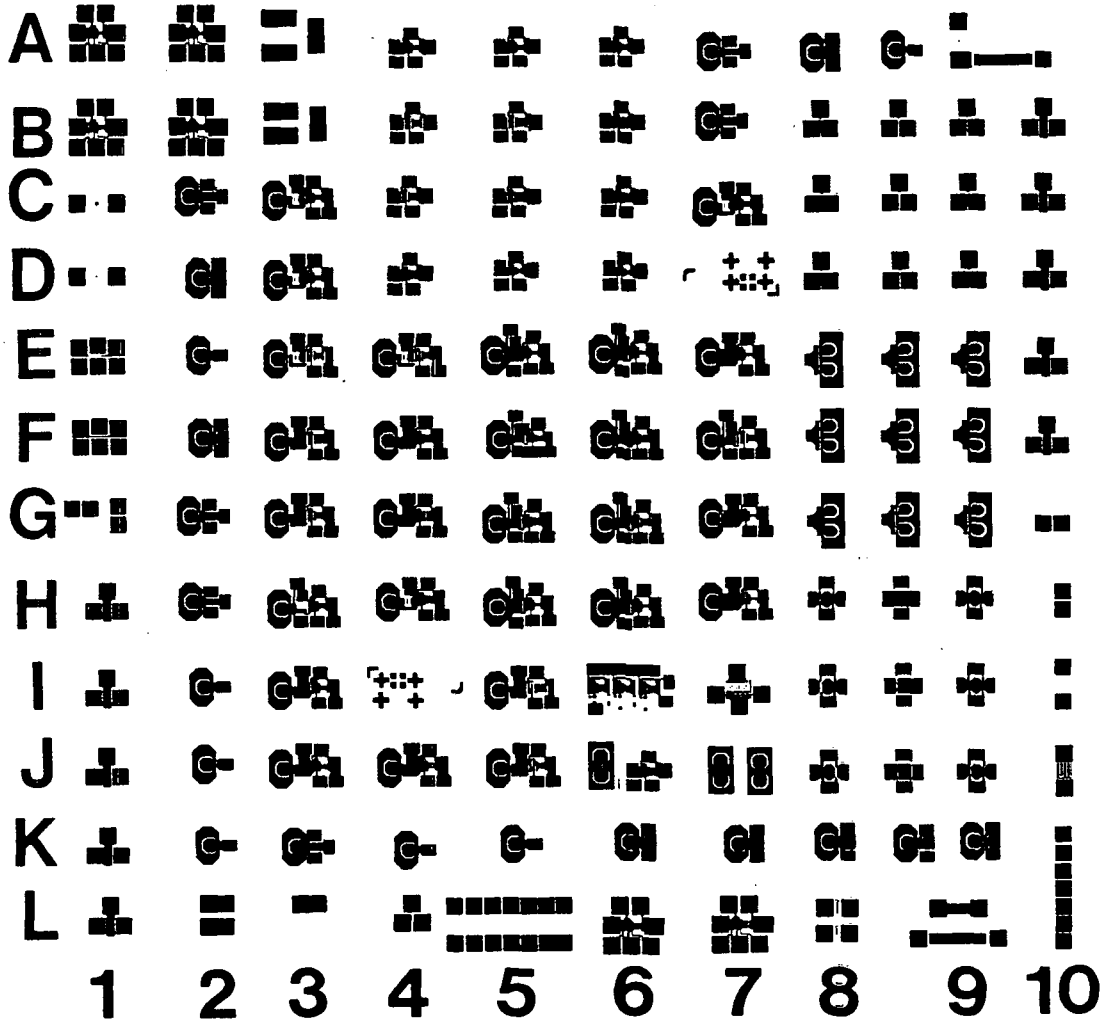


Fig. 1.3 Overall layout pattern.

to gate gaps, for a total of nine basic MESFET variations.

It was necessary to leave approximately 300μm channels between the device die to enable nondestructive separation with a narrow blade saw, assuming a cutting channel of about 100 μm and a chipping width of about 40μm [1.12]. This requirement served to motivate compaction of the device pad frame in order to maximize the number of ISAB units in the lithographically optimal inner 60% of the overall pattern[1.13]. A modified pad frame may be necessary later in the discrete phase of the project to enable automatic probing. Conversely the one chip acquisition system would have minimal pad requirements enabling circuit compaction within the limits of the transmission line geometries.

The first mask layer is used to control an alignment etch in the surface about 2μm deep to provide a reference for all subsequent layers. The second layer provides holes through which to implant the active regions for MESFET channel characteristics (N^-). The third layer provides a pattern for the t-gate top for the RSAG process, protecting regions of TiW from removal. The fourth layer provides an implant mask for the N^+ regions.

The fifth mask is for ohmic contact to the N^+ regions and production of MIM bottoms and inductors over nonactivated substrate. The sixth layer is a positive overlay mask protecting the MIM insulator Si_3N_4 dielectric from etching, (which could be eliminated). The seventh mask is for SI Schottky metalization providing a high quality

interface for N^+ diodes and MESFET gates. This metalization serves a dual purpose as the MIM capacitor top plate. The eighth mask defines openings which are to be gold plated to a few μm for airbridge bodies and bonding pad thickening. The N^- mask can be used with negative photo resist for implant isolation if necessary.

The overall pattern outer dimensions are approximately 8.8mm high by 9.2mm across. Test patterns for process calibration and device characterization are around the outer edge of the pattern. The devices are listed in table 1.1 with alphanumeric grid reference to figure 1.3. The trailing grid reference characters(L,R,T,B) refer to the left, right, top and bottom of the addressed cell.

Loc	Item	Description/Code
A 1	diagnostic amplifier	AORT2_9024
A 2	diagnostic amplifier	AORR2_9024
A 3LT	RD diagnostic diode	5μm L_S
A 3LB	RD diagnostic diode	10μm L_S
A 3R	RD diagnostic diode	3μm L_S
A 4	amplifier	AFRT3_9024
A 5	amplifier	AFRT3_9023
A 6	amplifier	AFRT3_9022
A 7	switch	R2_40_1_2
A 8	switch	R3_60_1_3
A 9L	switch	R1_40_1_2
A 9R	L C calibration	inductor test
B 1	diagnostic amplifier	AORT3_9024
B 2	diagnostic amplifier	AORR3_9024
B 3LT	TD diagnostic diode	5μm L_S
B 3LB	TD diagnostic diode	10μm L_S
B 3R	TD diagnostic diode	3μm L_S
B 4	amplifier	AFRT3_9014
B 5	amplifier	AFRT4_9014
B 6	amplifier	AFRR3_9012
B 7	switch	R3_60_1_2
B 8	100μm test FET	SF_100_1_3
B 9L	100μm test FET	SF_100_1_4

B 9R	100μm test FET	RF_100_2_4
B 10	fat FET	RSAG normal
C 1	inductor	large center
C 2	switch	R2_60_2_2
C 3	ISAB	RM16R924T3
C 4	amplifier	AFRT3_9013
C 5	amplifier	AFRT4_9013
C 6	amplifier	AFRR3_9013
C 7	ISAB	RM16R922T3
C 8	100μm test FET	SF_100_1_2
C 9L	100μm test FET	RF_100_1_4
C 9R	100μm test FET	RF_100_2_3
C 10	fat FET	RSAG no Nplus
D 1	inductor	small center
D 2	switch	R3_60_2_4
D 3	ISAB	RM16R923T3
D 4	amplifier	AFRT3_9012
D 5	amplifier	AFRR2_6012
D 6	amplifier	AFRR2_6013
D 7	alignment mark	
D 8	100μm test FET	RF_100_1_2
D 9L	100μm test FET	RF_100_1_3
D 9R	100μm test FET	RF_100_2_2
D 10	fat FET	SI on Nplus
E 1	stepped resistor	TiW 3 step
E 2	switch	R1_60_2_2
E 3	ISAB	RM16R914T3
E 4	ISAB	RM16R913T3
E 5	ISAB	SI3S912T3
E 6	ISAB	SI2S912T3
E 7	ISAB	SI1S912T3
E 8	π-gate FET	RF_236_1_4
E 9L	π-gate FET	SF_236_1_2
E 9R	π-gate FET	RF_236_2_4
E 10	fat FET	SI normal
F 1	stepped resistor	TiW 3 step
F 2	switch	R3_60_1_4
F 3	ISAB	RI16R913T4
F 4	ISAB	RI16R912T3
F 5	ISAB	RI34R612T3
F 6	ISAB	RI36R912T3
F 7	ISAB	RI36R913T3
F 8	π-gate FET	RF_236_1_3
F 9L	π-gate FET	SF_236_1_3
F 9R	π-gate FET	RF_236_2_3
F 10	fat FET	SI on both
G 1L	isolation monitor	lateral 10μm by 150μm gap
G 1R	isolation monitor	vertical
G 2	switch	R2_60_1_2
G 3	ISAB	RI16R913T3
G 4	ISAB	RI16R912R3
G 5	ISAB	RI26R912T3
G 6	ISAB	RI26R913T3
G 7	ISAB	SI1S913T3
G 8	π-gate FET	RF_236_1_2
G 9L	π-gate FET	SF_236_1_4
G 9R	π-gate FET	RF_236_2_4

G 10	isolation monitor	lateral
H 1	fat FET	RSAG normal
H 2	switch	R3_40_1_2
H 3	ISAB	RI26R922T3
H 4	ISAB	RM16R912T3
H 5	ISAB	SI3S913T3
H 6	ISAB	SI2S913T3
H 7	ISAB	SI1S914T3
H 8	dual gate FET	RMPR_1_2
H 9L	dual gate FET	SMPR_1_2
H 9R	dual gate FET	RMPR_2_2
H 10	isolation monitor	vertical
I 1	fat FET	RSAG no Nplus
I 2	switch	R1_60_1_2
I 3	ISAB	RI16R924T3
I 4	alignment mark	
I 5	ISAB	RI16R914T4
I 6	3 amp oscillator	OFRT39013
I 7	power FET	dfet-500μm
I 8	dual gate FET	RMPR_1_3
I 9L	dual gate FET	SMPR_1_3
I 9R	dual gate FET	RMPR_2_3
I 10	meander	AuGe
J 1	fat FET	SI on Nplus
J 2	switch	R1_60_1_3
J 3	ISAB	RI16R923T3
J 4	ISAB	RI16R922T3
J 5	ISAB	RI16R914T3
J 6	modulator	M26R912T3
J 7L	dual gate switch	rm2_40_1_2
J 7R	dual gate switch	rm2_40_1_3
J 8	dual gate FET	RMPR_1_4
J 9L	dual gate FET	SMPR_1_4
J 9R	dual gate FET	RMPR_2_4
J 10	meander	SI gate metal
K 1	Fat FET	SI on Nminus
K 2	switch	R1_60_2_3
K 3	switch	R3_60_2_2
K 4	switch	R1_60_2_4
K 5	switch	R1_60_1_4
K 6	switch	R2_60_1_4
K 7	switch	R2_60_1_3
K 8	switch	R2_60_2_4
K 9L	switch	R2_60_2_3
K 9R	switch	R3_60_2_3
L 1	fat FET	SI on both
L 2T	SD diagnostic diode	5μm L_S
L 2B	SD diagnostic diode	3μm L_S
L 3	SD diagnostic diode	10μm L_S
L 4	airbridge test	AuGe under bridge
L 5T	transmission line	on Nminus
L 5B	transmission line	on both
L 6	diagnostic amplifier	AORT4_9024
L 7	diagnostic amplifier	AORR4_9024
L 8T	MIM capacitor	area 5 by 100μm
L 8B	MIM capacitor	area 6 by 60μm

L 9T	Interdigitated capacitor	14 half pairs 200μm long
L 9B	MIM capacitor	area 50,000μm²
L 10	transmission line	on Nplus

Table 1.1 Overall mask pattern die locations

Device codes, for the most part, serve the dual purpose of CAD data base file name and unit description.

The switch identification code begins with the process type, 'R' for RSAG and 'S' for SI, followed by the number of gates, the gate width over the active region, the mask gate length and the source/drain to gate gap in μm. The π-gate FET code begins with the process type followed by 'F', the gate width over the active region, mask gate length and source/drain to gate gap. The dual gate FET code begins with the process type followed by the logo "MPR" of the target test facility, Microtel Pacific Research, then mask gate length and source/drain to gate gap.

For the amplifiers the first two characters identify configuration as open loop 'AO' or feedback 'AF' followed by the MESFET process type. The next two characters are the diode process type, 'T' for SI gate metal on Nplus, and the number of diodes in the stack. The first two of the last four digits indicate the output stage MESFET width, followed by the mask gate length and source/drain to gate gap.

The ISAB code starts with the switch process type followed by the hold capacitor type, 'M' for MIM and 'I' for interdigitated, the number of gates in the switch, a single digit representation of the switch gate width(ie. 6 for

60μm), the amplifier MESFET process type, a single digit representation of the output stage width(ie. 9 for 90μm), then source/drain to gate and intergate gap for both the switch and amplifier, and finally the diode process type and number of diodes in the stack.

2. PROCESS DEFINITION, PARAMETER EXTRACTION AND MASK LAYOUT

Process parameters required for layout were estimated from previous work, then adjusted by calculation for current process requirements.

2.0.1 PROCESS PARAMETERS

Table 2.1 represents averaged data from Dindo[2.1] at U.B.C. and Sadler[2.2] at Cornell University, concerning Si ion implanted processing of LEC GaAs.

Parameter	Value	Source
R_{si}	$3 \cdot 10^{3}$ Ω/□	[2.1]
Q_1	$2.2 \cdot 10^{12}$ ions/cm²	[2.1]
Φ_1	100 keV	[2.1]
R_{sht1}	1542 Ω/□	[2.1]
V_T	-1.97 V	[2.1]
V_P	2.67 V	[2.1]
R_{P1}	85 nm	[2.1]
ΔR_{P1}	44.2 nm	[2.1]
W_0	114 nm	[2.1]
W_1	244 nm	[2.1]
N_{max1}	$1.27 \cdot 10^{17}$	[2.1]
Q_2	$2 \cdot 10^{13}$ ions/cm²	[2.2]
Φ_2	150 keV	[2.2]
R_{sht2}	320 Ω/□	[2.2]
R_{P2}	110 nm	[2.2]
ΔR_{P2}	96 nm	[2.2]
N_{max2}	$5.2 \cdot 10^{17}$	[2.2]
Nplus to AuGe ρ_{C1}	65 Ω/μm²	[2.2]
AuGe to TiW ρ_{C2}	78 Ω/μm²	[2.2]

Table 2.1 Process Parameters

2.1 PROCESS DEFINITION

Plate definitions used for fabrication (Table 2.2) are a consequence of ISAB features and the process steps to build them. The plates can be used with discretion to include or omit device features for a given process run.

Plate	Name	Description
1N	Align	Align Etch pattern for subsequent layers.
2N	Nminus	The Nminus implant is the same for all FETs and Diodes active region.
3N	TiW	Defines t-gate and all TiW not etched.
4N	Nplus	Defines the Nplus implant window allowing selective FET fabrication.
5N	AuGe	Defines ohmic contacts and MIM capacitor bottoms.
6P	Dielectric	Si_3N_4 capacitor dielectric is etched back to PR islands.
7N	Schottky	Schottky SI FET, TD diode metal, MIM tops and airbridge footing.
8N	Airbridge	Airbridge body, connector run and bonding pad thickening.

Table 2.2 Process Plates

The plates are designated by their plate name in the following process listing. The letter "N" or "P" following the plate number corresponds to positive or negative in terms of relation of the residual photoresist on the wafer, using positive photoresist, to the enclosed layer on the CAD station screen. "N" refers to no positive photoresist(PR) left in the enclosed area and "P" refers to PR remaining in the enclosed area, being developed away elsewhere.

2.1.1 PROCESS LISTING

The process allows production of both SI and RSAG devices concurrently, specifically allowing the use of low resistance two implant (TD) type diodes for RSAG amplifiers. As process results will be optimized for a given subprocess individual ISAB units were constructed from components of the same type with the notable exception of the diode stack.

The RSAG process should be optimized with respect to ion implantation, TiW thickness, and plasma or reactive ion etch parameters, as a result of the 1 and 0.5μm mask gate lengths, only one may be made optimal on a given wafer run. These fabrication parameters should be optimized for switch transient characteristics as the main priority as long as this is consistent with amplifier operation and process yield.

Bevelling was found to be necessary on test pieces for reducing photoresist edge bead height. If the bevelling is omitted increased mask to surface gap results in loss of line width control and rectangular edge profile as seen in figure 2.1.

Process steps 30 to 57 are similar to those developed for MMIC manufacturing[2.3,2.4].

Problems with implant activation uniformity and dislocations due to handling are expected[2.5,2.6].

Step Description

1 Wafer bevelling(test pieces only) and surface layer removal:

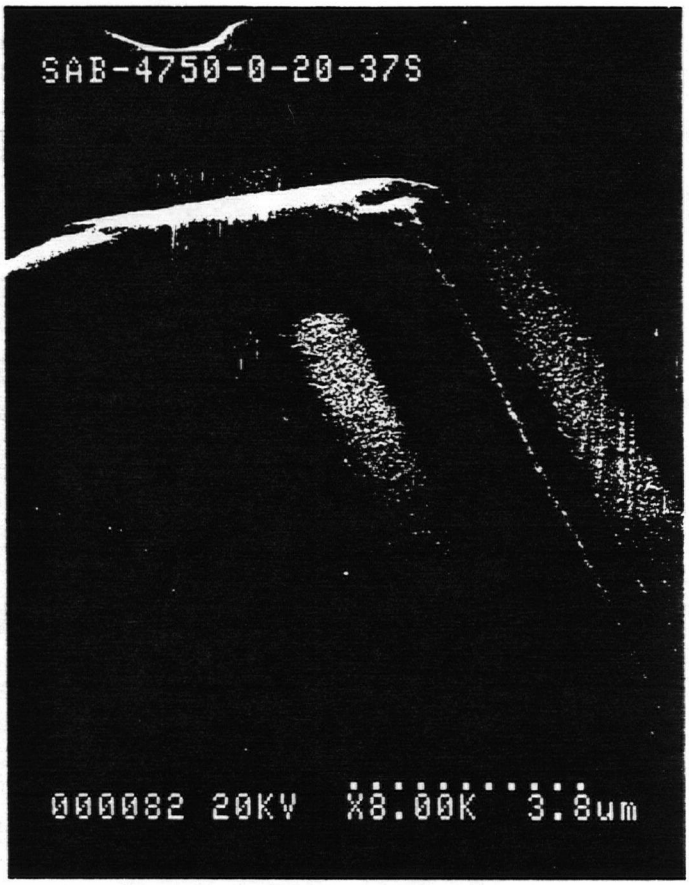


Fig. 2.1 Nonbevelled PR edge profile, no chlorobenzene soak.

-deposit silicon nitride or Al over new wafer
-scribe and break wafer as desired
-spin on photoresist at low rpm
-mount pieces to be bevelled with beeswax on glass slide or aluminum bevelling fixture for quarters
-bevel wafer edges using 1.0μm alumina polishing compound on polisher, heating beeswax on hot plate to rotate

-remove PR, beeswax and alumina in boiling acetone
-use hot acetone then trichloroethylene followed by Microstrip to remove residue, then rinse in DI water
-remove protective layer with HF
-1% Alconox solution
-DI water rinse
-First etch solution: 5:NH_4OH 2:H_2O_2 240:DI
-DI water rinse
-Buffered HF
-10% NH_4OH
-DI water rinse
-Nitrogen blow dry

2 Photoresist deposition for alignment etch
-Photoresist thickness: 1.5μm

3 Photoresist pattern exposure for alignment etch
-Plate: Align
-Mask to PR method: vacuum contact

4 Photoresist develop for alignment etch
-Developer type MF-316
-Spray application
-DI water rinse

5 Alignment etch of GaAs surface
-Etch solution: 5:NH_4OH 2:H_2O_2 240:DI

6 Photoresist removal
-Boiling acetone
-Boiling isopropanol

7 Photoresist deposition for Nminus implant
-Photoresist thickness: 1.5μm

8 Photoresist pattern exposure for Nminus implant
-Plate: Nminus
-Mask to PR method: depends on work piece

9 Photoresist develop for Nminus implant
-Developer type: MF-316
-Spray application
-DI water rinse

10 Nminus Implant
-Species: Si^{29}
-Energy: Φ_1 keV
-Dose: Q_1 ions/cm^2
-Wafer tilt: 11°
-Wafer rotation: 22°

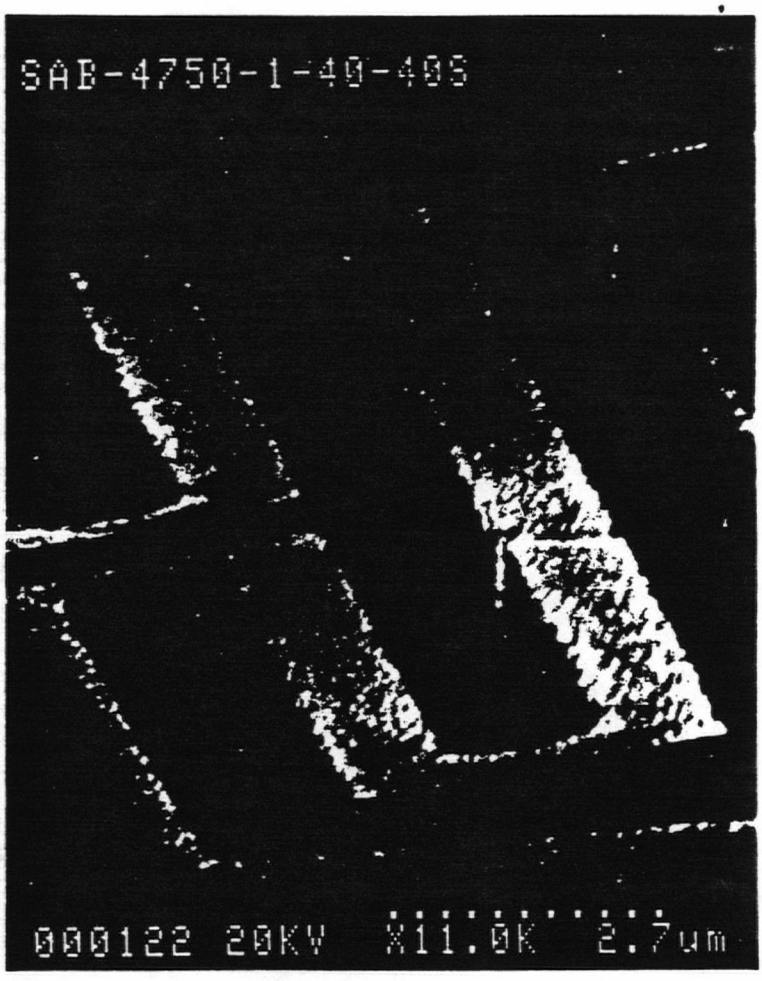


Fig. 2.2 Bevelled profile with chlorobenzene

11 Photoresist removal
- -Hot Microstrip ®™ Shipley Ltd.
- -Boiling acetone
- -Boiling isopropanol

12 Light cleaning etch
- -Etch solution: 1:NH_4OH 1:H_2O_2 240:DI
- -DI water rinse
- -Buffered HF
- -10% NH_4OH

-DI water rinse
-Nitrogen blow dry

13 Refractory metal deposition
-Method: rf sputter, Ar atmosphere, TiW
-Pressure 33 mTorr
-RSAG thickness optimization h_f

14 Refractory metal surface cleaning
-Buffered HF
-DI water rinse
-Nitrogen blow dry

15 Photoresist deposition for t-gate mask
-Photoresist thickness: 1.5μm
-Critical: prebake to remove water traces.
-Spin on
-Softbake

16 Photoresist pattern exposure for t-gate
-Plate: TiW
-Mask to PR method: vacuum contact

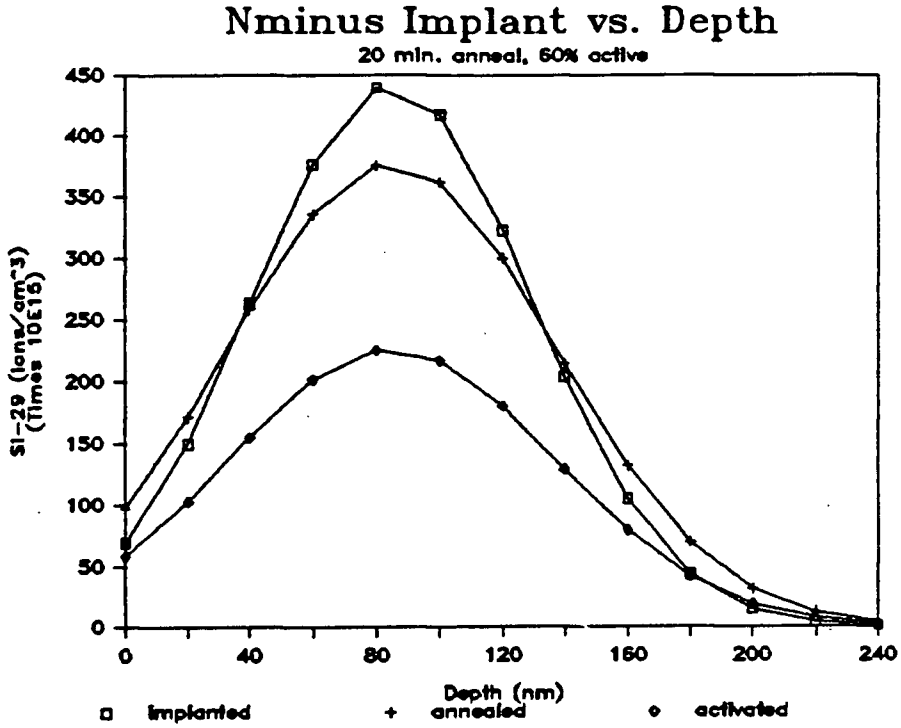


Fig. 2.3 Nminus implant profile

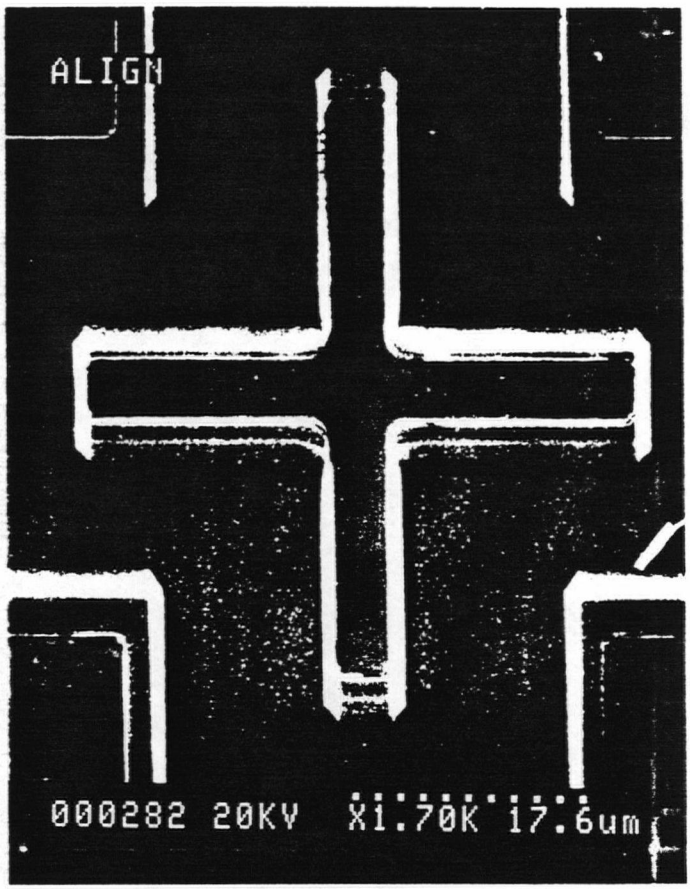


Fig. 2.4 SEM photograph of alignment

17 Photoresist develop for t-gate
- -Chlorobenzene soak
- -Developer type: MF-312
- -Immersion
- -DI water rinse

18 T-gate top metal deposition
- -Deposition method: slow evaporation

19 Photoresist removal and t-gate liftoff
- -Boiling acetone
- -Boiling isopropanol

20 Refractory metal undercut etch
- -Etch method: plasma or RIE
- -Plasma composition: CF_4
- -RSAG etch optimization t, A_{fp}, A_{fr}

21 Photoresist deposition for Nplus implant
- -Photoresist thickness: 1.5μm

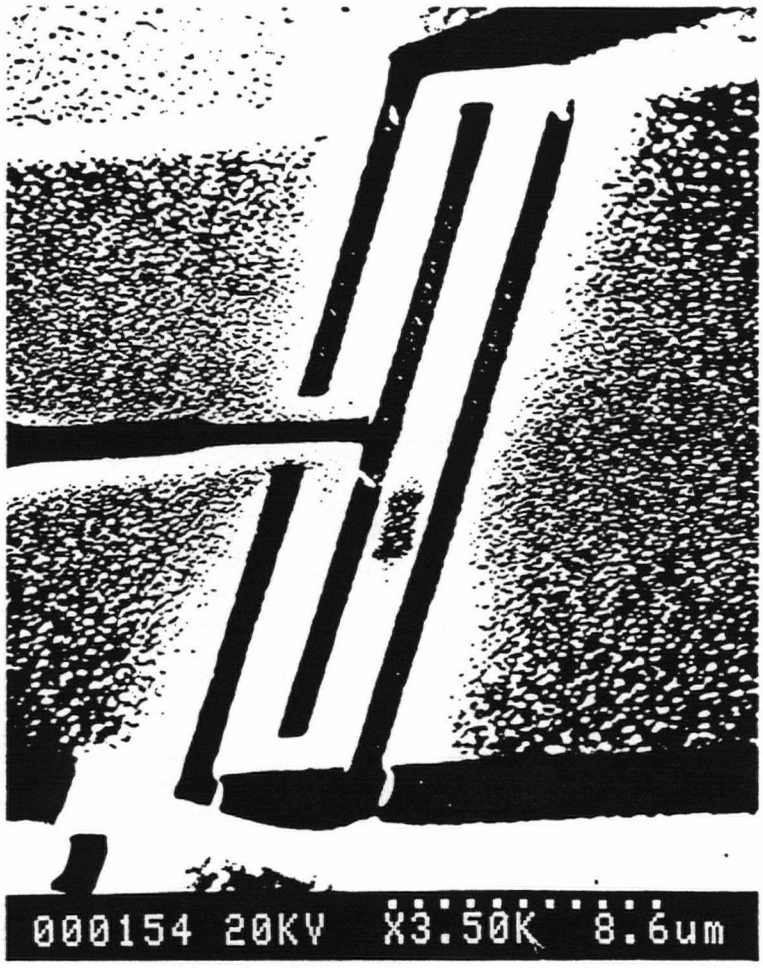


Fig. 2.5 SEM photograph of 1μm sampling gate before liftoff

22 Photoresist pattern exposure for Nplus implant
- -Plate: Nplus
- -Mask to PR method: vacuum contact

23 Photoresist develop for Nplus implant
- -Developer type: MF-316
- -Spray application
- -DI water rinse

24 Nplus implant
- -Species: Si^{29}
- -Optimization for L_G = 1μm
- -Energy: Φ_{22} keV
- -Dose:

Fig. 2.6 SEM Photograph of 1μm gate after liftoff.

Q_{22} ions/cm²
- -Wafer tilt: 11°
- -Wafer rotation: 22°
- -Optimization for L_G = 0.5μm
- -Energy: Φ_{21} keV
- -Dose: Q_{21} ions/cm²
- -Wafer tilt: 11°
- -Wafer rotation: 22°

25 Photoresist removal
- -Hot Microstrip ®™ Shipley Ltd.
- -Boiling acetone
- -Boiling isopropanol

26 T-gate top removal

-Wet etch solution: HCl
-DI water rinse
-Nitrogen blow dry

27 Silicon nitride blanket deposition
-Plasma preclean using: NH_3
-Plasma composition: He:500 sccm SiH_4:550 sccm, NH_3:37.6 sccm

28 Implant anneal
-furnace: 30 min. 800° C

29 Silicon nitride removal
-Wet etch solution: HF
-DI water rinse
-Nitrogen blow dry

30 Photoresist deposition for AuGe
-Photoresist thickness: 1μm

31 Photoresist pattern exposure for AuGe
-Plate: AuGe
-Mask to PR method: vacuum contact

32 Photoresist develop for AuGe
-Chlorobenzene soak
-Developer type MF-312
-Immersion
-DI water rinse

33 AuGe deposition
-Deposition method: evaporation

34 Photoresist removal and AuGe liftoff
-Boiling acetone
-Boiling isopropanol

35 Alloy AuGe to Nplus GaAs
-Optimization: furnace or rapid thermal alloy

36 Test process monitors enabled at this stage
Isolation leakage
TiW step resistor
AuGe ohmic meander
Transmission lines
RSAG test MESFETs
RD test diodes

37 Deposition of MIM capacitor dielectric: Si_3N_4
-Plasma preclean using: NH_3
-Deposition method: plasma
-Plasma composition: He:500 sccm SiH_4:550 sccm NH_3:37.6 sccm

38 Photoresist deposition Si_3N_4 etch
- -Photoresist thickness: 1.5μm
- -Spin on
- -Softbake

39 Photoresist pattern exposure for MIM dielectric
- -Plate: Dielectric
- -Mask to PR method: vacuum contact

40 Photoresist develop for MIM dielectric
- -Developer type: MF-316
- -Spray application
- -DI water rinse

41 Dielectric Etch to PR islands
- -Etch Solution 20% HF
- -Buffered HF
- -DI water rinse

42 Photoresist removal and liftoff
- -Boiling acetone
- -Boiling isopropanol

43 Photoresist deposition for Schottky metalization
- -Photoresist thickness: 1μm
- -Spin on
- -Softbake

44 Photoresist pattern exposure

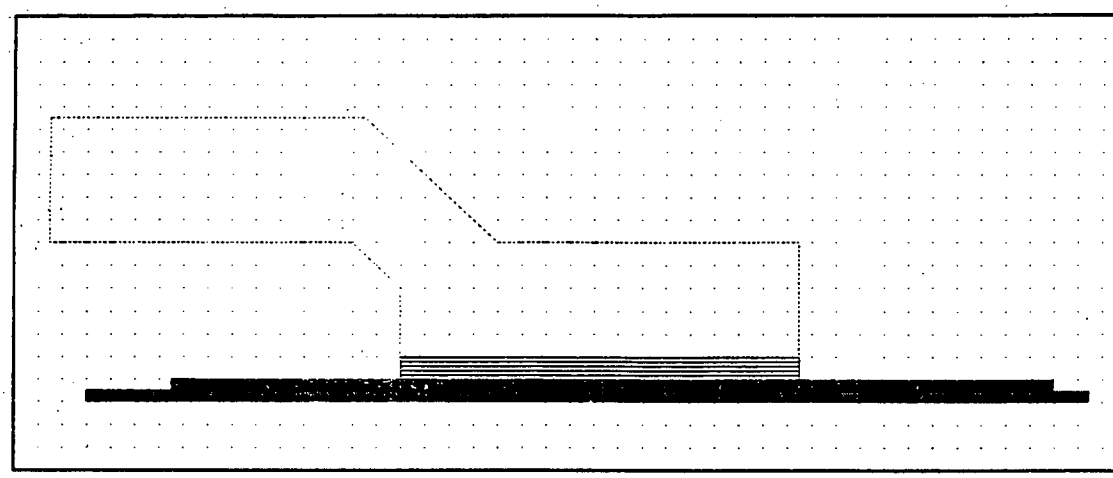


Fig. 2.7 Cross Section of MIM

-Plate: Schottky
-Mask to PR method: vacuum contact

45 Photoresist develop for Schottky metalization
-Developer type: MF-312
-Immersion
-DI water rinse

46 Schottky metalization deposition
-Deposition method: slow evaporation

47 Photoresist removal and metalization liftoff
-Boiling acetone
-Boiling isopropanol

48 Photoresist deposition for airbridge footing
-Photoresist thickness: 1.5μm

49 Photoresist pattern exposure for airbridge footing
-Plate: Schottky
-Mask to PR method: standard contact
-Exposure wavelength:
-Exposure

50 Photoresist develop for airbridge footing
-Developer type: MF-316
-Spray application
-DI water rinse

51 Deposition of airbridge footing and plate conduction metal
-Method: rf sputter, Ar atmosphere, Au 3 nm

52 Photoresist deposition for airbridge body
-Photoresist thickness: 1.5μm

53 Photoresist pattern exposure for airbridge body
-Plate: Airbridge
-Mask to PR method: standard contact

54 Photoresist develop for airbridge body
-Developer type MF-316
-Spray application
-DI water rinse

55 Gold plate airbridge body
-electrodes on exposed edge Au
-plate to few μm
-DI water rinse

56 Photoresist removal and plating metalization liftoff
-Boiling acetone
-Boiling isopropanol

57 Wafer/Slice completed

With respect to step 20, plasma etching has a vertical to lateral etch rate $v_{v1}:v_{l1}$ of about 15:1 whereas RIE is 18:1. Referring to figure 2.8 MESFET high frequency performance improvement could be achieved by gate width resistance reduction and capacitance per unit width reduction by maximizing the TiW cross section available for conduction and minimizing the Schottky contact length. As the t-top should remain firmly in place for subsequent operations d_{ft}, the final dimension of the TiW top, should be maximized with respect to d_{fb}, the final dimension of the TiW bottom.

The t-top, initially h_{ti} thick and d_{ti} wide should have $R_p+3\Delta R_p=h_{tf}$ thickness and $kd_{fb}=d_{tf}$, where k is in the order of 2, after etching to prevent 99% of the implant from reaching the channel[2.2]. Assuming the t-top material $v_{v2}:v_{l2}$ ratio is the same as TiW and the etch rates of significantly less magnitude the approximate maximum TiW thickness (h_f) can be calculated for the two mask line widths and both etch processes.

Taking as bias $B=(d_{ti}-d_{tf})/2 - d_{ft}$ and the degree of anisotropy $A_f=1-v_{l1}/v_{v1}$ as $A_f=1-B/2h_f$ after Mogab[2.7] then $d_{ft}\simeq d_m-(1-A_f)2h_f$ when etched to completion, where d_m is the mask gate width and at completion

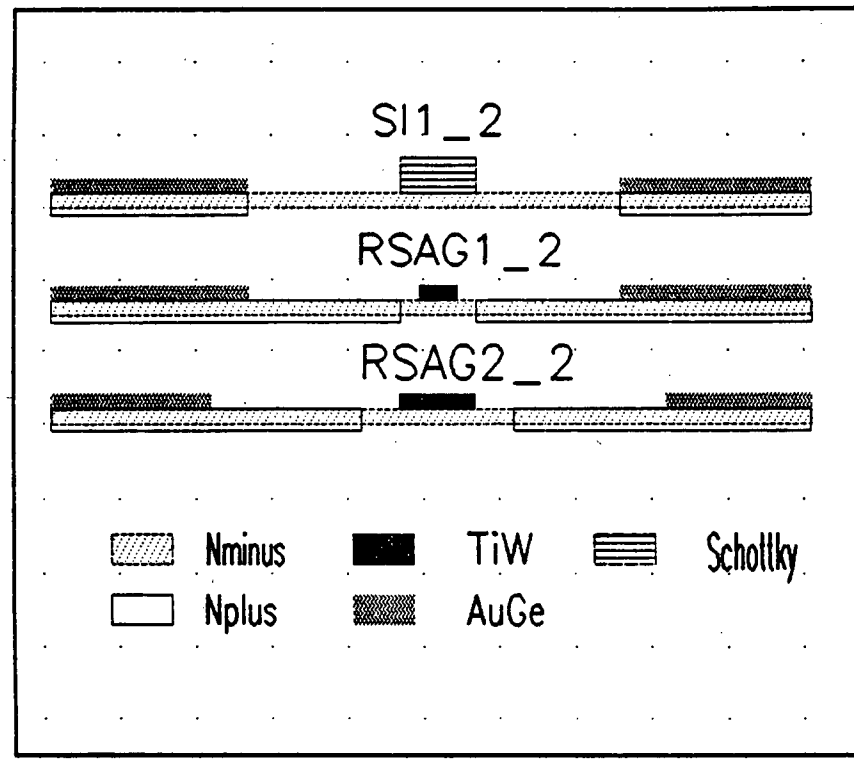


Fig. 2.8 MESFET Gate Cross Sections.

$d_{fb}=d_m$. If etching continues until the base is $½d_m$, or less, as required for RSAG $d_{ftc}\simeq d_{ft}-½d_m=½d_m-(1-A_f)2h_f$ where d_{ftc} is the critical TiW top width left to support the t-top through subsequent operations.

Choosing d_{ftc} as $0.9d_{fbc}$, where $d_{fbc}\simeq ½d_m$ corresponds to the Schottky contact width, for maximum t-top support, limits TiW thickness to $h_f\simeq 0.025d_m/[(1-A_f)]$. Neglecting t-top etching $h_f=0.025d_m v_{v1}/v_{11}$ or about 0.45μm for RIE and 0.37μm for plasma etching of a 1μm d_m t-top. For d_m=2μm a maximum 0.75μm of TiW can be used with the plasma etch and 0.9μm

with RIE. Over etching produces a shorter gate length at the risk of losing the t-tops.

3. SCHOTTKY DIODE PARAMETER EXTRACTION AND LAYOUT

The amplifier output stage diode stack requires diodes which provide voltage level shifting with reasonable transient performance, compact size and reliable fabrication. Comparing the TD and RD structures of figure

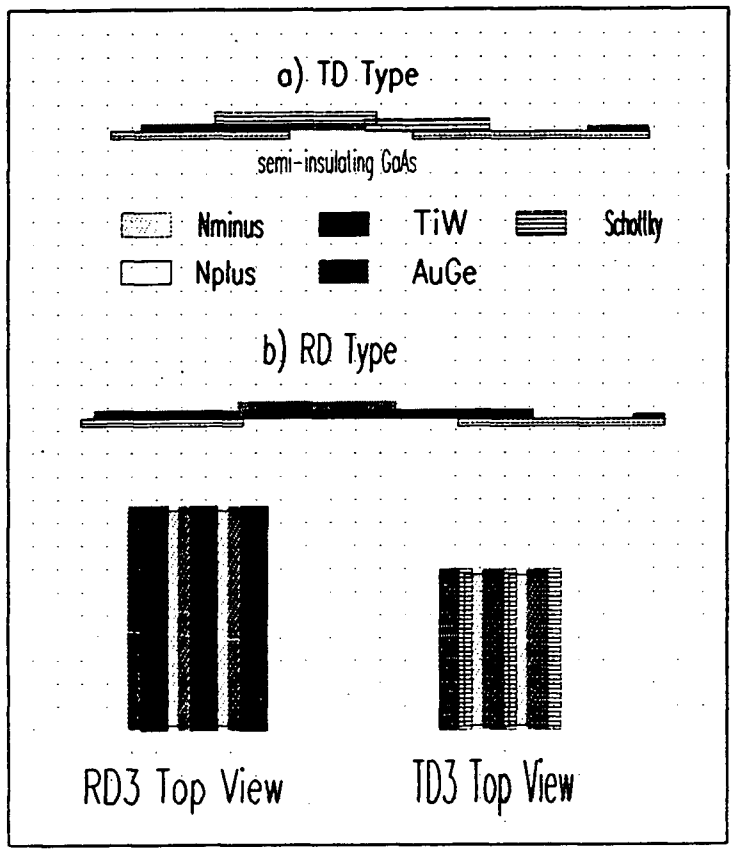


Fig. 3.1 Schottky diode cross sections.

a) TD Schottky gate metal on Nplus+Nminus
b) RD RSAG process

3.1, where the "dot grid" is 1μm for the cross sections and 10μm for the amplifier stack top views, the TD type diode used by Barta and Rode[1.2] is more compact but at the expense of increased capacitance when compared to the RD type.

In the forward biased mode of the amplifier stack the depletion width W diminishes as the applied voltage approaches V_{bi}. The major transport process is due to majority carriers tunneling from the GaAs under the depletion region over the potential barrier into the metal[3.1]. Thermionic emission theory is adequate for high mobility semiconductors and results in equation 3-1, [3.1].

$$I_S = SA^{**}T^2\exp(-q\phi_B/kT) \qquad [3\text{-}1]$$

For GaAs the Richardson constant changes from low to high field conditions at E_S as the effective electron mass changes due to scattering into the upper valley of the conduction band. The high field condition sets in at about 3kV/cm, which in consideration of the depletion width at zero bias for the N^- implant of table 2.1 holds for applied voltages above about 0.03. As such the value of A^{**} is taken as 144 $A/cm^2/K^2$ [3.1].

The Schottky diode barrier transit time(TT) for SPICE is approximated as $W_o/2v_S$, where $v_S=\mu_n E_S$ and E_S is taken as 3200 V/cm and μ_n is adjusted for doping level.

The parasitic series resistance (R_{ps}) per unit width of the diode determines the total width required for the amplifier diode stack, neglecting substrate shunt resistance. As can be seen from the cross sections in figure 3.1 $R_{ps}=R_c+R_b+R_s$, where R_c is the contact resistance, R_b is due to the gap and R_s is the average resistance under the depletion region. R_s is calculated after Kellner, Enders, Ristaw and Kniepkamp[3.2] via equation 3-2.

$$R_s \simeq \frac{L}{3W} R_{sht} \qquad [3\text{-}2]$$

Where R_{sht} is taken as the sheet resistance of the implant under the Schottky metal. R_b is taken as the sheet resistance between the ohmic and Schottky barrier contacts. R_c is calculated after Berger[3.3] for a 1μm strip as $R_c \simeq \sqrt{[R_{cv}(R_{ss})]}$ where R_{cv} is ρ_{c1}/(contact area) and R_{ss} is R_{sht2}(length)/(width).

The total series resistance due to the R_{ps} per unit width for the diode type is divided by the area factor taken as width included in the amplifier diode specifications in Appendix B.

A default value for the Schottky to ohmic metal spacing of 4μm is used for both diode types. Velocity saturation is achieved in the gap at approximately 1.2 V across the gap, or 2 V across the diode, or about 1.7 V for a 3μm gap. Both are adequate however the 4μm gap being more reliable with respect to process yield[3.4]. Only the diode stack number

and width is changed to match the diode stack to amplifier circuit requirements. Diodes were model characterized per unit width for standard gaps of 3 and 4 μm and Schottky metal length of 3 μm from alignment and capacitance considerations.

SPICE model Schottky diode trailing numbers are L_{gap}. SPICE input deck format specifies RS as R_{ps} in the following diode models.

```
.MODEL RD4 D(IS=0.31E-12, RS=3206, N=1.18, TT=0.45PS,
+ CJO=3.85E-15, VJ=0.72, EG=1.42, BV=8, IBV=1E-3)

.MODEL TD4 D(IS=0.31E-12, RS=1744, N=1.1, TT=0.59PS,
+ CJO=8.02E-15, VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
```

The cutoff frequency ($f_c=1/(2\pi R_{ps}C_j)$) is about 8.8 and 11.1 GHz for the TD and RD types, respectively, with a bias of 0 V. Equation 3-3 gives the diode I-V characteristic with the effect of R_{ps}.

$$V = IR_{ps} + (nkT/q)\ln(I/I_s + 1) \qquad [3\text{-}3]$$

Using data in Table 2.1 and referring to Figure 3.1 the parameters for a 1μm wide diode slice were constructed for the two types and used for amplifier stack layout calculations in section 6. Ideality factor n is taken as 1.18 for RSAG and 1.1 for SI. Schottky interface problems were assumed negligible for the layout calculations however can be determined from the FAT FETs and accounted for later in simulations[3.5].

4. MESFET PARAMETER EXTRACTION AND LAYOUT

The major limitations to MESFET fabrication using mask contact optical lithography are minimum linewidth and worst case alignment.

4.1 ALIGNMENT LIMITATIONS

Factors that dominate layout are interlayer alignment skew and minimum linewidth and line to gap ratio of mask lithography provided by the plate manufacturer. The line width limit of the current mask is 1μm and the line to gap ratio was fixed at 1:2 for mask production cost, fabrication and alignment reasons.

If the mask set has a tolerance of δ_I ($\pm$0.1μm) [4.1] lateral position within and $\pm$0.4μm (δ_L) between layers and the alignment can be manually made to $\pm$0.5μm (δ_A) under optimal conditions[4.2], a minimum spacing of $\delta_I+\delta_L+\delta_A$ must be allotted to avoid contact. A further margin must be allowed for lateral movement during alloying (δ_{LA}) with the total error times a safety factor (S) to account for the optimistic alignment assumption, as it is a time consuming manual operation and some misalignment may occur during the vacuum transfer phase of the exposure operation.

$$S(\delta_I+\delta_L+\delta_A+\delta_{LA}) = \text{MINIMUM SEPARATION} \qquad [4\text{-}1]$$

Taking δ_{LA} as 0.3μm and S as 1.5 gives about 2μm minimum separation between layers, or more conservatively 2.6μm with

S as 2. Minimum separation within a layer can be reduced by the compounding effect of interlayer mask skew and lateral spreading resulting in a minimum separation of less than 1μm. However previous experience at U.B.C. has shown that a 1μm intergate gap on a multiple gate RSAG MESFET causes liftoff problems in step 19 of section 2.1.1, asymmetric plasma undercutting in step 20[4.3] and is highly demanding of the current plate manufacturing process[4.1].

4.1.1 INTERLAYER ALIGNMENT MARKS

To maximize alignment accuracy a set of alignment marks shown in figure 4.1 were developed. As the mask aligner is capable of lateral movement at a magnification of 160X corresponding to a mask to wafer gap of 20μm, then an alignment checking operation with the mask and wafer at a 3 μm gap or under vacuum assisted direct contact, three levels of alignment mark are necessary. The first mark must allow the operator to align wafer to mask orientation easily, for which a simple stacked structure will suffice(corner brackets in fig. 4.1). The second mark should allow maximum alignment accuracy at 160X magnification at which the smallest visible feature is 1.5μm in a field of approximately 200 by 200μm. The proposed 0.5μm alignment accuracy of the process can only be obtained under these conditions by taking advantage of the symmetry detection capability of the operator by balancing light and dark

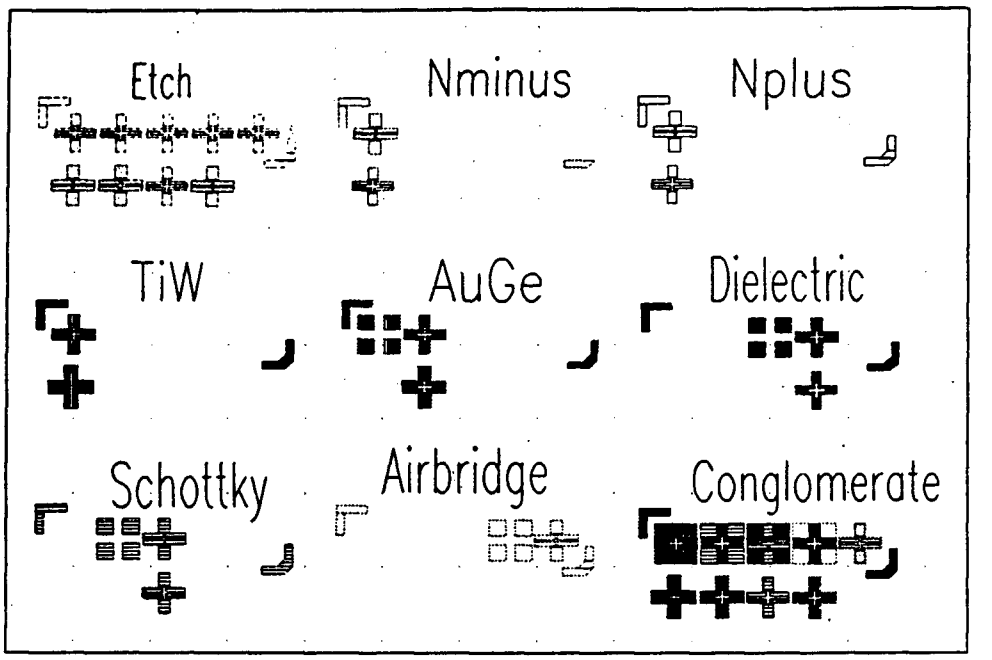


Fig. 4.1 Alignment Marks

fields[4.2] of greater than 1.5μm. As such 3 and 4μm were taken as a 2nd level gaps.

The third level mark should be able to take advantage of the 320X objective capability of detecting a 0.75μm minimum feature[4.2] to check the second mark alignment under direct contact through a 1 to 2μm photoresist layer with a depth of field of 3μm and a frame of less than 100μm.The inner cross has a 1 or 2μm gap to compensate the possible interference due to the photoresist, resulting in the multiple patterns for each layer.

In order to accommodate the demands of aligning to the original alignment etch, thus to avoid any error accumulation between layers, and check metal to metal alignment, separate alignment marks were used, including metal overlays of previous metal depositions. The fact that with positive photoresist the exposed area through the clear portion of the mask is subsequently developed away means that to obtain the light field symmetry for second level alignment the clear area must surround the periphery of the etch line by 4μm. Third level alignment can be accomplished by a internal etch periphery with a dark mask field 1μm inside it.

4.2 RSAG AND SELECTIVE IMPLANT PROCESS PARAMETER DIFFERENCES

As is apparent from figure 4.2, RSAG devices made with the same level of lithography as SI devices should have superior performance due to reduced gate length and source/drain parasitic resistance. Equally apparent though is the fact that RSAG process gate resistance is much higher leading to a loss of some of the gained benefit with respect to the SI process.

4.2.1 SOURCE AND DRAIN RESISTANCE

Source and drain resistances are minimized to minimize the channel transit time(τ) and increase I_{DS} at a given V_{DS}. Referring to Fig. 4.2 it can be seen that R_S and R_D have several series contributions. The

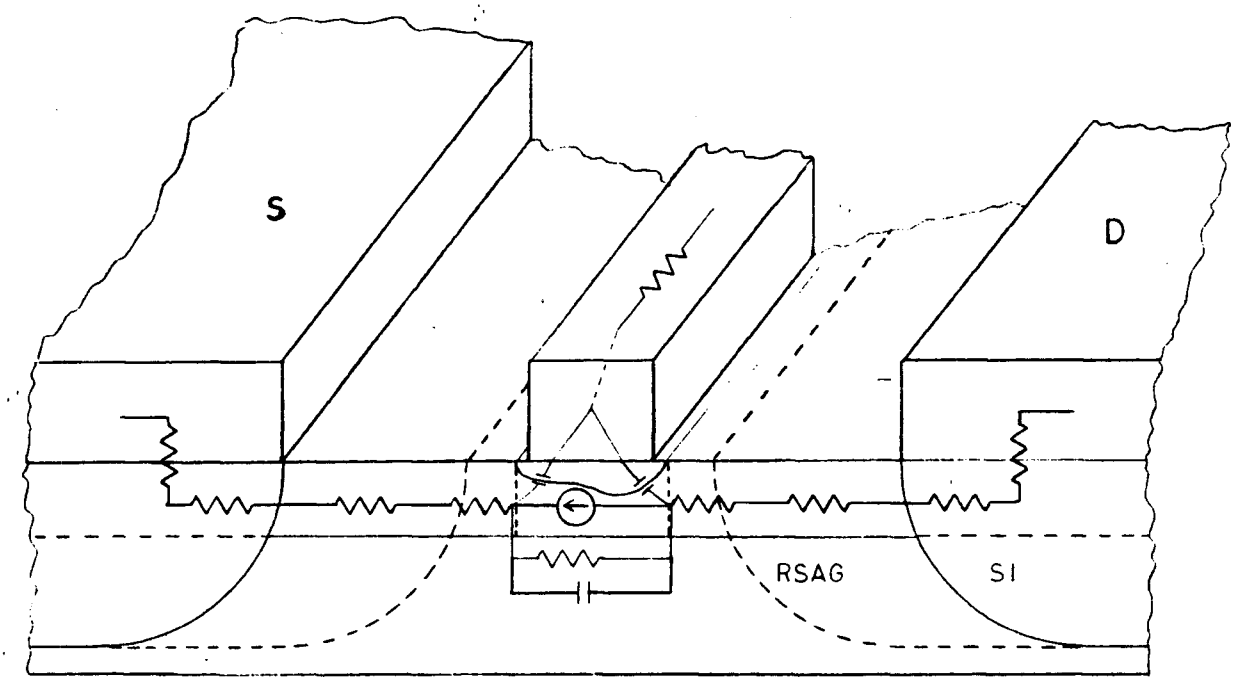


Fig. 4.2 Cross Section of MESFETs

trailing model numbers(ie. RSAG1_2) correspond to mask L_G and L_{gap}. The gap resistance R_{Sgap} or R_{Dgap} is calculated by using the applicable R_{sheet} times the number of squares in the gap, allowing for lateral diffusion during anneal in the RSAG case. This does not allow for alignment variations.

Ohmic contact resistance is calculated after Berger[3.3]. For the purposes of compaction and layout regularity for a large number of circuit variations a

standard contact length of 20μm was selected, however some layouts are adjusted slightly.

4.2.2 GATE PHASE SHIFT

A "well designed FET", with respect to gate series resistance, has gate metal evaporation onto thick double layer photoresist for lithographic accuracy with reliable liftoff of unwanted metal from a thick deposition[2.4]. Typical layers are 300 nm of TiW topped by 0.7 μm Au producing a "mushroom gate" profile. The thick gold layer is necessary to decrease R_g per unit width at high frequency, minimizing gain degradation due to transmission line and skin effects[4.4-4.8].

The current gain of a MESFET depends on a uniform voltage acting along the channel(Z axis). If a phase shift of the control signal occurs along the width of the gate, the source to drain flow of electrons through the channel varies with Z. This effect is a result of phase shift due to the transmission line character of the gate.

A second metal layer for the TiW RSAG gate has been attempted by Sadler[2.2] to make up for the discrepancy apparent in table 4.1, leaving Al, Ni, Au, and Pt t-gate tops in place during annealing. The result was "drastic interdiffusion and alloying ... between the top metal and the GaAs". With this in mind we considered post anneal processing as the only viable refractory gate

stripe resistance reduction strategy.

Metal	Bulk	Thin Film Estimate	Units
Al	2.56	5.12	μΩ-cm
Au	2.44	4.88	μΩ-cm
Ti	41.00	82.00	μΩ-cm
W	5.60	11.20	μΩ-cm
$Ti_{0.3}W_{0.7}$	16.22	74.61*	μΩ-cm

Table 4.1 Thin film resistivity.(* from [2.2])

A post anneal gate gold plating process was conjectured. An extra fabrication step would be added where a temporary interconnect web would provide plating current to the gates. This would cause electrolytic plating action at exposed areas, but would require precisely aligned mask windows to prevent unwanted plating. After plating the PR would be removed and a circuit shielding mask used to etch the plating current distribution grid.

The main problem with this plan is plating mask alignment and minimum line width. Alignment skew of 1.6μm is expected, and the mask minimum line width of 1μm is inadequate for 0.5μm RSAG gate lengths.

It has been demonstrated by Wolf[4.3] that the effect of gate metalization resistance is proportional to b^2, where b is the gate width. As such the design philosophy of this project has been to maximize TiW thickness and the gate width with respect to the maximum

frequency or pulse response required of the MESFET.

Separate considerations are included for the switch of section 5 and the amplifier of section 6.

4.3 MESFET CAPACITANCE

Capacitance due to the depletion layer(C_{GS} and C_{GD} varies with the specific two dimensional geometry of the depletion region, which is dependent on V_{GS} and V_{DS}. C_{DS} is considered to be relatively independent of the depletion region and as such is treated as a constant. The SPICE 2[4.4] MESFET model proposed by Curtice[4.5] and realized by Sussman-Fort[4.6] models C_{GS} as variable and treats C_{GD} as constant. Several other models have been published some of which are included in the references[4.7-4.11]. In the course of modeling ICDL and other logics(partial inclusion in appendix A) with the SPICE 2 MESFET model Abdel-Moteleb, Rutherford and Young[4.17] included a variable C_{GD} for some of the simulation runs.

The MESFET circuit model with an added shunt resistor, due to substrate conduction, appears in figure 4.3. A more accurate capacitance model has been proposed by Golio, Hauser and Blakey[4.13] of which the C_{GD} portion has been included in a version of SPICE 2 (re: appendix B).

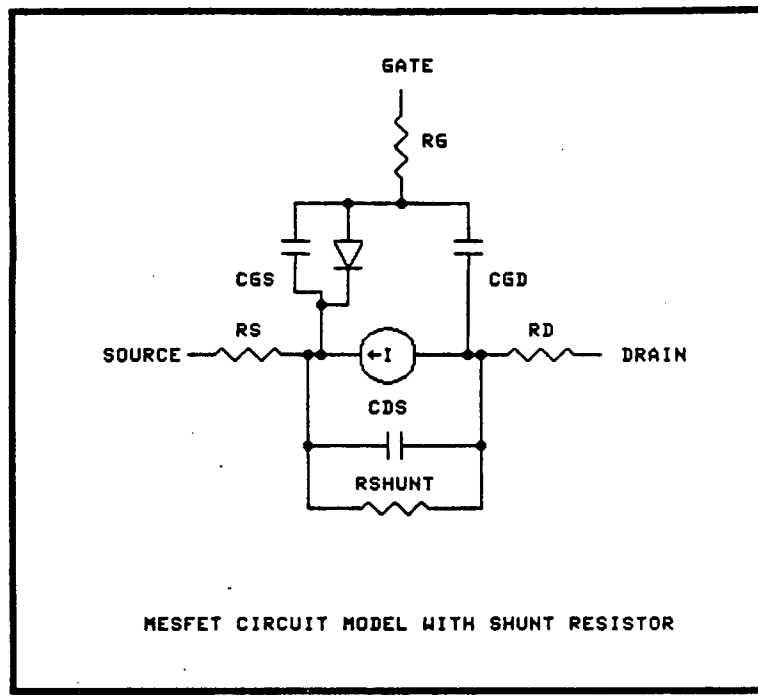


Fig. 4.3 MESFET circuit model

4.4 MESFET 1μM SLICE PARAMETERS

From the process definition and parameter estimation procedures nine MESFET SPICE models are maintained for circuit evaluation. Figure 4.4 a) represents a typical industry standard MESFET configuration which is used as a process benchmark for comparison of our variations to each other and MESFETs currently being produced by several manufacturers. Figure 4.4 b) has a 1μm dot grid superimposed on the magnified layout of the gate connect, as compared to the 100μm dot grid of figure 4.4 a). DC characteristics are accumulated from the 100μm test MESFET or 236 π-gate array of figure 1.2 with the use of a semiconductor parameter analyzer.

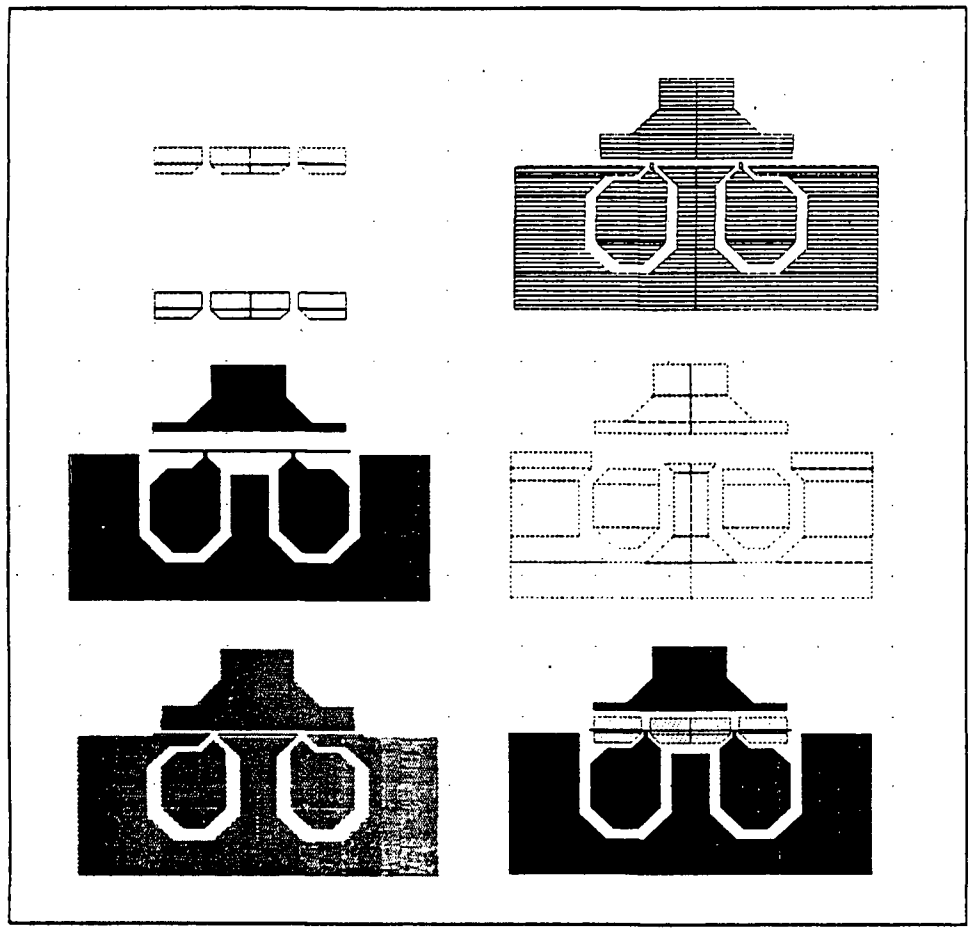


Fig. 4.4 a) π-Gate Layout

The simulated I-V characteristics are displayed for 100μm widths in figures 4.5 to 4.7 for the nine variations.

In the SPICE models below all width dependent constants are per μm. SPICE GGS0 and CGD are calculated at V_{GS} and V_{DS} = 0 V from the normal space charge equation 4-2. Comparing the measured results of Van Tuyl and Liechti[4.14]

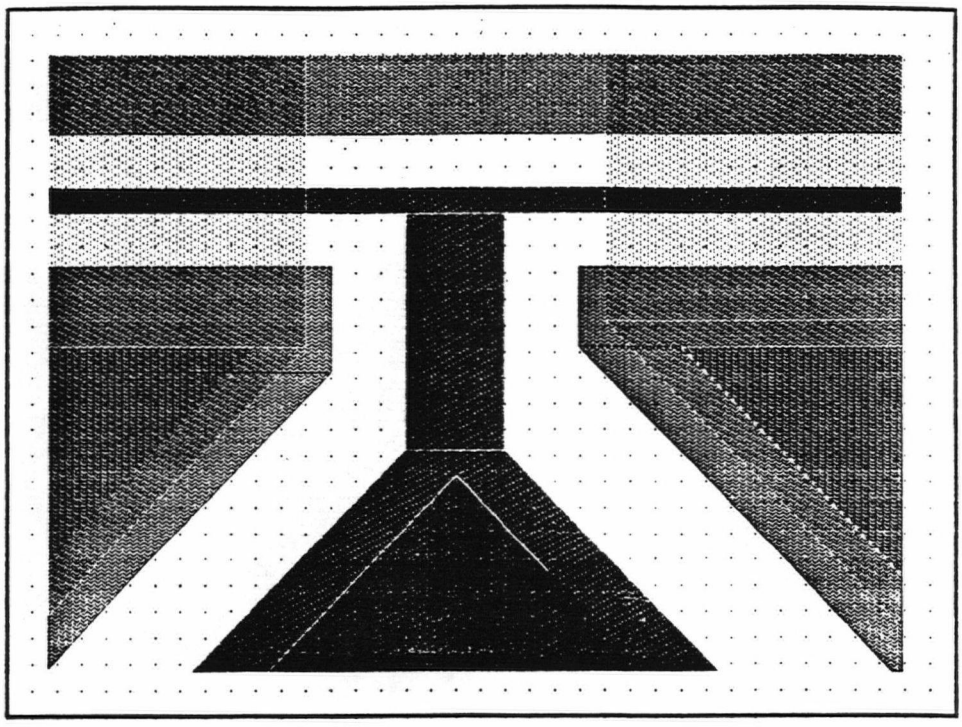


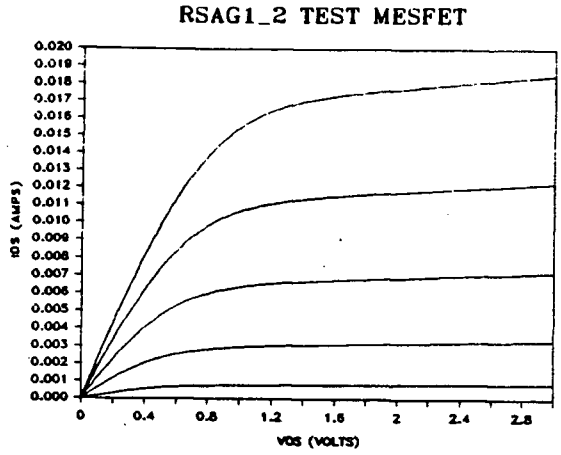
Fig. 4.4 b) π-Gate Magnified

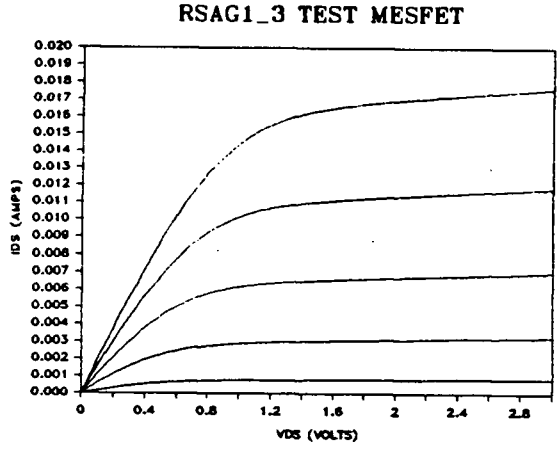
C_{SC} is approximately equal to C_{GS} until the MESFET is biased near V_{GS}=0.5 V where the measured C_{GS} is about $0.68C_{SC}$. From symmetry CGD is equal to CGS under these conditions. The SPICE simulation then proceeds to modify the initial values according to equations 4-3[4.5] and 4-4[4.13].

$$C_{SC}=LZ[q\epsilon N(x)\ /2(V_{bi}\ -\ V_{gs}\ -\ V_{th})]^{1/2} \qquad [4\text{-}2]$$

$$C_{GS}(V_{gs})=\ CGS0/[\,1-V_{gs}/V_{bi}\,]^{1/2} \qquad [4\text{-}3]$$

$$C_{GD}(V_{gs},V_{ds})=$$
$$C_{GD0}/[\,1-(\lambda_{GD1}V_{gs}-V_{ds})/(\lambda_{GD1}\phi_G)\,](1-\lambda_{GD2}V_{gs}) \qquad [4\text{-}4]$$





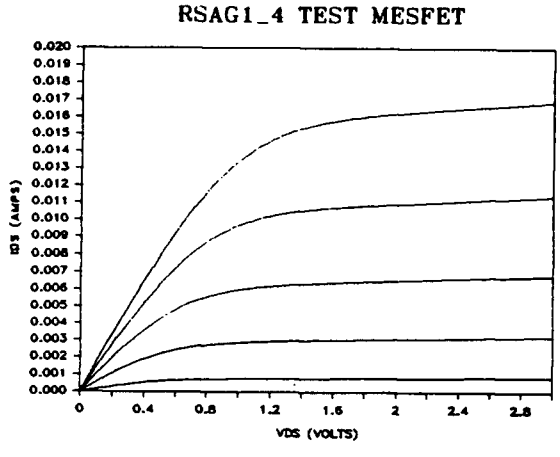
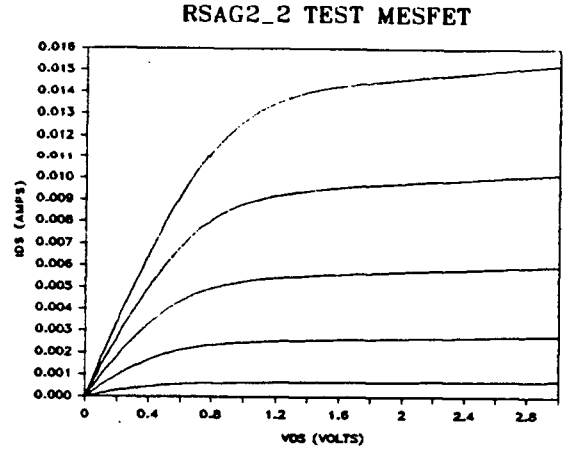
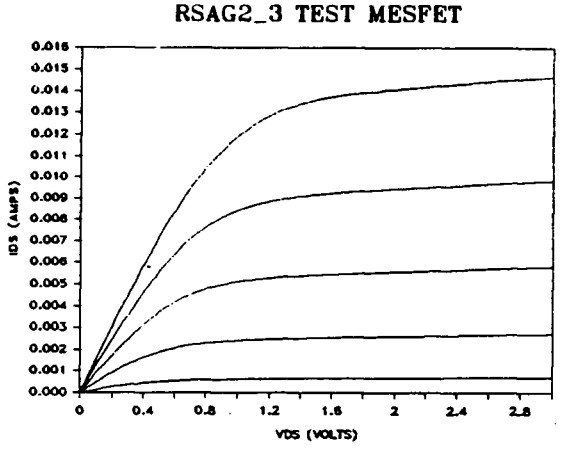


Fig. 4.5 RSAG 0.5μm I-V characteristics





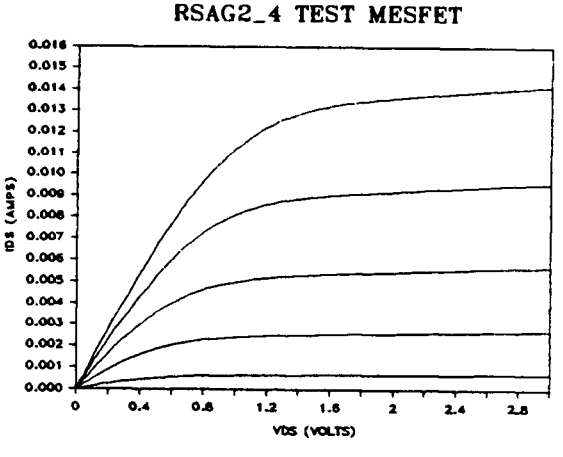
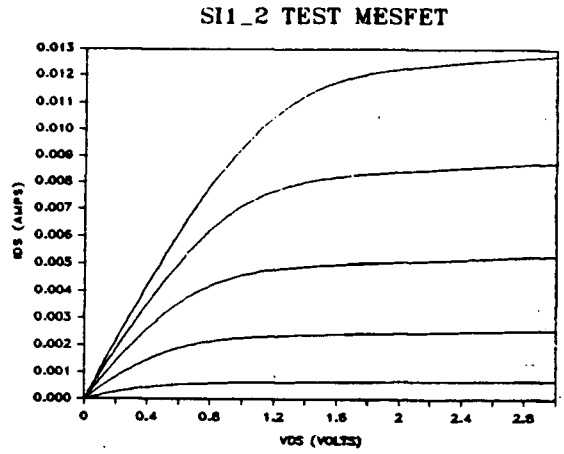
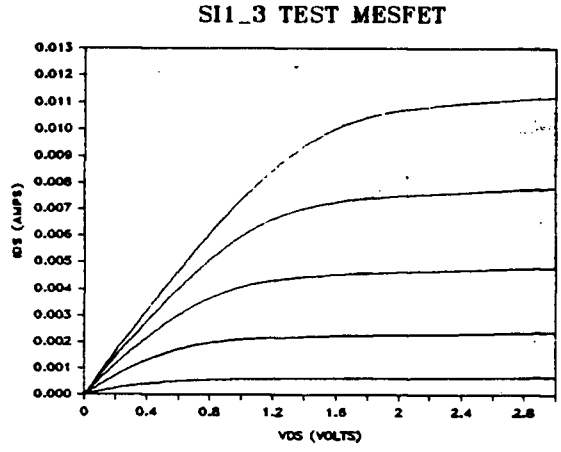


Fig. 4.6 RSAG 1μm I-V characteristics





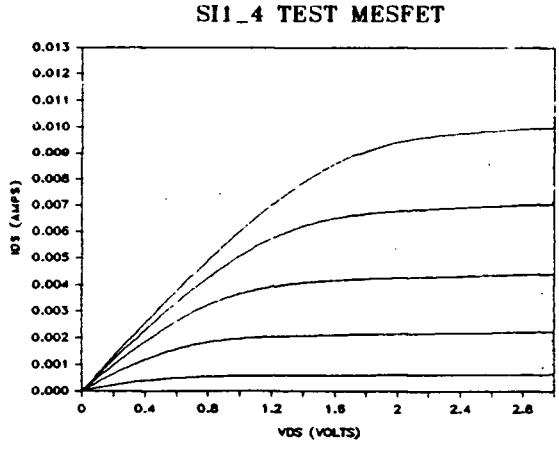


Fig. 4.7 SI 1μm I-V characteristics

The constants for equation 4-4 are listed in Appendix C as part of the GASFET subroutine source code. I_{ds} is empirically fitted with equation [4-5] after Curtice[4.5].

$$I_{ds}=\beta(V_{gs}+V_T)^2\cdot(1+\lambda V_{ds})\tanh(\alpha V_{ds}) \qquad [4\text{-}5]$$

Where λ is the channel length modulation factor and α is the hyperbolic tangent function parameter. α is used to fit the linear region and λ the slope of the saturation region.

The transconductance parameter $\beta=I_P/V_P^2$ and V_T are generally determined by plotting $\sqrt{I_{DS}}$ vs. V_{GS} and accounting for R_S and R_D. If devices are not available β can be approximated theoretically after Chen and Shur[4.15].

$$\beta=[2\epsilon_{GaAs}\upsilon_s W]/[A(V_P+3E_m L_1)] \qquad [4\text{-}6]$$

$$\text{where } A=[2\epsilon_{GaAs}V_P]/[qQ_a] \qquad [4\text{-}7]$$

$$\text{and } L_1=L-\frac{2A}{\pi}\sinh^{-1}\{[\pi K_d(V_{ds}-V_{is})]/[2AE_s]\} \qquad [4\text{-}8]$$

and the voltage drop across the channel at saturation is:

$$V_{is}=[E_s L(V_{gs}-V_T)]/[E_s L+V_{gs}-V_T] \qquad [4\text{-}9]$$

K_d is approximately 1 for self aligned gates and $K_d=\Delta V/(V_{ds}-V_{is})$ for SI gates where ΔV is the "voltage drop across part of the high field domain under the gate". When

$V_{gs} = V_{bi}$ the maximum $V_{is} = (E_sLV_{PO}/(E_sL+V_{PO})$ and increase in I_{ds} due to channel shortening is negligible for $V_{ds}>V_{is}+2$ volts at this point. β can be considered independent[4.10] of $V_{ds} >> V_{is}+2$ at $V_{gs}=V_{bi}$. Q_a is taken as the implant activation times the N^- dose for the purposes of initial approximation.

The following models are the result of layout and process calculations.

```
.MODEL RSAG1_2 GASFET(VTO=-2, VBI=1.23, RG=4.97, ALPHA=2.3,
+ BETA=3.1E-5, LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF,
+ CDS=0.0791FF, IS=2.07E-15, RD=1170, RS=1170,
+ TAU=0.71PS)

.MODEL RSAG1_3 GASFET(VTO=-2, VBI=1.23, RG=4.97, ALPHA=2.3,
+ BETA=3.1E-5, LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF,
+ CDS=0.0738FF, IS=2.07E-15, RD=1490, RS=1490,
+ TAU=0.71PS)

.MODEL RSAG1_4 GASFET(VTO=-2, VBI=1.23, RG=4.97, ALPHA=2.3,
+ BETA=3.1E-5, LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF,
+ CDS=0.0714FF, IS=2.07E-15, RD=1810, RS=1810,
+ TAU=0.71PS)

.MODEL RSAG2_2 GASFET(VTO=-2, VBI=1.23, RG=1.49, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.096FF, IS=4.13E-15, RD=1555, RS=1555, TAU=2.86PS)

.MODEL RSAG2_3 GASFET(VTO=-2, VBI=1.23, RG=1.49, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.0947FF, IS=4.13E-15, RD=1875, RS=1875, TAU=2.86PS)

.MODEL RSAG2_4 GASFET(VTO=-2, VBI=1.23, RG=1.49, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.0791FF, IS=4.13E-15, RD=2195, RS=2195, TAU=2.86PS)

.MODEL SI1_2 GASFET(VTO=-2, VBI=1.23, RG=0.13, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.096FF, IS=4.13E-15, RD=3228, RS=3228, TAU=2.86PS)

.MODEL SI1_3 GASFET(VTO=-2, VBI=1.23, RG=0.13, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.0847FF, IS=4.13E-15, RD=4770, RS=4770, TAU=2.86PS)

.MODEL SI1_4 GASFET(VTO=-2, VBI=1.23, RG=0.13, ALPHA=2.3,
+ BETA=2.61E-5, LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF,
+ CDS=0.0791FF, IS=4.13E-15, RD=6312, RS=6312,
```

+ TAU=2.86PS)

V_{bi} is taken as 0.5 V + ϕ_{Bn} after Curtice[4.5] allowing for a voltage drop across r_i in the conduction channel under the gate.

The transit time under the gate TAU is used in the model to include the delayed effect of a change in V_{gs} on I_{ds}. In the Curtice[4.5] model it is a constant. TAU is taken at V_{ds} = 1 V, using a conservative average low field mobility of 3500 $cm^2/V\text{-}s$, across the effective channel length. This value is then modified during program execution in a prototype SPICE version by dividing TAU by V_{ds}+k, where k is to prevent division by zero, to produce an effective transit time.

5. SWITCH CONSIDERATIONS AND LAYOUT

Figure 5.1 a) is the layout for a triple gate RSAG1_2 switch with a 100μm dot grid and figure 5.1 b) is a magnified view of the gate region. Assuming the existence of a ground plane a distance d under the metalization, circuit

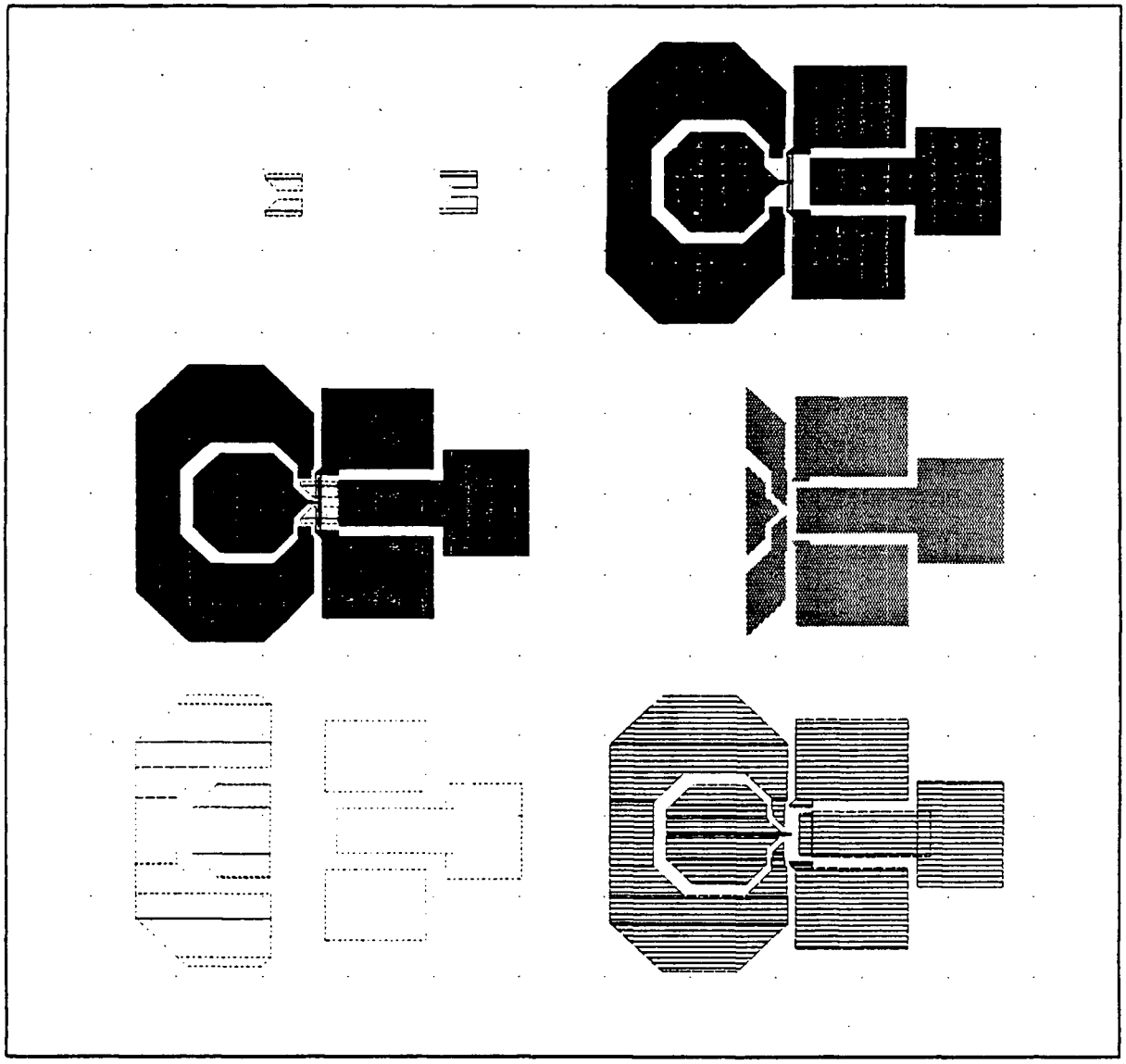


Fig. 5.1 a) Triple Gate Switch Layout

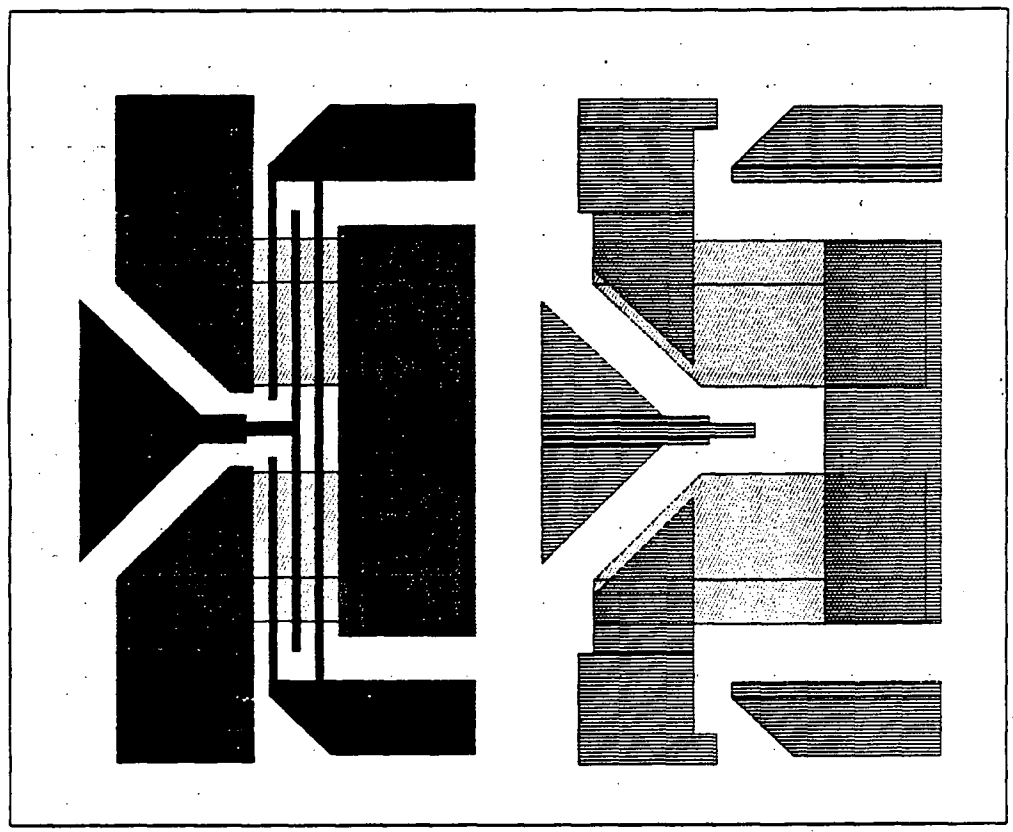


Fig. 5.1 b) Magnified Triple Gate Switch

parasitics can be calculated after Van Tuyl, Liechti, Lee and Gowen[5.1].

Switch sampling performance involves the combined effect of pulse edge propagation and reflection in the gate and channel reaction.

In a pulse modulated short channel MESFET transient behavior can be simulated by a two dimensional mesh model in fractions of a picosecond such as performed by Faricelli,

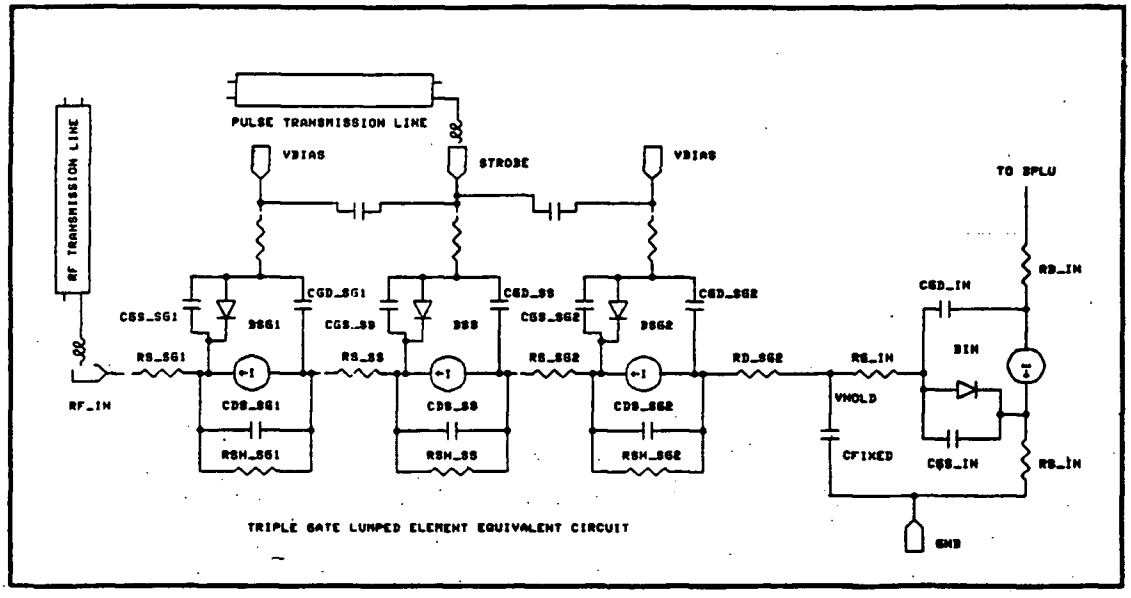


Fig. 5.2 Triple Gate Switch Slice Equivalent Circuit

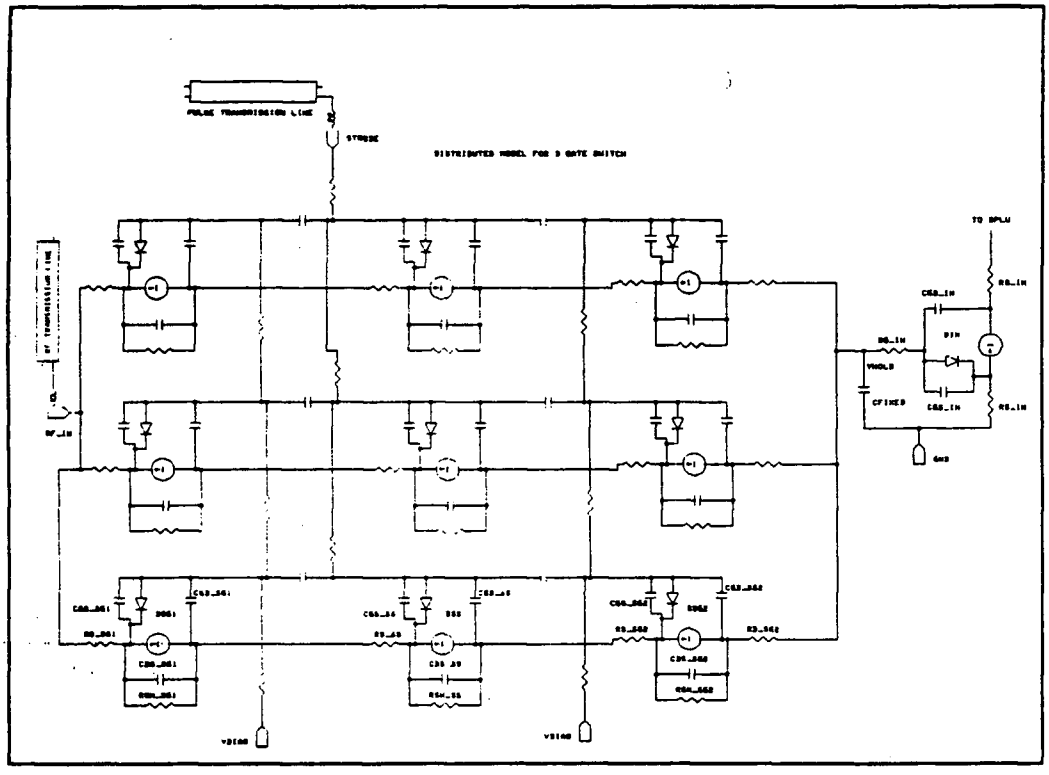


Fig. 5.3 Triple Gate Switch Distributed Model

Frey and Krusius[5.2] with respect to digital logic.

5.1 THE SAMPLING CYCLE

In a sampling cycle the switch is initially held at or below pinchoff by the sampling pulse transmission line bias. The rising edge of the pulse ramps from V_T to $V_{bi}-\Delta V$, where ΔV is to prevent forward conduction, in t_r. The voltage ramp propagates down the gate transmission line and reflects off the unterminated end.

In the channel the positive gate pulse causes fields to withdraw from the active layer, drawing majority carriers from the source and drain towards the gate, increasing C_{GS} and C_{GD}. The transverse field profile due to V_{DS} in combination with the altering depletion boundary accelerates mobile charge in the channel from source to drain moving charge from or to the hold node depending on the magnitude of V_{hold} vs. V_{in}.

After 25ps the down ramp propagates down and reflects from the unterminated gate end causing fields to penetrate the active layer. The majority carriers move down the potential gradient to the source and drain, decreasing C_{GS} and C_{GD} and reversing the source current of the previous state. The rapid displacement of charge from the channel to the source and drain areas likely causes most of the observed voltage change which is referred to as "sample strobe blow-by" by Barta and Rode[1.2].

Ideally the magnitude of the "strobe feedthrough" to the output of the sample and hold would be negligible. The bandwidth of the amplifier should be maximized for minimization of the number of ISAB units[1.1]. Thus the strobe feedthrough should be minimized at the switch.

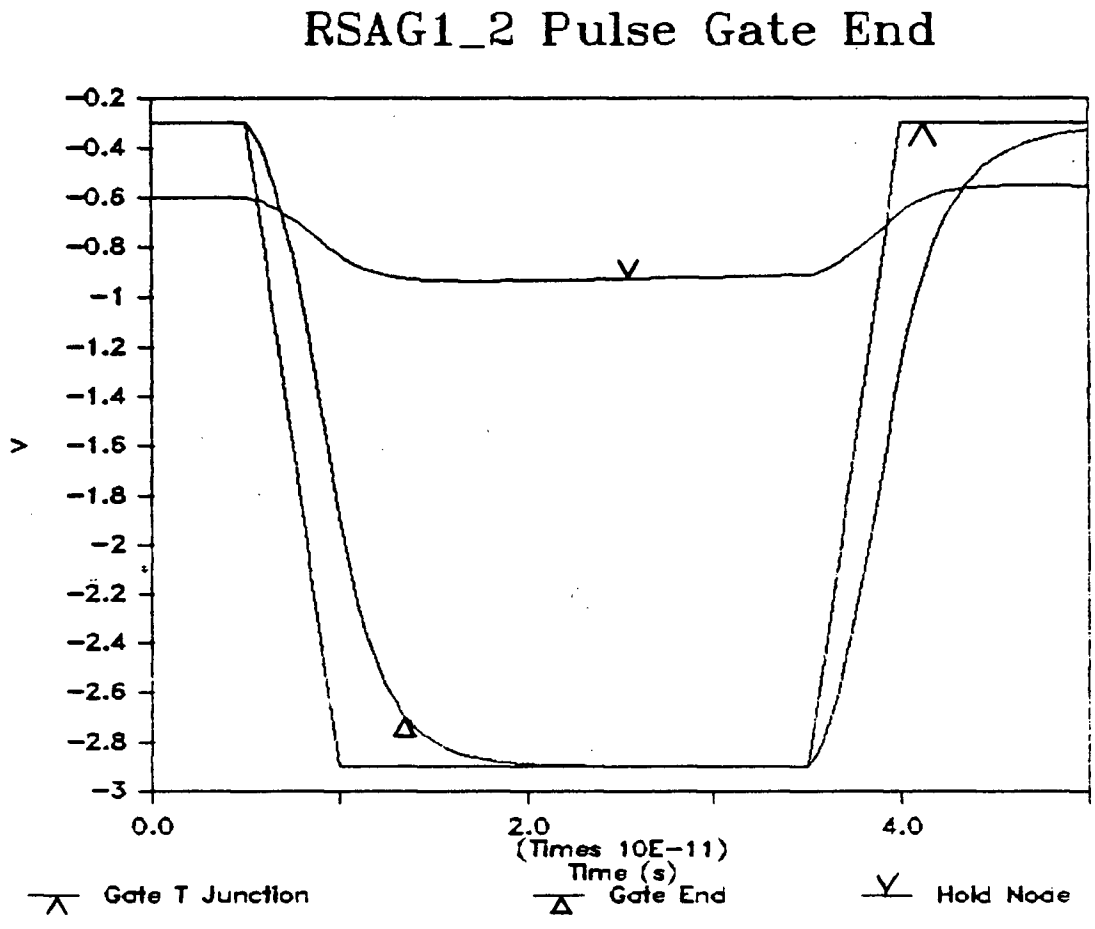


Fig. 5.4 Single Gate Distributed Simulation

5.2 GUARD AND SAMPLING GATE BIASING CONSIDERATIONS

The operation of the switch with respect to sample and hold is such that, when the switch is on, V_{DS} tends to zero while bringing the hold capacitance to a potential near the source potential. When the switch is off the source is free to follow excursions which do not inadvertently bias the switch on with the charged hold capacitance supplying a voltage to the amplifier input MESFET. The hold charge leakage paths include MIM or ID capacitor leakage, switch shunt leakage, amplifier input leakage and substrate shunt leakage.

The amplifier input bias should be such that the output bias is very close so as to enable cascade operation for several stages. Amplifier input bias is in the order of $0.3V_T$, varying with the specific amplifier component characteristics. Amplifier gain and output swing limit the input swing such that V_{hold} should vary by about 200mV about the symmetry bias point. The guard gate bias should be such that charging current is maximized without causing gate forward conduction, about 500 mV above the most negative input signal excursion.

5.3 HOLD CAPACITANCE CONSIDERATIONS

The optimum magnitude of the hold capacitance is determined by the rate of charging for the aperture available. The guideline aperture is the highest priority aspect of the design. Amplifier input capacitance is mainly C_{gs} of the input MESFET plus a small parasitic contribution and as such

is a function of V_{gs}. Reduction of potential distortion can be accomplished by increasing the ratio of fixed capacitance to variable capacitance. Fixed capacitance is from two sources, parasitic or layout dependent and MIM or interdigitated structures. The estimated node capacitance for the Barta and Rode ISAB is 0.3pF of which half is MIM and the other a combination of parasitic and depletion layer. The amplifier input width is 50μm implying C_{SC0} of about 60fF combined with the node side guard gate width of 100μm amounting to $C_{SC0} \simeq 120fF$, with the node at zero volts.

Parasitic capacitance originates with the layout separations, substrate thickness and dielectric constant. If the ISAB is mounted on a sheet of conducting epoxy at ground potential the surface metalizations form a MIM capacitor. Substrate thickness is about 450μm leading to an approximate capacitance per unit area of $\epsilon_{GaAs}/d \simeq 25,700fF/cm^2$. For a 100$\mu m^2$ pad this amounts to about 2.6fF. This would increase for a thinned substrate design incorporating the entire DRFM acquisition unit including microstrip delay line.

The rate of charging for a single gate switch at V_{DS} is determined by switch characteristics and V_{GS}. A multiple gate switch has a lower charging rate due to the added guard channels in series.

Barta and Rode[1.2] claim that in a three gate switch "the outside gates serve a shielding function by minimizing the effects of sample strobe blow-by reflected back into the input source and coupled onto the output signal."

Comparative lumped element modeling of this configuration with equivalent input time constant single and dual gate configurations is shown in section 7 simulations. The switch slice parameters are accumulated in table 5.1.

Figure 5.2 is the equivalent circuit of a triple gate switch slice connected to the amplifier input FET with a fixed capacitance(C_f). The distributed model of the switch incorporates the switch as a set of n slice elements connected to simulate the layout of figure 5.1 as demonstrated in figure 5.3 for n=3.

MESFET ID RSAG	CGSO (1) fF	Rc (2) ohms	Rs (3) ohms	Rd (4) ohms	TAU (5) psec
G1 1 1 2	0.59	144.2	1169.7	705.5	0.71
S 1 1 2	0.59	0.0	705.5	705.5	0.71
G2 1 1 2	0.59	144.2	705.5	1169.7	0.71
G1 1 2 2	1.17	144.2	1555.2	1091.0	2.86
S 1 2 2	1.17	0.0	1091.0	1091.0	2.86
G2 1 2 2	1.17	144.2	1091.0	1555.2	2.86
Ti/Au Selective Implant MESFETs					
G1 1 1 2	1.17	144.2	3228.2	1542.0	2.86
S 1 1 2	1.17	0.0	1542.0	1542.0	2.86
G2 1 1 2	1.17	144.2	1542.0	3228.2	2.86

Notes

1 Gate to Source Capacitance at Vgs=0 V

2 Contact Resistance

3 Source resistance

4 Drain resistance

5 Effective Channel Length/Saturation Velocity

Model	R1_2G1	R1_2S	R1_2G2	R2_2G1	R2_2S	R2_2G2	S1_2G1	S1_2S	S1_2G2	UNITS
Lg	0.5	0.5	0.5	1	1	1	1	1	1	um
S/D Gap	2	2	2	2	2	2	2	2	2	um
VTO	-2	-2	-2	-2	-2	-2	-2	-2	-2	V
VBI	1.23	1.23	1.23	1.23	1.23	1.23	1.23	1.23	1.23	V
RG	4.97	4.97	4.97	1.49	1.49	1.49	0.13	0.128	0.128	ohms
ALPHA	2.3	2.3	2.3	2.3	2.3	2.3	2.3	2.3	2.3	
BETA	3.055E-05	3.055E-05	3.055E-05	2.615E-05	2.615E-05	2.615E-05	2.615E-05	2.615E-05	2.615E-05	A/V^2
LAMBDA	0.055	0.055	0.055	0.055	0.055	0.055	0.055	0.055	0.055	
CGSO	0.586	0.586	0.586	1.173	1.173	1.173	1.190	1.190	1.190	fF
CGD	0.586	0.586	0.586	1.173	1.173	1.173	1.190	1.190	1.190	fF
CDS	0.0791	0.0738	0.0714	0.096	0.0847	0.0791	0.096	0.0847	0.0791	fF
IS	2.07E-05	2.07E-05	2.07E-05	4.13E-05	4.13E-05	4.13E-05	4.13E-05	4.13E-05	4.13E-05	A
RS	1169.7	705.5	705.5	1555.2	1091.0	1091.0	3228.2	1542.0	1542.0	ohms
RD	705.5	705.5	1169.7	1091.0	1091.0	1555.2	1542.0	1542.0	3228.2	ohms
TAU	0.71	0.71	0.71	2.86	2.86	2.86	2.86	2.86	2.86	ps

Table 5.1 MESFET Parameters for sampling switches.

6. AMPLIFIER LAYOUT

The amplifier equivalent circuit of figure 6.1 is realized with the layout of figure 6.2. The relative feedback MESFET width was taken as 25% of BPU after Van Tuyl [2.4] giving about 3dB gain. In the layout BPU is the MESFET most affected by gate metalization resistance, as it is not driven at both ends. For the SPICE transient simulations R_G is taken as 1/3 the end to end metalization resistance after Wolf[4.3] for an end driven gate and 1/2 of that for both ends driven.

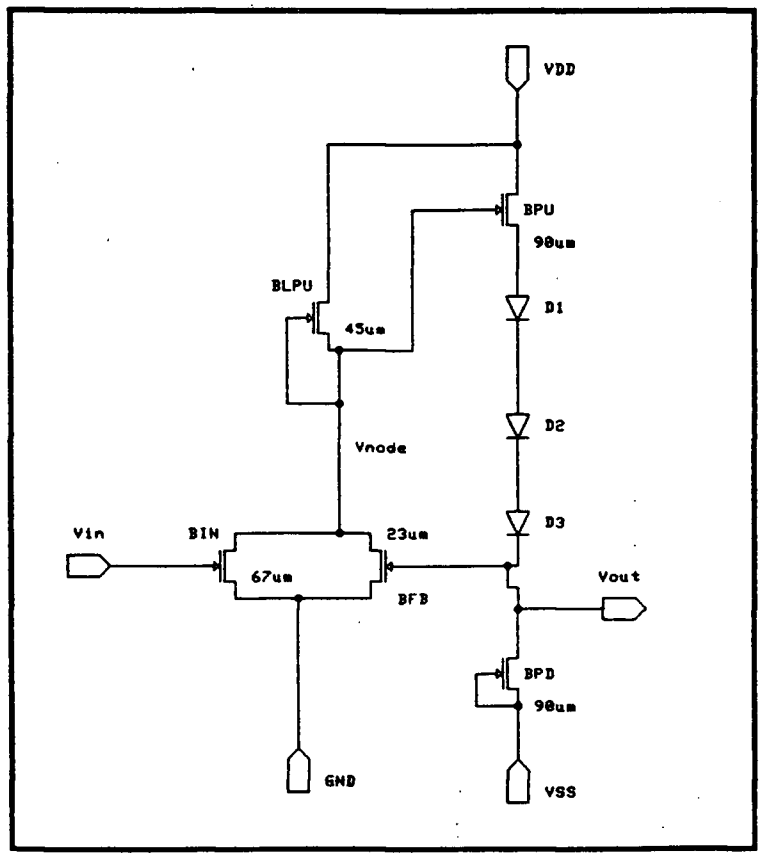


Fig. 6.1 Amplifier Equivalent Circuit.

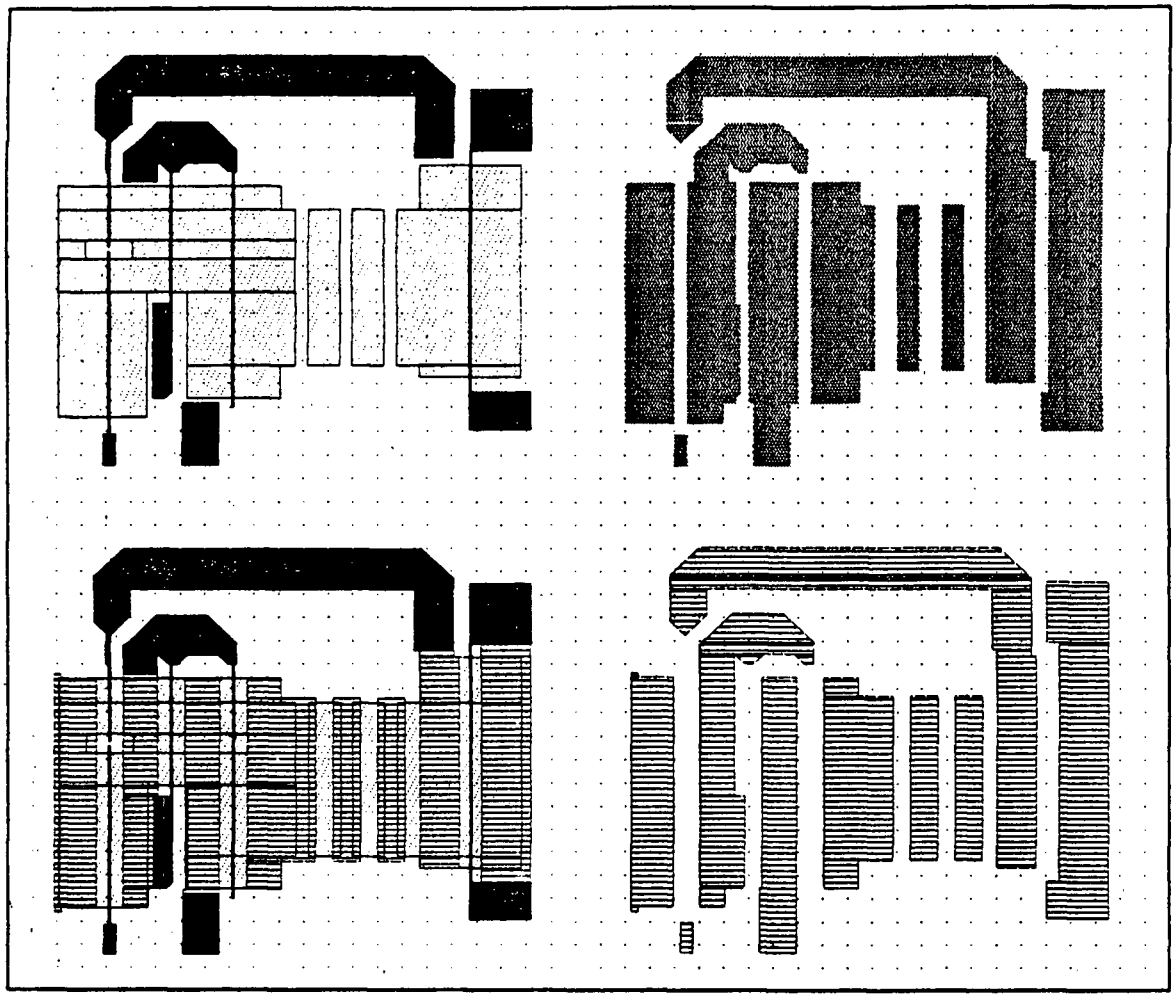


Fig. 6.2 Amplifier Layout

The -3dB frequency of the amplifier is determined by pole interaction treated by Hornbuckle and Van Tuyl[1.7]. Step response settling time is a more suitable performance measure for sampling. The input step of the simulations is a 0.1ps transition carried out about the amplifier symmetry bias point. The step amplitude is chosen to reflect the maximum excursions of the hold node with respect to keeping the amplifier output linear.

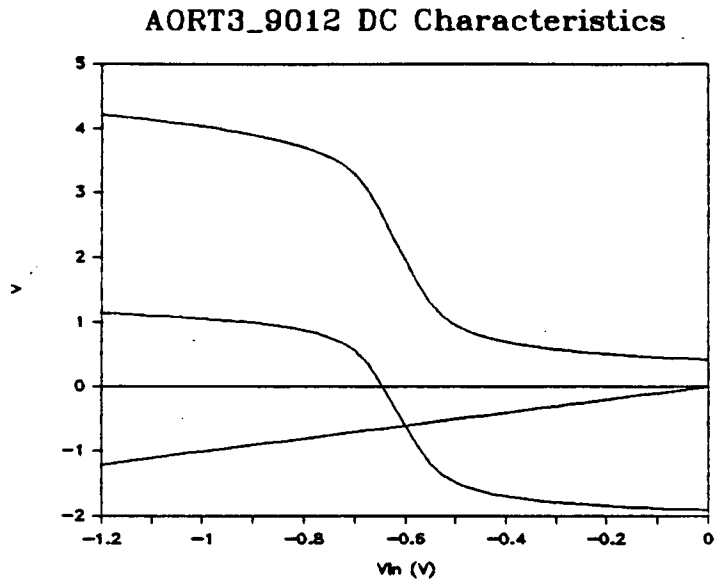


Fig. 6.3 Amplifier Open Loop DC Characteristics

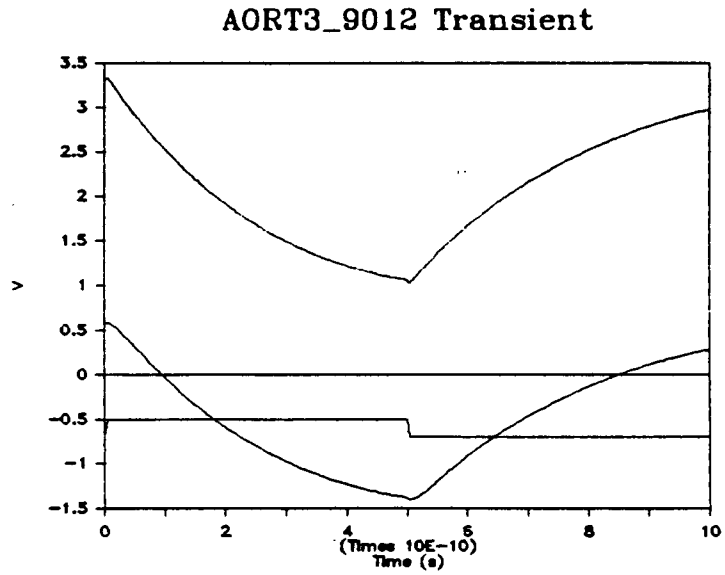


Fig. 6.4 AORT3_9012 Open Loop Transient

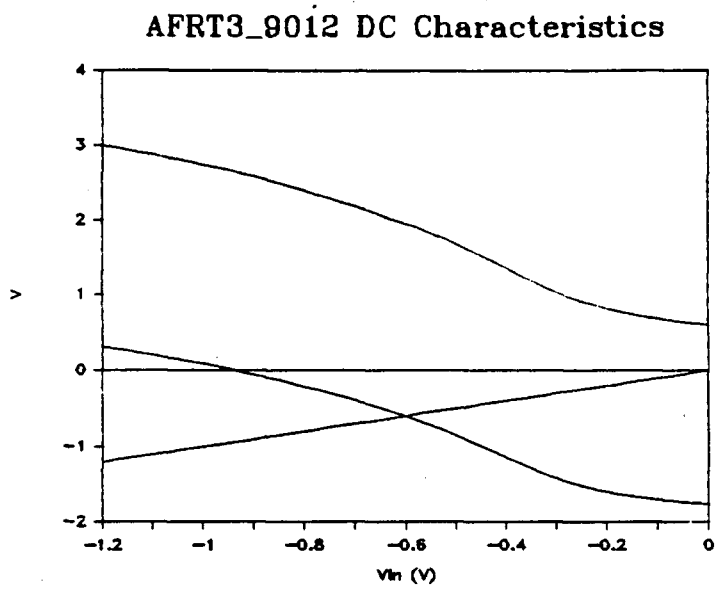


Fig. 6.5 90μm RSAG1_2 Amplifier DC Characteristics

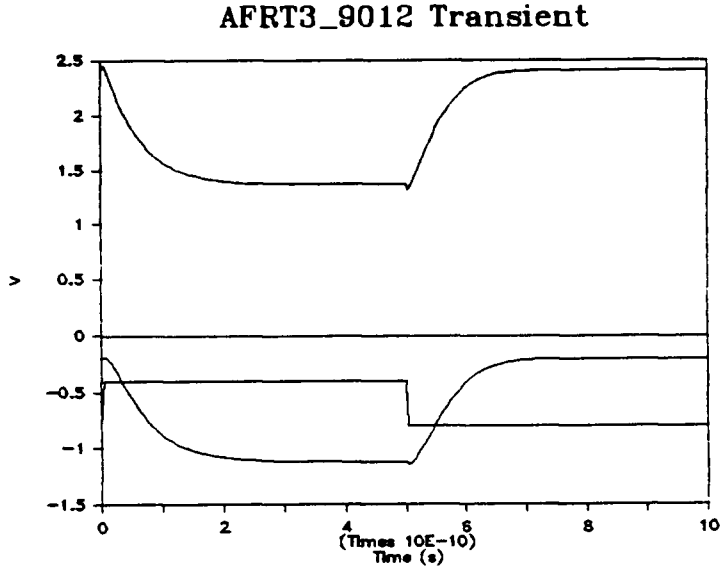


Fig. 6.6 90μm RSAG1_2 Amplifier Step Response

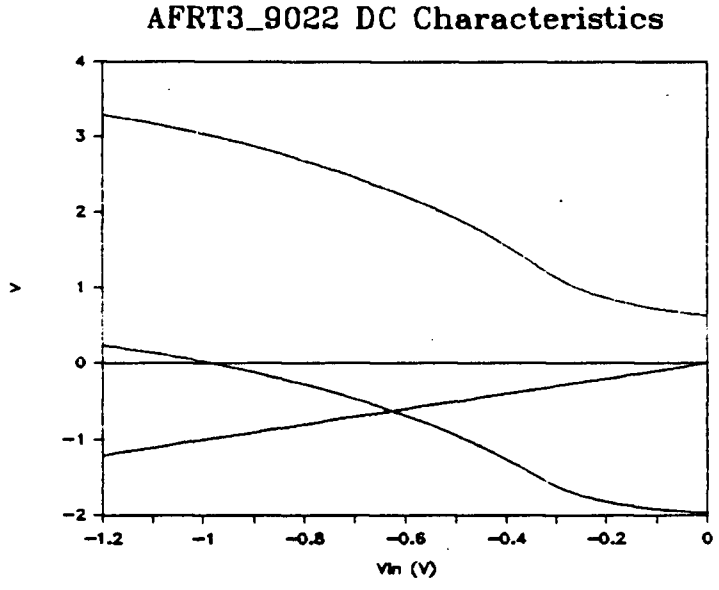


Fig. 6.7 90μm RSAG2_2 Amplifier DC Characteristics

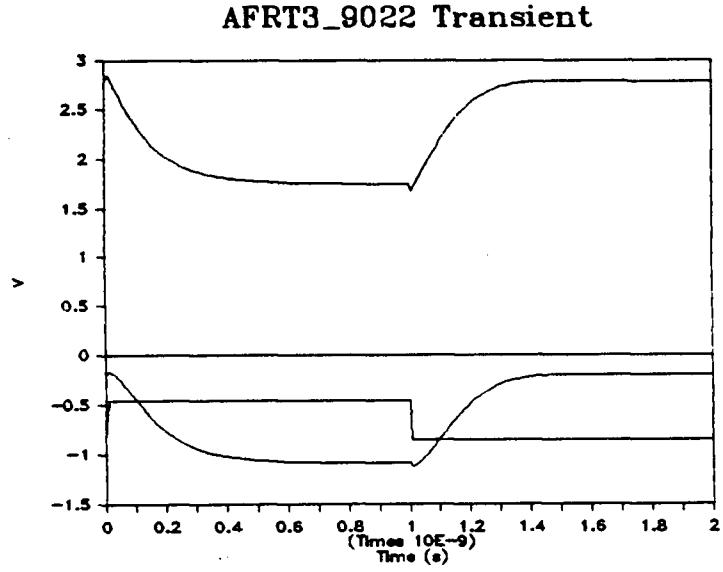


Fig. 6.8 90μm RSAG2_2 Amplifier Step Response

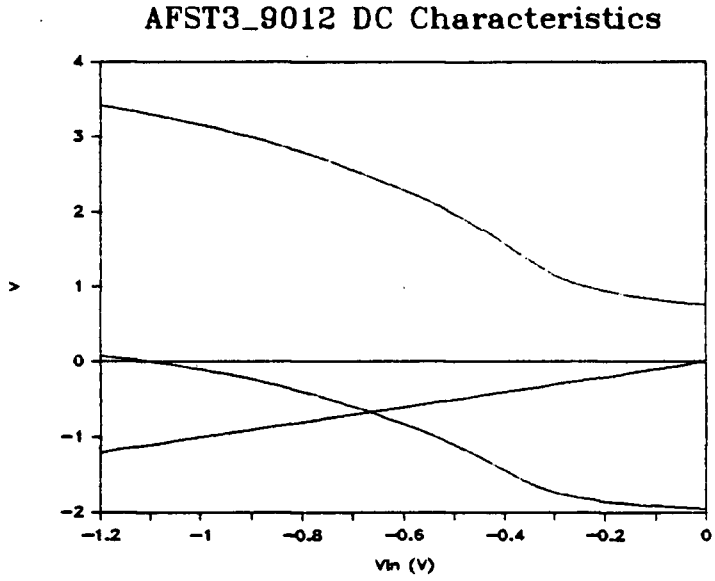


Fig. 6.9 90μm SI1_2 Amplifier DC Characteristics

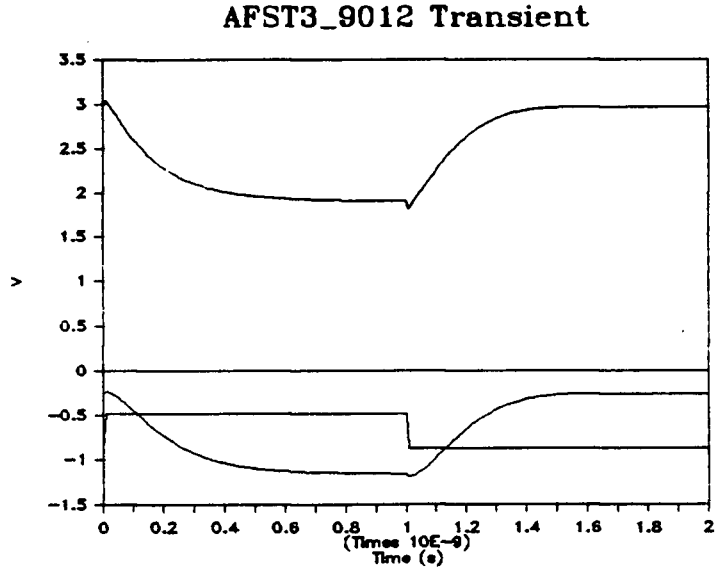


Fig. 6.10 90μm SI1_2 Amplifier Step Response

The Schottky diode stack number and width were chosen to maintain about a 1 V per diode voltage drop for a given supply voltage difference, scaled with V_T, and total R_{ps} to balance the output and input voltages. As the input voltage swing is biased near the center of the input MESFET operating characteristic the output voltage must coincide to give cascade capability.

The amplifier transient and DC characteristics are shown in figures 6.4 through 6.10 for the tightest lithographic tolerances of the three major performance groups. The fastest settling time is less than 200ps for RSAG1_2 technology.

Amplifier variations were generated for 30 to 120μm maximum MESFET width range, with 2, 3 and 4 diode stacks of both RD and TD type for the nine MESFET parameter sets. The role of the amplifier in this project was to demonstrate minimum settling time for the DRFM application, while providing a suitable adjunct for the switch. Variable hold capacitance increases with input width, output drive decreases with width and phase shift degradation of transient performance increases with width. The 67μm input width has a C_{ampin} of about 20fF for RSAG1_N and 40fF for the other processes at the required input bias. The combination of guard gate capacitance with C_{ampin} results in the approximate minimum capacitance for input time constant calculations for dual and triple gate switches.

7. ISAB DESIGN AND LAYOUTS

7.1 CONFIGURATIONS

The possible configurations include single, dual and triple gate switches of various widths in each of the nine MESFET variations, combined with an amplifier in the same or other process variation. A representative group of 28 ISAB configurations were included on the mask with a subset of 21 separate switches and 12 amplifiers(re: Fig. 1.3).

Seven SI process ISABs are included without separated components, as on chip priority was given to RSAG units in terms of research interest. The SI units encompass 140μm center tap single, dual and triple gate switches in both 2

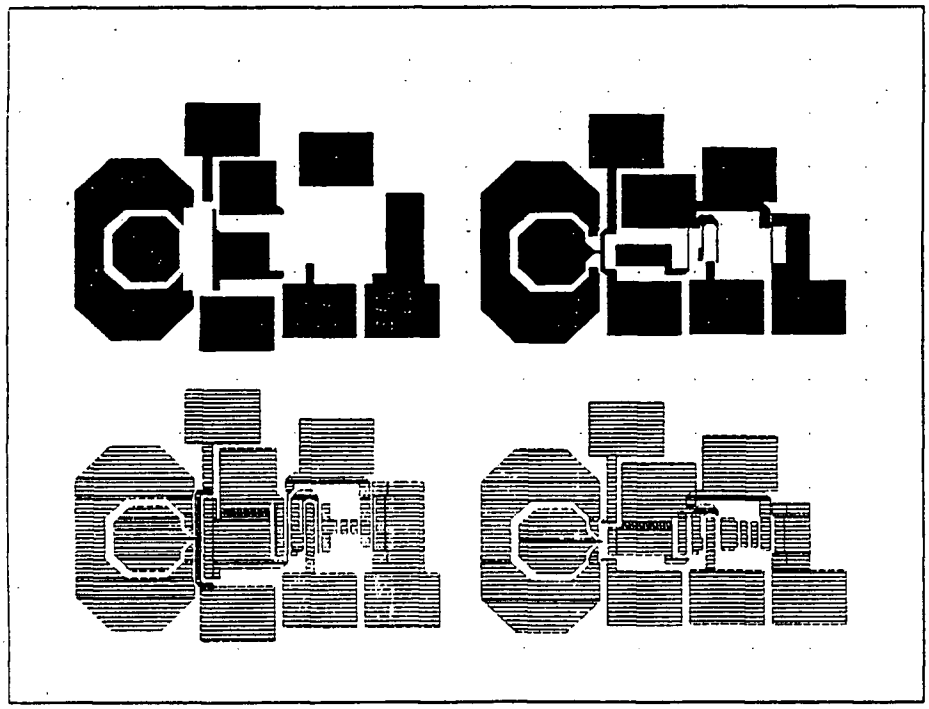


Fig. 7.1 SI and RSAG ISAB layout

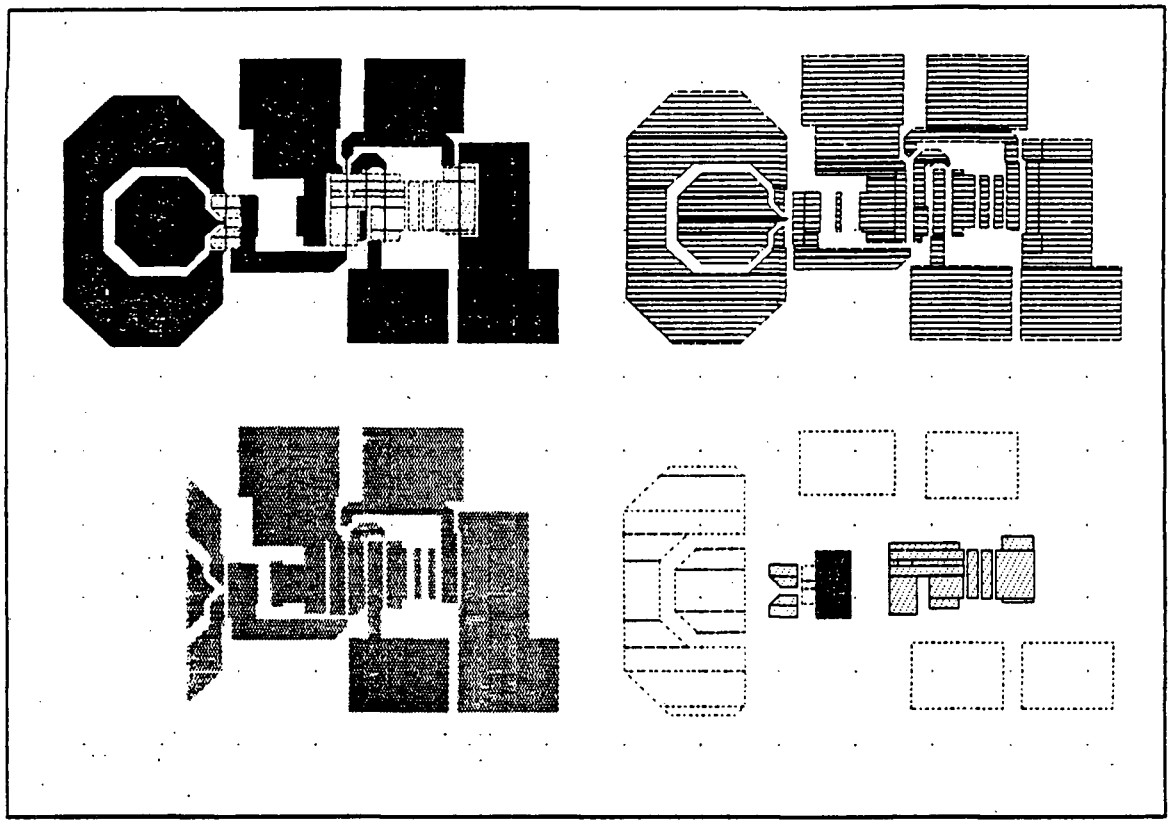


Fig. 7.2 MIM ISAB layout

and 3μm source/drain gap variations with 90μm amplifiers in the same variation plus one single gate 4μm gap ISAB. The ISAB layout on the left of figure 7.1 is the triple gate 2μm gap version, of which a full page layout is included in appendix B.

The minimum input time constant for a given switch is obtained by eliminating all fixed hold capacitance, as seen in equation 7-1.

$$C_{hold} = C_{fixed}+C_{ampin}+C_{guard}+C_{switch}+C_{parasitic} \qquad [7-1]$$

The switch contribution is a combination of C_{DS} and C_{GD} assuming the hold node is the switch drain side. As guard gates are added the resulting decrease of node charging current makes interdigitated capacitors a more attractive process option due to the process yield considerations of MIM shorts.

7.2 ISAB SIMULATION RESULTS

Taking the theoretically derived SPICE model parameters from table 4.1 a representative selection of large signal simulations were performed. These include simulations of expected pulse and transient conditions indicative of intrinsic performance with ideal input conditions. The overall performance of actual devices will depend on actual inputs and associated parasitics as well as the intrinsic performance highlighted here. The SPICE MESFET model version used has fixed C_{GD} with a value the same as C_{GS0}. More accurate capacitance modeling can be done at the expense of increased simulation time. Circuit parameters for the SPICE source listings for the simulations are in appendix D.

Figures 7.3 to 7.5 show the simulated open switch tracking of the three tightest tolerance RSAG ISABs with a 1GHz sine wave input. As the number of guard gates are increased fixed node capacitance is decreased to compensate, however as can be seen in figures 7.3 to 7.5 significant hold node attenuation and phase shift occurs.

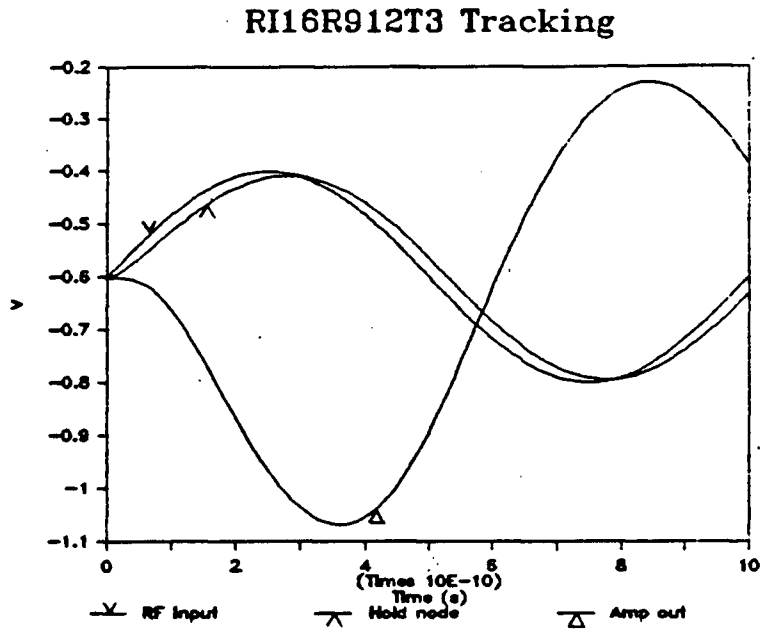


Fig. 7.3 RSAG1_2 Single Gate ISAB Tracking

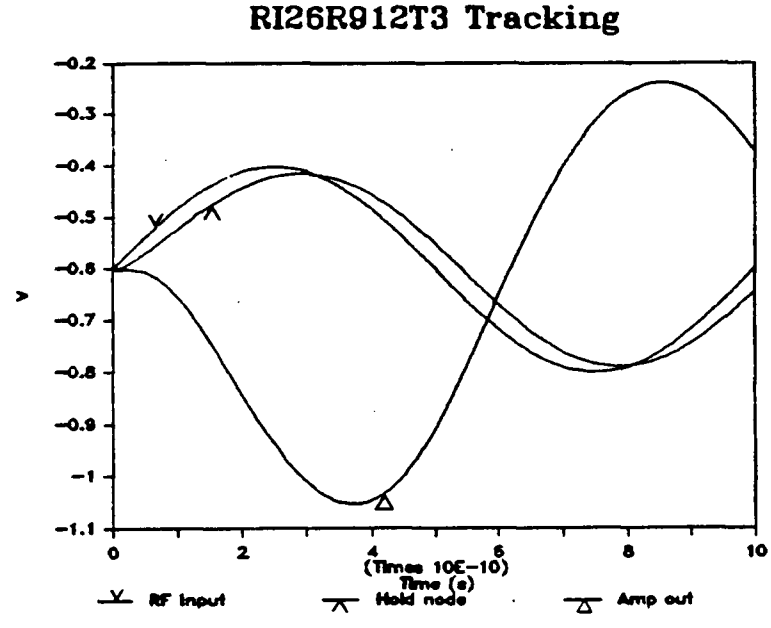


Fig. 7.4 RSAG1_2 Dual Gate ISAB Tracking

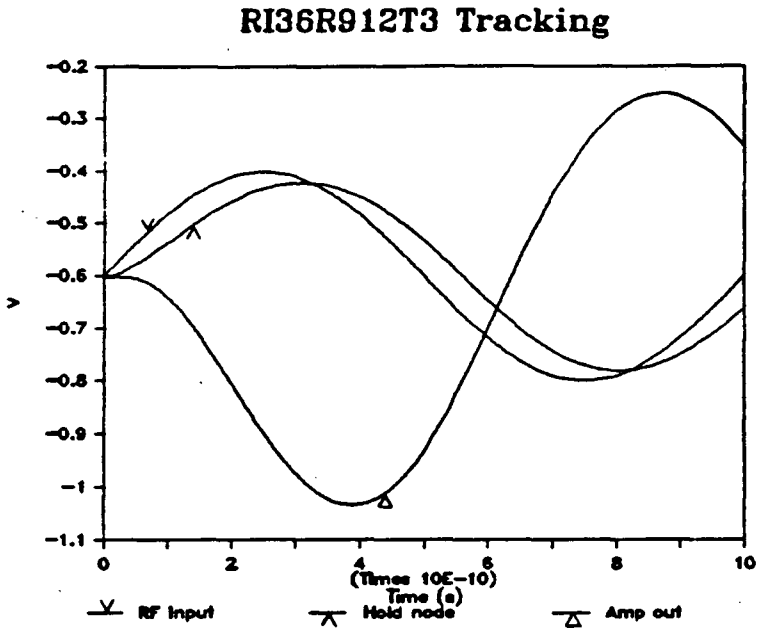


Fig. 7.5 RSAG1_2 Triple Gate ISAB Tracking

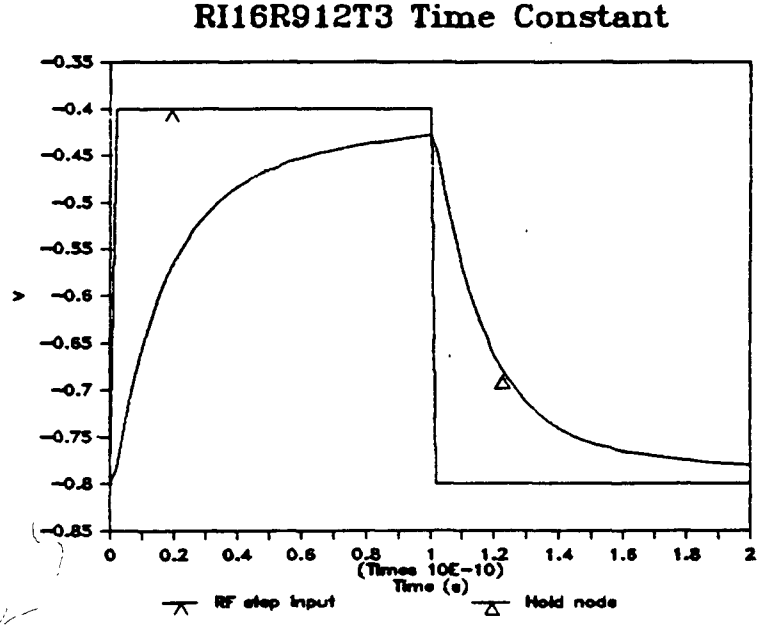


Fig. 7.6 RSAG1_2 Single Gate Time Constant

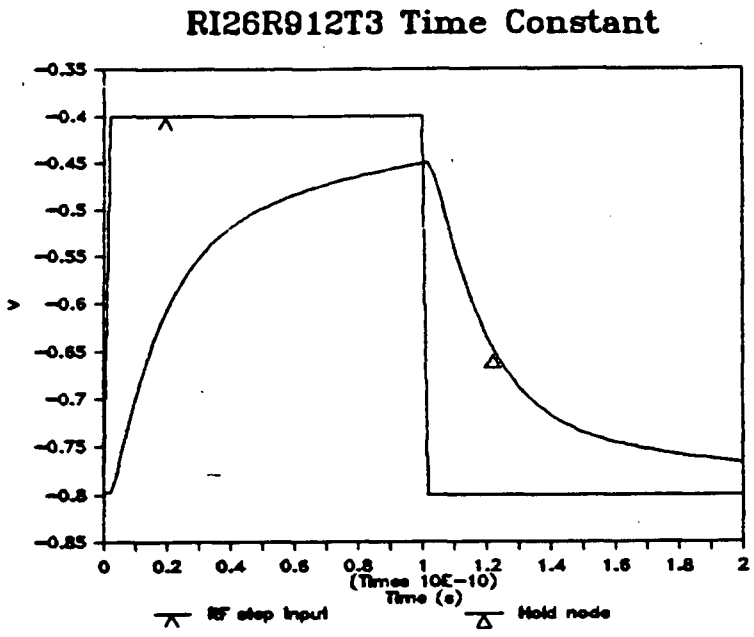


Fig. 7.7 RSAG1_2 Dual Gate Time Constant

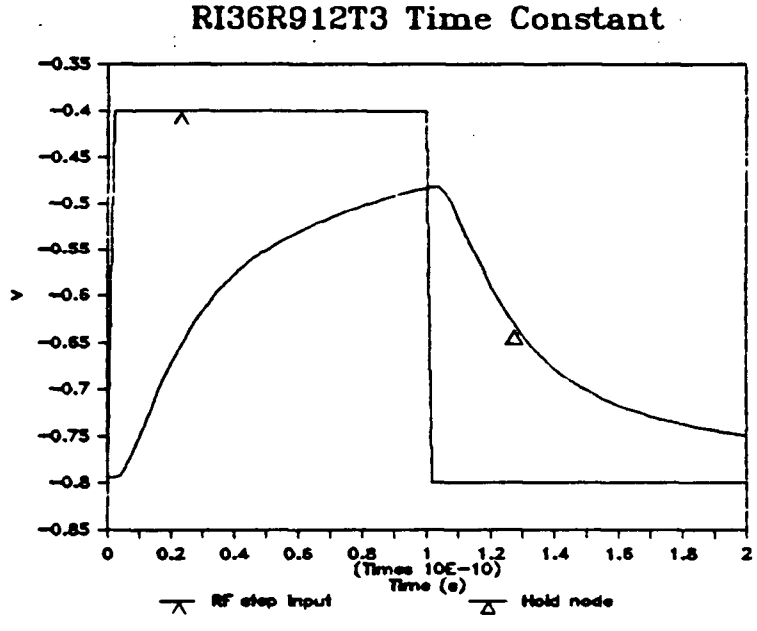


Fig. 7.8 RSAG1_2 Triple Gate Time Constant

Figures 7.6 to 7.8 use the same circuit model as figures 7.3 to 7.5 with a 0.1ps step input of the same magnitude. The input time constant increases with the number of gates from about 40ps for 90% sampling efficiency with a single gate switch to about 52ps and 71ps for dual and triple gate switches.

Figure 7.9 shows the simulated distortion of an ideal 50Ω transmission line pulse on the gate pad due to a single gold bond wire and variable capacitance of the gate. Figures 7.10 through 7.12 show the effect of guard gates on pulse feedthrough at both the RF input side and hold node side. The hold node voltage changes to a more negative value on switch closure due to channel majority carrier distribution across capacitances. Initially the single gate switch of

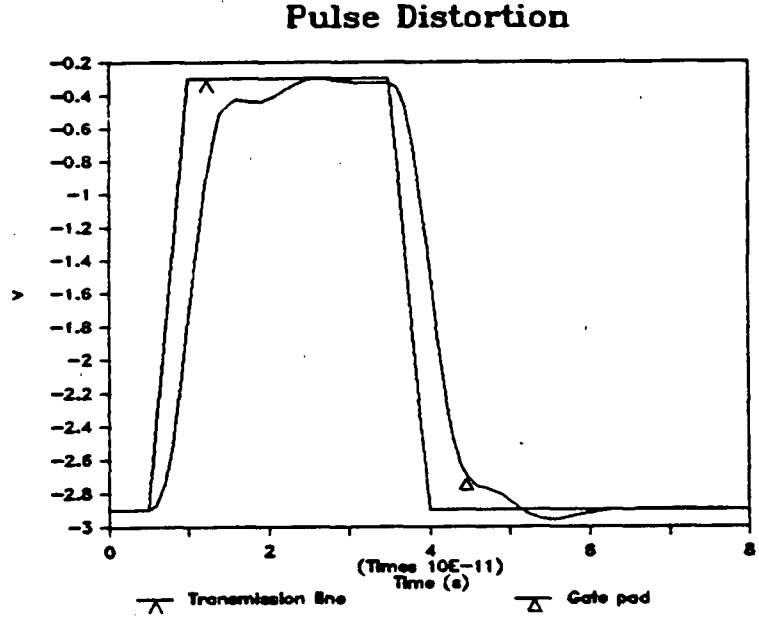


Fig. 7.9 Pad Pulse Distortion

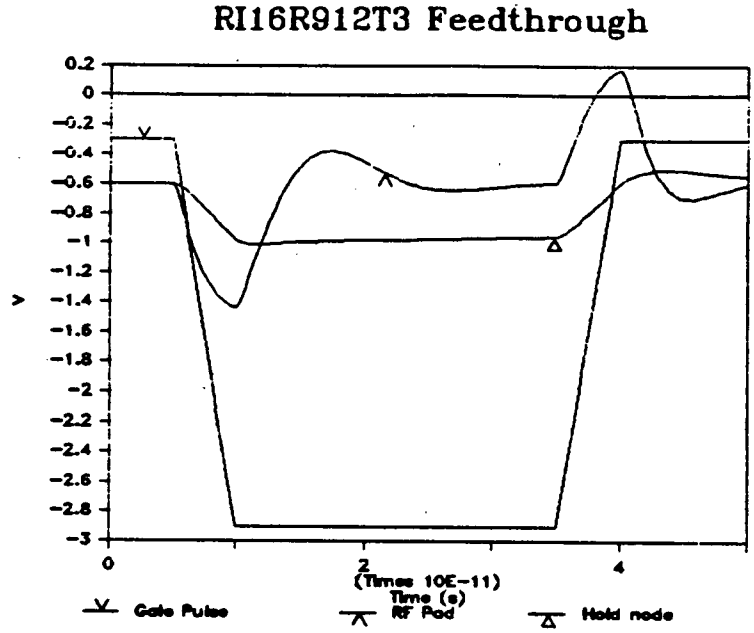


Fig. 7.10 Single Gate Feedthrough

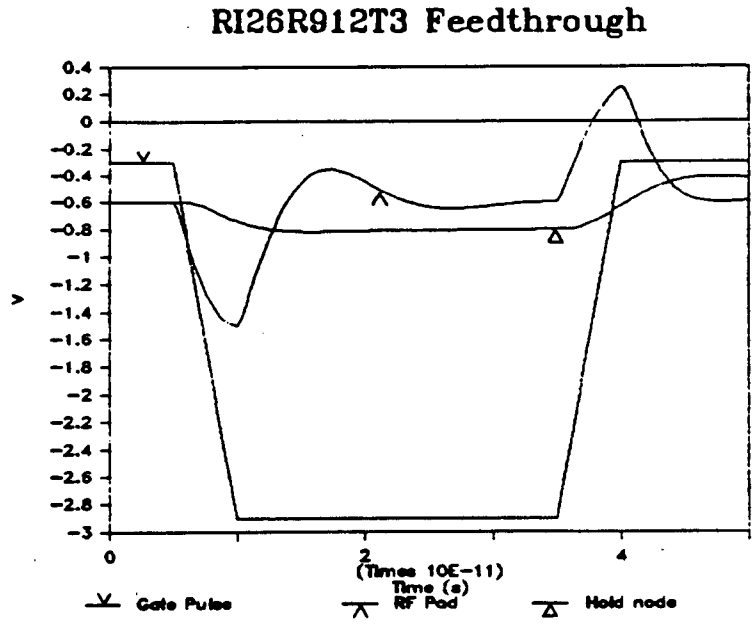


Fig. 7.11 Dual Gate Feedthrough

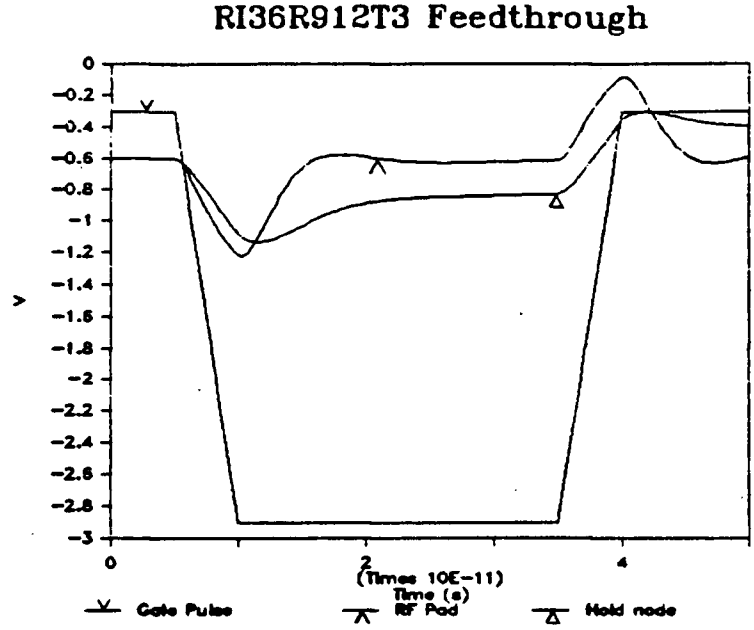


Fig. 7.12 Triple Gate Feedthrough

figure 7.10 is open with source and drain at the same potential as the 152fF fixed capacitor. When the switch ramps closed in 5ps both source and drain receive an injection of majority carrier causing a negative voltage swing. The lack of availability of neutralizing charge for the hold node produces a stored negative offset of about 0.4V inversely proportional to the node capacitance. The RF input side is neutralized returning to its original potential in about 20ps. On switch opening majority carriers are pulled into the channel leaving a temporary lack at source and drain, increasing voltage. The resultant transient decays in approximately the same time as for switch closure, about 20ps.

The dual gate switch of figure 7.11 has a single guard gate on the hold node side with a 39fF fixed capacitor. The hold node stored negative offset of figure 7.11 is reduced in the presence of the guard gate to about one half the single gate magnitude of figure 7.10. The post switch opening transient is about 100mV larger requiring a longer settling time. The guard gate C_{GS0} is about 36fF, and V_{GS} is 0.3 V at the amplifier symmetry point giving a C_{GS} of about 41fF from equation 4-3. Thus the combined distributed capacitance for the initial phase of the dual gate simulation is about $116fF+C_{switch}+C_{ampin}$ as compared to $152fF+C_{switch}+C_{ampin}$ for the single gate. As charge is transfered to the hold node during the switch down ramp guard gate C_{GS} increases responding to the change in potential to about 47fF. The displaced charge can be considered to be held on two nodes, the switch guard gate node and the hold node separated by the guard gate channel. The approximate simulated capacitance of the switch guard gate node is $C_{switch}+C_{GSguard}$ and that of the hold node $C_{ampin}+C_{fixed}+C_{GDguard}$. The charge holding ability of the various capacitances is directly proportional to the voltage across the capacitance. When the strobe down ramp levels off the switch gate is at -2.9V such that about -2.1V is across C_{switch}. $C_{GSguard}$ and $C_{GDguard}$ have about +0.5 volts across them and C_{fixed} and C_{ampin} are about +0.8 V. The distributed capacitance of the two nodes thus holds less charge than the single node of the single switch ISAB. The "blow-by"

displacement charge is the same however, thus some of the channel charge is being neutralized by another source of carriers. The most obvious path for these carriers is from the bias supply through the guard gate Schottky diode.

Figure 7.13 shows the voltage at the guard node between the switch and the guard gate for a dual gate switch, with the same transient conditions as figure 7.11. The guard node voltage drops suddenly in response to electrons being injected from the switch. The voltage from gate to source of the guard gate reaches about 0.9 V, causing electrons to tunnel through the Schottky barrier. Figure 7.14 shows the guard gate current increase in the positive going pulse, corresponding to the strobe down ramp. The negative going current pulse is mainly due to capacitive coupling, and as

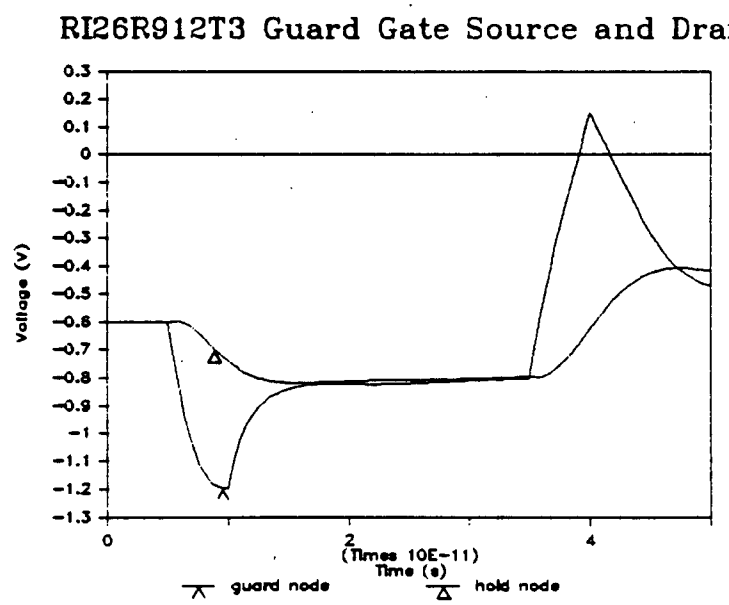


Fig. 7.13 Guard Gate Source and Drain Voltages

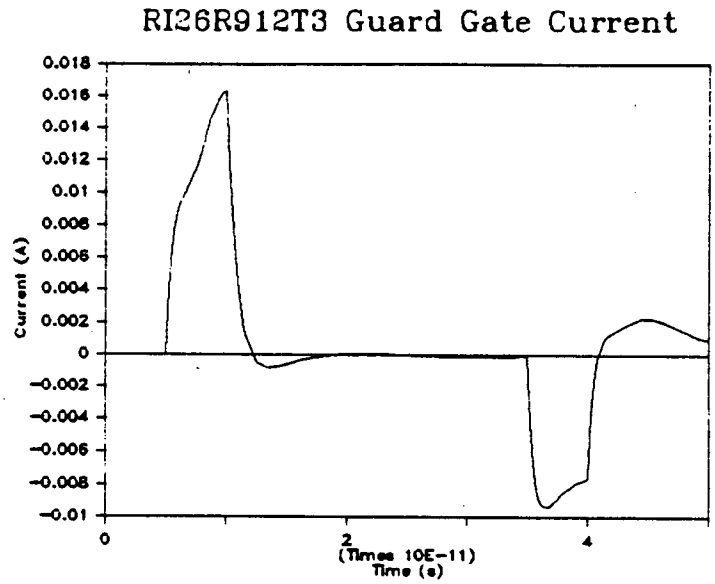


Fig. 7.14 Guard Gate Current

such is missing the conduction effect.

The triple gate switch of figure 7.12 exhibits a reduced RF pad transient due to its guard gate and a larger hold node swing than either the single or dual gate switch. The reason for the increased hold node swing is reduced hold node capacitance in an attempt to improve the input time constant. The hold node capacitance is thus mainly composed of guard gate and amplifier input depletion capacitance which varies with hold node voltage. Unfortunately the triple gate switch is both slower in terms of input time constant and as a result of minimal fixed capacitance at the hold node not as good in terms of hold node feedthrough.

While the single gate switch is predictably the fastest in terms of input time constant the dual gate exhibits about

one half the feedthrough, at the amplifier input bias voltage, with a 30% time constant increase.

Figures 7.15 to 7.20 show sampled tracking conditions similar to those of Barta and Rode[1.3] using a 36MHz sine wave input, however the strobe pulses are at 1 rather than 2ns intervals as suggested by the research sponsor. The strobe pulse rise time is taken as 20% of the strobe "ON" width for all the simulations. Figure 7.15 shows sampled tracking if the RF pad input bias is at the same level as the unsampled tracking of figure 7.3. Due to the stored negative offset at the hold node after switch closure the amplifier input is biased about 200mV below its symmetry transfer point. This can be corrected by changing the bias of the RF pad input by 200mV as seen in figure 7.16 resulting in a symmetrical amplifier output.

Figure 7.18 shows that the single gate ISAB still tracks when operated below the 90% sampling efficiency aperture. The simulation resolution of figure 7.18 is 50ps and as such some of the hold node detail is lost. It should be noted that the amplifier acts as a low pass filter with respect to hold node transients and as such their output magnitude can be limited with minimal sample and hold signal degradation by choosing the amplifier frequency response appropriately.

Figure 7.19 shows triple gate tracking with 300ps pulses. Signal divergence problems were encountered, where hold node voltage would consistently rise when using

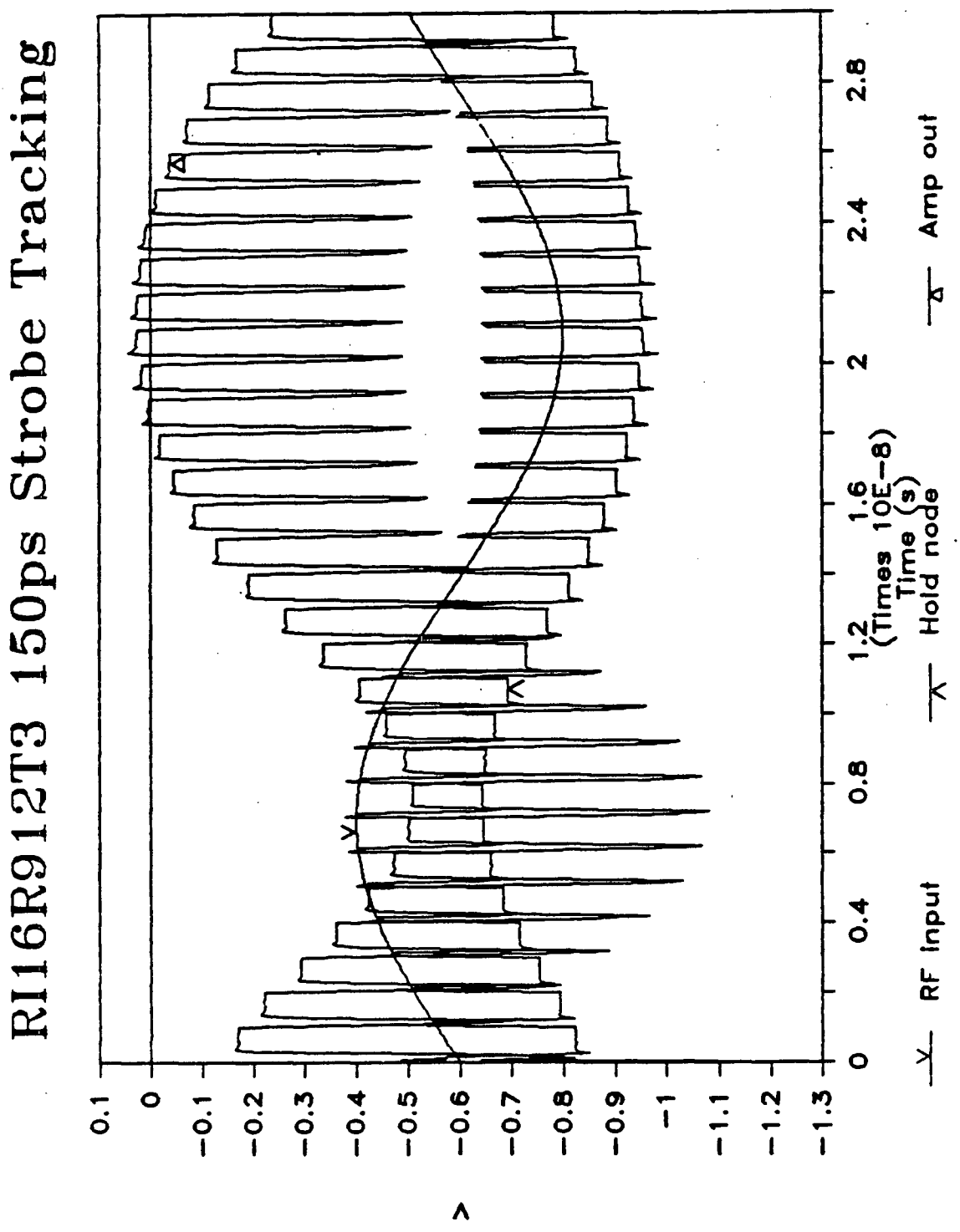


Fig. 7.15 RI16R912T3 150ps Tracking, 0.6 V Bias

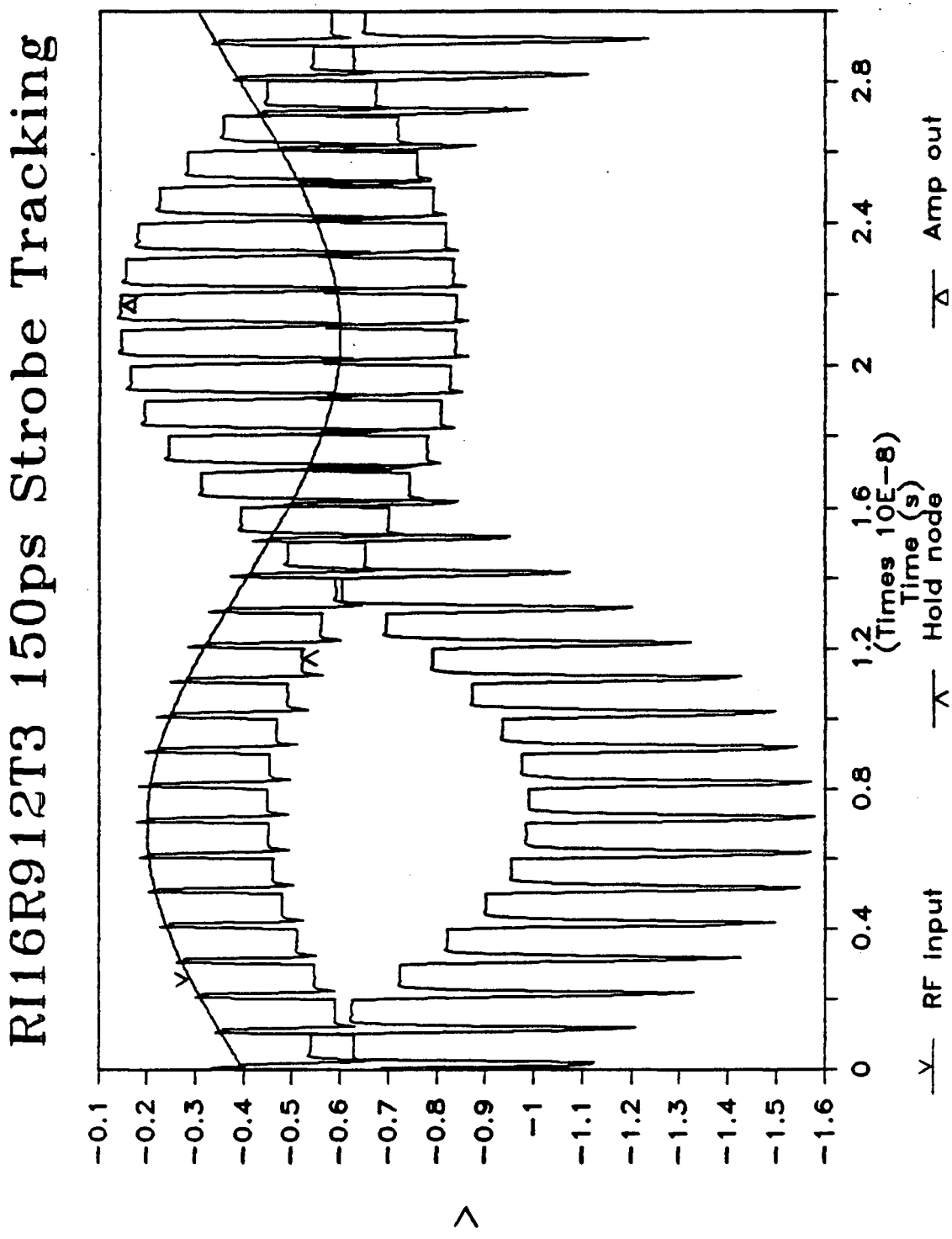


Fig. 7.16 RI16R912T3 150ps Tracking, 0.4 V Bias

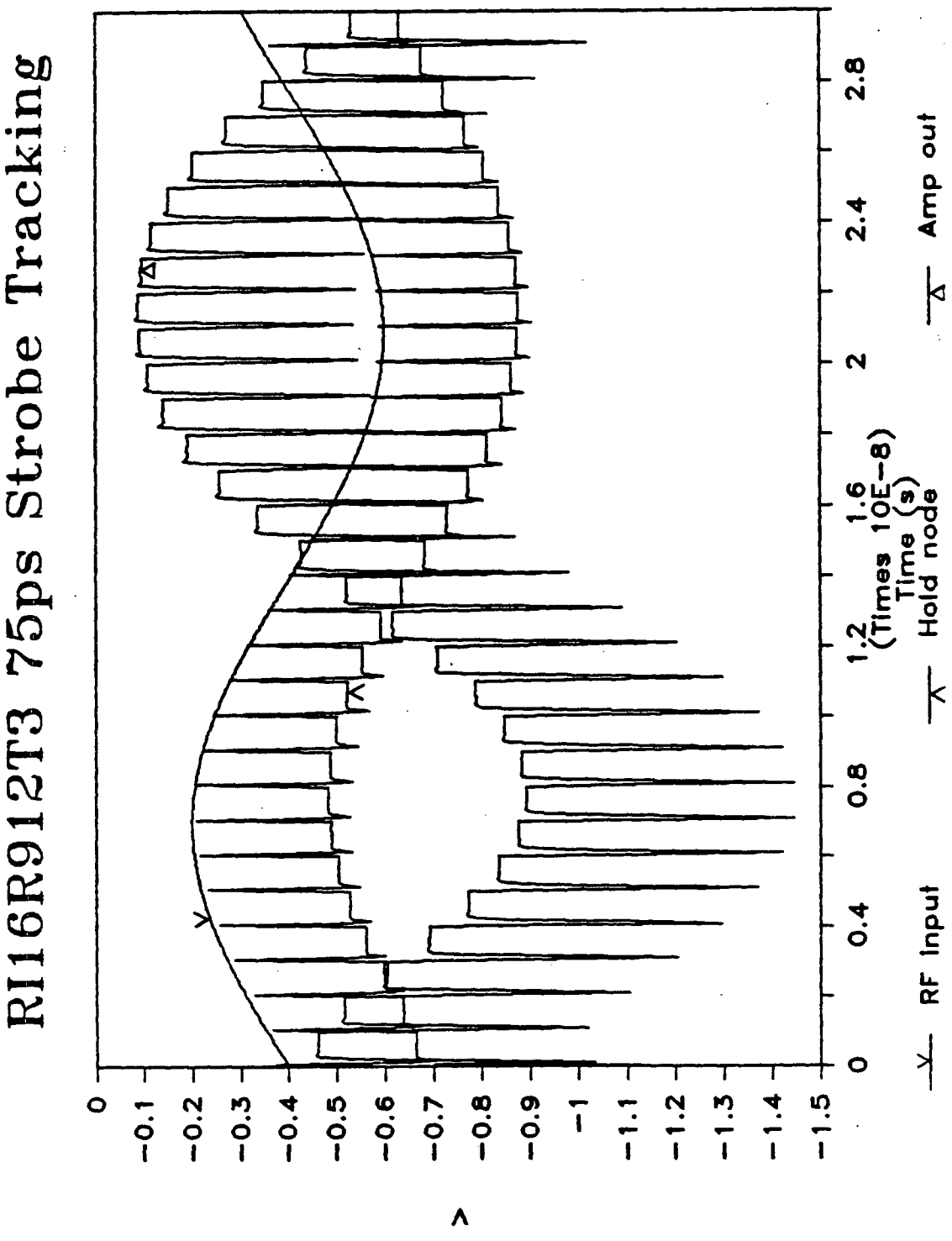


Fig. 7.17 RI16R912T3 75ps Tracking

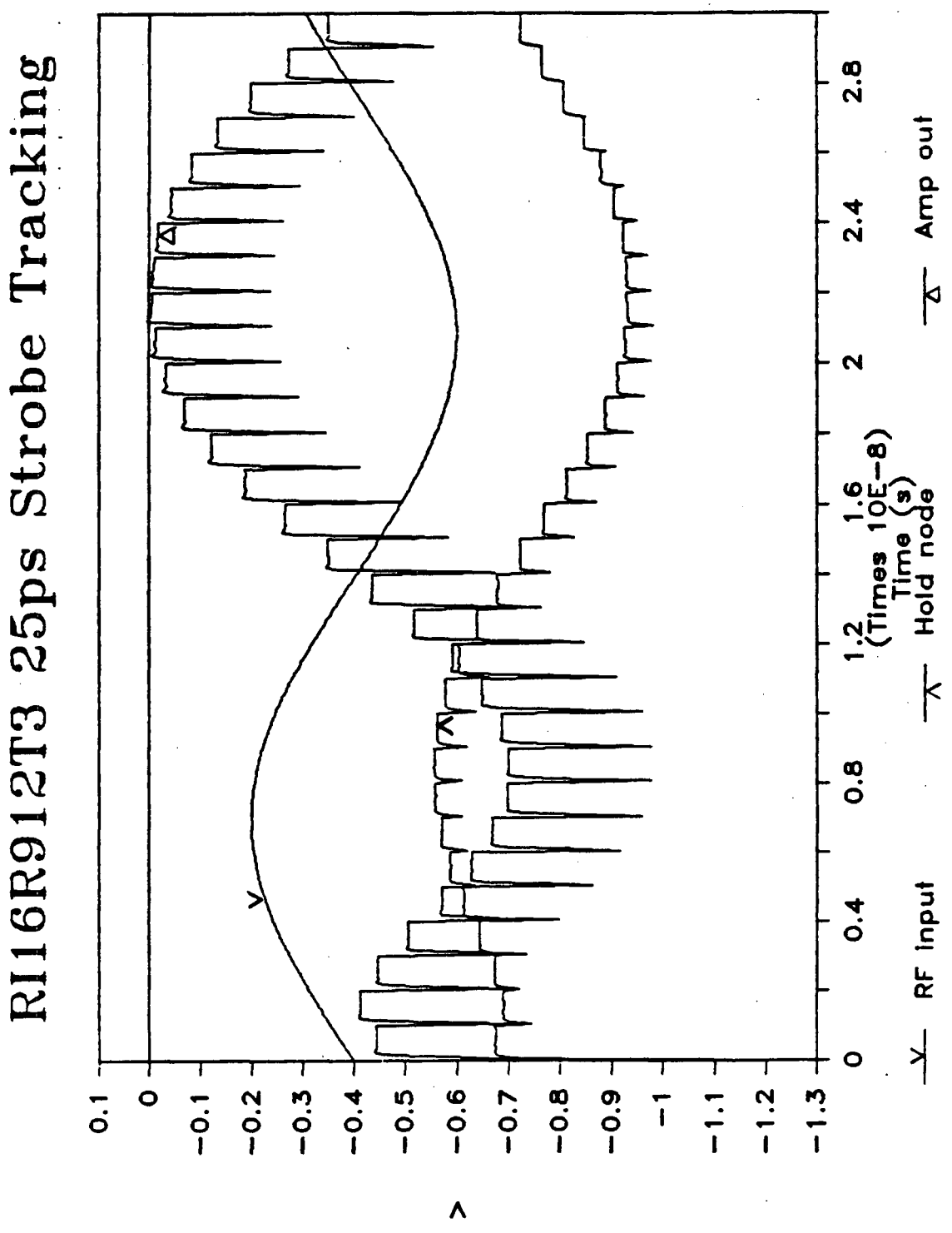


Fig. 7.18 RI16R912T3 25ps Tracking

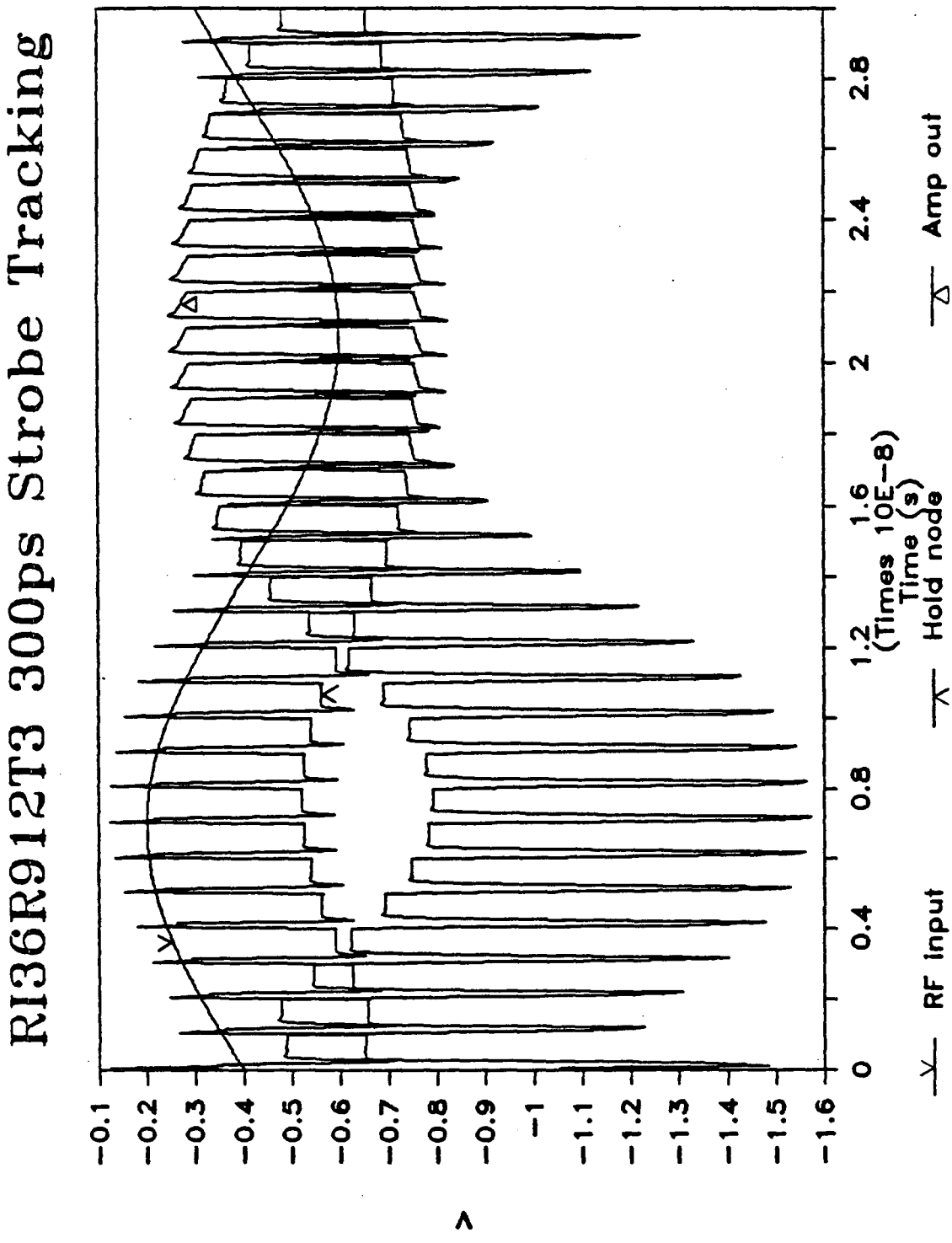


Fig. 7.19 RI36R912T3 300ps Tracking

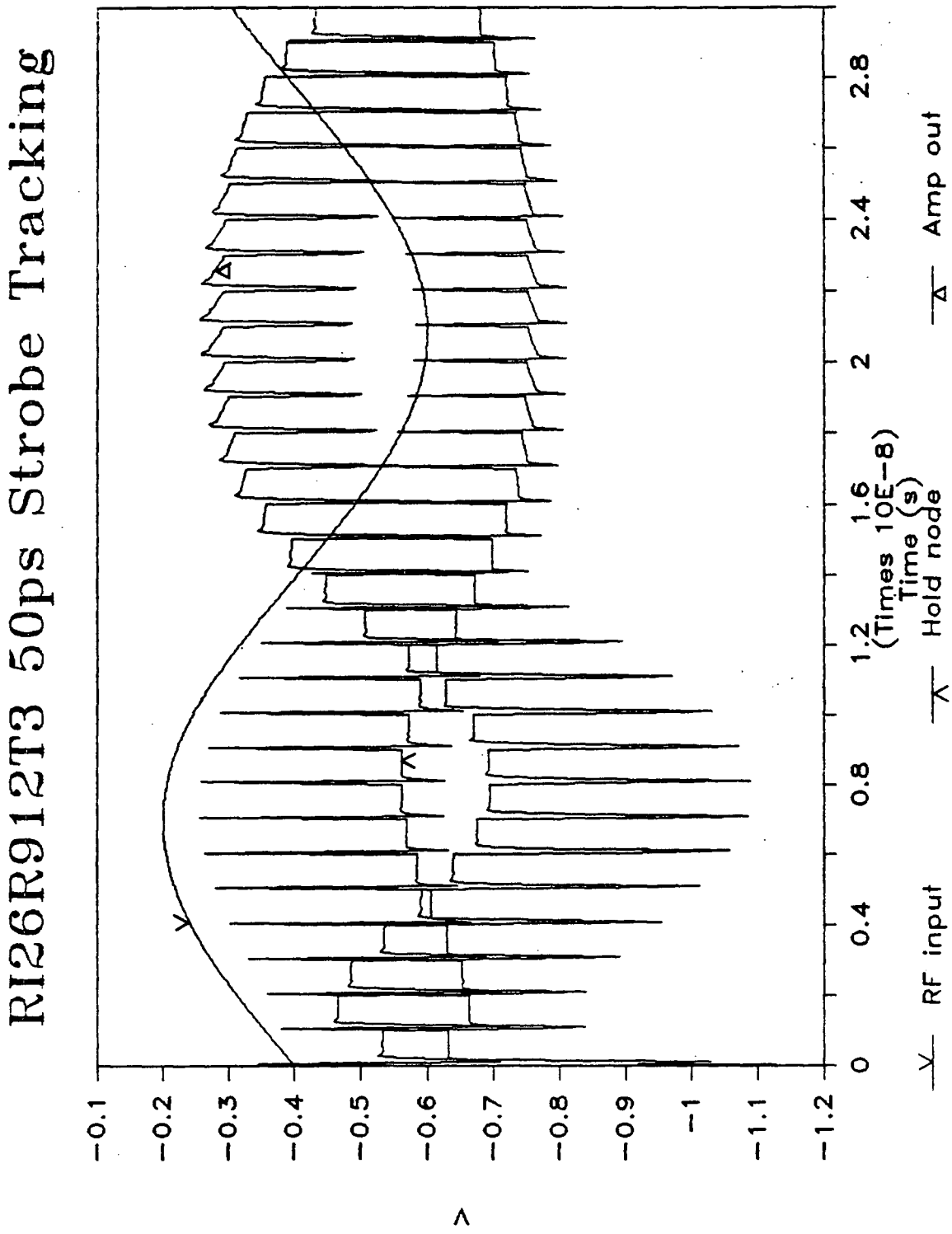


Fig. 7.20 RI26R912T3 50ps Tracking

narrower pulses. Figure 7.20 shows dual gate tracking at 50ps, close to the 90% sampling efficiency input time constant. Both figures 7.19 and 7.20 exhibit feedthrough compression on the negative swing of the input sine wave and a spreading effect on the positive going half cycle. This effect is not seen on the single gate tracking simulations of figures 7.16 to 7.18. The probable cause is hold node side guard gate bias with respect to the hold node voltage. The guard gate voltage is fixed such that any depletion region variation or gate conduction is caused by changing source or drain potentials. The depletion region capacitance will decrease as the source/drain potentials increase and vice versa. The amount of charge is being expelled from the switch by the action of the strobe is relatively constant. Greater capacitance is available at the hold node with more negative guard gate source/drain voltages thus the stored negative offset is less, however only slight change would be due to this as the capacitance change is only a few fF. The neutralizing charge injected by the hold side guard gate will depend on the initial bias of the hold node as this will determine the position of the negative transient on the voltage axis of figure 7.13. The more negative the peak the greater the amount of neutralizing charge passing through the guard gate Schottky diode under forward biased conditions. Thus feedthrough is less with lower hold node voltage.

The amplifier bandwidth is instrumental in determining the peak feedthrough voltage. Comparison of devices should thus be done on the basis of similar amplifier bandwidth. The amplifier bandwidth of Barta and Rode[1.3] is in the order of 1GHz whereas the RSAG1_2 amplifier bandwidth is in the order of 3GHz.

The simulations were done with fixed C_{GD} at C_{GS0} which is a reasonable approximation for V_{GD} near 0 V and low V_{DS}. More accurate capacitance simulation would be very unlikely to reduce the 200 to 800mV feedthrough transients of the simulations an order of magnitude to compare directly with the experimental 35mV feedthrough of Barta and Rode. The discrepancy would seem to be with the pulse parameters of the experimental setup compared to ideal pulses combined with transient response of the amplifier and measuring system compared to the simulated version.

8. PROCESS MONITORS AND MEASURED RESULTS

The early verification of device characteristics enhances fabrication troubleshooting. Test probes can be used, as soon as AuGe ohmics are present, to verify implant activation and ideality factor. At the same time MESFET DC characteristics and metal sheet resistance can be checked.

8.1 ISOLATION MONITORS

The isolation monitors (at coordinates G 1L, G 1R ,G 10, H 10 in figure 1.3) are ohmic pads on combined Nminus and Nplus implants separated by a gap to test the nonactivated substrate for retention of the semi-insulating sheet resistance of about $3 \cdot 10^8 \Omega/\square$ in both crystal directions with respect to the major flat. Should this isolation be less for some reason it is possible to incorporate an isolation implant[8.1].

8.2 TLMS

The three transmission lines (L 5T, L 5B, L 10) measure the contact resistance of the AuGe ohmic pads to the three possible implant combinations for calibration of process anneal characteristics. The pad gaps are measured by SEM and the data analyzed by use of the transmission line model[8.2] for accurate results.

8.3 POWER MESFET

The gate of an open drain power MESFET should be driven with the last amplifier output. A power MESFET requires airbridges for the interdigitated gate architecture. This architecture could be expanded to a dual gate configuration for output sampling to a time domain multiplexed transmission line. A single gate version power MESFET has been included on the mask for fabrication evaluation. [8.3].

8.4 TIW SHEET RESISTANCE

The stepped resistor pattern used to determine TiW sheet resistance is shown in figure 8.2. The actual segment widths can be measured by SEM and the resistivity calculated after [2.2].

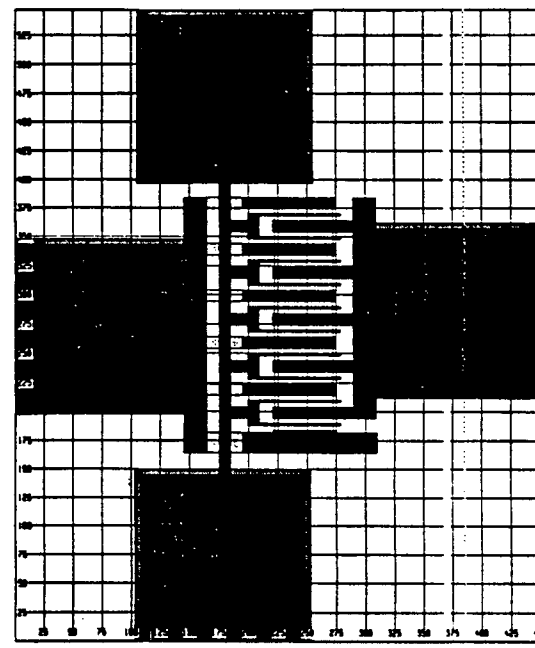


Fig. 8.1 Power MESFET Gate Strip Layout

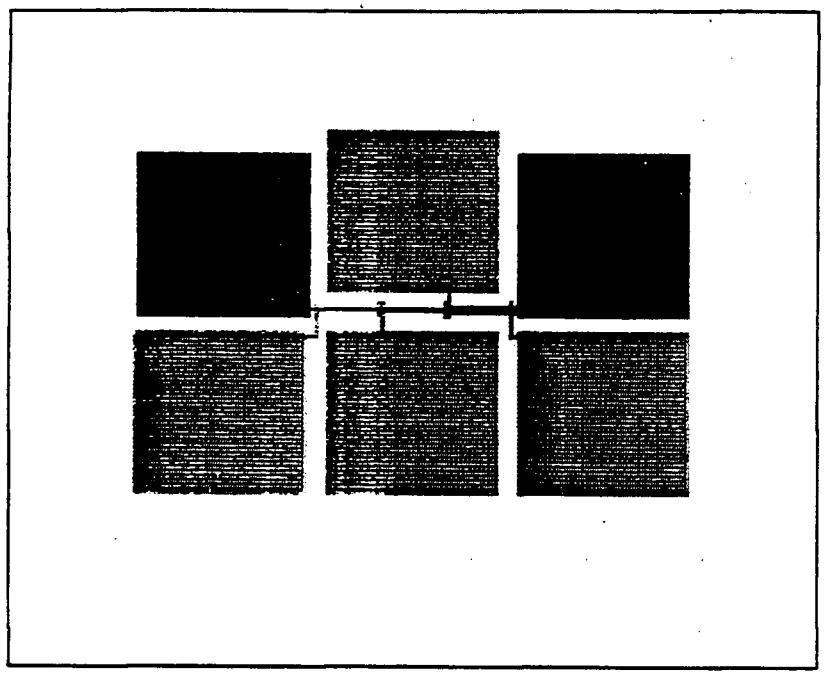


Fig. 8.2 TiW Stepped Resistor Layout

8.5 THREE AMPLIFIER OSCILLATOR

Airbridges were used to construct a three amplifier ring oscillator to verify simulation. The RSAG1_3 MESFET was used as a base unit to increase the probability of all three amplifiers working.

8.6 PEAKING INDUCTOR

The amplifier frequency response can be improved by adding a pole with a peaking inductor in series between the input and output stages.[1.8]

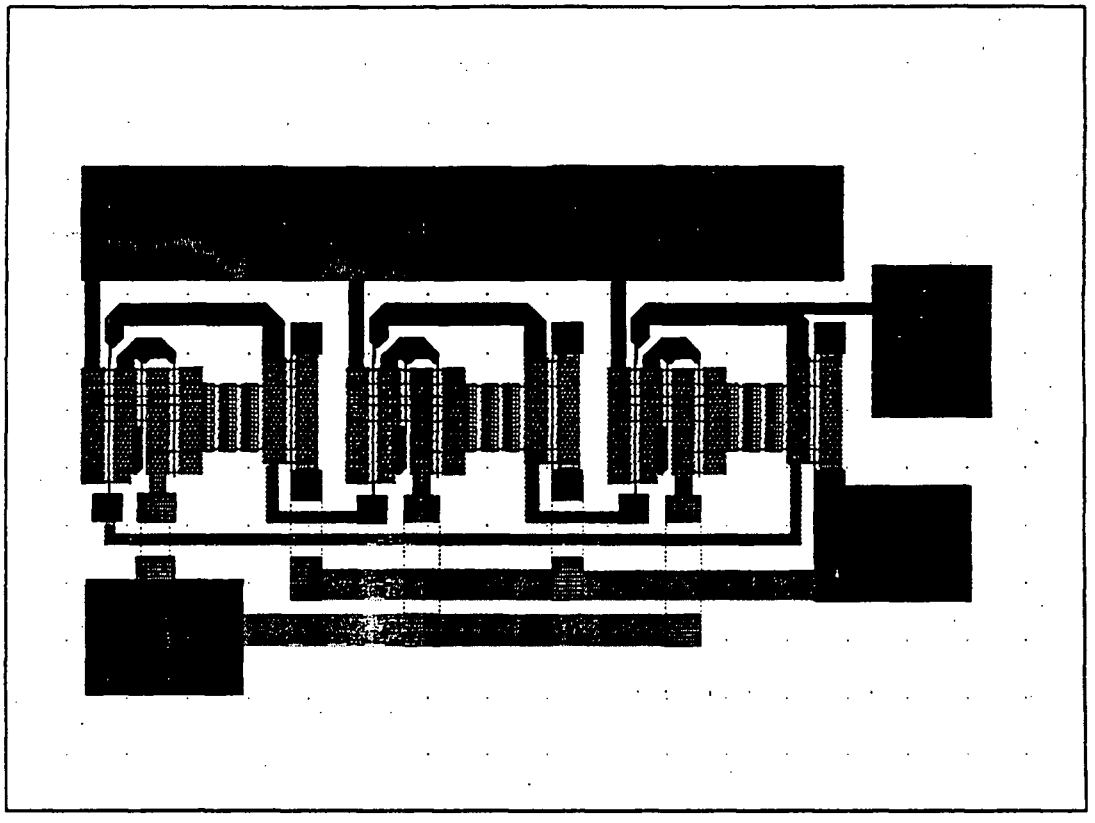


Fig. 8.3 Test Oscillator OFRT3_9013

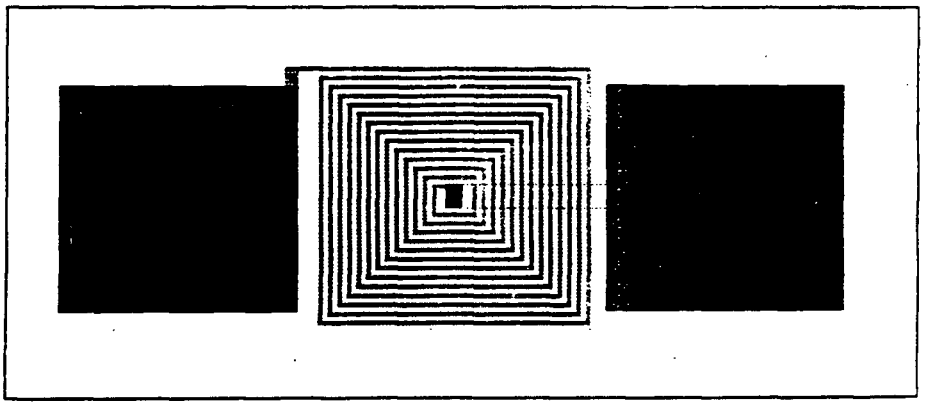


Fig. 8.4 Amplifier Peaking Inductor

8.7 SELECTIVE IMPLANT FABRICATION RUN RESULTS

8.7.1 ISOLATION

The isolation monitors are two 150μm square pads on Nplus GaAs separated by a 15μm gap of SI GaAs. Figure 8.5 shows the current and resistance plots for a low voltage scan of the monitor on test chip 8. Considering the positive voltage side a diode characteristic appears with a series resistance in the order of 15kΩ implying a sheet resistance of 150kΩ/□. Figure 8.6 from chip 5 shows about 5MΩ series resistance corresponding to about 50MΩ/□ of isolation which is an improvement over chip 8 however does not match the expected semi-insulating value of 300MΩ/□. Switch "OFF" isolation and hold mode

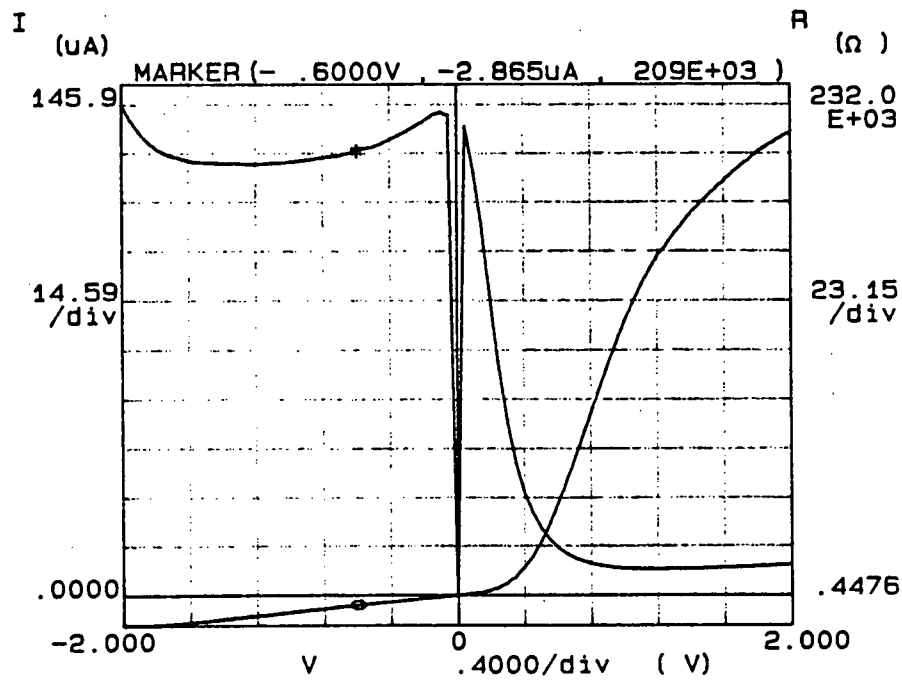


Fig. 8.5 Isolation monitor chip 8

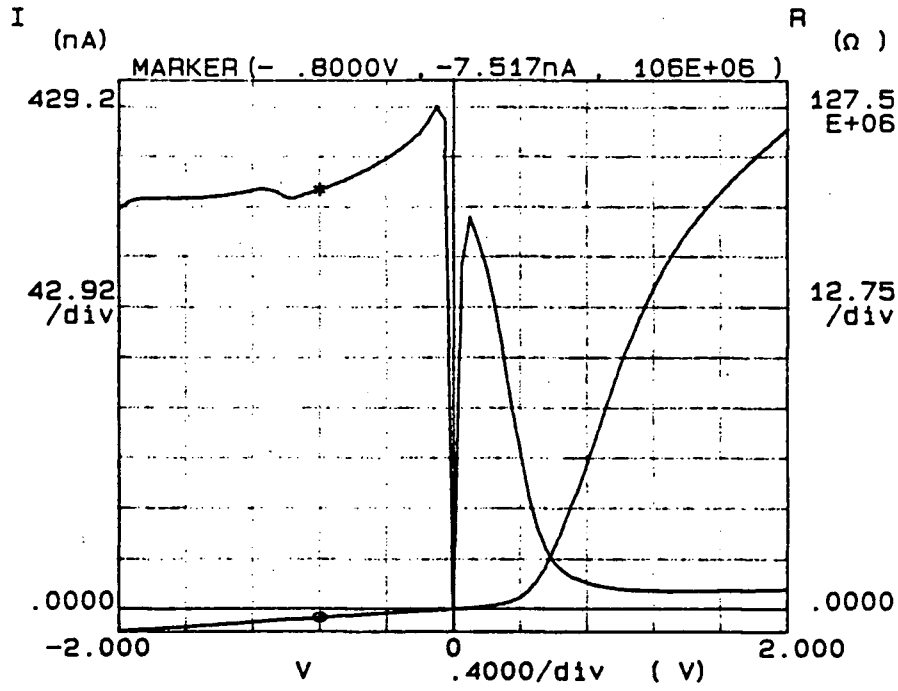


Fig. 8.6 Isolation monitor chip 5

leakage are the two most critical performance aspects of isolation.

8.7.2 DOPING AND MOBILITY PROFILES

Using the fat FET at grid position K-1 of figure 1.3 on test chip 8 the doping and mobility profiles of figures 8.7 and 8.8 are obtained. The Nminus implant for this run was a dose of $3 \cdot 10^{12}$ ions/cm² at 125keV. The peak depth is about 103nm with an activated dose of $2.6 \cdot 10_{12}$ ions/cm² or about 87%. This is higher than the design simulation calculation assumption of 60% activation representing a 45% increase for the SI process, however annealing is performed at a lower temperature for the RSAG process which may result in

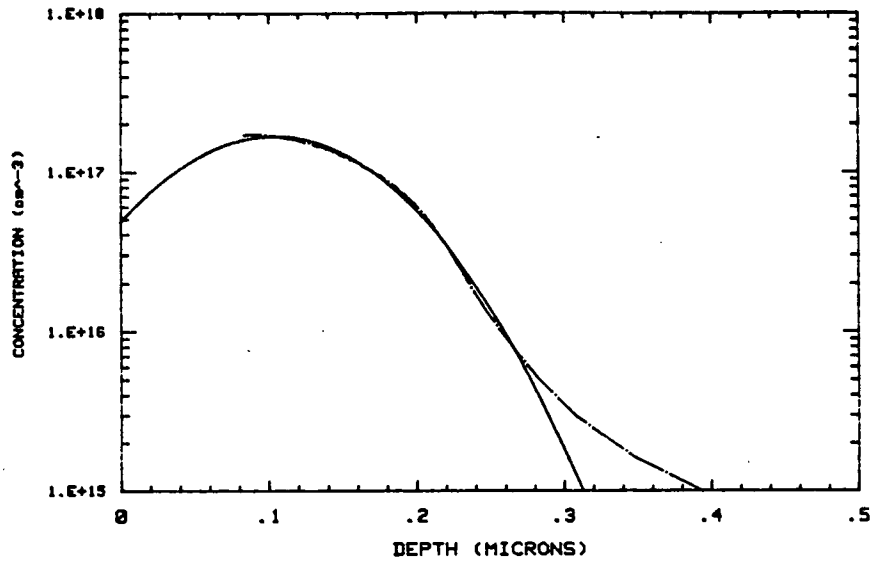


Fig. 8.7 SI doping profile.

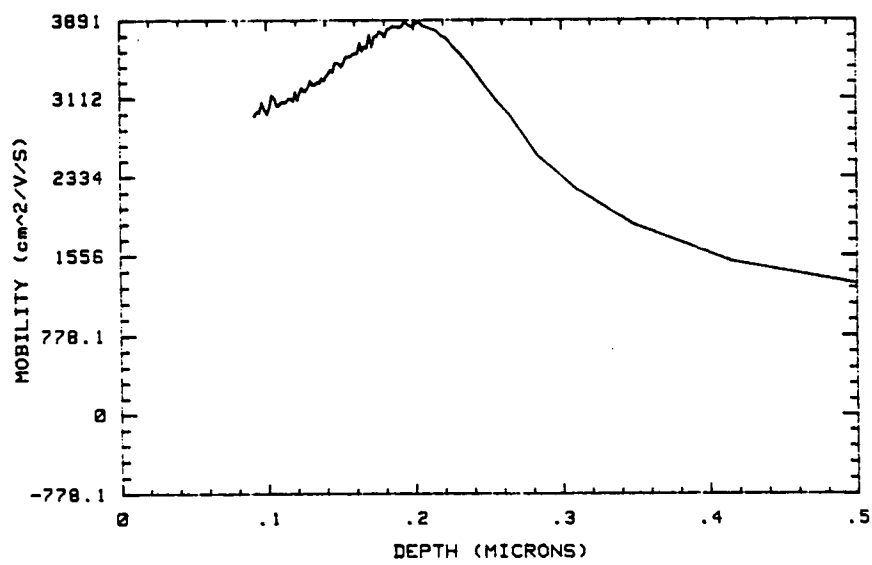
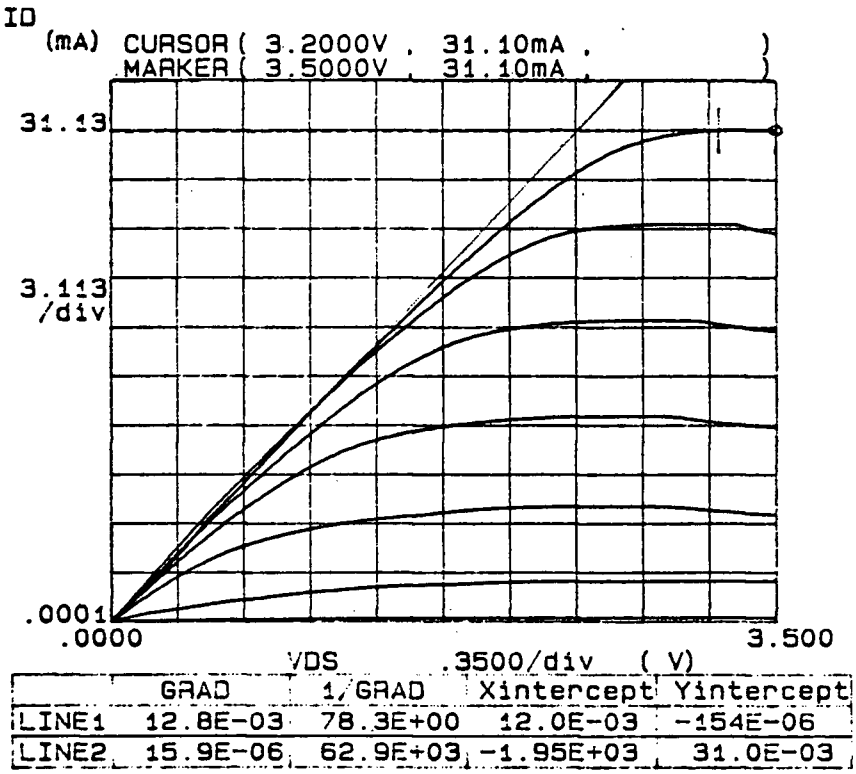


Fig. 8.8 SI mobility profile.

lower activation. Mobility is close to the assumed value of 3500 $cm^2/V\text{-}s$.

8.7.3 SI MESFET CHARACTERISTICS

The measured I-V characteristics of figures 8.9 and 8.10 are 236μm width π-gate MESFETs for which industry specifications are available. Three versions of this device are present on each chip, corresponding to source/drain gaps of 2, 3 and 4μm. The published device



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	12.8E-03	78.3E+00	12.0E-03	-154E-06
LINE2	15.9E-06	62.9E+03	-1.95E+03	31.0E-03

Fig. 8.9 SF_236_1_4 π-gate I-V characteristics, $V_T \simeq -2.7V$, $I_{DSS} \simeq 30mA$

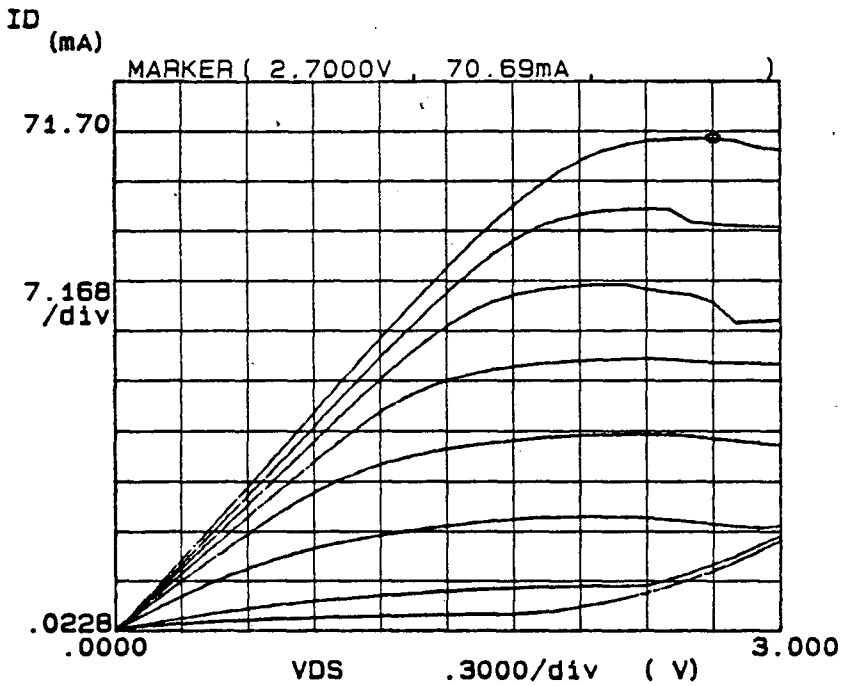


Fig. 8.10 SF_236_1_2 π-gate I-V characteristics, $V_T \simeq -3.7V$, $I_{DSS} \simeq 70mA$

specifications of manufacturers have a V_T and I_{DSS} tolerance typically ranging from -4 to -2V and 30 to 70mA respectively. The measured characteristics of our SI devices are in this range.

9. CONCLUSION

Sample and hold cycles, with ideal switch strobe pulses, indicate a single gate 0.5μm MESFET switch integrated sampling amplifier block will have the best input time constant, and likely be the only unit, at this level of lithography, capable of successful operation with 25ps pulses.

The mechanisms by which MESFET switch guard gates affect sample and hold switch operation have been demonstrated by simulation. Strobe pulse feedthrough is reduced by momentary forward conduction of the guard gate, allowing displaced carriers to tunnel out of the switch channel. The number of carriers involved in the tunneling action is guard gate bias and signal level sensitive causing some distortion of the output signal. The input time constant increases, due to the extra guard channels in series, is in the order of 30 to 40% when using a reduction of hold node capacitance.

The applicability of the GaAs RSAG process to sample and hold switch design has been verified by a multiple gate slice simulation, indicating in the order of 5ps gate center tap to gate end delay for a 30μm width t-gate.

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10. APPENDIX A -ICDL SIMULATIONS

10.1 DIGITAL INTEGRATED CIRCUIT SIMULATION OVERVIEW

Inverted common drain logic (ICDL), was modeled comparatively to other GaAs MESFET logics. ICDL is a new logic circuit configuration developed by Abdel-Motaleb[4.17] in which the logic functions are realized using the pullup rather than the pulldowm transistors which are normally used. Depletion ("normally on") transistors are employed. The basic switching modes and the advantages and problems are discussed. Simulations were done using both the JFET and the Sussman-Fort MESFET models in SPICE. Experimental results were first simulated using parametric data obtained from measurements. In order to attempt to compare performance with some well established logic approaches, these were simulated using the same parametric data for all the logics.

Depletion transistors (which conduct for $V_{GS} = 0$) were used in the first GaAs logic circuits because of the problems of fabricating enhancement type devices with sufficiently controlled threshold voltages and low enough series resistances (R_S and R_D). In the BFL (buffered FET logic) approach, logic functions are achieved, as shown in Fig. 10.1(a), using combinations of pulldown depletion transistors. This is the same, for example, as in silicon MOSFET DCFL (direct coupled FET logic) which uses enhancement devices (which are OFF for $V_{GS} = 0$), except that

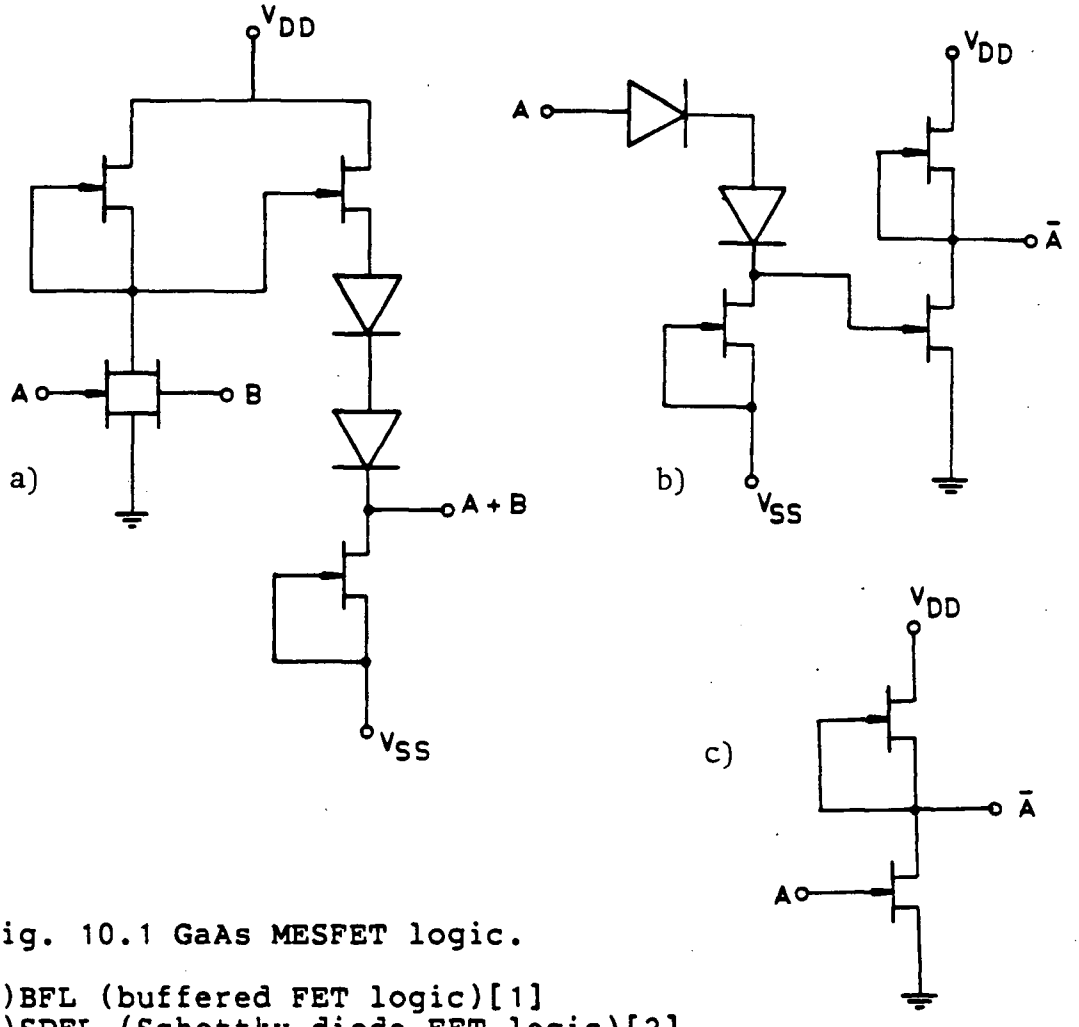


Fig. 10.1 GaAs MESFET logic.

a)BFL (buffered FET logic)[1]
b)SDFL (Schottky diode FET logic)[2]
c)DCFL (direct coupled FET logic)[3]

the output must be level-shifted before presentation to the next stage, since a negative gate voltage (with respect to the source) is required to turn off the depletion pulldown transistors. The level shifting is achieved using Schottky diodes. In SDFL (Schottky diode FET logic, Fig. 10.1(b)) the inputs are combined using diodes.

Eventually, it is commonly believed, VLSI using GaAs will be achieved by using enhancement pulldown devices [3]

and DCFL (Fig. 10.1(c)). The required threshold voltage and low series resistances may be obtained using a self-aligned gate technology [4-8] (once the ion implantation and activation process is better controlled) or else some form of etched recessed gate [9]. For the present we restrict ourselves, however, to depletion type transistors to form the logic and consider what advantages (or otherwise) may be obtained by, so to speak, turning the logic upside down by using the pullup transistors to form the logic with pulldown transistors acting as loads. The idea of doing this seems an obvious one, but there is surprisingly little previous consideration of it in the literature. Of what we could find, the most significant was the work of Nuzillat et al. [8,9].

10.2 ICDL BASIC CIRCUITS

The basic gates for ICDL [10] are assembled in Fig. 10.2 and are first briefly listed before discussion in later sections. The first (Fig. 10.2(a) is a non-inverting buffer. This buffer was proposed previously by Hartgring et al. [11] for use in connection with dynamic silicon MESFET logic. An inverter is needed and requires a second power supply V_{SS} for level shifting between stages. The inverter considered, Fig. 10.2(b), differs from the SDFL inverter, Fig. 10.1(c), in using an ion implanted, non-velocity saturating, resistor in place of diodes for level shifting. The buffered form of the inverter, with high input impedance, is actually the version most needed, and this is shown in Fig. 10.2(c). The AND gate is in Fig. 10.2(d) and the OR gate in Fig. 10.2(e), with possible complex gate configurations in Fig. 10.2(f) and (g). A similar inverted OR gate was previously listed by Nuzillat et al. in connection with their quasi-normally-off logic. Our logic gate differs by not having a diode between the pullup transistors and the pulldown load and also by using a transistor instead of a resistive load. Also Nuzillat et al. were specifically studying quasi-normally-off devices with small threshold voltages (either positive or negative) whereas we are considering depletion transistors. With this constraint Nuzillat et al. were able to require only one positive supply. In ICDL a supply rail is necessary to accommodate medium to large negative threshold voltages. ICDL differs from the SDFL

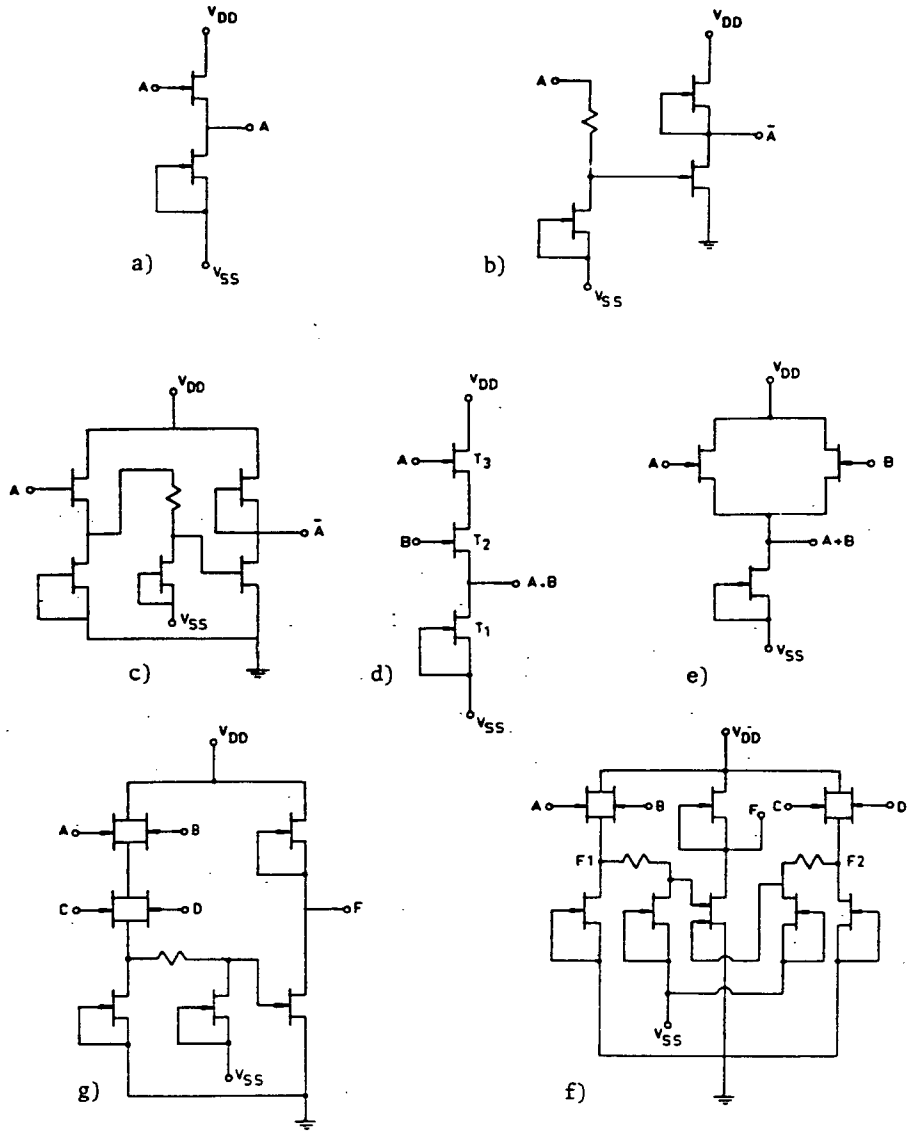


Fig. 10.2 ICDL configurations:

a)buffer, b)inverter, c)buffered inverter,
d)AND, e)OR, f)$F = \overline{F1 \cdot F2} = \overline{(A+B)} \cdot \overline{(C+D)}$
g)$F = \overline{(A+B) \cdot (C+D)}$

configuration not only in the use of a resistor as voltage translator, but in the use of the inverted logic as input buffer. Similarly ICDL differs from the BFL configuration by removing the voltage translation mechanism from the output path.

10.3 BUFFER CIRCUIT

Load line plots for the buffer are given in Fig. 10.3(a) to show how the logic levels are obtained. The I_{DS} vs V_{DS} characteristics are here plotted for constant

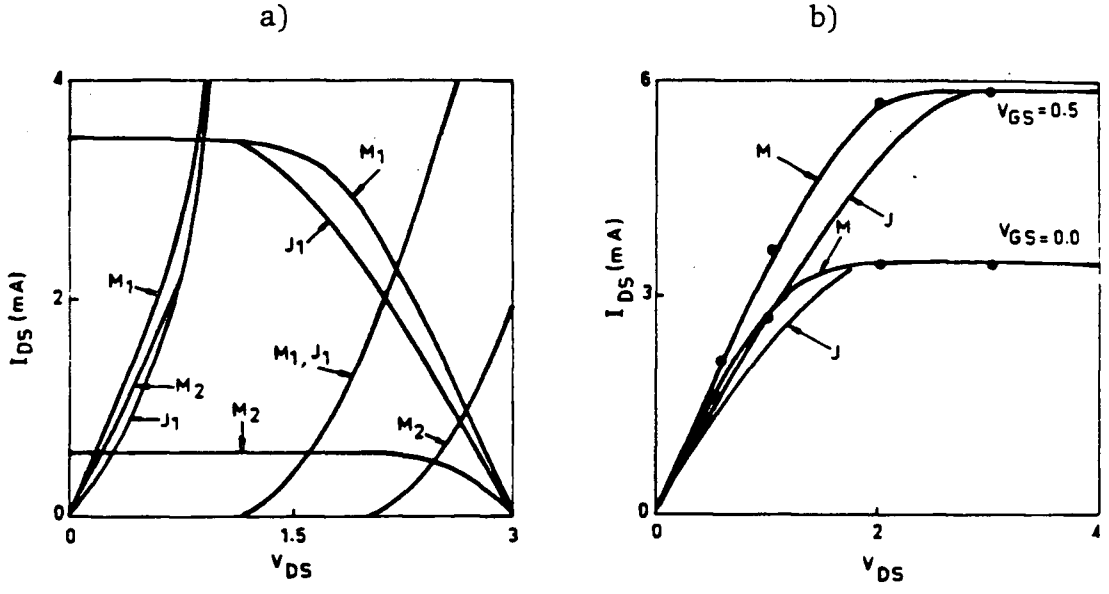


Fig. 10.3 Inverted buffer loadline with V_{DD}=3V, V_{SS}=0V, V_{GD}=0 and -2.5 V for the switching transistor corresponding to a high and low logic input, with measured vs. model JFET and MESFET characteristics in (b) for (M_1) and (J_1) in (a).

a) MESFET Model (M_1), JFET Model (J_1) where V_T = -1.37 V and MESFET Model (M_2) where V_T = -0.5 V
b) Comparison of the JFET(J) and MESFET(M) models vs. experimental(·) data: I_D vs. V_{DS} for V_{GS} = -0.5 and 0.0 V

V_{DS} instead of the usual constant V_{GS} needed for conventional FET logic. Using the common approximation for I_{DS} below saturation $I_{DS} = 2\beta((V_{GS} - V_T)V_{DS} - V_{DS}^2/2)$ we can use $V_{GS} = V_{DS} + V_{GD}$ to obtain the form we need $I_{DS} = 2\beta((V_{GD} - V_T)\ V_{DS} + V_{DS}^2/2)$. Here $I_{DS} > 0$ if $V_{GD} - V_T + V_{DS}/2 > 0$. Above saturation, instead of the usual $I_{DS} = \beta(V_{GS} - V_T)^2$ we obtain $I_{DS} = \beta(V_{DS} + V_{GD} - V_T)^2$. For a high input (ie small V_{GD}) V_{DS} for the switching transistor is small so that the output is high. For a low input (V_{GD} large and negative) V_{DS} is large so that the output is low. The load line plotted on these drain current characteristics for constant V_{GD} is the pulldown depletion transistor characteristic for its $V_{GS} = 0$. In Fig. 10.3(a) the JFET SPICE model [12] (which employs the above approximate characteristics) has been used and, also, an improved model due to Sussman-Fort et al. [13] following criticisms and proposed improvement of the JFET model by Curtice [14]. The chief differences are the use of a better representation of I_{DS} in the triode region as shown in Fig. 10.3(b) and the introduction of a gate transit time delay. The difference in representation of I_{DS} shows up in Fig. 10.3(a) but is more important in considering transients.

From Fig. 10.3(a) it is apparent that with a larger magnitude V_T the supply voltage needs to be larger to get good $V_T = -1.37$ (M_1), $V_T = -0.5$ (M_2)
'> separation of the logic levels. This appears again in Fig. 10.4(a) and (b) which shows the simulated transfer

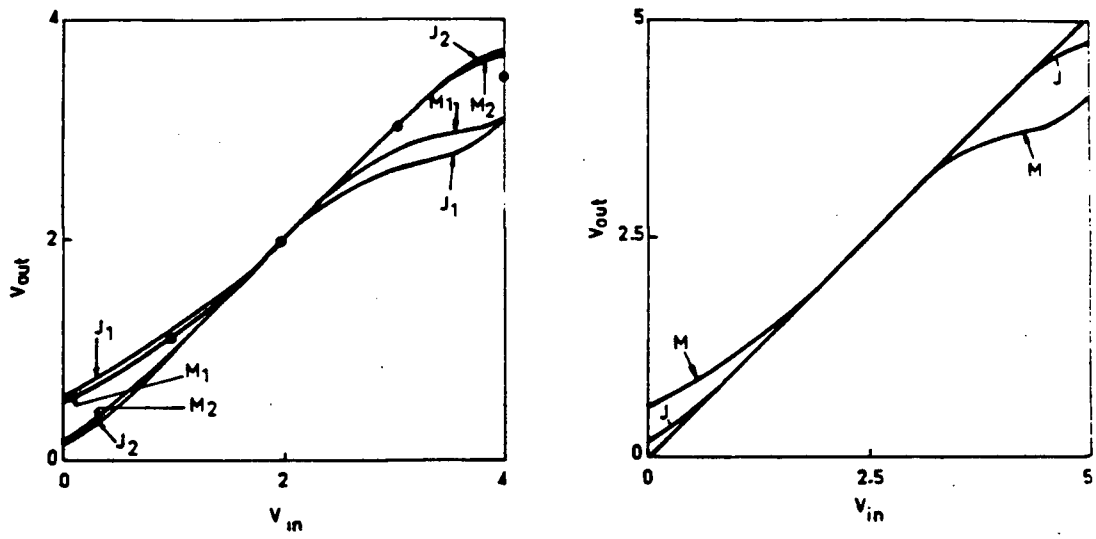
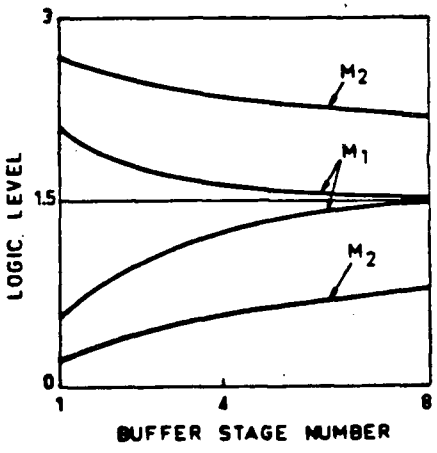


Fig. 10.4 Buffer transfer.

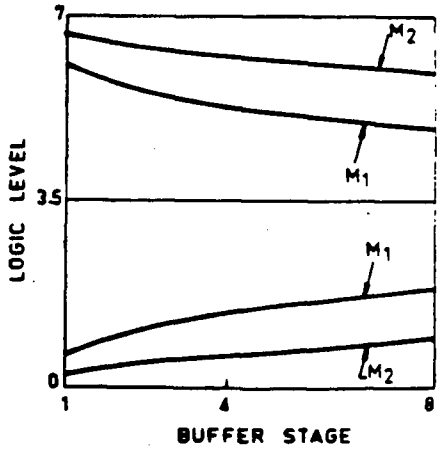
a)MESFET(M) vs. JFET(J): V_{DD} = 3 V, V_T = -1.37 (M_1, J_1), V_T = -0.5 (M_2, J_2)
b)MESFET(M) vs. JFET(J): V_T = -1.37, V_{DD} = 7 V

characteristic (V_{out} vs V_{in}) for different V_T and supply voltages V_{DD} using both JFET and MESFET models.

A computer simulation of the voltage transfer characteristics of the buffer, using the JFET and MESFET models, is shown in Fig. 10.4(a) and (b).The MESFET model is employed for simulation in Fig. 10.4(c) and (d). In Fig. 10.4(a) and (b) the switching and load transistors are identical. The voltage gain dV_{out}/dV_{in} for a single stage is close to 1 over a certain range for a choice of supply voltage scaled with device parameters (Fig. 10.4(b)). The simulation of several stages shown in Fig. 5(c) and (d) shows that the logic high and low levels saturate at about



c)



d)

Fig. 10.4
c)Logic levels as a function of sequential stages where: V_{DD} = 3,
d)Logic levels as a function of sequential buffer stages where: V_{DD} = 7, V_T = -1.37 (M_1), V_T = -0.5 (M_2)

V_{DD} - $|V_T|$ and at $|V_T|$ respectively.

10.4 INVERTER

The transistors for pullup and pulldown in the buffer will show process variations. Also as shown in Fig. 10.4(b) and (d) for a threshold voltage of a certain magnitude a sufficient supply voltage is needed to get well distinguished logic levels. Hence the logic levels may be lost after a few stages under certain adverse conditions. This indicated that an inverter with voltage gain greater than unity is required to regenerate the original values of the logic levels.

The proposed inverter, shown in Fig. 10.2(b), consists of a level shifter stage and an output stage which acts like a conventional ratioed logic inverter. The use of a resistor in place of the diodes, for example as used in the SDFL inverter, was chosen because it appeared to be easier to fabricate, since the diodes are required to be small and very accurate due to the need for reproducible current voltage characteristics. The resistance of the ion implanted resistor can be varied by varying the dose rather than the dimensions (which requires a different mask set). If small diodes of exact area are used to obtain strain on the photolithography. If, instead, a series combination of larger diodes is used (as in BFL, for example) then more space and power are consumed.

When replacing the diode stack with a resistor the I-V curves must coincide for the critical switching region quiescent condition to give the same DC transfer characteristics. The resistor is chosen by plotting resistance versus output voltage for a resistor input voltage in the center of the logic swing as shown in Fig. 10.5. When the input and output voltages are equal at the logic midpoint a symmetrical transfer characteristic is obtained. For the case in Fig. 10.5(a) and (b) this occurs at approximately 2.5 and 0.63 kohm respectively.

Using the criterion of equal current for a given voltage drop at the logic midpoint for the diode stack and resistor, the diode stack diode number and area can be

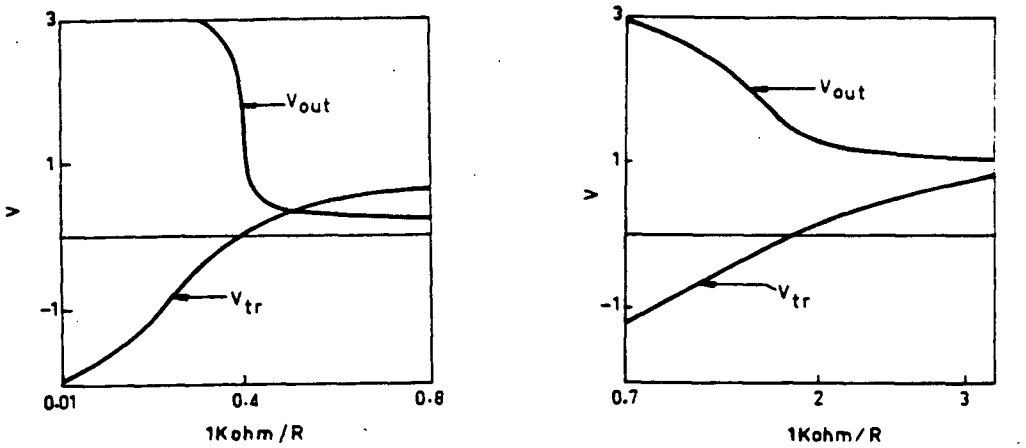


Fig. 10.5 Inverter output voltage vs. reciprocal of the voltage translator resistor value with fixed input voltage at $(V_{OH} - V_{OL})/2 + V_{OL}$, where V_{OH} = 3 V and V_{OL} = 0.2 V.

a) V_T = -0.5 V, V_{DD} = 3 V, V_{SS} = -2 V
b) V_T = -1.37 V, V_{DD} = 3 V, V_{SS} = -2 V

determined once average diode process constants are known. For the case in Fig. 10.5(a) the voltage drop across the resistor is 1.6 V and the current 0.64 mA. If the diode process is fixed only the number of diodes, the area, and the supply voltages can be changed. Assuming the same supply rails, and average diode process constants from reference [7], a two diode stack would be necessary to provide the voltage drop, which if equal in area would consume 1 μm^2 per diode, for a symmetrical transfer characteristic. The I-V characteristics of the resistor and diode stack are shown in Fig. 10.6. In the low input logic state the inverter with diodes dissipates about 85% less power and in the high input logic state, (assuming the inverter input peaks at 2 volts)

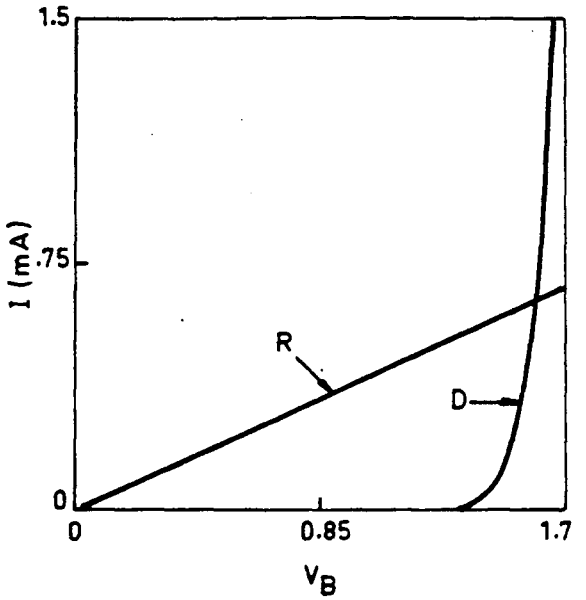


Fig. 10.6 I-V plots for translator resistor and diode stack.

dissipates about the same amount of power. However, if the inverter input rises to the supply rail, 3 volts, the diode circuit dissipates about five times more power than the resistor circuit.

The difference in dynamic behavior thereafter depends on the diode stack non-linearity. The simulated relative dynamic performance for the case under consideration is shown in Fig. 10.7. The diode stack circuit is predictably faster in the high to low transition, due to the diode stack current nonlinearity, but approximately equivalent to the resistor circuit in the low to high transition, where the depletion load must remove the accumulated charge. Thus, although the resistor circuit is slower on the down transition, it is delay symmetric making it a less complex timing design problem for large interactive systems, and it poses a less critical power consumption problem for logic

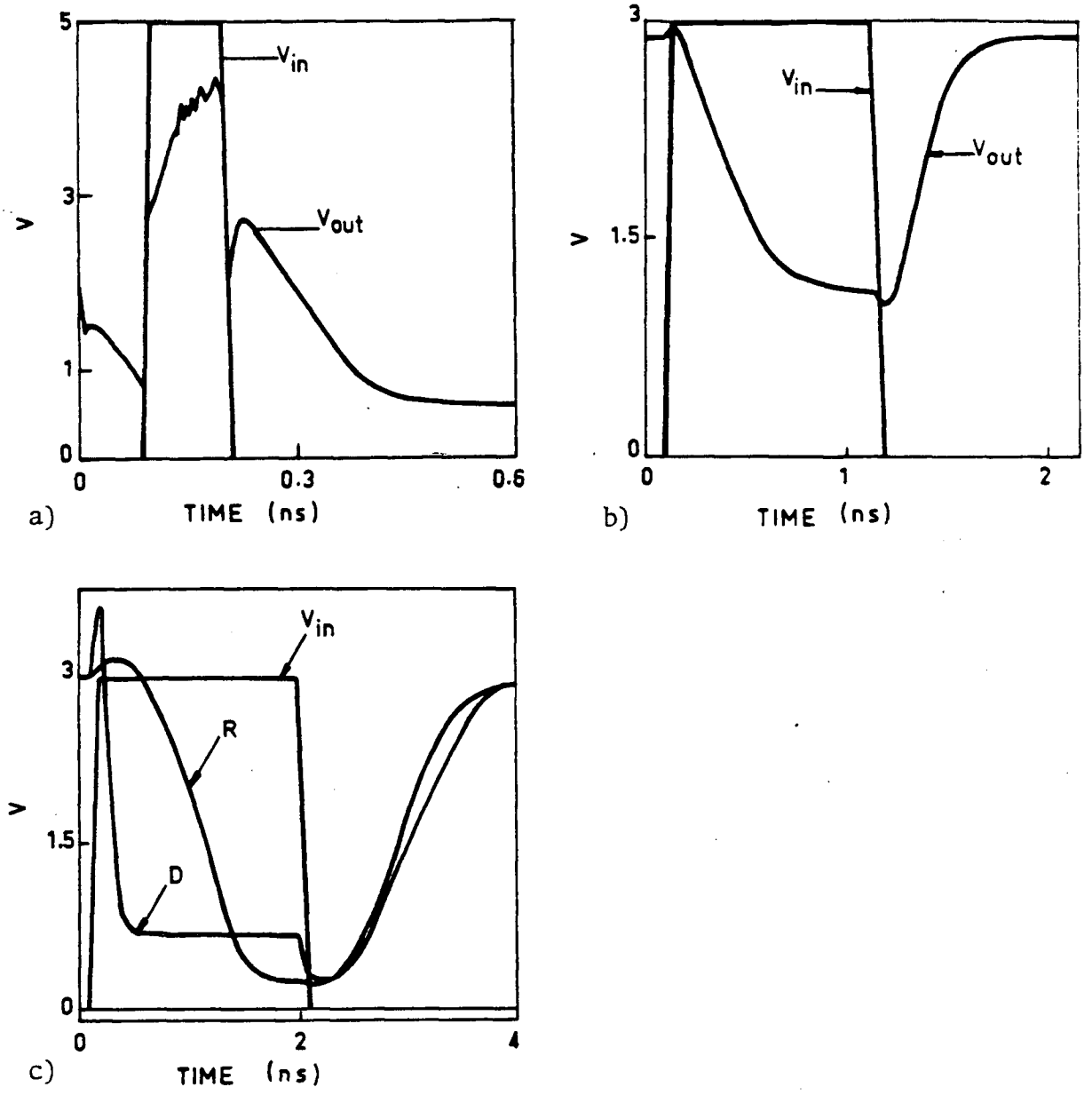


Fig. 10.7 Pulse response of buffer and inverter.

a) Buffer :V_{DD} = 5 V with one buffer load.
b) Inverter, R = 629 Ω, V_{DD} = 3 V, V_{SS} = -2 V, with one buffer load.
c) Inverter comparison, diode stack vs. resistor version, V_T = -0.5V, no load.

high inputs.

10.5 BUFFERED INVERTER

The ICDL inverter turns out to give a rather low fan-in and fan-out, similar to the case with SDFL, a large current must be driven into the next stage. This problem can be overcome if the buffer circuit or appropriate logic block is added as shown in Fig. 10.2(c). The sizing of the buffer transistors must account for the DC load, power dissipation, and dynamic considerations with respect to the inverter.

10.6 OR GATE

The operation of the OR logic follows from the discussion of the buffer with degraded dynamic performance due to the added capacitance.

10.7 AND GATE

The positive logic AND as shown in Fig. 10.2(d) suffers from a severe limitation not present for MISFET circuits. For logic high inputs forward current will flow through the Schottky diode gates of the input transistors when gate source voltage exceeds about 0.7V. The four possible input logic combination gate currents as a function of input voltage are shown in Fig. 10.8. The width of T_1 is taken as twice the width of T_2 and four times the width of T_3 to maintain a reasonable output swing for the voltage combinations that are acceptable before gate forward conduction sets in. The problem can be circumvented by using gates of the form of Fig. 10.2(g), instead. These are

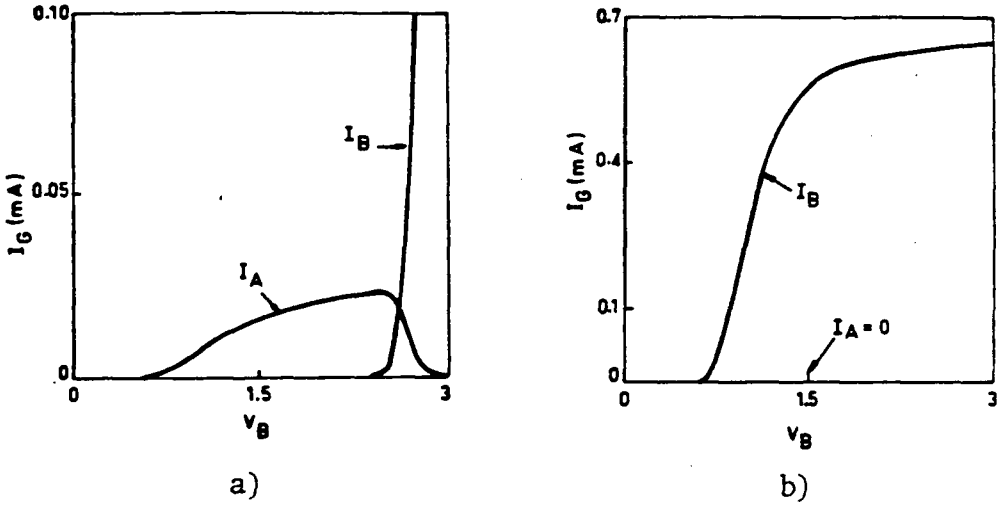


Fig. 10.8 Schottky diode gate current of transistors at inputs A and B of AND gate of Fig. (2) (d) as a result of fixed logic level on A with input voltage on B swept.

a)A high (V_{OH} = 3 V) B swept from 0 to 3 V.
b)A low (V_{OL} = 0.2 V) B swept from 0 to 3 V.

combinations of the logic OR of Fig. 10.2(e).

In summary, if a limited (0.5 V) logic swing is used, gates such as shown in Fig. 10.2(d) and (f) could be used. This would give lower power dissipation compared to Fig. 10.2(g), but probably at the expense of speed and reliability.

10.8 RESULTS AND THEIR SPICE SIMULATION

The measured parameters used for SPICE simulation for

experiment results matching are in Table 10.1.

Parameter	2um FET	Group 1	Group 2	Group 3
R_S Ω	68	100	200	400
R_D Ω	180	100	200	400
V_T	-1.37	-2.5	-1.0	-0.5 or 0
$\beta(A/V^2)$	$2.8 \cdot 10^{-3}$	$4.4 \cdot 10^{-4}$	$7 \cdot 10^{-4}$	1 or $1.4 \cdot 10^{-3}$
C_{GS} fF	100	5	5	5
C_{GD} fF	100	5	5	5

Table 10.1: Measured and Simulation MESFET parametric data. Simulation data adjusted from [20-23]. In Group 3 logic approaches designed for V_T = 0 or -0.5 V are considered, thus two values of β were used as listed, respectively. Capacitance and β for the measured data is total whereas for the parametric data it is per unit length.

As shown in Fig. 10.2(b) experimental characteristics were well fitted by the MESFET model both in the saturation and linear regions. The MESFET model successfully fits the whole DC characteristic better than the JFET model.

The measured and simulated DC characteristics of the buffer circuit and the inverter are shown in Fig. 10.4(b). Experimental results confirm the feasibility projected by the simulations. The small deviation between simulated and measured transfer characteristic for the buffer corresponds to the variation in the I_{DS} - V_{DS} characteristics of the transistors from the simulation values.

Simulated dynamic responses for the buffer and the inverter are given in Fig. 10.6. These were obtained neglecting parasitics due to interconnections. The justification for this is that these would depend on details

of layout and we are seeking the basic or intrinsic behavior of the circuit. The MESFET model simulated experimental buffer, using V_{DD} = 5 V, gave an average time delay of 105 ps for unity fanout with power dissipation (input held at the logic midpoint) of 18.7 mW, and power delay product of 1.96 pJ. The inverter gave an average delay of 550 ps using a buffer circuit as load with 22.2 mW dissipation and a power delay product of 12.2 pJ per gate.

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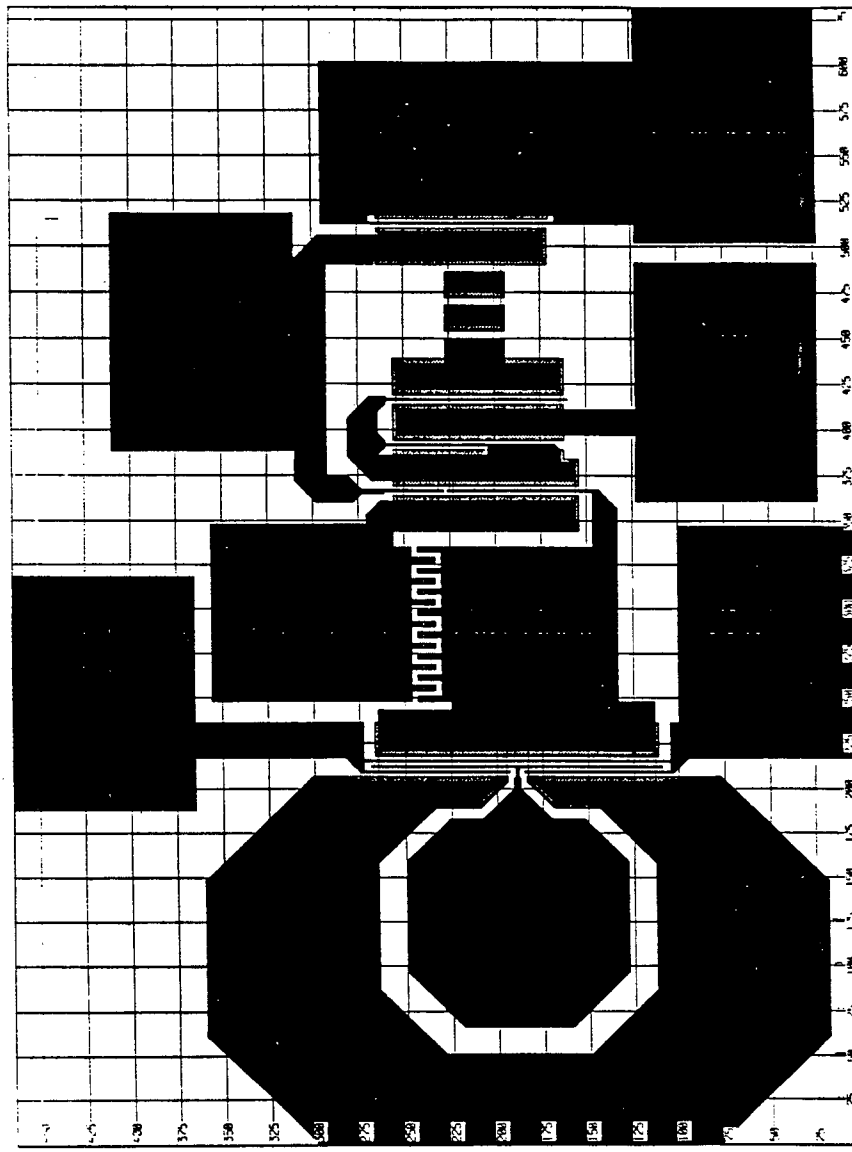
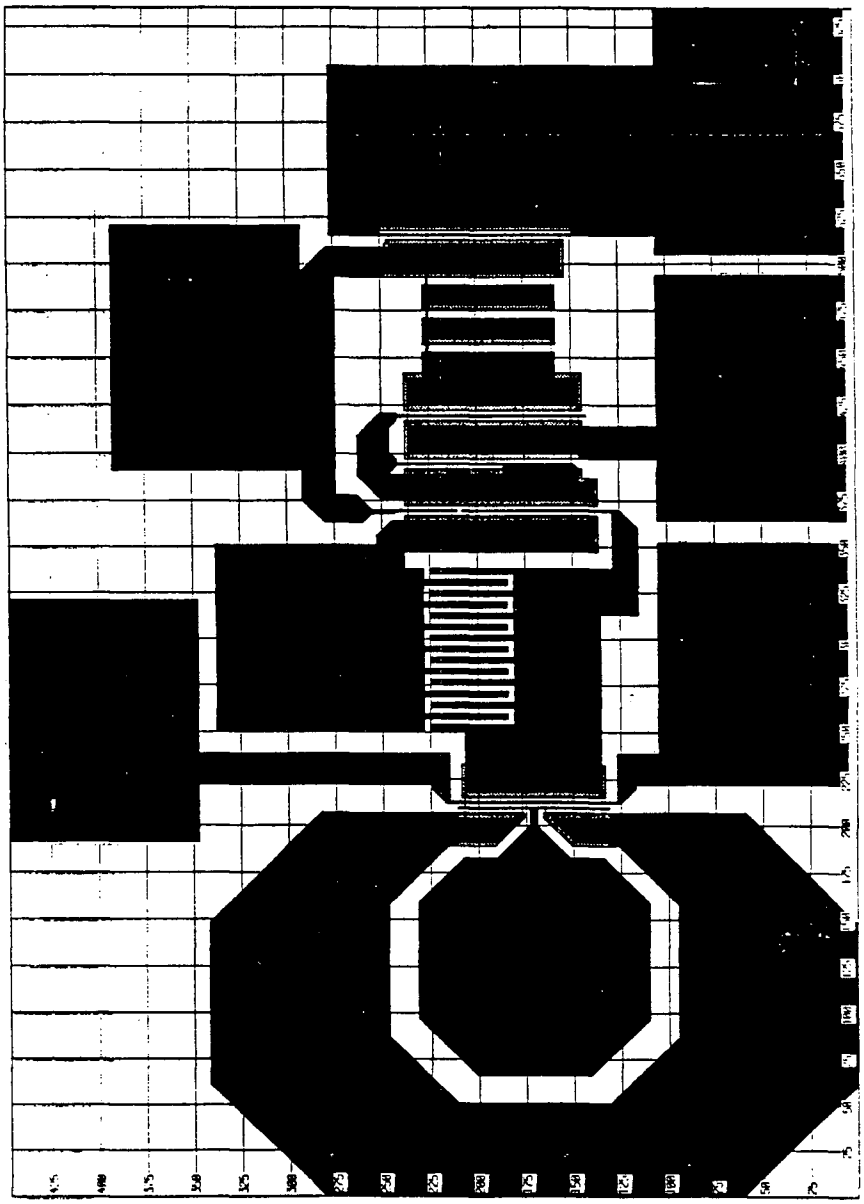
11. APPENDIX B -LAYOUTS



SI3S913T3 ISAB



RI26R912T3 ISAB

12. APPENDIX C -GASFET SUBROUTINE

```
      SUBROUTINE GASFET
      IMPLICIT REAL*8 (A-H,O-Z)
C
C     THIS ROUTINE PROCESSES GaAs MESFETS FOR DC AND
C     TRANSIENT ANALYSES.
C     BASED ON THE MODEL OF WALTER R. CURTICE
C     IEEE TRANS ON MICROWAVE THEORY AND TECHNIQUES
C     VOL MTT-28 NO. 5 MAY 1980
C
      COMMON /TABINF/IELMNT,ISBCKT,NSBCKT,IUNSAT,NUNSAT,ITEMPS,NUMTEM,
     1           ISENS,NSENS,IFOUR,NFOUR,IFIELD,ICODE,IDELIM,ICOLUM,INSIZE,
     2           JUNODE,LSBKPT,NUMBKP,IORDER,JMNODE,IUR,IUC,ILC,ILR,NUMOFF,ISR,
     3           NMOFFC,ISEQ,ISEQ1,NEQN,NODEVS,NDIAG,ISWAP,IEQUA,MACINS,LVNIM1,
     4           LX0,LVN,LYNL,LYU,LYL,LX1,LX2,LX3,LX4,LX5,LX6,LX7,LD0,LD1,LTD,
     5           IMYNL,IMVN,LCVN,NSNOD,NSMAT,NSVAL,ICNOD,ICMAT,ICVAL,
     6           LOUTPT,LPOL,LZER,IRSWPF,IRSWPR,ICSWPF,ICSWPR,IRPT,JCPT,
     7          IROWNO,JCOLNO,NTTBR,NTTAR,LVNTMP
      COMMON /CIRDAT/LOCATE(50),JELCNT(50),NUNODS,NCNODS,NUMNOD,NSTOP,
     1          NUT,NLT,NXTRM,NDIST,NTLIN,IBR,NUMVS
      COMMON /STATUS/OMEGA,TIME,DELTA,DELOLD(7),AG(7),VT,XNI,EGFET,
     1           XMU,MODE,MODEDC,ICALC,INITF,METHOD,IORD,MAXORD,NONCON,ITERNO,
     2           ITEMNO,NOSOLV,MODAC,IPIV,IVMFLG,IPOSTP,ISCRCH,IOFILE
      COMMON /KNSTNT/TWOPI,XLOG2,XLOG10,ROOT2,RAD,BOLTZ,CHARGE,CTOK,
     1           GMIN,RELTOL,ABSTOL,VNTOL,TRTOL,CHGTOL,EPS0,EPSSIL,EPSOX,
     2          PIVTOL,PIVREL
      COMMON /BLANK/ VALUE(200000)
      INTEGER NODPLC(64)
      COMPLEX * 16 CVALUE(32)
      EQUIVALENCE (VALUE(1),NODPLC(1),CVALUE(1))
C
C
      DIMENSION
VGSO(1),VGDO(1),CGO(1),CDO(1),CGDO(1),GMO(1),GDSO(1),
     1          GGSO(1),GGDO(1),QGS(1),CQGS(1),QGD(1),CQGD(1),
     2          QDS(1),CQDS(1),QTT(1),CQTT(1)
      EQUIVALENCE (VGSO(1),VALUE( 1)),(VGDO(1),VALUE( 2)),
     1          (CGO (1),VALUE( 3)),(CDO (1),VALUE( 4)),
     2          (CGDO(1),VALUE( 5)),(GMO (1),VALUE( 6)),
     3          (GDSO(1),VALUE( 7)),(GGSO(1),VALUE( 8)),
     4          (GGDO(1),VALUE( 9)),(QGS (1),VALUE(10)),
     5          (CQGS(1),VALUE(11)),(QGD (1),VALUE(12)),
     6          (CQGD(1),VALUE(13)),(QDS (1),VALUE(14)),
     7          (CQDS(1),VALUE(15)),(QTT (1),VALUE(16)),
     8          (CQTT(1),VALUE(17))
C
C
      LOC=LOCATE(16)
   10 IF (LOC.EQ.0) RETURN
      LOCV=NODPLC(LOC+1)
      NODE1=NODPLC(LOC+2)
      NODE2=NODPLC(LOC+3)
      NODE3=NODPLC(LOC+4)
      NODE4=NODPLC(LOC+5)
      NODE5=NODPLC(LOC+6)
      NODE6=NODPLC(LOC+25)
      LOCM=NODPLC(LOC+7)
      IOFF=NODPLC(LOC+8)
      TYPE=NODPLC(LOCM+2)
      LOCM=NODPLC(LOCM+1)
      LOCT=NODPLC(LOC+19)
C
C   DC MODEL PARAMETERS
C
```

```
      WIDTH=VALUE(LOCV+1)
      VTO=VALUE(LOCM+1)
      VBI=VALUE(LOCM+2)
C     GATE PARASITIC CONDUCTANCE: GGPR
      GGPR=VALUE(LOCM+3)*WIDTH
      ALPHA=VALUE(LOCM+4)
      BETA=VALUE(LOCM+5)*WIDTH
      XLAMB=VALUE(LOCM+6)
      CSAT=VALUE(LOCM+10)*WIDTH
C     DRAIN PARASITIC CONDUCTANCE: GDPR
      GDPR=VALUE(LOCM+11)*WIDTH
C     SOURCE PARASITIC CONDUCTANCE: GSPR
      GSPR=VALUE(LOCM+12)*WIDTH
      TAU=VALUE(LOCM+13)
      VCRIT=VALUE(LOCM+14)
C
C   INITIALIZATION
C
      ICHECK=1
      GO TO (100,20,30,50,60,70), INITF
   20 IF(MODE.NE.1.OR.MODEDC.NE.2.OR.NOSOLV.EQ.0) GO TO 25
      VDS=TYPE*VALUE(LOCV+2)
      VGS=TYPE*VALUE(LOCV+3)
      VGD=VGS-VDS
      GO TO 300
   25 IF(IOFF.NE.0) GO TO 40
      VGS=-1.0D0
      VGD=-1.0D0
      GO TO 300
   30 IF (IOFF.EQ.0) GO TO 100
   40 VGS=0.0D0
      VGD=0.0D0
      GO TO 300
   50 VGS=VGSO(LX0+LOCT)
      VGD=VGDO(LX0+LOCT)
      GO TO 300
   60 VGS=VGSO(LX1+LOCT)
      VGD=VGDO(LX1+LOCT)
      GO TO 300
   70 XFACT=DELTA/DELOLD(2)
      VGSO(LX0+LOCT)=VGSO(LX1+LOCT)
      VGS=(1.0D0+XFACT)*VGSO(LX1+LOCT)-XFACT*VGSO(LX2+LOCT)
      VGDO(LX0+LOCT)=VGDO(LX1+LOCT)
      VGD=(1.0D0+XFACT)*VGDO(LX1+LOCT)-XFACT*VGDO(LX2+LOCT)
      CGO(LX0+LOCT)=CGO(LX1+LOCT)
      CDO(LX0+LOCT)=CDO(LX1+LOCT)
      CGDO(LX0+LOCT)=CGDO(LX1+LOCT)
      GMO(LX0+LOCT)=GMO(LX1+LOCT)
      GDSO(LX0+LOCT)=GDSO(LX1+LOCT)
      GGSO(LX0+LOCT)=GGSO(LX1+LOCT)
      GGDO(LX0+LOCT)=GGDO(LX1+LOCT)
      GO TO 110
C
C   COMPUTE NEW NONLINEAR BRANCH VOLTAGES
C
  100 VGS=TYPE*(VALUE(LVNIM1+NODE6)-VALUE(LVNIM1+NODE5))
      VGD=TYPE*(VALUE(LVNIM1+NODE6)-VALUE(LVNIM1+NODE4))
  110 DELVGS=VGS-VGSO(LX0+LOCT)
      DELVGD=VGD-VGDO(LX0+LOCT)
      DELVDS=DELVGS-DELVGD

CGHAT=CGO(LX0+LOCT)+GGDO(LX0+LOCT)*DELVGD+GGSO(LX0+LOCT)*DELVGS

CDHAT=CDO(LX0+LOCT)+GMO(LX0+LOCT)*DELVGS+GDSO(LX0+LOCT)*DELVDS
     1           -GGDO(LX0+LOCT)*DELVGD
```

```
C
C  BYPASS IF SOLUTION HAS NOT CHANGED
C
      IF (INITF.EQ.6) GO TO 200
      TOL=RELTOL*DMAX1(DABS(VGS),DABS(VGSO(LX0+LOCT)))+VNTOL
      IF (DABS(DELVGS).GE.TOL) GO TO 200
      TOL=RELTOL*DMAX1(DABS(VGD),DABS(VGDO(LX0+LOCT)))+VNTOL
      IF (DABS(DELVGD).GE.TOL) GO TO 200
      TOL=RELTOL*DMAX1(DABS(CGHAT),DABS(CGO(LX0+LOCT)))+ABSTOL
      IF (DABS(CGHAT-CGO(LX0+LOCT)).GE.TOL) GO TO 200
      TOL=RELTOL*DMAX1(DABS(CDHAT),DABS(CDO(LX0+LOCT)))+ABSTOL
      IF (DABS(CDHAT-CDO(LX0+LOCT)).GE.TOL) GO TO 200
      VGS=VGSO(LX0+LOCT)
      VGD=VGDO(LX0+LOCT)
      VDS=VGS-VGD
      CG=CGO(LX0+LOCT)
      CD=CDO(LX0+LOCT)
      CGD=CGDO(LX0+LOCT)
      GM=GMO(LX0+LOCT)
      GDS=GDSO(LX0+LOCT)
      GGS=GGSO(LX0+LOCT)
      GGD=GGDO(LX0+LOCT)
      GO TO 900
C
C  LIMIT NONLINEAR BRANCH VOLTAGES
C
  200 ICHK1=1
      CALL PNJLIM(VGS,VGSO(LX0+LOCT),VT,VCRIT,ICHECK)
      CALL PNJLIM(VGD,VGDO(LX0+LOCT),VT,VCRIT,ICHK1)
      IF (ICHK1.EQ.1) ICHECK=1
      CALL FETLIM(VGS,VGSO(LX0+LOCT),VTO)
      CALL FETLIM(VGD,VGDO(LX0+LOCT),VTO)
C
C  DETERMINE DC CURRENT AND DERIVATIVES
C
  300 VDS=VGS-VGD
      IF(VGS.GT.-5.0D0*VT) THEN
      EVGS=DEXP(VGS/VT)
      GGS=CSAT*EVGS/VT+GMIN
      CG=CSAT*(EVGS-1.0D0)+GMIN*VGS
      ELSE
      GGS=-CSAT/VGS+GMIN
      CG=GGS*VGS
      END IF
C       IF(VGD.GT.-5.0D0*VT) THEN
C       EVGD=DEXP(VGD/VT)
C       GGD=CSAT*EVGD/VT+GMIN
C       CGD=CSAT*(EVGD-1.0D0)+GMIN*VGD
C       ELSE
C       GGD=-CSAT/VGD+GMIN
C       CGD=GGD*VGD
C       END IF
       GGD=GMIN
       CGD=0.0D0
      CG=CG+CGD
C
C  COMPUTE DRAIN CURRENT AND DERIVITIVES
C
       IF(VDS.GE.0) THEN
C      NORMAL MODE
       VGST=VGS-VTO
     IF(VGST.LE.0) THEN
C
C    CUT-OFF SUBTHRESHOLD EFFECTS NOT INCLUDED
C
```

```
      CDRAIN=0.0D0
      GM=0.0D0
      GDS=0.0D0
      ELSE
C      LINEAR AND SATURATION REGION
       BETAP=BETA*(1.0D0+XLAMB*VDS)
       TWOB=BETAP+BETAP
       CDRAIN=BETAP*VGST*VGST*DTANH(ALPHA*VDS)
       GM=TWOB*VGST*DTANH(ALPHA*VDS)
       GDS=XLAMB*BETA*VGST*VGST*DTANH(ALPHA*VDS)+
      1            (BETAP*VGST*VGST*ALPHA*(1.0D0-
      2            (DTANH(ALPHA*VDS)*DTANH(ALPHA*VDS))))
      END IF
        ELSE
C       INVERSE MODE
        VGDT=VGD-VTO
      IF(VGDT.LE.0) THEN
C     CUT-OFF
      CDRAIN=0.0D0
      GM=0.0D0
      GDS=0.0D0
      ELSE
C     LINEAR AND SATURATION REGION
      BETAP=BETA*(1.0D0-XLAMB*VDS)
      TWOB=BETAP+BETAP
C
      CDRAIN=BETAP*VGDT*VGDT*DTANH(ALPHA*VDS)
      GM=-TWOB*VGDT*DTANH(ALPHA*VDS)
        GDS=-XLAMB*BETA*VGDT*VGDT*DTANH(ALPHA*VDS)+
      1           (BETAP*VGDT*VGDT*ALPHA*(1.0D0-
      2           (DTANH(ALPHA*VDS)*DTANH(ALPHA*VDS))))
      END IF
        END IF
C
C
C  COMPUTE EQUIVALENT DRAIN CURRENT SOURCE
C
       CD=CDRAIN-CGD
       IF (MODE.NE.1) GO TO 500
       IF ((MODEDC.EQ.2).AND.(NOSOLV.NE.0)) GO TO 500
       IF (INITF.EQ.4) GO TO 500
       GO TO 700
C
C  CHARGE STORAGE ELEMENTS
C
  500 CZGS=VALUE(LOCM+7)*WIDTH
      CZGD=VALUE(LOCM+8)*WIDTH
      CZDS=VALUE(LOCM+9)*WIDTH
      TWOP=VBI+VBI
C
C  IF VGS APPROACHES VBI NON ZERO CAPGS GOES TO INFINITY
C  VBI IS SCHOTTKY BARRIER JCT. PLUS 0.5V DUE TO DROP
C  IN CONDUCTION CHANNEL UNDER GATE
C
      SARG=DSQRT(1.0D0-VGS/VBI)
      QGS(LX0+LOCT)=TWOP*CZGS*(1.0D0-SARG)
      CAPGS=CZGS/SARG
      QGD(LX0+LOCT)=CZGD*VGD
C
C  GATE DRAIN CAPACITANCE HAS BEEN MODIFIED
C  TO THAT BELOW.
C  VDS AND VGS INCORPORATED FOR AC AND TRANSIENT ANALYSIS
C  ADAPTED FROM THE PAPER BY GOLIO ET AL.
C  IEEE CIRCUITS AND DEVICES MAGAZINE SEPTEMBER 1985 P 21.
C  VBI ASSUMED TO BE PHIG + CHANNEL DROP(0.5)
```

```
C
      CAPGD=(CZGD*(1.0D0-6.0D-1*VGS))/((1.0D0-(1.23D0*VGS-VDS)/
     1          (1.23D0*(VBI-5.0D-1)))*6.6D-1)
      QDS(LX0+LOCT)=CZDS*VDS
      CAPDS=CZDS
C
C  QTT IS CHARGE TRANSPORTED UNDER GATE IN TIME TAU
C
      QTT(LX0+LOCT)=TAU*CDRAIN
      CAPTT=TAU*GM
C
C  STORE SMALL-SIGNAL PARAMETERS
C
  560 IF ((MODE.EQ.1).AND.(MODEDC.EQ.2).AND.(NOSOLV.NE.0))
      GO TO 700
      IF (INITF.NE.4) GO TO 600
      VALUE(LX0+LOCT+9)=CAPGS
      VALUE(LX0+LOCT+11)=CAPGD
      VALUE(LX0+LOCT+13)=CAPDS
      VALUE(LX0+LOCT+15)=CAPTT
      GO TO 1000
C
C  TRANSIENT ANALYSIS
C
  600 IF (INITF.NE.5) GO TO 610
      QGS(LX1+LOCT)=QGS(LX0+LOCT)
      QGD(LX1+LOCT)=QGD(LX0+LOCT)
      QDS(LX1+LOCT)=QDS(LX0+LOCT)
      QTT(LX1+LOCT)=QTT(LX0+LOCT)
  610 CALL INTGR8(GEQ,CEQ,CAPGS,LOCT+9)
      GGS=GGS+GEQ
      CG=CG+CQGS(LX0+LOCT)
      CALL INTGR8(GEQ,CEQ,CAPGD,LOCT+11)
      GGD=GGD+GEQ
      CG=CG+CQGD(LX0+LOCT)
      CD=CD-CQGD(LX0+LOCT)
      CGD=CGD+CQGD(LX0+LOCT)
      CALL INTGR8(GEQ,CEQ,CAPDS,LOCT+13)
      GDS=GDS+GEQ
      CD=CD+CQDS(LX0+LOCT)
      CALL INTGR8(GEQTT,CEQ,CAPTT,LOCT+15)
      GM=GM-GEQTT
      CD=CD-CQTT(LX0+LOCT)
      IF (INITF.NE.5) GO TO 700
      CQGS(LX1+LOCT)=CQGS(LX0+LOCT)
      CQGD(LX1+LOCT)=CQGD(LX0+LOCT)
      CQDS(LX1+LOCT)=CQDS(LX0+LOCT)
      CQTT(LX1+LOCT)=CQTT(LX0+LOCT)
C
C  CHECK CONVERGENCE
C
  700 IF (INITF.NE.3) GO TO 710
      IF (IOFF.EQ.0) GO TO 710
      GO TO 750
  710 IF (ICHECK.EQ.1) GO TO 720
      TOL=RELTOL*DMAX1(DABS(CGHAT),DABS(CG))+ABSTOL
      IF (DABS(CGHAT-CG).GE.TOL) GO TO 720
      TOL=RELTOL*DMAX1(DABS(CDHAT),DABS(CD))+ABSTOL
      IF (DABS(CDHAT-CD).LE.TOL) GO TO 750
  720 NONCON=NONCON+1
  750 VGSO(LX0+LOCT)=VGS
      VGDO(LX0+LOCT)=VGD
      CGO(LX0+LOCT)=CG
      CDO(LX0+LOCT)=CD
      CGDO(LX0+LOCT)=CGD
```

```
      GMO(LX0+LOCT)=GM
      GDSO(LX0+LOCT)=GDS
      GGSO(LX0+LOCT)=GGS
      GGDO(LX0+LOCT)=GGD
C
C  LOAD CURRENT VECTOR
C
  900 CEQGD=TYPE*(CGD-GGD*VGD)
      CEQGS=TYPE*((CG-CGD)-GGS*VGS)
      CDREQ=TYPE*((CD+CGD)-GDS*VDS-GM*VGS)
      VALUE(LVN+NODE6)=VALUE(LVN+NODE6)-CEQGS-CEQGD
      VALUE(LVN+NODE4)=VALUE(LVN+NODE4)-CDREQ+CEQGD
      VALUE(LVN+NODE5)=VALUE(LVN+NODE5)+CDREQ+CEQGS
C
C  LOAD Y MATRIX
C
      LOCY=LVN+NODPLC(LOC+20)
      VALUE(LOCY)=VALUE(LOCY)+GDPR
      LOCY=LVN+NODPLC(LOC+21)
      VALUE(LOCY)=VALUE(LOCY)+GGD+GGS+GGPR
      LOCY=LVN+NODPLC(LOC+22)
      VALUE(LOCY)=VALUE(LOCY)+GSPR
      LOCY=LVN+NODPLC(LOC+23)
      VALUE(LOCY)=VALUE(LOCY)+GDPR+GDS+GGD
      LOCY=LVN+NODPLC(LOC+24)
      VALUE(LOCY)=VALUE(LOCY)+GSPR+GDS+GM+GGS
      LOCY=LVN+NODPLC(LOC+26)
      VALUE(LOCY)=VALUE(LOCY)+GGPR
      LOCY=LVN+NODPLC(LOC+9)
      VALUE(LOCY)=VALUE(LOCY)-GDPR
      LOCY=LVN+NODPLC(LOC+10)
      VALUE(LOCY)=VALUE(LOCY)-GGD
      LOCY=LVN+NODPLC(LOC+11)
      VALUE(LOCY)=VALUE(LOCY)-GGS
      LOCY=LVN+NODPLC(LOC+12)
      VALUE(LOCY)=VALUE(LOCY)-GSPR
      LOCY=LVN+NODPLC(LOC+13)
      VALUE(LOCY)=VALUE(LOCY)-GDPR
      LOCY=LVN+NODPLC(LOC+14)
      VALUE(LOCY)=VALUE(LOCY)+GM-GGD
      LOCY=LVN+NODPLC(LOC+15)
      VALUE(LOCY)=VALUE(LOCY)-GDS-GM
      LOCY=LVN+NODPLC(LOC+16)
      VALUE(LOCY)=VALUE(LOCY)-GGS-GM
      LOCY=LVN+NODPLC(LOC+17)
      VALUE(LOCY)=VALUE(LOCY)-GSPR
      LOCY=LVN+NODPLC(LOC+18)
      VALUE(LOCY)=VALUE(LOCY)-GDS
      LOCY=LVN+NODPLC(LOC+27)
      VALUE(LOCY)=VALUE(LOCY)-GGPR
      LOCY=LVN+NODPLC(LOC+28)
      VALUE(LOCY)=VALUE(LOCY)-GGPR
 1000 LOC=NODPLC(LOC)
      GO TO 10
      END
```

13. APPENDIX D -SIMULATION SOURCE LISTINGS

```
PROCESS TEST 100 um MESFET CHARACTERIZATION
*Cycle Controls
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
*
*Listing Options
.WIDTH OUT=80
*
*Active Elements
*Bn ND NG NS GFETn (width in um)
B1 1 2 0 SI12 100
B2 3 4 0 SI12 100
B3 5 6 0 SI12 100
B4 7 8 0 SI12 100
B5 9 10 0 SI12 100
*
*Active Element Models
*model is for 1 um slice of MESFET which is multiplied by length
*factor in device definition
*
.MODEL SI12 GASFET(VTO=-2, VBI=1.23, RG=0.13, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=3228, RS=3228, TAU=2.86PS)
*
*Independent Sources
VDS 11 0
VDS1 11 1 DC 0
VGS1 2 0 DC -1.5
VDS2 11 3 DC 0
VGS2 4 0 DC -1
VDS3 11 5 DC 0
VGS3 6 0 DC -0.5
VDS4 11 7 DC 0
VGS4 8 0 DC 0
VDS5 11 9 DC 0
VGS5 10 0 DC 0.5
*
*DC Analysis Parameters
.DC VDS 0 3 0.025
*
*Output Parameters
.PRINT DC I(VDS1) I(VDS2) I(VDS3) I(VDS4) I(VDS5)
.END

ISAB RI36R912T3 Strobe Pulse Distortion
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
```

```
CFIXED 11 0 9FF
CSPAD 25 0 10FF
CRFPAD 23 0 20FF
CGPAD 24 0 20FF
LSIN 15 25 0.16NH
LRFIN 13 23 0.16NH
LGIN 14 24 0.16NH
RSIN 5 15 50
RRFIN 3 13 50
RGIN 4 14 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=4.97, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=4.97, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Strobe Pulse Distortion due to Parasitics
*
VSIN 5 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VRFB 3 0 -0.6
VGGB 4 0 -0.3
.TRAN 0.1PS 50PS
.PRINT TRAN V(5) V(25)
.END
ISAB RI36R912T3 Time Constant Determination
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
```

```
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Input Time Constant Determination
*
VSGB 25 0 -0.3
VGGB 24 0 -0.3
VRFIN 23 0 -0.6 PWL(0PS -.8 0.1PS -.4 100PS -0.4 100.1PS -0.8 200PS -0.8)
.TRAN 2PS 200PS
.PRINT TRAN V(6) V(20)
.END
ISAB RI36R912T3 Pulse Feedthrough at Vbias
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
```

```
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
CRFPAD 23 0 20FF
CGPAD 24 0 20FF
LRFIN 13 23 0.16NH
LGIN 14 24 0.16NH
RRFIN 3 13 50
RGIN 4 14 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VGGB 4 0 -0.3
VRFB 3 0 -0.6
.TRAN 0.1PS 50PS
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI36R912T3 Off Isolation at 10GHz
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
```

```
*
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 15M
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
VGGB 24 0 -0.3
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI36R912T3 Open Switch Tracking
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
```

```
*
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
Sine Wave Tracking Open Switch
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSGB 25 0 -0.3
VGGB 24 0 -0.3
.TRAN 10PS 1NS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI36R912T3 Tracking at 2.3Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
```

```
BSG1 7 24 6 R12G1
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 57.5PS 100PS)
VGGB 24 0 -0.3
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI36R912T3 Tracking at Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSG1 7 24 6 R12G1
```

```
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 26 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 100PS)
VGGB 4 0 -0.3
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI26R912T3 Time Constant Determination
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
```

```
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Input Time Constant Determination
*
VSGB 25 0 -0.3
VGGB 24 0 -0.3
VRFIN 23 0 -0.6 PWL(0PS -.8 0.1PS -.4 100PS -0.4 100.1PS -0.8 200PS -0.8)
.TRAN 2PS 200PS
.PRINT TRAN V(6) V(20)
.END
ISAB RI26R912T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
```

```
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VGGB 24 0 -0.3
VRFB 23 0 -0.6
.TRAN 0.1PS 50PS
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI26R912T3 Off Isolation
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
```

```
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 10M
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
VGGB 24 0 -0.3
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI26R912T3 Open Switch Tracking
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
```

```
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
Sine Wave Tracking Open Switch
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSGB 25 0 -0.3
VGGB 24 0 -0.3
.TRAN 10PS 1NS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB R126R912T3 Tracking with 2.3Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
```

```
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 57.5PS 100PS)
VGGB 24 0 -0.3
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
*
.END
ISAB RI26R912T3 Tracking with Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
```

```
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 100PS)
VGGB 4 0 -0.3
.TRAN 1PS 1NS
.PRINT TRAN V(25) V(23) V(20) V(21)
.END
ISAB RI16R912T3 Time Constant Determination
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
***********End ISAB Circuit********
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Input Time Constant Determination
```

```
*
VSGB 25 0 -0.3
VRFIN 23 0 -0.6 PWL(0PS -.8 0.1PS -.4 100PS -0.4 100.1PS -0.8 200PS -0.8)
.TRAN 2PS 200PS
.PRINT TRAN V(6) V(20)
.END
ISAB RI16R912T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
CRFPAD 23 0 20FF
CGPAD 24 0 20FF
LRFIN 13 23 0.16NH
LGIN 14 24 0.16NH
RRFIN 3 13 50
RGIN 4 14 50
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VRFB 3 0 -0.6
.TRAN 0.1PS 50PS
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI16R912T3 Off Isolation
*
*Cycle Controls and Listing Options
```

```
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
***********End ISAB Circuit********
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 5M
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R912T3 Open Switch Tracking
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
```

```
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
Sine Wave Tracking Open Switch
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSGB 25 0 -0.3
.TRAN 10PS 1NS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R912T3 Tracking with 2.3Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
```

```
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 53PS 100PS)
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI16R912T3 Tracking with Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 23PS 100PS)
```

```
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI16R922T3 Time Constant Determination
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Input Time Constant Determination
*
VSGB 25 0 -0.35
VRFIN 23 0 -0.65 PWL(0PS -.8 0.1PS -.4 100PS -0.4 100.1PS -0.8 200PS -0.8)
.TRAN 2PS 200PS
.PRINT TRAN V(6) V(20)
.END
ISAB RI16R922T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
```

```
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
CRFPAD 23 0 20FF
CGPAD 24 0 20FF
LRFIN 13 23 0.16NH
LGIN 14 24 0.16NH
RRFIN 3 13 50
RGIN 4 14 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 25PS 200PS)
VRFB 3 0 -0.65
.TRAN 0.1PS 50PS
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI16R922T3 Off Isolation
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
```

```
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 10M
VRFIN 23 0 SIN(-0.65 0.2 10GHZ)
VSGB 25 0 -2.95
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R922T3 Open Switch Tracking
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
```

```
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
Sine Wave Tracking Open Switch
*
VRFIN 23 0 SIN(-0.65 0.2 1GHZ)
VSGB 25 0 -0.35
.TRAN 10PS 1NS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R922T3 Tracking with 2.3Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.65 0.2 1GHZ)
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 53PS 100PS)
.TRAN 1PS 1NS
.PRINT TRAN V(25) V(23) V(20) V(21)
.END
```

```
ISAB RI16R922T3 Tracking with Tau Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
***********End ISAB Circuit********
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.25, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.65 0.2 1GHZ)
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 23PS 100PS)
.TRAN 1PS 1NS
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI36R912T3 Pulse Feedthrough at Vbias
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSG1 7 24 6 R12G1 60
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
```

```
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF IC=-0.6
CRFPAD 23 0 20FF
CGPAD 24 0 20FF
LRFIN 13 23 0.16NH
LGIN 14 24 0.16NH
RRFIN 3 13 50
RGIN 4 14 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VGGB 4 0 -0.6
VRFB 3 0 -0.6
.TRAN 0.25PS 50PS UIC
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI36R912T3 Off Isolation at 10GHz
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSG1 7 24 6 R12G1 60
BSS 9 26 8 R12S 60
```

```
BSG2 11 24 10 R12G2 60
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 0.5E8
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
VGGB 24 0 -0.3
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI36R912T3 Open Switch Tracking
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSG1 7 24 6 R12G1 60
BSS 9 26 8 R12S 60
```

```
BSG2 11 24 10 R12G2 60
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking Open Switch
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSGB 25 0 -0.3
VGGB 24 0 -0.3
.TRAN 10PS 1NS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI36R912T3 Tracking at 100PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSG1 7 24 6 R12G1 60
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2 60
```

```
V1 23 6 0
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF IC=-0.6
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture
*
VRFIN 23 0 SIN(-0.6 0.2 250MEG)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 100PS 410PS)
VGGB 24 0 -0.3
.TRAN 10PS 4NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI36R912T3 Tracking at 25PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSG1 7 24 6 R12G1 60
BSS 9 26 8 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
```

```
V2 7 8 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 9FF IC=-0.6
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
.MODEL R12G1 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=705, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 110PS)
VGGB 24 0 -0.3
.TRAN 2.5PS 1NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI26R912T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
V3 9 10 0
V4 11 20 0
```

```
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF IC=-0.6
CRFPAD 23 0 20FF
LRFIN 13 23 0.16NH
RRFIN 3 13 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VGGB 24 0 -0.3
VRFB 3 0 -0.6
.TRAN 0.25PS 50PS UIC
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI26R912T3 Off Isolation
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
```

```
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 0.4E8
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
VGGB 24 0 -0.3
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB R126R912T3 Tracking with 100PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF IC=-0.6
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
```

```
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.6 0.2 250MEG)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 100PS 410PS)
VGGB 24 0 -0.3
.TRAN 10PS 4NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
*
.END
ISAB RI26R912T3 Tracking with 25PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 9 26 6 R12S 60
BSG2 11 24 10 R12G2 60
V1 23 6 0
V3 9 10 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 39FF IC=-0.6
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
```

```
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL R12S GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=705, RS=1170, TAU=0.71PS)
.MODEL R12G2 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=705, TAU=0.71PS)
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 110PS)
VGGB 24 0 -0.3
.TRAN 2.5PS 1NS
.PRINT TRAN V(25) V(23) V(20) V(21)
.END
ISAB RI16R912T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit********
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF IC=-0.6
CRFPAD 23 0 20FF
LRFIN 13 23 0.16NH
RRFIN 3 13 50
*
***********End ISAB Circuit********
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
```

```
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 200PS)
VRFB 3 0 -0.6
.TRAN 0.25PS 50PS UIC
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI16R912T3 Off Isolation
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
```

```
*
RSHUNT 23 20 .25E8
VRFIN 23 0 SIN(-0.6 0.2 10GHZ)
VSGB 25 0 -2.9
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R912T3 Tracking with 100PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF IC=-0.6
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture
*
VRFIN 23 0 SIN(-0.6 0.2 250MEG)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 100PS 410PS)
.TRAN 2.5PS 1NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI16R912T3 Tracking with 25PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
```

```
BSS 11 26 6 RSAG12 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 152FF IC=-0.6
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG12 67
BFB 4 5 0 RSAG12 23
BLPU 2 4 4 RSAG12 45
BPU 2 4 6 RSAG12 90
D1 6 7 TD4 66
D2 7 8 TD4 66
D3 8 5 TD4 66
BPD 5 1 1 RSAG12 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG12 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture
*
VRFIN 23 0 SIN(-0.6 0.2 1GHZ)
VSIN 25 0 PULSE(-2.9 -.3 5PS 5PS 5PS 25PS 110PS)
.TRAN 2.5PS 1NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
ISAB RI16R922T3 Pulse Feedthrough
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**********ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF IC=-0.65
CRFPAD 23 0 20FF
LRFIN 13 23 0.16NH
RRFIN 3 13 50
*
**********End ISAB Circuit*******
*Amplifier Subcircuit
*
```

```
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Pulse Feedthrough at Vbias
*
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 25PS 200PS)
VRFB 3 0 -0.65
.TRAN 0.25PS 50PS UIC
.PRINT TRAN V(26) V(23) V(20)
.END
ISAB RI16R922T3 Off Isolation
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.5, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
```

```
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Off Isolation with 10 GHz Sine RF Input
*
RSHUNT 23 20 0.5E8
VRFIN 23 0 SIN(-0.65 0.2 10GHZ)
VSGB 25 0 -2.95
.TRAN 2PS 100PS
.PRINT TRAN V(23) V(20) V(21)
.END
ISAB RI16R922T3 Tracking with 100PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF IC=-0.65
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.83, ALPHA=2.3, BETA=3.1E-5
+ LAMBDA=0.055, CGS0=0.595FF, CGD=0.595FF, CDS=0.0791FF, IS=2.07E-15,
+ RD=1170, RS=1170, TAU=0.71PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture 2.3Tau
*
VRFIN 23 0 SIN(-0.65 0.2 250MEG)
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 100PS 410PS)
.TRAN 10PS 4NS UIC
.PRINT TRAN V(25) V(23) V(20) V(21)
```

```
.END
ISAB RI16R922T3 Tracking with 25PS Aperture
*
*Cycle Controls and Listing Options
.OPTIONS ITL4=1000 ITL5=0 LIMPTS=2000 NOPAGE NOMOD
.WIDTH OUT=80
*
**************ISAB Circuit*******
*
BSS 11 26 6 RSAG22 60
V1 23 6 0
V4 11 20 0
V5 25 26 0
*
XAMP1 20 21 1 2 AMP
*ISAB Circuit Passive and Parasitic Components
CFIXED 11 0 74FF IC=-0.65
*
***********End ISAB Circuit*******
*Amplifier Subcircuit
*
.SUBCKT AMP 3 5 1 2
BIN 4 3 0 RSAG22 67
BFB 4 5 0 RSAG22 23
BLPU 2 4 4 RSAG22 45
BPU 2 4 6 RSAG22 90
D1 6 7 TD4 40
D2 7 8 TD4 40
D3 8 5 TD4 40
BPD 5 1 1 RSAG22 90
.ENDS AMP
*
*Active Element Models
.MODEL RSAG22 GASFET(VTO=-2, VBI=1.23, RG=0.25, ALPHA=2.3, BETA=2.61E-5
+ LAMBDA=0.055, CGS0=1.19FF, CGD=1.19FF, CDS=0.096FF, IS=4.13E-15,
+ RD=1555, RS=1555, TAU=2.86PS)
*
.MODEL TD4 D(IS=.312E-12, RS=1745, N=1.1, TT=.59PS, CJO=8.02E-15,
+ VJ=0.72, EG=1.42, BV=8, IBV=1E-3)
*
*Independent Sources
VDD 2 0 4.5
VSS 1 0 -3
*
*Sine Wave Tracking at Sampling Aperture Tau
*
VRFIN 23 0 SIN(-0.65 0.2 1GHZ)
VSIN 25 0 PULSE(-2.95 -.35 5PS 5PS 5PS 25PS 110PS)
.TRAN 2.5PS 1NS UIC
.PRINT TRAN V(26) V(23) V(20) V(21)
.END
```