A WIDELY TUNABLE ACTIVE CMOS RADIO-FREQUENCY FILTER

by

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ABSTRACT

There has always been a drive by industry to add as much functionality and flexibility to electronic devices as possible. Tunable circuits are among useful sub-blocks that facilitate achieving these goals. This thesis presents a fully integrated radio-frequency filter whose centre frequency and bandwidth are tunable.

Radio-frequency filters are essential components in transceivers. However, due to the poor quality factor and large area of on-chip passive inductors, these blocks are typically implemented off-chip. The filter presented in this work uses active inductors, i.e., transistor-based structures that emulate the response of a passive inductor. Not only is the quality factor of an active inductor superior to that of its passive counterpart, but also its size is a relatively smaller fraction of the chip area. It should be noted that passive inductors have better performance in terms of noise, linearity, and power consumption as compared to their active counterparts. Special care has been taken to minimize the power, noise, and nonlinear distortions of the proposed filter.

The filter is designed and fabricated in a 0.18μm CMOS technology. Its centre frequency is tunable over the range of 580MHz to 3.3GHz and its quality factor can also be tuned, making it suitable for a variety of applications requiring different bandwidths. The fully differential filter, including the biasing circuitry and output buffers required to drive the 50Ω impedance of high-frequency measurement equipment, consumes between 12 to 26mW from a 1.8V supply and occupies a chip area of 115μm × 70μm.

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LIST OF ACRONYMS

AC	Alternating Current
ADS	Advanced Design System
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CMOS	Complementary Metal Oxide Semiconductor
DBPSK	Differential Binary Phase Shift Keying
DC	Direct Current
FoM	Figure of Merit
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GPS	Global Positioning System
GSM	Global System for Mobile Communication
IEEE	Institute of Electrical and Electronic Engineers
IF	Intermediate Frequency
IIP3	Input Third-Order Intercept Point
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LAN	Local Area Network
LNA	Low Noise Amplifier
LO	Local Oscillator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NIC	Negative Impedance Circuit
OFDM	Orthogonal Frequency Division Multiplexing
OQPSK	Offset Quadrature Phase Shift Keying
PCS	Personal Communications System
QPSK	Quadrature Phase Shift Keying
RF	Radio-Frequency
SFDR	Spurious Free Dynamic Range
SS	Spread Spectrum
UMTS	Universal Mobile Telephone System
VCCS	Voltage Controlled Current Source

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Chapter 1

Motivation

1.1 Filters in Multi-Standard Radio-Frequency Circuits

The growing number of wireless communications standards and the desire for global roaming has stimulated research and development of low-cost compact transceivers that are capable of supporting as many communications standards as possible [1], [2]. This is especially relevant in the highly populated frequency band of 900MHz to 2.4GHz, which is used for applications such as Bluetooth, wireless LANs (e.g., IEEE802.11b/g), cellular phones (e.g., GSM), and global positioning systems (GPS). There is also a growing trend toward the use of highly integrated transceivers to address low-cost and low-power requirements of portable devices. A high degree of integration not only reduces the cost of the product by minimizing the number of off-chip elements, but also reduces power consumption by eliminating the need for driving typically low-impedance off-chip components.

Radio-frequency (RF) filters are essential components of any RF wireless transceiver and are used to attenuate undesired out of band signals. RF filters typically use passive components; however, on-chip passive inductors are notorious for their low quality factor and the large amount of chip area they consume [3], [4]. As a result, RF

filters are usually implemented off-chip, a process which adds extra cost and manufacturing time to the design cycle. By using active inductors, the required chip area is reduced while the quality factor, and potentially the performance of the emulated inductor, is improved. Additionally, both the frequency and selectivity (bandwidth) of the active filter can be tuned by changing the amount of current channeled through the transistors of these active structures. This tunable nature makes active filters especially suitable for multi-standard systems. However, it should be pointed out that passive inductors perform better in terms of linearity and power consumption [5].

1.2 Research Goals

The goal of this research is to design a widely tunable active filter that is suitable for radio transceivers operating at frequencies in the band of 900MHz to 2.4GHz. Table 1.1 shows some of the standards in this frequency range [6-9].

Wireless Standard	Carrier Frequency	Channel Spacing	Modulation Technique	Maximum Data Rate
GSM	880-960MHz	200kHz	GMSK	270.8kb/s
PCS 1900	1.88-1.93GHz	200kHz	GMSK	270.8kb/s
GPS L1	1.575GHz	2MHz (C/A Code)	BPSK/SS	50b/s
IEEE 802.11b	2.4-2.48GHz	25MHz	DBPSK/CCK	11Mb/s
IEEE 802.11g	2.4-2.48GHz	25MHz	OFDM	54Mb/s
Bluetooth	2.4-2.48GHz	1MHz	GFSK	1Mb/s
UMTS	1.92-2.17GHz	5MHz	QPSK	3.84Mb/s
Zigbee Band 1	2.4-2.48GHz	5MHz	OQPSK	250kb/s
Zigbee Band 2	902-928MHz	5MHz	OQPSK	40kb/s

Table 1.1 – Example of Standards Operating Near the Range of 900MHz to 2.4GHz

In this research, a method of increasing the tuning range of active filters is presented and issues affecting filter performance such as noise and dynamic range are

investigated. The filter is implemented in a 0.18μm CMOS technology and its performance is measured.

1.3 Thesis Organization

This thesis is organized as follows. Chapter 2 provides background discussion on why filters are needed and how they are implemented. It also introduces the concept of using gyrators to simulate inductive components for on-chip active filters. In Chapter 3, a detailed analysis of the proposed active filter is discussed, and modifications to enhance the range of operating frequencies are presented. Chapter 4 contains an analysis and optimization of noise in the active filter, and Chapter 5 discusses issues affecting large-signal operation and the linearity of the filter. Each chapter contains simulation results to verify the analytical discussions presented. Chapter 6 describes layout techniques and test results of the fabricated chip, and presents a comparison with other works. Finally, Chapter 7 concludes this thesis and presents ideas for future work.

Chapter 2

Background

2.1 The Need for Filters

Filters are a necessary part of any type of radio transceiver and in general their function is to pass the desired signal while blocking out all other signals. A block diagram of a typical receiver front-end is shown in Figure 2.1 [9].

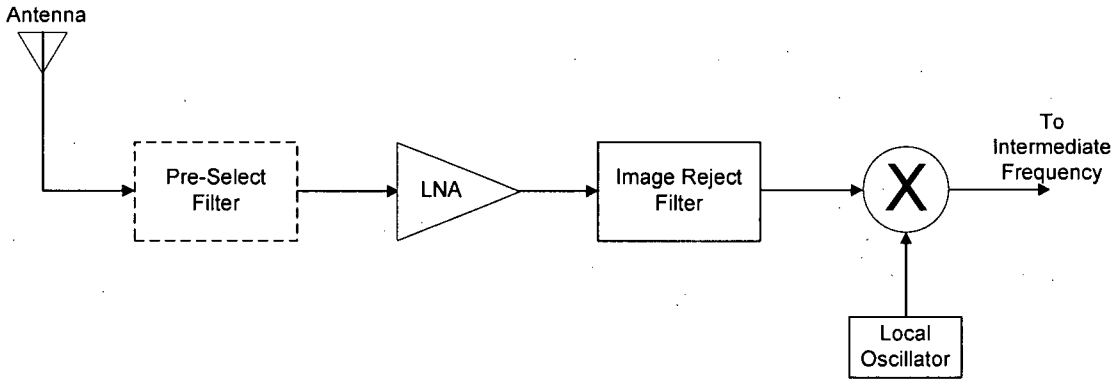

Figure 2.1 - Receiver Front-End

The radio-frequency (RF) signal is first received by an antenna and then passes through an optional pre-select filter. This filter is used to select an entire band of signals, but is not always necessary because the antenna may also filter out many frequencies. The signal is then fed into a low-noise amplifier (LNA) which is responsible for amplifying the signal while adding as little noise as possible. In heterodyne receivers, an image-

reject filter is typically needed to prevent errors in the mixer which down-converts the RF signal to a lower frequency known as the intermediate frequency (IF) for further signal processing.

The selectivity of the image-reject filter has a direct impact on the choice of intermediate frequencies used in the transceiver. Low IFs are desired to relax the complexity of signal processing circuits or analog-to-digital converters, and to realize a low IF the LO must be located close to the desired signal (in terms of frequency). This also means that the image frequency will be closer to the desired signal's frequency and a more selective filter will be needed [9]. The next section will discuss the parameters needed to classify the response of a bandpass filter.

2.2 Filter Parameters

The focus of this work is on bandpass filters; however, all filter types are characterized by the same general parameters. The response of a typical bandpass filter is shown in Figure 2.2.

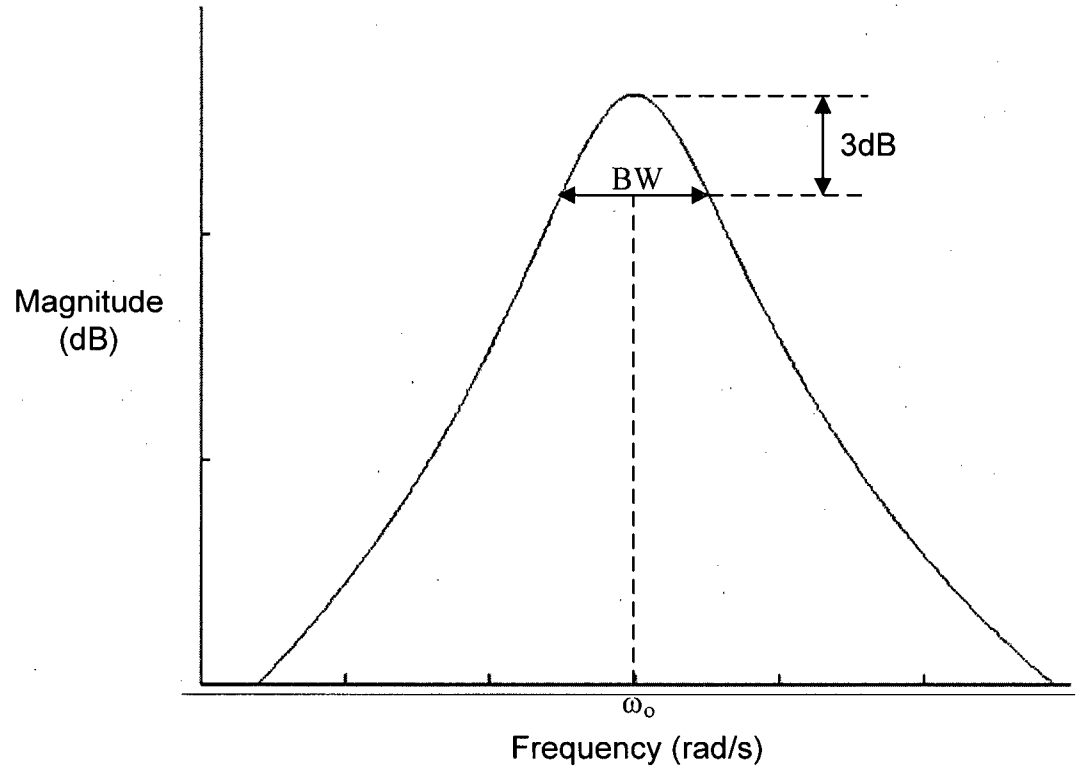

Figure 2.2 - Second Order Bandpass Filter Response

The center frequency of the filter is given by ω_o, and the bandwidth (BW) is measured where the frequency response is 3dB lower than the peak. The quality factor (Q) of the filter is defined as [9]:

$$Q = \frac{\omega_o}{BW} \tag{2.1}$$

and it is a direct measurement of the filter selectivity. The standard form of the transfer function for a second-order bandpass filter is [10]:

$$T(s) = \frac{a_1 s}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{2.2}$$

where a_1 is a constant relating to the gain of the filter. The gain at the centre frequency is given by [10]:

$$A_v(\omega_o) = \frac{a_1 Q}{\omega_o} \tag{2.3}$$

Higher-order filters can be formed by cascading second-order filter stages, and this can improve the selectivity and the stop-band attenuation of the filter.

Now that we have looked at the parameters of a bandpass filter, we can look at common circuits used to implement them.

2.3 Passive Bandpass Filters

One of the most basic passive bandpass filters is formed by a parallel combination of an inductor, capacitor, and resistor. This structure is known as a second-order RLC resonator and is shown in Figure 2.3 [10].

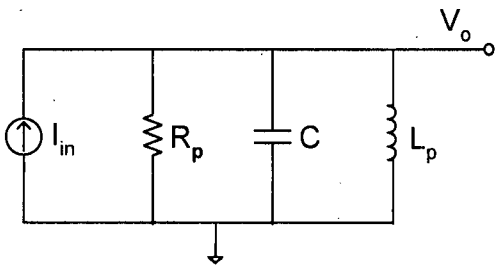

Figure 2.3 - Second Order RLC Resonator

The circuit is excited by the parallel current source I_{in} and the transfer function is:

$$\frac{V_o}{I_{in}} = \frac{s/C}{s^2 + \frac{s}{R_p C} + \frac{1}{L_p C}} \tag{2.4}$$

By comparing this equation to the standard bandpass filter transfer function given in Equation 2.2 we can determine the parameters of the RLC resonator as:

$$\omega_o = \frac{1}{\sqrt{L_p C}}$$
$$Q = R_p\sqrt{\frac{C}{L_p}} \text{ or } \frac{R_p}{\omega_o L_p} \qquad (2.5)$$
$$a_1 = 1/C$$

The main advantages of an RLC resonator arise from its passive structure; it consumes no power and adds minimal noise to the input signal [11]. Also, since it is made up of linear components, it can handle large signals without causing distortion [12]. The major disadvantage of the structure are the passive reactive components, in particular the inductors. A good quality inductor is fabricated by winding spiral coils of wire around a ferrite core. This method works fine for discrete components, but is incompatible with current integrated circuit technology. State-of-the-art passive integrated inductors are typically flat devices and, as such, on-chip inductors are large and of relatively poor quality [5].

The quality of an inductor is defined in the same manner as the quality of a filter, because an inductor itself (to the first order) actually forms an RLC resonator as shown in Figure 2.4 [9].

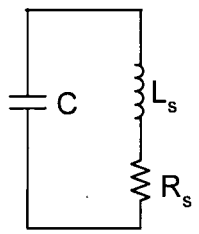

Figure 2.4 - Equivalent Circuit for a Spiral Inductor

The capacitor C is due to the parasitic capacitance between the inductor windings, and the resistor R_s represents the resistive loss of the coils. The frequency at which the inductance and the coil capacitance resonate is known as the self-resonant frequency of the inductor and, after this point, the impedance of the inductor actually becomes capacitive. The expression for the self-resonant frequency and the quality factor of the above circuit are given by [9].

$$\omega_o = \frac{1}{\sqrt{L_s C}}$$
$$Q = \frac{1}{R_s}\sqrt{\frac{L_s}{C}} \text{ or } \frac{\omega_o L_s}{R_s} \tag{2.6}$$

The series resistance for an on-chip inductor can be relatively large due to the relatively narrow and long metal traces used. Also, the large area of metal needed produces a relatively large capacitive coupling to the substrate. These effects, combined with the small inductance achievable using planar structures, lead to the low quality factor of on-chip inductors.

It is useful to see how the low quality factor of an inductor will affect the quality of the RLC resonator shown in Figure 2.3. We can transform the series inductor and resistor shown in Figure 2.4 into the parallel inductor and resistor shown in the RLC resonator by equating the two equivalent impedances [9]. For the purpose of this derivation, we will assume that the parasitic capacitance of the inductor is the same as the one in the RLC resonator. It should be noted that the transformation is an approximation and will only be valid at the frequencies around the resonant frequency. The impedance relationship is given by:

$$j\omega_o L_s + R_s = (j\omega_o L_p) \| R_p = \frac{(\omega_o L_p)^2 R_p + j\omega_o L_p R_p^2}{R_p^2 + (\omega_o L_p)^2} \tag{2.7}$$

By equating the real and imaginary parts of this equation and using the expression for Q in Equation 2.6 we can write:

$$\begin{aligned} R_p &= R_s(Q^2 + 1) \\ L_p &= L_s\left(\frac{Q^2 + 1}{Q^2}\right) \end{aligned} \tag{2.8}$$

This shows that the parallel inductance is almost identical to the series one but the parallel resistance in the RLC resonator will be limited by the quality of the inductor used. Since the Q of the resonator is directly proportional to the parallel resistance (as seen by Equation 2.5), a low quality inductor will lead to a filter with poor selectivity [9].

2.4 Active Filters

It is possible to implement an active bandpass filter without inductors by using op-amps, capacitors, and resistors in a feedback configuration. One common structure is shown in Figure 2.5, and it is called the KHN biquadratic filter (named after its inventors Kerwin, Huelsman, and Newcomb) [10].

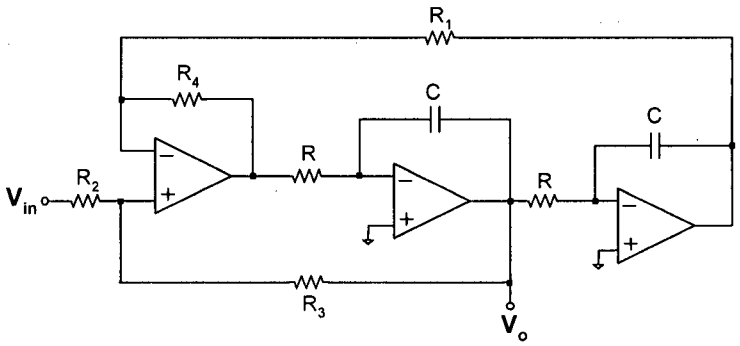

Figure 2.5 - Schematic of KHN Biquadratic Active Filter

The transfer function of this circuit is given by:

$$\frac{V_o}{V_{in}} = \frac{s\dfrac{R_3(R_1+R_4)}{RCR_1(R_2+R_3)}}{s^2 + s\dfrac{R_2(R_1+R_4)}{RCR_1(R_2+R_3)} + \dfrac{R_4}{C^2R^2R_1}} \tag{2.9}$$

The transfer function shows that this circuit does function as a bandpass filter but the op-amps, in addition to increasing the circuit complexity and the power dissipation, limit the frequency operation of this architecture [10].

Negative feedback can also be used to create an active inductor using a circuit known as a gyrator [13]. This type of circuit functions as an impedance inverter [14], and is shown in Figure 2.6.

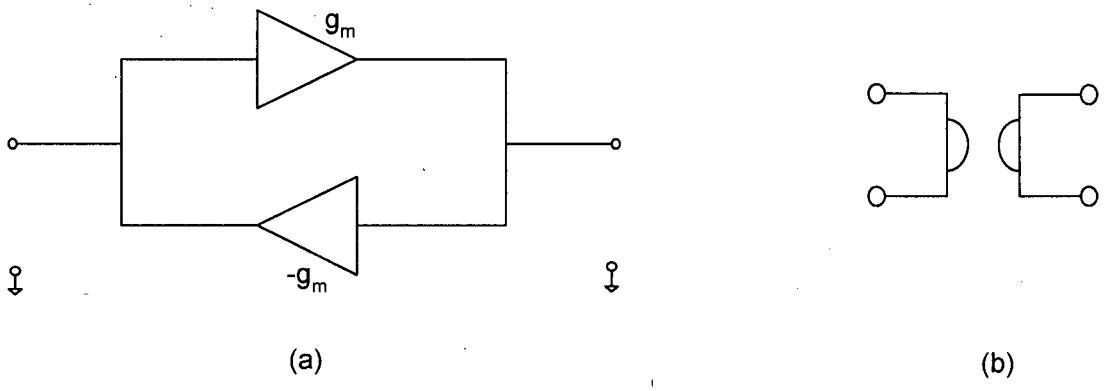

Figure 2.6 - (a) An ideal gyrator, (b) The gyrator symbol

A gyrator is made up of two transconductors in a negative feedback configuration, and for the purpose of this analysis the transconductors will be considered ideal. This means that they have infinite input and output impedances. If a capacitor is placed at one of the gyrator ports, the impedance seen at the other port will be inductive. This can be shown by analyzing the circuit of Figure 2.7.

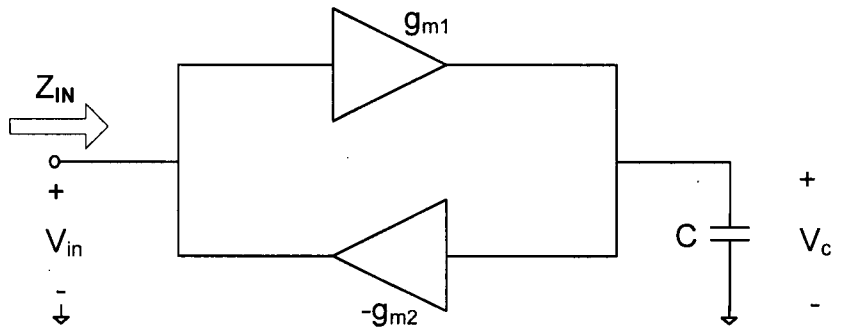

Figure 2.7 - Gyrator Based Inductor

By using Kirchhoff's Current Law (KCL) at the two nodes in the circuit, we obtain the following two expressions:

$$\begin{aligned} g_{m1}V_{in} &= V_c sC \\ g_{m2}V_c &= I_{in} \end{aligned} \tag{2.10}$$

Solving for the input impedance gives:

$$Z_{IN} = \frac{V_{in}}{I_{in}} = \frac{sC}{g_{m1}g_{m2}} \tag{2.11}$$

Thus, the impedance looking into the gyrator increases with frequency, which is exactly the response obtained from an inductor. It can also be seen that the inductance can be adjusted by changing the value of the load capacitance or the transconductance of either transconconductor. It will also be shown in the next chapter that the quality factor of the active inductor is also tunable. This means that gyrators can be used to create high quality inductors that occupy a small chip area enabling us to create on-chip filters based on the simple RLC resonator structure [14]. Also, a transconductor can be formed using a single transistor which minimizes parasitic capacitances and allows for high frequency operation.

However, there are some disadvantages in using gyrators to emulate inductors and these are due to the nature of active devices in general [15]. Specifically, transistors consume power, generate noise, and exhibit nonlinear behaviour, all of which will be shown to adversely affect filter performance.

2.5 Previous Work

A gyrator needs both a positive and a negative transconductor. This limits the topologies that can be used. In a two-transistor gyrator, a common-source stage (CS) forms the negative transconductor, and a common-gate (CG) or common-drain (CD) stage must be used for the positive transconductor. Four of the eight possible arrangements using two transistors are shown in Figure 2.8 [16].

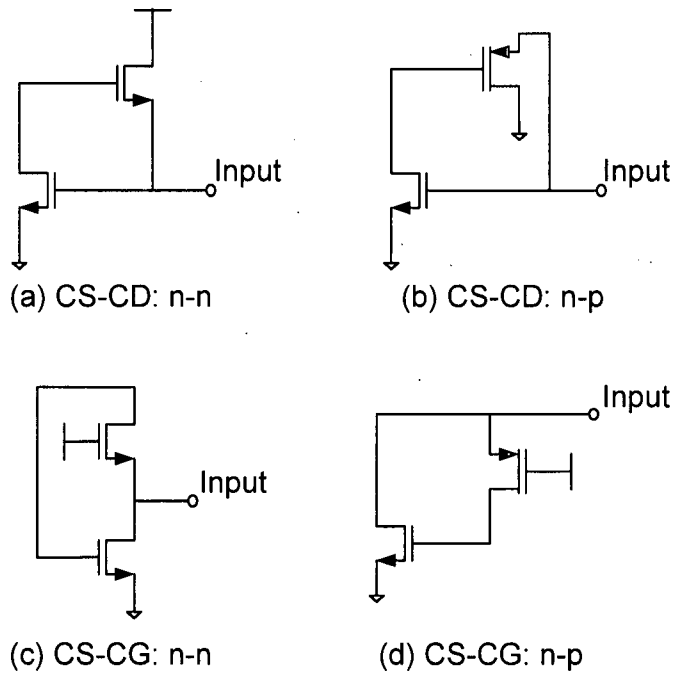

Figure 2.8 – Four of Eight Possible Two-Transistor Gyrators

The other four possibilities are obtained by switching the NMOS transistors to PMOS and vice-versa. The capacitance needed to form an active inductor is not shown in these diagrams, but it could either be placed at the terminal node in the circuit or be due to the parasitic capacitances of the transistors.

The structures involving a common-drain stage put greater restrictions on the voltage levels required to properly bias the transistors [16], which has a negative impact on the inductance tuning range. The circuits involving a common-gate stage have a wider tuning range, but to achieve high-quality inductors ($Q > 20$) some means of compensation such as using negative resistance is required [16]. However, contrary to [16], it is shown in [17] that the negative resistance can improve the noise performance of high Q inductors. This work will show that negative resistance can also be used to improve the inductance tuning range.

It is also possible to form active inductors using three or more transistors, and an exhaustive study of all possible three-transistor active inductors is performed in [18]. In structures with three transistors, the extra transistor is normally used to improve the quality factor by boosting the loop gain through feedback [19]. However, the extra transistor decreases the maximum operating frequency of the circuit [16] without the improvement in inductance tuning range obtained from negative resistance.

System-level analyses of the noise and dynamic range in active resonators have been performed in [20], [21], and [22]. It has been shown that the noise of an active resonator is proportional to Q at best, but can also be proportional to a power of Q depending on the circuit. The dynamic range also gets worse in proportion to Q, and also decreases at high frequencies.

Active filters in the GHz range have been designed in [17, 19, 23-25], to name a few, but most are not able to achieve the wide range of operating frequencies needed for multi-standard radios. Widely tunable filters have also been designed by switching in different sizes of capacitors or tuning with varactors to change the operating frequency [26], [27]. However, the area consumed by capacitors in order to operate in the low GHz range is larger than that consumed by the transistors in an active inductor. An active inductor also has a larger tuning range than a CMOS varactor, which has a maximum tuning ratio (C_{max}/C_{min}) ranging from only 2 to 12 times [28], [29].

In the subsequent chapters, a method for using active inductors with an increased tuning range to implement a widely tunable RF filter is presented. A noise analysis and optimization at the circuit level will be performed, and insights into the design issues affecting the dynamic range of the filter will be given.

Chapter 3

Tunable Filter

3.1 Basic Filter Circuit

Figure 3.1(a) shows the circuit used to implement the gyrator in this work. It consists of a PMOS common-gate amplifier to provide the positive transconductance and an NMOS common-source amplifier to provide the negative transconductance. By analyzing the simplified small-signal model shown in Figure 3.1(b), an intuitive understanding of the impedance inversion can be obtained.

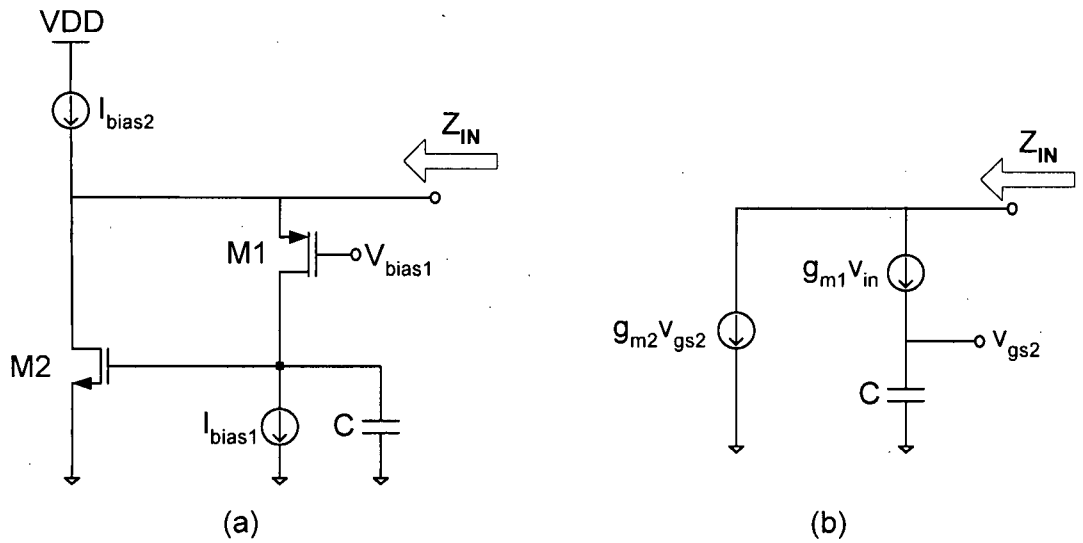

Figure 3.1 - (a) Circuit used to Implement the Gyrator, (b) Simplified Small-Signal Model

The simplified small-signal model contains two dependent current sources: one that is proportional to V_{in} (from transistor M1) and one that is proportional to the voltage across the capacitor (from transistor M2). At low frequencies the capacitor exhibits a large impedance, which creates a correspondingly large voltage drop across it. This causes M2 to draw a large current, which leads to a small Z_{IN}. As the frequency increases the impedance of the capacitor decreases, reducing the voltage drop across it. This also decreases the current drawn by M2, which causes Z_{IN} to increase. The net effect is a linear increase in input impedance with frequency, which is exactly the response expected from an inductor.

Mathematically, the input impedance of the simplified small-signal model can be found by applying a test voltage source and solving for v_{in}/i_{in}. Using KCL, the following equations can be written:

$$i_{in} = g_{m1}v_{in} + g_{m2}v_{gs2} \tag{3.1}$$

$$g_{m1}v_{in} = v_{gs2}sC \tag{3.2}$$

Solving this set of equations gives:

$$Z_{IN} = \frac{v_{in}}{i_{in}} = \frac{sC}{g_{m1}g_{m2} + g_{m1}sC}. \tag{3.3}$$

which, at relatively low frequencies, reduces to:

$$Z_{IN} = \frac{v_{in}}{i_{in}} = \frac{sC}{g_{m1}g_{m2}}. \tag{3.4}$$

The impedance of an inductor is given by sL, so the inductance emulated by this circuit is given by:

$$L = \frac{C}{g_{m1}g_{m2}} \tag{3.5}$$

As mentioned in the previous chapter, the frequency at which the input impedance of the circuit ceases to be inductive is known as the self-resonant frequency. It can be seen from Equation 3.3 that a small capacitance value will increase the self-resonant frequency of the circuit, making the circuit usable at higher frequencies. It should also be noted that in the simplified analysis performed above, once the self-resonant frequency is reached the impedance of the circuit becomes resistive. In actuality, the impedance will become capacitive at this point, as will be seen in the more detailed analysis performed in the next section.

3.2 A Detailed Analysis

A more detailed small-signal model of the circuit in Figure 3.1(a) is shown in Figure 3.2.

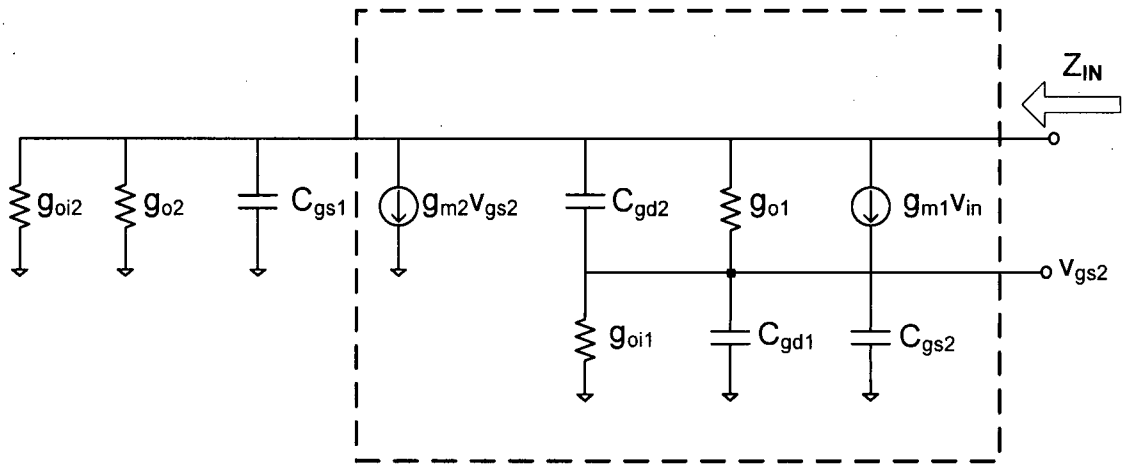

Figure 3.2 - Detailed Small-Signal Model of Active Inductor

In this figure, g_{o1} and g_{o2} are the drain-source conductances of the transistors, and g_{oi1} and g_{oi2} represent the non-ideal output conductances of the current sources. To increase the self-resonant frequency of the active inductor to the gigahertz range, the capacitance is implemented using the parasitics of the transistors. This means the self-resonant frequency of the active inductor itself will be used to implement the active filter. It should also be noted that the body-effect is not considered because the PMOS transistor M1 can be placed in a separate n-well.

The inductive part of the input impedance is due to the components within the dashed box in Figure 3.2, and this impedance is in parallel with the components outside the dashed box as well as the resistance seen looking into the source of transistor M1. KCL is used to find the inductive portion of the input impedance and it gives the following two equations:

$$i_{in} = g_{m1}v_{in} + g_{m2}v_{gs2} + (v_{in} - v_{gs2})(g_{o1} + sC_{gd2}) \tag{3.6}$$

$$g_{m1}v_{in} = v_{gs2}(g_{oi1} + sC_{gd1} + sC_{gs2}) - (v_{in} - v_{gs2})(g_{o1} + sC_{gd2}) \tag{3.7}$$

Solving this set of equations gives:

$$Z_{IN,Inductive} = \frac{v_{in}}{i_{in}} \cong \frac{g_{oi1} + g_{o1} + s(C_{gs2} + C_{gd1} + C_{gd2})}{g_{m1}g_{m2} + g_{m1}g_{oi1} + g_{oi1}g_{o1} + g_{m2}g_{o1} + s(g_{m1}C_{gs2} + g_{m1}C_{gd1} + g_{m2}C_{gd2})} \tag{3.8}$$

where some small terms and higher order terms in the denominator have been disregarded. Although it should be noted that these higher order terms in the denominator will give rise to the capacitive input impedance once the self-resonant frequency of the inductor is surpassed. The impedance of Equation 3.8 can be simplified further by noticing that the $g_{m1}g_{m2}$ term in the denominator will be dominant for

frequencies less than the self-resonant frequency of the active inductor. The equation becomes:

$$Z_{IN,Inductive} \cong \frac{s(C_{gs2}+C_{gd1}+C_{gd2})}{g_{m1}g_{m2}} + \frac{g_{oi1}+g_{o1}}{g_{m1}g_{m2}} \tag{3.9}$$

where the first term represents the inductance and the second term represents a resistance in series with the inductor.

By taking into account the components in parallel with this impedance, (i.e., the components outside of the dashed box in Figure 3.2 and the resistance looking into the source of M1), the entire circuit can be modeled as the parallel RLC network shown in Figure 3.3 [17].

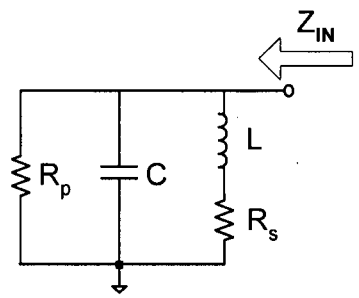

Figure 3.3 - Equivalent Parallel RLC Circuit for the Active Inductor

In this diagram, the values are as follows:

$$C = C_{gs1} \qquad R_p = \frac{1}{g_{m1}} \| \frac{1}{g_{o2}} \| \frac{1}{g_{oi2}}$$

$$R_s = \frac{g_{o1}+g_{oi1}}{g_{m1}g_{m2}} \qquad L = \frac{C_{gs2}+C_{gd1}+C_{gd2}}{g_{m1}g_{m2}} \tag{3.10}$$

Ideally, R_s should be zero to eliminate the loss of the inductor, and R_p should be as large as possible to increase the quality factor of the resonator. This underscores the importance of high output impedance in the transistors and current sources. By assuming

infinite output impedances and neglecting C_{gd} of the transistors, the center frequency (ω_o) and the quality factor (Q) of this resonator can be calculated as:

$$\omega_o = \frac{1}{\sqrt{LC}} = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} = \sqrt{\omega_{t1}\omega_{t2}}$$
$$Q = R_p\sqrt{\frac{C}{L}} = \sqrt{\frac{C_{gs1}g_{m2}}{g_{m1}C_{gs2}}} = \sqrt{\frac{\omega_{t2}}{\omega_{t1}}} \quad (3.11)$$

where ω_{t1} and ω_{t2} are the transit (unity-gain) frequencies of M1 and M2, respectively. Thus, for a high-frequency active filter, both transistors need to be biased for a high unity-gain frequency. However, if M1 has a high unity-gain frequency, the selectivity of the filter will suffer.

This problem can be circumvented by using a negative impedance circuit (NIC) to increase the Q of the filter. The negative resistance will approximately cancel out the parallel resistance, causing the equivalent parallel resistance to become incredibly large. This approach also means the intrinsic Q of the active inductor can be reduced while still maintaining a high overall filter Q, which also improves the noise performance of the filter as will be shown in the next chapter. Another benefit of adding negative resistance is that the circuit can function over a wider range of frequencies since M1 and M2 are only used to tune the center frequency.

3.3 Proposed Wideband Topology

A modified active inductor circuit with enhanced tuning range is shown in Figure 3.4.

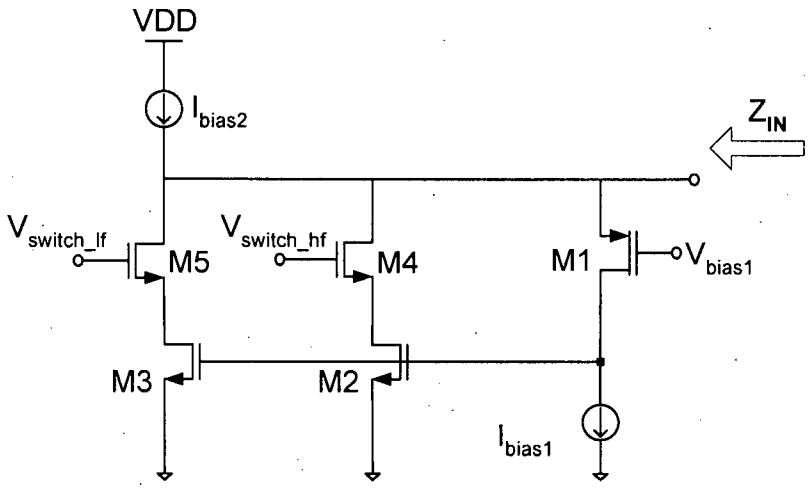

Figure 3.4 - Modified Active Inductor Circuit

In this circuit, M2 has a minimum channel length while the channel of M3 is longer (e.g., three times longer than M2). M4 and M5 are switches used to enable or disable M2 and M3, respectively. Assuming these two switches are ideal, the circuit has three useful regions of operation determined by the unity-gain frequency of M2 and M3 as follows:

1) For low-frequency operation, M3 is enabled and M2 is disabled, and the active inductor is formed by transistors M1 and M3. Since the channel length of M3 is three times the feature length of the technology, its unity-gain frequency is lower than that of M2. Also, this long channel length increases the capacitance added to the signal path, which also serves to decrease the unity-gain frequency.
2) For mid-frequency operation, M2 is enabled and M3 is disabled. The active filter is now formed by transistors M1 and M2, and the minimum channel length of M2 provides a higher unity-gain frequency and less capacitance.

3) For high-frequency operation, both M2 and M3 are enabled. In this case the active filter is formed by transistors M1 and the parallel combination of transistors M2 and M3. While this does increase capacitance along the signal path, there is a larger increase in the transconductance of the combined device, leading to a net increase in the unity-gain frequency.

In each of these frequency bands (i.e., low, mid, and high) the current through the transistors forming the active inductor can be tuned to further adjust the inductance value.

In reality, M4 and M5 are not ideal switches and will have a finite source-drain impedance that increases the noise and the effective loss of the inductor. The latter problem can be dealt with by the negative impedance circuit (NIC) used to enhance the filter's quality factor, which will be described in the next section. The increased noise is a price that must be paid for enhanced tuning range. These transistors will also increase the total capacitance of the circuit, lowering the highest center frequency achievable by the filter.

3.4 Negative Impedance Circuit

One possible realization of a negative impedance circuit is shown in Figure 3.5. The circuit consists of a cross-coupled differential pair [30].

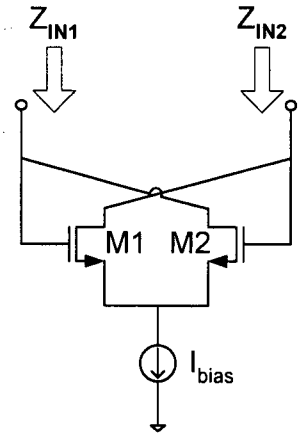

Figure 3.5 - Cross-Coupled Differential Pair NIC Circuit

M1 and M2 should be sized identically, which means

$$Z_{IN1} = Z_{IN2} = -\frac{1}{g_m} \tag{3.12}$$

where the body effect and capacitances have been disregarded. The negative impedance circuit can be modeled as an RC network in parallel with the active filter model, as shown in Figure 3.6.

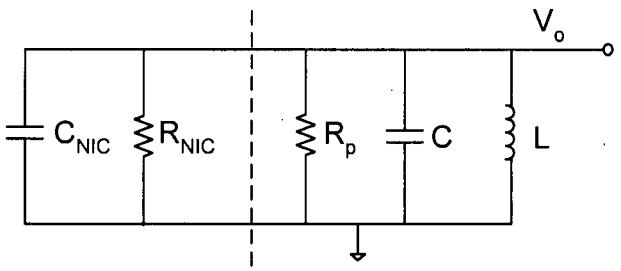

Figure 3.6 - Active Filter Model Including Negative Impedance Circuit

3.5 Active Filter

The circuit schematic of the entire active filter is shown in Figure 3.7 (with DC biasing omitted for brevity).

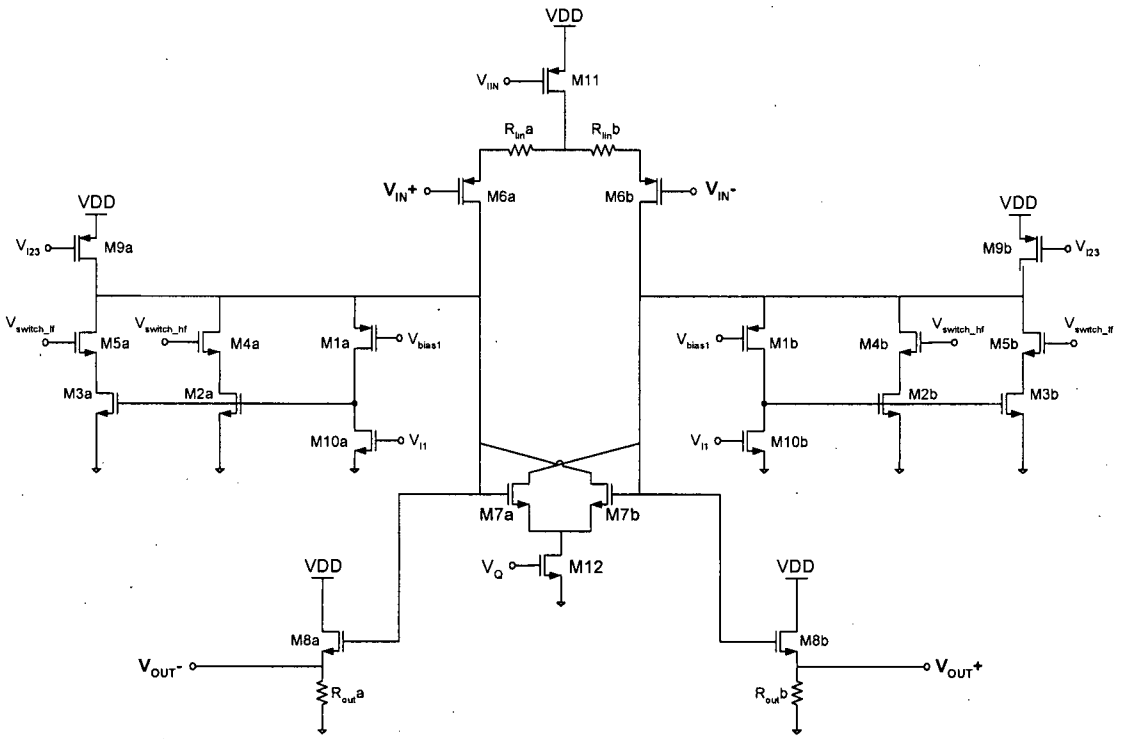

Figure 3.7 - Entire Tunable Filter Schematic

This design is fully differential, which leads to common-mode noise benefits although it doubles the power consumption. Transistors M1a,b – M5a,b form the core of the active filter used in the proposed wideband topology. In this figure, the voltages V_{I23} and V_{I1} are used to tune the current sources M9a,b and M10a,b, respectively. Transistors M7a,b form the cross-coupled differential pair to provide the necessary negative resistance to adjust the quality factor of the filter and this can be tuned by using V_Q to adjust the current through M12. Transistors M6a,b form a differential input pair, and they are biased by M11. This bias current is also reused by the other portions of the circuit to reduce power consumption. To improve the linearity, the input stage also uses the resistors R_{lin}a,b for source degeneration of the differential pair, a technique that will be discussed in Chapter 5. Finally, M8a,b and R_{out}a,b form the differential output buffers. These buffers

are necessary so the circuit can drive the 50Ω load presented by test equipment, and would not be necessary if the filter was integrated with other receiver components.

Initial component values for the transistors forming the active inductor are obtained using the formulas derived in Section 3.2 and simulations are used to fine tune these sizes to achieve the desired centre frequencies. To achieve a wide tuning range, the transistors in the active inductor and NIC must operate in the saturation region for a wide range of bias currents, and their sizes reflect this.

The sizes of the input stage transistors are smaller to account for the relatively high gain of the active inductor at resonance and the size of the degeneration resistors were obtained from the analysis that will be presented in Chapter 5.

The final component sizes are shown in Table 3.1.

Component	Size
M1	60 / 0.18 μm
M2	60 / 0.54 μm
M3	50 / 0.18 μm
M4	20 / 0.18 μm
M5	20 / 0.18 μm
M6	10 / 0.18 μm
M7	40 / 0.25 μm
M8	30 / 0.18 μm
M9	180 / 0.36 μm
M10	20 / 0.36 μm
M11	40 / 0.36 μm
M12	54 / 0.36 μm
Rlin	500 Ω
Rout	150 Ω

Table 3.1 - Component Sizes for Active Filter

DC biasing circuitry is needed only for the input differential pair (M6a,b), its current source (M11) and the common gate transistors in the active inductors (M1a,b). The other voltages are tunable in order to adjust the current through the active inductor

and the negative impedance circuit. The DC biasing circuitry used for M11 and M1a,b is shown in Figure 3.8, and this structure is a supply independent biasing circuit [30].

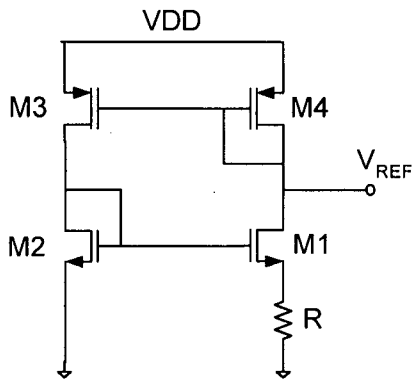

Figure 3.8 - Constant g_m Biasing Circuit

The circuit is made up of two current mirrors which work to bias each other depending on the size ratios and the value of the resistance R. This makes the bias voltage tolerant of power-supply fluctuations although some error is introduced by the process variations in R and the non-equal threshold voltages of transistors M1 and M2 due to the body effect.

To bias the input differential pair of M6a,b, a voltage divider was formed using two diode-connected transistors. If the transistors are sized correctly, the input resistance can be made to equal 50Ω to match the internal impedance of the test equipment and the transistors will produce a more accurate voltage and consume less power than an equivalent voltage divider made up of resistors.

3.6 Simulation Results

Agilent Advanced Design System (ADS) S-Parameter [31] simulations were run to quantify the frequency response of the circuit. Figures 3.9, 3.10, and 3.11 show

operation at the limits of the low, mid, and high frequency bands respectively. In all of these simulations the Q of the filter is approximately 40.

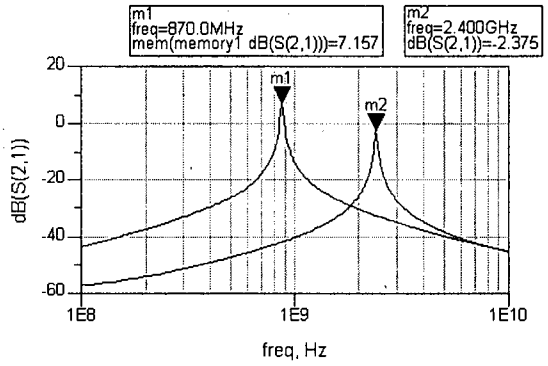

Figure 3.9 - Frequency Operation Limits of the Low-Frequency Band

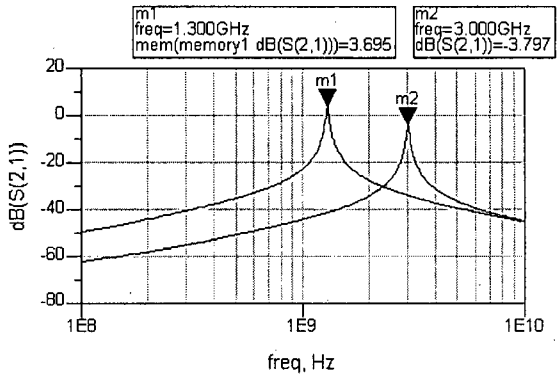

Figure 3.10 - Frequency Operation Limits of the Mid-Frequency Band

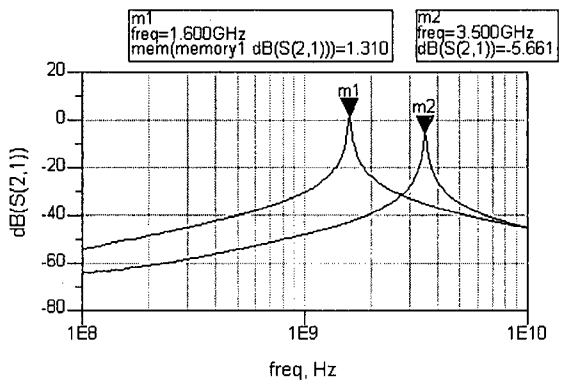

Figure 3.11 - Frequency Operation Limits of the High-Frequency Band

The centre frequency of the filter ranges from 870MHz to 3.5GHz, and the inductance generated ranges from 6nH to 123nH. Over the 2.63GHz tuning range, the filter gain changes by approximately 12.8dB, which is a result of keeping the quality factor of the filter constant. As shown in Chapter 2, for a second-order bandpass filter the following relationship holds between the gain, quality factor, and centre frequency [10]:

$$A_v(\omega_0) \propto \frac{Q}{\omega_0} \tag{3.13}$$

Thus, as the centre frequency is increased while the Q is held constant the gain should drop by 20dB/decade, which is the response seen in the above plots.

The power consumption of the circuit depends mainly on the frequency of operation since higher frequencies require more current to increase the transconductances of the transistors. A plot of the power consumption versus the centre frequency of the filter for all three bands with a Q of 40 is shown in Figure 3.12.

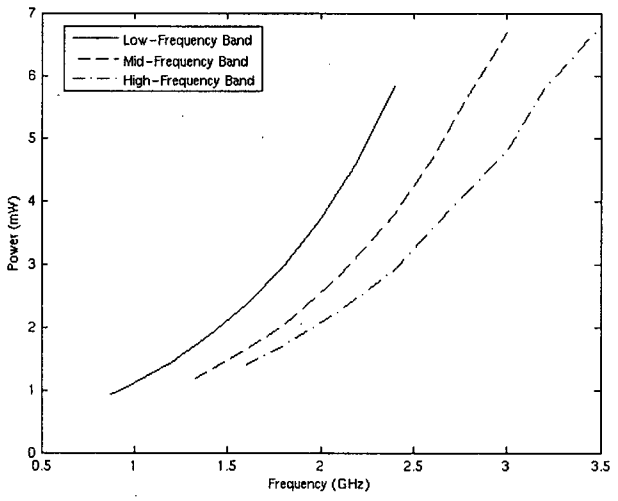

Figure 3.12 - Power Consumption vs. Frequency for all Three Bands of Operation

The power consumption shown is only for one side of the differential filter, and does not include the output buffers or biasing circuitry. It can be seen that the low frequency band consumes less power over its range than the other two bands. This is due to the use of longer channel transistors in the signal path leading to a higher output resistance, decreasing the loss of the inductor. Therefore, the NIC does not need to provide as much negative resistance for a specific filter Q.

The overlap of the three bands can also be used to reduce the power consumption at a given frequency. For instance, the high-frequency band would consume around 1.6mW less to achieve a centre frequency of 2GHz than the low frequency band. However, this approach will have trade-offs with respect to linearity and noise which will be discussed in the following chapters.

Figure 3.13 shows how the power consumption varies with the quality factor of the filter. This simulation was run at a centre frequency of 2.1GHz using the mid-frequency band; however, similar behaviour is seen at all frequencies in all three bands.

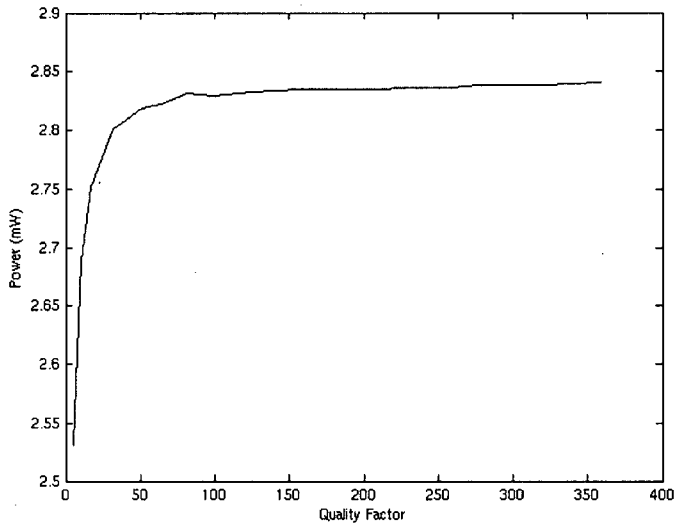

Figure 3.13 - Power Consumption vs. Quality Factor

It can be seen that a larger change in the power consumption is needed to alter the Q of the filter at low values and this is due to the way parallel resistances combine. This is best explained by the plot in Figure 3.14 which shows the equivalent resistance when a 500Ω resistor is combined in parallel with various values of negative resistance.

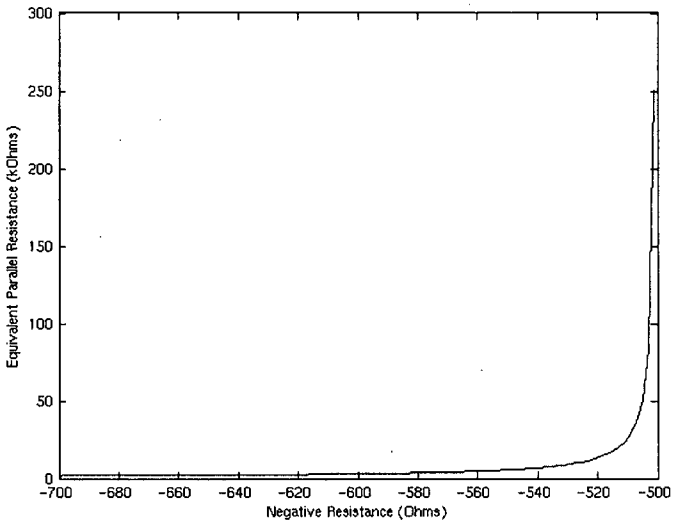

Figure 3.14 - Equivalent Resistance for a Negative Resistor in Parallel with 500Ω

A greater change in the negative resistance is required to create smaller equivalent resistance values. This means that the transconductance of the NIC must be changed by a greater amount to alter the Q of the filter at low values which explains the change in power consumption. However, as seen in Figure 3.13, the power consumption only changes by 0.3mW to achieve a change in Q from 5 to 350.

Figure 3.15 shows how the filter shape changes as the quality factor is tuned.

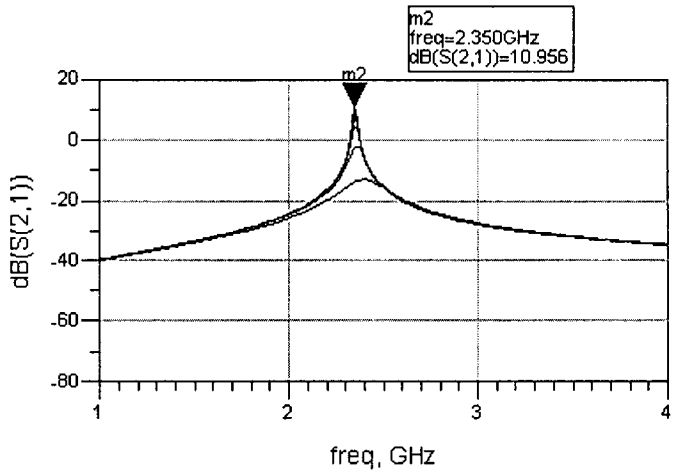

Figure 3.15 - Simulations Showing the Tunable Quality Factor

In this simulation the quality factor ranges from 10 to 200, and it is seen that the centre frequency changes by around 50MHz. This is because the NIC is steering current away from the active inductor, so to keep a constant centre frequency more current needs to be sourced into the circuit. Figure 3.16 shows an example of tuning the quality factor from 10 to 200 while keeping the centre frequency constant.

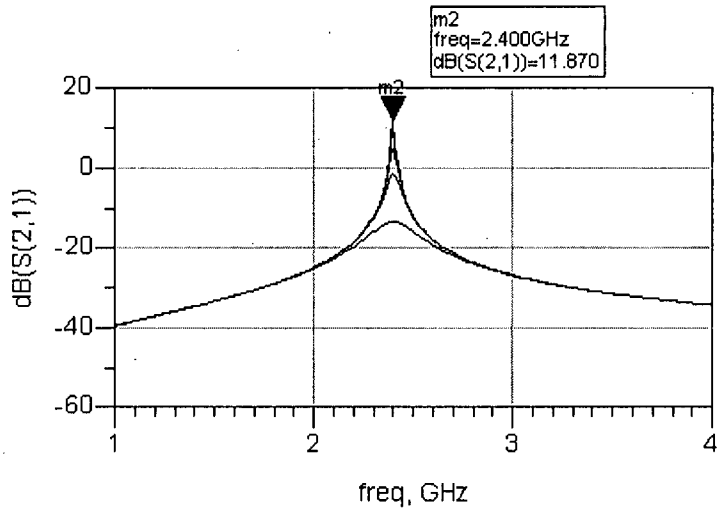

Figure 3.16 – Simulations Showing the Tunable Quality Factor at a Constant Centre Frequency

The gain is seen to change by roughly 24dB, and this effect is more troublesome because it will have a large impact on the linearity of the filter, as we will see in Chapter 5. The reason for the gain change with Q is the same as the predicted by Equation 3.13, and again, the 20dB/decade change agrees with theory.

Now that the frequency response of the filter has been established, the next chapter will analyze its noise behaviour.

Chapter 4

Noise Optimization

4.1 Noise in MOSFETs

The sources of noise in a MOSFET are thermal noise caused by the drain current, gate noise caused by the finite resistance of the gate, shot noise due to the DC gate leakage current (tunneling), and flicker noise which is inversely proportional to frequency [9]. In this work, only thermal noise will be considered since it has the strongest contribution. This noise can be either modeled as a noise current source between the source and the drain, or as an equivalent input-referred noise voltage source at the gate of the transistor. The two possible equivalent MOSFET models are shown in Figure 4.1 [32].

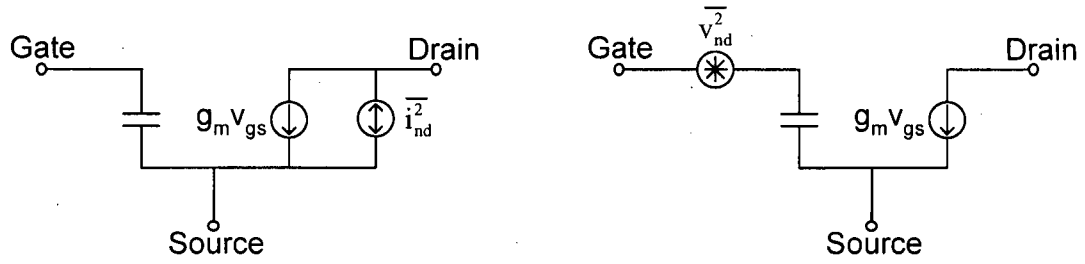

Figure 4.1 - Equivalent MOSFET Noise Models

The equations that define these noise sources are [32]:

$$\overline{i_{nd}^2} = 4kT\gamma g_m$$
$$\overline{v_{nd}^2} = \frac{4kT\gamma}{g_m} \tag{4.1}$$

where k is Boltzman's constant, T is the temperature (in Kelvins), and γ is the thermal noise coefficient (usually around 2/3 in long channel devices and around 4/3 for short channel devices) [9]. The units of noise power from a voltage source are $\overline{V^2}/Hz$, and for a current source the units are $\overline{I^2}/Hz$. These sources give a spectral density value for the noise, so their value must be integrated over bandwidth of the circuit to get the total noise present in the time domain.

In circuit analysis, the square root of these terms must be taken to obtain a voltage or a current. It is also important to realize that noise powers can be added directly (if the sources are uncorrelated), but noise voltages cannot [33].

4.2 Noise Analysis of the Basic Active Inductor Structure

The noise model of the equivalent RLC circuit representing the active inductor is shown in Figure 4.2.

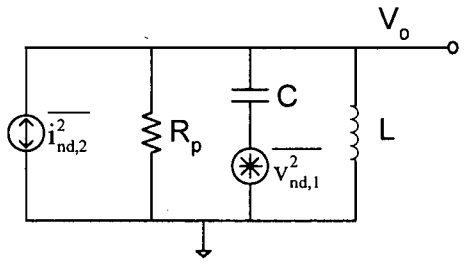

Figure 4.2 - Noise Model for RLC Circuit

where the noise current source is associated with transistor M2 and the noise voltage source is associated with transistor M1. The parameters are given by:

$$\overline{i_{nd,2}^2} = 4kT\gamma g_{m2} \qquad \overline{v_{nd,1}^2} = \frac{4kT\gamma}{g_{m1}} \tag{4.2}$$

$$C = C_{gs1} \qquad R_p = \frac{1}{g_{m1}} \qquad L = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{4.3}$$

This is for the original active inductor circuit, and for a simplified analysis C_{gd} has been neglected and infinite transistor output impedance has been assumed. It should also be noted that the resistor R_p is a fictitious resistor created by modeling of the transistors, therefore its noise has already been taken into account. The noise sources can each be analyzed separately to obtain the total noise of the resonator.

The noise current source sees a parallel RLC, which means the noise transferred to the output at resonance is:

$$\overline{v_{o,n2}} = \overline{i_{nd,2}} R_p \tag{4.4}$$

This noise spectral density is filtered by the RLC network, and the total noise power at the output can be found by multiplying the noise spectral density at the output by an equivalent noise bandwidth [32]. The derivation for the noise bandwidth of a second-order filter is shown in Appendix A, and the result is given by:

$$\Delta f = \frac{1}{2\pi R_p C}\frac{\pi}{2} \tag{4.5}$$

By substituting the transistor parameters for the variables, the total noise power at the output produced by transistor M2 is:

$$\overline{v_{o,n2}^2} = kT\gamma \frac{g_{m2}}{g_{m1}C_{gs1}} \tag{4.6}$$

The noise voltage source sees a series-parallel RLC circuit, and the total noise transferred to the output at resonance is given by:

$$\overline{v_{o,n1}} = \overline{v_{nd,1}} R_p \sqrt{\frac{C}{L}} \tag{4.7}$$

The equivalent noise bandwidth in this case is also given by Equation 4.5, which means the total noise power at the output produced by transistor M1 is:

$$\overline{v_{o,n1}^2} = kT\gamma \frac{g_{m2}}{g_{m1}C_{gs2}} \tag{4.8}$$

The total noise power at the output is given by:

$$\overline{v_{o,n}^2} = \overline{v_{o,n1}^2} + \overline{v_{o,n2}^2} = kT\gamma \left(\frac{1}{C_{gs1}} + \frac{1}{C_{gs2}} \right) \frac{g_{m2}}{g_{m1}} \tag{4.9}$$

This indicates that larger capacitors will decrease the noise. However, larger capacitors also reduce the maximum operation frequency of the circuit. Another interesting conclusion involves the term g_{m2}/g_{m1}. This was the same term that appeared in the expression for Q (Equation 2.11), which means that increased selectivity of the filter will also lead to increased noise [17, 22]. This allows us to rewrite the noise equation as:

$$\overline{v_{o,n}^2} = kT\gamma \left(\frac{1}{C_{gs1}} + \frac{1}{C_{gs2}} \right) \frac{C_{gs2}}{C_{gs1}} Q^2 \tag{4.10}$$

4.3 Noise Analysis Including Negative Resistance

As seen in the last chapter, a NIC is used to enhance the Q of the filter. Since this parameter strongly influences the noise of the active filter, an analysis including the NIC must be performed. The noise model for the active inductor circuit and the NIC is shown in Figure 4.3.

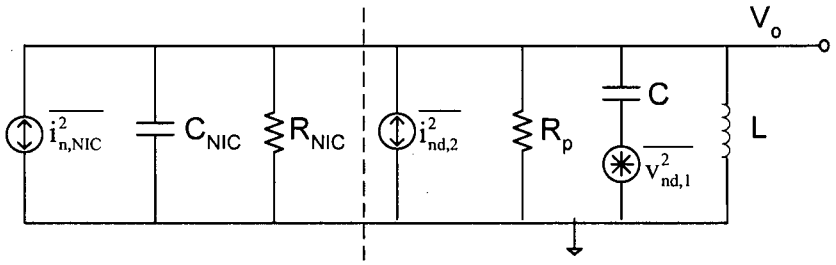

Figure 4.3 - Noise Model for RLC and NIC Circuits

R_{NIC} is the negative resistance caused by the NIC, C_{NIC} is the associated capacitance, and the noise from the NIC has been modeled by a noise current source whose value is given by [17]:

$$\overline{i_{n,NIC}^2} = 4kT\xi g_{NIC} \tag{4.11}$$

where ξ is the noise coefficient for the NIC and g_{NIC} is the associated transconductance. Since a capacitance has been added, the center frequency of the filter will be lowered. The new center frequency is given by:

$$\omega_c = \frac{1}{\sqrt{L(C+C_{NIC})}} = \sqrt{\frac{C}{C+C_{NIC}}}\omega_o = \alpha\omega_o \tag{4.12}$$

where ω_o is the center frequency when the NIC is not present, and α represents the multiplier that lowers the center frequency. The quality factor without the NIC was found earlier, and is re-written here with the substitution of $R_p = 1/g_{m1}$.

$$Q_o = \frac{1}{g_{m1}}\sqrt{\frac{C}{L}} \tag{4.13}$$

The quality factor including the NIC is given by:

$$Q_N = \frac{1}{g_{m1} - g_{NIC}}\sqrt{\frac{C + C_{NIC}}{L}} \tag{4.14}$$

This equation can be solved for g_{NIC}, and the result is:

$$g_{NIC} = g_{m1}\left(1 - \frac{Q_o}{\alpha Q_N}\right) \tag{4.15}$$

which can now be used in the noise current source of the NIC circuit. The noise contribution for each of the three noise sources is found in the same way as before, except the added capacitance and resistance of the NIC is now accounted for. The results after some algebra are:

$$\begin{aligned}
\overline{v_{o,n1}^2} &= kT\gamma Q_o Q_N \alpha \frac{1}{C_{gs2}} \\
\overline{v_{o,n2}^2} &= kT\gamma Q_o Q_N \alpha^3 \frac{C_{gs2}}{C_{gs1}^2} \\
\overline{v_{o,NIC}^2} &= kT\xi\left(\frac{Q_N}{Q_o}\alpha - 1\right)\frac{\alpha^2}{C_{gs1}}
\end{aligned} \tag{4.16}$$

One conclusion from these equations is that a larger capacitance can decrease the noise, but at the expense of a lower obtainable center frequency. We can also see that the noise from all three sources is proportional to Q_N, the quality factor of the overall filter. However, the noise from the active inductor is proportional to Q_o, and the noise from the NIC is proportional to $1/Q_o$. This can be explained as follows:

- A large Q_o means that the active inductor is contributing more to the selectivity of the filter, and thus producing more noise. At the same time less negative

resistance is needed to enhance the selectivity to reach Q_N, therefore the NIC produces less noise.

- A small Q_o means the active inductor is not contributing much to the selectivity of the filter, so it produces less noise. In this case the NIC must provide a lot of enhancement to reach the desired Q_N, which causes it to produce more noise.

Based on the above reasoning, there is an optimal point at which the total noise contribution is minimized. MATLAB was used to plot these equations using the parameters shown in Table 4.1.

Parameter	Value
k	1.381×10^{-23} J/K
T	298°K
γ	4/3
ξ	3
C_{gs1}	100fF
C_{gs2}	250fF
C_{NIC}	60fF
Q_N	40
Q_o	Swept from 0.1 to 5

Table 4.1 - Parameters for Noise Equations

These parameters take short channel device characteristics into account, and the capacitances were obtained from preliminary simulations. The total system Q is fixed at 40 and the selectivity contribution from the active inductor is swept. The results are shown in Figure 4.4, and the noise power obtained is referred to the input to account for the gain of the filter.

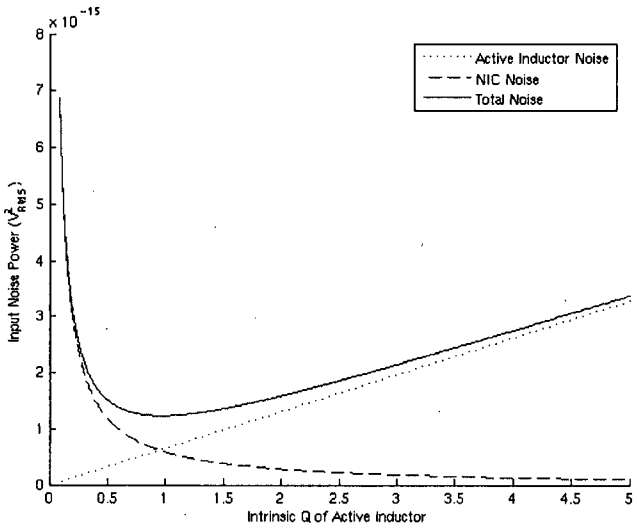

Figure 4.4 - Noise Power vs. Intrinsic Active Inductor Quality Factor. (Total Q = 40)

It can be seen from this figure that the minimum total noise is obtained when the noise from the active inductor circuit equals the noise from the NIC. This happens when the intrinsic Q (Q_o) is equal to 0.87, which means the NIC is providing appreciable enhancement. However, it is seen that below this point the total noise increases rapidly due to an increase in the necessary enhancement from the NIC. To avoid operation in this region, the design goal for the intrinsic Q of the active inductor should be chosen to be larger than 0.87 (e.g., between 1 and 1.5).

Figure 4.5 shows a comparison of the input referred noise produced by the active inductor with and without the NIC as a function of the total filter Q.

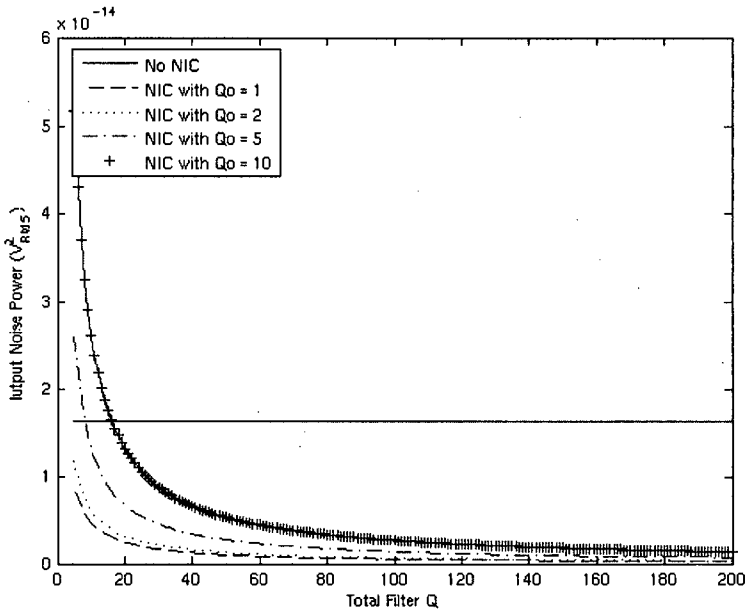

Figure 4.5 - Comparison of Active Inductor With and Without NIC

It can be seen that for low Q values, the active inductor with NIC compensation may perform worse due to the extra noise produced by the NIC. However, as the Q increases the active inductor with NIC compensation produces less noise. And, as expected from the plot shown in Figure 4.4, the circuit with NIC compensation and a lower intrinsic inductor Q does produce less noise than when the inductor has a higher intrinsic Q.

By analyzing the equations used to plot this graph, the reason for this noise advantage can be quantified. Without using NIC compensation, the noise of the active inductor increases as a function of Q^2. By keeping the intrinsic Q of the active inductor constant and using the NIC to achieve the desired overall Q, the noise increases linearly.

4.4 Simulation Results

Simulation results were used to verify the theory developed in the last section. Figure 4.6 shows a plot of the input referred noise for various active inductor intrinsic Q values. The centre frequency is kept constant and the total Q of the circuit is fixed at 40.

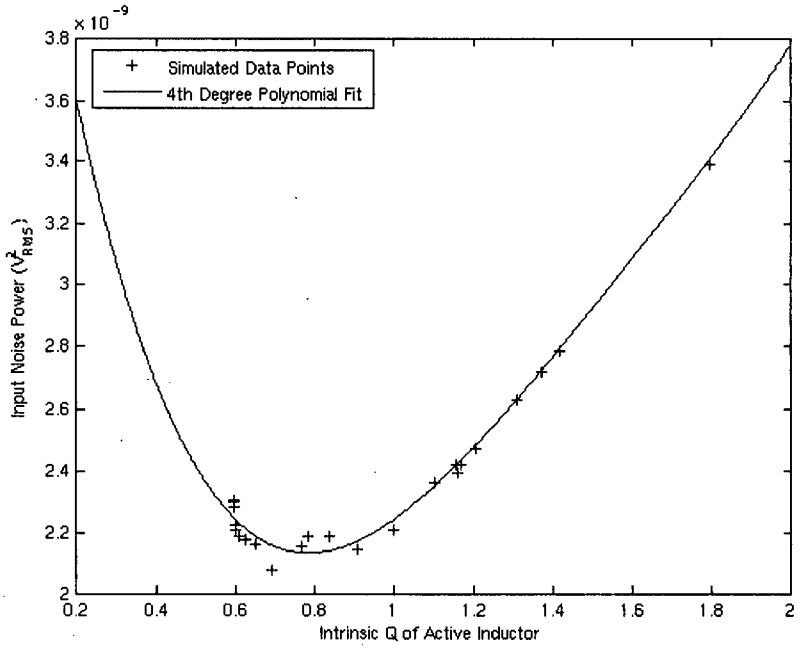

Figure 4.6 - Simulation Results for Noise Power vs. Intrinsic Active Inductor Quality Factor. (Total Q = 40)

MATLAB was used to fit a 4th degree polynomial to the points, and the resulting curve looks very similar to the one obtained from theory in Figure 4.5. The optimal point for the intrinsic Q of the active inductor is around 0.8, which also agrees closely with the presented theory. The simulated noise power is higher than that obtained from the theoretical analysis because the entire filter was simulated, not just the active inductor itself.

Simulations were also run to determine the noise behaviour as a function of total Q. Figure 4.7 shows one such simulation at a centre frequency of 3.1 GHz.

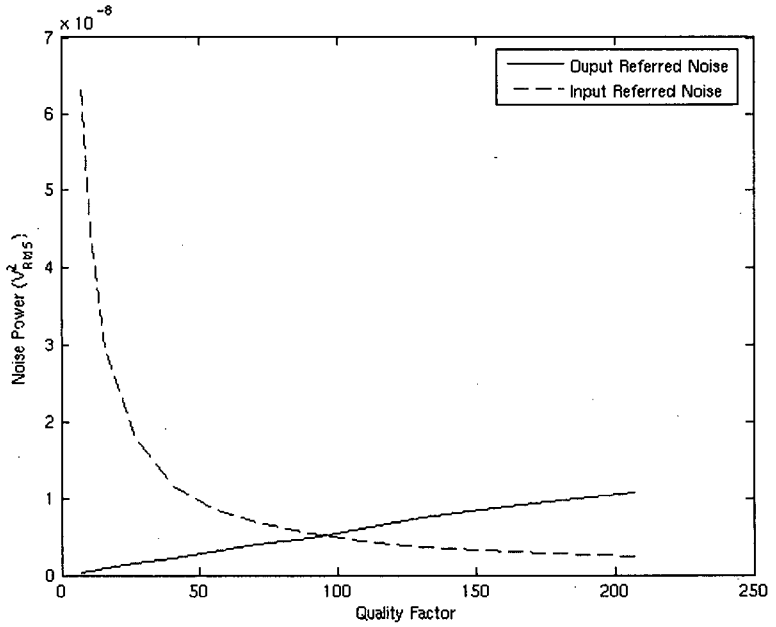

Figure 4.7 - Simulation Results of Input- and Output-Referred Noise vs. Quality Factor

It can be seen that the output-referred noise does indeed increase linearly as expected, but that there is an exponential decrease in the input-referred noise. This is due to the exponential increase in the gain of the circuit as a function of Q. This is a very important result because the noise power referred to the input of the circuit determines the amplitude of the minimum detectable signal [33]. From that point of view it is best to have a circuit with a high gain, however, there is a trade-off between the smallest detectable signal and the largest signal that can be applied without adverse effects [34], as we will see in the next chapter.

Figure 4.8 shows how the input referred noise power changes with frequency in each of the three bands of operation. The filter Q is fixed at 40.

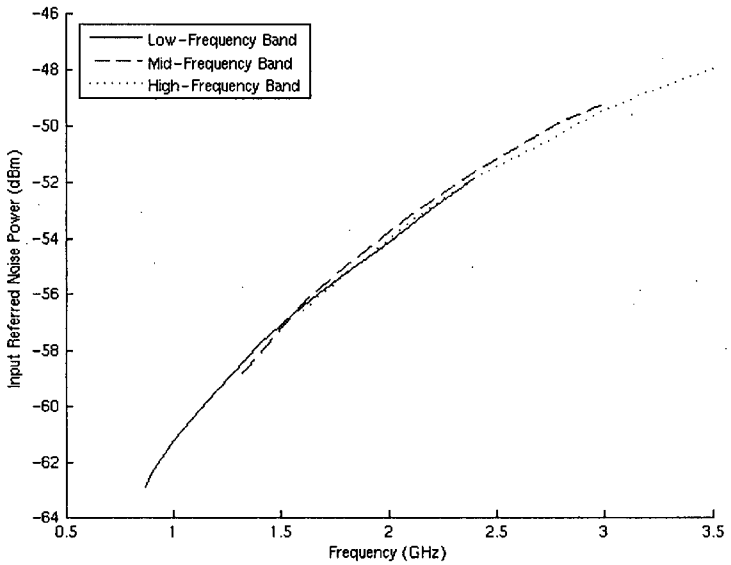

Figure 4.8 – Input-Referred Noise Power vs. Frequency for all Three Bands

The input referred noise power increases with frequency, and this is mainly because the gain of the filter decreases as the centre frequency is increased and the quality factor remains the same. Over all three bands, the input referred noise floor ranges from -63dBm to -48dBm, and these numbers correspond to the minimum detectable signal at the input. The upper limit on signal amplitude is governed by the linearity of a circuit, and this will be discussed in the next chapter.

Chapter 5

Large-Signal Performance

5.1 Range of Tuning Voltage

In order to design a widely tunable filter, the range of bias voltages necessary for proper circuit operation must be maximized. This gives a larger range for the transconductance of the transistors, which allows for a larger range of inductance values. By analyzing the structure of Figure 5.1, the maximum and minimum DC voltage at the node V_{IN} can be determined.

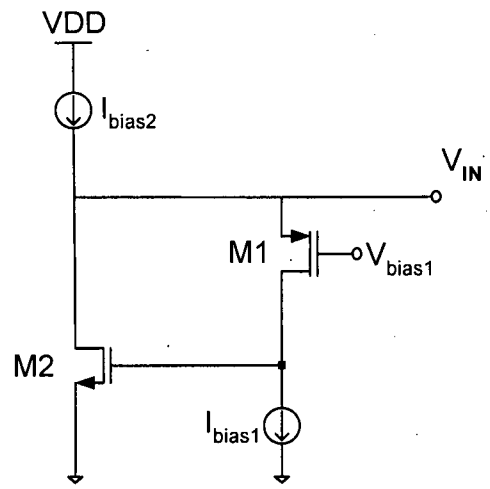

Figure 5.1 - Basic Active Inductor Circuit

The maximum DC voltage at the node V_{IN} is limited to that needed to keep the current source I_{bias2} in saturation, which gives the equation:

$$V_{IN,\max} = V_{DD} - V_{dsat,Ibias2} \tag{5.1}$$

Using Kirchhoff's Voltage Law (KVL) several expressions can be written to determine the minimum DC voltage at the node V_{IN}:

$$\begin{aligned} V_{IN,\min} &= V_{dsat,M2} \\ V_{IN,\min} &= V_{dsat,M1} + V_{dsat,Ibias2} \\ V_{IN,\min} &= V_{bias1} + V_{th,M1} \\ V_{IN,\min} &= V_{dsat,M1} + V_{th,M2} \end{aligned} \tag{5.2}$$

The bottom two equations are the most restrictive in terms of the minimum allowable V_{IN}, however, since the voltage V_{bias1} can be selected as any value it is the bottom equation that is the most important. Thus, the bounds on V_{IN} are:

$$V_{dsat,M1} + V_{th,M2} < V_{IN} < V_{DD} - V_{dsat,Ibias2} \tag{5.3}$$

Assuming the voltages needed to keep transistors in saturation is roughly 300mV and the threshold voltage is roughly 500mV, the maximum range of voltages at the node V_{IN} is around 700mV in a 0.18μm CMOS technology.

5.2 Linearity

The linearity of a circuit is a measure of the distortion it adds to the input signal. The current through an NMOS transistor in saturation (neglecting channel length modulation) can be modeled by the equation [30, 35]:

$$I_{DS} = WC_{ox}v_{sat}\frac{(V_{GS}-V_{th})^2}{(V_{GS}-V_{th})+2\frac{v_{sat}L}{\mu_{eff}}} \tag{5.4}$$

where C_{ox} is the oxide capacitance, W is the width of the transistor, L is the length of the transistor, v_{sat} is the saturation velocity, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, and μ_{eff} is the effective mobility of electrons. In long channel devices, or for short channel devices with a small overdrive voltage, this equation reduces to:

$$I_{DS} = \frac{W}{L}\frac{C_{ox}\mu_{eff}}{2}(V_{GS}-V_{th})^2 \tag{5.5}$$

which is the familiar square-law current equation. In short channel devices velocity saturation effects are more pronounced due to the large horizontal and vertical electric fields and the I-V characteristic becomes more linear [30, 35]. Nevertheless, a MOSFET is a nonlinear device and when multiple tones are passed through a MOS transistor, spurious emissions occur through intermodulation [9]. This term is defined as a process where multiple signals mix together in a nonlinear circuit to create undesired output frequencies that were not present at the input.

Of particular importance are the third-order intermodulation products because they are most likely to appear in the frequency band of interest. If two signals at closely spaced frequencies f_1 and f_2 pass through a nonlinear block the frequencies of the third-order distortion signals that result will be given by the sum and difference frequencies [9]:

$$f_{out} = \begin{cases} 2f_1 + f_2 \\ 2f_2 + f_1 \\ 2f_1 - f_2 \\ 2f_2 - f_1 \end{cases} \tag{5.6}$$

The first two frequencies can often be filtered out; however, the second two may fall directly in the band of interest and can interfere with the desired signal. This is shown graphically in Figure 5.2.

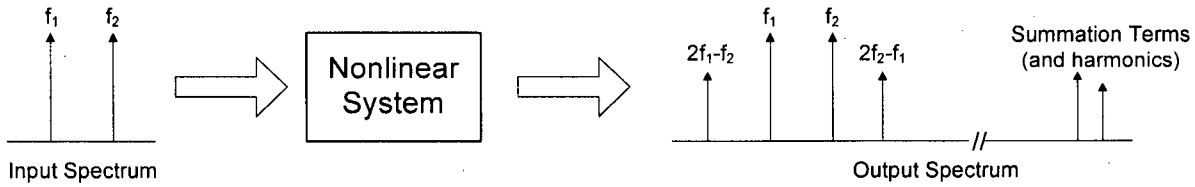

Figure 5.2 - Graphic Example of Intermodulation

This is especially detrimental in a filter, whose main purpose is to remove unwanted signals. The amount of intermodulation distortion produced by a circuit is quantified by the third-order intercept point. This is the point where the extrapolated linear output curve crosses the extrapolated linear third-order intermodulation curve, as illustrated in Figure 5.3 [9, 33, 36].

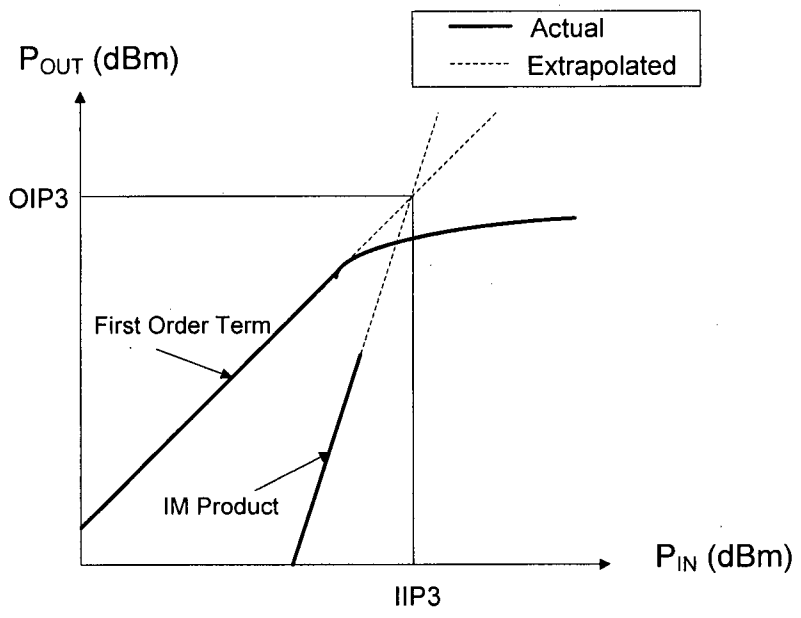

Figure 5.3 - Graphical Definition of Third Order Intercept Point

Typically the input third-order intercept point (IIP3) is used because it quantifies the largest signal that can be tolerated at the input to the circuit. This point can be obtained from the output spectral plot of Figure 5.2 via the following formula [36]:

$$IIP3 = P_{IN} + \frac{P_{fund} - P_{IM\_Product}}{2} \tag{5.7}$$

where P_{IN} is the input power of the two tones, P_{fund} is the output power of either fundamental tone, and $P_{IM\_Product}$ is the output power of either third-order intermodulation product. This formula assumes that the two input signals are at the same power level and that the circuit is operating in the linear region of the curves in Figure 5.3.

5.3 Improving Linearity

One of the causes of nonlinear distortion in a MOSFET is the result of an AC input changing the DC operating point of a transistor. By examining the I_{DS} vs. V_{GS} characteristic, insight into how to reduce the nonlinearity of a circuit can be obtained. Figure 5.4 shows the I-V characteristic obtained from a transistor in the 0.18μm CMOS process used in this work. V_{DS} is fixed at 1.2V, the W/L ratio is fixed at 10, and the response is shown for various lengths (in μm).

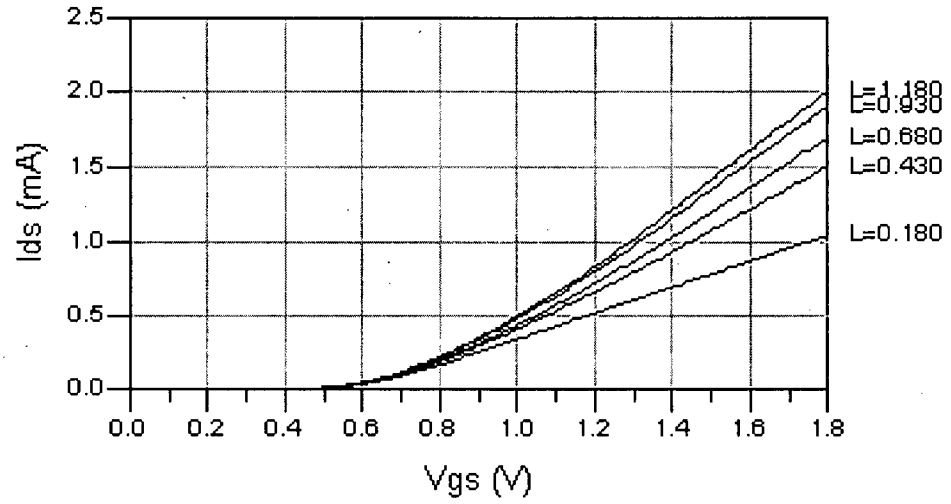

Figure 5.4 - I_{DS} vs. V_{GS} for Different Channel Lengths

As the length decreases, the response at larger V_{GS} values becomes more linear. Operating in this range will help reduce intermodulation distortion because the transconductance of the transistor will not be as dependent on the gate-source voltage.

As mentioned earlier, nonlinearities are caused by changes in the transistor's DC operating point, which will always occur when an AC input is present. Operating at low values of V_{GS} should be avoided since the current is approximated by a square-law, therefore, a change in the operating point will cause more nonlinearities. The relative change in operating point can also be reduced by biasing the transistor with a larger DC current. This can be shown by first solving the long-channel drain current equation for V_{GS}, which gives:

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\mu_n C_{ox}} \frac{L}{W}} + V_{th} \tag{5.8}$$

Taking the partial derivative of this with respect to I_{DS} gives:

$$\frac{\partial V_{GS}}{\partial I_{DS}} = \sqrt{\frac{1}{I_{DS}} \frac{1}{2\mu_n C_{ox}} \frac{L}{W}} \tag{5.9}$$

Thus, the change in V_{GS} caused by a change in I_{DS} is divided by the square root of the DC current through the transistor. This means that a larger current makes the circuit more linear, but at the expense of higher power dissipation.

Source degeneration is another way to improve the linearity of a transistor [37], and this was the technique used in the input differential pair of the tunable filter. To see how this works we will consider the simple differential pair shown in Figure 4.5.

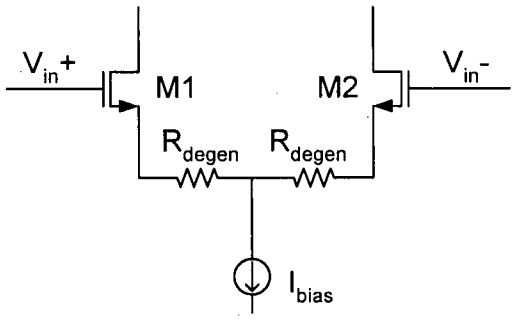

Figure 5.5 - Differential Pair with Source Degeneration

The source degeneration resistors act as a negative feedback mechanism to increase the linear range of the differential pair. If a positive differential signal is applied to the circuit, more current will pass through M1 than M2. Since this current also passes through R_{degen}, the voltage drop across it will increase causing a smaller change in V_{GS1} than usual. This serves to keep the operating point of the transistor relatively constant, thus improving the linear range. However, the total available transconductance of the differential pair will change according to the equation (ignoring the body effect) [34]:

$$G_{diff} = \frac{G_m}{1 + \frac{G_m R_{degen}}{2}} \tag{5.10}$$

where G_m corresponds to the transconductance of the differential pair without source degeneration. This shows that source degeneration causes a decrease in the gain of the differential pair. Figure 5.6 shows simulation results of the circuit in Figure 5.5 to illustrate the effects of source degeneration.

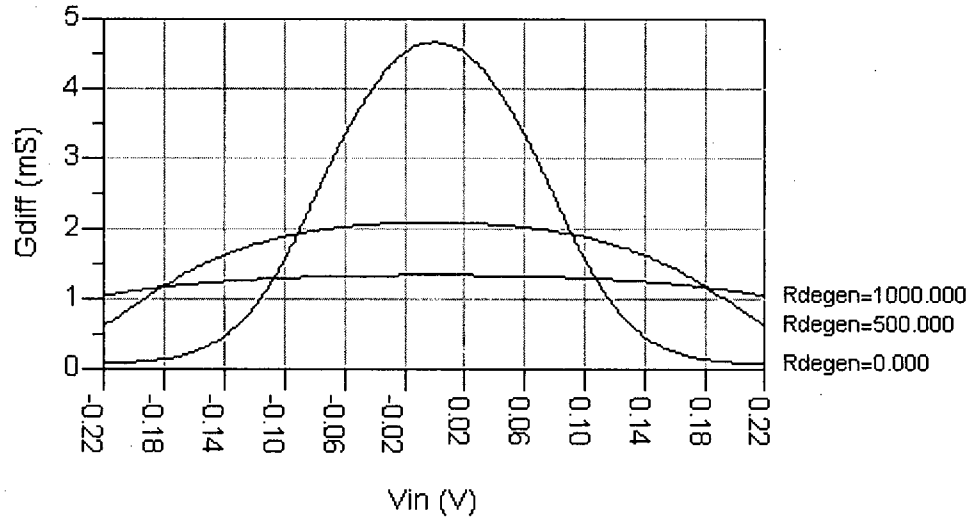

Figure 5.6 - G_{diff} vs. V_{in} for Different Source Degeneration Resistors

It can be seen that the total transconductance does decrease as the degeneration resistance increases, however it is fairly constant over a larger input voltage range which improves the linearity of the circuit.

It should be noted that this technique cannot be used as effectively on the cross-coupled differential pair that makes up the NIC [34]. The negative resistance is caused by the overall transconductance of the cross-coupled pair and since source degeneration decreases this parameter, a larger current would be needed to obtain the desired compensation. There are techniques to increase the linear range that do not suffer from this problem such as an unbalanced differential pair [38], which is the equivalent of a

multi-tanh circuit [39] in a bi-polar process. However, it will be shown in the next section that the NIC does not play a significant role in the nonlinearity of the filter.

5.4 Simulation Results

Simulation results of the filter's IIP3 are shown for each frequency band in Figure 5.7. For these simulations the overall filter Q fixed at 40.

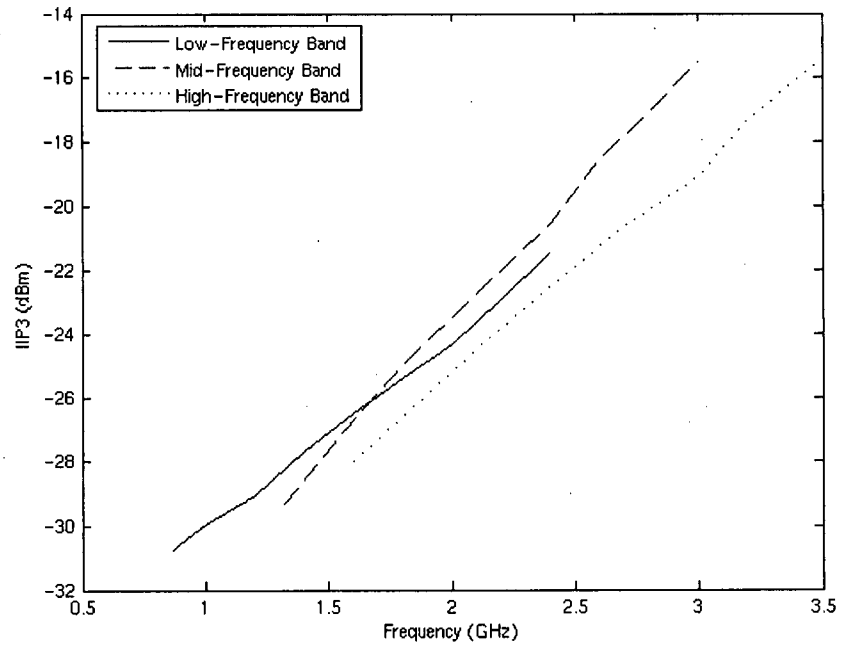

Figure 5.7 - IIP3 Simulation Results for all Three Frequency Bands

This figure shows that the IIP3 ranges from -31dBm to -16dBm. The low-frequency band offers the worst performance in terms of linearity, and this is because the longer channel device suffers from a more quadratic I-V characteristic.

In order to improve linearity, it is important to ascertain which part of the circuit is responsible for the nonlinearities. First the input stage will be dealt with, and

simulation results are presented with and without source degeneration. Furthermore, simulations were run with the ideal input stage shown in Figure 5.8.

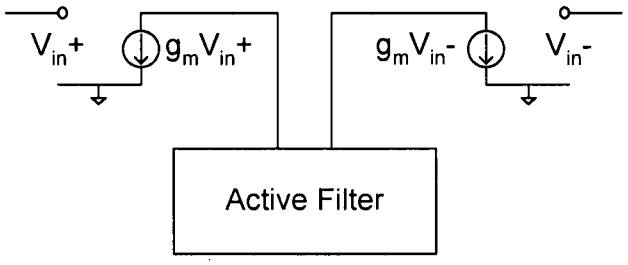

Figure 5.8 - Ideal Input Differential Pair

In this figure the input stage functions as a perfectly linear voltage-controlled current source (VCCS) and appropriate capacitances were added in to account for the capacitance of the PMOS differential pair input stage. The simulation results are shown in Figure 5.9.

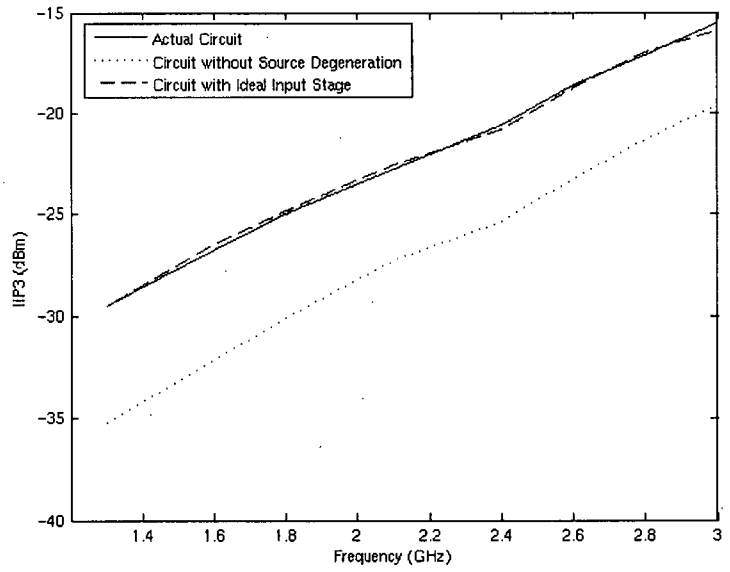

Figure 5.9 - IIP3 Simulation Results with Different Input Stages

This figure shows that the source degeneration of the input stage improves the IIP3 by around 5dBm. Also, since the IIP3 is the same for the ideal input stage and the

real circuit with source degeneration, the input stage is not a primary cause of nonlinearities in the circuit.

The same idea was used to see if the NIC is responsible for the nonlinear behavior using the ideal NIC shown in Figure 5.10.

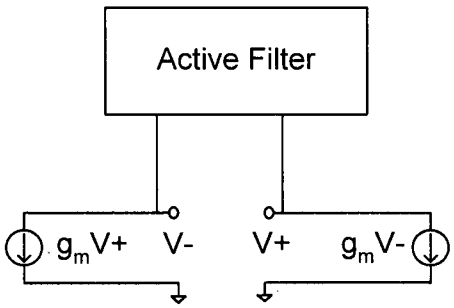

Figure 5.10 - Ideal Cross-Coupled Differential Pair for the NIC

Again, proper capacitances were added to each side to simulate the real NMOS cross-coupled differential pair. The simulation results are shown in Figure 5.11.

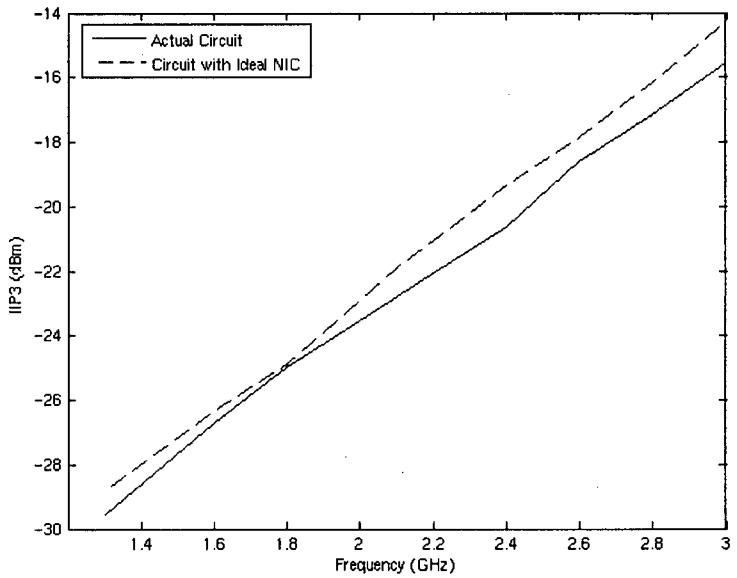

Figure 5.11 - IIP3 Simulation Results with NICs

This figure shows that less than 1dB of improvement could be obtained by implementing a NIC with greater linearity. Thus, it is the active inductor itself that is contributing most of the nonlinearities and one reason is because the transconductors in the active inductor consist of only a single transistor. One solution would be to replace the transistors in the active inductor with more linear transconductors, but the added complexity would increase the capacitance of the structure, decreasing the maximum possible operating frequency [16]. It would also create problems with having enough voltage headroom to keep the transistors in saturation and still obtain a large tuning range.

The area of linearity in active inductor design still needs to be investigated further, especially since a passive inductor does not suffer from this shortcoming.

5.4.1 Spurious Free Dynamic Range

The spurious free dynamic range (SFDR) of a circuit gives the range of input signals that are large enough to be detectable, but small enough to not cause distortion. In RF applications the definition for SFDR is the signal-to-noise ratio corresponding to the input amplitude at which the third-order intermodulation power equals the noise power [9]. The formula for calculating the SFDR is given by [9]:

$$SFDR = \frac{2}{3}(IIP3 - N_i) \tag{5.11}$$

where N_i is the input referred noise power. The concept of SFDR is extremely useful due to the trade-off between noise, linearity, and gain. Improving the noise performance of a circuit by increasing the gain will degrade the linearity performance, however the SFDR

will stay fairly constant. This enables a designer to determine whether or not the overall circuit performance has been improved instead of just one parameter. Using the IIP3 results in Figure 5.7 and the input-referred noise power results in Figure 4.8, the SFDR was calculated and plotted for each frequency band. The results are shown in Figure 5.12.

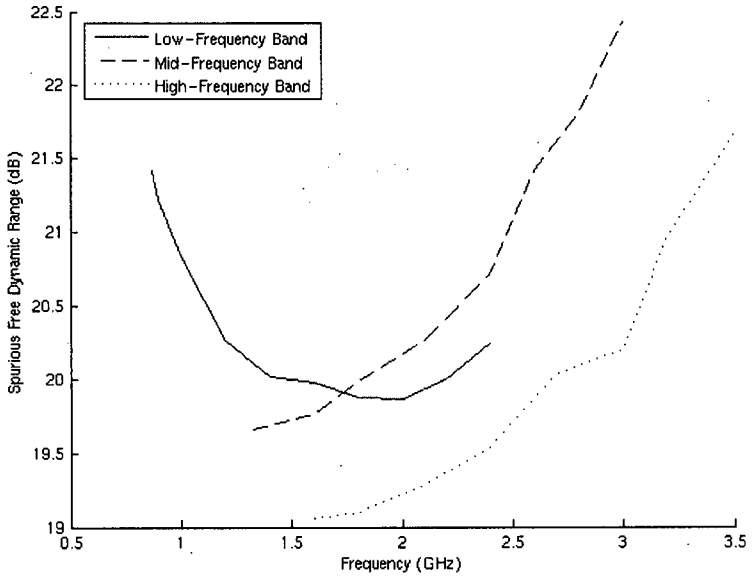

Figure 5.12 – Spurious Free Dynamic Range vs. Frequency

The SFDR of the circuit ranges from around 19dB to 22.5dB. It is interesting to note that over this frequency range the IIP3 and the input-referred noise power change by 15dB, however, the SFDR only changes by 3.5dB. This shows that the SFDR stays fairly constant by incorporating both metrics.

Chapter 6

Layout Techniques and Chip Testing

6.1 Layout Issues

The tunable filter is laid out in a 6 metal 0.18μm CMOS process using the Cadence Virtuoso layout tool. Careful layout techniques are always required for a high-performance circuit, especially for high-frequency and differential designs. The technique of gate-splitting can be used to address both of these issues [40]. This method involves splitting a large transistor into multiple parallel transistors, as shown in Figure 6.1.

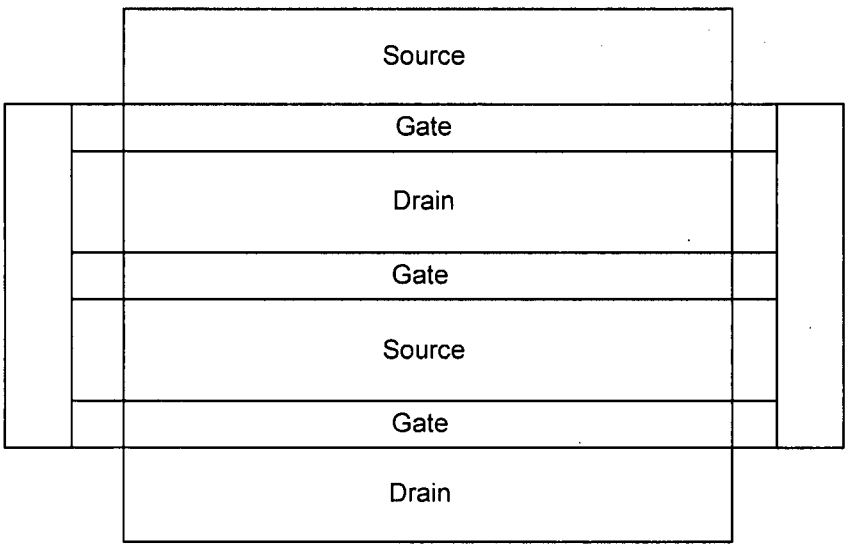

Figure 6.1 – Illustration of Gate-Splitting

In this figure a transistor has been split into 3 fingers, typically around 5μm wide in a 0.18μm CMOS process. This serves to reduce the gate resistance of the device, improving the high-frequency and noise response of the circuit. Metal (as opposed to polysilicon) should be used to tie both sides of the three gates together to further reduce gate resistance and, of course, the sources and drains of each parallel device should be connected.

The main issue in differential design is matching, i.e., to ensure that both halves of the circuit undergo the same process and temperature variations. In layout, this is called matching the devices. If two differential transistors share the same drain or source terminal, the technique of gate-splitting can be used to interdigitate the transistors [40]. An example of this is shown in Figure 6.2.

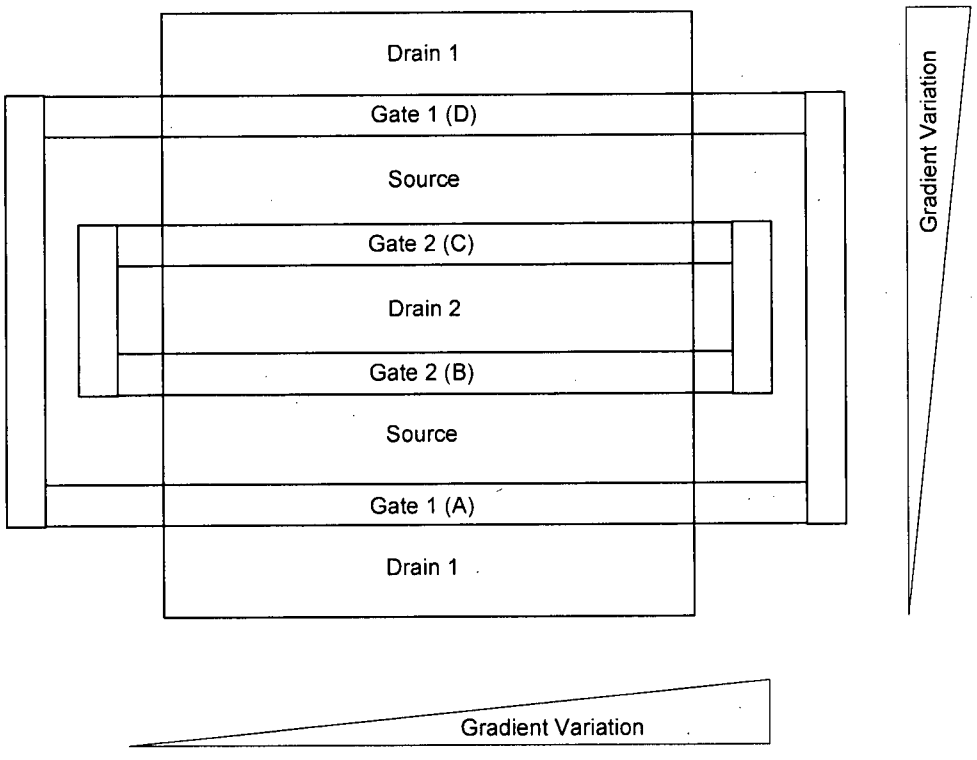

Figure 6.2 – Illustration of Interdigitation and Process Variation Gradients

In this figure both transistors share a common source, such as in a differential pair. This technique also has the benefit of reduced capacitance since both transistors share a common diffusion area. Linear gradients and gate labels have been added to the diagram to illustrate how this structure protects against process variations. In the horizontal direction it is easy to see that both transistors will experience the same changes due to the gradient. To illustrate how the structure is relatively gradient independent in the vertical direction, we will assign numbers representing the size of the variation. Table 6.1 shows the magnitude of variation applied to each transistor gate, which are only valid if the gates are equally spaced.

Gate Label	Variation Magnitude
A	1
B	2
C	3
D	4

Table 6.1 – Variation Applied to Each Gate in Figure 6.2

The total variation applied to each transistor is the sum of the variations on each gate belonging to that transistor. Gates A and D compose transistor 1 and gates B and C compose transistor 2, which means the total variation in the vertical direction for both transistors will be 5. This structure can be repeated as many times as necessary to obtain the desired transistor size. Efforts should also be made to make the entire structure as square as possible to protect against process variations in the diagonal direction.

If the two differential transistors do not share a common source or a common drain, such as in a differential pair with source degeneration, interdigitation cannot be

used. In this case the common centroid layout technique [40] must be used, as illustrated in Figure 6.3.

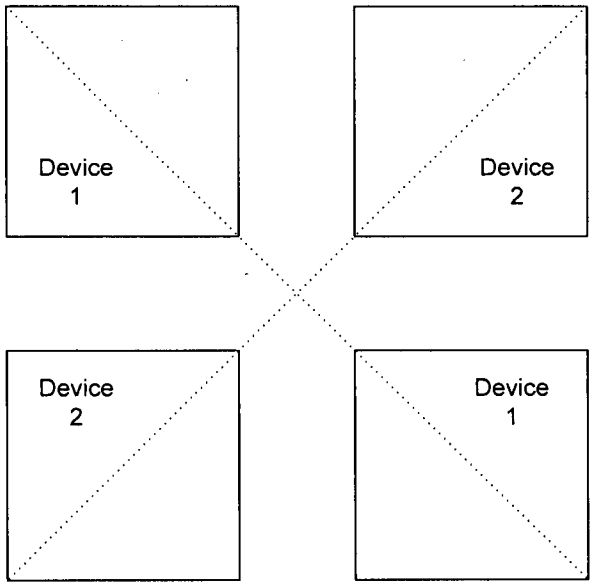

Figure 6.3 – Common Centroid Layout

The layout of each device should use the technique of gate-splitting if the transistors are large enough to warrant it. By performing the same simplistic process variation analysis as the one above, it can be seen that the devices in this structure will undergo the same changes in the case of linear horizontal, vertical, and diagonal gradients. The downside of using this structure is the greater amount of connections that must be made to connect the parallel transistors together.

The common-centroid technique can also be used to match passive devices such as resistors, and this was the approach used in this design. However, it should be noted that if large resistors are used, they should be laid out in a serpentine fashion [40]. Matching of these structures is possible using a technique similar to interdigitation, and the final layout should be as square as possible.

Other fairly universal layout practices used are to keep trace lengths to a minimum to reduce parasitic resistances and to overlap different metal layers as little as possible to reduce parasitic capacitances. When multiple metal layers are used it is also a good idea to connect them with multiple vias in order to reduce parasitic via resistance, and to ensure functionality if some vias do happen to fail [40]. Longer traces, such as those going to pads, should be routed with a wide trace of upper-level metal because these layers are thicker than the lower metal layers [35]. This reduces both parasitic resistance and capacitance. Substrate contacts are also placed close to all active devices to ensure a proper body bias.

The final layout of the active inductor is shown in Figure 6.4.

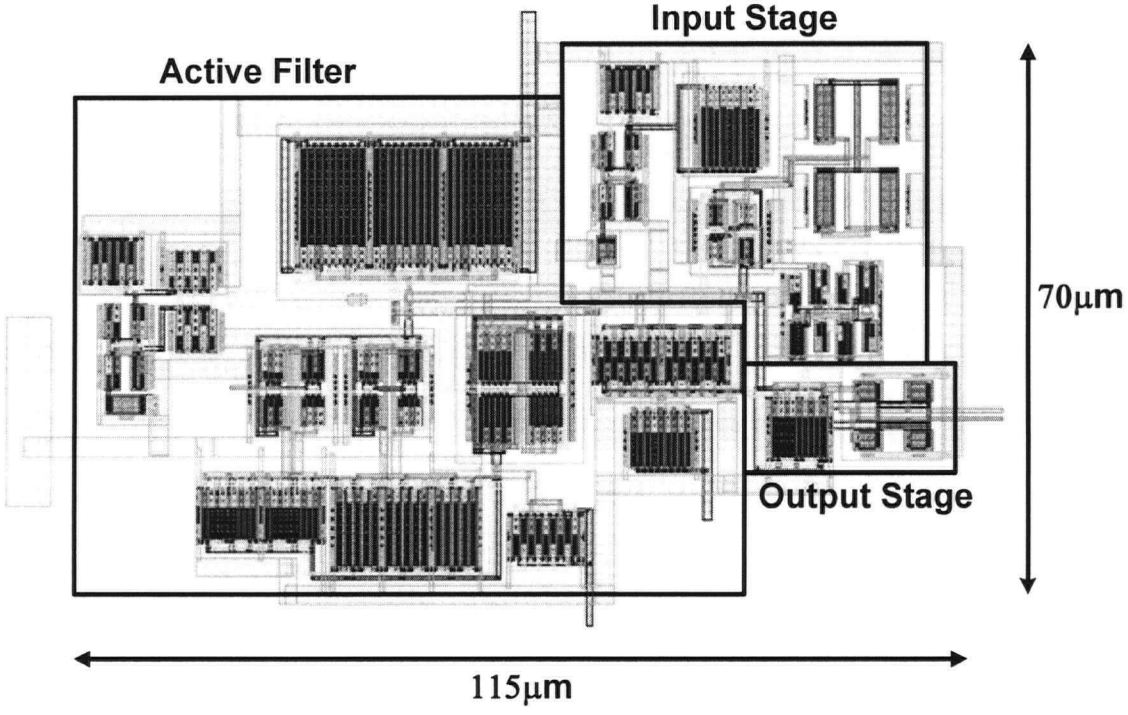

Figure 6.4 – Final Active Filter Layout

6.2 Chip Fabrication

The chip was fabricated in a 0.18um CMOS process provided by Taiwan Semiconductor Manufacturing Company (TSMC) through the Canadian Microelectronics Corporation (CMC). To obtain accurate measurements of the inductance and other parameters, it was decided that probing the chip would be a better idea than getting it packaged.

A low-noise amplifier design was also fabricated on the same chip and since the LNA contained passive inductors the size reduction that can be obtained with active inductors is visible. A picture of the fabricated chip is shown in Figure 6.5. The passive inductors have values of a few nano-Henries, while the active version can generate inductances of 6nH to 123nH.

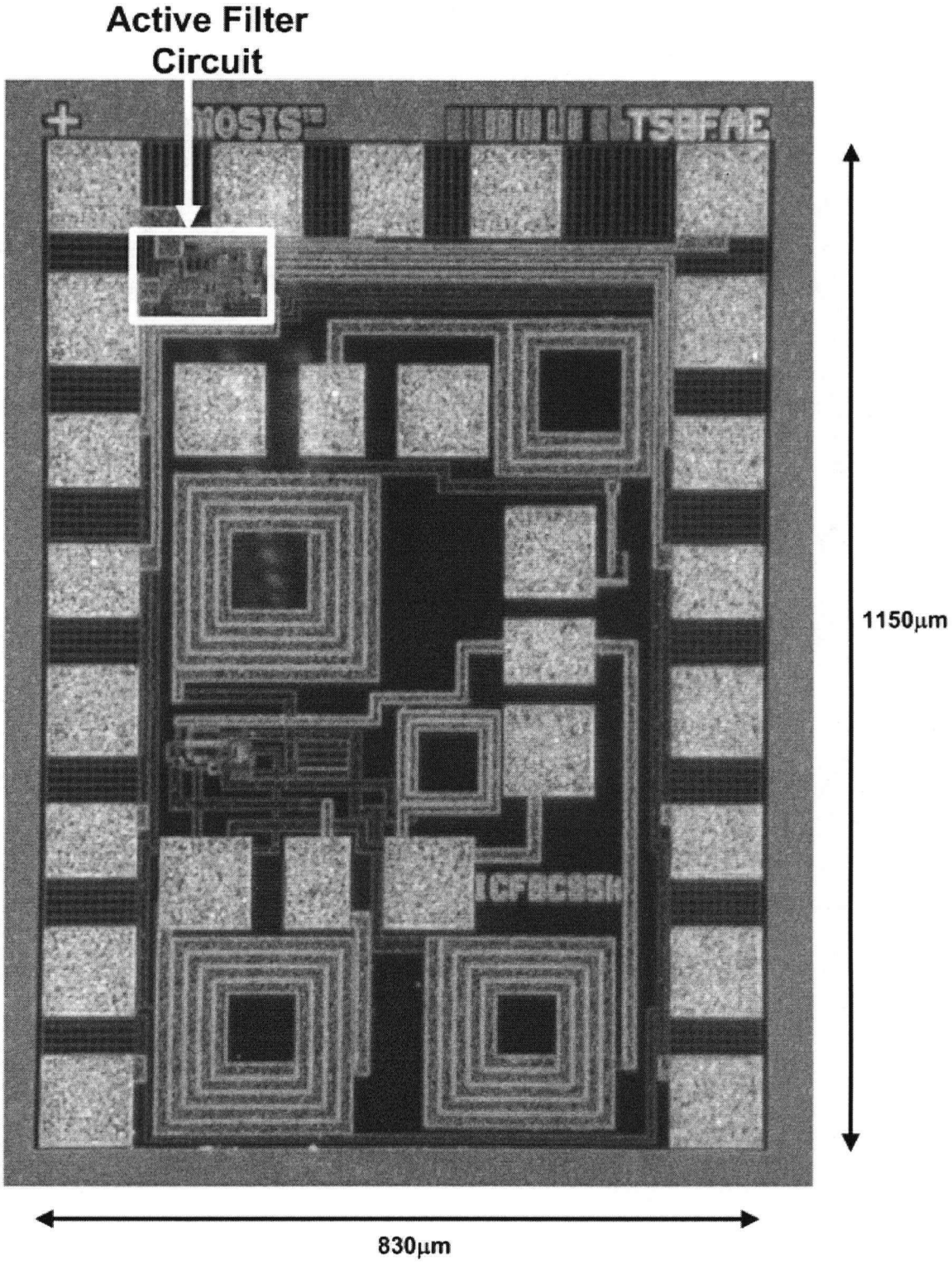

Figure 6.5 – Fabricated Chip

6.3 Test Results

An Agilent E83624B performance network analyzer (PNA) is used to test the response of the filter. To reduce the complexity of the setup, the amplifier is fed using a single-ended signal instead of a differential one, and the output is also single-ended. Most of the DC sources used are the Xantrex LXQ 20-3 DC power supplies, but a two-channel semiconductor analyzer (Keithley 2602 System Source Meter) is used to produce accurate tuning voltages. The data obtained from the PNA is saved and MATLAB is used for plotting and analyzing the results.

Figures 6.6, 6.7, and 6.8 show operation at the limits of the low, mid, and high frequency bands, respectively. As it is difficult to measure the Q of the filter directly from the PNA, the Q of the filter in each measurement is labeled on the corresponding plot.

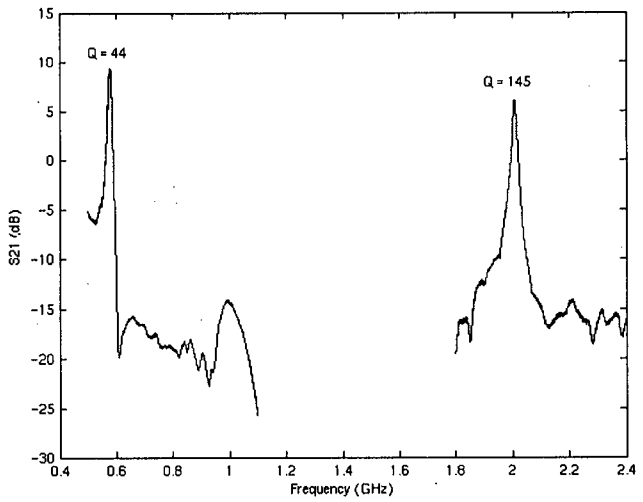

Figure 6.6 - Frequency Operation Limits of the Low-Frequency Band

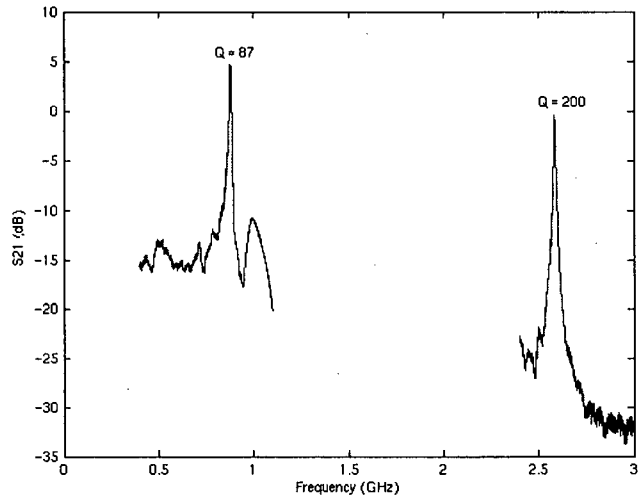

Figure 6.7 - Frequency Operation Limits of the Mid-Frequency Band

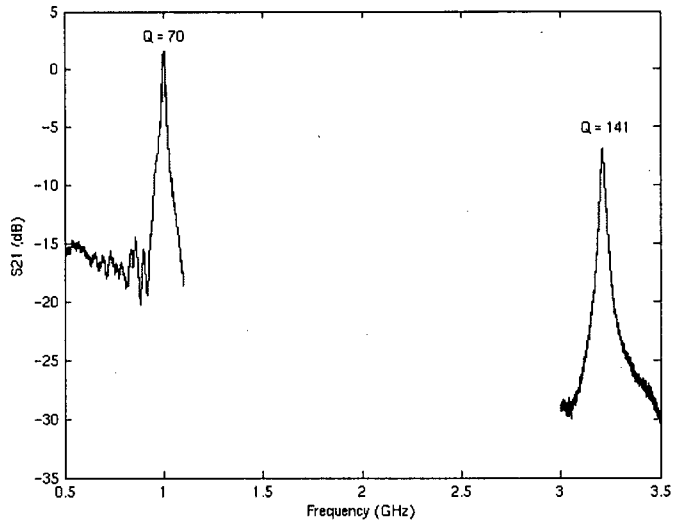

Figure 6.8 - Frequency Operation Limits of the High-Frequency Band

These plots show that the gain is inversely proportional to frequency and directly proportional to Q as expected (and discussed in Chapter 3).

A comparison of the filter tuning ranges obtained from circuit simulation, post-layout simulation (including pads), and chip testing is shown in Table 6.2. The total power consumption is also given, which includes the power dissipation of the DC biasing circuitry and output buffers.

	Cicuit Level Simulation	Post-Layout Simulation	Fabricated Chip Results
Frequency Range of Low Frequency Band	870MHz -> 2.4GHz	925MHz -> 2.51GHz	580MHz -> 2GHz
Power Consumption of Low Frequency Band	12.4mW -> 25.1mW	12.4mW -> 25.1mW	15.1mW -> 26.5mW
Frequency Range of Mid Frequency Band	1.3GHz -> 3GHz	1.34GHz -> 3.1GHz	880MHz -> 2.6GHz
Power Consumption of Mid Frequency Band	13.5mW -> 26.5mW	13.5mW -> 26.5mW	16.2mW -> 26.5mW
Frequency Range of High Frequency Band	1.6GHz -> 3.5GHz	1.66GHz -> 3.64GHz	1GHz -> 3.2GHz
Power Consumption of High Frequency Band	14.1mW -> 26.3mW	14.2mW -> 26.4mW	16.5mW -> 28.4mW

Table 6.2 – Comparison of Circuit for Simulation and Chip Test Results

The frequencies obtained in each band increase from the circuit-level simulation to post-layout simulations due to the capacitance-reducing layout techniques used, but they are lower in the actual chip test results. This can be attributed to both inaccurate parasitic extraction and/or process variations. For example, the results for process variation simulations using the slow NMOS slow PMOS corner are shown in Table 6.3.

	Schematic Simulation at SS Corner	Extracted Simulation at SS Corner	Fabricated Chip Results
Low-Frequency Band	560MHz -> 2.09GHz	630MHz -> 2.18GHz	580MHz -> 2GHz
Mid-Frequency Band	820MHz -> 2.65GHz	920MHz -> 2.76GHz	880MHz -> 2.6GHz
High-Frequency Band	1.04GHz -> 3.3GHz	1.2GHz -> 3.42GHz	1GHz -> 3.2GHz

Table 6.3 – Simulation Results with Process Variations

There is a fairly good agreement between the power consumption in both simulations and measurements, and the slight variations could be due to component tolerances, particularly the resistor values.

A plot showing the tunability of the quality factor of the filter is shown in Figure 6.9.

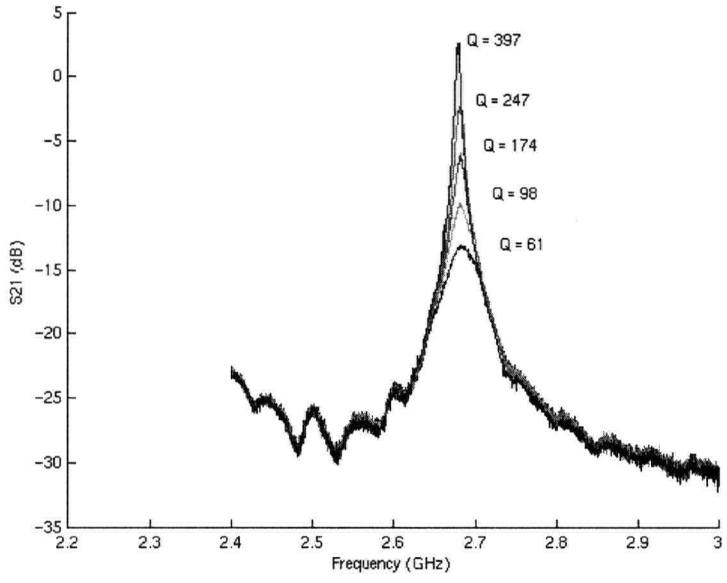

Figure 6.9 – Filter with Different Q Values

Although the Q values in this plot can be as high as 400, it is also possible to obtain higher Q values. One of the limiting factors is the large signal response of the circuit. Increasing Q increases the gain, but once the gain saturates the increase in Q can no longer be accurately measured. This plot also shows that the centre frequency stays fairly constant as Q changes.

The noise of the active filter is found using an Agilent E4440A spectrum analyzer. To measure the noise, the DC biasing voltages are set and the input is grounded. The output power is then integrated with respect to frequency, and the total power is the output referred noise power [17]. The gain of the filter is subtracted to get the input referred noise power.

The spectrum analyzer is also used to measure the linearity of the filter, along with two Agilent 83752A high-frequency signal sources. Two tones are generated at $f_o \pm 1MHz$ and the IIP3 was found. A comparison of the simulation and measurement results for noise, linearity, and spurious free dynamic range is given in Table 6.4. In all cases, the fact that the circuit is being used in a single-ended configuration was accounted for as much as possible.

	Circuit Level Simulation	Fabricated Chip Results
Noise Floor of Low Frequency Band	-63dBm -> -52dBm	-61dBm -> -52dBm
IIP3 of Low Frequency Band	-31dBm -> -22dBm	-32dBm -> -19dBm
SFDR of Low Frequency Band	20dB -> 21.5dB	19dB -> 22dB
Noise Floor of Mid Frequency Band	-59dBm -> -50dBm	-58dBm -> -53dBm
IIP3 of Mid Frequency Band	-30dBm -> -16dBm	-31dBm -> -17dBm
SFDR of Mid Frequency Band	19.5dB -> 22.5dB	18dB -> 24dB
Noise Floor of High Frequency Band	-56dBm -> -48dBm	-55dBm -> -49dBm
IIP3 of High Frequency Band	-28dBm -> -16dBm	-31dBm -> -16dBm
SFDR of High Frequency Band	19dB -> 22dB	16dB -> 22dB

Table 6.4 – Comparison of Simulated and Measured Noise, IIP3, and SFDR Results

Some error is introduced into the measurement results since the Q of the filter could not be fixed at exactly 40. We can see that both the noise and intermodulation measurement results match fairly closely with simulations; however, there is a bit more variability in the SFDR.

Table 6.5 presents a comparison between this work and other recent studies. For the purpose of comparing tuning ranges, the center of the tuning range is defined as f_c,

and the tuning range is defined as Δf. This lets us use the fractional tuning range ($\Delta f/f_c$) for a fair comparison [41].

	This Work	[17]	[19]+	[42]++	[43]++
Technology	CMOS 0.18µm	CMOS 0.35µm	CMOS 0.5µm	CMOS 0.35µm	BiCMOS 0.25µm
Supply Voltage	1.8V	3V	5V	1.3V	2.7V
Area	0.0081mm^2	0.028mm^2	NR	0.1mm^2	1.19mm^2
Predicted Area in CMOS 0.18µm Tehnology	0.0081mm^2	0.007mm^2	NR	0.025mm^2	0.30mm^2
Filter Order	2	2	2	2	4
Center of Tuning Range (f_o)	1.9GHz	725MHz	1.14GHz	2.1GHz	1.86GHz
Tuning Range (Δf)	2.8GHz	650MHz	1.03GHz	270MHz	190MHz
$\Delta f / f_c$	1.47	0.90	0.90	0.13	0.10
Center Frequency (GHz)	2.00	0.90	1.68	2.19	1.88
Quality Factor	50	40	33	40	12.5
SFDR (dB)	21	27	23.2+++	31	49
Power Dissipation (mW)	20.5	51.0	24.3	NR	48.6
Power Dissipation Excluding Biasing and Buffers (mW)	5.1	NR	NR	5.2	NR
Figure of Merit (dB-GHz/mW)	204.88	38.12	105.86	NR	94.77
Figure of Merit Excluding Biasing and Buffers (dB-GHz/mW)	823.53	NR	NR	1044.46	NR

+ Simulation Results
++ Uses Q-Enhanced Passive Inductors Instead of Active Inductors
+++ Calculated Based on Reported Data
NR = Not Reported

Table 6.5 – Comparison with Other Filter Works

The figure of merit (FoM) used to compare the different filters is defined as [42]:

$$\text{FoM} = \frac{N \cdot SFDR \cdot f_o \cdot Q}{P_D} \tag{6.1}$$

where N is the filter order and P_D is the power dissipation. The filter in this work performs better than most in terms of the FoM, but the smaller SFDR is a drawback. This parameter can be improved, but at the expense of increased power dissipation. It can also be seen that this filter has a wider tuning range than the other works, which was one of the design goals. The layout is also smaller than other works, but this is partially due to the technology used. Although analog circuits cannot be scaled as aggressively as

digital circuits, a simple extrapolation using the square of the scaling factor shows that the area consumed by this circuit is comparable, if not smaller, than other works.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis explored the use of active inductors in a widely tunable on-chip radio-frequency filter. The concepts of filters and common circuits used to implement them are first reviewed, along with a discussion of their advantages and disadvantages. Passive inductors are typically found to be the main problem with implementing on-chip filters due to their low quality factor and large area, motivating the use of an active structure. It is shown that circuits made up of transconductors and capacitors can be used to form a gyrator and simulate the performance of an inductor.

A detailed analysis of the active inductor circuit used in this work is performed, and it is shown that it could be modeled by an RLC resonator. Modifications are made to increase the range of operating frequencies and a negative resistance circuit is used to increase the quality factor of the filter. A noise analysis and optimization is performed, which showed the negative resistance circuit to be an asset in reducing the noise contribution of the filter. The causes of nonlinear behaviour in the filter are also explored and some methods of circuit design to improve linearity are studied.

The filter is designed, simulated, and fabricated using a CMOS 0.18μm process, and the final chip results showed that the filter operates from around 500Mhz to 3.3GHz. Not only is the size of the active inductor shown to be a fraction of that of a passive inductor, but the active version is also able to emulate much larger inductance values.

7.2 Future Work

The linearity of the active inductor is a major drawback and warrants further study. This can be done by modeling the active inductor using Volterra series, which may give insights on how to design for improved linearity. More linear transconductors would also help and various topologies should be examined to determine which will add the least capacitance in the signal path so that the high-frequency performance is not sacrificed.

Methods of automatic tuning for both the centre frequency and the quality factor should also be explored. One common arrangement that can be used to tune the centre frequency is a master-slave filter topology [44], which has parallels to a standard phase-locked loop. Quality factor tuning can be achieved by the use of a magnitude-locked loop [44] since the gain of a bandpass filter is directly proportional to the quality factor.

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APPENDIX A
NOISE BANDWIDTH OF A SECOND-ORDER BANDPASS FILTER

The transfer function of a second-order bandpass filter can be described by:

$$H(s) = \frac{as}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{A.1}$$

The total noise at the output of the filter is found by multiplying the input noise spectral density (assuming it is a white noise source) by the magnitude squared of this transfer function integrated over all frequencies. The noise power spectral density will be defined as S_n, which makes the noise of a second-order bandpass filter:

$$\overline{V_{n,out}^2} = S_{n,in} \int_0^\infty |H(f)|^2 df \tag{A.2}$$

The transfer function is written in terms of Hz instead of rad/s to account for the units of noise spectral density, which are V^2/Hz. After taking the magnitude squared of the transfer function and converting the frequency units, the integral becomes:

$$\int_0^\infty |H(f)|^2 df = \left(\frac{a}{2\pi}\right)^2 \int_0^\infty \frac{f^2}{(b^2 - f^2)^2 + cf^2} df \tag{A.3}$$

where

$$\begin{aligned} b &= f_o \\ c &= \frac{f_o^2}{Q^2} \end{aligned} \tag{A.4}$$

The integral works out to be:[1]

$$\int_0^\infty |H(f)|^2 df = \left[\left(\frac{a}{2\pi}\right)^2 * \frac{\sqrt{c-2b^2+\sqrt{c(c-4b^2)}} * \arctan\left\{\frac{\sqrt{2}f}{\sqrt{c-2b^2+\sqrt{c(c-4b^2)}}}\right\} - \sqrt{c-2b^2-\sqrt{c(c-4b^2)}} * \arctan\left\{\frac{\sqrt{2}f}{\sqrt{c-2b^2-\sqrt{c(c-4b^2)}}}\right\}}{\sqrt{2c(c-4b^2)}} \right]_0^\infty \tag{A.5}$$

[1] Using the Integrator from the Mathworld website: http://integrals.wolfram.com/index.jsp

The evaluation of this function for f=0 is simply 0. As f->∞, the arctan terms both approach π/2. We can also substitute for the variables b and c, which gives the equation:

$$\int_0^\infty |H(f)|^2 df = \left(\frac{1}{2\pi C}\right)^2 \frac{\pi}{2} * \frac{\sqrt{\left(\frac{f_o}{Q}\right)^2 - 2f_o^2 + \sqrt{\left(\frac{f_o}{Q}\right)^2\left(\left(\frac{f_o}{Q}\right)^2 - 4f_o^2\right)}} - \sqrt{\left(\frac{f_o}{Q}\right)^2 - 2f_o^2 - \sqrt{\left(\frac{f_o}{Q}\right)^2\left(\left(\frac{f_o}{Q}\right)^2 - 4f_o^2\right)}}}{\sqrt{2\left(\frac{f_o}{Q}\right)^2\left(\left(\frac{f_o}{Q}\right)^2 - 4f_o^2\right)}} \quad \text{(A.6)}$$

In most cases, Q will be greater than 5 which means:

$$4f_o^2 >> \left(\frac{fo}{Q}\right)^2 \quad \text{(A.7)}$$

and the following equation can be obtained:

$$\left[|H(f)|^2\right]_0^\infty = \left(\frac{1}{2\pi C}\right)^2 \frac{\pi}{2} * \frac{\sqrt{2f_o^2\left(-1+\frac{j}{Q}\right)} - \sqrt{2f_o^2\left(-1-\frac{j}{Q}\right)}}{j2\sqrt{2}\frac{f_o^2}{Q}} \quad \text{(A.8)}$$

The square roots in the numerator were evaluated using the formula:

$$\sqrt{x+jy} = \frac{1}{2}\sqrt{2}\left(\sqrt{\sqrt{x^2+y^2}+x} + j\,\mathrm{sgn}(y)\sqrt{\sqrt{x^2+y^2}-x}\right) \quad \text{(A.9)}$$

Using the same assumption of Q > 5, the following expression is obtained:

$$\left[|H(f)|^2\right]_0^\infty = \left(\frac{1}{2\pi C}\right)^2 \frac{\pi}{2} \frac{j2\sqrt{2}f_o}{j2\sqrt{2}\frac{f_o^2}{Q}} \quad \text{(A.10)}$$

This can be simplified to get the final equation:

$$\int_0^\infty |H(f)|^2 df = \frac{a^2}{8\pi}\frac{Q}{f_o} = \frac{a^2}{8\pi BW} \quad \text{(A.11)}$$

which is the equivalent noise bandwidth seen by a noise source at the input of the filter. Thus, the total noise at the output of a second-order bandpass filter is given by:

$$\overline{V_{n,out}^2} = S_{n,in}\frac{a^2}{8\pi BW} \tag{A.12}$$

where the bandwidth is in units of Hertz. It is also useful to find the equivalent noise bandwidth seen by a noise spectral density at the output of the filter. The input noise spectral density can be replaced with an output noise spectral density divided by the gain squared, i.e.,

$$\overline{V_{n,out}^2} = S_{n,in}\frac{a^2}{8\pi BW} = \frac{S_{n,out}}{A_v^2}\frac{a^2}{8\pi BW} \tag{A.13}$$

The gain of a second-order bandpass filter (at resonance) using the transfer function in Equation A.1 is given by:

$$A_v = a\frac{Q}{\omega_o} = \frac{a}{2\pi BW} \tag{A.14}$$

where the bandwidth is given in Hertz. Substituting this in Equation A.13 gives:

$$\overline{V_{n,out}^2} = S_{n,out}\frac{\pi}{2}BW \tag{A.15}$$

which is the expression used in [17, 20].