DELAY COMPENSATED FADE PREDICTION BASED CDMA CLOSED LOOP POWER CONTROL

by

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Abstract

Power control is essential in Code Division Multiple Access (CDMA) systems in order to reduce the near-far effect, optimize the system capacity, and combat the signal degradation due to fading. One problem with Closed Loop Power Control (CLPC) is the delay introduced by power measurement and round-trip delay in the power control loop. We study the impact of power control loop delays on Frame Error Rate (FER) performance under a range of channel conditions. A new CLPC algorithm with delay compensation and fade prediction is then proposed to mitigate the effects of loop delays on CLPC. Delay compensation can reduce power oscillation amplitude around the desired received power level and fade prediction can forecast an upcoming fade in order to mitigate its effect. The FER performance on the forward link of an Interim Standard – 2000 (IS-2000) CDMA system using the delay compensated fade prediction based CLPC algorithm is studied. Simulations with a detailed IS-2000 physical layer model and various Third Generation Partnership Project 2 (3GPP2) channel models are used to illustrate the performance gains of the proposed CLPC algorithm over the conventional CLPC algorithm. The performance of the proposed CLPC algorithm as a function of mobile speed, delay, and carrier frequency is analyzed. It is found that the proposed CLPC algorithm performs better than the conventional CLPC algorithm by about 1 dB for a range of mobile speeds of interest. The performance improvement obtainable by using the proposed CLPC algorithm can reduce the interference and result in an increase in the system capacity. Finally, the effect of power control bit (PCB) errors on the performance of the proposed CLPC algorithm is studied. Simulation results indicate that the proposed CLPC algorithm is still beneficial when the PCB error rate is 5%.

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List of Abbreviations

2G – Second Generation

3G – Third Generation

3GPP2 – Third Generation Partnership Project 2

AWGN – Additive White Gaussian Noise

BER – Bit Error Rate

BS – Base Station

CDMA – Code Division Multiple Access

CLPC – Closed Loop Power Control

DSCDMA – Direct Sequence Code Division Multiple Access

EIA – Electronic Industries Alliance

ESN – Electronic Serial Number

FER – Frame Error Rate

GPS – Global Positioning System

IS – Interim Standard

MMSE – Minimum Mean Square Error

MRC – Maximum Ratio Combining

MS – Mobile Station

MSE – Mean Square Error

NIST – National Institute of Science and Technology

OCNS – Orthogonal Channel Noise Simulator

PCB – Power Control Bit

PCG – Power Control Group

PCS – Personal Communications Services

PN – Pseudo Noise

QoS – Quality of Service

QPSK – Quadriphase-Shift Keying

RLS – Recursive Least Square

SIR – Signal to Interference Ratio

SPW – Signal Processing Worksystem

TDC – Time Delay Compensation

TIA – Telecommunications Industry Association

List of Symbols

α^* – Complex conjugate of channel gain

β – Time in fraction of a slot at which a power control command is sent

B_r – MS receive frequency band

B_t – MS transmit frequency band

Δ - Power control step size

δ – MS transmit power fraction for traffic data

E_b – Received energy per bit

E_c – Received energy per PN chip

e_i – Difference between SIR threshold and measured SIR at receiver i

η – Background noise power due to spurious interference and thermal noise

f_D^T – Doppler frequency threshold

f_i – Relative received sector power at MS i

γ_i – SIR measured at receiver i

$\hat{\gamma}_i$ – Adjusted SIR measurement at receiver i

I_o – Total power spectral density (signal and interference) at the MS antenna

I_{oc} – Other cell interference power spectral density

I_{or} – Total transmit power spectral density

$\hat{I}_{or}$ – Total transmit power spectral density after channel simulator

k – Number of correlators

M – Number of users in one cell

M_s – Number of users in one sector

N_o – Noise power spectral density

N_t – Noise power spectral density at MS antenna

n_c – Computation and signaling delay in slot units

n_r – Round trip delay in slot units

n_t – Total power control loop delay in slot units

p_i – Received signal power at receiver i

R – Information bit rate

r – Signal after MRC

ρ – BS transmit power fraction for traffic data

S – Received signal power

s_i – Single bit power control command (up or down) sent by receiver i

S_{T_1} – Received signal power from home BS

T – Slot duration

T_{SIR} – SIR threshold

t_d – Power control command detection delay

t_m – Signal quality measurement delay

t_o – Transmitter power output delay

t_p – Signal propagation delay

t_s – Power control signaling delay

v_n – Output of the n-th correlator at sampling time

W – Total bandwidth

w_n – Weight of the n-th correlator

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1.0 Introduction

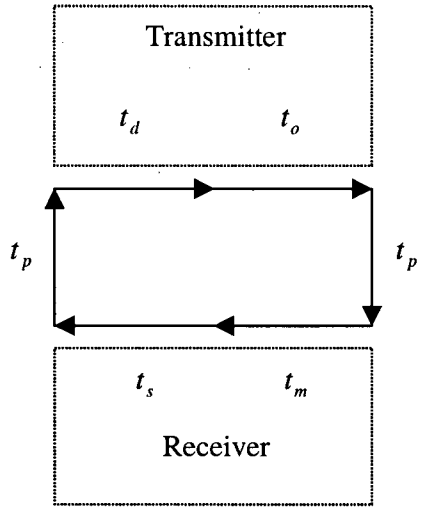
Over the past decade, wireless technology has undergone an enormous evolution. The rapid growth of the cellular telephone industry and the increasing demand for mobile multimedia services have necessitated an efficient cellular system. As a result, Direct Sequence Code Division Multiple Access (DSCDMA) has been proposed to meet the needs of the cellular industry. A popular Third Generation (3G) mobile communication standard based on DSCDMA technology is the Telecommunications Industry Association / Electronic Industries Alliance (TIA/EIA) Interim Standard – 2000 (IS-2000). IS-2000 is the successor of the Second Generation (2G) IS-95 standard and it is an evolutional step to provide next generation capacity, data rates, and services. TIA/EIA released the first version of IS-2000 in 1999, and has published several revisions in subsequent years. The wireless industry is enthusiastic about the commercialization of IS-2000 because it is a technology developed to accommodate the growing demand for higher data rates and increased system capacity.

The incentive for using a DSCDMA communication system is its ability to reject interference from other users simultaneously attempting to transmit over the channel. Since a CDMA system is interference limited, system capacity is maximized when signals are transmitted at the minimum required power to satisfy the signal-to-interference ratio (SIR) requirement. Therefore, power control is a critical issue in CDMA systems, as efficient power control maintains the SIR and reduces a user's interference to other users in the system.

1.1 Motivation

Closed Loop Power Control (CLPC) is commonly used to compensate for power fluctuations due to fast fading in a cellular multiple access environment. It is closed loop in that the process involves both the transmitter and the receiver. Given that CLPC is essential to reduce inter-user interference, much effort has been devoted to improving the CLPC algorithm. A better CLPC algorithm will not only help to maintain the SIR in a fading environment, but it can also increase the system capacity by mitigating the near-far problem. Therefore, it is highly desirable to make the CLPC algorithm as efficient as possible.

Generally, a CLPC algorithm requires input data, i.e. power control command, periodically with a hard timing deadline, and adjusts the output power after a fixed amount of time relative to the received power control command. The power control command and output power can be treated as sampled values at the transmitter and receiver of the CLPC algorithm with a fixed sampling rate. A major problem that can hamper the performance of a CLPC algorithm is time delay. In practice, it takes some time, t_m, to measure the signal quality (assuming signal quality is averaged over a certain period). After the signal quality is measured, there is a delay, t_s, before the power control command is sent to the transmitter. Furthermore, there are propagation delays, t_p, when the power control command is sent to the transmitter, and when the adjusted power arrives at the receiver. The transmitter requires a time, t_d, to detect the power control command. In addition, there is a delay, t_o, before the power control command is acted upon and applied in the transmitter output. Figure 1 shows the sources of delay in the power control loop.



t_m - Measurement Delay

t_s - Signaling Delay

t_p - Propagation Delay

t_d - Detection Delay

t_o - Output Delay

Figure 1 Sources of Delay in Power Control Loop

In general, time is divided into slots by the CLPC algorithm and one power control command is sent at a fixed time in each slot. Let T be the slot duration ($t_m \leq T$) and β be a value between 0 and 1 that represents the time in fraction of a slot at which a power control command is sent. For instance, β=0.5 means the power control command is sent in the middle of the slot. Assuming t_m starts from the beginning of each slot. For the signal quality measured in slot i to be used to generate the power control command sent in slot i, $t_m + t_s$ must be less than βT. Otherwise, the signal quality measured in slot i can only be used to generate a power control command in some future slot. Let n_c be the delay in slot units in generating a power control command based on the most recent signal quality measurement. Then,

$$n_c = \left\lceil \frac{t_m + t_s}{T} - \beta \right\rceil, \qquad n_c = 0,1,2.... \qquad (1.1)$$

The round trip delay in the power control loop is the time interval between the transmission of the power control command and the arrival of the corresponding adjusted power at the receiver, i.e. $t_p + t_d + t_o + t_p$. In most cases, the transmitter

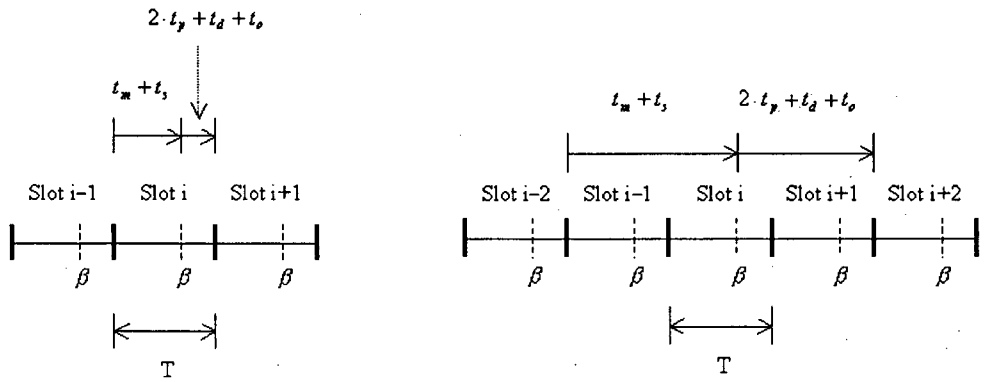
output power is changed at a fixed time in each slot. Assuming the transmitter power is only changed at the beginning of a slot and let n_r be the round trip delay in slot units. Then,

$$n_r = \left\lceil \frac{2 \cdot t_p + t_d + t_o}{T} + \beta \right\rceil, \qquad n_r = 1,2,3.... \qquad (1.2)$$

Hence, the total delay, n_t, in slot units in the power control loop is

$$n_t = n_c + n_r, \qquad n_t = 1,2,3.... \qquad (1.3)$$

Figure 2 shows two examples of power control loop delays in slot units. Let slot i be the current slot and a power control command is just sent to the transmitter in slot i. Figure 2(a) shows the case when $n_t = 1$ ($n_c = 0, n_r = 1$). It can be seen that the signal quality measured in slot i was used to generate the power control command sent in slot i. The power control command will be applied in the transmitter output at the beginning of slot $i+1$. Figure 2(b) shows the case when $n_t = 3$ ($n_c = 1, n_r = 2$). It can be seen that the signal quality measured in slot $i-1$ was used to generate the power control command sent in slot i. The power control command will be applied in the transmitter output at the beginning of slot $i+2$.



(a) $n_t = 1$ ($n_c = 0, n_r = 1$) (b) $n_t = 3$ ($n_c = 1, n_r = 2$)

Figure 2 Examples of Power Control Loop Delays

Since the channel condition is changing over time, a delay in the power control loop means that the power control commands may be outdated and do not reflect the latest channel condition. As a result, the performance of CLPC is degraded due to the loop delays.

1.2 Goals

The IS-2000 standard has been widely adopted because of its superior features and CLPC is essential to the smooth operation of an IS-2000 system. Since loop delays can cause CLPC to be ineffective, the overall system performance can be improved if the effects of loop delays are reduced or compensated. The objectives in this thesis are to investigate the impact of power control loop delays on the overall system performance, improve the existing CLPC algorithm, and demonstrate the advantages of the improved CLPC algorithm. Computer simulations will be used to verify the performance gains of the improved CLPC algorithm and expressions will be provided to show how the improvements will result in an increased system capacity.

1.3 Contributions

The main contributions of this thesis are:

1. The effects of power control loop delays on Quality of Service (QoS) in terms of Frame Error Rate (FER) in an IS-2000 system were studied.
2. A new CLPC algorithm based on delay compensation and fade prediction was proposed to mitigate the effects of loop delays. The new algorithm is applicable to IS-2000 compliant systems with no additional hardware requirements as well as to other power controlled CDMA systems.

3. The performance of the proposed CLPC algorithm was examined using simulations to confirm the benefits of using the proposed CLPC algorithm in different fading environments and with different loop delays. A complete IS-2000 forward link physical layer model that includes channel coding / decoding, interleaving / deinterleaving, and spectrum spreading / despreading was used to evaluate the overall FER performance. In this thesis, the focus is on the forward link CLPC since it is not used in IS-95 but has been introduced in IS-2000.

1.4 Thesis Outline

The rest of this thesis is organized as follows. In Chapter 2, some of the fundamental concepts in CDMA systems are reviewed. This chapter also summarizes the standard CLPC algorithm used in IS-2000. Chapter 3 examines the state of the art in power control and previous works. In this chapter, the effects of power control loop delays are studied. In Chapter 4, the IS-2000 forward link system simulation model is presented, along with the test conditions specified in Third Generation Partnership Project 2 (3GPP2) C.S0011-A, Recommended Minimum Performance Standards for cdma2000 Spread Spectrum Mobile Stations. In Chapter 5, the use of delay compensation and fade prediction in IS-2000 CLPC algorithm is discussed and a new CLPC algorithm is proposed. Furthermore, the relationship between SIR and IS-2000 forward / reverse link system capacities are depicted. In Chapter 6, FER simulation results of the proposed CLPC algorithm are provided and compared against those of the conventional CLPC algorithm. Conclusions and future research suggestions are given in Chapter 7.

2.0 Background

Spread spectrum has been used for a long time in military communications to combat intentional jamming and reduce the probability of intercept. More recently, spread spectrum has been employed in civilian applications, and has profoundly influenced the digital cellular industry. IS-2000 utilizes DSCDMA, which differs from the traditional system design objective of minimizing the utilization of channel bandwidth, to achieve a higher system capacity. In DSCDMA, a wideband code sequence that is independent of the data sequence is used to accomplish spectrum spreading. The information-bearing signal is multiplied by the wideband code to make the signal appear wideband and noise-like. Different users can occupy the same band at the same time and they are separated from each other via a set of codes. The transmitted signal, along with background noise, external interference (interference from unknown sources), and internal interference (interference from co-channel users), arrive at the receiver at the same time. The receiver sifts the desired signal out of the composite signal by correlating the composite signal with the original code. All the unwanted signals that do not match the original code will result in a low correlation when they are despread and are rejected by the receiver. Figure 3 shows the spreading and despreading of the data signal in an IS-95 / IS-2000 system.

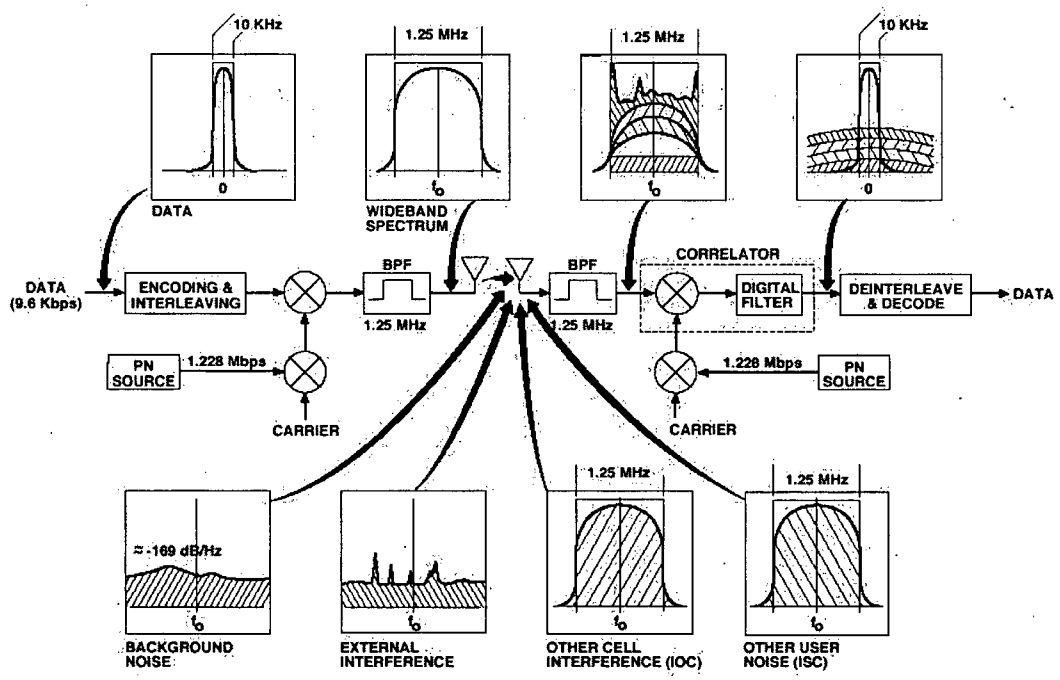


Figure 3 Spectral Spreading and Despreading in IS-95 / IS-2000

(adapted from [1])

In addition to noise and interference, the transmitted signal may be subject to other propagation impairments. Multipath fading is often a major impediment to reliable communication. Another issue is the near-far problem caused by propagation loss and the geographical locations of the users. In IS-2000, power control is employed to mitigate multipath distortion and the near-far problem. A description of the CLPC procedure in IS-2000 is given at the end of this chapter.

2.1 Multipath Rayleigh Fading

A signal can be reflected from various physical structures, such as buildings and walls, on its way to the receiver. Due to the reflections, the signal arrives at the receiver via a number of different paths. The different reflected signals arrive at slightly different times, with different amplitudes, and with different phases. These

reflected signals may add constructively or destructively to the original signal, resulting in multipath fading [2]. The envelope of a received signal for a moving mobile is often modeled by a Rayleigh distribution [3]. The performance of a communication system can be severely degraded by Rayleigh fading. Possible solutions to combat multipath Rayleigh fading are to increase transmit power or to use diversity techniques [4].

In IS-2000, with a pilot signal that provides timing reference, the signal arriving from different paths may be independently received to reduce the severity of the multipath fading. This multipath diversity is a form of time diversity in which the signals from different paths are combined to reduce the effect of fading and improve SIR. As long as the time separations between the signals are greater than one chip time, the signals can be resolved and can be combined to provide better signal quality [5]. In IS-2000, the chip rate is 1.2288 Mcps. Therefore, two signals can be separately combined using the technique discussed in the next section if they are at least 814 ns apart.

2.2 Maximal Ratio Combining

A common technique that is used in CDMA systems to combat multipath fading is maximal ratio combining (MRC). With the aid of a pilot signal in IS-2000, the outputs from the correlators that have been synchronized to the signals from the multipaths are combined in an optimum manner. Let v_n be the output of the n-th correlator at the sampling time. In MRC, the outputs are combined with some weights, w_n, to give

$$r = \sum_{n=1}^{k} w_n v_n , \tag{2.1}$$

where r is the signal after MRC and k is the number of correlators. The weights are selected to emphasize the contributions of stronger signal components. The optimum combining law is [6]:

$$r = \sum_{n=1}^{k} \alpha_n^* v_n \,, \tag{2.2}$$

where α_n^* is the complex conjugate of the gain of path n. The advantage of this combining technique is that it avoids the loss of information about the received signal from the multipaths. By combining the signal energy from different paths, the multipath distortion is mitigated. This diversity combining receiver is also called a rake receiver.

Note that the rake receiver improves signal quality by coherently combining the multipath signals. The earliest arrived signal is delayed until the end of the rake receiver combining window, which is the arrival time of the latest multipath signal used for MRC. The added delay can contribute to the delay in the CLPC algorithm.

2.3 Near-Far Problem

The near-far effect, which is caused by propagation loss, distance between the base station (BS) and the mobile station (MS), and transmitter power, is a critical issue in CDMA systems. For example, MS's are geographically dispersed but transmit in the same frequency band, B_t, and receive in the same frequency band, B_r. In the forward link (BS to MS direction), an MS close to a BS usually requires a lower received signal power than an MS which is far from the BS in order to achieve the same SIR. This is because inter cell interference is more severe at cell boundaries. In the reverse link (MS to BS direction), an MS transmitting near a BS can significantly degrade the performance of an MS which is far away from the BS if all

MS's transmit at the same power. This is because the BS receives a higher power signal from the closer MS, and this higher power signal can severely interfere with the distant MS. Without solving the near-far problem, CDMA would be ineffective in a wireless multiple access environment. In IS-2000, forward link and reverse link power control are employed to ensure that the desired signals received at the MS and BS all have the same strength.

2.4 Power Control

IS-2000 employs forward link and reverse link power control in order to solve the near-far problem, achieve high capacity and meet SIR requirement. The objective of BS / MS power control is to produce a nominal signal power at the receiver regardless of the channel condition and MS's locations.

From the system operator's point of view, it is highly desirable to maximize the capacity of the CDMA system, i.e. the number of simultaneous traffic channels that can be handled in a given bandwidth, while maintaining the QoS. If a transmitted signal arrives at the receiver with a received power that is too low, the FER will be too high to maintain high quality communications. On the other hand, if the received power is too high, the FER will satisfy requirements, but the interference introduced to other system users is increased. Power control provides a way to reduce average power by transmitting at high power levels only during fades and when interference is severe. The system capacity is maximized when the transmitted power is controlled so that signals arrive at the receiver with the minimum required SIR. For data services traffic, power control can lower the FER and reduce the number of packet retransmissions. Also, by reducing the reverse link average power, MS power consumption is reduced, thereby resulting in a longer handset operating time.

There are three types of power control that are employed in IS-2000: open loop power control, closed loop power control and outer loop power control [7]. The purpose of each power control type is described below.

2.4.1 Open Loop Power Control

On the reverse link in an IS-2000 system, open loop power control is employed. Open loop power control refers to the process of adjusting the MS transmit power according to changes in the MS received power. The stronger the power received by the MS, the lower is the MS transmit power. Thus, the MS transmit power is made inversely proportional to the power received by the MS. After a traffic channel is set up, and as the MS moves around, the path loss and shadowing effect between the MS and the BS will change. As a result, the received power at the receiver will change, and the open loop power control will continue to monitor the received power and adjust the transmit power accordingly. The response time of the open loop power control is made slow intentionally to ignore small-scale fading [8]. In other words, open loop power control is used to compensate for slowly varying and shadowing effects where there is a correlation between the forward link and reverse link fades. However, since the forward and reverse links operate at different frequencies, the open loop power control is inadequate and too slow to compensate for fast fading.

2.4.2 Closed Loop Power Control

The goal of closed loop power control is for the BS to instruct the MS, or the MS to instruct the BS, to change the transmit power in a rapid manner in order to combat fast fading. In IS-2000, the transmit and receive frequencies are separated, and the frequency separation generally exceeds the coherence bandwidth of the

channel [9]. Therefore, the fast fading processes on the forward and reverse channels are not highly correlated, and it is more appropriate to power control the forward link and reverse link separately. A one-bit power control signaling scheme is used for powering up or down the transmitter by a fixed amount, and the signaling bit is called the power control bit (PCB). The PCB is generated once every power control group (PCG), which is 1.25 ms in duration, by comparing the received SIR to an adjustable threshold. While the method for measuring SIR is not specified in IS-2000, it is usually obtained by averaging the traffic channel signal quality over a short duration in order to get an accurate SIR measurement. If the received SIR is larger than or equal to the threshold, a power down command is generated. Otherwise, a power up command is generated. The PCB is transmitted through the forward or reverse power control subchannel with specific timing requirements. The closed loop power control provides correction to the open loop power control.

It is important that the latency in generating a PCB based on the received SIR and the signaling process be kept small so that the channel condition will not change significantly before the PCB is received and acted upon. However, delay is introduced when averaging the SIR over time, and this delay can degrade the power control performance. Hence, there is a tradeoff between obtaining a more accurate SIR measurement and shortening the power control delay. Furthermore, sending the PCB over the power control subchannel adds an additional delay to the process.

2.4.3 Outer Loop Power Control

Outer loop power control is the process of adjusting the threshold value used in closed loop power control. Since the power control objective is to maintain an acceptable FER, and since in a cellular environment, there is no simple relationship between FER and SIR, the SIR threshold has to be dynamically adjusted to maintain

the desired FER. Increasing the threshold reduces FER, thereby, improving the QoS. Reducing the threshold tends to increase FER. The threshold is selected to ensure that enough power is received to satisfy the required FER for the call and it can be dynamically changed every frame. Closed loop power control and outer loop power control work together to ensure that the desired SIR is maintained and the required FER is met. Figure 4 shows the closed loop power control and outer loop power control flow chart. The received energy per bit to the effective noise power spectral density (E_b/N_t) is used as the figure of merit for the received SIR and SIR threshold.

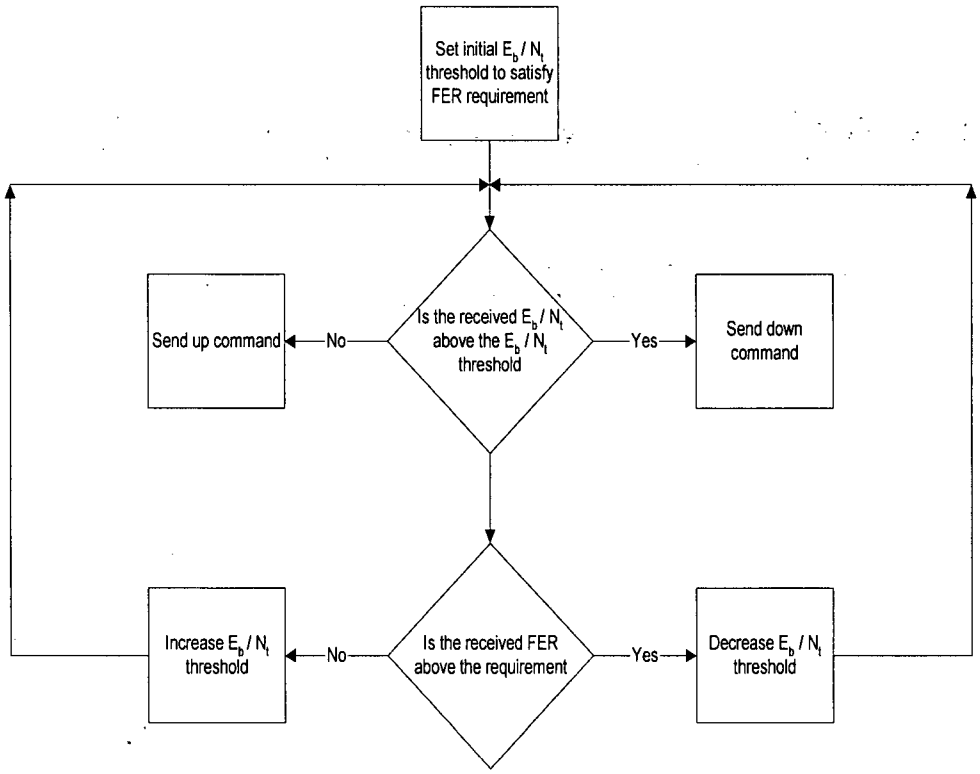


Figure 4 Closed Loop Power Control and Outer Loop Power Control Flow Chart

2.5 IS-2000 Closed Loop Power Control Procedure

This section describes the forward link CLPC procedure in IS-2000 [10]. Forward link CLPC is newly introduced in IS-2000 and does not exist in IS-95.

An IS-2000 BS can transmit up to three data channels (one fundamental channel and up to two supplemental channels) for a single user, together with a common pilot and some signaling channels for all users in a cell. The main purpose of the forward link CLPC algorithm is to maintain the forward link FER of the target channel at the desired level by adapting the BS transmit power. Recall that the outer power control loop estimates the SIR threshold value based on E_b/N_t required to achieve the target FER on the forward traffic channel. The MS estimates the E_b/N_t using the received forward traffic channel and compares the estimated E_b/N_t with the corresponding outer power control loop threshold to determine the value of the PCB to be sent to the BS on the reverse power control subchannel. The estimation is performed in 1.25 ms PCG interval and a PCB is generated every PCG resulting in a PCB rate of 800 bps. A '0' PCB corresponds to an up command, meaning an increase in transmit power and a '1' PCB corresponds to a down command, meaning a decrease in transmit power. The PCB is transmitted to the BS through the reverse power control subchannel in the reverse link. The PCBs are inserted in the reverse pilot channel by a multiplexer (MUX). Each 1.25 ms PCG on the reverse pilot channel contains 1536 chips for 1.2288 MHz chip rate. The MS transmits the reverse pilot signal in the first 1152 PN chips, and transmits the reverse power control subchannel in the following 384 PN chips in each PCG on the reverse pilot channel. Each of the 384 PN chips on the reverse power control subchannel is a repetition of the PCB generated by the MS. Figure 5 illustrates the reverse power control subchannel structure.

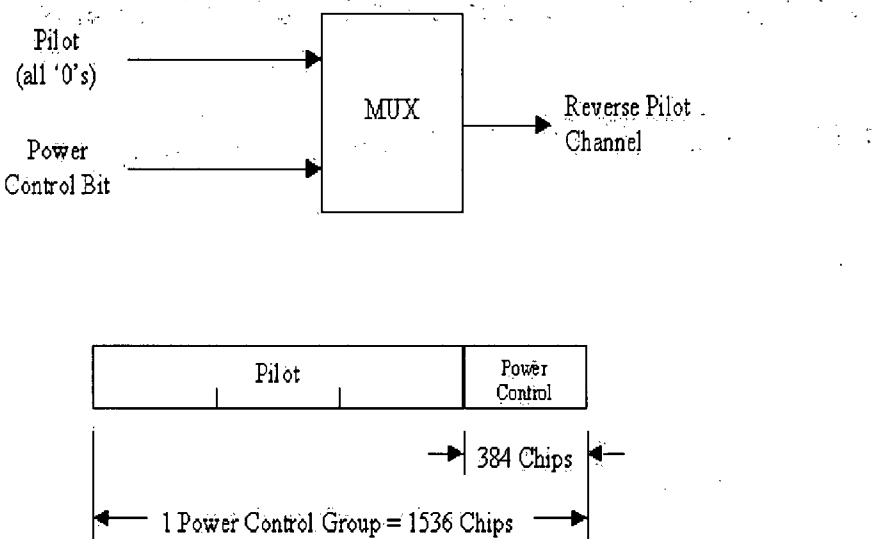


Figure 5 Reverse Pilot Channel Showing the Power Control Subchannel Structure

(adapted from [10])

In one 20 ms frame, there are 16 PCGs, and thus 16 PCBs. The PCGs within a 20 ms frame are numbered from 0 to 15. Figure 6 shows the reverse power control subchannel and the PCGs in a 20 ms frame.

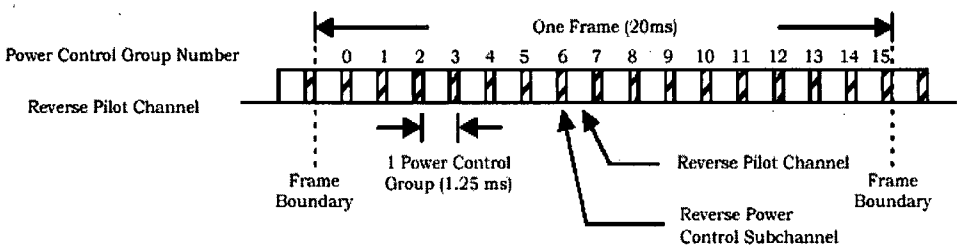


Figure 6 Reverse Power Control Subchannel

(adapted from [10])

The BS adjusts its mean output power level in response to each PCB received in order to reduce the effects of the fading fluctuation and interference in the forward link channel. The nominal change in mean output power per PCB is fixed and can be 1 dB, 0.5 dB or 0.25 dB depending on the BS's setting. The total change in the closed loop mean output power is the accumulation of the valid level changes.

The forward fundamental channel and forward supplemental channel have to share the reverse power control subchannel. Thus, the reverse power control subchannel is further divided into primary reverse power control subchannel and secondary reverse power control subchannel. The reverse power control subchannel carries PCB on the primary channel for the fundamental channel and on the secondary channel for the supplemental channel. The fundamental channel and supplemental channel PCBs are multiplexed onto the reverse power control subchannel. This results in reduced effective PCB per second for each traffic channel. The forward link CLPC has different modes (FPC_MODE) to control the PCB rate for the fundamental and supplemental channel. The reverse power control subchannel configurations are shown in Table 1.

Table 1 Reverse Power Control Subchannel Configurations

(adapted from [10])

	Reverse Power Control Subchannel Allocations (Power Control Group Numbers 0 – 15)	
	Primary Reverse Power Control Subchannel	Secondary Reverse Power Control Subchannel
FPC_MODE = '000'	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	Not Supported
FPC_MODE = '001'	0, 2, 4, 6, 8, 10, 12, 14	1, 3, 5, 7, 9, 11, 13, 15
FPC_MODE = '010'	1, 5, 9, 13	0, 2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15

Note that all IS-2000 BS transmissions are referenced to a common CDMA system-wide time scale that uses the Global Positioning System (GPS) time. The system time at various points in the transmission and reception processes is the absolute time referenced at the BS transmit antenna offset by the one-way or two-way delay of the transmission. Figure 7 shows the relation of system time at different points in the CDMA system. The BS starts transmission for the $i+1^{th}$ PCG before it has finished receiving the PCB on the reverse power control subchannel from the i^{th} PCG.

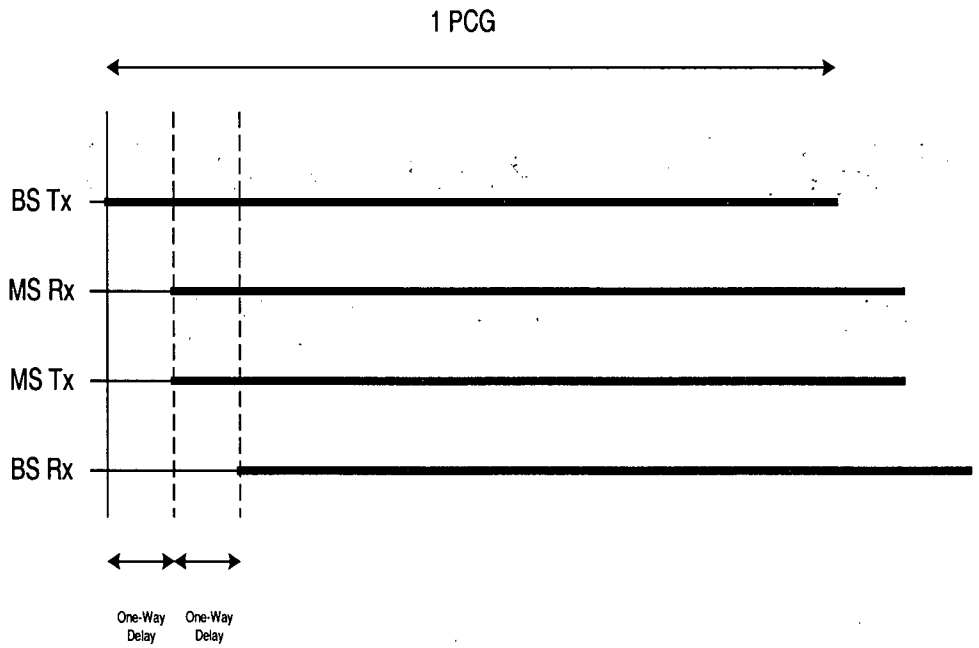


Figure 7 CDMA System Timing

The idea of reverse link CLPC is similar to the forward link CLPC. The reverse link CLPC controls the MS to transmit enough power to achieve the target FER for the target channel. The PCB is transmitted on the forward power control subchannel, which is inserted on the forward traffic channel by puncturing the symbols according to the MS's Electronic Serial Number (ESN) and the long Pseudo-

Noise (PN) code sequence [10]. In other words, the PCB is pseudo randomly punctured in the forward traffic channel and the PCB starting position is determined by the long PN code sequence masked by the MS's ESN.

3.0 Previous Work

CLPC plays an important role in CDMA cellular radio systems in reducing mutual interference and compensating for time varying propagation conditions. A CLPC algorithm in which the transmitter power is increased or decreased based on a comparison of the received SIR and a threshold is proposed in [11]. This algorithm is used in IS-95 and IS-2000. In this thesis, this algorithm is referred to as the conventional CLPC algorithm. Due to the increased interest in managing radio resources efficiently, CLPC has been an area which has attracted much extensive research attention in recent years. Many variations to the conventional CLPC algorithm have been proposed, for instance, using multiple code PCBs, employing centralized power control, and modified PCB signaling [12, 13, 14]. However, most of these CLPC algorithms are not directly applicable to IS-2000 compliant systems. On the other hand, some papers have proposed methods to improve the existing CLPC algorithm. In [15], it is stated that time delays hamper the power control performance in two different ways:

1. Internal dynamics of the power control loop.
2. Delayed reactions to changes in external disturbances.

Schemes to compensate for delays and predict channel fades are possible methods to overcome the performance degradation. This section examines previous studies in these two areas.

3.1 Delay Compensation

The ideal behavior of the CLPC algorithm in IS-2000 is that the received SIR oscillates up and down around the threshold every alternate PCG. However, in real

systems, CLPC is imperfect. One of the main problems in CLPC is time delay due to measuring and reporting. CLPC is based on feedback information which may be outdated. When the power control delay is large, the power control can become ineffective. It is noted in [16] that power control performance is degraded when subject to time delays in the algorithm. Power control delay can lead to an oscillatory behavior in received power and result in larger bounds on the deviations from the desired SIR [17]. In [18], an analysis of power control in WCDMA reveals that a distributed power control algorithm, which works well under ideal circumstances, may result in large power oscillation amplitude when subject to a small delay.

Since the power control command signaling is standardized, the power control delays are known exactly. Time Delay Compensation (TDC) is proposed in [18] to reduce the effects of time delays caused by internal dynamics of the power control loop and hence mitigate the power oscillation amplitudes. Let $\gamma_i[n]$ be the SIR measured at receiver i and T_{SIR} be the SIR threshold used in the CLPC. Then,

$$e_i[n] = T_{SIR} - \gamma_i[n - n_c], \tag{3.1}$$

$$s_i[n] = sign(e_i[n]). \tag{3.2}$$

n_c is from equation (1.1) and

$$sign(x) = \begin{cases} +1 & if \quad x > 0 \\ -1 & if \quad x \le 0 \end{cases}.$$

The signal $s_i[n]$ is sent to the transmitter using a single bit command (up or down) for power control. Assuming the power control command is the only cause for a change in the received signal power and there is no external disturbance such as fading, we can write

$$p_i[n+1] = p_i[n] + \Delta s_i[n - (n_r - 1)]. \tag{3.3}$$

where $p_i[n]$ is the received signal power at receiver i in dB, Δ is the power control step size in dB, and n_r is the round trip delay before the power adjustment has arrived at the receiver. Now, in order to compensate for the delays of the power control loop, an adjustment is made to the measured SIR before it is used to generate a power control decision. In logarithmic scale, let

$$\hat{\gamma}_i[n] = \gamma_i[n - n_c] + \Delta \sum_{j=1}^{n_r - 1} s_i[n - j], \tag{3.4}$$

where $\hat{\gamma}_i[n]$ takes into account the delayed power control commands. The new decision is based on $\hat{\gamma}_i[n]$ and

$$s_i[n] = sign\left(T_{SIR} - \hat{\gamma}_i[n]\right). \tag{3.5}$$

When there is no external disturbance such as fading, the merits of TDC are evident since the delays are cancelled in the loop. By employing TDC, the power control algorithm exhibits lower power oscillation amplitude, which is important from a network perspective (see [18] for the proof and analysis of TDC). With power control loop delays, the amplitude of the oscillations without TDC is larger than the one with TDC as seen in Figure 8.

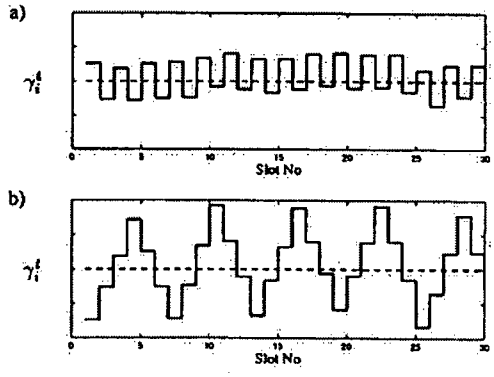


Figure 8 Received SIR when Power Control Commands are Delayed by Two Slots. (a) TDC Employed and (b) No TDC

(adapted from [18])

3.2 Fade Prediction

In a mobile radio environment, the signal quality is significantly affected by fading. Since outdated measurements used in power control result in delayed reactions to changes in external disturbances, accurate prediction of the channel fade may improve the performance of the power control loop. This is because the transmitter power can be adjusted beforehand when an upcoming fade is predicted. Prediction methods using recursive least square (RLS) algorithm and minimum mean square error (MMSE) based polynomial have been proposed [19, 20]. While all the proposed prediction methods show improvements in fade tracking capability, another important factor that determines the applicability of a prediction algorithm is complexity. On the MS side, where processing power is limited, a simpler algorithm is especially important.

The use of the slope of the received SIR to predict the Rayleigh fading envelope in a multi-step SIR-based power control algorithm is discussed in [21]. The main idea is to predict the variation of Rayleigh fading from the received SIR and to track it in time. In [21], the slope of the Rayleigh fading curve is assumed to be constant during the interval between adjacent local highest and local lowest points. Figure 9 shows a block diagram of the multi-step SIR-based fade prediction power control method.

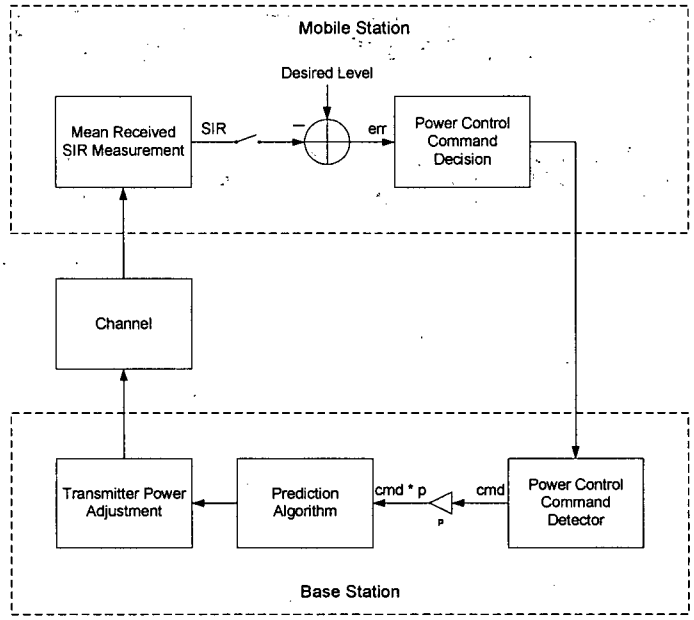


Figure 9 Block Diagram of Multi-step SIR-based Power Control Method with Fade Prediction

(adapted from [21])

In [21], the signal outage probability, which is the probability of the received SIR being less that the SIR threshold is used to access the performance of the prediction method at 900MHz and vehicle speeds from 6 to 60 km/hr. From the simulation results, the fade prediction based power control method performs better than the method without fade prediction.

The algorithm in [21] is a multi-step CLPC algorithm, meaning that a multi-bit power control command is used, and the transmitter changes its output power based on the multi-bit command times the power control step size. With some modifications, the prediction idea should be applicable to the single bit CLPC algorithm used in IS-2000. However, no such studies can be found in previous works. Also, as the Doppler rate decreases in lower frequency band and increases in higher frequency band, studies on linear fade prediction in different frequency bands, for instance, the commonly used 800 MHz and 1900 MHz bands for IS-2000, are desired.

4.0 Simulation Model

Many simulation studies have been carried out on CLPC [12 – 21]. However, most of these simulations are based on simplified models which do not include coding and interleaving. When investigating the performance of IS-2000 CLPC algorithm in different fading environments, we need to take into account the effect of coding and interleaving. It is commonly accepted that CLPC is effective at low speeds and ineffective at high speeds [16]. When errors tend to occur in bursts, interleaving is the main process to mitigate fading. As specified in [22], the QoS metric used is the FER. In this thesis, simulation is done using the physical layer model in the IS-2000 library provided by Signal Processing Worksystem® (SPW™), a software platform commonly used for system design [23]. SPW's IS-2000 library was a joint effort of Cadence and the National Institute of Standards and Technology (NIST) to provide library support for the physical layer of IS-2000. Figure 10 shows the block diagram of the forward link simulation model.

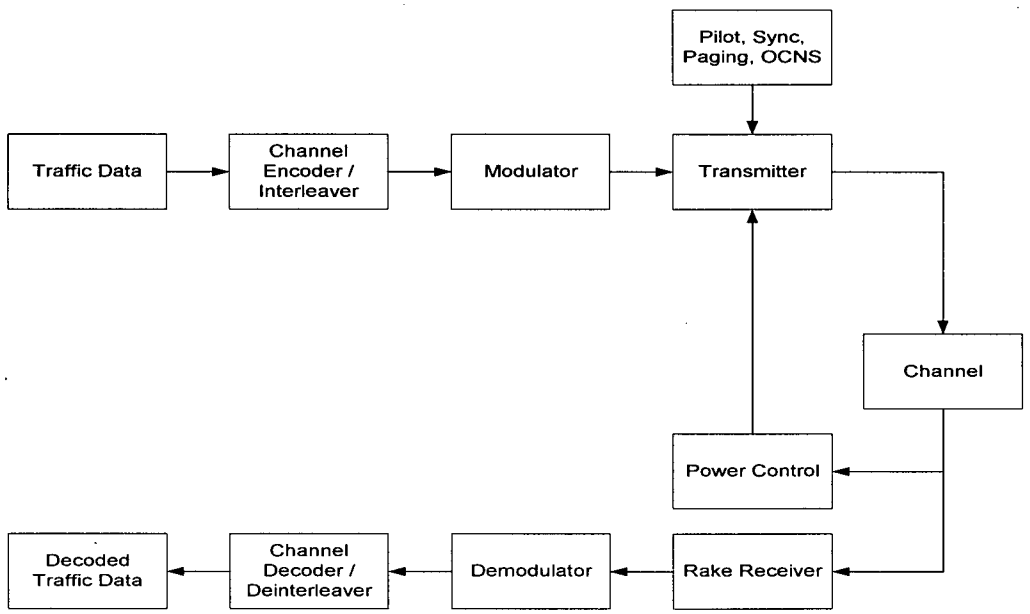


Figure 10 Block Diagram of SPW IS-2000 Forward Link Model

The Traffic Data block generates random bits to simulate the user data on the forward fundamental channel. The Channel Encoder / Interleaver block and the Modulator block implement the IS-2000 forward fundamental channel structure, which includes the convolutional encoder, interleaver, spreader, QPSK modulator, etc. The Transmitter block adds the pilot channel, overhead signaling channels (sync channel and paging channel), and orthogonal channel noise simulator (OCNS) to the user traffic channel. The OCNS simulates the users on the other orthogonal channels of a forward CDMA channel. The Transmitter block also adjusts the transmitter power according to the accumulated power control commands. The Channel block contains a Rayleigh fading simulator and an Additive White Gaussian Noise (AWGN) generator. The flat Rayleigh fading channel is simulated using Jakes' model [3]. The Power Control block executes the CLPC algorithm and is the main focus of this thesis. It measures the received SIR and makes a PCB decision every PCG. The Rake Receiver block has 3 correlator elements and uses MRC to combine the received signals. The Demodulator block and the Channel Decoder / Deinterleaver block are inverses of the IS-2000 forward link process. The received user data is collected and FER is measured in the Decoded Traffic Data block.

System performance is evaluated using the test conditions defined in 3GPP2 C.S0011-A [22]. The C.S0011-A specification details definitions, methods of measurement, and minimum performance characteristics for an IS-2000 MS. Test 3.4.7, Demodulation of Forward Traffic Channel in Multipath Fading Channel with Closed Loop Power Control (FPC_MODE = '000'), in [22] is used to analyze the impact of loop delays on CLPC, and compare the performances of the conventional CLPC algorithm and other CLPC algorithms.

All simulations are performed for the forward fundamental traffic channel, with 20 ms frames and fixed data rate. With the SPW IS-2000 model, random data is transmitted from the BS to the MS. The MS measures the E_b/N_t of the received forward fundamental traffic channel, and compares it with the E_b/N_t threshold. The PCBs are transmitted from the MS to the BS, and the BS adjusts its transmitter power accordingly. The following assumptions are made in the simulation:

1. There is no line of sight path to the MS; therefore, a Rayleigh fading model is assumed.
2. The total transmitted power of the BS is assumed to be constant in each PCG. That is, the BS will not change the transmitter power in the middle of a PCG and the transmitter power is only adjusted at the beginning of a PCG according to the PCB.
3. The mobile speed is assumed to be constant during the simulation.
4. The propagation loss and long-term fading effects are fully compensated for by the open loop power control so that the propagation loss, long-term fading and open loop power control are omitted from the simulation.
5. The data rate is fixed at 9600 bps on the forward fundamental traffic channel with R=1/4 convolutional coding as in Radio Configuration 3 [10].
6. The outer loop power control threshold is fixed during the simulation.
7. The MS starts measuring the SIR from the beginning of each PCG for 0.625 ms (half of a PCG), and the SIR mean during the first half of the PCG is used to generate a PCB. Perfect SIR measurement is assumed. Simulations were used to verify that change in FER was negligible for an estimation error to signal power ratio of –20 dB.

8. Background noise is assumed to be negligible and inter cell interference is assumed to be the dominant source of interference. Therefore, the figure of merit for SIR, E_b/N_t, equals to the received energy per bit to the inter cell interference power spectral density.

Figure 11 shows the functional block diagram of the set-up for the simulation model. I_{or} is the total transmit power spectral density of the forward CDMA channel at the BS antenna. After the channel simulator, I_{or} becomes $\hat{I}_{or}$, which is the received power spectral density of the forward CDMA channel as measured at the MS antenna. Then, an AWGN source is used to simulate interference from other cells. The power spectral density of the AWGN source as measured at the MS antenna, I_{oc}, is added to $\hat{I}_{or}$, to give I_o, which is the total received power spectral density, including signal and interference, as measured at the MS antenna.

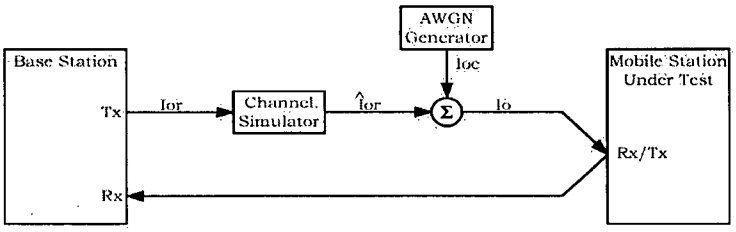


Figure 11 Functional Set-up for Traffic Channel Tests in Fading Channel
(adapted from [22])

The BS simulation parameters for the forward CDMA channel are shown in Table 2. The Pilot E_c/I_{or}, Sync E_c/I_{or}, Paging E_c/I_{or}, and Traffic E_c/I_{or} are the

ratio of the average transmit energy per PN chip for the corresponding channels to the total transmit power spectral density. The paging channel data rate is the rate of the signaling data that is sent on the forward CDMA channel. As the Traffic E_c/I_{or} changes according to the received PCB and it is not possible to allocate unlimited power for the traffic channel when the accumulated power control commands results in continuous power increase, an upper limit is set for the Traffic E_c/I_{or}. The Traffic E_c/I_{or} will be clipped at the limit when the maximum Traffic E_c/I_{or} is reached and the MS asks for more power by sending an up command. FPC_MODE is the reverse power control subchannel configuration for sending PCB. The power control step size is the amount of power change in response to a PCB.

Table 2 BS Simulation Parameters

Parameter	Value
Pilot E_c/I_{or} [dB]	-7
Sync E_c/I_{or} [dB]	-16
Paging E_c/I_{or} [dB]	-12
Paging Channel Data Rate [bps]	4800
Maximum Traffic E_c/I_{or} [dB]	-3
FPC_MODE	'000' (800 bps Primary)
Power Control Step Size [dB]	0.5

The equation below describes the relationship of the different channels and the transmit power of the BS [22].

$$\frac{Pilot \quad E_c}{I_{or}} + \frac{Sync \quad E_c}{I_{or}} + \frac{Paging \quad E_c}{I_{or}} + \frac{Traffic \quad E_c}{I_{or}} + \frac{OCNS \quad E_c}{I_{or}} = 1 \qquad (4.1)$$

In our simulations, two different multipath configurations are used to represent rural and urban fading environments. Table 3 specifies the channel simulator configurations. All paths are independently faded.

Table 3 Channel Simulator Configurations

Parameter	1 path fading	3 path fading
Number of Paths	1	3
Path 2 Power (Relative to Path 1) [dB]	N/A	0
Path 3 Power (Relative to Path 1) [dB]	N/A	-3
Delay from Path 1 to Input [us]	0	0
Delay from Path 2 to Input [us]	N/A	2
Delay from Path 3 to Input [us]	N/A	14.5

According to the two multipath configurations, the ratio of the combined received traffic channel energy per bit to the effective noise power spectral density at the MS antenna, Traffic E_b/N_t, can be described by the following two equations where Traffic_Chip_Bit is the number of PN chips per traffic channel bit [22]:

One-Path Case:

$$Traffic \quad \frac{E_b}{N_t} = \frac{\frac{Traffic \quad E_c}{I_{or}} \times Traffic \_ Chip \_ Bit}{\frac{I_{oc}}{\hat{I}_{or}}} \tag{4.2}$$

Three-Path Case:

$$Traffic \quad \frac{E_b}{N_t} = \frac{Traffic \quad E_c}{I_{or}} \times Traffic\_Chip\_Bit \times \left(2 \times \frac{\frac{2}{5}}{\frac{I_{oc}}{\hat{I}_{or}} + \frac{3}{5}} + \frac{\frac{1}{5}}{\frac{I_{oc}}{\hat{I}_{or}} + \frac{4}{5}} \right). \tag{4.3}$$

As the Doppler frequency is a function of carrier frequency and mobile speed, a range of carrier frequencies and mobile speeds are selected for simulations. Two common IS-2000 frequency bands are the 800 MHz cellular band and the 1.9 GHz Personal Communications Services (PCS) band. Since the forward link traffic is simulated, two BS transmitting frequencies, 870 MHz and 1.93 GHz, from the cellular band and PCS band are chosen for simulations. The channel simulation configuration specifies the channel simulator configuration from Table 3 and the mobile speed to be used. Table 4 shows the simulation parameters for the channel model. These parameters are suggested in [22].

Table 4 Channel Parameters and Target FER

Channel Simulation Configuration	$\hat{I}_{or}/I_{oc}$ [dB]	I_{oc} [dBm / 1.23 MHz]	Target FER
1 path 3 km/hr	6	-61	10 %
1 path 30 km/hr	4	-59	1 %
3 path 100 km/hr	2	-57	1 %

In addition to the settings specified in [22], more scenarios are selected for simulations. This is because the channel parameters from [22] are selected to ensure the MS meets minimum standard requirements. To study the CLPC algorithm performance, extended coverage is needed to show the effectiveness of CLPC at different mobile speeds and channel configurations. Table 5 shows the additional simulation parameters used for simulations.

Table 5 Additional Channel Parameters and Target FER

Channel Simulation Configuration	$\hat{I}_{or}/I_{oc}$ [dB]	I_{oc} [dBm / 1.23 MHz]	Target FER
1 path 50 km/hr	4	-59	1 %
1 path 100 km/hr	4	-59	1 %
3 path 30 km/hr	2	-57	1 %

In our simulations, 5000 frames are run when the targeted FER is set to 10% and 10000 frames when the targeted FER is set to 1%. This translates into a minimum of approximately 500 frame errors and 100 frame errors for 10% FER and 1% FER respectively. The simulation duration and number of fade cycles for various channel simulation configurations are shown in Table 6.

Table 6 Simulation Duration and Number of Fade Cycles

CDMA Frequency [MHz]	Vehicle Speed [km/hr]	Doppler Frequency [Hz]	Number of 20 ms Frames	Number of Fade Cycles in Simulation
870	3	2.4	5000	241.7
	30	24.2	10000	4833.3
	50	40.3	10000	8055.6
	100	80.6	10000	16111.1
1930	3	5.4	5000	536.1
	30	53.6	10000	10722.2
	50	89.4	10000	17870.4
	100	178.7	10000	35740.7

At the end of a simulation, a FER will be obtained, and the Traffic E_b/N_t measured in each PCG is averaged over the simulation duration to obtain a mean

Traffic E_b/N_t . For each test case, two simulations are run to obtain two (mean Traffic E_b/N_t , FER) sets. The two (mean Traffic E_b/N_t , FER) sets are plotted and joined by a straight line. The mean Traffic E_b/N_t needed to achieve the target FER is used for performance evaluation.

5.0 Delay Compensated Fade Prediction Based Closed Loop Power Control Algorithm

In the conventional CLPC algorithm, power control can become ineffective if the loop delay is large or the fade rate is high. As seen in Chapter 3, delay compensation can eliminate the delays introduced by SIR measurement and round trip delay of the power control loop. However, changes in channel conditions which occur during the loop delay are not compensated for. One method for keeping track of channel fading is fade prediction. Since a PCB command is executed every PCG and the PCB could be delayed for several PCGs, fade prediction can be disturbed in the sense that changes in measured SIR are not only caused by fading, but also by PCB command executions. Consequently, PCB commands should be taken into consideration in order to predict the channel fade more accurately. The effect of PCB command execution on fade prediction is specially significant when the Doppler frequency is low because the SIR change as a result of PCB commands may be comparable to the change in fading envelope between SIR samples.

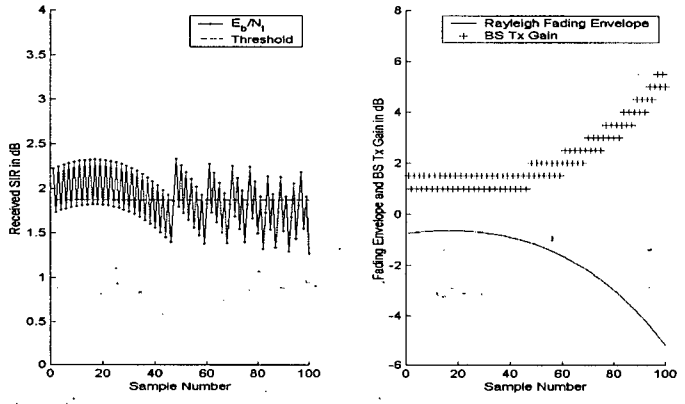
In this chapter, it is first verified that loop delays in the conventional IS-2000 CLPC algorithm produces large power oscillation amplitudes as described in [18]. Then, the linearity of Rayleigh fading is studied to access the applicability of piecewise linear fade prediction for CLPC when the PCG interval is 1.25 ms. A new CLPC algorithm that combines the benefits of both delay compensation and fade prediction is proposed.

5.1 Power Oscillations

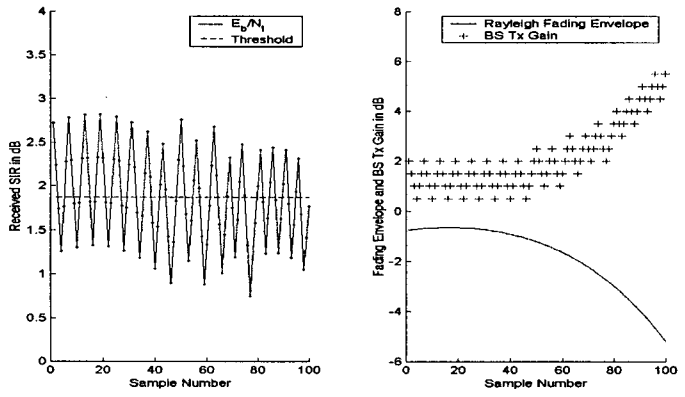
First, we study the effects of loop delays in the conventional IS-2000 forward link CLPC algorithm using the SPW model described in Chapter 4. A PCB is generated every PCG and we assume that the BS transmitter power is constant in each PCG. The sources of delay in PCG slot units are given in equations (1.1), (1.2) and (1.3). Figure 12 shows the effects of three different loop delays on the received E_b/N_t and BS power gain adjustment in a 1 path 3 km/hr Rayleigh fading environment. Figure 12 (a) represents the minimum delay case in our model since the total delay, n_t, cannot be less than 1. Each E_b/N_t sample is compared against the threshold to generate a PCB that is sent to the BS. If the E_b/N_t is above the threshold, a "down" command is generated, and if the E_b/N_t is below the threshold, an "up" command is generated. The BS Tx Gain is the transmitter gain which corresponds to the accumulation of the PCBs and the difference between two consecutive BS Tx Gain samples is the power control step size (i.e. 0.5 dB in our simulations). The difference between two consecutive E_b/N_t samples is the result of changes in the BS Tx Gain, the total noise power, and the channel fading gain. It can be seen that as the loop delay increases, so does the received SIR oscillation amplitude. When the total delay, n_t, is 1 PCG, the oscillation amplitude is about ±0.5 dB around the desired value. The oscillation amplitude is approximately ±1 dB when there is a 2 PCG delay, and approximately ±1.5 dB when there is a 3 PCG delay. Simulation results show that when TDC is employed, the oscillation amplitudes in Figure 12(b) and (c) are reduced, and the received E_b/N_t and BS power gain adjustment with 2 PCG delay or 3 PCG delay are similar to those with 1 PCG delay

as shown in Figure 12(a). The simulation results indicate that TDC stabilizes the power control algorithm by reducing the power oscillation amplitude.

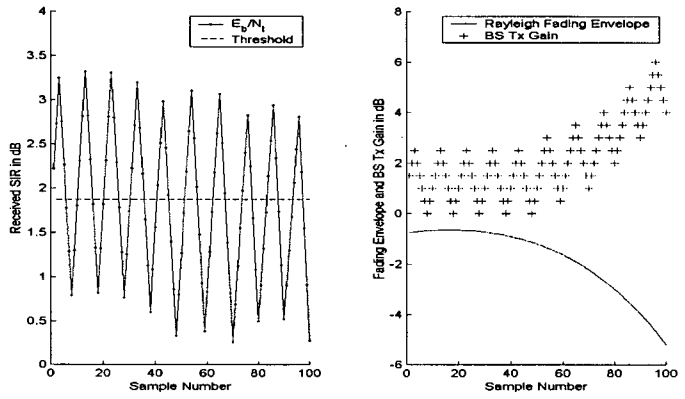
When the Doppler frequency is low, the merit of TDC is clear. However, when the Doppler frequency increases and the change in channel gain between adjacent PCGs becomes larger, the change in SIR can be larger than what the power control step size can compensate for. In this case, large power oscillation amplitudes are often unavoidable. TDC is most effective when the change in channel gain is comparable to the power control step size. Figure 13 shows the effects of three different loop delays on the received E_b/N_t and BS power gain adjustment in a more rapidly changing channel environment, namely the 1 path 30 km/hr Rayleigh fading environment. We can see that the differences between consecutive samples in the first 40 faded E_b/N_t samples have a magnitude comparable to the power control step size, and TDC can reduce the oscillation amplitude. However, TDC cannot reduce the oscillation amplitudes when the change in fading envelope is large, as in samples 40 to 100 in Figure 13.



(a) 1 PCG Delay

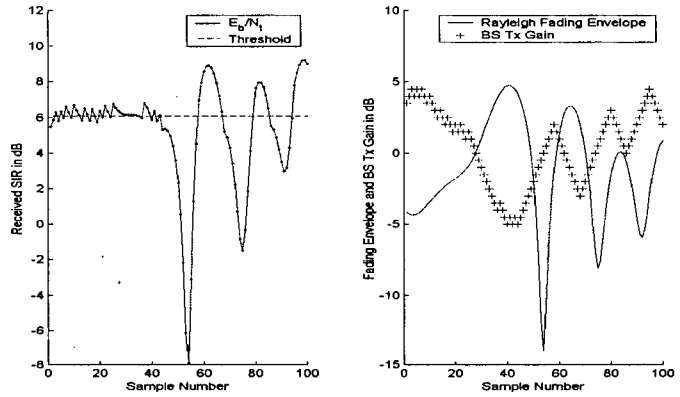


(b) 2 PCG Delay

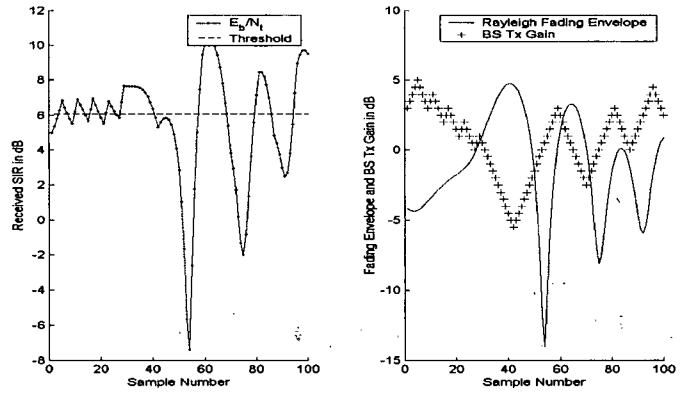


(c) 3 PCG Delay

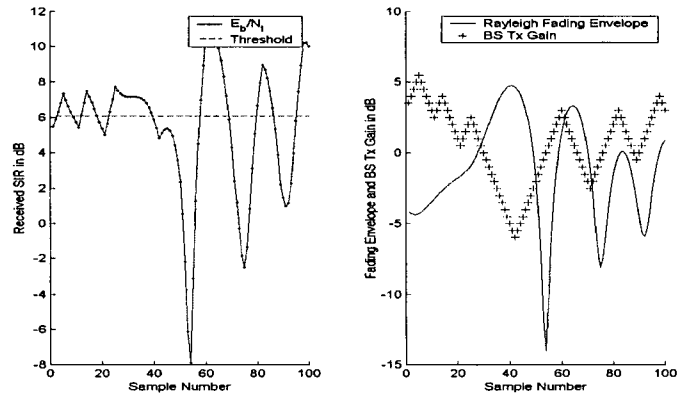
Figure 12 Effects of Power Control Delay on Received E_b/N_t and BS Tx Gain in 1 path 3 km/hr Rayleigh Fading



(a) 1 PCG Delay



(b) 2 PCG Delay



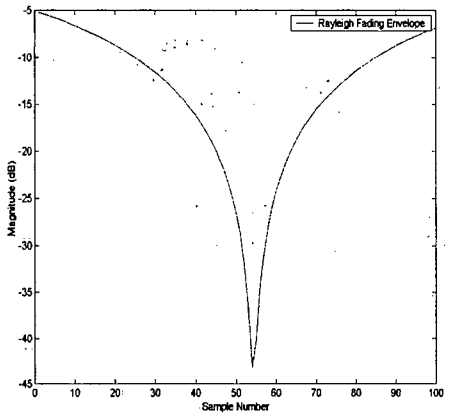
(c) 3 PCG Delay

Figure 13 Effects of Power Control Delay on Received E_b/N_t and BS Tx Gain in 1 path 30 km/hr Rayleigh Fading

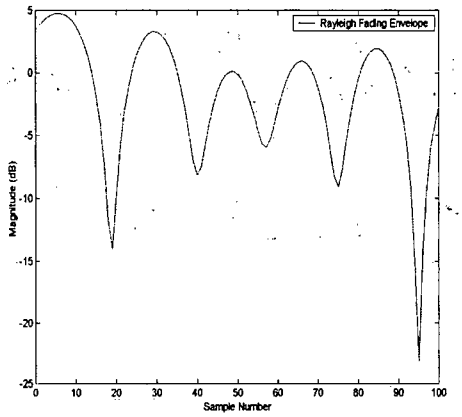
5.2 Fade Linearity

In [21], it is proposed that the slope of the fading curve can be used to predict future fades. In this section, the linearity of Rayleigh fading is studied. Figure 14 shows the Rayleigh fading envelopes for different channel environments at 870 MHz with a sample period of 1.25 ms. Future channel conditions can be predicted using linear extrapolation, i.e. $x[n+a] = (x[n] - x[n-1]) \cdot a + x[n]$. The most recent SIR sample and the preceding SIR sample in linear scale can be used to estimate the slope of the fading curve for predicting channel conditions.

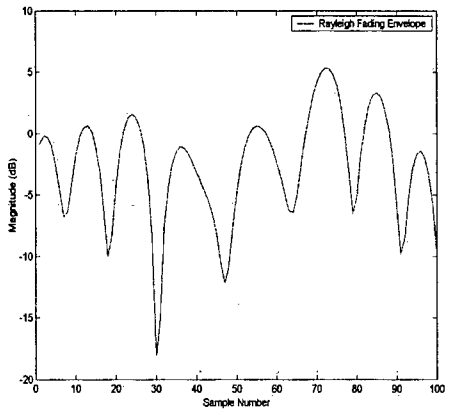
Ideally, the E_b/N_t measured in PCG i is used to generate a PCB that is sent in PCG i to control the power in PCG $i+1$. This happens when $n_t = 1$. Without fade prediction and assuming the PCB is delayed by $n_t > 1$ PCG (i.e. PCB generated using E_b/N_t measured in PCG i is executed in PCG $i+n_t$), the E_b/N_t error is the difference between the E_b/N_t measured in PCG i delay compensated by the $n_t - 1$ previously sent PCBs, and the actual E_b/N_t in PCG $i+n_t-1$. Note that PCG $i+n_t-1$ immediately precedes the PCG in which the currently generated PCB (i.e. in PCG $i+n_c$) is executed. Using linear extrapolation to predict fade can improve the accuracy of the estimated E_b/N_t. However, the predicted value may differ significantly from the actual value when the fading curve passes through local maxima and minima. Therefore, prediction performance will degrade when the number of local maxima and minima increases in a given time period. In a cellular environment with pedestrian and vehicular users, the advantage of using linear fade prediction can be significant when the user mobility is low or moderate.



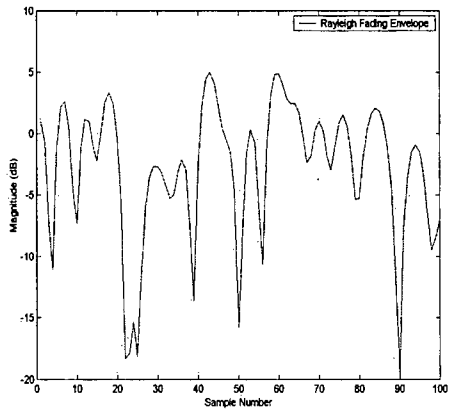
(a) One Path 3 km/hr Rayleigh Fading



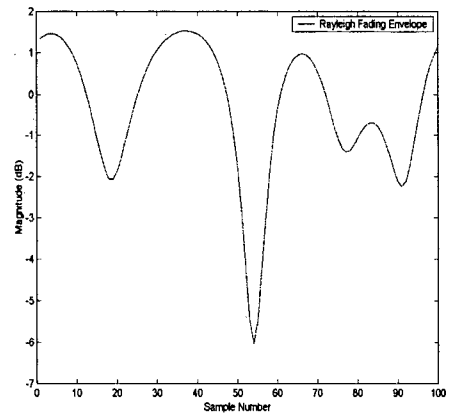
(b) One Path 30 km/hr Rayleigh Fading



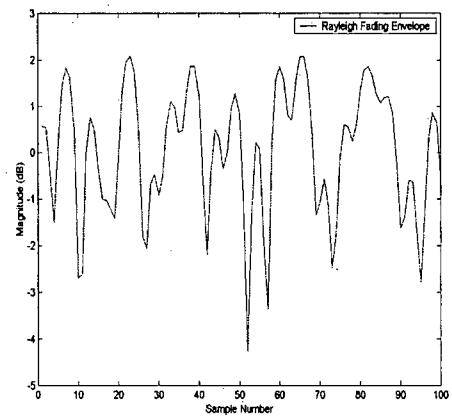
(c) One Path 50 km/hr Rayleigh Fading



(d) One Path 100 km/hr Rayleigh Fading



(e) Three Path 30 km/hr Rayleigh Fading



(f) Three Path 100 km/hr Rayleigh Fading

Figure 14 Rayleigh Fading Envelopes for Different Channel Environments at 870 MHz

Assuming changes in SIR are only caused by fading and ignoring PCB execution for the moment, we study how prediction can improve SIR estimation in the presence of loop delays. Table 7 shows the MSE between the fading envelope values at time n and $n+a$ with and without the use of prediction.

Table 7 MSE Comparisons of Fade Envelopes with No Prediction and with Linear Prediction

No Prediction MSE: average value of $(x[n]-x[n+a])^2$

Linear Prediction MSE: average value of $((x[n]-x[n-1])\cdot a + x[n]-x[n+a])^2$

Channel Simulation Configuration	a	No Prediction MSE	Linear Prediction MSE
1 path 3 km/hr	1	3.32e-4	8.37e-7
	2	1.33e-3	4.13e-6
1 path 30 km/hr	1	3.50e-2	2.74e-3
	2	1.37e-1	2.41e-2
1 path 50 km/hr	1	9.27e-2	1.94e-2
	2	3.51e-1	1.64e-1
1 path 100 km/hr	1	3.46e-1	2.68e-1
	2	1.12	1.90
3 path 30 km/hr	1	3.82e-3	4.07e-4
	2	1.49e-2	3.49e-3
3 path 100 km/hr	1	3.80e-2	3.55e-2
	2	1.16e-1	2.23e-1

With linear prediction, the MSE is reduced at low and moderate speeds (less than or equal to 50km/hr), and is about the same or worse (depending on delay) at high speed. Recall that local maxima or minima degrade fade prediction accuracy. This explains why the MSE with prediction is larger at high mobile speeds. Note that Table 7 only shows how prediction can improve the MSE of the E_b/N_t estimation when there are loop delays. Since there is no simple relationship between the received

E_b/N_t and FER, computer simulations will be used to show the FER performance improvements when fade prediction is used in the CLPC algorithm.

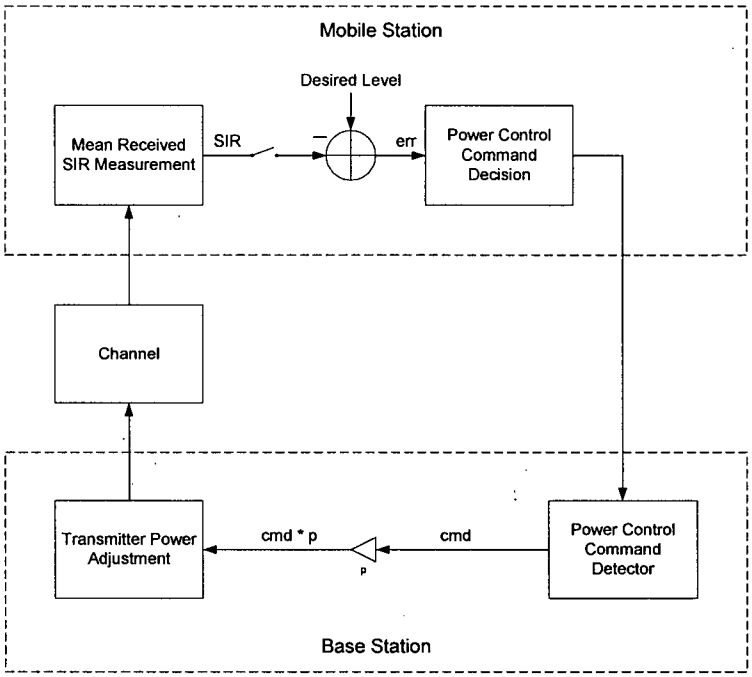
5.3 Proposed Closed Loop Power Control Algorithm

Based on the available information from previous works and simulation results using the SPW IS-2000 model, a new CLPC algorithm using delay compensation and linear fade prediction is proposed. The proposed CLPC algorithm can be easily implemented in software for both the forward link and reverse link traffic channels. No modifications are required in the IS-2000 standard, the mobile terminal hardware, or the base station hardware. The only component in the cellular system that has to be changed is the firmware which generate the PCBs. This new CLPC algorithm is not only applicable to IS-2000, but can also be used in other power controlled CDMA systems employing a command-based, threshold comparing CLPC scheme.

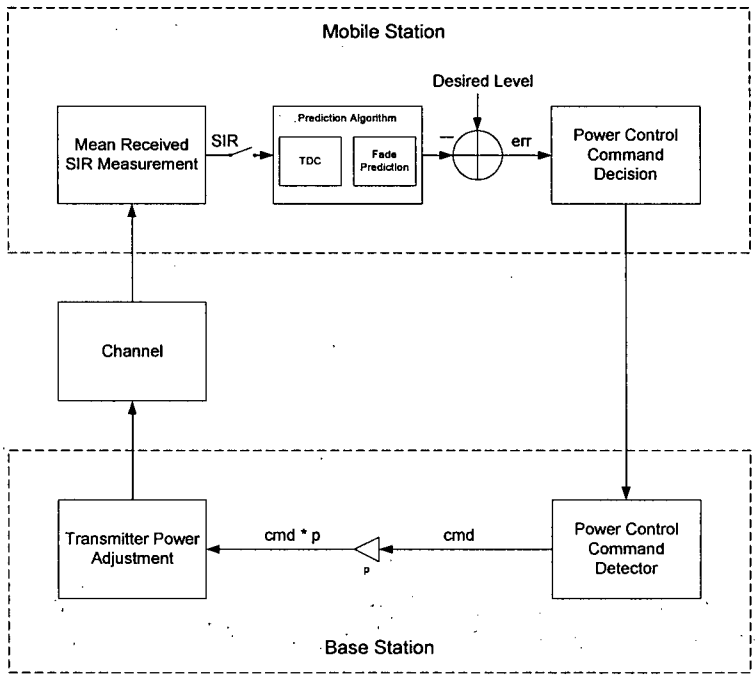
Figure 15 (a) shows the block diagram of the conventional CLPC algorithm. The MS measures the E_b/N_t and compares the measured value against a threshold value to make a decision on the PCB. The algorithm is simple and straightforward.

Figure 15 (b) shows the block diagram of the proposed CLPC algorithm. The MS measures the E_b/N_t in the same way as for the conventional CLPC algorithm. But the measured E_b/N_t is further processed to improve the accuracy of the estimated channel condition. The new prediction block performs delay compensation and linear fade prediction using past PCB decisions and E_b/N_t samples. For $n_t > 1$, the proposed CLPC algorithm expressed in a linear scale is

$$\hat{\gamma}_i[n] = \left\{\left(\gamma_i[n-n_c] - \gamma_i[n-1-n_c]\cdot\Delta^{s_i[n-n_t]}\right)\cdot(n_t-1) + \gamma_i[n-n_c]\right\}\cdot\Delta^{\sum_{j=1}^{n_t-1} s_i[n-j]} \quad (5.1)$$



(a) Conventional CLPC Algorithm



(b) Proposed CLPC Algorithm

Figure 15 Conventional CLPC Algorithm and Proposed CLPC Algorithm

First, the second last measured SIR, $\gamma_i[n-1-n_c]$, is power adjusted using the PCB that was sent as $s_i[n-n_t]$ and executed in PCG $n-n_c$. This power adjusted SIR is subtracted from the latest measured SIR, $\gamma_i[n-n_c]$, to give the slope of the fading envelope. Second, fading envelope is linearly extrapolated for n_t-1 PCG slots. Finally, the extrapolated fade envelope is added to the latest measured SIR, and the delay compensated PCBs, $\Delta^{\sum_{j=1}^{n_t-1} s_i[n-j]}$, are used to adjust the SIR estimation. $\hat{\gamma}_i[n]$, the SIR estimation with delay compensation and fade prediction, is then compared against the threshold to generate a PCB just like the conventional CLPC algorithm.

Comparing Figure 15 (b) with Figure 9 in Chapter 3, we note that the two block diagrams differ in the locations of the prediction algorithms. In IS-2000, the BS does not know the power control threshold of the MS since the MS's outer loop power control algorithm maintains the threshold locally. Due to this reason, in order to use the improved SIR estimation with the threshold, the prediction block must reside in the MS.

5.4 System Capacity

Capacity is defined as the number of simultaneous users which the system can support while the radio link conditions of all users still meet QoS requirements. In IS-2000, the QoS requirement is stated in terms of the FER. In a CDMA system, each user accessing the system is power controlled so that system resources can be shared equitably among users and capacity maximized. Due to the interference limited nature of CDMA networks, any reduction in interference translates directly into an increase in capacity [24]. For completeness, this section summarizes the relationship between CDMA capacity and SIR from [24, 25].

In digital communications, E_b/N_o is often used as the radio link metric [4]. In [22], E_b/N_t refers to the E_b/N_o at the MS antenna. This quantity can be related to the SIR. We will start with a simplified SIR definition in a single cell environment, and then refine the equation according to the forward link and reverse link characteristics of IS-2000 in a multi-cell environment.

We first consider a single cell CDMA system with M users, in which all the user signals are assumed to be perfectly power controlled and each is received with power S. Let η be the background noise due to spurious interference as well as thermal noise. Then, a simplified SIR expression that ignores various performance factors (e.g. voice activity and sectorization gain) at any receiver is

$$SIR = \frac{S}{(M-1)S+\eta} = \frac{1}{(M-1)+\eta/S}. \tag{5.2}$$

This is so because the total interference power in the band is equal to the sum of powers from individual users and the background noise. To get E_b/N_o, whose numerator is obtained by dividing the desired signal power by the information bit rate, R, and the denominator is obtained by dividing the noise (or interference) by the total bandwidth, W, equation (5.2) becomes

$$E_b/N_o = \frac{S/R}{((M-1)S+\eta)/W} = \frac{W/R}{(M-1)+\eta/S}. \tag{5.3}$$

The term W/R is generally referred to as the processing gain. Therefore, the capacity in terms of number of users supported is

$$M = \frac{W/R}{E_b/N_o} - \frac{\eta}{S} + 1. \tag{5.4}$$

Generally, η/S is small. As shown in equation (5.4), the capacity in terms of number of simultaneous users is approximately inversely proportional to E_b/N_o. Next, we show the capacity equations for IS-2000 forward link and reverse link.

5.4.1 Multi-cell IS-2000 Forward Link Capacity

Sectorization is used in IS-2000 to improve capacity. Typically, three antennas per cell site, each having a 120° effective beam width, are used to reduce mutual interference. With three sectors, $M = 3M_s$ where M_s is the number of users in each sector.

In a multi-cell environment, more forward link power must be provided to users near the boundaries of cells because they receive more interference from other cell-site transmitters [25]. Suppose that MS i, communicating via the sector 1 antenna, receives power S_{T_1} from the sector 1 BS, and MS i can receive a total of K signal powers from K different sector antennas. Therefore, the total power received by MS i is $\sum_{j=1}^{K} S_{T_j}$ and S_{T_j} for $j \neq 1$ are interference powers. For MS i to select the sector 1 BS as the home BS, S_{T_1} should be the largest power among all the received signal powers. Let

$$S_{T_1} > S_{T_2} > \ldots > S_{T_K} > 0. \tag{5.5}$$

In general, a fraction of the total power transmitted by any sector is devoted to the pilot signal and other overhead signals destined to all MS's. The remaining fraction ρ is then allocated to all M_s users of the sector. Let f_i be the relative received sector power at MS i where

$$f_i = \left(1 + \sum_{j=2}^{K} S_{T_j} / S_{T_1}\right)_i, \qquad i = 1, \ldots, M_s. \tag{5.6}$$

Then, it can be shown that [25]

$$\sum_{i=1}^{M_s} f_i \le \frac{\rho W / R}{E_b / N_o} - \sum_{i=1}^{M_s} \frac{\eta}{S_{T_{1_i}}}. \tag{5.7}$$

The background noise is usually negligible even when compared to the smallest received sector power from the home BS of any MS, i.e. $\min\{S_{T_{1_1}}, S_{T_{1_2}}, \ldots, S_{T_{1_{M_s}}}\}$. Therefore, the second sum in the right hand side of (5.7) is almost negligible. As the E_b/N_o requirement in the system is lowered, the value in the right hand side of (5.7) increases. However, the relative received sector power at MS i, f_i, remains unchanged when E_b/N_o changes. Therefore, more users can be added to the system when the E_b/N_o requirement is lowered. For a given decrease in E_b/N_o, the number of users which can be added depends on their relative received sector powers, f_i. The smaller these powers are, the larger is the number of additional users which can be supported, e.g. more MS's can be supported if they are close to their home BS's.

5.4.2 Multi-cell IS-2000 Reverse Link Capacity

Similarly, we can estimate the reverse link capacity. In the reverse link, although MS's communicating via different sector antennas are power controlled by their respective BS's, the signal powers from these MS's constitute interference to the neighboring cells. Therefore, a loading factor l, which typically has a value between 0% and 100%, is used to account for this interference [26]. Furthermore, a fraction of the total power transmitted by the MS is devoted to the reverse pilot signal. The remaining fraction δ is then used for traffic channel signal. Equation (5.3) then becomes

$$E_b / N_o = \frac{\delta W / R}{(M_s - 1)(1 + l) + \eta / S}. \tag{5.8}$$

The capacity is

$$M_s = (\frac{\delta W/R}{E_b/N_o} - \frac{\eta}{S})(\frac{1}{1+l}) + 1. \tag{5.9}$$

The reverse link capacity is seen to be approximately inversely proportional to E_b/N_o.

From the capacity analyses of the forward link and reverse link, it can be seen that a reduction in the E_b/N_o requirement results in an increase in the system capacity.

6.0 Simulations

In power controlled cellular networks, a power competition between users occurs since a power increase by one transmitter creates additional interference to unintended receivers, which can result in the receivers contending for more power to improve their SIR. The opposite is true when one transmitter reduces its power and the overall interference is reduced. The proposed CLPC algorithm can reduce power oscillation amplitude and improve SIR estimation, which means less fading margin is needed and the mutual interference in the system is reduced. In this chapter, system simulations using the IS-2000 model described in Chapter 4 are used to illustrate the performance of the proposed CLPC algorithm. Simulation runs have been carried out by changing the total delay, n_t, and the channel condition. The effect of PCB errors on the proposed CLPC algorithm performance is also studied using system simulations. The numerical results from simulations are presented in sections 6.1, 6.2 and 6.3, and the results are analyzed in section 6.4.

6.1 Numerical Results for 800 MHz Band

We first study the effect of loop delays on FER. The various delay values considered are n_t = 1, 2 and 3 PCG slots. Furthermore, we compare the FER performance of the conventional and the proposed CLPC algorithms. Two results for the proposed CLPC algorithm, Proposed(D) and Proposed(D+0.5), where D is the number of PCG slots that is linearly extrapolated (D=n_t−1) in order to obtain a SIR estimation are run. The two results show the performance of the proposed CLPC algorithm from equation (5.1) when linear extrapolation is used to predict fade values D PCG slots and D+0.5 PCG slots ahead. In our simulations, we use half of a PCG to

measure SIR and the SIR measurement is available in the middle of the PCG slot. As a PCB is executed at the beginning of a PCG, there is a gap of 0.5 PCG between the SIR estimation using Proposed(D) and the execution of the corresponding PCB. Since the channel condition is changing over time, Proposed(D) and Proposed(D+0.5) show the outcome of including the 0.5 PCG delay in the prediction algorithm. Figure 16 illustrates the difference between Proposed(D) and Proposed(D+0.5).

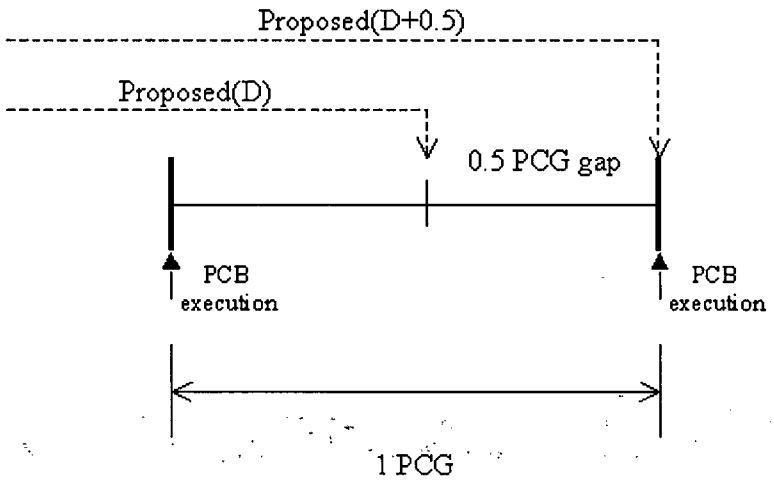


Figure 16 Difference between Proposed(D) and Proposed(D+0.5)

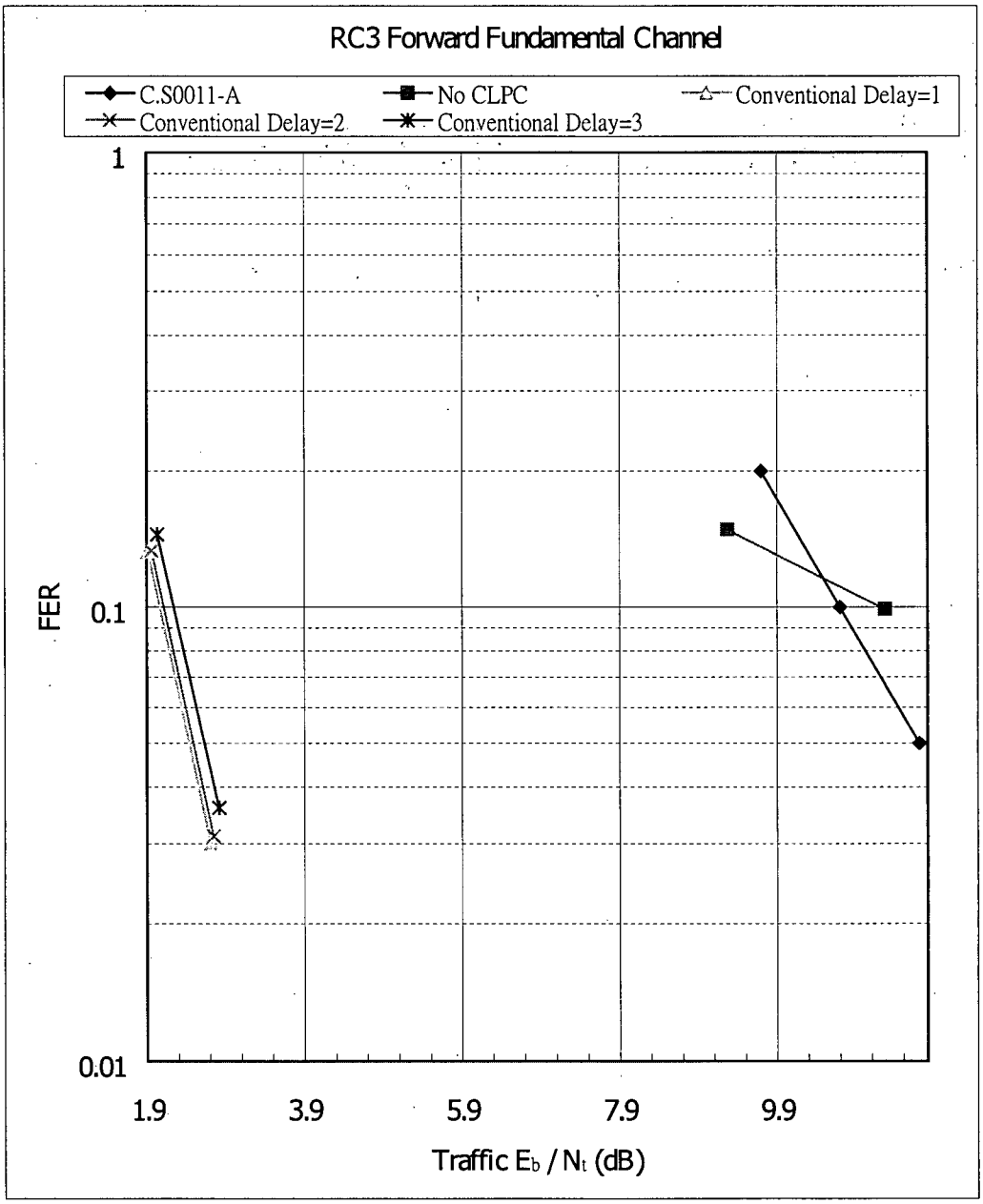
Figure 17 illustrates the effects of delays on FER in a 1 path 3 km/hr Rayleigh fading environment at 870 MHz. The minimum FER requirement stated in [22] and the FER performance without any CLPC are shown for comparison purposes. As expected, the FER performance is degraded when loop delay is increased.

Figure 18 and Figure 19 compare the proposed CLPC algorithm against the conventional CLPC algorithm in a 1 path 3 km/hr Rayleigh fading environment at 870 MHz when delay is 2 and 3 PCG respectively.

Similarly, different channel configuration simulations were run following the above structure. Table 8 summarizes the 800 MHz band simulation figures.

Table 8 Summary of 800 MHz Band Simulation Figures

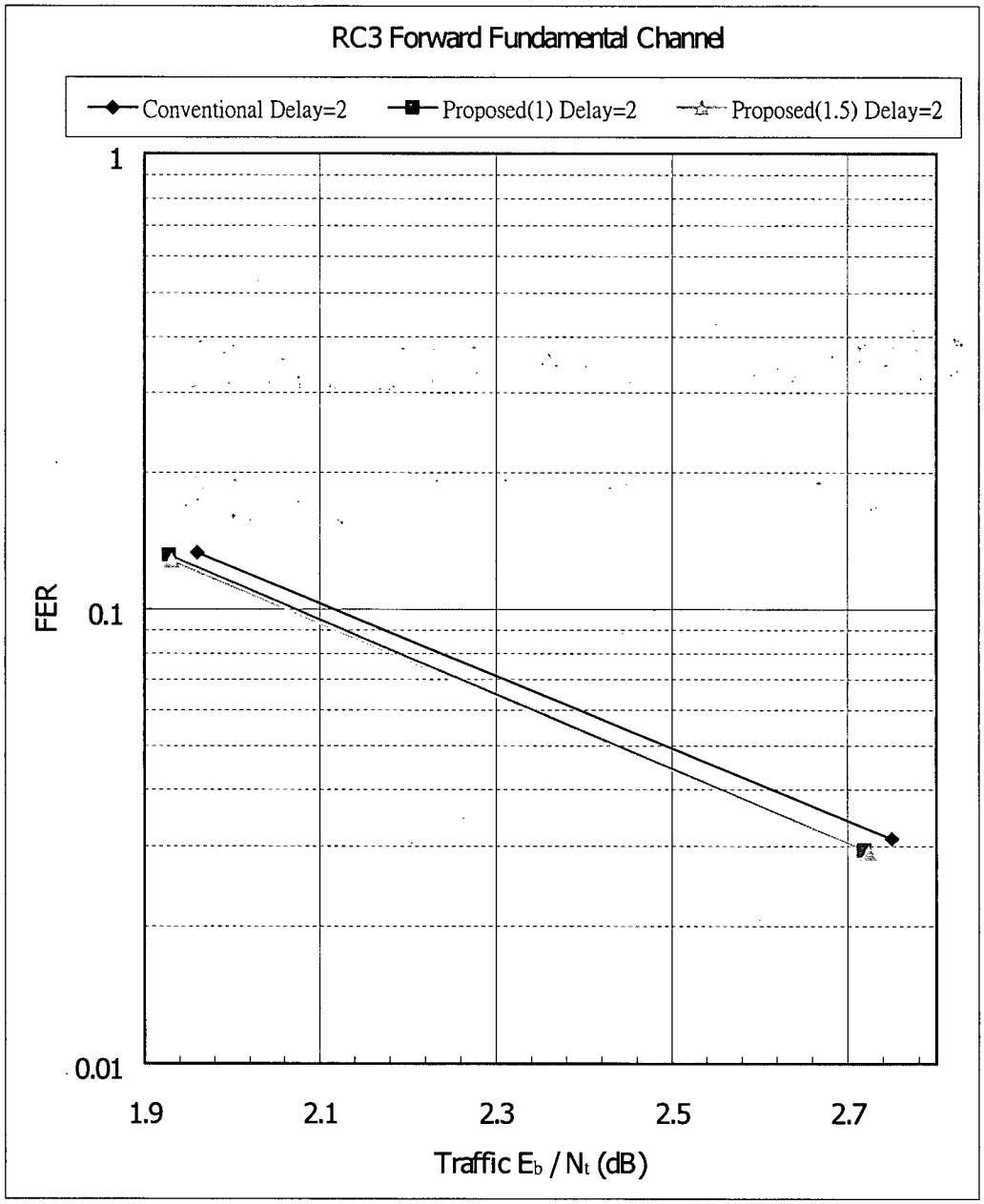
Channel Configuration	Description	Figure Number
1 path 3 km/hr	Effects of PCG delays on FER	Figure 17
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 18
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 19
1 path 30 km/hr	Effects of PCG delays on FER	Figure 20
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 21
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 22
3 path 100 km/hr	Effects of PCG delays on FER	Figure 23
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 24
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 25
1 path 50 km/hr	Effects of PCG delays on FER	Figure 26
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 27
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 28
1 path 100 km/hr	Effects of PCG delays on FER	Figure 29
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 30
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 31
3 path 30 km/hr	Effects of PCG delays on FER	Figure 32
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 33
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 34



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±7.3%	±8.9%
Conventional Delay=1	±7.7%	±16.3%
Conventional Delay=2	±7.6%	±16%
Conventional Delay=3	±7.4%	±14.9%

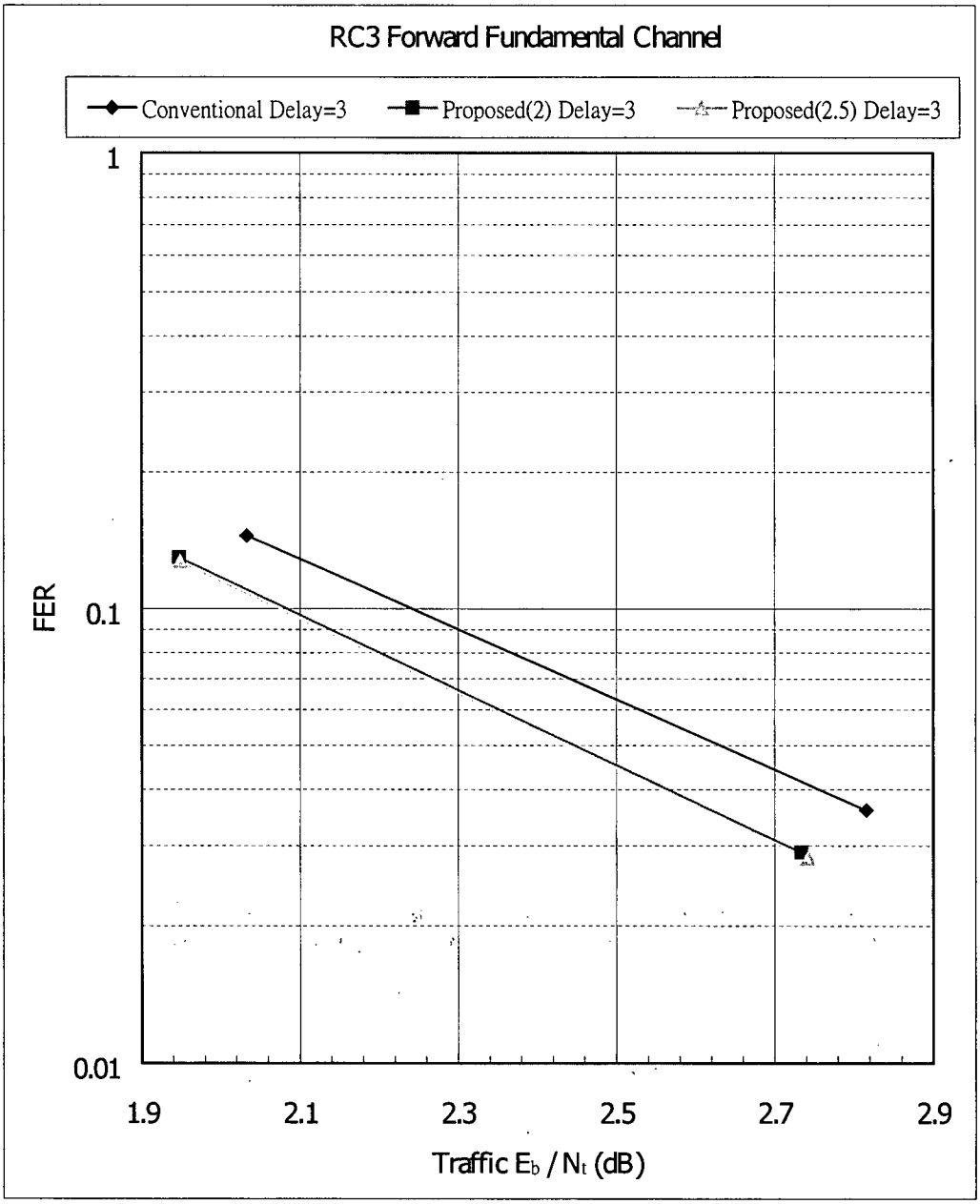
Figure 17 Effects of PCG Delays on FER (1 path 3 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±7.6%	±16%
Proposed(1) Delay=2	±7.7%	±16.5%
Proposed(1.5) Delay=2	±7.8%	±16.6%

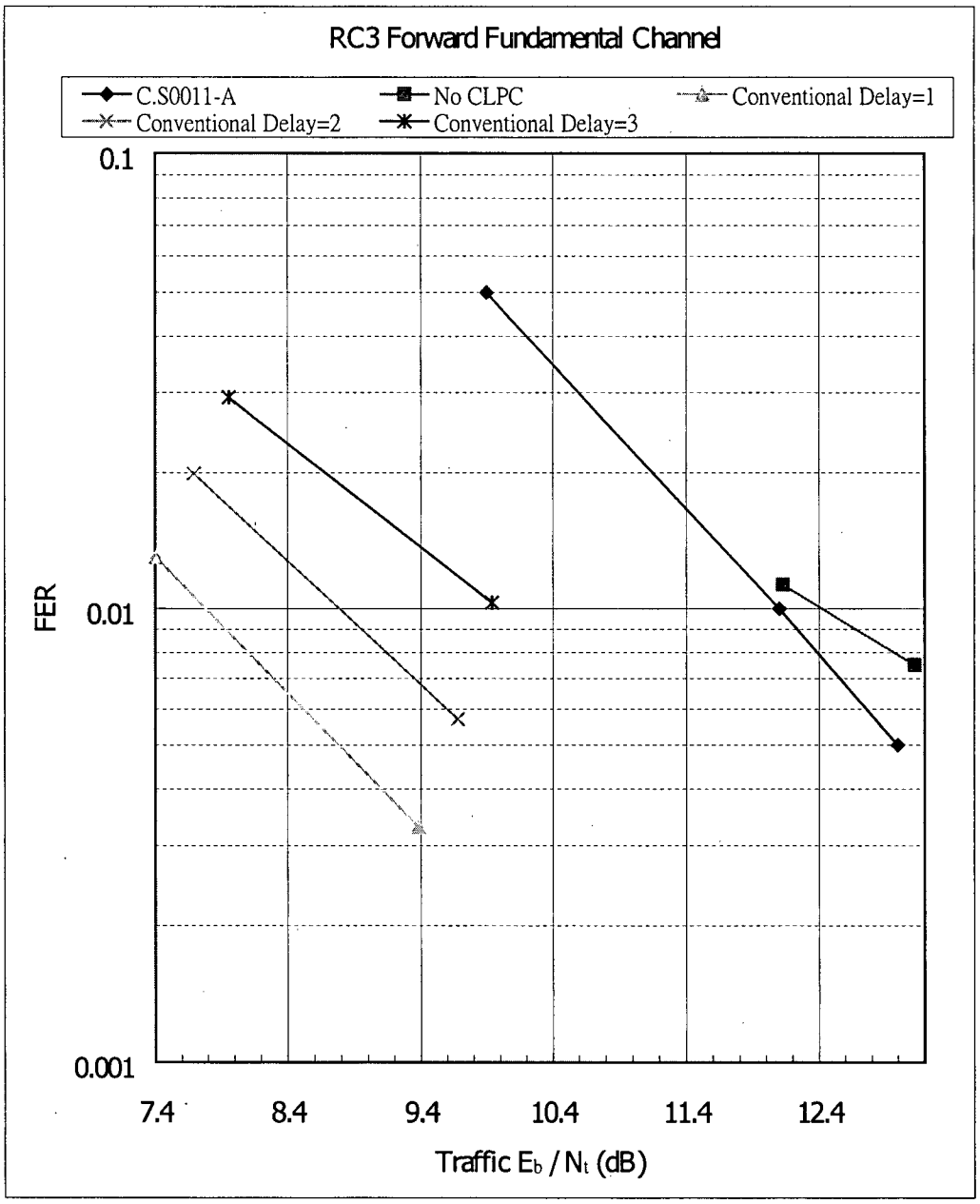
Figure 18 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 3 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±7.4%	±14.9%
Proposed(2) Delay=3	±7.8%	±16.6%
Proposed(2.5) Delay=3	±7.8%	±16.8%

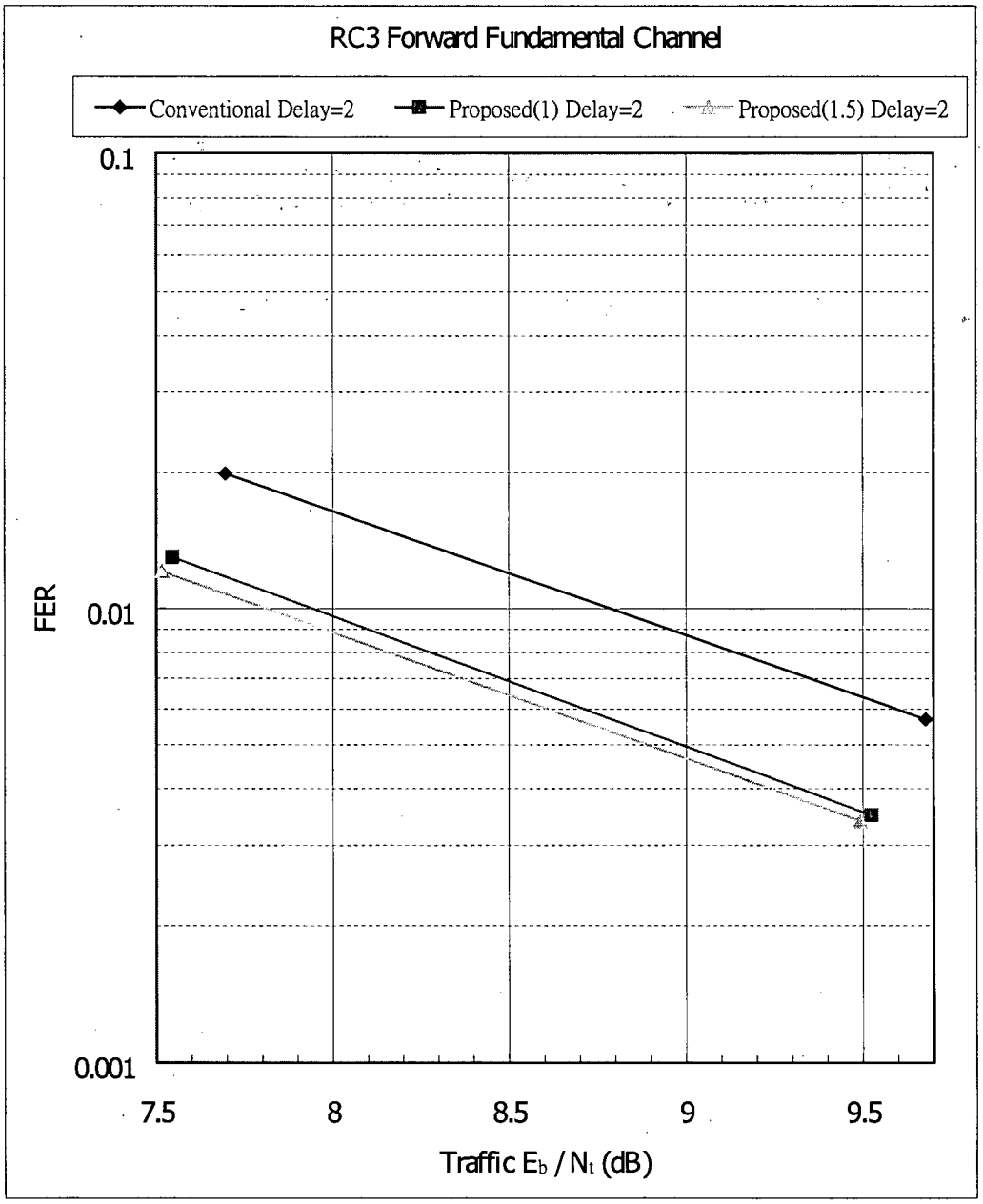
Figure 19 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 3 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±18.9%	±23.3%
Conventional Delay=1	±17.5%	±35.8%
Conventional Delay=2	±14.1%	±26.9%
Conventional Delay=3	±11.6%	±19.5%

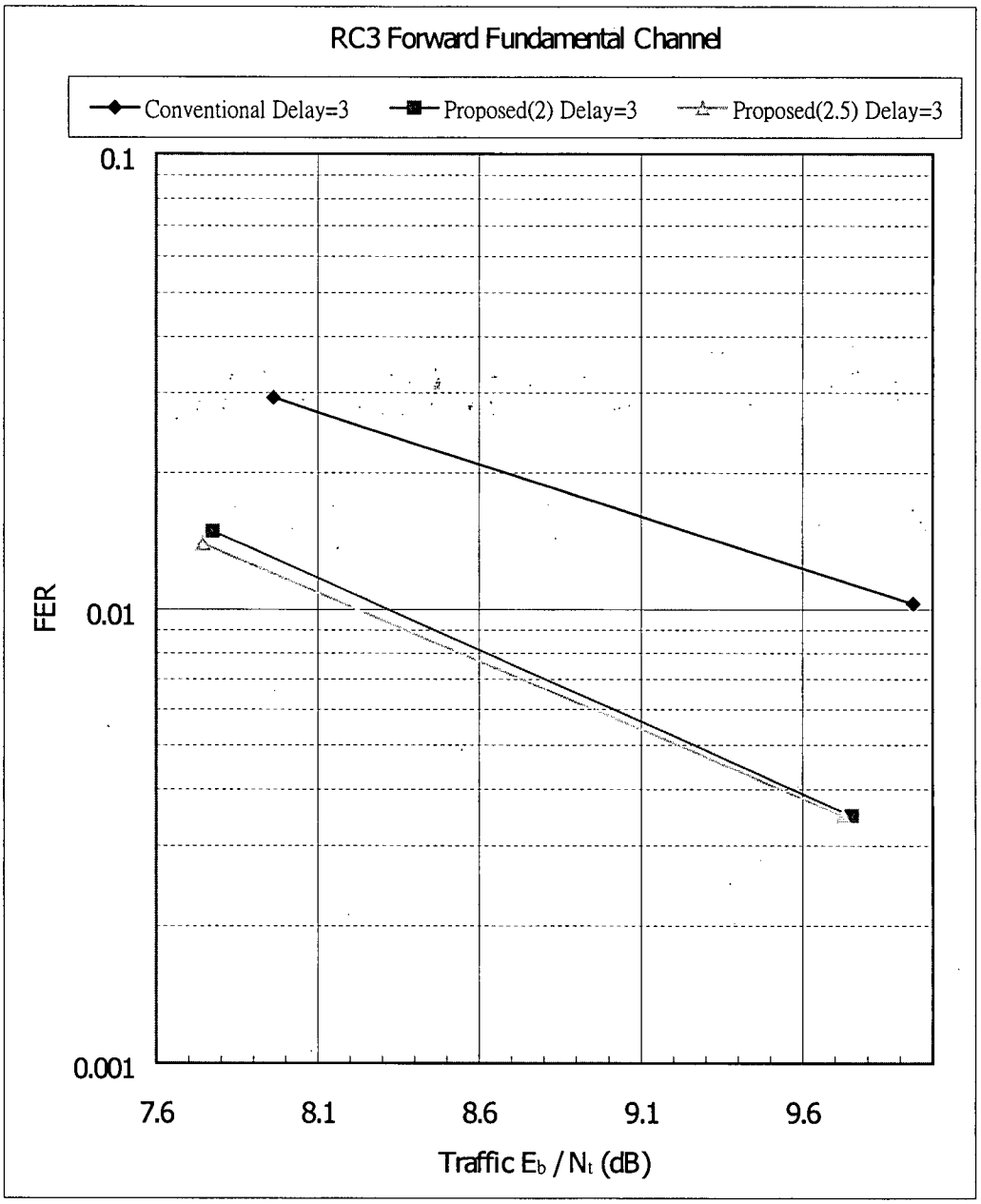
Figure 20 Effects of PCG Delays on FER (1 path 30 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±14.1%	±26.9%
Proposed(1) Delay=2	±17.5%	±34.7%
Proposed(1.5) Delay=2	±18.2%	±35.2%

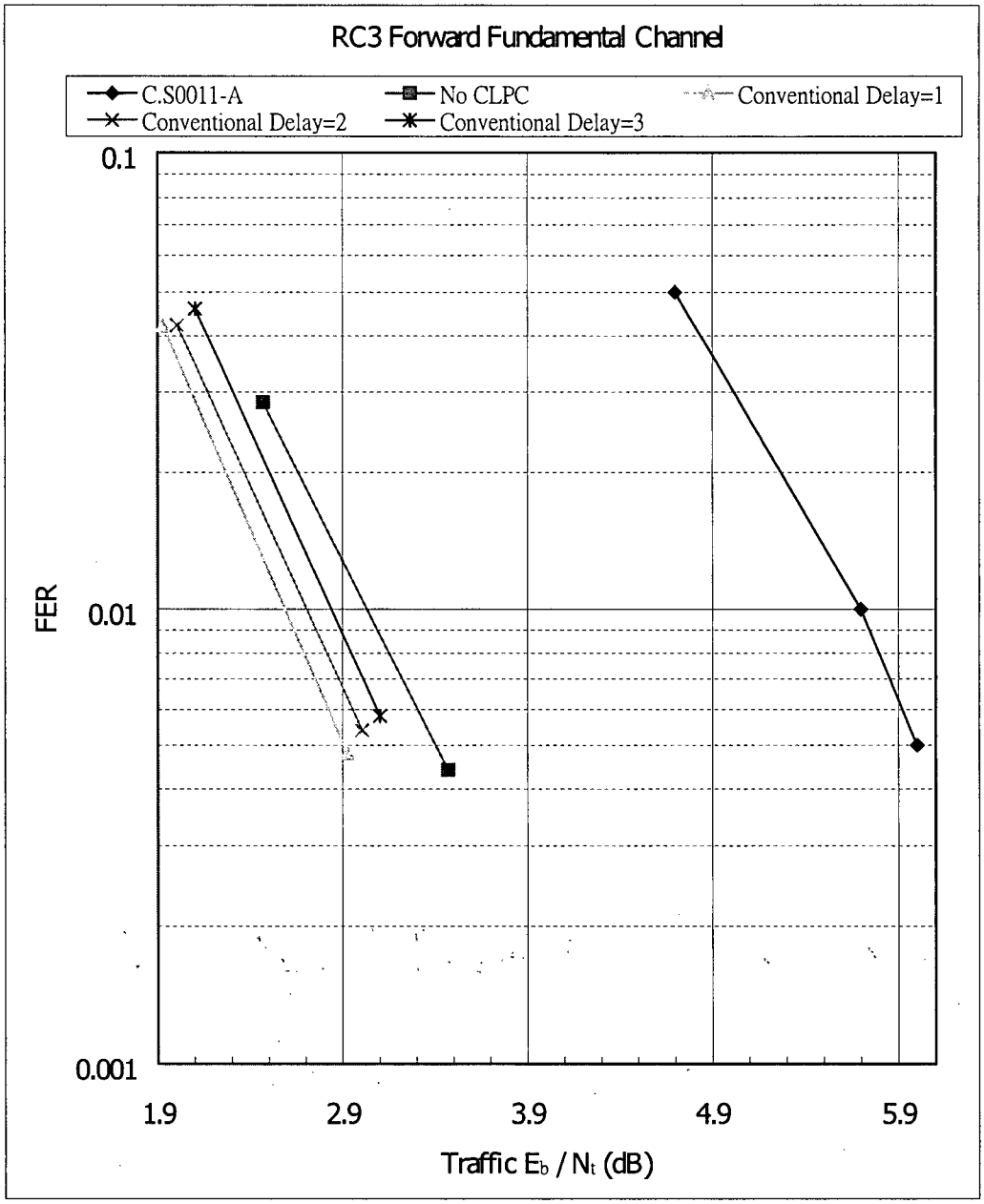
Figure 21 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 30 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±11.6%	±19.5%
Proposed(2) Delay=3	±16.4%	±34.7%
Proposed(2.5) Delay=3	±16.9%	±34.7%

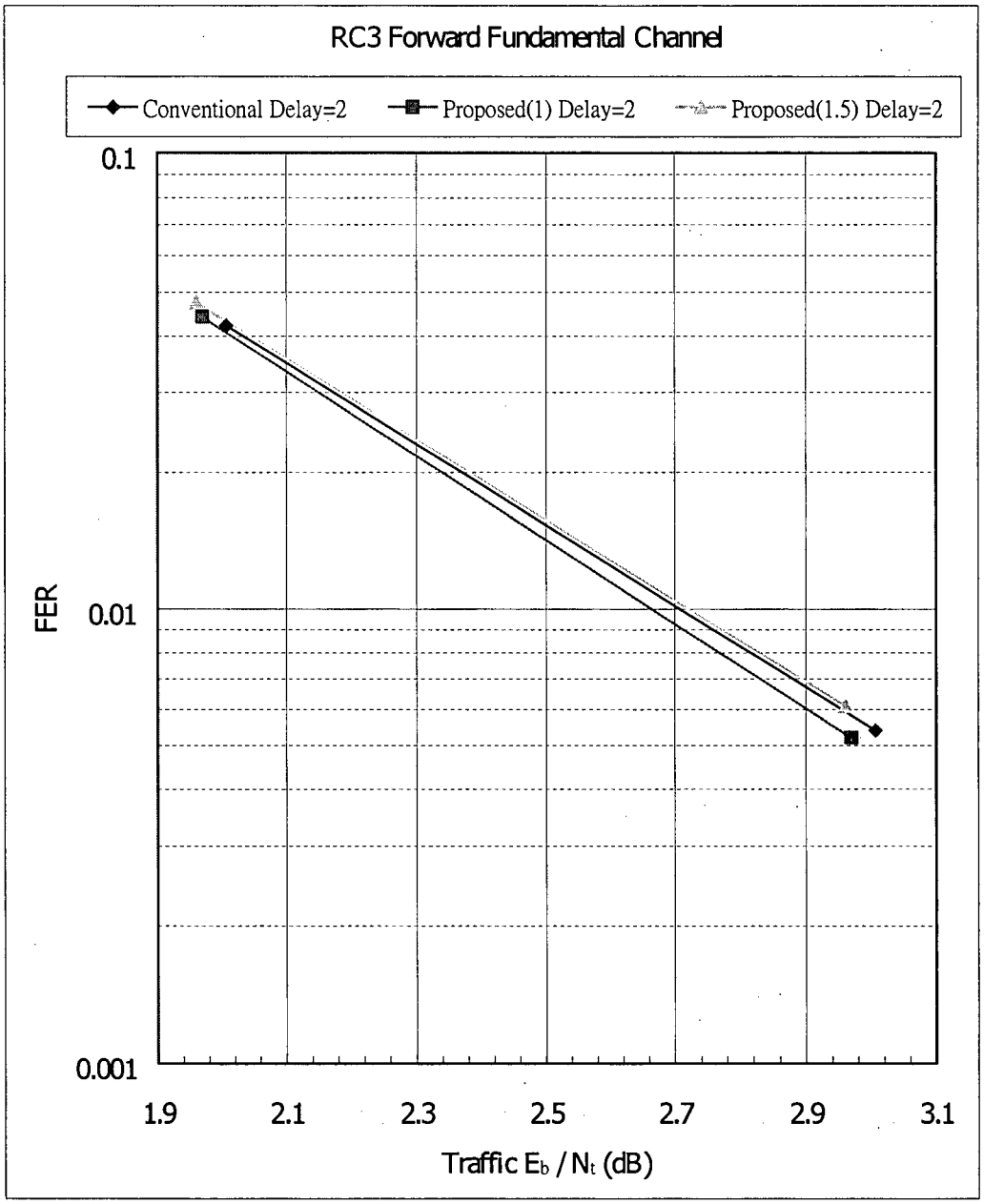
Figure 22 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 30 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±11.8%	±30.7%
Conventional Delay=1	±9.6%	±29.4%
Conventional Delay=2	±9.6%	±27.7%
Conventional Delay=3	±9.2%	±26.7%

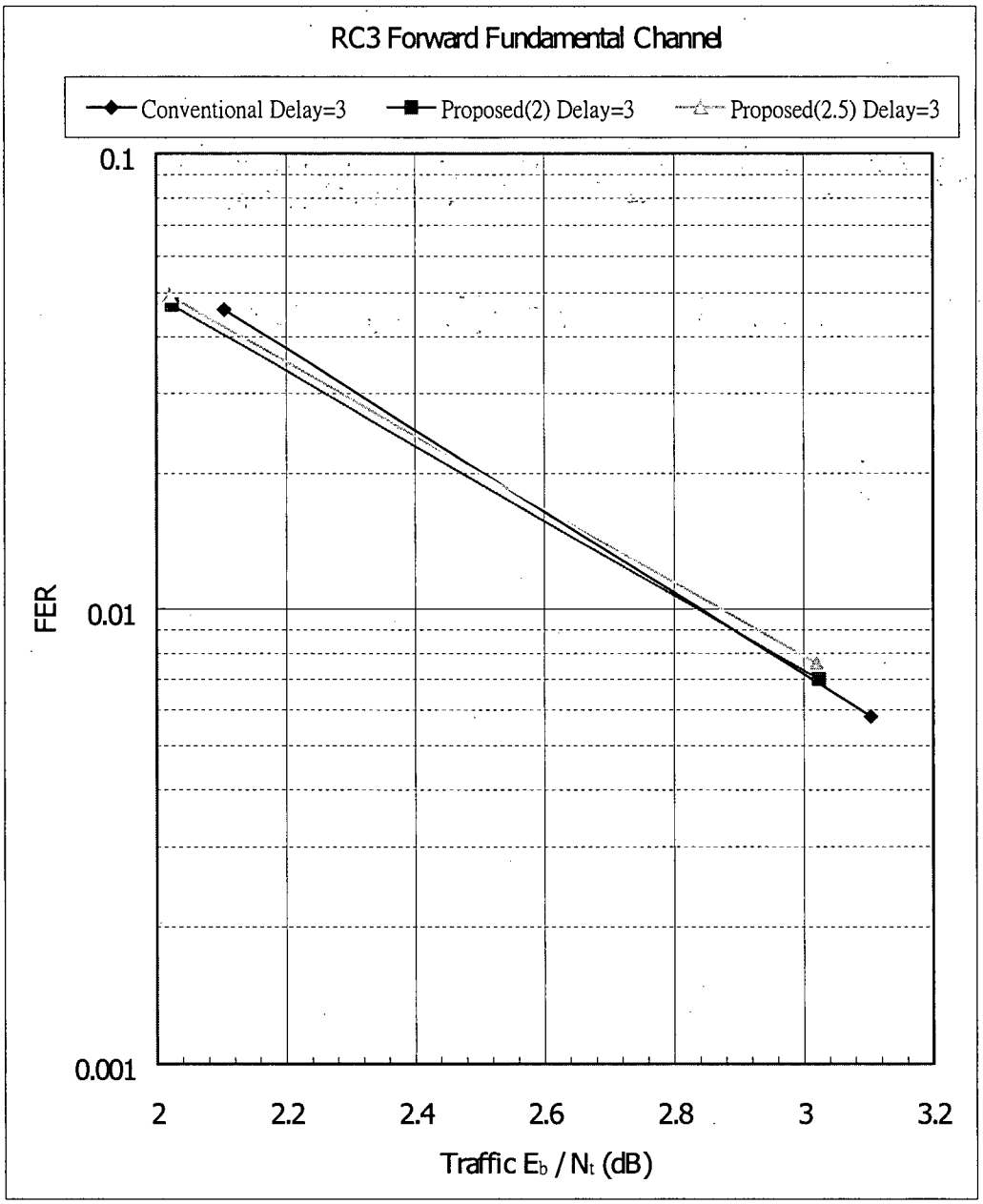
Figure 23 Effects of PCG Delays on FER (3 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±9.6%	±27.7%
Proposed(1) Delay=2	±9.4%	±28.2%
Proposed(1.5) Delay=2	±9.1%	±26%

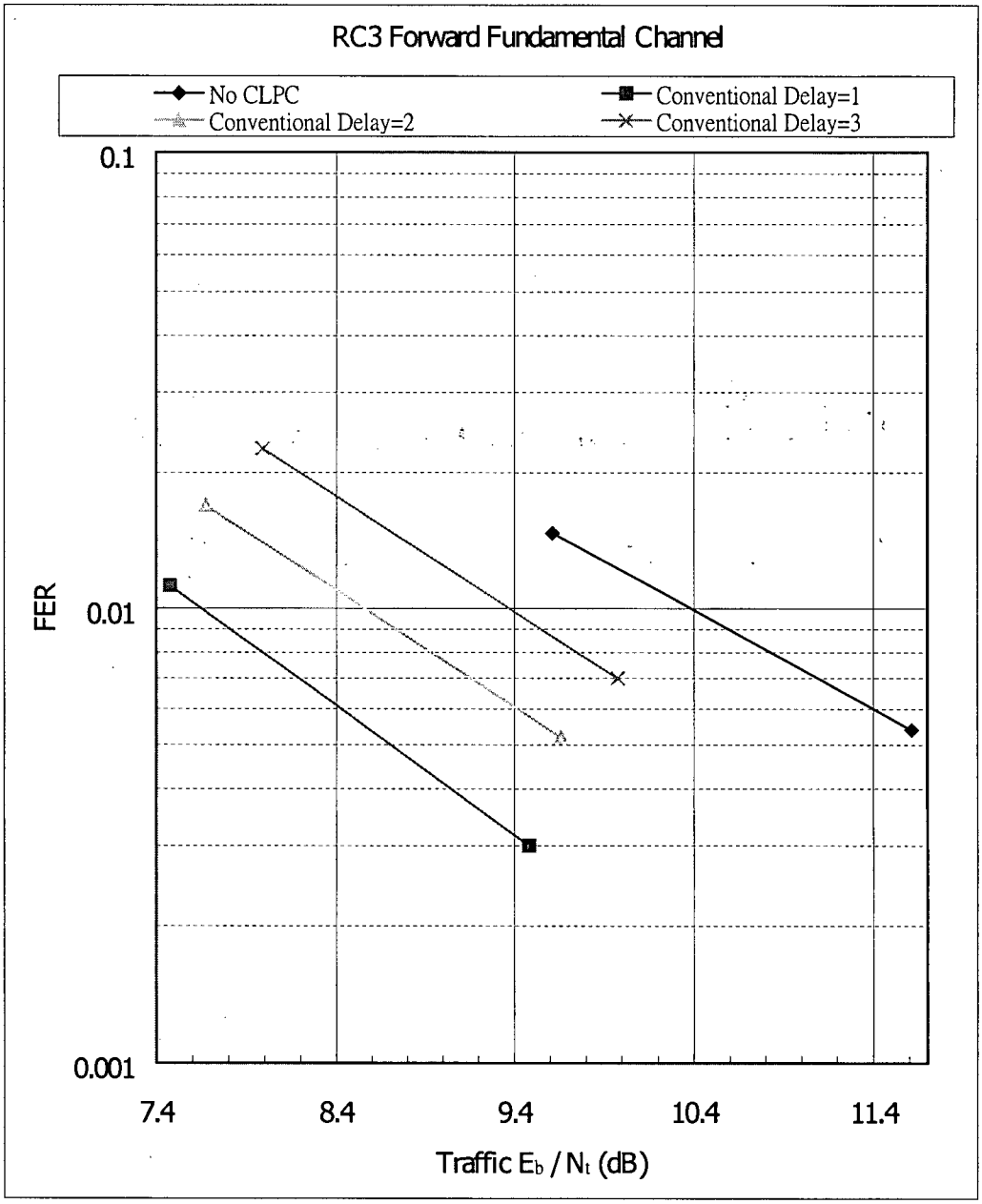
Figure 24 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (3 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±9.2%	±26.7%
Proposed(2) Delay=3	±9.1%	±24.1%
Proposed(2.5) Delay=3	±8.9%	±23.2%

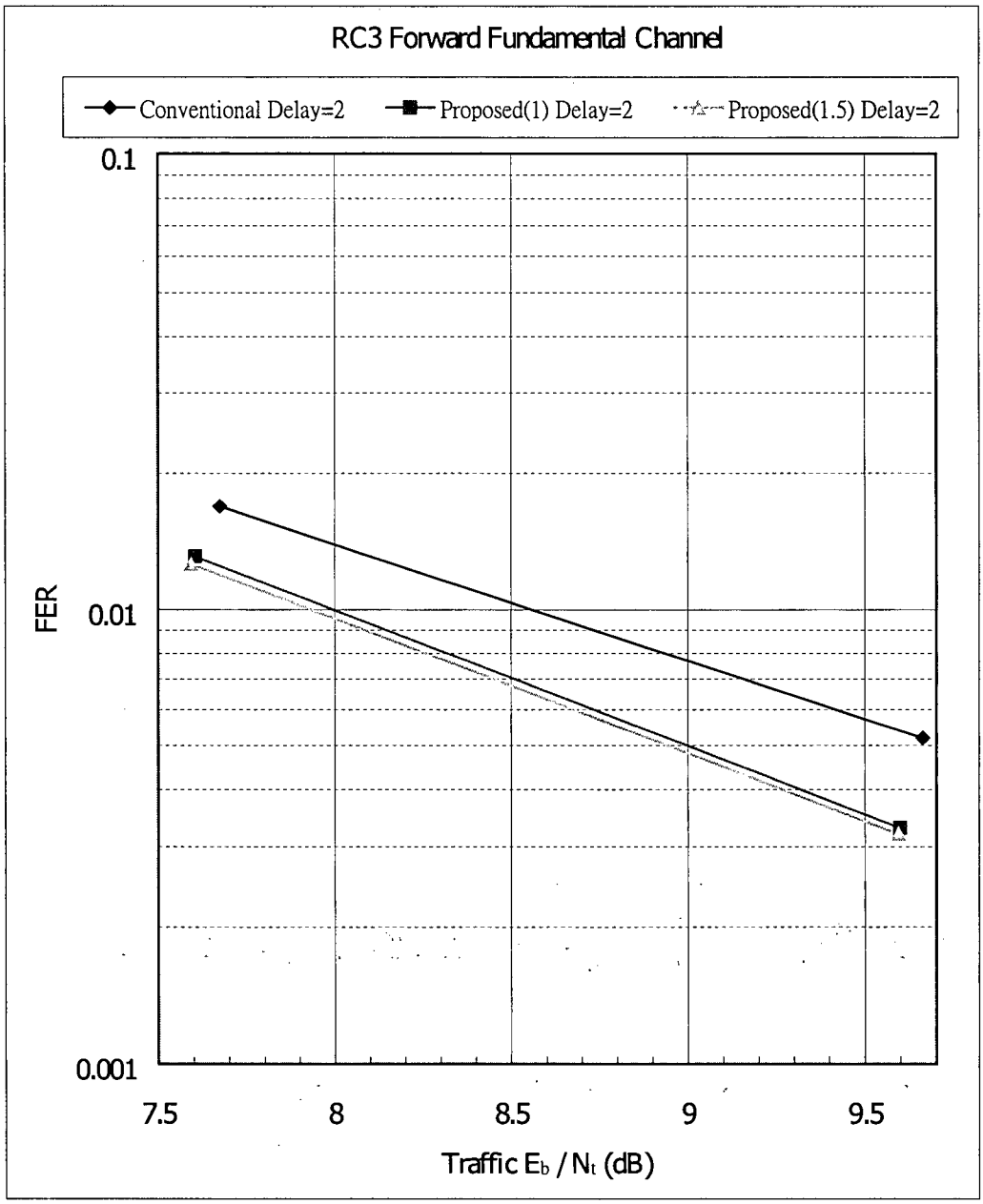
Figure 25 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (3 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±16.5%	±27.7%
Conventional Delay=1	±19%	±37.6%
Conventional Delay=2	±15.4%	±28.2%
Conventional Delay=3	±13.2%	±24.1%

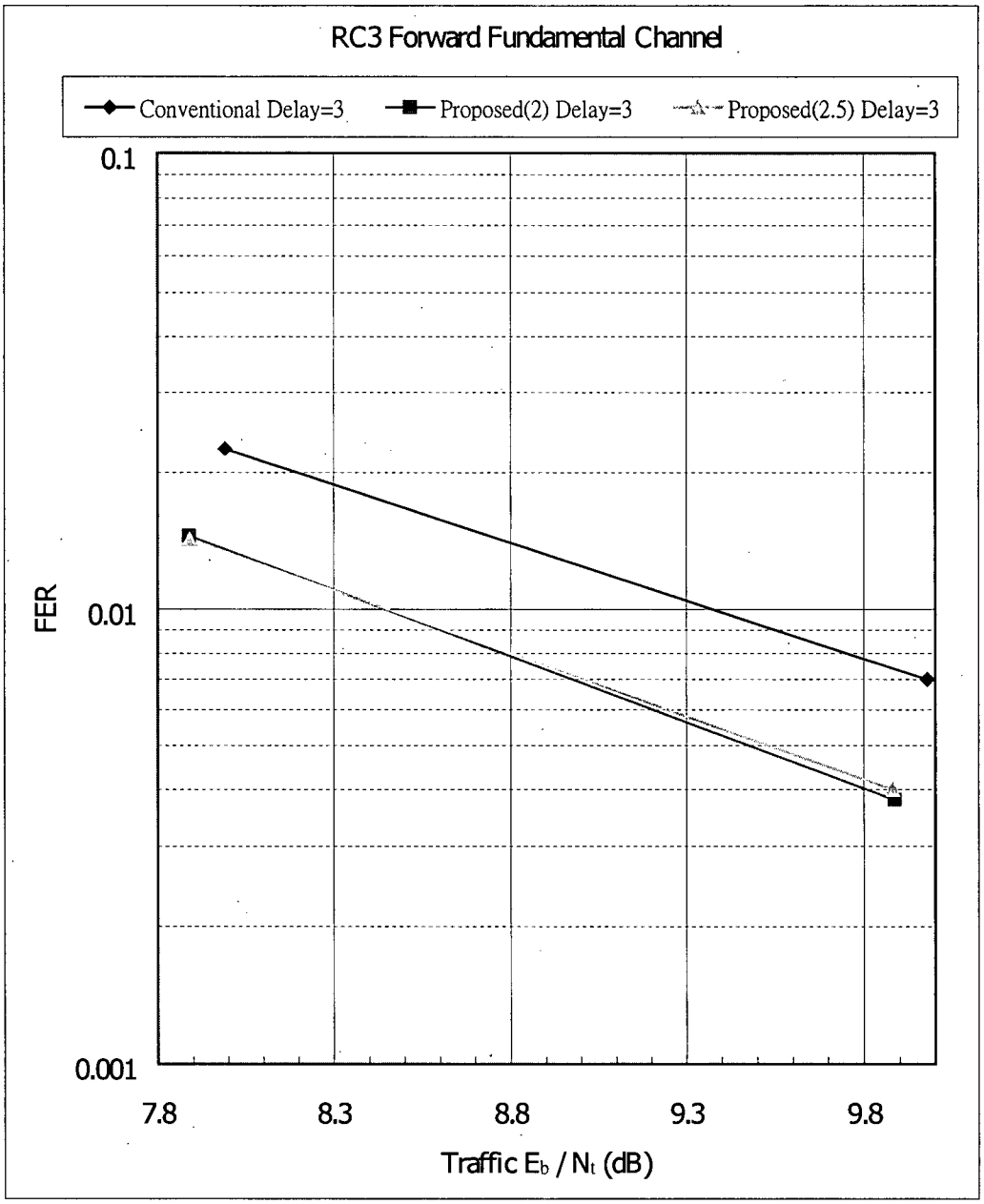
Figure 26 Effects of PCG Delays on FER (1 path 50 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±15.4%	±28.2%
Proposed(1) Delay=2	±17.5%	±35.8%
Proposed(1.5) Delay=2	±17.9%	±36.4%

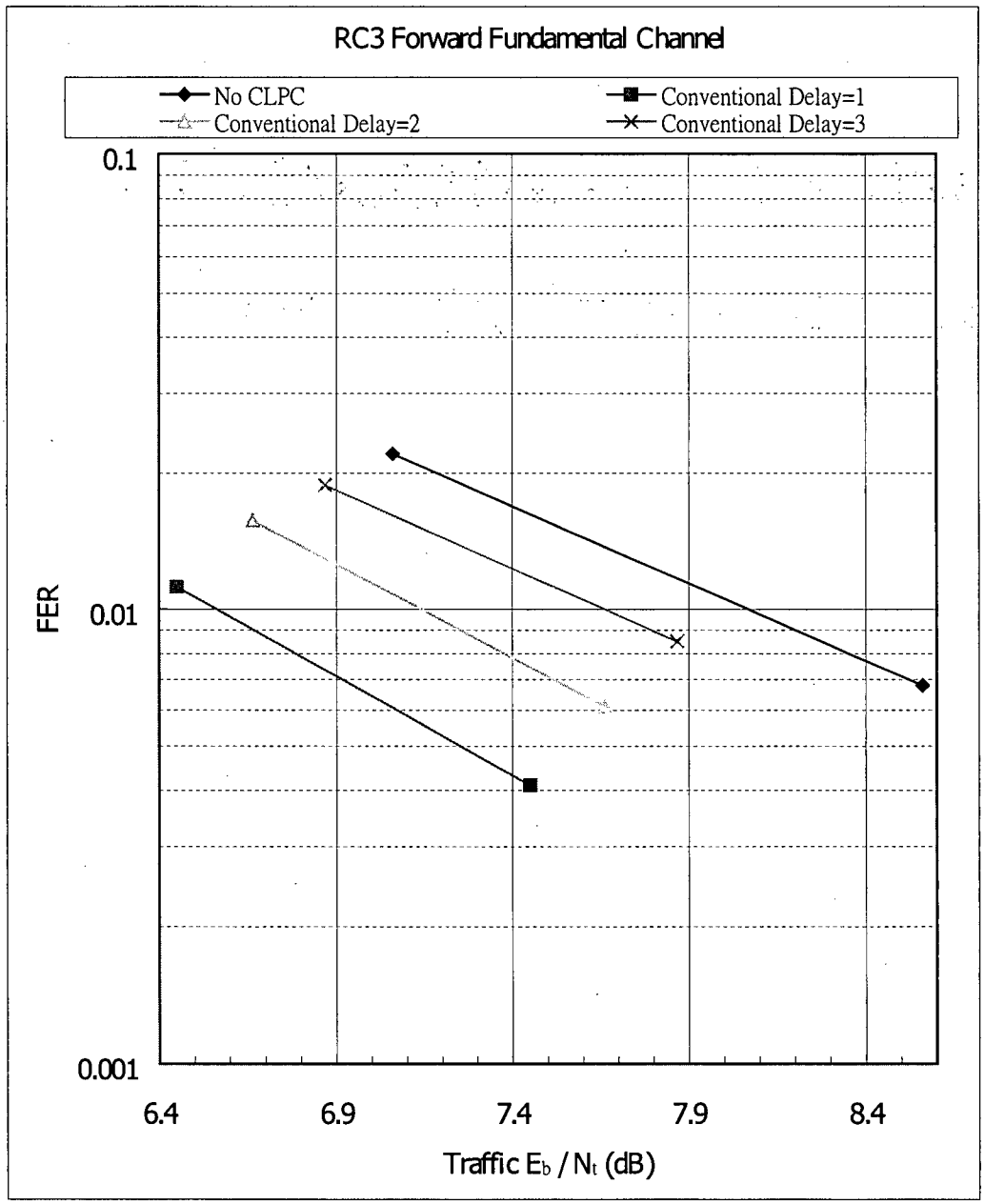
Figure 27 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 50 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±13.2%	±24.1%
Proposed(2) Delay=3	±16.6%	±33.2%
Proposed(2.5) Delay=3	±16.7%	±32.4%

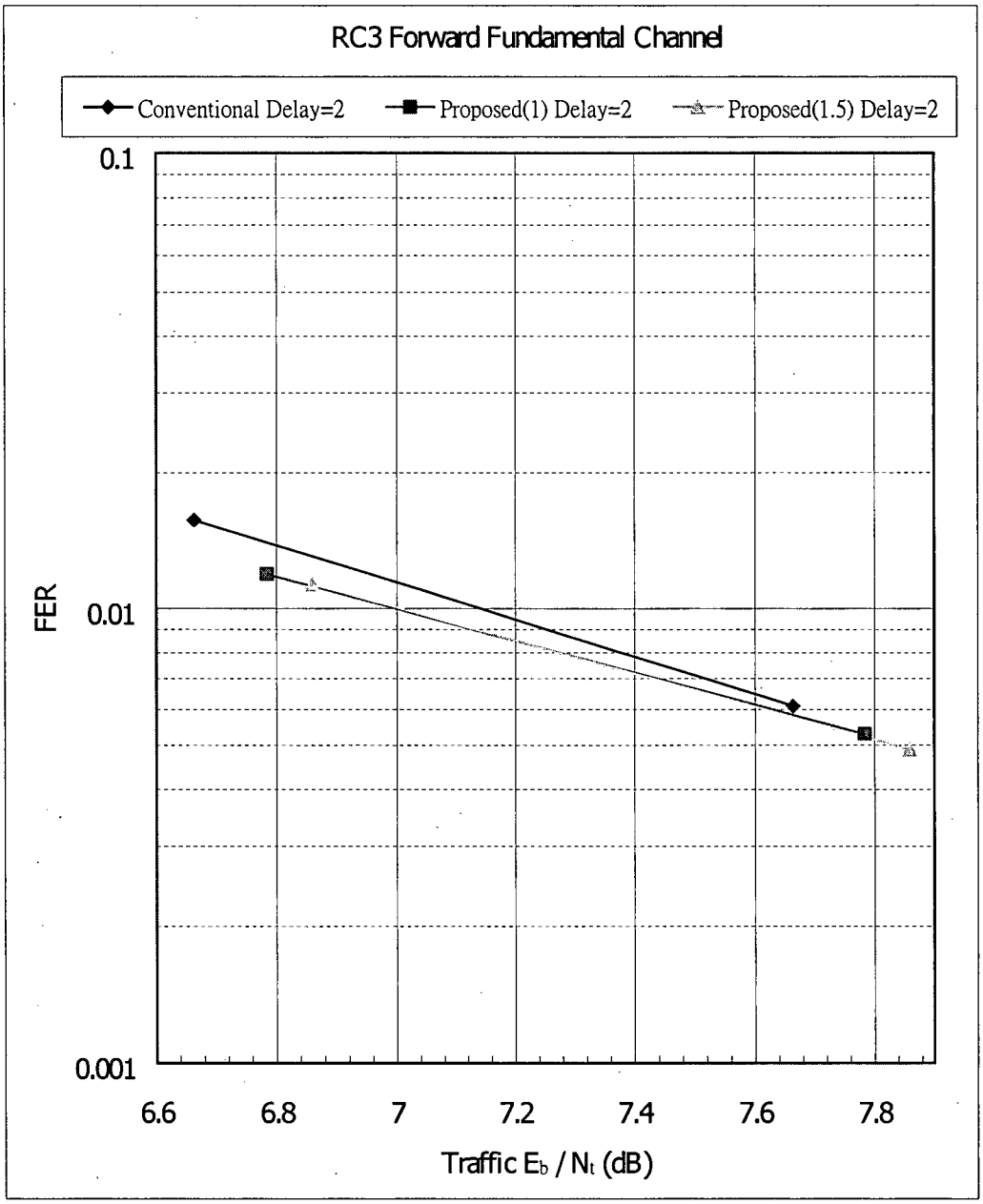
Figure 28 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 50 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±13.4%	±24.5%
Conventional Delay=1	±18.9%	±31.9%
Conventional Delay=2	±15.9%	±25.9%
Conventional Delay=3	±14.6%	±21.8%

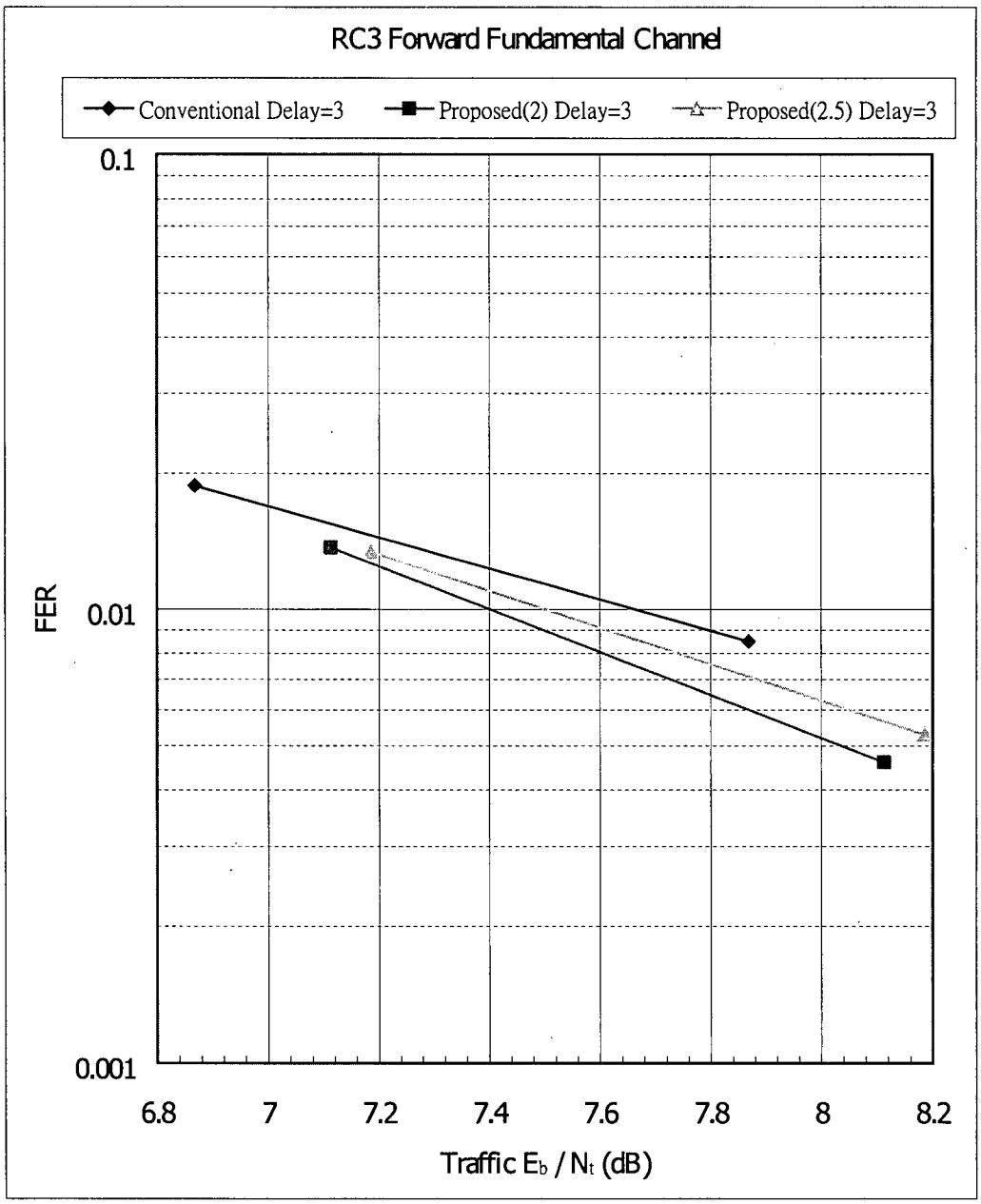
Figure 29 Effects of PCG Delays on FER (1 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±15.9%	±26%
Proposed(1) Delay=2	±18.4%	±27.9%
Proposed(1.5) Delay=2	±18.9%	±29.2%

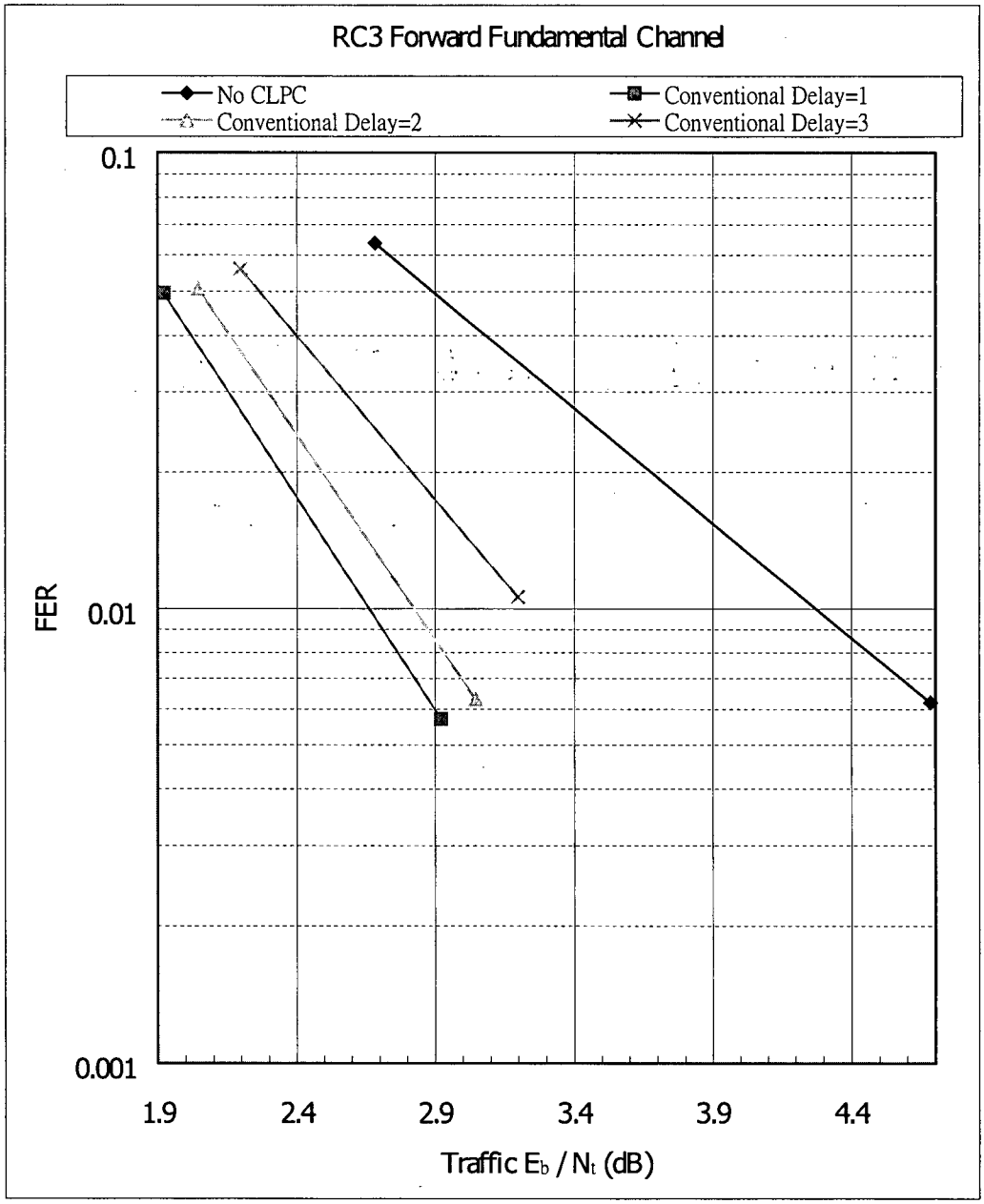
Figure 30 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±14.6%	±21.9%
Proposed(2) Delay=3	±17.1%	±30.1%
Proposed(2.5) Delay=3	±17.3%	±27.9%

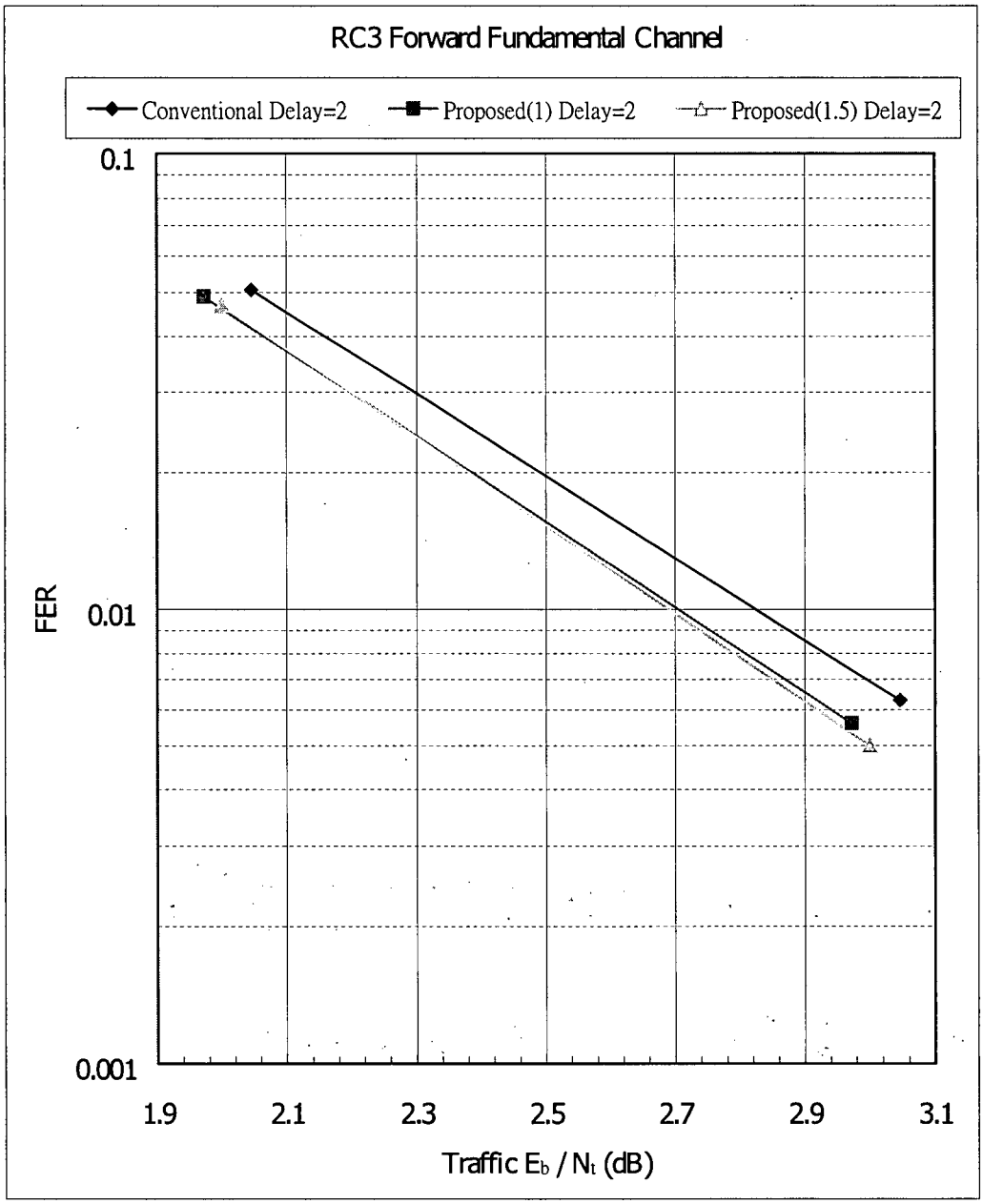
Figure 31 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 100 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±7.8%	±25.7%
Conventional Delay=1	±8.9%	±26.9%
Conventional Delay=2	±8.8%	±25.5%
Conventional Delay=3	±8.3%	±18.9%

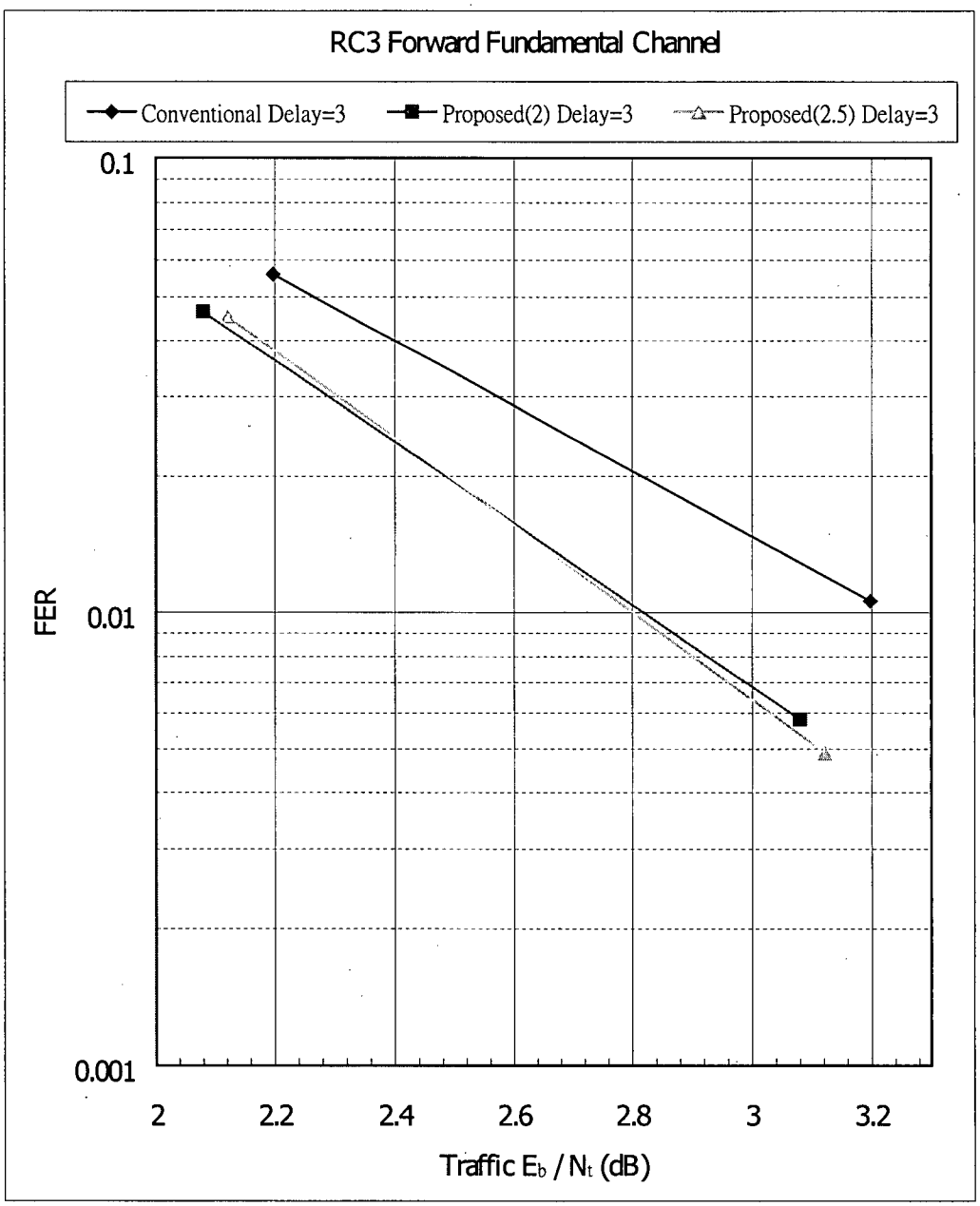
Figure 32 Effects of PCG Delays on FER (3 path 30 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±8.8%	±25.5%
Proposed(1) Delay=2	±9%	±27.2%
Proposed(1.5) Delay=2	±9.1%	±28.8%

Figure 33 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (3 path 30 km/hr Rayleigh Fading at 870 MHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±8.3%	±18.9%
Proposed(2) Delay=3	±9.2%	±26.6%
Proposed(2.5) Delay=3	±9.3%	±29.1%

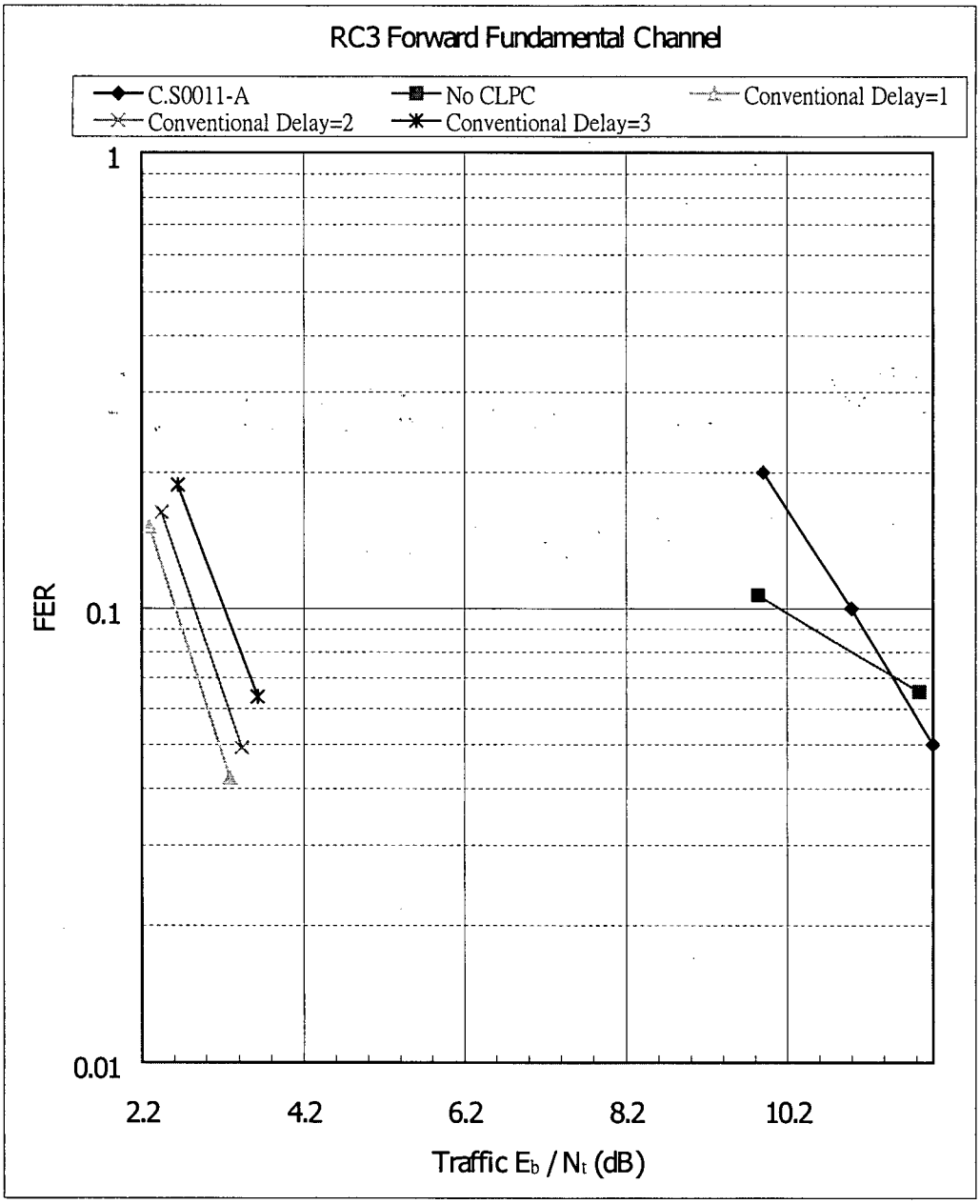
Figure 34 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (3 path 30 km/hr Rayleigh Fading at 870 MHz)

6.2 Numerical Results for 1.9 GHz Band

Another popular carrier frequency used for IS-2000 is in the 1.9 GHz band. Fading is more severe in the 1.9 GHz band when compared to the 800 MHz band for the same mobile speed because the Doppler frequency is higher. Table 9 summarizes the 1.9 GHz band simulations figures.

Table 9 Summary of 1.9 GHz Band Simulation Figures

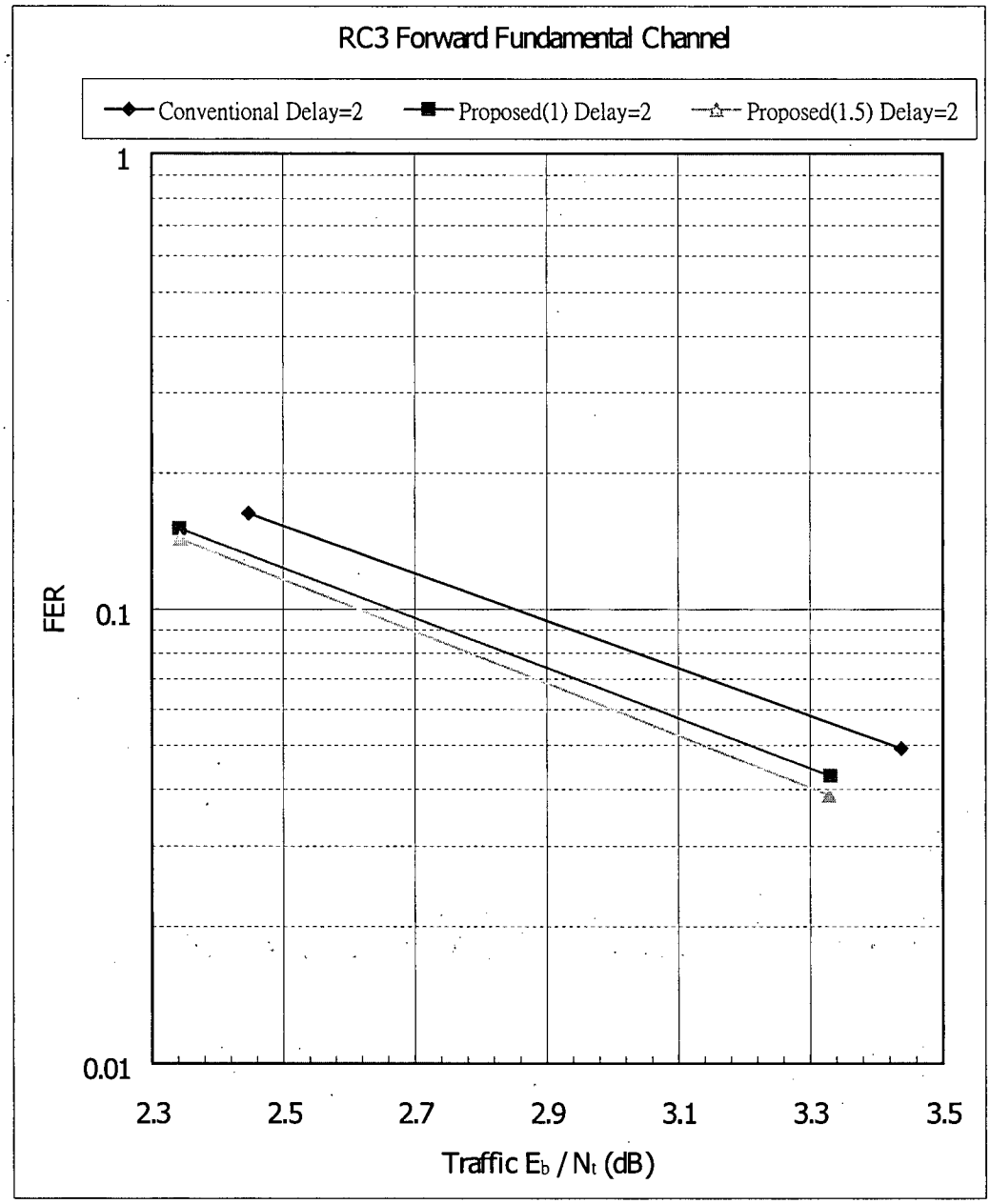
Channel Configuration	Description	Figure Number
1 path 3 km/hr	Effects of PCG delays on FER	Figure 35
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 36
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 37
1 path 30 km/hr	Effects of PCG delays on FER	Figure 38
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 39
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 40
3 path 100 km/hr	Effects of PCG delays on FER	Figure 41
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 42
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 43
1 path 50 km/hr	Effects of PCG delays on FER	Figure 44
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 45
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 46
1 path 100 km/hr	Effects of PCG delays on FER	Figure 47
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 48
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 49
3 path 30 km/hr	Effects of PCG delays on FER	Figure 50
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 51
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 52



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±8.3%	±11%
Conventional Delay=1	±7.2%	±13.7%
Conventional Delay=2	±6.9%	±12.7%
Conventional Delay=3	±6.4%	±11.1%

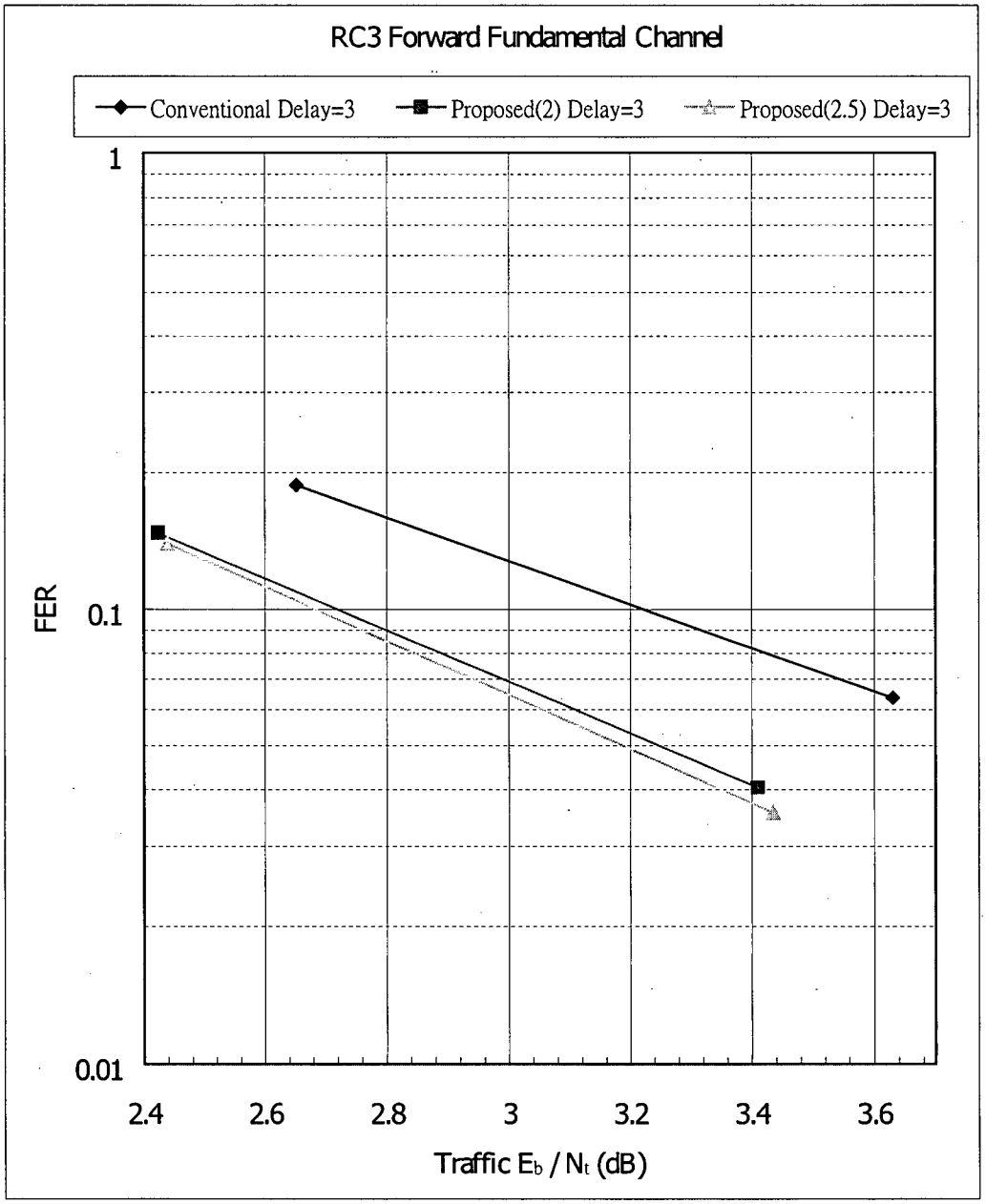
Figure 35 Effects of PCG Delays on FER (1 path 3 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±6.9%	±12.7%
Proposed(1) Delay=2	±7.2%	±13.6%
Proposed(1.5) Delay=2	±7.4%	±14.3%

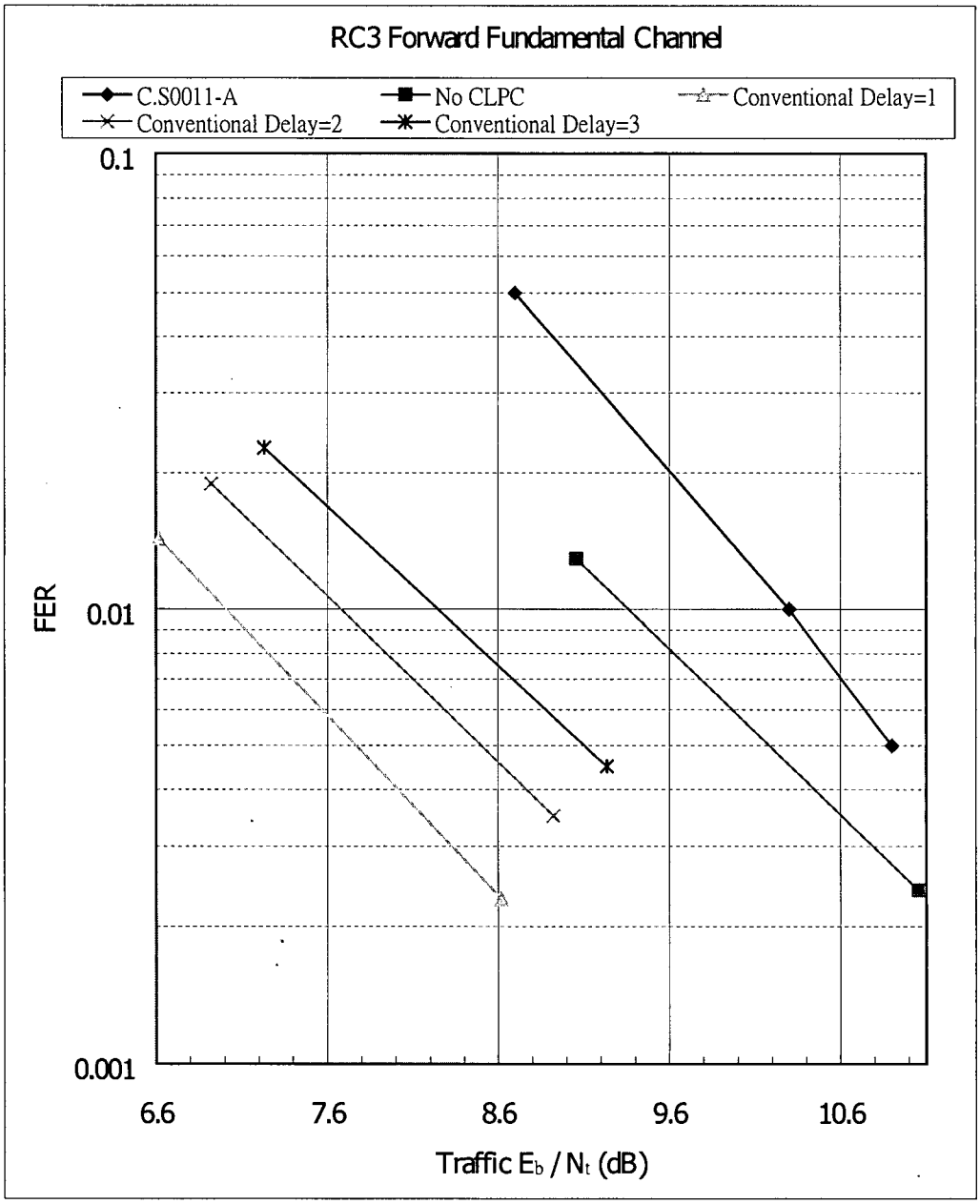
Figure 36 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 3 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±6.5%	±11.2%
Proposed(2) Delay=3	±7.3%	±14%
Proposed(2.5) Delay=3	±7.5%	±15%

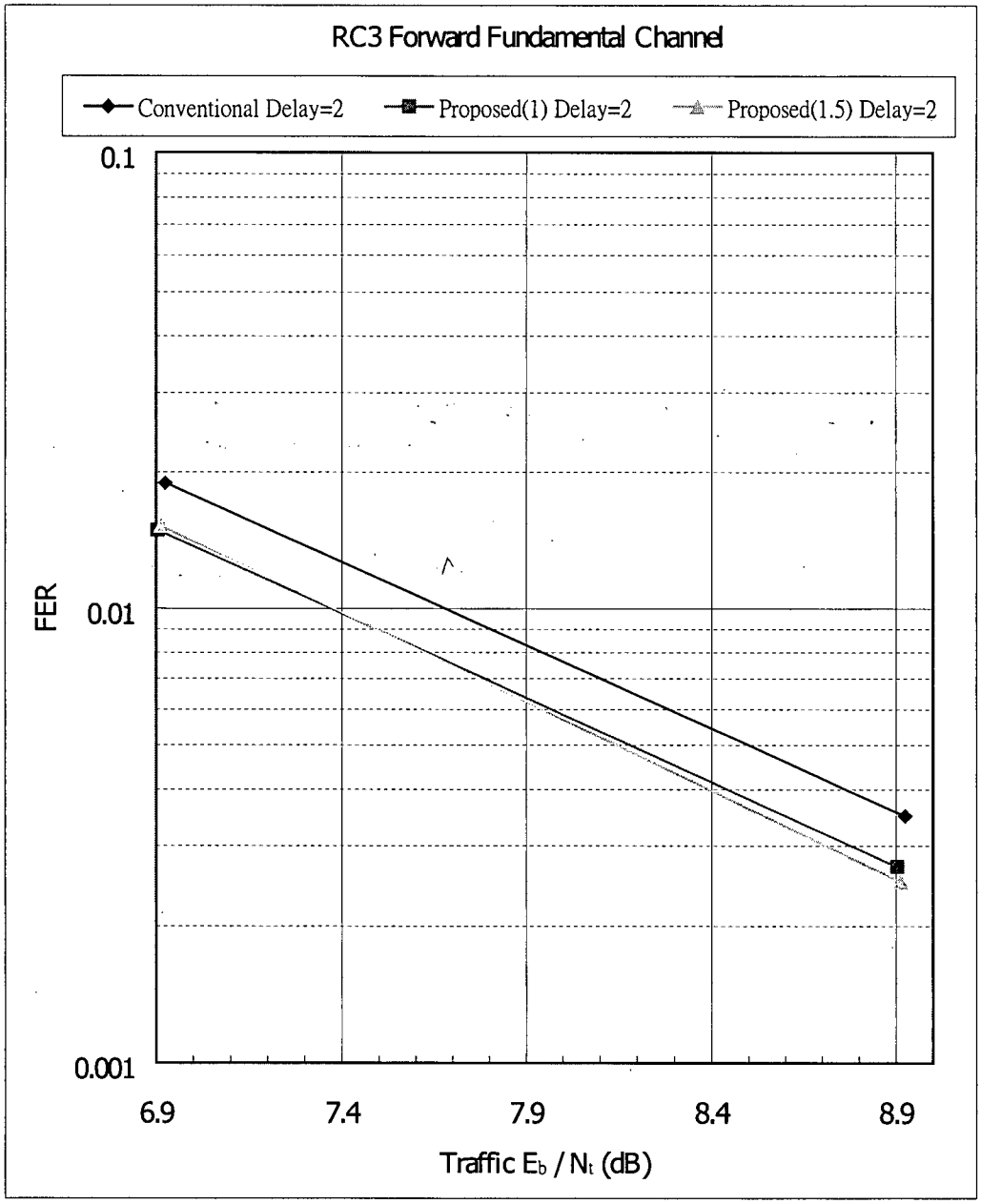
Figure 37 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 3 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±17.7%	±42.4%
Conventional Delay=1	±16.8%	±43.3%
Conventional Delay=2	±14.5%	±34.7%
Conventional Delay=3	±13.2%	±30.4%

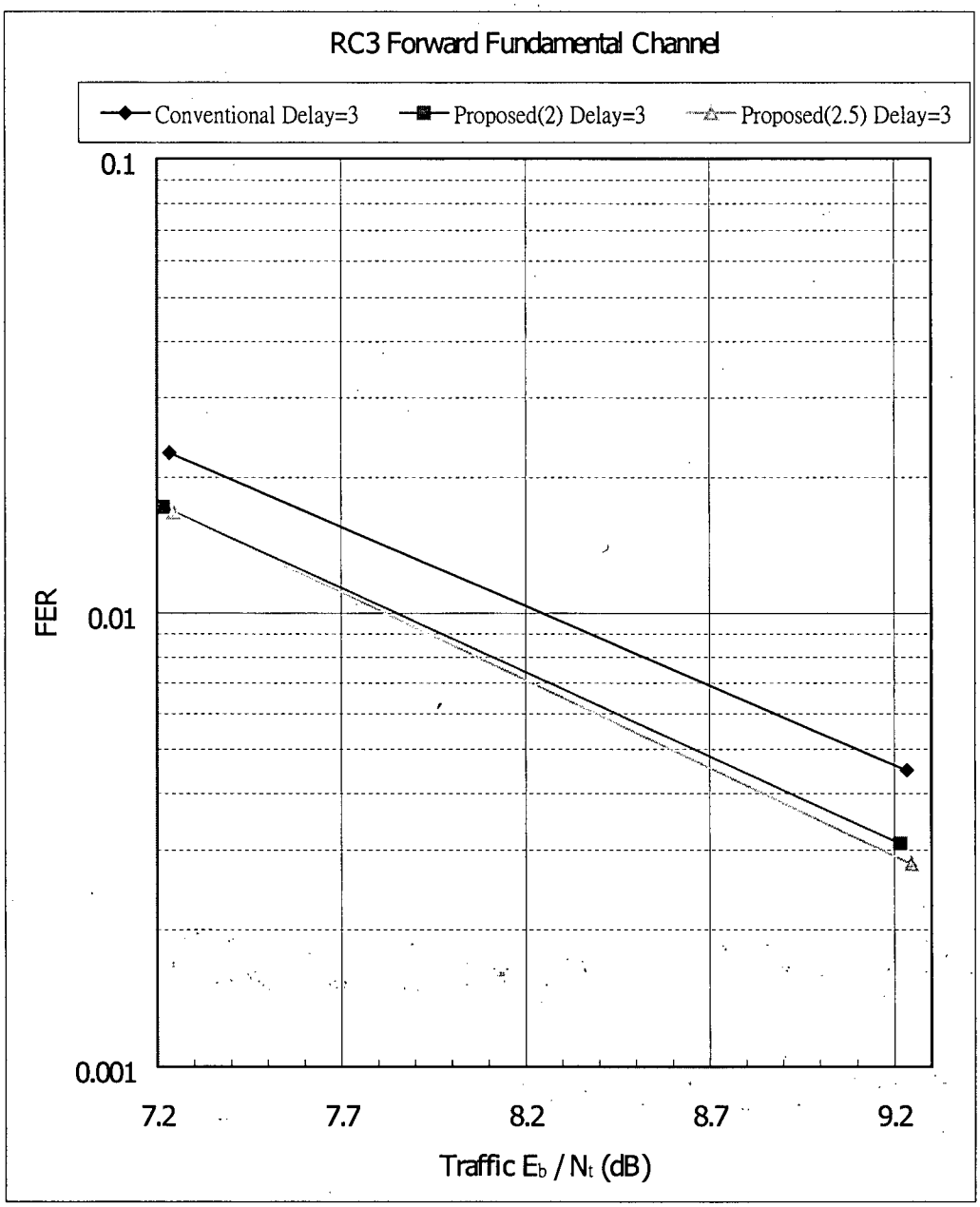
Figure 38 Effects of PCG Delays on FER (1 path 30 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±14.5%	±34.7%
Proposed(1) Delay=2	±16.4%	±39.8%
Proposed(1.5) Delay=2	±16.2%	±41.5%

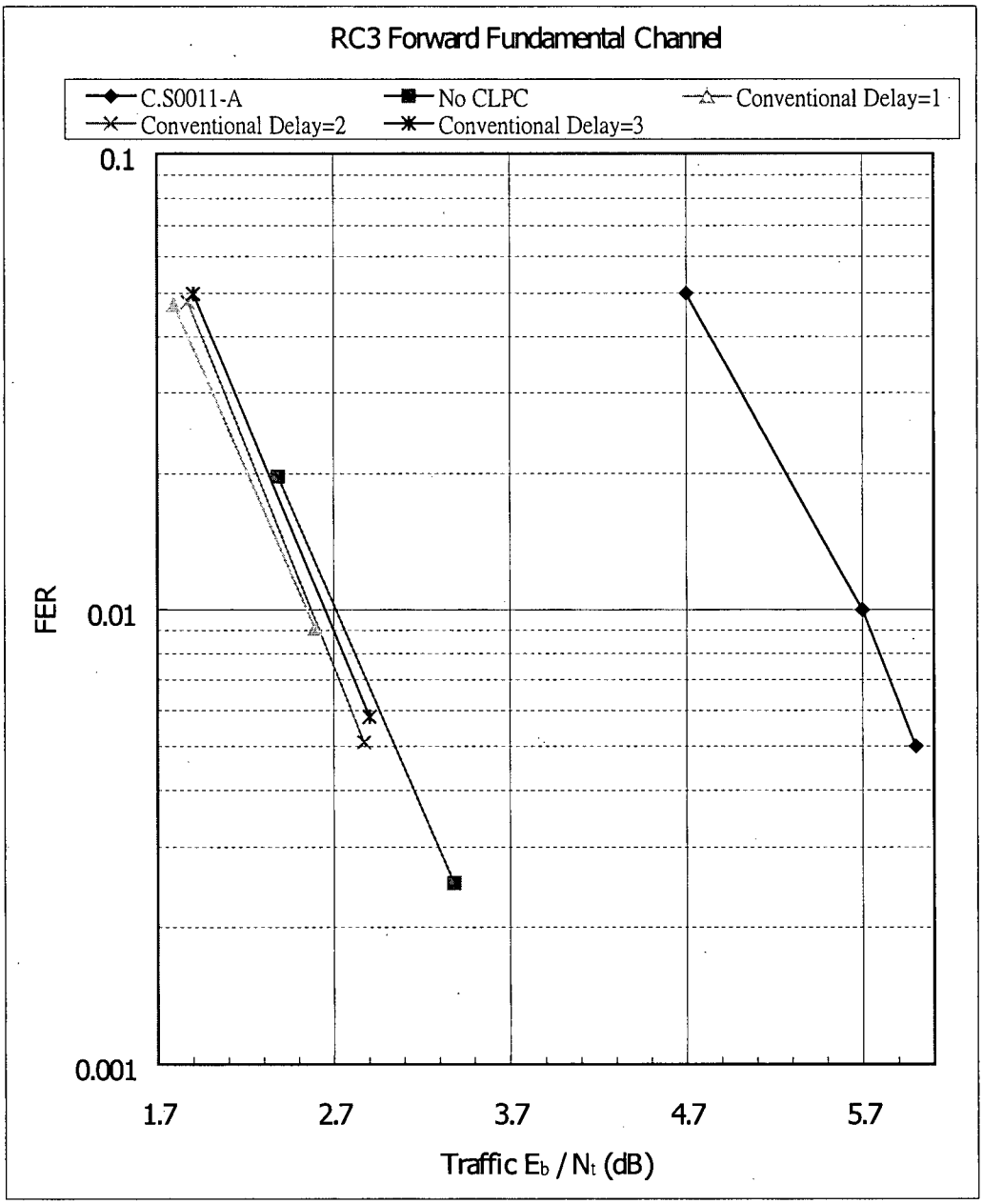
Figure 39 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 30 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±13.2%	±30.4%
Proposed(2) Delay=3	±15.2%	±37%
Proposed(2.5) Delay=3	±15.5%	±39%

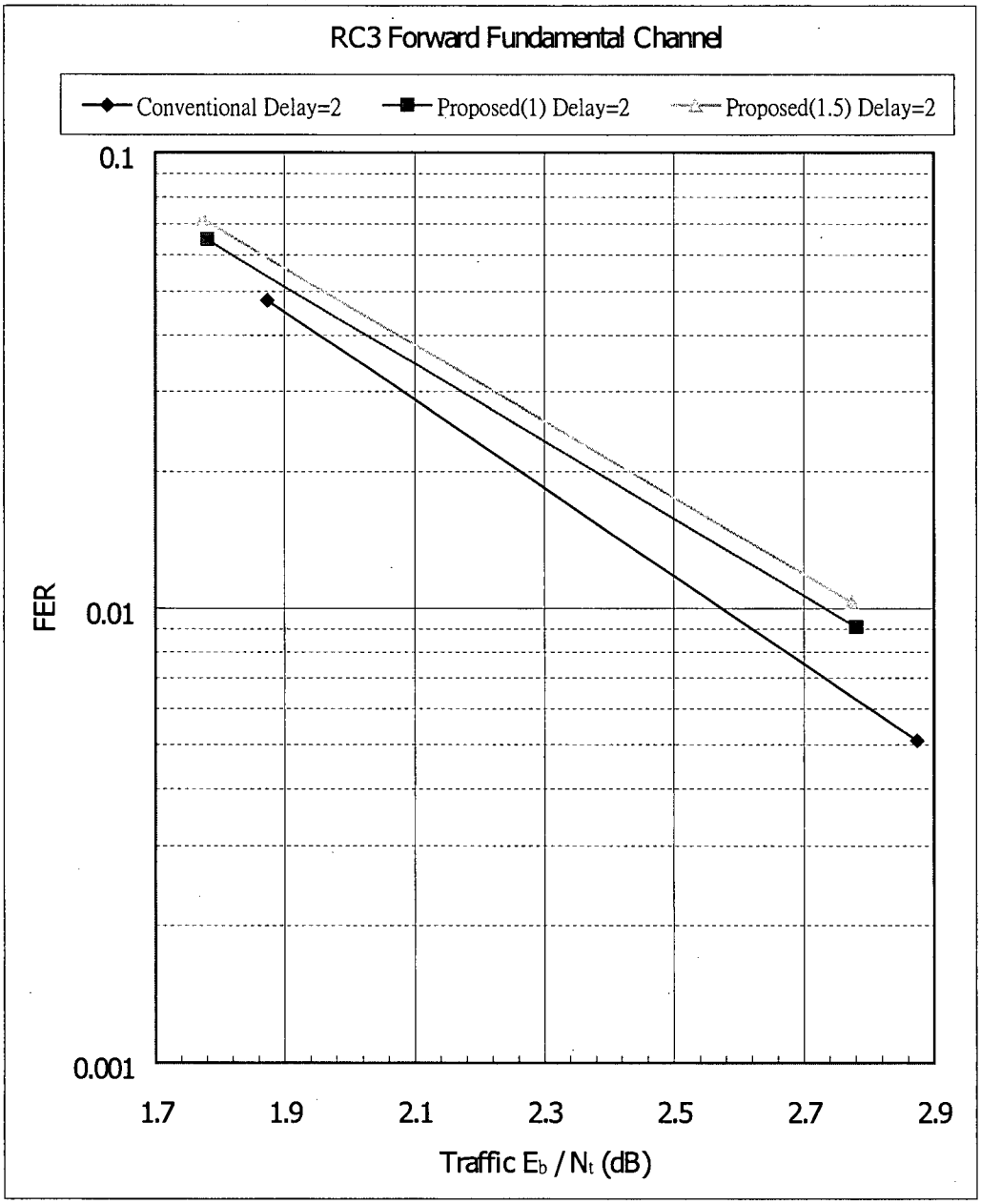
Figure 40 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 30 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±14.2%	±41.5%
Conventional Delay=1	±9.1%	±21.1%
Conventional Delay=2	±9.1%	±28.5%
Conventional Delay=3	±8.9%	±26.7%

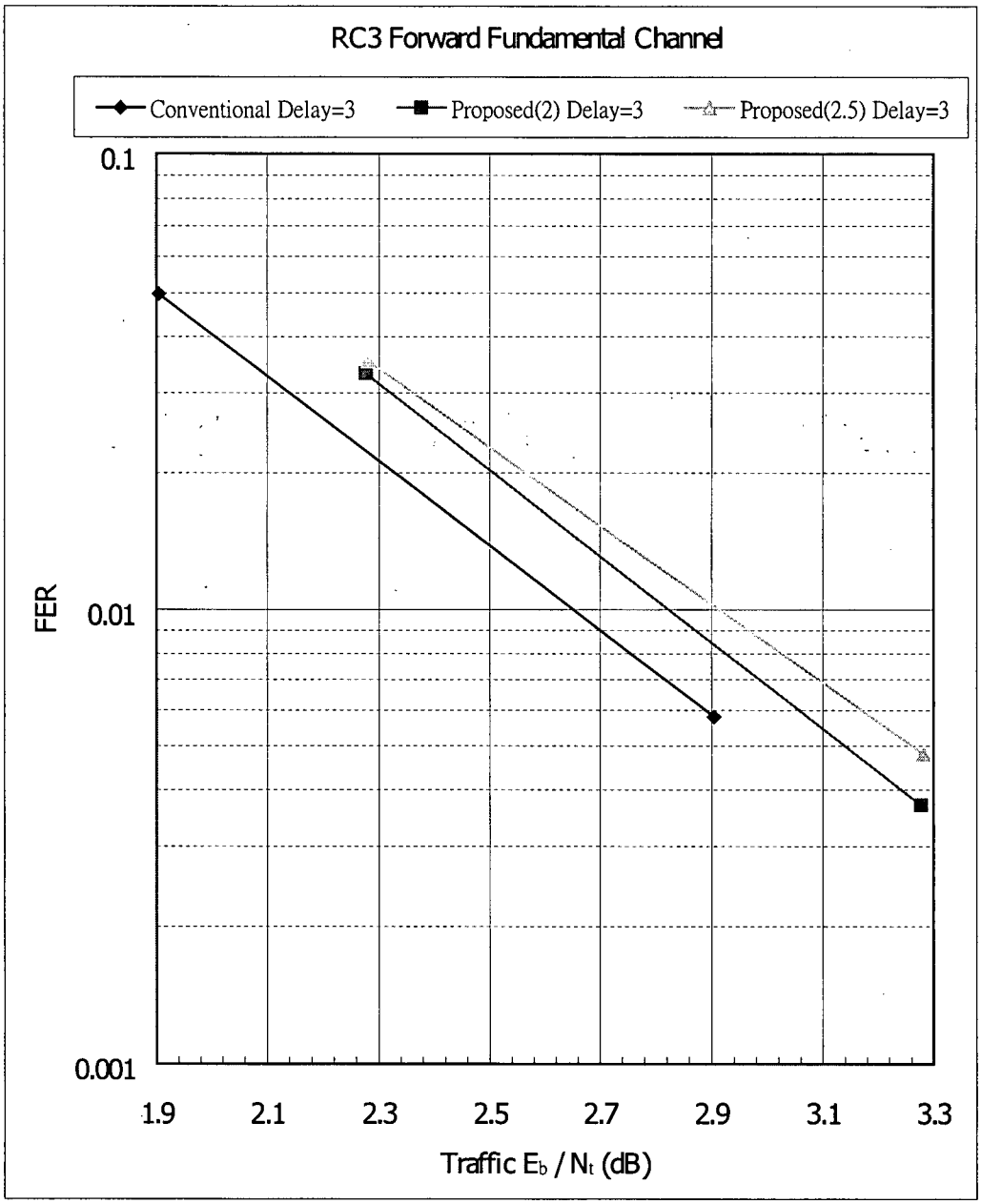
Figure 41 Effects of PCG Delays on FER (3 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±9.1%	±28.5%
Proposed(1) Delay=2	±7.8%	±21.1%
Proposed(1.5) Delay=2	±7.4%	±19.5%

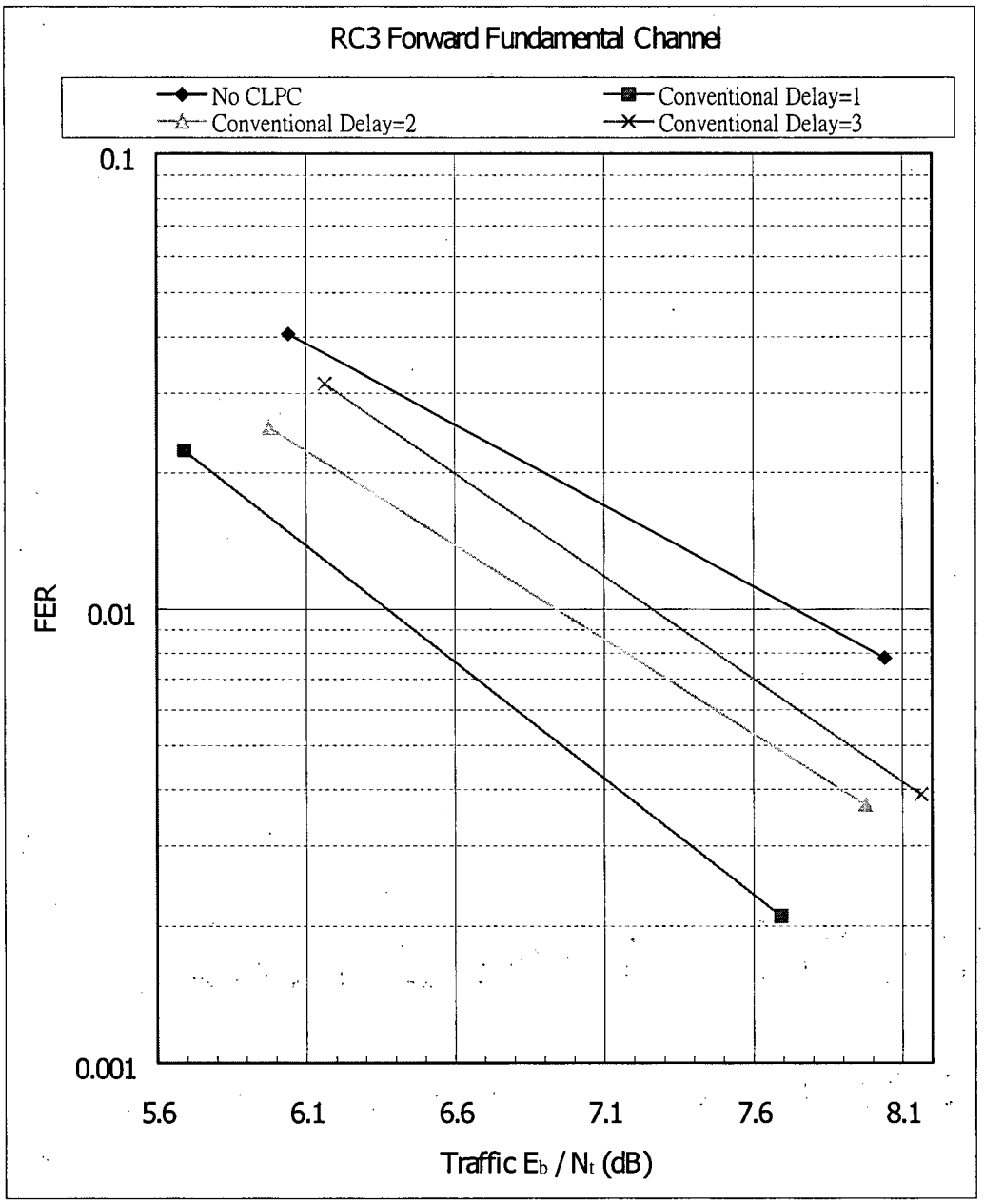
Figure 42 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (3 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±8.9%	±26.7%
Proposed(2) Delay=3	±10.9%	±33.7%
Proposed(2.5) Delay=3	±10.6%	±29.4%

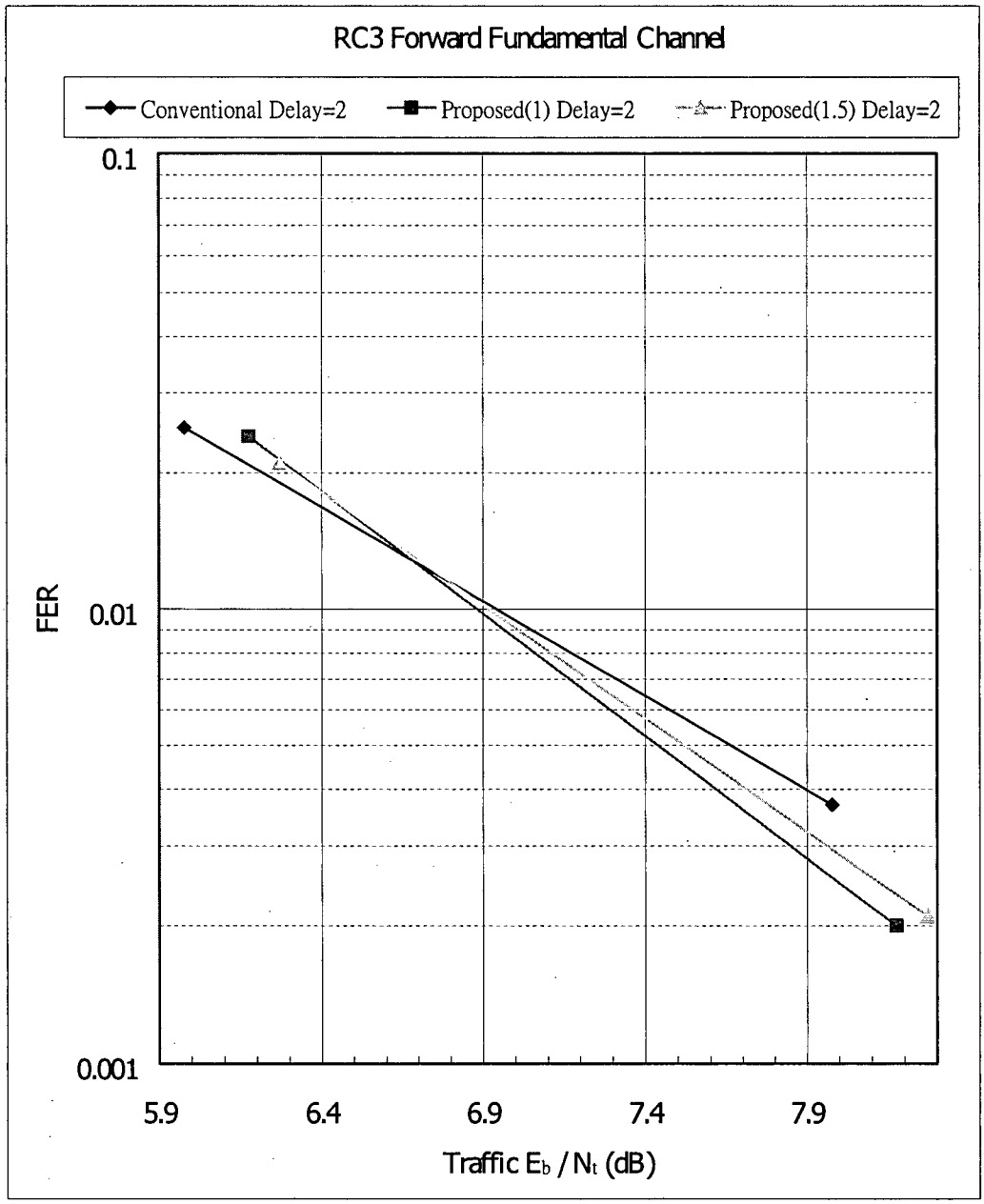
Figure 43 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (3 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±9.9%	±22.9%
Conventional Delay=1	±13.3%	±45.5%
Conventional Delay=2	±12.6%	±33.7%
Conventional Delay=3	±11.2%	±32.8%

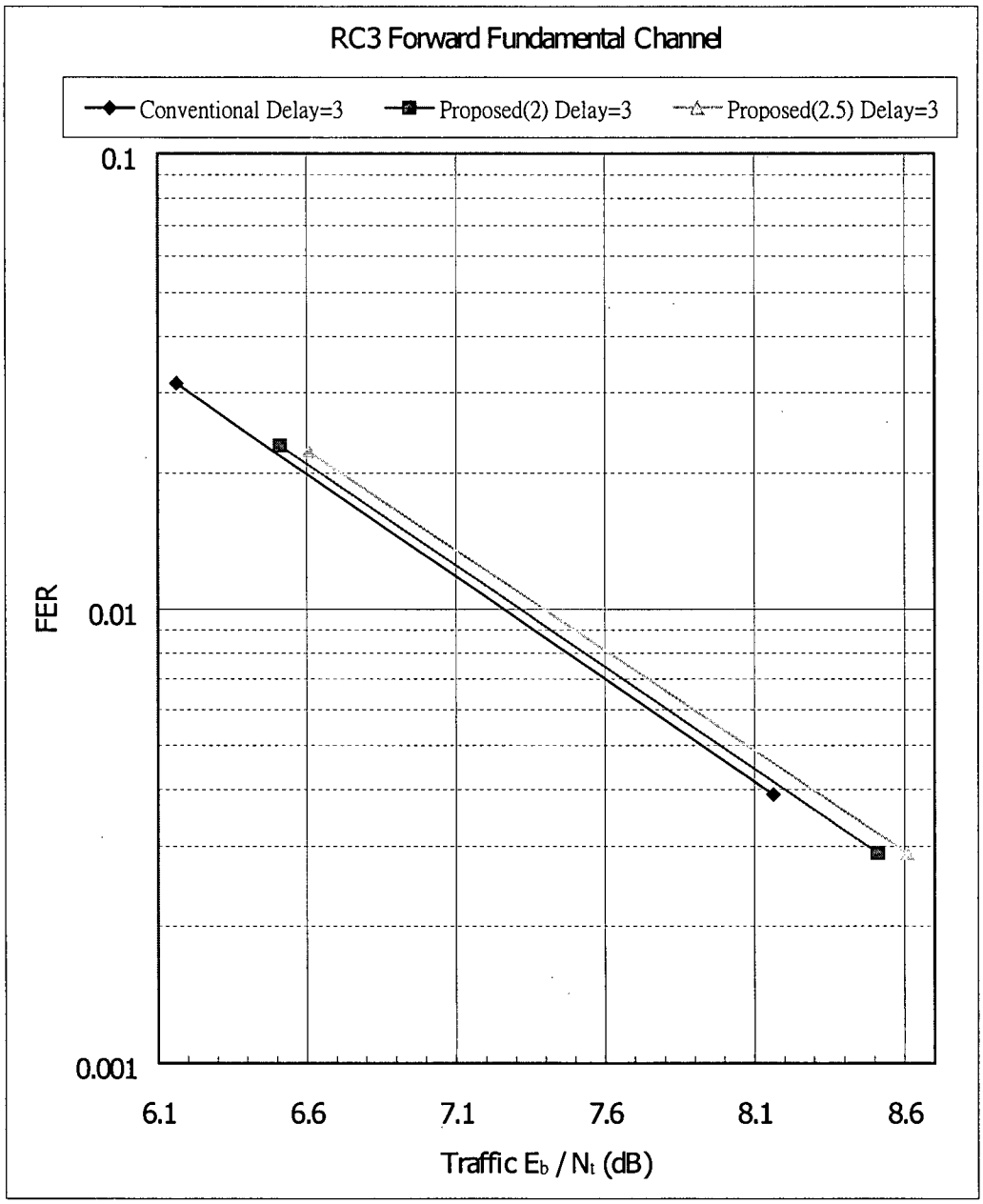
Figure 44 Effects of PCG Delays on FER (1 path 50 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±12.6%	±33.7%
Proposed(1) Delay=2	±12.8%	±46.7%
Proposed(1.5) Delay=2	±13.7%	±45.5%

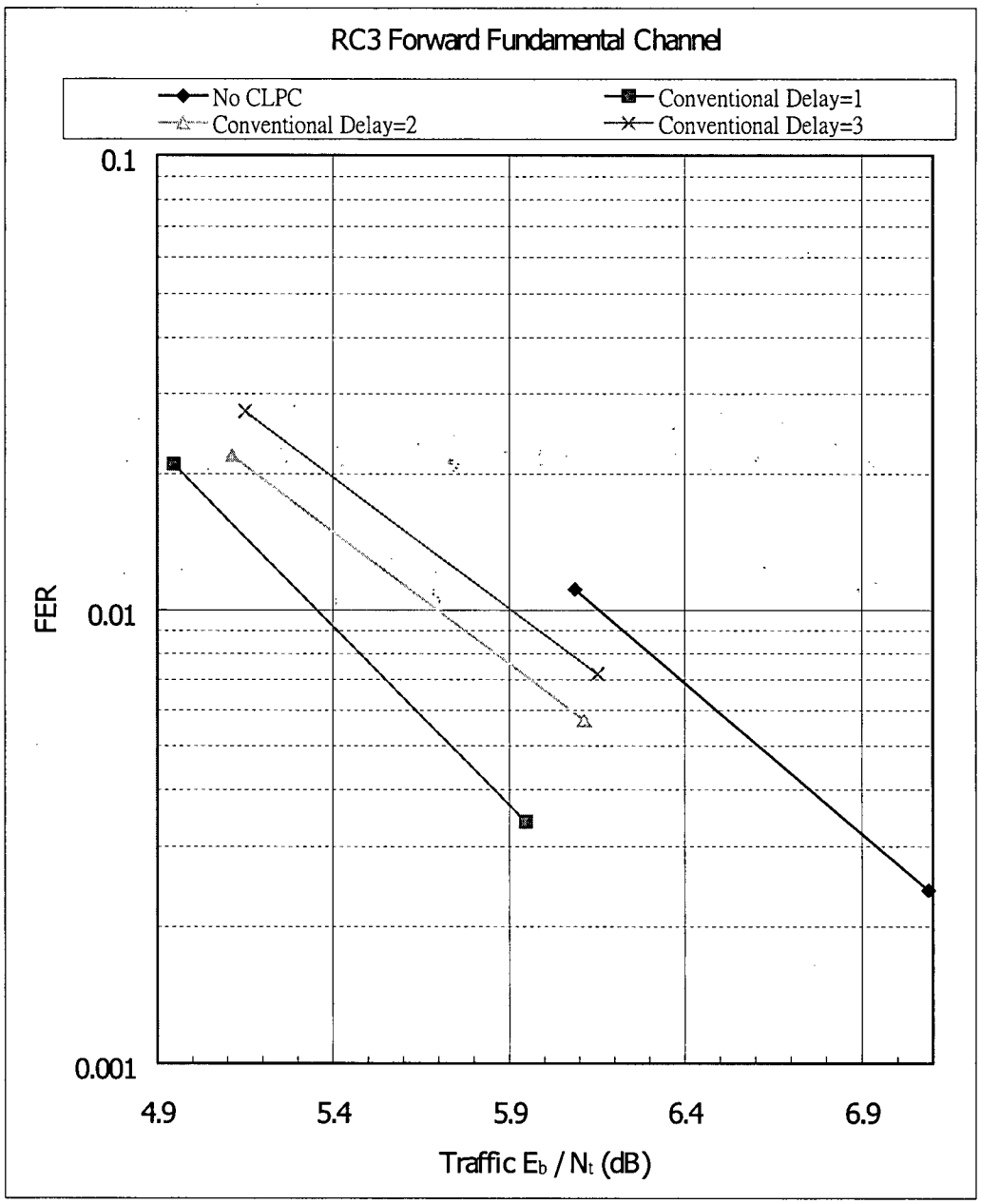
Figure 45 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 50 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±11.2%	±32.8%
Proposed(2) Delay=3	±13.2%	±38.3%
Proposed(2.5) Delay=3	±13.4%	±38.3%

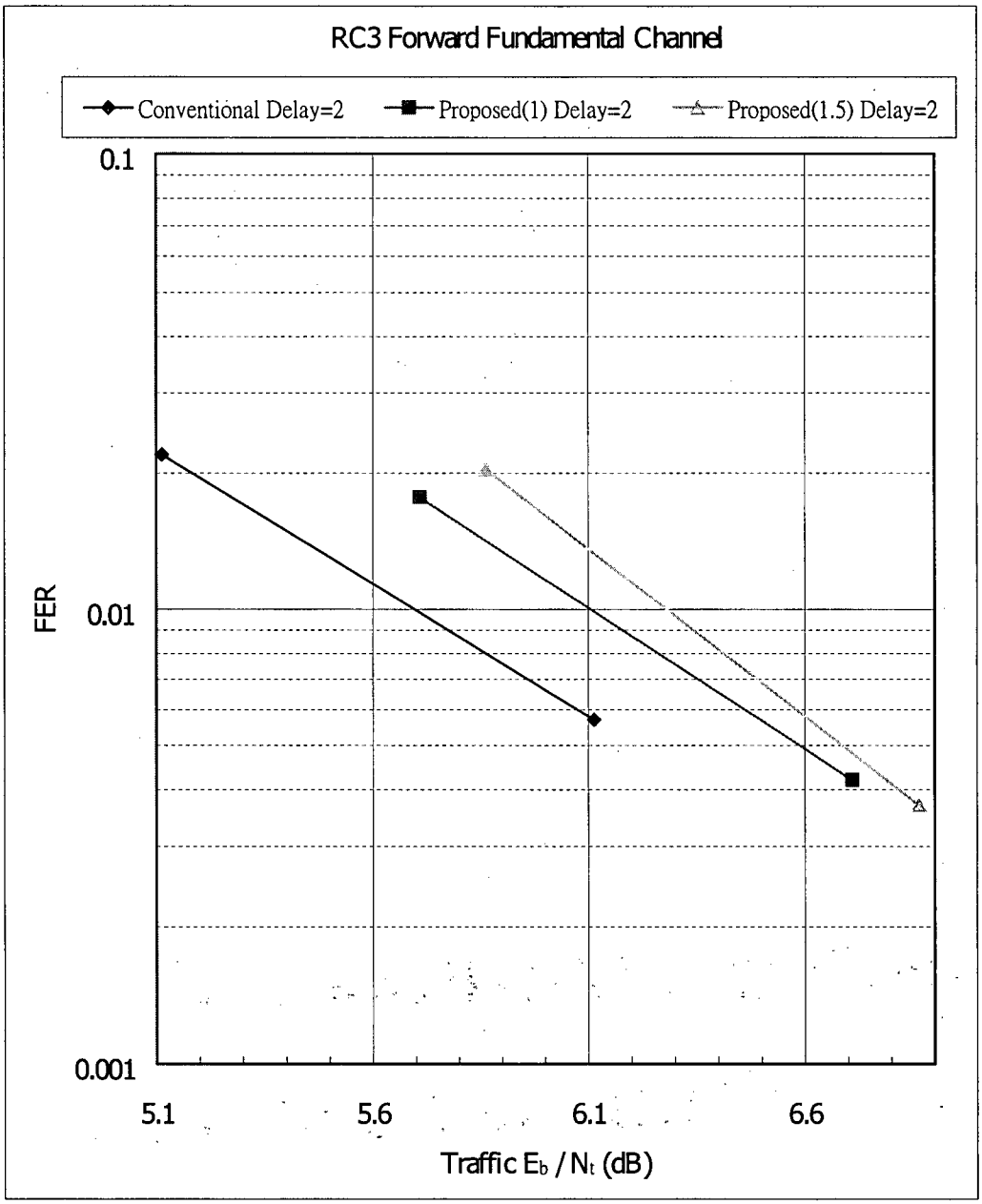
Figure 46 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 50 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±19.1%	±42.4%
Conventional Delay=1	±13.8%	±35.2%
Conventional Delay=2	±13.5%	±26.9%
Conventional Delay=3	±12%	±23.8%

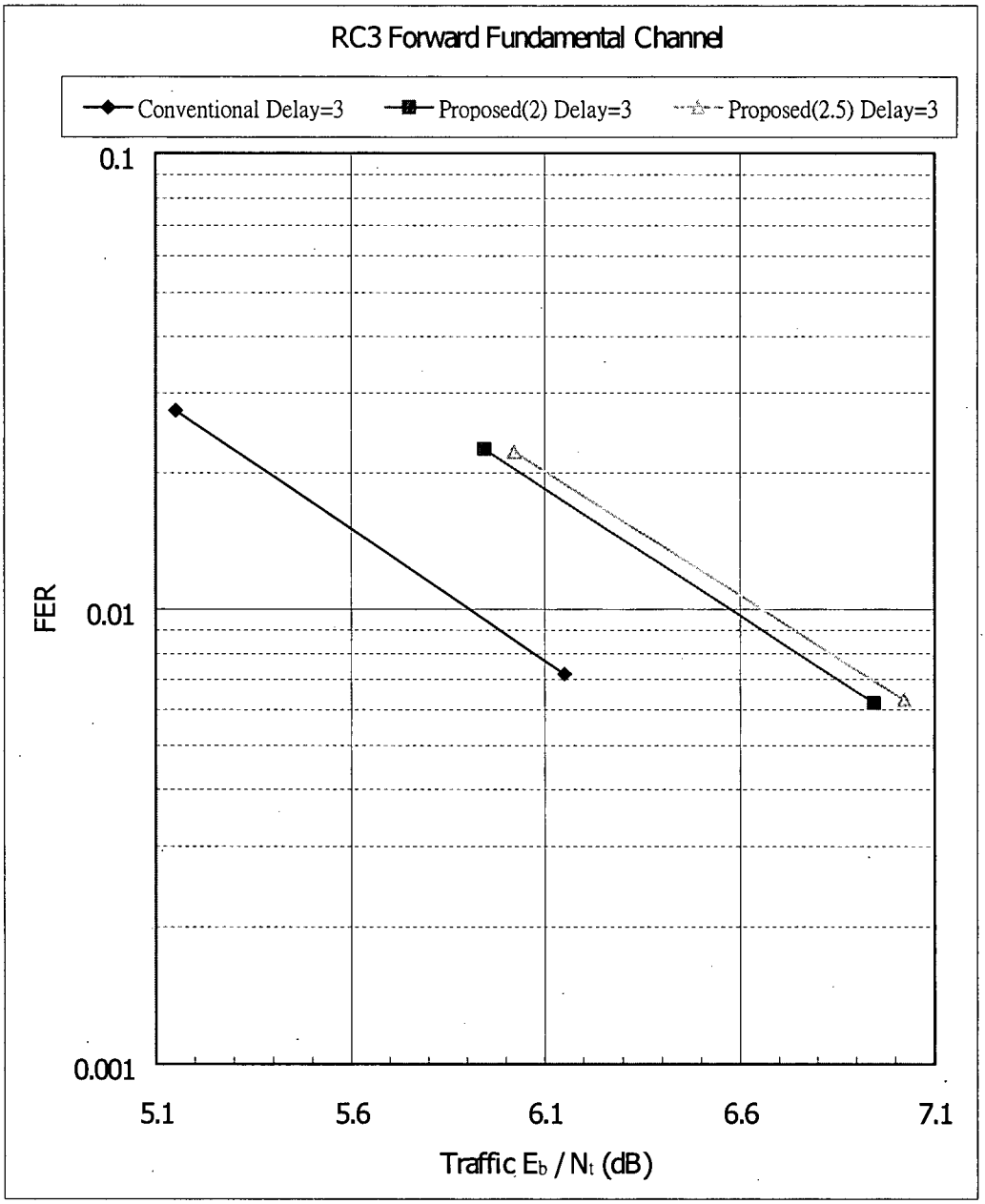
Figure 47 Effects of PCG Delays on FER (1 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±13.5%	±26.9%
Proposed(1) Delay=2	±15%	±31.5%
Proposed(1.5) Delay=2	±14%	±33.7%

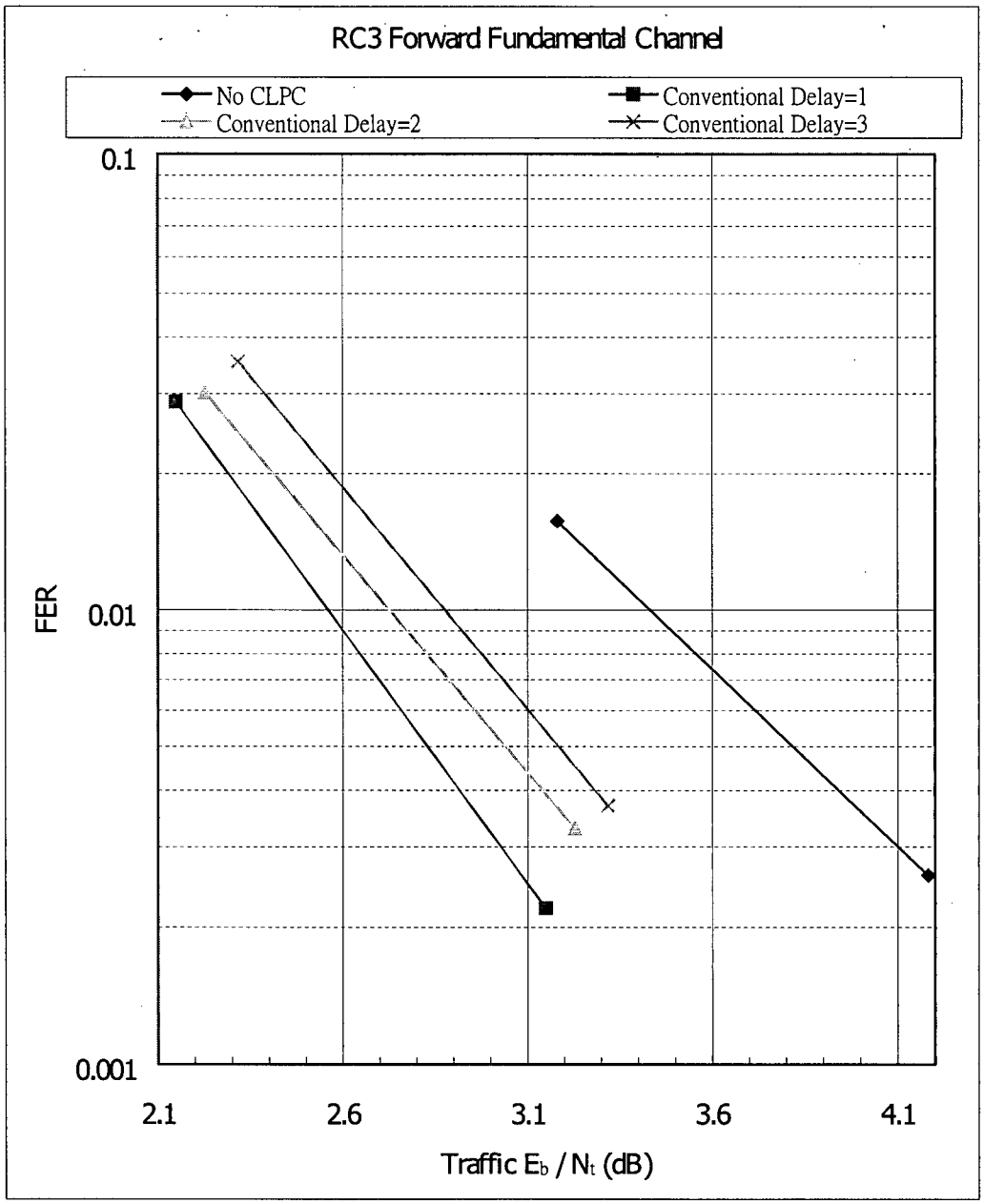
Figure 48 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±12%	±23.8%
Proposed(2) Delay=3	±13.3%	±25.8%
Proposed(2.5) Delay=3	±13.4%	±25.6%

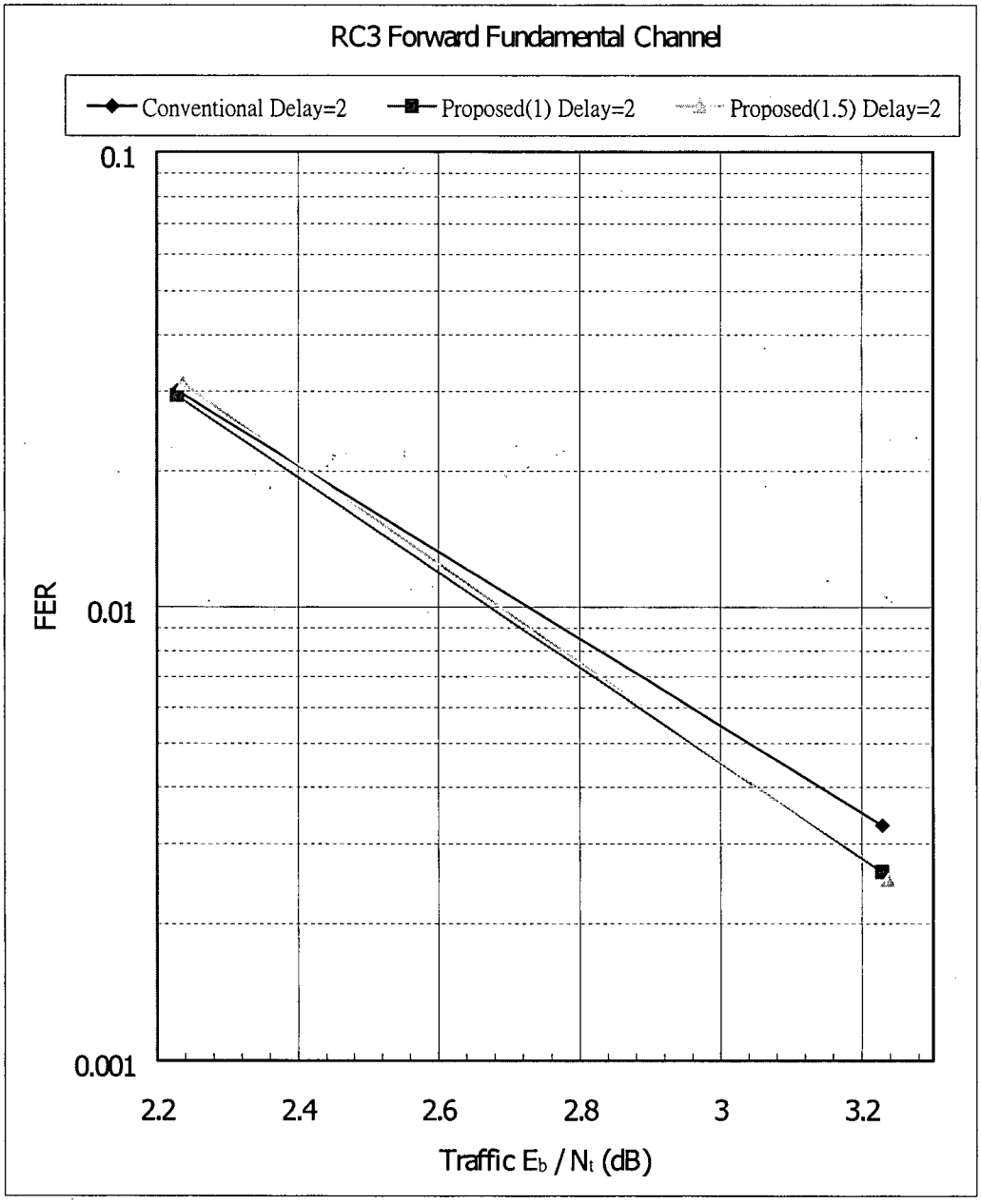
Figure 49 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 100 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±16%	±40.6%
Conventional Delay=1	±11.7%	±44.4%
Conventional Delay=2	±11.5%	±35.8%
Conventional Delay=3	±10.6%	±33.7%

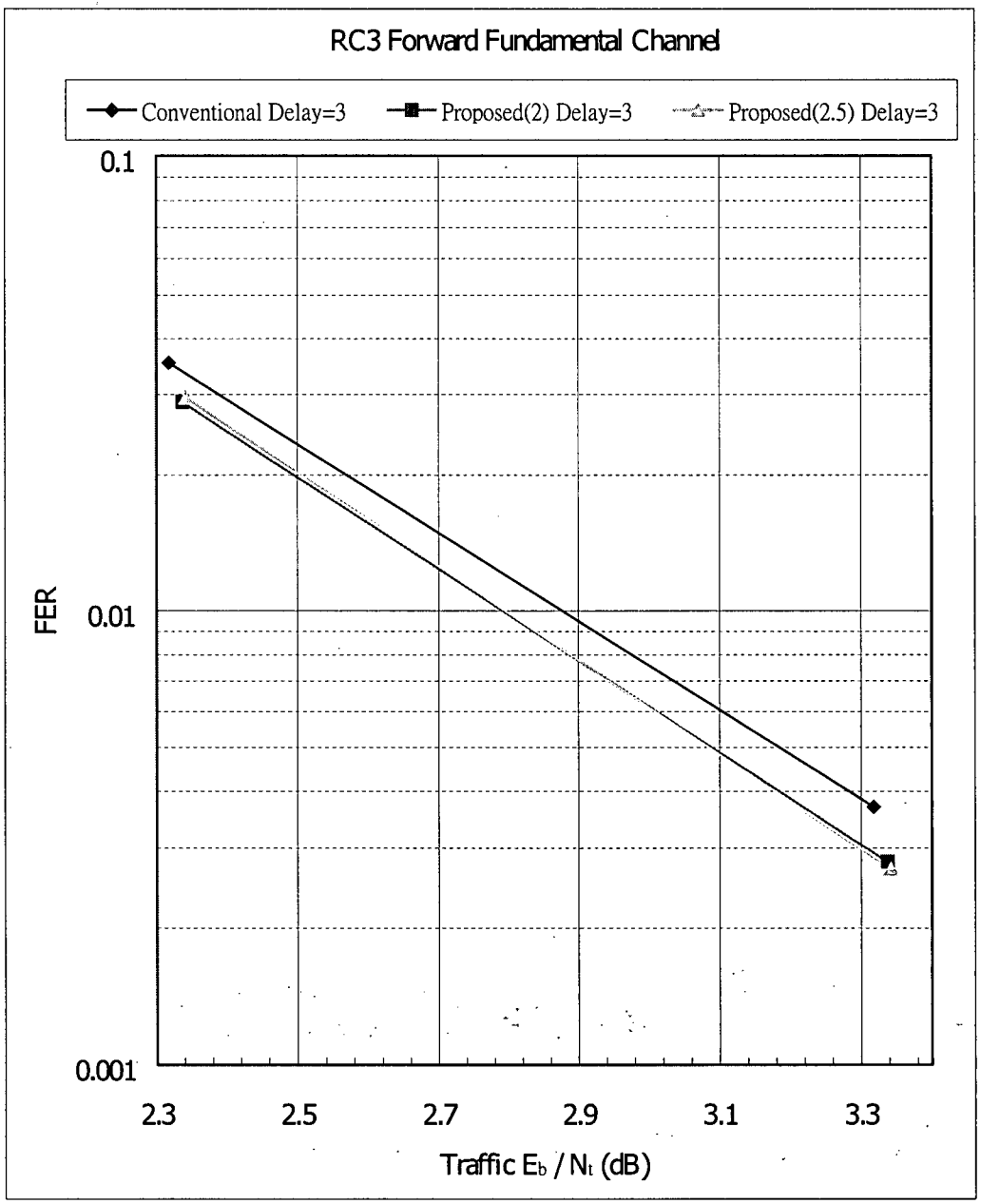
Figure 50 Effects of PCG Delays on FER (3 path 30 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±11.5%	±35.8%
Proposed(1) Delay=2	±11.6%	±40.6%
Proposed(1.5) Delay=2	±11.3%	±41.5%

Figure 51 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (3 path 30 km/hr Rayleigh Fading at 1.93 GHz)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±10.6%	±33.7%
Proposed(2) Delay=3	±11.7%	±39%
Proposed(2.5) Delay=3	±11.6%	±39.8%

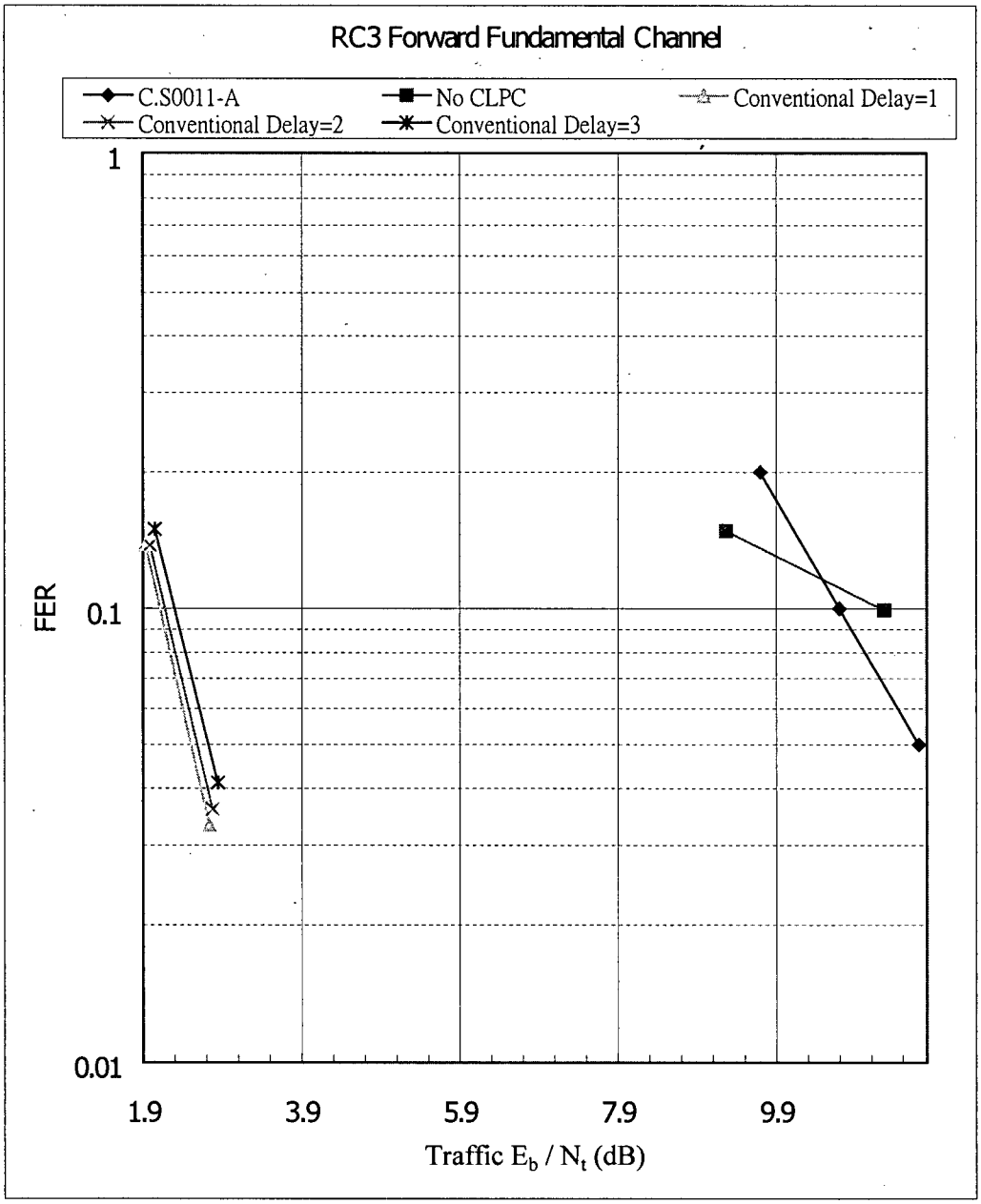
Figure 52 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (3 path 30 km/hr Rayleigh Fading at 1.93 GHz)

6.3 Numerical Results for 800 MHz Band with 5% PCB Error Rate

The PCBs in IS-2000 are not protected by coding so that a PCB can be used immediately after it is received and no decoding is required. However, this means that the PCBs are unprotected and subject to higher error rate. Since the MS does not know whether the PCB transmitted is correctly received by the BS or not, an increase in PCB error probability degrades the performance of the proposed CLPC algorithm. In this section, we study the effect of PCB errors on the FER and the performance of the proposed CLPC algorithm using the standard channel configurations in [22] (1 path 3 km/hr, 1 path 30 km/hr and 3 path 100 km/hr). The additional channel configurations (1 path 50 km/hr, 1 path 100 km/hr and 3 path 30 km/hr) are not used because the standard channel configurations are sufficient to show the effect of PCB errors on the proposed CLPC algorithm. The PCB error rate is set to 5%. Table 10 summarizes the 800 MHz band with 5% PCB error rate simulation figures.

Table 10 Summary of 800 MHz Band with 5% PCB Error Rate Simulation Figures

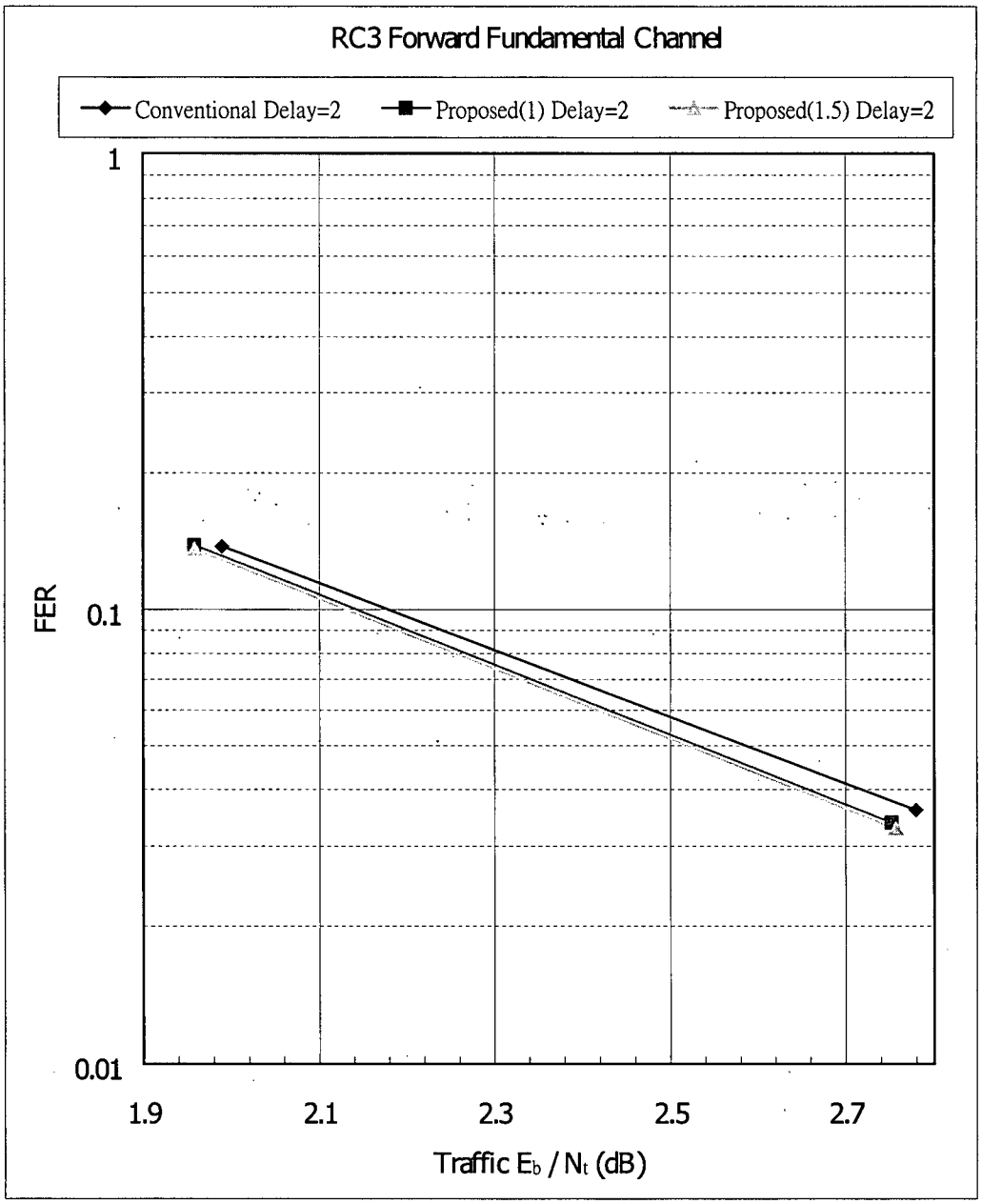
Channel Configuration	Description	Figure Number
1 path 3 km/hr	Effects of PCG delays on FER	Figure 53
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 54
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 55
1 path 30 km/hr	Effects of PCG delays on FER	Figure 56
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 57
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 58
3 path 100 km/hr	Effects of PCG delays on FER	Figure 59
	Comparison of conventional and proposed algorithms when $n_t = 2$	Figure 60
	Comparison of conventional and proposed algorithms when $n_t = 3$	Figure 61



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±7.3%	±8.9%
Conventional Delay=1	±7.5%	±15.5%
Conventional Delay=2	±7.5%	±14.9%
Conventional Delay=3	±7.2%	±13.9%

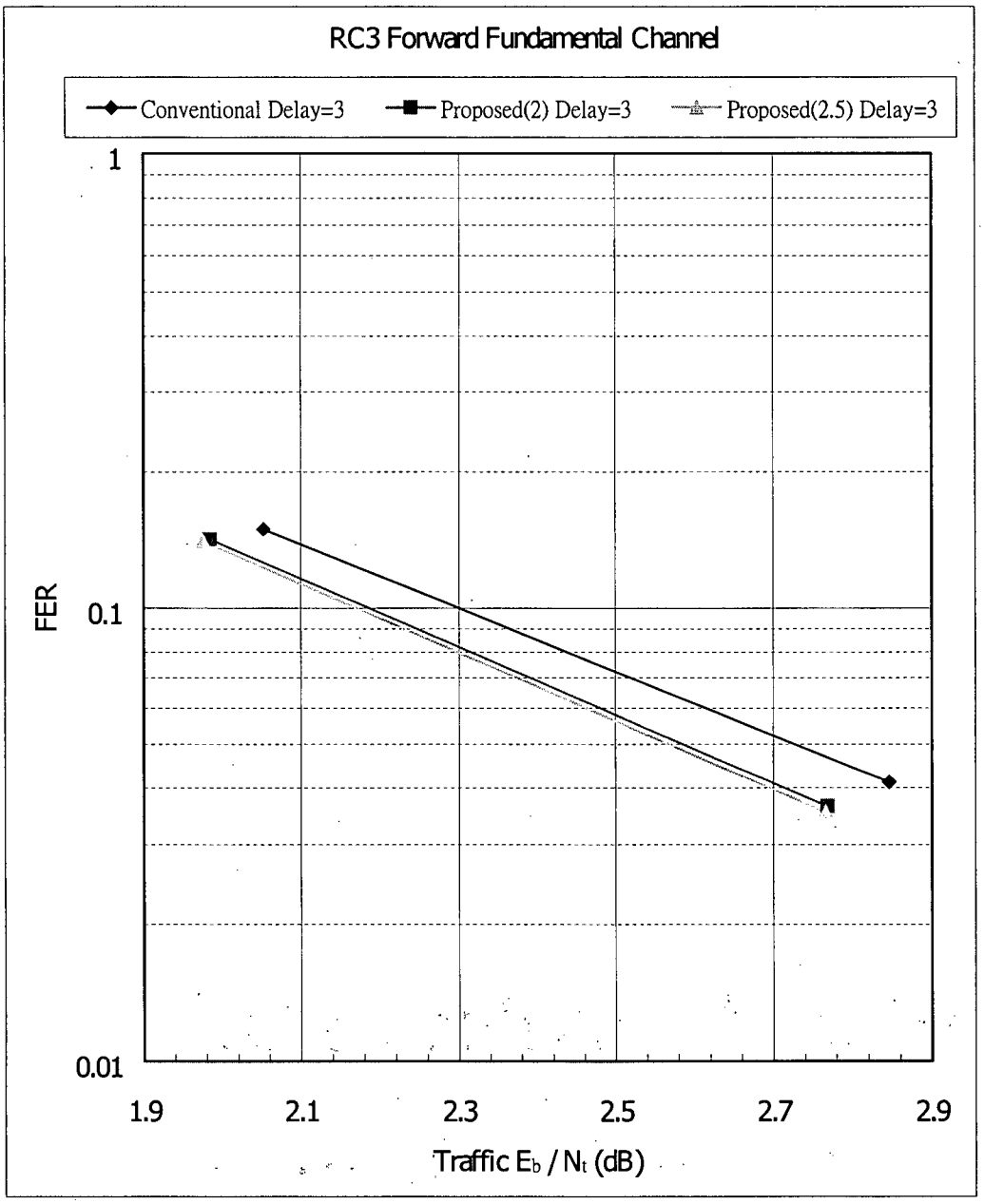
Figure 53 Effects of PCG Delays on FER (1 path 3 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±7.5%	±14.9%
Proposed(1) Delay=2	±7.5%	±15.4%
Proposed(1.5) Delay=2	±7.6%	±15.6%

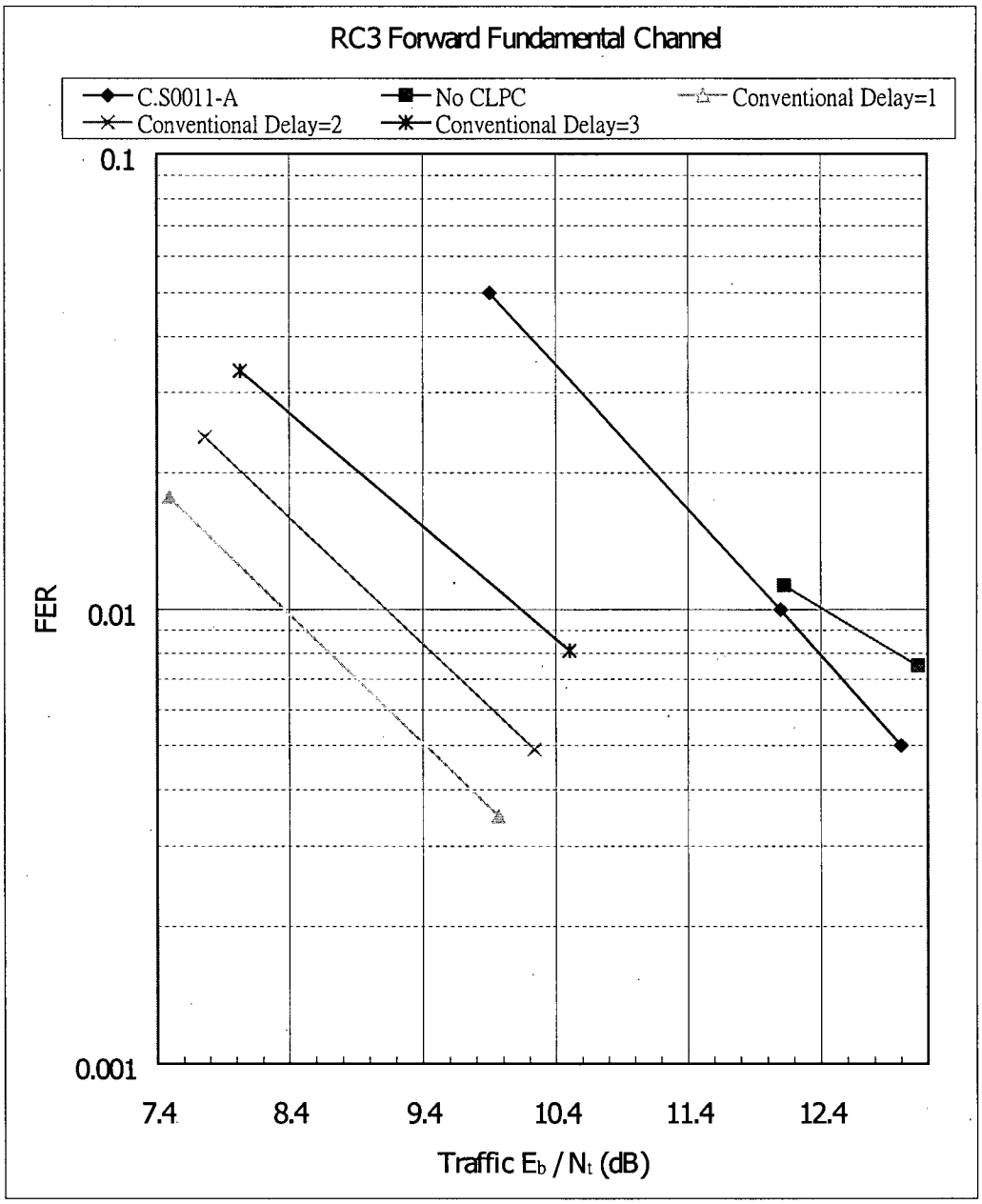
Figure 54 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 3 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±7.2%	±13.9%
Proposed(2) Delay=3	±7.4%	±14.8%
Proposed(2.5) Delay=3	±7.5%	±15%

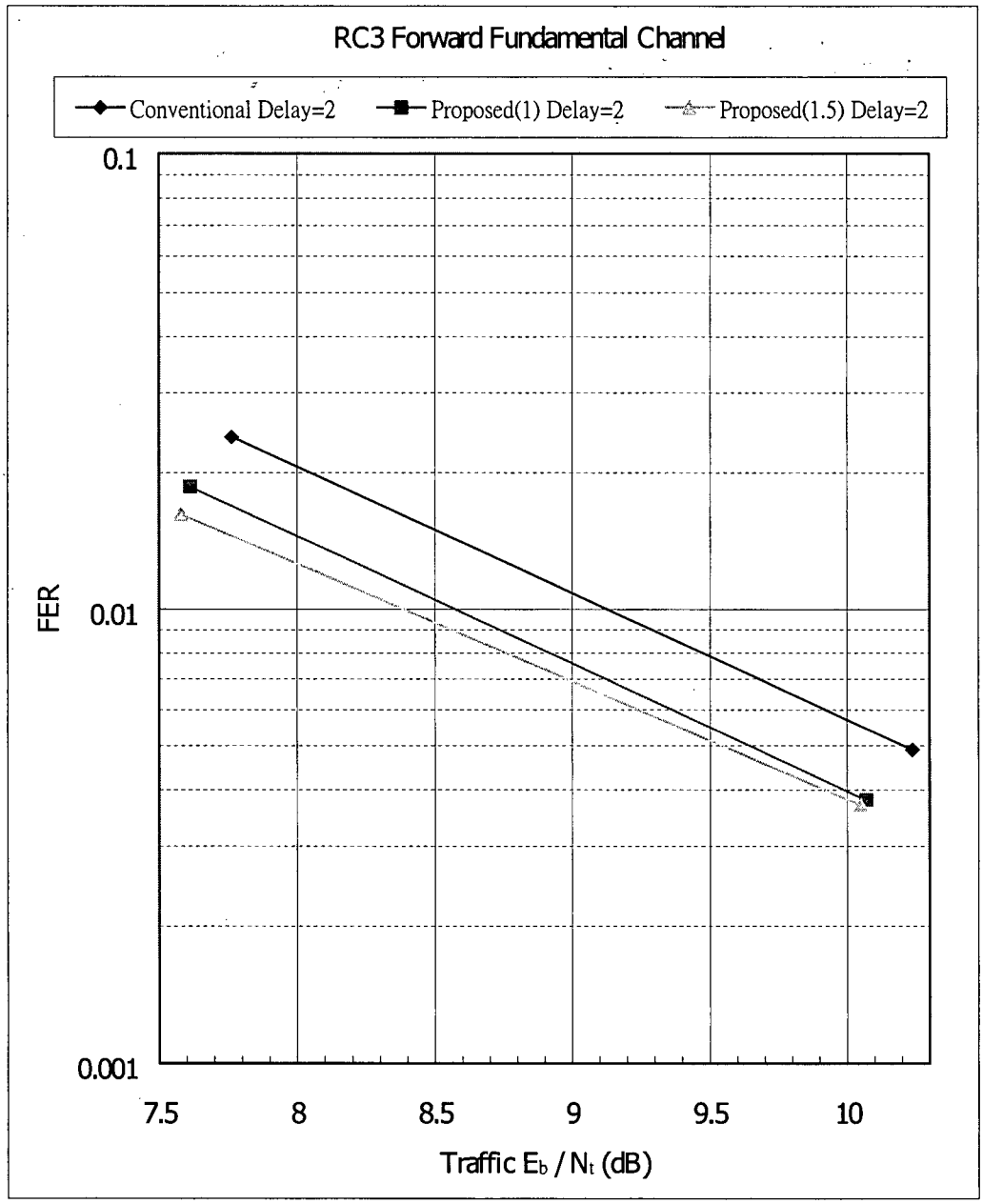
Figure 55 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 3 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±18.9%	±23.3%
Conventional Delay=1	±15%	±34.7%
Conventional Delay=2	±12.9%	±29.1%
Conventional Delay=3	±10.9%	±22.4%

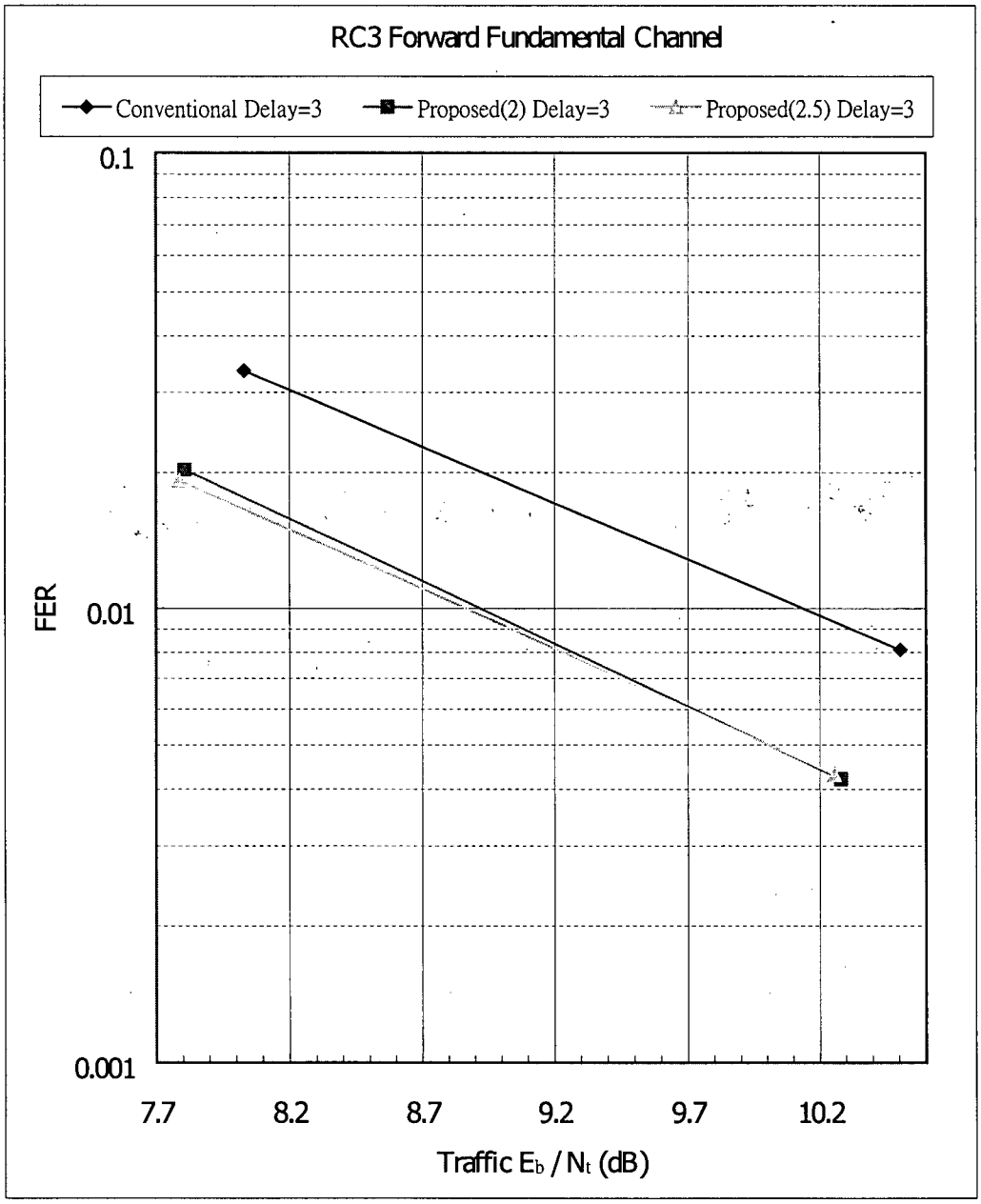
Figure 56 Effects of PCG Delays on FER (1 path 30 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±12.9%	±29.1%
Proposed(1) Delay=2	±14.7%	±33.2%
Proposed(1.5) Delay=2	±15.7%	±33.7%

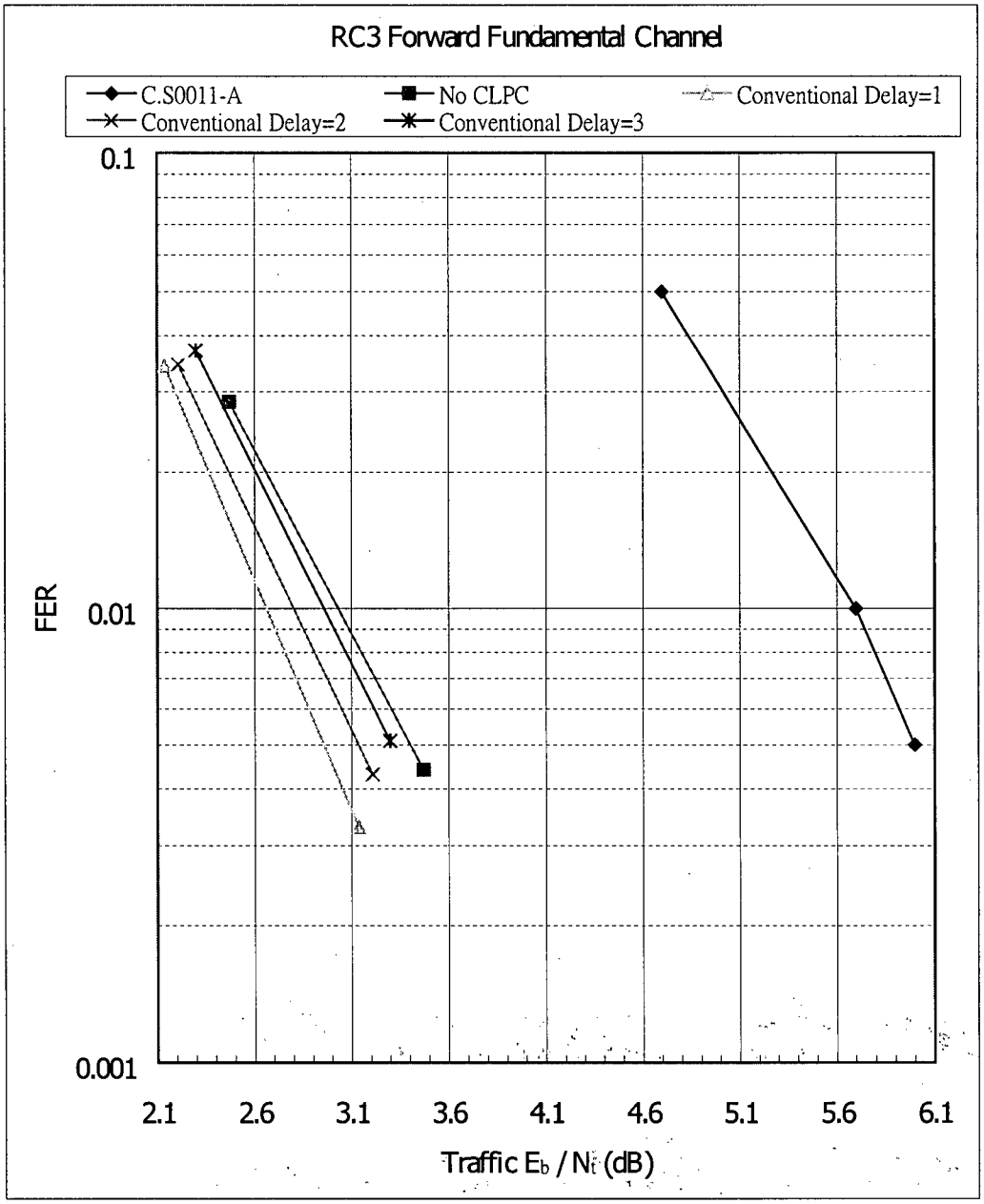
Figure 57 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (1 path 30 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±10.9%	±22.4%
Proposed(2) Delay=3	±14%	±31.5%
Proposed(2.5) Delay=3	±14.4%	±31.2%

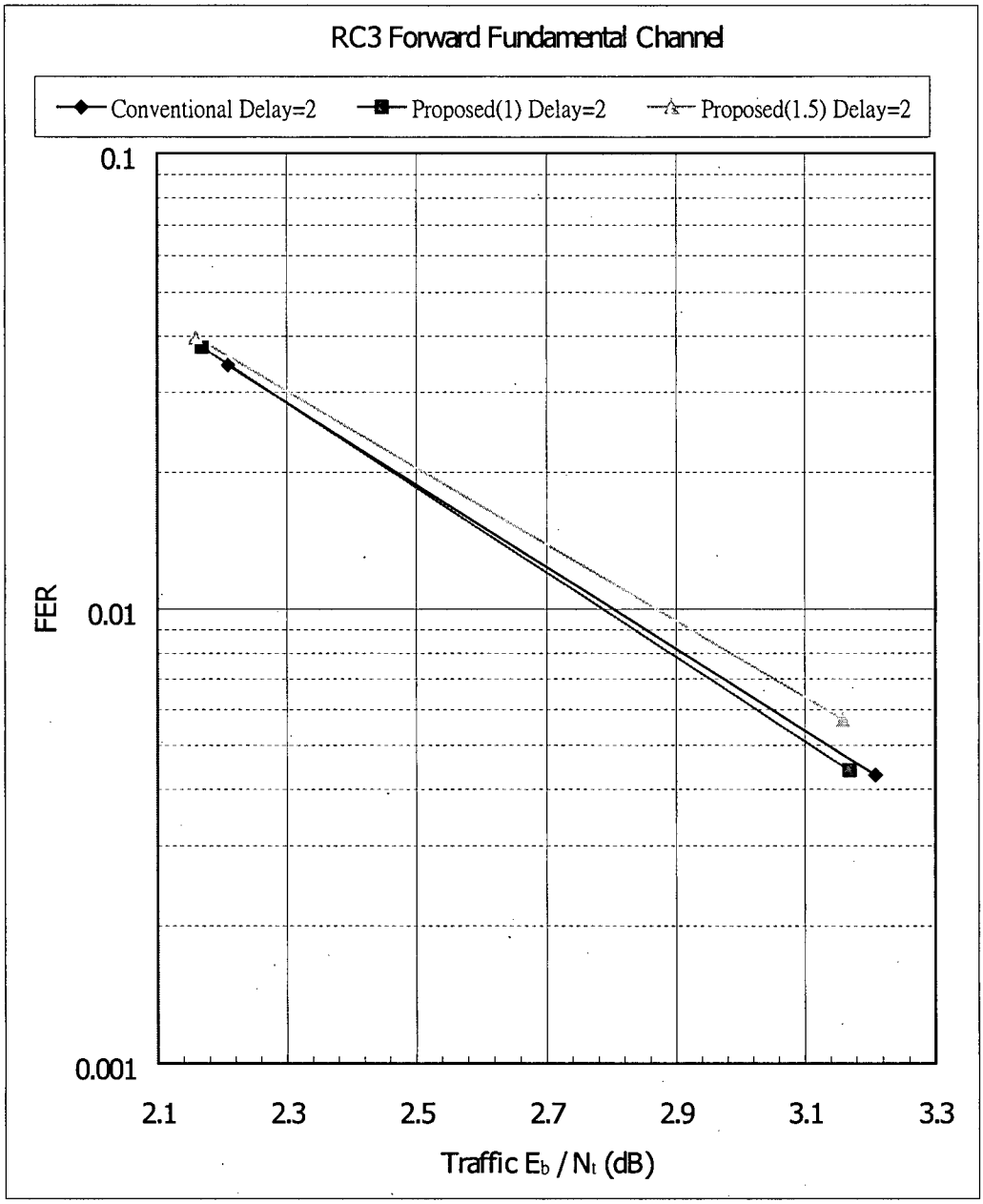
Figure 58 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (1 path 30 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
No CLPC	±11.8%	±30.8%
Conventional Delay=1	±10.7%	±35.8%
Conventional Delay=2	±10.7%	±31.2%
Conventional Delay=3	±10.3%	±28.5%

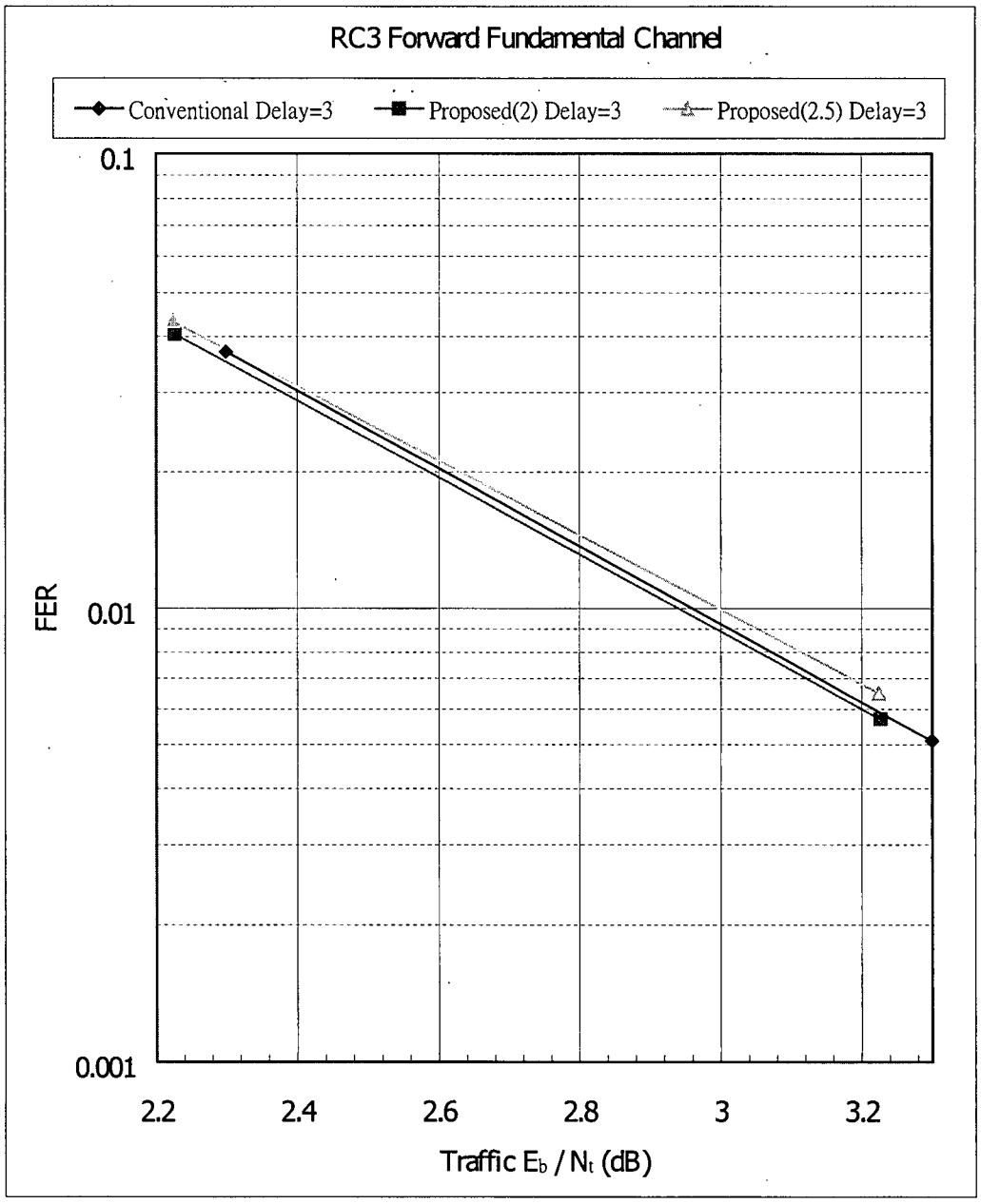
Figure 59 Effects of PCG Delays on FER (3 path 100 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=2	±10.7%	±31.2%
Proposed(1) Delay=2	±10.2%	±30.8%
Proposed(1.5) Delay=2	±10%	±26.9%

Figure 60 Comparison of Conventional and Proposed Algorithms when Delay=2 PCG Slots (3 path 100 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)



Statistical Accuracy:

	Higher FER Point	Lower FER Point
Conventional Delay=3	±10.3%	±28.5%
Proposed(2) Delay=3	±9.9%	±26.9%
Proposed(2.5) Delay=3	±9.5%	±25.1%

Figure 61 Comparison of Conventional and Proposed Algorithms when Delay=3 PCG Slots (3 path 100 km/hr Rayleigh Fading at 870 MHz with 5 % PCB Error Rate)

6.4 Discussion of Simulation Results

As mentioned in Chapter 4, we use the mean traffic E_b/N_t required to achieve the target FER for performance evaluation. The relative performance gain or degradation is the difference between the two traffic E_b/N_t values obtained. The lower the required mean traffic E_b/N_t to achieve the target FER, the better is the performance of the CLPC algorithm. We first investigate the impact of loop delays on the FER performance of the conventional CLPC algorithm. Table 11 and Table 12 show the change in E_b/N_t required to achieve the target FER. The required E_b/N_t when there is no CLPC is shown for comparison purposes.

Table 11 Impact of CLPC and Loop Delays on E_b/N_t Required by the Conventional CLPC Algorithm to Achieve the Target FER at 870 MHz

Channel Configuration	E_b/N_t (No CLPC)	E_b/N_t (Delay=1)	E_b/N_t (Delay=2) – E_b/N_t (Delay=1)	E_b/N_t (Delay=3) – E_b/N_t (Delay=1)
1 path 3 km/hr	11.22	2.07	+0.046	+0.17
1 path 30 km/hr	12.42	7.78	+1.00	+2.21
1 path 50 km/hr	10.38	7.65	+0.91	+1.72
1 path 100 km/hr	8.07	6.56	+0.58	+1.10
3 path 30 km/hr	4.27	2.66	+0.16	+0.57
3 path 100 km/hr	3.03	2.59	+0.12	+0.25

Table 12 Impact of CLPC and Loop Delays on E_b/N_t Required by the Conventional CLPC Algorithm to Achieve the Target FER at 1.93 GHz

Channel Configuration	E_b/N_t (No CLPC)	E_b/N_t (Delay=1)	E_b/N_t (Delay=2) – E_b/N_t (Delay=1)	E_b/N_t (Delay=3) – E_b/N_t (Delay=1)
1 path 3 km/hr	10.1	2.62	+0.23	+0.60
1 path 30 km/hr	9.36	7.01	+0.67	+1.24
1 path 50 km/hr	7.74	6.37	+0.57	+0.89
1 path 100 km/hr	6.16	5.35	+0.34	+0.55
3 path 30 km/hr	3.43	2.56	+0.17	+0.32
3 path 100 km/hr	2.71	2.55	+0.024	+0.10

It can be seen that CLPC improves performance significantly at low Doppler frequencies and its performance decreases as Doppler frequency increases. This is because CLPC can keep up with the channel changes at lower Doppler frequencies. However, as the Doppler frequency increases, CLPC can hardly keep up with the channel changes.

As the loop delay increases, the conventional CLPC algorithm requires a higher E_b/N_t to achieve the target FER in all the channel configurations. However, it is found that at low Doppler frequencies (1 path 3 km/hr at 870 MHz), the FER degradations due to loop delays are relatively small. Again, this is because the conventional CLPC algorithm can keep up with the channel changes at lower Doppler frequencies even when there is a small loop delay. At moderate Doppler frequencies (1 path 30 km/hr and 1 path 50 km/hr at 870 MHz), the FER performance of the conventional CLPC algorithm is very sensitive to loop delays. This is because the conventional CLPC algorithm can cope with fading in this Doppler frequency range when the loop delay is 1 PCG slot. However, any further loop delays slow down the reaction of the CLPC algorithm to a fade. As a result, the FER performance is degraded by a significant amount. It can be seen that the delay sensitivity decreases as the Doppler frequency increases beyond some value (1 path 30 km/hr at 870 MHz and 1.93 GHz). At higher Doppler frequencies, the conventional CLPC algorithm is ineffective and interleaving is the main process that mitigates fading. Therefore, loop delay sensitivity decreases at high Doppler frequencies. The delay sensitivity is smaller when there are 3 multipaths. This is because the multipaths reduce the received signal power variance.

Next we study the relative performance of the proposed CLPC algorithm compared to the conventional CLPC algorithm. Table 13 and Table 14 summarize the

relative performance gain of the proposed CLPC algorithm in dB (a positive gain corresponds to an improvement and a negative gain corresponds to a degradation).

Table 13 Relative Performance Gain of Proposed CLPC Algorithm at 870 MHz

Channel Configuration	Delay (n_t)	Proposed(D) Performance Gain (dB) Compared to Conventional	Proposed(D+0.5) Performance Gain (dB) Compared to Conventional
1 path 3 km/hr	2 PCG Delay	0.044	0.054
	3 PCG Delay	0.16	0.17
1 path 30 km/hr	2 PCG Delay	0.85	0.97
	3 PCG Delay	1.7	1.8
1 path 50 km/hr	2 PCG Delay	0.56	0.63
	3 PCG Delay	0.93	0.92
1 path 100 km/hr	2 PCG Delay	0.14	0.13
	3 PCG Delay	0.26	0.16
3 path 30 km/hr	2 PCG Delay	0.12	0.13
	3 PCG Delay	0.41	0.43
3 path 100 km/hr	2 PCG Delay	0.043	-0.012
	3 PCG Delay	0.0043	-0.033

Table 14 Relative Performance Gain of Proposed CLPC Algorithm at 1.93 GHz

Channel Configuration	Delay (n_t)	Proposed(D) Performance Gain (dB) Compared to Conventional	Proposed(D+0.5) Performance Gain (dB) Compared to Conventional
1 path 3 km/hr	2 PCG Delay	0.19	0.24
	3 PCG Delay	0.50	0.54
1 path 30 km/hr	2 PCG Delay	0.31	0.30
	3 PCG Delay	0.40	0.43
1 path 50 km/hr	2 PCG Delay	0.059	0.023
	3 PCG Delay	-0.054	-0.13
1 path 100 km/hr	2 PCG Delay	-0.41	-0.58
	3 PCG Delay	-0.67	-0.75
3 path 30 km/hr	2 PCG Delay	0.054	0.040
	3 PCG Delay	0.085	0.082
3 path 100 km/hr	2 PCG Delay	-0.16	-0.22
	3 PCG Delay	-0.17	-0.26

In the 800 MHz band with no PCB error (Table 13), the proposed CLPC algorithm has a positive gain for all channel configurations except for the 3 path 100 km/hr case with Proposed(D+0.5). The proposed CLPC algorithm shows the best performance in 1 path 30 km/hr with gains of approximately 1 dB and 1.8 dB using Proposed(D+0.5) when the loop delay is 2 PCG and 3 PCG slots respectively. The FER performances of the proposed CLPC algorithm when delay is 2 and 3 PCG slots are almost the same as the FER of the conventional CLPC when there is 1 PCG delay. This indicates that the proposed CLPC is quite effective in reducing the impact of the delay in the power control loop. As the speed is increased to 50 km/hr with 1 signal path, the performance gain becomes smaller; but there is still 0.6 dB and 0.9 dB gain using Proposed(D+0.5) when delay is 2 PCG and 3 PCG slots respectively. It can be seen that when the mobile speed is low (1 path 3 km/hr), the improvement using the proposed CLPC algorithm is small. This is expected because the conventional CLPC algorithm can effectively track the fade variations when the channel changes slowly even when there are some delays. In general, when a single bit PCB scheme is used for CLPC, prediction will only improve CLPC performance when the E_b/N_t crosses the power control threshold. That is, with prediction, the future E_b/N_t value will be used for decision making for the current PCB. If the signal is entering or exiting a fade, the corresponding PCB based on the predicted E_b/N_t value can be sent earlier to mitigate the effect of the upcoming channel condition. At low speed, the Doppler frequency is low and the number of times E_b/N_t crosses the power control threshold in a given time interval is small. Therefore, the gain from the use of prediction is less obvious at low speeds. But TDC reduces power oscillation amplitudes when the Doppler frequency is low. This means that a smaller fade margin is required which in turn increases the capacity. At high speed (1 path 100 km/hr and 3 path 100 km/hr),

the improvement is small because the Doppler frequency is too high for accurate prediction of future fades. This is because for E_b/N_t to cross the power control threshold, there must be a local maximum or minimum. An increased number of local maxima or minima in a given time period generally results in poorer fade prediction accuracy. It is found that Proposed(D+0.5) gives similar results to Proposed(D) in all channel configurations. Therefore, the impact of the 0.5 PCG delay between the SIR estimation and the execution of the PCB is small.

In the 1.9 GHz band with no PCB error (Table 14), the proposed CLPC algorithm has positive gains in all 3 km/hr and 30 km/hr simulations. However, the proposed CLCP algorithm has negative gains in the 1 path 50 km/hr simulation when delay is 3 PCG slots, and all 100 km/hr simulations. The performance of the proposed CLPC algorithm running in the 1.9 GHz band follows the observations made for the 800 MHz band. That is, the proposed algorithm performs better at low to moderate Doppler frequencies and its performance degrades at high Doppler frequencies, as fade prediction is inaccurate at high Doppler frequencies. In the 1.9 GHz band, the Doppler frequency is more than two times the Doppler frequency in the 800 MHz band. In Table 14, we can see that the performance at low speed (1 path 3 km/hr) is improved when compared to the results in Table 13. As the proposed CLPC algorithm gives best performance at moderate speed (30 to 50 km/hr) in the 800 MHz band, we can expect similar performance at approximately 15 to 25 km/hr in the 1.9 GHz band.

One way to avoid degradations caused by the proposed CLPC algorithm is to check the fade prediction accuracy during run time. When the differences between the predicted SIR's for successive PCG slots and the actual SIR's of these PCG slots are greater than some threshold value for a certain period of time, we can conclude that the proposed CLPC algorithm can no longer track the channel changes. In this case,

the proposed CLPC algorithm can run with TDC only until prediction is re-enabled when the differences between the predicted SIR's and the actual SIR's are below some threshold value for a certain period of time.

When PCB errors occur at a rate of 5%, a higher E_b/N_t is required to achieve the target FER in all the channel configurations simulated. Table 15 shows the impact of a 5% PCB error rate on the conventional CLPC algorithm. The E_b/N_t required to achieve the target FER when PCB error rate is 5% is compared to the case when PCB error rate is 0%.

Table 15 Impact of 5% PCB Error Rate on E_b/N_t for the Conventional CLPC Algorithm to Achieve the Target FER at 870 MHz

Channel Configuration	E_b/N_t 5% PCB error rate (Delay=1) – E_b/N_t No PCB error (Delay=1)	E_b/N_t 5% PCB error rate (Delay=2) – E_b/N_t No PCB error (Delay=2)	E_b/N_t 5% PCB error rate (Delay=3) – E_b/N_t No PCB error (Delay=3)
1 path 3 km/hr	+0.049	+0.061	+0.059
1 path 30 km/hr	+0.58	+0.34	+0.14
3 path 100 km/hr	+0.073	+0.096	+0.12

In the 1 path 3 km/hr and 3 path 100 km/hr simulations, the impact of a 5% PCB error rate on the required E_b/N_t to achieve the target FER is relatively small. However, it is noted that the impact of PCB errors on the required E_b/N_t to achieve the target FER in the 1 path 30 km/hr channel configuration is significant and the impact decreases as the loop delay increases. This is because with no PCB errors, the performance degrades as the loop delay increases. This is most noticeable for the 1 path 30 km/hr channel configuration as shown in Table 11. It is expected that PCB

errors will tend to have the greatest impact when the CLPC algorithm is quite effective and the loop delay is small.

Next, we investigate the impact of PCB errors on the proposed CLPC algorithm. Table 16 summarizes the relative performance gain of the proposed algorithm in dB when the PCB error rate is 5%.

Table 16 Relative Performance Gain of Proposed CLPC Algorithm at 870 MHz with 5% PCB Error

Channel Configuration	Delay (n_t)	Proposed(D) Performance Gain (dB) Compared to Conventional	Proposed(D+0.5) Performance Gain (dB) Compared to Conventional
1 path 3 km/hr	2 PCG Delay	0.036	0.047
	3 PCG Delay	0.11	0.13
1 path 30 km/hr	2 PCG Delay	0.55	0.74
	3 PCG Delay	1.2	1.3
3 path 100 km/hr	2 PCG Delay	0.016	-0.067
	3 PCG Delay	0.020	-0.037

In the 800 MHz band with 5% PCB error rate, the relative performance gain of the proposed CLPC algorithm is smaller compared to the case with no errors. The proposed CLPC algorithm still shows the best performance in the 1 path 30 km/hr channel configuration with gains of approximately 0.7 dB and 1.3 dB using Proposed(D+0.5) when delay is 2 PCG and 3 PCG respectively. The performance gains drop by about 0.3 dB and 0.5 dB for delay of 2 PCG and 3 PCG respectively when compared to the 1 path 30 km/hr channel configuration with no PCB errors. A PCB error results in cascaded errors in the proposed CLPC algorithm since previously

transmitted PCB values are used for delay compensation and fade prediction. From equation (5.1), it can be seen that in the proposed CLPC algorithm, a PCB error affects up to n_t PCB decisions.

Overall, with the proposed CLPC algorithm, the same system performance can be achieved with a lower traffic E_b/N_t for a range of mobile speeds of interest, thereby increasing the capacity of the IS-2000 system.

7.0 Conclusion

In this thesis, the effects of power control loop delays on the FER of an IS-2000 forward link using the conventional CLPC algorithm and a proposed delay compensated, fade prediction based CLPC algorithm have been studied. In this chapter, we summarize the main contributions of this thesis and provide some suggestions for further study.

7.1 Contributions of the Thesis

1. **The effects of loop delays on IS-2000 forward link CLPC**

   The FER performance of the conventional IS-2000 forward link CLPC algorithm in the presence of loop delays is studied. It is shown that the increase in power oscillation amplitude with loop delays reported in [17] exists in the conventional IS-2000 CLPC algorithm. Furthermore, simulations were used to show the impact of loop delays on the FER using a detailed system model that includes coding / decoding, interleaving / de-interleaving, and spreading / despreading. The forward link CLPC test configurations from [22] were used, and simulations were run for the 800 MHz and 1.9 GHz frequency bands with total delay n_t=1, 2 and 3 PCG slots. It is also observed that the conventional CLPC algorithm FER degradations due to loop delays are relatively small at low Doppler frequencies. This is because at low Doppler frequencies, the CLPC algorithm can track the fading envelope even when there is a small time delay. For moderate Doppler frequencies, the FER performance of the conventional CLPC algorithm is sensitive to loop delays. However, the delay sensitivity decreases as the Doppler frequency increases

from moderate to high. At high Doppler frequencies, the CLPC algorithm is ineffective and interleaving is the main process that mitigates fading.

2. **A delay compensated fade prediction based CLPC algorithm**

A delay compensated, fade prediction based CLPC algorithm that can reduce power oscillation amplitude and improve SIR estimation in the presence of loop delays is proposed. The proposed CLPC algorithm can reduce the required fading margin and lower the E_b/N_t needed to achieve the target FER thereby resulting in an increase in the system capacity. The proposed CLPC algorithm can be easily implemented in an IS-2000 compliant system with no additional hardware requirements. The only change required is an upgrade of the firmware which controls the generation of the PCBs.

3. **FER performance comparison of the conventional and proposed CLPC algorithms**

A detailed IS-2000 system model was used to simulate the FER performance of the proposed CLPC algorithm. Using CLPC test setups from [22], simulation results for the forward link show that the proposed CLPC algorithm performs better than the conventional CLPC algorithm for a range of Doppler frequencies of interest. As the Doppler frequency increases from 0, the relative performance of the proposed CLPC algorithm improves until some threshold value, f_D^T. Above f_D^T, the relative performance degrades gradually. This is because the prediction algorithm cannot accurately track the fading envelope and the SIR estimation becomes inaccurate at high Doppler frequencies. Studies on the effect of PCB errors on the proposed CLPC algorithm show that the difference between the FER performance of the conventional and proposed algorithms decreases when the PCB error rate is

5%. This is because the proposed CLPC algorithm uses previously sent PCBs to correct the SIR estimation and PCB errors reduce the accuracy of the SIR estimation. It is found that the proposed CLPC algorithm offers a noticeable improvement in the FER performance compared to the conventional CLPC algorithm when the Doppler frequency is moderate.

7.2 Topics for Further Study

Several methods by which the performance of the proposed CLPC algorithm can be improved are suggested below.

1. **Suppression of fade prediction at high Doppler frequencies**

   It was observed that at high Doppler frequencies, the proposed CLPC algorithm could have a worse FER performance than the conventional CLPC algorithm. Thus a scheme which disables fade prediction when the Doppler frequency exceeds some threshold value could be studied. Its performance could be compared with the scheme suggested in Chapter 6.4 which is based on the difference between the predicted SIR and the actual received SIR.

2. **Application of prediction on each multipath**

   The proposed CLPC algorithm uses the E_b/N_t values after MRC to predict channel fades. Simulation results show that the relative FER performance of the proposed CLPC algorithm is better in the 1 path case than in the 3 path case at moderate Doppler frequencies. It is expected that if channel information from each multipath were used for prediction, the performance in the 3 path case would be improved. The predicted channel condition from each multipath can be combined at the end and then used to generate an

E_b/N_t estimation for future PCGs. The performance improvement which can be obtained by such an approach should be studied.

3. **Higher order prediction algorithm**

Linear extrapolation was used in this thesis to predict channel fades. Other fade prediction algorithms can be studied and used with delay compensation to possibly improve the proposed CLPC algorithm performance. For example, quadratic curve fitting can be used on the SIR samples to predict channel fades. It is expected that when a higher order prediction algorithm is used, more delay compensated E_b/N_t samples will be needed by the prediction algorithm. Higher order prediction algorithm sensitivity to PCB errors should be studied.

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