MODELLING OF HVDC CONVERTERS FOR REAL-TIME
TRANSIENT SIMULATORS

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We accept this thesis as conforming
to the required standard

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This thesis presents developments in the computer modelling of High Voltage Direct Current (HVDC) converters and other FACTS devices for EMTP-type simulators.

The high number and frequency of switching operations in power electronic converters cause numerical difficulties that require additional computational effort. The additional computational burden requires the development of techniques that can accelerate the simulation speeds of conventional electromagnetic transient modelling and may allow real-time simulations.

The main results are two models that effectively reduce the computational time required to obtain the solution of an electrical network containing HVDC converters. Both approaches have in common the principle of subdividing an electrical circuit containing a 6n-valve converter into at least n subsystems. For each 6-valve subsystem, the 64 matrix combinations are precalculated and prestored in computer memory. The interaction between subsystems to obtain the network solution is particular to each approach. With this criterion, the number of precalculated combinations for a 24-valve HVDC substation is reduced from more than 16 million to only 256. Both models present a considerable reduction in the computational time required to simulate circuits containing HVDC converters. The most efficient model has been successfully implemented in the real time power systems simulator under development by the power research group at the University of British Columbia.

The exact calculation of the network solution at switching events is another important aspect required to accurately simulate power electronic converters in power systems. The thesis proposes the zero crossing detection algorithm, which eliminates the erroneous delays present in
traditional EMTP simulators. The proposed algorithm resynchronizes the solution to the original simulation time increment.

To solve the problem originated by the forced commutation of Gate Turn Off Thyristors, an exploratory solution technique is proposed. This methodology eliminates the unrealistic voltage spikes that arise when chopping currents in discrete-time simulators. The resultant algorithm avoids the necessity of forcing the semiconductors to work as pairs, as some EMTP simulators solve the problem.

Finally, the thesis includes a model for a Thyristor Controlled Reactor that maintains a constant conductance at switching operations, thus reducing the computational time when modelling Static Var Compensator substations.
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DEDICATION

To my parents:

Salvador Acevedo Ricárdez

Alicia Lilia Porras de Acevedo

Through my life I always have had the unconditional support of my parents in all my personal and professional activities. They consistently have encouraged me to pursue a new goal after finishing the previous one. They have been there for me at all times. I would like to recognize their invaluable support, constant encouragement, and truthfully love by dedicating this especial achievement to both of them.
Introducción

Electric power system networks transport electric energy from generating stations to consumption loads. The optimal and efficient operation of these systems requires constant research and development from power system engineers.

For many years, power system simulators have helped not only to analyze, understand and improve the operation of power systems, but also to design new configurations and new applications. The testing of equipment under abnormal situations is another important feature that some simulators provide.

Analog simulators are extensively used for both analyzing and testing power networks and their equipment. Their drawbacks are their high cost and restricted flexibility.

Digital simulators have the flexibility to simulate almost any kind of network topology. They rely on the availability of accurate models and are widely accepted nowadays.

When modelling electromagnetic transient phenomena, digital simulators solve the electrical network at discrete time steps, and commonly, this requires important amounts of computation. In most cases, the number of computations is so large that the time required to obtain the solution is several times longer than the actual simulated time. This is especially true when simulating large networks or networks with switching operations.

Power electronic circuits contain semiconductor devices that are operated as switches with periodical closing and opening. If the semiconductors are modeled using a digital simulator, the switching actions increase the required simulation time.
The Power Systems Group at the University of British Columbia (UBC) is presently working on the development of a general-purpose digital simulator for power systems. One of the objectives is to be able to simulate cases in real time. Among other applications, this feature will allow users to test protective devices and control equipment.

The development of a real-time simulator requires models that are not only accurate, but are fast enough to solve the network under study as fast as the real-time events that the simulator interfaces.

During the work of this thesis, the author has developed models for High Voltage Direct Current (HVDC) converters and other Flexible Alternating Current Transmission System devices (FACTS) for electromagnetic transients simulation. The form and solution algorithmic design of these models is aimed at allowing much faster solutions than conventional models while giving results that are accurate and free of numerical noise and numerical stability problems.

1.1. HVDC Transmission Systems

High Voltage Direct Current (HVDC) transmission systems have several advantages over their AC counterparts.

The main problem of AC systems is the necessity to maintain all the synchronous generators operating in synchronism. Synchronous operation requires to keep the AC lines loaded below the steady-state and transient stability limits, and to have a common frequency for the entire system at all times. It is particularly difficult to maintain a stable weak connection between two large AC systems. On the other hand, if a DC link is used, then the power transfer capability is not related
to the transmission line and the two AC systems joined by the DC link are not required to be in synchronism [76], [78].

Cables and lines for DC transmission have fewer losses and are less likely to be affected by disturbances. However, difficulties to convert DC signals, most notably in the early years of power systems, made alternating current systems more popular. It was not until the development of the high voltage mercury arc valve during the 1950s, and the introduction of solid-state technology in HVDC systems at the end of the 1960s, that DC systems became commercially competitive. Fig. 1-1 depicts the HVDC world scenario.

Despite the benefits of DC systems and the economical savings in cables and lines, the high cost of the required equipment in HVDC substations explains the reduced amount of HVDC systems in the world. It is at the bulk level of transmission of electric energy, where long transmission lines, underground and submarine lines, asynchronous interconnection of AC systems, and interconnection of AC systems with independent control strategies, make the cost and technical performance of DC transmission links advantageous [78]. For example, the largest application in the world is the 6,300 MW Itaipu HVDC system installed in Brazil [84]. The HVDC link at Itaipu provides a 50/60 Hz asynchronous tie which allows transmission distances in the order of 800 km.

To achieve high voltages, Silicon Controlled Rectifiers (SCRs, also called thyristors) are connected in series to form a valve. A single thyristor is commonly designed for 8 kV, and typical applications have up to 60 series-thyristors per valve [32]. The operation of thyristors is explained in further detail in section 3.1.
An HVDC link has one sending end and one receiving end. There are several configurations in use depending on the number of converters and lines. A monopolar system has only one pole that may have either positive or negative voltage, and normally has a ground return. A bipolar system essentially consists of two monopolar systems of opposite polarity. A back-to-back converter is mainly used to interconnect systems with different frequencies; it does not have a DC transmission line and both converters are at the same substation.

The converter located at the sending end is called the rectifier and the converter at the receiving end is the inverter. For power reversal, the voltage polarity is changed and the rectifier now receives energy, thus becoming the inverter, and vice versa. It should also be noted that, because of the commutation requirements of thyristor valves, thyristor based DC links require AC systems at both ends. Fig. 1-2 shows the sending end and receiving end for each polarity of the DC line.
Fig. 1-2. HVDC link:
(a) Line is operating as a positive pole. (b) Line is operating as a negative pole.

From the power system perspective, the control of an HVDC system is fast and simple. However, the power electronic semiconductors that constitute the DC bridges require sophisticated controllers with accurate and reliable circuitry and the substation design and installation are fairly complicated when compared to AC transformer substations. Also, the interactions among AC-DC systems can be quite complex [83]. It is at this level where analog and digital simulators provide an excellent tool for the planning, design and development of DC based systems [60].
1.2. Applications of Power Electronic Devices in Power Systems

The application of power electronic devices in power systems has been gaining popularity as manufacturing companies increase the rating of semiconductor devices, and as more reliable controllers become available. These factors have permitted and encouraged a substantial growth of HVDC links during the last two decades [12], [32], [76]. The use of thyristors has evolved into the development of FACTS devices to improve the operation and control of AC systems [12], [31], [33].

Thanks to the semiconductor revolution, Direct Current transmission systems now are practical. There are yet other HVDC related applications, and some of them are now briefly described.

Static Var Compensators (SVC) improve voltage regulation by generating or absorbing the required reactive power at strategic points in the network [28]. The first SVCs were developed in the late 1960s. The basis of their operation is the dynamic adjustment of reactive power by connecting or disconnecting Thyristor-Switched Capacitor banks (TSC) and by controlling Thyristor-Controlled Reactors (TCR) [71].

In addition to their present use in certain applications, newer developments in high power Gate Turn Off thyristor (GTO) technologies are the future for a large spectrum of modern and sophisticated power system applications [53], [70], [77], [105], [108], [109], [110]. Chapter 5 includes models developed in this thesis for efficient modelling of GTO-based converters.

The advanced static VAR compensator or STATCOM is the power electronic version of the synchronous condenser. A modulated GTO inverter converts the DC voltage of a charged capacitor into an AC voltage. STATCOMs provide both lagging and leading reactive powers by
adjusting the inverted voltage. Detailed theory on advanced static VAR compensators can be found in [21] and [29].

In [92], Schauder et al. planned the first large application of a ±100 MVAR STATCON (now STATCOM) substation. Another application presented by Kimura et al. demonstrates how a static condenser can help improve the performance of an HVDC inverter when feeding a weak AC system [46].

The use of GTO thyristors in HVDC converters allows the supply of remote passive loads without AC generation. A large 300 MW self commutated inverter is under development [95].

HVDC Light [1] is the first successful application of a self commutated HVDC inverter feeding a passive load (where there is no AC source). Instead of dealing with bulk power transmission, HVDC Light is designed to use the advantages of DC transmission when transmitting just a few MW to a passive load. This first 10 km, 3 MW ±10 kV HVDC Light installation was commissioned in Sweden in March, 1997 and is based on a forced commutated voltage source converter (VSC). This new technology promises to be an alternative to conventional AC transmission or local generation under situations where the load size and location are relatively small when compared to traditional HVDC links.

1.3. A Real-Time Power System Simulator

Software based power system simulators have turned out to be not only an excellent tool in the analysis and design of networks and devices, but also have become an essential instrument for the power systems engineer.
When studies are performed off-line, system data is collected and entered into the computer, processed by the simulator, and analyzed once the simulation output is ready. Sometimes several iterations give a clearer picture of the situation under study and help make decisions.

In the case of performing online simulations, the user can interact with the power system with the help of a computer simulator. The importance of the interaction between the user and the computer becomes crucial if the simulator results are used to control the network. The actions that the operator takes after obtaining the computer results will affect the system response. Stand-alone online simulators do not require contact with any operator but may exchange information with other computers or with a physical controller.

Critical factors in real-time applications are the simulation time and the accuracy of the models. The simulation time is the time that the simulator takes to solve the programmed models that represent a particular system. In an online simulator, real-time simulation is essential.

Real-time simulation implies computation of a phenomenon and precise reproduction of its behaviour at the same rate as the phenomenon occurs. For slow changing systems, the currently available digital computers are likely to be able to simulate and reproduce a case in real time. For power electronic applications in power systems, a frequency bandwidth of about 2 kHz in the solution waveforms is considered adequate. If real-time performance is desired, the simulator has to produce a solution in less than the chosen integration step. Taking into account the distortion introduced by the integration rule (e.g. trapezoidal or backward Euler) in the numerical solution, an integration step of 100 μs produces a distortion error of about 10% while an integration step of 50 μs reduces this error to about 3%. On the other hand, a 50 μs step corresponds to approximately 1° in the firing angle of the converter valves, and this resolution or better may be
desirable in some cases involving the proper operation and testing of controller actions. With the use of such small time steps, it is possible to perform accurate investigation of faults, harmonic interference, resonance and other fast transient phenomena of special interest when modelling HVDC systems [88].

During the past few years, the main interest of the Power Systems Group at UBC has turned to the development of a software-based real-time simulator for power systems. References [64], [67], and [68] present the latest efforts of the group. This simulator is named Object-oriented Virtual Network Integrator (OVNI™) [52], [68]. It is a goal to have the first release ready within the next year.

The main intention of OVNI involves having a computer program that is running continuously while simulating the power system. For instance, the program simulates any normal or abnormal behaviour of a power system network in real time and may suggest actions to prevent instability. Another application is the testing of protective equipment and control equipment without having to provoke faults in the actual power system. New control strategies can be extensively experimented using such a simulator. If the simulator behaves as the power system, then the tested device may be connected directly to a hardware interface, and the computer simulates the power system behaviour to prove and adjust the equipment. More advanced applications will allow prediction and correction under disturbances with the support of artificial intelligence routines.
1.4. Thesis Objectives

The OVNI simulator requires the development of models for each element of a power network that are suitable for real-time simulation. Power electronic devices are of special interest to the power systems community involved in the development of real-time digital simulators.

The objective of this thesis is to provide a model for High Voltage Direct Current Converters that can be adapted to the OVNI simulator under development.

As a result of the research, the author presents two approaches to modelling HVDC converters that considerably improve solution times over off-line simulators like MicroTran® (UBC’s Electromagnetic Transients Program). One of these approaches has already been implemented in a companion research project [52] and proven its real-time performance [64].

It is important to mention that the models developed in this work achieve real-time performance within the context of a simultaneous solution with the rest of the power network. To this author’s knowledge no other research group working on real-time simulators has achieved real-time performance for full-size converters (12 and 24 valves) with simultaneous power system and converter solutions. Alternatives have been proposed in which the solution of the converter is decoupled from the solution of the network by a time delay equal to the solution time step [101]. This approach allows an independent solution (possibly in separate processors) of the network and of the converter. The problem with this approach is that it can lead, depending on the simulation, to not only inaccurate solutions but also to numerical instability. The possibility of having these problems was considered unacceptable under the concept of OVNI which is that of a continuously running simulator, thus requiring high confidence in the results and absolute long-term numerical stability of the output.
In addition to the modelling of HVDC converters for real-time simulators, research was also done on accuracy and numerical optimization issues pertaining to other FACTS devices. One of these issues was the development of an efficient zero crossing detection and interpolation algorithm to accurately simulate the commutation point of the valves within the context of the Critical Damping Adjustment algorithm (CDA) of the EMTP [66]. Another development is an efficient exploratory solution algorithm for the accurate simulation of GTO-based forced commutated converters such as the HVDC GTO-inverter feeding passive loads and the Advanced Static Converter (STATCOM). Further work permitted the creation of a model for the simulation of Static VAR Compensator substations (SVC) with improved solution times.

All of the models and features described above have been programmed and tested in an Object Oriented Programming (OOP) environment using the ADA 95 programming language.

This document has six chapters including this Introduction in Chapter One. Although the complete document includes appropriate references, Chapter Two is an extensive literature review and a discussion of HVDC simulators. Chapter Three reviews briefly the nodal analysis and the discrete time solution technique of the original Electromagnetic Transients Program EMTP. This chapter also includes the diode and thyristor models, the filter models, the zero crossing detection algorithm, and an example of application of the Multi-Area Thévenin Equivalent Algorithm (MATE). Two HVDC models, with very good solution speed times, are proposed in Chapter Four, while Chapter Five is reserved for the models of some FACTS devices, such as forced commutated inverters, STATCOMs and SVCs. Finally, Chapter Six contains the conclusions of this work and suggestions for future developments. Appendix A includes a description of the MATE algorithm. Appendix B contains the derivation of the discrete-time equivalent model for power transformers.
2. CHAPTER 2

HVDC AND POWER SYSTEMS SIMULATORS

Both analog and digital simulators are useful tools to model the behaviour of fast transients in power systems and play an important role when analyzing HVDC systems and their controls. A literature review of power system simulators for HVDC and related problems is now presented.

2.1. Analog Simulators

Analog simulators are also known as Transient Network Analyzers (TNA) and those for HVDC systems are known as DC simulators. A DC simulator consists of a physical scaled-down replica of the system under study. These simulators always operate in real time because they are physical devices interconnected as the original system they represent. They also give a practical sense of the case under study.

The real-time ability of DC simulators makes them excellent tools for testing of protective devices and HVDC or FACTS controllers. DC simulators have been successfully used for many years in the design of HVDC schemes [37], [60].

The disadvantages of DC simulators are the expensive cost of the equipment, the restricted flexibility to represent different networks, and the lack of accurate representation of some elements. For example, to represent a transmission line, a TNA uses multiple $\Pi$ or $T$ sections of resistors, inductors and capacitors. This configuration cannot very accurately represent the distributed nature and frequency dependence of the line parameters [67]. To overcome this
problem, Mathur and Wang [69] have proposed to incorporate a digital model of the transmission line to a TNA using digital-to-analog converters.

2.2. Digital Simulators

The most common approaches used to solve transients in HVDC systems are: the use of programs developed under the Electromagnetic Transients Program (EMTP) technique, the State Variable technique, the Transmission Line Modelling (TLM) method, and the use of transient stability programs.

2.2.1. The Electromagnetic Transient Program and EMTP-Type Simulators

These digital simulators use a mathematical discrete-time model for each network element. By choosing an appropriate methodology, they combine the element models to solve the system equations. Among the advantages of digital simulators, it is worthwhile to emphasize their accuracy, their non-susceptibility to environmental factors, their flexibility, and their lower cost.

The EMTP is based on Dommel's algorithm [17] and is probably the most widely accepted computer program for electromagnetic transient studies in power systems. In [56], Long et al. presented a summary of the different EMTP capabilities. The models in this thesis are based on EMTP methodology. Due to the importance that this has for this project, section 3.1 is dedicated to illustrate the EMTP foundation. All the models and cases developed during this research were compared against the results obtained with the program MicroTran, which is based on the UBC version of the EMTP.

EMTP simulators have been extensively validated in the simulation of power systems containing HVDC converters. In [26], [30], and [60], there are complete validations of HVDC
models in the EMTP with field data obtained from the Pacific HVDC Intertie and the Intermountain Power Project HVDC transmission systems. Additionally, [60] compared EMTP simulations with tests performed on a DC simulator. These papers’ conclusions coincide in stating that EMTP simulators are excellent tools for the simulation of HVDC transmission systems. A paper comparing EMTP with field test measurements on the Hydro-Quebec - New England system is presented by Morin, Buri, Casoria and Reeve in reference [73].

Woodford, Gole and Menzies presented the structure and performance of the Manitoba Hydro Electromagnetic Transients Program for DC systems (EMTDC) as compared to field data for a fault recorded at the Nelson River DC Transmission system [103]. EMTDC is also based on Dommel’s algorithm placing emphasis on the simulation of HVDC systems, and in particular, their controllers. EMTDC has proved to be an excellent simulator for the solution of HVDC control problems [100] and is the base for the Real Time Digital Simulator (RTDS\textsuperscript{TM}) developed by the Manitoba HVDC Research Centre [48], [74].

Other comparisons useful for the validation of HVDC cases with EMTP-type simulators can be found in [11], [13], [45], [85], [93], [96], [98], [102], [104], and [111]. For those involving FACTS devices the reader may consult [51], [87], and [91].

NETOMAC is a digital program used in Europe for the simulation of electromagnetic transients developed under the EMTP methodology. In [47], Kruger and Lasseter used NETOMAC to simulate the transient behaviour in HVDC converters. The main difference of NETOMAC is that it allows the shifting of the time mesh to coincide with a switching event. This shift, coupled with the correction in the integration solution, eliminates the problem of
numerical oscillations. With this scheme, however, the simulator output is not available at uniform time steps, which poses a problem for real-time solutions.

PECAN, now PSPIM, is another example of a circuit analysis simulator useful for the analysis of power electronic circuits [3], [39], [90]. PSIM has a user friendly interface. It has been a useful simulator for HVDC studies, and has good capability to model the converter controllers as demonstrated by Jin, Sood, and Chen in [40].

Simulators such as EMTP, MicroTran, EMTDC, NETOMAC and PSIM have demonstrated how to produce accurate results when modelling HVDC systems, and are widely used worldwide. In all these simulators, however, there is a notorious increase in the computational effort required to obtain the solution at switching events. The resultant augmented solution times hinder any attempt to obtain simulations of power electronic devices in real time.

The iterative solution of the discrete-time equations of a network equations with the Newton-Raphson leads to the development of important general-purpose programs such as SPICE (Simulation Program with Integrated Circuit Emphasis) [75] and Saber [60]. One advantage of these programs is their ability to use elaborate models of microelectronics and integrated circuits, a very important feature for the design of semiconductors and chips. Despite the emphasis on integrated circuitry that SPICE has, it is also useful for the simulation of power converters in power systems. See [106] as an example of the simulation of a STATCOM using PSPICE.

In SPICE-type simulators, the solutions are even slower because the detailed modelling of semiconductors involves sets of non linear equations that in many instances increase the number of iterations per time step. An appropriate set of equations for semiconductors is essential for the modelling of electronic amplifiers and integrated circuits, because their transistors operate in the
active zone at almost all times. For power electronic applications, though, the semiconductors are operated as switches; in the case of using transistors, this is accomplished by turning them either into saturation or cutoff. Therefore an on/off representation is satisfactory.

2.2.2. State Variable Simulators

The state variable formulation uses the network topology to generate incidence matrices. Kirchhoff laws are then applied and differential equations are generated using a Tableau. The solution is then found using any integration technique.

As opposed to the EMTP, a variable time step is allowed with the state variable technique. In fact, this has been advantageous when simulating power electronic converters and some authors have interfaced EMTDC solutions of power systems with the state variable representation of HVDC and SVC converters. In [27], Gole and Sood used a state representation for a SVC converter and an EMTP representation for the rest of the network. Their excellent work uses a reduced time step during switching operations for the SVC only and keeps a fixed time step for the rest of the network. A similar procedure is presented for an HVDC converter by Zavahir, Arrillaga and Watson [107]. The simulation does not slow down notoriously because only the solution of the converters are simulated with a reduced time step. In [72], Milias, Hatziadoniu and Galanos developed a general and computationally efficient algorithm for the construction of state equations of power converters as a function of the state of their switching elements, thus reducing the number of operations required by the algorithm.

The simulation of any circuit is feasible with the state variable algorithm since it is of general purpose. Examples of programs using this technique for the simulation of HVDC and other power electronic converter systems are the Converter Analysis Program (CAP) [54], the
Switched Electronic Analysis Program (SWEAP) [16] and ATOSEC5 and ATOSECM [97], just to mention a few.

There is an interesting comparison between the EMTDC and a Transient Convertor Simulator (TCS) based on the state variable formulation showing similar results and similar simulation times for an HVDC test circuit under certain circumstances [7]. The authors of this paper mention that despite the reputation of less efficiency attributed to the TCS, the results obtained show its advantages.

The main drawback of simulators based on the state variable formulation is the requirement of an iterative algorithm to find the solution at each time step. The number of iterations is sensitive to non-linearities in the circuit, thus considerably increasing the computational time at switching events. Such a disadvantage makes state variable-based simulators much slower than EMTP-based simulators. This explains why the authors in [22] and [95] (from the discussion presented above) combined the EMTP representation for the network with the state representation for the converters.

2.2.3. TLM Simulators

The Transmission Line Modelling (TLM) technique applied to the solution of power electronic switching networks is detailed in [34]. Each element is converted to a discrete-time equivalent by the use of transmission line sections and a constant matrix is formed. In order to keep the matrix constant, Hui and Christopoulous [34] model diodes and thyristors as an inductance for the closed state and as a capacitance for the open state. Applications of the TLM technique to the simulation of power electronic converters can be studied in [24], [34], [35], and [36].
The approximation of a switch as an inductance/capacitance for the on/off states can also be
done with the EMTP by using a constant conductance and changing the history source equation
in the discrete-time equivalent. In [82], Pejovic and Maksimovic related both approaches.

TLM is an innovative way to discretize an electric circuit, and can be visualized as an EMTP
dual. Nevertheless, the representation of the elements as a transmission line introduces modelling
inaccuracies. A transmission line always includes both inductive and capacitive effects, and,
most likely, the simulation of pure inductors or capacitors is subject to error.

2.2.4. Transient Stability Programs for HVDC Simulation

Transient stability programs are used to solve the dynamic response of power networks, and
in particular, the effects of the disturbance on the frequency. In transient stability programs,
HVDC converters and FACTS devices can be modeled as quasi-steady state elements where the
DC and AC quantities are related by transfer functions [41], [79], [88], [104]. Because in these
programs HVDC converters are visualized from the outside terminals, it is not necessary to
represent the valves' behaviour in detail. If the DC converter is not the main focus of attention
during the analysis of a network, this approach may have some merit. The lack of detail in the
simulation of the HVDC converter saves computational effort. Moreover, because the individual
valves are not modeled thoroughly, it is possible to use large calculation steps, in the order of
100-200 μs, as suggested by Woodford et al. [104].

Since this approach lacks a detailed representation of the converter's components, it is not
useful for modelling the behaviour of the HVDC converter during fast transient phenomena, AC
faults, DC faults, converter faults (e.g., commutation failures and misfiring), or to study the
HVDC controls and protection schemes.
2.3. Real Time HVDC Studies

Researchers around the world are working on optimizing models and algorithms and on using state of the art technology to make real-time digital simulation of HVDC systems a reality.

The large number of switching operations in the digital simulation of power electronic devices requires special attention if real-time performance is attempted.

In EMTP-type simulators, each switching operation requires a change in the admittance matrix, which is a time consuming task. In [60], Martensson et al. emphasized that EMTP does not offer the advantages of real-time simulation, capability inherent with a DC simulator which is of critical importance to suppliers of HVDC equipment.

The state variable technique requires a reformulation of the state equations. This process is computationally expensive. Attempts to maintain the admittance matrix constant during an EMTP simulation and the use of the TLM method have been referred to in section 2.2.3.

Other attempts to achieve real-time simulation are now discussed, and some of them have already been successful when using appropriate hardware/software technology.

The Manitoba HVDC Research Centre developed a Real-Time Digital Simulator (RTDS). This real-time digital simulator is probably the most recognized application of this kind available for power systems. In [48], Kuffel et al. presented details on the design, architecture and applications of RTDS. The simulator is a combination of specialized computer hardware and software designed specifically for the solution of power system electromagnetic transients. Its capabilities allowed it to substitute for existing analog simulators in applications such as the testing of protective relays and the testing of system controllers. The hardware is organized into
individual racks. Each one contains digital processing cards for interfacing with a host computer, and for communication among processors. The software includes a graphical user interface, a compiler, and a library with power system component models written in low level machine language code. The systems under study are subdivided into areas isolated by transmission lines and these areas are solved separately in individual intercommunicated racks using nodal analysis as in the EMTP.

RTDS has also been used to expand the capability of traditional DC simulators. For example, an interconnection of an analogue simulator to RTDS is shown in [9] and [50]. This application permits the representation of larger AC networks and the use of the accurate modelling of system elements available when using digital simulators. An actual HVDC controller may be completely modeled with RTDS as demonstrated by Giesbrecht, Jiang and Mazur in [25]. In [99], Valiquette et al. used RTDS to optimize the controller system of an HVDC station in the Manitoba Hydro Power System.

In RTDS, the splitting of the network into independent areas can introduce inaccuracies if these areas have coupling between them. This is not a problem when the areas are separated by transmission lines, since the lines effectively decouple the network. However, to achieve real-time performance, the user needs to chose other points for subdividing the network where there are no transmission lines. For these cases, Kuffel et al. suggest to identify tightly coupled components to subdivide the network [48]. The solution in terms of these tightly coupled areas with a time-step delay may lead to poor accuracy and instability problems. Moreover, the user requires a vast knowledge of computer modelling of electrical networks, and an extensive familiarity with the tested system. Interconnection of the RTDS simulator to analogue simulators can introduce the same problems. Another limitation is the rigidity of a test system once it has
been set up; making changes to the network topology may be difficult and time consuming. In addition, the high cost of the RTDS equipment gives it a limited market.

The subdivision of the system into areas is similar to the methodology proposed and implemented in UBC’s Real Time Network Simulator (RTNS), by Martí and Linares in [67]. RTNS has as an advantage that it is completely software-based providing flexibility to simulate different configurations. RTNS was the starting point for the new OVNI development [52], [68].

Parallel processing techniques using multiple processors have also been proposed to achieve improvements in the solution speed. In [10], Bridges et al. used parallel processing techniques to simulate the behavior of a Static Var Compensator.

In the parity simulator presented in [42], the state variable equations of the studied circuit are hardwired in an analog computer. Physical modules for integrators, summers, multipliers, divisors, source generators, limiters, and other basic components are interconnected and the solution is obtained in real-time. Unfortunately, topological changes require a reformulation of the equations and new interconnections of the components.

Another power electronics simulator, using the state variable approach, uses multiple digital signal processors and solves the network at nearly real-time speeds [86].

For relay testing, reference [44] illustrates an EMTP-type digital simulator with real-time performance. Although it is not directly related to HVDC systems, this application presents a clear example of the usefulness of a real-time simulator. This design uses a conventional single processor in combination with advanced digital signal processors.
Computer simulation is an important step when developing new systems. Detailed modelling of the power electronic equipment is needed when testing actual physical controls and protective relay equipment. The use of analog simulators and real-time digital simulators is the easiest way to corroborate an adequate functionality whenever new equipment is introduced or changes in the system operation are studied.
3. Chapter 3

Computer Solution Techniques

The first part of this chapter reviews the fundamentals of nodal analysis and EMTP discretization techniques, and describes how these are applied in the models developed in this thesis for the elements of an HVDC converter station. The second part contains an algorithm that improves the accuracy of the solution of circuits containing switches by detecting the exact instant at which the current crosses zero; the algorithm resynchronizes the solution to maintain a fixed time step in the output. The last part reviews the use of the Multi-Area Thévenin Equivalent (MATE) algorithm to subdivide a network into subsystems that can be solved independently.

The contents of this chapter are the base for the development of the new HVDC and FACTS models derived during this thesis work which are part of the OVNI Project in progress in the Power System Simulation research group [68].

3.1. Discrete-Time Solution of Networks using Nodal Analysis

In the EMTP, every element is converted into its discrete-time equivalent. If a constant time-step size is used, nodal analysis can be applied by forming a constant conductance matrix and a current source vector. If a variable time step is desired, the conductance matrix has to be reevaluated whenever the time-step size is changed. The matrix also needs to be reevaluated if there is a change in the network topology. For example, to simulate power electronic circuits, the EMTP models the semiconductors as ideal switching devices. Every time a valve opens or closes, a switching event is generated and the conductance matrix is changed accordingly [18], [20].
The EMTP uses the trapezoidal rule of integration which has good accuracy as demonstrated in [65]. The trapezoidal rule, however, produces numerical oscillations when discontinuities arise; the use of Critical Damping Adjustment (CDA), developed by Martí and Lin [66], solves this problem.

3.1.1. Nodal Analysis

Nodal analysis is based on Kirchhoff’s Current Law leading to the formulation of a system of N equations of the form,

\[ YV = J \]  

(3-1)

where:
- \( N \) is the number of nodes in the system, excluding ground
- \( Y \) is the admittance matrix (order N\times N)
- \( V \) is the vector of N voltages referred to ground
- \( J \) is the vector of N current sources injected into the nodes

For each independent voltage source, the voltage of the node at which the source is connected is known. If there are N2 sources, the number of nodes with unknown voltages is \( N_1 = N - N_2 \) and (3-1) can be partitioned as follows,

\[
\begin{bmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{22}
\end{bmatrix}
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix} =
\begin{bmatrix}
J_1 \\
J_2
\end{bmatrix}
\]

then

\[ Y_{11}V_1 = (J_1 - Y_{12}V_2) \]  

(3-2)

where:
- \( V_1 \) is the vector of N1 nodes with unknown voltages referred to ground
- \( V_2 \) is the vector of N2 nodes with voltage sources connected to it (known voltages)
- \( Y_{11}, Y_{12}, Y_{21}, Y_{22} \) are admittance submatrices of order N1\times N1, N1\times N2, N2\times N1, N2\times N2, respectively
- \( J_1 \) is the vector of source currents entering the N1 unknown voltage nodes
- \( J_2 \) is the vector of source currents entering the N2 known voltage nodes
Equation (3-2) is a system of \( N_l \) equations that can be solved for \( V_1 \) by any numerical method. Currents in the element are then obtained using the original elements' branch equations.

### 3.1.2. Integration Rules

Each element in an electric circuit has a certain relationship between its voltage(s) and current(s). Sometimes this relationship is a differential equation (or a set of differential equations) that can be translated to the discrete-time domain generating difference equations. These equations can be represented by a discrete-time equivalent circuit consisting of resistance and source combinations. Their values depend on the integration rule.

If each element of a network is represented by its discrete-time equivalent, nodal analysis can be applied for the solution of the circuit at discrete time steps. Since the discrete-time equivalents contain only conductances, the admittance matrix \( Y \) in (3-1) does not have reactive components and becomes a conductance matrix \( G \) [17].

#### 3.1.2.1. Resistors, Inductors and Capacitors

Table 3-1 shows the discrete-time equivalents for resistors, inductors, and capacitors using both the trapezoidal and the backward Euler integration rules. The reader may consult [18] and [66] to review the basis of the derivation of these equivalents.

#### 3.1.2.2. Transformers

Transformers are modeled as ideal transformers with leakage inductance. Winding resistances and a magnetization branch can be added externally. The derivation of the transformer equivalent of Fig. 3-1 using the trapezoidal rule is presented in Appendix B. The same procedure can be extended to three-phase transformers and to \( n \)-winding transformers.
Both the trapezoidal and the backward Euler equivalents for the two-winding single-phase transformer of Fig. 3-1 are summarized in Table 3-2.

![Fig. 3-1. Two-winding single-phase transformer with leakage inductance \( L_t \).](image)

3.1.2.3. Transmission Lines

There are several transmission line models for EMTP-type programs; among them we have the constant parameter line model [20], and those including frequency dependence [14], [59], [61]. For simplicity in the initial development of the proposed HVDC model, the constant parameter line model was implemented (Table 3-2). To include the line resistance (losses), two line segments are used with concentrated resistances at both ends of each segment. In the context of the OVNI real time simulator, transmission lines in the proximity of the part of the system under study are more accurately represented using a frequency dependent line model, particularly when line to ground faults are involved. For the range of frequencies under consideration (<4 kHz), a two- or three-pole frequency dependent model for the ground mode with the rest of the modes modeled as constant parameters is sufficient for a very accurate line representation. The increase in the total system solution time would normally be in the order of 20 to 30% (closure to [67]).
<table>
<thead>
<tr>
<th>Element</th>
<th>RESISTANCE</th>
<th>INDUCTANCE</th>
<th>CAPACITANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>( i_R )</td>
<td>( i_L )</td>
<td>( i_C )</td>
</tr>
<tr>
<td></td>
<td>( R )</td>
<td>( L )</td>
<td>( C )</td>
</tr>
<tr>
<td></td>
<td>+ ( v_R )</td>
<td>+ ( v_L )</td>
<td>+ ( v_C )</td>
</tr>
<tr>
<td>v-i relation</td>
<td>( v_R(t) = R \ i_R(t) )</td>
<td>( v_L(t) = L \frac{di_L(t)}{dt} )</td>
<td>( i_C(t) = C \frac{dv_C(t)}{dt} )</td>
</tr>
<tr>
<td>(time domain)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Discrete-time</td>
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<td></td>
</tr>
<tr>
<td>equivalent</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( i_R(t) = \frac{1}{G} v_R(t) )</td>
<td>( i_L(t) = G_{Leq} v_L(t) + h_L(t) )</td>
<td>( i_C(t) = G_{Ceq} v_C(t) + h_C(t) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Values for</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>trapezoidal rule</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( G = \frac{1}{R} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{Leq} = \frac{2L}{\Delta t}, \ G_{Leq} = \frac{1}{R_{Leq}} = \frac{\Delta t}{2L} )</td>
<td>( h_L(t) = i_L(t-\Delta t) + G_{Leq} v_L(t-\Delta t) )</td>
<td>( R_{Ceq} = \frac{\Delta t}{2C}, \ G_{Ceq} = \frac{1}{R_{Ceq}} = \frac{2C}{\Delta t} )</td>
<td></td>
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<tr>
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<tr>
<td>Values for</td>
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<tr>
<td>backward Euler rule</td>
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<tr>
<td>( G = \frac{1}{R} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{Leq} = \frac{L}{\Delta t}, \ G_{Leq} = \frac{1}{R_{Leq}} = \frac{\Delta t}{L} )</td>
<td>( h_L(t) = i_L(t-\Delta t) )</td>
<td>( R_{Ceq} = \frac{\Delta t}{C}, \ G_{Ceq} = \frac{1}{R_{Ceq}} = \frac{C}{\Delta t} )</td>
<td></td>
</tr>
</tbody>
</table>

Table 3-1. Trapezoidal and backward Euler discrete-time equivalents for basic electric circuit elements.
<table>
<thead>
<tr>
<th>Element</th>
<th>TWO WINDING SINGLE-PHASE TRANSFORMER</th>
<th>LOSSLESS SINGLE-PHASE TRANSMISSION LINE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td><img src="image1" alt="Symbol Diagram" /></td>
<td><img src="image2" alt="Symbol Diagram" /></td>
</tr>
</tbody>
</table>
| v-i relation (time domain) | \[
\begin{bmatrix}
    di_1 \\
    di_2
\end{bmatrix} = \frac{1}{Lt} \begin{bmatrix}
    1 & -n \\
    -n & n^2
\end{bmatrix} \begin{bmatrix}
    v_1 dt \\
    v_2 dt
\end{bmatrix} 
\] \(n\): turns ratio \(Lt\): Leakeage inductance | \[
- \frac{\partial v}{\partial x} = L_i \frac{\partial i}{\partial t}, \quad - \frac{\partial i}{\partial x} = C \frac{\partial v}{\partial t}
\]
i\(x, t\) = \(f_1(x - vt) + f_2(x + vt)\) \(v(x, t) = Z_C f_1(x - vt) - Z_C f_2(x + vt)\) |
| Discrete-time equivalent | ![Discrete-time Equivalent](image3) | ![Discrete-time Equivalent](image4) |
| Values for trapezoidal rule | \[
\begin{bmatrix}
    i_1(t) \\
    i_2(t)
\end{bmatrix} = \begin{bmatrix}
    G_{11} & G_{12} \\
    G_{21} & G_{22}
\end{bmatrix} \begin{bmatrix}
    v_1(t) \\
    v_2(t)
\end{bmatrix} + \begin{bmatrix}
    h_1(t) \\
    h_2(t)
\end{bmatrix}
\] | The transmission line model does not change with integration rule |
| Values for backward Euler rule | \[
\begin{bmatrix}
    h_1(t) \\
    h_2(t)
\end{bmatrix} = \begin{bmatrix}
    G_{11} & G_{12} \\
    G_{21} & G_{22}
\end{bmatrix} \begin{bmatrix}
    v_1(t - \Delta t) \\
    v_2(t - \Delta t)
\end{bmatrix} + \begin{bmatrix}
    h_1(t - \Delta t) \\
    h_2(t - \Delta t)
\end{bmatrix}
\] | \[
\frac{1}{Z_C} \begin{bmatrix}
    i_1(t) \\
    i_2(t)
\end{bmatrix} = \begin{bmatrix}
    
    \begin{bmatrix}
    1 & 0 \\
    0 & 1
\end{bmatrix}
\end{bmatrix} \begin{bmatrix}
    v_1(t) \\
    v_2(t)
\end{bmatrix} + \begin{bmatrix}
    h_1(t) \\
    h_2(t)
\end{bmatrix}
\] |

\[Z_C = \sqrt{\frac{L}{C}}\]

\[\tau = \sqrt{LC}\]

\[
i_1(t) = \frac{1}{Z_C} v_1(t) + h_1(t) \quad h_1(t) = \frac{1}{Z_C} v_2(t - \tau) + i_2(t - \tau)
\]

\[
i_2(t) = \frac{1}{Z_C} v_2(t) + h_2(t) \quad h_2(t) = \frac{1}{Z_C} v_1(t - \tau) + i_1(t - \tau)
\]

For frequency dependent line \(Z_C\) is a function of the frequency and the history terms are multiplied by the factor \(e^{\tau}\)

Table 3-2. Discrete-time equivalents for transformers and lossless transmission lines.
The structure of the transmission line models in the discrete-time domain both for constant and frequency dependent parameter line models (such as [14], [20], [59], and [61]) allows an effective decoupling of both ends of the line through the traveling time \( \tau \). As long as the solution time step is smaller than the traveling time, the equivalent circuit at one end of the line is independent of the equivalent circuit at the other end. This peculiarity presents a numerical advantage because the nodal analysis formulation can be subdivided to solve the independent subnetworks split by the transmission line [67].

### 3.1.3. Filter Models

A more efficient converter station filter model can be obtained by combining the components of the filter branch into a single equivalent discrete-time equation. A discussion of the filters' functionality, its usefulness in power systems, and the details of an HVDC substation, can be found in Section 4.1. Two cases are considered: RLC series, and parallel RL with series C. Fig. 3-2 shows two passive filter arrangements used in HVDC substations on both DC and AC sides [85].

![Filter Diagram](image)

Fig. 3-2. Filters for HVDC converters: (a) Tuned filter. (b) High pass filter.
3.1.3.1. RLC Series

Using the trapezoidal discrete-time equivalents shown in Table 3-1, the series RLC circuit of Fig. 3-2(a) is represented as shown in Fig. 3-3 (as proposed in [18]).

From the circuit,

\[ v = v_L + v_R + v_C \]  \hspace{1cm} (3-3)

If we define:

- \( i \equiv i(t) \) \hspace{1cm} \Rightarrow \text{current at time ‘t’}
- \( i' \equiv i(t-\Delta t) \) \hspace{1cm} \Rightarrow \text{current at time ‘t-\Delta t’}
- \( v_L \equiv v_L(t) \) \hspace{1cm} \Rightarrow \text{voltage across the inductance at time ‘t’}
- \( v'_L \equiv v_L(t-\Delta t) \) \hspace{1cm} \Rightarrow \text{voltage across the inductance at time ‘t-\Delta t’}
- \( v_C \equiv v_C(t) \) \hspace{1cm} \Rightarrow \text{voltage across the capacitance at time ‘t’}
- \( v'_C \equiv v_C(t-\Delta t) \) \hspace{1cm} \Rightarrow \text{voltage across the capacitance at time ‘t-\Delta t’}
- \( v_R \equiv v_R(t) \) \hspace{1cm} \Rightarrow \text{voltage across the resistance at time ‘t’}
- \( v'_R \equiv v_R(t-\Delta t) \) \hspace{1cm} \Rightarrow \text{voltage across the resistance at time ‘t-\Delta t’}
\( v \equiv v(t) \) \( \Rightarrow \) total RLC voltage at time 't'

\( v' \equiv v(t-\Delta t) \) \( \Rightarrow \) total RLC voltage at time 't-\Delta t'

\( e_{hL} \equiv e_{hL}(t) \) \( \Rightarrow \) inductance history source voltage at time 't'

\( e_{hC} \equiv e_{hC}(t) \) \( \Rightarrow \) inductance history source voltage at time 't'

\( e_{eq} \equiv e_{eq}(t) \) \( \Rightarrow \) equivalent history source voltage at time 't'

\( h_{eq} \equiv h(t) \) \( \Rightarrow \) equivalent history source value at time 't'

The history sources for the trapezoidal rule of integration are:

\[
e_{hL} = \frac{2L}{\Delta t} i' + v_{L}'
\]

\[
e_{hC} = -\frac{\Delta t}{2C} v_{C}'
\]

(3-4)

The resistances obtained in Fig. 3-3(b) can be added to give an equivalent resistance. Adding the individual sources also produces an equivalent source. The result is in Fig. 3-4.

![Equivalent circuit diagram](image)

**Fig. 3-4.** Discrete-time equivalent for a RLC filter.

The values and the expressions for the equivalent elements are presented in Table 3-3. The same procedure can be repeated using the backward Euler integration rule to obtain the circuit of Fig. 3-4 with different values for the equivalent elements (also shown in Table 3-3).
Table 3-3. Element values and expressions for the RLC filter in the discrete-time domain.

3.1.3.2. Parallel RL in series with C

For the filter of Fig. 3-2(b), the discrete-time equivalents for the resistance and the inductance connected in parallel are first combined into a single one, and then are added to the capacitance equivalent to generate the discrete-time equivalent for this filter. The steps are presented in Fig. 3-5.
Fig. 3-5. Steps for the derivation of the discrete-time equivalent of Fig. 3-2(b).

As it may be expected, the values for the equivalent depend again on the integration rule (see Table 3-4).
TRAPEZOIDAL RULE

\[ i = v \frac{G_{eq}}{R_{eq}} + h_{eq} \quad \quad h_{eq} = \left[ A v' + B v_c' + C i' \right] \]

\[ G_{eq} = \frac{1}{R_{eq}} \quad \quad R_{eq} = \left( \frac{1}{R + \frac{\Delta t}{2C}} + \frac{\Delta t}{2C} \right) \]

\[ A = G_{eq} \left[ \frac{\Delta t - 1}{2L \cdot R} \right] + \frac{\Delta t}{2L + R} \quad B = -G_{eq} \left[ \frac{\Delta t - 1}{2L \cdot R} \right] + 1 \quad C = G_{eq} \left[ \frac{1}{\left( \frac{1}{R + \frac{\Delta t}{2C}} \right)} - \frac{\Delta t}{2C} \right] \]

\[ v_c = \frac{\Delta t}{2C} (i + i') + v_c' \]

BACKWARD EULER RULE

\[ i = v \frac{G_{eq}}{R_{eq}} + h_{eq} \quad \quad h_{eq} = \left[ A v' + B v_c' + C i' \right] \]

\[ G_{eq} = \frac{1}{R_{eq}} \quad \quad R_{eq} = \left( \frac{1}{R + \frac{\Delta t}{L}} + \frac{\Delta t}{C} \right) \]

\[ A = G_{eq} \left[ -\frac{1}{R} \frac{1}{\Delta t} \frac{\frac{1}{L}}{R} \right] \quad B = G_{eq} \left[ \frac{\frac{1}{R}}{\Delta t + \frac{1}{R}} \right] - 1 \quad C = G_{eq} \left[ \frac{1}{\left( \frac{1}{R + \frac{\Delta t}{L}} \right)} \right] \]

\[ v_c = \frac{\Delta t}{C} i + v_c' \]

Table 3-4. Equations for the high pass filter in the discrete-time domain.
3.1.4. Semiconductors

The semiconductor devices commonly used in HVDC systems and FACTS devices are diodes, thyristors and GTOs. Thyristors and GTOs are used to control the transfer of electric energy by behaving as controlled switches.

Among the available computer models for semiconductors, the one to use depends on the level of detail desired during the simulation. For power converters, an ON/OFF switch is generally sufficient for the analysis of the transferred energy and for the study of the behaviour of voltages and currents in the converter. In this case, the semiconductor may be visualized as an ideal or quasi-ideal switch. Semiconductor designers, on the other hand, often require the use of more detailed models than those commonly used in EMTP simulators.

The original EMTP and different EMTP-type programs such as MicroTran use ideal switches. In these programs, each switch in the circuit is defined between two network nodes. If a switch closes, the two nodes collapse forming a common node. The program then reduces the order of the admittance matrix. If the switch opens, the nodes are separated, and the order of the matrix is now increased [18].

In addition, when modelling diodes, appropriate voltage polarity is checked for closing the switch, and zero crossing of the current is checked when opening. When the device is a thyristor, a firing signal must also be present to allow switch closing. GTO’s forced commutation is achieved by comparing the current with a very large value (normally many times higher than the order of magnitude found in the circuit). Once the order to open has been given, opening takes place if this value is larger than the current [18].
Another approach for switch modelling uses a variable resistance with a high value when the switch is opened and a low value when the switch is closed. Collapsing of nodes is not necessary in this case, thus maintaining the dimensions of the conductances matrix constant. A high/low variable inductance is a variant to this approach [94].

When switches are modeled as ON/OFF binary elements, a switching operation modifies the admittance matrix. This requires a new matrix factorization or matrix inversion depending on the solution algorithm.

As an attempt to improve the solution speed, [34] and [82] model a switch as an inductor/capacitor that has the same resistance value in the discrete-time equivalent for both states (open and closed). For a given Δt, a small value for the inductance in the ON state provides the required capacitance value for the OFF state. Since the inductance and capacitance equivalents are reciprocal, a small inductance provides a low impedance and the corresponding capacitance value gives a large impedance. This is an excellent approach because it keeps the conductance matrix constant despite the switch status and only the history source expression needs to be changed. This author has tried this technique but ran into the problem of choosing the inductor and capacitor values that would meet appropriate impedance values for the modelling of HVDC converters. In these cases, the required value of the inductor/capacitor to present an appropriate low/high impedance requested in values comparable with other impedances in the system in the system.

In this thesis, the representation of diodes and thyristors as low/high resistances is adopted. This keeps the number of nodes constant and translates into less programming effort. It maintains the same network topology during the entire simulation, thus saving the computational time.
needed to reduce or increase the system matrix when using ideal switches. The HVDC cases simulated with this model were successfully compared with MicroTran, which also uses ideal switches to represent semiconductor valves.

The problems that arise in a circuit when modelling GTO thyristors are solved with the exploratory solution algorithm proposed in section 5.1.

3.1.4.1. Diodes

Fig. 3-6 shows the diode symbol and the parameters included in its model. The diode current is given by,

\[ i_D(t) = \begin{cases} g_{on}v_D(t) & \text{for the ON state} \\ g_{off}v_D(t) & \text{for the OFF state} \end{cases} \]

\[ (3-5) \]

\[ i_D \]

\[ \text{anode (A)} \quad \text{cathode (K)} \]

\[ + \quad v_D \quad - \]

DIODE PARAMETERS
- \( R_{ON} \): Resistance value for ON state
- \( R_{OFF} \): Resistance value for OFF state
- \( G_{ON} \): Conductance value for ON state (\( G_{ON} = 1/R_{ON} \))
- \( G_{OFF} \): Conductance value for OFF state (\( G_{OFF} = 1/R_{OFF} \))
- \( I_H \): Holding current
- \( V_{THR} \): Threshold voltage

Fig. 3-6. Diode symbol and model parameters.

To model the changes of state in the diode, the steps from Table 3-5 are applied at the end of each step of the solution.
1. If diode state is ON and $i_D(t) < \text{Holding Current} (I_H) \rightarrow$ change to OFF state
2. Else if diode state is OFF and $v_D(t) \geq \text{Threshold Voltage} (V_{THR}) \rightarrow$ change to ON state

Table 3-5. Procedure to check and change the state of a diode.

As a result, the characteristic of the model is that of Fig. 3-7(a), which is parameter dependent. The transition when the switch closes is shown in Fig. 3-7(b), and the transition when it opens is in Fig. 3-7(c).

Fig. 3-7. Diode model:
(a) V-I characteristic. (b) Turn on transition. (c) Turn off transition.
3.1.4.2. Thyristors

To a certain extent the thyristor and the diode models are similar. The thyristor symbol and parameters are shown in Fig. 3-8.

Compared to the diode, the thyristor has two more attributes, both of which we need to include in its model: first, to turn on, a thyristor must have a firing signal applied to its gate terminal; second, after conduction, a thyristor requires a period of time $t_q$ to recombine the internal charges before operating in the blocking state. If the device voltage becomes positive before the internal charges have recombined totally, the thyristor will conduct again with or without the presence of a firing signal. This event, which may lead to undesired reclosure of a thyristor, is known as *commutation failure*.

The extinction angle is a quantity used to measure and prevent the occurrence of a commutation failure. It is defined as the time interval (converted to electrical degrees) between the instant that the current crosses zero and the instant at which the thyristor voltage becomes positive. The algorithm for updating states in a thyristor is presented in Table 3-6 and the modeled thyristor characteristic is presented in Fig. 3-9.

The calculation of the extinction angle is performed in the computer code. An integrator is started when a thyristor opens. If the time value that the integrator has when the opened thyristor’s voltage becomes positive is smaller than the recombination time $t_q$ the thyristor is closed again (this is not shown in the characteristic of Fig. 3-9).
THYRISTOR PARAMETERS

- $R_{ON}$: Resistance value for ON state
- $R_{OFF}$: Resistance value for OFF state
- $G_{ON}$: Conductance value for ON state ($G_{ON} = 1/R_{ON}$)
- $G_{OFF}$: Conductance value for OFF state ($G_{OFF} = 1/R_{OFF}$)
- $I_H$: Holding current
- $V_{THR}$: Threshold voltage
- $t_q$: Minimum recombination time

Fig. 3-8. Thyristor symbol and parameters.

Fig. 3-9. Thyristor characteristic.

1. If thyristor state is ON and $i_T(t) < $ Holding Current ($I_H$) → change to OFF state
2. Else if thyristor state is OFF and $v_{AK}(t) \geq $ Threshold Voltage ($V_{THR}$), then
   If a firing signal ($i_g$) is present and the extinction angle $\geq t_q$ → change to ON state

Table 3-6. Procedure to check and change the state of a thyristor.
3.2. Zero Crossing Detection

The transient solution relies on the integration method, on the time step, and on how closely the device models reproduce the behaviour of the physical devices.

Diodes and thyristors open at the time instant at which the current crosses zero. Since the transient simulation is performed at discrete time steps, the exact instant at which the current becomes zero rarely coincides with an evaluated instant. The detection of a zero crossing event occurs at the end of the time interval at which the current crossed zero, and the network is not solved with the switch (diode or thyristor) open until the following time step. This generates a delay of up to two time steps between the instant at which the switch should have opened and the instant at which the simulator does open the switch.

Fig. 3-10(a) depicts the traditional procedure for opening a switch when using a fixed time-step pattern (assuming a null value for the holding current parameter \(I_{H}\)). At point 1, the switch is at its conducting state. Since the current is positive, the state is not changed. When the current crosses zero (point 2), the algorithm changes the switch to its off state. However, the solution at point 2 has already been obtained with the switch closed. It is not until point 3 that the system is solved with the switch open for the first time during this transition. To avoid numerical oscillations, it is recommended to use CDA after a switching event. The solution for the opening of the switch using CDA is illustrated in Fig. 3-10(b).

The closing of a switch has also slight imprecisions. The instant at which the voltage exceeds the threshold value does not necessarily coincide with an obtained solution. Moreover, when working with thyristors the origination of a firing signal will probably occur between two simulation steps, thus delaying the closure of the switch.
1. switch closed (current is positive → no action)
2. switch closed (polarity changed detects zero crossing → switch will open at next Δt)
3. 1\textsuperscript{st} solution with switch opened
4. solution continues with switch opened until switch voltage becomes positive

Fig. 3-10. Switch current for the opening transition in traditional EMTP simulators:
(a) Trapezoidal rule for all points (b) CDA algorithm at switching events.
A diode voltage for the off-to-on transition of a switch is illustrated in Fig. 3-11 (we assume a zero value for the threshold voltage $V_{\text{THR}}$). The diode is open at points 1 and 2. At point 2, however, the voltage has become positive, and the diode changes to the on state for point 3.

![Diode Voltage Diagram](image)

1. switch opened (voltage is negative → no action)
2. switch is still opened (positive polarity zero crossing → switch will close at next $\Delta t$)
3. 1st solution with switch closed
4. solution continues with switch closed until next switching event

Fig. 3-11. Diode voltage during the closing transition with a fixed time-step scheme.

Corrective measures to overcome these slight deviations include the use of a smaller time step, the application of variable time-step algorithms, and the utilization of interpolation techniques.

The uncertainties produced by switching operations in the discrete-time domain become important when modelling thyristors in HVDC and FACTS devices, as they may produce
improper results and lack of control precision. Clear examples and suggestions to diminish their effects are neatly presented in [4] and [49].

The use of linear interpolation, as presented in [4], brings the solution closer to reality because the interpolated opening time will be nearer to the actual zero crossing. The solution output though, is no longer obtained at fixed time steps introducing a dynamic change in the time intervals.

In Fig. 3-12, the switch is assumed to be originally closed at point 1. If we use a fixed simulation time step, we find that the next solution (point 2) is negative. This signals that the current has crossed zero at some instant in between points 1 and 2. With the solution at these two points, linear interpolation allows us to find point 3. Point 2 can now be neglected, allowing us to resume the analysis with the original time step and with the switch open to find point 4, and then continuing until the next switching event. It is clear from Fig. 3-12 that the solution points are no longer at fixed time intervals.
At time 4, the solution is now known at zero crossing. 2 (not an output value)

1. switch closed (current is positive → no action)
2. switch closed (current is negative → interpolate points 1 & 2 and negelect 2)
3. result from interpolation of points 1 & 2 (switch closed)
4. first solution in this transition with switch opened and original time step
5. solution continues with original time step

Fig. 3-12. Switch current transition with linear interpolation.

Numerical oscillations will most likely arise when a switch opens. To eliminate them, Kuffel, Kent and Irwin [49] used an extra ½ step interpolation whereas Araujo, Martí and Dommel [4] opted for the always stable and well proven CDA algorithm [66].

Let us recognize that the methods described above improve the accuracy of the numerical solutions. Let us also focus our attention to the circumstance that the time intervals are non-uniform. The non-uniformity of the time intervals can actually be an important issue in real-time simulators.

As an example, assume a 50 μs time step. If point 3 in Fig. 3-12 is too close to point 1, say at only 5 μs, the solution for points 2 and 3 needs to be ready in less than 5 μs. If we had a “super computer” that was able to solve points 2 and 3 in the required 5 μs, we still would be achieving
real-time. What if the distance between point 1 and 3 were only 1 μs? or 0.5 μs? or 0.1 μs? or …?

Of course, it was easy to take the above example to an extreme. There are yet other consequences emerged as a result of the variable time interval.

A real-time simulator is expected to generate output values. Suppose, for example that the output device is a simple oscilloscope. The real-time simulator and the oscilloscope need to establish an intercommunication by an appropriate interface. This communication requires two important factors: timing and synchronization. Both factors have limitations and implementation difficulties. If the data exchange between the external device and the real-time simulator is performed at constant time intervals, the synchronization is made simpler: both devices can work independently, knowing the time frame that each one has to perform its tasks before the next data exchange occurs. Other examples of output devices are: an equipment under testing (such as a controller or a protective relay), an analog simulator, another digital simulator, a real power system, another computer processing another area of the power system in parallel, etc.

The discussion above has been presented to emphasize both the importance and the benefits of having a constant interval for output. The solution to this problem (in the zero crossing detection scheme) is straightforward and only requires an extra linear interpolation or extrapolation calculation.

Fig. 3-13 annexes points 6 and 7 to the solution presented in Fig. 3-12. In this case, points 4 and 5 are the two backward Euler ½ time steps that CDA requires. Point 6 is the final interpolation or extrapolation to synchronize the solution back to the original time increment. Point 7 resumes the simulation with the trapezoidal rule of integration.
Solid circles are output points at equal intervals

Blank squares are only evaluated and are not output points

1. switch closed (current is positive $\Rightarrow$ no action)
2. switch closed (current is negative $\Rightarrow$ interpolate points 1 & 2 and negelect 2)
3. result from interpolation of points 1 & 2 (switch closed)
4. 1st backward Euler $\frac{1}{2}$ step solution (first solution with switch open).
5. 2nd backward Euler $\frac{1}{2}$ step solution
6. result from interpolation of points 4 & 5 (resynchronized to original time step)
7. solution continues with original time step and trapezoidal

Fig. 3-13. Diode current with complete interpolation algorithm plus synchronization.

Table 3-7 summarizes the complete algorithm for the detection of zero crossing\(^1\) and synchronization with the original time increment.

Fig. 3-14 shows a simulation comparing the proposed interpolation scheme with the solution when using CDA. The proposed technique does not show spikes at switching events. The plot corresponds to the current of one thyristor of a three-phase bridge that is feeding a predominantly inductive load.

\(^1\) If modelling semiconductors, it may be adequate to use the holding current ($I_H$) or threshold voltage ($V_{THR}$) parameters as the values for crossing detection. The same interpolation scheme is also valid to improve HVDC controllers accuracy.
Table 3-7. Algorithm for zero crossing detection and synchronization.
Fig. 3-14. Thyristor current in a rectifier:
(a) Interpolation scheme II. (b) CDA (MicroTran).

Table 3-8 establishes a comparison of the computational effort between EMTP, CDA without zero crossing adjustment, the method suggested in [49], and the approach proposed here (fourth column).

<table>
<thead>
<tr>
<th></th>
<th>EMTP</th>
<th>CDA (MicroTran)</th>
<th>Interpolation scheme I</th>
<th>Interpolation scheme II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of solutions</td>
<td>3 Trapezoidal</td>
<td>2 Trapezoidal &amp; 2 B. Euler</td>
<td>5 Trapezoidal &amp; 2 B. Euler</td>
<td></td>
</tr>
<tr>
<td>Number of interpolations</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Numerical oscillations?</td>
<td>yes</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>Negative current?</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
</tbody>
</table>

Interpolation scheme I: Corresponds to the one presented in [49].
Interpolation scheme II: Corresponds to the one studied in this section.

Table 3-8. Comparison between EMTP, CDA, and interpolation schemes for 3 time steps during a switching action.
3.3. The Multi-Area Thévenin Equivalent Algorithm (MATE)

The compensation method used in the EMTP [17], [20] is extended in [62] to subdivide a network into independent subsystems that can be solved separately. Current injections between Thévenin equivalents interconnect the subsystems and determine the combined network solution.

The MATE algorithm is reviewed in Appendix A. Because the methodology is general, it can be used to subdivide a network at any point and in as many subsystems as desired. One or more “links” are inserted at each point where the network is to be split into two independent subsystems. For the purposes of the MATE methodology, the definition of a link is a device that has two states and is somehow similar to an ideal switch. The link, however, serves as a tie between two subsystems and is not part of the solution of either one.

With the MATE concept, equation (3-2) is used to apply nodal analysis to each subnetwork with all the links in their open state. Finally, the link currents needed to interconnect the subsystems are obtained from Thévenin equivalents as seen from the link terminals. Using these equivalents, the link currents are injected into each subsystem to modify all the voltages accordingly.

Similarly to the transmission line model, MATE presents the advantage of splitting a circuit into independent subnetworks. The price is the additional expense of evaluating the link currents and performing the corresponding current injections. The example of Fig. 3-15 shows how both, transmission lines and MATE, divide a system’s admittance matrix into decoupled submatrices.
Fig. 3-15. Network subdivided by links and transmission lines.

**General case: M links connecting N areas**

If we study with detail the examples presented in Appendix A, we will be able to formulate the equations directly from the circuit. As an example, let us generate the equations for the 4-area 7-link system presented in Fig. 3-16. Assume that area 1 has 3 nodes, area 2 has 3 nodes, area 3 has 4 nodes and area 4 has 4 nodes.
If we select two links at a time, we can either have them connecting two or three areas. If the chosen pair does not connect two consecutive areas, it does not contribute to the solution. This produces:

\[
Z_{\text{links}} = \begin{bmatrix}
  Z_{11}^{41} + Z_{12}^{42} & Z_{11}^{41} + Z_{12}^{42} & -Z_{11}^{42} & -Z_{12}^{42} & 0 & 0 & 0 \\
  Z_{11}^{41} + Z_{12}^{42} & Z_{11}^{41} + Z_{12}^{42} & -Z_{11}^{42} & -Z_{12}^{42} & 0 & 0 & 0 \\
  -Z_{11}^{42} & -Z_{12}^{42} & Z_{13}^{42} + Z_{14}^{43} & Z_{13}^{42} + Z_{14}^{43} & Z_{11}^{43} & Z_{12}^{43} & Z_{13}^{43} \\
  -Z_{11}^{42} & -Z_{12}^{42} & Z_{13}^{42} + Z_{14}^{43} & Z_{13}^{42} + Z_{14}^{43} & Z_{11}^{43} & Z_{12}^{43} & Z_{13}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} + Z_{14}^{44} & Z_{13}^{43} + Z_{14}^{44} & Z_{11}^{44} + Z_{12}^{44} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} + Z_{14}^{44} & Z_{13}^{43} + Z_{14}^{44} & Z_{11}^{44} + Z_{12}^{44} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} + Z_{14}^{44} & Z_{13}^{43} + Z_{14}^{44} & Z_{11}^{44} + Z_{12}^{44} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} + Z_{14}^{44} & Z_{13}^{43} + Z_{14}^{44} & Z_{11}^{44} + Z_{12}^{44} \\
\end{bmatrix}
\]

\[
E_{\text{links}} = \begin{bmatrix}
  E_{11}^{41} & E_{11}^{41} \\
  E_{12}^{41} & E_{12}^{41} \\
  E_{13}^{41} & E_{13}^{41} \\
  E_{14}^{41} & E_{14}^{41} \\
  E_{21}^{42} & E_{21}^{42} \\
  E_{22}^{42} & E_{22}^{42} \\
  E_{23}^{42} & E_{23}^{42} \\
  E_{24}^{42} & E_{24}^{42} \\
\end{bmatrix}
\]

\[
\Delta E_{\text{links}} = \begin{bmatrix}
  E_{11}^{41} - E_{11}^{41} \\
  E_{12}^{41} - E_{12}^{41} \\
  E_{13}^{41} - E_{13}^{41} \\
  E_{14}^{41} - E_{14}^{41} \\
  E_{21}^{42} - E_{21}^{42} \\
  E_{22}^{42} - E_{22}^{42} \\
  E_{23}^{42} - E_{23}^{42} \\
  E_{24}^{42} - E_{24}^{42} \\
\end{bmatrix}
\]

\[
\hat{Z} = \begin{bmatrix}
  Z_{11}^{41} & Z_{11}^{41} & 0 & 0 & 0 & 0 & 0 \\
  Z_{11}^{41} & Z_{11}^{41} & 0 & 0 & 0 & 0 & 0 \\
  Z_{11}^{41} & Z_{11}^{41} & 0 & 0 & 0 & 0 & 0 \\
  Z_{11}^{41} & Z_{11}^{41} & 0 & 0 & 0 & 0 & 0 \\
  Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{12}^{42} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
  0 & 0 & -Z_{11}^{43} & -Z_{12}^{43} & Z_{13}^{43} & Z_{13}^{43} & Z_{14}^{43} \\
\end{bmatrix}
\]

(3-6)
This result can be corroborated following the procedure presented in Appendix A, and the system solution can be obtained from the algorithm presented in Table 3-9.

1. **Divide any given network in M areas** $A_1, A_2, ... A_M$.

2. **Interconnect areas with L links with a link as in Fig. A-3 (from Appendix A).**

3. **Form admittance matrices** $Y^{A_1}, Y^{A_2}, ..., Y^{A_M}$ and obtain the corresponding inverse matrices $Z^{A_1}, Z^{A_2}, ..., Z^{A_M}$. Form matrices $Z_{\text{links}}$ and $\hat{Z}$ by row elimination as for the 2 areas example in Eq. A-4 and in Eq. A-5, or by direct inspection.

4. **Solve areas separately using Eq. 3-2 with links opened. This produces the Thévenin vector voltage** $E_{\text{links}}$ **needed in steps 5 and 6.**

5. **Obtain matrix** $Z_{\text{links}}$ **and solve for the link currents using Eq. A-8.**

6. **Inject vector** $i_{\text{links}}$ **using Eq. A-9 to obtain the final solution.**

Table 3-9. Generalized MATE algorithm.

The Multi-Area Thévenin Equivalent Algorithm (MATE) is one of the approaches presented in the next chapter to attempt modelling HVDC converters in real time.
The large number and frequency of switching operations that take place in power electronic converters originate numerical difficulties that require supplementary computational effort. In the previous chapter, the use of CDA and zero crossing detection helped to eliminate the arising oscillations and reduce the resulting inaccuracies.

To overcome the subsequent increase of computational time, it is necessary to study other aspects of the solution algorithm that effectively reduce the number of operations.

For example, if at a certain time step an element’s equivalent conductance changes, the admittance matrix also changes. As a result, the new solution requires a matrix refactorization or a matrix inversion. Due to the involved number of multiplications, this is probably one of the most time consuming tasks during the transient simulation.

One solution to the system matrix recalculation problem is to precalculate and prestore all possible matrix combinations. This option, however, is not always practical, particularly when there is a large number of varying elements in the circuit.

The two HVDC models presented in this chapter use the criterion of prestoring the system matrices. However, the approaches permit the sectionalizing of the network in such a way that the number of prestored matrices is relatively low.

Before describing the two models, it is worthwhile to gain familiarity with the modelling requirements of HVDC converters.
4.1. The High Voltage Direct Current Substation

The operation of HVDC substations has been extensively studied through the years and the analytical details can be found in [6], [78]. This section briefly reviews the components in an HVDC substation and discusses some considerations for electromagnetic transient simulations.

The basic components that make up an HVDC substation are converter bridges, power transformers, smoothing reactors, and filters. Fig. 4-1 shows the schematic diagram for a typical monopolar 12-pulse HVDC substation. The filters supply part of the reactive power required by the converters. In addition, shunt capacitors, synchronous condensers and static VAR systems are often used as reactive power sources depending on the speed of control desired.

---

**Fig. 4-1. Monopolar 12-pulse HVDC substation.**
4.1.1. Bridges

Each bridge in Fig. 4-1 consists of 6 valves. When the valves in a bridge are arranged as in Fig. 4-2, it is named a Graetz Bridge. A valve is used to switch in a segment of an AC voltage waveform. The term valve originates from the mercury arc valves used in the original HVDC bridges. Nowadays thyristors are grouped in series and parallel to form a thyristor valve. Commonly, HVDC applications use only series connected thyristors.

![Diagram of Graetz bridge and symbol](image)

Fig. 4-2. Graetz bridge and symbol.

Bridges control the electrical energy transferred between AC and DC sides by adjusting the firing angle $\alpha$ at which the valves are fired. The firing angle parameter is normally measured from the instant at which valve T1 is able to be fired (when its voltage crosses zero becoming positive). In a 6-pulse converter, each subsequent valve is fired at 60° intervals to maintain the AC system balanced in steady-state operation. For a 12-pulse converter the intervals are spaced 30°. The thyristor numbers in Fig. 4-2 correspond to the firing signals sequence (T1, T2, ..., T6).

The bridge’s operation mode determines the power flow direction. A bridge operating as a rectifier transfers energy from the AC side to the DC side. The same bridge in inverter mode transfers energy from the DC side to the AC side.
Fig. 4-3. A 6-pulse HVDC converter feeding a passive load.

However, the AC to DC conversion is far from ideal and harmonics arise on both AC and DC sides. To illustrate this consider the 6-pulse bridge of Fig. 4-3 operating as a rectifier in steady-state and feeding a passive load. Fig. 4-4 shows the AC and DC waveforms and the corresponding Fourier spectrum for a 15° firing angle.

4.1.2. Smoothing reactors

A large reactor installed in series with the bridge output terminals provides DC current smoothing and protection. This linear reactor is therefore named "smoothing reactor" (the inductance connected in series with the bridge in Fig. 4-3). Fig. 4-5 shows the smoothed DC current provided by the smoothing reactor. If the smoothing reactor was not present, the current waveform would be equal to the voltage waveform, thus increasing the current ripple.
Fig. 4-4. Rectified DC voltage and AC phase-a current including their corresponding harmonics for the circuit of Fig. 4-3.

Fig. 4-5. Effect of the smoothing reactor in the DC current.
4.1.3. Converter transformers

Three single-phase two-winding units form a three-phase converter transformer. For 12-pulse operation, two three-phase transformers connected in Y-Y and Y-Δ feed two series connected bridges (Fig. 4-6). In both cases the AC side neutral is solidly grounded. Sometimes, single-phase three-winding transformers or three-phase transformers are used. The transformer’s design should consider DC voltage stresses and DC magnetization due to unsymmetric firing and increased eddy current losses provoked by high order harmonics. Additionally, the leakage reactance’s design limits short circuit currents.

![Fig. 4-6. A 12-pulse HVDC converter feeding a passive load.](image-url)
Fig. 4-7. Operation of the 12-pulse bridge.
The 30° phase shift provided by the Y-Δ transformer allows 12-pulse operation. In this type of operation the firing is alternated between the two bridges (i.e., T1, T1', T2, T2', etc.). Because the bridges are connected in series, the sum of the phase-shifted rectified voltages produces a 12-pulse DC voltage as demonstrated in Fig. 4-7. Also shown in this figure is the benefits in the harmonic content for 12-pulse operation (compare Fig. 4-4 with Fig. 4-7). Passive filters installed on both AC and DC sides reduce the effects of the higher order harmonics.

4.1.4. Filters

Filters for AC and DC sides are passive circuits that provide low impedance paths for harmonics (review the filters location in Fig. 4-1). With an appropriate design and location, filters confine harmonics to the substation boundaries and avoid their flow to the rest of the system. Fig. 4-8 shows two filter configurations commonly used in HVDC systems.

Tuned filters eliminate specific harmonics, and high pass filters filter out higher order harmonics that might exist above the HVDC operational switching frequency. For details on filter design for HVDC systems please refer to [78].

Fig. 4-9 illustrates the reduced harmonic content in the AC current for the complete 12-pulse HVDC substation when installing one single tuned filter per phase for the 11th harmonic, one single tuned filter per phase for the 13th harmonic, and one second order high pass filter per phase for higher order harmonics (20th and above). The original AC current harmonic distortion factor (THD) has been reduced from 29.5% for the 6-pulse converter (Fig. 4-4) to 2% for the 12-pulse converter substation (including transformers and filters, Fig. 4-9).
Fig. 4-8. Filter configurations and frequency response.

Fig. 4-9. Phase-a line current when installing AC filters.
4.1.5. Controllers

HVDC systems have the advantage of permitting a fast controllability of transmitted power. The controls also offer reliable protection during the presence of faults. Modern controllers use high speed microprocessors for many of the control functions.

In an HVDC link, the rectifier is commonly operated at constant current, and the inverter at minimum extinction angle. This facilitates the protection against line faults, and produces a better voltage regulation [78].

The most widely used firing angle control in HVDC converters is the equidistant pulse control [2], [6], [22], [78]. The controlled variable (dc current or extinction angle) is measured and compared to a reference set point value (this deviation is named error). The error is applied to a control amplifier, which generates a corrective order. In many instances, this controller rectifier is a proportional integral controller. Then a voltage controlled oscillator and a ring counter alter the firing angle trying to eliminate the error. Fig. 4-10 shows the block diagram of the equidistant controller scheme.
The controlled oscillator is essentially a pulse generator. It consists of a ramp function with a frequency proportional to the AC system frequency. When the ramp reaches its peak value, it generates a pulse that is fed into a ring counter and used to fire the next valve. In steady state operation, the pulses are equidistant. When an error exists, the reference value of the ramp is changed (as shown in Fig. 4-11), changing the distance between pulses until a new steady state is reached.

The firing angle control constitutes only one of the many components of a practical HVDC controller. It is beyond the scope of this thesis to model a complete controller. To get a panorama of some controller implementations in digital simulators, the reader is encouraged to consult references [8], [15], [37], [45], [55], [57], [80], [81], and [102].
Fig. 4-11. Voltage controlled oscillator:
(a) Steady-state. (b) Idc>set point → error>0 and Uc>0.
4.2. HVDC Model I - The HVDC Object

In chapter 3 we studied methodologies for the discrete-time solution of electrical circuits and we reviewed the discrete-time equivalents for the various elements of an HVDC substation. We also discussed some of the numerical difficulties that power electronics circuits have and possible solutions.

This section addresses the problem of changing the admittance matrix after a switching operation and proposes a new way to solve an electrical network containing several HVDC converters. The strategy for fast solutions is based on both, the precalculation of a certain amount of matrices, and the appropriate formulation of the system solution. The result is a discrete-time model for an HVDC converter that produces a noticeable reduction of the computational time required to solve the network.

In a recent conference in Montréal, Kelper, Dessaint, Do, and Sybille [43] presented a real-time simulator for a 6-thyristor converter precalculating and storing the 64 possible matrices resulting from all the possible combinations of the valve states. However, they did not present an algorithm to allow the inclusion of more than one bridge without including the entire number of combinations of valve states: $2^n$, where $n$ equals the number of valves.

In the approach proposed in this section, it is possible to store only 64 combinations for each 6-valve bridge, and then combine the bridges to obtain the system solution with simulation times that are adequate for real-time simulation.
4.2.1. The HVDC Object Definition

The first step in this development is to define a subcircuit with elements that are common to typical HVDC substations. We will name this subcircuit the *HVDC Object*. It is obvious that different Object definitions are feasible; the one presented here is only one particular case.

Consider an HVDC Object containing the elements indicated in Fig. 4-12. The Object’s core is the 6-pulse bridge; the transformer can be connected in Y-Y or Y-Δ, and the smoothing reactor is optional.

The discrete-time models for each of the elements were detailed in Chapter 3. The bridge valves are modeled as thyristors, the transformers consist of three single-phase units, and the smoothing reactor is modeled as an inductance.

To review the different discrete-time models available, please refer to Tables 3-1 and 3-2. Diodes and thyristors are modeled with a conductance that can have two values. Inductors and capacitors consist of a fixed conductance in parallel with a history current source. Transformers and transmission lines have conductance matrices and history source vectors. Although the filters are not included in the HVDC Object, they can be incorporated without difficulties using the filter models presented in Tables 3-3 and 3-4. The object in Fig. 4-12 does not contain reactive
power sources either; in the case of using SVCs, they can be modeled as proposed in the next chapter.

The discrete-time equivalent for an HVDC Object developed here has a conductance matrix (with 64 possibilities) and a history source vector.

Associated with the HVDC Object there are 64 states resulting from all the possible valves' combinations\(^2\).

At this point, it is important to emphasize the feasibility and convenience of storing the 64 possible matrices in the computer memory, before the beginning of the transient analysis loop. Since the Object defined in Fig. 4-12 has only up to 9 nodes, the number of elements in the Object's conductance matrix for one state is 81. The RAM required to store the 64 combinations is approximately 20 Kbytes when using double precision.

The HVDC Object of Fig. 4-12 has 5 external nodes that are used as terminals to connect it to an external network. The number of internal nodes varies from 3 to 5 depending on the transformer connection and on the presence of the smoothing reactor. As long as the filters are modeled as proposed in subsection 3.1.3, the number of nodes is not affected when AC and DC filters are included in the object.

---

\(^2\) Each valve has 2 positions (ON and OFF) giving 2^6 combinations.
The nodal analysis representation of an electrical network in the discrete-time domain [65] is of the form:

\[ G v = i - h \] (4-1)

where:
- \( G \) is the conductance matrix at time \( t \)
- \( v \) is the voltages vector at time \( t \) (for both external and internal nodes)
- \( I \) is the independent current sources vector (the HVDC object does not have any)
- \( h \) is the history sources vector at time \( t \)

The contribution of an HVDC Object based on (4-1) can be written as:

\[
\begin{bmatrix}
G_{xx} & G_{xy} \\
G_{yx} & G_{yy}
\end{bmatrix}
\begin{bmatrix}
v_x \\
v_y
\end{bmatrix}
= 
\begin{bmatrix}
-h_x \\
-h_y
\end{bmatrix}
\] (4-2)

The matrix contribution has been partitioned in external and internal nodes (subindex ‘x’ denotes external nodes and subindex ‘y’ denotes internal nodes).

Assume that at time \( t \) the external voltages \( v_x \) are known. The internal voltages for time \( t \) can be found from (4-2) as follows:

\[ v_y = -G_{yy}^{-1}(h_y + G_{yx}v_x) \] (4-3)

The new state of the valves can now be determined. For each closed valve, zero current crossing is checked to decide if that valve needs to be opened for the next solution step. To close open valves, voltage polarity needs to be positive and a firing signal generated by the converter.
controller must be present at the gate terminal. The new state determines the Object’s matrices \( G_{xx}, G_{xy}, G_{yx}, \) and \( G_{yy} \) to be used at time \( t+\Delta t \).

The electrical network to which the HVDC Object is connected does not require to know the internal Object details. For the global solution, each HVDC Object appears as a block with a discrete-time equivalent consisting of an equivalent conductance matrix \( G_{eq} \) and an equivalent history source vector \( h_{eq} \). Since the object defined in Fig. 4-12 has 5 terminals, \( G_{eq} \) and \( h_{eq} \) are of order 5. The discrete-time equivalent seen by the external system is found by obtaining a relationship between external voltages \( v_x \) and the equivalent history source vector \( h_{eq} \) from the following procedure.

From (4-2) we rewrite the first row

\[
G_{xx} v_x + G_{xy} v_y = -h_x
\]

(4-4)

Secondly, we substitute (4-3) in (4-4) and solve for \( v_x \) to obtain the discrete-time equivalent for the HVDC Object:

\[
G_{eq} v_x = -h_{eq}
\]

(4-5)

where:

\[
G_{eq} = G_{xx} - G_{xy} G_{yy}^{-1} G_{yx}
\]
\[
h_{eq} = h_x - G_{xy} G_{yy}^{-1} h_y
\]

(4-6)
To obtain the complete solution of the network, the elements of the equivalent matrix $G_{eq}$ are properly inserted in the system's admittance matrix, and the currents of the equivalent history vector $h_{eq}$ are inserted into the system's currents vector at the nodes corresponding to the Object's external nodes. Fig. 4-13 illustrates the insertion of $G_{eq}$ into the system's $G$ for a particular Object state.

Fig. 4-13. Inserting one of the 64 HVDC Object's matrices into the network matrix.

4.2.2. Solution of a Network containing HVDC Objects

As an archetype, Fig. 4-14 presents a 24-valve system fragmented into 4 HVDC Objects. The system represents a 12-pulse bipolar HVDC converter substation (the bipolar version of the one shown in Fig. 4-1). Note that the HVDC Objects do not need to be identical, and that a load has been inserted at each DC output.
The network of Fig. 4-14 can be seen as a 10-node circuit containing 2 load resistances (DC system), 3 inductances, 3 resistances and 3 voltage sources (AC system), 3 sets of filters (AC filters and DC filters), and 4 HVDC Objects. For this case, the external elements are constant and only the HVDC Objects may change. The representation of the same network in MicroTran or EMTP would require a minimum of 31 nodes.

![Diagram of Fig. 4-14](image)

Fig. 4-14. Four HVDC Objects constituting a 24-valve, 12-pulse bipolar HVDC substation.

The simulator's *driver* is the main program that integrates the network elements and obtains the discretized transient solution at fixed time intervals.

To solve a circuit like the one presented in Fig. 4-14, the *driver* updates the circuit's conductance matrix at every time step. To do so, at any given time \( t \) the *driver* subtracts each of the HVDC Objects' matrices that were used to solve the circuit at \( t-\Delta t \), and then adds the new
HVDC Objects’ matrices (based on the updated valves’ positions). In addition, CDA is used when there is a switching operation.

Table 4-1 details the generalized algorithm to solve a network containing one or more HVDC Objects. Each HVDC Object may be physically and mathematically represented as the one proposed in the previous subsection. Remember that for each HVDC Object in the network that we intend to solve, there are 64 matrices (and related submatrices) that need to be stored and processed before the transient solution starts. Section 4.4 presents simulation results for several test cases demonstrating the solution times for this algorithm.

This algorithm presents several benefits:

1. Precalculating and prestoring the 64 matrix combinations for each object saves computational effort during the transient solution.

2. The way in which the algorithm combines the matrices of the circuit Objects presents an important advantage: “If a network has $n$ HVDC objects, only $64n$ matrices are prestored”. As an example, consider the sending end of a 24-valve HVDC converter. It is not practical to store the $2^{24}=16,772,216$ combinations that the 24 valves in the converter give. However, with the new methodology proposed here, if we define 4 HVDC Objects, we only need to precalculate and prestore 256 combinations (i.e., 4 Objects x 64 matrices/Object=256).

3. The internal Objects’ nodes are not seen by the network simulator, thus reducing the total number of nodes in the external system and the computational time required. When attempting real-time simulation, it is important to minimize the number of operations; the
number of total nodes is directly related to the size of the system's matrix, and, therefore, to the computational time required to obtain the solution.

4. The algorithm can be extended to include other devices, whenever it is feasible to predetermine the number of possible states and the related matrices.
For each HVDC Object, precalculate and prestore the Object's matrices. Assume an initial state for each Object.

Build the system's conductance matrix $G$-system with all the elements in the system except for the HVDC Objects.

Start transient analysis $t=0$.

Update the system's matrix $G$-system by including the active $G$-matrix of each HVDC Object.

Solve the network at time $t$.

For each HVDC Object, determine the valve positions and the new HVDC Object status (use the known voltages, obtain currents and check controller firing signals).

Evaluate histories for all the elements in the system.

Increment time-step: $t = t + \Delta t$.

**Increment half time-step if there is any switching event (CDA)**

Table 4-1. Generalized algorithm to solve a network containing 'n' HVDC Objects.
4.3. HVDC Model II - The MATE Approach

The second model bases its functionality on the Multi Area Thévenin Equivalent (MATE) algorithm. The theory for MATE is presented in section 3.3, and in Appendix A.

With MATE, a network containing HVDC converters can be subdivided into several areas. The areas are interconnected by the minimum possible number of links. As in the HVDC Object model, the areas containing HVDC converters have states that change according to the valves’ states (ON or OFF). By defining an appropriate segmentation of the network, the number of combinations can be kept reasonable (e.g., 64 combinations per area).

4.3.1. HVDC Converter as an Independent Area

Consider an electrical circuit containing only one 6-pulse HVDC converter. The four links inserted in Fig. 4-15 divide the circuit into three independent areas: the first area A1 contains the sources and line inductances, the second area A2 contains the HVDC substation, and the third area A3 contains the load. There are three links connecting areas A1 and A2, and one link containing areas A2 and A3. For this example, areas A1 and A3 have constant elements, and area A2 has 6 valves that cause 64 states.

We can apply the MATE algorithm with slight adjustments. The main difference with respect to the MATE, as introduced in section 3.3, is that at switching events area A2 changes. As a consequence, elements in the links matrix \( z_{\text{links}} \) need to be updated at switching events.
Fig. 4-15. Areas for a circuit containing one 6-pulse HVDC converter.

To get an efficient solution using MATE\textsuperscript{3} for this circuit, use the following procedure:

i. For each area containing changing elements, predetermine all the possible combinations before the transient solutions starts.

ii. Precalculate, preinvert and prestore in memory all the conductance matrices for each area. The inverted matrices are impedance matrices. For each area A1 and A3, there is only one matrix, whereas for area A2, there are 64 matrices.

iii. Assume an initial state for area A2 (initial conditions) and form the links’ impedance matrix $z_{\text{links}}$, using elements from the impedance matrix of area A1 and from the initial state’s impedance matrix of area A2. Factorize $z_{\text{links}}$.

iv. Start the transient analysis.

v. Solve areas A1 and A2 separately with links open. For area A2 use the correct state according to the valves’ position. Form Thévenin voltages vector $v_{\text{links}}$.

\textsuperscript{3} Refer to Appendix A for the details of MATE and the corresponding variable definitions.
vi. If in step iii the state of area A2 is different from the state in the previous time step, form and factorize the new links impedance matrix $z_{\text{links}}$.

vii. Calculate the links currents vector $i_{\text{links}}$ from $z_{\text{links}}$, $i_{\text{links}} = v_{\text{links}}$.

viii. Inject vector $i_{\text{links}}$ into areas A1 and A2 and update all the internal voltages in each area.

ix. In area A2, determine what switches need to change their position and decide the new state for area A2. This new state will be used for the next time step.

x. If there has been a switching operation, activate CDA (the next two solutions are at $\frac{1}{2}$ time steps and use the backward Euler rule).

xi. Stop here if the final simulation time has been reached. Otherwise, increase the time step counter and go to step v.

Regardless of the number of nodes in the system, the order of the system of equations to solve after a switching event, is equal to the number of links (4 in this case). Compare this with the system size required to simulate the circuit with MicroTran, where the order of the system is equal to the number of nodes with unknown voltages (9 nodes).

4.3.2. Multiple HVDC Converters Interconnected by Links

The generalization of MATE for circuits containing several bridges is straightforward. Consider the 24-valve system of Fig. 4-16. The circuit corresponds to the bipolar 12-pulse substation utilized in the previous sections. As a first attempt we may divide the circuit into 6 areas interconnected by 16 links: the sources and line inductances are grouped in Area A1; the
HVDC substation is split into four areas A2, A3, A4, and A5, each one containing a 6-valve bridge (and therefore 64 combinations); and the last, area A6, corresponds to the load resistances.

Fig. 4-16. A 24-valve HVDC substation divided in 6 areas by 16 links.

We can improve the circuit partition (see Fig. 4-17) by considering some practical issues:

i. In HVDC transmission links, the DC side feeds transmission lines. In this case, the links on the DC side can be eliminated and the equivalent circuit of the sending (or receiving) end of the transmission line can be incorporated into the area to which the line is connected. Remember that the transmission lines already have the property of subdividing a network in subsystems without the use of the links required by the MATE algorithm.
ii. If the source side consists of constant elements, the source area can be incorporated into any of the converter areas. Examples of constant sources are constant Thévenin equivalents; constant sources in series with constant parameters; or as in the DC side, transmission lines feeding the AC side.

Applying these considerations, the 24-valve circuit can be subdivided into 4 areas interconnected by 11 links as shown in Fig. 4-17.

The general algorithm to solve networks containing multiple HVDC converters using MATE is detailed in Table 4-2.

Section 4.4 presents test cases to validate this methodology, and makes a comparison with the results obtained with the HVDC Object model presented before.
The benefits of this algorithm are:

1. Precalculation, preinversion and prestoring of all the possible combinations for each area saves computational effort during the transient solution.

2. The order of the system of equations to be solved is equal to the number of links. If the number of links is considerably smaller than the number of nodes, there is a considerable saving in computational effort. (For the 24-valve example, the solution with MATE was obtained with 11 links; whereas the entire circuit has 26 nodes).
Inspect the circuit and insert Links to subdivide it in $N$ independent Areas (try to minimize the number of links)

Determine the number of combinations per Area and precalculate, preinvert and prestore the corresponding matrices

Form the matrices $Z_{\text{links}}$ and $\hat{Z}$ needed in Eqs. A - 8 and A - 9 (from Appendix)

Start transient analysis $t=0$

Solve Areas independently using Eq. 3-2. This is the Thevenin solution. Calculate vector $\Delta F_{\text{links}}$

Update values in matrices $Z_{\text{links}}$ and $\hat{Z}$ according to the Areas' states

Solve for links' currents using Eq. A-8:

$$i_{\text{links}} = [Z_{\text{links}}]^{-1} \Delta F_{\text{links}}$$

Inject links' currents using Eq. A-9 to obtain all the node voltages: $V = \hat{Z} i_{\text{links}}$

For each Area, determine the new valves' positions and the consequent Area state

Increment time-step

end of simulation time?

No

Yes

end

Table 4-2. Generalized MATE algorithm for circuits containing 'N' HVDC converters.
4.4. Test Cases

This section presents several test cases that confirm the accuracy and solution speed of the two models and their corresponding methodologies proposed in this thesis (sections 4.2 and 4.3). The section is divided into two parts. The first part simulates a 12-pulse HVDC converter substation, and shows the behaviour of the converter in steady-state and under different fault situations. The second part simulates different HVDC converter configurations and shows simulation time comparisons.

4.4.1. Simulations for a 12-pulse test system

The 12-pulse HVDC converter of Fig. 4-18 is simulated in steady-state and under the influence of DC and AC faults. Table 4-3 summarizes the five tested cases for this circuit.

Switches S1 and S2 are time controlled. Closure of S1 simulates a DC fault, whereas closure of S2 simulates a single-phase AC fault.

The load is represented by a resistance and a DC source. The value of the DC source is set to zero for those cases where the converter operates in rectifier mode, and is negative for the inverter mode. The spikes in the valve currents can be eliminated using the zero crossing technique presented in section 3.2.
Table 4-3. Description of the test cases.

<table>
<thead>
<tr>
<th>Case</th>
<th>Description</th>
<th>Operating mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>steady-state operation</td>
<td>Rectifier</td>
</tr>
<tr>
<td>2</td>
<td>dc fault</td>
<td>Rectifier</td>
</tr>
<tr>
<td>3</td>
<td>single-phase ac fault</td>
<td>Rectifier</td>
</tr>
<tr>
<td>4</td>
<td>steady-state operation</td>
<td>Inverter</td>
</tr>
<tr>
<td>5</td>
<td>commutation failure</td>
<td>Inverter</td>
</tr>
</tbody>
</table>

4.4.1.1. Case 1: Steady-state operation

The steady-state operation is shown in Fig. 4-19. The DC current set point is 1600 amperes and the controller starts operation at 50 milliseconds. The plots include the rectified DC current, the non-filtered DC voltage (before the filtering action of the smoothing reactor), and the voltage and current of one valve.
Fig. 4-19. Case 1. Results for steady-state operation.
4.4.1.2. Case 2: DC fault

The influence of a DC fault in the test circuit is presented in Fig. 4-20. The fault is simulated by closing the switch S1 in Fig. 4-18 from 0.2 to 0.3 seconds.

The controller limits the current by increasing the firing angle during the fault, thus reducing the rectified voltage and the fault current. Once the firing angle exceeds 90°, the converter operates in the inverter mode. This help rapidly reducing the short circuit current to zero.

In Fig. 4-21, the controller has been turned off to show the worst case condition. Note the constant increase in the current during the duration of the fault. The high short circuit current that circulates without the controller can cause damage to the converter valves. The controlled current of Fig. 4-20 has also been plotted in Fig. 4-21 to show the favorable effect of the controller.
Fig. 4-20. Case 2. Results for a DC fault with controller.
Fig. 4-21. Case 2. Results for a DC fault without controller, and current comparison against the controlled case.

4.4.1.3. Case 3: Single-phase AC fault

An AC fault is applied to phase-a by closing switch S2 in Fig. 4-18 from 0.2 to 0.3 seconds. The behaviour of the circuit under the action of the controller is now shown in Fig. 4-22. The lack of AC voltage produces reduced rectified voltage and current. The controller tries to compensate by decreasing the firing angle to its minimum value.
Fig. 4-22. Case 3. Results for a single-phase AC fault.
4.4.1.4. Case 4: Inverter operation in steady-state

To operate as an inverter, the HVDC converter requires a power supply on the DC side to transfer energy from the DC side to the AC side. The DC source in Fig. 4-18 has a negative value and the steady-state operation is shown in Fig. 4-23.

The power flow reversal can be found by multiplying the DC current times the DC voltage. Since the voltage polarity is negative at all times, the power is also negative. A negative value for the power indicates that the DC side delivers energy to the AC side.

The time interval between the instant at which a valve is turned off, and the instant at which the same valve voltage becomes positive is the extinction angle $\gamma$. As discussed in Chapter 3, the angle (converted to seconds) needs to be larger than the valve’s minimum recombination time $t_q$. The extinction angle for this operating condition is shown in Fig. 4-23.

4.4.1.5. Case 5: Commutation failure

During the influence of a single-phase AC fault from 0.25 to 0.29 seconds, the inverter controller tries to compensate for the lack of power transferred by taking the firing angle to the maximum limit. For an inverter, this corresponds to a minimum extinction angle.

Fig. 4-24 shows the increased DC current during the fault. The higher current and the increased firing angle reduce the time of the commutating voltage for valve 1, producing a commutation failure. When this voltage changes polarity, the valve current starts growing, not permitting the current commutation from valve 1 to valve 3. Note from Fig. 4-24 that during the fault the extinction angle $\gamma$ is decreased until the commutation failure arises. Fig. 4-24 also shows the overlapping angle $\mu$, which is the commutation time interval.
Fig. 4-23. Case 4. Results for inverter operation in steady-state.
Fig. 4-24. Case 5. Commutation failure.
4.4.2. Simulation times

To compare the simulation times required by different HVDC converter models, the three configurations shown in Table 4-4 and Fig. 4-25 were run first with MicroTran, and then using the algorithms proposed earlier in sections 4.2 and 4.3, which are denominated Model I and Model II, respectively. Model I corresponds to the HVDC Object, and Model II to the use of MATE. The platform used for these simulations is an Intel-based personal computer with a Pentium Pro 200 MHz CPU, and the time step used for all the simulations is 50 μs.

4.4.2.1. Model I and Model II performance

To evaluate the speed performance of the models proposed in sections 4.2 and 4.3, both approaches were programmed in a power system simulator written in the ADA 95 programming language.

The bar graph of Fig. 4-26 presents the average computer times per one second of simulation for the cases presented in Table 4-4 and Fig. 4-25. The timings show the improved performance of both models over MicroTran. Notice that the advantage of both models over MicroTran increases as the number of valves grows. Because the best times correspond to Model I, this model was chosen to be tested in the real-time simulator OVNI, as presented in the next subsection.
Table 4-4. Test cases for simulation times comparisons.

<table>
<thead>
<tr>
<th>Case 1</th>
<th>6-valve monopolar HVDC converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 2</td>
<td>12-valve monopolar HVDC converter</td>
</tr>
<tr>
<td>Case 3</td>
<td>24-valve bipolar HVDC converter</td>
</tr>
</tbody>
</table>

Fig. 4-25. Test systems:
(a) 6-valve monopolar. (b) 12-valve monopolar. (c) 24-valve bipolar.
4.4.2.2. Simulation in OVNI

Based on the benchmarks obtained for the two proposed models for the HVDC converter, it was decided to code Model I for the OVNI real-time simulator [68]. This work was performed by Luis Linares as part of his Ph. D. research work [52]. The results presented next correspond to the OVNI driver using the backward Euler integration rule. For these tests, the AC network consisted of a simple Thévenin equivalent (source with impedances). The HVDC converter was represented in full, as presented in this thesis. The public-domain gcc (C++) compiler of the GNU toolset of the Free Software Foundation was used to compile the code.

These simulations show the real-time performance of OVNI when simulating circuits containing HVDC converters modeled as described in section 4.2. These results are consistent with those obtained when using MicroTran and have been published in [64].

Due to the fact that the number of operations per time step changes during the transient solution, the associated solution times are different for different time steps. Those time steps

Fig. 4-26. Solution times for the test cases with ADA 95 and MicroTran ($\Delta t=50$ $\mu$s).
involving switching operations require more operations and longer solution times. Real-time performance is restricted by the solution time required by the time step that takes the longest. The solution times presented in Table 4-5 and Fig. 4-27 correspond to the longest time step during the simulation of the test cases of Fig. 4-25. As indicated, these timings correspond to a single processor Pentium Pro 200 MHz computer. Even though not yet tested, these timings should be reduced to about 2/3 with the new Pentium II-300 MHz machines. This should bring the timings for the 24-valve case down to the 50 μs real-time performance benchmark.

<table>
<thead>
<tr>
<th></th>
<th>6-valve</th>
<th>12-valve</th>
<th>24-valve</th>
</tr>
</thead>
<tbody>
<tr>
<td>MicroTran (v2.06)</td>
<td>459</td>
<td>983</td>
<td>3120</td>
</tr>
<tr>
<td>Model I in OVNI</td>
<td>26</td>
<td>45</td>
<td>81</td>
</tr>
<tr>
<td>Ratio:</td>
<td>17.7</td>
<td>21.8</td>
<td>38.5</td>
</tr>
</tbody>
</table>

Table 4-5. Simulation times in microseconds per time step.

Fig. 4-27. Simulation times per time step (platform: single-processor Pentium Pro 200 MHz).
Flexible Alternating Current Transmission System (FACTS) are another important example of the issue of modelling multiple switching operations. This chapter presents models for FACTS devices that include forced-commutated inverters and Static VAR Compensators (SVC). The objective again is to support the development of models of power electronic converters for the OVNI real-time simulator. The first part of this Chapter proposes a general methodology to solve circuits involving forced commutations. The second part proposes a new model for the Thyristor Controlled Reactor (TCR), an essential device in SVC stations.

During this decade, forced-commutated inverters based on Gate Turn Off (GTO) thyristors are finding newer and more flexible applications in power systems [53], [70], [77], [105], [108], [109], [110]. In Chapter One, two applications were already mentioned: the Advanced Static VAR Compensator (STATCOM) used for reactive power compensation [21], [29], [46], [92], and the HVDC inverter used for feeding remote passive loads without local AC generation [1], [95].

GTOs have similar behaviour to conventional thyristors but they can also be turned off with a gate signal. Currently there are GTOs with up to 6 kV and 3kA ratings, as described in [70], [95], and [105].

STATCOMs are the static version of the synchronous condenser, but with the advantages of improved dynamic capabilities and less maintenance. STATCOMs operate on the principle of the forced commutated voltage source converter (VSC). They also have the advantage of requiring lower ratings while occupying less space than conventional SVCs. In HVDC systems,
STATCOMs are installed at the receiving end to improve the HVDC inverter operation, especially when feeding weak AC systems. For more details consult references [29], [46], and [92].

SVCs were first developed in the 1960s but in late 1970s their use has increased dramatically [28]. SVCs provide leading and lagging current by switching capacitor and reactor banks with the use of conventional thyristors; detailed theory can be found in [71].

5.1. Forced Commutated Inverters

The basic 6-pulse inverter has 6 GTOs with 6 anti-parallel diodes as shown in Fig. 5-1. The DC supply can be the output of a rectifier or a charged capacitor. When the current through a GTO crosses zero, it is instantaneously transferred to the anti-parallel connected diode constituting natural commutation. The diode either turns off naturally or by turning on the GTO on the opposite side of the same branch. Forced commutation requires a gate signal applied to the GTO to turn it off.

![Basic 6-pulse inverter bridge](image)

Fig. 5-1. Basic 6-pulse inverter bridge.

An alternating voltage is obtained in phase-a by switching GTO1 and GTO4, alternatively. The same applies for the other phases when switching their corresponding semiconductors on
and off. Fig. 5-2 depicts the basic inverter concept, and shows the semiconductors that must be conducting in order to produce such voltages. The inverter controls the AC voltage magnitude and the harmonic content using pulse width modulation techniques and multilevel configurations [29], [70], [92], [110]. To prevent the GTO valves from overheating, the carrier frequency is limited to less than 600 Hz.

![Diagram of inverter output voltage waveforms.](image)

Fig. 5-2. Basic inverter output voltage waveforms.

If the inverter is feeding a passive load, electrical energy flows from the DC to the AC side as in the case of an HVDC transmission system.

If the inverter operates as a reactive power compensator (STATCOM), there is no real power nor reactive power transferred from the DC to the AC side. Hence, the DC supply can be a relatively small charged capacitor. In a similar way as the synchronous condenser interacts with an AC system via the synchronous reactance, the reactive power exchange takes place between the AC inverter's terminals and the AC system via an inductance (e.g., the transformers inductance).
The STATCOM can supply or absorb reactive power by controlling the inverter voltage [29]. If the magnitude of the inverter voltage exceeds the system’s voltage magnitude, the inverter supplies reactive power. If the system’s voltage magnitude is greater than the inverter’s voltage, the inverter absorbs reactive power. The converter controller maintains the inverter’s and the system’s voltages in phase.

5.1.1. Exploratory Solution in Circuits with GTOs

The forced commutation of a GTO induces negative voltages in inductors located in the chopped current’s path. In practical power electronic converters, a freewheeling diode provides a low impedance trajectory for the current. The diode turns on at the exact instant it becomes positively polarized, and the current is instantaneously transferred from the GTO to the freewheeling diode.

However, the discrete time nature of the traditional EMTP methodology has difficulties modelling GTO thyristors. When a GTO opens, its current goes to zero in one time step, causing numerical problems.
Consider the buck regulator of Fig. 5-3. Assume the GTO is conducting current \( I_1 \) at time \( t_1 \), and the diode is blocking. Under this condition, the inductor current equals the GTO current. If at time \( t_2 = t_1 + \Delta t \) the GTO is forced to open, then its current becomes zero. The inductor voltage at time \( t_2 \) is \( v_L(t_2) = -LI_1/\Delta t \). For example, if \( V_s = 100 \text{ V} \), \( I_1 = 10 \text{ A} \), \( L = 10 \text{ mH} \), and \( \Delta t = 50 \mu \text{s} \), then \( v_L(t_2) = -2 \text{ kV} \). Since at \( t_2 \), both the GTO and the diode are open, then \( i_L(t_2) = 0 \). The influence of this large voltage changes the diode to the conducting state for \( t_3 = t_2 + \Delta t/2 \) (if using CDA). At time \( t_3 \), however, the inductor history current is zero (if using CDA). Both the inductor and the diode current become \( i_D(t_3) = i_L(t_3) = -v_C(t_3)/(2L/\Delta t) < 0 \), forcing the diode to open again for time \( t_4 = t_3 + \Delta t/2 \). The result is that both the GTO and the diode are opened, and there will not be a current until the GTO is fired again. The currents and voltages for the described events are depicted (not to scale) in Fig. 5-4. The half time-step solution at time \( t_3 \) is skipped for plotting in MicroTran.

![Fig. 5-3. Buck regulator.](image)
Fig. 5-4. Forced commutation of a GTO in the discrete time solution.
EMTP simulators, such as MicroTran, solve this problem by making the GTO and freewheeling diode work as a pair [18]. The diode is doing the opposite of the GTO. If the GTO is opened at time $t_2$, the diode is forced to close at the same instant $t_2$, regardless of the diode operating conditions. This provides a path for the $i_L(t_2)$ current through the diode, and, therefore, the inductor current is never forced to be zero. This solution has three disadvantages: first, the user needs to select those semiconductors working as pairs (this requires some knowledge of the circuit behaviour; which can be difficult for some complicated circuits involving many GTOs, diodes, and inductors); second, the diode model is altered so that it works as the GTO's pair, affecting the basic diode fundamentals; finally, the diode is a pair of a specific GTO, not guarantying an appropriate operation as a freewheeling diode for any other chopped current.

The exploratory solution proposed below provides a solution to the problem of switching off GTOs. It is easy to program and is used here to simulate circuits with several GTOs and diodes, such as the inverter of Fig. 5-1. Similar techniques have also been proposed by other authors [38], [89].

Assume that a GTO firing signal ceases. Before proceeding to the next time-step solution we can perform an experimental half time-step solution, which we will name an exploratory solution. This exploration consists of solving the network with the GTO opened. With the exploratory results, we can decide which diodes need to close due to the high voltages induced in the inductors, whose currents were chopped. The exploratory solution is then neglected, except for the new diode positions, and the solution is resumed normally. The exploratory solution algorithm is summarized in Table 5-1.
Table 5-1. Exploratory solution algorithm for circuits containing GTO thyristors.

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To visualize how the algorithm works, consider the buck regulator again, and refer to the plots of Fig. 5-5. Assume that the GTO conducts at time $t_1$. If at time $t_2 = t_1 + \Delta t$, the firing signal ceases, we perform a one-step exploratory solution. The high negative voltage $v_L(t_2)$ helps us decide to close the diode. We then go back to $t_1$, and solve for $t_3 = t_1 + \Delta t/2$ with the diode closed (and with the GTO opened). With the diode closed, the inductance current $i_L$ flows through the diode. Since this current is positive, the diode remains closed at time $t_4 = t_2 = t_3 + \Delta t/2$.

Fig. 5-6 compares the solution of the buck regulator with and without the proposed algorithm, where the benefits of the exploratory solution can be appreciated. If CDA is used alone, the inductor current goes to zero when the GTO is switched off, thus impeding the buck regulator to build up a load voltage.

Fig. 5-7 presents the exploratory solution for the forced commutated inverter circuit of Fig. 5-1.
Fig. 5-5. Effect of the exploratory solution algorithm in solution of the buck regulator.
Fig. 5-6. Buck regulator simulations with and without the exploratory solution.
5.1.2. Modelling a Forced Commutated Inverter using the HVDC Object

The exploratory solution presented above was adapted to use the HVDC Object of section 4.2 for the simulation of forced commutated inverters.

Consider the anti-parallel connection of GTO1 and diode D1 from the basic 6-pulse inverter presented in Fig. 5-1. Both GTO1 and D1 can be in their open state at the same time, but only GTO1 or D1 can close at a specific time. Hence, the combination GTO1-D1 has two states (on or off) and the total number of combinations for the inverter is 64. The difference with respect to the conventional thyristor bridge is that a valve current can now flow in both directions (either through a GTO or through the anti-parallel diode).

If the inverter bridge is defined as the HVDC Object, then there are 64 related matrices seen by the external system as a consequence of the 64 bridge status.
The Object's status and the corresponding matrix are selected according to the controller firing signals. The firing signals are modeled as pulses that are present when a particular valve has to be in the closed position. A GTO closes if there is a firing signal and a positive voltage applied. The GTO opens when the firing signal ceases or when the current crosses zero. When opening GTOs, one extra exploratory backward Euler solution is performed to check for required closure of diodes.

The simulation results for the circuit of Fig. 5-8 with modified sinusoidal pulse width modulation (MS-PWM) are shown in Fig. 5-9. The simulation uses the exploratory solution algorithm, and the inverter as an HVDC Object. The plots show the good performance of the exploratory solution algorithm under the influence of multiple switching operations.

![Fig. 5-8. Inverter as an HVDC Object.](image)
Fig. 5-9. MS-PWM inverter simulation using the *exploratory solution* algorithm:
(a) Load is predominantly resistive (b) Load is predominantly inductive.
Advanced Static VAR Compensators (STATCOMs) use a 12-, 24- and 48-pulse operation to improve the harmonic content. The 12-pulse STATCOM of Fig. 5-10 is now simulated to control the reactive power direction. Fig. 5-11 shows the 12 pulse operation case when generating and absorbing reactive power. In [29], Gyugyi et al. described the fundamentals of a 24-pulse STATCOM. In [92], Schauder et al. presented a ±100 MVAR STATCOM based on a 48-pulse scheme.

The exploratory solution increases the solution times at those time steps involving forced commutations. At the time steps involving the exploratory solution, the implementation of this algorithm in the ADA-95 driver showed an increase of 50% in the solution time for the 6-pulse inverter and 63% for the 12-pulse STATCOM. As in Chapter 4, the simulations are performed in an off-the-shelf Pentium Pro 200 MHz personal computer.

Fig. 5-10. A 12-pulse STATCOM.
Fig. 5-11. System voltage, inverted voltage, and inverted current for a 12-pulse STATCOM: (a) Supplying reactive power (b) Absorbing reactive power.

5.2. Static Var Compensators

An ideal Static VAR Compensator (SVC) provides any required amount of reactive power at the bus where the compensator is connected. The most common way to achieve this task is to connect a capacitor bank by means of a Thyristor Switched Capacitor (TSC), in parallel with a Thyristor Controlled Reactor (TCR) that neutralizes the leading effect of the capacitor bank. A TCR is a varying inductance obtained by an appropriate change of the thyristors’ conduction angle. Fig. 5-12 shows the basic idea under the SVC.

The nominal power of the TCR inductor normally exceeds that of the capacitor bank to compensate or overcompensate the capacitor’s leading reactive power. The net reactive power is
adjusted as needed between the rating of the TSC (leading reactive power) and the combined effect of the TSC, minus the operating point of the TCR (leading to lagging reactive power).

The circuit in Fig. 5-13 corresponds to a single-phase TCR connected to an ideal source. Let the voltage source be \( v_s(t) = V_m \sin \omega t \) volts. If T1 and T2 are alternately fired at \( T/2, 3T/2, 5T/2, 7T/2, \ldots \), then full conduction occurs and each thyristor conducts for half a cycle. The resulting current is sinusoidal with no harmonics. The firing angle ‘\( \beta \)’ is 90°.

As the firing angle increases, the current is no longer continuous and harmonics arise (see Fig. 5-14). For \( \beta < 90^\circ \), an undesired DC component of current appears. No conduction exists for \( \beta > 180^\circ \). When the firing angle varies, the apparent inductance changes. The reactive power absorbed by the TCR changes with the fundamental current variation.
Fig. 5-14. TCR current for $\beta=90^\circ$, $120^\circ$, and $150^\circ$.

Fig. 5-15 shows an SVC and its current-voltage characteristic. The operating point "Q" is found at the intersection between this characteristic and the system load line. The equivalent system in Fig. 5-15 consists of a source in series with an impedance $jX_1$. The value for the inductance that creates the SVC characteristic is obtained by using the fundamental current through the inductance and neglecting the higher order harmonics. A control circuit determines the conduction angle required for the TCR. The TSC is either fully connected or fully disconnected.

Fig. 5-15. SVC operating point (combined TSC and TCR).
The discrete-time equivalent circuit for the single-phase TCR of Fig. 5-13 is shown in Fig. 5-16a where the conductance and the history current source represent the inductance.

![Diagrams of TCR models](image_url)

(a) Normal representation (MicroTran). (b) Proposed model.

In the proposed TCR model of Fig. 5-16b the series connection of thyristors and inductance are treated as a *special inductance* that contains a resistance in parallel with a history current source [19], [23]. Up to this point, the thyristors have been modeled as switches, and the admittance matrix has been changed at switching events. The thyristors in the proposed model are not modeled as switches. Instead, the *special inductance* model senses the thyristors conduction or blocking condition and adjusts the history term of the inductance’s discrete time equivalent as follows:

\[
h_{eq}(t) = \begin{cases} 
    h_{eq}(t - \Delta t) + 2G_{eq}v(t - \Delta t) & \text{if } T_1 \text{ or } T_2 \text{ ON} \\
    0 & \text{if } T_1 \text{ and } T_2 \text{ OFF}
\end{cases}
\] (5-1)
The TCR model checks for the presence of a firing signal and turns on the history term. The model then waits for the current to change direction to turn off the history term. This approach avoids the use of switches and permits having a constant conductance matrix.

As an example, let us use typical values, e.g., $L=10 \text{ mH}$, $\Delta t=50 \mu \text{sec}$, and a frequency of 60 Hz. The steady-state value of the TCR impedance at full conduction is $Z=\frac{2\pi f L}{\Delta t} = 3.77 \, \Omega$. In the discrete-time equivalent, this TCR impedance is the parallel equivalent of the history current source in the on state and a resistance of value $\frac{2L}{\Delta t} = 400 \, \Omega$ (trapezoidal rule).

If the thyristors open, the history term is set to zero and the impedance increases from 3.77 $\Omega$ to 400 $\Omega$ (a factor of more than 100). Since 400 $\Omega$ is not an infinite impedance, some current will flow through it. As the firing angle increases, the ratio between the apparent inductance at 60 Hz and the 400 $\Omega$ resistance decreases, and the error becomes larger. Fortunately, at high firing angles the effective current is only a small percentage of the nominal reactor current. Moreover, the error only exists during no-conduction intervals.

Fig. 5-18 shows the simulation results with the new TCR model and with MicroTran for the single-phase circuit of Fig. 5-17. To evaluate the model accuracy and limitations, the Thévenin of the system is simplified to a voltage source and an inductance.
As mentioned earlier, the impedance for the off state is simply the discrete-time equivalent conductance ($\Delta t/2L$ for trapezoidal) with the history term set to zero. To get acceptable results, the time step needs to be small, and the conductance in the off state needs to be much smaller than the external impedance. If these conditions are not satisfied, the simulation results do not accurately represent the TCR behaviour. A simulation with a TCR inductor that is much smaller than the system impedance is shown in Fig. 5-19. The solution is compared against MicroTran.
The effect of increasing the time step by a factor of ten is shown in Fig. 5-20. This plot is compared to the solution obtained with MicroTran for the same time-step size and with the new model for a smaller time step.

In practical situations, there are two factors that allow us to have the conditions under which the model is accurate. First, electromagnetic transient studies for power electronic devices in
power systems require small time steps (100 μ or less). Second, TCR are large reactor banks connected as reactive power compensators and the reactance value is typically several times larger than the combined system impedance.

The proposed TCR model was validated by simulating the SVC substation shown in Fig. 5-21. This substation was simulated using MicroTran and also using the proposed new model in the ADA 95 simulator. The simulated currents and voltages closely match those obtained with MicroTran, as can be appreciated in Fig. 5-22.

Fig. 5-21. SVC substation at Langdon, Alberta.
Fig. 5-22. Simulation results for a SVC substation.
In the simulation shown, the TCRs are operated with a firing angle equal to 120°, the TSC are fully connected and the station is supplying reactive power to the power system. The plots include phase current in the TCR connected in the secondary side of the transformer, the corresponding line current in the TCR, the total line current in the secondary side which includes the filter and TSC currents, and the line-to-neutral and line-to-line secondary voltages. A similar match between the results of this new model and MicroTran was found in the primary and tertiary sides of the substation transformer.

The main benefit of the proposed TCR model is that the system's matrix is not affected by the TCR switching, and, as a consequence, the simulation times are considerably diminished. The simulation times per simulated second for the example presented above are summarized in Table 5-2.

<table>
<thead>
<tr>
<th>MicroTran</th>
<th>New TCR Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>18.61</td>
<td>8.73</td>
</tr>
</tbody>
</table>

Table 5-2. Simulation time per simulated second-step in seconds for the SVC substation of Fig. 5-21.
6. Chapter 6

Conclusions and Recommendations

Two approaches to model HVDC converters are proposed in this thesis which permit considerable reductions in the solution times as compared to traditional EMTP solutions.

The first model, denominated the HVDC Object, presents the best solution times for the cases tested. The savings in computational time are obtained when all possible equivalent matrices presented by the Object are precalculated and prestored in the computer memory before the starting of the transient solution loop. If the HVDC Object contains 6 valves, then the number of combinations to be prestored is only 64. The use of four HVDC Objects allows the simulation of a 24-valve converter substation by prestoring only $4 \times 64 = 256$ combinations, instead of trying to prestore over 16 million combinations.

If the HVDC Object is programmed as an OOP object, the model's structure allows the programmer to plug it into OOP electromagnetic transient circuit simulators. This transportability was demonstrated by programming this model as an ADA 95 object and connecting it to an electromagnetic transients stand-alone program written in ADA 95. The real-time performance was demonstrated by Mr. Luis Linares in a C++ simulator of the OVNI family. In addition, Mr. Yasushi Fujimoto of Mitsubishi, incorporated the HVDC Object into their electrical networks' simulator, and successfully tested it for real-time performance on a Cray supercomputer.

The second HVDC model presented uses the Multi-Area Thévenin Equivalent algorithm. This approach also permits the prestoring of the 64 combinations existing in a 6-valve converter. The network is subdivided by links into independent areas that are solved separately, then the
system solution is obtained after calculating the links' currents. Even though the solution times obtained when programming this model in the ADA 95 circuit simulator were considerably better than using MicroTran, they were inferior to the timings obtained with the HVDC Object model.

Both tested approaches include a detailed modelling of the HVDC converter components. The proposed modelling brings out the advantages of EMTP simulators in providing a highly efficient and sufficiently accurate representation of semiconductor valves. The individual modelling of each valve also allows the detailed simulation and analysis of internal bridge faults (such as commutation failure, misfiring, fire-through, etc.).

Another advantage that both proposed converter models share is that there is no delay between the system solution and the HVDC converter solution. This is consistent with the EMTP and OVNI's modelling philosophy, and assures an accurate and numerically stable solution under all system conditions. Other approaches that allow a time step decoupling between network and converter cannot guarantee high accuracy and robustness under all system conditions.

The zero crossing detection algorithm proposed in Chapter 3 improves the accuracy of the simulations when modelling power electronic converters. The program solves the network for the exact instant at which any semiconductor changes its state. Because it is important for applications in real-time simulators to have output values at fixed time intervals, this interpolation scheme includes a resynchronization to the original time increment.

The problems originated by forced commutations of GTO thyristors have been solved with the exploratory solution algorithm proposed in Chapter 5. Combining this algorithm with the
HVDC Object model, it is possible to simulate the behaviour of GTO-based forced commutated
inverters, commonly used in FACTS applications (inverters feeding passive loads and Advanced
Static Var Compensators -STATCOMs).

When modelling SVC substations, the TCR antiparallel thyristors’ pair in series with the
reactor is combined in an equivalent element with a constant conductance and a varying history
source. This proposed implementation avoids the need to recalculate the system’s matrix when
the only switching events are originated by the thyristors.

The following list presents some aspects that I visualize as recommendations for future
developments:

1. The HVDC Object model needs to be interfaced to a generalized digital controller. This
   will permit a simulation of HVDC substations with complete control schemes.

2. The problem of a time-step delay between the controller and the network simulation in
   the EMTP has not yet been solved. Further research needs to be done to simultaneously
   solve the electrical network and the controller equations efficiently without substantially
   affecting the computational speed improvements already gained.

3. The zero crossing detection algorithm needs to be combined with the exploratory
   solution algorithm. Both algorithms were not tried together. A careful analysis is required
   for switching events where both algorithms (an interpolation to find the zero crossing
   instant and an exploratory solution) need to be invoked at the same time.
4. The models developed in this thesis have been aimed at permitting their implementation in real-time simulators. In fact, one of the models (the HVDC Object) has already been coded for real-time performance in a companion Ph. D. project. It is believed that it will also be possible to implement other FACTS devices in the context of real-time simulators. For example, the SVC substation can be programmed as an SVC Object with the same principles used in the HVDC Object model.

This concludes this thesis work. Hopefully this research can be useful in the future development of computer modelling of power electronics applications in power systems, and in particular for the further development of real-time power system simulators.
BIBLIOGRAPHY


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APPENDIX A

THE MULTI-AREA THEVENIN EQUIVALENT ALGORITHM

This appendix describes the Multi-Area Thévenin Equivalent (MATE) formulation [62]. The MATE concept is based in the hybrid approach for networks solution. MATE is also used in OVNI [52] to subdivide a complex network into independent subnetworks interconnected by links.

A.1 Two Areas Interconnected by One Link

Let us illustrate the very simple case of Fig. A-1, where one link divides an electrical network into two areas A1 (n nodes) and A2 (m nodes), with admittance matrices $Y^{A1}$ and $Y^{A2}$, respectively.

Fig. A-1. One link dividing a network into two areas.
The link terminals are nodes \( j \) and \( k \), and from the circuit the link current is:

\[
i_{\text{link}} = g_{\text{link}} (v_j^{A1} - v_k^{A2})
\]

Eq. A-1

where \( g_{\text{link}} \) is the link conductance. For an ideal link \( g_{\text{link}} \) can be either 0 or \( \infty \).

The right-hand side vector in the nodal admittance solution of equation (3-2) in Chapter 3 includes all currents, except the link current \( i_{\text{link}} \). To consistently apply nodal analysis to each subsystem of Fig. A-1, \( i_{\text{link}} \) needs to be included in the nodal equations as follows:

\[
\begin{align*}
\begin{bmatrix}
Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} \\
0 & \cdots & 0 & \cdots & 0 \\
Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} \\
0 & \cdots & 0 & \cdots & 0 \\
Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} & \cdots & Y_{\text{link}}^{A1} \\
\end{bmatrix}
\begin{bmatrix}
v_{\text{link}}^{A1} \\
v_{\text{link}}^{A2} \\
v_{\text{link}}^{A1} \\
v_{\text{link}}^{A2} \\
v_{\text{link}}^{A1} \\
\end{bmatrix}
= \begin{bmatrix}
J_{\text{link}}^{A1} \\
J_{\text{link}}^{A2} \\
0 \\
0 \\
0 \\
\end{bmatrix} + \begin{bmatrix}
0 \\
J_{\text{link}}^{A2} \\
-i_{\text{link}} \\
0 \\
-i_{\text{link}} \\
\end{bmatrix}
\end{align*}
\]

Eq. A-2
Combining Eq. A- 1 with Eq. A- 2 we get:

\[
\begin{bmatrix}
Y_{11}^{A1} & \ldots & Y_{1j}^{A1} & \ldots & Y_{1n}^{A1} \\
\vdots & \ddots & \vdots & \ddots & \vdots \\
Y_{j1}^{A1} & \ldots & Y_{jk}^{A1} & \ldots & Y_{jn}^{A1} \\
\vdots & \ddots & \vdots & \ddots & \vdots \\
Y_{m1}^{A1} & Y_{m2}^{A1} & \ldots & Y_{mn}^{A1}
\end{bmatrix}
\begin{bmatrix}
y_1^{A1} \\
y_j^{A1} \\
y_m^{A1}
\end{bmatrix}
= 
\begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix}
\begin{bmatrix}
J_1^{A1} \\
J_j^{A1} \\
J_m^{A1}
\end{bmatrix}
\]

Eq. A- 3

In Eq. A- 3, the third partition row corresponds to Eq. A- 1. The final solution is obtained in two steps. When \(g_{\text{link}} = 0, i_{\text{link}} = 0\), leaving the first two rows with a decoupled solution. After obtaining the decoupled solution, we close the link\(^4\) by letting \(g_{\text{link}} \to \infty\). Eq. A- 3 is solved again in the way described below.

\(^4\) The link current can not be determined from this equation when \(g_{\text{link}} \to \infty\). Its value will be evaluated by other means.
Both sides of the first two rows in Eq. A-3 are premultiplied by the inverse matrices $Z^{A1}=(Y^{A1})^{-1}$ and $Z^{A2}=(Y^{A2})^{-1}$ respectively, yielding:

\[
\begin{bmatrix}
1 & 0 \\
0 & 1 \\
\end{bmatrix}
\begin{bmatrix}
Z^{A1}_{ij} \\
Z^{A1}_{i} \\
Z^{A2}_{ij} \\
Z^{A2}_{i} \\
-Z^{A3}_{kk} \\
-Z^{A3}_{i} \\
0 \\
0 \\
\end{bmatrix}
\begin{bmatrix}
v^{A1}_1 \\
v^{A1}_j \\
v^{A1}_k \\
v^{A2}_1 \\
v^{A2}_j \\
v^{A2}_k \\
0 \\
0 \\
\end{bmatrix}
\begin{bmatrix}
J^{A1}_1 \\
J^{A1}_j \\
J^{A1}_k \\
J^{A2}_1 \\
J^{A2}_j \\
J^{A2}_k \\
0 \\
0 \\
\end{bmatrix}
= 
\begin{bmatrix}
E^{A1}_1 \\
E^{A1}_j \\
E^{A1}_k \\
E^{A2}_1 \\
E^{A2}_j \\
E^{A2}_k \\
0 \\
0 \\
\end{bmatrix}
\]

where the first two submatrices on the third column contain the $j$-th and $k$-th columns of the inverse matrices $Z^{A1}$ and $Z^{A2}$, respectively.

The first two submatrices on the right hand side of Eq. A-4 are of the form $Y^{-1}J$ and contain the voltages' decoupled solution or Thévenin voltages.
Applying row elimination, the first two submatrices on the third row can be expunged, producing:

\[
\begin{bmatrix}
1 & 0 & Z_{ij}^{A1} & \vdots & \vdots \\
0 & 1 & Z_{jj}^{A1} & \vdots & \vdots \\
0 & 0 & \ldots & \ldots & \ldots \\
0 & 0 & Z_{ij}^{A1} + Z_{kk}^{A2} + \frac{1}{g_{link}} & i_{link} & E_j^{A1} - E_k^{A2}
\end{bmatrix}
\]

Eq. A-5

Now, if in Eq. A-5, \(g_{link} \to \infty\) we obtain:

\[
i_{link} = \frac{E_j^{A1} - E_k^{A2}}{Z_{ij}^{A1} + Z_{kk}^{A2} + \frac{1}{g_{link}}} = \frac{E_j^{A1} - E_k^{A2}}{Z_{ij}^{A1} + Z_{kk}^{A2}}
\]

\[
i_{link} = \left[ Z_{ij}^{A1} + Z_{kk}^{A2} \right]^{-1} \left[ E_j^{A1} - E_k^{A2} \right]
\]

Eq. A-6

Eq. A-6 may be visualized by the Thévenin equivalents of each area interlaced by the link as illustrated in Fig. A-2.
Finally, Eq. A-5 is used to calculate the actual values of the node voltages when the link current is obtained from Eq. A-6:

\[
\begin{bmatrix}
  v_1^{A1} \\
  \vdots \\
  v_j^{A1} \\
  \vdots \\
  v_a^{A1} \\
  v_1^{A2} \\
  \vdots \\
  v_k^{A2} \\
  \vdots \\
  v_m^{A2}
\end{bmatrix} = \begin{bmatrix}
  E_1^{A1} \\
  \vdots \\
  E_j^{A1} \\
  \vdots \\
  E_a^{A1} \\
  -\frac{E_1^{A2}}{E_1^{A1}} \\
  \vdots \\
  -\frac{E_k^{A2}}{E_k^{A1}} \\
  \vdots \\
  -\frac{E_m^{A2}}{E_m^{A1}}
\end{bmatrix} - \begin{bmatrix}
  Z_{ij}^{A1} \\
  \vdots \\
  Z_{jk}^{A1} \\
  \vdots \\
  Z_{ak}^{A1} \\
  -Z_{11}^{A2} \\
  \vdots \\
  -Z_{kk}^{A2} \\
  \vdots \\
  -Z_{mk}^{A2}
\end{bmatrix} [i_{link}]
\]

Eq. A-7
The impedances $Z_{ji}^{A1}$ and $Z_{kk}^{A2}$ can be directly found from the impedance matrices $Z^{A1}$ and $Z^{A2}$, and the voltages $E_j^{A1}$ and $E_k^{A2}$ from an open circuit solution of the networks. The algorithm is summarized in Table A-1.

1. Divide any given network in 2 areas $A1$ and $A2$ at any node-$i$. This will split node-$i$ in 2 nodes. Name resulting nodes: node-$j$ (the one in $A1$) and node-$k$ (the one in $A2$). In the final solution the voltages for both nodes must be the same since they represent the same original node-$i$.

2. Interconnect $A1$ and $A2$ with a link as in Eq. A-1.

3. Form admittance matrices $Y^{A1}$ and $Y^{A2}$ and obtain the corresponding inverse matrices $Z^{A1}$ and $Z^{A2}$ (of particular interest are the $j$-th column of $Z^{A1}$ and the $k$-th column of $Z^{A2}$).

4. Solve $A1$ and $A2$ separately using (3-2) with link opened. This produces the Thévenin vector voltages $E^{A1}$ and $E^{A2}$ of Eq. A-5.

5. Interconnect the Thévenin equivalents to form a circuit as the one in Fig. A-2. Solve for $i_{link}$ with the link on its closed state using Eq. A-6.

6. Inject $i_{link}$ into $A1$ and $A2$ using Eq. A-7 to obtain the vectors $V^{A1}$ and $V^{A2}$ containing the final solution. To verify the result check if $v_j^{A1} = v_k^{A2}$ (this is the voltage of the original node-$i$).

<table>
<thead>
<tr>
<th>Table A-1. MATE algorithm for two areas connected by one link.</th>
</tr>
</thead>
</table>

**A.2 Generalizing MATE**

To generalize MATE, an $N$-node network can be subdivided into $M$ areas interconnected by $L$ links as shown in Fig. A-3. The same algorithm presented in the previous section can be applied to the general case.
The starting point again is to build a nodal formulation as the one presented in Eq. A-3, that can be simplified to equations analogous to Eq. A-6 and Eq. A-7. Due to the fact that there are \( L \) links, Eq. A-7 takes the matrix form:

\[
i_{\text{links}} = Z_{\text{links}}^{-1} \Delta E_{\text{links}}
\]

Eq. A-8

where:
- \( i_{\text{links}} \): L-order vector containing links' currents
- \( Z_{\text{links}} \): LxL-order links impedance matrix containing appropriate Thévenin impedances
- \( \Delta E_{\text{links}} \): L-order vector containing Thévenin voltages across each link (from the decoupled solution)
whereas Eq. A-7 becomes:

\[ \mathbf{V} = \mathbf{E} - \hat{\mathbf{Z}} \mathbf{i}_{\text{links}} \]  

Eq. A-9

where:
- \( \mathbf{V} \): N-order vector containing all the system's voltages
- \( \hat{\mathbf{Z}} \): NxL-order impedance matrix containing appropriate Thévenin impedances
- \( \mathbf{E} \): N-order vector containing Thévenin voltages obtained from the decoupled solution

For completeness, Table 3-9 is repeated here as Table A-2, presenting the generalized MATE algorithm.

1. Divide any given network in \( M \) areas \( A_1, A_2, \ldots A_M \).
2. Interconnect areas with \( L \) links with a link as in Fig. A-3.
3. Form admittance matrices \( \mathbf{Y}^{A_1}, \mathbf{Y}^{A_2}, \ldots, \mathbf{Y}^{A_M} \) and obtain the corresponding inverse matrices \( \mathbf{Z}^{A_1}, \mathbf{Z}^{A_2}, \ldots, \mathbf{Z}^{A_M} \). Form matrices \( \mathbf{Z}_{\text{links}} \) and \( \hat{\mathbf{Z}} \) by row elimination as for the 2 areas example in Eq. A-4 and in Eq. A-5, or by direct inspection.
4. Solve areas separately using Equation 3-2 with links opened. This produces the Thévenin vector voltage \( \mathbf{E}_{\text{links}} \) needed in steps 5 and 6.
5. Obtain matrix \( \mathbf{Z}_{\text{links}} \) and solve for link currents using Eq. A-8.
6. Inject vector \( \mathbf{i}_{\text{links}} \) using Eq. A-9 to obtain the final solution.

Table A-2. Generalized MATE algorithm.
A.2.1 Two links connecting two areas

Fig. A-4. Two areas joined by two links: (a) Link currents flowing from A1 to A2. (b) First link current from A1 to A2, second link current from A2 to A1.

If we apply MATE formulation to the circuit of Fig. A-4(a), the elements of Eq. A-8 and Eq. A-9 become:

\[
Z_{\text{links}} = \begin{bmatrix}
Z_{ii}^{A1} + Z_{pp} & Z_{ij}^{A1} + Z_{pq} \\
Z_{ji}^{A1} + Z_{pq} & Z_{jj}^{A1} + Z_{qq} \\
\end{bmatrix}
\]

\[
\Delta E_{\text{links}} = \begin{bmatrix}
E_i^{A1} - E_p^{A2} \\
E_j^{A1} - E_q^{A2} \\
\end{bmatrix}
\]

\[
\hat{Z} = \begin{bmatrix}
0 & \cdots & Z_{ii}^{A1} & \cdots & Z_{ij}^{A1} & \cdots & 0 \\
0 & \cdots & Z_{ij}^{A1} & \cdots & Z_{jj}^{A1} & \cdots & 0 \\
\end{bmatrix}
\]

Eq. A-10
The definition of current direction in the links deserves especial attention. For example, if we reverse the current direction of one link, some elements in Eq. A-10 must change sign. For the current direction shown on Fig. A-4(b) the changes in signs give:

\[
Z_{\text{links}} = \begin{bmatrix}
Z_{ii}^{A1} + Z_{pp}^{A2} & -Z_{ij}^{A1} - Z_{pq}^{A2} \\
-Z_{ji}^{A1} - Z_{pq}^{A2} & Z_{jj}^{A1} + Z_{qq}^{A2}
\end{bmatrix}
\]

\[
\Delta E_{\text{links}} = \begin{bmatrix}
E_i^{A1} - E_p^{A2} \\
-E_j^{A1} + E_q^{A2}
\end{bmatrix}
\]

\[
\hat{Z} = \begin{bmatrix}
0 & \cdots & Z_{ii}^{A1} & \cdots & Z_{ij}^{A1} & \cdots & 0 & \cdots & 0 & \cdots & 0 \\
0 & \cdots & -Z_{ij}^{A1} & \cdots & -Z_{jj}^{A1} & \cdots & 0 & \cdots & 0 & \cdots & 0
\end{bmatrix}^	op
\]

Eq. A-11
A.2.2 Two links connecting three areas

For Fig. A- 5, the new set of equations is:

\[
Z_{\text{links}} = \begin{bmatrix}
Z_{ii}^{A1} + Z_{pp}^{A2} & -Z_{pq}^{A2} \\
-Z_{qp}^{A2} & Z_{qq}^{A2} + Z_{xx}^{A3}
\end{bmatrix}
\]

\[
\Delta E_{\text{links}} = \begin{bmatrix}
E_i^{A1} - E_p^{A2} \\
E_p^{A2} - E_x^{A3}
\end{bmatrix}
\]

\[
\hat{Z} = \begin{bmatrix}
0 & \cdots & Z_{ii}^{A1} & \cdots & 0 & \cdots & -Z_{pp}^{A2} & \cdots & -Z_{pq}^{A2} & \cdots & 0 & \cdots & 0 & \cdots & 0 \\
0 & \cdots & 0 & \cdots & 0 & \cdots & Z_{pq}^{A2} & \cdots & Z_{qq}^{A2} & \cdots & 0 & \cdots & -Z_{xx}^{A3} & \cdots & 0
\end{bmatrix}^T
\]

Eq. A- 12

Again, reversal of the current of any link changes the signs of some elements. In Chapter 3, section 3.3 presents an example of how to use this section to generalize MATE.
APPENDIX B

TRANSFORMER DISCRETE-TIME EQUIVALENT

This appendix presents the derivation of the discrete-time equivalent for a two-winding, single-phase transformer using the trapezoidal integration rule [63]. The discrete-time equivalents for multiphase, multi-winding transformers can be easily obtained using these concepts. The use of a different rule of integration is also straightforward.

![Two-winding single-phase transformer with leakage inductance Lt.](image)

For the two-winding single-phase transformer shown in Fig. B-1, using Kirchhoff's Voltage law, we can write:

\[
v_1(t) = L_t \frac{d i_1}{d t} + n v_2 \\

n v_2(t) = \frac{L_t}{n} \frac{d i_2}{d t} + v_1
\]

Eq. B-1

Expressed in matrix form,

\[
\begin{bmatrix}
  d i_1 \\
  d i_2
\end{bmatrix} = \frac{1}{L_t} \begin{bmatrix}
  1 & -n \\
  -n & n^2
\end{bmatrix} \begin{bmatrix}
  v_1 dt \\
  v_2 dt
\end{bmatrix}
\]

Eq. B-2
Using the trapezoidal rule to discretize Eq. B-2,

\[
\begin{bmatrix}
    i_1(t) - i_1(t - \Delta t) \\
    i_2(t) - i_2(t - \Delta t)
\end{bmatrix} = \frac{\Delta t}{2Lt} \begin{bmatrix}
    1 & -n & -n^2
\end{bmatrix} \begin{bmatrix}
    v_1(t) + v_1(t - \Delta t) \\
    v_2(t) + v_2(t - \Delta t)
\end{bmatrix}
\]

Eq. B-3

Equation Eq. B-3 is now rearranged:

\[
\begin{bmatrix}
    i_1(t) \\
    i_2(t)
\end{bmatrix} = \begin{bmatrix}
    G_{11} & G_{12} \\
    G_{21} & G_{22}
\end{bmatrix} \begin{bmatrix}
    v_1(t) \\
    v_2(t)
\end{bmatrix} + \begin{bmatrix}
    h_1(t) \\
    h_2(t)
\end{bmatrix}
\]

\[
\begin{bmatrix}
    h_1(t) \\
    h_2(t)
\end{bmatrix} = \begin{bmatrix}
    G_{11} & G_{12} \\
    G_{21} & G_{22}
\end{bmatrix} \begin{bmatrix}
    v_1(t - \Delta t) \\
    v_2(t - \Delta t)
\end{bmatrix} + \begin{bmatrix}
    i_1(t - \Delta t) \\
    i_2(t - \Delta t)
\end{bmatrix} = 2 \begin{bmatrix}
    G_{11} & G_{12} \\
    G_{21} & G_{22}
\end{bmatrix} \begin{bmatrix}
    v_1(t - \Delta t) \\
    v_2(t - \Delta t)
\end{bmatrix} + \begin{bmatrix}
    h_1(t - \Delta t) \\
    h_2(t - \Delta t)
\end{bmatrix}
\]

Eq. B-4

where:

\[
G_{11} = \frac{\Delta t}{2Lt}, \quad G_{12} = G_{21} = -n \left(\frac{\Delta t}{2Lt}\right), \quad G_{22} = n^2 \left(\frac{\Delta t}{2Lt}\right)
\]

and \(n\) is the transformer ratio \(\frac{N1}{N2}\)

Eq. B-4 can be rewritten in compact form:

\[
\vec{i}(t) = [G]\vec{v}(t) + \vec{h}(t)
\]

\[
\vec{h}(t) = 2[G]\vec{v}(t - \Delta t) + \vec{h}(t - \Delta t)
\]

Eq. B-5