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Date \textit{APRIL 18, 2000}
Abstract

In order to ensure true redundancy, expandability and good reliability of a power supply system, a distributed Uninterruptible Power Supply (UPS) system is required. A distributed UPS system can be realized by connecting many inverters in parallel. A technically challenging aspect of such a system is to develop a flexible control technique for proper load sharing among the parallel connected inverters without control interconnection and in the presence of unit to unit variations and the line impedance imbalances. The primary goal of this research is to develop such a new control technique to achieve a proper load sharing in a distributed fashion.

Existing control techniques to operate inverters in parallel either require some form of control interconnections or do not guarantee the proper sharing of the reactive and distortion power. The interconnecting lines restrict the location of the inverters, and they are sources of noise and failure. In order to obtain a truly distributed power supply system with reliability, redundancy and expandability, these control interconnections will have to be removed.

In this research, a new concept of sharing the reactive and distortion power has been developed. Two small signals, at a frequency other than the power frequency and its harmonics, are injected for the reactive and distortion power sharing in the power supply system. This technique allows proper sharing of both linear and nonlinear load among the inverters without any control interconnections. The technique can also automatically compensate for the differences between the units and the effect of line impedance. Techniques are also developed to enable the units to self-synchronize with the ac bus before connection. A unique method to handle the overload conditions and the constraints on the voltage adjustment band has been developed. In addition, efficient ways of calculating the reactive and distortion power have been developed. The proposed techniques were implemented in a fixed point DSP and were found to work well in a prototype system consisting of two commercial single-phase inverters under various operating conditions.
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Dedicated to my mother who taught me to follow the path of knowledge.
1 Introduction

1.1 Background

The increasing dependency of our life on electronic equipment and computerized systems has demanded highly reliable power supply systems. This is especially true for critical loads such as hospitals, telecommunications, financial institutions, etc. [1,2]. The existing utility system, however, cannot meet such a high reliability requirement as there are voltage sags, brownouts, faults, and scheduled and unscheduled outages. Providing reliable power requires a UPS (uninterruptible power supply) system. A UPS system can consist of a single inverter unit, or several inverters in parallel. The work in this thesis focuses on UPS systems with parallel-connected inverters as they provide higher reliability, greater fault tolerance, and greater expandability as compared to the single-inverter-unit configuration.

The important issues of operating inverters in parallel are synchronizing and load sharing. The lack of synchronizing makes the whole system unstable. Improper load sharing will result in overloading in some units. This increases the risk of failure and reduces the reliability of the system. Improper sharing of reactive power, for example, will worsen the voltage profile of the power supply system, which in turn results in more circulating currents. Therefore, a robust control technique that ensures synchronizing and proper load sharing is essential to ensure the stability and reliability of the system.

Operating inverters in parallel has more applications than just the UPS systems. In recent years, for example, special interest in broadening the application areas of clean energy sources such as solar power, fuel cell and wind turbine is growing. The usefulness of these non-conventional energy sources can be enhanced by connecting them in parallel. S. J. Strong in [29] indicates that every house in the future can produce some (~ 3 kW) electricity by using PV-cells. The power generated by a few close-by houses can be pooled together by using parallel connected inverter system. S. Nonaka reports in [30] that the interconnections of residential PV arrays are already under practical test. One of the limiting factors in such an endeavor is the control interconnection required among the inverters to obtain a proper sharing of load. Therefore, a control method, which allows the units to share the load according to its capacity without any control interconnections, will be very valuable for such a distributed system. These new possibilities of utilizing non-conventional energy sources will not only save financially but also contribute towards a cleaner environment by reducing the consumption of fossil fuel.

Operating several inverters in parallel, however, is not trivial. Not only the output voltage amplitudes and frequencies, but also the phase angles of all the inverters must be perfectly synchronized. Therefore, each inverter must regulate its own output voltage very precisely to avoid imbalances in output currents. The
feedback mechanism must also ensure a balanced output even with nonlinear loads [3] and under line impedance imbalance.

1.2 Problems Addressed

A desired distributed power supply system is shown in Fig. 1.1.

In the figure, $V_{dc}$ is the dc bus voltage, and $Z_i$ is the connecting line impedance of the $i^{th}$ unit. Key features of this system are:

- There are no control-interconnections between units. This ensures easier installation and higher reliability. Maintenance and inspection of a unit can easily be done without disturbing the system. The system will thus be truly redundant. In addition, there is no possibility of the system being down due to the failure of any one unit.

- Each unit can be of different power rating. This ensures true expandability. There is theoretically no limit on the capacity of the system.

- The line impedance can be different. This ensures the flexibility in terms of the unit location.
The load could be either linear or nonlinear.
Like the inverters, the load can also be distributed.

Such a system presents challenges in the following aspects:

- A proper load sharing among the inverters has to be obtained without knowing the total load in the system.
- The lack of information on the total system load causes difficulty in formulating a performance criterion to develop advanced control strategies.
- Along with the real and fundamental reactive currents, the distortion current from nonlinear loads has also to be shared properly.
- A low output impedance and quick response characteristics make the inverter current change rapidly and thereby easily reach an overload condition if there are any disturbances in the output. This makes the parallel operation of inverters very sensitive to disturbances from the load and other sources.
- Some of the control techniques used for the three phase inverters cannot be used for a single-phase system. For example, the space vector control method.

1.3 Literature Review

There are a number of control techniques for the load sharing of a parallel inverter system in the literature. They can be broadly divided into the following three categories:

- Master/Slave technique.
- Current/Power deviation control technique.
- Frequency and voltage droop technique (without control interconnection).

Most of the methods found in the literature are for three phase systems with linear loads. All of the publications dealing with the nonlinear loads and single-phase system require some form of control interconnections to achieve a proper load sharing.

1.3.1 Master/Slave Technique
Master/Slave configuration generally uses a voltage controlled PWM inverter as the master unit and current controlled PWM inverters as the slave units. The master unit maintains the output voltage sinusoidal, and generates proper current commands for the slave units. One configuration of the Master/Slave technique is depicted in Fig. 1.2.

This configuration has many good characteristics. The system does not need to measure the load current. This makes the system easily expandable. The line impedance of the interconnecting lines does not affect the load sharing. There are, however, a few serious disadvantages. One of the major disadvantages is that the system is not truly redundant, and there is a single point of failure. If the master unit fails, the whole system shuts down. Another disadvantage of this configuration is that the stability of the system depends upon the number of slave units in the system [4].

The reliability of the system is also reduced as the communication wire, which is needed from the master unit to all the slave units, is fault prone. Furthermore, the system is not truly distributed as the master unit
maintains the sinusoidal voltage only at a single load point. Another Master/Slave configuration has been suggested by Jiann-Fuh Chen and Ching-Lung Chu [2]. The system is shown in Fig. 1.3. In this configuration, a distribution center is used to generate the set points for the slave units. It measures the total current and distributes among the slave units. The master unit just maintains the sinusoidal voltage at the output. The advantage of this configuration is that the delicate line carrying the current set point comes from the power distribution board near the load, hence can be run along with the power cable.

This technique gives very good load sharing despite the presence of line impedance and is straightforward to design and implement. The disadvantages, however, are that the system is not truly redundant since a failure in the master or the power distribution center will shut down the whole system.

Holtz et al in [5] suggested using a microcomputer to detect the faulty unit and make one of the healthy units as the master. In this way the redundancy is maintained even with a Master/Slave configuration. Petruzzello et al in [6] described a Master/slave configuration using a rotating priority window which provides random selection of a new master and therefore results in true redundancy.

Chiang et al in [7] discusses a different Master/Slave controller configuration for a multi-module parallel operation of a battery energy storage system. Fig. 1.4 depicts the configuration. It contains a master controller, n slave controllers and n inverter modules. The master controller generates the current

![Fig. 1.3. Combined voltage and current source inverters.](image)
reference signal for the power distribution controller. The power distribution controller generates the current command for each slave module by weighing current signal according to the unit capacity and the load management strategy.

Each slave module consists of the current forced switching scheme which generates the gating signals for the power modules as illustrated in Fig. 1.5.
The current forced switching scheme has good tracking characteristics. Through the use of central power distribution control approach, good transient as well as steady state current sharing characteristics are obtained. However, the need of extensive interconnections makes this scheme less suitable for realizing a distributed power supply system. The system is not redundant and reliable as the failure of the master unit shuts down the whole system.

All these Master/slave techniques, however, need control interconnections, so they are not reliable for a distributed power supply system.

1.3.2 Current/Power Deviation Control Technique

Another paralleling technique found in the literature is the Current Deviation Control technique. In this approach, the total load current is measured and divided by the number of units in the system to obtain the average unit current. The actual current from each unit is measured and the difference from the average value is calculated to generate the control signal for the load sharing. Using a high speed current loop, as suggested by Tamai et al [1], Kawabata et al [8], Oshima et al [9], Hoffmann et al [10], and Vorell et al [11], we can quickly correct the deviations in load sharing. The inverter shown in Fig 1.6 has a high-speed current loop, and therefore there is no possibility of output overcurrent by limiting the current reference [8].
In this approach, the voltage controller adjusts the small voltage deviation and keeps the voltage constant. The ΔI signal is detected and given to the current loop as a correction factor, and the ΔP signal controls the phase of the reference sinewave. The system has many desirable characteristics. A very good load sharing can be obtained. Transient response is very good due to the feed-forward control signal.

Some authors have suggested power deviation control to achieve synchronization and current sharing. In such a scheme, each unity can calculate the real and reactive power delivered to the load. The total load on the system is calculated and divided by the number of units in the system to obtain an average value of power each unit is supposed to put. The deviation of power from the average power is found. The main aim in such an approach is to minimize the deviation in power. It is known that the flow of the real power is mainly a function of the phase angle difference and the flow of the reactive power is mainly a function of the voltage amplitude difference. So the deviation in real power sharing is used to adjust the phase angle of the voltage while the deviation in the reactive power sharing is used to adjust the voltage amplitude. When the deviation in the powers becomes negligible, the circulating current also become negligible. The control block diagram for such a scheme is shown in Fig 1.7 [8].
The system calculates $\Delta i$ which is the difference between the average current signal ($i_L/n$) and the unit current $i_{inv}$. The unit calculates the deviation in the real power $\Delta P$ and the deviation in the reactive power sharing $\Delta Q$ using this deviation in the current signal. The real power deviation $\Delta P$ is used to adjust the frequency of the system to affect the phase and the reactive power deviation $\Delta Q$ is used to adjust the amplitude of the voltage signal $V_c$.

The system has many desirable characteristics. A very good load sharing can be obtained. This reduces the circulating current. However, the need of measuring the load current and total number of inverters in the system reduces the expandability. Also, the system will not be truly redundant and distributed. This technique also does not address the issue of distortion power sharing. Again, the need of interconnections makes the system less reliable.

1.3.3 Frequency and Voltage Droop Technique

Kawabata et al in [12] and Divan et al in [13,14] suggested a completely independent parallel control system by adopting the conventional frequency and voltage droop techniques which have been in use in the utility power systems. Each inverter has its own oscillator and voltage control circuit. It controls its load...
sharing by adjusting the frequency, phase and voltage amplitude according to the voltage and load information at the output bus. Consequently, no common parallel panel or the control interconnections are necessary. There is also no single point of failure.

The concept of this technique is based on the fact that the real power (P) flow in an ac network depends mainly on the power angle, and the reactive power (Q) flow depends mainly on the difference in voltage magnitudes [13]. By controlling the frequency of the inverter, the power angle can be controlled. To avoid overloading, each inverter is set with a predefined frequency droop. By selecting the droop inversely proportional to the ratings of the inverters, a proper sharing of the real power can be achieved. Similarly, by drooping the inverter output voltage, the reactive power sharing can be improved. Divan et al. have suggested a space vector control method to control the load sharing. The entire control of the inverter is performed in the stationary d-q reference frame and is a type of vector control [13]. The control scheme is reproduced in Fig. 1.8.

![Fig. 1.8. Control scheme to operate 3 phase inverters in parallel.](image)

The parallel control system suggested by Kawabata et al. in [12] and Divan et al. in [13,14] results in a truly distributed power supply system. However, these techniques as such work well for three phase systems with linear loads only. Even for the linear loads, the reactive power sharing will suffer significantly if the line impedances of the units are different or the output voltages of the units are not equal. Please refer to Chapter 2, section 2.4 and 2.5 for more details.

There are many US patents on the technique for operating static inverters in parallel. Hamilton holds a patent on operating inverters in parallel without any interconnections [15]. He uses the real and the reactive part of the current signal to adjust the frequency and the amplitude of the voltage to share the load among the parallel connected inverters. The technique is implemented using discrete digital circuits.
Tassitino et al patented a simple technique using the frequency droop to share the real power in [16] without any control interconnections. The invention neglects the imbalance in sharing both reactive and distortion components of the load current. The invention uses the power in the DC side of the inverter which simplifies the power calculation algorithm.

Abbondanti patented a technique [17] based on the frequency and voltage droop to control the current sharing among the parallel connected converters. The invention makes use of a current transformer and phasing circuit to detect the in-phase and quadrature components of the current to control the frequency and the amplitude of the voltage signal. This technique does not share the distortion component of the load current and the voltage droop technique proposed in the patent does not guarantee the sharing of the reactive power when the unit to unit variation as well as the line impedance imbalance are significant.

Divan et al in [18] patented a method and apparatus for decentralized signal frequency restoration in a distributed UPS system. Again the system does not address the issues of the line impedance imbalance and unit to unit variation on the reactive and distortion power sharing.

From the description it is clear that the existing techniques with no control interconnections have adopted the conventional frequency and voltage droop technique used by the utility system with small or no modifications. In order to understand why the conventional techniques are not sufficient for the distributed UPS systems, it is important to consider some of the fundamental differences between the desired system and the utility system. They are outlined below:

- The utility system is three phase while the UPS system is mainly single-phase [19]. Three phase systems offer the ability to resolve a single rotating vector for control purposes. They also allow a simple transformation to derive dc quantities from the AC variables thus making the control easier. Neither of these approaches is available in a single-phase system.

- Most of the deliverable VA from the utility goes into loads that are linear and of fairly good power factor. On the other hand, the UPS often has to deliver its full VA rating into nonlinear loads.

- Synchronous generators used in utilities automatically tend to droop their speed as a function of the output real power. This is not naturally present in inverters.

- Synchronous generators have slow dynamics associated with the field current control - impacting the bandwidth of the voltage control. On the other hand, inverters can have a voltage control loop of much higher bandwidth.

- The utility power lines are mostly inductive (of known value and thus can be canceled by line capacitors where needed) while the power lines on the UPS system are mostly resistive and
not so well known. The inductive lines make it uneconomical to share the reactive VA among the utility generators. The resistive lines on the UPS system do not have this problem.

These differences must be considered before applying the load sharing techniques of the utility system to a localized multi-module UPS grid composed of inverters. The existing paralleling techniques do not consider all these issues so the performance of the system is not optimum. The existing techniques also do not offer a good solution for sharing the reactive powers.

1.4 Proposed Techniques

It has been seen that the conventional voltage droop mechanism does not work well for a distributed power supply system where the units may not be identical and the line impedances may not be balanced. To solve this problem, a new technique has been developed in this thesis.

The basic concept of this new technique came from the careful study of the conventional frequency droop mechanism. It is observed that the real power sharing is always perfect in an ac system despite the line impedance imbalances when the frequency is drooped as a function of the real power output. It is worth noting that the phase angles of the voltages will have to be different at each inverter to provide the same real power if the line impedances are different. It is, therefore, clear that the frequency droop mechanism is able to adjust the phase angles automatically to compensate for the line impedance variations. This property of frequency droop mechanism has been used in the new control technique to adjust the voltages automatically to compensate for the line impedance imbalances and share the reactive power properly.

In order to use the frequency droop technique, a voltage signal of a small amplitude (less than 1% of the fundamental voltage and a frequency different from the fundamental frequency) is added to the inverter voltage. The frequency of this injected signal is drooped as a function of the fundamental reactive power output. When the reactive power sharing is not proper, the frequency of the injected signal will change, causing a small real power \( p_q \) to flow in the network. The unit sharing more reactive power will droop its frequency more, causing \( p_q \) to decrease. Making the amplitude of the voltage a function of \( p_q \), the voltage decreases with the increase in the reactive power. The change in the voltage will reschedule the reactive power flow. This, in turn, will change the frequency of the injected signal so that \( p_q \) is changed. This process continues until a perfect balance in reactive power sharing is obtained.

The same idea can be used to share the nonlinear component of the current. By introducing one more voltage signal, the frequency of this new signal can be drooped as a function of the distortion power. Unequal sharing of the distortion power will cause the frequency deviation in this second injected signal,
again causing a small real power to flow. Making the bandwidth of the inverter a function of this small real power, a proper sharing of nonlinear load can also be obtained.

The control algorithm is first verified by carrying out extensive simulations using general simulation packages PSpice, PSIM, and Simulink (MATLAB). The technique is finally implemented in a Digital Signal Processor (DSP) to control a prototype of a parallel system consisting of two commercial inverters. The predicted performance of the system is then verified from the real results. Data from various experimental conditions are presented and analyzed in subsequent chapters.

1.5 Outline of the Thesis

The thesis is divided into 7 chapters. Chapter 2 outlines the control techniques developed for linear and nonlinear load sharing. This chapter explains why the conventional simple droop technique is not sufficient when the line impedances are significant and the load is highly reactive or nonlinear. The chapter then introduces the adaptive droop technique to improve the reactive load sharing. Since the adaptive droop technique does not guarantee the reactive power sharing, another technique, called signal injection method, is proposed which automatically compensates for the unit to unit variations and the line impedance effects. The technique is refined further to account for the noise effect and other factors that could influence the system stability. The control loop stability and design of the signal injection technique are discussed in Chapter 3. Chapter 3 also includes details on an anti-windup mechanism to address the stability problem arising from the saturation of the voltage adjustment band and the bandwidth adjustment band. The software implementation aspect of the proposed control technique is given in Chapter 4. The hardware implementation of the control technique is explained in Chapter 5. Experimental results are presented in Chapter 6 to validate the proposed control technique. Conclusions and future work are presented in Chapter 7.
2 Proposed Control Techniques

2.1 Introduction

This chapter explains the control techniques developed to share the load in a distributed power supply system composed of single-phase inverters. It is organized as follows: Section 2.2 explains the basic control technique developed to share the linear load. This technique is derived directly from the existing control techniques in three phase systems. The implementation details are significantly different from the three phase system. This section also shows that, even though the proposed scheme works well for mostly resistive linear loads, it does not work well when the load is nonlinear or highly reactive. Section 2.3 introduces a new concept of bandwidth drooping to share the distortion component of the current due to the nonlinear loads. The effect of line impedance imbalance is explained in detail in Section 2.4. Section 2.5 explains the adverse effect of unit to unit variations on reactive power sharing. The proposed control techniques to share the reactive powers are explained in Section 2.6 which include the adaptive droop mechanism and the signal injection technique. Section 2.7 provides sensitivity analysis to parameter variations for the proposed signal injection method. Section 2.8 explains a new self-synchronizing technique to make the inverter hot-swappable. Section 2.9 summarizes the chapter.

2.2 Linear Load Sharing

In order to understand the linear load sharing, the basic concepts of power flow in an ac system are first reviewed.

Two inverters connected to a linear load through pure inductances are shown in Fig. 2.1. The line impedance is represented by a pure inductance to simplify the analysis.

Fig. 2.1. Two inverters connected to a load.
The complex power supplied to the load by Inverter 1 is given by

\[ \overline{S}_1 = P_1 + jQ_1 = E_1 I_1^* \]  

(2.1)

where \( I_1^* \) is the conjugate of the inverter 1 current and is given by

\[ I_1^* = \left[ \frac{E_1 \cos \delta_1 + jE_1 \sin \delta_1 - V}{jX} \right]^* \]  

(2.2)

\[ \overline{S}_1 = (E_1 \cos \delta_1 + jE_1 \sin \delta_1) \left[ \frac{E_1 \cos \delta_1 + jE_1 \sin \delta_1 - V}{jX} \right]^* \]  

(2.3)

This gives us

\[ P_1 = \frac{E_1 V}{X} \sin \delta_1 \]  

(2.4)

\[ Q_1 = \frac{E_1^2}{X} - \frac{E_1 V \cos \delta_1}{X} \]  

(2.5)

Similarly for the second inverter,

\[ P_2 = \frac{E_2 V}{X} \sin \delta_2 \]  

(2.6)

\[ Q_2 = \frac{E_2^2}{X} - \frac{E_2 V \cos \delta_2}{X} \]  

(2.7)

As shown by (2.4) - (2.7), the real power flow mainly depends on the power angles \( \delta_1 \) and \( \delta_2 \), while the reactive power flow is mostly influenced by the amplitude of the inverter voltages \( E_1 \) and \( E_2 \). To avoid overloading one inverter, each inverter should be able to respond to the load change automatically and share the load proportionally based on its power rating.

Since the inverter is a relatively stiff source, even with a small difference on voltage or the phase angle, large circulating currents would result if they were connected in parallel without additional control. This problem can be mitigated to some extent by introducing some droop in the inverter frequency and voltage. Based on these predetermined droop characteristics, the frequency and the voltage amplitude are obtained as:

\[ \omega = \omega_0 - mP \]  

(2.8)

\[ V = V_0 - nQ \]  

(2.9)
where $\omega_0$ is the frequency at no load, $V_a$ is the voltage amplitude at no load, $m$ is the droop coefficient for frequency $\omega$, and $n$ is the droop coefficient for voltage amplitude $V$.

For the convenience of discussion, the droop characteristics for two inverters of different power ratings are re-displayed in Fig. 2.2.

![Diagram of Frequency and Voltage Droop](image)

**Fig. 2.2. Frequency and voltage droop.**

To ensure proper load sharing according to the inverter rating, the droop coefficients are selected as follows:

$$m_1 S_1 = m_2 S_2 = m_3 S_3 \ldots = m_n S_n \quad (2.30)$$

$$n_1 S_1 = n_2 S_2 = n_3 S_3 \ldots = n_n S_n \quad (2.31)$$

where $S_1, S_2 \ldots S_n$ are the apparent power ratings of the inverters. Because of the droop characteristics, the frequency and voltage of the system will drop to such a value that all units will be operating at new frequency and voltage values, thus reducing the circulating current. More importantly, the concept of droop leads each module to respond to the power flow in a controlled way. The tradeoff of this approach, however, is the deviation in frequency and voltage from the nominal values. In theory, the frequency droop coefficient can be made arbitrarily small but practical concerns will put a lower bound on how small the droop factor can be. The voltage droop coefficient has to be selected carefully. A very small value will result poor reactive power sharing. A bigger value helps to share the reactive power better, but degrades the voltage quality. If the drop in voltage exceeds the allowable limit, the reactive power sharing will be adversely affected. This is especially true when the load is highly inductive. The following vector diagrams (Fig. 2.3) explain this situation.
Fig. 2.3 Vector diagrams for purely inductive and purely resistive load.

Fig. 2.3 shows that the voltage drop across the output/line impedance is in the direction of the load voltage when the load is purely inductive. However, the voltage drop across the line impedance for a purely resistive load is in the direction perpendicular to the load voltage $V_L$. In other words, the natural drop in voltage is higher for the inductive load than for a resistive load. So selecting a higher droop coefficient can potentially exceed the voltage drop limit rendering the droop mechanism ineffective when the load is highly inductive. For further details, please refer to Section 2.4 and 2.5.

The proposed control scheme for the linear load sharing is shown in Fig. 2.4.

Fig. 2.4. Proposed control scheme for linear load sharing.
Fig. 2.4 shows a basic inverter circuit with the conventional inner current loop and outer voltage loop. The load sharing control forms the outermost loop which changes the frequency and voltage magnitude of the voltage reference signal.

The inductor current and the output voltage of each unit are measured and used to calculate the real and reactive power. The frequency and the amplitude of the voltage are adjusted as a function of the real and reactive power, respectively. The technique works like this: when units of the same capacities are connected in parallel, the units may share the load differently due to the non-uniformity in unit parameters and line impedances. According to the technique, we droop the frequency of the unit as a function of the real power output of the unit. Since the sharing is not equal, different units will have different frequencies. This difference in frequencies will integrate over time and gives rise to phase differences between the units. The unit with more power output will droop its frequency more causing its phase angle to decrease over time. Meantime, the unit with relatively less power output will droop its frequency less, so its phase angle will increase over time. Since the real power output is predominantly a function of the phase angle (see Eq 2.4), the unit with more power output will start decreasing its output while the unit with less power output will start producing more power. This self-adjusting process continues until a perfect sharing of the real power is obtained. It is important to note that the real power sharing is not affected by the imbalance in line impedances. This technique automatically adjusts the phase angles as a function of the line impedance to compensate for them and the real power sharing is always proper.

We can visualize a feedback control hidden in this process which is depicted in Fig 2.5. As shown in the figure, any deviation in the real power sharing manifests itself as the frequency deviation due to the frequency droop mechanism. This frequency deviation will integrate over time to give a phase deviation. This phase deviation in turn will reschedule the real power sharing which in turn changes the real power deviation. This establishes a negative feedback loop as depicted in the figure.

![Fig 2.5. Control system representing the frequency droop method.](image-url)
The integrator in the loop gives this system a reset characteristic. The deviation in the real power sharing is always reset to zero irrespective of the line impedance and unit to unit variations. This is a very desirable feature.

We can add the proportional and differential control signals to the control loop which enhance the dynamic behavior of the load sharing. The new control block diagram for the system is shown in Fig 2.6. The deviation in power sharing is multiplied by a constant gain to obtain a proportional control signal. The rate of change in the power sharing can also be used to adjust the phase angle directly to realize a differential control signal.

![Fig 2.6. Improved implementation of the frequency droop technique.]

It is clear from the above analysis that the real power sharing is always proper.

Now the reactive power sharing system is analyzed. Eq. (2.5) shows that the reactive power flow is mainly a function of the voltage amplitude. When we droop the amplitude of the voltage as a function of the reactive power output of the unit, we establish a feedback loop which is depicted in Fig 2.7.

![Fig 2.7. Control structure for the voltage droop technique.]

It is clear from the above analysis that the real power sharing is always proper.
The control loop is a proportional one and does not have an integrator in the loop. We can reduce the error in the reactive power sharing by increasing the droop coefficient \( n \). However, we cannot share the reactive power perfectly with this simple droop technique. Furthermore, the limitation on the maximum allowable droop in the output voltage will affect the reactive power sharing.

Besides the poor performance of the simple droop mechanism in sharing the reactive power, the technique also does not help to share the harmonic currents. Depending upon the nature of the load, the harmonic content of the current can be very high. If we do not share the harmonic components properly, the overall sharing of the rms current will suffer.

### 2.3 Nonlinear Load Sharing

As explained above, the simple droop technique works well for linear and mostly resistive loads. The harmonic current resulted from nonlinear loads cannot be shared by drooping the fundamental component of the voltage alone.

The total harmonic distortion for typical nonlinear loads (for example, rectified capacitor loads such as most dc power supplies) can be as high as 150\%. That is, the rms sum of the current harmonics is 1.5 times the magnitude of the fundamental current. If the paralleled modules cannot ensure sharing of these harmonics, the system needs to be severely de-rated in the presence of nonlinear loads.

Like the fundamental reactive power, the distortion power also increases the apparent power. But unlike the fundamental reactive power, the distortion power cannot be compensated by using a simple capacitor or a reactor. There still does not exist a satisfactory physical interpretation of this power [32].

This power can, however, be related to the apparent power mathematically. The inverter voltage and current are given by (2.34) and (2.35), respectively. The inverter voltage is assumed to be purely sinusoidal while the current can have any number of harmonics.

\[
e_1 = \sqrt{2} E_1 \sin \omega t \tag{2.34}
\]

\[
i_1 = \sqrt{2} \left( I_1 \sin(\alpha - \phi_1) + I_2 \sin(2\alpha - \phi_2) + \ldots + I_n \sin(n\alpha - \phi_n) \right) \tag{2.35}
\]

where

\[
I_n : \text{rms values of current components}
\]

\[
\phi_n : \text{phase angles between the currents and the output voltage.}
\]
The instantaneous power is given by:

\[ p = e_i i_1 = E_1 I_1 \cos \phi_1 - E_1 I_1 \cos(2\omega t + \phi_1) + E_1 \sum_{j=2}^n I_j \sin \omega t \sin(j \omega t + \phi_j) \] (2.36)

The first term in the right hand side of (2.36) is the real power. The second term indicates the presence of fundamental reactive power. The third term indicates the harmonic reactive power (distortion power). It is therefore clear that the distortion power is due to the combination of voltage and current components of unlike frequencies. While there is no real power (avg(V-I) = 0) in these harmonic terms, there are reactive powers in them (V_{rms}I_{rms} \neq 0). This can be shown as follows:

The apparent power \( S \) is given by

\[ S = E_1 \cdot I \] (2.37)

where \( I \) is the rms current defined as:

\[ I = \sqrt{(I_1^2 + I_2^2 + I_3^2 + \ldots + I_n^2)} \] (2.38)

Squaring both sides of (2.38),

\[ S^2 = E_1^2 \cdot I^2 \] (2.39)

Using (2.37) and (2.39),

\[ S^2 = E_1^2 I_1^2 \cos^2 \Phi_1 + E_1^2 I_1^2 \sin^2 \Phi_1 + E_1^2 \sum_{j=2}^n I_j^2 \] (2.40)

\[ S^2 = P^2 + Q^2 + D^2 \] (2.41)

where \( P = E_1 I_1 \cos \Phi_1 \) is the real power, \( Q = E_1 I_1 \sin \Phi_1 \) is the reactive power, and \( D = E_1 \sqrt{\sum_{j=2}^n I_j^2} \) is the distortion power.

Unlike the fundamental reactive power, the flow of the distortion power cannot be influenced by adjusting the fundamental component of the inverter voltage alone. We need to adjust the amplitudes of the harmonic components. Therefore a new method of controlling distortion power flow has been developed. This method reduces the gain of the voltage loop as a function of the distortion power. Fig. 2.8 shows the control mechanism.
By reducing the gain (and bandwidth) of the voltage loop in the presence of distortion components, all the harmonic currents are effectively drooped. In this way, the module with more distortion power output will be discouraged while the modules with less distortion power output will be encouraged to share the current harmonics. The control scheme is shown in Fig.2.9.

\[ V_{ref} = V \cos \omega t \]

\[ V_{ref} = V \cos \omega t \]

\[ V_{ref} = V \cos \omega t \]

\[ V_{ref} = V \cos \omega t \]

Fig. 2.8 Mechanism to share the harmonic currents.

Fig. 2.9 Control scheme which also accounts for nonlinear load.

\[ P = \text{Real power} \]

\[ D = \text{Distortion power} \]

\[ Q = \text{Reactive power} \] (Fundamental)
The downside of this approach is a reduction in the output waveform quality. As is true for all droop-based methods, the higher the droop, the better the sharing, but the lower the output voltage quality. There is a compromise between the waveform quality and the accuracy of the distortion power sharing.

### 2.4 Line Impedance Imbalance

The line impedance imbalance causes the units to provide different reactive power to the load. Fig. 2.10 shows the influence of different line impedance on the conventional droop mechanism.

In this section, we try to quantify this effect in terms of the line impedance, the droop coefficient, and the allowable deviation in the reactive power sharing.

For simplicity, two inverters of the same rating are considered. These inverters are connected to a common load through two different line impedances $Z_1$ and $Z_2$ as shown in Fig. 2.8. The reference voltage to the inverter (hence the output voltage of the inverter) is drooped as a function of its reactive power output. Considering the worst case, when the line impedance and the load impedance are purely inductive, the vector equations become algebraic.

$$V_1 = V_L + I_1 Z_1 \quad (2.42)$$

$$V_2 = V_L + I_2 Z_2 \quad (2.43)$$

where $V_1$, $V_2$, and $V_L$ are the voltages at Inverter 1, Inverter 2, and the load, respectively.

From the definition of droop,
\[ V_1 = E - Q_1 d_q \quad (2.44) \]
\[ V_2 = E - Q_2 d_q \quad (2.45) \]

where \( E \) is the nominal inverter voltage at no load, \( d_q \) is the voltage droop coefficient, and \( Q_1 \) and \( Q_2 \) are the reactive power outputs of the units. From (2.42) and (2.45), we have:

\[ E - V_L = I_1 Z_1 + Q_1 d_q \quad (2.46) \]
\[ E - V_L = I_2 Z_2 + Q_2 d_q \quad (2.47) \]

From (2.46) and (2.47), we have:

\[ I_1 Z_1 - I_2 Z_2 = (Q_2 - Q_1) d_q \quad (2.48) \]

If \( Z_1 \) is twice as big as \( Z_2 \), \( I_1 \) will be smaller than \( I_2 \) but not half due to the effect of droop mechanism (the droop mechanism will try to equalize the sharing). Since \( I_1 \) is less than \( I_2 \) but not half of it, \( I_1 Z_1 \) will always be greater than \( I_2 Z_2 \). Consequently, \( Q_2 \) will be greater than \( Q_1 \). It is also clear from (2.48) that the deviation in \( Q_1 \) and \( Q_2 \) can be made smaller by increasing the droop coefficient, \( d_q \). However, we can never achieve a perfect sharing of the reactive power when the line impedances are not balanced. Some deviation in the reactive power sharing should therefore be accepted.

Assuming the acceptable deviation in the reactive power sharing to be \( x \% \).

\[ Q_2 = (1 + x) Q_1 \quad (2.49) \]

From (2.47) and (2.48), we get

\[ d_q = (I_1 Z_1 - I_2 Z_2) / (x \cdot Q_1) \quad (2.50) \]

Accepting 20% (\( x = 0.2 \)) deviation in the load sharing, we get

\[ Q_1 d_q = 5(I_1 Z_1 - I_2 Z_2) \quad (2.51) \]

This implies that the drop in voltage due to the droop has to be 5 times the difference between the voltage drop across the two line impedances to obtain the sharing of the reactive power within 20%. If the droop found from (2.51) exceeds the permissible voltage regulation range, some compromise will have to be made with the sharing of the reactive power (i.e. \( x \) will have to be increased).

The following plot shows the droop required for different values of \( x \).
Fig. 2.11. Droop required to obtain sharing within an acceptable deviation range when $Z_2=2Z_1$.

A practical method of calculating the voltage drop suggested in [40], shows that the voltage drop across a line carrying 20 A current will be around 9.3 V for a 60% inductive load if a wire size of 10 Standard Wire Gauge and a length of 300 ft is used. If there is another unit at 150 ft using the same wire gauge, the voltage drop across the wire will be 5.6 V (assuming the current to be 20% more). Thus the equation derived above gives us the desired drop due to droop as

$$Q_d = 5\times 3.7 = 18.5 \text{ V}$$  \hspace{2cm} (2.52)

This drop alone is too large to be acceptable. There are extra voltage drops due to the output impedance and the line impedances. The total voltage drop, therefore, is unacceptably high and degrades the quality of the voltage.

### 2.5 Effect of Unit to Unit Variation

Due to the component tolerances and effect of various other factors, no two units will be identical. The parameters of the units will be affected by the operating conditions, age, temperature and other factors
which can easily vary the output voltage of the unit by +/- 3% and the output impedance by a few percentage. Though 3% variation in the output voltage seems to be acceptable for a stand alone unit, its impact on the reactive power sharing will be significant when two or more units are connected in parallel. There will also be a large circulating current. A simple droop mechanism described in Section 2.4 does not help to alleviate this problem. The deviation in load current sharing can easily exceed 50% for highly inductive loads. Two units supplying an inductive load is shown in Fig 2.12.

![Fig. 2.12. Two inverters connected to an inductive load.](image)

The phase angles $\delta_1$, $\delta_2$, the load voltage $V$, and the unit currents $I_1$, $I_2$ can be analytically calculated by using the known parameters such as the rms voltages $V_1$, $V_2$, the line impedances $x_1$, $x_2$ and the load impedance $Z_L$. A MATLAB program has been written to carry out these calculations. The program is provided in appendix IV. The program also accounts for the frequency droop mechanism which ensures that the real power is always shared properly between the units.

Some results are tabulated below to illustrate the effect of unit to unit variations on reactive power sharing. Table 2.1 shows the parameters of the system as well as the results for a balanced case. As expected the reactive power sharing is found to be well balanced.

<table>
<thead>
<tr>
<th></th>
<th>Unit # 1</th>
<th>Unit # 2</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line (output) impedance $X$</td>
<td>0.1 $\Omega$</td>
<td>0.1 $\Omega$</td>
<td>3 + j 2 $\Omega$</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>120 V</td>
<td>120 V</td>
<td>119.1 V</td>
</tr>
<tr>
<td>Phase angle</td>
<td>0.0115 rad</td>
<td>0.0115 rad</td>
<td>0 rad</td>
</tr>
<tr>
<td>Complex current</td>
<td>13.8- 9.1i</td>
<td>13.8- 9.1i</td>
<td>27.5-18.2i</td>
</tr>
<tr>
<td>RMS current</td>
<td>16.5 A</td>
<td>16.5 A</td>
<td>33 A</td>
</tr>
<tr>
<td>Real Power</td>
<td>1637 W</td>
<td>1637 W</td>
<td>3274 W</td>
</tr>
<tr>
<td>Reactive Power</td>
<td>1108 VAR</td>
<td>1108 VAR</td>
<td>2162 VAR</td>
</tr>
</tbody>
</table>

Table 2.2 shows parameters and results for an unbalanced case where the output impedance of one of the units is increased by 5 fold. Because of the real power sharing loop, the phase angles are automatically
adjusted so the real power sharing is still maintained equal. However, the reactive power sharing suffered significantly. This caused the rms currents to differ. The unit currents are off by more than 30%.

Table 2.2 Parameters and results for unbalanced line impedances.

<table>
<thead>
<tr>
<th></th>
<th>Unit # 1</th>
<th>Unit # 2</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output impedance X</td>
<td>0.1 Ω</td>
<td>0.5 Ω</td>
<td>3 + j 2 Ω</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>120 V</td>
<td>120 V</td>
<td>119.1 V</td>
</tr>
<tr>
<td>Phase angle</td>
<td>0.0114 rad</td>
<td>0.0570 rad</td>
<td>0 rad</td>
</tr>
<tr>
<td>Complex current</td>
<td>13.7-15.1i</td>
<td>13.7-2.6i</td>
<td>27.4-17.8i</td>
</tr>
<tr>
<td>RMS current</td>
<td>20.4 A</td>
<td>13.9 A</td>
<td>32.6 A</td>
</tr>
<tr>
<td>Real Power</td>
<td>1621 W</td>
<td>1621 W</td>
<td>3241 W</td>
</tr>
<tr>
<td>Reactive Power</td>
<td>1831 VAR</td>
<td>411 VAR</td>
<td>2104 VAR</td>
</tr>
</tbody>
</table>

Table 2.3 shows the parameter and results when the units have different output voltages and different output impedances. The real power sharing loop is still working well. However, the reactive power sharing loop does not seem to work. Note that one of the units is putting a negative reactive power suggesting a circulating reactive power. This caused the unit currents to differ by more than 40%.

Table 2.3: Parameters and results for unbalanced line impedance and output voltages.

<table>
<thead>
<tr>
<th></th>
<th>Unit # 1</th>
<th>Unit # 2</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output impedance X</td>
<td>0.1 Ω</td>
<td>0.5 Ω</td>
<td>3 + j 2 Ω</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>124 V</td>
<td>116 V</td>
<td>119.1 V</td>
</tr>
<tr>
<td>Phase angle</td>
<td>0.0113 rad</td>
<td>0.0603 rad</td>
<td>0 rad</td>
</tr>
<tr>
<td>Complex current</td>
<td>14.0 - 28.8i</td>
<td>14.9+10.7i</td>
<td>28.9-18.1i</td>
</tr>
<tr>
<td>RMS current</td>
<td>31.9 A</td>
<td>18.4 A</td>
<td>34.1 A</td>
</tr>
<tr>
<td>Real Power</td>
<td>1694 W</td>
<td>1694 W</td>
<td>3503 W</td>
</tr>
<tr>
<td>Reactive Power</td>
<td>3588 VAR</td>
<td>-1129 VAR</td>
<td>2195 VAR</td>
</tr>
</tbody>
</table>

Table 2.4 shows the parameters and results for a worst case scenario when the unit to unit variation of the output voltage is also high, the line impedances are also unbalanced and the load is highly inductive.

Table 2.4: Parameters and results for worst case scenario.

<table>
<thead>
<tr>
<th></th>
<th>Unit # 1</th>
<th>Unit # 2</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output impedance X</td>
<td>0.1 Ω</td>
<td>0.5 Ω</td>
<td>1 + j 3.5 Ω</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>124 V</td>
<td>116 V</td>
<td>120.0 V</td>
</tr>
<tr>
<td>Phase angle</td>
<td>0.0036 rad</td>
<td>0.0195 rad</td>
<td>0 rad</td>
</tr>
<tr>
<td>Complex current</td>
<td>4.52 - 39.7i</td>
<td>4.83 + 8.1i</td>
<td>9.34 - 31.6i</td>
</tr>
<tr>
<td>RMS current</td>
<td>40.0 A</td>
<td>9.4 A</td>
<td>33.0 A</td>
</tr>
<tr>
<td>Real Power</td>
<td>542 W</td>
<td>542 W</td>
<td>1121 W</td>
</tr>
<tr>
<td>Reactive Power</td>
<td>4926 VAR</td>
<td>-928.6 VAR</td>
<td>3794 VAR</td>
</tr>
</tbody>
</table>
As expected the reactive power sharing is very bad. One unit is supplying the reactive power while the currents are off by more than 70%.

Employing the simple droop mechanism with a droop of 4V/ kVAR, we obtain the following results:

Table 2.5: Parameters and results for worst case scenario with a droop

<table>
<thead>
<tr>
<th></th>
<th>Unit # 1</th>
<th>Unit # 2</th>
<th>Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output impedance X</td>
<td>0.1 Ω</td>
<td>0.5 Ω</td>
<td>1 + j 3.5 Ω</td>
</tr>
<tr>
<td>RMS Voltage</td>
<td>112.5 V</td>
<td>113.9 V</td>
<td>110 V</td>
</tr>
<tr>
<td>Phase angle</td>
<td>0.0037 rad</td>
<td>0.0182 rad</td>
<td>0 rad</td>
</tr>
<tr>
<td>Complex current</td>
<td>4.15-21.9i</td>
<td>4.09-7.2i</td>
<td>8.24-29.1i</td>
</tr>
<tr>
<td>RMS current</td>
<td>22.2 A</td>
<td>8.3 A</td>
<td>30.2 A</td>
</tr>
<tr>
<td>Real Power</td>
<td>457 W</td>
<td>457 W</td>
<td>910 W</td>
</tr>
<tr>
<td>Reactive Power</td>
<td>2459 VAR</td>
<td>827 VAR</td>
<td>3140 VAR</td>
</tr>
</tbody>
</table>

The load voltage has dropped to 110 V, but the currents are still off by almost 33%. Reactive power shared by each units are also off by more than 33%. These results show that the conventional simple droop technique does not give a good reactive power sharing and it deteriorates the voltage quality.

2.6 Proposed Methods

As discussed above, with the conventional droop mechanism, a steep droop is required to mitigate the effect of line impedance imbalances or unit to unit variations. This degrades the voltage quality. This section explores two new methods to improve the reactive and distortion power sharing.

The theory developed in this thesis makes the following key assumptions:

- The inverters under consideration have highly inductive output impedance at the power frequency. This assumption is generally true as almost all of the inverters have some filter inductor at its output. This filter gives relatively big inductive impedance to the inverter at the power frequency. Even if the output impedance is very small and mostly resistive, the signal injection method works well. The only thing that needs to be changed in the system is the pairing between the controlled and manipulated variables. In such a case the fundamental frequency will have to be drooped as a function of the reactive power and the injected signal will have to be drooped as a function of the real power.

- The line impedance is reasonable (< 0.5 Ohms). This assumption is realistic as any impedance higher than 0.5 Ohms will cause excessive voltage drop at the full load which is not acceptable. Even if the
line impedance exceeds 0.5 Ohms, the technique does not become unstable. The unit having higher impedance will share less power than the other units.

- Inverters use inner current loop and outer voltage loop configuration. This assumption allows the adjustment of the voltage loop bandwidth easily. However, this assumption is not mandatory for the proposed signal injection method.

- The outer voltage loop has enough phase margin so that the adjustment of the bandwidth by 50% does not affect the stability of the loop. This assumption is crucial. However, it is important to note that the bandwidth adjustment will be required whenever there is a nonlinear load and nonlinear load reduces the bandwidth of the system so provides enough margin for the adjustment.

- The A/D has enough resolutions to detect the small real power due to the injected signal.

2.6.1 Adaptive Droop Mechanism

The conventional droop mechanism is sensitive to the line impedance imbalance and unit to unit variations. Any imbalance in the line impedance or the unit to unit variations will cause a significant deviation in reactive power sharing. The sharing can be improved to some extent by increasing the droop. There is, however, a limit on the maximum permissible droop. In order to make the sharing better for all types of line impedance imbalances, the maximum permissible droop will have to be used. As a result, the unit will droop its voltage even when the line impedance are well balanced.

An adaptive droop mechanism has been developed to solve some of the problems mentioned above. This mechanism droops the voltage of the unit as a function of the line impedance. With this mechanism, the unit with more line impedance will droop its voltage less while the unit with less line impedance will droop more. Thus the line impedance imbalance will be compensated to some extent and a much better sharing of the reactive power is obtained. The idea is shown in Fig. 2.13.
In the figure, the voltage of unit 1, which has more line impedance, is drooped less \( d_1 \) while that of unit 2 having less impedance is drooped more \( d_2 \). A significant improvement in reactive power sharing is observed.

In the proposed adaptive droop mechanism, the droop coefficient consists of two parts: a constant part which is the same for all units and a variable part which adjusts its value as a function of the information on the line impedance. If line impedances are small and well balanced, the droop will be small and constant. When the line impedances are different, the second part of the droop will become different causing each unit to put proper reactive power.

With this technique, a very good control of reactive power sharing can be obtained if the values of line impedances are precisely known. However, the line impedances are not known so we need some ways to derive this information.

The information on the line impedance imbalance can be obtained from the output voltage itself. It is clear from (2.5.3) and (2.5.4) that the unit with less reactive power output will have higher output voltage than the unit with more reactive power output. Thus the imbalance in the reactive power flow (or line impedance) manifests itself as the difference in inverter output voltages. The deviation of the inverter output voltage from a fixed common reference voltage signal, \( E \), can, therefore, be used as a piece of information to adjust the droop. If the deviation \( (E - V_1) \) is high, the unit is providing more reactive power, so its droop has to be increased more. If the deviation is small, the unit is providing less reactive power, so the droop has to be increased less.

\[
\begin{align*}
    d_1 &= d_q + K.(E - V_1) \\
    d_2 &= d_q + K.(E - V_2)
\end{align*}
\]
The proportional constant, $K$, has to be selected carefully. A very small value will make the mechanism ineffective at light loads, while a large value will cause an excessive droop at the higher loads. The sensitivity of the droop mechanism towards the voltage deviation can be increased by using the following nonlinear relationship.

The square term makes the droop more sensitive to the variation in the voltage deviation. The square root term makes the droop moderately high even for the light load condition. The constants $K_1$ and $K_2$ should be carefully selected. Increasing $K_1$ will make the system more sensitive to the light load but causes more deviation in the heavy load conditions. The reverse is true for the higher value of $K_2$.

The level of the output voltage can be improved by boosting the output voltage of all units as a function of the real power output. Since the real power sharing is always perfect, the boost obtained in each inverter will be the same. Therefore the sharing of reactive power will not be affected. An analytical model for the load flow in a two unit system has been derived and a simulation program has been written in MATLAB codes. Simulation results show a good sharing of reactive power for up to 5 times difference in line impedances. The simulation used $d_q = 0.002$, $K_1 = 0.00274$, and $K_2 = 2.25 \times 10^6$. These values are found to give good sharing of load from 30% to 150% of the full load.

One of the problems associated with this technique is the requirement of a very accurate sensing of the voltage deviation. Any error in the reference voltage signal or the output voltage signal will adversely affect the adaptive mechanism.

It is interesting to note that there are other two pieces of information locally available which indicate the imbalances in the line impedance. One is the reactive power itself (or the reactive power margin) and the other is the power factor seen by each unit.

The output voltage can be drooped as a function of the reactive power. At the same time, the voltage can be boosted as a function of the power factor ($\text{pf}$) seen by the unit. Since the unit putting more reactive power will see a smaller power factor, the boost will be small for that unit but the unit putting less reactive power will boost its voltage more. This improves both the output voltage quality as well as the sharing of load. The expression for the droops are given in (2.57) and (2.58).

\begin{align}
  d_1 &= d_q + K_1 \sqrt{E - V_1} + K_2 (E - V_1)^2 \\
  d_2 &= d_q + K_1 \sqrt{E - V_2} + K_2 (E - V_2)^2
\end{align}

\begin{align}
  d_1 &= d_q + K_4 \cdot Q_1 - K_9 \cdot p f_1 \\
  d_2 &= d_q + K_4 \cdot Q_2 - K_9 \cdot p f_2
\end{align}

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The constant droop $d_q$ and gains $K_q$ and $K_p$ are to be selected carefully. The attractive features of this mechanism are the local availability of information, simplicity in concept, and implementation.

But the pieces of information used are not accurate representation of the line impedance so the method improves the sharing to some extent but does not guarantee perfect sharing. The need of higher precision on the voltage signal or the power factor signal imposes some practical problems.

### 2.6.2 Signal Injection Method

It has been shown that the conventional voltage droop mechanism does not work well for a distributed power supply system where the line impedances are not necessarily well balanced. The adaptive droop mechanism can improve the load sharing but does not guarantee perfect sharing. So a new method has been developed. This method adjusts the voltages of the inverters automatically until perfect sharing of reactive power is obtained, despite the line impedance imbalances.

The concept of this new technique came from the conventional frequency droop mechanism. In the conventional frequency droop mechanism, the frequency of a unit is drooped as a function of the real power output. The unit with more real power output will droop the frequency more so that the relative phase angle of the inverter voltage will decrease. As a result, the real power flow will decrease. Since the frequency is drooped as a function of the real power, the change in power is reflected on the frequency, causing the phase angle to change again. This process of adjusting the phase angle continues until a perfect sharing of real power is obtained. The perfect sharing obtained by this mechanism is generally attributed to the natural tendency of a network to settle to a unique frequency. This, however, is not strictly true. There is no natural reason why the frequency of a network has to be unique. The self-organizing property is not coming from the natural tendency to equalize the frequencies but from the logical combination of three things in the system: the droop, the relationship between the frequency and the phase angle, and the relationship between the phase angle and the real power flow. If we could have a similar relationship between the variables associated with the reactive power flow, a perfect sharing of this power can also be achieved.

In order to impart this self-organizing property to the reactive power sharing loop, a small signal is injected and combined with the voltage reference of the inverter at the fundamental frequency. The frequency of the injected signal is drooped as a function of the reactive power output of the unit. When the reactive power sharing is not equitable, the frequency of this injected signal for all the units in the system will be different. This difference will integrate over time causing the phase difference to appear. This phase difference will then cause some current at the injected signal frequency to flow in the system. This current is detected and the
small power in the signal is calculated. It is to be noted that the small real power is locally measurable but it conveys information on the phase difference which is locally not available. This signal is then used to adjust the voltage of the system. Unlike the conventional concept, the voltage of the system is boosted as a function of this small real power. As the voltage is adjusted, the distribution of the reactive power sharing will be rescheduled which in turn changes the frequency of the injected signal differently. This process continues until an equitable sharing of the reactive power is obtained.

Let us consider two units each sharing \( Q_1 \) and \( Q_2 \). The injected frequency \( \omega_q \) for these units as per the droop concept, the actual frequencies for the units will then be given by the following equations:

\[
\begin{align*}
\omega_{q1} &= \omega_{q0} - Q_1 B_q \\
\omega_{q2} &= \omega_{q0} - Q_2 B_q
\end{align*}
\] (2.59) (2.60)

where \( \omega_{q0} \) is the reference frequency for the injected signal and \( B_q \) is the frequency droop coefficient.

The error in frequency as seen by the unit 1 will be \( \Delta \omega_1 = \omega_{q1} - \omega_{q2} \). This will integrate over time to give a phase difference \( \delta_1 \):

\[
\delta_1 = \int \Delta \omega_1 \, dt 
\] (2.61)

This phase difference will cause a small real power to flow:

\[
p_{q1} = \frac{1}{X} \sin \delta_1
\] (2.62)

where \( X \) represents the reactance of the circuit for the injected signal \( v_q \) which includes the output impedances of the units and the line impedances. Though the line impedances are predominantly resistive, the output impedances of the units are comparatively bigger and predominantly inductive at the injected signal frequency hence the symbol \( X \) is used here.

We use this power to adjust the voltage amplitude as follows:

\[
V_1 = 170 + b_v \cdot p_{q1}
\] (2.63)

where \( b_v \) is the voltage boost coefficient.

Let us assume that \( Q_1 > Q_2 \). Then \( \omega_{q1} < \omega_{q2} \). So \( \Delta \omega_1 \) will be negative. This will make \( p_{q1} \) negative assuming that \( X \) is much smaller than the load impedance.

On the other hand, the same logic will make \( \Delta \omega_2 \) positive, making \( p_{q2} \) positive. So as desired, the unit putting more \( Q \) will start decreasing its voltage while the unit putting less \( Q \) will start increasing its output voltage. This process continues until a proper sharing of \( Q \) is achieved. The process can be represented in a control block diagram as shown in Fig. 2.14.
In the figure, the controlled quantity is the deviation in Q sharing. This quantity should be zero in the steady state, hence the set point for the control loop is shown as zero. Any deviation will cause the frequency deviation, which in turn is integrated to give a phase difference. The filter block after the phase block represents the low pass filter required to extract the small real power in the injected signal. The gain block after the filter represents the gain of the circuit. The gain block $G$ represents the reactive power gain of the system for a unit variation in the voltage. This is mainly a function of the total impedance of the system.

In the real life, the load impedance can be quite small, so $p_{q1}$ and $p_{q2}$ both will have some positive portions especially when the load is higher. This automatically boosts the voltage nullifying the natural drop in voltage due to the output impedance of the unit. This is a very desirable effect.

We can apply the same approach to share the distortion power. We droop the frequency of the second injected signal $\omega_d$ for the both units as follows:

$$\omega_{d1} = \omega_d - D_1 B_d$$  \hfill (2.64)  
$$\omega_{d2} = \omega_d - D_2 B_d$$  \hfill (2.65)  

where $D_1$ and $D_2$ represent the distortion power output of the units and $B_d$ is the frequency droop coefficient.

The same explanation holds true for the distortion power sharing loop. The small real power $p_{d1}$ and $p_{d2}$ are used to adjust the bandwidth of the voltage loop to change its gain in the high frequency range effectively.

Fig 2.15 shows the details of the signal injection method.
One of the key blocks in the proposed control technique is the power component calculation. Fig 2.15 also shows the detailed block diagram for the power calculation. The reference voltage signal \( v \) is first phase shifted to coincide with the output voltage signal. This signal is then multiplied with the inductor current to obtain the instantaneous power, and consequently the real power after filtering. Similarly, the voltage signal at quadrature to the reference voltage signal is phase shifted and multiplied by the inductor current to obtain the reactive power. The distortion power is obtained by calculating the apparent power, and then subtracting the real and reactive power from it. In order to find the apparent power, the mean square value of the current is required. In order to calculate the mean square current, the current signal is first sampled at 4098 Hz, re-sampled at 227 Hz, and squared. The square value of the current is accumulated for 5 cycles. The mean square (MS) is found by shifting the sum by a proper number of bits. Once the MS current is known, the square of the apparent power is calculated. The square of the real power and the square of the reactive power are subtracted from the square of the apparent power to yield the square of the distortion power. Now finding the square root of this quantity will give us the distortion power.

Fig. 2.15. Schematic diagram of implementing the signal injection technique.
Another important block in the proposed control technique is the signal extraction block. Fig 2.16 shows the detailed block diagram to extract the current due to the first injected signal. The most challenging aspect of this task is the very low level of the current due to the injected signal and the presence of a large current at the power frequency. Due to the small signal to noise ratio, a simple method of filtering will not be able to yield better results. Hence a PLL type of algorithm has been developed to address the problem.

\[ u_q = \cos \omega_q t \]

As shown in the figure, the inductor current is first multiplied by the phase shifted injected signal \( u_q \). The product is filtered to yield the amplitude of the current in phase with the injected signal voltage at the output. This amplitude is multiplied by the unit vector in phase with the injected signal at the output to yield the estimate of the current due to the injected signal. This estimate of the current is then subtracted from the total inductor current. The remaining current is multiplied with the unit vector in phase with the injected voltage signal at the output. This process continues until all the current in phase with the injected signal at the output is extracted. This algorithm has excellent noise immunity. Since there is only one integrator in the loop, unlike the conventional PLL, the system is very stable. Once the small real powers in the injected signals are calculated, the voltage amplitude as well as the bandwidth of the outer voltage control loop is adjusted as a function of the small real power.

Fig 2.17 shows an improved control loop for the reactive power sharing. In the figure \( X_q \) represents the inductive reactance of the system for the injected signal \( v_q \). This includes the output impedance of the unit at the injected signal frequency, the line impedance and the equivalent impedance of the power supply system. \( G \) represents the reactive power gain of the system towards a unit variation in the voltage amplitude.
Fig 2.17. Reactive power sharing control loop.

The lower and upper limit on the voltage amplitude imposes constraints on the control effort. Since there is an integrator in the control loop due to the frequency droop mechanism, the constraints on the voltage amplitude can cause oscillations. This will be clear when we consider an extremely unbalanced situation. Considering a two-unit system where one unit is sharing almost all the reactive power while the other unit is sharing none. According to the proposed control technique, the unit sharing more reactive power will decrease the frequency of its injected signal while the other unit sharing none will keep the frequency of its injected signal the same. The frequency difference will integrate over time and produce a phase difference. This phase difference will cause a small real power circulation. The unit sharing more reactive power will see a negative phase angle while the unit sharing less reactive power will see a positive phase angle.

As mentioned earlier, the phase difference is a remote quantity so cannot be sensed locally. However, the small real power caused by this phase difference can be measured locally. Theoretically the unit sharing more reactive power should see a negative real power while the unit sharing less reactive power should see a positive real power. Since the proposed signal injection method boosts the voltage amplitude as a function of this small real power, the unit sharing more reactive power will start decreasing its voltage while the unit sharing less reactive power will start increasing its voltage. This process will continue and the voltage of the units will continue to change in the opposite direction. Since the system in extremely unbalanced, it is possible that the voltage has already reached its limit but the sharing has not been equalized. Because the sharing is not equalized, the frequency of the injected signals in two units will remain different, hence the phase angle will continue to increase. When the phase angle difference exceeds 90 degrees, the real power flow will start decreasing with the increase of the phase angle. This sudden change of direction in the real power flow will destabilize the reactive power sharing loop. This phenomenon is more complex than the conventional integral windup phenomenon.

To address this problem, an integral anti-windup mechanism is implemented. It is important to realize that since there exists the interaction of more than one unit in the system, it is inconvenient to use the conventional anti-integral mechanism. A new anti-windup technique has been developed. The way it
works is that whenever the limit on the voltage amplitude is exceeded, the extra voltage is detected and multiplied by a suitable gain to calculate the extra reactive power that would have resulted had there been no limit on the voltage amplitude. This extra reactive power is added to the true reactive power of the unit. Thus the mechanism adjusts the reactive power artificially as if there is no limit on the voltage signal. In Fig. 2.17, the block H represents the gain for the anti-windup loop.

Some of the desirable features of the signal injection scheme are:

- The required variation in voltages of the inverters from the nominal value is comparatively small for the load sharing. This is equivalent to a smaller droop/boost in the conventional method.
- The circulating current is very small.
- A very good load sharing is obtained despite the line impedance variations.
- The accuracy of the voltage/current sensor or references is no longer an issue. Instead the frequency reference must be accurate. Crystals with 1ppm accuracy are readily available. This greatly improves the accuracy of load sharing control.
- Units of different capacities can be connected to share the load according to their ratings.
- The lower and upper voltage limits can be set independently for each inverter unit.

2.7 Sensitivity Analysis

2.7.1 Real Power Sharing

The sensitivity of the real power sharing towards the error in the frequency reference signal is studied. As shown in Fig.2.18, the deviation in the real power sharing due to the deviation in the frequency of the reference voltage signal is affected by the magnitude of the droop introduced in the system.
From the figure, the relationship between the droop, frequency and power deviation can be expressed as:

\[ S_r = \frac{\Delta P}{\Delta \omega} = \frac{1}{D} \]  

(2.66)

For a 0.2% full load droop in the frequency (D=0.2%), 0.1% variation in the frequency reference will result in 50% variation in the real power sharing. If the droop is increased to 2%, the real load sharing variation will be 5%, a ten times reduction. Researchers have suggested to use a very accurate (10 ppm) frequency reference source so that a droop of 0.1% is sufficient [10][3]. A frequency source with 1ppm accuracy is readily available. With this accuracy of frequency reference, even a 0.01% droop will be enough to get a good load sharing control.

2.7.2 Reactive Power Sharing

With the conventional voltage droop mechanism, the reactive power sharing is very sensitive to the reference voltage deviations. But the signal injection method is not sensitive to the reference voltage signal error. This is because the signal injection method uses the voltage as an intermediate control signal. The main control signal is the reactive power \( Q \) itself. If the reactive power sharing changes, the frequency of the injected signal changes. This in turn changes the flow of small real power which changes the voltage in such a way that the \( Q \) sharing will again converge to the desired values.
This method is, however, sensitive to the error in the frequency reference of the injected signals. As explained for the real power sharing, its sensitivity can be reduced by selecting a higher droop. Since crystals with the accuracy up to 10ppm are practically realizable, a droop of 0.1% is sufficient.

2.8 Self Synchronizing Control

It is desirable to synchronize the unit to the AC bus before the unit is connected to it. This will reduce the transient disturbances to the interconnected system and also makes the units hot-swappable. The straightforward method to achieve this is to use an analog or a digital PLL technique. However it is desirable to have some technique which could be integrated with the load sharing technique smoothly. So a new frequency locking technique has been developed which can be smoothly integrated with the proposed load sharing control.

2.8.1 Theory of Operation

The technique uses the property of frequency droop mechanism itself to achieve the synchronization. The AC bus voltage $V_{ac}$ is sensed and subtracted from the reference voltage $V_{ref}$ of the unit. This would be the difference in voltage impressed across the output impedance of the inverter if we were to connect the unit to the AC bus. So the current that would flow would be

$$I_{sim} = \frac{V_{ref} - V_{ac}}{jX}$$

(2.67)

The real power that would be resulted by this current can also be calculated. Then the frequency of the inverter can be drooped as a function of this fictitious real power. If the voltages are not in phase, the phase difference gives rise to Isim which in turn changes the fictitious power PS. PS in turn changes the frequency of the unit. This process continues until the synchronization is obtained.

However, calculation of Isim is not straightforward. The reactance X is a complex quantity so we need complex computation to realize Isim. We can get around this problem by using a real number for X. This would cause Isim to be in phase with the voltage difference $\Delta V$ as shown in Fig. 2.19.
The angle between the voltage difference $\Delta V$ and the unit voltage $V_{ref}$ would be $(90 - \delta/2)$. Ideally we want $V_{ref}$ and $V_{ac}$ to coincide. This happens only when $\delta$ is zero. If $\delta$ is zero, then $I_{sim}$ and $V_{ref}$ are out of phase by 90 degrees. This will cause the fictitious power $PS$ to drop to zero. So the controller will not have any synchronizing force as $\delta$ approaches zero. This is not desirable.

This problem can be resolved by introducing some phase shift to $I_{sim}$ by using an all pass filter. Maximum control is obtained by making the filtered current $I_{simf}$ in phase with $V_{ref}$.

We can summarize the synchronization process in the following steps:

- Sense the AC bus voltage.
- Subtract it from the reference voltage to obtain $\Delta V$.
- Divide $\Delta V$ by a number (a fictitious resistance) to obtain $I_{sim}$.
- Filter this simulated current to make it lag the voltage difference by some angle (~90 degrees).
- Calculate the synchronizing power $PS$ by multiplying this current with the reference voltage signal and subsequent filtering.
- Droop the frequency of the unit as a function this synchronizing power $PS$.

Let us assume that the frequency of $V_{ref}$ is more than the frequency of $V_{ac}$ and the $V_{ref}$ is leading $V_{ac}$. This will cause $PS$ to be positive and growing with time as the phase angle increases. This will cause the frequency of $V_{ref}$ to decrease. At one point the frequency of $V_{ref}$ will become equal to the frequency of the AC bus. The phase angle will then assume a small constant value. We can reduce this phase angle by increasing the droop coefficient.
2.8.2 Some Other Issues

Though the method is simple, there are many factors to be considered before implementing this technique in DSP. The most important one is the phase shift associated with the unit itself. The output voltage of the unit will lag behind the reference voltage signal by certain angle. The method outlined above treats the output voltage to be in phase with the reference voltage. So we need to compensate for this angle.

Another factor is in the theory of operation itself. It is true that the frequency droop mechanism has a self synchronizing property, but the property will be lost if the phase difference exceeds 90 degrees. To add to the complication, the system has another equilibrium point besides the near zero phase angle point. This point is where the phase difference is nearly 180 degrees. Both of these problems can be avoided by incorporating a mechanism which forces the phase difference below 90 degrees. If the phase angles are more than 90 degrees or around it, the mechanism forces the system to change the state and come closer to the desired equilibrium point. The measure of the phase difference can be accurately obtained by looking at the maximum amplitude of the $I_{sim}$. This mechanism has been included in the synchronization control loop.

2.9 Summary

The chapter reviewed the conventional droop technique developed for the linear loads. The bandwidth droop technique was introduced to extend the technique to share the nonlinear loads. The undesirable effect of unit to unit variations and the line impedance imbalances on reactive power sharing was discussed. To mitigate these effects, a new concept of adaptive droop mechanism was presented. However, the adaptive droop mechanism was insufficient to achieve a good load sharing among the parallel connected inverters in a distributed fashion. To overcome the problem, the signal injection method was presented. This technique ensures proper sharing of all kinds of loads among the units connected inverters in a distributed fashion despite the unit to unit variations and the line impedance imbalances. Sensitivity analysis shows that, with the signal injection method, both the real and reactive power sharing is sensitive to reference frequency error, but not the reference voltage error. Yet the frequency sensitivity problem can be solved by using a high-precision frequency source. The self synchronization technique presented in this chapter is simple to implement and computationally less demanding than most of the conventional PLL techniques. Since the technique is based on the same frequency droop technique used for the load sharing, a smooth transition from synchronizing phase to the load sharing phase is possible.
3 Stability Analysis

3.1 Introduction

This chapter explores the stability aspect of the proposed frequency droop mechanism and signal injection method. Since the adaptive droop mechanism was not implemented in the prototype system, the stability aspect of that method is also not discussed here. This chapter is organized as follows: Section 3.2 explains the stability of the control loop sharing the real power. Potential sources of instability in the real power sharing loop are identified and solutions are presented. Section 3.3 explains the stability of the reactive power sharing control loop. The main sources of instability are identified and remedies are suggested. Section 3.4 shows the reduction in the system stability due to the variation in the bandwidth of the outer voltage loop to share the distortion power. The interaction between the distortion power sharing loop and the reactive power sharing loop is also discussed. The de-coupling technique for this problem is also presented in the section. Section 3.5 explains the effect of noise on the proposed control techniques. Section 3.6 shows simulation results to illustrate the robustness of the proposed control technique. Section 3.7 summarizes the contents of the chapter.

3.2 Real Power Sharing Control Loop

The frequency droop technique proposed in Chapter 2 to share the real power among the inverters is in many ways similar to the frequency droop technique found in the utility system. There are, however, some differences that have direct influence on the stability of the system.

One of the major differences is the inherent characteristic of the synchronous generators to droop their speeds (frequencies) as a function of the system load. This natural droop is not present in the inverter system. We have incorporated this feature to the system artificially. Despite this there exists differences between the utility system and the inverter system. In the inverter system, there is no rotor or governor dynamics present. This allows faster control of the real power sharing which improves the stability. This fact has been illustrated below with more details.
In the conventional utility system, the load change is reflected on the electrical torque $T_e$ of the generator. This will cause $T_e$ to mismatch the mechanical torque $T_m$. This mismatch in turn results in speed variations as shown in the following block diagram:

\[
\begin{align*}
T_m & \quad \Sigma \quad T_a \quad 1 \\ & \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad 2Hs \quad \Delta \omega_r \\
T_e &
\end{align*}
\]

Fig. 3.1 Block Diagram relating speed and torques.

Where

- $s$ = Laplace operator
- $T_s$ = Accelerating torque in (pu)
- $T_m$ = Mechanical torque in (pu)
- $T_e$ = Electromagnetic torque in (pu)
- $H$ = Inertia constant (MW-Sec/MVA)
- $\Delta \omega_r$ = Rotor speed deviation (pu)

It is shown from the diagram that any deviation in load will change the speed of the rotor. However, there is a time constant associated with the rotor inertia. Also note the presence of integrator in the transfer function. The difference between the mechanical torque and the electrical torque will integrate over time to cause a progressive change in the speed of the system. In order to avoid the progressive deviation of the speed (frequency) from the nominal value, a governor is used. The governor adjusts the input power to meet the demand. If the unit under consideration is a standalone system, it is possible to restore the frequency back to the nominal value through the action of the governor. However, when there are two or more units in the system, it is not possible to restore the frequency back to the nominal value since each unit would have to have precisely the same frequency setting. Otherwise they would interact with each other, trying to control system frequency to its own setting. For stable load sharing between two or more units, the governors are provided with a droop characteristic so that the speed (frequency) drops as the load increases [42]. The block diagram representation of the governor is shown below [42]:

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The output of the governor is used to adjust the valve/gate to adjust the input energy. The control block diagram to represent the above system is shown in Fig 3.3[42].

From the above discussion it is clear that the real power sharing in the utility system is directly affected by the dynamics of the rotor and the governor. The typical values of $H$ and $T_G$ are in seconds. So the real power sharing in the utility system is a slow process.

The inverter system, on the other hand, does not have the natural droop characteristic. The artificial droop introduced to the system has some dynamics associated with the filters used for the power calculations but there are no dynamics associated to the rotor or the governor. This makes the real power sharing in the inverter system much faster.

As discussed in Section 2.2, the real power flow in an ac network is given by the following equation:

$$ P_1 = \frac{E_i V}{X} \sin \delta_i $$

(3.1)
The real power is a function of the $\sin$ of the phase angle $\delta$. For smaller values of $\delta$, the real power can be assumed to be a linear function of the phase angle. However, for bigger phase angles the relationship becomes nonlinear. There are several factors that affect the stability of the real power sharing loop: the droop coefficient, the output/line impedance, the cutoff frequency of the power calculating filters, the voltage amplitudes, and the magnitude of the phase angle. In order to assess the effect of these factors on the stability of the system, we need to reconsider the real power sharing control loop described in Chapter 2. The linear control model is reproduced in Fig. 3.4 for the convenience of discussion.

Due to the droop mechanism, the deviation in the power sharing results in a deviation in the frequency. This frequency deviation integrates over time to give the phase difference. This phase difference in turn reschedules the deviation in real power. Note that the droop coefficient $m$ appears as a gain in the control loop. So it has a significant role in the stability of the real power control loop. The bode plot for the above control loop is shown in Fig. 3.2 below with 5 different values of the droop coefficient $m$ (from $0.001 \text{rad/sec/W}$ to $0.005 \text{rad/sec/W}$). Other parameter are:

$V=120 \text{ V};$ cutoff frequency of the low pass filter $= 10 \text{ Hz}.$; $X = 0.5 \text{ Ohms}$
Fig. 3.5 shows that the given system will become unstable for the droop coefficient equal to 0.005 rad/sec/watt. This droop is equivalent to 4% drop in frequency for a load of 3000 W. Keeping the droop coefficient small will not only reduce the deviation of the frequency from the nominal value but also improves the stability margin. We can choose the droop coefficient as low as 0.0001 rad/sec/watt. This would give us the frequency error as low as 0.08%. However, there is also a limit on the minimum droop coefficient. The accuracy of the crystals used in the oscillators imposes the lower bound on the droop coefficient. For example, if the crystals of the oscillators have an accuracy of 100 ppm (0.01%), the droop coefficient has to be at least 0.1%. This ensures that the error in the real power sharing due to the oscillator crystal error will be reduced to 10%. In fact crystals as accurate as 1 ppm (0.0001%) are readily available in the market.

Similarly, the stability of the system is also affected by the reactance $X$ which represents the output impedance (including the line impedance) of the units. As explained above, selecting a small frequency droop coefficient provides enough phase margin for a wide range of output impedances. For example, in
the above case, we can have a stable system even if the output impedance of the units changes by a factor of 50.

The cutoff frequency of the low pass filter used in the real power calculation has a significant influence on the stability of the real power sharing loop. The bode plots for different cutoff frequencies of the filter are plotted in Fig. 3.6. Other parameter are: V=120 V; m = 0.001 rad/s/W; X = 0.5 Ohms.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{bode_plots.png}
\caption{Bode plots for Filter $f_c = 2$ to 20 Hz}
\end{figure}

It is seen that the lower filter bandwidth for the real power calculation can cause system instability. However, the system has fairly good phase margin when the filter bandwidth is around 20 Hz. It is also important to note that the droop coefficient used for the above analysis is sufficiently high (0.001 rad/s/W).
In the real system, the droop used more than 10 times smaller. Smaller droop coefficient and a higher filter bandwidth increases the stability of the real power sharing loop.

Besides the droop coefficient and the filter bandwidth, the fundamental nonlinear relationship between the phase angle and the real power flow also affects the stability of the system. This situation arises when a large transient load change occurs or some faults develop in the system. The effect of the nonlinearity becomes clear when we consider the following two cases: one is with the linear model and another with the nonlinear model.

Fig. 3.7 depicts a linear model in SIMULINK. Fig. 3.8 shows the effect of a load change of 15 kW on the linear system.

*Fig. 3.7 SIMULINK model for the discretized linear system.*
Fig. 3.8 Response to a step disturbance.

Fig. 3.9 shows a nonlinear model in SIMULINK. Fig. 3.10 shows the response of the nonlinear system to the same transient load change of 15 kW.

![Diagram](image)

Fig. 3.9 Nonlinear model in SIMULINK.

50
Fig. 3.10 The response of the nonlinear system to a step disturbance of 15 kW.

Fig. 3.10 shows that the nonlinearity associated with the phase angle causes instability. Since the nonlinearity is in the phase angle which in turn is the result of the frequency droop, it appears that the higher frequency droop played a role in destabilizing the system. However this is not true. The frequency droop coefficient does not cause this type of nonlinearity. To illustrate this, the droop coefficient of the system is reduced to 0.0005 (20 times smaller) and the response of the system is shown in Fig. 3.11.
Fig. 3.11 Response of the nonlinear system when the droop coefficient is reduced by 20 times.

Fig. 3.11 shows that the reduction of the droop coefficient only delayed the instability but did not stop it. A careful analysis reveals that the instability is arising from the combined effect of the nonlinearity and the insufficient network gain of the system. The network gain is defined as the ratio of the real power flow to the phase angle. It is affected by the output/line impedance and the voltage amplitudes. If the output impedance or the line impedance is big, the network gain will reduce. The reduction of the voltage amplitudes also lowers the network gain. Lower network gain implies smaller real power flow for a given deviation in the phase angles. Therefore, if the deviation in real power sharing is big, the angle will have to be much bigger with a smaller network gain. If the deviation in real power is very big, the angle can easily exceed 90 degrees causing instability.

We can increase the voltage to increase the network gain. Increasing the voltage by 5% would result in the following response.
It can be concluded that the instability arising from the fundamental nonlinear relationship between the phase angle and the real power flow can be avoided by rapidly controlling the voltage amplitude so that the gain of the system increases. This will bring the system back to a more linear region by reducing the phase angle below 90 degrees. The voltage amplitude decides the restoring force. This problem is exactly same as the transient stability problem of the utility system. The solution proposed here is also similar to the reactive power compensation techniques used in the utility system to improve the stability.

### 3.3 Reactive Power Sharing Control Loop

As outlined in Chapter 2, the reactive power sharing loop uses the signal injection method. The signal injection method involves generating a signal at a frequency other than the power frequency, mixing the signal to the fundamental reference signal, detecting the small real power due to this injected signal, and adjusting the voltage amplitude of the unit to influence the reactive power sharing.
The basic reactive power sharing loop is reproduced in Fig 3.13 for the convenience of discussion.

In the above diagram, the low-pass filter represents the filter associated with the signal extraction loop. The signal extraction loop is one of the most important components of the reactive power sharing loop. In order to ensure the stability of the reactive power sharing, the dynamics of the signal extraction loop have to be carefully tuned. The droop/boost coefficients can then be carefully selected to guarantee the stability of the overall loop. The signal extraction loop is analyzed below from the stability point of view.

The signal extraction loop extracts the signal in phase with the injected signal. The load current is multiplied with the injected signal and the output is filtered to obtain a dc quantity that represents the power in the injected signal. Using this quantity and the unit vector in phase with the injected signal, an estimate of the injected current is obtained. This estimate is subtracted from the total current. The remaining current is again multiplied by the unit vector in phase with the injected signal. The process continues until all of the current in phase with the injected voltage are extracted.

Two major design parameters for the control loop are the cut-off frequency of the filter and the gain of the loop. The speed of the signal extraction loop will be limited by the cut-off frequency of the filter. If the cut-off frequency of the filter is high, the ac component in the phase information will be large and it will interfere with the system operation. On the other hand, if the cut-off frequency is low, the response will be slower. In order to ensure small ripples in the phase information, the cut-off frequency of the loop filter is selected to be 5 Hz.

Two filters in cascade are used to attenuate the ripple further. Since the bandwidth of the filter used in the signal extraction loop (5 Hz) is much lower than the bandwidth of the filter used to calculate the reactive power (20 Hz), the later one is neglected.
Once the cut-off frequency of the loop filter is selected, the gain of the loop can be adjusted to obtain a good phase margin. In order to select the loop gain properly, the frequency response of the linearized model shown in Fig 3.14 is studied.

![Linearized model for the signal extraction loop.](image)

**Fig. 3.14. Linearized model for the signal extraction loop.**

The bode plot of the linear system for various gains are studied. Some results are shown in the following table:

<table>
<thead>
<tr>
<th>K</th>
<th>Gain Margin</th>
<th>Phase Margin in degrees</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>3.43</td>
<td>63.89</td>
</tr>
<tr>
<td>10</td>
<td>1.72</td>
<td>36.86</td>
</tr>
<tr>
<td>15</td>
<td>1.14</td>
<td>10.40</td>
</tr>
<tr>
<td>20</td>
<td>Unstable</td>
<td>Unstable</td>
</tr>
</tbody>
</table>

After tuning the signal extraction loop carefully, the frequency droop coefficient $B_q$ and the voltage boost coefficient $b_q$ are selected. The stability of the reactive power sharing loop is affected by these coefficients. It is noted that the frequency droop coefficient $B_q$ must be selected carefully. It should be as big as possible to obtain a good sharing of reactive power. A big value will minimize the sharing error due to the unit to unit variation of the frequency reference crystals. However, the droop coefficient appears as a gain in the reactive power sharing loop, so too bigger a value could cause instability. The slow filter in the loop restricts the higher gain in the loop.
Selecting the voltage boost coefficient $b_q$ is equally important. A small value may cause sinusoidal nonlinearity by failing to correct the reactive power deviations when the phase angle is below 90 degrees. In other words, a small boost coefficient means small variation in voltage for a given change in phase angle. If this change is very small, the deviation in reactive power sharing will not be corrected. If the deviation persists, the frequency droop will cause the phase angle to increase continuously. When the phase angle exceeds 90 degrees, the information on phase angle, $p$, changes its slope and the system will start oscillating. A bigger boost on the other hand may result in the saturation of the voltage amplitude signal. There are maximum and minimum limits on the voltage amplitude. If the voltage reaches these limits, the control is lost and the system will oscillate.

Therefore, the boost coefficient has to meet two conflicting requirements. This problem has been resolved by selecting sufficiently big boost coefficient. This could potentially lead to the saturation problem. However, an integral anti-windup control loop has been employed to avoid the oscillations. The improved reactive power sharing loop is shown in Fig. 3.15.

![Fig. 3.15 Improved reactive power sharing loop.](image)

In the figure, the washout block $W$ is used to improve the transient stability of the system. The block acts as a high-pass filter, with the time constant $T_w$ high enough to pass signals associated with oscillations in the reactive power sharing. In the steady state, the output of the wash-out block will be zero. This block acts as a transient boost mechanism. The transfer function of the wash-out block is given below:

$$T_{wsh} = \frac{sT_w}{1 + sT_w} \quad (3.2)$$

The integral anti-windup mechanism ($H$) is also shown in the diagram. The way it works is as follows: when a unit is sharing less reactive power, the reactive power control loop will increase its output voltage. If the reactive power deviation is very high, the output voltage may reach its limit. But if the sharing is still not equal, the controller will try to raise the voltage even further. However, the saturation will cause the output voltage to remain unchanged. On the other hand, the deviation in reactive power sharing will
continue to produce the frequency deviation which in turn will continue to increase the phase error. When this phase angle exceeds 90 degrees, the controller will start to oscillate.

The conventional method of anti-windup is to set the gain of the integrator to zero so that the control effort is not continuously accumulated. However, in our case the integrator in the control system is arising from the frequency difference between the units which is not locally accessible. So a new method of anti-windup has been developed. In this method, the voltage difference between the actual voltage and the voltage after the limiter is used to generate a signal which is used to droop the frequency of the injected signal. This new signal represents the extra reactive power that would have been put by the unit if there were no limit on the voltage amplitude. Thus we found a method to generate the extra reactive power signal locally so that the frequency of the injected signal is equalized with others. This ensures stability.

### 3.4 Distortion Power Sharing Control Loop

The distortion power sharing loop adjusts the outer voltage loop gain to share the distortion component of the current. This has serious implications on the stability of the system. The distortion power sharing loop is reproduced below for the convenience of discussion.

Since the distortion power control involves adjusting the gain of the inverter voltage loop, it does affect the dynamics of the inverter itself. It is therefore necessary to analyze the dynamic behaviour of the inverter with the proposed harmonic current sharing technique to assess the stability aspect of the proposed harmonic current sharing method.

The inverter stage is a power MOSFET H bridge followed by a LC filter. A simplified schematic diagram of the inverter stage is shown in Fig 3.17.
Fig. 3.17 illustrates a typical control structure consisting of an inner current loop and an outer voltage loop. The set point for the inner current loop is supplied by the outer voltage loop. The harmonic control loop adjusts the current reference signal to share the harmonic currents properly. We will now study the dynamics of the system with this modification.

The dynamics of the inverter is mainly determined by the LC filter and the load connected to the output. The load can be anything from a simple resistive load to a highly nonlinear rectifier type of load. We will consider a nominal resistive load for the derivation of the dynamic model. We will then consider the load variations and model uncertainties as specified load disturbances.

The LC filter with a resistive load can be modeled as a second order system with the inductor current \( i_L \) and the capacitor voltage \( v_C \) as two state variables. Considering the ESR of inductor as \( r_L \) and ESR of capacitor as \( r_c \), we obtain the following state equations:

\[
\begin{bmatrix}
\dot{i}_L \\
\dot{v}_C
\end{bmatrix} = \begin{bmatrix}
\frac{r_L r_C + R(r_L + r_C)}{L(R + r_C)} & \frac{R}{L(R + r_C)} \\
\frac{R}{C(R + r_C)} & -\frac{1}{C(R + r_C)}
\end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_i
\]

(3.3)

The output voltage is given by the following state equation:

\[
v_o = \begin{bmatrix}
\frac{r_C R}{R + r_C} & \frac{R}{R + r_C}
\end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}
\]

(3.4)

These two state equations give us the transfer function for the system as:

58
\[ G(s) = \frac{v_o(s)}{v_i(s)} = \frac{r_RC s + R}{(R + r_c)LC s^2 + \{L + (r_L + r_c)RC + r_Lr_cC\} s + (r_L + R)} \] (3.5)

The output impedance of the system without any load \((R = \infty)\) is given by the following equation:

\[ Z_o(s) = \frac{r_c L C s^2 + (r_c r_L C + L) s + r_L}{L C s^2 + (r_L + r_c)C s + 1} \] (3.6)

If we neglect the ESR of the capacitor and the inductor, we get much simpler expressions for the transfer function and the output impedance of the inverter. The simplified expressions are given below:

\[ G(s) = \frac{v_o(s)}{v_i(s)} = \frac{R}{RLC s^2 + L s + R} \] (3.7)

\[ Z_o(s) = \frac{L s}{L C s^2 + 1} \] (3.8)

It is clear from the output impedance equation that the inverters are highly inductive in the power frequency range. From the transfer function equation, we can derive the following block diagram for the inverter:

![Block diagram of the inverter system without any control loop.](image)

*Fig. 3.18. The inverter system without any control loop.*

After adding the inner current loop, the outer voltage loop and the gain block, \(K_{pwm}\), representing the PWM of the inverter, we obtain the following block diagram:
Where $\alpha$ and $\beta$ are the gains of the current and voltage sensors respectively. The transfer function derived from the above block diagram is given below:

$$T_i(s) = \frac{i_L(s)}{i_L(s)} = \frac{K_{pwm} G_c (RCs + 1)}{RLCs^2 + (L + K_{pwm} G_c CR\beta)s + (R + K_{pwm} G_c \beta)}$$ (3.9)

Now when we use the bandwidth adjustment technique, we introduce a variable gain block in series with the voltage loop controller. Let us represent the variable gain block by $V_G$. The loop-gain transfer function of the voltage loop becomes:

$$LoopTF = \frac{V_G K_{pwm} G_v G_c R}{RLCs^2 + (L + K_{pwm} G_c CR\beta)s + (R + K_{pwm} G_c \beta)}$$ (3.10)

The close-loop transfer function of the outer voltage loop is given by the following equation:

$$T_v(s) = \frac{v_o(s)}{v_o(s)} = \frac{V_G K_{pwm} G_v G_c R}{RLCs^2 + (L + K_{pwm} G_c CR\beta)s + (R + K_{pwm} G_c \beta + VG_c K_{pwm} G_c R \alpha)}$$ (3.11)

The frequency response behavior of different values of $V_G$ are shown in Fig. 3.19. The system under consideration uses the following values for its current loop and voltage loop controllers:

$\alpha = 0.05, \beta = 0.078, K_{pwm} = 26, K_i = 5, T_i = 0.00016667, T_v = 0.0001, K_v = 0.1, L = 0.0012 \text{ H}$

$C = 10 \text{ uF}$,

$$G_c(s) = \frac{K_i (1 + sT_i)}{sT_i}$$ (3.12)
\[ G_v(s) = \frac{K_v(1 + sT_v)}{sT_v} \]  

(3.13)

Five different values of the load resistance are selected to cover a wide range of the load.

Some important results are also tabulated in Table 3.2 through Table 3.5.

---

**Table 3.2. When \( V_G = 0.5 \)**

<table>
<thead>
<tr>
<th>R in Ω</th>
<th>Phase margin</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 (full load)</td>
<td>86.9 °</td>
<td>1612 rad/sec</td>
</tr>
<tr>
<td>10 (half load)</td>
<td>72.6 °</td>
<td>2706 rad/sec</td>
</tr>
<tr>
<td>20 (25% load)</td>
<td>58.4 °</td>
<td>3457 rad/sec</td>
</tr>
<tr>
<td>40 (12.5% load)</td>
<td>50.0 °</td>
<td>3841 rad/sec</td>
</tr>
<tr>
<td>500 (1% load)</td>
<td>41.7 °</td>
<td>4186 rad/sec</td>
</tr>
</tbody>
</table>

**Table 3.3. When \( V_G = 1.0 \)**

<table>
<thead>
<tr>
<th>R in Ω</th>
<th>Phase margin</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 (full load)</td>
<td>83.2 °</td>
<td>3272 rad/sec</td>
</tr>
<tr>
<td>10 (half load)</td>
<td>69.0 °</td>
<td>4916 rad/sec</td>
</tr>
<tr>
<td>20 (25% load)</td>
<td>60.5 °</td>
<td>6160 rad/sec</td>
</tr>
<tr>
<td>40 (12.5% load)</td>
<td>55.0 °</td>
<td>7268 rad/sec</td>
</tr>
<tr>
<td>500 (1% load)</td>
<td>40.4 °</td>
<td>9437.7 rad/sec</td>
</tr>
</tbody>
</table>

**Table 3.4. When \( V_G = 1.5 \)**

<table>
<thead>
<tr>
<th>R in Ω</th>
<th>Phase margin</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 (full load)</td>
<td>78.6 °</td>
<td>4985 rad/sec</td>
</tr>
<tr>
<td>10 (half load)</td>
<td>64.6 °</td>
<td>7356 rad/sec</td>
</tr>
<tr>
<td>20 (25% load)</td>
<td>48.5 °</td>
<td>10035 rad/sec</td>
</tr>
<tr>
<td>40 (12.5% load)</td>
<td>31.0 °</td>
<td>11701.6 rad/sec</td>
</tr>
<tr>
<td>500 (1% load)</td>
<td>13.8 °</td>
<td>12694 rad/sec</td>
</tr>
</tbody>
</table>

**Table 3.5. When \( V_G = 2.0 \)**

<table>
<thead>
<tr>
<th>R in Ω</th>
<th>Phase margin</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 (full load)</td>
<td>73.2 °</td>
<td>6695 Rad/sec</td>
</tr>
<tr>
<td>10 (half load)</td>
<td>55 °</td>
<td>9920 Rad/sec</td>
</tr>
<tr>
<td>20 (25% load)</td>
<td>32.4 °</td>
<td>12678 Rad/sec</td>
</tr>
<tr>
<td>40 (12.5% load)</td>
<td>17.7 °</td>
<td>13700 Rad/sec</td>
</tr>
<tr>
<td>500 (1% load)</td>
<td>3.8 °</td>
<td>14355 Rad/sec</td>
</tr>
</tbody>
</table>

---
The tables show that, as the gain of the loop is increased from 1 to 2, the phase margin for the light load condition dropped from 40 degrees to 4 degrees. This implies a potentially detrimental effect on the stability. However, it is important to notice that the bandwidth adjustment is required only when the distortion load on the system is heavy. Above results clearly show that the phase margin is exceptionally good when the load is heavy. So the bandwidth adjustment technique proposed here does not really pose any serious problem.

Bode plots for $R_L = [5, 10, 20, 40, 500] \Omega$

![Bode plots](image)

**Fig. 3.20** Frequency response of the voltage control loop for different loads when $V=1.5$.

Furthermore, a limit on $V_a$ has been imposed to ensure a good phase margin for all possible situations. $V_a$ is allowed to vary from 0.5 to 1.5 only. The frequency response for different loads when $V_a$ is 1.5 is plotted in Fig. 3.20.
3.5 Noise Effect

Since the injected voltage is just 1% of the fundamental voltage, depending upon the network impedance and the phase mismatch, the current resulted from the injected signal can be very small. Therefore, the signal extraction loop to detect the currents should be sensitive enough to detect the currents. At the same time it should also be robust enough to avoid any undesirable effects of noise. A noise source is added to the nonlinear model. The resulted system is shown in Fig. 3.21.

![Diagram](image)

*Fig. 3.21 Noise added to the signal extraction loop.*

The input corrupted signal as well as the extracted signal are plotted in Fig. 3.22.
Fig. 3.22 Noisy input and clean extracted signal.

Fig. 3.22 shows that the signal extraction loop is able to extract the signal accurately even from the noisy signal. The noise used in this simulation is a continuous white noise bandlimited to 5 kHz.

3.6 Simulation Results

Simulation results are presented below to illustrate the problems and the remedies discussed in this chapter. PSIM has been used for the simulations.

Fig 3.23 depicts a PSIM model of a two-unit system with distributed load and different line impedances.
3.6.1 Case I: Balanced Line Impedances and Output Voltages

The parameters used during the simulation are listed below:

\[
Z_1 = 0.005 + j0.08 \, \Omega, \quad Z_2 = 0.002 + j0.04 \, \Omega, \quad Z_3 = 0.003 + j0.04 \, \Omega, \quad Z_{L1} = 1000 + j10 \, \Omega, \\
Z_{L2} = 1000 + j10 \, \Omega, \quad C = 6000 \, \mu F, \quad R_l = 10 \, \Omega, \quad Z_{L3} = 5 + j5 \, \Omega
\]

\[V_{ref1} = 8.5 \, V, \quad V_{ref2} = 8.5\]

The load is shared perfectly between the units. The reactive power sharing and the voltage reference signals are plotted in Fig 3.24.
Fig. 3.24. Reactive powers and the reference voltages of the units.

Fig. 3.24 shows that the reference voltages are slightly higher than the preset reference value. This is expected due to the presence of the nonlinear load in the system. The huge capacitor in the nonlinear load acts as a sink for the injected signal. This makes a portion of the power in the injected signal always positive for all the units. This has a beneficial effect. The natural drop in voltage due to the loading effect is effectively cancelled by the boost due to the injected power. The reactive power sharing is proper.
3.6.2 Case II: Balanced Line Impedances and 3.5% Voltage Unbalance

The external parameters used for the simulation are:

\[ Z_1 = 0.005 + j0.08 \ \Omega, \ Z_2 = 0.002 + j0.04 \ \Omega, \ Z_3 = 0.003 + j0.04 \ \Omega, \ Z_{L1} = 1000 + j10 \ \Omega, \]
\[ Z_{L2} = 1000 + j10 \ \Omega, \ C = 6000 \ \mu F, \ RL = 10 \ \Omega, \ Z_{L3} = 5 + j5 \ \Omega \]

\[ V_{ref1} = 8.5 \ \text{V}, \ V_{ref2} = 8.2 \ \text{V} \]

Note that the units now have 3.5% variation in their output voltages. It is shown in Fig. 3.25 that the reactive power control technique brings the reference voltage back to the desired value forcing the proper sharing of the reactive power.

*Fig. 3.25 Reactive powers and reference voltages for the parallel connected inverters.*
The reference voltage for the second unit is automatically adjusted to the desired level to obtain a proper sharing of the reactive power.

3.6.3 Case III: Both Line Impedance and Voltages are Unbalanced

The worse case scenario is when both the line impedances and the voltages are all unbalanced. This case is studied below. The external parameters selected for the simulations are:

\[ Z_1 = 0.005 + j0.04 \, \Omega, \quad Z_2 = 0.2 + j0.04 \, \Omega, \quad Z_3 = 0.3 + j0.04 \, \Omega, \quad Z_{L1} = 1000 + j10 \, \Omega, \]
\[ Z_{L2} = 1000 + j10 \, \Omega, \quad C = 6000 \, \mu F, \quad RL = 10 \, \Omega, \quad Z_{L3} = 5 + j5 \, \Omega \]

\[ V_{ref1} = 8.5 \, V, \quad V_{ref2} = 8.2 \, V \]

A very good sharing in current is obtained despite the line impedance as well as the unit to unit voltage variations. The reactive power sharing and the reference voltages of each unit are plotted in Fig. 3.26.

Fig. 3.26 The reactive powers and reference voltages of the parallel connected units.
It is evident from the plot that the reactive power control loop adjusts the reference voltage automatically to obtain a proper sharing of the reactive power. Irrespective of the initial reference voltages and the line impedances, the units will eventually assume proper voltages to share the reactive power.

### 3.6.4 Case IV: Over Loading

The load on the system is deliberately increased to see its effect on the sharing. The unbalance in line impedances is also increased. The external parameters used for the simulations are:

\[
Z_1 = 0.005 + j0.04 \, \Omega, \quad Z_2 = 0.3 + j0.04 \, \Omega, \quad Z_3 = 0.4 + j0.04 \, \Omega, \quad Z_{L1} = 100 + j10 \, \Omega, \quad Z_{L2} = 100 + j10 \, \Omega
\]

\[C = 9000 \, \mu F, \quad R_L = 2 \, \Omega, \quad Z_{L3} = 2 + j2 \, \Omega, \quad V_{ref1} = 8.5 \, V, \quad V_{ref2} = 8.2 \, V\]

*Fig. 3.27 Reactive powers and reference voltage signals for the parallel connected inverters.*
It is found that the integral anti-windup mechanism detects the limit on the voltage amplitude and adjust the reactive power sharing in such a way that the unit facing higher impedance and having lower output voltage will share less reactive power. This prevents the system from instability.

The anti-winding control loop is now disabled to see the problems associated with the saturation effect due to the limits imposed on the voltage amplitude. The following figure shows the reactive power sharing and the reference voltage signal for the units:

![Graph](image)

**Fig. 3.28 Reactive powers and reference voltages of the parallel connected units.**

The figure shows that the reference voltages are oscillating and the reactive power sharing is badly affected by this.
3.7 Summary

This chapter outlined the stability aspects of the proposed control techniques. Real power sharing loop can become unstable when the frequency droop coefficient is too big or when the bandwidth of the lowpass filter used for the power calculation is too small. A big transient load can also cause instability due to the phase angle nonlinearity. It was illustrated that increasing the voltage even by a small percentage improved the transient stability significantly. The proposed technique uses the concept of voltage boost instead of droop, hence the stability of the system is much better with the proposed control technique than with the conventional droop technique.

The injected signal voltage level, the line and output impedances of the inverter system, and the constraints on the voltage amplitudes are some of the factors which can destabilize the reactive power sharing loop. The boost/droop coefficients selected for the frequency and the output voltage also affect the stability of the reactive power sharing system. Selecting a smaller frequency droop coefficient can make the system more stable. Similarly, the selection of the voltage boost coefficient is very crucial for the stability of the reactive power sharing loop. If the value is too small, the phase angle nonlinearity may occur. Too big a value, however, can saturate the voltage amplitude. It is recommended that a big boost coefficient be used and the possible saturation on the voltage amplitude be handled using the anti-windup control technique.

The stability of the distortion current sharing loop is explained by deriving the frequency response behavior of the system. It was shown that the bandwidth could be adjusted by +/-50% without affecting the stability of the system. It was also shown that the phase margin of the system is very good when the inverters are sufficiently loaded.
4 Software Implementation

4.1 Introduction

This chapter explains some of the issues related to the software implementation. Section 4.2 outlines the need of discretizing the control algorithms and sampling the input signals. The selection of the sampling rate and the use of decimation technique to implement the multi rate calculations are highlighted in this section. Section 4.3 explains the need of bandlimiting the signal prior to decimation and explains the design aspects of Finite Impulse Response (FIR) filters. Section 4.4 explains the circular buffer technique employed to reduce the computational time in realizing FIR filters and also explains an efficient square root algorithm to calculate the rms of the load current signal. Section 4.5 gives complete details on the software with relevant flowcharts and timing diagrams. Section 4.6 summarizes the chapter.

4.2 Sampling Rate and Decimation

The control techniques proposed in Chapter 2 are in analog domain. Software implementation of these techniques in DSP requires discretization. Since discretization introduces some delay in the control loops, the selection of a proper sampling rate and proper signal processing techniques becomes very important to ensure the performance and stability of the controller. If a sufficiently higher sampling rate is chosen, the analog control loop can directly be transformed into its discrete counterparts by using Bilinear transformation. This is possible in our system because the bandwidths of the control loops are very low (< 5 Hz). The delay associated with the sample and hold can be neglected if sufficiently higher sampling rate is used. The finite resolution of the fixed point calculations and the finite resolution of the A/D are some other factors which could destabilize the controllers.

Choosing a higher sampling rate improves the accuracy and the stability of the controller. Since the frequency range of interest on one of the inputs (load current) is from 0 to 300 Hz (5th harmonics), theoretically a sampling rate more than 600 Hz is assumed to be sufficiently enough. However, selecting a sampling rate much higher than 600 Hz helps to simplify the anti-aliasing filter design. For example, selecting a sampling rate of 900 Hz would require an anti-aliasing filter that would roll off the gain from unity at or below 300 Hz to -50 dB at or above 450 Hz. This specification can only be met with a very high order filter and it is very difficult to realize such a filter. If we select a sampling rate of 4 kHz instead, the anti-aliasing filter will need to have unity gain at or below 300 Hz and the gain should drop to -50 dB only at and above 2 kHz. It is easier to realize such a filter. So a sampling rate of 4098 Hz has been used for the
prototype system. Since the bandwidth of the load sharing controllers are very small ( < 5 Hz ), the delay introduced by the sample and hold at 4098 Hz has been neglected. All the variables and the constants used in the algorithms have been properly scaled to maintain the numerical stability. The list of variables and their scaling factors are given in appendix III.

For the sampling rate of 4098 Hz, the period between two consecutive samples is just 244 μsec. The DSP under consideration has a computational power of .40 MIPS. This implies that the DSP takes around 25 nanoseconds to execute every instruction. Apparently 244 μsec is not long enough to implement even one hundred instructions. Some of the modules in the proposed control takes more than 200 instructions to complete. So it is not possible to run the controller at 4098 Hz. Since the bandwidth of the controllers are very small, we do not need to run the controller at 4098 Hz. For simplifying the anti-aliasing filter design we have to sample the input signals at 4098 Hz, but we can decimate the signal to a much smaller sampling rate to save the computational time. Most of the calculations involved in implementing the control algorithm can be performed at much reduced sampling rate. For example, the real, reactive, distortion, and injected power calculation can be done at around 200 Hz. However, the signal extraction loop and the rms calculation of the load current need to be done at or above 600 Hz. Therefore, it is needed to carry out the decimation in two stages. In the first stage, we decimate the input signal by a factor of 6 to 683 Hz. In the second stage we decimate it further by a factor of 3 to 227 Hz. The multi-stage decimation also saves the computational time of the DSP by simplifying the design of digital filters needed to bandlimit the signals prior to decimation.

4.3 Filter Design

The simplest way to bandlimit a signal prior to decimation is to use a low pass FIR filter. FIR filters are easy to design and implement. FIR filters have an exactly linear phase response characteristic and are always stable. This allows us to compensate the phase lag introduced to the signal which traverse it. The phase delay for a FIR filter is given by the following relationship:

\[ T_p = \frac{(N - 1) \ast T}{2} \]  

(4.1)

where N is the length of the filter (number of coefficients) and T is the sampling period in seconds. Knowing the filter length, we can calculate the phase shift at any frequency.

In our software one of the inputs is the load current. We are sampling it at a rate of 4098 Hz. Before we resample it at 683 Hz, we need to bandlimit it. We are interested up to the 5th harmonics in the current signal. So we need to bandlimit the signal to 341 Hz so that the decimation process won’t cause aliasing.
Obviously the filter needs to pass the injected signals unattenuated while all the signals above 341 Hz should be effectively attenuated. The frequencies of the injected signals can be any except the fundamental frequency and its harmonics. If we assume the injected signals to be 90 and 130 Hz we need to have a passband of the filter to be at least 130 Hz. Given the cutoff frequency of 130 Hz, the transition width of 211 Hz, and the sampling rate of 4098 Hz, filter coefficients can be calculated. Using the window based FIR filter design method and Hamming’s window, the length of filter N will be 65 to meet the specification given above. We can save some computational time by reducing the number of taps to 55. In order to achieve this, we will have to increase the transition band to 245 Hz. This can only be done if we reduce the pass band frequency from 130 to 100. The frequency response characteristics of a 55 points long FIR filter is shown in Fig. 4.1.

Reducing the passband cause the gain of the filter to drop by 0.3 db (less than 5%) at 130 Hz. This attenuation is tolerable for the second injected signal. This filter introduces some phase shift to the fundamental as well as the injected signals. The phase shift introduced to the fundamental signal is given
by $T_p$ which is: $T_p = \frac{27}{4098}\times 60 = 0.3953$ seconds. Converting into degrees, we have: Phase shift = $0.3953\times 360 = 142.3$ degrees.

This phase shift is also observed in the phase plot shown in Fig 4.1.

Similarly, the phase shift in 90 Hz and 130 Hz signals are 213.5 and 308.3 degrees respectively. These pieces of information are very important as the proposed control techniques are sensitive to the phase shifts in the current signals. For instance, the signal extraction loop extracts the component of the current in phase with the injected signal from the load current.

This is done by multiplying the total load current signal with a vector in phase with the injected voltage signal. The phase angle of the current signal due to the injected signal with respect to the injected voltage is the key information we use to control the voltage amplitude to share the reactive power. Any error in phase angle will affect this loop. A sufficiently big error in the phase angle can potentially destabilize the reactive power sharing loop.

This applies to the power calculation block of the real power sharing loop as well. For the real and reactive power calculations, the current signal is further decimated down to 227 Hz. The phase of the fundamental current signal will suffer further phase shifts.

The effect of phase shift can be compensated by shifting the phase angles of the other signals which interact with these signals. For example, the signal extraction loop requires the current signal be multiplied with a unit vector in phase with the injected voltage signal. If the phase angle of the unit vector in phase with the voltage signal is shifted by the exact amount of the phase lag suffered by the current signal, the control algorithm will remain unaffected. Since the injected voltage signal is locally generated, phase shifting this signal to obtain the unit vector is not difficult. Similarly we can generate the phase shifted versions of the fundamental voltage signal and quadrature voltage signal to calculate the real and reactive powers.

The calculation of the real and reactive power in a single-phase system involves multiplying the voltage and current signals and low pass filtering. IIR filters are used for the filtering purpose. It is easy to realize IIR filters from its analog counter part directly. IIR filters are the most efficient filters as they use only a few coefficients. How IIR filter does not have guaranteed stability so care should be taken while designing an IIR filter.

An IIR filter is also used in the signal extraction loop. Since the current due to the injected signal can be very small but the load current can be very high, a wide dynamic range is required to preserve the current information. This can only be achieved by using floating point variables. So the filters used in the signal extraction loops have floating point coefficients making them computationally intensive.
4.4 Code Optimization

Because of the real-time constraint of the control scheme and the limited computation power of the DSP, the computational time of the control algorithm should be reduced as much as possible. Some of the steps that have been taken to reduce the computational time in the current implementations are explained below.

4.4.1 Use of Circular Buffers

The implementation of FIR filters involves convoluting the coefficient vector with the input signal vector. Since the input is a continuous stream of data, the convolution can be achieved in sections by first storing N input data and convoluting the input vector with the coefficient vector. Every time we receive a new reading, we move all the data in the vector by one step up to make the room for the new data. This shifting process alone consumes almost 1/3rd of the total filter execution time, which is significant.

The computational time can be significantly reduced by using a circular buffer. An ordinary buffer (array) and a pointer to the buffer are required to realize a circular buffer. The following figure shows a circular buffer realization:

![Circular buffer and coefficient vector](image)

The circular buffer pointer first points to $X_0$ of the array and the first input is saved there. As a new value arrives, the pointer is incremented and the new value is saved in the second location. This continues until N (number of filter coefficients) inputs are obtained. After N inputs, the pointer points back to the first location. So the new input will overwrite the oldest input data.

The input data array is then convoluted with the coefficient array. There is, however, a complication in convolution because the starting point of the input vector is not fixed. The convolution involves
multiplying the two vectors where one of the vectors is reversed. In the conventional algorithm, the first location of the input buffer will be multiplied by the last coefficient \( h(N) \). However, with the circular buffer concept, the recent data is saved to a different location. This problem has been resolved by introducing a variable which keeps track of the offset of the newest data from the first buffer location. This offset demands that the coefficient vector is also offset by the same amount to obtain a proper convolution. One way to achieve this is to check the index of the coefficient vector and, as soon as it exceeds \( N \), start from the beginning of the coefficient vector. The need of checking the index of the coefficient slows down the computation to some extent. We can avoid this by doubling the length of the coefficient vector.

4.4.2 New Square Root Function

The calculation of the apparent power requires rms values of the voltage and current signals. The rms value of the voltage signal is known because the signal is locally generated. However, the rms calculation of the current signal involves many mathematical functions such as multiplication, summation and a square root function.

Multiplication and summation are less computationally demanding than the square root function. The square root function found in the compiler library is computationally intensive. For example, one square root function is equivalent to almost 250 summations or multiplication.

It is, therefore, necessary to find a simpler algorithm to calculate the square root. A new method based on a search technique has been developed. The procedure is outlined below:

1. Set the upper and lower bounds arbitrarily.
2. Make a guess for the rms value.
3. Find its square. Compare the result with the mean square (MS) of the variable.
4. If the guess is found to be smaller, the new guess will be the mean of the upper bound and the old guess, and save the old guess as the lower bound.
5. If the guess is found to be bigger than expected, the new guess will be the mean of the lower bound and the old guess and save the old guess as the upper bound.
6. Continue this until the difference between the old guess and new guess is smaller than a designated value (tolerance band).

This algorithm converges to the correct square root value in 1 to 7 iterations with a tolerance of less than 1%. Since the algorithm uses bit shift operator to realize mean values, the computation time is greatly minimized.
4.5 Software Details

The software can be divided into two groups of modules: the initialization and control modules. The initialization modules include hardware initialization module and software initialization module. The control modules include the following modules: self synchronization; negative power detection; power calculation; droop implementation; fundamental voltage signal generation; injected voltage signal generation; signal extraction; filter; decimation; rms calculation; and injected power calculation. The initialization modules are called only once during the start up whereas the control modules, except the self-synchronization module, are called continuously at different sampling rates coordinated by the interrupt. The synchronization module is run only when the unit sees the voltage at its output but the unit itself is not operating in the inverter mode. This happens at the start up or immediately after the trip.

The hardware initializing module sets the interrupt mask register of the DSP so that only the timer interrupt (INT2) is enabled. A sampling rate of 4098 Hz is obtained by writing 0xFA26 in Timer 1 register. For more details on hardware initialization module, please refer to appendix II. The software initialization module initializes the variables used in the control algorithm. After the initialization phase, the program runs a dummy wait loop. As soon as the interrupt occurs, the control jumps to the interrupt service routine, reads/writes input/output channels if they are ready, does all the calculations in the ISR and returns back to the dummy wait loop.

The general software flowchart is shown in Fig. 4.3.

![General Software Flowchart](image)
The timing diagram for the overall software system is shown in Fig 4.4.

![Timing Diagram](image)

Fig. 4.4 Timing diagram for the overall software.

Fig. 4.4 only shows the averaged timing sequence. There are a few control modules which take more than 244 uS so cannot be called at every interrupt. In order to handle such modules, the technique of decimation has been employed. These computationally demanding modules are called only once every six interrupts or only once every 18 interrupts. Fig. 4.5 shows the detailed timing diagram for the software.

![Detailed Timing Diagram](image)

- **Input/output function, fundamental voltage generation, negative power detection and correction, 1st stage pre decimation filtering. Occurring at every interrupt (4098 Hz).**

- **Injected voltage generation, signal extraction, droop implementation, 2nd stage pre decimation filtering, anti-windup mechanism implementation and rms calculation of the decimated current. Occurring at every 6 interrupts.**

- **Real, reactive, distortion and injected power calculations. This module is called every 18 interrupts.**

Fig. 4.5: Detailed timing diagram for the control algorithm.

The timing diagram shows how the decimation technique is employed to run the slow modules on a piece meal basis. At every interrupt, the input/output functions and reference voltage generation are done. As soon
as these calculations are completed, the DSP works on much slower processes at the second level. When another interrupt occurs, the control goes back to the ISR, does essential calculations and comes back to work on the slower modules. The flowchart for the ISR is shown in Fig. 4.6. Description of the flowchart follows the diagram.

*Fig. 4.6. Flowchart for the ISR.*
At every interrupt, the routine checks the interrupt status register and decides if the input data registry and output data registry are ready. If the input data registry is ready, the system status is saved and inputs (voltage and current information) are read. If the output data registry is ready, the output (reference voltage signal) is written to the output port.

The input current is then decimated by a factor of six. The routine scans the digital port. If bit one of the port is found to be zero, the frequency is advanced to counter the negative power condition. If bit zero is also found to be zero, the unit has tripped, hence the unit is put into self synchronization mode and all the variables are re-initialized.

Before leaving the routine, the system state is restored and the interrupt is enabled.

The following flowchart shows the various events occurring in the main control algorithm. Description of each block is given after the flowchart.

- **Real Power (P) Calculation:**
  - Multiply v & i
  - Filter the result to get P
  - Limit
  - $P_{\text{min}} < P < P_{\text{max}}$

- **Reactive Power (Q) Calculation:**
  - Generate a signal lagging 90 to the output voltage ($v_q$)
  - Multiply this voltage with i and filter to get Q
  - Limit
  - $Q_{\text{min}} \leq Q \leq Q_{\text{max}}$

- **Distortion Power (H) Calculation:**
  - Find the RMS of current
  - Find the apparent power $S^2$
  - Calculate $H = \sqrt{S^2 - P^2 - Q^2}$
  - $H_{\text{min}} \leq H \leq H_{\text{max}}$
Droop the fundamental frequency as a function of P:
\[ w = w_0 - Df.P - \text{syncon} \times \text{PS} \]

Droop the frequency of the injected signal \( v_{hl} \) as a function of Q:
\[ w_{hl} = w_{hl0} - Df.Q \]

Droop the frequency of the 2nd injected signal as a function of H:
\[ w_{h2} = w_{h20} - Df_2.H \]

Generate the signal to be injected:
\[ v_{hl} = \cos(w_{hl}.t) \]
\[ v_{h2} = \cos(w_{h2}.t) \]

Extract the current due to this signal from the load current:
\[ i_{hl} \]
\[ i_{h2} \]

Calculate the small real power \( \Phi_1 \) due to the injected signal 1:

Adjust the voltage amplitude as a function of \( \Phi_1 \):
\[ V = E + Dv \times \Phi_1 \]

Calculate \( v_{\text{ref}} = V \cos(w_{hl}.t) + v_{hl} + v_{h2} \)

Fig. 4.7. Flowchart for the control algorithms.

The variable 'i' in the first block of the flowchart is the inductor current obtained from the inverter unit. The sampling rate used is 4098 Hz. The signal is then decimated to 227 Hz in two stages. The variable 'v'
in the block represents the output signal, which is obtained by properly shifting the phase of the reference voltage signal.

For the calculation of the reactive power, a signal, $v_n$, is generated which lags behind the output voltage by 90 deg (plus the phase shift suffered by the current). When multiplied by the current signal and filtered, the reactive power is obtained.

The fundamental frequency of the voltage signal is drooped as a function of the real power, $P$. The frequency of the first injected signal, $wh_{10}$, is drooped as a function of the reactive power. This signal is then combined with the fundamental signal and injected to the system. This signal will interact with other similar signals from other units. We need to know the current resulted due to the interaction with other units. So the most important part of the reactive power control loop is signal extraction loop. The small power due to the injected signal, $Ph_1$, is extracted and is used to boost the output voltage of the unit.

Besides the real power sharing, the fundamental frequency droop technique is also used to synchronize the unit to the AC bus. There are two variables named ‘syncon’ and ‘PS’ used for this purpose. The variable ‘syncon’ is a control variable which becomes one only when the unit trips. PS is the synchronizing power. This power automatically adjusts the frequency of the inverter to synchronize with the AC bus voltage. As soon as the synchronization takes place, the variable syncon starts to decrease, eventually going down to zero. This gives us a smooth transfer of load from the system to the incoming unit. The following Flowchart explains the synchronization control technique in detail.

```
Start
  ↓
Detect the AC signal
  ↓
Calculate the voltage difference
  ↓
Generate the simulated current signal by filtering the voltage difference signal
  ↓
Is phase > 90
    Yes
        PS = 30000
    No
        Calculate the Synchronizing power PS
  ↓
RET
```

_Fig.4.8. Flowchart for the synchronization control._
Fig. 4.9 show the flowcharts for the complete software.

![Flowchart](image)

Fig. 4.9. Flowchart for the complete software except the ISR.
4.6 Summary

This chapter described the software implementation of the proposed control techniques. The essential components of software implementation such as sample rate selection, digital filtering and decimation were explained in detail. The phase shifts introduced by the FIR filters were highlighted and their undesirable effect on real and reactive power sharing were stressed. It was shown in the chapter that the effect of these phase shifts could be compensated by shifting the phases of the other signals by the same amount which interact with these signals.

This chapter also explained the circular buffer technique and a new square root function to save the computational time. The circular buffer concept saves time by avoiding the need of shifting the each element of the input vector at every iteration. The new square root algorithm trades accuracy with the computational time. The algorithm gives square root with an accuracy of 1%. Since 1% error is acceptable for the current application, the use of the new square root algorithm makes more sense than using the standard square root function which is very accurate but takes extremely long time.

Finally the chapter presented the software details with timing diagrams and flowcharts. The important blocks of the flowchart were explained in detail.
5 Hardware Implementation

5.1 Introduction

This chapter describes the hardware aspect of implementation. There are seven sections in the chapter. Section 5.2 explains the overall system structure of the prototype system. Section 5.3 explains the DSP boards used in the prototype. Section 5.4 explains the hardware details of the circuits used to process the signals prior to interfacing with the DSP board. Section 5.5 explains the structure of the inverter under consideration. Section 5.6 gives some details on the power converter simulators used for the preliminary experiments. Section 5.7 summarizes the chapter.

5.2 Overall System structure

Fig. 5.1 shows the overall system structure of the prototype. DSPs are housed in the computer expansion slots. However, in the final production unit, they will be housed inside the inverter in the form of a control card. The line impedance of 0.5 Ohm is inserted between the first inverter and the load bus which is labeled as "line impedance" in the diagram. The load sockets are connected to the knife switch.

![Diagram of prototype system](image)

*Fig. 5.1. The layout of the prototype system consisting of two inverters.*

The picture of the real setup is shown in Fig. 5.2.
Fig. 5.2. The assembly of the prototype.

Each inverter has a separate DSP to implement the load sharing control. The load current, and the AC bus voltage are sensed and connected to the analog port of the corresponding DSP board. The DC bus voltage and the trip signal from the units are connected to the digital ports of the corresponding DSP boards.

5.3 DSP Boards

There are two types of DSPs in the market: the fixed point type and the floating point type. The fixed point DSPs are comparatively cheaper but demands more programming efforts as all the variables and the constants to be used in the software need to be properly scaled to obtain integer values. The finite word length and the numerical overflow associated with the fixed point calculations can sometimes lead to numeric instability so care should be taken in scaling the variables and constants used in the program. The floating point DSPs, on the other hand, simplifies the software implementation by removing the painful scaling process but are more expensive. With the cost as the major factor, the fixed point TI TMS320C5x DSPs are chosen for the current research work.
One of the DSP boards is obtained from a local company (Spectrum Signals) and another one is obtained from an U.S. company (Dalanco Spry).

5.4 Signal Conditioning and Interface Circuits

DSPs are digital devices while the inverters are analog in nature. The voltage and current signals obtained from the inverter are analog, so we need an analog to digital converter (ADC) to read these signals into the DSP. The DSP boards have onboard ADCs to accomplish this. However, the output of the current and voltage sensors in the inverter does not match the voltage range of the ADCs on the DSP boards. The current sensor gives +/- 5V for +/- 64 amps of current and the voltage sensor gives +/- 12 V for +/- 250 V of voltage. The DC bus voltage sensor gives 2.5 V for 236 V. The Spectrum unit has an ADC with the voltage range of +/- 3 Vmax while the Dalanco unit has the voltage range of +/- 5 Vmax.

Since the output voltages of the sensors do not match the voltage specification of the ADCs, we need signal conditioning circuits. We also need a protection circuit to make sure that the ADC of the DSP boards won't get damaged from over voltages. Besides, the analog signals obtained from the sensors are usually noisy. The limited sampling rate will therefore fold back all the signals beyond the Nyquist frequency in the form of low frequency signals. This aliasing effect can be avoided by band limiting the signals prior to sampling. We need antialiasing filters to band limit the signals.

This section describes the signal conditioning circuits used in the prototype.

5.4.1 Anti-Aliasing Filter

When a composite signal is sampled, the signals whose frequencies are above the Nyquist frequency (half of the sampling rate) fold themselves around the Nyquist frequency and show up in the sampled signal as low frequency signals. This phenomenon is called aliasing. The aliasing effect can be decreased by band limiting the signal prior to sampling. The idea is to attenuate all the signals above the Nyquist frequency well below the detectable level.

A sampling rate of 4098 Hz has been selected to simplify the analog filter design. A 6th order low-pass filter, with a cut-off frequency of 2 kHz has been designed. This filter attenuates any signal above 2 kHz by at least 42 dB. The schematic diagram of the filter is given in Fig.5.3.
5.4.2 Voltage Limiting Circuits

In order to prevent the ADC channels from being damaged due to the excessive voltage, the following circuit is used. The back-to-back connected zener diodes clip the voltage to +/- 4.2 V.

The gain of the second amplifier stage can be adjusted to change the voltage level to the desired voltage range.
5.4.3 Connecting the Current Signal to DSP

The current sensor in the inverter gives the load current scaled down by a factor 12.8. This signal is bandlimited by passing through an anti-aliasing filter. The output of the filter is passed through the voltage limiting circuit. The output of the voltage limiting circuit is eventually connected to one of the input ports of the Dalanco unit. However for the Spectrum unit, it is scaled further down by a factor 1.666 before applied to its input port. The second stage of scaling is required because the ADC port of Spectrum unit accepts only +/-3V opposed to the Dalanco unit, which accepts +/-5V.

5.4.4 Connecting the DC Bus Voltage to DSP

The DC bus voltage indirectly indicates the direction of the power flow. As the power flow reverses, the DC bus voltage rises continuously. It is therefore possible to detect the negative power condition by detecting the DC bus voltage. There is a circuit in the inverter unit which gives output proportional to the DC bus voltage. For the DC bus voltage of 236 V, the output of this circuit is 2.5 V. This signal is compared with a fixed voltage of 2.29 V. When the power is flowing in positive direction, the bus voltage drops down to 210 V so the output of the circuit will be less than 2.22 V. When the DC voltage rises and exceeds 216 V, the external comparator trips taking its output voltage to zero. When the DC bus voltage exceeds 235 V, the output voltage of the circuit becomes 2.5 V. This causes the unit to trip. These two pieces of information are used to detect and control the negative power condition and the trip condition. Please refer to Fig. 5.5, Fig 5.8 and Fig. 5.10 for more details.

![Diagram](image)

*Fig.5.5. Generating the NEGP signal by comparing the DC bus voltage with a fixed reference.*
It is important to note that the hysteresis effect of the comparator circuit should be taken into account to avoid the unexpected results. The hysteresis effect comes from the loading effect of the reference signal. When the comparator trips ON, the output voltage goes to zero. This causes some current to flow from the 5V supply through the feedback resistor and the upper resistor of the potential divider circuit. This increased current flow will cause the reference voltage to drop below its previous value so the comparator will not turn off unless the sensed DC bus voltage goes below this new reference voltage. Smaller values for the voltage divider circuit and larger values for the feedback resistor will reduce the hysteresis to an acceptable value.

5.4.5 Sensing the AC Bus Voltage

In order to make the units to synchronize with the AC bus automatically, we need to sense the AC bus voltage. The following circuit is used to sense the AC bus voltage. The choke at the input side cancels the common-mode noise. Two zener diodes connected back-to-back will limit the voltage within the desired band of +/- 5V.

![AC bus voltage sensing circuit.](image)

5.4.6 Digital I/O Interface Circuits

Two analog inputs available on the DSP boards had already been used up to read the current and the AC bus voltage. Two more pieces of information required to detect are the negative power condition and the trip condition. These are digital pieces of information so the analog input ports are not required to read them. A digital port has been realized using the digital I/O signals available on the DSP board to read these
Since there was a slight difference between the Digital I/O ports of two DSP systems, two different circuits have been employed to realize the digital ports. Each one of them is separately described below:

### 5.4.6.1 Spectrum DSP Board

The Spectrum Board has two places where the digital signals are available. One is the DSPLINK interface which is basically a buffered extension of the DSP chip’s local bus signals. The pinout connection of the DSPLINK Connector is shown below:

![DSPLINK Connector Pin-out Diagram](image)

Fig. 5.7 DSPLINK connector pin-out diagram.

Another source of digital signals is the prototype area. The signals available in this area includes both the serial ports, a maskable and non-maskable interrupt, interrupt acknowledge and C5x timer outputs.

Besides the six signals indicated in the DSPLINK connector, other signals required for decoding the digital information are taken from the prototyping area. The decoding circuit is shown in Fig. 5.12 which realizes port 7.

![Decoding Circuit](image)

Fig. 5.8 Decoding circuit for the Spectrum unit.

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The decoder 74HC138 will produce the enable signal at pin 7 whenever the program reads the digital port. The tri-state latch 74HC373N will transfer the input signals at pin 3 and 4 to pin 2 and 5 respectively. If the unit is experiencing some negative power flow, D1 bit will be set to zero, hence the program will read 16. If the unit is tripped, the program will read 0. If no negative power condition is detected, the program will read 18.

5.4.6.2 Dalanco DSP Board

J3 is the digital logic connector provided in Dalanco Unit. Its pin configuration is shown below:

*BIS  *BSTRB

\[
\begin{array}{cccccc}
\text{WAIT} & D0 & D1 & A1 & A2 & A3 & A4 \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} & \text{●} \\
\end{array}
\]

+5 V  *BRW  GND

Fig. 5.9. 50 pin Digital I/O port of Dalanco DSP Board.

The PAL Equation

\[\text{Trigger} = (1 \& 2 \& 3 \& 4 \& 5 \& 6 \& 7)\]

Fig. 5.10. Decoding circuit for the Dalanco DSP board.
The Dalanco unit uses a PAL (programmable array logic) to realize a decoder which generates the enable signal for the tri-state latch 74HC573. Note that the latch 74HC573 is completely different from the latch 74HC373N. The input and output pins are separated. Pin 2 and 3 are two input pins which generates outputs at pin 19 and 20 respectively. The program scans the digital port regularly. As soon as the program sees 2 (bit 1 is 1 and bit 0 is 0), the negative power condition is detected and the required action is initiated. When the program sees 0 (both bit 1 and bit 0 are 0), the trip condition is detected. In normal condition, the digital port reads 3 (both bits 1).

5.5 Structure of the Inverter

5.5.1 Basic Inverter Module

The basic inverter module under consideration is a bi-directional inverter/charger unit, as shown in Fig. 5.11. It consists of two stages: a dc/dc converter stage with transformer isolation followed by a dc/ac inverter stage.

The dc/dc converter provides isolation to the battery and maintains an internal dc bus which has a voltage above the peak of the ac voltage (dc bus voltage 230 V, ac peak voltage 170 V for the system under study.). The dc bus is supported by a large bank of electrolytic capacitors so it can be treated as a voltage source.

The inverter stage is a power MOSFET H bridge followed by an LC filter. A simplified schematic diagram of the inverter stage is shown in Fig. 5.12.
The inverter can further be divided into two parts: power circuit and control circuit. The power circuit of the inverter consists of a full bridge with Pulse Width Modulation (PWM) system. It converts a dc bus voltage into an ac voltage using a PWM scheme with bipolar voltage switching. The output of the inverter is passed through a second order LC filter to block the switching frequency and its harmonics.

Fig. 5.7 illustrates a typical control structure consisting of an inner current loop and an outer voltage loop. The advantage of the current loop is that it provides inherent current limiting capability, and it also facilitates the outer voltage loop design by reducing the second-order system to a first-order system. A high gain integrating current amplifier used in the current loop ensures an accurate control of the inductor current. The set point for the inner current loop is supplied by the outer voltage loop.

The AC/DC section of the inverter is bi-directional so the inverter can potentially overcharge the DC bus capacitor when the power flows in (negative power condition). Over voltage can damage the capacitor. So the inverter has been equipped with a protection system. The protection scheme consists of DC voltage sensing circuit, a level detector, a PAL (programmable Array Logic) and a microcontroller (supervisory control) system which trips off the unit when the DC bus voltage exceeds 235 V.

### 5.5.2 Inverter Parameters

The parameters of the inverter under consideration are tabulated in Table 5.1.
Table 5.1. Inverter Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter Inductor</td>
<td>1.2 mH</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>10 uF</td>
</tr>
<tr>
<td>DC Bus Voltage</td>
<td>230 V</td>
</tr>
<tr>
<td>Output AC Voltage</td>
<td>120 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>40 kHz</td>
</tr>
<tr>
<td>Permissible Frequency Deviation</td>
<td>0.5%</td>
</tr>
<tr>
<td>Permissible Voltage Deviation</td>
<td>+5% -10%</td>
</tr>
<tr>
<td>Current Loop Bandwidth</td>
<td>~5 kHz</td>
</tr>
<tr>
<td>Voltage Loop Bandwidth</td>
<td>~1 kHz</td>
</tr>
</tbody>
</table>

5.6 Power Converter Simulators

Before using the high power units, the control algorithm was first tested and verified on a parallel system consisting of two low power simulators. The dynamic characteristics of these simulator units are made identical to those of the real units by scaling its parameters properly.

The dynamic characteristics of the simulator circuits were analyzed by using a Network Analyzer. The bode plots of the current and voltage loops were found to be similar to those of the real unit. In order to implement the bandwidth droop technique, a precision analog multiplier was also added to the circuit. The schematic diagram and some results from the network analyzer are provided in appendix I. The parameters of the real unit and its simulator are listed in Table 5.2.

Table 5.2. Parameters of the inverter and its simulator circuit.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Real Inverter</th>
<th>Simulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter Inductor</td>
<td>1.2 mH</td>
<td>750 mH</td>
</tr>
<tr>
<td>Filter Capacitor</td>
<td>10 uF</td>
<td>10 nF</td>
</tr>
<tr>
<td>DC Bus Voltage</td>
<td>230 V</td>
<td>30 V</td>
</tr>
<tr>
<td>Output AC Voltage</td>
<td>120 V</td>
<td>18 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>60 Hz</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>40 kHz</td>
<td>N/A</td>
</tr>
<tr>
<td>Permissible Frequency Deviation</td>
<td>0.1%</td>
<td></td>
</tr>
<tr>
<td>Permissible Voltage Deviation</td>
<td>+5% -10%</td>
<td></td>
</tr>
<tr>
<td>Current Loop Bandwidth</td>
<td>~5 kHz</td>
<td>~5 kHz</td>
</tr>
<tr>
<td>Voltage Loop Bandwidth</td>
<td>~1 kHz</td>
<td>~1 kHz</td>
</tr>
</tbody>
</table>
5.7 Summary

This chapter highlighted the major hardware components used in the prototype system. The chapter included a brief description of the DSP and its input output sections. Since the voltage range of the input/output channels are different from the sensor outputs of the inverter, the signal conditioning circuits are used to modify and scale the signals to suit the DSP input ports. These circuits include AC voltage sensing circuit, anti-aliasing filters, and voltage limiting circuits. AC voltage sensing circuit senses the bus voltage and scales it down to a voltage level suitable for the corresponding DSP input channel. This signal is used to self synchronize the unit with the bus at the normal start up or after the trip. The anti-aliasing filter band limits the current signal to 2000 Hz so that the signal could be sampled at 4098 Hz. The voltage limiting circuit limits the signal within the suitable range of the corresponding DSP input channel. Besides the signal conditioning circuits, the chapter also included details on the circuits used to detect the negative power and trip condition. DC bus voltage sensing circuit and the digital port realization by using digital I/O signals and tri-state latch are described in detail with schematic diagrams.
6 Experimental Results

6.1 Introduction

This chapter presents the experimental results obtained from a prototype of a parallel system consisting of two commercial single-phase inverters. Section 6.2 discusses the importance of sharing the real and reactive power. Some results with and without reactive power sharing loop are included in the section to illustrate the importance of sharing the reactive power. Section 6.3 presents the steady state load sharing for different conditions of line impedance and loads. Section 6.4 presents the transient load sharing. Section 6.5 includes some results from a parallel system consisting of low power simulator units. The software used in the simulator system implements both reactive and distortion power sharing control. Section 6.6 includes more results from other three sets of experiments. Results on self-synchronization are presented in Section 6.7. Section 6.8 summarizes the chapter.

6.1 Reactive Power Sharing

Several experiments were carried out to evaluate the load sharing with and without the proposed reactive power sharing technique. The real power sharing loop is responsible for the synchronization, and is always enabled.

6.1.1 No Load Condition

6.1.1.1 With No Reactive Power Sharing

Two units are connected without any load. These units are not identical. One of the units has the output voltage of 120.2 V while the other has 116.8 V. Furthermore, the line impedances are not balanced. One unit has 0.5 ohms of line impedance while the other has no line impedance.

The results are shown in Fig 6.1:
There is a significant circulating current. This circulating current decreases the efficiency of the unit. The load voltage is measured to be 118.6 V.

6.1.1.2 With Reactive Power Sharing

When the reactive power-sharing loop is enabled, the output voltage is increased to 119.2 V. The results are shown in Fig. 6.2.
The results show that the circulating current has been significantly reduced. Some circulating current is still observed in Fig 6.2. This is due to the error in the frequency references of the units. As explained in Chapter 2, the error in reactive power sharing is a function of the error in the reference frequencies of the units. Using a larger droop coefficient can reduce the error further but could affect the stability of the system.

6.1.2 Inductive Load

6.1.2.1 With No Reactive Power Sharing
An inductive load is applied to the system without any reactive power sharing loop. The inductive load consists of a 10 mH choke in series with a resistive load bank of 10 Ohms. The results are shown in Fig. 6.3. The current sharing is poor. The load voltage drooped to 116.0 V.

![Steady State current for inductive load (No reactive power Control)](image)

*Fig. 6.3 The unit currents for an inductive load.*

The currents are almost 90 degrees out of phase. This indicates some circulation of reactive power. One unit must be absorbing the reactive power while the other must be supplying the reactive power more than the demand of the load. Obviously the reactive power is not shared equally. This decreases the efficiency.

### 6.1.2.2 With reactive power sharing

Enabling the reactive power sharing loop improved the output voltage to 119 V. The load sharing is much better than without the reactive power sharing loop. Fig. 6.4 shows the results after controlling the reactive power sharing.
The currents are now in phase. We expect to see some decrease in the amplitude of the current. However, as the load voltage is increased by 3V, the decrease in the current amplitude due to the reduction in the circulating currents is offset to some extent by the increase in current due to the load voltage increase.

6.1.3 Motor Load

6.1.3.1 With No Reactive Power Sharing

The load currents for a 1HP free running induction motor are plotted in Fig 6.5. The load voltage dropped to 114.5 V.
Steady State currents for 1 HP motor load (No reactive power control)

Fig. 6.5 Currents without using the reactive power sharing loop.

A free running induction motor is a highly inductive load. So the lack of reactive power sharing control resulted in a very poor load sharing.

6.1.3.2 With Reactive Power Sharing

Enabling the reactive power sharing improved the current sharing significantly. The output voltage is also improved to 116.7 V. The currents after enabling the reactive power-sharing loop are shown in Fig. 6.6
The current sharing has improved significantly. Their amplitudes are almost equal.

6.1.4 Nonlinear Load

6.1.4.1 With No Reactive Power Sharing

A nonlinear load of 1420 VA was applied to the bus. The load sharing is found to be poor. The load voltage is dropped to 116.1 V. Fig. 6.7 shows the current waveforms for the units. It is clearly seen that the units experience reactive power circulation.
It should be pointed out that the circulating current observed in Fig. 6.7 is not due to the harmonic currents but due to the fundamental current. Nonlinear load does not absorb significant amount of reactive power. The circulating currents observed in Fig 6.7 is caused by the imbalance in voltages and output impedances.

The voltage waveform for the nonlinear load is shown in Fig. 6.8. Note that the voltage waveform is not sinusoidal due the nonlinear load nature.

Fig. 6.7: Unit currents for nonlinear loads.
6.1.4.2 With Reactive Power Sharing

A good sharing of nonlinear load is obtained by using the reactive power-sharing loop. The load voltage now becomes 122.8 V. The current and voltage waveforms are shown in Fig 6.9 and 6.10, respectively.
The reactive power sharing loop reduced the circulating reactive power significantly. The amplitudes of the current waveforms are also almost equal. Note that the amplitudes were quite different when the reactive power control was disabled (see Fig. 6.7).

Fig. 6.9: Current waveforms for the nonlinear load.
The amplitude of the load voltage has also improved. In fact the load voltage has exceeded the nominal value of 120 V. The reason for this lies on the fact that the proposed reactive power sharing loop uses a voltage boost technique. This has a very beneficial effect on the quality of the voltage. The natural voltage drop associated with a higher load is offset by the boost associated with the control technique. With a capacitive load or a nonlinear load, the boost obtained is higher. However, it never exceeds the allowed limit of +5%.

**6.2 Steady State Load Sharing**

Section 6.2 will demonstrate that the load sharing performance will be significantly deteriorated when the reactive power-sharing loop is disabled. This section explores the performance of the proposed sharing techniques for various conditions of line impedances, output voltages and loads. It is important to make it clear that the currents shown in the following results are inductor currents, which is converted into a
voltage signal (0 - 5 V) by using a series resistance and a voltage amplifier. The oscilloscope used for the experiment is Tektronics TDS 340A. The waveforms are averaged over 8 points to get rid of some of the noises.

6.2.1 With Line Impedance

The parallel inverter system consists of two inverters connected to a common load bus. One of the inverters is connected directly to the load bus while the other unit is connected through a resistance of 0.5 Ω. This resistance represents the line impedance of about 500 ft of 10 AWG wire. At no-load, the inverter output voltage is 120 V for both the units and the nominal frequency is 60.02 Hz.

6.2.1.1 Linear Resistive Load

A resistive load of 2880 W is applied to the parallel system. The load voltage as well as the frequency of the system is noted down. The inverter currents of both units are recorded. Fig. 6.11 depicts the load

![Steady state sharing of a linear load](image)

Fig. 6.11. Inverter currents with a linear resistive load.
sharing between the units. The load voltage was 118.5V and frequency was 59.99 Hz.

The load sharing is found to be quite good. A small discrepancy in load sharing comes from the error in the frequency references of the two DSP crystals. This effect can be reduced to a very small level by increasing the frequency droop coefficients. This will however compromise on the frequency of the voltage signal. To illustrate this point, the same load is applied to the system. This time however, the droop coefficient is increased by three folds. The sharing is shown in Fig. 6.12.

Now the load voltage is 119 V and the frequency dropped to 59.95 Hz. With this droop coefficient, the frequency of the system droops to 59.88 Hz at the full load. Therefore, the total deviation in frequency is around 0.2 % from no-load to full load. The frequency can be restored back to the nominal value of 60 Hz using a frequency-restoring loop. This, however, demands more computational power and more complex algorithm implementation which overloads the DSP. However, if we use the previous value of the droop coefficient, the full load frequency deviation will be just 0.067% (max) which is acceptable without

![Steady state sharing of a resistive load (more droop)](image)

*Fig. 6.12 Inverter currents when the droop coefficient is increased.*
restoring. As a result, a smaller droop has been used for sharing the real power. All the results included in this chapter are obtained with the small droop coefficient.

6.2.1.2 Inductive load

A 1 HP motor load is connected to the system. The current waveforms recorded are shown in Fig. 6.13.

![Steady state sharing of an inductive load](image)

*Fig. 6.13. Inverter currents when a load is inductive.*

The load sharing is good. The load voltage was found to be 118.2 V and the frequency is 60.01 Hz. The current waveforms in Fig. 6.13 show that the proposed control technique is capable of sharing the reactive power despite the presence of the line impedance.
6.2.1.3 Compressor Load

A 3 HP compressor was connected to the system. The steady state current waveforms are shown in Fig. 6.14. The output voltage was 118.5 V and the frequency was 60.00 Hz.

![Steady state sharing of a compressor load](image)

*Fig. 6.14. Inverter currents when the load is a 3 HP compressor.*

Note that a single unit is not capable of starting the compressor but that the parallel system had no problem of supply the load.
6.2.1.4 Nonlinear Load

A nonlinear load of 3 kVA was applied to the system. The load voltage was found to be 120 V and the frequency was found to be 60.00 Hz. The currents of both the inverters are plotted in Fig. 6.16.

Fig. 6.15. Inverter currents when the load is nonlinear.
Results show that the load sharing is very good. The voltage waveform shown in Fig. 6.16.

It is worthy mentioning that the automatic droop in the bandwidth due to the capacitive loading helps to share the distortion component of the current.

6.2.1.5 Two Units of Different Capacities

The droop coefficients of one of the units are doubled to make the unit to share the half of the total power. Note that the line impedance is greater in the other unit which is suppose to provide more power, and this represents the worst case scenario. A 1 HP motor and 1440 W of real power is applied to the system. The current waveforms are shown in Fig 6.17.

The voltage at the output was found to be 116 V and the frequency was found to be 60.00 Hz.
Two units of different capacities

![Graph of inverter currents](image)

Fig. 6.17. Inverter currents when the droop coefficients are different.

The sharing is as predicted by the theory. The unit having less droop coefficient is taking more power and the one with more droop is taking less power.

### 6.2.2 Without Line Impedance

As expected, the absence of the line impedance should improve the output voltage for all loading conditions. To illustrate this, the system without the line impedance is loaded with 2880 W and a 1 HP motor. This load caused the load voltage to 116.7 V. The load voltage with the same load was 115.2 V when the line impedance was present. The current waveforms are shown in Fig. 6.18.
6.3 Transient response

6.3.1 With line impedance

It is interesting to see the transient load sharing when the load is a motor. A 1-HP motor is started and its start-up transient is captured and shown in Fig. 6.19.
Transient sharing of a motor start up (inductive load)

![Graph](image)

**Fig. 6.19. Inverter transient currents when a 1 HP motor is started.**

It is clear from Fig. 6.19 that the sharing is good even in the transient state.

### 6.3.2 Without line impedance

The transient is less severe without the line impedance. It is also shorter than with the line impedance. Note that the sharing is much better even in the transient state, as can be seen from Fig. 6.20 and Fig. 6.19.
In this case, both currents are almost equal even in the transient state.

6.4 Results from Low Power Simulators

Results from the experiments performed on the parallel system consisting of two low power simulators are included here to show the effect of distortion power sharing control loop. The simulator units (refer to appendix I for the circuit details) are provided with a variable gain block in its outer voltage loop. This facilitates the implementation of the distortion power sharing controller. It is to be noted that, with the distortion power sharing loop, the fundamental voltage signal was generated at 683 Hz, not at 4098 Hz, due to insufficient DSP computation power.

When the fundamental voltage signal was generated at 683 Hz, the frequency of the output voltage was found to fluctuate by +/- 0.1 Hz. This problem can be solved by increasing the sampling rate to 4098 Hz.

The following table shows the results from the tests performed on the simulator system.
Table 6.1 Results from the parallel system of simulators

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Load Voltage</th>
<th>System Load</th>
<th>$V_{Rs} = \text{Current} \times 12.8 \text{ V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_1 = 17.4 \text{ V}, V_2 = 18 \text{ V}$</td>
<td>18.7 V</td>
<td>No load</td>
<td>Unit#1</td>
</tr>
<tr>
<td>$Z_1 = 11 \Omega, Z_2 = 0 \Omega,$</td>
<td>17.8 V</td>
<td>Bulb</td>
<td>260 mV</td>
</tr>
<tr>
<td>Bulb = (~ 300 $\Omega$)</td>
<td>17.4 V</td>
<td>Bulb $|$ R</td>
<td>760 mV</td>
</tr>
<tr>
<td>R = 250 $\Omega$ resistor</td>
<td>16.7 V</td>
<td>R $|$ L</td>
<td>1.17 V</td>
</tr>
<tr>
<td>L = 200 mH Inductor</td>
<td></td>
<td></td>
<td>1.47 V</td>
</tr>
<tr>
<td>Nonlinear Load = Diode</td>
<td>17.6 V</td>
<td>Bulb $|$ 680 uF</td>
<td>1.03 V</td>
</tr>
<tr>
<td>Bridge+load</td>
<td>17.1 V</td>
<td>Bulb $|$ 680 uF $|$ L</td>
<td>1.62 V</td>
</tr>
</tbody>
</table>

It is found that the current sharing is good for all types of load. The load voltage is also good for the whole range of load.

A few more results are presented below to illustrate the validity of the reactive and distortion power sharing techniques.

6.4.1 Without Reactive and Distortion Power Sharing Control

Fig 6.21 shows the current sharing between the simulator units when a combination of a nonlinear load and an inductive load is applied to the system. The nonlinear load is a full-bridge rectifier with a 680 uF capacitor at its output. The inductive load is a pure inductor of 200 mH. The reactive as well as the distortion power sharing loops are disabled.
The lack of reactive and distortion power controller resulted in a very poor current sharing. There is a large circulation of reactive power between the units.

6.4.2 With Reactive and Distortion Power Control

Fig. 6.22 shows the current sharing when the reactive and distortion (Q/D) control is enabled. The current sharing is much better as compared to the previous case.
Fig. 6.23 shows the current sharing between the simulator units when the reactive/distortion (Q/D) sharing controller is enabled and a load consisting of a 250 Ohms and a full bridge rectifier with a 680 uF capacitor is applied to the system.
With reactive and distortion power control loops

![Graph showing current sharing between units with Q/D control.](image)

**Fig. 6.23 Current sharing between the simulator units with Q/D control.**

Again, currents are found to be shared equally between the units.

### 6.5 Other Experiments

Other three sets of experiments were performed on the prototype. The first set is when the line impedance is absent and the units have the same output voltages. The second set is when the units have different line impedances but the output voltages are the same. The third set is the worst case condition: when the units
have different output voltages and they also have different line impedances. The results are summarized in Table 6.2, Table 6.3 and Table 6.4, respectively. The some results of the worse condition (Case III) are also plotted.

Here are a few comments pertaining to Table 6.2, Table 6.3 and Table 6.4. The first column in the table gives details on the prototype parameters such as line impedances, the output voltages of the units prior to paralleling, and the nature of the load. The second and third columns are the unit voltages after connecting in parallel and loading the system. The fourth column shows the total load applied to the system. The fifth column shows the frequency of the system after loading. The sixth and seventh columns show the unit currents. Then last column shows the deviation in unit current expressed as a percentage.

Table 6.2 Results when the system is balanced

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Output Voltages (Parallel Connected)</th>
<th>Total Load</th>
<th>Freq. Hz</th>
<th>Currents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Unit#1</td>
<td>Unit#2</td>
<td></td>
<td>Unit#1</td>
</tr>
<tr>
<td>V1 = 120 V, V2 = 120 V</td>
<td>119.1 V</td>
<td>119.1 V</td>
<td>3600 W</td>
<td>59.99</td>
</tr>
<tr>
<td>Z1 = 0 Ohms, Z2 = 0 Ohms</td>
<td>117.5 V</td>
<td>117.5 V</td>
<td>5400 W</td>
<td>59.98</td>
</tr>
<tr>
<td>Load = Linear Resistive Load</td>
<td>120.7 V</td>
<td>120.7 V</td>
<td>720 W</td>
<td>60.01</td>
</tr>
<tr>
<td>V1 = 120 V, V2 = 120 V</td>
<td>119.3 V</td>
<td>119.3 V</td>
<td>2880 VA</td>
<td>60.00</td>
</tr>
<tr>
<td>Z1 = 0 Ohms, Z2 = 0 Ohms</td>
<td>121.0 V</td>
<td>121.0 V</td>
<td>1440 VA</td>
<td>60.01</td>
</tr>
<tr>
<td>Load = Nonlinear</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1 = 120 V, V2 = 120 V</td>
<td>117.7 V</td>
<td>117.7 V</td>
<td>1 HP</td>
<td>60.02</td>
</tr>
<tr>
<td>Z1 = 0 Ohms, Z2 = 0 Ohms</td>
<td>115.4 V</td>
<td>115.4 V</td>
<td>2 HP</td>
<td>60.01</td>
</tr>
<tr>
<td>Load = Inductive</td>
<td>118.5 V</td>
<td>118.5 V</td>
<td>3 HPC</td>
<td>60.00</td>
</tr>
<tr>
<td>3 HPC = 3 HP Compressor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Units of two different capacities</td>
<td>118.9</td>
<td>118.9</td>
<td>2880 W</td>
<td>59.99</td>
</tr>
<tr>
<td>V1 = 120 V, V2 = 120 V</td>
<td>118.3</td>
<td>118.3</td>
<td>2880 VA</td>
<td>59.99</td>
</tr>
<tr>
<td>Z1 = 0 Ohms, Z2 = 0 Ohms</td>
<td>110.5</td>
<td>110.5</td>
<td>2 HP+3 HPC</td>
<td>60.00</td>
</tr>
<tr>
<td>Load = Linear/Nonlinear/Motor</td>
<td>114.1</td>
<td>114.1</td>
<td>2 HP</td>
<td>60.01</td>
</tr>
</tbody>
</table>
Table 6.3 Line Impedances are not balanced.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Output Voltages (Parallel Connected)</th>
<th>Total Load</th>
<th>Freq. Hz</th>
<th>Currents</th>
</tr>
</thead>
</table>
|                                   | Unit#1 | Unit#2 | Load     | Hz       | Unit#1 | Unit#2 | |%
| V1 = 120 V, V2 = 120 V            | 123 V  | 116.5 V | 3600 W   | 59.99   | 14.66  | 16.09  | 8.9%
| Z1 = 0.5 Ohms, Z2 = 0 Ohms        | 121.7 V| 113.5 V | 5400 W   | 59.97   | 20.48  | 22.23  | 8.1%
| Load = Linear Resistive Load      | 121.6 V| 120.3 V | 720 W    | 60.01   | 3.76   | 3.88   | 3.1%
| V1 = 120V, V2 = 120V              | 123.7 V| 119.6 V | 2880 VA  | 60.00   | 10.93  | 12.02  | 9.0%
| Z1 = 0.5 Ohms, Z2 = 0 Ohms        | 122.8  | 120.9 V | 1440 VA  | 60.01   | 6.20   | 6.91   | 10.3%
| Load = Nonlinear                  |         |         |          |         |        |        |%
| V1 = 120V, V2 = 120V              | 118 V  | 117.6 V | 1 HP     | 60.01   | 4.66   | 4.83   | 3.5%
| Z1 = 0.5 Ohms, Z2 = 0 Ohms        | 116.1 V| 115.3 V | 2 HP     | 60.01   | 7.94   | 8.23   | 3.5%
| Load = Inductive                  | 121.3 V| 118.9 V | 3 HPC    | 60.00   | 7.58   | 7.01   | 8.1%
| 3 HPC = 3 HP Compressor           | 118.7 V| 115.1   | 3HPC+1 HP| 60.00   | 10.16  | 10.94  | 7.1%
| Units of two different capacities |         |         |          |         |        |        |%
| V1=120 V, V2 = 120 V              | 122.9  | 118.9   | 2880 W   | 59.99   | 8.37   | 16.58  | 0.9%
| Z1 = 0.5 Ohms, Z2 = 0 Ohms        | 121.3  | 118.6   | 2880 VA  | 60.00   | 8.35   | 14.21  | 17.5%
| Load = Linear/Nonlinear/Motor     | 113.4  | 110.7   | 2HP+3 HPC| 60.00   | 8.58   | 16.42  | 4.5%
|                                   | 114.4  | 113.9   | 2HP      | 60.01   | 5.52   | 10.18  | 8.5%
Table 6.4 Line Impedances as well as output voltages are not balanced.

<table>
<thead>
<tr>
<th>Experiment Conditions</th>
<th>Output Voltages (Parallel Connected)</th>
<th>Total Load</th>
<th>Freq. Hz</th>
<th>Currents</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Unit#1</td>
<td>Unit#2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1 = 115.7 V, V2 = 120 V</td>
<td>120.2 V</td>
<td>113.7 V</td>
<td>3600 W</td>
<td>59.99</td>
</tr>
<tr>
<td>Z1 = 0.5 Ohms, Z2 = 0 Ohms</td>
<td>121.7 V</td>
<td>112.4 V</td>
<td>5400 W</td>
<td>59.97</td>
</tr>
<tr>
<td>Load = Linear Resistive Load</td>
<td>119.6 V</td>
<td>118.2 V</td>
<td>720 W</td>
<td>60.01</td>
</tr>
<tr>
<td>V1 = 115.7 V, V2 = 120 V</td>
<td>122.9 V</td>
<td>118.9 V</td>
<td>2880 VA</td>
<td>60.00</td>
</tr>
<tr>
<td>Z1 = 0.5 Ohms, Z2 = 0 Ohms</td>
<td>122.8 V</td>
<td>121.0 V</td>
<td>1440 VA</td>
<td>60.01</td>
</tr>
<tr>
<td>Load = Nonlinear</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1 = 115.7 V, V2 = 120 V</td>
<td>116.1 V</td>
<td>115.4 V</td>
<td>1 HP</td>
<td>60.01</td>
</tr>
<tr>
<td>Z1 = 0.5 Ohms, Z2 = 0 Ohms</td>
<td>115.4 V</td>
<td>114.4 V</td>
<td>2 HP</td>
<td>60.01</td>
</tr>
<tr>
<td>Load = Inductive</td>
<td>119.9 V</td>
<td>116.9 V</td>
<td>3 HPC</td>
<td>60.00</td>
</tr>
<tr>
<td>3 HPC = 3 HP Compressor</td>
<td>117.4 V</td>
<td>114.1 V</td>
<td>3HPC+1 HP</td>
<td>60.00</td>
</tr>
<tr>
<td>Units of two different capacities</td>
<td>121.3</td>
<td>117.4</td>
<td>2880 W</td>
<td>59.99</td>
</tr>
<tr>
<td>V1 = 115.7 V, V2 = 120 V</td>
<td>122.7</td>
<td>120.4</td>
<td>2880 VA</td>
<td>60.00</td>
</tr>
<tr>
<td>Z1 = 0.5 Ohms, Z2 = 0 Ohms</td>
<td>114.4</td>
<td>114.0</td>
<td>2HP</td>
<td>60.01</td>
</tr>
<tr>
<td>Load = Inductive</td>
<td>113.6</td>
<td>110.9</td>
<td>2HP+3 HPC</td>
<td>60.00</td>
</tr>
</tbody>
</table>

In order to assess the current sharing quality, we need to compare the currents of both units. Though it seems trivial, there are many factors that need to be considered before we could derive any meaningful quality information from the measurements. One of the main challenges is the accuracy of the current sensors itself. The inductor current is measured by using a series resistance. The resistance converts the inductor current into a small voltage signal. This signal is then amplified using an op-amp circuit. Since it is not possible to have exactly the same resistance value and the same gain for the op-amp circuits for all the units, some error in the measurement is inevitable. Another challenge is in measuring the voltage signal output of the amplifier stage correctly. Since we use a differential probe which reduces the input voltage by 50 times in one of the channels, the output of the probe can only be measured with an oscilloscope that with a different scale. The accuracy of the oscilloscope probes at different levels introduces another error in current measurement.
The results do show that the sharing is not so good when the units are of different capacities and the load is nonlinear. This is to be expected as the voltage loops of the inverters still have the same bandwidth since they are actually of the same ratings.

Therefore, the difference in the current readings ($\Delta I$) shown in the above tables may not really reflect the degree of sharing error. Actual sharing error could be slightly different than that suggested by the $\Delta I$ column in the tables.

Besides the steady state data shown in the above tables, some transient state data have also been collected. The transient state data obtained from the worst case scenario (case III) are included below.

A full load resistive load (5400 w) is imposed on the system and taken off after a while. The inverter currents are captured during the transient state are shown in Fig. 6.24.
The transient load sharing is found to be pretty good. Both units start sharing the load from the beginning itself. Despite the line impedance and the output voltage variations, the currents seem to be properly shared. The reason for this lies on the fact that the gain of the real power sharing loop is very high so speed of control is also good.

A nonlinear load is switched on suddenly and turned off after a while. The results are shown in Fig. 6.25

![Transients Load Sharing](image)

**Fig. 6.25 Transient response with a nonlinear load.**

The initial high peak in current is due to the capacitor charging current. Then we see some circulation of the reactive power. The transient current sharing is still found to be pretty good except for the first one or two cycles.

A 1 HP motor is started up and the transient response is captured. Fig 6.26 shows the
Currents during the transient state. The transient current sharing is good. The voltage waveforms are shown in Fig. 6.27. Note that the voltage waveforms are not recorded concurrently. So the starting points of the motor in two plots are different.
The voltage momentarily goes down to 150 V but recovers back to the 160 V after a cycle or two. The oscillations observed in the voltage waveform during the motor start up are due to the hardware current limiting circuit. At the start up of the motor, the current drawn easily exceeds the maximum limit of 50 Amps. This current limit circuitry will momentarily reduces the duty cycle to a very low value to limit the current below the maximum allowed value (50 A) value. We note that the voltage waveform recovers to a sinusoidal form quickly after the transient distortion.

6.5.1 Result Analysis

Results shown in above tables can be used to evaluate the performance of the parallel operation. Some of the conclusions drawn from the analysis are discussed below.
6.5.1.1 Voltage Quality

There are three quantities associated with the quality of a voltage signal. They are the voltage amplitude, the frequency; and the waveform.

The rms voltage at the unit outputs and the load are plotted below.

![Output and load voltages in the parallel network](image)

*Fig. 6.28 The Voltage at the unit outputs and the load.*

All the voltage readings are within the specified voltage limits. This clearly shows that the proposed control techniques are capable of sharing all types of load without excessive voltage drop even when the line impedance condition and the unit to unit variations are worst. The frequency of the load voltage is also within ±0.03 Hz which is small enough to be acceptable. The voltage waveform and its frequency spectrum for the worst nonlinear loading condition are shown in Fig. 6.25.
The power in the third, fifth and other odd harmonics are more than 20 dB below the fundamental frequency. We can compare the voltage waveform quality with a single unit supplying the same load. Fig. 6.30 compares the voltage waveform shown in Fig. 6.29 with the voltage waveform when a single unit supplies the same load. The solid line curves are for the two unit system and the dashed line curves are for the single unit system.
As expected, the waveform quality degraded further when a single unit is used to supply the load. The power spectrum density plot (dashed line) for the single unit system has the fundamental peak lower than the that of the two unit system but the peaks of the 3rd and other odd harmonics are higher than those of the two units system. The time domain plot also shows that the amplitude of the voltage dropped significantly when a single unit is used.

6.6 Self-Synchronization

One of the desirable features in paralleling is the hot-swappability. It will be very convenient for the user if a new unit could simply be connected to the system without any need of manual synchronization. This can be achieved by imparting a self-synchronizing capability to the unit. The theory behind the self-synchronizing control developed in this research work has been explained in Chapter 2. This section
shows the performance of the self-synchronization control. Fig 6.31 illustrated the self-synchronization process. Initially the entire load of 2880W was supplied by one of the units only. Then after some 350 ms, another unit comes in parallel and shares the load smoothly.

Fig. 6.31. Self-synchronization.

The expanded view of the above figure is shown in Fig. 6.32. The figure shows that the incoming unit starts to share the load smoothly.
Another unit coming in synchronized

Fig. 6.32. Expanded view of Fig 6.31.

6.7 Summary

This chapter presented experimental results to verify the proposed control techniques. The experiments presented in the chapter cover various scenarios of line impedance variations and unit to unit variations of output voltages. The chapter also illustrated the importance of reactive power sharing which many previous researchers ignored. With experimental results, the impact of reactive power sharing on circulating currents and load sharing are demonstrated.

The chapter also highlighted the importance of sensor accuracy and their impact on the signal measurement. The chapter also shows some results of self-synchronization which imparts hot-swap ability to the units. The chapter also included some results from simulator circuits to show the effect of distortion power sharing.
7 Conclusions and Future Works

This research lays the theoretical basis for distributed control of UPS systems using the signal injection method. Experimental results presented in this thesis have shown a close match with the expected performance as determined analytically with MATLAB and in time domain simulations with PSIM and PSpice.

7.1 Contributions

The main contributions are summarized below

a. A novel concept to share the reactive power in a distributed power supply system.

The method developed in this research does not require any control interconnections nor uses the conventional droop mechanism. It guarantees proper sharing of reactive power despite unit to unit variations and line impedance imbalances. Unlike the conventional droop mechanism, the proposed technique boosts the output voltage to share the load. As the load increases, the load voltage tends to decrease due to the drop across the source impedance. The boost obtained from the proposed control technique compensates for the drop, hence improves the voltage quality and system stability.

b. A novel concept to share the distortion component of the current in a distributed power supply system.

The method developed here is well suited for a distributed ac power supply system consisting of single-phase inverters. Similar to the reactive power sharing loop, the distortion power sharing loop also does not need any control interconnections. The concept of bandwidth adjustment is a novel idea to influence distortion power sharing. Besides sharing the distortion component of the load current, the proposed technique also improves the voltage waveform.

c. A new concept of signal injection and signal extraction methods.

The concept of modulating and demodulating a signal with a carrier wave is very common in communication area. However, it is very uncommon to modulate a low frequency signal with a very low frequency signal. A new concept of modulating and demodulating at low frequency range has been proposed in the research work. This allows inverters to communicate and control without any control interconnections. In effect the proposed signal
injection method combines the communication signal with the control signal. This avoids any further need of communications. Another very desirable feature of the proposed technique is its ability to automatically adjust the voltages so that the deviation in reactive power sharing due to the unit to unit variations of the reference voltages is completely compensated. This resetting characteristics results from the introduction of an integrator in the reactive power sharing loop.

Also, the total load in the system can be shared in any proportion among the parallel connected inverters by simply selecting the droop coefficients in inverse proportions. This is a very desirable feature. Inverters can now be designed in modular forms with different capacities. We can meet any capacity demand by connecting the desired number of units in parallel. The modular design not only increases the efficiency but also simplifies the inventory problem, resulting in reduced manufacturing cost.

d. An efficient approach in calculating the reactive and distortion power.

An efficient method of using the phase shifted versions of the output voltage has been developed to calculate the real and reactive power components. This avoids the need of continuously scanning the output voltage which saves significant amount of DSP time. Another contribution is in the square root algorithm. A simple but fast algorithm to calculate the square root has been developed.

e. A novel anti-integral windup technique.

Another contribution of the research work is the development of the anti-windup mechanism. Without this mechanism, the proposed control technique can become unstable when the control inputs saturate. The proposed anti-integral windup mechanism improves the stability of the system.


Yet another innovation is the algorithm to synchronize the unit with the ac bus voltage. This method is simple but very effective and practical. This method does not guarantee the phase matching but the phase difference can be reduced to a negligible level. The method is very similar to the load sharing technique so can be integrated seamlessly with the load sharing controller.

The self synchronizing capability makes the inverters hot swappable. We can connect the unit to the ac bus directly without synchronization. The unit synchronizes with the ac bus automatically and starts sharing the load smoothly.
7.2 Improvements and Future works

The theory developed in this research brings a new control solution to the distributed UPS systems. While the general concepts have been covered in this thesis, further research is necessary, particularly in the following areas:

a. To study the effect of low frequency harmonics introduced in the system by the injected signal.

b. To study the possibility of using a very high frequency signal as the injected signal.

c. To study the possibility of adopting the technique for a three phase system. The possibility of calculating the real and reactive power instantaneously would help improve the speed of load sharing in a three phase system. However, the effect of unbalanced load conditions on the signal injection method needs to be studied.

d. To study the possibility of using the technique to operate two or more active filters in parallel without any control interconnections.
Bibliography


Appendices
A Schematic Diagram of the Simulator

Appendix I: Low Power Simulator Circuits
B. Voltage Loop Response

The following figure shows the frequency response behaviour of the outer voltage loop of the simulator with half load obtained by using a network analyzer.
C. Current Loop Response

The following figure shows the frequency response behaviour of the inner current loop of the simulator when supplying half load. This is also obtained by using the network analyzer on the circuit.
Appendix II: DSP Boards

A. Handling the DSP boards

DSPs are complex digital devices needing complicated initialization process. The memory management of DSPs is equally complex. The codes required to perform input/output functions can also be tricky as the values obtained from the A/D ports are not always valid. These all things make the DSP a complex device to handle.

In this project, we acquired one DSP board from a local company named Spectrum Signal Processing and one from Dalanco Spry. The Spectrum board uses TMS320C50 DSP while Dalanco Board uses TMS320C51 DSP. Besides the DSPs, these two boards are different in other aspects as well. The Spectrum board has two I/O channels. The input channels have dual 16 bit A/D converters with an anti-aliasing filter. Dalanco board has 8 I/O channels but only one 12 bit A/D, so using two channels would required time sharing the A/D. The output channels of the Spectrum board has a dual 16 bit D/A with a smoothing filter. However, the Dalanco board has to share one 12 bit D/A for all the channels and there are no smoothing filters. Furthermore the Spectrum board uses +/-3 V for its analog input and output channels while the Dalanco board uses +/-5 V. The analog inputs are inverted through a unity gain stage before being presented to the A/D in the Spectrum board while the data is not inverted in the Dalanco board. More details on the DSP boards are provided in [35,36].

The Spectrum board A/D being a 16 bit, does not need extra manipulation of the input data, however, the Dalanco board needs extra lines of codes to convert the 12 bit unsigned data obtained from A/D into a 16 bit signed number. Please refer to the source code provided in the appendix for more details.

The following flowchart show the procedure to configure the Spectrum DSP board.
Set the wait states for the program memory, data memory, control, and I/O register

Write A440h to User Control Register

Write the value F2h to the AMELIA Control Register

Write the value Fa26h to the timer 1 register

Write the value 8DF7h to the configuration register.

Write the value 02h to the Interrupt Mask Register to use INT2

RETR

Fig A.1 Flowchart to initialize the Spectrum board.

Start

Disable all the maskable interrupts

Set the wait states for Program and data memory, Input/Output ports.

Mask all except INT2

Write the value F7C2h to port0 to achieve a sample rate of 4096 Hz

Enable the interrupt

RETR

Fig. A.2. Flowchart to initialize the Dalanco DSP Board.
B. Memory Management

One of the challenging aspects of using DSP is to manage its on-chip as well as the external memory efficiently. If these memories are not properly configured the performance of the system degrades significantly. Sometimes the program may not execute at all. We describe here some of the important aspects of the memory management.

Both C50 and C51 can access the following types and ranges of memory space:

- 64 K-word program
- 64 K-word local data
- 64 K-word input/output ports
- 32 K-word global data

The parallel architecture lets the C5x devices perform three concurrent memory operations in any given machine cycle: fetching an instruction, reading an operand, and writing an operand.

The C50 includes 2K words of boot ROM, 9K words program/data SARAM, and 1056 words of DARAM. The boot ROM resides in program space at address range 0000h-7ffh. The 9 K words of SARAM can be mapped into program or data space and reside at address range 0800h-2BFFh.

The C51 removes the 2K-word boot ROM from program memory space and replaces 8K words of program/data SARAM with an 8K-word block of maskable ROM. The C51 also includes 1K word of program/data SARAM and 1056 words of DARAM. The 8K words of ROM reside in program space at address range 0000h-1FFFh. The 1K word of SARAM can be mapped into data space (address range 0800h-0BFFh), program space (address range 2000h-23ffh), or both spaces.

The program memory can reside both on and off chip depending upon the device configuration and the size of the program to be run. If the size of the program is bigger than the available on-chip memory, the program is loaded on the external memory. Loading the program in the internal memory gives higher performance, lower cost and lower power consumption. The most important thing to set in the program memory configuration is the address map for the interrupt vector. If we are using INT2 (timer interrupt), its location in the interrupt vector table is 4. So the address of the Interrupt Service Routine (ISR) has to be written at the 4th location (offset 4).

For the local data also it is desirable to load them in the internal memory (on-chip) space if possible. If the size is too big, we will have to load them in the external memory.
The configuration of the global memory becomes important when we need to as we are not using multi-modules. The command files to set the program and data memory of the DSPs are given in the appendix.

C. Compiling/linking

C.1 For the Spectrum Unit

The following command is used to compile the program:

dspcl -q -c -q -v50 -mx -as -i %1.c -s -x2 -o
dspa -v50 %3.asm -s
dsplnk -q -c -vO %1.obj %3.obj -o %1.out %2.cmd -l c:\320tools\rts50.lib
c5xsort %1.out

The first command line compiles a C source file. The options are explained below:
-quiet
-compile only no linking
-symbolic debugging enabled
-v50 for C5x (target processor)
-avoid C5x silicon bugs
-keep local symbols
-insert library search path
-strip symbol table
-enable all inline functions
-optimize level2

The second line assembles an assembly file which calls C functions to implement the filters. This approach saves some calculation time.

The third line links the object files created by the first two lines with the library file. The options are described below:
-quiet
-ROM initialization
-generate old COFF file
-output file name
-library name

The last line takes the COFF file generated by the link command and extracts the debugging information and sorts the symbols to make the file loadable to Mon5X debugger.
C.2 For the Dalanco Unit

dspcl -q -c -g -v50 -mx -as -i %1.c -s -x2 -o
dspa -v50 %3.asm -s
dsplnk -q -c -v0 %1.obj %3.obj -o %1.out %2.cmd -l c:\320tools\rts50

Note that the most of the compiling and linking commands are essentially the same. However, we do not have to sort the symbols for the debugging so only the last command line is missing here.

C.3 Loading to the DSP

It is easy to load the program in the Spectrum unit. All we have to do is to run the debugging program 'view5x' and use its menu command 'load' to load the program. Spectrum Signals have also provided other functions and tools to design our own loader if we wish.

Loading the program to the Dalanco unit is also easy. We have to run the following two lines to load the program and run.

load500 %1

d5000

Then press 'g' to start the program.
Appendix III: Scaling Factors

Since the DSP used in the project is a fixed-point type, scaling of variables is needed to avoid overflow/underflow. The following lists the variables and the corresponding scaling factors. The value inside the DSP equal to the actual value multiplied by the scaling factor. Note that some of the variables are of long and some are of float type.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Scaling Factor</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCI</td>
<td>64</td>
<td>Current after the first decimation</td>
</tr>
<tr>
<td>IN1</td>
<td>512</td>
<td>Input current signal</td>
</tr>
<tr>
<td>IN2</td>
<td>96</td>
<td>Input voltage signal</td>
</tr>
<tr>
<td>IN3</td>
<td>1</td>
<td>Input from the Digital Port</td>
</tr>
<tr>
<td>XD[55]</td>
<td>512</td>
<td>55 points long vector of input data</td>
</tr>
<tr>
<td>XD2[45]</td>
<td>64</td>
<td>45 points long vector of filtered input data after decimation (1:6)</td>
</tr>
<tr>
<td>YD[1]</td>
<td>64</td>
<td>The most recent filtered output from the first stage of decimation</td>
</tr>
<tr>
<td>YD2[1]</td>
<td>8</td>
<td>The most recent filtered output from the second stage of decimation</td>
</tr>
<tr>
<td>V</td>
<td>128</td>
<td>Peak voltage amplitude</td>
</tr>
<tr>
<td>W</td>
<td>64</td>
<td>Frequency in radians/sec for the fundamental 60 Hz signal. For scaling, a “shifted window” technique has been used. ((w - 300) \times 64)</td>
</tr>
<tr>
<td>P</td>
<td>4</td>
<td>Real Power</td>
</tr>
<tr>
<td>Q</td>
<td>4</td>
<td>Reactive Power</td>
</tr>
<tr>
<td>H2</td>
<td>4</td>
<td>Distortion Power</td>
</tr>
<tr>
<td>sensedv</td>
<td>128</td>
<td>Simulated current assuming the inductive reactance to be 1 ohm.</td>
</tr>
<tr>
<td>Isimu</td>
<td>2</td>
<td>Simulated current after scaling down</td>
</tr>
<tr>
<td>PS</td>
<td>1</td>
<td>Simulated real power</td>
</tr>
<tr>
<td>HI</td>
<td>4</td>
<td>Upper bound for the variable in the RMS algorithm</td>
</tr>
<tr>
<td>LO</td>
<td>4</td>
<td>Lower bound for the variable in the RMS algorithm</td>
</tr>
<tr>
<td>Old</td>
<td>1024</td>
<td>Previous value of the guess used in the RMS algorithm</td>
</tr>
<tr>
<td>SQI</td>
<td>1024*64</td>
<td>Sum of the square of the load current (64 points).</td>
</tr>
<tr>
<td>S2</td>
<td>16</td>
<td>Apparent power squared</td>
</tr>
<tr>
<td>HS</td>
<td>16</td>
<td>Square of the harmonic (distortion) power</td>
</tr>
<tr>
<td>Vr</td>
<td>32767</td>
<td>The first extracted current signal converted to a voltage signal</td>
</tr>
<tr>
<td>Symbol</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>Vr2</td>
<td>32767</td>
<td>The second extracted current signal converted to a voltage signal</td>
</tr>
<tr>
<td>Ph1</td>
<td>2000</td>
<td>Small real power due to the first injected signal</td>
</tr>
<tr>
<td>Ph2</td>
<td>400</td>
<td>Small real power due to the second injected signal</td>
</tr>
<tr>
<td>wt0</td>
<td>786816</td>
<td>A variable to accumulate the phase angle for the fundamental signal</td>
</tr>
<tr>
<td>wt0t</td>
<td>192</td>
<td>Incremental phase for the fundamental frequency signal</td>
</tr>
<tr>
<td>wt0c</td>
<td>786816</td>
<td>A variable to accumulate the phase angle for the fundamental signal phase shifted to match with the output voltage</td>
</tr>
<tr>
<td>wh1</td>
<td>64</td>
<td>Frequency in radians/sec for the first injected signal. For scaling, a “shifted window” technique has been used. (wh1 - 300)*64</td>
</tr>
<tr>
<td>wt01</td>
<td>131136</td>
<td>A variable to accumulate the phase angle for the first injected signal</td>
</tr>
<tr>
<td>wt01c</td>
<td>131136</td>
<td>A variable to accumulate the phase angle for the first injected signal phase shifted to match with the signal at the inverter output.</td>
</tr>
<tr>
<td>wt01t</td>
<td>192</td>
<td>A variable to accumulate the phase angle for the first injected signal phase shifted to match with the signal at the inverter output.</td>
</tr>
<tr>
<td>wh2</td>
<td>64</td>
<td>A variable to accumulate the phase angle for the fundamental signal</td>
</tr>
<tr>
<td>wt02</td>
<td>131136</td>
<td>Incremental phase for the second injected signal</td>
</tr>
<tr>
<td>wt02c</td>
<td>131136</td>
<td>A variable to accumulate the phase angle for the second injected signal phase shifted to match with the output voltage.</td>
</tr>
<tr>
<td>wt02t</td>
<td>192</td>
<td>A variable to accumulate the phase angle for the second injected signal</td>
</tr>
<tr>
<td>wh20</td>
<td>64</td>
<td>Radian changes with the time,(*4096) to get the int form</td>
</tr>
<tr>
<td>BW</td>
<td>512</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>Vref</td>
<td>128</td>
<td>Output voltage</td>
</tr>
<tr>
<td>Vrefc</td>
<td>128</td>
<td>Output voltage</td>
</tr>
<tr>
<td>V</td>
<td>128</td>
<td>Peak output voltage</td>
</tr>
<tr>
<td>ih1</td>
<td>32767</td>
<td>The first injected current</td>
</tr>
<tr>
<td>ih2</td>
<td>32767</td>
<td>The first injected current</td>
</tr>
<tr>
<td>Ihh</td>
<td>16</td>
<td>harmonic current RMS</td>
</tr>
<tr>
<td>Vh1</td>
<td>128</td>
<td>/PEAK injected voltage 1 ,(*16384) to get the int form</td>
</tr>
<tr>
<td>Vh2</td>
<td>128</td>
<td>PEAK injected voltage 2 ,(*16384) to get the int form</td>
</tr>
<tr>
<td>Vh1</td>
<td>128</td>
<td>injected voltage 1</td>
</tr>
<tr>
<td>Vh2</td>
<td>128</td>
<td>injected voltage 2</td>
</tr>
<tr>
<td>Uvh1</td>
<td>16384</td>
<td>reference to get ih1</td>
</tr>
<tr>
<td>Uvh2</td>
<td>16384</td>
<td>reference to get ih2</td>
</tr>
<tr>
<td>Uvp</td>
<td>16384</td>
<td>reference to get ip</td>
</tr>
<tr>
<td>Uvq</td>
<td>16384</td>
<td>reference to get iq</td>
</tr>
<tr>
<td>Vq</td>
<td>128</td>
<td>quadrature voltage signal</td>
</tr>
<tr>
<td>XIH1F1[3]</td>
<td>1</td>
<td>IIR lowpass filter with floating point coefficients for the signal extraction loop.</td>
</tr>
<tr>
<td>YIH1F1[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>XIH1F2[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YIH1F2[3]</td>
<td>1</td>
<td>for LPF in getting ih1</td>
</tr>
<tr>
<td>XIH1P[2]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YIH1P[2]</td>
<td>1</td>
<td>for I/PI in getting ih1</td>
</tr>
<tr>
<td>XIH2F1[3]</td>
<td>1</td>
<td>for LPF in getting ih2</td>
</tr>
<tr>
<td>YIH2F1[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>XIH2F2[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YIH2F2[3]</td>
<td>1</td>
<td>for LPF in getting ih2</td>
</tr>
<tr>
<td>XIH2P[2]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YIH2P[2]</td>
<td>1</td>
<td>for I/PI in getting ih2</td>
</tr>
<tr>
<td>XPL[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YPL[3]</td>
<td>1</td>
<td>for LPF in getting P</td>
</tr>
<tr>
<td>XQL[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YQL[3]</td>
<td>1</td>
<td>for LPF in getting Q</td>
</tr>
<tr>
<td>XHL[3]</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>YHL[3]</td>
<td>1</td>
<td>for H calculation</td>
</tr>
<tr>
<td>Htemp</td>
<td>1</td>
<td>temp variable used in PLLs</td>
</tr>
<tr>
<td>Rtemp</td>
<td>1</td>
<td>temp variable used in PLLs feedback loop</td>
</tr>
<tr>
<td>Temp</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Htemp2</td>
<td>1</td>
<td>temp variable used in PLLs</td>
</tr>
<tr>
<td>Rtemp2</td>
<td>1</td>
<td>temp variable used in PLLs feedback loop</td>
</tr>
<tr>
<td>Temp2</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

The following shows the constants used in the C code.

<table>
<thead>
<tr>
<th>H</th>
<th>4096</th>
<th>FIR Filter coefficients for the first stage of decimation (1:6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hh</td>
<td>4096</td>
<td>FIR Filter coefficients for the second stage of decimation (1:3)</td>
</tr>
<tr>
<td>Wh20</td>
<td>64</td>
<td>Second injected frequency at no load</td>
</tr>
<tr>
<td>BW0</td>
<td>512</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>Vmax</td>
<td>128</td>
<td>Maximum allowable voltage amplitude</td>
</tr>
<tr>
<td>Vmin</td>
<td>128</td>
<td>Minimum allowable voltage amplitude</td>
</tr>
<tr>
<td>E</td>
<td>128</td>
<td>Nominal output voltage amplitude</td>
</tr>
<tr>
<td>Pmax</td>
<td>4</td>
<td>Maximum real power limit</td>
</tr>
<tr>
<td>Pmin</td>
<td>4</td>
<td>Minimum real power limit</td>
</tr>
<tr>
<td>Qmax</td>
<td>4</td>
<td>Maximum reactive power output</td>
</tr>
<tr>
<td>Qmin</td>
<td>4</td>
<td>Minimum reactive power output</td>
</tr>
<tr>
<td>H2max</td>
<td>4</td>
<td>Maximum harmonic power output</td>
</tr>
<tr>
<td>Bwmax</td>
<td>512</td>
<td>Minimum bandwidth output</td>
</tr>
<tr>
<td>Bwmin</td>
<td>512</td>
<td>Minimum bandwidth output</td>
</tr>
<tr>
<td>Df</td>
<td>16</td>
<td>Droop coefficient for the fundamental frequency</td>
</tr>
<tr>
<td>Df1</td>
<td>16</td>
<td>Droop coefficient for the injected signal 1</td>
</tr>
<tr>
<td>Df2</td>
<td>16</td>
<td>Droop coefficient for the injected signal 2</td>
</tr>
<tr>
<td>Dv</td>
<td>0.5</td>
<td>Droop coefficient for the voltage droop</td>
</tr>
<tr>
<td>Dbw</td>
<td>512</td>
<td>Droop coefficient for the bandwidth droop</td>
</tr>
</tbody>
</table>
Appendix IV: M-files

% The following M File simulates the effect of line impedance and % unit to unit variations on reactive power sharing.

r=2; % Load resistance
L=0.0053; % Load inductance
w = 377; % System frequency
x1 = 0.1; % Output/line impedance of unit 1
x2 = 0.5; % Output/line impedance of unit 2
v1 = 120; % Output voltage of unit 1
v2 = 120; % Output voltage of unit 2
D = 0.00001; % Droop coefficient used

for i=1:100
    % dl is the phase angle of unit 1 voltage
    dl = (v1*x2+x1*v2)*(r*(x1*x2+w*L*(x1+x2))-w*L*r*(x1+x2))/(2*v1*x2*(w*L*(x1*x2+w*L*(x1+x2))+r*r*(x1+x2)));
    % v is the load voltage
    v = (-2*v1*x2*w*L*dl+r*(v1*x2+v2*x1))/(r*(x1+x2));
    % d2 is the phase angle of unit 2 voltage
    d2 = dl*x2*v1/v2/x1;
    % I1 and I2 are unit currents
    I1 = (v1*cos(dl)+j*v1*sin(dl)-v)/(j*x1);
    I2 = (v2*cos(d2)+j*v1*sin(d2)-v)/(j*x2);
    % I is the load current
    I = I1+I2;
    % Find the rms values of the currents
    llrms = abs(I1);
    l2rms = abs(I2);
    lrm = abs(I);
    % calculate the powers
    P1 = v1*v/x1*dl;
    P2 = v2*v/x2*d2;
    P1cal = real((v1*cos(dl)+j*v1*sin(d1))*conj(I1));
    Q1cal = imag((v1*cos(dl)+j*v1*sin(d1))*conj(I1));
    P2cal = real((v2*cos(d2)+j*v2*sin(d2))*conj(I2));
    Q2cal = imag((v2*cos(d2)+j*v2*sin(d2))*conj(I2));
Pcal = real(v*conj(I));
Qcal = imag(v*conj(I));

% calculate the unit voltage after the droop.
vl = vl - Q1cal*D;
v2 = v2 - Q2cal*D;

% Impose the limit on voltage variation
if vl < 108
 v1=108
end
if v2 < 108
 v2=108
end
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% The following M-File calculates the coefficients of a FIR filter %
% using a Hamming window. %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

fc=100; % Passband
tw=245 % Transition band
fs=4098; % sampling rate
delf=tw/fs;

N=round(3.3/delf); % Hamming window

if (round(N/2) - N/2) == 0,
 N=N+1;
end
fcdash=(fc+tw/2)/fs;

hd(1)=2*fcdash;
h(1)=hd(1);
h((N-1)/2+1)=h(1);

for n =2:(N-1)/2+1,
hd(n-1)=2*fcdash*sin(2*pi*fcdash*(n-1))/(2*pi*fcdash*(n-1));
w(n-1)=0.54+0.46*cos(2*pi*(n-1)/N);
h(n-1)=hd(n-1)*w(n-1);
h((N-1)/2+n)=h(n-1);
end

h(1)=h(N);
for n = 2:(N-1)/2,
h((N-1)/2-n+2)=h((N-1)/2+n);
end

hint=round(4096*h); % Convert into integers
wc = 5*2*pi;  % 5 hz cutoff frequency
fs = 683;    % 683 Hz sampling rate
zeta = 0.5;
wc dash = tan(wc*l/2/fs);
B0 = (1+2*zeta*wc dash + wcdash*wcdash);
B1 = -2+2*wcdash*wcdash;
B2 = l-2*zeta*wc dash + wcdash*wcdash;
B = [B0/B0 B1/B0 B2/B0];
A = (wcdash*wcdash/B0)*[1 2 1];

Fgain=0.05;        % Feedback gain (voltage sensor gain)
Ki = 5;            % Current controller proportional gain
Kv = 0.1;          % Voltage controller proportional gain
Ti = 0.00016667;   % Current controller integral gain
Tv = 0.0001;       % Voltage controller integral gain
V = 1.5;           % variable gain in the voltage loop (0.5 - 2.0)
L = 0.0012;        % Filter inductance of the inverter
C = 10e-6;         % Filter capacitance of the filter
B = 0.0781;        % Current sensor gain

hold off
for R=5:20:100    % Load resistance changed
    numGc = Ki*[Ti 1];
    denGc = [Ti 0];
    numGv = Kv*[Tv 1];
    denGv = [Tv 0];

    numn = Fgain*V*conv(numGc,numGv)*R;

    denCV=conv(denGc,denGv);
    dend1 = R*L*C*conv([l 0 0],denCV);
    dend2 = L*conv([l 0],denCV);
    dend3 = B*C*R*conv([l 0],conv(numGc,denGv));
    dend4 = (R+B)*denCV+conv(numGc,denGv);
dend = dend1+[0 dend2]+[0 dend3]+[0 0 dend4];
bode(numn,dend);
if R==5
  hold
  end
end

hold off