A Built-In RMS-to-DC Converter for Power Supply Monitoring of Analog/Mixed-Signal Circuits

by

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Abstract

Recently, the interest in analog and mixed-signal IC test has been raised dramatically. The development of high speed and high performance analog/mixed-signal circuits embedded in a single chip with their digital peer keeps posing new challenges to VLSI test engineers. Built-in self-test (BIST) schemes have been recognized as capable of bringing improvements to analog and mixed-signal circuits testing. The power supply current monitoring as a structural testing methodology, which is applicable to both digital and analog/mixed-signal circuits testing, has recently been attracting more attention from both academia and industry.

In this thesis, the power supply monitoring of analog and mixed-signal circuits testing is reviewed. A BIST scheme is presented for power supply rms current testing. A new built-in rms-to-dc converter is proposed. The RMS-to-DC computation is carried out in the current domain. The system generates a digital signature proportional to the RMS value of the supply current. The digital signature is critical for an effective on-chip decision. A new MOS current squarer/divider circuit required in the converter is also proposed and implemented in a standard 0.18 μm CMOS technology. Silicon measurement results illustrate that the total harmonic distortion is less than 1.1%. The RMS-to-DC converter has been implemented in the standard 0.35 μm CMOS technology. The total on-chip capacitance is only 74 pF. The effectiveness of the RMS-to-DC converter has been verified by simulation. The simulated relative error of the RMS-to-DC converter is less than 1% with a 100 KHz sinusoidal input signal. This circuit is suitable for BIST applications on analog and mixed-signal ICs.
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<td>VLSI</td>
<td>Very Large Scale Integration</td>
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<td>BIST</td>
<td>Built-In Self-Test</td>
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<tr>
<td>DFT</td>
<td>Design For Testability</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>ASIC</td>
<td>Applications Specific Integrated Circuit</td>
</tr>
<tr>
<td>ATE</td>
<td>Automatic Test Equipment</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
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<tr>
<td>RMS</td>
<td>Root Mean Square</td>
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<tr>
<td>LPF</td>
<td>Low-Pass Filter</td>
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<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
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<tr>
<td>LFSR</td>
<td>Linear Feedback Shift Register</td>
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<tr>
<td>I/O</td>
<td>Input/Output</td>
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<td>HCI</td>
<td>Half Cycle Integrator</td>
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To my family and Susan Nan, for their endless help and encouragement in my life
Chapter One

Introduction

1.1 Motivation for Analog and Mixed-Signal Testing

Since 1960's, the integrated circuit (IC) technology has brought great progress to all aspects of daily life in the fields as diverse as entertainment, computing, communication and so on. The IC testing technology development has always accompanied this continuing trend. With the rapid advancement in IC technology, testing became one of the major factors in determining the time to market of ICs. Historically, the primary goal of a test process is to determine if the units produced by the manufacturing process are defect-free and will function as desired. A second important goal of a test process is to improve the process yield and thereby reduce the costs. The process yield refers to the ratio of good ICs to the total number of ICs fabricated [1]. Testing plays an indispensable role in the IC manufacturing process.

The development of complex and high performance digital ICs technology has created a great need for new methods of system testing and fault prediction. A variety of test techniques for digital circuits enable us to clearly predict the importance and success of testing. With the growth of IC technology, ICs with digital, analog, and mixed-signal circuits (e.g., ADC and DAC as interface between ICs and real world) on the same substrate are common. Generally, the analog and mixed-signal components merely serve as interfaces between digital processing circuitry and real-world analog signals, and usually occupy a much smaller fraction of silicon area than the digital components. The testing time and costs for these so-called “big-D, little-A” structures, however, constitute a large portion of the entire test procedure. For example, many companies report that
80% of test effort is directed at the 20% of the chip area that is mixed-signal [2]. This obstacle significantly increases the time-to-market and engineering costs. The primary reason for this is the lack of Automatic Test Equipment (ATE) comparable to that which successfully exists for testing digital circuits. The ATE for analog/mixed-signal testing is not widely available due to the stringent demands of analog and mixed-signal circuits testing. This drawback brings up a strong economic imperative to advance analog and mixed-signal IC test. Recently, analog and mixed-signal IC testing has received substantial attention from both academic researchers and industry. It has become one of the hottest issues in IC testing research. Instead of conventional external ATE and Design for Test (DFT), a new hierarchical test solution, embedded test, has been raised by both industry and academia. Embedded test is a combination of external ATE and DFT that integrates the high-speed and high bandwidth portions of the external ATE directly into the ICs. An attractive solution of embedded test is the application of BIST and test access port (TAP) that is widely used in the digital boundary scan testing.

1.2 Analog and Mixed-Signal Test Issues and BIST

Unlike the testing of digital ICs that has profited from the use of structured design for testability to achieve high fault coverage, analog and mixed-signal circuits, traditionally, have been tested by verifying their functional specifications. In general, structural testing, which verifies the individual logic gates or transistors, uses a pattern set that has a known fault coverage to stimulate the circuit under test (CUT). Functional testing, on the other hand, checks certain aspect of the expected design behavior. In analog functional testing, the measured value is compared with the expected value within a range of values, whereas only one specific value is required for digital testing. Since the analog and
mixed-signal circuits are more sensitive to the parasitic than digital circuit, the acceptable tolerances are often determined by simulation, measurement inaccuracies, and process variations. Some test methodologies have been widely studied for analog and mixed-signal circuit testing, such as fault modeling, test generation, design-for-test (DFT), and built-in self-test (BIST). Among these methods, BIST, as a hierarchical DFT, attracts more attentions from both academia and industry because of some of its excellent features, such as high-quality testing and low cost.

1.2.1 Generic IC BIST Structures

Built-in self-test (BIST) is one of the practical design-for-test (DFT) strategies [3]. It reduces the need of external test. A typical BIST methodology is shown in Fig. 1.1. Generally, a test task may be broken down into two aspects. Firstly, the device-under-test (DUT) or the circuit under test (CUT) must be stimulated. Then, the measured output must be analyzed.

![Fig 1.1 Generic IC BIST Methodology](image)

With BIST, a micro tester with a pattern generator is brought onto the chip, enabling the chip to test itself. To stimulate the analog CUT in BIST, a precise analog test stimulus generator must be integrated to form the BIST circuitry. A number of papers have been published on the so-called on-chip Delta-Sigma (ΔΣ) signal generation [4][5]. Also, to analyze the stimulated response, a test response analyzer is required. For analog circuits, the analysis of the output response is complicated by the fact that analog signals are
inherently imprecise due to the noise and parametric tolerances of the circuits under test (CUT). Some main approaches have been reported for analyzing the test response [6]. They are

1) Analog checkers: Analog checkers directly compare the stimulated response with the expected analog behavior, which might be previously stored results or simultaneously stimulated results from a fault free circuit. Analog checkers provide a common and straightforward approach which widely applied in board level analog verification.

2) Analog signature: Compression schemes for compacting the output response of CUT can be included to generate a distinct signature. For example, the simplest compression scheme, a digital integrator, can be used to compress analog output waveform into a single integration value as an analog signature [7] by which more information of an analog circuit can be obtained with a BIST scheme. With BIST, since testing is performed on-chip, the internal nodes of a CUT can be accessed by a BIST core. Therefore, by using a multiple-input analog signature analyzer for on-chip response evaluation, the information of the internal nodes of CUT can be observed in addition to that of the primary outputs [8].

3) Digital signature: In this approach, the analog to digital conversion scheme presents to convert the analog response into digital vectors proportional to the analog response as a digital signature. This digital signature can be treated as that of digital BIST, for example, shifted off chip with the boundary scan available on most digital chips or evaluated by on-chip digital circuity. With respect to area overhead and design simplicity, integrating ADCs based on the switched-capacitor integrator and counter are suggested in [9] to replace complex analog-to-digital conversion techniques.
4) **Pseudorandom testing**: Another effective BIST technique that attracts attention is pseudorandom testing for mixed-signal circuits [10]. With this strategy, one models the analog circuit under test (CUT) as a digital system by embedding the analog CUT between a DAC and an ADC, and then applies digital pseudorandom patterns generated from a linear feedback shift register (LFSR) to the CUT. By this way, the on-chip analog signal generation can be avoided and the test response analysis can be evaluated with the digital signature. However, since the input of analog circuit after DAC is a pseudorandom waveform, it is critical to differentiate the result from other stimulated response. Therefore, the efficiency of the pseudorandom technique relies on the proper choice of signatures and discrimination schemes to distinguish between the fault-free circuit and the faulty circuit in the signature space. This poses difficulties in actual applications.

**1.2.2 The Characteristics of a BIST Scheme**

The advantages of BIST schemes originate from several features:

1) **Low cost**: This includes the savings on both the test equipment and the chip cost. The developments of the analog and mixed-signal circuits, e.g. high performance (resolution, signal-to-noise, and signal bandwidth), lead to more stringent requirements and challenges to the analog and mixed-signal test instrumentation. This type of testers with demanding requirements of speed, precision, memory and noise margin are usually very expensive. For example, today, high-end ATE cost is approximately five million U.S. dollars [11]. Also, the rapid upgrading requirement with fast ICs development hazards the long-term capital investment of ICs Industry on ATE. Unlike external equipment, a one-time investment of BIST scheme stays with the semiconductor product throughout its complete lifecycle. It goes wherever the semiconductor product goes: from wafer to
system, from factory to field. BIST, by nature, is re-usable. Also, the off-chip test usually requires extra testing I/O pins that increase the chip costs. Although, with BIST scheme, the cost on extra silicon and on-chip memory may increase, the cost on the entire chip can be saved significantly when we compare the cost increase with the saving from external ATE and extra testing I/O.

2) *Good accuracy*: Since BIST does not require the off-chip test equipments, it reduces the external cable effect and packaging effects present with off-chip testing. Also, it increases the possibility of monitoring the internal nodes of a CUT. Analog circuits usually require high precision test due to tight design margins, however, the external cables between the tester and the chip introduce parasitic that affects test quality. A BIST scheme also avoids the performance degradation resulting from packaging effects by bringing the analog signal into or off-chip. Just getting test signals into and out of the IC can cause crosstalk and jeopardize the IC's performance. It results in an expensive solution to acquire a better mixed-signal tester to improve the testing environment. Also, BIST offers the ability of observing the internal nodes of the CUT. It allows the testing of untestable performance characteristics, such as noise levels of internal nodes of an IC, on a wafer, or in a system. A panel discussion at the 1996 VLSI Test Symposium (VTS) concluded that BIST eventually would be the only practical design-for-test (DFT) method for high-frequency ICs, because of the difficulty of accessing signals without affecting the signals themselves [2].

3) *Fast test*: Embedding equipment functionality into semiconductor-based products not only reduces the burden on the complexity of external equipment, but also improves on-chip access of internal signal and speeds up testing. With BIST, the CUT contains the test
stimulus generation and responses capture hardware. The time to generate, apply test patterns to a CUT, and compare the test response signature during production-time testing can easily become shorter. Moreover, since no external tests are supplied, many blocks can run their own self-test simultaneously at a high clock rate. Thus, the main advantages of BIST are the reduced testing time through parallel test execution and high-speed testing. For high volume production of mixed-signal ICs, the high-speed testing time reduces the time-to-market of ICs.

Although mixed-signal BIST has many advantages and attracts the most attention from academia, few companies have reported using these BIST solutions in their own products. Why? Is the BIST solution not of industrial strength? The lack of practical applications exposes the significant limitations of BIST schemes. These limitations include:

1) *Area overhead:* Although it saves extra testing pins, BIST circuitry usually occupies extra silicon area. Additionally, the partition technique, which is often applicable in BIST application to partitions the CUT into small blocks for testing purpose, demands more BIST modules and then more chip area. In turn, the additional BIST area required on chip results in a decrease in both yield and reliability because of its influence on the function blocks.

2) *Performance degradation:* Inserting analog and mixed-signal BIST circuits may impact performance of the CUT. For example, the added capacitance and resistance may decrease speed, add noise, and increase crosstalk. Any reduction in power supply voltage or current delivery due to addition of test circuitry also impacts the performance of the CUT.
3) *Implementation difficulty*: Sometimes, the BIST scheme requires the added circuitry for greater accuracy than the CUT. However, because the CUT usually has been designed with the maximum accuracy available from the manufacturing process, any additional accuracy needed for test circuitry is impractical. This fact puts implementation difficulties on a BIST designer.

4) *Process sensitivity*: Generally, analog circuitry proven in one manufacturing process must be re-proven in each new process. Also, any change to an analog design must be re-simulated to determine the impact of parasitics.

5) *Non-Automation CAD*: Automatic insertion CAD of analog circuitry is not yet commercially available at the schematic or layout level. Up to now, the BIST had to be inserted manually.

To concisely summarize the above, industry and academia agree that mixed-signal BIST would be the best solution to mixed-signal test because it addresses test access, test reuse, and ever-higher performance. However, area-efficient BIST solutions offered to date are not of industrial strength because they are not robust, automated, or diagnostic [2].

1.2.3 Analog BIST Architectures

Basically, there are two general BIST approaches, structural and non-structural. Structural approaches are of a general nature and they are suitable to reduce design time at the expense of higher area overhead. Non-structural approaches, or so-called functional specification approaches, are customized for specific designs. They can improve test quality and require less area overhead than the structured approaches. However, they require long design time. For example, due to the requirement for different types of test stimulus in functional testing, it becomes very difficult to thoroughly test the CUT. Also,
the functional test techniques usually cannot provide a measure of test effectiveness with respect to physical defects. In other words, it cannot diagnose and locate the defects. Unfortunately, this is important for testing since testing eventually has to increase the yield and reduce cost through diagnosing and locating the defects. To date, testing of analog circuits is mainly done by functional criteria. This is opposed to testing digital ICs in which the functionality of the circuit is verified during the design simulation phases and the final tests concentrate on verifying the structure of the fabricated circuits. Therefore, in order to diagnose and locate the defects, it is important to develop the effective structural BIST approaches for analog and mixed-signal circuit testing instead of the functional testing.

In summary, the structural techniques can provide a uniform test solution for most mixed-signal circuits. Furthermore, the diagnosis of defects requires the application of structural BIST.

1.3 BIST for Current Testing - Power Supply Current Monitoring

Conventional analog tests are based on voltage measurements, but recently a great deal of effort has been dedicated to the field of power supply current monitoring in both digital and analog/mixed-signal circuit testing, e.g. [12][13][14][15]. In current-based testing, the current passing through the VDD or GND terminals of an IC is monitored during the application of an input stimulus. The use of current rather than voltage may help reduce the problem of limited voltage swing encountered in modern VLSI processes caused by technology scaling. As the power supply current is a general parameter for both digital and analog devices, it is reasonable to develop a structural test technique applicable to both digital and analog/mixed-signal circuits by monitoring the power supply current. As
quiescent supply current monitoring (I\textsubscript{DDQ}) has become a standard test technique for CMOS digital circuits, this success has promoted its extension to analog and mixed-signal circuits testing (I\textsubscript{DD}) [16][17]. Practical experience has demonstrated that using current monitoring as a preliminary screening test can eliminate a large number of faulty chips. The supply current monitoring in analog and mixed-signal circuits (I\textsubscript{DD} testing), however, is a more difficult task because the power supply current depends not only on the state of the circuit and the value of the circuit parameters, but also on the input signal and the internal branch currents of the circuit [18]. Since the supply current monitoring is a structural approach, it may be required to test over a broad range of input signals and may result in a relatively long testing time window. Some investigation results suggest that supply current monitoring, although not sufficient alone, can offer additional fault coverage for analog and mixed-signal circuits. In practice, a combination of structural and functional test has been adopted to increase the fault coverage [19].

1.4 Thesis Organization

The motivation of this research work was to provide a built-in current RMS-to-DC converter as a means of signature generation for the power supply current monitoring BIST applications. By introducing the power supply current monitoring as one of the effective BIST solution, this thesis focuses on the signature generation circuitry design of the analog/mixed-signal supply current monitoring. The organization of this thesis is as following.

In this thesis, the contents are divided into 5 chapters. A graphical overview structure of thesis organization is shown in Fig. 1.2.
Chapter 1. Introduction. Review of the typical BIST schemes usually adopted in the analog and mixed-signal testing is presented. Pertinent characteristics of BIST schemes, including both advantages and drawbacks, are presented. Both structural and non-
structural (functional) BIST architectures are discussed. The power supply current monitoring is introduced as an effective structural BIST solution.

Chapter 2. Power Supply Current Monitoring. The power supply current monitoring method is reviewed for both digital and analog/mixed-signal testing. Some successful methods are compared according to their effectiveness. The RMS current monitoring is studied in depth and concluded to be a better solution as a means of signature generation technique. Previous work in our group at UBC, a built-in current integrating circuit, is reviewed and a further application of this new technique to an RMS-to-DC converter is described. RMS-to-DC conversion, one of the off-chip testing techniques available in most ATE, is discussed.

Chapter 3. A Built-In RMS-to-DC Converter. In order to design a built-in power supply current monitoring circuit, a novel built-in RMS-to-DC converter is proposed for the BIST application. The converter adopts the classical implicit method of RMS-to-DC conversion technique. The operation of the RMS-to-DC converter is described. Before the description of a new MOS current squarer/divider, which is required in the RMS-to-DC converter, is presented, the MOS translinear principle is reviewed. The detailed synthesis and analysis procedure of the current squarer/divider is explained.

Chapter 4. The Simulation and Measurement Results. The class B current squarer/divider is implemented in standard 0.18μm CMOS process. The silicon measurement results are reported. The built-in RMS-to-DC converter is designed in 0.35μm CMOS process. The simulation results illustrate that it is an alternative solution for the BIST application.

Chapter 5. Conclusions.
1.5 Conclusion

In this introduction chapter, the generic BIST scheme has been reviewed. A few characteristics are presented to depict that BIST is one of the most effective analog and mixed-signal circuits testing solutions. Structured BIST is studied due to its capability of diagnosing and locating the defects. Both academia and industry agree that mixed-signal BIST will be the best solution for mixed-signal test because it addresses test access, test re-use and ever-higher performance. However, area-efficient BIST solutions offered to date are not industrial strength because they are not robust, automated, or diagnostic. The power supply current monitoring is recently attracting more attention from both academia and industry. It is proposed as a good alternative solution of structured BIST both in the digital and analog/mixed-signal testing domain.
Chapter Two

Power Supply Current Monitoring

2.1 Power Supply Current Monitoring Applicable To Both Digital And Analog/Mixed-Signal Circuit Testing

With the fast development of the high performance IC techniques, there is a continuing trend to put more functionality, both digital and analog/mixed-signal functions, on the same silicon die. For example, most data communication application specific integrated circuit (ASIC) chips today, e.g., asynchronous transfer mode (ATM) chips, have both digital processors and analog/mixed-signal data/clock recovery modules on the same die. Time-to-market and test costs have pushed industries to invest a huge amount of capital in developing a variety of test techniques for both digital and analog/mixed-signal circuits. From another point of view, the number of developed testing methods makes it difficult to make a decision on which strategy to apply to a specific design. Also, a number of different testing methods applied on a single chip would increase the testing difficulty. For example, the majority of structured testing approaches available today require careful portioning of the digital and analog sections to satisfy the controllability and observability requirements to test each section [20]. Then, a different testing method is applied to each part. In this way, it could result that many different test strategies be present on the same chip. The chip designers have to design testing modules with different technique and the test engineers also have to handle and analyze different types of testing data.

To minimize the number of different testing strategies on the same chip, some researchers tried to figure out if a structural testing methodology applicable to both digital and
analog/mixed-signal circuits exists. If this kind of uniform method is possible, we can test the mixed-signal chip by a single testing strategy. In this case, the ideal uniform testing methodology would have the following features [21]:

1) Applicable to digital as well as analog systems;

2) Reduced fault modeling requirements;

3) Eliminated completely the need of any partitioning of hybrid systems into their respective analog & digital subsystems for purposes of testing;

4) Simplified the test generation process;

5) BIST or ATE feature.

Power supply current monitoring satisfies the above objective and is applicable to both digital and analog/mixed-signal circuits. As the general parameter of both digital and analog/mixed-signal circuits, power supply current can be monitored for detection of faults. Generally, in the power supply current monitoring technique, the current passing through the VDD or GND terminals is monitored during the application of an input stimulus. For specific inputs, this current may raise or drop to abnormal levels in the presence of defects. Power supply current monitoring is also notated as $I_{DDX}$ monitoring, which includes a variety of $I_{DD}$ testing types, such as dynamic supply current $I_{DDD}$, quiescent supply current $I_{DDQ}$, and transient supply current $I_{DDT}$.

Quiescent supply current monitoring ($I_{DDQ}$ test) has proven to be a cost-effective technique able to achieve a high test quality and improve design reliability for digital circuits by monitoring the quiescent supply current [22]. Practical experience has demonstrated that using current monitoring as a preliminary screening test can eliminate a large number of faulty chips [23]. Studies have also indicated that the dynamic supply
current $I_{DD}$ monitoring technique for analog and mixed-signal circuits can have similar advantages as $I_{DDQ}$ testing applied to digital CMOS circuits [24]. The practical application of the power supply current monitoring technique to a mixed-signal phase-locked loop (PLL) has revealed the effectiveness at detecting faulty circuits [25].

2.2 Power Supply Current Testing of Analog Circuits

2.2.1 Power Supply Current Monitoring Architectures

In general, power supply current measurement can be carried in two ways, off-chip and on-chip (BIST). The off-chip power supply current measurement approach requires an automatic test machine (ATE) to apply stimulus and sense the supply current. Also, as other off-chip testing, extra testing pins are usually needed to bring the current off chip. In [26], an analog off-chip $I_{DD}$ Measurement Unit (AOCIMU) was developed to perform power supply current testing of analog ICs in conjunction with a mixed-signal tester. The tester injects the analog stimulus and senses the supply current $I_{DD}$ from the CUT. Similar to many other off-chip testing, this approach results in cost penalty because extra test pins are required to bring the signals in and off chip. Also, a good testing environment is needed to eliminate the effect of parasitics introduced by interfacing the on/off-chip signals.

An alternative low-cost solution is a BIST scheme. A typical power supply current monitoring BIST methodology is shown in Fig. 2.1. In this case, the difference from the general BIST scheme shown in Fig. 1.1 is the presence of the built-in current sensing (BIC) circuit and the built-in test signature compression/generation circuit. The inclusion of a built-in current sensor (BICS) in a mixed-signal design makes it capable of providing on-chip current sensing. This application offers improved accuracy in the measurement of
$I_{DD}$ compared to that of the off-chip current sensing approach. Due to testing performance degradation because of the packaging effect, the off-chip current sensing approach reveals more limitations in a high-speed circuit. The BICS, therefore, is a practical solution which provides both a sensitive and comprehensive capability, particularly useful for the testing of high quality and high reliability ICs. The test signature generation block shown in Fig. 2.1 generates the test response signature, which can either be a digital or an analog compact signature. The actual signature type can be decided according to the testing application. For example, a digital signature may be chosen to perform an on-chip evaluation due to its simplicity and an analog signature may be chosen for its forward performance monitoring. More details on signatures are discussed in section 2.2.3.

![Fig. 2.1 BIST Structure for Power Supply Current Monitoring](image)
2.2.2 Built-In Current Sensors

Built-in current sensors (BICS) overcome the problems of off-chip current sensors, e.g., limited resolution, packaging effect (high currents in the I/O pad drivers), and fault masking by the digital noise or the noise from other analog blocks. The simplest MOS built-in current sensor is a simple current mirror based on two transistors. This general current mirror sensor has been applied to operational amplifier and 3-bit flash converter testing [27]. The results show that the area overhead and performance degradation are in the acceptable range.

However, as the CMOS technology is scaling down, e.g., from 0.5 μm to 0.35 μm and then to 0.18 μm, the second-order effects of MOS transistor, such as the $V_{DS}$ mismatch of simple current mirror due to the short channel effect, becomes obvious. This impacts the sensing accuracy and the normal operation of the CUT significantly. Therefore, the simple two transistor current sensor cannot be used without eliminating the second-order effects. Furthermore, in designing a built-in current sensor (BICS), two important factors must be considered. They are

1. $V_{DS}$ matching;
2. $V_{BIAS} = 0$ V.

The condition (1) is required to reduce the distortion between the supply current and sensed current. The condition (2) guarantees that the functionality of the CUT is not affected by supply voltage drop due to the BICS insertion.

A current mirror can be applied as a BICS, however, the traditional approach used to reduce the short channel effect to keep condition (1) in the 0.5 μm technology, simply
increasing the transistor length, is not suitable to the 0.18 μm technology with a lower 1.8v power supply. A new BICS is needed for the new low voltage technology.

A very successful BIC sensor architecture was proposed for first time in 1991 as a testing application. This is shown in Fig. 2.2 [28]. The test response evaluation block is not shown in this figure.

In this structure, two operational amplifiers (OPAMP) are adopted to modify the basic two transistor sensor. OPAMP1 sets the $V_{\text{BIC}}$ equal to $V_{\text{ref}}$ and offers a low input impedance for the basic current mirror. This reduces the CUT ground bounce effect ($V_{\text{BIC}} \neq 0$ V) caused by introducing the BICS. OPAMP2 keeps the $V_{ds}$ matched for the two transistors of the basic current mirror. In [29], the effectiveness of detecting defects by $I_{\text{DDQ}}$ testing was evaluated and showed to be a practical and accurate on-line current monitoring means. The silicon characteristics for the deep sub-micron application have been studied in depth by Tabatabaei and Ivanov [30]. Since the BICS is added into silicon
as an extra analog circuit, the influence on the performance of the CUT due to this inclusion should be considered. In order to minimize the influence of BICS, in practice, a partitioned structure should be considered such as a structure shown in Fig. 2.3 [31]. In this structure, the CUT is partitioned into smaller modules and multiple BICS are inserted to each partitioned block. There are two reasons to partition the CUT into smaller modules: the area overhead and the testing speed. The size of the BIC sensor is determined by the amount of current through the CUT. Partitioning the CUT into smaller modules reduces the current drop in the individual BIC sensor. In this way, smaller BICS are needed to sense smaller currents. Meanwhile, smaller BICS also reduce the capacitance seen by the BICS, C shown in Fig. 2.3, which in turn reduces the settling time for $I_{DD}$ measurement.

![Partitioned CUT](image)

**Fig 2.3 Partitioning and signature compression**

### 2.2.3 BIST Signature Types

The traditional concept for a supply current monitoring BIST scheme with different stimulus and different signature types is shown in Fig 2.4. To achieve effective testing, a suitable input stimulus must be derived [32]. Various signature generation methods exist,
such as transient response testing (TRT), quiescent (DC) and dynamic ($I_{DD}$) supply current monitoring, and steady-state supply current monitoring ($I_{rms}$). Among these methods, the DC and RMS current monitoring have been widely studied for offering simplicity and testing effectiveness.

In [33], several power supply current monitoring approaches are discussed and compared for analog/mixed-signal circuit testing: quiescent supply current monitoring (average $I_{DD}$), dynamic supply current monitoring ($I_{DD}$), and steady-state supply current monitoring ($I_{rms}$). Quiescent current monitoring is based on measuring the average $I_{DD}$ and dynamic testing is based on measuring the integral of $I_{DD}$ over time after applying a test vector, whereas $I_{rms}$ testing is based on measuring the root-mean square (RMS) value of the AC steady-state response of the supply current. In each case, if the measured value falls outside the predetermined fault-free tolerance range, the circuit is declared faulty. In practice, both average DC and RMS supply current tests may be applied, however,
research results have demonstrated that the RMS monitoring approach has the advantage over the average DC monitoring method because of the inclusion of the signal energy information which potentially avoids masking of faults occurring in the quiescent and dynamic supply current monitoring approaches and avoids employing complicated post-processing techniques to analyze the fault response [34].

To be applicable for full BIST, the approaches mentioned above require the integration of on-chip average and RMS current measurement circuits to replace the off-chip ATE instruments. Together with an on-chip signature analyzer, the pass/fail decision can be integrated on-chip. An on-chip current integrating circuit has been proposed in [30]. The latter has small silicon area, large bandwidth, good accuracy, and digital signatures, all indicating that the circuit is suitable for embedded analog circuit testing.

2.3 A Proposed Built-In Current ‘Averaging’ Circuit For DC Signature Generation

To design an on-chip average current or RMS current measurement circuit is equivalent to emulating the ATE instrument functionality. In general, there are two methods to emulate the ATE instrument functionality on-chip: DSP-based modules or analog modules. With the DSP-based test modules approach, an accurate analog-to-digital converter (ADC) and a digital signal-processing core are required. Although this method has been discussed widely, the analog modules approach is also attracting attention.

Equations 2.1 and 2.2 show the coherent form of two familiar currents measurements: DC and true RMS. In both cases, low-pass filters are used to produce a steady DC output in the analog implementation approach.

\[
\bar{I} = \frac{1}{T} \int I_a dt
\]

(2.1)
where $T$ represents the test period, or integration interval. In order to minimize signal ripple, a relatively large averaging time constant is always required to provide considerable attenuation at the test frequency, e.g., 100 ms in AD735 (Analog Devices) and MX536A/636 (MAXIM) is needed to average the signal down to 10 Hz. The conventional RC low pass filter with this large time constant requires an averaging capacitor in µF. This capacitance is far beyond the acceptable on-chip capacitance limited to 20~50 pF. This is why the analog signal processing method requires the off-chip capacitor. A number of methods have been investigated to find a good solution for the large on-chip time constant [35][36][37]. Although these methods can provide large time constants, the silicon area or the special process requirement make them unsuitable for on-chip implementation.

In [38], one technique was reported for DSP-based testing which replaced the filtering by *timed integration*. In this method, the integration DC current is computed by the discrete equivalents of an analog waveform, as shown in equation 2.3.

$$I_{in} = \frac{1}{M} \sum_{i=0}^{M-1} \left( \frac{1}{T_s} \int_{t_{i+1}}^{t_{i}} I_{in} dt \right)$$

where $T_s$ is the short timed integration window. By this technique, the long integration time is divided into multiple short time intervals.

Tabatabaei and Ivanov have designed and implemented a current integrating circuit by using the timed integration technique above aiming at BIST application. Strictly speaking, their built-in integrating circuit is actually an integrating ADC. It generates a digital signature proportional to the integration of the input current. The structure of this
proportional to the integration of the input current. The structure of this circuit is shown in Fig. 2.5. It is based on two identical switched-capacitor integrators and a counter.

![Fig. 2.5 Built-In integrating circuit block diagram with timed integration technique](image)

The operation of the integrating circuit in Fig. 2.5 is as follows. Two switched-capacitor integrators are used to integrate the input current in two separate short time windows. The duration of the short time window is chosen properly to reduce the amount of current to be integrated in a single short time window. In this way, the required on-chip capacitance can be reduced to a suitable value. In addition, either of the two switched-capacitor integrators and the counter constitute a single-slope integrating ADC that integrates the input signal only during the short timed integration window $T_s$.

There are two distinct characteristics required for achieving high accuracy with the above structure. These are:

1. To achieve a successive integration, a second switched-capacitor integrator is added to operate with the first in complementary time intervals resulting in a so-called double-phase built-in current integrator (double-phase BICI):
(2) The quantization residue from each integration interval is fed forward to the next to prevent the accumulation of quantization noise error. The integrating ADC implements the following equation (2.4):

\[ K_c \int I dt = V_\Delta \sum_{i=0}^{N-1} N_i + V_{R_{M-1}} \]  

(2.4)

where \( K_c \) is a constant. \( V_\Delta \) is the ADC quantization step, \( V_{R_{M-1}} \) is the (M-1)-th quantization error, and \( \sum_{i=0}^{N-1} N_i \) is the ADC output. Finally, the ADC gives the following result:

\[ N = \sum_{i=0}^{M-1} N_i = (Kc/V_\Delta) \int I dt - (V_{R_{M-1}}/V_\Delta) \]  

(2.5)

where \( N \) is the digital output number of integrating ADC. It is also the digital signature. In [38], the testing clock \( (f_{ck}) \) is 20 MHz. The \textit{short timed integration window} \( T_s \) equals 1 \( \mu s \) which results in the total number of short integration intervals \( M=1000 \) in equation (2.3). The total testing integration time can be as large as 1 ms. By using this ADC, the total on-chip capacitance can be reduced to as little as 74 pF. The simulation and the silicon results have shown a good accuracy (error <1%).

In summary, this built-in integrating circuit has several characteristics suitable for BIST applications, e.g. small area overhead, good accuracy, and digital signature. Moreover, the measurement result is an integration of the input value. With some small digital circuitry, for instance a counter and a divider, an average can be obtained.
2.4 Supply Current RMS Monitoring for Built-In Self-Test

2.4.1 On-chip RMS Current Measurement

In [38], a built-in power supply current DC monitoring scheme has presented. In a similar way, we propose a built-in power supply RMS current measurement scheme as shown in Fig. 2.6. In this structure, there are four testing blocks: on-chip signal generation, BICS, signature generation (built-in RMS-to-DC converter) and signature analyzer.

This thesis focuses on the built-in current RMS-to-DC conversion circuit design as a means of signature generation. The detailed design information for the current sensor described in Section 2.2.2 can be found in [30]. The silicon results show that this current sensor has very good properties for built-in applications.

In the proposed structure above, the power supply current is sensed by the built-in current sensor (BICS) and the RMS value is computed over a relatively long time window compared to the signal bandwidth. The RMS-to-DC converter generates a digital signature proportional to \( I_{\text{rms}} \). The digital signature is compared to the predetermined values in the signature analyzer to make the pass/fail decision. This feature is suitable for BIST applications since the digital signature can be easily evaluated on-chip by simple digital circuitry or off-chip by shifting the digital signature out of the chip serially. For
BIST applications, an on-chip RMS-to-DC converter requires the following features: small silicon area, good measurement accuracy, reasonable settling time, and a digital signature output.

2.4.2 Methods for RMS Computation

The root mean square (RMS) of the supply current is expressed as:

\[ I_{rms} = \sqrt{\frac{1}{T} \int_0^{T} i^2(t) \, dt} \quad \text{or} \quad I_{rms} = \sqrt{i^2(t)} \]  \hspace{1cm} (2.4)

where \( T \) is the measurement period of the input waveform \( i(t) \). There are plenty of methods known for measuring the RMS value of arbitrary current signals, e.g., thermal, electronic, electro-dynamic and electrostatic types. However, only the thermal and electronic converters have been monolithically fabricated to date. The thermal method is based on measuring the temperature of a resistor, heated by the Joule heat of the electrical current. The advantage of this converter type is the high bandwidth, which is limited by the parasitic capacitances of the input resistor to about 100 MHz. Although this method provides a wide bandwidth and good accuracy, it requires extra processing steps and complex packaging, making this method unsuitable for an on-chip implementation in a standard CMOS process. A second approach is the computing or electronic method. This method is based on nonlinear analogue signal processing, digital signal processing, or delta-sigma RMS conversion [39]. The digital signal processing method offers a fast response and good accuracy, but for arbitrary signal waveforms, spectral analysis, e.g., FFT, may be required to calculate the true RMS value of the input signal. This implies that the digital computing processor would occupy a large chip area and will require a relatively complex digital design. Thus, this approach does not lead to a low-cost and relatively non-complicated BIST solution.
Analog signal processing is an alternative solution. Traditionally, the analog signal processing method is based on the translinear property of bipolar circuitry. The difficulty of this method results from the need for at least one nonlinear function circuit, e.g., square, square root, multiplication or division. The disadvantages are the limited dynamic range and restricted bandwidth, e.g. 1% bandwidth of most electronic converters is less than 1 MHz.

Some research results [40] and market products, e.g. AD734 from Analog Devices and MX536A/636 from MAXIM, provide elegant solutions based on bipolar circuitry. Although the translinear method has been recognized as difficult to implement in standard CMOS processes, the recent development of CMOS translinear techniques offers the possibility.

Another important issue stopping the RMS-to-DC converters to be integrated into a single CMOS chip, is the low-pass filter. The low-pass filter acts as an averaging function in the RMS-to-DC converter. The requirement of large capacitance makes the integration difficult. In this thesis, we describe a new on-chip RMS-to-DC conversion circuit which utilizes the integrating circuit and timed integration techniques proposed in [30] and combines the analog and digital methods.

2.5 Analog Processing Methods for RMS-to-DC Conversion

There are two known methods for computing the RMS value of arbitrary signals based on nonlinear analog signal processing: the explicit method, and the implicit method [41]. The explicit method follows the RMS definition exactly and is based on the use of squaring, low-pass filter averaging, and square-rooting circuits, shown in Fig. 2.7. Researchers have developed a current-mode CMOS RMS-to-DC converter based on the
explicit method [42]. The major drawback of this method is its limited dynamic range and design complexity, which result from the direct squaring of the input signal and the nonlinear analog designs of both the squaring and the square-rooting circuitry, respectively.

Fig. 2.7 Classical explicit nonlinear circuit for RMS-to-DC conversion

The implicit method, shown in Fig. 2.8, solves the limited dynamic range problem by the automatic scale ranging provided by the feedback.

Fig. 2.8 Classical implicit nonlinear circuit for RMS-to-DC conversion

In the structure of Fig. 2.8, the low-pass filter outputs two identical currents. One is the output current $I_{\text{out}}$. The other is fed back as the divider of the current squarer-divider block. As shown in Eq. (2.5), the output current $I_{\text{out}}$ equals the mean value of $I_{\text{in}}^2$ divided by $I_{\text{out}}$. When the system reaches the steady state, $I_{\text{out}}$ will equal $I_{\text{rms}}$, the rms current of the input signal,
i.e.,

\[ I_{out} = \left( \frac{I_{in}}{I_{out}} \right)^2 \rightarrow I_{out} = \sqrt{I_{in}^2} \]  \hspace{1cm} (2.5)

This method is also the basis of nearly all commercially available RMS-to-DC converters. In this thesis, we present a built-in current RMS-to-DC converter based on the implicit method.

2.6 Conclusion

In this chapter, we have introduced that power supply current monitoring is an effective test methodology for both digital circuit quiescent \( I_{DDQ} \) and analog/mixed-signal circuit \( I_{DD} \) testing. BIST schemes which adopt supply current monitoring are shown to have speed and cost efficiency. The built-in current sensor (BICS) is introduced as a means for high speed and high performance circuit testing. A previous work on a built-in integrating circuit was reviewed. The theory of RMS-to-DC conversion was described. The pure digital processing method has an area overhead penalty, while the pure analog processing method including a nonlinear analog circuit may be hard to design and less accurate. Furthermore, the implicit method is more powerful and practical than the explicit method.

In the next chapter, we describe a built-in RMS-to-DC converter that uses the implicit method and integrating circuit discussed in this chapter. With the timed integration technique, the area overhead for the BIST application can be reduced.
Chapter Three

A Built-In RMS-to-DC Converter

3.1 Proposed Architecture of Built-In RMS-to-DC Converter

3.1.1 Basic Architecture

With the great progress of VLSI technologies, most instrumentation circuitry, e.g., a multimeter, can be integrated onto a single CMOS chip except for RMS-to-DC converters. Conventionally, monolithic electronics true RMS-to-DC converters are constructed in bipolar circuitry. However, to most applications that are fabricated in a modern CMOS process, a MOS RMS-to-DC converter is required in the BIST application for testing purposes. Thus, the integration of a MOS RMS-to-DC converter into a single chip is essential for BIST applications. Based on the classical implicit method and the integrating circuit reviewed in the Section 2.3, we propose a CMOS built-in RMS-to-DC converter architecture aimed at BIST applications for power supply RMS current monitoring as shown in Fig. 3.1.

![Diagram](image)

Fig. 3.1 Proposed built-in RMS-to-DC converter
The functional block diagram in Fig. 3.1 illustrates the basis of the proposed *built-in RMS-to-DC converter*. This circuit contains four blocks: the *current squarer/divider; the integrating ADC; the accumulating divider; and the current-mode DAC*.

The current squarer/divider is an analog translinear signal processing circuit. The detailed current-mode translinear background knowledge and the design of the circuit are discussed in the later Section 3.2. The integrating ADC used here is the one reviewed in Section 2.3. The accumulating divider and the current-mode DAC will be described in Section 3.3.

The circuit operation is based on the classical implicit method for RMS-to-DC calculation. From a structural aspect, the major difference between the proposed converter and known analog RMS-to-DC converters based on the classical implicit method is the implementation of the averaging low-pass filter. As an on-chip averaging function circuitry, the circuit should not require a large capacitor. To avoid the large capacitor, the *timed window integration* technique is used. Reducing the integration time \( T \) results in a proportional reduction in the size of the integrating capacitor. Integration over a specific time can be expressed as the summation of a series of integrations over short-time window intervals. As shown in Section 2.3, we have the averaging equation (3.1):

\[
\bar{I} = \frac{1}{T} \int_0^T I_{in} dt = \frac{1}{T_s} \left\{ \frac{1}{M} \sum_{i=0}^{M-1} \int_{T_i}^{(i+1)T_i} I_{in} dt \right\}
\]

where \( T=MT_s \), \( T_s \) is the short integration time interval, and \( I \) is the input current.

Instead of applying a conventional RC filter, we perform averaging by using digital circuitry. The integrating ADC integrates its input signal and outputs a digital number proportional to the integration result in each of the short time integration intervals \( T_s \). In
turn, the digital number is fed to the accumulating divider, which divides the integration number by a number $M$ associated with the integration time period, $T=MT_s$. By using the circuit and technique, titled double-phase current integrator half-wave current integrator (HCI), reviewed in the Section 2.3 as the integrating ADC, the on-chip capacitance can be reduced significantly and high conversion accuracy can be achieved.

### 3.1.2 Circuit Structure

A detailed circuit schematic is illustrated in Fig. 3.2.

![Fig. 3.2 The schematic of built-in RMS-to-DC converter](image)

The integrating ADC, half-wave current integrator (HCI), functions according to the following:

$$K_c \int_0^t Idt = K_c \sum_{i=0}^{M-1} \int_{iT_s}^{(i+1)T_s} Idt$$

$$= V_o \sum_{i=0}^{N-1} N_i + V_{RM}^R$$  \hspace{1cm} (3.2)
where \( K_c \) is a constant, \( \sum_{i=0}^{N-1} N_i \) is the ADC output, \( V_{R}^{R_{M-1}} \) is the (M-1)-th integration quantization error, and \( V_\Delta \) is ADC quantization step, and \( V_{R}^{R_{M-1}} < V_\Delta \). The RMS-to-DC converter's functionality is summarized as follows. The output of the accumulating divider is the averaged \( \frac{I_{in}^2}{I_{out}} \). Substituting this average into (3.2), we have

\[
K_c \cdot \left( \frac{I_{in}^2}{I_{out}} \right) = K_c \cdot \frac{1}{T} \int \frac{I_{in}^2}{I_{out}} dt
\]

\[
= \frac{K_c}{M \cdot T_s} \left( \sum_{i=0}^{M-1} \frac{1}{T_s} dt \right)
\]

\[
= \frac{1}{M \cdot T_s} \left( V_\Delta \sum_{i=0}^{N-1} N_i + V_{R}^{R_{M-1}} \right)
\]

(3.3)

Then, we have

\[
N = \frac{1}{M} \sum_{i=0}^{N-1} N_i = \frac{K_c \cdot T_s}{V_\Delta} \left( \frac{I_{in}^2}{I_{out}} \right) - \frac{1}{M \cdot V_\Delta} V_{R}^{R_{M-1}}
\]

(3.4)

In Eqn. (3.4), the term \( \frac{1}{M \cdot V_\Delta} V_{R}^{R_{M-1}} = 0 \) as the \( \frac{V_{R}^{R_{M-1}}}{V_\Delta} < 1 \) and \( M \gg 1 \) (\( M=1000 \) in this design). Hence, we can drop this term reasonably. So, we have

\[
N = \frac{1}{M} \sum_{i=0}^{N-1} N_i = \frac{K_c \cdot T_s}{V_\Delta} \left( \frac{I_{in}^2}{I_{out}} \right)
\]

(3.5)

The transfer function of the current-mode DAC can be expressed as

\[
I_{out} = K_D \cdot N
\]

(3.6)

where \( K_D \) is a constant of the DAC and \( K_D = I_{LSB} \).
Substituting Eqn. (3.6) into Eqn. (3.5), we get the final expression of the output when the RMS-to-DC converter reaches its steady state.

\[
N = \sqrt[\frac{K_C \cdot T_s}{K_D \cdot V_\Delta}} \cdot \sqrt{I_{in}^2}
\]  

(3.7)

Notice that \(\sqrt{I_{in}^2}\) is the RMS value of input current \(I_{in}\). In the steady state, we have

\[
N = \sqrt[\frac{K_C \cdot T_s}{K_D \cdot V_\Delta}} \cdot I_{rms}
\]  

(3.8)

The above solution is an idealized analysis. In practice, the analog and mixed-signal circuit design raises limitations, discussed in later sections. For BIST applications, both (3.6) and (3.8) provide analog and digital signature information, respectively. In an actual BIST application, the digital signature can be evaluated by simple digital circuitry such as a signature analyzer. For simulation purposes, the analog signature is more easily observed and evaluated than the digital signature to verify the functionality of the converter. In this thesis, the analog signature is monitored to simplify the verification of the mixed-signal simulation.

### 3.1.3 Notation and Definitions

Before we describe the operation of the proposed rms-to-dc circuit in detail, the notations and definitions used are listed as follows:

- **CLK**: testing clock signal;
- **Φ**: Signal with period \(T_s\) that controls the integration time;
- **\(T\)**: the total integration time window duration, i.e., \(T=MT_s\);
- **\(T_s\)**: Short integration time sub-window;
- **\(M\)**: number of integration sub-windows;
• \( N_i \): \( i \)-th integer number of the RMS-to-DC converter output;

• \( N \): final integer number of the converter proportional to the RMS value of \( I_m \) over time \( T \), i.e., \( N = \frac{1}{M} \sum_{i=0}^{N-1} N_i \);

• \( V_{i}^{q} \): \( i \)-th integrating ADC quantization noise;

• \( V^{q} \): total quantization noise over time \( T \);

• \( rst \): reset signal;

• \( EN \): circuit enable signal;

• \( Init \): initial state control signal.

### 3.1.4 Circuit Implementation and Operation

The circuit operating clock-timing diagram is illustrated in Fig. 3.3. The control block generates the control signals, i.e., \( rst \), \( EN \), \( Init \), \( \Phi \) and \( \overline{\Phi} \). The signal \( \Phi \) is divided by 10 from the testing clock signal \( CLK \) with 50% duty cycle.

With the reset signal \( rst \), the circuit is reset to its initial state, zeroing the counters of both the integrating ADC and accumulating divider, and discharging the capacitors of the...
integrating ADCs. The signal EN enables the circuit. A critical aspect of this circuit is the initial status of the divider input of the current squarer/divider input. We may set this starting value by presetting the initial value of the current-mode DAC. Setting this value to its maximum or minimum may cause a long settling time since we do not have a detailed information about the range of input signal \( I_{in} \). An additional current mirror and switch controlled by signal Init are added to feed the input current \( I_{in} \) to the analog divider terminal. The use of this adaptive scheme reduces the total converter settling time of the converter. During the signal \( \Phi \) low phase, the HCI (A) integrates \( I_{in}^2/I_{out} \) and a number proportional to the current integration is added to the counter. Similarly, during the low phase of \( \Phi \), the HCI (B) operates and a number is added to the counter. Since the two integrators, HCI (A) and HCI (B), perform integration during complementary time windows, the state of the counter at the end of the operation will be proportional to the integral of \( I_{in}^2/I_{out} \) over the testing time \( T \). Every two short time integrals, the counter controlled by \( \Phi \) in the accumulating divider increases by a count according to the integration value. Then, to compute the average, this number is divided by the output of the integrating ADC. The current-mode DAC keeps transforming this average number to the analog current as the divider input of the analog block. After a relatively long time window, this feedback current will be stable and corresponded to the RMS current of the input signal. At steady status, the digital number of the DAC input is a digital signature of the RMS value, meanwhile, the output of the DAC is an analog signature. The following parameters were chosen in our design of the RMS-to-DC converter:

- \( T=1 \text{ ms}, T_s=1 \mu\text{s}, M=1000; \)
- \( f_{CLK}=20 \text{ MHz}; \)
• Counter size: 18-bits;
• Divider size: 18-bits;
• DAC: 8-bits binary weighted.

As shown in the Eqn. (3.8), the calculated RMS value is not an exact RMS value because of the existence of the constant coefficient, resulting in a value linearly proportional to the true RMS value. Moreover, Eqn. (3.8) shows an ideal case. In the actual implementation, offsets will exist in the measurement results as well. We can calibrate the circuit for the actual testing. A two-point calibration can be applied to the RMS-to-DC converter.

In summary, this circuit has several features which make it suitable for a BIST application. These include simplicity, small silicon area, good accuracy, and digital signature. The current squarer/divider is a relatively simple analog circuit. The integrating ADC is based on the single-slope architecture, which is a well-known class of high resolution and inexpensive ADC. The accumulating divider is based on a digital counter and an iterative shift/subtract divider. The current-mode DAC is a binary-weighted current-steering DAC. The next section discusses the block design of the RMS-to-DC converter in detail.

3.2 The Current Squarer/Divider

In the proposed built-in RMS-to-DC converter, a current squarer/divider circuit is required. This section describes a novel current squarer/divider for this application, beginning with a review of the MOS translinear circuit principle.

Most MOS analog signal processing circuits can be designed based on the translinear principle. Several analog current squarer/divider circuits exist [43][44][45]. These
circuits are designed with either switched-current or class A translinear techniques. The
switched-current technique usually requires relatively complex control signals and is a
time consuming technique. In this section, the MOS translinear circuit principle is
reviewed and a novel current-mode squarer/divider circuit is presented. This circuit has
good precision and is insensitive to temperature and process variations.

3.2.1 MOS Translinear Principle

The concept of translinear, transconductance linear with collector current, was
originally based on the property of bipolar transistors. When applied to circuits that are
connected in loops of junction voltages with the inputs and outputs in the form of
currents, this property allows the implementation of exact temperature and process
insensitive analog signal processing functions. In 1991, this translinear principle was
extended to MOS technology by Seevinck and Wiegerink [46]. Detailed analysis and
practically synthesized example designs were described in a later book [47] published in
1993 by Wiegerink. To describe the MOS translinear principle, we start from the basic
current through a MOS transistor by considering a MOS transistor operating in saturation
and characterized by a first order square-low models shown in Eqn. (3.9).

\[ I_D = \frac{k}{2} (V_{gs} - V_{th})^2 \] (3.9)

where \( I_D \) is the drain current of a MOS transistor, \( V_{gs} \) is the gate-source voltage, and \( V_{th} \) is
the threshold voltage.

The transconductance of the MOS transistor can be expressed as

\[ g_m = \frac{\partial I_D}{\partial V_{gs}} \] (3.10)

where \( g_m \) is the transconductance.
Solving eqn. (3.9) and (3.10) yields

\[ g_m = k \cdot (V_{gs} - V_{th}) \]  \hspace{1cm} (3.11)

where

\[ k = \mu C_{ox} \frac{W}{L} \]  \hspace{1cm} (3.12)

Equ (3.11) states that the transconductance of a MOS transistor is linearly proportional to the excess gate-source drive voltage \( V_{gs} - V_{th} \).

The characteristics of a MOS translinear circuit can be summarized as follows [48]:

- **Translinear**: The primary function of translinear circuits arises from the exploitation of the proportionality of transconductance to the excess gate-source voltage of a MOS transistor;

- **Current-mode**: The translinear circuits are often arranged in a loop of drive voltages and inputs and outputs in the form of currents;

Unlike bipolar transistors with their conformance over wide ranges of current, the square-law behavior of MOS transistor is limited to a much smaller current range. It is bounded at the low end by weak inversion operation and at the high end by mobility reduction.

As stated in the second feature of the MOS translinear circuit, the principle is based on a MOS transistor loop, in which the gate-source is connected in series between transistors and has equal numbers of transistors arranged clockwise and counterclockwise as shown in Fig. 3.4. From Kerchhoff's voltage law, it follows that

\[ \sum_{cw} V_{gs} = \sum_{ccw} V_{gs} \]  \hspace{1cm} (3.13)

where the subscript \( cw \) and \( ccw \) indicate the transistors connected clockwise and counterclockwise in the loop, respectively. In other words, (3.13) indicates the
characteristic of the MOS translinear loop, the gate-source voltage drops are equal for the clockwise and counterclockwise transistors.

![Diagram of MOS translinear loop]

**Fig. 3.4** The concept of MOS translinear loop [46]

From (3.9) and (3.11) we obtain the gate-source voltage $V_{gs}$

$$V_{gs} = V_{th} + \frac{I_D}{k}$$  \hspace{1cm} (3.14)

Substituting (3.14) into (3.13) results in

$$\sum_{cw} \left( V_{sh} + \frac{I_D}{k} \right) = \sum_{ccw} \left( V_{sh} + \frac{I_D}{k} \right)$$  \hspace{1cm} (3.15)

If we assume well-matched threshold voltages and neglecting the body effect, the threshold voltages can be dropped since equal numbers of transistors are connected in the clockwise and counterclockwise. This yields:

$$\sum_{cw} \sqrt[2]{\frac{I_D}{W/L}} = \sum_{ccw} \sqrt[2]{\frac{I_D}{W/L}}$$  \hspace{1cm} (3.16)

Obviously, both parameters in (3.16), i.e., $I_D$ and $W/L$, which are the only parameters that the designer can control in the analog design procedure, are temperature and process independent. Therefore, this design principle is insensitive to temperature and processing because the absence of the $\mu C_{ox}$ [47]. Both the electron mobility $\mu$ and the gate-oxide...
capacitance $C_{ox}$ are temperature or process sensitive parameters.

Generally, the simplest and most often used MOS translinear loop is a loop consisting of four transistors. A four NMOS transistors loop is shown in Fig. 3.5(a). In this case, we have

$$V_{g1} + V_{g2} = V_{g3} + V_{g4} \quad (3.17)$$

Applying (3.14) yields:

$$V_{a1} + \sqrt{\frac{I_{D1}}{(W/L)_M}} + V_{a2} + \sqrt{\frac{I_{D2}}{(W/L)_M}} = V_{a3} + \sqrt{\frac{I_{D3}}{(W/L)_M}} + V_{a4} + \sqrt{\frac{I_{D4}}{(W/L)_M}} \quad (3.18)$$

Dropping the threshold voltages $V_{th}$, Eqn. (3.18) becomes

$$\sqrt{\frac{I_{D1}}{(W/L)_M}} + \sqrt{\frac{I_{D2}}{(W/L)_M}} = \sqrt{\frac{I_{D3}}{(W/L)_M}} + \sqrt{\frac{I_{D4}}{(W/L)_M}} \quad (3.19)$$

Assuming that all four transistors have the same size in design yields:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \quad (3.20)$$

![Fig. 3.5 MOS translinear circuits of four transistors](image)

The structure in Fig. 3.5(a) is called a class A or stacked topology [47]. The problem with this topology is the existence of the body-effect with transistors M2 and M3. Thus, the threshold voltage $V_{th}$ cannot be dropped from (3.18). Including the body-effect, (3.20) can be rewritten in form of body-effect as in (3.21).
\[ \sqrt{I_{D1}} + (k'V_{sb2} + \sqrt{I_{D2}}) = (k'V_{sb3} + \sqrt{I_{D3}}) + \sqrt{I_{D4}} \] 

(3.21)

where \( V_{sb} \) is the source-substrate voltage with the process parameter \( k' \), and usually \( V_{sb2} \neq V_{sb3} \). It is possible to eliminate the body-effect by using transistors M2 and M3 with individual wells connected to their sources. However, the large well-to-substrate capacitance will slow down the circuit performance in this way. The influence of the body effect can be significantly reduced if a \textit{class B} or \textit{up-down topology} is used as shown in Fig. 3.5(b). In this structure, the relation of the gate-source voltage \( V_{gs} \) in (3.17) holds. Furthermore, since the two pairs of transistors M1, M4 and M2, M3 have the sources connected together, the body-effect is the same for each pair of transistors, i.e.,

\[ V_{gs1} = V_{gs4} \quad \text{and} \quad V_{gs2} = V_{gs3} \] 

(3.22)

In other words, the body-effect in a class B topology can be minimized without the inclusion of individual wells.

In summary, a class A topology of translinear circuit often results in a compact circuit and can be implemented with a limited bandwidth because of the inclusion of individual wells. A class B topology generally is probably a good choice if the high frequency performance is required since the absence of the large parasitic associated to the individual transistor wells [47]. Compromising the speed and complexity can guide the selection of topology. In the next section, we describe the class A and class B translinear current squarer/divider circuits.

\textbf{3.2.2 Proposed Current Squarer/Divider}

\textbf{3.2.2.1 Class A Circuit Synthesis}

The current squarer/divider implements the following function:
where \( x, y, z \) are all current signals. \( x \) and \( y \) are input signals. \( z \) is an output signal. For mathematic simplicity and consistent to reference, we describe the circuit design procedure with the common mathematic notation \( x, y, z \) instead of conventional electrical notation \( I \) for current.

(3.23) is the target function that we want to synthesize a circuit by the use of the translinear principle (3.16) to (3.20). The key to the circuit synthesizing procedure is the following relationship:

\[
a^2 + 2ab + b^2 = (a + b)^2
\]  

(3.24)

To synthesize (3.23), it is reformulated into:

\[
x^2 = yz
\]

Taking square roots to both sides yields:

\[
x = \sqrt{yz}
\]

Multiplying by 2 and adding \((y+z)\) to both sides yields:

\[
2x + y + z = y + z + 2\sqrt{yz}
\]

Applying (3.24) to the above results in:

\[
2x + y + z = (\sqrt{y} + \sqrt{z})^2
\]

Finally, taking square roots of both sides yields:

\[
\sqrt{2x + y + z} = \sqrt{y} + \sqrt{z}
\]  

(3.25)

Rearranging (3.25) to a much clearer form gives:

\[
2\sqrt{\frac{2x + y + z}{4}} = \sqrt{y} + \sqrt{z}
\]  

(3.26)
Comparing (3.26) with (3.20), we can define the current through the drain of the transistors as follows:

\[
I_{D1} = I_{D2} = \frac{x}{2} + \frac{1}{4}(y + z) \tag{3.27}
\]

\[
I_{D3} = y \tag{3.28}
\]

\[
I_{D4} = z \tag{3.29}
\]

We can then rewrite the functionality of (3.23) in the terms of the MOS transistor drain currents, i.e., as

\[
I_{D4} = \frac{x^2}{I_{D3}} \tag{3.30}
\]

The schematic of the current squarer/divider circuit based on class A topology is illustrated in Fig. 3.6.

All NMOS transistors M1 to M4 have the same size, i.e., \((W/L)_{M1} = (W/L)_{M2} = (W/L)_{M3} = (W/L)_{M4}\). The input current \(y\) is forced into the source of the transistor M3 by the current source. The output current \(z\) is the current through M4. With the current mirror...
formed by M5 and M6, the current \((y+z)/4\) or \((I_{D3}+I_{D4})/4\) is fed into M1 and M2. Together with the input current \(x/2\), the current through transistor M1 and M2 are forced to \(x/2+(y+z)/4\) that is shown in (3.27).

In summary, as a simple class A translinear circuit, this circuit suffers two drawbacks:

- To eliminate the body-effect, the transistors M2 and M3 should be implemented in their individual wells. This characteristic slows down the circuit due to the large well parasitic;
- In an actual implementation, it is difficult to copy the current \(z\) out of transistor M4 accurately. Although a single transistor M7 can do this as shown in Fig. 3.6, the second order effects of the current mirror, i.e., \(v_{ds}\) mismatching, and low output impedance degrade the current mirror accuracy.

3.2.2.2 Class B Circuit Synthesis and Analysis

In the last section, we synthesized the class A current squarer/divider. The elimination of the body-effect, by laying out transistors in individual wells, slows down the circuit performance. If a fast performance is needed, the class B topology is generally a better choice. In this section, we describe a class B circuit with the same functionality. Unlike the design of the class A circuit, in which we have only described the synthesis procedure, we describe the class B circuit in regard to both its synthesis and analysis.

A. Synthesis

In the design of the class A circuit, all input currents, \(x\) and \(y\), are forced into the transistors M1, M2 and M3. Directly forcing the desired currents into the class B circuit loop is often more complicated than in the class A topology. Generally, in the class B topology, the drain currents through two transistors M1 and M2, e.g., \(I_{D1}\) and \(I_{D2}\), are
forced directly. A third drain current has to be forced by adding extra current sources and transistors.

The schematic of the synthesized class B current squarer/divider circuit is illustrated in Fig. 3.7. The W/L ratios of transistors M7 to M10 are 1:1:n1:n1 and the W/L ratio of transistor M5 to M6 is n:1. The input and output currents are presented as \( k_1x \) and \( k_2y \), respectively. The synthesis procedure determines the circuit variables, i.e., \( n, n1, k_1, k_2, \) and \( I \). In this circuit the drain currents \( ID_1 \) and \( ID_2 \), through transistor M1 and M2 are forced directly. The third drain current \( ID_3 \) through transistor M3 is forced by an extra current source generating a current \( k_2y \).

![Fig. 3.7 Class B current squarer/divider](image)

To synthesize the circuit, the equations (3.26) to (3.29) are used. Eqn. (3.27) can be re-expressed in the following form:

\[
I_{D1} = I_{D2} = \frac{x}{2} + \frac{1}{4}(I_{D3} + I_{D4})
\]  

(3.31)
Again, for simplicity, we choose the same aspect ratios for transistors M1 to M4, i.e.,
\((W/L)_{M1} = (W/L)_{M2} = (W/L)_{M3} = (W/L)_{M4}\). With the current mirror formed by M7 to M9 and
the input current source \(x/2\), the drain current in M1 and M2 can be forced as in (3.31).
Choosing \(n_j = 4\), then it is easy to see the forward solution for \(k_1, k_1 = l/2\). From the
synthesis procedure for the class A current squarer/divider discussed in Section 3.2.2.1,
Eqn. (3.23) is synthesized by forcing current \(y\) through the transistor M3. Thus, the next
task is to determine the remaining variables \(l, n\) and \(k_2\) in Fig. 3.7 in order to force the
input current \(y\) into M3.

The drain currents through M5 and M6 can be expressed as

\[ I_{D5} = I + I_{D1} + I_{D4} \]  \hspace{1cm} (3.32)

and

\[ I_{D6} = I_{D2} + I_{D3} - k_2 y \]  \hspace{1cm} (3.33)

The relation of transistor M5 and M6 is

\[ I_{D5} = n \ I_{D6} \]  \hspace{1cm} (3.34)

Substituting (3.32) and (3.33) into (3.34) yields

\[ I + I_{D1} + I_{D4} = nI_{D2} + nI_{D3} + nk_2 y \]  \hspace{1cm} (3.35)

or

\[ I = (n-1)I_{D1} + nI_{D3} - I_{D4} - nk_2 y \]

Again, substituting (3.31) into (3.35) gives

\[ I = (n-1)\left(\frac{x}{2} + \frac{1}{4}I_{D3} + \frac{1}{4}I_{D4}\right) + nI_{D3} - I_{D4} - nk_2 y \]

or
Since (3.36) is a multiple variable equation, its unique solution requires some assumptions. Choosing \( n=5 \), (3.36) becomes

\[
I = (n-1)\frac{x}{2} + \frac{5n-1}{4}I_{D3} + \frac{n-5}{4}I_{D4} - nk_2y
\]

(3.36)

If we choose \( I=2x \) and \( k_2=6/5 \), we can force \( I_{D3}=y \). This indicates if the currents are forced into transistor M1 and M2 directly, then, with an extra current source generating a current \((6/5)y\), the current \( y \) is forced through transistor M3. The schematic of the resulting circuit is shown in Fig. 3.8. By subtracting \( y \) with an extra current mirror, we can derive the output current \( z \).

![Fig. 3.8 Schematic of class B current squarer/divider](image)

**B. Analysis**

To verify the functionality of the circuit design shown in Fig. 3.8, we analyze the circuit starting from the upper current mirror. With the current mirror formed by M7 to M9 and the input current source \( x/2 \), we have the following currents through M1 and M2.

\[
I_{D1} = I_{D2} = \frac{x}{2} + \frac{1}{4} (I_{D3} + I_{D4})
\]

(3.38a)
With the help of the current mirror M5 and M6, the current through M3 can be forced to
equal the second input current $y$. The currents through M5 and M6 are

$$I_{D5} = 2x + I_{D1} + I_{D4}$$  \hspace{1cm} (3.35b)

and

$$I_{D6} = I_{D2} + I_{D3} - \frac{6}{5}y$$  \hspace{1cm} (3.38c)

Solving the equation (3.38b) and (3.38c) yields

$$I_{D3} = y$$  \hspace{1cm} (3.38d)

If we define the output current $z$ as the current through M4, say,

$$I_{D4} = z$$  \hspace{1cm} (3.38e)

Then, substituting (3.38d) and (3.38e) into (3.38a) yields the currents through M1 and
M2 as

$$I_{D1} = I_{D2} = \frac{x}{2} + \frac{1}{4}(y + z)$$  \hspace{1cm} (3.38f)

Now, (3.26) becomes

$$2\sqrt{\frac{x}{2} + \frac{1}{4}(y + z)} = \sqrt{y} + \sqrt{z}$$  \hspace{1cm} (3.38g)

Squaring both sides of (3.38g), we have

$$2x + y + z = y + z + 2\sqrt{yz}$$  \hspace{1cm} (3.38h)

Reforming (3.38h) yields the final solution

$$z = \frac{x^2}{y}$$  \hspace{1cm} (3.38i)

In summary, a class B current squarer/divider is designed as shown in Fig. 3.8.
3.2.2.3 Uniform Scaling Feature

In the practical application of the circuit in Fig. 3.8, two design questions may arise:

- How to design a circuit according to the different input current dynamic range?
- How to supply the currents required in the circuit?

The second question is discussed in the next section. The dynamic range of a current squarer/divider circuit may vary according to different application. For example, the quiescent current of a CMOS digital circuit can rise to 100 ~ 200 µA, whereas the current of an analog circuit may rise to 1 mA. Designers usually focus their efforts on improving the circuit dynamic range to meet the specification in the design procedure. One simple approach is to design a functional core circuit with a small dynamic range and scale down the large input signal down to be within this small range. After processing, the output signal is then transformed back to its actual range. The scaling of signals can be performed by simple current mirrors. Here, we describe a scaling approach for the synthesized current squarer/divider circuit.

With the increase of the input current $x$, the output current $z$ will increase significantly due to the property of squarer/divider circuit. Thus, the transistors conducting large currents must larger to keep them in saturation. This results in larger parasitics and a larger supply voltage requirement as well, which in turn slows down the circuit and reduces the bandwidth. A uniform scaling feature of the circuit can provide design information to designers.

Reformulating the (3.23) to

\[
\frac{z}{2^m} = \left(\frac{x}{2^m}\right)^2 \frac{y}{2^m}
\]

(3.39)
where \( m \) is an integer, we can reduce the currents in individual transistors by factors of \( 2^m \). Based on this approach, the circuit can be re-synthesized as shown in Fig. 3.9. The circuit in Fig. 3.9 provides the information to scale the signals to designed dynamic range while keeping the core function formed by transistors M1 to M10 unchanged in different input dynamic range. It indicates that, in different actual applications, we can reuse the same function core.

Fig. 3.9 Circuit schematic with dynamic range adjustment strategy

The analysis of the circuit in Fig. 3.9 is described in Appendix A. By pre-determining the variable \( m \), versatile circuits can be designed. The circuit in Fig. 3.8 is a first-order case of this design strategy with \( m=0 \). Again, we need extra circuitry to supply the input currents and derive the output current. This can be done with the basic current mirrors by scaling their size. This uniform scaling design strategy, in which \( m \) is the only design parameter in choosing the amounts of currents, is useful for designers to optimize the circuit to meet desired dynamic ranges.
3.2.2.4 Implementation

As discussed in the last section, in practice, extra transistors are required to supply the input currents and derive the output current. A basic current mirror, e.g., two transistors current mirror, can perform this task, however, the accuracy of it is low due to its low output impedance. An alternative instead of a basic current mirror is a high output impedance current mirror, e.g., a cascade current mirror. On the other hand, with the rapid scaling of technology, e.g., from 0.5\(\mu\)m to 0.35\(\mu\)m and the more recent 0.18\(\mu\)m and 0.13 \(\mu\)m, and the power supply voltage as well, the voltage margin to keep the individual transistors in saturation drops rapidly. A low output voltage current mirror is required for low voltage applications. The requirement of low output voltage and high output impedance can be accomplished by using the high output impedance wide-swing current mirrors. Wide-swing current mirrors enable keeping transistors M1 to M4 in saturation. They provide high output impedance with the relatively small voltage drop compared to the conventional cascade current mirrors, especially for the low power supply voltage applications, e.g., 3.3 V or 1.8 V. Since the range of the input signal is unknown, the self-biased wide-swing current mirrors provide better alternatives. They can provide the bias current according to the input signals by the self-biased scheme.

The complete schematic of the current squarer/divider circuit in Fig. 3.8 based on self-biased wide-swing current mirrors is shown in Fig. 3.10. This circuit has been designed in both 0.18 \(\mu\)m and 0.35\(\mu\)m technologies assuming a 3.3 V power supply. Channel widths and lengths for all transistors are given in Table 3.1 and 3.2 for 0.18 \(\mu\)m and 0.35\(\mu\)m technology, respectively.
Fig. 3.10 Schematic of the implemented class B current squarer/divider

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width, Length</th>
<th>Transistor</th>
<th>Width, Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>12 µm, 3 µm</td>
<td>M12, M12', ...M13'</td>
<td>50 µm, 1 µm</td>
</tr>
<tr>
<td>M5, M5', M6, M6'</td>
<td>300 µm, 1 µm</td>
<td>M17, M17', ...M18'</td>
<td>50 µm, 1 µm</td>
</tr>
<tr>
<td>M7, M7', M8, M8'</td>
<td>50 µm, 1 µm</td>
<td>M21, M21', ...M23'</td>
<td>60 µm, 1 µm</td>
</tr>
<tr>
<td>M9, M9', ... M11'</td>
<td>200 µm, 1µm</td>
<td>M25, M25'</td>
<td>60 µm, 1 µm</td>
</tr>
</tbody>
</table>

Table 3.1 Transistor dimensions in Fig. 3.10 for 0.18 µm technology

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width, Length</th>
<th>Transistor</th>
<th>Width, Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>8 µm, 5 µm</td>
<td>M12, M12', ...M13'</td>
<td>30 µm, 1 µm</td>
</tr>
<tr>
<td>M5, M5', M6, M6'</td>
<td>150 µm, 1 µm</td>
<td>M17, M17', ...M18'</td>
<td>30 µm, 1 µm</td>
</tr>
<tr>
<td>M7, M7', M8, M8'</td>
<td>25 µm, 1 µm</td>
<td>M21, M21', ...M23'</td>
<td>30 µm, 1 µm</td>
</tr>
<tr>
<td>M9, M9', ... M11'</td>
<td>100 µm, 1µm</td>
<td>M25, M25'</td>
<td>80 µm, 1 µm</td>
</tr>
</tbody>
</table>

Table 3.2 Transistor dimensions in Fig. 3.10 for 0.35 µm technology

The simulation and silicon measurement results are provided in Chapter 4.
3.2.3 Error Analysis

The discussion and circuit design up to now have been based on the first-order MOS model. However, in reality, there are several second-order effects causing deviations from the ideal square-law behavior. In this section, we discuss some of major second-order effects: channel length modulation, mobility reduction, and transistor mismatch.

3.2.3.1 Channel Length Modulation

Channel length modulation in a MOS transistor causes the drain current to be dependent not only on the gate-source voltage $v_{gs}$ but also on the drain-source voltage $v_{ds}$. In a first-order approximation, this may be modeled as follows [49]:

$$I_D = \frac{k}{2} (v_{gs} - v_{th})^2 \cdot (1 + \lambda (v_{ds} - v_{ds, sat}))$$  \hspace{1cm} (3.40)

where

$$v_{ds, sat} = (v_{gs} - v_{th})$$

and

$$\lambda = \frac{1}{L} \sqrt{\frac{2e_0 e_t}{qN_d}}$$  \hspace{1cm} (3.41)

where $\lambda$ is the channel-length modulation parameter. From (3.41), we can see that parameter $\lambda$ is process dependent and inversely proportional to the channel length $L$.

Considering the effect of the channel-length modulation in our circuit, (3.16) can be reformed as

$$\sum \sqrt{\frac{I_D}{W/L} \cdot \left(1 + \lambda (v_{ds} - v_{ds, sat})\right)} = \sum \sqrt{\frac{I_D}{W/L} \cdot \left(1 + \lambda (v_{ds} - v_{ds, sat})\right)}$$  \hspace{1cm} (3.42)

To eliminate the channel-length modulation effect, two methods can be used:

- Forcing the same drain-source voltage $v_{ds}$ for transistors in the translinear loop;
• Using long channel length.

If we can keep the drain-source voltage $v_{ds}$ the same for transistors M1 to M4 in our circuit, the channel-length modulation effect will be the same for both sides of (3.42) allowing to drop the term $I + \lambda (V_{ds} - V_{ds_{sat}})$. The technique introduced in the design of the built-in current sensor in Chapter 2 could be used to force the drain-source voltage of the loop transistors by including two operational amplifiers as shown in Fig. 2.2. However, this would require significant extra circuitry. Another way to eliminate the channel-length modulation effect is to use long channel length transistors since parameter $\lambda$ decreases with increasing $L$. Although, theoretically, the longer the channel length, the less the channel-length modulation effect, long channel transistors result in large parasitics which slows the circuit. In our circuit, by experiments, we chose $L=5\mu m$ and $L=3\mu m$ for 0.18 $\mu m$ and 0.35 $\mu m$, respectively.

3.2.3.2 Mobility Reduction

The mobility reduction effect as the drain current can be modeled according to [50]:

$$I_D = \frac{k}{2(1 + \theta (V_{gs} - V_{th})) (V_{gs} - V_{th})^2} \quad (3.43)$$

where the mobility reduction parameter

$$\theta = \frac{1}{d_{ox} \cdot E_{cr}} \quad (3.44)$$

where $d_{ox}$ is the oxide thickness and $E_{cr}$ is the critical field.

In (3.44), the mobility reduction parameter $\theta$ depends on a critical electric field. The strong electric field across the gate oxide causes the charge carriers in the channel to be pulled towards the Si-SiO$_2$ interface and the carrier mobility decreases. Since there is no
design parameter associated with mobility reduction that a designer can control to eliminate the effect, as it is the case for channel-length modulation, the mobility reduction effect cannot be removed by design. Mobility reduction is major cause of distortion among the second-order effects.

3.2.3.3 Transistor Mismatch

Mismatches of MOS transistors, in general, consist of two terms [51]:

- Mismatches in threshold voltages;
- Mismatches in geometry ratios W/L.

If these two second-order effects appear, (3.18) cannot be simplified by dropping the threshold and W/L terms to become (3.20). In general, the transistor mismatches can be reduced by careful layout [52]. For example,

- Placing transistors close to each other with the same orientation;
- Connecting unit transistors in parallel for large W/L ratios.

In our circuit, all transistors were separated into several unit transistors and laid out in parallel to reduce mismatch effects.

In summary, we mentioned the major second-order effects that influence circuit performance and thereby accuracy. In our circuit, the channel-length modulation and transistor mismatch effects have been reduced by the design and layout procedures. The mobility reduction effect remains the major distortion source of circuit performance.

3.3 Integrating ADC and Accumulating Divider

As mentioned in Section 3.1, the output current of the current squarer/divider has to be averaged. In a major difference from a pure analog RMS-to-DC converter circuit, we propose to implement the averaging function by digital circuitry instead of using the
conventional RC filter. The averaging function includes two blocks, as shown in Fig. 3.2, the integrating ADC and the accumulating divider. These achieve the functionality of (2.3).

The role of the integrating ADC is to integrate the current of current squarer/divider. The integrating ADC utilized here is the one discussed as previous work in section 2.3, which is based on the single-slope integrating ADC.

The functionality of the accumulating divider is to record the integration time. It divides the integrated number by the recorded integration time to calculate the average. The accumulating divider is based on an iterative shift/subtract divider and an 18-bit counter. Although the number of bits for the counters in both the integrating ADC and accumulating divider can vary according to the design and duration of testing time, we reused the designed block and save designed time to make them uniformly 18-bits. The counter records the integration time by counting the number of cycles of the control signal $\Phi$ in Fig. 3.3. The recorded number $M$ of the counter is proportional to the integrating time period as shown in Eqn. (2.3). Both the integrating ADC and the accumulating divider together achieve an averaging function over a certain time window. The accumulating divider was designed in Verilog-HDL and synthesized by Synopsys digital synthesizer in a standard 0.35 $\mu$m CMOS technology. The Verilog code is appended in Appendix C.
3.4 Current-mode DAC

As discussed in Section 3.1, the implementation method for the proposed built-in RMS-to-DC converter requires a feedback current. Since the current squarer/divider is an analog block with inputs and outputs of analog signals, a current-mode DAC is required to convert the averaged digital number back to an analog current. This is the role of the fourth block of the RMS-to-DC converter circuit. There are many methods to implement a current-mode DAC [53][54][55]. Here, we apply the 8-bit binary-weighted current-steering DAC in Fig. 3.11 to maintain circuit simplicity. The 1-LSB current of the DAC was set to 1μA. There are two reasons for this selection of LSB current level.

- Current range. The 1-LSB=1μA for an 8-bit DAC implies that the full output current range of the DAC can reach 255 μA. This current range is suitable for the proposed RMS-to-DC converter;
- DAC accuracy. Theoretically, the smaller the 1-LSB current, the better the circuit sensitivity of a current-mode DAC. However it is difficult to design an accurate current source less than 1 μA in a mixed-signal design.

![Fig. 3.11 Structure of 8-bit binary-weighted current-steering DAC](image-url)
In Fig. 3.11, the current sources can be implemented by basic current mirrors. To increase the output impedance of the current source which then improves the matching of current sources, a cascade-connected current mirror shown in Fig. 3.12 can be used.

![Cascade Current Source Diagram](image)

**Fig. 3.12 Configuration of cascade current source**

In Fig. 3.12, the transistors M1 and M2 form the cascade current source. This class of current sources has a gain over 100 and a small channel length modulation factor. The mismatch in drain-source voltage $v_{ds}$ does not introduce appreciable error in the current. The clock feedthrough associated with the digital bit switch is compensated by the addition of the drain-source connected half-sized dummy transistor M5 in the output current path.

The complete schematic of the 8-bit binary-weighted current-steering DAC is shown in Fig. 3.13.
Generally, a drawback of this class of circuit is the switching glitches, which occur when several bits of the binary-code are in transition at the same time. However, simulation results demonstrated that switching glitches are not the critical factor to cause failure, e.g. missing code, in our relatively low 10 MHz clock frequency application. The critical factors in our case are the linearity and process variations. Because the matching of the current sources influences the linearity of the DAC, careful layout must be performed to improve the matching of the current sources. The simulated DNL (differential nonlinearity) and INL (integral nonlinearity) of this DAC shown in Fig. 3.14 (a) and (b) respectively, are both within ± 0.5 LSB. Fig. 3.14 also demonstrates that nonlinearity error increases when the more bits of DAC switch.
Fig. 3.14 Simulated DNL and INL of DAC
This accuracy is obtained by the following two procedures to derive the binary-weighted currents out of an approximately square matrix of 255 equally sized MOS current sources [56].

- **Unit current sources.** Each binary-weighted current is supplied by arranging the appropriate amount of N unit current sources in parallel. In our circuit, the unit current source is a source of 1 μA. All other current sources are formed by putting the appropriate number of 1 μA current sources in parallel;

- **Physical matching.** The 255 unit current sources have to be matched physically.

The optimal distribution of the unit current sources is illustrated in Table 3.3.

<table>
<thead>
<tr>
<th>7 6 7 5 7 6 7 4 7 6 7 5 7 6 7 *</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 7 6 7 5 7 6 6 7 6 7 5 7 6 7</td>
</tr>
<tr>
<td>7 2 7 6 7 5 7 6 7 4 7 6 7 5 6 7</td>
</tr>
<tr>
<td>6 7 3 7 6 7 5 7 6 7 4 7 6 7 5 7</td>
</tr>
<tr>
<td>7 6 7 1 7 6 7 5 7 6 7 4 7 6 7 5</td>
</tr>
<tr>
<td>5 7 6 7 3 7 6 7 5 7 6 7 4 7 6 7</td>
</tr>
<tr>
<td>7 5 7 6 7 2 7 6 7 5 7 6 7 4 7 6</td>
</tr>
<tr>
<td>6 7 5 7 6 7 3 7 6 7 5 7 6 7 4 7</td>
</tr>
<tr>
<td>7 6 7 5 7 6 7 0 7 6 7 5 7 6 7 4</td>
</tr>
<tr>
<td>4 7 6 7 5 7 6 7 3 7 6 7 5 7 6 7</td>
</tr>
<tr>
<td>7 4 7 6 7 5 7 6 7 2 7 6 7 5 7 6</td>
</tr>
<tr>
<td>6 7 4 7 6 7 5 7 6 7 3 7 6 7 5 7</td>
</tr>
<tr>
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</tr>
<tr>
<td>5 7 6 7 4 7 6 7 3 7 6 7 3 7 6 7</td>
</tr>
<tr>
<td>7 5 7 6 7 4 7 6 7 5 7 6 7 2 7 6</td>
</tr>
<tr>
<td>6 7 5 7 6 7 4 7 6 7 5 7 6 7 3 7</td>
</tr>
</tbody>
</table>

Table 3.3 Distribution of 8-bit binary-weighted DAC current sources

This distribution architecture cancels the effects of process gradients across the matrix.

The entries in Table 3.3 indicate the numbers of the DAC bit, to which the unit current source belongs. The symbol * implies a dummy current source. Because the layout of current sources is a 16×16 array and actually only 255 current sources need to be matched, one extra dummy current source is added in the array.
Other special layout techniques used were:

- **Close layout.** All current sources are laid out as close as possible to each other. This improves matching by reducing the ohmic drops between the current sources;

- **Separate digital and analog layouts.** To reduce noise coupling and improve matching of current sources, the analog current sources and digital switches were laid out separately. We also separated power supplies for analog and digital blocks and used guard rings (p+ - substrate) to prevent noise coupling via the substrate.

The sizes of the transistors are reported in Table 3.4. The layout of Fig. 3.13 is illustrated in Fig. 3.15.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width, Length</th>
<th>Transistor</th>
<th>Width, Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0, M0'</td>
<td>256 μm, 1 μm</td>
<td>M9, M10</td>
<td>16 μm, 0.35 μm</td>
</tr>
<tr>
<td>M1, M1'</td>
<td>128 μm, 1 μm</td>
<td>M9'</td>
<td>8 μm, 0.35 μm</td>
</tr>
<tr>
<td>M2, M2'</td>
<td>64 μm, 1 μm</td>
<td>M11, M12</td>
<td>8 μm, 0.35 μm</td>
</tr>
<tr>
<td>M3, M3'</td>
<td>32 μm, 1 μm</td>
<td>M11'</td>
<td>4 μm, 0.35 μm</td>
</tr>
<tr>
<td>M4, M4'</td>
<td>16 μm, 1 μm</td>
<td>M13, M14</td>
<td>4 μm, 0.35 μm</td>
</tr>
<tr>
<td>M5, M5'</td>
<td>8 μm, 1 μm</td>
<td>M13'</td>
<td>2 μm, 0.35 μm</td>
</tr>
<tr>
<td>M6, M6'</td>
<td>4 μm, 1 μm</td>
<td>M15, M16, ... M24</td>
<td>1 μm, 0.35 μm</td>
</tr>
<tr>
<td>M7, M7'</td>
<td>2 μm, 1 μm</td>
<td>M15', ... M23'</td>
<td>0.5μm, 0.35 μm</td>
</tr>
<tr>
<td>M8, M8'</td>
<td>1 μm, 1 μm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3.4 Transistors dimension in Fig. 3.13
Fig. 3.15 Layout of 8-bit current-steering DAC
In Fig. 3.15, the left side is the physical matched current sources array according to the distribution of Table 3.3. The bottom structure of the right side is the switching transistors laid out of other analog parts and separated by a guide ring.

In summary, an 8-bit current-steering DAC was designed and implemented in a standard CMOS 0.35μm technology. Simulations show an acceptable error (within ± 0.5 LSB) for both DNL and INL. Special layout techniques have been adopted to improve the accuracy of the DAC.

3.5 Conclusion

In this chapter, we proposed a built-in RMS-to-DC converter for a BIST application. The architecture of the converter is based on the classical implicit method. The major difference between the proposed structure and the classical implicit structure lies in the implementation of the low-pass filter. Instead of the conventional RC low-pass filter, we implement the filter with a switched-capacitor integrator developed earlier work.

The current squarer/divider circuit required in the converter is a translinear analog circuit. The translinear principle was reviewed and a novel current squarer/divider was described. The synthesis procedure for the class A circuit was presented. Both synthesis and analysis procedures for class B circuits were described. The class B circuit was showed the posses of the uniform scalable. The major second-order effects: channel-length modulation, mobility reduction, and transistor mismatch were discussed. Long channel transistors were chosen to reduce the channel-length modulation effect. Careful layout and special layout techniques were applied to reduce the transistor mismatch effect.

An 8-bit binary-weighted current-steering DAC was designed. The mismatch of current sources influences the linearity of the DAC. Special layout techniques were also adopted
to improve the matching of current sources. The simulation results of DNL and INL are both within ±0.5 LSB.
Chapter Four

Simulation and Measurement Results

To verify the functionality of the proposed built-in RMS-to-DC converter, the current squarer/divider was implemented in a standard 0.18 μm and the rest of the converter was implemented in a standard 0.35 μm technology. There are three reasons for the separate fabrication. They are:

- Since the current squarer/divider was a purely analog circuit, to avoid the influence due to inclusion of other mixed-signal and digital parts, a separate fabrication was chosen. Also, the characteristics of the circuit for a new technology was interested, therefore, a standard 0.18 μm technology was chosen;
- Reuse the previous integrating ADC core that was implemented in a 0.35 μm technology;
- To meet the TSMC fabrication schedule.

The Cadence Verilog-XL mixed-signal simulator was used to simulate the converter. Before presenting simulation results of the RMS-to-DC converter, we describe the simulation and measurement results of the current squarer/divider.

4.1 Simulation and Measurement Results of a Class B Current Squarer/Divider

The class B current squarer/divider circuit, shown in Fig. 3.10, was implemented in the standard 0.18 μm CMOS technology. The chip was fabricated by TSMC (Taiwan Semiconductor Manufacture Corporation) through the CMC (Canadian Microelectronics Corporation). The layout of the chip is shown in Fig. 4.1. The standard TSMC 0.18 μm technology supported dual power supply: 3.3 V power supply with thick oxide transistors.
and 1.8 V power supply with thin oxide transistors. In our case, a 3.3 V power supply with thick oxide transistors was used.

![Layout of the fabricated current squarer/divider in 0.18 um CMOS technology](image)

Since the current squarer/divider circuit is a purely analog block, the complete circuit was laid out manually. Careful analog layout techniques were used to reduce the first-order and second-order effects. Besides the layout techniques mentioned in Section 3.2.3, i.e., transistors matching and long channel-lengths, some other layout techniques were used to reduce the environment noise and distortion between simulation and measurement.

The following layout techniques were used:

- **Unit transistor.** Large transistors were separated into unit transistors placed in parallel. Two reasons to do so. 1) Improving the matching between transistors as mentioned in Section 3.2.3; 2) Reducing the distortion between simulation and
measurement due to the different transistor models used by simulator according to the different aspect ratios.

- **Low resistance path.** Relatively wider metal for current interconnect path was adopted to reduce the resistance causing in voltage drops along the current path and further performance distortion. Special care was taken at the current input and output pads to minimize the ohmic voltage drops by modifying the traditional analog pads;

- **Guard ring.** The p+ - substrate guard ring was placed to surround the analog block to reduce the noise coupling from other analog or digital blocks.

The experimental setup for measurement of current squarer/divider is shown in Fig. 4.2.

Fig. 4.2 Experimental setup for measurements of the current squarer/divider circuit

The bipolar transistors Q1 and Q2 (MPS 3836) form the input current sources to the terminal x and y of the current squarer/divider, respectively. The function generator provides the sinusoidal signal. The DC voltage source provides the constant voltage for generating constant current through Q2. Measuring the voltages across the resistor R3 and R4 verifies the input signals. The output response is measured across resistor R_L. The
relationship between the output voltage $V_L$ and the voltages $V_3$ and $V_4$ across the resistors $R_3$ and $R_4$ respectively is:

$$V_L = \frac{V_3^2}{V_4} \left( \frac{R_4 \cdot R_L}{R_3^2} \right)$$  \hspace{1cm} (4.1)

Ideally, we can choose the same resistance value for $R_3$, $R_4$, and $R_L$, e.g., $R_3=R_4=R_L=10 \text{ k}\Omega$. From (4.1), we can see that any variation of resistance results in measurement distortion. To reduce the measurement error, 1% tolerance resistors were used and the resistance value of each resistor was measured accurately to compensate for the final measurement result.

Since the output terminal $V_L$ is a high impedance port, a voltage follower OPAMP (operational amplifier) with high impedance input and wide bandwidth is included to match the impedance between the circuit under test and the oscilloscope probe.

The simulation is performed in Cadence Analog Artist with SpectreS simulator. Both simulation and silicon measurement results are shown in Fig. 4.3. Here, the input signal $x$ is sinusoidal signal, $x=50[1+ \sin (2\pi f t)]$ $\mu A$, $f=1$ $\text{KHz}$, $y$ is a constant current, $y=61$ $\mu A$. Although the input signal $y$ can also be a sinusoidal signal, we chose a constant value for $y$ reflecting the application of this circuit for RMS-to-DC measurement. The input $y$ is the feedback terminal of $I_{\text{out}}$ in Fig. 3.1, which is the constant value $I_{\text{rms}}$ in steady state.
Fig. 4.3 The total nonlinearity of current squarer/divider circuit

The total harmonic distortion or nonlinearity defined as the absolute error divided by the maximum output range swing, is < 1.1%. As discussed in Chapter 3, the distortion is expected to result from the mobility reduction of transistors.

The simulated frequency response, in Fig. 4.4, shows that the 3-dB bandwidth of the class B current squarer/divider is $f = 5 \text{ MHz}$. 
The bandwidth of 5 MHz is a relatively small bandwidth in this class of translinear circuits. Two reasons result in this frequency response limitation in our circuit.

- **Feedback structure.** The current squarer/divider in Fig. 3.8 includes transistor M9, which feeds the current back into M1 and M2 through M7 and M8, respectively. The inner feedback structure limits the circuit bandwidth;

- **Large transistor dimensions.** To reduce the channel-length modulation effect, the large transistor dimension, \(L=3 \, \mu \text{m}\), is chosen for loop transistors M1 to M4 in Fig. 3.10. Also, since the low power supply voltage, e.g. 3.3 V, is assumed in our design, the transistor size of the current mirrors had to be enlarged to ensure the sufficient voltage swing to keep loop transistors M1 to M4 in saturation for the
specified current dynamic range. The large dimension of transistors results in large parasitics and therefore also limiting the bandwidth.

The measured bandwidth was approximately 1 MHz. To investigate the reason for bandwidth limitation, we modeled the measurement environment [57], also shown in Fig. 4.2. Since the current squarer/divider circuit operates in current-mode, the output terminal is a high impedance port, which is sensitive to the capacitive load. By modeling the testing environment and re-simulating the circuit including the modeled parameters, we found that the bandwidth reduction was resulted from the capacitive load $C_L$ due to the packaging and testing board. Since the commercial standard 40-DIP package was chosen as packaging and a relatively simple PCB was designed to test the chip, the total capacitive load from the packaging and the PCB is approximately 30 pF. The simulation results including this capacitive load matched the experimental result. To reduce the influence of capacitive load in measuring the frequency response, an on-chip buffer, high bandwidth buffer can be placed on-chip in the design cycle for testing purpose. In the intended BIST on-chip application of RMS-to-DC converter, this capacitive loading effect would not arise.

To reuse the integrating ADC design blocks from previous work and meet fabrication schedules, we designed the other parts of built-in RMS-to-DC converter, e.g., integrating ADC, accumulating divider and current-mode DAC, in a standard 0.35 μm technology. This required a redesign of current squarer/divider in 0.35 μm technology. We designed the class B current squarer/divider circuit with the same structure as that shown in Fig. 3.10 in 0.35μm technology. In this design, we applied the current dynamic scaling technique discussed in Chapter 3 to decrease the amount of current in the translinear
loop. The transistor sizes can be decreased within the same dynamic range specification. Because of the smaller transistor dimension and larger electron mobility in 0.35 \( \mu \text{m} \) compared to those in 0.18 \( \mu \text{m} \) technology, the bandwidth could be wider. The simulated bandwidth is 10 MHz.

In summary, the class B current squarer/divider was implemented in the standard 0.18 \( \mu \text{m} \) CMOS technology. The silicon measurement results demonstrated that the total nonlinearity of this circuit is less than 1.1% with a 1 KHz sinusoidal input signal. The simulated bandwidth is approximately 5 MHz.

4.2 The Simulation Results of the RMS-to-DC Converter

The RMS-to-DC converter shown in Fig. 3.1 has been implemented in a standard 0.35 \( \mu \text{m} \) CMOS technology expect the current squarer/divider. The power supply is 3.3 V. In order to study the feasibility of the circuit, the circuit was first modeled in the Verilog-A language. The code is presented in Appendix B. The schematic of the RMS-to-DC converter is presented in Appendix C.

The functionality of the RMS-to-DC converter was verified by simulation. The Cadence Verilog-XL mixed-signal simulator was used to perform a mixed-signal simulation in the Cadence Analog Artist environment.

A. Transient Response

The transient response of the converter is shown in Fig. 4.5 for the input sinusoidal signal, \( i=50[1+ \sin(2\pi ft)] \mu \text{A} \) and the input signal frequency \( f=100 \text{ KHz} \). The output signal is the analog current of the current-mode DAC output in Fig. 3.1. This is the analog signature of the built-in RMS-to-DC converter.
In Fig. 4.5, the built-in RMS-to-DC converter reaches its steady state after a period of rippling. Also, the appearance of the large switching glitches in the rippling period disappears, or more specifically, are reduced in the steady state. Since the glitches only happen at the time of current-mode DAC switching and the digital signature is taken in the actual BIST application, the switching glitches will not affect the digital signature. The accuracy of the simulated results is shown in next section.
B. Accuracy

The RMS-to-DC converter, by itself, is a nonlinear system. However, we have studied the linearity of the circuit for a wide range of current since the circuit should present a linear property for different input amplitudes.

A plot of simulated linearity versus a 100 KHz input sinusoidal signal is shown in Fig. 4.6.

In Fig. 4.6, the input sinusoidal is $I_0 [1 + \sin (2\pi f t)] \mu A$. We sweep the amplitude and offset $I_0$ through the current range 0 to 70 $\mu$A, which represents the total peak-to-peak swing range 0 to 140 $\mu$A.
The simulated result is linearly proportional to the ideal results. The difference between the ideal curve and the simulation is the constant coefficient and offset, $I_{rms} = K I_{in} + I_{offset}$, which could be accounted for in a real application by the two point calibration method. The relative error of the simulated results after removing the offset is shown in Fig. 4.7. For the specified input dynamic range, the converter has a full-scale relative error less than 1%.

In summary, the built-in current RMS-to-DC converter is designed in the standard 0.35 μm technology. The transient response has shown that the circuit has a similar function as a traditional RMS-to-DC converter. The relative error of less than 1% shows that it is suitable for a BIST application.
Chapter Five

Conclusions

This thesis introduced a built-in current RMS-to-DC converter as a means of generating an on-chip signature for power supply current monitoring. The operation and design procedure of the converter were discussed in detail. Simulation and some silicon measurement results were included. This final chapter presents some conclusions.

5.1 Summary of Thesis

In this thesis, power supply current monitoring was reviewed as an effective test methodology for both digital circuit quiescent $I_{DQ}$ testing and analog/mixed-signal circuit $I_{DD}$ testing. It was concluded as a possible alternative solution to structured BIST for both digital and analog/mixed-signal testing domain. A built-in RMS-to-DC converter for the BIST application was proposed. The architecture of the converter is based on the classical implicit method. A current squarer/divider circuit required in the converter was designed by using the MOS translinear principle.

The class B current squarer/divider was implemented in a standard 0.18 µm technology. Careful layout techniques were used in the manual implementing procedure. The silicon measurement results demonstrate that the total harmonic distortion of this circuit is less than 1.1% with a 1 KHz sinusoidal input signal, which is suitable for an on-chip BIST application. The simulated bandwidth and measured silicon bandwidth are approximately 5 MHz and 1 MHz, respectively.

The RMS-to-DC converter except the current squarer/divider was implemented in a 0.35 µm technology. A total required on-chip capacitance required by the integrating ADC was 74 pF. Special architectural and layout techniques were also applied to the 8-bit
binary-weighted current-steering DAC. The simulated DNL and INL are both within ±0.5 LSB. The simulated relative error of the RMS-to-DC converter is less than 1% for a specified peak-to-peak input current range 0 to 140 µA. These results show that the proposed RMS-to-DC converter is suitable for a BIST application.

5.2 Suggestions For Future Research

The BIST application of power supply RMS current monitoring is a complex topic. This thesis focuses on one aspect of this topic. To make this method suitable for industrial purposes, future research efforts should focus on the following aspects:

- **Improved Current squarer/divider.** The MOS current squarer/divider designed by using the well-known MOS translinear principle has a serious drawback due to its limited dynamic range compared to the bipolar circuitry. Enlarging the dynamic range usually results in a large silicon area or a less accuracy. For a single chip application, the accuracy is more important than the silicon area. However, for a BIST application, a better MOS current squarer/divider with less area overhead and more accurate property needs to be developed;

- **Smaller silicon area of low-pass filter.** The low-pass filter required in the RMS-to-DC converter was based on the switched-capacitor integrator method in our design. Although the on-chip capacitance is already as little as 74 pF, it is still larger than the acceptable value 20 ~ 50 pF. For a BIST application, it is required to design an integrating ADC with a smaller on-chip capacitance value;

- **Study of fault coverage.** The fault coverage of BIST scheme with the RMS-to-DC converter proposed in this thesis needs to be studied.
References


Appendix A

Here, we analyze the class B current squarer/divider circuit shown in Fig. 3.9.

With the current sources, $x/2^{2m+1}$, the currents through transistors M1 and M2 can be represented as

$$I_{D_1} = I_{D_2} = \frac{x}{2^{m+1}} + \frac{1}{4} \cdot (I_{D_3} + I_{D_4}) \quad (1)$$

The current $I_{D_3}$ and $I_{D_4}$ are fed back by the current mirror formed by transistors M7, M8 and M9.

With the help of a current source with current amplitude, $x/2^{m-1}$, the current through M5 can be forced to

$$I_{D_5} = \frac{x}{2^{m-1}} + I_{D_1} + I_{D_4} \quad (2)$$

By including the current source of value, $(3/5)(1/2^{m-1})y$, the current through transistor M6 is

$$I_{D_6} = I_{D_2} + I_{D_3} - \frac{3}{5} \left( \frac{1}{2^{m-1}} \right) \cdot y \quad (3)$$

The current relationship between transistors M5 and M6 is given by:

$$I_{D_5} = n \cdot I_{D_6} \quad (4)$$

Substituting (2) and (3) into (4), we obtain

$$\frac{x}{2^{m-1}} + I_{D_1} + I_{D_4} = n \cdot I_{D_2} + n \cdot I_{D_3} - n \cdot \frac{3}{5} \cdot \frac{1}{2^{m-1}} \cdot y \quad (5)$$

Substituting (1) into (5), (5) becomes

$$\frac{x}{2^{m-1}} = (n-1) \cdot \frac{x}{2^{m+1}} + \frac{5n-1}{4} \cdot I_{D_3} + \frac{n-5}{4} \cdot I_{D_4} - n \cdot \frac{3}{5} \cdot \frac{1}{2^{m-1}} \cdot y \quad (6)$$

If we choose $n=5$, we can drop the term with $I_{D_4}$. This yields:
\[
\frac{x}{2^{m+1}} = 4 \cdot \frac{x}{2^{n+1}} + 6 \cdot I_{D3} - 3 \cdot \frac{1}{2^{m+1}} \cdot y
\] (7)

We can derive the current through transistor M3 as

\[I_{D3} = \frac{1}{2^m} \cdot y\] (8)

If we assume the current through transistor M4 is the output current and

\[I_{D4} = \frac{1}{2^m} \cdot z\] (9)

(1) can be rewritten as

\[I_{D1} = I_{D2} = \frac{x}{2^{m+1}} + \frac{1}{4} \cdot \frac{1}{2^m} \cdot (y + z)\] (10)

The transistor loop formed by M1 to M4 has the translinear relation as follows:

\[\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}}\] (11)

Substituting (9) and (10) into (11), (11) becomes

\[2 \cdot \sqrt{\frac{x}{2^{m+1}} + \frac{1}{4} \cdot \frac{1}{2^m} \cdot (y + z)} = \sqrt{\frac{1}{2^m} \cdot y} + \sqrt{\frac{1}{2^m} \cdot z}\] (12)

By squaring both sides of (12), we obtain the relationship among x, y, z as

\[z = \frac{x^2}{y}\] (13)
Appendix B

This appendix contains the VerilogA modeling of the RMS-to-DC converter. The simulation results are also reported.

Fig. B1 Schematic of modeled RMS-to-DC converter with Verilog-A
The VerilogA program of the squarer/divider for modeling/simulation purposes.

```verbatim
// VerilogA for RMSDC, SD, veriloga

#include "constants.h"
#include "discipline.h"

module SD(z1,z2, x, y,vdd,vss);
inout vdd,vss;
electrical vdd,vss;
output z1;
electrical z1;
output z2;
electrical z2;
input x;
electrical x;
input y;
electrical y;
parameter real min_sigdenom = 1.0e-9 from (0:inf);
parameter real gain = 1;

    real denominator;
    real I0;
    analog begin
        denominator = I(y);
        if (abs(denominator) < min_sigdenom)
            denominator = (denominator > 0.0) ? min_sigdenom : -min_sigdenom;
        I0=gain*pow(I(x),2)/denominator; //z=x^2/y
        I(z1) <+ -I0;
        I(z2) <+ -I0;
    end
endmodule
```
The VerilogA program of HCIinteg for modeling/simulation

```
// VerilogA for RMSDC, HCIinteg, veriloga

'include "constants.h"
'include "discipline.h"

module HCIinteg(EN,phi,sigin,sigout);
    input EN;
    electrical EN;
    input phi;
    electrical phi;
    input sigin;
    electrical sigin;
    output sigout;
    electrical sigout;
    parameter real vlogic_high = 3.3;
    parameter real vlogic_low = 0;
    parameter real vtrans_clk = 1.65;
    parameter real gain = 1e6;
    parameter real sigout0 = 0.0;
    real itrans;
    real itrans0;
    real itrans00;
    integer i;

    analog begin
        @(initial_step)
            begin
                i=0;
                itrans0=sigout0;
                itrans00=sigout0;
                I(sigout)<+sigout0;
            end
        itrans=idt(gain*I(sigin),0) + sigout0;
        @ (cross(V(phi) - vtrans_clk, 1.0))
            begin
                // itransO=itrans;
                if(V(EN))begin
                    itrans0=itrans;
                    i=1;
                end
                else
                    begin
                        i=0; itrans00=0;
                    end
            end
    end
```
@ (cross(V(phi) - vtrans_clk, -1.0))
begin
//
itrans0=itrans;
itrans00=itrans-itrans0;
if(V(EN)) begin
itrans00=itrans-itrans0;
i=0;// itrans00=0;
end
end

if(V(EN)) begin
if(i)begin
I(sigout)<+ itrans-itrans0;
end
else begin
I(sigout)<+ itrans00;
end
end
else begin
I(sigout)<+ sigout0;
end
end
endmodule
The veriloga program of HCIADC for modeling simulation

// VerilogA for RMSDC, HCIADC, veriloga

'include "constants.h"
'include "discipline.h"

module adc8(vd7, vd6, vd5, vd4, vd3, vd2, vd1, 
vdo, inhibit, iin, clk, EN, phi);
output vd7;
electrical vd7;
output vd6;
electrical vd6;
output vd5;
electrical vd5;
output vd4;
electrical vd4;
output vd3;
electrical vd3;
output vd2;
electrical vd2;
output vd1;
electrical vd1;
output vd0;
electrical vd0;
output inhibit;
electrical inhibit;
input iin;
electrical iin;
input clk;
electrical clk;
input EN;
electrical EN;
input phi;
electrical phi;

parameter real vref = 270e-6 ;
parameter real vtrans_clk = 1.65 ;
parameter real vlogic_low = 0.0 ;
parameter real vlogic_high = 3.3 ;
parameter real tdel = 0.0 ;
parameter real tfall = 100e-12 ;
parameter real trise = 100e-12 ;
'define NUM_ADC_BITS 8
  real unconverted;
  real halfref;
  real inh;

  real vd[0:NUM_ADC_BITS-1];
  integer i;
analog begin

@ ( initial_step ) begin
    halfref = vref / 2;
end

@ (cross(V(phi) - vtrans_clk, -1.0))
begin
    inh = vlogic_low;
end

@ (cross(V(phi) - vtrans_clk, 1.0)) begin
    if(V(EN)) begin
        unconverted = -I(iin);
        for (i = ('NUM.ADC.BITS-1); i >= 0 ; i = i - 1) begin
            vd[i] = 0;
            if (unconverted > halfref) begin
                vd[i] = vlogic_high;
                unconverted = unconverted - halfref;
            end else begin
                vd[i] = vlogic_low;
            end
            unconverted = unconverted * 2;
        end
        inh = vlogic_high;
    end
end

// assign the outputs
V(vd7) <+ transition( vd[7], tdel, trise, tfall );
V(vd6) <+ transition( vd[6], tdel, trise, tfall );
V(vd5) <+ transition( vd[5], tdel, trise, tfall );
V(vd4) <+ transition( vd[4], tdel, trise, tfall );
V(vd3) <+ transition( vd[3], tdel, trise, tfall );
V(vd2) <+ transition( vd[2], tdel, trise, tfall );
V(vd1) <+ transition( vd[1], tdel, trise, tfall );
V(vd0) <+ transition( vd[0], tdel, trise, tfall );
V(inhibit) <+ transition( inh, tdel, trise, tfall );

Continue.....

'undef NUM_ADC_BITS
end
endmodule
module Summation(inhibita,inhibitb,clk,phi,Din1,Din2,Dout,math_cntrl) ;
input [7:0] Din1,Din2;
input inhibita,inhibitb,clk,phi;
output [31:0] Dout;
reg [31:0] Dout;
output math_cntrl;
reg math_cntrl;
reg [31:0] Data;
reg cntrl;
reg i;
integer counter;
initial begin
Dout =32'b00000000000000000000000000000000;
Data =32'b00000000000000000000000000000000;
i=0;
cntrl=0;
counter=0;
end
always begin
@(posedge inhibita or posedge inhibitb)
i=1;
end
always begin
@(posedge clk)
if(i) begin
if(inhibita) begin
Data=Data+Din1;
i=0;
end
if(inhibitb) begin
Data=Data+Din2;
i=0;
end
end
counter=counter+1;
end
else begin
if(counter<2) begin
//10 == 5us, 2 == 1us
cntrl=0;
end
end
endmodule
else
    begin
        cntrl=1;
        counter=0;
    end

Dout = Data;
    math_cntrl =cntrl;
end

endmodule
The verilog program of avgVal_2 for modeling/simulation

```verilog
module avgCal_2(rst,EN,cntrl,Din,Dout,Init,Init_b);
  //32-bit input
  //8-bit output
  input rst;
  input EN;
  input cntrl;
  input [31:0] Din;         //32-bit input
  output [7:0] Dout;         //8-bit output
  reg [7:0] Dout;
  output Init;
  reg Init;
  output Init_b;
  reg Init_b;
  reg [15:0] quotient;      //16-bit internal output
  reg [31:0] dividend;      //dividend==Din
  reg [15:0] divisor;       //divisor==counter

  integer counter;
  integer i;

  //synopsys asynch_set_reset "rst"
  always @(posedge cntrl or posedge rst)
    begin
      if(rst) begin
        Dout=8'd0;
        counter=1;
        Init=1'b1;
        Init_b=~Init;
      end
      else if(EN)
        begin
          divisor=counter;
          dividend=Din*10;
          quotient=16'b0000000000000000;
          if(divisor) begin
            for(i=1;i<=16;i=i+1)
              begin
                if(!dividend[31])
                  begin
                    quotient=quotient+1;
                  end
                else
                  begin
                  end
            end
        end
    end
endmodule
```
if(i<=15)
  begin
    quotient=quotient<<1;
    dividend=dividend<<1;
  end
else
  begin
    counter=counter+1;
  end
end  //while begin
if(quotient>255)
  begin
    Dout=8'b11111111;
  end
else
  begin
    Dout = quotient[7:0];
    Init=(Dout==0)?1'b1:1'b0;
    Init_b=~Init;
  end
end  //if(divisor)
end   //if(EN=1)
end  //always begin
dendmodule
The VerilogA program of 8-bit DAC for modeling simulation

// VerilogA for RMSDC, DAC8, veriloga
#include "constants.h"
#include "discipline.h"

module DAC8(vd7, vd6, vd5, vd4, vd3, vd2, vd1, vd0, iout, vdd, vss);
inout vdd, vss;
electrical vdd, vss;
electrical vd7;
inout vd6;
electrical vd6;
inout vd5;
electrical vd5;
inout vd4;
electrical vd4;
inout vd3;
electrical vd3;
inout vd2;
electrical vd2;
inout vd1;
electrical vd1;
inout vd0;
electrical vd0;
inout iout;
electrical iout;
parameter real vtrans = 1.65;
parameter real tfall = 100e-12;
parameter real trise = 100e-12;
parameter real tdel = 0.0;
parameter real iref = 256e-6;

real out_scaled; // output scaled as fraction of 256

analog begin // output scaled as fraction of 256
  @ (initial_step) begin
    // I(out) <+ iref/2; // transition (iref/2, tdel, trise, tfall);
    // end
    out_scaled = 0;
    out_scaled = out_scaled + (((V(vd7) > vtrans) ? 128 : 0);
    out_scaled = out_scaled + (((V(vd6) > vtrans) ? 64 : 0);
    out_scaled = out_scaled + (((V(vd5) > vtrans) ? 32 : 0);
    out_scaled = out_scaled + (((V(vd4) > vtrans) ? 16 : 0);
    out_scaled = out_scaled + (((V(vd3) > vtrans) ? 8 : 0);
    out_scaled = out_scaled + (((V(vd2) > vtrans) ? 4 : 0);
    out_scaled = out_scaled + (((V(vd1) > vtrans) ? 2 : 0);
    out_scaled = out_scaled + (((V(vd0) > vtrans) ? 1 : 0);
end}
if(out_scaled==0) begin
  out_scaled = 128;
end

I(iout) <+ transition( iref*out_scaled/256, tdel, trise, tfall );
end
endmodule
The VerilogA program for the stimulus block for modeling
/simulation.

```
// VerilogA for RMSDC, CLOCK, veriloga

#include "constants.h"
#include "discipline.h"

module CLOCK(clkin,EN,clk,phia,phib,rst);
inout clkin;
electrical clkin;
inout EN;
electrical EN;
inout clk;
electrical clk;
inout phia;
electrical phia;
inout phib;
electrical phib;
output rst;
electrical rst;

parameter real trise = 100e-12 from (0:inf);
parameter real tfall = 100e-12 from (0:inf);
parameter real tdel = 0 from [0:inf);

parameter real vlogic_high = 3.3;
parameter real vlogic_low = 0.0;
parameter real vtrans_clk = 1.65;

real phiaa;
real phibb;
real ena;
real rsta;

parameter integer N=20 from(0:inf);
parameter integer en_start=21 from(0:inf);
parameter integer en_fini= 10e4-20 from(0:inf);

parameter integer rst_start=10 from(0:inf);
parameter integer rst_fini=12 from(0:inf);

integer i,j;
integer NN;
integer counter;

analog begin

@ (initial_step) begin
```
NN=N/2;
i=0;
j=1;
counter=1;
end

@(cross(V(clkin)-vtrans_clk,1.0))
begin
if(NN-i)begin
phiaa= vlogic_low;
phibb= vlogic_high;
i=i+1;
end
else begin
if(NN-j)begin
phiaa= vlogic_high;
phibb= vlogic_low;
j=j+1;
end
else begin
i=0;
j=1;
end
end
if((counter<=en_start)||(counter>en_fini))begin
ena =vlogic_low;
end
else begin
ena=vlogic_high;
end
if((counter<=rst_start)||(counter>rst_fini))begin
rsta=vlogic_low;
end
else begin
rsta=vlogic_high;
end
counter=counter+1;
end
V(phia) <+ transition(phiaa,tdel,trise,tfall);
V(phib) <+ transition(phibb,tdel,trise,tfall);
V(clk) <+ transition(V(clkin),tdel,trise,tfall);
V(EN) <+ transition(ena,tdel,trise,tfall);
V(rst) <+ transition(rsta,tdel,trise,tfall);
end
endmodule
The verilog program of avgVal_2 for modeling/simulation

```
// Verilog HDL for "RMSDC", "avgCal_2" "functional"
// this is the initialized avgCal

module avgCal_2(rst, EN, cntrl, Din, Dout, Init, Init_b);
    input rst;
    input EN;
    input cntrl;
    input [31:0] Din;  //32-bit input
    output [7:0] Dout;  //8-bit output
    reg [7:0] Dout;
    output Init;
    reg Init;
    output Init_b;
    reg Init_b;

    reg [15:0] quotient;  //16-bit internal output
    reg [31:0] dividend;  //dividend==Din
    reg [15:0] divisor;  //divisor==counter

    integer counter;
    integer i;

    //synopsys asynch_set_reset "rst"
    always @(posedge cntrl or posedge rst)
    begin
        if(rst) begin
            Dout=8'd0;
            counter=1;
            Init=1'b1;
            Init_b=-Init;
        end
        else if(EN)
        begin
            divisor=counter;
            dividend=Din*10;
            quotient=16'b0000000000000000;
            if(divisor) begin
                for(i=1;i<=16;i=i+1)
                begin
                    if(!dividend[31])
                    begin
                        quotient=quotient+1;
                    end
                    else
                    begin
                    end
                end
            end
```

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if(i<=15)
  begin
    quotient=quotient<<1;
    dividend=dividend<<1;
  end
else
  begin
    counter=counter+1;
  end
end //while begin
if(quotient>255)
  begin
    Dout=8'b11111111;
  end
else
  begin
    Dout = quotient[7:0];
    Init=(Dout==0)?1'b1:1'b0;
    Init_b=~Init;
  end
end //if(divisor)
end //if(EN=1)
endmodule //always begin
The simulation results of the modeled RMS-to-DC converter are shown below.

The input signal are $100 + 100 \times \sin(2\pi f t)$ with $f = 100$KHz, 1MHz, and 10KHz. From the transient response, we can see the different rippling time for different input frequencies.
Fig. B4 Linearity of different input signals with 100 KHz frequency

The ideal curve is derived by RMS value calculation of input sinusoidal signals. The simulation results illustrate a good linearity of the modeled RMS-to-DC converter. The difference between the ideal and simulation is the slope of the line, which we can calibrate, in an actual application.
Appendix C

In appendix C, the schematic of the RMS-to-DC converter is given.

Fig. C1 Schematic of rms-to-dc converter for simulation
Class B current Squarer/divider

Part I
Fig. C2 Schematic of current squarer/divider (Part II)
Fig. C2 Schematic of current squarer/divider (Part III)
Fig. C3 Schematic of HCI
Fig. C4 Schematic of digital circuit of HCI
Fig. C5 Schematic of analog circuit of HCI
Fig. C6: Schematic of analog circuit of DAC (Part I)

8-bit current-steering DAC Part I
Fig. C6: Schematic of analog circuit of DAC (Part II)
Fig. C7 Schematic of digital circuit of DAC
The stimulus VerilogA program for supplying input stimulus of RMS-to-DC converter.

// VerilogA for RMSDC, CLOCK, veriloga

`include "constants.h"
`include "discipline.h"

module CLOCK(clkin, EN, elk, phia, phib, rst);
inout clkin;
electrical clkin;
inout EN;
electrical EN;
inout clk;
electrical clk;
inout phia;
electrical phia;
inout phib;
electrical phib;
output rst;
electrical rst;

parameter real trise = 100e-12 from (0:inf);
parameter real tfall = 100e-12 from (0:inf);
parameter real tdel = 0 from (0:inf);

parameter real vlogic_high = 3.3;
parameter real vlogic_low = 0.0;
parameter real vtrans_clk = 1.65;

real phiaa;
real phibb;
real ena;
real rsta;

parameter integer N=20 from(0:inf);
parameter integer en_start=21 from(0:inf);
parameter integer en_fini= 10e4-20 from(0:inf);

parameter integer rst_start=10 from(0:inf);
parameter integer rst_fini=12 from(0:inf);

integer i,j;
integer NN;
integer counter;

analog begin

@(initial_step) begin
    NN=N/2;
    i=0 ;
    j=1;


counter=1;
    end

@(cross(V(clkin)-vtrans_clk,1.0))
begin
    if(NN-i)begin
        phiaa= vlogic_low;
        phibb= vlogic_high;
        i=i+1;
        end
    else begin
        if(NN-j)begin
            phiaa= vlogic_high;
            phibb= vlogic_low;
            j=j+1;
            end
        else begin
            i=0;
            j=1;
            end
        end
    end
    if((counter<=en_start)||(counter>en_fini))begin
        ena=vlogic_low;
        end
    else begin
        ena=vlogic_high;
        end
    if((counter<=rst_start)||(counter>rst_fini))begin
        rsta=vlogic_low;
        end
    else begin
        rsta=vlogic_high;
        end
    counter=counter+1;
end
V(phia) <+ transition(phiaa,tddl,trise,tfall);
V(phib) <+ transition(phibb,tddl,trise,tfall);
V(clk) <+ transition(V(clkin),tddl,trise,tfall);
V(EN) <+ transition(ena,tddl,trise,tfall);
V(rst) <+ transition(rsta,tddl,trise,tfall);
endmodule
The verilog program of avg_2 block.

// Verilog HDL for "RMSDC", "avgCal_2" "functional"
//this is the initialized avgCal

module avgCal_2(rst,EN,cntrl,Din,Dout,Init,Init_b);
input rst;
input EN;
input cntrl;
input [31:0] Din; //32-bit input
output [7:0] Dout; //8-bit output
reg [7:0] Dout;
output Init;
reg Init;
output Init_b;
reg Init_b;
reg [7:15:0] quotient; //16-bit internal output
reg [31:0] dividend; //dividend==Din
reg [15:0] divisor; //divisor==counter

integer counter;
integer i;

//synopsys asynch_set_reset "rst"
always @(posedge cntrl or posedge rst)
begin
if(rst) begin
Dout=8'0;
counter=1;
Init=1'b1;
Init_b=~Init;
end
else if(EN)
begin
divisor=counter;
dividend=Din*10;
quotient=16'b0000000000000000;
if(divisor) begin
for(i=1;i<16;i=i+1)
begin
if(!dividend[31])
begin
quotient=quotient+1;
end
else
begin
end
if(i<15)
begin
  quotient=quotient<<1;
  dividend=dividend<<1;
  end
else
  begin
    counter=counter+1;
  end
end //while begin
if(quotient>255)
  begin
    Dout=8'b11111111;
  end
else
  begin
    Dout = quotient[7:0];
    Init=(Dout==0)?1'b1:1'b0;
    Init_b=~Init;
  end
end //if(divisor)
end //if(EN=1)
end //always begin
dendmodule