In presenting this thesis in partial fulfilment of the requirements for an advanced degree at the University of British Columbia, I agree that the Library shall make it freely available for reference and study. I further agree that permission for extensive copying of this thesis for scholarly purposes may be granted by the head of my department or by his or her representatives. It is understood that copying or publication of this thesis for financial gain shall not be allowed without my written permission.

Department of Electrical Engineering

The University of British Columbia
Vancouver, Canada

Date August 11, 2000

DE-6 (2/88)
Abstract

Switch mode power converters have been used in high power applications such as DC links and variable frequency motor drives for a number of decades. In these applications the load is fixed and well known, and therefore the nature of the power demand placed on the inverter is also well known. In more recent years, high frequency switch mode inverters have become available at smaller power levels as consumer products. These inverters are marketed as capable of providing AC power to ANY AC load which the customer may have. In this case the inverter is called upon to supply power to a diverse variety of loads, presenting it with very challenging operational issues, especially with regards start up surge currents.

This thesis investigates the characteristics of the input current drawn by consumer type AC loads, when driven by a standard sinusoidal 60 Hz 110VAC source, with particular emphasis on the inrush current transients found during start up. It then goes on to look at how the surge currents differ when the driving voltage is a non-sinusoidal single step waveform as produced by the vast majority of small inverters. This is followed by a discussion on the benefit of having multiple step waveforms and trapezoidal waveforms, in terms of their effect on the surge current transients. From the discussion on multi step and trapezoidal waveforms, it is shown that a current regulated output is the optimum solution for...
small modified sinewave inverters when they are used to drive typical consumer type loads. This approach is demonstrated in a 300W inverter through the implementation of hysteretic output current control. Finally, AC output bridge switching losses are investigated, and the benefit of a small amount of series output inductance is demonstrated through simulations and circuit trials.
## Contents:

Abstract ...................................................................................................................... ii
List of Tables ............................................................................................................... vi
List of Figures .............................................................................................................. vii
Acknowledgments ....................................................................................................... xi

1. Introduction ............................................................................................................ 1

2. Inrush current characteristics of Typical AC loads ............................................. 6
   2.1 Incandescent Light Bulbs .................................................................................. 6
   2.2 Capacitive Rectified Loads ............................................................................. 8
   2.3 Compact Fluorescent Light Bulbs ................................................................. 12
   2.4 Inductive Loads .............................................................................................. 14

3. Load Simulations ................................................................................................... 16
   3.1 Analytical Investigation of the start up inrush current in AC loads ................ 16
   3.2 Load Models .................................................................................................. 21
      3.2.1 Incandescent Light Bulbs ...................................................................... 21
      3.2.2 Capacitive Rectified Loads ................................................................. 25
      3.2.3 Compact Fluorescent Light Bulbs ....................................................... 27
      3.2.4 Inductive Loads .................................................................................... 29

4. Simulated Inverter Models ................................................................................... 31
   4.1 Single and Multi Step Models ......................................................................... 31
   4.2 THD and RMS voltage .................................................................................. 35
      4.2.1 One step waves ..................................................................................... 35
      4.2.2 Two, three and four step waves ............................................................ 39
   4.3 Simulations of surge currents with 1, 2, 3, and 4 step waves ..................... 46
      4.3.1 Incandescent Light Bulbs ...................................................................... 46
      4.3.2 13" Computer Monitor ......................................................................... 49
   4.4 Trapezoidal waves ......................................................................................... 53
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Hysteretic Current Control</td>
<td>55</td>
</tr>
<tr>
<td>5.1</td>
<td>Hysteretic current control simulation model</td>
<td>55</td>
</tr>
<tr>
<td>5.2</td>
<td>Hysteretic current control circuit</td>
<td>61</td>
</tr>
<tr>
<td>5.3</td>
<td>Experimental results with hysteretic current control</td>
<td>64</td>
</tr>
<tr>
<td>6</td>
<td>Switching Losses</td>
<td>71</td>
</tr>
<tr>
<td>6.1</td>
<td>Theoretical analysis</td>
<td>71</td>
</tr>
<tr>
<td>6.2</td>
<td>Switching Loss Simulations</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td>Experimental Switching Loss Measurements</td>
<td>79</td>
</tr>
<tr>
<td>7</td>
<td>Conclusion</td>
<td>85</td>
</tr>
<tr>
<td>Appendix A</td>
<td>Matlab, T.H.D. minimization program listings</td>
<td>86</td>
</tr>
<tr>
<td>Appendix B</td>
<td>UC3525B PWM data sheets</td>
<td>91</td>
</tr>
<tr>
<td>Appendix C</td>
<td>Typical circuit breaker trip time graph</td>
<td>100</td>
</tr>
<tr>
<td>Appendix D</td>
<td>Typical SOA graph for a 200 Volt, 9 Amp power MOSFET</td>
<td>101</td>
</tr>
<tr>
<td>References</td>
<td>102</td>
<td></td>
</tr>
</tbody>
</table>
List of Tables

Table 1  Breaker trip times versus overload current in percent of rated current .................2
Table 2  Simulation results of peak surge current versus switching angle for monitor load ...............................................................................................................................20
Table 3  Minimum T.H.D. step voltages and pulse lengths for 1, 2, 3 and 4 step waves ....45
Table 4  Output bridge device temperature versus series output inductor value ..................83
List of Figures

Figure 1  Modified "sinewave" ................................................................. 3
Figure 2  Two step wave ................................................................. 4
Figure 3  Measured inrush current for a 75W incandescent light bulb .... 7
Figure 4  Capacitive rectified power supply input stage ................... 9
Figure 5  Measured inrush surge current for 13" IBM PS/1 monitor .... 10
Figure 6  Steady state input current into 13" IBM PS/1 monitor ........... 11
Figure 7  Inrush current into self starting compact fluorescent light bulb 13
Figure 8  Inrush current into ballast type fluorescent light ............... 14
Figure 9  Start up surge into 300W handheld drill .......................... 15
Figure 10 Series RC circuit ............................................................ 16
Figure 11 Instantaneous load voltage at different switching points .... 18
Figure 12 Simulated surge current for first ½ AC cycle .................... 19
Figure 13 Incandescent light bulb load simulation ......................... 21
Figure 14 Simulated inrush current into 75W incandescent light bulb 23
Figure 15 Measured inrush current into 75W incandescent light bulb 23
Figure 16 Typical capacitive rectified load .................................... 25
Figure 17 Simulated inrush surge into 13" IBM PS/1 monitor .......... 26
Figure 18 Measured inrush surge current into IBM PS/1 monitor .... 26
Figure 19 Simulated surge current into self starting compact fluorescent light bulb 28
Figure 20 Measured surge current into self starting compact fluorescent light bulb 28
Figure 21 Load current path during bridge device off state ................ 29
Figure 22 Measured inrush surge current for ballast driven fluorescent light 
when driven by modified sinewave inverter ................................... 30
Figure 23 Measured inrush surge for 300W handheld drill when driven by modified 
sinewave inverter ........................................................................ 30
Figure 24 Output bridge of typical small inverter ......................... 31
Figure 25 Gate drive signals for output bridge, to produce modified sinewave output 32
Figure 26 Modified sinewave output waveform ............................... 32
Figure 27 Multi step inverter simulation model ............................... 33
Figure 28 Gate drive signals for multi step inverter ......................... 34
Figure 29 Definition of pulse length and step height variables for modified sinewave .... 35
Figure 30  T.H.D. as function of pulse length for a single step wave ........................................38
Figure 31  Variable definition for two step wave .................................................................39
Figure 32  Variable definition for three step wave ..............................................................39
Figure 33  Decomposition of two step wave into two, single step waves .............................40
Figure 34  Measured inrush surge for 75W incandescent light bulb when
     driven by inverter ...........................................................................................................46
Figure 35  Simulated inrush surge for 75W incandescent light bulb when
     driven by inverter ...........................................................................................................47
Figure 36  Simulated inrush surge for 75W incandescent light bulb when
     driven by 2 step wave ....................................................................................................47
Figure 37  Simulated inrush surge for 75W incandescent light bulb when
     driven by 3 step wave ....................................................................................................48
Figure 38  Simulated inrush surge for 75W incandescent light bulb when
     driven by 4 step wave ....................................................................................................48
Figure 39  Measured inrush surge for 13" IBM PS/1 monitor when driven by
     modified sinewave ........................................................................................................50
Figure 40  Simulated inrush surge for 13" IBM PS/1 monitor when driven by
     modified sinewave ........................................................................................................50
Figure 41  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by 2 step wave ....................................................................................................51
Figure 42  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by 3 step wave ....................................................................................................51
Figure 43  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by 4 step wave ....................................................................................................52
Figure 44  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by sinewave ........................................................................................................53
Figure 45  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by modified sinewave .......................................................................................54
Figure 46  Simulated inrush surge for 13" IBM PS/1 monitor when
     driven by trapezoidal wave ...........................................................................................54
Figure 47  Basic 300W inverter utilizing push-pull DC-DC stage and
     full bridge DC-AC stage ..............................................................................................56

Masc Thesis for Electrical Engineering  Jarmo Venalainen

viii
Figure 48  Simulation of 300W inverter with voltage control and hysteretic current control ..............................................................58
Figure 49  Simulated inrush surge for 13" IBM PS/1 monitor when driven current controlled inverter ..................................................60
Figure 50  Simulated inrush surge for 13" IBM PS/1 monitor when driven by current controlled inverter, showing current control and HV bus voltage ramp up ..................................................60
Figure 51  Simulated inrush surge current and inverter output voltage for 13" IBM PS/1 monitor when driven by modified sinewave inverter with current control ......................................................61
Figure 52  DC-DC PWM circuit for 300W inverter ..................................................62
Figure 53  Simulation of 300W inverter c/w voltage and current control ..................................................63
Figure 54  Measured inrush surge for 13" IBM PS/1 monitor when driven by modified sinewave inverter ..................................................65
Figure 55  Measured inrush surge current and inverter output voltage for 13" IBM PS/1 monitor when driven by modified sinewave inverter ..................................................65
Figure 56  Measured inrush surge for 13" IBM PS/1 monitor with hysteretic current control in the inverter ..................................................66
Figure 57  Measured inrush surge for 13" IBM PS/1 monitor when driven by inverter with hysteretic current control ..................................................67
Figure 58  Measured inrush surge for 75W incandescent light bulb with no current control ..................................................68
Figure 59  Measured inrush surge for 75W incandescent light bulb with hysteretic current control ..................................................68
Figure 60  Measured inrush surge for compact fluorescent light bulb with no current control ..................................................69
Figure 61  Measured inrush surge for compact fluorescent light bulb with hysteretic current control ..................................................70
Figure 62  Current, voltage and switching loss during switching transition ..................................................72
Figure 63  Switch loss sensing model c/w switch loss integrator ..................................................73
Figure 64  Simulated switch loss with differing voltage steps ..................................................74
Figure 65  Simulated switch loss with differing rise rates ..................................................74
Figure 66  Simulated switch losses with differing load values ..................................................75
Figure 67  Series inductor location on output bridge output ..................................................76
Figure 68  Simulated output bridge switching loss with and without 1.8 uH output inductor .................................................................78
Figure 69  Output current rise rate into compact fluorescent light bulb with no series output inductance .................................................................79
Figure 70  Output current rise rate into compact fluorescent light bulb with 1 uH of series output inductance .................................................................80
Figure 71  Output current rise rate into compact fluorescent light bulb with 10uH of series output inductance .................................................................81
Figure 72  Current spike rate into 0.7 uF capacitor, with no series output inductance ........82
Figure 73  Current spike rate into 0.7 uF capacitor, with 20uH series output inductor ........83
Acknowledgments

The author would like to thank Dr. L. M. Wedepohl and Dr. W. G. Dunford, for their patient support and encouragement throughout the course of study through which this thesis has come to fruition.

A special thank you goes to my parents and my two boys, Kevin and Erik, for their encouragement, love and support. And, thank you Kevin for helping me number all of the figures and equations.

I also want to thank all my friends and associates who have helped me stay on the path to completion.

Finally I would like to acknowledge Dr. Jin and the PSIM program, which has proved to be a very effective and efficient tool for fleshing out and simulating many of the ideas presented here.
Introduction

In the past decade or so, high frequency switch mode power inverters in the range of 50W through to a few Kilowatts have become available for off grid AC power applications such as in solar power installations, boats and motor homes. These inverters are marketed as capable of driving any AC load which the customer may have. Typically the only stated stipulation on what loads a given size inverter is capable of driving is done by identifying steady state power requirements. However, steady state power requirements can be very misleading, primarily due to the large inrush current currents present in the vast majority of “generic” AC loads.

In typical AC loads a large amount of surge power is required to energize and initialize circuitry, or in the case of incandescent light bulbs, a surge is created as the cold filament heats up. For example, a standard filament type light bulb, TV, monitor, or computer, all draw peak inrush surges of about 10 times their normal operating currents during the first AC half cycle after they are switched on, and often continue to draw many times their normal operating current for up to a full second.

When the load is plugged into the AC grid, power is provided through a 15Amp circuit breaker and inrush currents are not a problem. This is because a standard 15 Amp service breaker has very generous over current trip limits. The full graphs are in Appendix C, but the
salient features are summarized in the table below.

<table>
<thead>
<tr>
<th>Current as a percentage of breaker rating</th>
<th>Time to trip (minimum, seconds)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100%</td>
<td>no trip</td>
</tr>
<tr>
<td>110%</td>
<td>300</td>
</tr>
<tr>
<td>200%</td>
<td>30</td>
</tr>
<tr>
<td>500%</td>
<td>5</td>
</tr>
<tr>
<td>1000%</td>
<td>0.9</td>
</tr>
</tbody>
</table>

*Table 1  Breaker trip times versus overload current in percent of rated current*

Because of these generous surge limits, surge limiting during AC load design has generally not received very much attention.

In the case of small inverters, however, the inrush surge is a serious problem. For example, when power is provided by a 300W inverter, the maximum surge current which it can supply is less than 3 Amps, and even in a 1500W inverter, peak currents are limited to about 10 -12 Amps. The difficulty for inverter designers is in creating an overload protection circuit which will protect the inverter's internal circuitry, while at the same time allow enough surge to start loads. Inverter manufacturers have arrived at solutions by introducing various over current sensing and re-start circuits but often with greatly varying degrees of success.
This thesis specifically focuses on the inrush current performance of small inverters, beginning by illustrating the fundamental causes of the start up surge in typical “generic” AC loads, when driven by a pure sinewave. Then investigating how the surge currents differ when loads are driven by a small inverter having a tri state, or also known as, a modified “sinewave” output voltage. Shown below is the modified “sinewave” waveform produced by a typical small inverter, superimposed on a regular sinewave.

![Figure 1. Modified “sinewave”](image)

The voltage swings from +MAX to ZERO to -MAX during each cycle, hence its designation as a tri state wave. The reference to modified “sinewave” is used to differentiate the tri-state wave from a square wave.

This is followed by an investigation of the surge performance of multi step modified sinewave inverters, focusing on how the peak inrush current transients vary with the introduction of additional steps.
A typical two-step wave has the form,

![Two step wave](image)

Figure 2. Two step wave

The two step wave looks like a staircase which loosely follows the sinewave. As additional steps are introduced, the output stepped voltage wave shape begins to approach the shape of a pure sinewave. Indeed, most "true" sinewave inverters produce their output sinewave by pulse width modulation, (PWM), techniques, whereby the output is a filtered multi step wave composed of thousands of steps. At this high step count, the Total Harmonic Distortion diminishes to virtually zero. Next, the benefit of having a reduced rise rate on the AC voltage is looked at through simulations of a trapezoidal output voltage waveform. Through the investigations into the multi-step and trapezoidal waveforms it is shown that optimum surge current performance for small inverters can be achieved, whether stepped,
trapezoidal or sinewave, by utilizing output current regulation in the inverter. This is demonstrated by implementing a hysteretic output current regulation circuit into a small generic 300W inverter.

In the final section, switching losses in the output bridge devices are looked at in detail, and it is shown that they can be greatly reduced by the introduction of a small amount of series inductance.

All simulations are done with PSIM, by Dr. Jin.
SECTION 2: Inrush Current Characteristics of Typical AC loads

Experimental measurements of the start up inrush current in typical consumer type AC loads.

2.1 Incandescent Light Bulbs

Filament type light bulbs are perhaps the most common AC load, and purely resistive. However, due to the fact that the filament must heat up from room temperature to more than a thousand degrees Kelvin, the resistance of the filament changes by an order of magnitude during start up. For example, a typical 100W light bulb starts off with a cold resistance of about 10 ohms, which then rises to a steady state operating resistance of approximately 100 ohms in a few mS. This large resistance swing results in start up surge currents an order of magnitude larger than the steady state current. Shown on the next page is the experimentally measured surge current for a Phillips 75W soft white incandescent light bulb,
In the graph above, the instantaneous voltage at the point where the switch is thrown is about 125 V, and the peak surge current is about 8.7 Amps, (870 mV with the current probe set to 100mV/Amp). This translates to an effective surge load of just under 1100 Watts. During the second half AC cycle, the peak current is down to about 3.6 Amps, and it settles to its steady state value after about three full AC cycles.

Although the steady state load is very small, the transient load during the first AC cycle is
more than an order of magnitude larger. When this current is provided by the output bridge of a small inverter, the surge pulse, though only about 2 mS in duration, is of a large enough amplitude that it comes close exceeding the safe operating area limits of a typical output FET such as an IRF630. SEE APPENDIX D. It should also be noted that this surge was created by only one light bulb, quite frequently inverters are asked to simultaneously switch on multiple light bulbs, which severely compounds the problem.

2.2 Rectified Capacitive Loads

Another common type of household load is a capacitive rectified power supply. This kind of front end power supply circuit is very common, regardless of how the power is filtered and regulated deeper within the load device, and is found in most modern, TV’s, computers, stereos, VCR’s, and many other such appliances and products.
Shown below is a typical capacitive rectified front end for a power supply,

![Capacitive rectified power supply input stage](image)

*Figure 4. Capacitive rectified power supply input stage.*

Although the actual steady state load in these devices is often only a few hundred Watts, during start up, the fully discharged bus capacitor as well as all the rest of the discharged circuits in the load, present what is essentially a short circuit to the source AC voltage. This surge current is usually somewhat limited by designers by using series impedance, R, as shown in the schematic above. The amount of surge limitation however is typically very little given the generous AC grid current supply characteristics as was discussed above.
A typical capacitive rectified load is a common computer monitor. Shown below is the start up surge for a 13" - IBM PS/1 monitor,

![Figure 5. Measured inrush surge current for 13" IBM PS/1 monitor.](image)

The peak current is 22.2 Amps at a switching instant step voltage of 135 V, (just under 3000 W). The surge dies to 9.6 Amps peak during the next ½ AC cycle, then to 5 Amps peak for the next 10 cycles, finally decaying to a steady state current of about 2 amps peak after about 12 full AC cycles. In the case of capacitive rectified loads, even the steady state peak current is exaggerated from the actual steady state load requirements due to current cresting caused by the capacitive rectified input stage. In the graph on the next page, the monitor current is
shown under steady state conditions. The capacitive rectified load can be seen only drawing current from the AC source while the voltage in the bulk capacitor is less than the instantaneous line voltage.

![Graph showing steady state input current into 13" IBM PS/1 monitor](image)

*Figure 6. Steady state input current into 13" IBM PS/1 monitor*

Typical steady state peak currents drawn by various capacitive rectified loads are 4 - 7 times larger than would be the required peak current if the load were purely resistive. The ratio between the peak value drawn by the capacitive rectified load versus a resistive load of the same value is known as the crest factor. In this case, for small inverters, the problem is one of being able to provide the very large peak current at start up, and being able to provide the
steady state peak currents during every cycle of normal operation. When multiple computers and monitors are connected to a single inverter, the peak currents are ALL inherently synchronized with each other and therefore additive. Due to the start up and current crest factor problems, a typical 1000W inverter can only operate about 300 - 400W worth of capacitive rectified loads.

2.3 Compact Fluorescent light Bulbs

Some very small loads, such as self starting compact fluorescent light bulbs, also use capacitive rectified front ends in their power supplies. In this case the actual load is very small, 10 -30 Watts, so the value of the bus capacitance and its surge resistance is also very small. The result is that although the load itself is almost negligible for even the smallest inverters, the surge load into the low impedance bus capacitor can be of the order of 20 times larger than this.
Figure 7. Inrush current into self starting compact fluorescent light bulb.

Once again, as for the monitor, due to the nature of the capacitive rectified load, the peak currents of all the lights will be synchronized when many of them are connected in parallel. In practice, due to this problem, often no more than 3 compact fluorescent lights with can be operated from a small inverter, such as a 300W model. In this case the average load is only about 70W, versus the possible 300W which the inverter should be capable of providing.
2.4 Inductive Loads

Another class of standard consumer loads are inductive loads. Examples in this category are motor loads and ballast driven fluorescent lights. These types of loads do not present the surge current problems shown previously. In this case, although the series inductance shifts the phase of the output current, it also serves to limit surge currents. Shown below is the start up surge for a 75W ballast driven fluorescent light, and a 300W handheld drill.

Figure 8. Inrush current into ballast type fluorescent light.
Figure 9. Start up surge into 300W handheld drill.
3 Load Simulations

3.1 Analytical Investigation of the start up inrush current in AC loads:

The largest peak surge current occurs during the first half AC cycle, and by the second AC half cycle, the peak is down by about 50% from the first cycle. Analytically the current during the first \( \frac{1}{2} \) cycle can be described by a series RC circuit.

\[ V(t) = V_0 \left(1 - e^{-t/RC}\right) \]

for \( t = 0 \) to \( 8 \) 1/3 mSec

Figure 10  Series RC circuit

Where, the values of R, and C depend on the characteristics of the particular load. At the instant when the switch is thrown, the capacitor is fully discharged, leaving only the resistance, R, as the circuit impedance. At any time after the switch is thrown, the capacitor begins to charge up, and hence the current through the circuit begins to go down.
A series RC circuit follows a first order linear differential equation,

\[ V_0 \sin \omega t = \frac{Q}{C} + RI \]

where: \( Q \) = charge on capacitor
\( I \) = current through circuit  \( Eqn \ 1 \)

\[ V_0 \sin \omega t = \frac{Q}{C} + R \frac{dQ}{dt} \]

For which the general solution is,

\[ i(t) = Ae^{-t/\tau} + B \sin(\omega t - \phi) \tau \]

\[ \tau = RC \]

where: \( \phi = \arctan\left(\frac{\tau}{R}\right) \)

\( Eqn \ 2 \)

Where A and B are determined by initial conditions, and in this case are a function of the point at which the load is turned on. In general, the load could be switched on at any point during the AC cycle. Shown on the next page is a graph of the load voltage with two different switching points, \( \phi = 30^\circ \) and \( \phi = 40^\circ \), showing the step voltage change which results in each case.
To simulate a particular load, R is chosen to be equal to the surge resistance of the load and C is chosen to give the correct time constant for the surge in the load. For example, based on the experimental results for the 75W light bulb the surge resistance is about 17 ohms, and the time constant is about 3 mS. Using these values, the required value of C can be computed using, $\tau = RC$, in this case giving a value of 175 uF. The graph on the following page shows the simulated surge current for the first half AC cycle for a 75W bulb at four different switching angles. The time scale is in degrees, where 90° corresponds to one complete AC half cycle, i.e. 8 1/3 mSec.
Switching the load on at a zero crossing produces the lowest peak surge, since in this case the voltage ramps up gradually along with the 60 Hz AC cycle. If the load is switched on at any other point during the cycle, then the step change in voltage, produces a step change in current. For the step change conditions, the peak current at the switching instant is limited only by the surge impedance in the circuit, consisting of the circuit resistance and a negligible amount of inductance in the wiring. The table on the following page lists the peak surge current magnitude as a function of the switching delay in degrees.
In general, the long term solution for current is characterized by a decaying transient component and a driven steady state component. The peak surge current is determined primarily by the magnitude of the surge impedance, R in the load, and secondarily by the switching angle, which determines the step voltage at the point of switching. It is of interest to note that the single most significant factor which determines the peak surge current is the surge impedance of the load, and changing the switching point from a zero crossing to the worst case 90° point, only affects the peak surge by 20%.

The preceding discussion focuses on the peak surge during the first half cycle, showing that the main determinant of the peak surge is simply the surge impedance of the load. The previous model, however, is only valid for the first ½ AC cycle. The next section goes on to develop complete load models.
3.2 Load Models

3.2.1 Incandescent light bulbs:

A complete load model for the incandescent light could be created with a piecewise linear resistance. I.E. increasing values of resistance would be switched into the circuit as a function of time. Alternately, it can be created by utilizing a capacitive rectified circuit, where the transient capacitor current represents the increased current during the time the filament is heating up. In this model, a parallel resistance equal to the steady state resistance of the light bulb provides for the steady state current of the bulb. Below is the complete load model for a simulated incandescent light bulb load.

\[ \text{AC SOURCE} \]

\[ \text{R1} \]

\[ \text{R2} \]

\[ \text{C} \]

\[ \text{Figure 13 Incandescent light bulb load simulation} \]
R1 is the primary load resistance which is chosen to give the normal operating Wattage of the bulb. R2 and C are chosen so that a simulated filament heating current surge is produced. For example to simulate the 75W bulb which was tested previously, R1 is chosen to be 210 ohms to simulate the steady state load of 75W. The surge current was measured at 8.7 Amps when driven by an initial step voltage of 147 volts, therefore the surge resistance needs to be 17 ohms. Finally the time constant for the filament heating surge current is about 3 mS, so C=175uF. Shown on the next page is the simulated and measured surge current for the 75W incandescent light bulb.
Figure 14  Simulated inrush current into 75W incandescent light bulb

Figure 15  Measured inrush current into 75W incandescent light bulb
As can be seen the simulated load current closely follows the actual measured current. The primary difference being that in the capacitive rectified simulation, the transient surge current into the rectified series RC circuit is not drawn for complete half cycles. Rather, current is drawn into the capacitor only at the peaks of the AC cycles when the capacitor voltage is less than the instantaneous line voltage, as is characteristic for capacitive rectified loads. The simulation does however arrive at the same peak currents for all AC pulses, and very closely follows the measured load current during the critical first half cycle.
3.2.2. Rectified Capacitive Loads

A typical rectified capacitive load is as shown below,

\[
\begin{align*}
R_s & \quad \uparrow \quad \text{Diode} \quad \downarrow \quad \text{Diode} \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \quad \uparrow \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
C & \quad \downarrow \quad \text{Diode} \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
R_{load} & \quad \downarrow \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
\text{Diode} & \quad \downarrow \quad \text{Diode} \\
R_s & \quad \downarrow \\
\end{align*}
\]

\[\text{Figure 16 Typical capacitive rectified load}\]

The value of the bulk storage capacitor is typically quite large so as to minimize the ripple current in the load, \( R_{load} \). For the PS/1 computer monitor which was previously measured, the steady state RMS load current is 350 mA, and the peak surge current is 22.2 Amps at a step voltage of 147 Volts, which gives a surge resistance of 7.4 ohms. The value of the bulk capacitance is 1350 \( \mu \)F, and the steady state load is 600 ohms. Shown on the next page is the measured and simulated inrush surge into a capacitive rectified load, (13" IBM PS/1 monitor).
Figure 17  Simulated inrush surge into 13" IBM PS/1 monitor

Figure 18  Measured inrush surge current into IBM PS/1 monitor
The simulated surge current closely follows the measured. The major difference being that the measured monitor load appears to be drawing some additional resistive current outside of the capacitive rectified current. This can be seen as a current drawn outside of the peak currents as shown on the graph inside the green circle.

3.2.3 Compact Fluorescent Light

A compact fluorescent light is a rectified capacitive load, except that the values of the surge resistance and bus capacitance differ. For the 20W Phillips light which was tested, the surge current was 4Amps at a step voltage of 100V, giving a surge resistance of 25ohms. The steady state load is 0.28Amps, giving a steady state load resistance of 430ohms. Finally, the surge current transient lasted about 5mS, giving a required C value of 20uF. Shown on the next page is the simulation with these values as well as the original measured surge current,
Figure 19  Simulated surge current into self starting compact fluorescent light bulb

Figure 20  Measured surge current into self starting compact fluorescent light bulb
3.2.4 Inductive Loads

Motor loads and ballast driven fluorescent lights are inductive, and do not exhibit the start up surge current problems associated with the incandescent and capacitive rectified loads. They do however, produce a large amount phase shift between the AC voltage and current. A full bridge topology as utilized in small inverters, however, has a path for this phase shifted current even during the off period of the bridge devices, by virtue of the MOSFET body diodes as shown below.

![Diagram](image)

*Figure 21 Load current path during bridge device off state*

On the following page are shown the start up current for the ballast driven fluorescent light and 300W handheld drill when driven by a small inverter. The current in either case is stable.
and bounded, although it should be pointed out that the peak surge into the 300W drill at 5 Amps, is over limit for the 300W inverter.

Figure 22 Measured inrush current for ballast driven fluorescent light when driven by modified sinewave inverter

Figure 23 Measured inrush surge for 300W handheld drill when driven by modified sinewave inverter

Masc Thesis for Electrical Engineering

Jarmo Venalainen
4 Simulated Inverter Models

4.1 Single and Multi Step Models

A typical output bridge in a small inverter consists of a full bridge configuration as shown below.

![Diagram of a typical output bridge of a small inverter](image)

*Figure 24 Output bridge of typical small inverter*

To produce a tri state modified "sinewave", diagonally opposite pairs of switches are turned on with the timing sequence as shown on the next page.
Figure 25 Gate drive signals for output bridge, to produce modified sinewave output

And, the resulting output waveform is as follows,

Figure 26 Modified sinewave output waveform
In order to produce multi step waves, two approaches are possible. One is to use PWM techniques to switch the output bridge power devices to produce the desired output waveform. The second is to use additional DC-DC circuitry to create multiple DC potentials and switching circuits to switch them accordingly to produce the multi step output. For this analysis, multiple step waveforms are simulated by using separate DC sources as shown below.

![Multi step inverter simulation model](image)

*Figure 27 Multi step inverter simulation model*

The gate drive signal for the step control is synchronized with the DC/AC bridge control to produce the desired step waveform. For a three step system, the complete timing sequence is
as follows, where signals S1, S2, S3 AND S4 are the bridge drive signals, and signals S5, S6, and S7 are the step control signals as shown labeled in diagram 27 on the previous page.

Regardless of the number of steps, the multi step waveforms are made to follow a pure sinewave as closely possible. In this regard, two parameters are of primary importance. The first one is that the Root Mean Square, (RMS) voltage of the stepped wave should be equal to that of a pure sinewave, and the second is that Total Harmonic Distortion, (THD), as compared to a pure sinewave, should be as low as possible. The following discussion goes through the process of determining the step heights and pulse lengths for a 1, 2, 3 and 4 step wave.

Figure 28  Gate drive signals for multi step inverter
4.2 THD and RMS Voltage

4.2.1 One Step Waves

In a one step wave there are only two parameters to be set, the amplitude, E, and the pulse length, \( \theta \).

![Diagram of one step wave with parameters E and \( \theta \).]

\[ t=0 \]

Since the amplitude of the wave must be set in the end to give the correct rms voltage regardless of the chosen pulse length, this leaves the on period of the wave as the determinant of the T.H.D. The wave is symmetrical and hence has no even harmonics. Taking the \( t=0 \) at the center of the single pulse as shown in figure 29 above, yields the following Fourier Series,
\[ a_n = 0 \quad b_n = \frac{2}{\pi} \int_{-\frac{\theta}{2}}^{+\frac{\theta}{2}} E \cos nxdx = \frac{4E}{n\pi} \sin \frac{n\theta}{2} \quad n = 1, 3, 5, ... \quad \text{Eqn 3} \]

which gives an RMS voltage for each term as,

\[ V_{\text{RMS}}(n) = \frac{2\sqrt{2}E}{n\pi} \sin \frac{n\theta}{2} \quad n = 1, 3, 5, ... \quad \text{Eqn 4} \]

The Total Harmonic Distortion Factor is defined as,

\[ T.H.D. = \sqrt{\frac{V_{2(rms)}^2 + V_{3(rms)}^2 + V_{4(rms)}^2 + ... + V_{n(rms)}^2}{V_{1(rms)}^2}} \quad \text{Eqn 5} \]

Since the sum of the rms voltages of all the harmonic components is equal to rms voltage of the complete wave minus the rms voltage of the fundamental, equation 5 can be rewritten as,

\[ T.H.D. = \sqrt{\frac{V_{\text{rms}}^2 - V_{1(rms)}^2}{V_{1(rms)}^2}} \quad \text{Eqn 6} \]
Where $V_{rms}$ is the rms voltage of the quasi "sinewave", and $V_{1(rms)}$ is the rms voltage of the fundamental component. Using the parameters as set in figure 29, the rms value of the complete wave is,

$$V_{ac-rms} = \sqrt{\frac{1}{\pi} \int_{\frac{\pi-\theta}{2}}^{\frac{\pi}{2}} E^2 d(\omega t)} = E \sqrt{\frac{\theta}{\pi}} \quad \text{Eqn 7}$$

And the rms value of the fundamental component is given by equation 4, as

$$V_{RMS}(1) = \frac{2\sqrt{2}E}{\pi} \sin \frac{\theta}{2} \quad \text{Eqn 8}$$

Substituting these into equation 6, yields the following expression,

$$T.H.D. = \sqrt{\left(E \sqrt{\frac{\theta}{\pi}}\right)^2 - \left(\frac{2\sqrt{2}E}{\pi} \sin \frac{\theta}{2}\right)^2} \quad \text{Eqn 9}$$
This equation needs to be solved to find the value of $\theta$ which will give the minimum T.H.D.

Using numerical methods in Matlab, T.H.D. as a function of $\theta$ has the following form,

![T.H.D. versus pulse length for a quasi sinewave](image)

*Figure 30  T.H.D. as function of pulse length for a single step wave*

The minimum T.H.D. is 29% at a pulse length of 130°, however the trough is fairly wide, so any pulse length between 126° to 143° will give a T.H.D. of less than 30%. We want the rms output voltage to be 120 VAC, so using equation 7, and setting $\theta$ to 130° degrees gives, $E=141V$. The minimum T.H.D. for a single step modified sinewave occurs when the on period is 130°, and the step voltage is 141V.
4.2.2 Two, Three and Four Step Waves

For a two step waveform there are four parameters to set, the amplitude and on period of each step, as shown below,

![Figure 31 Variable definition for two step wave](image)

For a three step waveform, there are 6, and for a 4 step, 8.

![Figure 32 Variable definition for three step wave](image)
Regardless of the number of steps, the aim is still to get the correct RMS voltage while minimizing the THD. The problem of specifying the step sizes and pulse lengths for each individual step in a multi step waveform becomes an n-dimensional minimization problem, where n, is equal to 2 times the number of steps. Any step waveform can be decomposed into a sum of multiple single step quasi "sinewaves" as shown below,

\[ u = u' + u'' \]

**Figure 33** Decomposition of two step wave into two, single step waves
Referring to figure 32, and equation 7, the \( V_{\text{rms}} \) voltage for the complete two step wave is,

\[
V_{\text{rms}} = \sqrt{\frac{1}{\pi} \int_{\frac{\pi+\theta_1}{2}}^{\frac{\pi-\theta_1}{2}} E_1^2 d(\omega t) + \frac{1}{\pi} \int_{\frac{\pi+\theta_2}{2}}^{\frac{\pi-\theta_2}{2}} E_2^2 d(\omega t)}
\]

\[
V_{\text{rms}} = \sqrt{\frac{E_1^2}{\pi} \theta_1 + \frac{E_2^2}{\pi} \theta_2}
\]

\text{Eqn 10}

Similarly, based on figure 32 and equation 4, the \( V_{\text{rms}} \) voltage of the fundamental is given by,

\[
V_{(1)\text{rms}} = \frac{2\sqrt{2}E_1}{\pi} \sin \frac{\theta_1}{2} + \frac{2\sqrt{2}E_2}{\pi} \sin \frac{\theta_2}{2}
\]

\text{Eqn 11}

By analogy, the \( V_{\text{rms}} \) voltage for a step wave with \( m \) steps, and its first harmonic is,

\[
V_{\text{rms}} = \sqrt{\sum_{m=1}^{\infty} E_m^2 \frac{\theta_m}{\pi}}
\]

\[
m = 1,3,5,\ldots,n
\]

\text{Eqn 12}

\[
V_{(1)\text{rms}} = \sum_{m=1}^{\infty} \frac{2\sqrt{2}E_m}{\pi} \sin \frac{\theta_m}{2}
\]

\[
m = 1,3,5,\ldots,n
\]

\text{Eqn 13}
For the two step wave the T.H.D. expression becomes,

\[
T.H.D. = \sqrt{\left( \frac{E_1}{\pi} \frac{\theta_1}{\pi} + \frac{E_2}{\pi} \frac{\theta_2}{\pi} \right) - \left( \frac{2\sqrt{2}E_1}{\pi} \sin \frac{\theta_1}{2} + \frac{2\sqrt{2}E_2}{\pi} \sin \frac{\theta_2}{2} \right)^2}
\]

\text{Eqn 14}

By normalizing the maximum voltage for the two step wave, \( E_{\text{max}} \), one variable can be eliminated,

\[
E_{\text{max}} = E_1 + E_2
\]

\text{Eqn 15}

\[
: \cdot 1 = E_1 + E_2
\]

Eliminating \( E_2 \) from equation 14,

\[
T.H.D. = \sqrt{\left( \frac{E_1}{\pi} \frac{\theta_1}{\pi} + \frac{(1 - E_1)}{\pi} \frac{\theta_2}{\pi} \right) - \left( \frac{2\sqrt{2}E_1}{\pi} \sin \frac{\theta_1}{2} + \frac{2\sqrt{2}(1 - E_1)}{\pi} \sin \frac{\theta_2}{2} \right)^2}
\]

\text{Eqn 16}
This three dimensional minimization problem can be solved by numerical methods by systematically computing the T.H.D. for all possible combinations of the given variables and looking for the minimum. Using Matlab, (see appendix A), gives the following result,

**Minimum T.H.D., step lengths, and step sizes for a two step wave:**

\[
T.H.D. \text{(min)} = 16.6\% \quad \text{at} \\
\theta_1 = 2.7\text{rad} \\
\theta_2 = 1.7\text{rad} \\
E_1 = 0.5 \\
E_2 = 0.5
\]
To complete calculation, the maximum voltage must be set so that the rms voltage of the two
step wave is equal to the desired rms voltage, (120 VAC).

\[
V_{ac-rms} = \sqrt{\frac{E_1^2 \theta_1}{\pi} + \frac{E_2^2 \theta_2}{\pi}}
\]

and,

\[
E_1 = E_2 = \frac{1}{2} E_{\max}
\]

and,

\[
E_{\max} = E_1 + E_2
\]

\[
120 = \sqrt{\left(\frac{E_{\max}}{2}\right)^2 \left(\frac{2.7 - 1.7}{\pi}\right) + \left(\frac{1.7}{\pi}\right)^2 (E_{\max})^2}
\]

\[
120^2 = 0.318 \left(\frac{E_{\max}}{2}\right)^2 + 0.541 (E_{\max})^2
\]

\[
120^2 = 0.0795 \left(E_{\max}^2\right) + 0.541 (E_{\max})^2
\]

\[
120^2 = 0.6205 E_{\max}^2
\]

\[
23207 = E_{\max}^2
\]

\[
E_{\max} = 152
\]
To reduce the dimension of the minimization, for 3 and 4 step waves, the incremental step sizes will be set to $E_{\text{max}}/3$ and $E_{\text{max}}/4$ respectively. Using equations 6, 12 and 13, and the numerical optimization programs in Appendix A, the minimum T.H.D and pulse lengths for the three and four step waves were determined. After the minimum T.H.D. pulse lengths were known, the maximum voltage $E_{\text{max}}$ was determined using equation 12. The following table lists the complete results.

<table>
<thead>
<tr>
<th># of steps</th>
<th>T.H.D.</th>
<th>$\theta_1$</th>
<th>$\theta_2$</th>
<th>$\theta_3$</th>
<th>$\theta_4$</th>
<th>$E_1$</th>
<th>step size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>29%</td>
<td>130°</td>
<td></td>
<td></td>
<td></td>
<td>141V</td>
<td>$E_{\text{max}}$</td>
</tr>
<tr>
<td>2</td>
<td>17%</td>
<td>97°</td>
<td>155°</td>
<td></td>
<td></td>
<td>152V</td>
<td>$E_{\text{max}}/2$</td>
</tr>
<tr>
<td>3</td>
<td>12%</td>
<td>80°</td>
<td>126°</td>
<td>160°</td>
<td></td>
<td>158V</td>
<td>$E_{\text{max}}/3$</td>
</tr>
<tr>
<td>4</td>
<td>9%</td>
<td>69°</td>
<td>109°</td>
<td>138°</td>
<td>166°</td>
<td>160V</td>
<td>$E_{\text{max}}/4$</td>
</tr>
</tbody>
</table>

*Table 3 Minimum T.H.D. step voltages and pulse lengths for 1, 2, 3 and 4 step waves*
4.3 Simulations of surge currents with one, two, three and four step waves

4.3.1. Incandescent Light Bulb

The following graph shows the measured surge for an incandescent light bulb when driven by a modified sinewave inverter, and on the following pages are simulations of how the input surge current varies with a 1, 2, 3, and 4 step waveform.

![Graph showing surge currents](image)

*Figure 34* Measured inrush surge for 75W incandescent light bulb when driven by inverter
Figure 35  Simulated inrush surge for 75W incandescent light bulb when driven by inverter

Figure 36  Simulated inrush surge for 75W incandescent light bulb when driven by 2 step wave
As can be seen the surge current in the one step simulation is very close to that of the measured. One difference is that AC output voltage droops briefly after the load is turned on, until the voltage control loop can respond.

**Figure 37** Simulated inrush surge for 75W incandescent light bulb when driven by 3 step wave

**Figure 38** Simulated inrush surge for 75W incandescent light bulb when driven by 4 step wave
In the simulations there is a 50% reduction in the maximum peak current, from 9.3 Amps with one step down to 5.2 Amps with four steps. However, this reduction is only available if the load is switched on at a zero crossing. For any other switching point the surge will be determined by the step voltage at the switching point. Also visible is the fact that the filament warms up during the first half cycle, i.e. the transient surge lasts only for the first half period. For loads which have surge currents of longer duration, there is much less reduction in peak surge currents between 1 step and 4 step waves, even if the load is switched on at a zero crossing.

4.3.2. 13" Computer Monitor

Shown on the next page is the measured and simulated surge for the IBM PS/1 monitor when driven with a one step modified sinewave.
Figure 39  Measured inrush surge for 13" IBM PS/1 monitor when driven by modified sinewave

Figure 40  Simulated inrush surge for 13" IBM PS/1 monitor when driven by modified sinewave
Figure 41  Simulated inrush surge for 13" IBM PS/1 monitor when driven by 2 step wave

Figure 42  Simulated inrush surge for 13" IBM PS/1 monitor when driven by 3 step wave
In this case introducing additional steps does not significantly reduce the peak surge current, (22 Amps for one step down to 21 Amps for four steps), and this only if the load is turned on at a zero crossing. In the limit as the number of steps goes to infinity the system becomes equal to that of a pure sinewave. From the previous results shown earlier, this means that there will at most be 20% reduction in the peak surge current and this is only present if the load is switched on at zero crossing.
4.4 Trapezoidal Waves

From the analytical analysis into the surge current on pages 14 - 17, and from previous discussion on multi step waves, it is clear that reducing the rise rate of a modified sinewave will at best reduce the peak surge current by 20%, and this only under zero voltage switching conditions. The next three simulations, show the surge current for the 13" IBM PS/1 monitor when driven with a sinewave, a one step wave and trapezoidal wave. As can be seen the trapezoidal wave produces very little reduction in the peak surge.

![Figure 4.4 Simulated inrush surge for 13" IBM PS/1 monitor when driven by sinewave](image-url)
Figure 45  Simulated inrush surge for 13" IBM PS/1 monitor when driven by modified sinewave

Figure 46  Simulated inrush surge for 13" IBM PS/1 monitor when driven by trapezoidal wave
5 Hysteretic Current Control

5.1 Hysteretic Current Control Simulation Model

In the previous three sections it was shown that most AC loads have inrush surge currents with peak magnitudes up to 10 times their normal steady state values for the first few AC cycles. Furthermore it was shown that generating multiple step, trapezoidal, or even sinusoidal waveforms has negligible effect on reducing the peak inrush surge current, (reducing it by 20% at best). Even the smallest inverters are nevertheless called to operate all such loads, and since they are inherently limited in their current sourcing ability, then current regulation is left as the solution. With current regulation, the inverter will behave as a voltage source when the output current is below the maximum which the inverter can source, and become a current source whenever the load tries to draw more current. The specific regulation level is set according to the capability of a particular inverter.

Implementation of current regulation into a switch mode inverter requires a current control circuit in the form of a current loop. A number of approaches are well known, examples of which are average current control, peak current control and hysteretic current control. The current control method used in this instance is implemented through the use of hysteretic current control in the DC-DC section. Hysteretic current control has as its benefits inherent stability and simplicity at the expense of accuracy in the controlled current. Simplicity is
always desired in consumer electronics not only for reliability reasons, but also for achieving the lowest possible cost in a fiercely competitive market. Accuracy of the current control is not necessary here, because the intent is to control peak currents which are an order of magnitude out of bounds, so the residual ripple inherent in hysteretic current control is not significant in this application.

The following schematic shows a typical 300W modified sinewave inverter utilizing a push-pull DC-DC section and full bridge DC-AC as discussed previously.

![Figure 47 Basic 300W inverter utilizing push-pull DC-DC stage and full bridge DC-AC stage](image-url)
This circuit can be operated open loop, since the push-pull topology DC-DC can only produce a peak high voltage DC bus voltage which is limited by the turns ratio of the transformer, analogous to how a conventional 60Hz transformer operates. In practice however, most inverters use a voltage feedback loop to make the DC bus voltage more stable. Shown on the following page is the simulation model of the hysteretically current limited inverter.

The circuit is the same as shown on page 53, except now it has a voltage feedback loop and a hysteretic current limit circuit. In this circuit, the voltage loop operates normally provided
that the output current is below the set point as set by the reference source, I limit set. When
the output current goes above the set point, the current limit OP amp immediately goes low
and shuts down the gate drive to the primary side FET’s. With the DC-DC PWM shut down,
the output current begins to decay as the DC bus capacitor discharges. After the bus
capacitor has discharged to a point where the output current is below the set point, the current
limit OP amp once again allows the DC-DC PWM to start up. The net effect is that the
current control OP-AMP shuts down the primary side DC-DC PWM gate drives whenever
the current is above the set point and allows them to occur whenever the output current is
below the set point.

Hysteresis is introduced into the system, by either having hysteresis on the current control
OP-AMP itself, or by putting an integrator into the current sensing signal, and in this case the
latter was used and can be seen as RX and CX on the inverting input of the current limit
comparator. The amount of hysteresis determines the magnitude of the ripple in the
controlled output current.

The circuit itself has no impact on the steady state efficiency of the inverter since it neither
introduces nor eliminates any switchings during normal steady state operation, merely
eliminating some during transient conditions. Shown on the next page is the simulated surge
current into the 13" IBM PS/1 monitor with the current limit circuit switched on, and set at a
2.5Amps.

Masc Thesis for Electrical Engineering
Jarmo Venalainen

-59-
Figure 49  Simulated inrush surge for 13" IBM PS/1 monitor when driven current controlled inverter

Figure 50  Simulated inrush surge for 13" IBM PS/1 monitor when driven by current controlled inverter, showing current control and HV bus voltage ramp up
As can be seen the output current is limited to 2.5 Amps for the first few AC cycles after start up. In the figure below, the current limit circuit can be seen cutting out after the 8th AC cycle.

![Simulated inrush surge current and inverter output voltage for 13" IBM PS/1 monitor when driven by modified sinewave inverter with current control](image)

**Figure 51** Simulated inrush surge current and inverter output voltage for 13" IBM PS/1 monitor when driven by modified sinewave inverter with current control

### 5.2 Hysteretic Current Control Circuit

The hysteretic current control circuit was implemented in a readily available 300W inverter. In this inverter, the DC-DC PWM utilizes a 3525 PWM chip. This chip directly provides the required push-pull drive signals and also has a couple of other useful features.
including a soft start circuit, built in 5V reference and an external compensation pin on the error amp. Figure 53 above shows a schematic for a 3525 PWM with the main signals.

Voltage divider R1 and R2 set the set point for the desired HV bus voltage by utilizing the built in +5V, Vref signal. C2 and R3 provide for compensation on the error amp, typically in small inverters, as an integrator with fairly high time constant. Push-pull gate drive signals
are produced at the output pins A and B. The soft start capacitor value determines the rate at which the 3525 PWM starts up on power up, or at any time after the shutdown signal has commanded a shutdown.

The hysteretic current control circuit as implemented, is shown in the schematic below in figure 54.

Figure 53  Simulation of 300W inverter c/w voltage and current control

Comparator, COMP1, has an integrator on the input with a time constant of mS, which
provides the required hysteresis for the circuit, and also has a gain of 10 to amplify the sensed current signal. Given that the current sense resistor is 0.1 ohms, the output of COMP1 then becomes a voltage which is directly proportional to the output current. Resistors, R5 and R7, set the current limit, which given the +5V reference voltage and values shown, is set at 2.5 Amps, and it can be adjusted by changing R5/R7. The shutdown pin on the 3525 PWM has a small amount of capacitance to prevent noise signals from triggering the shutdown pin.

5.3 Experimental Results with Hysteretic Current Control

Shown on the next page is the measured surge current graph for the 13" IBM PS/1 monitor without the current limit circuit switched on.
Figure 54 Measured inrush surge for 13” IBM PS/1 monitor when driven by modified sinewave inverter

Figure 55 Measured inrush surge current and inverter output voltage for 13” IBM PS/1 monitor when driven by modified sinewave inverter
Without the current limit, the monitor draws a peak current of 22 Amps, and tries to draw more than 5 Amps for the next few cycles. The inverter cannot supply 5 Amps, as evidenced by the bus voltage which drops to about 105 V. The inverter output peak voltage eventually rises to near its normal value after about 30 full AC cycles.

With the current limit circuit switched on, the output current is limited to 2.5 Amps. The hysteresis band is about 1 Amp peak to peak, and it has a period of about 0.8 mS. It should be noted that the current limit circuit cannot regulate the current at the very beginning of each AC cycle. This is because the HV bus capacitor is fully charged at these points, so that even
though the DC-DC is shutdown, high levels of current are provided directly by the HV bus capacitor. Shown below is the measured monitor start up surge current and shutdown signal as generated by the hysteretic current controller.

![Graph showing measured inrush surge for 13" IBM PS/1 monitor when driven by inverter with hysteretic current control.]

*Figure 57  Measured inrush surge for 13" IBM PS/1 monitor when driven by inverter with hysteretic current control*

The inrush surge current limiting can be seen ending after only 6 full AC cycles.
Similar results for the incandescent light.

![Graph showing measured inrush surge for 75W incandescent light bulb with no current control](image1)

**Figure 58**  Measured inrush surge for 75W incandescent light bulb with no current control

![Graph showing measured inrush surge for 75W incandescent light bulb with hysteretic current control](image2)

**Figure 59**  Measured inrush surge for 75W incandescent light bulb with hysteretic current control
In this case the load is switched on halfway through an AC ½ cycle. With the current limit circuit switched on, the instantaneous output voltage can be seen first decaying to about 30V during the latter half of the first ½ AC cycle as the current limit circuit has told the PWM to shut down. Once the output current is below 1.4 Amps, the PWM starts operating hysteretically and the output voltage can be seen rising up to its nominal value of 145V by the fourth ½ AC cycle.

As shown below, the results are similar in the case of the compact fluorescent light.

Figure 60  Measured inrush surge for compact fluorescent light bulb with no current control
In all cases the current limit circuit keeps the output current in bounds, with exception of the leading edge of each AC pulse. In order to control the current at the leading edge of the AC output pulses, the hysteretic power control would have to be implemented onto the AC bridge power switches, or alternately a method would have to be devised whereby the high voltage bus voltage is brought to zero after each AC half cycle.

Perhaps more significant than the peak magnitude of the leading edge current peak is the fact that it occurs exactly at the leading edge of each AC pulse. Since it is exactly at the leading edge, it causes extremely large switching losses. This is looked at in the next section.

Figure 61  Measured inrush surge for compact fluorescent light bulb with hysteretic current control
6 Switching Losses

6.1 Theoretical Analysis

In relation to the DC-DC switching devices, output bridge losses in a one step modified "sinewave" inverter are very small. Firstly, because the switching rate in the output bridge is only 120Hz versus about 70KHz for the DC-DC. Secondly, although the on resistance of the high voltage output bridge devices is higher than that of the DC-DC switching devices, this is more than offset by the fact that they need only switch $1/10^\text{th}$ the current of the primary side devices. However, as discussed in the previous sections, looking at the switching in detail shows that for most loads the bridge devices are called on to switch load currents which are many times the measured average load current. Under some circumstances, such as when many capacitive rectified loads, such as compact fluorescent lights are connected in parallel, the start up load can rise well beyond the safe operating region of the FET’s, and even under steady state conditions the leading edge current spikes are up to 4 times the steady state current.

Switching losses occur at the switching points, when both the current through, and the voltage drop across the switching devices is changing. Graphically this can represented as shown on the next page,
The peak loss occurs when the switching device is halfway through its switching transition, and the total loss is given by the area under the power, \((VI)\), graph. The following section introduces the switch loss model.
6.2 Switching Loss Simulations

Shown below is the switching loss simulation model.

In this model the voltage across the switching device is equal to the difference between $V_s$ and $V_c$, which is simply the voltage across the resistor $R$. The current through the switching device is sensed by current sensor on the output of the Voltage Controlled Voltage Source, (VCVS). The value of $R$ and $C$ set the simulated switching rise rate. The voltage drop across the switching device and the load current are multiplied to produce the switch power loss signal. Finally, the power loss signal is integrated to compute the total energy lost during switching. On the following page are switch loss simulation results.
In the above graph the step voltage is changed from $\frac{1}{2}V$ to 1V to 2V. The peak increases as a function of $V^2$, as expected from ohms law.

The peak loss is independent of rise rate, but the total switching loss rises a function of $\sim t^2$. 
The simulation below was done with relative load resistances of 1, 2 and 4.

In this case the both the peak loss and total loss vary directly as function of the load. For inverters this means that a 150W monitor will appear as a 3000W load for the output bridge FET’s on a cold start up. And even during normal steady state operation any rectified capacitive load will appear by a ratio equal to the crest factor that it creates. This means that even under steady state conditions, loads such as computers and monitors, appear in terms of output bridge switching losses as loads which are 4 to 7 times larger. Or, in other words, a 300W computer system appears as a 1 to 2 kW effective load in terms of output bridge switching losses.
The step voltage of a modified sinewave needs to be 145V to satisfy the rms voltage requirement, and since the minimum switching time is set by the characteristics of the power devices, there is only one other parameter which can be changed during the switching time, the current. The current during critical switching period can be reduced by introducing series inductance into the output circuit, as shown below.

![Diagram](Figure 67 Series inductor location on output bridge output)

The amount of inductance is chosen so that it will limit the rise of current for just longer than the switching time of the MOSFET's, i.e. in this case about 300nS.
We know that the surge resistance in AC loads must be so that the surge current is limited to less than about 25 Amps, at voltages of 147V, giving a surge resistance of about 6 ohms.

Using \( \tau = \frac{L}{R} \),

\[
\tau = \frac{L}{R} \quad \text{Eqn 18}
\]

\[
\therefore L = \tau R = (3 \times 10^{-7})(6) = 1.8 \mu H
\]

As was shown for the inductive loads, the stored energy in the inductor can be dissipated into the load through the MOSFET body diodes at the end of every AC pulse, (see page 29). The simulation results on the following page show the leading edge switch loss for the 13" IBM PS/1 monitor with and without the 1.8uH series inductor.
With the inductor in place, the peak loss is down by a factor of 10, and the total loss by a factor of 5.
6.3 Experimental Switch Loss Measurements

The graph below shows the current ramping up on the leading edge of an AC pulse with a compact fluorescent light as the load. The compact fluorescent light appears as a virtually purely capacitive load during the turn on edge.

![Graph showing current ramping up on the leading edge of an AC pulse with a compact fluorescent light as the load.](image)

*Figure 69  Output current rise rate into compact fluorescent light bulb with no series output inductance*
As can be seen, the current ramps up in about 500nS, and as this is the time during which the MOSFET voltage drop is also changing from 145V to 0V, it is when the switching losses occur. It should be noted that the current is changing from 0Amps to 3 Amps, since the shunt resistor used to measure the current, was 0.5ohms. Introducing just 1uH of inductance gives the following graph.

Figure 70 Output current rise rate into compact fluorescent light bulb with 1 uH of series output inductance

The rise time has already increased to 1500nS.
With a 10uH series inductor, the following graph results.

![Graph showing output current rise rate into compact fluorescent light bulb with 10uH of series output inductance.](image)

*Figure 71  Output current rise rate into compact fluorescent light bulb with 10uH of series output inductance*

The rise time is up to 11 microseconds.

An Empirical way to confirm that the switching losses are indeed reduced, is to measure the temperature rise of the output bridge FET’s with different amounts of series inductance in the circuit. To do this we use a 0.7 uF capacitor as the load. This capacitor will produce quickly rising current edges, but will have a negligible steady state load. This will mean that the heating in the output FET’s will be due only to switching losses. The following graph shows
the current spike on a leading edge of an AC cycle with the inverter driving the capacitor.

![Graph showing current spike into a 0.7 µF capacitor](image)

*Figure 72: Current spike rate into 0.7 µF capacitor, with no series output inductance*

With the 0.7µF capacitor as the load, the output bridge FET's reached a temperature of 52.3°C, which was indicative of the switching losses they were experiencing. The following table lists the temperature of the output FET's as function of the output inductor value.
The ambient temperature was 22°C. Clearly the inductor dramatically reduces the switching losses. The temperature figures show that switching losses are reduced by 25% with just 2.8uH of series inductance, and 50%, with 20uH. The graph below shows the rising current with 20uH of series inductance. Core saturation can be seen as a rise in the rate at which the current rises, but is not a problem in this case, since the current only needs to be limited for the 300nS turn on time of the bridge FET’s.

![Current spike rate into 0.7 uF capacitor, with 20µH series output inductor](image)

**Table 4** Output bridge device temperature versus series output inductor value

<table>
<thead>
<tr>
<th>INDUCTOR</th>
<th>0uH</th>
<th>1uH</th>
<th>2.8uH</th>
<th>5.3uH</th>
<th>8.7uH</th>
<th>20uH</th>
<th>40uH</th>
<th>60uH</th>
<th>80uH</th>
<th>100uH</th>
<th>160uH</th>
</tr>
</thead>
<tbody>
<tr>
<td>°C</td>
<td>52.3°</td>
<td>45.7°</td>
<td>44.4°</td>
<td>38.2°</td>
<td>36.4°</td>
<td>32.3°</td>
<td>31.3°</td>
<td>30.7°</td>
<td>30.6°</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 73** Current spike rate into 0.7 µF capacitor, with 20µH series output inductor
Also visible is ringing produced by what is now a series LC circuit under the impact of a step voltage change.
CONCLUSION:

Small inverters have become more and more popular in the last 10 or so years in portable power applications. These inverters are called on to power a very wide variety of typical AC devices. Many of these AC loads exhibit very large inrush currents during start up, as well as steady state current cresting in the case of rectified capacitive loads. Sourcing these large peaking currents presents a serious challenge for small inverters. In this thesis it was shown that using stepped or trapezoidal wave forms had negligible impact in terms of reducing the peak surges. A hysteretic current limit circuit was shown to be an effective solution for limiting inrush surge currents. It was also shown that output bridge switching losses in small single step inverters can be significantly reduced by the use of series inductance in the output circuit.
APPENDIX A:

Matlab T.H.D. minimization program listings
% This Matlab M-file finds the plots the value of THD versus pulse length for a single step waveform

x=1.5:0.005:pi
a=(x./pi).^0.5
b=(0.9).*sin(x./2)
sol=((a.^2)-(b.^2)).^0.5./b
thd=sol
plot(x,thd,'b-')
xlabel('Pulse length, degrees')
ylabel('Total Harmonic Distortion Factor, units')
title('T.H.D. versus pulse length for a quasi sinewave')
% This Matlab M-file computes the minimum value of THD for a two step waveform and outputs the pulse lengths and step sizes at the minimum.

echo off all
min=10
for i=1.5:0.01:1.75
    for j=2.2:0.01:2.7
        for k=0.4:0.01:0.55
            echo off all
            a1=(i)/pi
            a2=(k^2)*((j-i)/pi)
            b=((0.9/2)*sin(i/2))+((0.9/2)*sin(j/2))
            b=((0.9*(1-k))*sin(i/2))+((0.9*(k))*sin(j/2))
            a=((a1+a2)^0.5)
            thd=((a^2)-(b^2))^0.5)/b
            if thd <= min
                min = thd
                jmin = j
                jmin = j
                kmin = k
            end
        end
    end
end
min
jmin
inmin
kmin
% This Matlab M-file computes the minimum value of THD for a three step waveform and outputs the pulse lengths and step sizes at the minimum.

```
% This Matlab M-file computes the minimum value of THD for a three step waveform and outputs the pulse lengths and step sizes at the minimum.

echo off all
min=10
for i=1:0.1:pi
    for j=1:0.1:pi
        for k=0:0.1:pi
            echo off all
            a1=(i)/pi
            a2=(k/9)*((j-i)/pi)
            a3=(1/9)*((k-j)/pi)
            b=((0.9*(1/3))*sin(i/2))+(0.9*(1/3))*sin(j/2)+(0.9*(1/3))*sin(k/2))
            a=((a1+a2+a3)*0.5)
            thd=(((a^2)-(b^2))^{0.5})/b
            if thd <= min
                min = thd
                inin = i
                jnin = j
                kmin = k
            end
        end
    end
end
min
jinin
inin
kmin
```
% This Matlab M-file computes the minimum value of THD for a
% four step waveform and outputs the pulse lengths and step
% sizes at the minimum.

echo off all
min=10
for i=1:0.1:pi/2
    for j=1.5:0.1:pi
        for k=2:0.1:pi
            for l=2.5:0.1:pi
                echo off all
                a1=(i)/pi
                a2=(9/16)*((j-i)/pi)
                a3=(1/4)*((k-j)/pi)
                a4=(1/16)*((l-k)/pi)
                b1=((0.9*(1/i»))*sin(i/2))
                b2=((0.9*(1/4))*sin(j/2))
                b3=((0.9*(1/4))*sin(k/2))
                b4=((0.9*(1/4))*sin(l/2))
                a=((a1+a2+a3+a4)^0.5)
                b=b1+b2+b3+b4
                thd=((a^2)-(b^2))^0.5/b
                if thd <= min
                    min = thd
                    imin = i
                    jmin = j
                    kmin = k
                    lmin = l
                end
            end
        end
    end
end
min
imin
jmin
kmin
lmin
APPENDIX B:

UC3525B Regulating Pulse Width Modulator Data Sheet.

Courtesy of Texas Instruments
Regulating Pulse Width Modulators

FEATURES
- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to ±0.75%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

DESCRIPTION
The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to ±0.75% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, (+VIN) ........................................... +40V
Collector Supply Voltage (VC) .................................. +40V
Logic Inputs ......................................................... -0.3V to +5.5V
Analog Inputs ...................................................... -0.3V to VIN
Output Current, Source or Sink ................................. 500mA
Reference Output Current ....................................... 50mA
Oscillator Charging Current .................................... 5mA
Power Dissipation at TA = +25°C ................................. 1000mW
Power Dissipation at TC = +25°C ............................... 2000mW
Operating Junction Temperature .............................. -55°C to +150°C
Storage Temperature Range .................................. -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ......................... +300°C

All currents are positive into, negative out of the specified terminal.

Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS
(Note 1)

Input Voltage (+VIN) ................................................ +8V to +35V
Collector Supply Voltage (VC) .................................. +4.5V to +35V
Sink/Source Load Current (steady state) ....................... 0 to 100mA
Sink/Source Load Current (peak) ............................... 0 to 400mA
Reference Load Current .......................................... 0 to 20mA
Oscillator Frequency Range ..................................... 100Hz to 400kHz
Oscillator Timing Resistor ...................................... 2kΩ to 150kΩ
Oscillator Timing Capacitor .................................... 0.001μF to 0.1μF
Dead Time Resistor Range ..................................... 0Ω to 500Ω

Note 1: Range over which the device is functional and parameter limits are guaranteed.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1525B and UC1527B; -40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, TA = TJ.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>UC1525B/UC2525B</th>
<th>UC1527B/UC2527B</th>
<th>UC3525B</th>
<th>UC3527B</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>UC1525B/UC2525B</td>
<td>UC1527B/UC2527B</td>
<td>UC3525B</td>
<td>UC3527B</td>
<td></td>
</tr>
<tr>
<td>Reference Section</td>
<td>Tj = 25°C</td>
<td>5.062</td>
<td>5.10</td>
<td>5.138</td>
<td>5.036</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>VIN = 8V to 35V</td>
<td>5</td>
<td>10</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>IL = 0mA to 20mA</td>
<td>7</td>
<td>15</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>Over Operating Range</td>
<td>10</td>
<td>50</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Temperature Stability (Note 2)</td>
<td>Over Operating Range</td>
<td>5.036</td>
<td>5.164</td>
<td>5.024</td>
<td>5.176</td>
</tr>
<tr>
<td>Total Output Variation</td>
<td>Line, Load, and Temperature</td>
<td>80</td>
<td>100</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>VREF = 0, Tj = 25°C</td>
<td>10</td>
<td>200</td>
<td>40</td>
<td>200</td>
</tr>
<tr>
<td>Output Noise Voltage (Note 2)</td>
<td>10Hz ≤ f ≤ 10kHz, Tj = 25°C</td>
<td>3</td>
<td>10</td>
<td>3</td>
<td>10</td>
</tr>
<tr>
<td>Long Term Stability (Note 2)</td>
<td>Tj = 125°C, 1000 Hrs.</td>
<td>500mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N Package, DW Package

<table>
<thead>
<tr>
<th>INV</th>
<th>1</th>
<th>16 VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td>NI</td>
<td>2</td>
<td>15 +VIN</td>
</tr>
<tr>
<td>SYNC</td>
<td>3</td>
<td>14 OUTPUT B</td>
</tr>
<tr>
<td>OSC OUT</td>
<td>4</td>
<td>13 VC</td>
</tr>
<tr>
<td>CT</td>
<td>5</td>
<td>12 GND</td>
</tr>
<tr>
<td>RT</td>
<td>6</td>
<td>11 OUTPUT A</td>
</tr>
<tr>
<td>DISCH</td>
<td>7</td>
<td>10 SHUTDOWN</td>
</tr>
<tr>
<td>SOFT-START</td>
<td>8</td>
<td>9 COMP</td>
</tr>
</tbody>
</table>

PLCC-20, LCC-20 (Top View)
Q or L Package

<table>
<thead>
<tr>
<th>N/C</th>
<th>INV</th>
<th>VREF</th>
</tr>
</thead>
<tbody>
<tr>
<td>NI</td>
<td></td>
<td>+VIN</td>
</tr>
<tr>
<td>SYNC</td>
<td>4</td>
<td>18 OUTPUT B</td>
</tr>
<tr>
<td>OSC OUT</td>
<td>5</td>
<td>17 VC</td>
</tr>
<tr>
<td>N/C</td>
<td>6</td>
<td>16 N/C</td>
</tr>
<tr>
<td>CT</td>
<td>7</td>
<td>15 GND</td>
</tr>
<tr>
<td>RT</td>
<td>8</td>
<td>14 OUTPUT A</td>
</tr>
<tr>
<td>DISCH</td>
<td>9</td>
<td>10 SHUTDOWN</td>
</tr>
<tr>
<td>SOFT-START</td>
<td>11</td>
<td>12 COMP</td>
</tr>
<tr>
<td></td>
<td>13 N/C</td>
<td></td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1525B and UC1527B; -40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, TA = TJ.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>UC1525B/UC2525B</th>
<th>UC1527B/UC2527B</th>
<th>UC3525B/UC2527B</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator Section (Note 3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initial Accuracy (Notes 2 &amp; 3)</td>
<td>TJ = 25°C</td>
<td>±2 ±6</td>
<td>±2 ±6</td>
<td>±2 ±6</td>
<td>%</td>
</tr>
<tr>
<td>Voltage Stability (Notes 2 &amp; 3)</td>
<td>VIN = 8V to 35V</td>
<td>±0.3 ±1</td>
<td>±1 ±2</td>
<td>±3 ±6</td>
<td>%</td>
</tr>
<tr>
<td>Temperature Stability (Note 2)</td>
<td>Over Operating Range</td>
<td>±3 ±6</td>
<td>±3 ±6</td>
<td>±3 ±6</td>
<td>%</td>
</tr>
<tr>
<td>Minimum Frequency</td>
<td>RT = 200kΩ, CT = 0.1μF</td>
<td>120</td>
<td>120</td>
<td>120</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum Frequency</td>
<td>RT = 2kΩ, CT = 470pF</td>
<td>400</td>
<td>400</td>
<td>400</td>
<td>kHz</td>
</tr>
<tr>
<td>Current Mirror</td>
<td>IRT = 2mA</td>
<td>1.7 2.0 2.2</td>
<td>1.7 2.0 2.2</td>
<td>1.7 2.0 2.2</td>
<td>mA</td>
</tr>
<tr>
<td>Clock Amplitude (Notes 2 &amp; 3)</td>
<td></td>
<td>3.0 3.5</td>
<td>3.0 3.5</td>
<td>3.0 3.5</td>
<td>V</td>
</tr>
<tr>
<td>Clock Width (Notes 2 &amp; 3)</td>
<td>TJ = 25°C</td>
<td>0.3 0.5 1.0</td>
<td>0.3 0.5 1.0</td>
<td>0.3 0.5 1.0</td>
<td>μs</td>
</tr>
<tr>
<td>Sync Threshold</td>
<td></td>
<td>1.2 2.0 2.8</td>
<td>1.2 2.0 2.8</td>
<td>1.2 2.0 2.8</td>
<td>V</td>
</tr>
<tr>
<td>Sync input Current</td>
<td>Sync Voltage = 3.5V</td>
<td>1.0 2.5</td>
<td>1.0 2.5</td>
<td>1.0 2.5</td>
<td>mA</td>
</tr>
<tr>
<td>Error Amplifier Section (VCM = 5.1V)</td>
<td></td>
<td>0.5 5 2 10</td>
<td>0.5 5 2 10</td>
<td>0.5 5 2 10</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>1 10</td>
<td>1 10</td>
<td>1 10</td>
<td>μA</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>DC Open Loop Gain</td>
<td>RL ≥ 10 MegΩ</td>
<td>60 75</td>
<td>60 75</td>
<td>60 75</td>
<td>dB</td>
</tr>
<tr>
<td>Gain-Bandwidth Product (Note 2)</td>
<td>Av = 0dB, TJ = 25°C</td>
<td>1 2</td>
<td>1 2</td>
<td>1 2</td>
<td>MHz</td>
</tr>
<tr>
<td>Output Low Level</td>
<td></td>
<td>0.2 0.5</td>
<td>0.2 0.5</td>
<td>0.2 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Output High Level</td>
<td></td>
<td>3.8 5.6</td>
<td>3.8 5.6</td>
<td>3.8 5.6</td>
<td>V</td>
</tr>
<tr>
<td>Common Mode Rejection</td>
<td>VCM = 1.5V to 5.2V</td>
<td>60 75</td>
<td>60 75</td>
<td>60 75</td>
<td>dB</td>
</tr>
<tr>
<td>Supply Voltage Rejection</td>
<td>VIN = 8V to 35V</td>
<td>50 60</td>
<td>50 60</td>
<td>50 60</td>
<td>V</td>
</tr>
<tr>
<td>PWM Comparator</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Duty Cycle</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>%</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td></td>
<td>45 49</td>
<td>45 49</td>
<td>45 49</td>
<td>%</td>
</tr>
<tr>
<td>Input Threshold (Note 3)</td>
<td>Zero Duty Cycle</td>
<td>0.7 0.9</td>
<td>0.7 0.9</td>
<td>0.7 0.9</td>
<td>V</td>
</tr>
<tr>
<td>Input Threshold (Note 3)</td>
<td>Maximum Duty Cycle</td>
<td>3.3 3.6</td>
<td>3.3 3.6</td>
<td>3.3 3.6</td>
<td>V</td>
</tr>
<tr>
<td>Input Bias Current (Note 2)</td>
<td></td>
<td>0.05 1.0</td>
<td>0.05 1.0</td>
<td>0.05 1.0</td>
<td>μA</td>
</tr>
<tr>
<td>Shutdown Section</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft Start Current</td>
<td>VSHUTDOWN = 0V,</td>
<td>25 50 80</td>
<td>25 50 80</td>
<td>25 50 80</td>
<td>μA</td>
</tr>
<tr>
<td>Soft Start Low Level</td>
<td>VSOFTSTART = 0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Threshold</td>
<td>VSHUTDOWN = 2.5V</td>
<td>0.4 0.7</td>
<td>0.4 0.7</td>
<td>0.4 0.7</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>VSHUTDOWN = 2.5V</td>
<td>0.6 0.8 1.0</td>
<td>0.6 0.8 1.0</td>
<td>0.6 0.8 1.0</td>
<td>V</td>
</tr>
<tr>
<td>Shutdown Input Current</td>
<td>VSHUTDOWN = 2.5V</td>
<td>0.2 0.5</td>
<td>0.2 0.5</td>
<td>0.2 0.5</td>
<td>mA</td>
</tr>
<tr>
<td>Soft Start Delay (Note 2)</td>
<td>VSHUTDOWN = 2.5V</td>
<td></td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Output Drivers (Each Output) (VC = 20V)</td>
<td></td>
<td>0.2 0.4</td>
<td>0.2 0.4</td>
<td>0.2 0.4</td>
<td>V</td>
</tr>
<tr>
<td>Output Low Level</td>
<td>ISINK = 20mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output High Level</td>
<td>ISOURCE = 20mA</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Undervoltage Lockout</td>
<td>VCOMP and VSOFTSTART = High</td>
<td>6 7 8</td>
<td>6 7 8</td>
<td>6 7 8</td>
<td>V</td>
</tr>
<tr>
<td>Collector Leakage</td>
<td>VC = 35V</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>μA</td>
</tr>
</tbody>
</table>
ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1525B and UC1527B; -40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, TA = TJ.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>UC1525B/UC2525B</th>
<th>UC1527B/UC2527B</th>
<th>UC3525B</th>
<th>UC2527B</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Drivers (Each Output) (VC = 20V) (cont.)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rise Time (Note 2)</td>
<td>CL = 1nF, TJ = 25°C</td>
<td>100</td>
<td>600</td>
<td>100</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time (Note 2)</td>
<td>CL = 1nF, TJ = 25°C</td>
<td>50</td>
<td>300</td>
<td>50</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>Cross conduction charge</td>
<td>Per cycle, TJ = 25°C</td>
<td>30</td>
<td></td>
<td>30</td>
<td></td>
<td>nc</td>
</tr>
<tr>
<td>Total Standby Current</td>
<td>Supply Current</td>
<td>VIN = 35V</td>
<td>14</td>
<td>20</td>
<td>14</td>
<td>20</td>
</tr>
</tbody>
</table>

Note 2: Guaranteed by design. Not 100% tested in production.
Note 3. Tested at fosc= 40kHz (Rr = 3.6kΩ, Cτ = 0.01µF, RD = 0Ω). Approximate oscillator frequency is defined by:

\[
f = \frac{1}{CT \cdot (0.7 \cdot RT + 3RD)}
\]

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.
The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

Shutdown Options (See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

UC1525B Oscillator Schematic

VREF [16]
RT [6]
CT [5]
SYNC [3]
DISCH [7]
GND [12]

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14
7.4k 14k 2k 1k 25k 6pF 400μA 23k 1k 6.2k 250

RAMP TO PWM
BLANKING TO OUTPUT
OSC OUT

UDG-95052
Oscillator Charge Time vs. $R_T$ and $C_T$

![Oscillator Charge Time Graph]

Oscillator Discharge Time vs. $R_D$ and $C_T$

![Oscillator Discharge Time Graph]

UC1525B Error Amplifier

![Error Amplifier Schematic]

Error Amplifier Open-Loop Frequency Response

![Error Amplifier Frequency Response Graph]
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated
APPENDIX C: Typical Circuit breaker trip time graph
APPENDIX D:

Typical Safe Operating Area plot for a 200Volt, 9Amp power FET, showing maximum safe peak pulse currents at various pulse lengths and drain to source voltages.
REFERENCES:


