Differential Testing of

CMOS Integrated Circuits

by

Ashish Syal

B.E. (Electronics and Communication Engineering), University of Delhi

Delhi, India, 1999

A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE MASTER OF
APPLIED SCIENCE DEGREE

in

THE FACULTY OF GRADUATE STUDIES
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

We accept this thesis as conforming to the required standard

THE UNIVERSITY OF BRITISH COLUMBIA

March, 2002

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Department of Electrical Engineering

The University of British Columbia
Vancouver, Canada

Date: 16th Oct 2002.

Abstract

As CMOS technologies scale down, background leakage current increases inexorably, primarily due to device sub-threshold leakage. As a result, conventional single-threshold pass/fail IDDQ testing may no longer be valid for deep sub-micron technology. A number of alternatives to single threshold IDDQ testing have been proposed. A testing technique to complement IDDQ testing that has shown promise is thermal signature testing.

The validity of using temperature as a test observable was investigated. After establishing this, the use of differential thermal sensing as a possible way of detecting bridging faults in CMOS gates was studied. Differential sensing provides high sensitivity to temperature changes generated by internal changes of the power distribution due to defects and immunity to ambient temperature changes. Different topologies for such sensors have been proposed targeting bipolar and BiCMOS. The novelty of the work is that these were the first such sensors to have been developed in CMOS technology. The thermal sensors were designed, simulated, fabricated and the chips that came back were tested. Three different types of sensors were designed and developed. They have the advantage that the performance of the CUT is unaffected by the sensors, as there is no direct electrical loading of the circuit due to them. Since these sensors do not directly load the circuit under test, they allow a non-intrusive methodology for testing. Also the sensors allow for on-line and off-line test, and diagnosis capabilities.

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Acknowledgement

I would like to express my sincere gratitude to Dr. Andre Ivanov for giving me a chance to work with him and providing me with excellent guidance, encouragement, and support during the last two years.

I would also like to acknowledge the support and help which I got from Dr. Res Saleh and Dr. Josep Altet and for their being there for me when I needed them. A special thanks to Mr. Roozbeh Mehrabadi for his technical and personal support in the lab. I also acknowledge Micronet, NSERC, and CMC for providing financial support and equipment for this research. I would also like to thank all the members in the SOC lab for their comments and suggestions and also my friends Karthi, Dave, and Mohsen.

Finally though I cannot express it in words I express my heart felt gratitude and indebtedness to my parents who have encouraged me and helped me in all my endeavors.

Chapter 1

Introduction

The rapid advances in fabrication processes for integrated circuits (ICs) and the market requirements has increased the need to design complex mixed signal application specific circuits (ASIC). The ability to build large chips of unlimited variety and functionality introduces the problem of determining whether those chips have been manufactured correctly or not. Chip designs are simulated to ensure that the circuits compute the proper functions to a sequence of inputs chosen to exercise the chip. But every chip that comes off the manufacturing line must also undergo manufacturing test, i.e., the chip must be exercised to demonstrate that no manufacturing defects rendered it unusable.

A high-speed tester that can adequately handle the millions of transistors on present day chips comes at astronomical costs [1]. Reducing the test time for a single component can help increase the throughput of the tester and has an important impact on the testing cost. This need has evolved the concept of Design for Testability (DFT), where the goal of reducing the cost of testing is facilitated by introducing testability criteria early in the design stage. Testability criteria have become so important that they may even dictate the overall structure of the design [2].

The most important properties for testability of designs are observability and controllability. The observability implies the ease of measuring the value of a node at the output pins. A node of high observability is one that can be observed directly at the output while one with a low observability needs a number of cycles before its state can appear at

the output. Controllability measures the ease of bringing a circuit node to a given condition using only the input pins. An easily controllable node can be brought to a given condition by a single input vector.

1.1 Digital Testing Overview

The testing of digital circuits is usually based on certain well-established test methodologies which include Ad-Hoc testing, Scan Based testing, Automatic Test Pattern Generation (ATPG), and Built-in-Self-Test (BIST).

1) Ad Hoc Testing: Ad hoc testing combines a collection of techniques that can be used to increase the observability and controllability of a design and are generally applied in an application-dependent fashion [1]. The methods includes techniques like partitioning of large state machines, addition of extra test points, provision of reset states, and introduction of test buses.
2) Scan-Based Test: The most popular structured DFT technique used for testing is referred to as scan design as it employs a scan register. In this approach, the registers in the flip-flop are modified to support two operation modes. In the normal mode, they act as clocked registers and in the test mode, the registers are chained together as a single shift-register. This approach incurs only a minimal overhead and the serial nature of the scan chain reduces routing overhead [1].
3) Boundary-Scan Design: With the introduction of new packaging techniques like surface mount and multi-chip modules, the observability and controllability provided by the bed-of-nails approach of testing for circuit boards decreased [1]. This problem was addressed by extending scan based testing to the component and board levels. This

approach called the boundary scan design involves connecting the input and output pins of the component board into a serial scan chain. During the normal operation, the boundary-scan pads act as normal input-output devices. In test mode, vectors can be scanned in and out of pads, providing controllability and observability at the boundary of the components and hence the name [2].

4) Built-in-Self Test (BIST): Built in Self-Test refers to the capability of a circuit to test itself. The BIST techniques can be classified into two categories, namely on-line BIST, which includes concurrent and non-concurrent techniques, and off-line BIST, which includes structural and functional approaches [2]. In on-line BIST, testing can occur during the normal functional operating conditions (concurrent BIST) i.e., the circuit under test (CUT) is not placed into a test mode where functional operation is locked out or during idle state (non-concurrent BIST). Off-line BIST deals with testing a system when it is not carrying out its normal functions. Systems, boards, and chips can be tested in this mode.

1.2 IDDQ Testing

Quiescent power supply current (IDDQ) testing of CMOS integrated circuits is a technique for producing quality and reliability improvement, design validation, and failure analysis [3]. IDDQ plays a complementary role with logic response tests in the detection of faults. The basic principle behind IDDQ testing is that a CMOS circuit in the normal mode of operation would consume very little power [31] and when in standby mode it would draw practically no current, just the leakage current. IDDQ testing is performed by measuring the current of the VDD power supply in the quiescent logic condition after the inputs have

changed, and prior to the next input change. Fig 1.1, shows the basic principles of IDDQ testing. In this Figure, a generalized IC has a gate oxide defect in a p-channel transistor of an internal logic gate. When the input to a logic gate changes from logic 1 to logic 0, the magnitude of IDDQ changes from a low value to an elevated value. Built-in current sensors attached to this circuit can detect elevated values of current, and if this value is above a threshold value, the circuit is declared faulty.

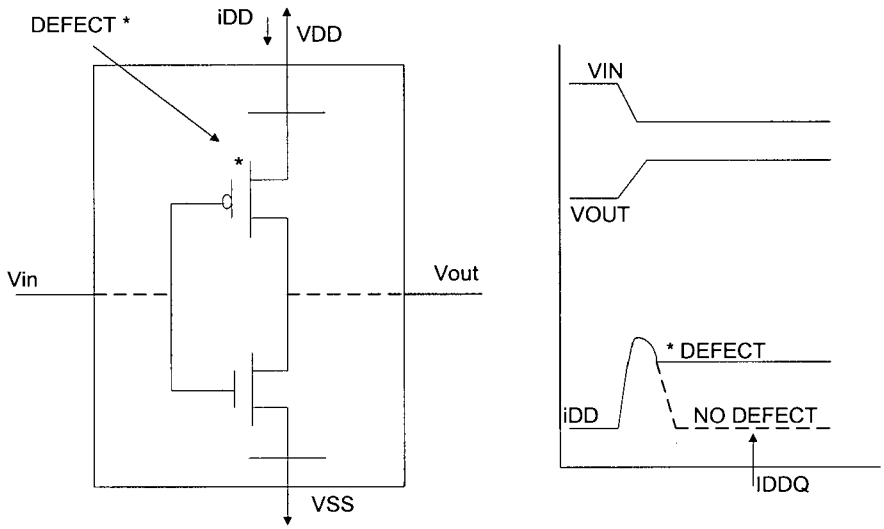

Fig 1.1: CMOS Inverter with voltage and current waveforms

A very critical requirement for IDDQ testing is that very small values of current be measured at the VDD and VSS supply of the circuit under test (CUT). The threshold value for a pass/fail IDDQ test is in the range of 1-10 μA [4]. For a clear decision that the CUT has passed the test, the measured value of the current must be an order of magnitude smaller than the set threshold. However the problem of diagnostics and the pass/fail decision making with IDDQ testing become increasingly difficult as the feature size and supply voltage are reduced with the scaling of technology. As CMOS processes are scaled

to the deep sub-micron region, device reliability and low power constraints enforce a reduction in the power supply voltage [5,6] which in turn necessitates lower transistor threshold voltages. For a lower threshold voltage there is an increase in the sub- threshold leakage currents. The off or standby current will increase by 100 times as we move from 0.5 micron to 0.1 micron [4]. The off current for an enhancement mode transistor is defined as the leakage current when V_{GS} = 0V [2]. As a result of this scaling we see that single threshold IDDQ testing loses its effectiveness.

In order to extend the lifetime of IDDQ testing a number of new techniques have been put forward. Some of these will last for a single generation and some will last longer. Techniques such as splitting power supply lines last only a single generation but techniques such as measurement analysis which treats finding a defective current within an IDDQ measurement as a signal extraction from a noisy reading will last longer [5]. A number of new approaches that can last for longer than a generation are dynamic current measurement, energy consumption measurement, and thermal testing. The purpose of this thesis is to advance the idea of thermal testing.

1.2 Thermal Testing of Integrated Circuits

In [7], a built-in dynamic thermal strategy is presented as an alternative testing technique for integrated circuits: CMOS digital circuits generally have a very low power dissipation during the quiescent phase between two logic transitions. If there is a defect in the CUT structure and a test vector activates it, an electrical path can be established between the power supply and the ground rails. Thus, it can be concluded that some MOS devices dissipate an extra amount of power, behaving as unexpected heat sources and increasing

the temperature around their location. The magnitude of the power dissipated by these devices depends on their dimensions, supply voltage, and topology of the defect [8]. Built-in temperature sensors can be used to detect this extra power dissipation, and therefore, to detect a defective circuit. Thus , temperature is used as a test observable. The advantage of this technique is that the temperature sensor is not electrically connected to the test circuit, preventing circuit performance degradations.

Failure analysis [9] and failure prevention of the circuit under test can be done by using temperature as a measuring parameter. The heat flow path from the heat source to heat sink is modified if there are breaks in it and these can be found out by checking the absolute temperature of the IC at specific points. CMOS built-in temperature sensors have been proposed [10,11,12] in order to guarantee thermal integrity and the presence of safe values of the CUT working temperature. In [13], abnormal temperature increase profiles generated by defects in the CUT are detected by using thermographic images and liquid crystals. In [14], transient differential thermal measures of the silicon surface are taken, using a built-in temperature to build short circuit protection for a current booster.

1.3 Scope of thesis

The first part of this thesis presents a broad understanding of thermal testing of integrated circuits and the latter part concentrates on a specific type of thermal testing, which is differential thermal testing. In Chapter 2, we look into the prevalent methods of thermal testing, which include differential and absolute thermal testing. A brief overview of absolute thermal testing is provided and the concept of differential thermal testing is introduced and the work done in differential Bi-CMOS thermal sensors is described by

discussing one such sensor circuit. In Chapter 3, a thermal strategy for reading out the thermal data is presented. This Chapter also covers an investigative study of the variation of the temperature across the silicon surface for a fault free and faulty Operational Amplifier. Chapter 4 presents three differential thermal sensors designed in CMOS technology. The sensors are the first such sensors to be designed in CMOS and are presented in this chapter with simulation and test results. After this the application of the developed sensors to the testing of analog circuits is shown. Chapter 5 presents a critical evaluation of the thermal testing process and recommendations for future work required in this area are given.

Chapter 2

Background Work

The design of an electrical circuit in ICs also creates a thermal system. The downscaling of technologies has led to greater power and packaging densities resulting in thermal effects becoming more and more significant. The increased power density results in higher chip temperatures, leading to changes in device parameters, and thereby a reduction in the reliability of the circuit. The reliability of the circuit depends exponentially on the temperature of the junction. Such small differences in operating temperature (10-15°C) can result in a ~2X difference in the life span of the devices [15]. Also, it is necessary to maintain the temperature of the device at a certain level, as the speed of the device, in many cases, depends on the operating temperature. Various tools and design methods enable thermal measurement of operating circuits and hence early detection of faults.

2.1 Thermal protection of microcomputer elements

High-clock- rate devices dissipate a considerable amount of power. Maximum power trends (e.g., for microprocessor units) are divided into two categories:

1) High performance desktop applications, for which a heat sink on the package is permitted.
2) Portable battery operations.

In both cases, the total power consumption continues to increase, despite the use of lower supply voltage. The increased power consumption is driven by higher operating

frequencies and higher overall resistance of larger chips with more on-chip functions. The power consumption for today's high power applications is expected to increase from 100W in the year 2000 to 160W in 2005 [15]. Sophisticated cooling techniques such as finned dissipaters on the package, forced convection, and cooling fans reduce even such high amounts of heat. Small thermal disturbances can affect the effectiveness of the cooling process and cause unacceptable temperature increase across the chip. To avoid damage, these processors require active temperature monitoring that launch power reducing actions when the danger of overheating occurs.

2.2 Sensing Strategies

Temperature mapping reflects the temperature distribution across the chip surface. There are two general strategies for the detection of active heat sources on the chips:

(1) Off-chip temperature measurement strategies.

(2) On-chip temperature sensors.

The most commonly used off-chip method is infrared thermography [31]. The core of the equipment is an infrared (λ = 2,4,...12μm) camera with its infrared detector cooled to an extremely low temperature to eliminate noise. It usually scans the image mechanically, using rotating mirrors or prisms. Infrared thermography provides a high temperature resolution, of the order of .1°C with a spatial resolution of the order of 10μm. The method is very fast and can be used to investigate transient phenomena, but it is highly expensive. Another popular off-chip method in popular use is liquid crystal thermography [17]. This is based on the fact that liquid crystals have different phases, which show different optical properties. The phase transitions occur at well-defined temperatures. The surface of the

chip is covered with a liquid crystal, which makes transition lines optically inspectable, and each transition represents an isotherm of the temperature map. The temperature resolution of this method is higher than 0.1°C and the spatial resolution is about 3μm. This method is cheaper than infrared thermography but takes a much longer time to obtain the thermal map [17]. Reflectrometric and interferometric techniques provide high sensitive and wide dynamic range temperature measurements and have been used successfully for failure analysis [17].

On-chip or built-in temperature sensors, albeit an area overhead, provide flexibility for the test procedure, allowing both laboratory testing and in-field testing. Neither direct visual access to the silicon die nor a laboratory environment is required. Direct thermal coupling measurements can be taken, without being affected by any layer over the silicon. The output signal of the built-in-sensor can be proportional to absolute temperature or proportional to the difference of temperature at two points of the silicon surface.

2.3 Desired Characteristics of an On-Chip Thermal Sensor

Thermal sensors are used for a variety of purposes, for on-chip and off-chip applications. However, designing a temperature sensor for IC testing applications is a different task. An effective sensor must have the following characteristics: small area, easy accessibility and low power dissipation in addition to high reliability and high sensitivity. A smaller sensor is easier to place and route within a large CMOS chip. Small sensors are also more effective in sensing defects as they can be placed closer to probable defect locations and small variations in temperature can also be detected. By reducing the distance between the

sensor and the defect, more sensors can be deployed to increase coverage and decrease the average distance between the sensor and a potential defect.

The second criterion for a temperature sensor is easy accessibility of results. Many modern sensors can sense temperature, but extracting results from those sensors proves to be troublesome. Voltage and current output sensors are susceptible to noise from core power supply and from the automatic test equipment (ATE). Some sensors that have digital outputs tend to generate a clock as an output [12]. A clock output is fine for a single on-chip sensor. However, it may become very time-consuming to read the results from a large number of on chip sensors within a short period of time [18].

The third criterion for temperature sensor effectiveness is power consumption. A power hungry sensor may dissipate more heat than the fault that it is trying to sense. If a large number of thermal sensors were placed within an IC, the total power consumption of the test structure may overwhelm the current handling capability of the IC. Hence, the IC would have to be modified to handle the extra current that the test structure requires when active.

The fourth criterion is a high resolution of the temperature sensor. Some defects cause an increase in temperature. This increase can be high or can be very small. A sensor with a high resolution can detect very small increases in temperature.

The fifth criterion is high sensitivity of the temperature sensors. Sensitivity of a sensor is determined by the amount by which the output variable, which could be current, voltage or frequency, of the sensor is affected by the increases in temperature. For a sensor with a high sensitivity, even small changes in temperature causes the output variable to change appreciably.

Finally, one very important criterion for a temperature sensor is compatibility with a target process, without any additional fabrication steps. In our case this implies that the sensors be designed in CMOS technology. MOS technology is less appropriate to realize temperature sensors than bipolar process, so providing a good CMOS sensor is a real challenge today [16]. A large number of temperature sensors in CMOS technology are made using the parasitic bipolar transistors. But the use of MOS only sensors provides a better alternative as the parameters of the MOS transistors are strictly controlled whereas the control of parasitic bipolar transistors is not so. Also, this provides a process independent production as only the MOS technology parameters are to be taken care of.

Two different thermal testing strategies are discussed here: differential temperature sensing and absolute temperature sensing. Differential sensing provides high sensitivity to temperature changes generated by internal changes of the power distribution due to defects and immunity to ambient temperature changes [17]. On the other hand, absolute temperature sensors provide information about working temperature of the CUT, information that can be important for reliability purposes.

2.4 Absolute Temperature Sensors

Absolute temperature sensors increase the system reliability by predicting eventual faults caused by excessive chip temperatures. The main objective of on-chip absolute thermal sensors, from a reliability and test point of view, is to provide continuous thermal verification, which is useful to detect the excessive power dissipation and eventually chip deterioration. Transistors, MOSFETs, and diodes can be used as absolute temperature sensors. Transistors are in general much better sensors than diodes because their base is

very thin and they are three port devices, makes the incorporation of these devices in electronic circuits much more convenient. The use of a transistor as a temperature sensor is based on I_c-V_{be} characteristics where I_c is the collector and V_{be} is the base to emitter voltage of the transistor. The emitter current I_e consists of a diffusion, a surface leakage and a recombination component. The collector current, I_c consists of the diffusion component, and the base current I_b consists of the other two components. The expression for the dependence of V_{be} on collector current I_c and temperature T of the device is given by [33]:

$$V = V_g(0) + (kT / q) \ln[I_c - \ln(KT^r / \eta)] \qquad (2.1)$$

Where $V_g(0)$ is the band gap voltage at 0 K, k is the Boltzman constant, T is the temperature in Kelvin, q is equal to the charge of an electron, I_c is the collector current, r is a constant varying between 3 to 5 for commercially available devices, and η is the ionization factor. Based on Equation 2.1 a transistor can be used as an electrical thermometer. Making use of only one transistor, the collector current can be varied between a fairly high value I_{c1} and a fairly low value I_{c2} with corresponding base values V_{be1} and V_{be2}. The voltage difference is given by:

$$\Delta V_{be} = V_{be1} - V_{be2} = (kT / q) \ln(I_{c1} / I_{c2}) \qquad (2.2)$$

Differentiating this voltage difference to temperature gives :

$$\alpha = d(\Delta V_{be})/dT = (k/q)\ln(I_{c1}/I_{c2}) \qquad (2.3)$$

The temperature coefficient α is a constant and ΔV_{be} is directly proportional to the absolute temperature T. Also, α and ΔV_{be} are independent of materials or transistor parameters. Such sensors are known as Proportional to Absolute Temperature (PTAT) sensors. A number of sensors using the same principle but more sophisticated techniques have been proposed and implemented [33]. It is also possible to use the same idea for MOS technology sensors. It appears that a MOS transistor in weak inversion exhibits a similar exponential relationship between the control-gate voltage and the channel current as V_{be} and I_e in bipolar transistors, but the spread in data is still very large [33].

In CMOS technology there are three possible devices which can be used as temperature sensors, which are, lateral bipolar transistors, vertical bipolar transistors, and CMOS transistors operating in weak inversion. The temperature sensed by these sensors is then converted into an oscillating signal and thus facilitates the evaluation of the temperature sensed.

The basic architecture of an absolute thermal sensor is as shown in Fig 2.1 [18]. The sensor is based on the Proportional to Absolute Thermal (PTAT) current reference generator driving a counter through a ring oscillator. The delta V_{gs} generator performs the temperature sensing and a ring oscillator converts the current to an oscillating square wave. The counter measures the frequency of the ring oscillator and makes the results available to

a scan chain. The oscillator's frequency depends on the temperature. By counting the oscillator's pulses in a time window, we obtain a measure of the temperature.

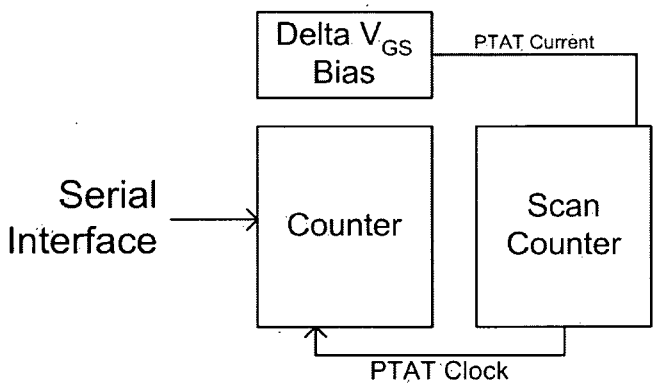

Fig 2.1: Basic architecture of an Absolute Thermal Sensor

2.5 Differential Thermal Sensors

If the thermal disturbance generated by defect activation is to be used as a test observable, differential thermal testing can be used as the test strategy. Differential thermal sensors compare the temperature of the circuit under test to the ambient temperature of the silicon surface and determine whether the thermal variation of the temperature is due to defect activation or not.

Previous work in differential thermal sensors has been done using BiCMOS technology. [17] provides a good perspective to the differential thermal sensors developed in BiCMOS technology. Here, we present a brief look at the concept behind these sensors by reviewing one such sensor. Fig 2.2 shows the schematic of the sensor.

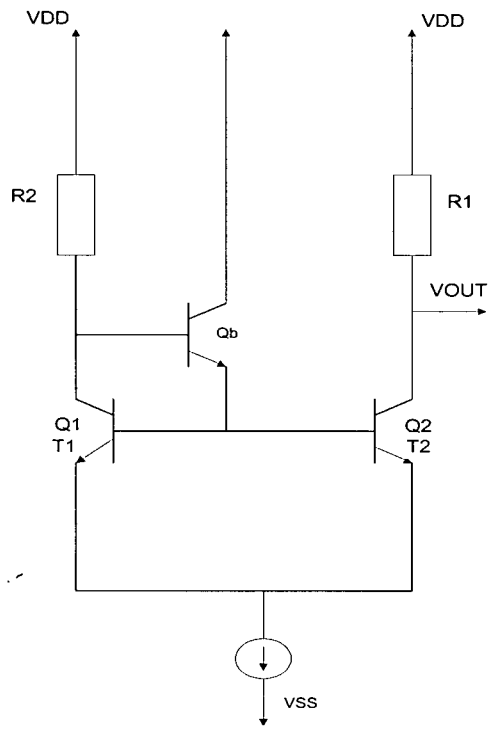

Fig 2.2: Schematic of a BiCMOS differential thermal sensor

This sensor has the same structure as a differential amplifier. In the case of a differential amplifier if there is a small difference in the base-emitter voltage, it results in a different currents flowing through the two transistors. Here, however, temperatures difference between the two transistors imbalances the structure and this causes a difference in the current flowing through the two transistors Q1 and Q2. If the ambient temperature of the silicon surface were T, and if a heat source is activated, the temperature of the bipolar transistors will increase and will be:

$$T1 = T + \Delta T1$$
$$T2 = T + \Delta T2 \qquad (2.4)$$

where T1 is the final temperature of the transistor Q1 and T2 is the final temperature of the transistor Q2. ΔT1 is the change in temperature of Q1 and ΔT2 is the change in temperature of Q2. When the base current of the transistor Q_b is zero and R=R1= R2, Q1 and Q2 would have the same operating point and thus the same small signal model. If the temperature of Q_b remains at the temperature of T, and the output resistance of the current source I_e be assumed to be infinite, then the output voltage is given by [17]:

$$\Delta V_{out} = S_T r_o R[\Delta T1 - \Delta T2]/[2(r_o + R)] \qquad (2.5)$$

where r_o is the output resistance of Q2 and S_T is the sensitivity parameter given by $\partial I_c/\partial T$. Fig 2.3 shows the complete schematic of a BiCMOS thermal sensor. Devices MR1 to MR4 are connected in a cascode configuration and hence provide a high output impedance. The imbalance in current caused by a temperature differential across the sensor in the two transistors Q1 and Q2, is amplified by the cascoded output configuration. Thus the presence of these sensors allows the detection of bridging faults in the circuits by using the change in temperature caused by these faults to cause a variation of the output voltage of these sensors.

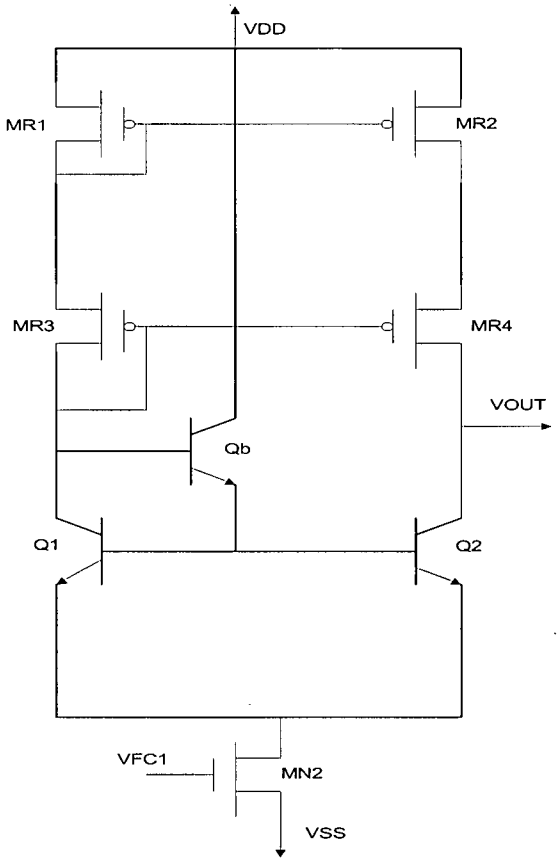

Fig 2.3: Cascoded BiCMOS differential thermal sensor

Chapter 3

Feasibility of Thermal Testing

Every circuit dissipates power within a range/distribution, when it is in a normal mode of operation. This consumed power is converted into heat and spreads across the silicon surface causing a thermal gradient. Each circuit forms a specific thermal gradient, which is known as the thermal signature of the circuit. This thermal signature can be determined using off-chip measurement techniques or on-chip absolute thermal sensors of a functionally correct integrated circuit. The differential thermal sensors placed near the circuit are biased based on the thermal gradient around the circuit. If there is a defect in the circuit, the thermal gradient around the circuit changes and the differential thermal sensors detect this change. The placement of the sensors on the silicon chip can be done on an ad-hoc basis or by using a well-defined methodology. This methodology is given the name design for thermal testability (DFTT).

3.1 Design for Thermal Testability (DFTT) methodology

Recent research works have proposed that instead of ad-hoc solutions, we should establish a regular, commonly accepted methodology for insertion of thermal sensors [19]. A DFTT methodology for testing of integrated circuits should encapsulate a broad based strategy, which includes the important characteristics of the designed thermal sensors, placement strategy, a readout strategy, an evaluation strategy, and the type of faults that can be detected. This methodology would result, as is also the case with Design for Testability (DFT), with enhanced thermal testability but at the expense of excess silicon area.

3.1.1 Sensor Features

The most important features of thermal sensors as was discussed in Chapter 2 are small area, easy accessibility, low power dissipation, high reliability and high sensitivity. The designed sensor is realized in the form of a cell that becomes part of a standard library cell. The sensor also has the advantage of portability in that its operation is independent of the type of CUT.

3.1.2 Placement Strategies

The designer must decide how to place the thermal sensor to achieve the best fault coverage properties. The placement is done either manually or by using place and route tools. The manual placement requires that the thermal gradient of the silicon surface of a defect free integrated circuit be analyzed and the sensors be placed where there is a maximum probability of a defect and/or maximum power dissipation. Automatic place and route tools allow the sensors to be placed in a regular arrangement of 2*2 or 4*4 or n*n cells. A weakness of this approach is that the sensors would not be placed at optimum positions hence the probability of detection of faults is reduced.

3.1.3 Readout strategy

The output of differential thermal sensing is a change in output voltage of the sensors. This change in output voltage is converted into a digital output, either a code word or a square wave function, using analog to digital converters. Stand-alone circuits are a possible solution to accessing the results of the output voltage of the sensors, but the better alternative is to combine the readout circuits with other built-in test hardware [12]. One such method involves combining the thermal test circuitry into the boundary scan architecture and is shown in Fig 3.1. This technique has the advantage that no extra pins are required. All the thermal sensors on the chip can be multiplexed together. They can then be

accessed using signals from the test access port controller. Thermal testing can be interfaced with other built-in self-test schemes.

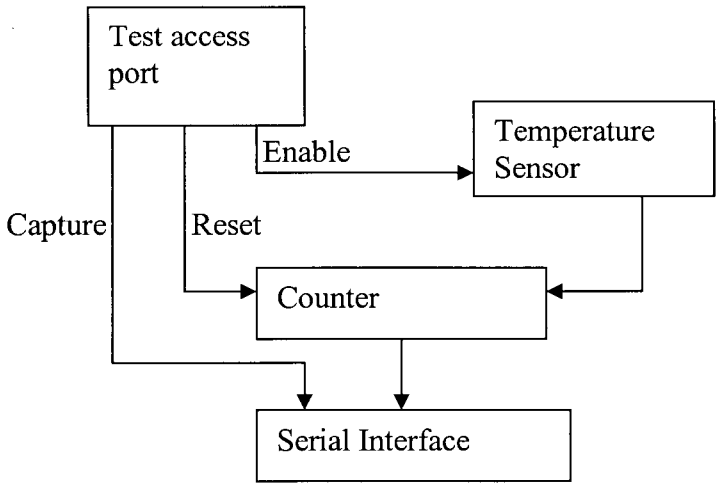

Fig 3.1: Serial interface of the CMOS-compatible temperature sensor

3.1.4 Evaluation Strategy

The simplest evaluation technique is for the test software system to scan the temperature of all sensors and compare it to a known template. If there is a variation from the known set of temperature template, then a fault has been detected. Thermal testing provides not only detection but also diagnostic abilities. Due to the diffusion nature of the thermal transfer of heat through the silicon die, simple signal processing of the waveform sensed at the monitoring point can provide the distance between the heat source and the monitoring points. Therefore, by processing the information from the various temperature sensors the exact location of the heat source can be calculated. [17]

3.2. Concept of Electrothermal Networking

An extracted RC network was used to understand the heat flow through the substrate. This extracted RC network allows us to estimate the heat flow through the silicon substrate. The concept behind the network is the analogy that can be drawn between basic electrical and thermal variables (Fig 3.2).

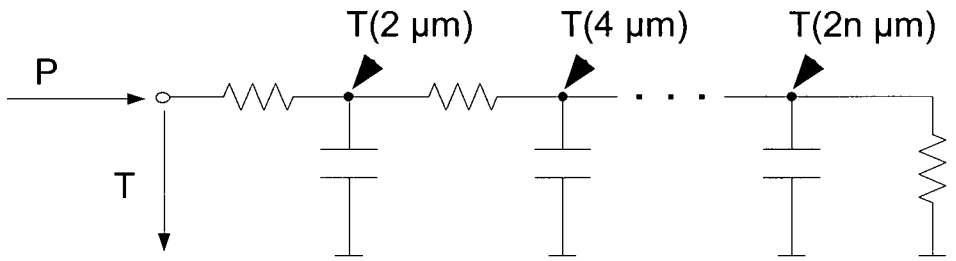

Fig 3.2: Representation of silicon surface as a RC network

In Fig. 3.2 the substrate is represented as an RC network. The temperature is measured at distances of 2μm, 4μm, 6μm and so on from the heat source. Voltage difference and current flow in an electrical circuit are considered analogous to temperature difference and power flow due to heat dissipation in a thermal circuit, respectively. An electrical simulator gathers information on power dissipation and couples it into the RC mesh that models the heat flow in the substrate [22]. The substrate temperature information is simultaneously coupled from the thermal solver to the electrical solver. Incorporating the coupled electrothermal effects into the circuit simulator requires that the differential heat equations (3.1 and 3.2) be solved.

$$J_u = -k\nabla T \qquad (3.1)$$

$$\rho c \partial T/\partial t + \nabla . J_u = 0 \qquad (3.2)$$

Where J_u is the heat flux density, T is the absolute temperature, k,ρ, and c are the thermal conductivity, density, and specific heat of the substrate material respectively. Simulators like Sabre solve the system of equations by iterating the system variables such that component of current flow into electrical node sums to zero (Kirchoff's current law) and also the components of power flow into the thermal node sum to zero (energy conservation).

The maximum power dissipated by three basic digital gates, i.e., an inverter, NAND and NOR in .18μm CMOS technology when their NMOS transistors are short-circuited to V_{dd} (3.3V) with a bridging resistance of 200 Ω[20] at 25°C are as shown in Table 3.1. The power dissipated depends on the topology of the circuit, the supply voltage, the technology used and the type of fault. All the dissipated power is converted to heat. The heat dissipated is thermally coupled to the silicon substrate and causes an increase in temperature in the region adjacent to the heat source. The heat flow through the substrate due to a device dissipating power was simulated using a RC network model [21], extracted by using the finite difference method [22].

Table 3.2, shows a set of data for the transient simulation of the temperature increase at different distances from a 16μm/1μm NMOS transistor, in .18μm CMOS technology at V_{dd} = 3.3V. The transistor dissipates 13.8mW of power. This power is applied as a pulse (Time period=50μs, Duty cycle=50%) to the RC network. The data shows the variation of the temperature of the silicon substrate due to the heat source.

Digital Circuit	Sizes (W/L)	Power (Steady state, W)	Power (Fault, W)
Inverter	NMOS=16μm/1μm PMOS=32μm/1μm	$3*10^{-12}$	$13.80*10^{-03}$
NAND	NMOS=16μm/1μm PMOS=16μm/1μm	$68*10^{-09}$	$7.80*10^{-03}$
NOR	NMOS=16μm/1μm PMOS=64μm/1μm	$116*10^{-09}$	$13.80*10^{-03}$

Table 3.1: Power dissipation of basic CMOS gates in 0.18μm CMOS

Distance (μm)	Temperature Increase (°C)
2	3.28
4	2.24
6	1.65
10	1.12
50	0.13
100	0.02
200	$76*10^{-6}$

Table 3.2: Temperature increase at various distances from heat source

3.3 Effect of Faults on Specific CUT

We studied the case of heat dissipation using a specific CUT in order to understand the temperature changes which occur when there is a short circuit fault. A CMOS operational

amplifier was simulated, designed, and fabricated in CMOS .18μm technology, and faults were induced in the operational amplifier. The operational amplifier was chosen to be the CUT for our experiment as its thermal characteristics had been studied as part of our research effort at UBC [23]. The fault free and the faulty case were analyzed and studied.

3.3.1 Operational amplifier design and specifications

A two-stage differential input, single output operational amplifier was designed. Figure 3.3, shows the designed operational amplifier. The operational amplifier had the following specifications:

Bandwidth: 10 MHz

Slew Rate: 20 V/μs

Common Mode Range: 1.4V- 1.9V

Common Mode Rejection Ratio: 80 dB

Gain: 83 dB

The first step of the design involved choosing the device length for the transistors in the operational amplifier and was chosen to be 1μm. This allows for the determination of the channel length parameter λ. After this the determination of the compensation capacitance is done using the output capacitance attached to the operational amplifier output. In our case the output capacitance was taken to be 5pF and the compensation capacitance was calculated to be 1.2pF for a gain phase margin of 60°. The value of the widths of the MOS transistors used in the operational amplifier were calculated in accordance to the specifications of the operational amplifier to be designed.

Transistor No.	Width
M1	16μm
M2	16μm
M3	1μm
M4	1μm
M5	35μm
M6	28μm
M7	24μm
M8	5μm
M9	18μm
M10	1μm
M11	1μm

Table 3.3: Widths of transistors in operational amplifier

The transistor sizes were selected after the Spice simulations were conducted and a layout of the circuit was done.

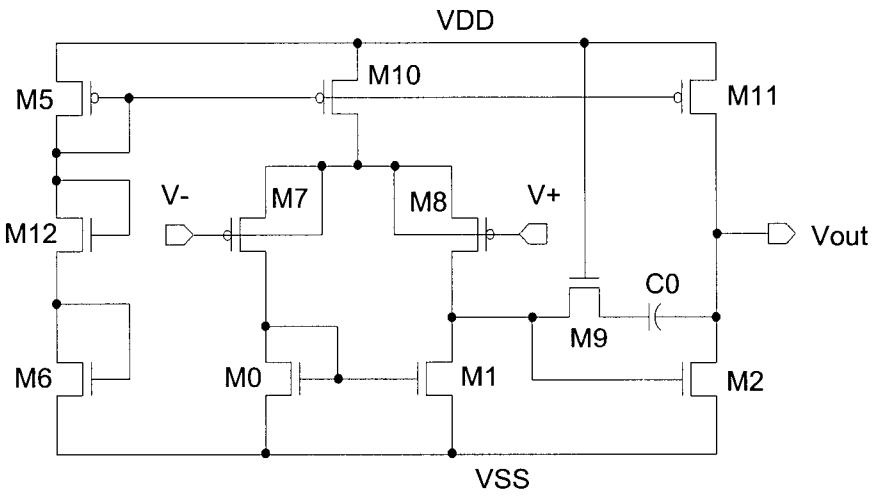

Fig 3.3: Schematic of the designed operational amplifier

3.3.2 Methodology

An operational amplifier was taken to be the circuit under test and its thermal properties were investigated. The power absorbed by the operational amplifier in its faulty and fault free states was recorded. The faults which were studied included short circuit bridging faults, short circuit node to node and node to power supply faults were investigated. The thermal mapping of the circuit is done by mapping the power consumed by each element, i.e., the MOS transistor, as it travels towards the silicon surface and the boundaries of the chip die. The test sensor determines if there is a fault in a given location by comparing the ambient temperature at a given place with its temperature in a fault free state. The sensors are placed at either the hottest regions on the chip surface and/or by placing them in places of critical importance and in places where there is a maximum probability of defects.

3.3.3 Power Calculation

The power consumed by the MOS transistor was extracted using Spectre, the simulator under the environment of Cadence Analog Environment. In Analog Artist, it can be

automatically done by saving all the current and all the node voltages of the circuit. In order to obtain the instantaneous power of a MOS transistor, the current through the transistor is multiplied with the potential difference between the source and the drain terminals. Hence, we have :

$$P_{MOS}(t) = I_S(t) * [V_S(t) - V_D(t)] \qquad (3.3)$$

where $P_{MOS}(t)$ is the power consumed by the MOS transistor at a given time, $I_S(t)$ is the current through its source, $V_S(t)$ is the voltage of the source at a given time, $V_D(t)$ is the voltage of the drain at a given time.

Obtaining the average power of a transistor of the operational amplifier is theoretically very simple. For the case where there is a constant difference in the voltage applied to the transistors M7 and M8 of the operational amplifier, the power consumed is equal to the product of the supply voltage and the sum of the currents flowing in through the various branches of the operational amplifier. For the case where the input voltage at the transistors M7 and M8 is a periodically varying signal the power of each transistor is calculated simply by dividing the instantaneous power, or the power spectral density, over one time period of oscillation. In other words,

$$P_{ave} = \frac{1}{(T_2 - T_1)} \cdot \int_{T_1}^{T_2} [P(t) * t] \qquad (3.4)$$

where P_{ave} is the average power consumed by the transistor, and $(T2\text{-}T1)$ is the time for one period of oscillation.

In the Cadence simulation environment, in order to determine the average power of all transistors, when the input signal is periodically varying, Analog Artist needs to know the exact start and stop simulation times. The spectral density of each transistor is different, and hence the periods of the function are also different. Thus, determining the start and stop simulation time for one cycle of every transistor requires multiple simulations of getting one average power value at a time, making the simulations very tedious and extremely inefficient. As an alternative, we can approximate the average power by integrating the power density over a long period of time. The time window used was 10μs. This was because the operational amplifier had a cut off frequency of 10 MHz and hence 10μs is equivalent to 100 oscillation periods of the operational amplifier.

$$P_{ave} = \frac{1}{T_{long}} \cdot \int_{0}^{T_{long}} [P(t) * t] = \frac{1}{10\mu s} \cdot \int_{0}^{10\mu s} [P(t) * t] \qquad (3.5)$$

Thus, although the power is averaged over a much longer period of time, multiple simulations do not have to be performed to determine the power of each transistor.

3.4 Operational Amplifier: Discussion and Results

The temperature of the operational amplifier is recorded in the fault-free state and in the faulty state under normal operating conditions. The operational amplifier is connected in the voltage follower configuration as shown in Fig 3.4. The simulation results that are shown are part of the combined work done by Lungwai et. all [30]. A DC analysis was performed, sweeping the input voltage, *Vin*, from 0 to 3.3V.

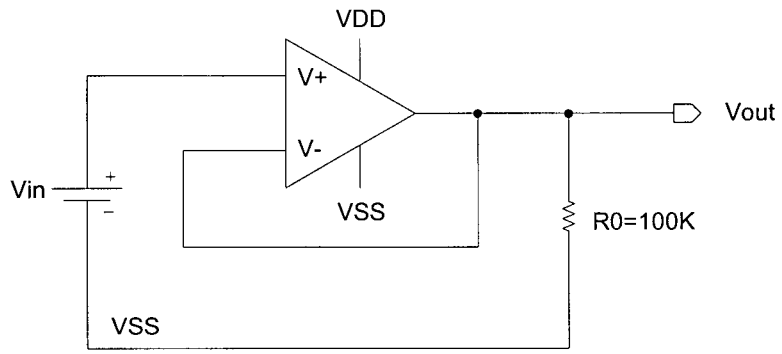

Fig 3.4. Voltage Follower Configuration

Four points around the CUT were chosen and the surface temperature recorded at these specified points. Fig 3.5 displays four points around the layout of the operational amplifier. Points P_1 and P_3 are located near the power supply lines, point P_2 was chosen randomly and point P_4 was chosen as it was near the capacitor. Because the temperature is highly dependent upon the position of sensing device, the distances between each transistor and the measuring point must be measured in the layout of the circuit. For example, the partial thermal resistances and heat capacitances of the heat flow path from each transistor dissipating power to point, P_1, contributes to the total temperature contribution at P_1. Hence the power consumed by each transistor is simulated, and fed into the RC network and the corresponding increase in temperature at point P_1 is found.

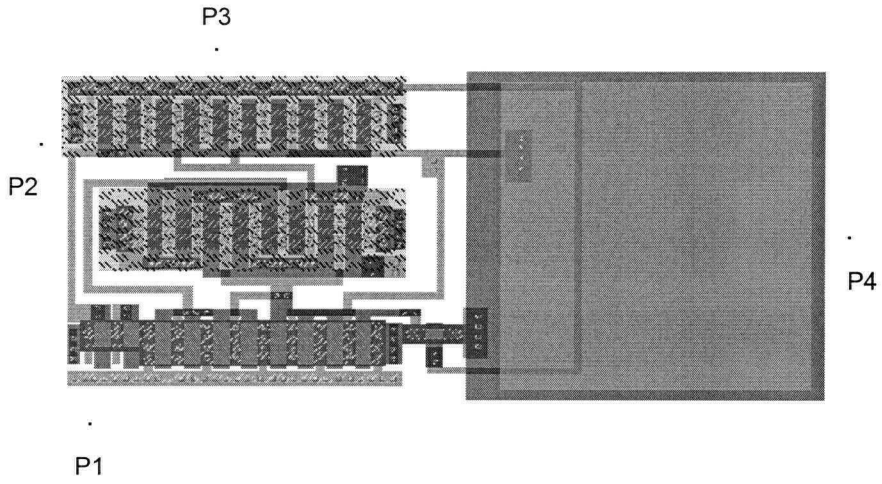

Fig 3.5. Points around the operational amplifier chosen for measuring the temperature change in a fault-free and faulty case

Fig 3.6 displays a plot of the temperature change in a fault-free circuit at the four different points for sweeping the input voltage of transistors M7 and M8 from 0 to 3.3V. At all of these positions, it shows a decrease in temperature with increasing *Vin*.

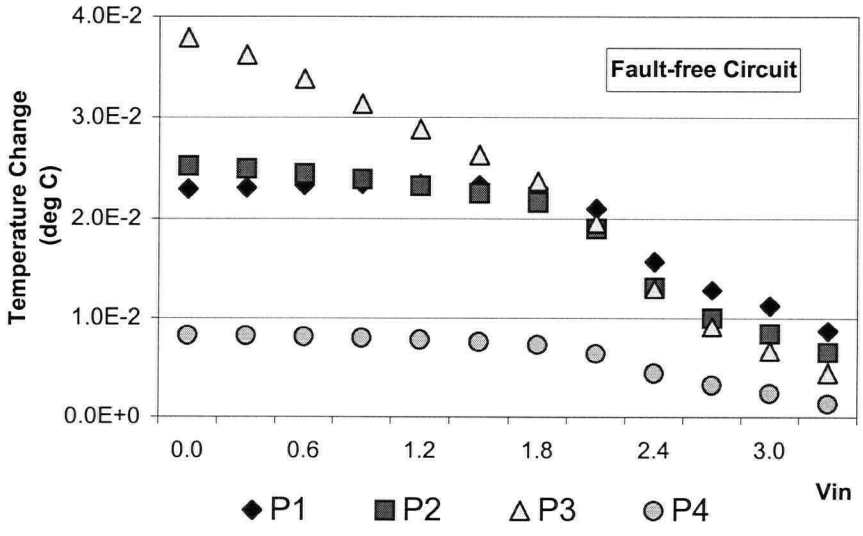

Fig 3.6: Temperature computed at points P1, P2, P3, and P4 as a function of Vin

The study focussed on node to node, node to power supply and node to ground bridging faults. For this reason the three faults, *R1*, *R2*, *R3*, shown in Fig 3.7 were investigated.

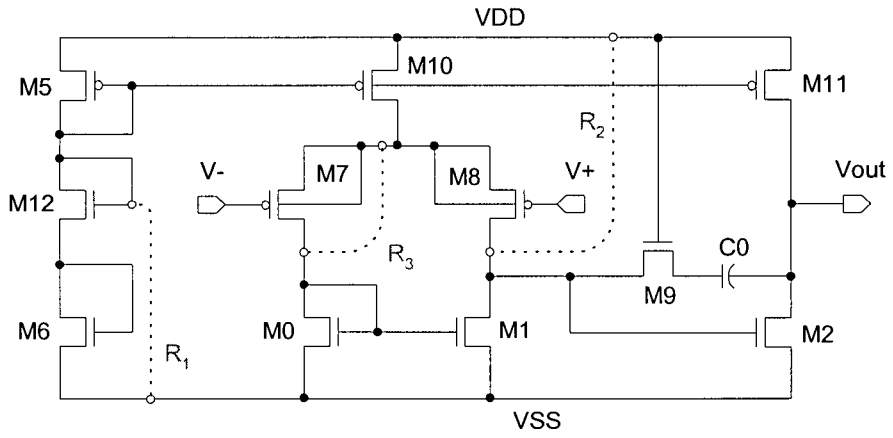

Fig 3.7: Faults injected into the circuit

The R1 is a node to ground fault, R2 is a node to power supply fault, and R3 is node to node fault. Fig 3.8 presents the simulation results due to these bridge faults at point P1. The bar graph shows the relative temperature difference between the faulty and fault-free case. For example, the relative variation for an input voltage of 0 Volts at point P1, due to fault R1 is 0.59° C. That is, the temperature above the ambient in a fault free case at point P1 was 0.23° C but when fault due to R1 was introduced it rose to 0.82° C.

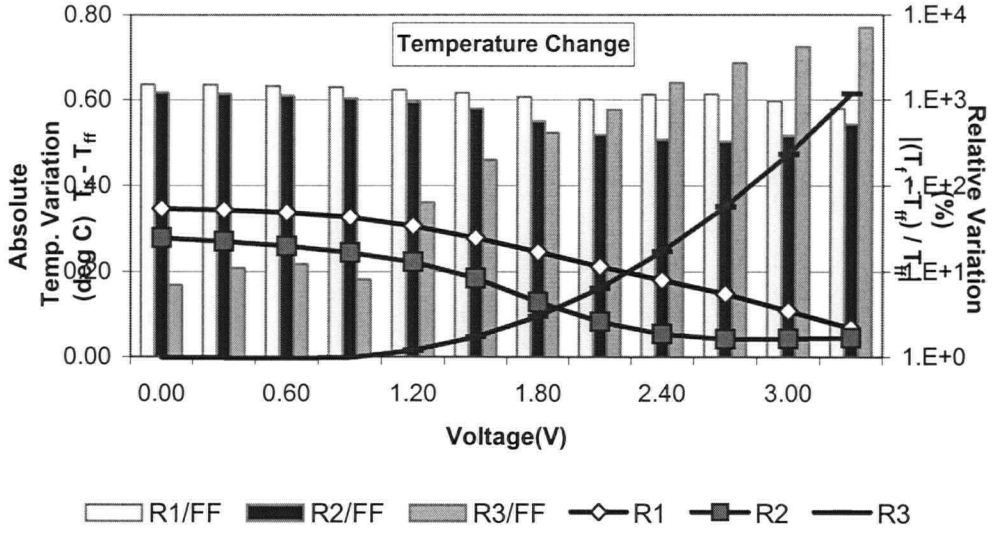

Fig 3.8: Temperature variation between the faulty cases and the fault free at P1

The line graph shows the relative variation in percentage terms. For point P1 the increase in temperature is 120% due to fault R1 as compared to the fault-free case. The simulation results show the changes in the temperature of the silicon substrate caused by these faults. If a thermal sensor, which can detect these changes in temperature, is placed in the locality of these faults, it shows the presence of these faults.

Chapter 4

Differential Thermal Sensors

This chapter deals with introduction to the concept of differential thermal testing, the differential sensors that were designed and the results obtained from testing one of the fabricated sensors.

4.1 Effect of temperature on mobility and threshold voltage

The current through a CMOS transistor in saturation mode be based on the Square Law model given by [29]:

$$I_{ds} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{gs} - V_t\right)^2 \qquad (4.1)$$

where μ is the carrier mobility, V_t is the threshold voltage, W is the width, and L be the length of the MOS device, V_{gs} is the gate to source voltage of the transistor, and C_{ox} is the gate oxide capacitance per unit area The short channel effects assume significance at transistor lengths of 0.5μm and below. In order to avoid these effects, the minimum length of each transistor used in the temperature sensors was 1.4μm. Hence the use of quadratic model to describe the current flow through the transistor can be assumed to be valid. As the temperature across the silicon die changes, the mobility and the threshold voltage parameters of the MOS transistor are affected.

The temperature dependence of mobility of the majority charge carrier in a MOS transistor is given by the equation [25]:

$$\mu(T) = \mu(T_0) \cdot (T / T_0)^{\alpha_\mu} \qquad (4.2)$$

The parameter α_μ is independent of temperature and usually set to -1.5[]. The rate of change of mobility with temperature is given by:

$$\partial\mu(T) / \partial T = \mu(T_0) \cdot \alpha_\mu \cdot (T / T_0)^{\alpha_\mu} / T$$

$$\partial\mu(T) / \partial T = \mu(T) \cdot \alpha_\mu / T \qquad (4.3)$$

From Equation 4.3, the mobility of the majority charge carried decreases with an increase in temperature. The threshold voltage of a MOS transistor is given by the equation [30]

$$V_T = \phi_{ms} / T - Q_{ss} / C_{ox} + 2\phi_F + \Delta V_T(N_i) + \gamma(N_s, t_{ox}, L, W) \cdot \sqrt{(2\phi_F + V_0)} \quad (4.4)$$

where ϕ_{ms} is the contact potential between gate and substrate, Q_{ss} is the surface-state charge density per unit area, ϕ_F is the Fermi potential of substrate, $\Delta V_T(N_i)$ is the threshold shift owing to a channel implant N_i with depth d_i , γ is the body effect coefficient depending on the substrate doping N_s, t_{ox} is gate oxide thickness, L is the channel length, and width is W and

V_0 is the correction term for the threshold shift implant. [30] shows that the rate of change of threshold voltage with temperature is given by:

$$\partial V_T / \partial T = \phi_{ms} / T + 2\phi_F / T + \gamma / \sqrt{(2\phi_F + V_0)} \cdot \partial\phi_F / \partial T \qquad (4.5)$$

The temperature coefficient of the threshold voltage over a range of -100°C to 100°C is given by:

$$TCV_T = 1 / V_T \cdot \partial V_T / \partial T \qquad (4.6)$$

This threshold coefficient is used to determine the threshold voltage for a given temperature, which is given by [30]:

$$V_T(T) = V_T(T_0)[1 + TCV_T \cdot (T - T_0)] \qquad (4.7)$$

The temperature coefficient of the threshold voltage is a negative quantity and hence the value of threshold voltage decreases with an increase in temperature. At very low drain currents the decrease in threshold voltage dominates the change in drain current with temperature but at higher values of drain current the decrease in mobility dominates

Fig 4.1 is the simulation results using HSPICE, where the temperature of the NMOS device is swept from -100°C to 100°C. The graph shows four points of interests, at temperatures of -100°C, -33°C, 33°C and 100°C. For an NMOS transistor in 0.18μm technology for a value of V_{gs} around or below 1.4V, the higher the temperature the higher the value of the current of the NMOS device for a given value of V_{gs}. For values of V_{gs} above 1.4V, the opposite is true, i.e., the higher the temperature the lower the value of current through it.

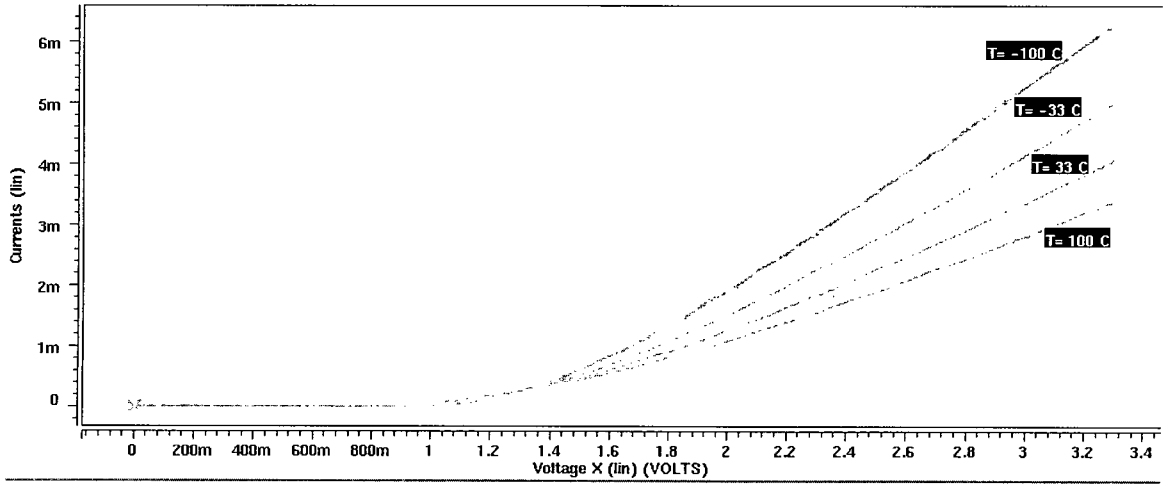

Fig 4.1: Variation of the MOS current with temperature

This also holds for a PMOS transistor and forms the basis of the differential thermal sensors that were designed for this study.

4.2 Differential Temperature Sensor Fundamentals

The goal of a differential temperature sensor is to detect thermal gradients that appear due to heat source activation in faulty circuits. The output voltage of the sensor can be written as [18]:

$$V_{out} = S_T \cdot (T_1 - T_2) + S_c \cdot \frac{(T_1 + T_2)}{2} \qquad (4.8)$$

where T_1 and T_2 are the temperature at two points of the silicon surface, S_T is the differential sensitivity to temperature and S_c is the common sensitivity to temperature. High values of S_T and low values of S_c provide high sensitivity to internal heat source activation and low sensitivity to ambient temperature changes. Different topologies for such sensors have been proposed targeting bipolar and BiCMOS technology [8]. The novelty of this work lies in being the first differential thermal sensor being implemented in CMOS technology. Three different types of differential sensors were designed. These are:

1) PMOS Cascoded Differential Thermal Sensor

2) NMOS Cascoded Differential Thermal Sensor

3) Differential amplifier-based Differential Thermal Sensor.

These three sensors represent a subset of the sensors that can be designed. The main idea that each of these sensor uses is the change in current through the MOS transistor when there is a change in temperature. This change in current is propagated to the output of the sensor.

4.3 PMOS Cascoded Differential Thermal Sensor

The sensor circuit in Fig. 4.2 consists of six PMOS transistors and four NMOS transistors with an input current source. The circuit designed consists of three parts: the sensor

transistor, bias circuitry, and a high impedance cascoded output. Transistor M4 is the sensing transistor. The other nine transistors form the biasing circuit. The circuit contains two NMOS current mirrors and three PMOS current mirrors. The current source determines the gate voltage of transistor M2 and hence, also the gate voltage of M1. The current through M4 and M7 is determined by the gate to source voltage of M2 as these transistors form a current mirror. The layout is done such that the sensing transistor is placed at a large distance from the bias circuitry, i.e., the biasing circuitry is thermally isolated from the sensor. A distance of 200μm was chosen as the RC network simulation showed a negligible heating effect on the bias circuitry by a heat source placed at such a distance. In our simulations, the sensing transistor was placed near the heat source. The gate to source voltage of the sensing transistor is independent of temperature and is a constant determined by the bias circuitry. The transistor M4 is biased such that it is always in saturation and thus given by Equation 4.1.

The V_{gs} value of the PMOS sensor is 2.3V and hence as the temperature increases the current through M4 increases. This increase in current through M4 results in a corresponding increase in current through M5 and consequently through M9. But the current through M7 is constant as it is determined by the gate voltage of M1, which remains a constant. Thus, at node V_{out}, a difference in current is caused due to the constant value of I_{d8} and the changing value of I_{d9}. Table 4.1, shows the simulated results when the temperature of M4 is increased by 1°C relative to the nominal temperature. The nominal temperature is 25°C and the input current is 25μA. The simulation results for the case where the temperature of all the transistors in the sensor are increased by 1°C are shown in Table 4.2.The layout of the sensor is shown in Fig 4.3. As explained above, transistor

M3 is placed at a distance of 200 um from the bias circuitry. The layout shows the placing of the transistor. The dimensions of the transistor are given in Appendix A.

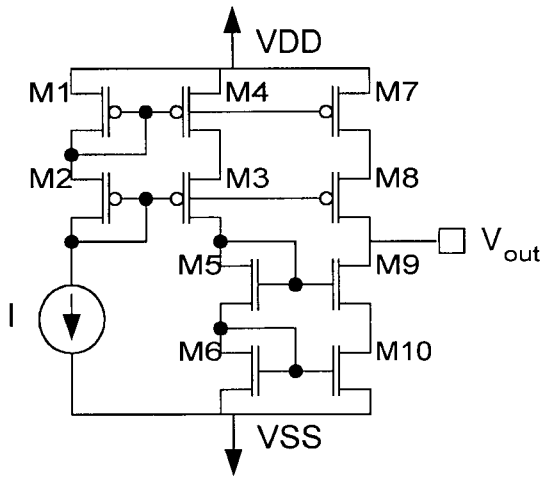

Fig 4.2: Schematic of the PMOS Cascode Thermal Sensor

The change in sensor output voltage caused by the change of temperature at M4 is given by:

$$\partial V(out)/\partial T = (I_{d8} - I_{d9})R_{out} \qquad 4.9$$

where R_{out} is the output resistance of the circuit at node V_{out} and I_{d8} and I_{d9} are the drain currents of transistors M8 and M9. Since I_{d8} is a constant and I_{d9} has increased, a large swing in the output voltage is caused due to the high output resistance of the cascoded output.

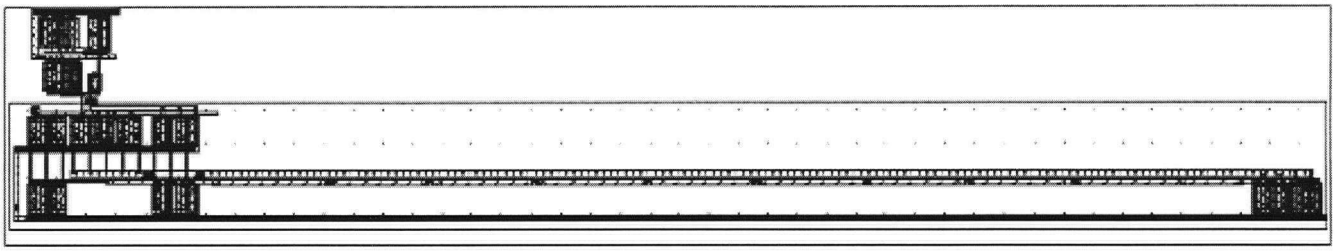

Fig 4.3: Layout of PMOS Cascode thermal sensor

Variable	Initial Value	Final Value	Change/°C
I_{d4}	24.97μA	25.13μA	.16μA
I_{d8}	24.98μA	25.00μA	.02μA
I_{d9}	24.77μA	24.90μA	.13μA
V_{out}	2.25V	1.13V	1.12V

Table 4.1: Temperature of M4 increased by 1°C at ambient temperature of 25°C

Variable	Initial Value	Final Value	Change/°C
I_{d4}	24.96μA	25.97μA	7.20nA
I_{d8}	24.99μA	24.98μA	.01μA
I_{d9}	24.77μA	24.78μA	8.00nA
V_{out}	2.21V	2.20V	10mV

Table 4.2: Temperature of all transistors increased by 1°C at ambient temperature of 25°C

Results

Our sensor has a differential voltage sensitivity [4] of 1.12V/°C, consumes at most 140μW of power in a 0.18μm CMOS technology for supply voltage of 3.3V at a temperature of 25°C. The layout area is 1600μm^2.

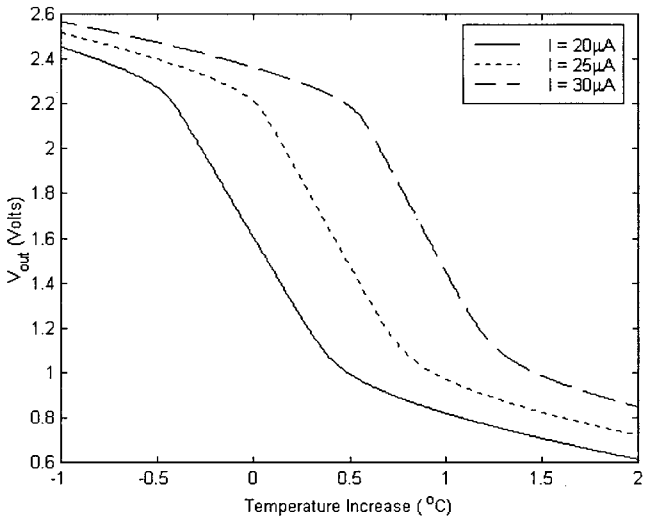

Fig 4.4: Output voltage variation of the differential sensor for different bias currents(I)

The high sensitivity of the sensor allows it to detect small increases in temperature. The differential current sensitivity of the sensing device (M4) is .16μA/°C and the common mode current sensitivity is 7.2nA/°C. Fig 4.4, shows the variation at the output node, V_{out}, for different input currents, I, applied to the sensor, as the temperature of sensing device is increasing. During the normal operation of the circuit under test (CUT), the local temperature may be higher than the ambient temperature of the entire chip. In order to compensate for this, the sensor can be biased at different current values. Thus, knowing the operating temperature of a normal CUT, we can dynamically bias the sensor by adjusting the input current. The sensor is biased at the edge of the triode and saturation region in

order to exploit the high gain of the sensor in the saturation region. This allows for maximum amplification of small changes in temperature occurring near the sensing device.

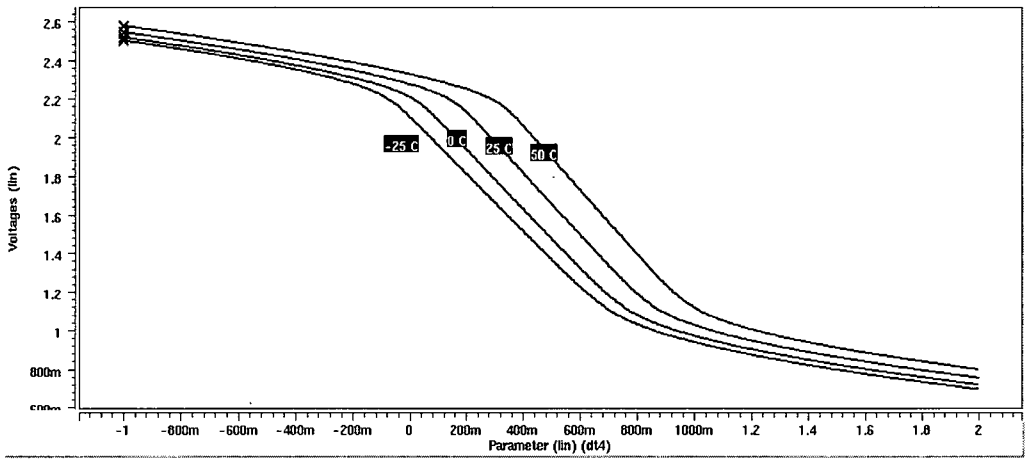

Fig 4.5: Variation of voltage sensitivity of sensor for different ambient temperature

Fig 4.5 shows the variation of the voltage sensitivity of the sensor for different ambient temperatures. Four random ambient temperature values of –25 °C , 0 °C , 25 ° C and 50 °C were taken for simulation. This graph shows that the changes in the ambient temperature cause a minimal change in the voltage sensitivity.

4.4 NMOS Cascode Thermal Sensor

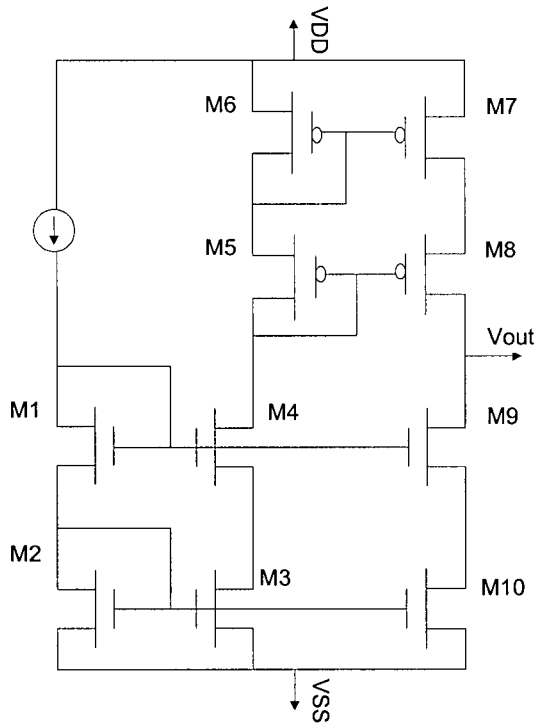

Fig 4.6: Schematic of our NMOS Cascode Thermal Sensor

The NMOS cascode thermal sensor is an inverted version of the PMOS cascode thermal sensor. As shown in Fig 4.6, the sensor circuit consists of 6 NMOS transistors and 4 PMOS transistors with an input current source. The circuit consists of three components: a sensor transistor, bias circuitry, and a high impedance cascoded output. The transistor M3 is the sensing transistor. The other nine transistors form the biasing circuit.

The circuit contains three NMOS current mirrors and two PMOS current mirrors. The current source determines the gate voltage of transistor M1 and hence, also the gate voltage of M2. The current through M3 and M10 is determined by the gate to source voltage of M2 as these transistors form a current mirror. The layout as shown in Fig.4.7 is done such that the sensing transistor, M3 is placed at a long distance from the bias circuitry i.e., the

biasing circuitry is thermally isolated from the sensor. The V_{gs} of the sensing transistor is independent of temperature and is a constant determined by the bias circuitry. The transistor M3 is biased such that it is always in saturation and the current through it is also given by Equation 4.1.

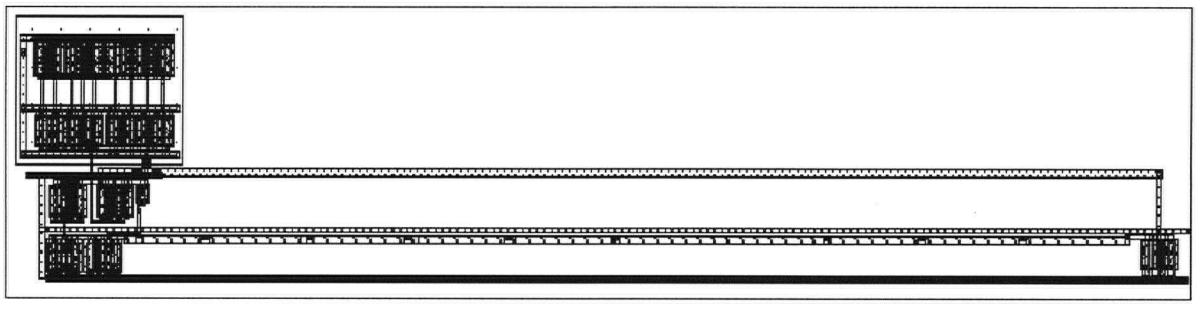

Fig 4.7: Layout of NMOS Thermal Cascode Sensor

As the temperature increases, the carrier mobility in device M3 drops due to increased thermal (lattice) scattering and its threshold voltage drops [12]. But since the transistor is in saturation, and hence the current through it is relatively high, the decrease in mobility has a much stronger effect and the current of the device decreases. This decrease in current through M3 results in a corresponding decrease in current through M5 and consequently through M8. But the current through M9 is a constant value as it is determined by the gate voltage of M1, which remains a constant. Thus, at node V_{out}, a difference in current is caused due to the constant value of I_{d8} and the changing value of I_{d9}. Table 4.3, shows the simulated results when the temperature of M3 is increased by 1°C relative to the nominal temperature. The nominal temperature is 25°C and the input current is 25μA. The simulation results for increasing the temperature of all the transistors in the sensor by 1°C are shown in Table 4.4.

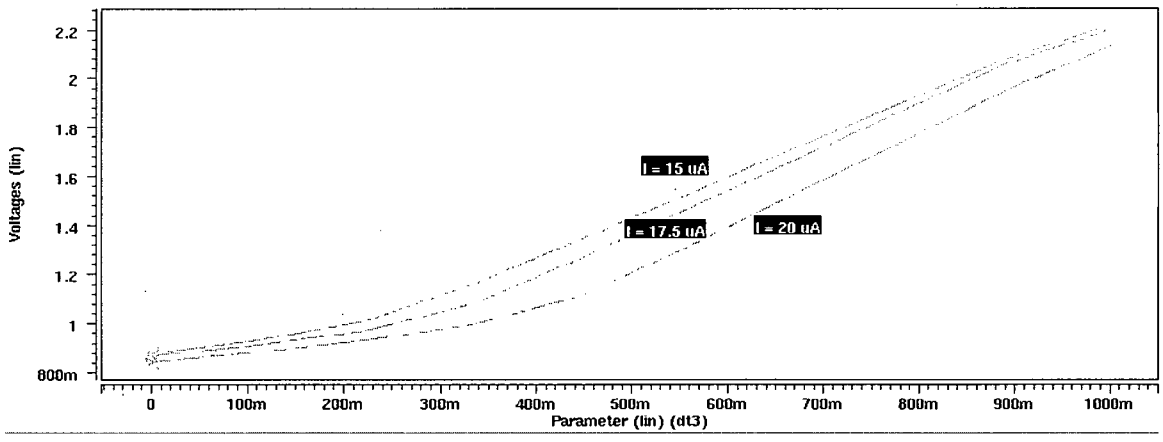

Fig 4.8: Output voltage variation of the NMOS sensor for different bias currents (I)

Variable	Initial Value	Final Value	ΔVariable/°C
I_{d3}	14.63μA	14.80μA	0.16 μA/°C
I_{d8}	14.63μA	14.80μA	0.16 μA/°C
I_{d9}	14.54μA	14.57μA	0.03 μA/°C
V_{out}	0.85V	2.21V	1.34 V/°C

Table 4.3: Temperature of M3 increased by 1°C from ambient temperature of 25°C

Variable	Initial Value	Final Value	ΔVariable/°C
I_{d3}	1463.18nA	1463.28nA	1 nA/°C
I_{d8}	1463.18nA	1463.28μA	1 nA/°C
I_{d9}	1454.43μA	1454.50nA	.7 nA/°C
V_{out}	0.877 V	0.875 V	2.0 mV

Table 4.4: Temperature of all transistors increased by 1°C from ambient temperature of 25°C

Results

Our sensor has a differential voltage sensitivity of 1.34 V/°C, consumes at most 110μW of power in 0.18μm CMOS technology for supply voltage of 3.3V at a temperature of 25°C. The layout area is 1520μm^2. The differential current sensitivity of the sensing device (M3) is .1667μA/°C and the common mode current sensitivity of the sensor is 1nA/°C. Fig. 4.8 shows the variation at the output node, V_{out}, for different input currents, I, applied to the sensor, as the temperature of sensing device is increasing. The sensitivity of the sensor for the current values of 15μA, 17.5μA and 20μA are 1.312V, 1.34V and 1.32V respectively. Fig. 4.9 shows the effect on the differential sensitivity of the sensor for ambient temperatures of the silicon surface of -25 °C, 0 °C, 25°C, 50 °C. We see that despite changes in the ambient temperature differential sensitivity of the sensor remains nearly constant and hence the sensor performs its function of detecting the variations of temperature from the ambient value.

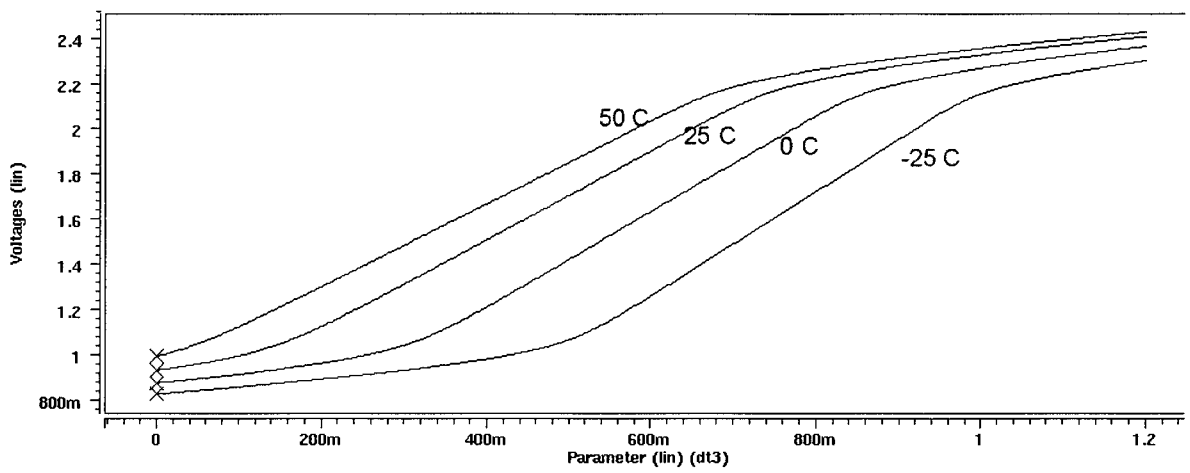

Fig 4.9: Variation of output voltage of sensor with variation in ambient temperature

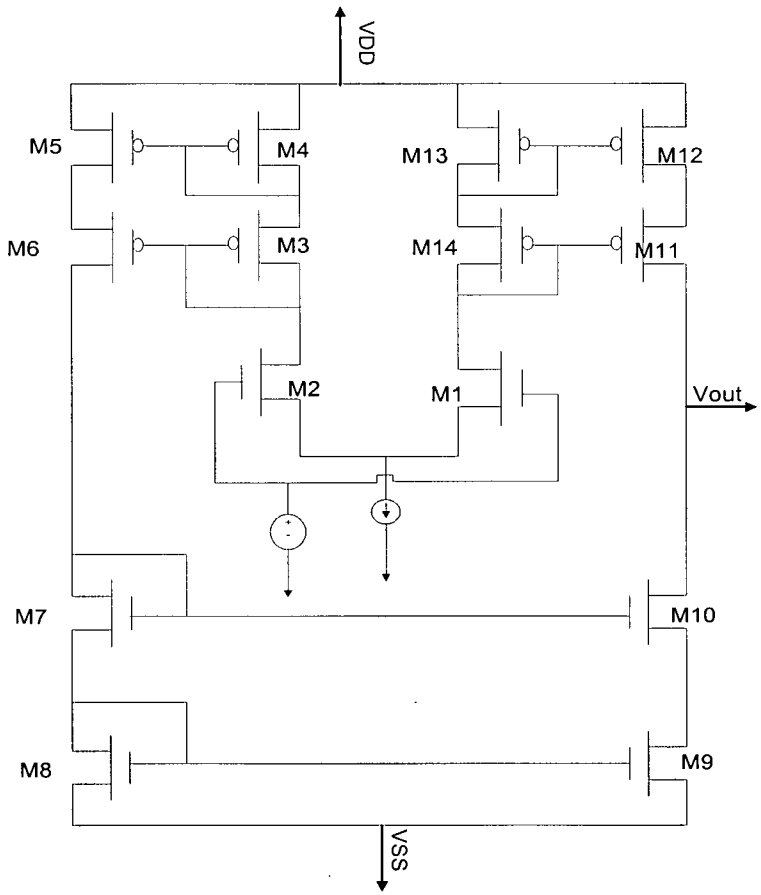

Fig 4.10: Schematic of Differential Amplifier Thermal Sensor

4.5 CMOS Differential Amplifier Thermal Sensor

This thermal sensor consists of a differential amplifier, a current source, a voltage source, and a cascoded gain stage. As shown in Fig 4.10, the total number of transistors is fourteen. Two of these transistors, M1 and M2, form a source coupled differential pair, and the other twelve are connected in a current mirror formation. The output part of the sensor is formed by four cascoded transistors and thus provides a very high output impedance to the sensor.

4.5.1 Differential Amplifier

A simple source coupled pair consists of two transistors M1 and M2 as shown in the Fig 4.11. The two transistors are of equal sizes, so that $\beta 1 = \beta 2 = \beta$, where β is the trans-conductance parameter of the transistor. Adding the dc and ac currents at the sources of M1 and M2, yields

$$I_{SS} = i_{D1} + i_{D2} \qquad (4.10)$$

Where i_{D1} is the drain current of M1 and i_{D2} is drain current of M2.

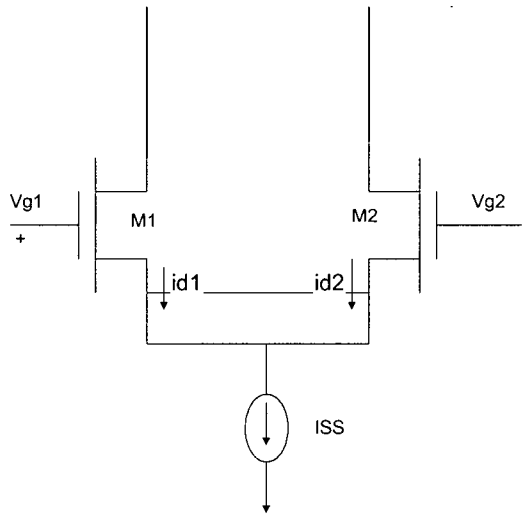

Fig 4.11: A simple source coupled differential amplifier

The voltage applied at the gate of M1 and M2 is v_{I1} and v_{I2} respectively and their voltage difference can be written as

$$v_{DI} = v_{I1} - v_{I2} = v_{GS1} - v_{GS2} \qquad (4.11)$$

When the gate of M2 is connected to ground, i.e., $v_{I2} = 0$, and M1 is connected to VDD, v_{I1}= VDD, that is, $v_{I1} = v_{D1}$, then M2 is off and M1 conducts the current I_{SS} (i.e., $I_{D1} = i_{D1} = I_{SS}$). If for linear operation, M1 and M2, are required to remain in saturation region, then

the point at which the input voltage turns M2 off is the same point at which all of I_{SS} begins to flow in M1.

4.5.2 Common Mode Range Voltage

When a common mode signal is applied to the gates of the transistors M1 and M2, a maximum and minimum voltage exists in which the transistors fail to stay in saturation region. This range of common input signals is known as common mode range (CMR). Thus, when the range of voltage is between the CMR, the transistors of the differential amplifier remain in saturation. The objective of a differential amplifier is to amplify only the difference between two potentials regardless of the common-mode values [26]. This objective is exploited in the way the differential thermal sensor has been designed, where both the gates of the differential amplifier are supplied a common voltage

4.5.3 Working of the sensor

The two transistors of the differential amplifier are laid out on chip in such a way that they are placed far apart from each other but are individually placed close to the circuit under tests as shown in the block diagram in Fig 4.12.

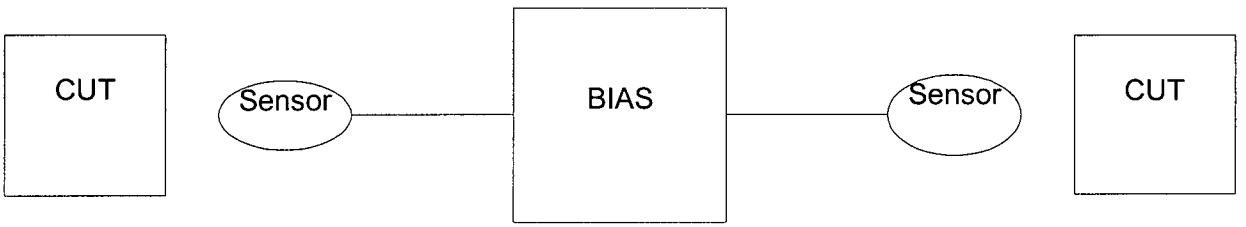

Fig 4.12: Block diagram of the differential amplifier thermal sensor

The two transistors M1 and M2, both act as the sensing transistors for this sensor. Thus, both of them can be placed separately in possible fault locations. This is shown in Fig 4.12. If we assume that the silicon surface temperature is T, and a heat source is activated, the temperature of the CMOS transistors is increased and is given by:

T1= T + ΔT1 for MOS M1

T2= T + ΔT2 for MOS M2

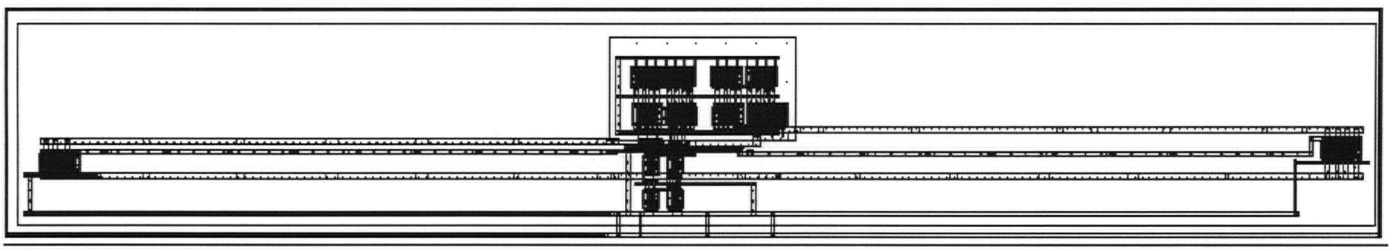

Fig 4.13: Layout of differential thermal amplifier sensor

Repeating Equation 4.8, the output voltage of the sensor is given by

$$V_{out} = S_T \cdot (T_1 - T_2) + S_c \cdot \frac{(T_1 + T_2)}{2}$$

Now replacing the value of T1 and T2 in the above equation we get

$$\Delta V_{out} = S_{dt} \cdot (\Delta T1 - \Delta T2) + S_{ct} \cdot (T + (\Delta T1 + \Delta T2)/2) \quad (4.12)$$

The placement of the temperature transducers must be such that the value of (ΔT1-ΔT2) be different from zero when the internal heat sources are activated.

In the normal working of a differential amplifier, a small difference in gate voltages of the source coupled transistors M1 and M2 results in a different value of current flowing through the two transistors. This difference in current is converted into a larger difference

of voltage by the high output impedance of the cascoded current mirrors connected to the differential amplifiers. In this case, the V_{gs} of the transistors M1 and M2 are the same and hence the current flowing through them is equal as the two transistors are sized equal. As we have seen in the previous discussion in Section 4.1, as the temperature near one transistor increases, the current through it increases or decreases depending on the V_{gs} value of the transistor. In our case for the NMOS transistors the value of V_{gs} is less than 1V and hence the current through the transistors increases with an increase in temperature. When there is a short circuit fault in the circuit under test (CUT), it may cause a rise in the temperature near the CUT. This rise in temperature is then propagated to the sensing transistor, which say in our case is M1, and there is a consequent decrease in current through the other transistor differential amplifier transistor M2, as the total sum of current through the two transistors is constant. This increase in current through M1 is then propagated to transistors M3 and M4, and is mirrored to transistors M5 and M6, which then propagate this to the output transistors M10 and M9 via the current mirrors of M7 and M8 respectively. Similarly, the decrease in current through M2 is then propagated to the transistors M11 and M12. Thus, at the node V_{out}, a difference in current is produced between the current that sources out from transistor M11 and the current that sinks into transistor M10. Since, the output transistors M12, M11, M10, and M9 are in cascode, the output impedance at node V_{out} is very high. Since I_{d11} has decreased and I_{d10} has increased, a large swing in the output voltage is caused due to the high output resistance of the cascoded output.

Variable	Initial Value	Final Value	Change/°C
I_{d2}	20.00μA	20.14μA	0.14μA
I_{d10}	14.91μA	19.80μA	0.11μA
I_{d11}	20.01μA	20.07μA	0.06μA
I_{d1}	20.00μA	19.86μA	0.14μA
V_{out}	0.96V	2.40V	1.40V

Table 4.5: Increasing the temperature of M1 by 1°C at ambient temperature of 25°C

Variable	Initial Value	Final Value	Change/°C
I_{d2}	20.00μA	20.00μA	0.00A
I_{d10}	19.91μA	19.91μA	0.00A
I_{d11}	20.01μA	20.02μA	0.01μA
I_{d1}	20.00μA	20.00μA	0.00μA
V_{out}	0.96V	0.95V	0.01V

Table 4.6: Increasing the temperature of all transistors by 1°C at ambient temperature of 25°C

Fig 4.14, shows the variation of the output voltage due to a defect in CUT1 causing a temperature rise in transistor M1.

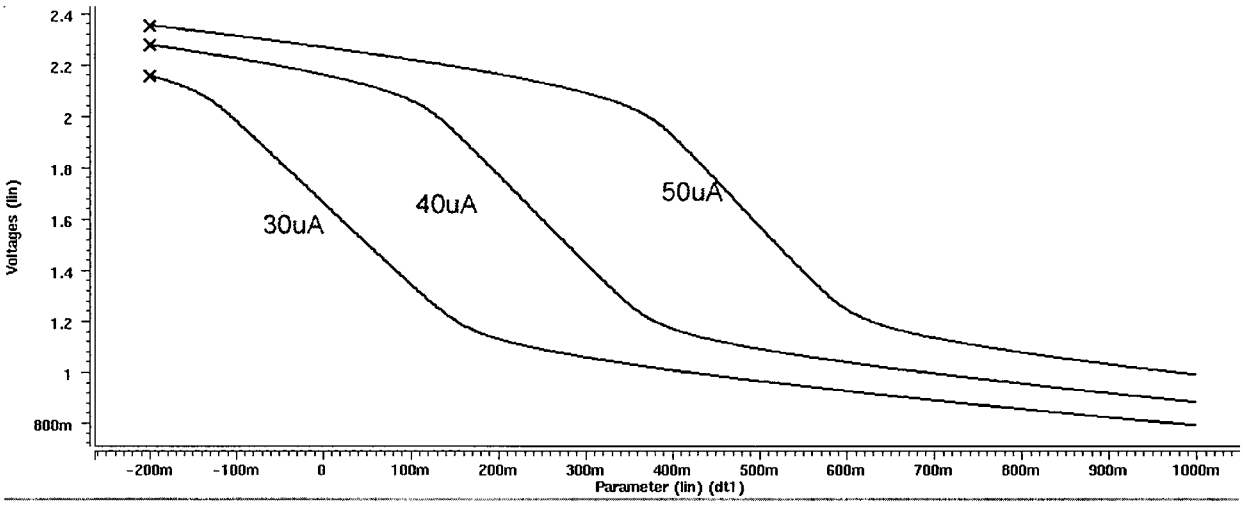

Fig 4.14: Output voltage variation of the differential sensor for different bias currents (I)

Results

Our sensor has a differential voltage sensitivity [4] of 1.40V/°C, consumes at most 140μW of power in a 0.18μm CMOS technology for supply voltage of 3.3V at a temperature of 25°C. The layout area is 2320μm^2. The advantage of using this structure over the thermal cascode sensors is that two transistors can be used as transducers in this structure whereas in the other sensors we can use only transistor as a transducer. This effectively doubles up the area covered by the sensor, albeit with a smaller area overhead. The differential structure also provides higher noise sensitivity, as the common noise at the gate of the two transistors is not amplified.

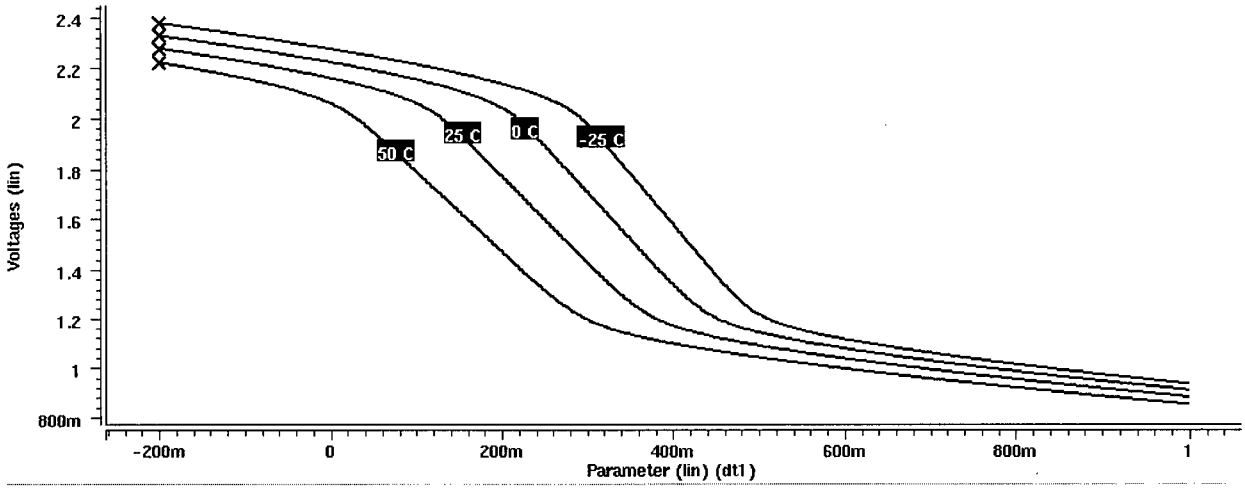

Fig 4.15: Variation of output voltage with variation in ambient temperature

4.6 Testing of designed sensor

The PMOS cascode temperature sensor shown in Fig 4.16, was fabricated in 0.18μm technology.

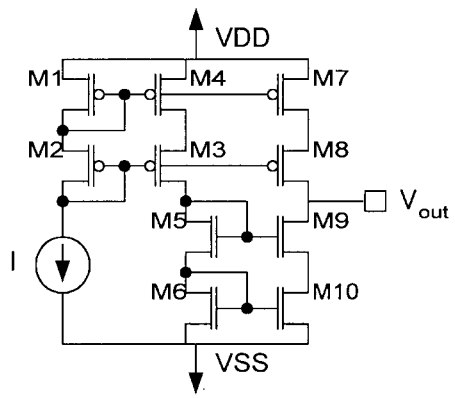

Fig 4.16: PMOS Cascode Temperature Sensor

The testing of the chip involved the comparison of the simulation results for the sensor and the chip measurements. Fig 4.17 shows the simulation results for the designed differential sensor, when a 10 MΩ probe is attached to the sensor output for different input currents. The designed sensor has a differential thermal sensitivity of 1.12 V/ °C. This implies that when the temperature around the sensing transistor changes by 1°C, the output voltage changes by 1.12 Volts.

The test setup used included an oscilloscope with an input impedance of 10 MΩ, a high precision digital multi-meter, a current source/sink, and a bread board. Two probes with impedance of 10 MΩ and 1 MΩ were used during the testing. The current source/sink was created using LM334, which is a three terminal device. The heat source was generated using a 16μm/1μm NMOS transistor connected in diode configuration.

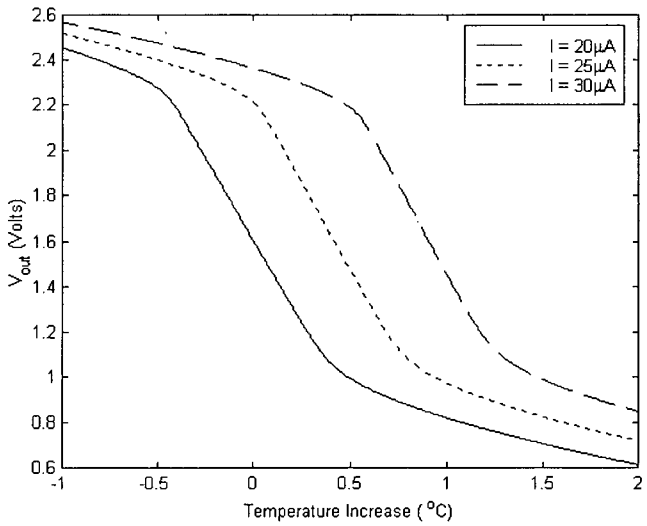

Fig 4.17: Output voltage variation of the differential sensor for different bias currents (I)

4.6.1 Test Setup

The test procedure involved the use of an external current source which could produce current values within the range of 5μA to 50μA. To do so, a three terminal current source/sink device, LM334, manufactured by National Semiconductors, was used. The device is a three terminal adjustable current source featuring 10,000:1 range in operating current, excellent voltage regulation and a wide dynamic current range of 1V to 40V [24]. Applications for the current source include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The main features are:

- Operates from 1V to 40V
- 0.02%/ V current regulation
- Programmable from 1μA to 40μA
- True 2 terminal operation

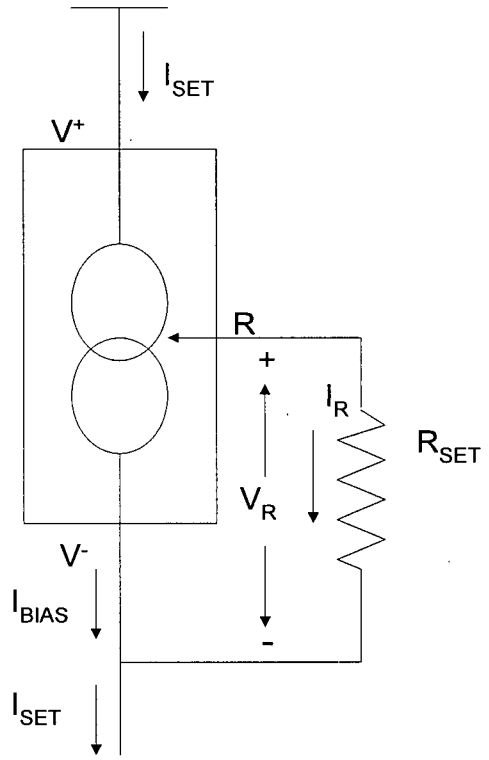

Fig 4.18 Block diagram of LM 334.

The total current through the LM334, is the sum of the current through R_{SET} (I_R) and the LM334's bias current (I_{BIAS}). The final current through the current source is calculated and simplified to [24]:

$$I_{SET} = (V_R/R_{SET})*1.059 = 227/R_{SET}\ \mu V/°K \qquad (4.13)$$

The first stage of testing involved the biasing of the sensing circuitry at the edge of the saturation region, so that as we increase the temperature the sensor enters the region of highest gain, and we can obtain the highest possible change in output voltage for a given change in temperature. For detecting this biasing point, current through the current source is swept and the voltage variation is noticed. The region of the highest slope is the saturation region of the sensor.

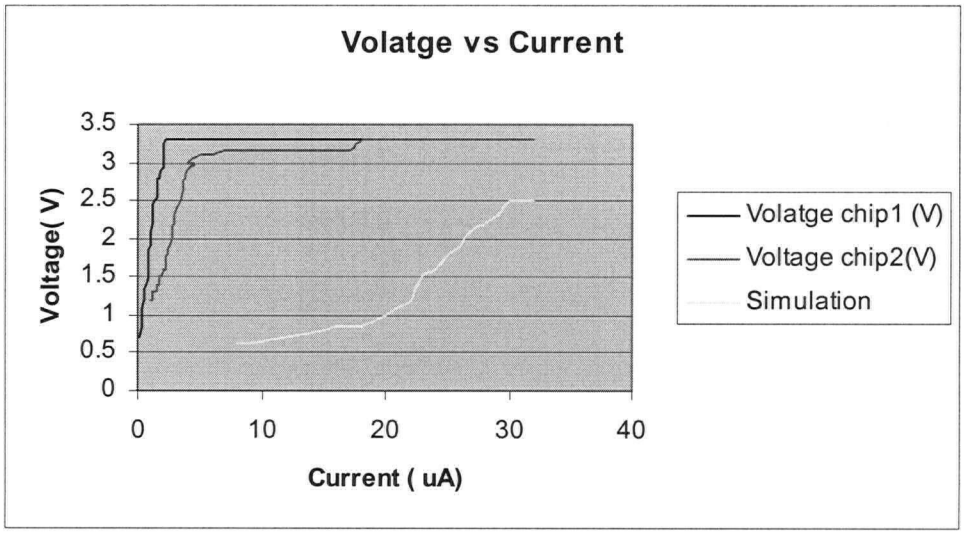

Fig 4.19: Voltage vs Current variation for a 10 MΩ probe.

A 10 MΩ resistance is placed at the output of the sensor. In Fig 4.19, we see the simulation results of the sensor showing a high sensitivity from 20μA to 25μA, and simulations show that the PMOS sensor must be biased at 25μA, to cause a maximum rate of change in voltage. On-chip measurements of sweeping the current of the sensor are also shown in the Fig 4.19. The measured results for two chips show the maximum rate of voltage change for one chip to be from 1μA to 2.5μA and for another to be from 3μA to 4.3μA. These changes imply higher output impedance at the output node, as compared to the simulation results. It also shows that the bandwidth of the current sweep is reduced by around 230 % for chip1 and around 284 % for chip2. It further shows a change in the region where the chip goes into saturation as around 1000% for chip1 and chip 2.

To understand this we must look into the cascode configuration of the sensor. Fig 4.20 shows the cascode structure.

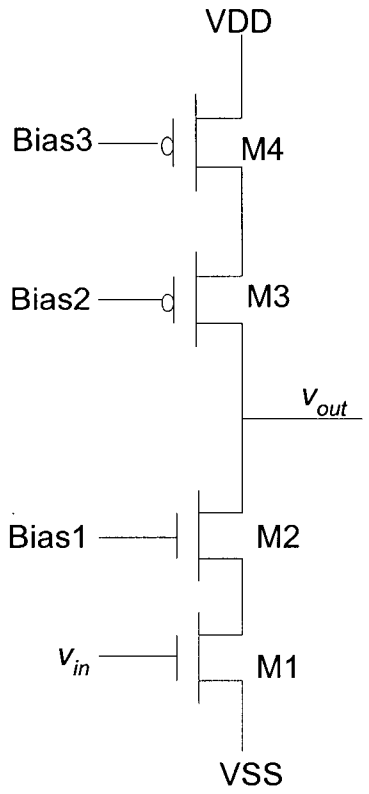

Fig 4.20: Cascode configuration of the output

The minimum output voltage that will keep all the transistors in saturation will be limited by the point at which M2 becomes unsaturated. This occurs when

$V_{GS2}-V_{THN2}=V_{DS2}$

where V_{GS2} is the gate to source voltage of M2, V_{THN2} is the threshold voltage of M2 and V_{DS2} is the drain to source voltage of M2. M2 becomes saturated before M1 because the impedance of the output node is much higher than the impedance at the drain of M1 and thus the voltage at the output will be decreasing at a much faster rate than the voltage at drain of M1. This is equivalent to saying that since the gain from the input to output is much higher than the gain from the input to the drain of M1, as the input voltage rises, the output voltage decreases faster than that at the drain of M1.

The maximum positive voltage that can appear at the output of the cascode while maintaining all the transistors in saturation will be limited by the point at which M3 becomes non-saturated. The maximum positive voltage occurs when

V_{SG3}- V_{THP3}=V_{SD3}

where V_{SG3} is the source to gate voltage of M3, V_{THP3} is the threshold voltage of M3, V_{SD3} is the source to drain voltage of M3. Expressed in an another way, this can be written as

$Vo(max) = V_{GG3}+V_{TH3}$

where Vo(max) is the maximum output voltage, V_{GG3} is the gate voltage of transistor M3, and V_{TH3} is the threshold voltage of transistor M3.

When a 10 MΩ probe is attached to the output of the cascode configuration, the rate of change of output voltage is much faster as compared to a smaller probe impedance. In Fig 4.19 as we increase input current supply, the bias voltage ,i.e., the gate voltage of M9 (V_{GG9})also increases. But at the same time the source voltage of M9 is also increasing due to increased input current supply. Hence, the overall increase in the gate to source voltage of M9 is minimal. But the increase in the threshold voltage of M9 causes an increase in the threshold voltage of M9 due to body effect phenomenon. Also process variations can cause an increase in the threshold voltage of M9. This phenomenon combined with body effect can make threshold voltage of transistor M9 to become higher than the gate source voltage of M9. And as a consequence transistor M9 enters cut-off region. As observed in Fig 4.19, the output of the sensor does not saturate to 2.4 V, as seen in the simulations, but it goes to 3.3 V. This is only possible if transistor M9 enters cut-off. So when we attach lower impedance probes to the output of the sensor, the same phenomenon should be observed but at a slightly lower rate. This hypothesis is validated by experimental observations.

From Fig 4.19 we see that the output of the sensor becomes saturates very fast and the output voltage reaches a high value very fast for very low value of input current. Thus M9 reaches cut off stage very fast and the sensor output becomes stuck at 3.3V. The widths of the NMOS transistors M9 and M10 are 2μm and 16μm and width of the PMOS transistors M7 and M8 are 20μm each. This implies a higher impedance of the two NMOS transistors as compared to the PMOS transistors, but a decrease in width in the NMOS transistors, due to process variations, especially M9 would imply a much earlier saturation for these transistors as compared to what it would be if there was no change in their widths.

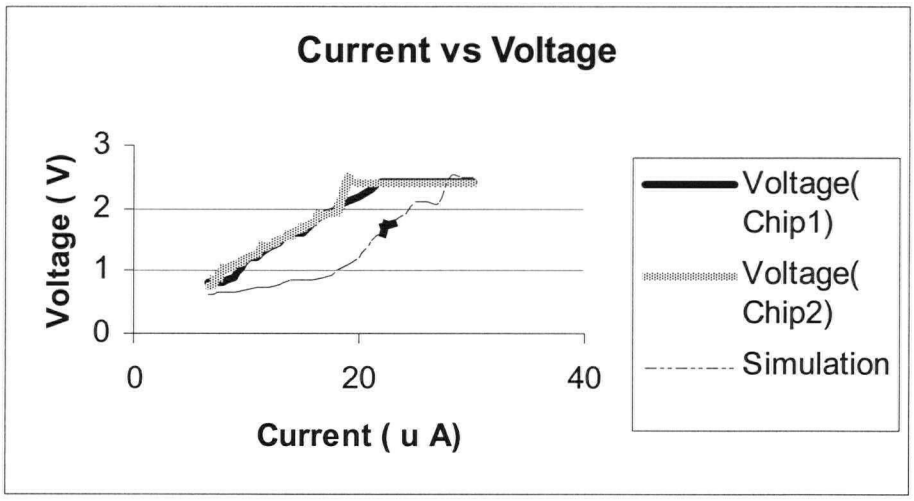

Fig 4.21: Voltage versus Current for a 1 Mega Ohm probe.

From Fig 4.21, we observe that the actual measurements for chip1 and chip2, have a steady voltage change from 10μA to 20μA, thus showing a much higher impedance than the designed output resistance of the sensor, which confirms the previous observation in Fig 4.19.

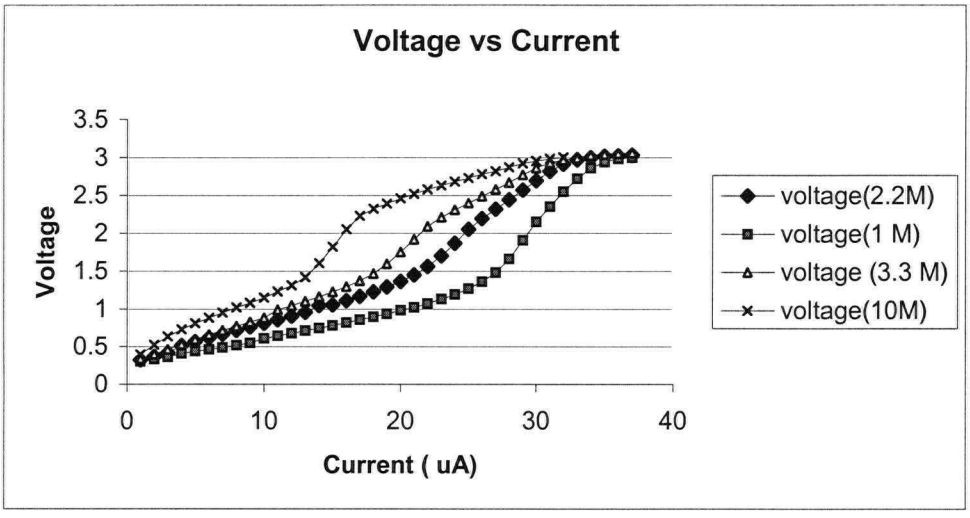

Fig 4.22: Simulation results showing the effects of attaching a 1, 2.2, 3.3,10 MΩ resistor to the sensor output.

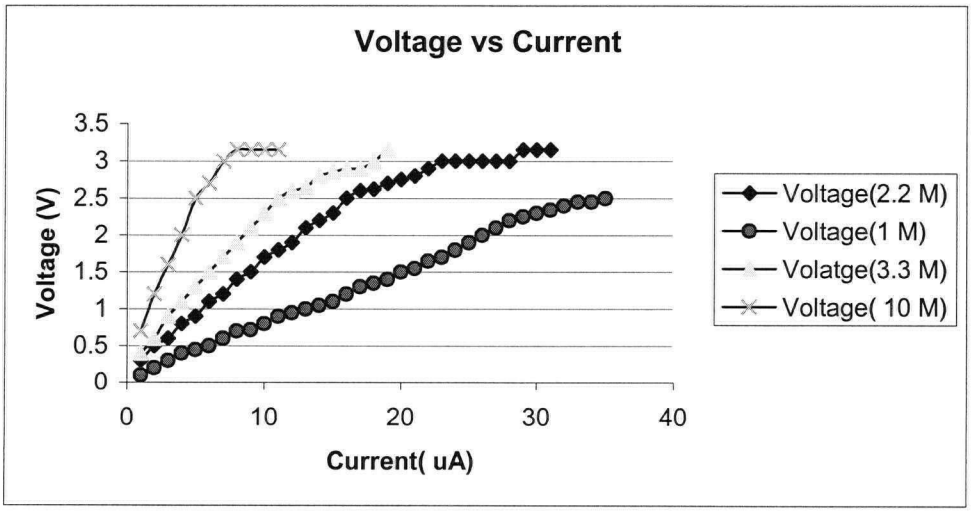

Fig 4.23: Chip results showing the effects of attaching a 1, 2.2, 3.3,10 MΩ resistor to the sensor output.

From Fig 4.22 and Fig 4.23, we see that the chip has a higher output than as was designed in the simulations. This again shows the effect of process variation and transistor mismatches on the designed sensor.

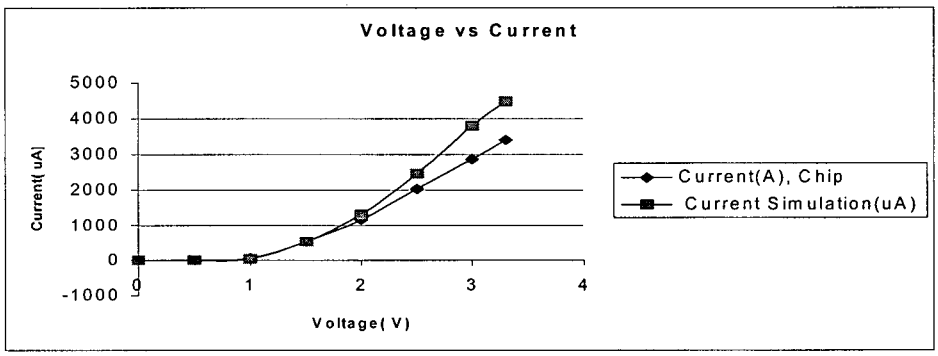

Fig 4.24: Voltage vs Current of heat source: Simulation and Chip result

From Fig 4.2, we see the measurement versus simulation results for varying the voltage across the heat source which is a 16μm/1μm NMOS transistor connected in diode configuration when the ambient temperature is 27°C. There is a 17 % decrease in the current through the heat source in the chip measurements and a corresponding 17% decrease in power dissipated when the maximum voltage of 3.3 V is applied to the heat source. The actual power being consumed is 11.26mW while a value of 13.9mW is expected from simulations. Now to understand the effects of the power consumed at a sensor transistor at a distance of 11.4μm we can derive it by the RC network simulation. A 1°C rise in temperature at this distance caused by the heat source for a power consumption of 11.26mW.

The following graph shows the effect on the output voltage, when the heat source is switched on. This shows that the output voltage is not affected by the heat source being turned on.

The possible reasons for this are:

1) Process variations and transistor mismatches have caused a change in the sensitivity of the designed sensor, and thus it shows very little effect when the temperature is increased.

2) The power supply reaching the sensor is less than 3.3V due to resistance of the ground lines, pads, and the VDD line. The following graph shows simulation results for the variation of the output voltage as we decrease the voltage across the sensor. This decrease in voltage starts matching the observed output variation of the sensor.

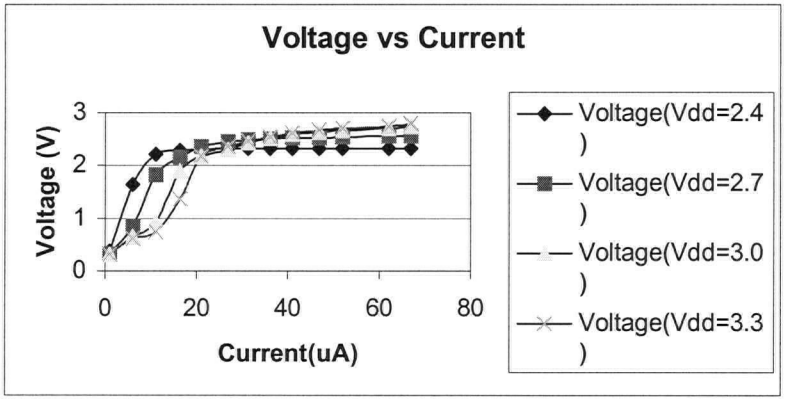

Fig 4.25 : Voltage vs Current when Voltage across the sensor is changed

4.6.2 Monte Carlo Simulations

MOS ICs have both a major and minor statistical distribution of manufacturing tolerance parameters. The major distribution is the wafer to wafer and run-to-run variation. The minor distribution is the transistor to transistor process variation. The minor distribution is responsible for critical second-order effects, such as amplifier offset voltage and flip-flop preference [33].

Worst case analysis is used for design and analysis of MOS and BJT ICs. Taking all variables to their 2-sigma or 3-sigma worst case values simulates the worst case. The parameter variations allow the circuit simulator to predict the actual circuit response to the extremes of the manufacturing process. The physically measurable model parameters are called skew parameters because they are skewed from a statistical mean to obtain a predicted performance variation [33]. Skew parameters are usually independent of each other, so that a combination of parameters can be used to represent worst case values. Typical skew parameters for CMOS technology include:

XL – Polysilicon CD (critical dimension of poly layer representing the difference between drawn size and actual size.)

XW_n , XW_p- Active CD (critical dimension of active layer representing the difference between actual and drawn sizes.)

TOX – Gate oxide thickness

$DELVTO_n$, $DELVTO_p$: Threshold voltage variation

The process parameters were modeled with Gaussian random variables, with variances of 3σ = 10% for the device model parameters, and 5% for the geometric sizes of the MOS transistors. The accuracy of Monte Carlo simulations depends on the generation of correct probability distributions of the random values of transistor values. For a large number of samples (> 1000 samples), the sample mean and variance is close to the parameter's actual mean and variance. Table 4.7 shows 3σ the worst case variations that were taken into account while doing the Monte Carlo simulations.

Model Parameter		Symbol	3σ
1	Oxide Thickness	T_{ox}	10%
2	Substrate doping	NSUB	10%
3	Substrate Mobility	μ_0	10%
4	Threshold voltage	V_{TO}	10%
5	Junction Depth	X_j	10%
6	Transistor Width	W	5%
7	Transistor length	L	5%

Table 4.7: Device model parameter

The following graph, Fig 4.26, shows the effect of variations of the above parameters by the quantities as specified in the table. The graph show that the variation of the output voltage with different input currents for a different variations of the parameters. We see that for some variation of the parameters the output voltage saturates very rapidly and for some variations in the parameters the change in output voltage is very minimal. Thus the output voltage shows a high variation as a result of changes in the transistor parameters.

The next graph, Fig 4.27, shows the variations in the output voltage for the temperature increase caused by the heat source. Here we see that the process variations can affect the sensor performance and cause a decrease in the sensitivity and in some case make the sensor circuit ineffective to the increase in temperature. These simulations show an exact matching between the desired sensor and the simulated sensor and we can thus see that process variations have clearly affected the performance of the sensors.

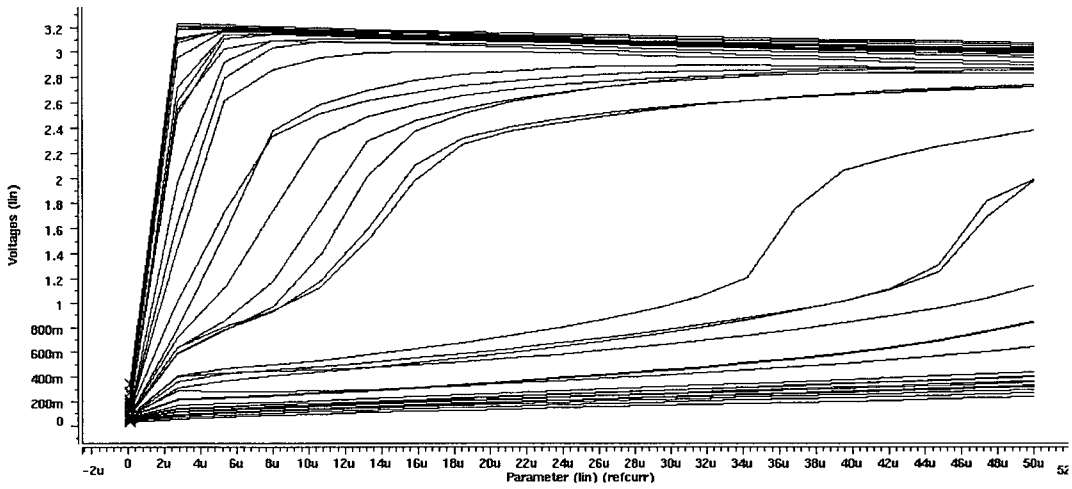

Fig 4.26: Monte Carlo simulation for varying the input current supply

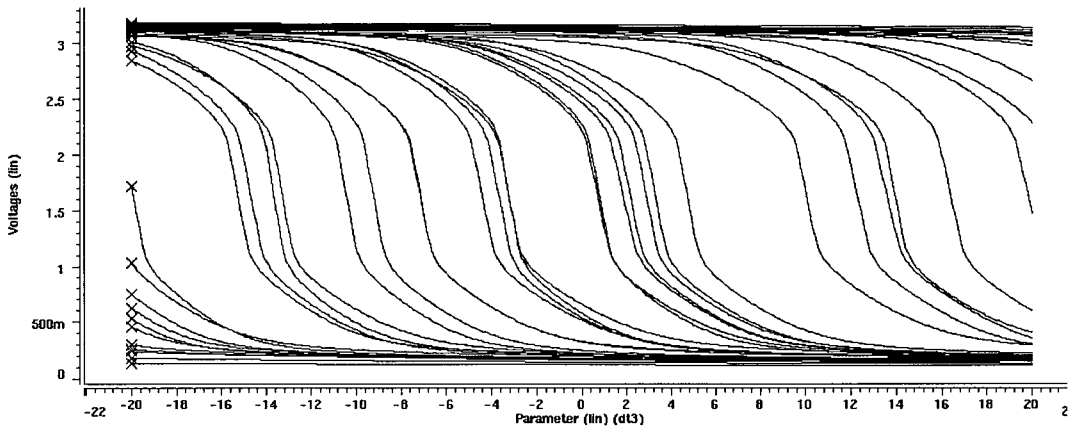

Fig 4.27: Monte Carlo simulations for increase in local temperature over ambient

Chapter 5

Conclusion

The purpose of this thesis was to explore the idea of using CMOS differential thermal testing of integrated circuits and to use this idea as a complementary testing technique to IDDQ. A brief introduction to IDDQ was presented and the limitations of single threshold IDDQ were stated. The first CMOS differential thermal sensors were designed, simulated, fabricated and tested. Simulation and silicon measurement results were presented.

5.1 Conclusions

The concept of thermal testing of integrated circuits is an off-shoot of the problems faced by the single threshold IDDQ testing. . The main disadvantage of IDDQ is that it requires a high V_t to be effective and is only applicable to static circuits. As CMOS technologies scale down, background leakage current increases inexorably, primarily due to device sub-threshold leakage [14]. As a result, conventional single-threshold pass/fail IDDQ testing may no longer be valid even for 0.25-micron technology [15]. Moreover, some analog circuits draw constant current to operate. Hence, IDDQ testing is not effective for these circuits [9].

A number of alternatives to single threshold IDDQ testing have been looked into. These solutions are both at technology and design levels [16]. This work provides a broad based idea of on-chip and off-chip thermal testing methodologies and their advantages and disadvantages. On-chip thermal testing is of two general types, absolute and differential thermal testing. This thesis looked into differential testing as a complementary methodology to IDDQ testing. Three differential temperature sensors were designed,

simulated, and fabricated in 0.18μm CMOS technology. The three designed sensors were a PMOS cascode thermal sensor, a NMOS cascode thermal sensor, and a differential amplifier thermal sensor. These were then implemented in 0.18μm CMOS technology. Careful layout techniques were used as part of the design process. The PMOS cascode thermal sensor had a differential sensitivity of 1.12 V/°C, and occupied an area of 1600μm^2 and consumed a power of approximately 140μW . The NMOS cascode thermal sensor had a differential sensitivity of 1.34 V/°C, and occupied an area of 1520μm^2 and consumed a power of approximately 110μW. The differential amplifier thermal sensor had a differential sensitivity of 1.40 V/°C, and occupied an area of 2320μm^2 and consumed a power of approximately 190μW. Further, research was done into the study of faults induced in an operational amplifier, and with respect to the placement of sensors around an operational amplifier. A testing methodology was proposed wherein the results of the temperature were read off the chip using boundary scan architecture.

The fabricated sensors were tested and the results evaluated. The results were found not match the desired results. This was thoroughly investigated and a reason put forward for this. This helped in formulating a design strategy to be used in further sensor design.

5.2 Future Work

Thermal testing of integrated circuits is a complex topic and requires a broad based understanding of thermodynamics, device physics, and analog integrated circuit design. To make this method more suitable for industrial purposes, future research must focus on the following aspects:

- More work will have to be done and much more thoroughly to the working of these sensors and how they respond to stress, and what their reliability is with time. Once

these tests are done, the sensor can be used as an intellectual property block and placed across the surface of the chip.

- More research must be done into the study of heat flow through the silicon substrate and this must be incorporated into the Spice and Spectre models.
- An on-chip implementation of the sensors used for testing complex integrated circuits would validate using the principles that have been put forward in this work. Future research efforts would help in knowing the area overhead, routing overhead, and in determining how effective this methodology is for industrial application.

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Appendix A

Transistor sizes for PMOS Differential Sensor

Transistor No.	Width/Length
M1	15μm/1.4μm
M2	15μm/1.4μm
M3	30μm/1.4μm
M4	30μm/1.4μm
M5	16μm/1.4μm
M6	16μm/1.4μm
M7	20.2μm/1.4μm
M8	12μm/1.4μm
M9	2.4μm/1.4μm
M10	10μm/1.4μm

Appendix B

Transistor sizes for NMOS Differential Sensor

Transistor No.	Width/Length
M1	16μm/1.4μm
M2	16μm/1.4μm
M3	32μm/1.4μm
M4	32μm/1.4μm
M5	16μm/1.4μm
M6	16μm/1.4μm
M7	2μm/1.4μm
M8	10μm/1.4μm
M9	16μm/1.4μm
M10	32μm/1.4μm

Appendix C

Transistor sizes for Differential Amplifier based Differential Sensor

Transistor No.	Width/Length
M1	32μm/1.4μm
M2	32μm/1.4μm
M3	24μm/1.4μm
M4	24μm/1.4μm
M5	24μm/1.4μm
M6	24μm/1.4μm
M7	12μm/1.4μm
M8	12μm/1.4μm
M9	12μm/1.4μm
M10	12μm/1.4μm
M11	32μm/1.4μm
M12	20μm/1.4μm
M13	24μm/1.4μm
M14	24μm/1.4μm