AN ALL-DIGITAL VLSI

MINIMUM SHIFT KEYING MODEM

By

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ABSTRACT

A general purpose all-digital VLSI minimum shift keying (MSK) modem with novel receiver synchronization capability is designed and implemented. The modulated output is binary and has a centre carrier frequency to bit rate ratio of 5.75. Demodulation is performed semi-coherently using a one-bit observation interval. Other on-chip functions include carrier detection, automatic self-test, and internal loopback. Fabricated with 1.2 μm CMOS standard cell technology, the chip can operate at a maximum clock speed of 50 MHz, rendering 0.19 Mbps binary transmission with the carrier centred at 1.1 MHz.

Modulation is provided with a data-controlled square-wave generating digital circuit. No on-chip RAM is needed. This approach also has the advantages of robustness and phase stability.

For ease of implementation, demodulation is accomplished with a binary quantized correlation-receiver. The theoretical BER performance of this discrete-time all-digital demodulator in AWGN with perfect synchronization is approximately 2 dB poorer than that of a continuous-time optimal detector. The demodulator's susceptibility to imperfect carrier and bit synchronization is also formulated.

Carrier phase recovery and bit timing extraction are provided by three novel first-order digital phase-locked loops (DPLLs). Owing to the special phase-detection techniques employed in these DPLLs, no front-end filtering structures are required. Markovian analyses of the error characteristics of these DPLLs are presented.

A compact almost-all-digital modem unit based on the MSK modem chip is built to facilitate data communications over intrabuilding powerlines at 19.2 kbps using 105.6 kHz and 115.2 kHz carriers. The measured BER performance of this powerline modem in AWGN is approximately 2 dB below theoretical prediction. When used for transmission over actual intrabuilding powerline networks where impulse noises are prevalent, the modem's performance depends on the powerline phase relationship between the transmit and receive points, powerline load profile, and, to a lesser extent, channel's physical length. Under normal circumstances with a transmitter output level of 70 dBmV rms, the BER typically ranges from 10^{-2} to 10^{-5} for cross-phase transmission, while a BER of 10^{-5} or less may be attained for same-phase transmission.

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1. INTRODUCTION

Networking facilitates the sharing and exchange of information among computing entities such as mainframe computers, workstations, PCs, file servers, and print servers, which specialize in the processing, acquisition, retrieval, and storage of information. Networking requires the use of communication protocols. They are rules governing the form, function, and mechanism of network messaging. CCITT's OSI Reference Model is the international standard of communication protocol architecture. The model comprises seven layers, each corresponding to a set of well-defined functions. The bottommost layer, known as "physical layer," provides the most basic yet most important and essential function of transmitting digital data across the communication channel between two nodes.

The physical layer implementation of a data network is largely determined by the transmission characteristics of the channels. A variety of physical channels exists. For example, in a 10BaseT Ethernet, computers are linked by unshielded twisted-pair copper wires; connectivity in a fibre LAN is achieved with optical fibres; and a wireless LAN makes use of nothing but free space as the transmission medium. In general, "digital" channels such as optical fibres and coaxial cables have a wide bandwidth and can therefore accommodate baseband transmission. On the contrary, "analog" channels have a narrow bandwidth and require passband transmission using a device known as "modem." In the transmit direction, a modem modulates by translating digital data into sinusoids; in the receive direction, it demodulates by extracting digital information from received sinusoids. The wireless LAN is an example that utilizes modems at the physical layer for transmission and reception.

1.1 Purpose

Minimum Shift Keying (MSK), one of the well-known modulation schemes, has the advantages of bandwidth efficiency, phase continuity, and constant signal envelope. This thesis involves the research and development of an all-digital MSK modem chip. The chip performs MSK modulation and demodulation, with built-in carrier phase recovery units, bit synchronizer, and carrier detection circuit. The centre carrier frequency to bit rate ratio is internally fixed at

5.75. Demodulation is semi-coherent using a one-bit observation interval. Depending on the system clock frequency, the modem's baud rate and centre carrier frequency can reach as high as 0.19 Mbps and 1.1 MHz, respectively.

1.2 Motivations

Digital implementation has several advantages: (1) the shortcomings of analog components such as aging, temperature drift and need for adjustment are avoided; (2) digital circuits, in general, are easier to design, analyze, as well as troubleshoot, and are more predictable and reliable than analog circuits; (3) with analog VLSI technology still very much in its infancy, digital circuits are more readily amenable to VLSI implementation than analog circuits.

By means of VLSI technology, the modem's size, power consumption, and manufacturing cost are considerably reduced. Miniaturization also enables the integration of modem functions onto a personal computer's motherboard, and the production of low-cost compact modem for laptop applications.

Aside from these attractions, this research project is motivated by the fact that, to the best of the author's knowledge, no such *all-digital bit-by-bit semi-coherent* MSK modems have ever been developed, let alone implemented as a VLSI chip. Innovation is needed for the digital implementation of carrier and bit synchronization functions that are inherently more amenable to analog implementation. The digital architecture and techniques devised in this work can be applied to the design and implementation of other continuous-phase frequency shift keying systems.

1.3 Applications

The modem chip may be used in MSK systems of different transmission requirements. Its baud rate and carrier frequencies are determined by the clock speed applied, which is allowed to be as fast as 50 MHz.

As a specific application demonstrating the modem chip's practicality, the chip is used to facilitate high speed (19.2 kbps) data communications over intrabuilding powerlines. In the early seventies, power utility companies began substantial use of powerlines for remote monitoring and control functions [1, 2, 3]. Not long after, several powerline communication

products appeared in the market. These products employed a master/slave polling scheme for connection set-up, and the maximum data transfer rate they could support was typically at or below 2.4 kbps [4, 5, 6]. As interest in using powerlines for computer networking grew in the early eighties, better powerline modems were developed [7, 8, 9, 10]. In addition, communication characteristics of powerlines were intensively studied. The possibility of applying channel coding techniques to combat powerline noise was explored. Nectar Electronics International Ltd. [11], a UK firm, has already started marketing its own line of powerline modems and network interface software for the realization of powerline-based PC LANs. Recently, Onunga and Donaldson [12, 13] have successfully designed and implemented a powerline network interface module that supports CSMA with priority acknowledgement. These research and development efforts are motivated by the following advantages of communication over intrabuilding powerlines:

1. Low cost: the use of powerlines obviates the need for specialized cabling and installation expense;
2. High convenience: powerlines have a reasonably universal building coverage and can easily be accessed via standard wall-plugs.

Powerline communication has the potential to provide a viable, cost-effective, and flexible means of bringing networking power to the desktop workstations, and for other applications.

1.4 Scope

This dissertation presents the theory, design, implementation, and testing of the all-digital bit-by-bit semi-coherent MSK modem chip. In Chapter 2, the theory of MSK signalling is reviewed. The two chapters that follow are concerned with the digital architecture of the chip: Chapter 3 focuses on the design and analysis of the modulator, demodulator, carrier detector, and built-in self-test circuit, while Chapter 4 explains the novel digital techniques developed for receiver synchronization. Chip design specifications are given in Chapter 5, which also includes a discussion of the design methodology. Chapter 6 examines the VLSI implementation of the design and describes the chip schematics given in the Appendix. In Chapter 7, the realization of a compact almost-all-digital powerline modem using the MSK modem chip is presented, along with a brief review of the communication characteristics of intrabuilding powerlines. Chapter 8

is dedicated to the testing and performance evaluation of the modem chip and powerline modem unit. Finally, in Chapter 9, a few conclusions are drawn, followed by discussions of design limitations and possible improvements.

2. THEORY OF MINIMUM SHIFT KEYING

When transmitting, a modem uses a data signal to "modulate" a sinusoidal carrier whose frequency is within the passband of the channel. When receiving, a modem "demodulates" received carrier signals to recover the data. A variety of modulation schemes are available, differing in performance, bandwidth efficiency, power requirement, and ease of implementation. The well known ones include PSK, ASK, and FSK. The one chosen for implementation in this thesis is MSK -- Minimum Shift Keying. MSK is often used as a quadrature modulation scheme for encoded symbol transmission, with demodulation based on a two-bit observation interval [14, pp. 286-298]. In the modem chip designed here, MSK is used as a *binary* modulation scheme for *single* bit transmission with a *one-bit* demodulation interval. In this chapter, the MSK modulation scheme is characterized, and the semi-coherent demodulation of MSK signals on a bit-by-bit basis is discussed with emphasis on theoretical performance in a zero-mean additive white Gaussian noise (AWGN) environment.

2.1 MSK Modulation

Digital modulation is the process by which a transmitter transforms digital symbols into waveforms that are compatible with the characteristics of the communication channel. In the case of binary bandpass modulation, this corresponds to mapping each bit (0 or 1) of duration T into a passband waveform $s_i(t)$ of equal duration:

$$\begin{aligned} 0 &\rightarrow s_0(t), \quad 0<t\leq T \\ 1 &\rightarrow s_1(t), \quad 0<t\leq T \end{aligned} \qquad \text{<2.1>}$$

Usually, sinusoidal waveforms are chosen, and they are referred to as "carriers" in the sense that they "carry" the digital information across the channel. A sinusoid

$$s(t) = A\sin(2\pi ft + \theta), \quad 0<t\leq T \qquad \text{<2.2>}$$

is characterized by amplitude A, frequency f, and phase angle Θ. Modulation is achieved by

varying one or a combination of these parameters in accordance with the digital information. For example, in PSK, the data signal shifts the carrier phase to either *0* or π. In ASK, it is the carrier amplitude that is altered between two values. FSK relies on the carrier frequency to convey data.

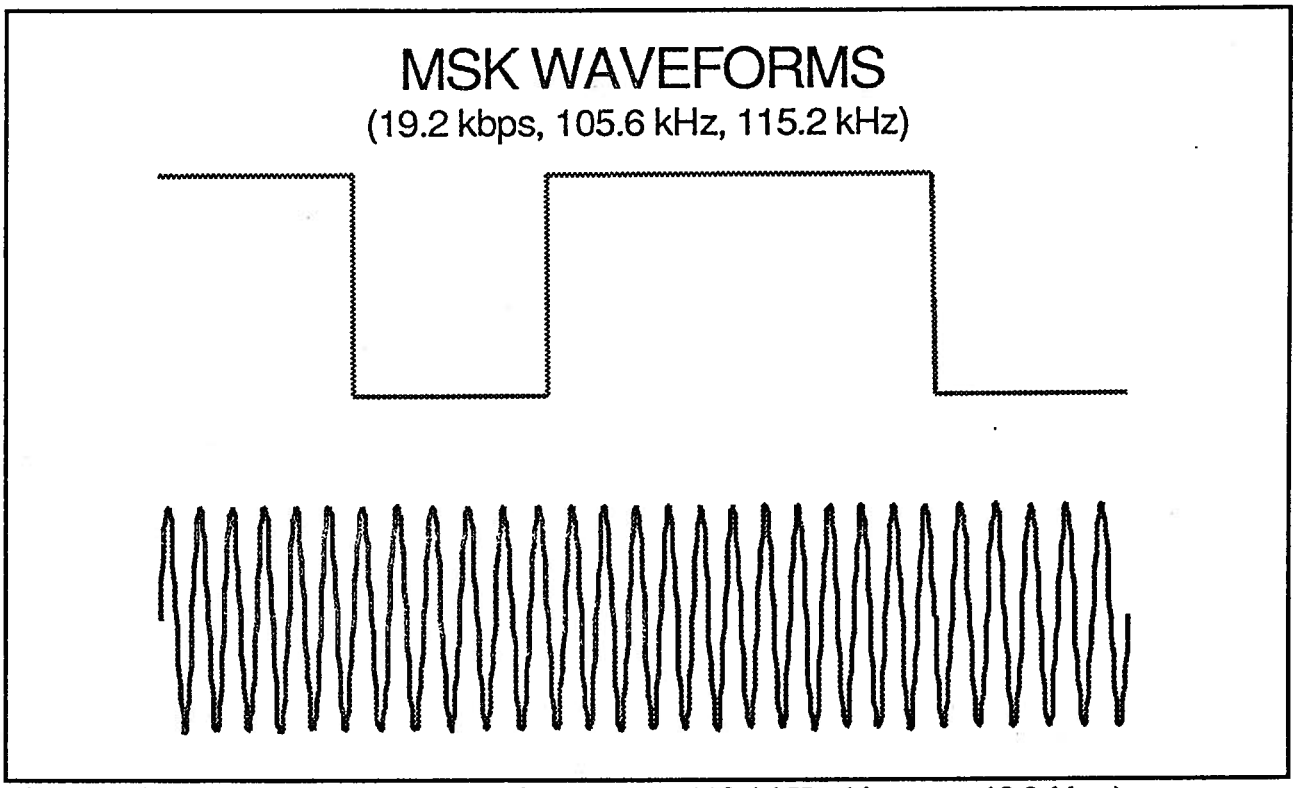


Figure 2.1: MSK waveforms (center frequency = 110.4 kHz, bit rate = 19.2 kbps).

Being a special case of FSK, MSK represents 0 and 1 with two orthogonal sinusoids. But, unlike conventional FSK, the frequency separation (f_1-f_0) of these two sinusoids is only half the bit rate R (= $1/T$), which is the smallest tone spacing possible for orthogonality to prevail. Mathematically, MSK modulation can be described as

$$\begin{aligned} 0 &\rightarrow A\sin(2\pi f_0 t + \theta_i), \quad 0<t\leq T \\ 1 &\rightarrow A\sin(2\pi f_1 t + \theta_i), \quad 0<t\leq T \end{aligned} \qquad \text{<2.3>}$$

where Θ_i, the phase angle of the MSK signal at the beginning of the bit interval, is chosen between *0* and π, whichever would maintain phase continuity at the bit boundary. Shown in Figure 2.1 is a digital data stream and its corresponding MSK waveform.

A modulation scheme can also be represented geometrically by plotting the locations of

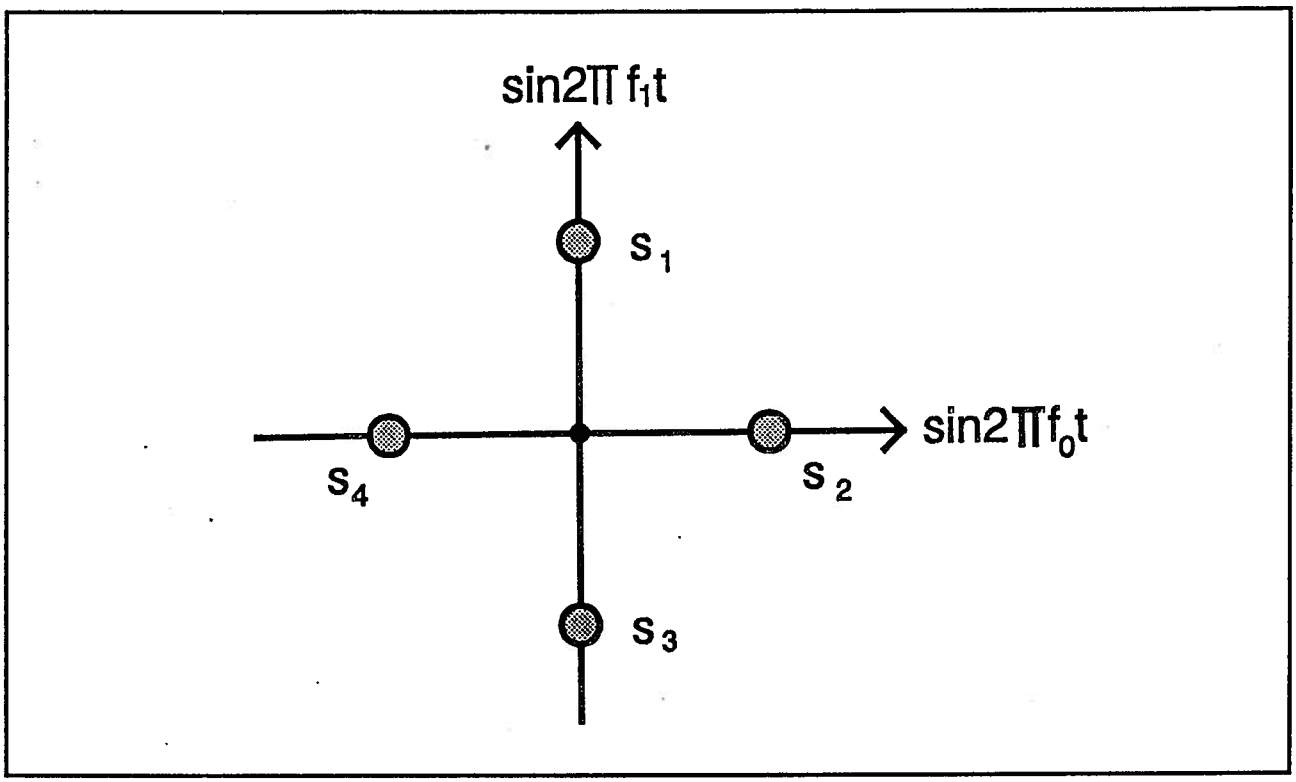


Figure 2.2: MSK signal constellation.

its carrier waveforms on a signal space. The signal constellation of MSK is constituted of four points on a two-dimensional signal space (Figure 2.2). Signals s_1, s_2, s_3, and s_4 together form a biorthogonal signal set, with the minimum distance between them being $d = (2E)^{0.5}$, E denoting the energy of individual signals. In each bit interval, only one of the two pairs of orthogonal signals, (s_1, s_2) or (s_3, s_4), is chosen for use. The choice is governed by the condition of phase continuity and depends on the history of the data sequence.

Another important characteristic of a modulation format is its output power spectral density function. It represents the distribution of average signal power in the frequency domain, and therefore defines the spectral occupancy and bandwidth of the signalling waveform. One of the goals in communication system design is to minimize transmission bandwidth. MSK is a bandwidth efficient modulation scheme. Its power spectral density function $G(f)$ reads

$$G(f) = \frac{8E}{\pi^2}\left[\left(\frac{\cos 2\pi (f-f_c)/R}{1-[4(f-f_c)/R]^2}\right)^2 + \left(\frac{\cos 2\pi (f+f_c)/R}{1-[4(f+f_c)/R]^2}\right)^2\right] \qquad \text{<2.4>}$$

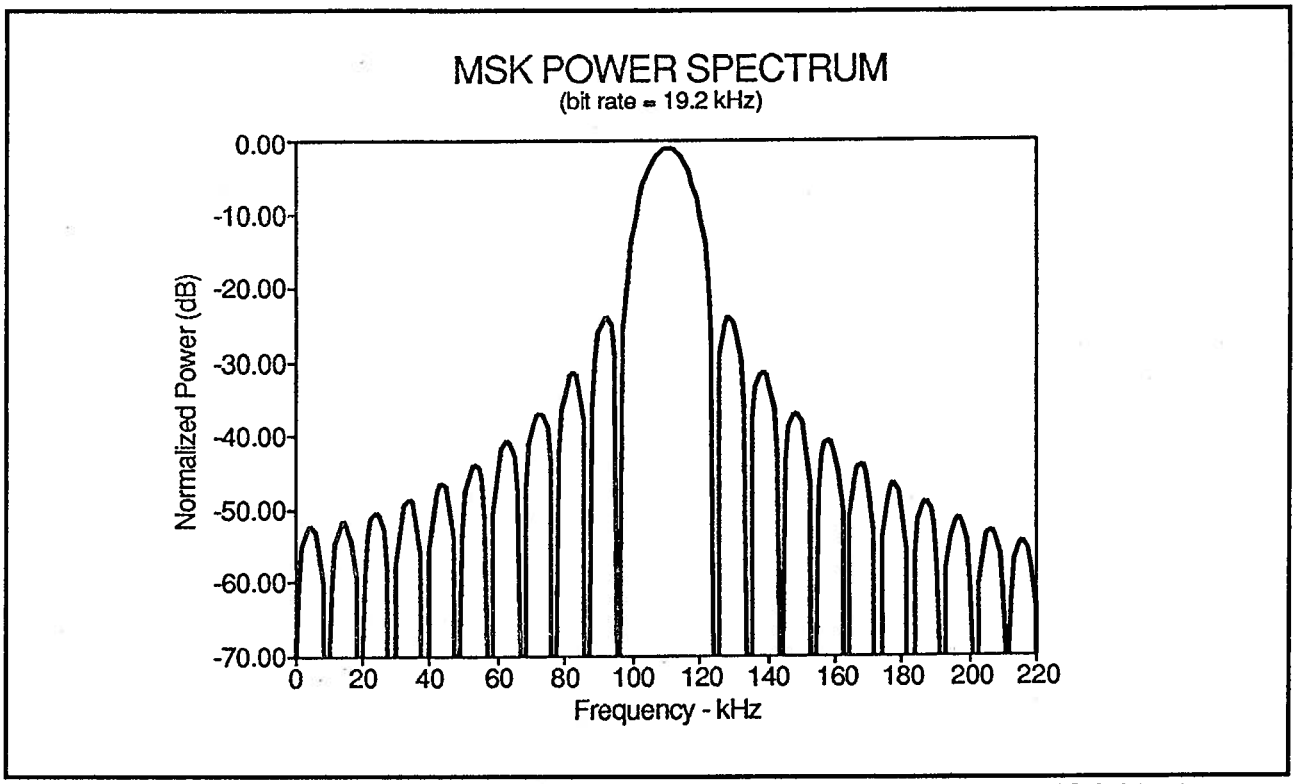


Figure 2.3: MSK power spectrum (center frequency = 110.4 kHz, bit rate = 19.2 kbps).

where $f_c = (f_0+f_1)/2$ is the centre carrier frequency. The envelope of $G(f)$ falls off as f^{-4}, as opposed to the slower f^{-2} roll-off rate characteristic of such schemes as PSK and FSK [14]. As a consequence, the side lobes in the MSK power spectrum are greatly suppressed (Figure 2.3). In fact, 99 % of the signal power in MSK is contained in a bandwidth of only about $1.2R$ [14].

Besides bandwidth efficiency, MSK has other advantages:

1. MSK waveforms exhibit phase continuity, thus minimizing any inter-symbol interference caused by amplifier non-linearity.
2. MSK signals have a constant envelope, thus avoiding amplitude-limiting distortion that could be introduced by power amplifier at the transmitter.

2.2 MSK Demodulation

Demodulation is the process by which a receiver retrieves digital information from the modulated carrier. In binary signalling, a receiver has to decide whether it is a 0 or 1 that is carried in each bit interval. In reality, a signal traversing the communication channel is subjected

to noise interference. When it reaches the receiver, the signal may be so corrupted that it misleads the receiver to a wrong bit decision. Minimization of bit error probability is one criterion of optimality in receiver design. Presented below is an overview of various methods of MSK detection and a description of the suboptimal (in AWGN sense) demodulation technique that is implemented on the MSK modem chip.

2.2.1 Methods of MSK Detection

MSK is a very special digital modulation scheme because it can be viewed either as a form of offset quadrature phase shift keying (OQPSK) with sinusoidal symbol weighting, or as a special case of continuous-phase frequency shift keying (CPFSK) [15].

In the first view, MSK is considered as being composed of two orthogonal data channels: in-phase (I) and quadrature-phase (Q). Optimal demodulation can be performed with a fully coherent I-Q receiver using a two-bit observation interval. Alternatively, differentially coherent detection may be used, but this yields suboptimal performance [15].

In the second view, MSK is treated as CPFSK with a modulation index of 0.5, and its detection may be either noncoherent or coherent [16]. Noncoherent detection is suboptimal, usually achieved by processing the signal over one or more bit intervals with limiter-discriminators. Optimal demodulation requires coherent detection over a two-bit observation interval. Such a receiver has a rather complex structure [17].

In the design of the MSK modem chip, the CPFSK view of MSK is adopted. For simplicity and other reasons to be explained shortly, the modem uses a semi-coherent demodulation scheme based on a one-bit observation interval. This scheme is suboptimal, but has the advantages of ease of implementation and compatibility with conventional FSK. Also, exact analysis of its performance in AWGN is possible.

2.2.2 Semi-Coherent Demodulation of MSK

MSK and conventional FSK are both a form of orthogonal CPFSK. In each bit interval, either one of the two orthogonal waveforms in <2.3> is transmitted. For conventional FSK, the initial phase angle, Θ_i, is fixed at 0 for every bit interval. For MSK, Θ_i may be either *0* or π, whichever is needed to maintain phase continuity at the bit boundary. To *coherently* receive MSK

signals using a one-bit observation interval, exact knowledge of Θ_i is required. Under this condition, the coherent MSK demodulator chooses between two orthogonal signals in each bit interval, and therefore has the same BER performance as the coherent FSK demodulator [18, pp. 406-407]. (Note that in *noncoherent detection*, Θ_i is treated as a random variable uniformly distributed between *0* and 2π.)

However, in practice, bit-by-bit coherent MSK demodulation is not realizable because exact knowledge of Θ_i is not available at the receiver. It is true that Θ_i might be estimated, but doing so would require information from previous bit intervals and would have a non-zero probability of error.

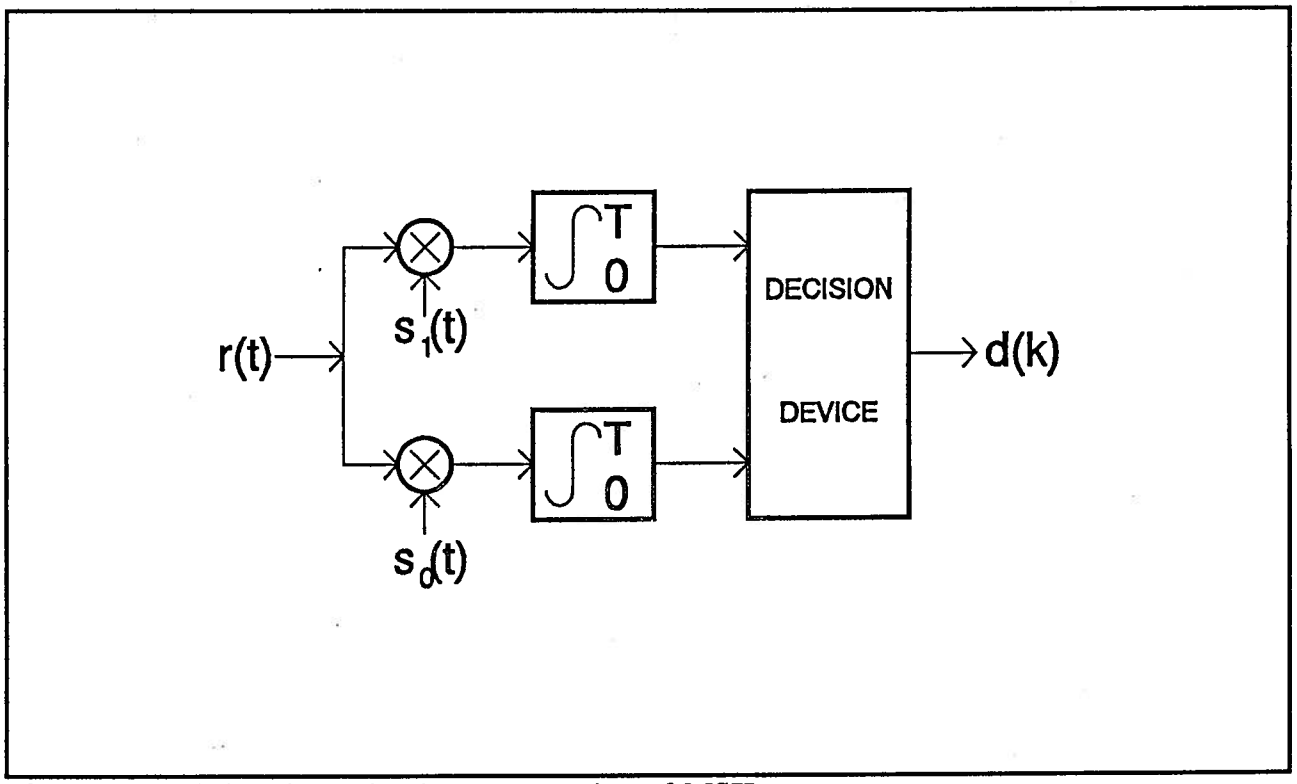


Figure 2.4: Bit-by-bit semi-coherent reception of MSK.

As a result of this difficulty, bit-by-bit demodulation of MSK can at best be realized *semi-coherently*. This is the approach used by the modem chip to receive MSK signals. Such a demodulator has the same structure as a coherent FSK detector, consisting of a pair of correlators and a decision device (Figure 2.4). Due to the lack of knowledge in Θ_i, there is *180°* phase uncertainty in the two locally recovered carrier references. So, in each bit interval, the

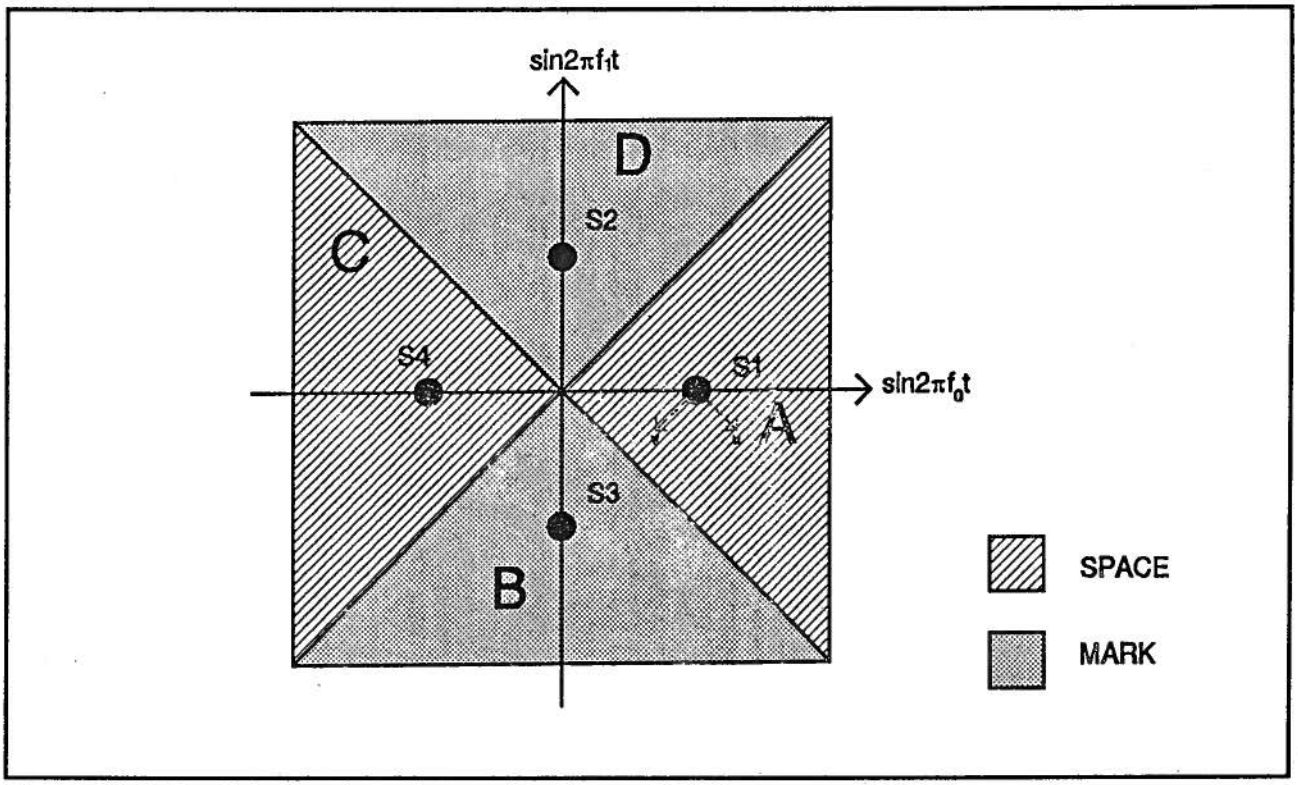


Figure 2.5: Decision regions for semi-coherent MSK.

demodulator has to choose among four biorthogonal signals (Figure 2.5). Bit decision is based on magnitude, not algebraic, comparison according to the following rule:

$$|c_1| \begin{matrix} 1 \\ > \\ < \\ 0 \end{matrix} |c_0| \qquad \text{<2.5>}$$

where c_0 is the output of the space frequency correlator, and c_1 is the output of the mark frequency correlator.

The theoretical BER performance of this semi-coherent detector in AWGN with one-sided power spectral density N, $P_{e,MSK}$, is related to that of coherent FSK, $P_{e,FSK}$, as follows [19, p. 244]:

$$P_{e,MSK} = 2P_{e,FSK}(1 - P_{e,FSK}) \qquad \text{<2.6>}$$

Under perfect receiver synchronization, $P_{e,FSK}$ is given by [20, p. 252]

$$P_{e,FSK} = \frac{1}{2} erfc \sqrt{\frac{E}{2N}} \qquad \text{<2.7>}$$

In Figure 2.6, the BER curve of semi-coherent MSK is plotted together with those of coherent PSK [20] and coherent FSK for comparison. With semi-coherent MSK, bandwidth efficiency is attained at a slight expense of bit error performance. Note also that in the limit of large signal to noise ratio, $P_{e,MSK}$ is twice as much as $P_{e,FSK}$.

In reality, because of hardware limitation and noise influence, perfect carrier and bit

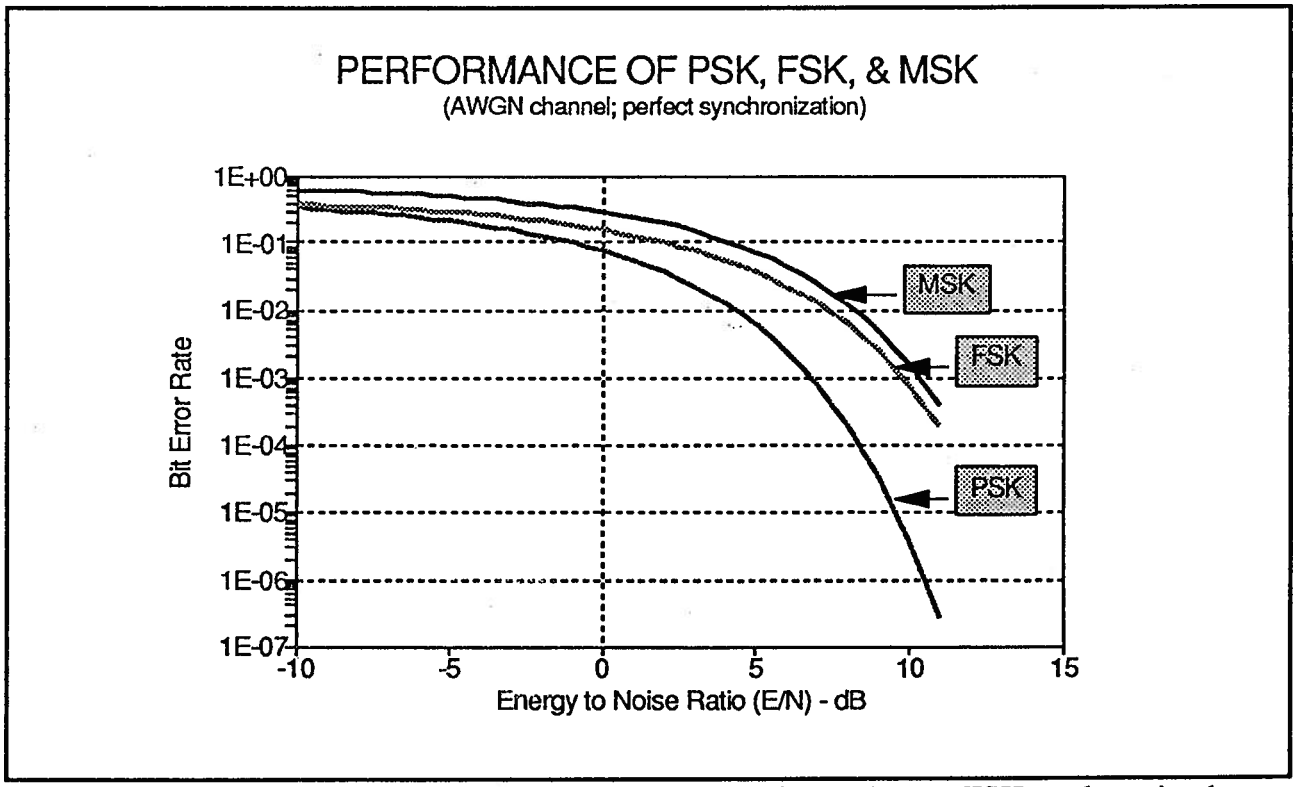


Figure 2.6: Theoretical BER performance of coherent PSK, coherent FSK, and semi-coherent MSK in AWGN.

synchronization is not available at the receiver. Under this circumstance, relation <2.6> still holds but $P_{e,FSK}$ is no longer given by <2.7>. First, in the case of imperfect carrier phase recovery, $P_{e,FSK}$ becomes [21, pp. 302-336]

$$P_{e,FSK} \cong \frac{1}{2} erfc \sqrt{\frac{E}{2N} \cos^2 \beta} \qquad \text{<2.8>}$$

where β denotes the phase difference between local carriers and received carriers.

Next, when bit synchronization is imperfect, the recovered bit clock is offset from the actual bit clock by τ (> 0) units of time. As a result, the period of integration extends not from 0 to T but rather from τ to $T+\tau$, thus overlapping two consecutive bits. Half of the times when the two overlapped bits have the same polarity, this error leads to no consequence. Half of the times when the two overlapped bits have opposite polarity, this error increases the probability of false detection. It can be shown that, for $\tau/T << R/f_c$, $P_{e,FSK}$ becomes

$$P_{e,FSK} \cong \frac{1}{2}\left[\frac{1}{2} erfc \sqrt{\frac{E}{2N}} + \frac{1}{2} erfc \sqrt{\frac{E}{2N}\left(1 - \frac{\mu^2|\tau|^3}{3T}\right)^2}\right] \qquad \text{<2.9>}$$

where $\mu = 2\pi(f_1 - f_0)$.

Finally, if both carrier phase error and bit timing error are present at the receiver, as is normally the case, $P_{e,FSK}$ should be corrected to read

$$P_{e,FSK} \cong \frac{1}{2}\left[\frac{1}{2} erfc \sqrt{\frac{E}{2N}\cos^2\beta} + \frac{1}{2} erfc \sqrt{\frac{E}{2N}\cos^2\beta\left(1 - \frac{\mu^2|\tau|^3}{3T}\right)^2}\right] \qquad \text{<2.10>}$$

Performance degradation due to imprecise synchronization is illustrated by the set of BER curves in Figure 2.7. Curve B belongs to a semi-coherent MSK receiver with 10% (= 36°) carrier phase error; curve C to one with 10% bit timing error; and curve D to one with both 10% carrier phase error and 10% bit timing error. As expected, these curves all lie above, and thus indicate a higher bit error probability than, curve A which represents the performance of a semi-coherent

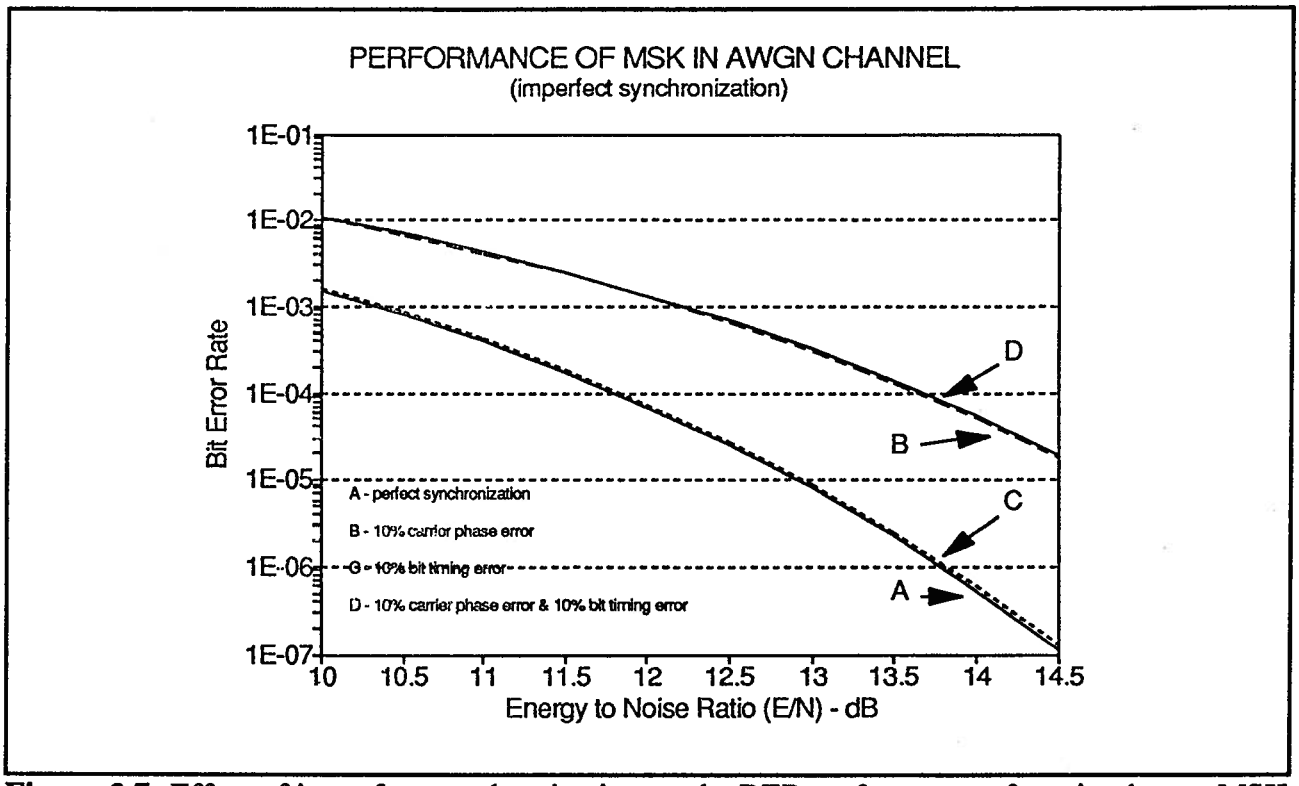


Figure 2.7: Effect of imperfect synchronization on the BER performance of semi-coherent MSK in AWGN.

MSK receiver under perfect synchronization condition. The effect of bit timing error is much less substantial than that of carrier phase error.

2.3 Analog Vs Digital

The formula cited in this chapter are based on continuous-time analysis under the assumption that the demodulation process has an analog implementation. However, the demodulator on the MSK modem chip is digitally implemented, and is therefore a sampled-data system. Its operation should be analyzed in discrete-time taking into account of sampling and quantization effects. Such an analysis is presented in the next chapter, and the result indicates that, not surprisingly, in terms of theoretical BER performance in AWGN, the digital system is inferior to the analog system.

3. A DIGITAL ARCHITECTURE FOR MSK SIGNALLING

Inside the MSK modem chip are four main functional modules: modulator, demodulator, carrier detector, and built-in-self-test controller (Figure 3.1). In this chapter, the operation principles and design considerations of these digitally implemented modules are explained, and their performance is analyzed.

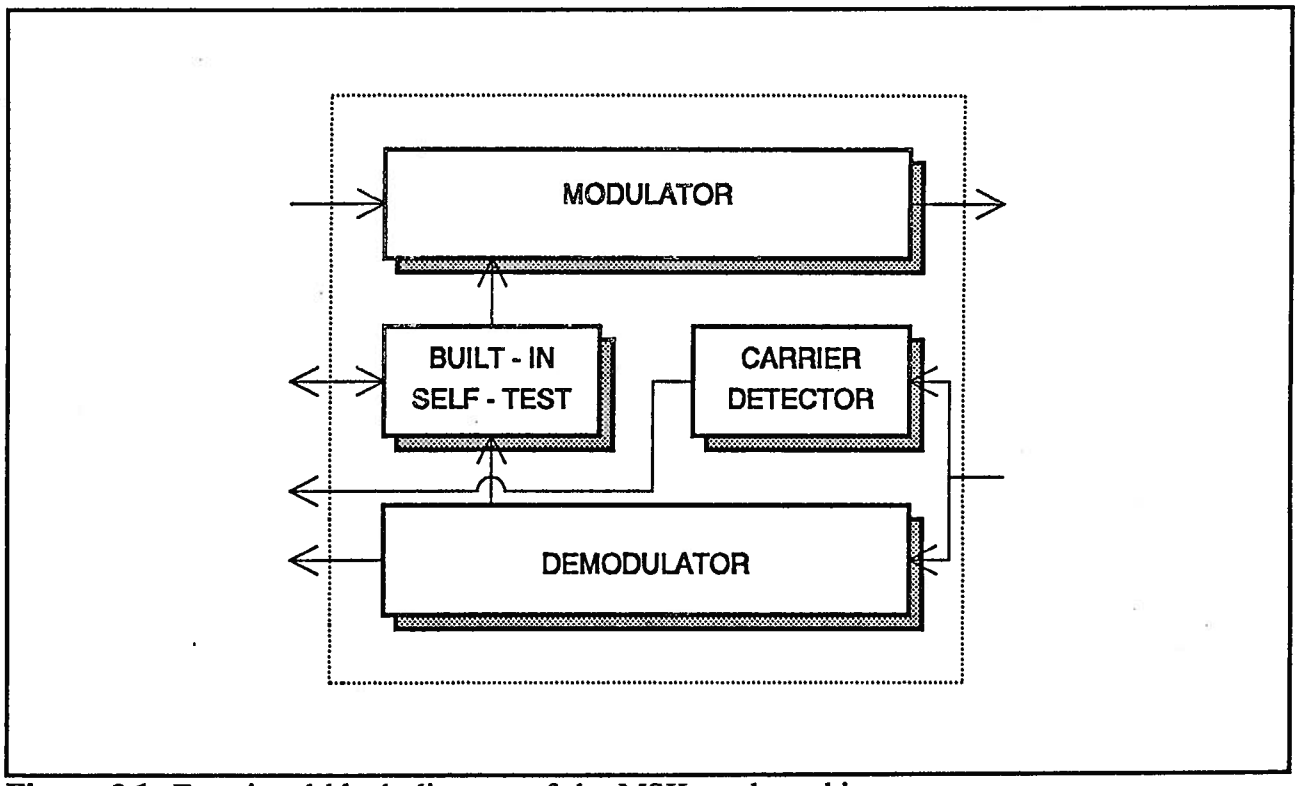


Figure 3.1: Functional block diagram of the MSK modem chip.

3.1 Modulation Structures

MSK modulation can be realized with analog components in two ways. One is simply by using the data to vary the output frequency of a voltage controlled oscillator (VCO) [22, pp. 189-191] (Figure 3.2). The other is slightly more complicated: the MSK signal is obtained by summing the output of two multipliers modulating the in-phase and quadrature-phase components of the centre carrier with baseband data [23] (Figure 3.3).

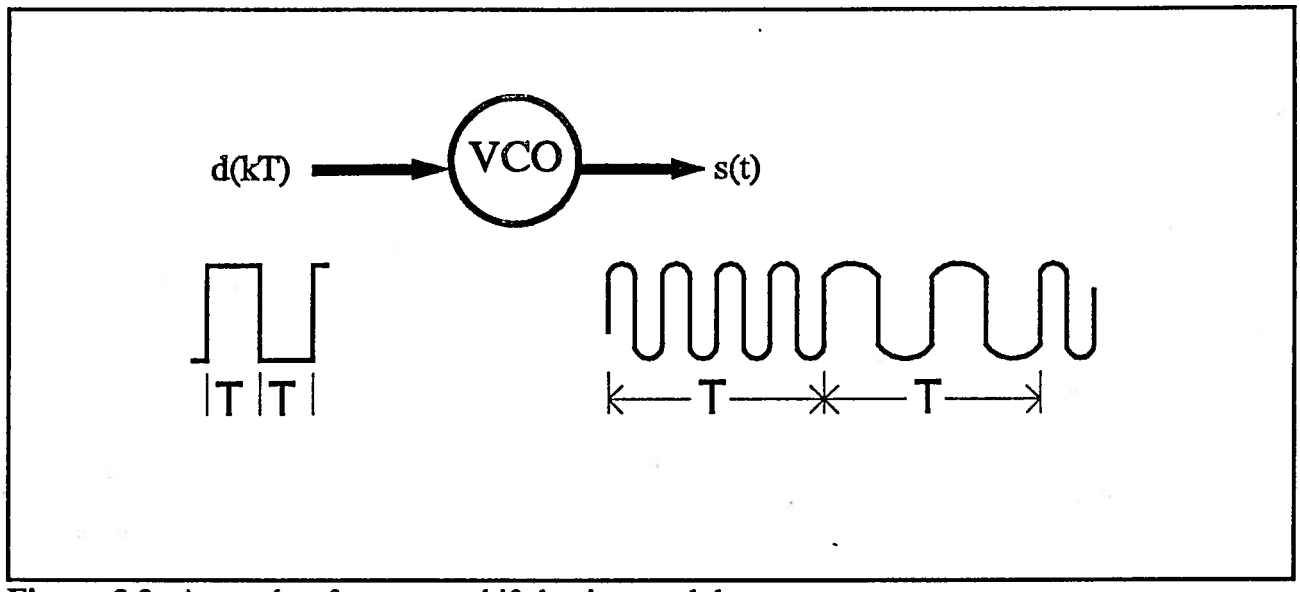


Figure 3.2: An analog frequency shift keying modulator.

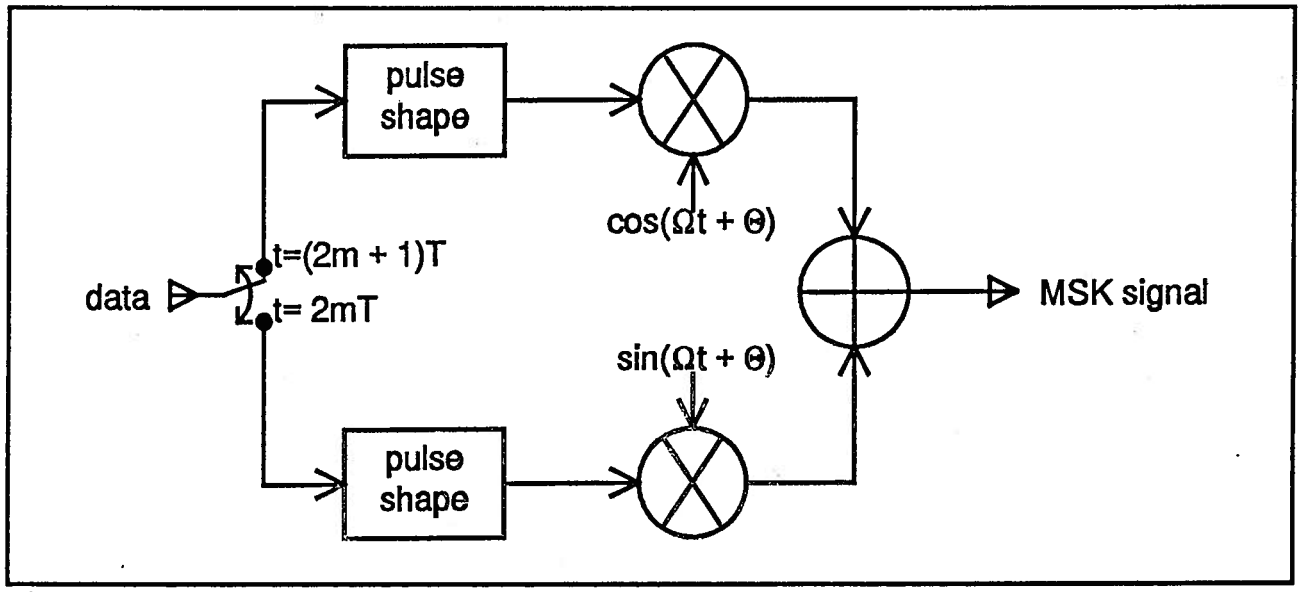


Figure 3.3: An analog I-Q type MSK modulator.

There are also a few possible ways to implement MSK modulation in the digital domain. One, referred to as table look-up technique [24, pp. 37-43], is illustrated in Figure 3.4. Multi-bit digital representation of each carrier sinusoid is pre-stored in a ROM. During each bit interval, the digital sequence corresponding to the data symbol for that interval is "looked up" from the memory and fed into a D/A converter which reconstructs the analog carrier wave. Alternatively, one may synthesize the signalling waveforms with a Johnson counter and a resistor network [25,

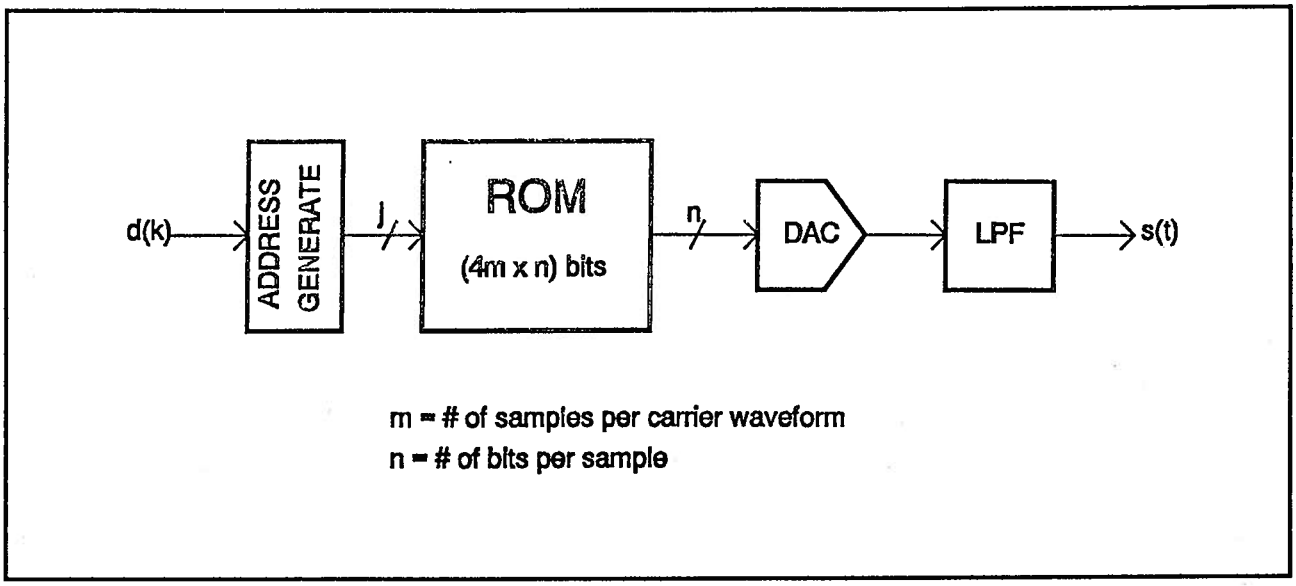


Figure 3.4: Table look-up sinewave generator.

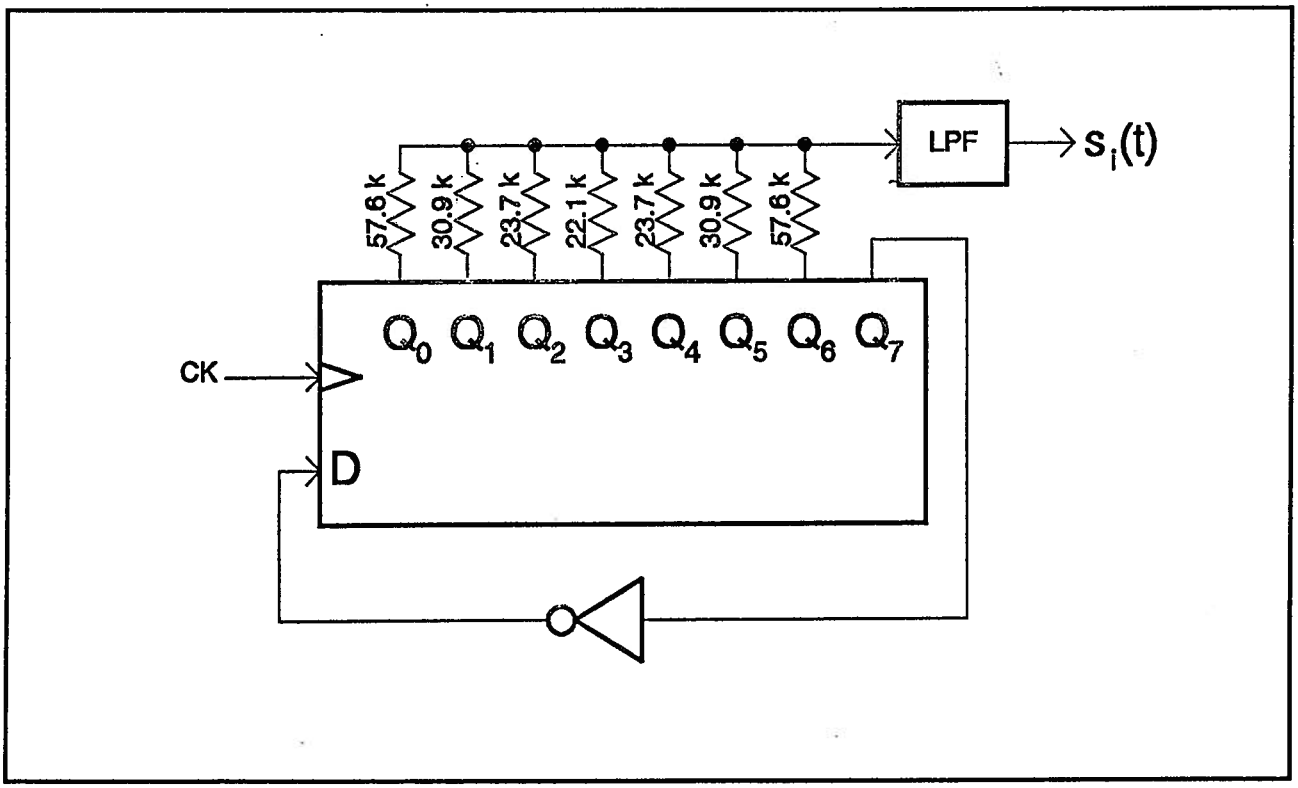


Figure 3.5: A Johnson counter based sinewave synthesizer.

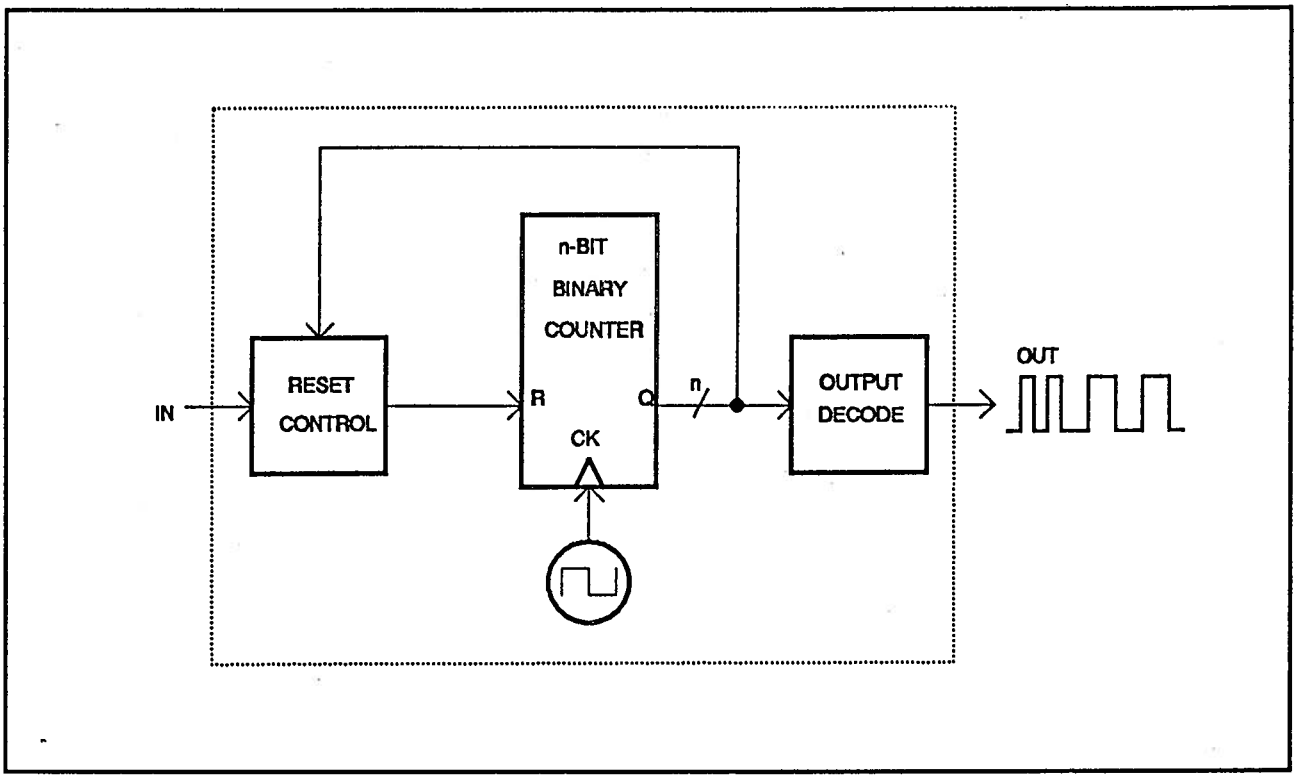


Figure 3.6: A numerically controlled oscillator (NCO).

p. 448]. Figure 3.5 shows an example of this which outputs an 8-level approximation to a sine wave. This approach alleviates the use of ROM and D/A convertor, but requires highly accurate resistors and is not easily amenable to VLSI implementation.

3.1.1 An All-Digital MSK Modulator

In the MSK modem chip, a different technique is used to achieve MSK modulation. Analogous to the VCO method, it makes use of a so-called numerically controlled oscillator (NCO) -- basically an adjustable divide-by-N circuit (Figure 3.6). The NCO outputs a square wave, the frequency of which is varied between f_0 and f_1 according to the digital data. In addition, an external low-pass filter is needed to "smooth out" the output waveshape. The merits of this approach include simplicity and robustness: the NCO can easily be implemented with a binary counter and random logic; unlike the table-look-up method, no on-chip memory nor external D/A converter is required.

3.1.2 Performance Analysis

Modulators are evaluated in terms of output phase stability. In the NCO-based digital MSK modulator described above, phase stability is determined by the accuracy of the system clock and the ratios of carrier frequencies (f_0, f_1) to system clock frequency f_s. Suppose that the system clock has absolute jitter δf_s. And let R_0 be f_0/f_s and R_1 be f_1/f_s. Then, depending on the data bit, the modulator output frequency would be either $f_0 \pm R_0\delta f_s$ or $f_1 \pm R_1\delta f_s$. Assuming equiprobable 0's and 1's and random Gaussian error statistics, the average output frequency f_{out} is given by

$$f_{out} = \frac{f_0+f_1}{2} \pm \frac{\sqrt{R_0^2+R_1^2}}{2}\delta f_s \qquad \text{<3.1>}$$

The error term in the above expression corresponds to the absolute output jitter δf_{out}, and the percentage output jitter $f_{out}/\delta f_{out}$ is

$$\frac{f_{out}}{\delta f_{out}} = \frac{\sqrt{R_0^2 + R_1^2}}{R_0 + R_1}\frac{\delta f_s}{f_s} \qquad \text{<3.2>}$$

3.2 Demodulation Structures

The digital demodulator in the MSK modem chip is designed to perform semi-coherent demodulation of MSK signals over a one-bit observation interval. As shown in Figure 3.7, it is structured as a correlation-receiver. First, the MSK signal received from the powerline is separately multiplied by two locally generated carrier references, and the products are integrated over one bit interval. Subsequently the outputs are compared in the decision device to determine the digital data. Also present in the demodulator are two carrier synchronizers which track the two orthogonal carriers, and a bit synchronizer which recovers the bit clock. Owing to the digital operation of this demodulator, it is necessary to digitize the received MSK signal before feeding it into the modem chip. This digitization can be achieved with either a hardlimiter or a multi-bit A/D converter.

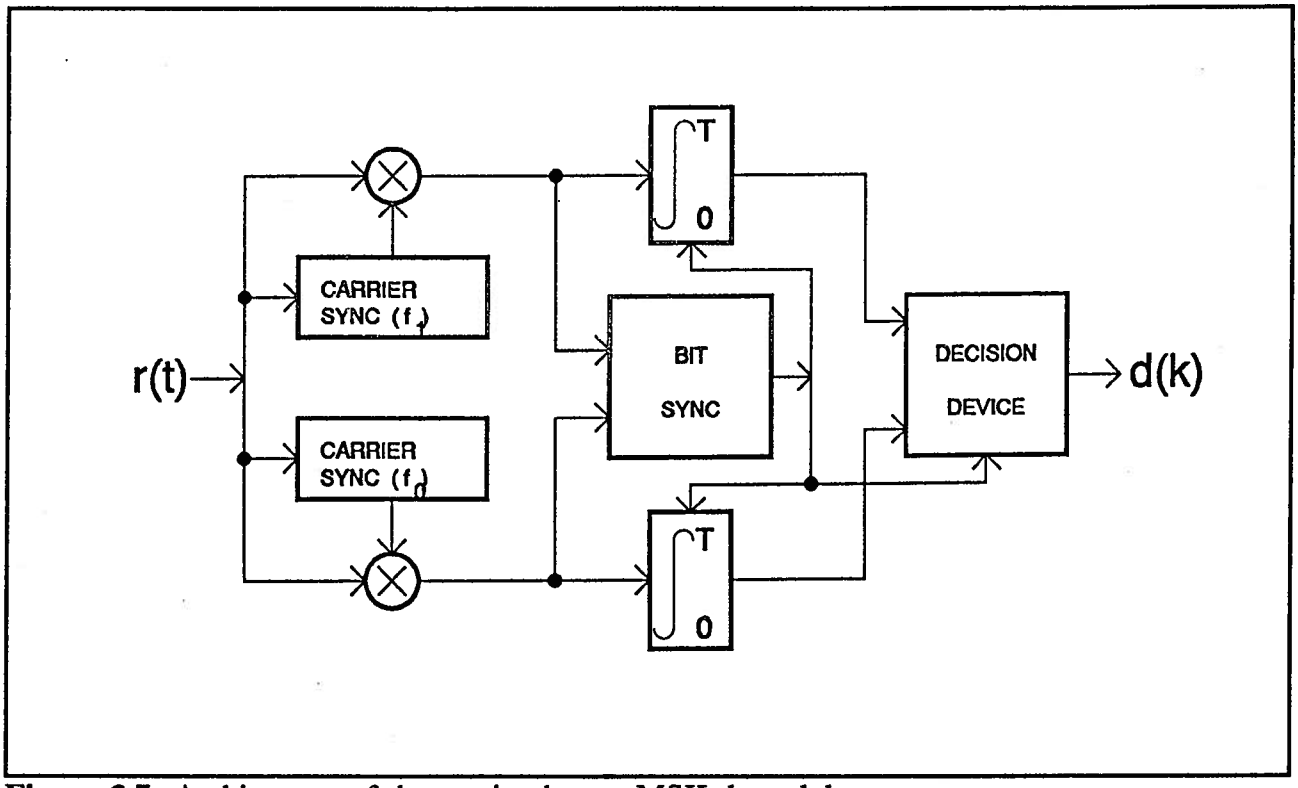


Figure 3.7: Architecture of the semi-coherent MSK demodulator.

3.2.1 Digital Correlation

An analog representation of a correlator is shown in Figure 3.8. The correlator consists of a multiplier and a time-domain integrator. Mathematically, the correlator computes the following integral:

$$c_c = \int_0^T r(t)s(t)dt \qquad \text{<3.3>}$$

where $r(t)$ is the received signal, and $s(t)$ is the local carrier reference. This integral measures the similarity between the two signals over bit interval T.

Discretizing equation <3.3> gives

$$c_d = \sum_{n=1}^{m} r(\frac{nm}{T})s(\frac{nm}{T}) \qquad \text{<3.4>}$$

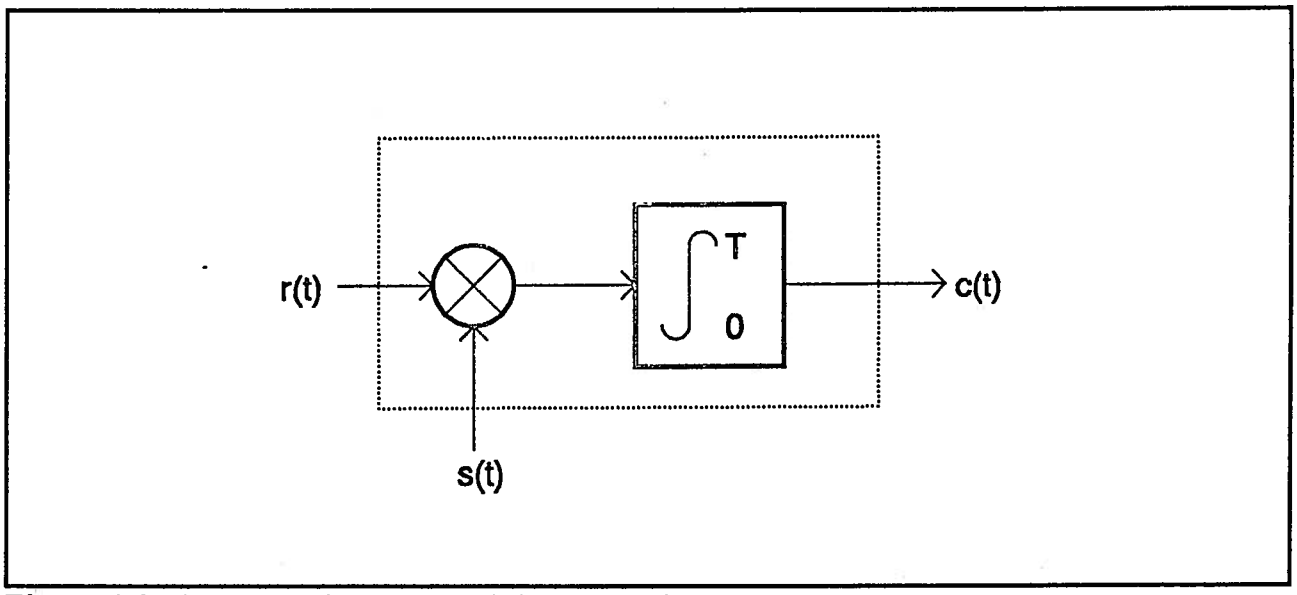


Figure 3.8: An analog integrate-and-dump correlator.

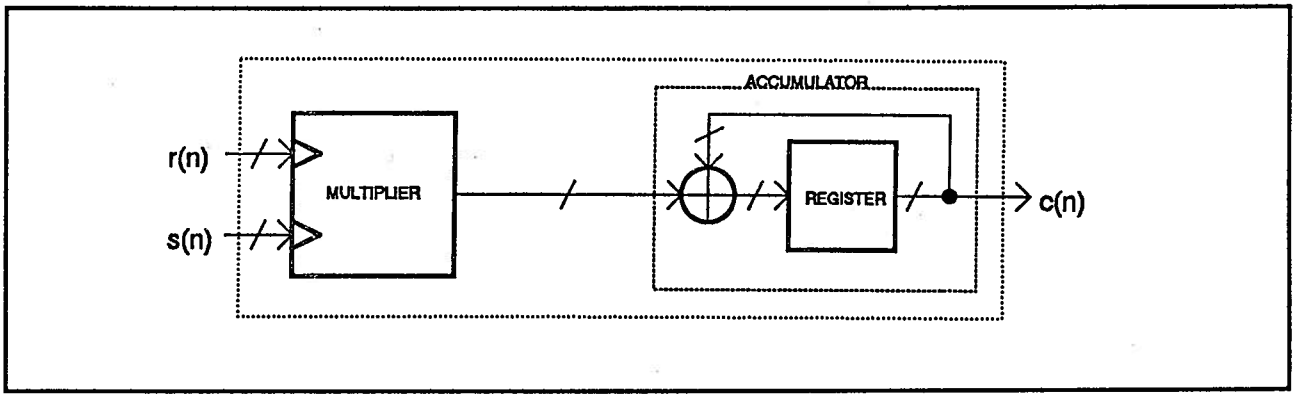


Figure 3.9: A multi-bit digital correlator.

with m denoting the number of equally-spaced samples taken over T. This equation suggests that a digital correlator can in general be implemented with two ADCs, a multi-bit multiplier, and a multi-bit adder, as shown in Figure 3.9. Simplification occurs when both $r(n)$ and $s(n)$ are 1-bit digitized (i.e. square wave). In this special case, the correlation function can be interpreted as follows [26]:

$$c_b = \frac{A-D}{A+D} = \frac{A-D}{m} = \frac{2A-m}{m} = \frac{m-2D}{m} \qquad \text{<3.5>}$$

where A and D are, respectively, the number of agreements and disagreements in the polarities

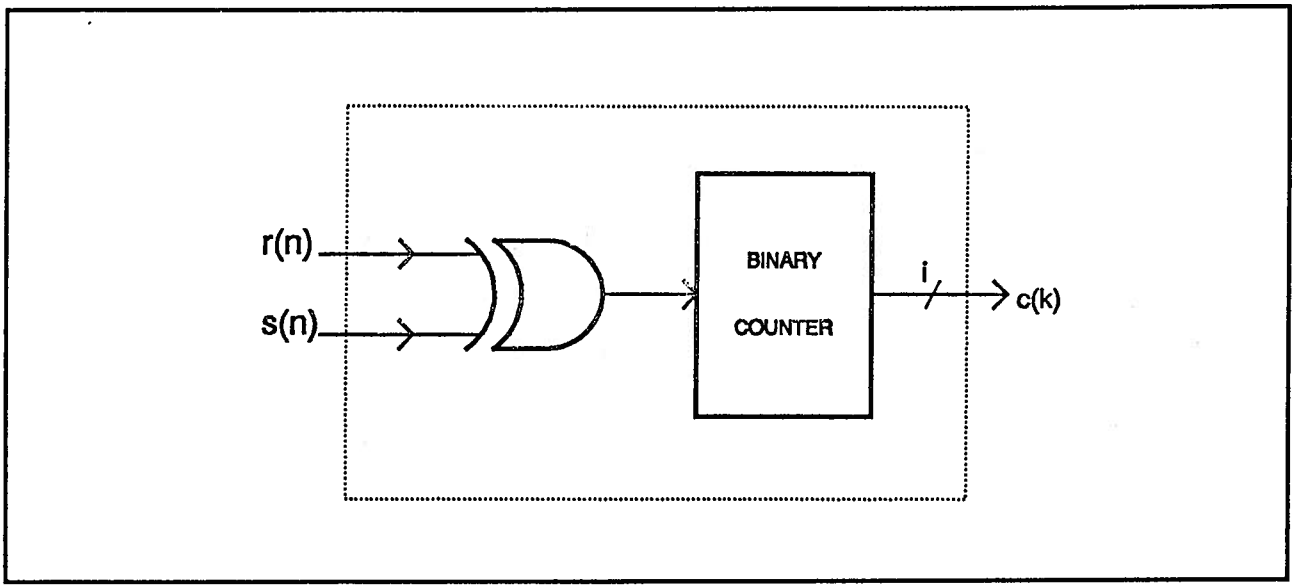


Figure 3.10: A one-bit digital correlator.

of the two signals over T. This function c_b can easily be computed, to within a constant of proportionality, by using a "binary correlator" like the one shown in Figure 3.10. The XOR gate compares the polarity of the inputs while the counter tallies the number of agreements and disagreements. This kind of implementation which considers only signal polarities is referred to as "binary partial decision" [27]. It readily lends itself to VLSI implementation.

For FSK demodulation, two binary correlators, one for each carrier frequency, and a decision device are needed, as shown in Figure 3.11. The decision device identifies datum in each bit interval according to the following rule:

$$c_1 \begin{array}{c} 1 \\ > \\ < \\ 0 \end{array} c_0 \qquad \text{<3.6>}$$

where c_0 and c_1 are the output of the space and mark frequency correlators, respectively.

The semi-coherent MSK demodulator on the modem chip is structurally identical to the coherent FSK demodulator just described, except that a different decision rule is used, which now

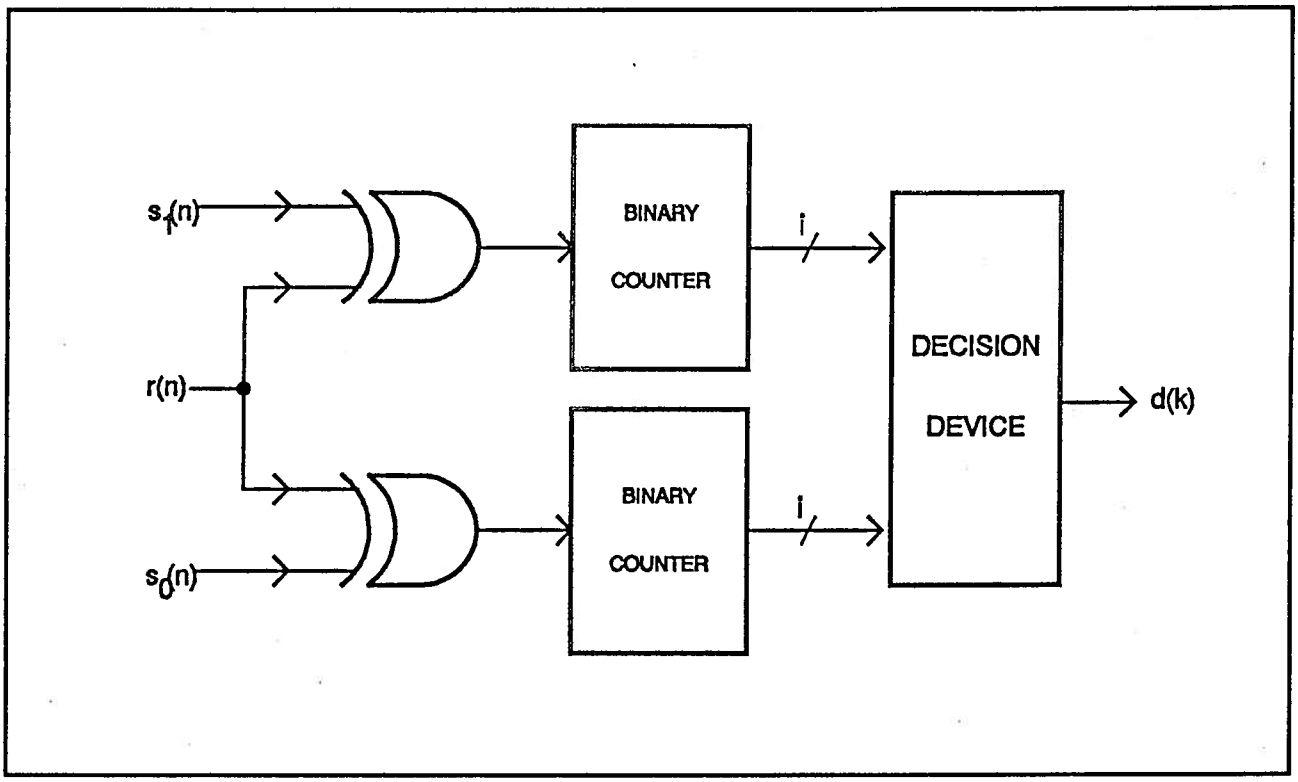


Figure 3.11: A binary partial detector for coherent FSK or semi-coherent MSK.

reads

$$|c_1| \underset{<}{\overset{>}{}} |c_0| \qquad \begin{matrix} 1 \\ \\ 0 \end{matrix} \qquad \text{<3.7>}$$

Bit decision is based on the absolute magnitude of the two correlation outputs, and can easily be implemented with combinational logic.

3.2.2 Performance Analysis

The BER performance of the binary quantized coherent FSK and semi-coherent MSK receivers in AWGN under conditions of perfect synchronization and imperfect synchronization is derived below.

Perfect Synchronization

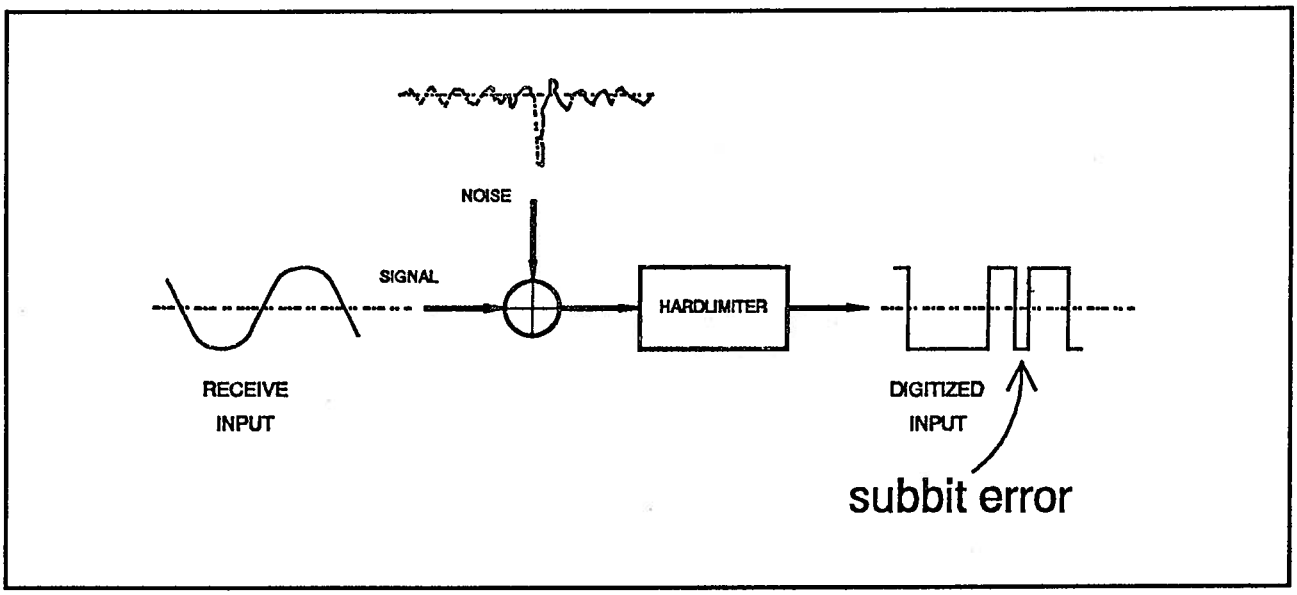


Figure 3.12: Subbit error caused by channel noise.

To begin, without loss of generality, assume that a space bit is transmitted to the binary-quantized coherent FSK demodulator via an ideal channel. During this bit interval, the space frequency correlator will observe m polarity agreements and 0 polarity disagreements, i.e. $A_0 = m$ and $D_0 = 0$, m being the total number of samples or "subbits" over T. Owing to orthogonality of the two carriers, the mark frequency correlator will observe $m/2$ agreements and $m/2$ disagreements in the same bit interval, i.e $A_1 = (m/2)$ and $D_1 = (m/2)$. Therefore, in the absence of channel interference, $c_0 = 1$ and $c_1 = 0$, and by <3.6> this will lead to a correct bit decision, as expected.

Now, let the channel be noisy so that subbit error probability is non-zero (Figure 3.12). Occurrence of a subbit error may reduce A_0 by 1 making c_0 smaller, but can either increase or decrease D_1 by 1, depending on the position of the inflicted subbit sample. If the subbit error does increase D_1 by 1 making c_1 more positive, this is said to be an "offending" subbit error. Otherwise, it is an "innocent" subbit error because it does not reduce the "distance" between c_0 and c_1. Owing to orthogonality of the two signals, the maximum number of offending subbit errors is $m/2$, and so is the maximum number of innocent subbit errors. If in one bit interval there are e_b offending subbit errors and e_g innocent subbit errors, then

$$A_0 = m - e_g - e_b \qquad \text{<3.8>}$$

$$D_0 = e_g + e_b \qquad \text{<3.9>}$$

$$\Rightarrow c_0 = \frac{1}{m}(m - 2e_g - 2e_b) \qquad \text{<3.10>}$$

and

$$A_1 = \frac{m}{2} + e_b - e_g \qquad \text{<3.11>}$$

$$D_1 = \frac{m}{2} - e_b + e_g \qquad \text{<3.12>}$$

$$\Rightarrow c_1 = \frac{2}{m}(e_b - e_g) \qquad \text{<3.13>}$$

Substituting <3.10> and <3.13> into decision rule <3.6> shows that the following condition has to be satisfied in order to correctly receive the datum:

$$e_b < \frac{m}{4} \qquad \text{<3.14>}$$

In other words, regardless of the number of innocent subbit errors, a bit decision will be wrong if the number of offending subbit errors in one bit interval exceeds *m/4*. So the bit error probability of the FSK demodulator, $P_{e,FSK}$, is equal to the probability of having more than *m/4* offending subbit errors in one bit interval. That is, assuming *m* to be divisible by 4,

$$P_{e,FSK} = \left[\sum_{i=0}^{\frac{m}{4}-1} \binom{\frac{m}{2}}{i} \varepsilon^{\frac{m}{2}-i}(1-\varepsilon)^{i}\right] + \left[\frac{1}{2}\binom{\frac{m}{2}}{\frac{m}{4}} \varepsilon^{\frac{m}{4}}(1-\varepsilon)^{\frac{m}{4}}\right] \quad \text{<3.15>}$$

where ε, the subbit error probability, is dependent upon channel noise statistics and signal amplitude. Under Nyquist sampling condition in AWGN with one-sided power spectral density N, ε is given by [28]

$$\varepsilon = \frac{1}{2} erfc \sqrt{\frac{E}{mN}} \quad \text{<3.16>}$$

where E denotes the bit energy.

The demodulation mechanism of the semi-coherent MSK demodulator is identical to that of the coherent FSK demodulator except that a different decision rule is applied. In this case, to correctly receive, for example, a 0, it is necessary that:

$$|c_0| > |c_1| \Leftrightarrow |A_0 - D_0| > |A_1 - D_1| \quad \text{<3.17>}$$

Depending on the signs of c_0 and c_1, this condition can be rewritten in four different ways:

$$\textit{Case } 1: \quad (A_0 - D_0) > (A_1 - D_1) \Rightarrow e_b < \frac{m}{4} \quad \text{<3.18>}$$

$$\textit{Case } 2: \quad (A_0 - D_0) > (D_1 - A_1) \Rightarrow e_g < \frac{m}{4} \quad \text{<3.19>}$$

$$\textit{Case } 3: \quad (D_0 - A_0) > (A_1 - D_1) \Rightarrow e_g > \frac{m}{4} \quad \text{<3.20>}$$

$$Case\ 4:\ (D_0-A_0) > (D_1-A_1) \Rightarrow e_b > \frac{m}{4} \qquad \text{<3.21>}$$

Thus the probability of correctness of the MSK binary demodulator, $P_{c,MSK}$, is given by

$$\begin{aligned} P_{c,MSK} = {} & P(case\ 1,\ e_b<\frac{m}{4}) + P(case\ 2,\ e_g<\frac{m}{4}) \\ & + P(case\ 3,\ e_g>\frac{m}{4}) + P(case\ 4,\ e_b>\frac{m}{4}) \end{aligned} \qquad \text{<3.22>}$$

This leads to

$$\begin{aligned} P_{c,MSK} = {} & P(e_t<\frac{m}{2},\ e_b>e_g,\ e_b<\frac{m}{4}) + P(e_t<\frac{m}{2},\ e_b<e_g,\ e_g<\frac{m}{4}) \\ & + P(e_t>\frac{m}{2},\ e_b>e_g,\ e_g>\frac{m}{4}) + P(e_t>\frac{m}{2},\ e_b<e_g,\ e_b>\frac{m}{4}) \end{aligned} \qquad \text{<3.23>}$$

Simplifying,

$$P_{c,MSK} = P(e_b<\frac{m}{4},\ e_g<\frac{m}{4}) + P(e_b>\frac{m}{4},\ e_g>\frac{m}{4}) \qquad \text{<3.24>}$$

But due to orthogonality,

$$P(e_b \begin{matrix} > \\ < \end{matrix} \frac{m}{4}) = P(e_g \begin{matrix} > \\ < \end{matrix} \frac{m}{4}) \qquad \text{<3.25>}$$

From <3.24>,

$$P_{c,MSK} = (1 - P_{e,FSK})^2 + (P_{e,FSK})^2 \qquad \text{<3.26>}$$

And therefore, the probability of error, $P_{e,MSK}$, is

$$P_{e,MSK} = 2P_{e,FSK}(1 - P_{e,FSK}) \qquad \text{<3.27>}$$

which, not surprisingly, is identical to the BER expression cited in Section 3.3.2 for the continuous-time MSK demodulator. Again, in the limit of small ε, $P_{e,MSK}$ is twice as much as $P_{e,FSK}$.

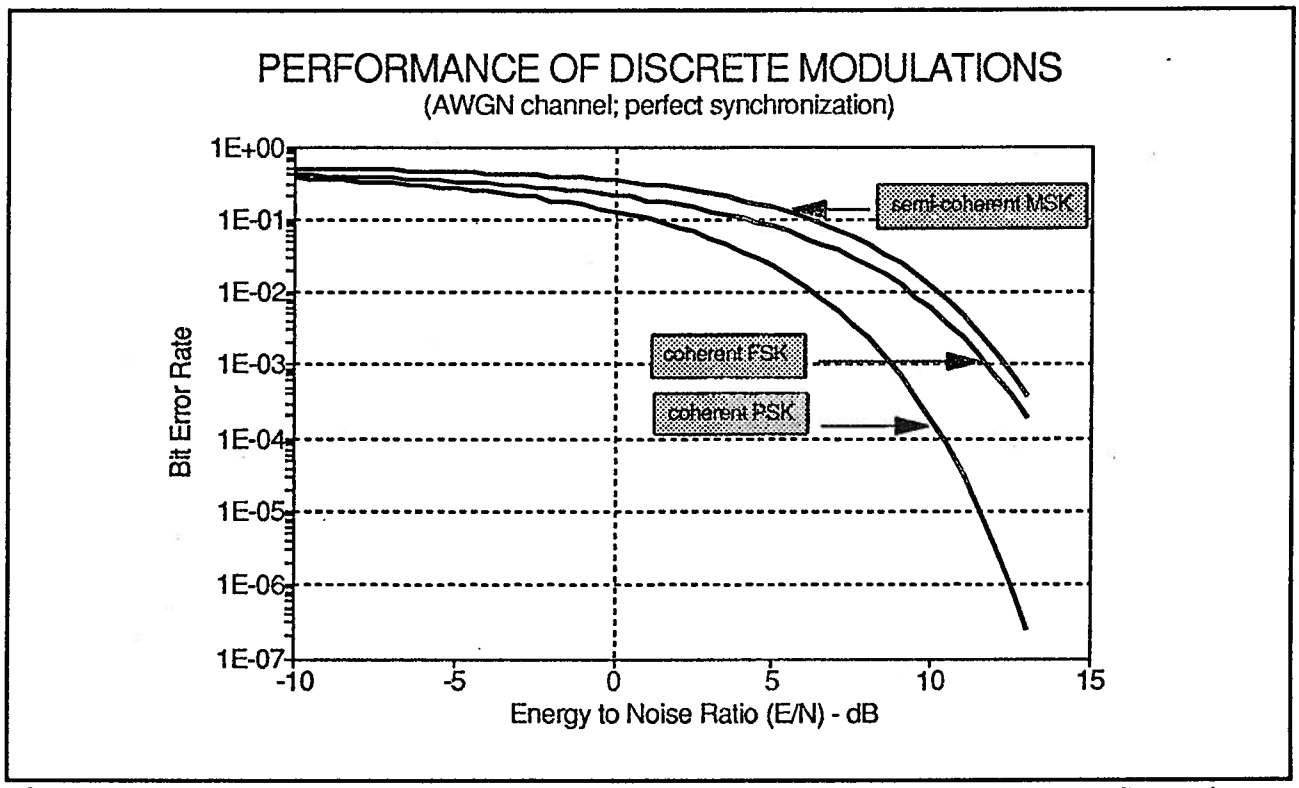


Figure 3.13: BER performance of the binary partial demodulators for coherent PSK, coherent FSK, and semi-coherent MSK.

Plotted in Figure 3.13 are the theoretical BER curves of the coherent PSK [27], coherent FSK, and semi-coherent MSK binary partial decision demodulators in AWGN under perfect carrier and bit synchronization condition. As expected, coherent PSK is superior to coherent FSK, which, in turn, is ever so slightly better than semi-coherent MSK. Additionally, in terms of energy to noise ratio (*E/N*), the discrete MSK demodulator is about 2 dB less efficient than its analog counterpart (dotted curve). Understandably, the degradation is caused by digital quantization and time-sampling effects.

Imperfect Carrier Synchronization

Consider the reception of a space bit by the discrete FSK demodulator with imprecise

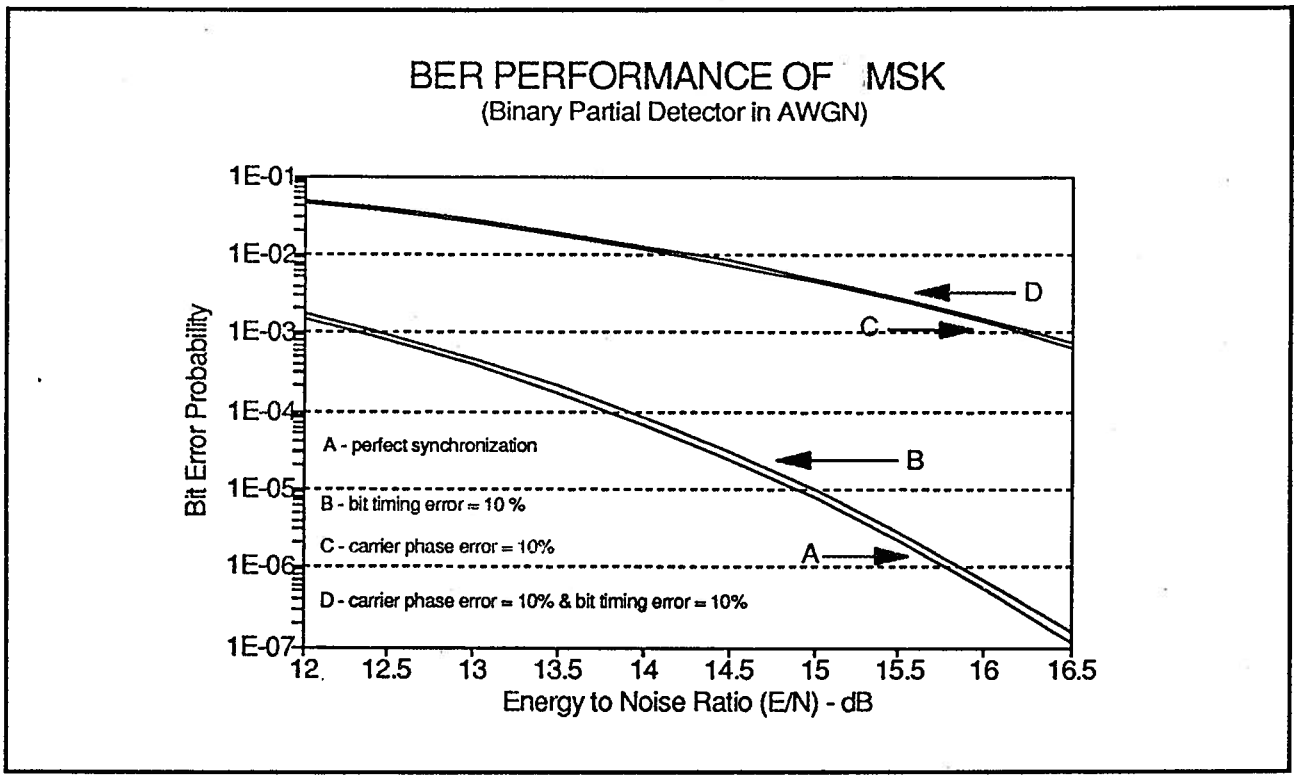


Figure 3.14: Theoretical BER performance of the semi-coherent MSK binary demodulator under different conditions in AWGN.

carrier synchronization. Even in the absence of channel noise, the space frequency correlator will detect polarity disagreement in some subbits. These "systematic" subbit errors are attributed to the fact that the local carrier is offset from the received carrier. The number of disagreement is equal to $2nc$, n being the number of subbits by which the local carrier is offset, and c the average number of carrier cycles in T. Under this circumstance, an incorrect bit decision would be reached as long as the number of noise-induced (random) subbit errors exceeds

$$\frac{1}{2}\left(\frac{m}{2} - 2nc\right) \qquad \text{<3.28>}$$

So the probability of error expression $P_{e,FSK}$ becomes

$$P_{e,FSK} = \sum_{j=0}^{2nc} \binom{2nc}{j} \varepsilon^{j}(1-\varepsilon)^{2nc-j}\Bigg[\sum_{\frac{m}{4}-nc+\frac{j}{2}+1}^{\frac{m}{2}-nc} \binom{\frac{m}{2}-nc}{i} \varepsilon^{i}(1-\varepsilon)^{\frac{m}{2}-nc-i} + \frac{1}{2}\binom{\frac{m}{2}-nc}{\frac{m}{4}-nc+\frac{j}{2}} \varepsilon^{\frac{m}{4}-nc-\frac{j}{2}}(1-\varepsilon)^{\frac{m}{4}+\frac{j}{2}}\Bigg] \quad \text{<3.29>}$$

The probability of error of the discrete MSK demodulator, $P_{e,MSK}$, in the presence of carrier synchronization error can be obtained simply by substituting <3.29> into <3.26>. Curve C in Figure 3.14 corresponds to the AWGN performance of the discrete MSK demodulator that suffers from a carrier phase error of 10%.

Imperfect Bit Synchronization

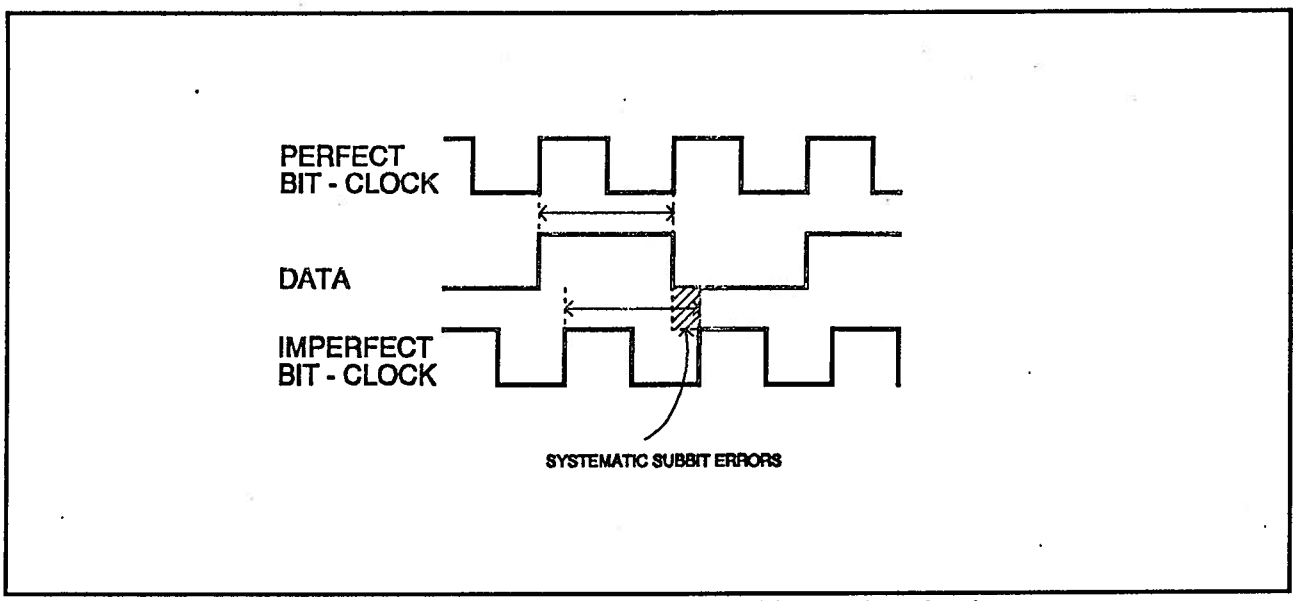


Figure 3.15: Detection degradation effect of imperfect bit synchronization.

Assume that due to imperfect bit synchronization, the bit clock regenerated in the demodulator is offset by τ (> 0) units from the actual bit interval T. As a consequence, instead of extending over one single bit, the period of integration of the correlators would overlap from one bit to the next. This would lead to performance degradation when the two overlapped bit intervals carry opposite data, because, as illustrated in Figure 3.15, some subbit agreements would be replaced with disagreements and vice versa.

For discrete FSK demodulation, the number of subbit errors caused by bit timing offset equals to the number of polarity mismatch between the two carriers in $[0, \tau]$. With this number denoted by g, the maximum number of noise-induced subbit errors that the demodulator can withstand is reduced to

$$\frac{1}{2}\left(\frac{m}{2} - g\right) \qquad \text{<3.30>}$$

Thus $P_{e,FSK}$ is now given by averaging <3.15> and the following:

$$\sum_{j=0}^{g}\binom{g}{j}\varepsilon^{j}(1-\varepsilon)^{g-j}\Bigg[\sum_{\frac{m}{4}-\frac{g}{2}+\frac{j}{2}+1}^{\frac{m}{2}-\frac{g}{2}}\binom{\frac{m}{2}-\frac{g}{2}}{i}\varepsilon^{i}(1-\varepsilon)^{\frac{m}{2}-\frac{g}{2}-i} + \frac{1}{2}\binom{\frac{m}{2}-\frac{g}{2}}{\frac{m}{4}-\frac{g}{2}+\frac{j}{2}}\varepsilon^{\frac{m}{4}-\frac{g}{2}+\frac{j}{2}}(1-\varepsilon)^{\frac{m}{4}-\frac{j}{2}}\Bigg] \qquad \text{<3.31>}$$

The BER performance of the semi-coherent MSK binary partial decision demodulator can simply be obtained by substituting <3.31> into <3.26>. Curve B in Figure 5.14 represents the result for a bit timing error of 10%. Performance is much less sensitive to bit timing error than it is to carrier phase error.

3.3 Carrier Detection

The carrier detector on the modem chip determines if MSK carrier waves are present in any received input signal. This function is needed to prevent the modem from transmitting while the channel is being utilized by another user in a multiple-access system. Otherwise, transmission collisions would occur, reducing overall channel utilization.

One method of carrier detection is by monitoring the average power at the receive input. When a signal is present, the power detected is usually considerably higher than background noise alone can yield. This kind of "power metering", though, is liable to out-of-band interference. Besides, it can only be rendered with analog components, and is therefore not suitable for implementation in the modem chip.

Another method of carrier detection, that provides better frequency resolution, relies on the operation of the carrier synchronizer loop [29, pp. 200-210]. When a carrier is being received, the loop would be in lock; otherwise it would become out-of-lock. So by monitoring the loop's lock condition, one can determine whether a carrier is present. But this method is not applicable here because the special digital carrier synchronizers used do not lend itself to reliable lock detection. As well, the detection delay associated with lock detection might be unacceptably long because of its direct relation to the lock acquisition time of the synchronizers.

In the MSK modem chip, carrier presence is determined by counting the number of positive zero crossings at the receive input in intervals of duration T_c. In the absence of a carrier, the number of positively-going zero-crossings within an interval should ideally be zero; in the presence of a carrier, this number should be at least f_0T_c. But because of channel noise impairment (e.g. burst errors), the actual count would be below or above these levels. So some threshold value between 0 and f_0T_c is used to decide between carrier absence and presence. If the count is less than the threshold, carrier absence is assumed, and vice versa. Frequency resolution depends on the position of the threshold value. The closer to f_0T_c the threshold is, the higher the resolution becomes. The choice of T_c is somewhat arbitrary, but it should be large enough so that a reasonable number of zero-crossings occur in its duration, and be small enough to keep the detection delay acceptable. The detection delay, which affects channel utilization [12], is about $1.5T_c$.

Finally, there is one subtlety associated with this carrier detection method: detection sensitivity is limited by the threshold or "dead zone" of the external ADC which digitizes the received signal. Any carrier signal with an amplitude below the threshold would be undetected because of lack of zero-crossings at chip input. However, if the threshold is too low, channel noise may be mistaken by the detector as carrier. Therefore, the threshold should be set at a value slightly above average background noise level of the channel.

3.4 Built-In-Self-Test

The built-in self-test (BIST) controller provides the MSK modem chip with the capability to functionally verify its modulation and demodulation circuitry. BIST [30, pp. 1-10] is a quick and convenient way of checking the integrity of critical paths in a VLSI device. BIST also contributes to overall chip testability, and can be used as a manufacturing test on the production floor. The BIST test is run in real-time at normal operating speed without the use of any external test equipment for pattern generation and comparison. At the end of the test, a pass/fail response is issued.

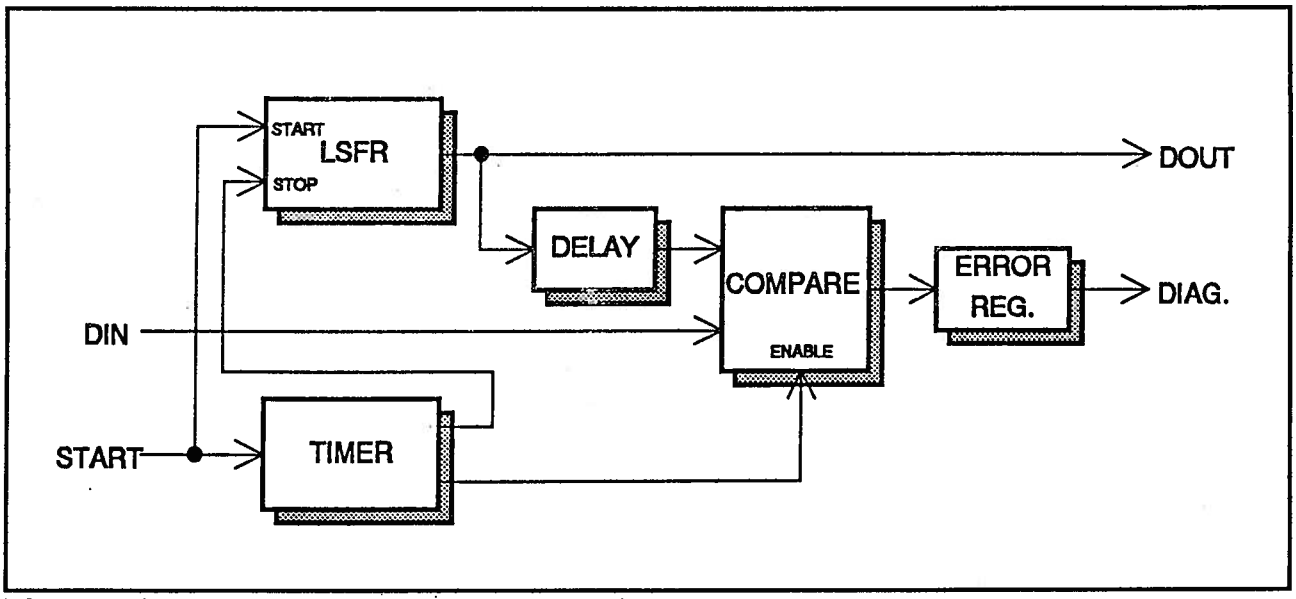


Figure 3.16: Built-in self-test pattern generation.

Upon initiation of BIST, the modem chip enters self-test mode. In this mode, the output of the modulator is connected to the input of the demodulator, thus forming an internal loopback. Then a sequence of test data is used to exercise the modulator. The resulting bit stream output from the demodulator is compared to the input stream. It is a binary output test. Should any mismatch occurs, an error signal will be flagged.

Shown in Figure 3.16 is the block diagram of the BIST controller. The circuit is responsible for the generation of test sequence and detection of compare errors. It makes use of a linear shift feedback register (LSFR) to generate a pseudo-random binary test sequence. An XOR gate compares the input sequence with the output response of the demodulator. Because of processing delay across the loopback path, it is necessary to delay the original sequence with flip-flops before it is actually compared to the demodulated data. Detection of any compare errors during the self-test would set a register to indicate test failure. A "timer" is used to provide timing control. It also ensures that the error detector is not activated until a sufficient number of bits have been transmitted to allow the demodulator to acquire carrier and bit synchronization. If the error detector was enabled too soon, the test outcome would always be negative.

4. ALL-DIGITAL RECEIVER SYNCHRONIZATION

In this chapter, the architectures of the all-digital carrier and bit synchronizers newly developed for MSK demodulation are presented and analyzed.

4.1 Carrier Synchronization

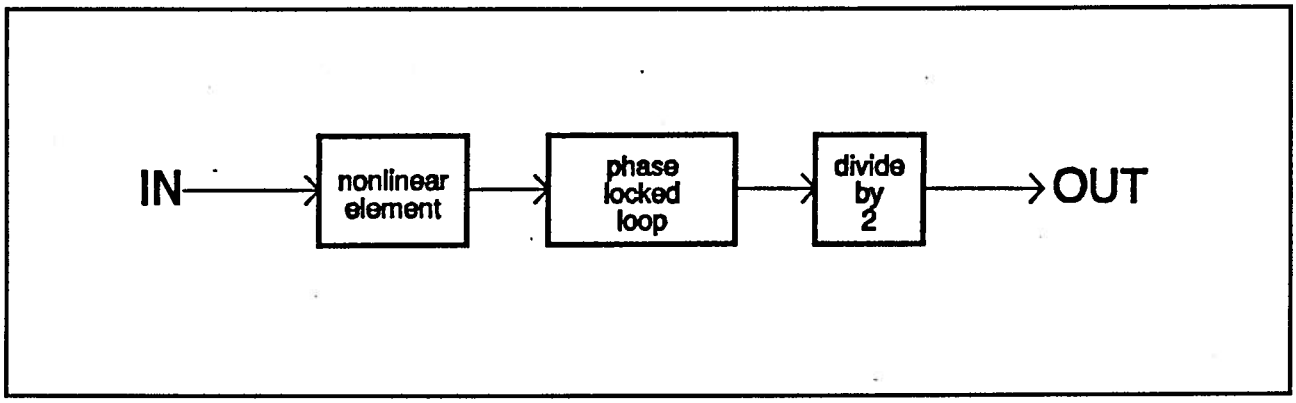


Figure 4.1: Squaring-loop carrier synchronizer.

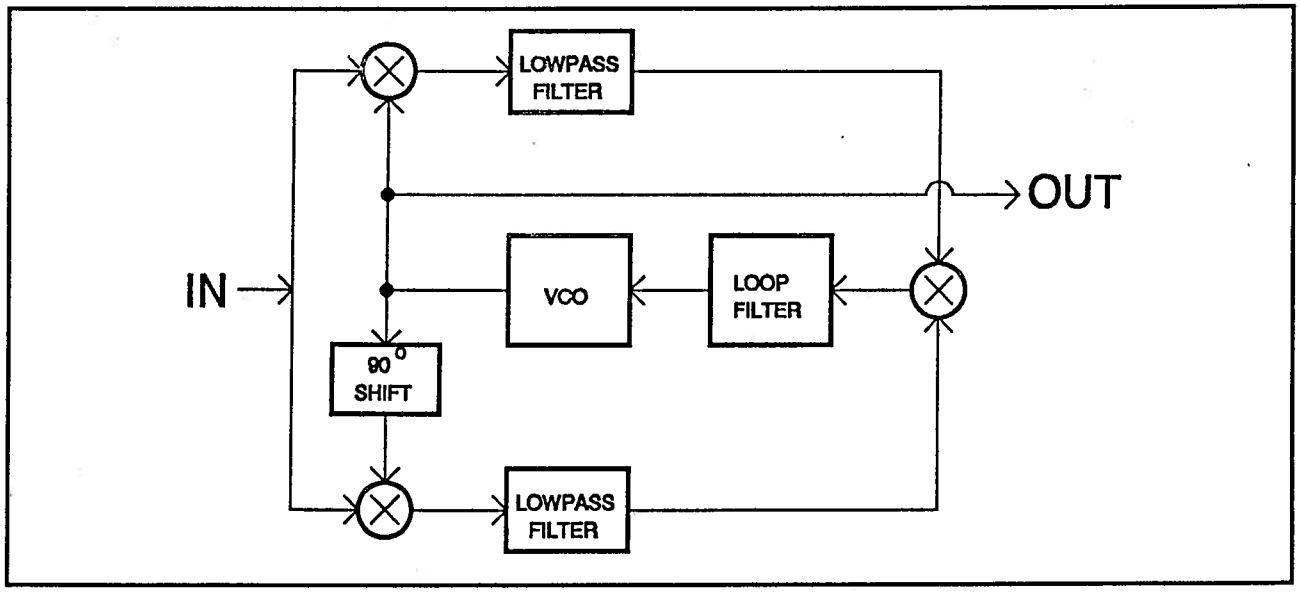


Figure 4.2: Costa's loop carrier synchronizer.

Correlator-based demodulation techniques requires time-aligned replication of signal carriers at the receiver. These replicates are directly extracted from received signals using carrier synchronizers. Carrier synchronizers track the carriers both in frequency and in phase. In the case of semi-coherent MSK detection, two carrier synchronizers are used at the receiver, one to recover the space frequency and the other the mark frequency. Like PSK, MSK is a suppressed carrier modulation scheme, meaning that its signal spectrum contains no discrete components at carrier frequencies. While suppressed carrier modulation has the merit of power efficiency [31], it complicates the carrier recovery process at the receiver.

4.1.1 Suppressed Carrier Recovery

In the analog domain, there are two methods of suppressed carrier recovery: squaring loop and Costa's loop [31]. A squaring loop (Figure 4.1) consists of a nonlinear element which regenerates the discrete components at an harmonic of the carrier frequencies, and a phase-locked loop (PLL) which isolates the harmonic. A Costa's loop, on the other hand, does not use any nonlinear element. Instead it utilizes two PLLs, employing a common controllable oscillator and loop filter, to track the two quadrature components of the incoming signal (Figure 4.2). In theory, the Costa's loop is equivalent to the squaring loop. Yet in general the former is more difficult to analyze and more complicated to implement than the latter [18, pp. 434-453].

Thus, for simplicity and ease of implementation, the all-digital carrier synchronizers on the MSK modem chip are designed on the basis of the squaring loop approach. But, unlike a conventional squaring loop, the design contains no nonlinear element. It simply consists of a digital phase-locked loop that is capable of recovering the carrier directly from MSK signals.

4.1.2 Phase-Locked Loop Basics

Typically, a PLL is made up of three components: phase detector, loop filter, and controllable oscillator (Figure 4.3). Its operation is based on negative feedback: the phase detector compares the phase of the oscillator to that of the input; the resulting error signal is used to "steer" the oscillator so that its output tracks the input in both frequency and phase. The loop filter conditions the error signal and controls feedback dynamics. Incidentally, when the transfer function of its loop filter has n poles, a PLL is said to be of $(n+1)^{th}$ order [32, pp. 8-24].

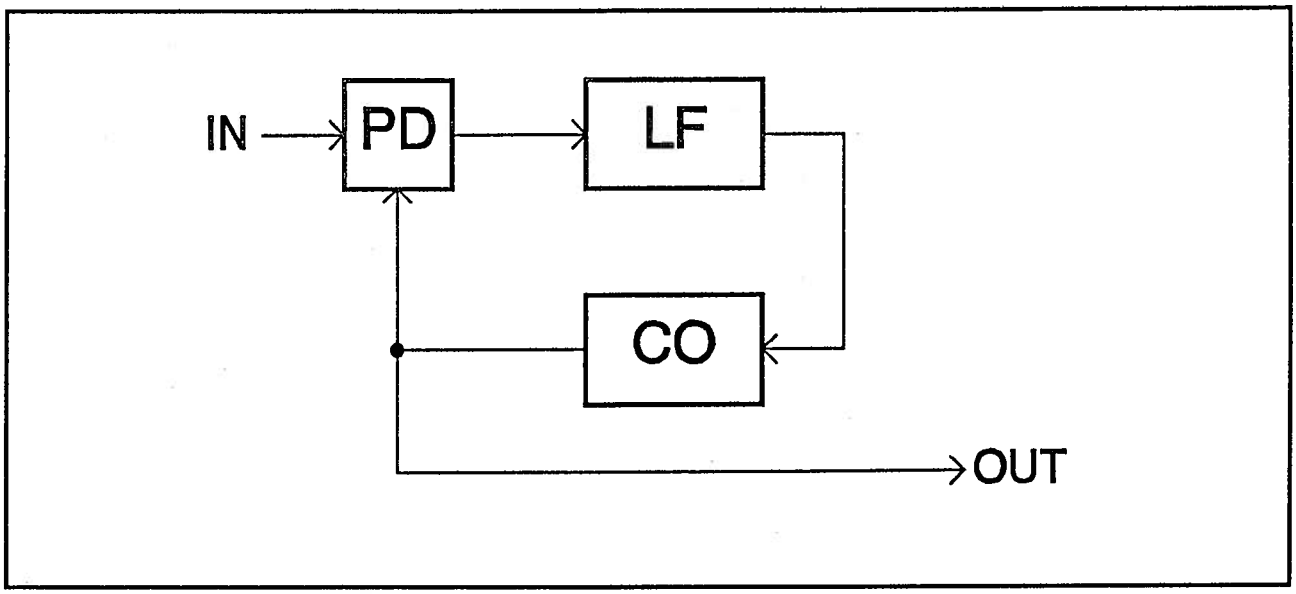


Figure 4.3: Structural representation of a phase-locked loop.

Analog phase-locked loops (APLLs) operate in continuous-time and are implemented using analog devices [33, pp. 9-24]. Usually, the output of an APLL is sinusoidal, generated from a voltage controlled oscillator (VCO). Digital components are used in digital phase-locked loops (DPLLs) [34, pp. 69-115]. Most DPLLs employs a digital structure called numerically controlled oscillator (NCO) to generate a square wave output. DPLLs operate in discrete-time as a sampled-data system, with phase comparison and oscillator adjustments made periodically.

The performance of an APLL or DPLL is characterized by its phase error, phase jitter, and acquisition time. Phase error corresponds to the steady state average phase difference between recovered signal and actual signal, and is a measure of loop accuracy. Phase jitter refers to the phase variance of loop output, and is a measure of stability. Loop acquisition time is that time required for the loop to "search for" and "lock onto" the input signal that it tracks. The conflicting goals in PLL design are the minimization of these three parameters.

4.1.3 An All-Digital MSK Carrier Synchronizer

The two carrier synchronizers on the MSK modem chip are structurally identical. Each is a first-order DPLL, one tuned to f_0 and the other f_1. According to the classification suggested by Lindsey and Chie [35], a ZC-DPLL performs phase detection by sampling at zero-crossings of the local signal, while a LL-DPLL determines at each cycle whether the input leads or lags

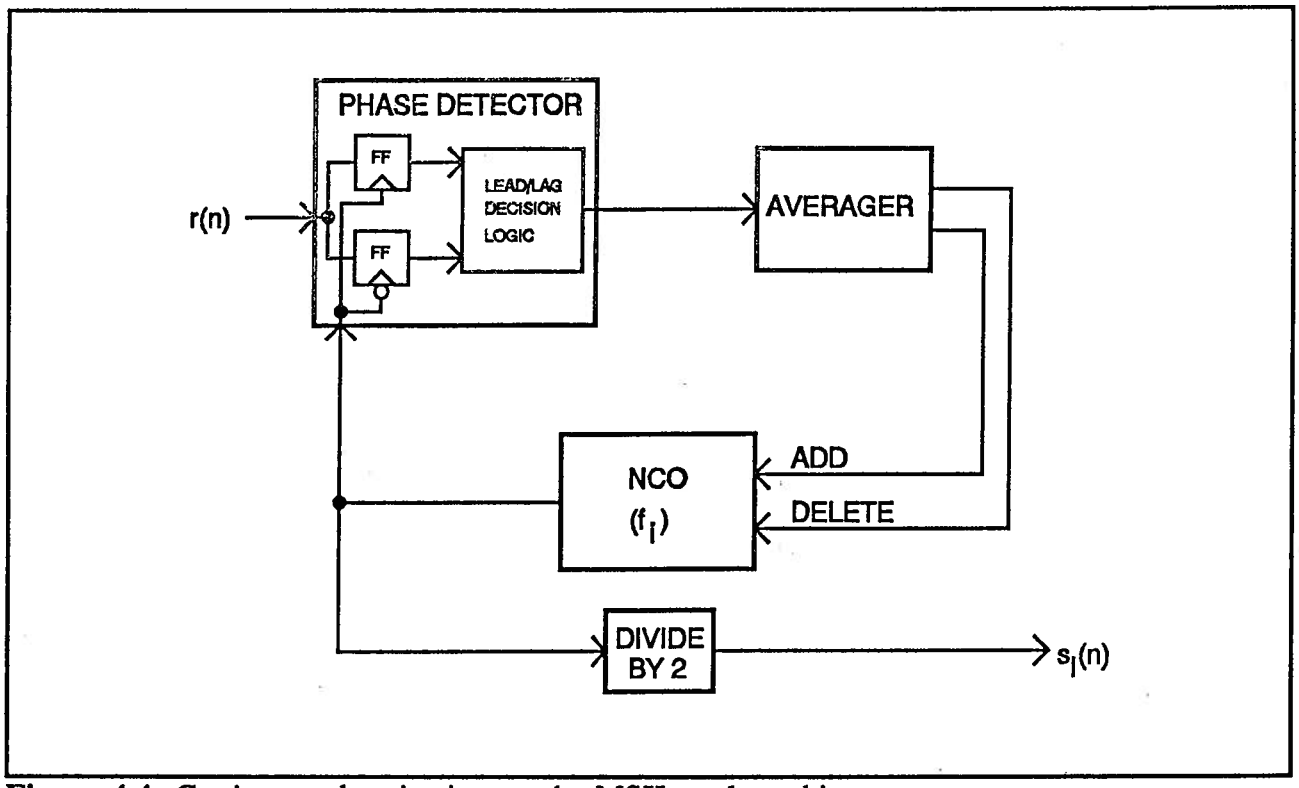


Figure 4.4: Carrier synchronization on the MSK modem chip.

the local signal. The MSK carrier synchronizer DPLL can be considered as a hybrid of these because it uses a zero-crossing-based phase detection scheme while operating like a LL-DPLL. In addition, unlike other so-called N-th order DPLLs proposed for suppressed carrier recovery [36], this DPLL does not require any zonal filter and/or nonlinear device at the front end.

The carrier synchronizer's block diagram appears in Figure 4.4. The square wave output from the NCO is at twice the carrier frequency to be tracked. Its zero-crossings are used by the phase detector to sample the modulated carrier. Twice every cycle, the phase detector determines whether the NCO output is leading or lagging the actual carrier. These lead/lag decisions are subsequently processed by the loop filter, which then instructs the NCO to either advance or delay its output. Finally, the coherent local carrier is obtained by dividing down the NCO output.

To enable the loop to extract the suppressed carrier from the MSK signal without using an external nonlinear element, a special zero-crossing-based phase detection algorithm is developed. This algorithm works as follows: first, the modulated signal is sampled on the rising edge of the local carrier; then another sample is taken on the falling edge; if the two samples

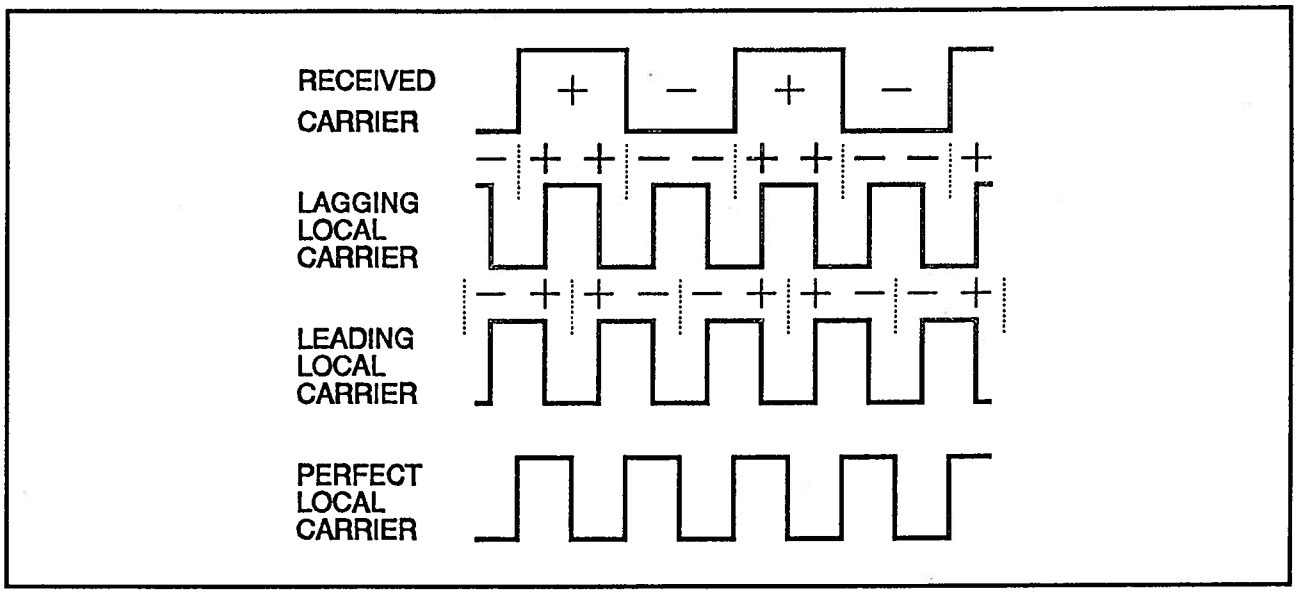


Figure 4.5: Phase detection for carrier recovery in the MSK modem.

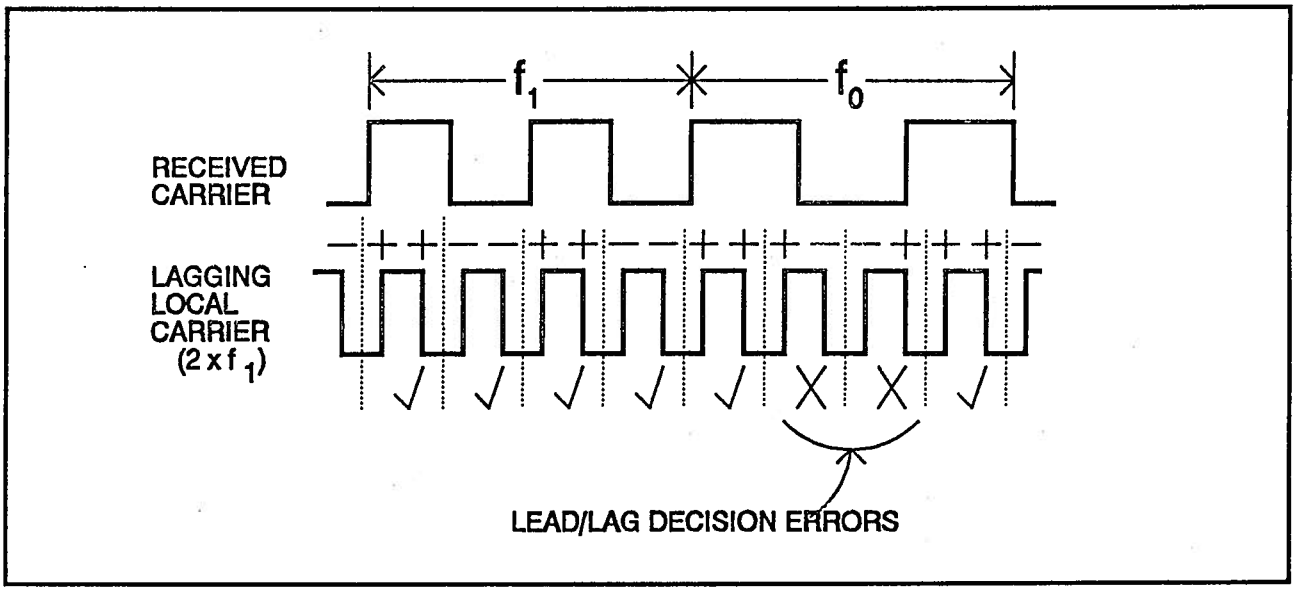


Figure 4.6: Phase detection errors due to reception of a non-tracking frequency component.

have the same polarity, the local carrier is lagging; otherwise, it is leading. Validity of this "like lag, unlike lead" algorithm is demonstrated in Figure 4.5 considering all four possibilities.

Still, some of the lead/lag decisions reached by the phase detector can be erroneous. There are two sources of errors. First, the input signal may be randomly corrupted by channel noise. Second and more important, the phase detector tracking one carrier frequency is subjected to interference from the other carrier frequency also present in MSK signals. This problem is

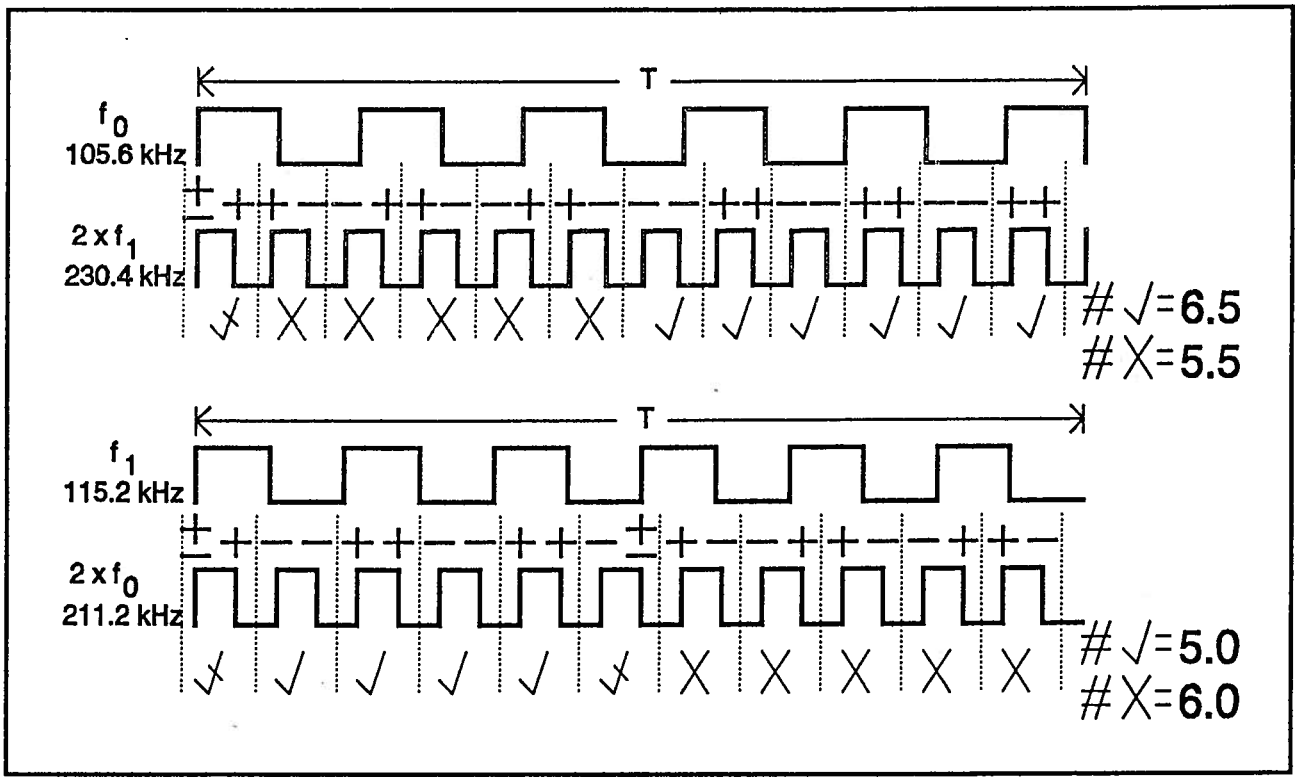


Figure 4.7: Lead/lag errors over one bit interval.

illustrated in Figure 4.6. Incidence of a second carrier frequency (in this case f_0) makes the local carrier signal appear to be leading at some instants despite that it is actually lagging behind the carrier frequency it is supposed to track. Thus it is necessary to "suppress" the effect of these misleading lead/lag decisions on the loop. This suppression is the responsibility of the loop filter.

The loop filter is a kind of sequential filter [37]. It counts the number of leads and lags detected over U samples. Majority voting is then applied to decide the actual lead/lag condition. For example, if there are more leads than lags, the local signal is decided to be leading. This approach is equivalent to "time averaging" the phase detector output. It is feasible for two reasons. First, as a result of channel noise randomness, signal statistics will tend to stand out from noise statistics. A time averaged decision has a higher SNR than individual decisions. Second, as shown in Figure 4.7, over a bit interval in which the offending frequency is received, the lead count and lag count are approximately equal; over a number of consecutive bit intervals, these frequency-induced errors would also be overridden by signal statistics.

Next, the loop filter adjusts the NCO according to the majority lead/lag decision over U

samples. The NCO generates the local carrier by dividing down a base clock. If the local carrier is leading, a base clock cycle will be added to delay the output; if the local signal is lagging, a base cycle will be deleted to advance the output.

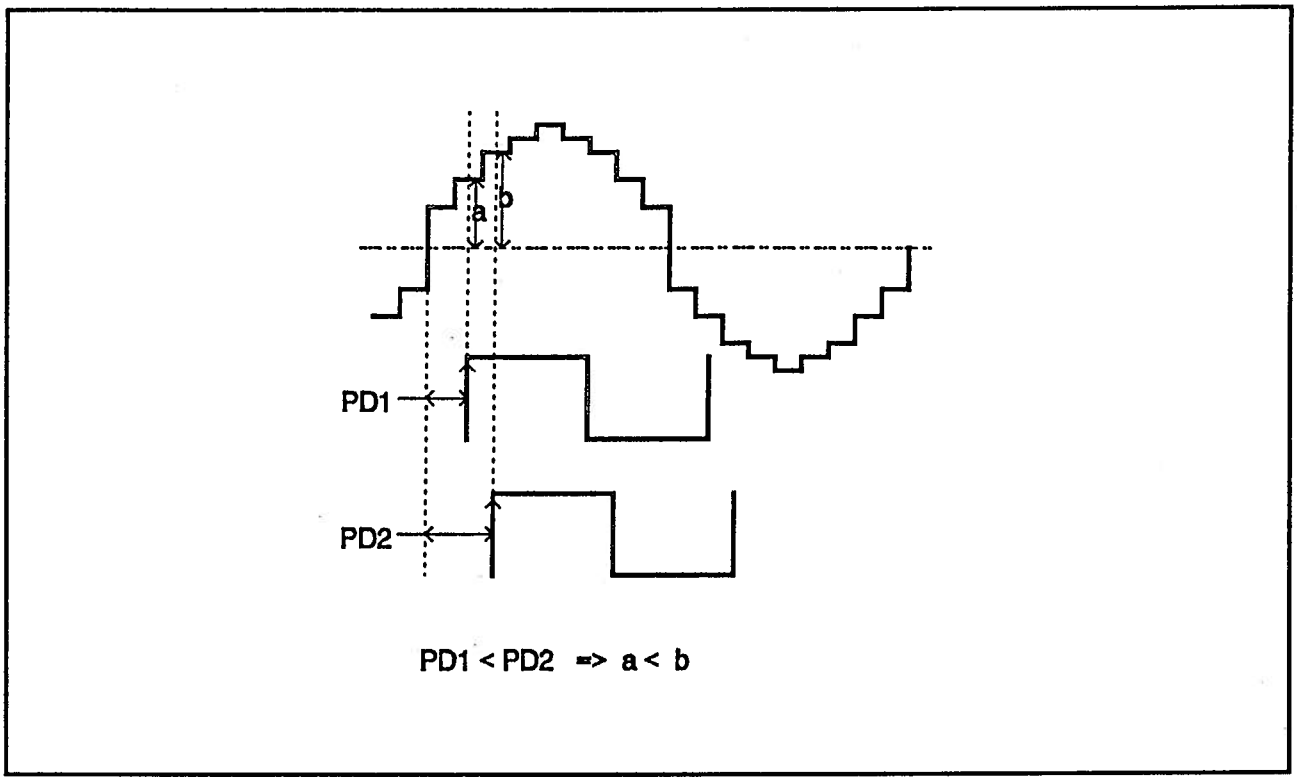


Figure 4.8: Improved detection of phase error.

In addition, for more versatility and higher performance, two enhancements are made, one to the phase detector, and the other to the loop filter:

1. In an initial design, it was mandatory that the input signal be hardlimited to square wave. However, the input can now also be presented to the carrier synchronizer as a 4-bit digitized sinusoid by using an external 4-bit ADC. A multi-bit input allows the phase detector to determine not only the direction but also the magnitude of phase difference between the input signal and local signal. Availability of magnitude information helps improving the accuracy and effectiveness of loop filtering process. As before, in each signal cycle, the input is sampled twice, the first on the rising edge and the second on the falling edge. But the phase decision is now a 4-bit binary number in sign-magnitude representation. Its sign reflecting the lead/lag relation is determined from the polarities of the two samples using the "like lag, unlike lead" rule. Its

magnitude is adopted from the first sample, which, as shown in Figure 4.8, is proportional to the phase difference.

2. The loop filter provides negative feedback control of the NCO according to phase detector decisions. Initially, each NCO adjustment was limited to one base clock cycle regardless of the phase error. However, the loop filter is modified to allow correction of the NCO output by either 1 or 2 base clock cycles at a time according to the size of the lead/lag statistics. Specifically, the following algorithm is used to determine the number of clock cycle that is to be added or deleted from the NCO output:

if AVG < LOW => no correction
else if LOW < AVG < HIGH => 1-step correction
else if HIGH < AVG => 2-step correction

where *AVG* is the computed lead/lag average, *LOW* the lower threshold, and *HIGH* the upper threshold. This algorithm has two benefits. First, the phase jitter of DPLL output is reduced as a result of the first condition, which states that no correction will be made unless the average exceeds the lower threshold. Second, the lock acquisition time of the DPLL is improved by introducing the third condition, which doubles the correction step if the average exceeds the upper threshold. The algorithm's validity is independent of the digitization level of the phase detector, although slightly better performance is expected with multi-bit sampling [35].

Note that the carrier recovered by the synchronizer can either be in-phase or 180° out-of-phase with the actual carrier. But this phase ambiguity problem has no avail here because only the magnitude of the correlator outputs matter in the MSK decision rule (see <3.7>).

4.1.4 Performance Analysis

DPLL operation can be analyzed theoretically in three ways. The first is by studying the dynamics of loop feedback mechanism in discrete domain. It involves discrete modelling of loop components, and deriving and solving difference equations [35]. This method is generally applicable to any kinds of DPLL. The second approach is to model loop operation as a discrete Markov process with a finite number of states [38, 39]. This approach involves state specification and calculation of state transition probabilities, and is mathematically complex if not intractable, and is therefore only applicable to simple DPLL systems. A third approach is to model the DPLL

as an APLL [40]. This "equivalent analog model" technique is acceptable if the DPLL step size is small as compared to the period of the synchronizing signal.

As shown below, the steady state and transient performance of the MSK carrier synchronizer DPLL can readily be analyzed with Markovian technique. In the analysis, the received carrier is assumed to be square wave and be hardlimited prior to entering the synchronizer.

Steady State Behaviour

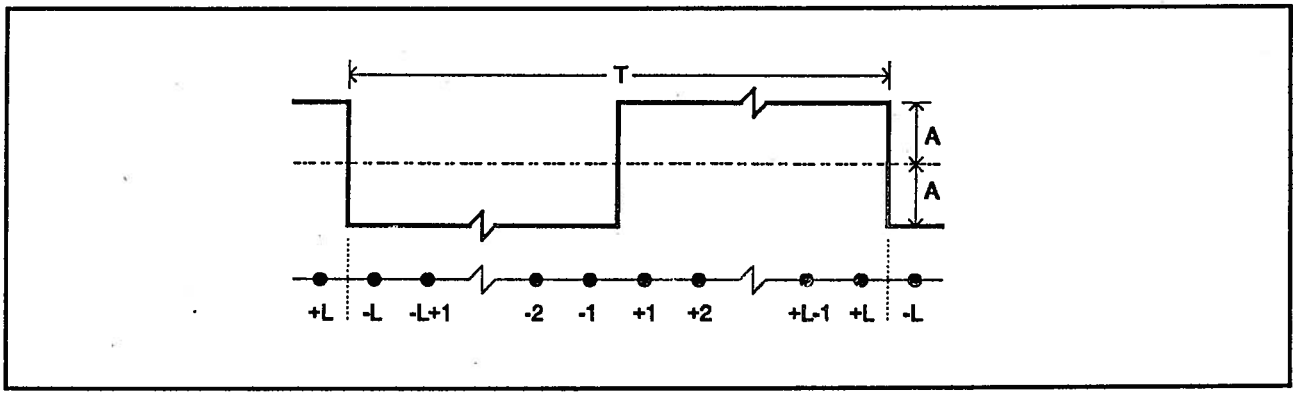


Figure 4.9: Error states of the all-digital MSK carrier synchronizer.

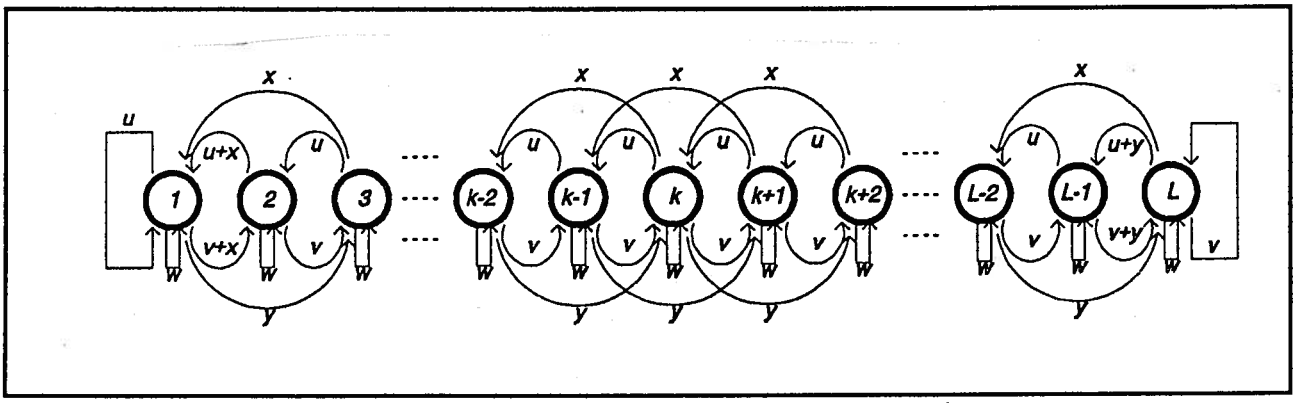


Figure 4.10: State transitions in the all-digital MSK carrier synchronizer.

The MSK carrier synchronizer is modelled as a discrete Markov process, with its states corresponding to the timing error of its output just before it is updated. As indicated in Figure 4.9, the total number of possible states N_s is simply $T/\delta t$, with δt being the size of one correction step. But, owing to symmetry and that we are only interested in computing the absolute error,

the number of states can be halved, with each state corresponding to the absolute offset of the loop output. State transition occurs when the NCO of the loop is updated. Shown in Figure 4.10 is the resulting state transition diagram. It corresponds to a multi-step random walk model with reflective boundaries. The size of each hop is limited to 0, 1, and 2. Parameters u, v, w, x, and y denote the probabilities of state transition: u or v is the probability of decreasing or increasing the offset by δt; x or y is the probability of decreasing or increasing it by $2\delta t$; and w is the probability of null correction. They are functions of phase detection error probability (β) and loop filter parameters (*LOW*, *HIGH*, *U*). Mathematically, with U, the number of lead/lag samples, assumed to be even,

$$u = \sum_{i=\frac{U}{2}-HIGH}^{\frac{U}{2}-LOW-1} \binom{U}{i} \beta^i (1-\beta)^{U-i} \qquad \text{<4.1>}$$

$$v = \sum_{i=\frac{U}{2}+LOW+1}^{\frac{U}{2}+HIGH} \binom{U}{i} \beta^i (1-\beta)^{U-i} \qquad \text{<4.2>}$$

$$x = \sum_{i=0}^{\frac{U}{2}-HIGH-1} \binom{U}{i} \beta^i (1-\beta)^{U-i} \qquad \text{<4.3>}$$

$$y = \sum_{i=\frac{U}{2}+HIGH+1}^{U} \binom{U}{i} \beta^i (1-\beta)^{U-i} \qquad \text{<4.4>}$$

$$w = 1 - u - v - x - y \qquad \text{<4.5>}$$

Quantity β depends on the noise statistics of the phase detection process. As mentioned before,

there are two sources of detection errors: channel noise and frequency interference. The former is extrinsic, and is assumed here to be AWGN with one-sided power spectral density N. The latter is intrinsic, and is caused by frequency shifts in MSK signalling. Without loss of generality, assume that the carrier synchronizer is designed to track the space frequency f_0. Then

$$\begin{aligned}\beta = {} & P(error \mid f_0 \text{ received})P(f_0 \text{ received}) \\ & + P(error \mid f_1 \text{ received})P(f_1 \text{ received})\end{aligned} \qquad \text{<4.6>}$$

For equiprobable transmission of 0's and 1's, <4.6> becomes

$$\beta = \frac{1}{2}[P(error \mid f_0 \text{ received}) + P(error \mid f_1 \text{ received})] \qquad \text{<4.7>}$$

The first term is attributed to channel noise only; from <3.16>,

$$P(error \mid f_0 \text{ received}) = \frac{1}{2}erfc\sqrt{\frac{E}{mN}} \qquad \text{<4.8>}$$

where E = bit energy, and m = number of subbits per bit interval. The second term has to account for both channel noise and frequency shift effect:

$$P(error \mid f_1 \text{ received}) \approx \frac{1}{2}[1-\frac{1}{2}erfc\sqrt{\frac{E}{mN}}] + \frac{1}{2}[\frac{1}{2}erfc\sqrt{\frac{E}{mN}}] = \frac{1}{2} \qquad \text{<4.9>}$$

Therefore, according to <4.7>,

$$\beta = \frac{1}{4}[1+erfc\sqrt{\frac{E}{mN}}] \qquad \text{<4.10>}$$

Now, let p_k denote the probability of occurrence of state k, k ranging from 1 to L ($= N_s/2$). Then, based on the state transition diagram, the following stochastic difference equation can be

written:

$$(1-w)p_k = yp_{k-2} + vp_{k-1} + up_{k+1} + xp_{k+2}, \quad 2<k<L-1 \qquad \text{<4.11>}$$

subjected to reflective boundary conditions

$$\begin{aligned} (1-w-u)p_1 &= (u+x)p_2 + xp_3 \\ (1-w)p_2 &= (v+x)p_1 + up_3 + xp_4 \\ (1-w)p_{L-1} &= yp_{L-3} + vp_{L-2} + (u+y)p_L \\ (1-w-v)p_L &= yp_{L-2} + (v+y)p_{L-1} \end{aligned} \qquad \text{<4.12>}$$

In addition, for normalization, it is required that

$$\sum_{k=1}^{L} p_k = 1 \qquad \text{<4.13>}$$

Equations <4.11-13> can be solved simultaneously to determine the state probabilities p_k's. Once the p_k's are known, the steady state tracking error variance σ^2 of the carrier synchronizer can be calculated as follows:

$$\sigma^2 = \sum_{k=1}^{L} (k - \frac{1}{2})^2 \, \delta t^2 \, p_k \qquad \text{<4.14>}$$

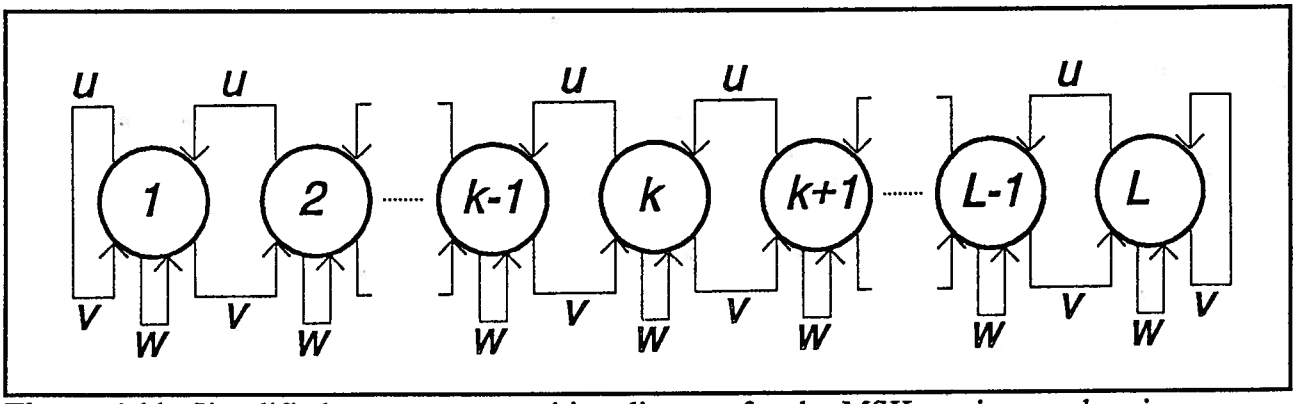


Figure 4.11: Simplified error state transition diagram for the MSK carrier synchronizer.

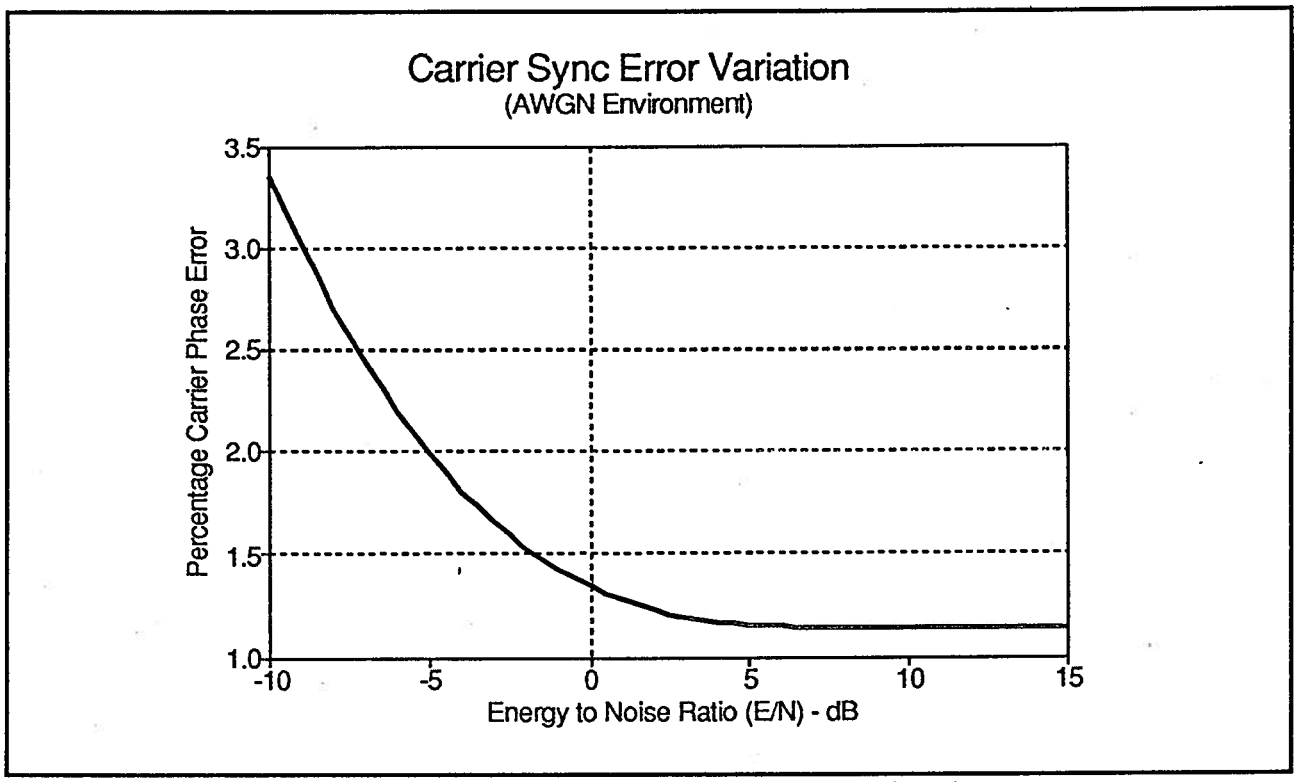


Figure 4.12: Computed output phase variance of the carrier synchronizer.

Unfortunately, in this case, analytic solution of equations <4.11-13> cannot be attained. An alternative is to solve them numerically using the Gauss-Seidel iteration method, as suggested in [41]. This method is not pursued here, though; instead, it is more useful to obtain a closed-form approximation of the solution. In order to do so, the original Markov process is treated as if it contains only unit-step transitions of size δt. This approximation is reasonable because, while in tracking mode, as opposed to acquisition mode, there would be much more zero and one-step transitions than two-step transitions; moreover, when L is large, distinguishability between one-step and two-step transitions actually diminishes. The result is a simplified state transition diagram (Figure 4.11), which is equivalent to that of a classical unit-step random walk problem with reflective boundaries [42, Ch. 14]. Its difference equations are:

$$\begin{aligned} (1-c)p_k &= bp_{k-1} + ap_{k+1}, \quad 1<k<L \\ (1-c-a)p_1 &= ap_2 \\ (1-c-b)p_L &= bp_{L-1} \end{aligned} \qquad \text{<4.15>}$$

In this model, the probability of reducing the error by one step, a, is simply equal to $u + x$; the probability of augmenting the error by one step, b, is equal to $v + y$; and the probability of null correction, c, is the same as w defined above. Solution to equations <4.15> subjected to normalization is well known [42, Ch. 14]:

$$p_k = \frac{1-\alpha}{1-\alpha^L}\alpha^{k-1}, \quad k = 1,...,L \qquad \text{<4.16>}$$

where $\alpha = b/a$. In turn, the state variance is given by

$$\sigma^2 = \frac{\delta t^2}{4} + \frac{\delta t^2}{1-\alpha^L}[-L(L+1)\alpha^L + 2(\frac{\alpha-(L+1)\alpha^{L+1}}{1-\alpha}) + 2(\frac{\alpha^2-\alpha^{L+2}}{(1-\alpha)^2})] \qquad \text{<4.17>}$$

Plotted in Figure 4.12 is the steady error tracking error performance of the MSK carrier synchronizer loop based on the above approximation.

Transient Behaviour

The mean acquisition time (T_A) of the DPLL is defined as the average time taken by the loop to reach the minimum possible phase error (i.e. state 1). Under the assumption of equally likely probabilities of initial state, T_A is given by

$$T_A = \frac{1}{L}\sum_{k=1}^{L} T_a(k) \qquad \text{<4.18>}$$

where $T_a(k)$ is time taken to acquire lock when the loop is initially at state k.

In the absence of noise, it is not hard to see that

$$T_a(k) = (k-1)\cdot U\cdot T, \quad 1 \le k \le L \qquad \text{<4.19>}$$

Thus

$$T_A = \frac{L-1}{2}\cdot U\cdot T \qquad \text{<4.20>}$$

However, in the presence of noise, $T_a(k)$ is governed by the following difference equation:

$$T_a(k) = UT + xT_a(k-2) + uT_a(k-1) + vT_a(k+1) + yT_a(k+2), \quad 3 \le k \le L-2 \qquad \text{<4.21>}$$

bounded by

$$\begin{aligned} T_a(1) &= 0 \\ T_a(2) &= UT + vT_a(3) + yT_a(4) \\ T_a(L-1) &= UT + xT_a(L-3) + uT_a(L-2) + (v+y)T_a(L) \\ T_a(L) &= UT + xT_a(L-2) + (u+y)T_a(L-1) + uT_a(L) \end{aligned} \qquad \text{<4.22>}$$

Numerical solution of the above for the $T_a(k)$'s is possible [41]. In general, the smaller L is, the smaller T_A becomes. Thus a design trade-off exists between the acquisition time and tracking accuracy of the DPLL.

General Signal Case

In the analysis presented above, the incoming signal is assumed to be square wave. When this is not the case (e.g. sinusoidal input), β, and therefore the state probabilities, are no longer constant, but vary with the error state of the system. The consequence is a considerable increase in computational complexity [38].

Frequency Lock Range

Also worth calculating is the frequency lock range f_{range} of the DPLL. It refers to the maximum possible frequency deviation, or "detuning," of loop output in tracking mode. This parameter is critical in designing the MSK carrier synchronizer because the incoming signal contains two carrier frequencies separated only by $R/2$. To prevent false locking, the f_{range} of the carrier synchronizer should be much less than $R/2$.

For large L, f_{range} of the carrier synchronizer is given by

$$f_{range} \approx 2\left(\frac{maximum\ number\ of\ phase\ hops\ per\ cycle}{total\ number\ of\ phase\ states\ per\ cycle}\right)f_l \approx 2\left(\frac{2/U}{2L}\right)f_l = \frac{2}{UL}f_l \quad \text{<4.23>}$$

where f_l is the DPLL's free running frequency.

4.2 Bit Synchronization

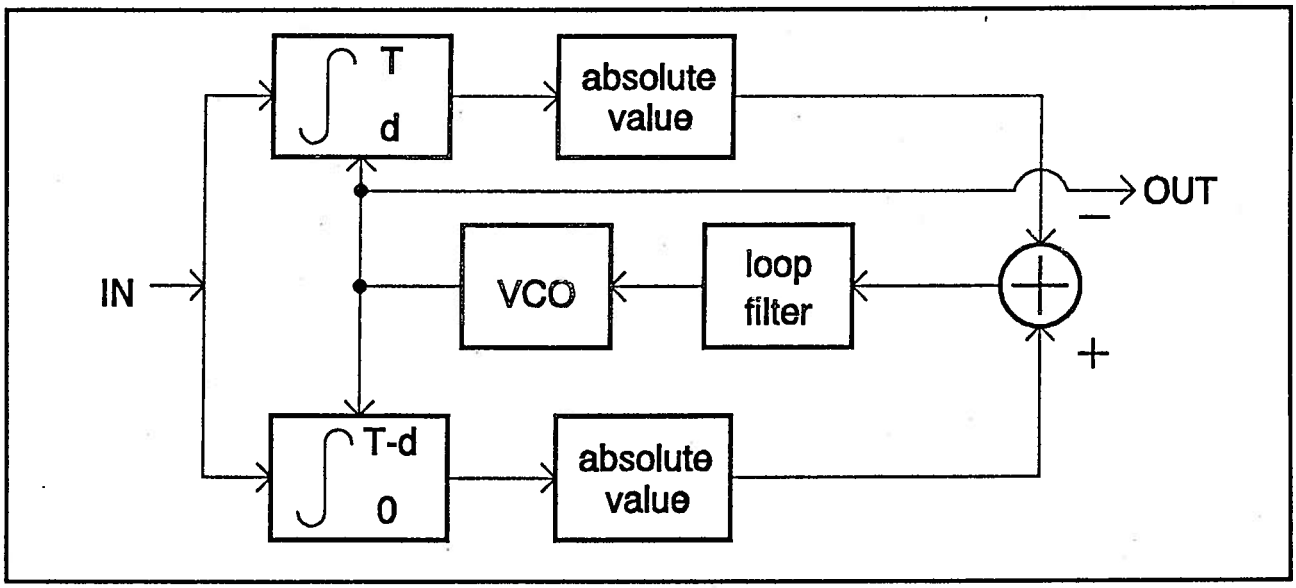


Figure 4.13: Early-late gate bit synchronizer.

The receive bit clock is required at the correlation receiver to time the demodulated data and, more importantly, to reset the correlators at the end of each bit interval. Usually, bit clock recovery is from demodulated baseband waveform. In a correlator-based demodulator, one can generate the baseband waveform by low-pass filtering the output of the multiplier. When NRZ data encoding is used, the spectrum of the baseband waveform contains no discrete component at bit clock frequency. In such case, bit synchronization is not unlike suppressed carrier recovery. One way of bit synchronization is to use the squaring loop mentioned in Section 4.1.1. But again, a nonlinear element, not amenable to digital implementation, is needed. An alternative is the early-late gate technique (Figure 4.13). Here a PLL is used in which phase detection is achieved

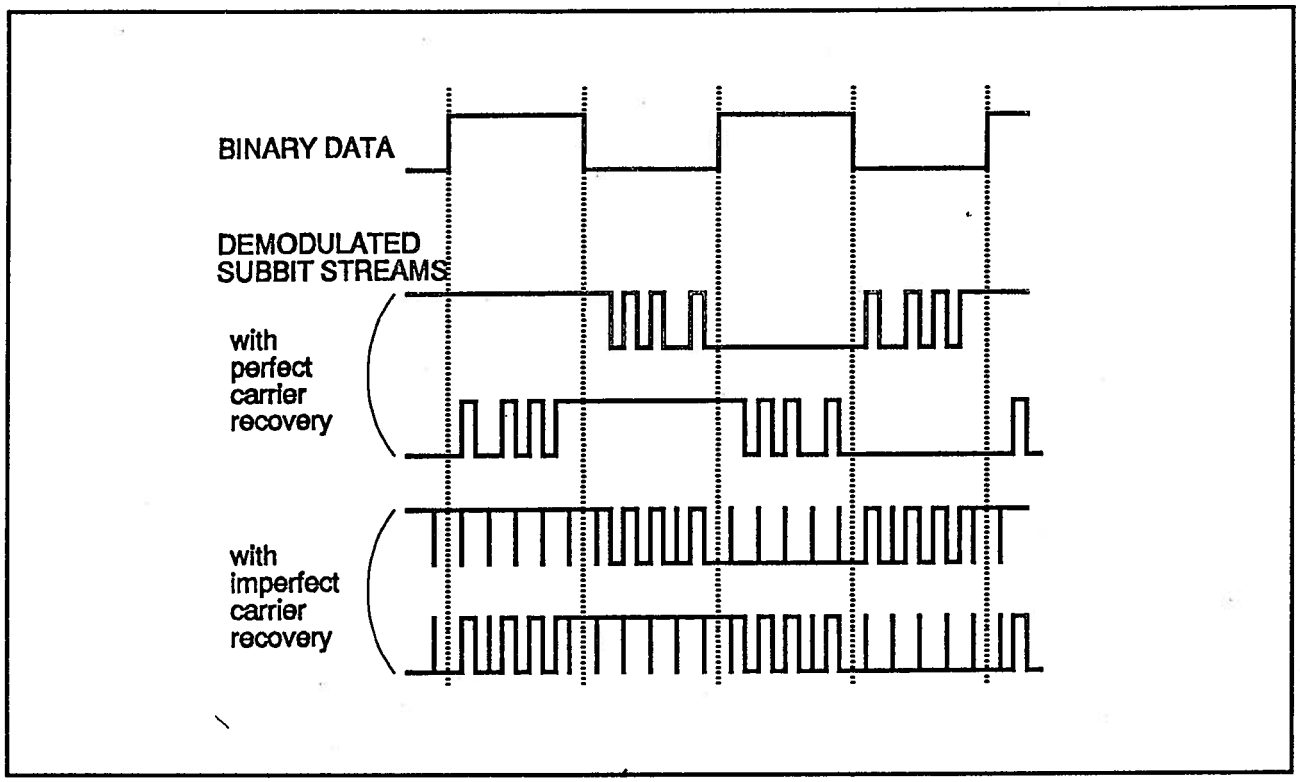


Figure 4.14: Effect of carrier phase error on demodulated bit streams.

with a pair of correlators. One correlator integrates the incoming data over an early portion of the local bit clock, and the other integrates over a late portion. The difference between these two time-shifted correlations provides a measure of the offset of the local bit clock from the bit timing of incoming data. Detailed discussions of early/late gate synchronizers may be found in [18, pp. 453-460].

4.2.1 An All-Digital MSK Bit Synchronizer

For use in the semi-coherent MSK modem chip, an unconventional but innovative bit synchronizer is designed. Conventional bit synchronizer structures are inappropriate because the baseband waveform is unavailable from the MSK demodulator for bit timing extraction. Instead, bit clock timing information is "hidden" in two subbit streams, one from each of the two XOR multipliers. The state of each stream corresponds to the polarity agreement/disagreement between local and received carriers. Zero-crossings in these streams bear no relationship to data bit transition. To make matters worse, owing to imperfect carrier synchronization, the two streams

are contaminated with high frequency transitions. They appear to be "spiky", spike width proportional to the carrier phase error (Figure 4.14).

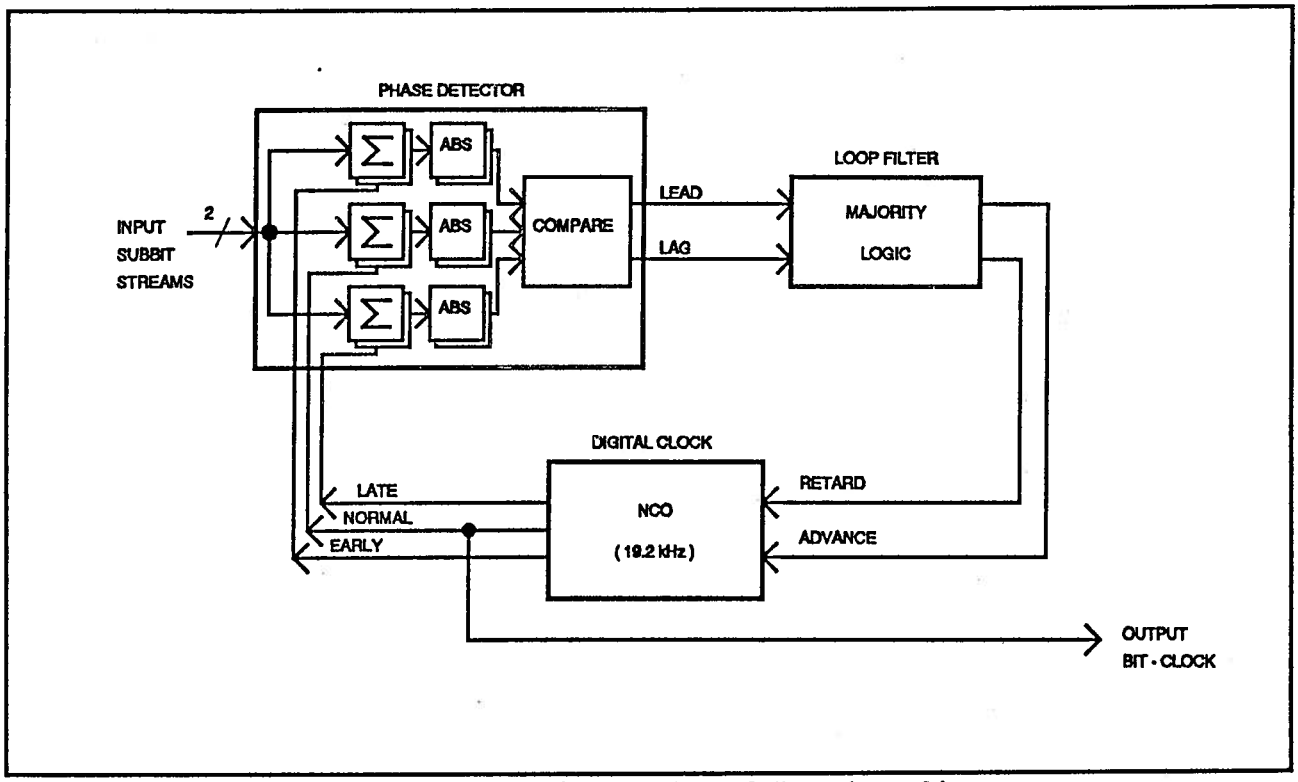


Figure 4.15: The all-digital bit synchronizer on the MSK modem chip.

Nonetheless, during each bit interval, a high density of polarity agreement or disagreement can always be found in either one of the two streams. The end of a high density region on one stream and the subsequent beginning of a high density region on the other stream mark a data transition. This suggests that one can search the bit boundary by monitoring the concentration of polarity agreement and disagreement in the two streams. It is exactly this fact that the MSK bit synchronizer exploits to extract bit timing directly from the two spiky streams.

The block diagram of the all-digital MSK bit synchronizer is shown in Figure 4.15. Like the carrier synchronizer, the bit synchronizer is basically a lead-lag-based first-order DPLL. The local bit clock which tracks receive bit timing is generated by a NCO that is periodically adjusted via negative feedback from the phase detector and loop filter. The phase detector determines whether the bit clock is leading or lagging with reference to the actual bit clock embedded in the two input subbit streams. How this is achieved is explained in the next section. After deciding

the majority of the lead/lag statistics over J samples, the loop filter instructs the NCO to adjust the output bit clock. When the bit clock is detected to be leading, it is retarded by one base clock cycle, and when lagging, advanced by one base clock cycle.

4.2.2 Decision-Aided Phase Detection

Unlike the phase detector used for carrier synchronization, this phase detector does not use the zero-crossings of the local clock to sample the input. Instead, inspired by the early/late gate technique, the phase detector integrates the input with the local bit clock (BCKN), an early version of it (BCKE), and a late version if it (BCKL). All three clocks are generated by the NCO, with the early and late clocks at equal distance apart from the nominal clock. Each clock is used to compute two integrals, one from each of the two subbit streams. So, a total of six integrals are obtained, each a measure of the density of polarity agreement or disagreement in one subbit stream over a bit interval. Next, the two integrals over BCKN are compared in magnitude. Let the greater of the two be denoted by I_N. Then I_N is compared to the other two integrals computed from the same subbit stream as I_N over BCKE and BCKN, Let these latter two integrals be denoted by I_E and I_L, respectively. A lead/lag decision is reached using the following "maximum seeking" rule:

$$\begin{aligned} &\textit{if } |I_E| < |I_N| < |I_L| \;\Rightarrow \textit{leading} \\ &\textit{else if } |I_E| > |I_N| > |I_L| \;\Rightarrow \textit{lagging} \\ &\textit{else} \;\Rightarrow \textit{inconclusive} \end{aligned}$$

This decision rule is founded on the basis that the more accurate the bit clock is, the greater the correlation integral becomes.

From the hardware implementation point of view, the two integrators timed by BCKN is equivalent to the two integrators on the two correlators. Besides, the magnitude comparator following those two integrators performs the same function as the decision device of the demodulator. Therefore, these four structures may be omitted from the phase detector. Interestingly, the phase detection process can be said to be "decision-directed" or "data-aided". because bit decision is relied upon to determine which one of two triplets of integrals should be selected for comparison in each bit interval.

4.2.3 Performance Analysis

Like the carrier synchronizing DPLL, the bit synchronizing DPLL can readily be analyzed by using Markov theory. Here the analysis is actually simpler because only one-step phase adjustments are allowed in this loop.

Steady State Behaviour

The DPLL is modelled as a discrete Markov chain, whose states are defined as the absolute number of phase steps by which its output clock deviates from the receive bit clock. The chain's state transition behaviour corresponds to a unit-step random walk (Figure 4.11), characterized by <4.13, 4.15>. The solution to this problem is given by <4.16>.

The associated transition probabilities, a, b, and c, are related to the algorithm of the loop filter and the reliability of the phase detector. Let p denotes the probability of a correct lead/lag decision, q the probability of a wrong lead/lag decision, and r the probability of a null decision. Furthermore, without loss of generality, assume that, out of J lead/lag decisions collected by the loop filter for each phase update, u of them are correct, v of them are wrong, and w of them are inconclusive. Then

$$a = prob(p>q) = \sum_{x=1}^{\frac{J}{2}} \sum_{y=0}^{x-1} \binom{J}{x} \binom{J-x}{y} p^x q^y r^{J-x-y} + \sum_{x=\frac{J}{2}+1}^{J} \binom{J}{x} p^x (1-p)^{J-x} \qquad \text{<4.24>}$$

$$c = prob(p=q) = \sum_{x=0}^{\frac{J}{2}} \binom{J}{x} \binom{J-x}{x} p^x q^x r^{J-2x} \qquad \text{<4.25>}$$

and

$$b = prob(p<q) = 1 - a - c \qquad \text{<4.26>}$$

In turn, the phase detector output probabilities, p, q, and r, depend on channel noise statistics and on error characteristic of the decision-feedback lead/lag detecting algorithm. Normally, though,

as in the carrier synchronizing loop, the intrinsic factor far outweighs the extrinsic factor. So, for simplicity, channel noise effect is neglected in the calculation of p, q, and r. Suppose that the phase detector samples the k^{th} bit interval in which a mark bit is transmitted, and that the probabilities of 0 and 1 in neighbouring bit intervals are equal. Then

$$\begin{aligned} u = 0.25[&p(correct \mid 0 \text{ in } (k-1)^{th} \ \& \ 0 \text{ in } (k+1)^{th} \text{ interval}) + \\ &p(correct \mid 1 \text{ in } (k-1)^{th} \ \& \ 0 \text{ in } (k+1)^{th} \text{ interval}) + \\ &p(correct \mid 0 \text{ in } (k-1)^{th} \ \& \ 1 \text{ in } (k+1)^{th} \text{ interval}) + \\ &p(correct \mid 1 \text{ in } (k-1)^{th} \ \& \ 1 \text{ in } (k+1)^{th} \text{ interval})] \end{aligned} \qquad \text{<4.27>}$$

Based on the "maximum seeking" algorithm specified previously, it can be shown that

$$\begin{aligned} p &\approx \frac{1}{4}[1 + \frac{1}{2} + \frac{1}{2} + \frac{1}{6}] = \frac{13}{24} \\ q &\approx \frac{1}{4}[0 + 0 + \frac{1}{2} + \frac{1}{6}] = \frac{4}{24} \\ r &= 1 - p - q \approx \frac{7}{24} \end{aligned} \qquad \text{<4.28>}$$

Transient Behaviour

In the noiseless case, from <4.18>, the mean acquisition time of the bit synchronizing DPLL is

$$T_A = \frac{1}{L}\sum_{k=1}^{L} T_a(k) = (\frac{L-1}{2}) \cdot J \cdot T \qquad \text{<4.29>}$$

In the noisy case, the following difference equations, which can be solved numerically, apply:

$$
\begin{aligned}
T_a(k) &= JT + pT_a(k-1) + bT_a(k+1), \quad 1<k<L \\
T_a(1) &= 0 \\
T_a(L) &= JT + pT_a(L-1) + qT_a(L)
\end{aligned}
\qquad \text{<4.30>}
$$

Frequency Lock Range

The frequency range f_{range} of the bit synchronizing loop is given by

$$f_{range} = (\frac{1}{JL})f_s \qquad \text{<4.31>}$$

where f_s is the NCO's free running frequency. The "1" in the numerator is attributed to the fact that individual clock phase adjustment in the loop is limited to a single step.

5. DESIGN METHODOLOGY AND CHIP SPECIFICATIONS

While the previous chapters examines the theoretical aspects of the all-digital modem chip, this chapter is concerned with the engineering aspects. The design methodology, design philosophy, and prototyping technique are discussed. Chip functions, pinouts, internal circuit parameters, modem capabilities and training requirements are specified.

5.1 Design Methodology

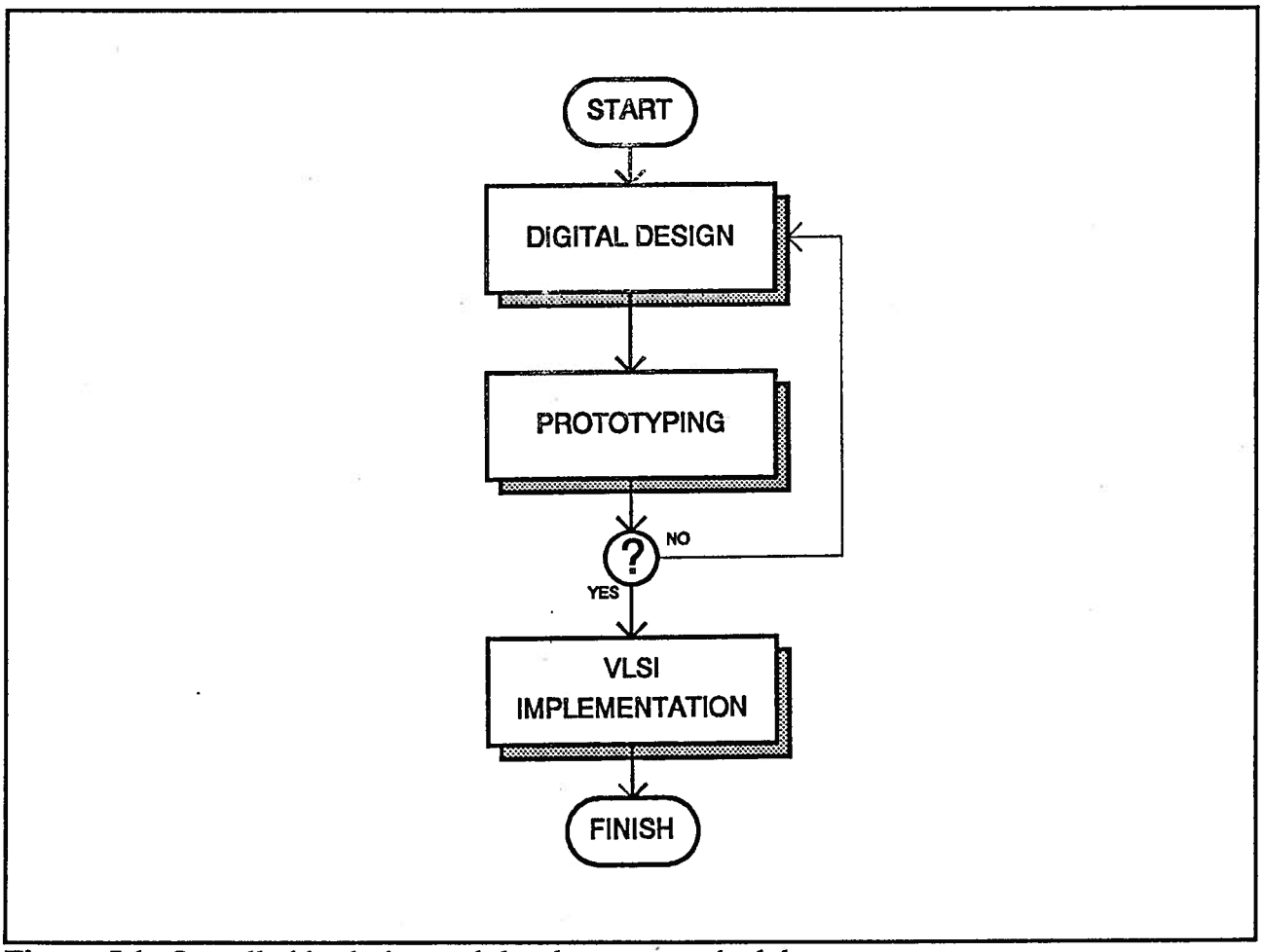


Figure 5.1: Overall chip design and development methodology.

Shown in Figure 5.1 is a flowchart representing the methodology used in the design and development of the MSK modem chip. After design specifications are firmed up, the first task is to design, synthesize, and draft the circuit schematics. Next, a prototype of the design is built and tested to determine whether it meets the functional requirements and how well the circuit performs. If the results are unsatisfactory, the original schematics are modified or, if necessary, re-designed. Then the prototype is changed accordingly for re-verification. This design-debug-modify cycle is repeated until a design that robustly meet all functional requirements is attained. The final design is then processed for VLSI implementation.

5.2 Digital Design

In developing the digital design of the MSK modem chip, a top-down approach [43, Ch. 5] is employed, with emphasis on functionality, modularity, and hierarchy. This comprises several steps. First, the top-level architecture of the chip is drawn, in the form of a block diagram indicating the functional blocks and their interconnections. Top-level blocks are defined by function rather than form; some blocks can be simple while some can be very complicated. Each top-level block is dedicated to a special purpose, and has a well-defined set of I/Os. For example, there are six top-level blocks in the MSK modem chip. These include the modulator which generates MSK waveforms; the demodulator which decodes MSK waveforms; the carrier detector which probes the receive input for carrier presence; the BIST controller which administers loopback self-test; the timing generator which produces on-chip timing clocks and strobes; and the chip controller which configures the chip.

The next step in the design process is to determine the internal hierarchy of each block. In the case of a simple block, no further partitioning is necessary. But, in the case of a complex block, subblock partitioning is usually needed. Besides, depending on the complexity of these subblocks, they themselves may be divided into smaller subblocks, called submacros. For example, the demodulator block of the MSK modem is such a block. It is made up of two carrier synchronizer subblocks and a bit timing recovery subblock. Within each one of these subblocks are a number of submacros.

The final step is to create the circuit schematics of each individual blocks, subblocks, and submacros. This, known as "gate-level design," involves the design and synthesis of

combinational and sequential logic circuits. Functions are transformed into structures out of logic gates and flip-flops.

At the end of the digital design, a set of circuit schematics is produced, describing the hardware implementation of the design, including both block-level organization and gate-level circuitry.

Also worth mentioning is the design philosophy adopted in the digital design of the MSK modem chip. It is one that stresses synchronizability and simplicity. Synchronizability requires the digital circuit to operate synchronously [44, p. 77]. A synchronous design has all its edge-sensitive elements responding to the same clock edge, and contains no level-sensitive storage elements. A synchronous circuit is, in general, more reliable and testable than an asynchronous one. Simplicity prescribes that the digital circuit is designed to be as simple as possible. A simple circuit tends to be more robust and easier to debug, contains less gates and thus occupies less silicon area.

5.3 Prototyping

The purpose of prototyping is to verify the feasibility and performance of the proposed circuit schematics. In particular, prototyping is necessary for the study, design, and development of the semi-coherent MSK demodulator. Included in the demodulator are two carrier synchronizers and a bit synchronizer, which, as explained in the previous chapter, are special purpose DPLLs. Because of signal feedback, the operation and performance of DPLLs are difficult to predict, analyze, and even simulate. There is always the question of whether a loop will ever acquire lock, and, if so, how long it will take. The phase detection methods employed in the synchronizers are new and thus unproven. It is uncertain whether they would work in practice, especially when subjected to channel noise interference. The best and easiest way to seek answers to these questions and to validate the feasibility and performance of the synchronizing circuits is via prototyping and testing in practical situation. One can experiment with the prototype to study its operation and gain insights into its optimization.

High speed CMOS LSI components [45] are used to prototype the modem chip design. These components are mounted on vector boards, and are interconnected using wire-wrap. Shown in Figure 5.2 is a photograph of the final version of the prototype modem. It is made up of five

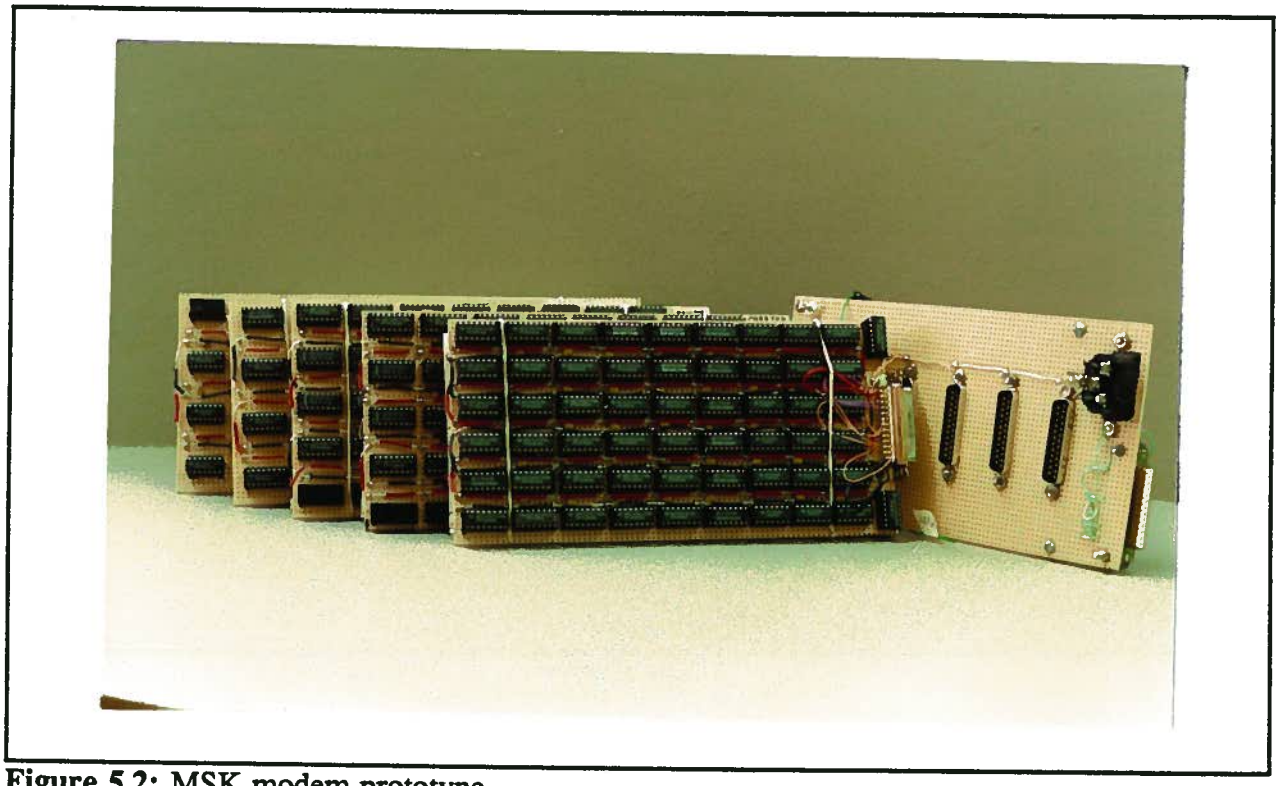


Figure 5.2: MSK modem prototype.

boards and one "backplane" board. Board 1 contains the modulation and timing circuits; board 2 contains the BIST and control circuits; carrier synchronization is provided on board 3 and 4; board 5 performs bit timing recovery and data extraction. Board-to-board interconnections are provided on the "backplane" board.

5.4 Modem Chip Design Specifications

In this section, the functions and I/Os of the modem chip are listed, related design equations and internal circuit parameters are discussed, including a few comments on the modem's training requirement and transmission capability.

5.4.1 Functions And Features

The primary functions of the MSK modem chip are:

1. MSK modulation.
2. Bit-by-bit semi-coherent demodulation of digitized MSK signals.

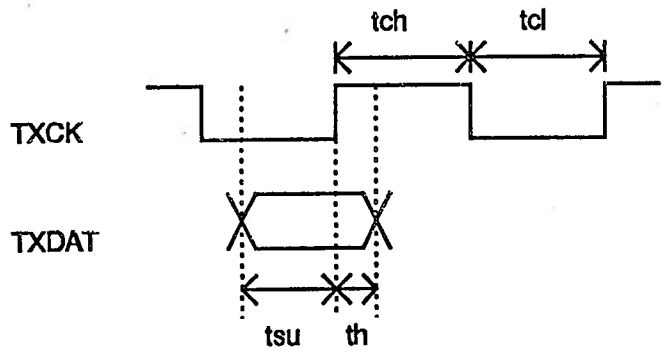
3. Detection of MSK carrier.

In addition, the following auxiliary features are provided:

1. Received MSK signal can be input to the chip in either 1-bit or 4-bit digitized form.
2. The chip can be programmed to establish an internal loopback, which is useful for out-of-service testing.
3. The chip has built-in-self-test (BIST) capability.

5.4.2 I/O Specifications

The MSK modem chip has a total of 36 pins: 11 inputs, 15 outputs, 5 power pins, and 5 ground pins. The voltage levels of the I/O pins are CMOS compatible. Listed below are the pin names, functions and usages:



	max	min	unit
tch	27	25	μs
tcl	27	25	μs
tsu	---	21	μs
th	---	1	μs

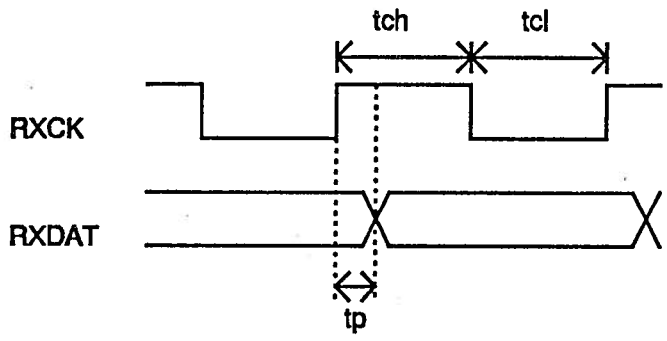
Figure 5.3: Transmit data transfer timing for 19.2 kbps transmission.

Pin #35: *TXDI* - transmit data input -- it is via this pin that NRZ data from the DTE is input into the modem chip for transmission (Figure 5.3).

Pin #34: *TXCK* - transmit clock output -- this pin outputs a 50/50 duty cycle clock to synchronize data transfer from the DTE to the modem (Figure 5.3).

Pin #10: *TXSO* - transmit signal output -- this pins outputs the MSK modulated square-wave signal.

Pin #32: *RXSI3* - receive signal input bit 3 -- this pin should be connected to either bit 3 (MSB) of the 4-bit ADC output or the output of the hardlimiter, whichever is used to digitize the received MSK signal.



	max	min	unit
tch	27	25	μs
tcl	27	25	μs
tp	11	0	μs

Figure 5.4: Receive data transfer timing for 19.2 kbps transmission.

Pin #31: *RXSI2* - receive signal input bit 2 -- this pin should be connected to bit 2 of the 4-bit ADC output, if present; otherwise, should be pulled up or down via a 10 kΩ resistor.

Pin #29: *RXSI1* - receive signal input bit 1 -- this pin should be connected to bit 1 of the 4-bit ADC output, if present; otherwise, should be pulled up or down via a 10 kΩ resistor.

Pin #28: *RXSI0* - receive signal input bit 0 -- this pin should be connected to bit 0 (LSB) of the

4-bit ADC output, if present; otherwise, should be pulled up or down via a 10 kΩ resistor.

Pin #13: *RXDO* - receive data output -- this pin outputs NRZ encoded data extracted from received MSK signal (Figure 5.4).

Pin #14: *RXCK* - receive clock output -- this pin outputs a 50/50 duty cycle clock in synchronism with the receive data (Figure 5.4).

Pin #11: *CD* - carrier detect -- this is an active-high output indicating the presence of MSK carrier waveform at the receive input.

Pin #16: *MODE1* - mode select bit 1 -- in conjunction with the MODE0 pin, this pin is used to configure the modem chip. There are four modes of operation: 1. Normal - 1-bit receive input (*MODE1*=0, *MODE0*=0); 2. Normal - 4-bit receive input (*MODE1*=0, *MODE0*=1); 3. Loopback - (*MODE1*=1, *MODE0*=0); 4. Self-test (*MODE1*=1, *MODE0*=0).

Pin #17: *MODE0* - mode select bit 0 -- see *MODE1*.

Pin #20: *RESET* - chip reset -- holding this pin high for ten or more system clock cycles will synchronously clear all on-chip flip-flops, counters, and registers.

Pin #09: *GOOD* - self-test outcome -- at the end of an automatic self-test, this pin will either remain high to indicate a success, or go from high to low to indicate a failure.

Pin #02: *SYSCK* - system clock input -- it is via this pin that the system clock (≤ 50 MHz) is supplied to the chip for internal timing and synchronization purposes.

Pin #27: *ADCCK* - ADC clock output -- this pin outputs a clock at the system clock frequency to trigger the external multi-bit ADC, if one is used to digitize the MSK signal received from the powerline.

Pin #03: *SIG0* - space carrier demodulated stream -- multiplied product of the input MSK signal and the local space carrier reference; for test-probing purpose only.

Pin #08: *SIG1* - mark carrier demodulated stream -- multiplied product of the input MSK signal and the local mark carrier reference; for test-probing purpose only.

Pin #05: *UD0* - "up/down" in space carrier recovery loop -- it indicates whether the space carrier loop is lagging or leading the receive input; for test-probing purpose only.

Pin #06: *UD1* - "up/down" in mark carrier recovery loop -- it indicates whether the mark carrier loop is lagging or leading the receive input; for test-probing purpose only.

Pin #23: *MAXM* - early receive bit clock -- this is an early version of the locally generated bit clock used for bit synchronization; for test-probing purpose only.

Pin #21: *MAXP* - late receive bit clock -- this is an early version of the locally generated bit clock used for bit synchronization; for test-probing purpose only.

Pin #26: *ADD* - "add" in bit clock recovery loop -- this is a signal in the bit clock recovery loop; when it is high, the bit clock is retarded by four system clock cycles; for test-probing purpose only.

Pin #24: *DEL* - "delete" in bit clock recovery loop -- this is a signal in the bit clock recovery loop; when it is high, the bit clock is advanced by four system clock cycles; for test-probing purpose only.

Pin #01, 07, 15, 19, & 25: V_{DD} - power -- these pins should be connected to +5 V supply.

Pin #04, 12, 18, 22, & 30: *GND* - ground -- these pins should be connected to digital ground close to the chip.

5.4.3 System Clock Requirement

All on-chip clocks and strobes are derived from the system clock. The system clock frequency f_s is required to be a common denominator of the frequencies of the internal clocks and strobes. Among these, the two carrier synchronizing frequencies are closest to each other, oscillating at $2f_0$ and $2f_1$, respectively. Therefore, as indicated in Figure 5.5, f_s should be set at

$$f_s = \frac{1}{2}\left(\frac{1}{2f_0} - \frac{1}{2f_1}\right) \qquad \text{<5.1>}$$

In terms of centre carrier frequency f_c and centre carrier frequency to bit rate ratio α,

$$f_s = \left(8\alpha - \frac{1}{2\alpha}\right) f_c \qquad \text{<5.2>}$$

In the MSK modem chip, α is fixed at 5.75. Thus

$$f_s = 264\left(\frac{4}{23}\right) f_c \qquad \text{<5.3>}$$

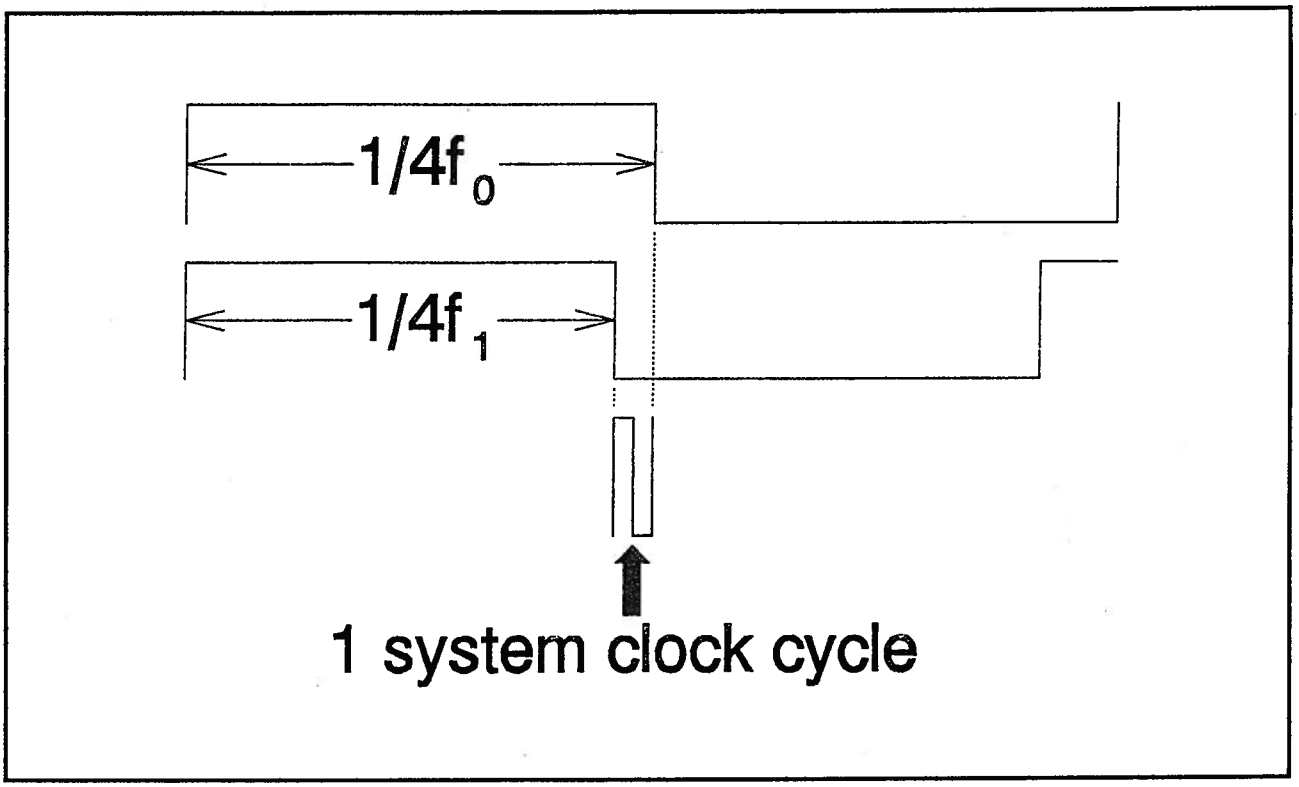


Figure 5.5: Calculation of system clock frequency.

Furthermore, it can be shown that

$$f_s = 46\, f_0 \qquad \text{<5.4>}$$

$$f_s = 48\, f_1 \qquad \text{<5.5>}$$

and

$$f_s = 264\, R \qquad \text{<5.6>}$$

Using these equations, one can determine the required system clock frequency based on the transmission specifications of the modem system.

5.4.4 Internal Circuitry

Modulator: Modulation is implemented with a one-bit NCO (Section 3.1.1). Based on equations <5.4-5>, the NCO divides the system clock by *46* when the datum is 0, by *48* when the

datum is 1.

Demodulator: Demodulation is coherent over a one-bit observation interval, and the method of binary partial decision is used (Section 3.2.1). The number of subbits per bit interval *(m)* equals to $R/f_s = 264$.

Carrier Synchronizer: It is a first-order DPLL of the lead/lag type (Section 4.1.3). Phase detection is by sampling the input carrier at the zero-crossings of the local carrier. Loop filtering is realized with majority logic. The number of lead/lag decisions per phase update *(U)* and the number of phase states $(N_{s,c})$ are *48* and *23*, respectively.

Bit Synchronizer: It is a two-input first-order lead-lag type of DPLL using an maximum seeking phase detection algorithm and a majority-vote loop filter (Section 4.2.1). The number of lead/lag decisions per phase update *(J)* and the number of phase state $(N_{s,b})$ are *12* and *66*, respectively.

Carrier Detector: Carrier presence is assumed if more than *8* positive-going zero-crossings occur at the input over *16* consecutive bit intervals (Section 3.3).

BIST Controller: In each run, six frames of test data is transmitted. Each frame contains 127 bits, generated from a 7-bit LSFR. The first five frames enables receiver synchronization, while error monitoring occurs in the last frame.

5.4.5 Training Requirement

To allow the receiving modem to acquire synchronization, a training sequence of alternating 0's and 1's should be appended to the beginning of the data sequence to be transmitted. Preamble length L_p is determined by the sum of the average lock acquisition times of the on-chip carrier and bit synchronizers. Specifically, from <4.20> and <4.29>,

$$L_p \approx \frac{N_{s,c}/2 - 1}{2}\frac{U}{\alpha} + \frac{N_{s,b}/2 - 1}{2}J \qquad \text{<5.7>}$$

Numerically, it can be shown that L_p is required to be approximately 236 bits long.

5.4.6 Modem Capability

The MSK modem chip is fabricated with 1.2 μm CMOS technology, which has a maximum speed limit of about 50 MHz. So, according to equation <5.6>, the maximum centre carrier frequency that the modem chip can support is 1.1 MHz, corresponding to a bit rate of 0.19 Mbps.

6. VLSI IMPLEMENTATION OF THE MODEM

In this chapter, some issues of VLSI implementation are discussed, and the schematics of the MSK modem chip are described in details.

6.1 VLSI Methodology

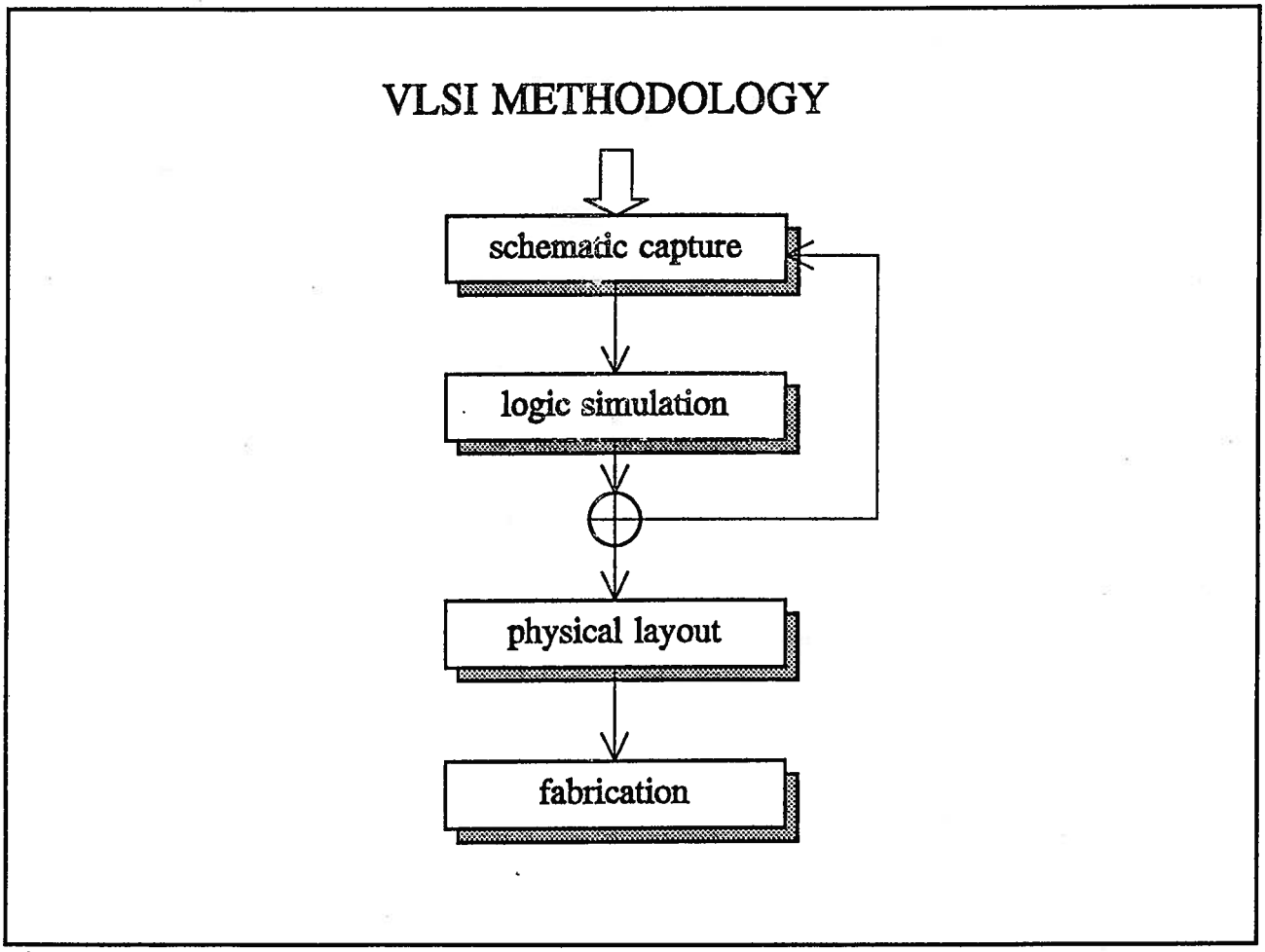


Figure 6.1: VLSI design methodology.

VLSI implementation of the modem chip is based on standard-cell design methodology [46, pp. 12-16]. A standard cell is a pre-designed full-custom circuit performing a basic logic function. The standard cell library that is available at the University of British Columbia contains most of the basic logic gates and a variety of flip-flops. Higher level structures such as counters and

comparators are not available from the library, and have to be assembled from basic cells by the designers.

Depicted in Figure 6.1 is the VLSI design process. It begins with the capturing of the design schematics using cells from the standard cell library. Next, the schematics are verified using computer simulation. A bottom-up approach is used, low level blocks simulated first and top-level circuitry last. In a simulation, a circuit is stimulated with a functional test pattern, and its resulting outputs are verified. Any circuit problems unveiled, such as fan-out and timing violations, are debugged and corrected. Simulations are repeated until the circuit is error-free. After the design schematic is thoroughly verified, a layout is created, which is a silicon-level physical representation of the schematics. The layout is produced by placing cells and routing signals as specified in the schematics.

Each of the above steps leading to fabrication is performed with CAD tools on a SUN workstation. CADENCE EDGE [47] is used for schematic capture and layout, while the SILOS simulator [48] is used for design verification. A clock speed of 50 MHz is assumed in the simulations. The cell library is provided by Canadian Microelectronics Corporation (CMC), a VLSI facility in Kingston, Ontario [49]. Design files containing layout information are submitted via electronic mail to CMC for fabrication.

The MSK modem chip is fabricated with 1.2 μm CMOS technology, which can support a maximum switching speed of approximately 50 MHz. CMOS has the advantages of high density, low power consumption [50, pp. 53-66]. The chip has a die size of 140 mil x 140 mil, and is packaged in a 68-pin Pin Grid Array.

6.2 VLSI Implementation Issues

In the design and implementation of a digital VLSI system, there are several technical issues worthy of special attention. These issues include: testability, clock distribution, and power/ground allocation. All are crucial to a successful VLSI design, and therefore must be addressed by the designers. How they are handled on the MSK modem chip is discussed below.

6.2.1 Testability

Testability refers to the ease of uncovering and identifying faults in the design. For reason

of economy, a VLSI device should be as testable as possible. This requirement is not easily met because one has no access to any of the internal nodes of the device. Only the I/O pins are available for testing purposes. Nonetheless, there are so-called "design for testability" techniques that can be applied to improve the testability of a design. Some of these techniques are used at various levels in the design of the modem chip.

At the logic level, the design has a high degree of synchronizability. All I/Os and internal signals can only change states at the edges of the system clock, thereby improving both the controllability and observability of the chip. Also, creation of test pattern for a synchronous design is more readily achieved than for an asynchronous design.

At the block level, a built-in-self-test (BIST) technique [51, pp. 146-190] is used to achieve testability. Testing of the modulator and demodulator blocks is automated with dedicated on-chip circuitry (BIST controller) which includes a test pattern generator and a signature analyzer. Run in real time, the test completes in a matter of seconds, and the result is indicated with a pass/fail signal. BIST helps to shorten diagnostic time and reduce testing costs. Also, the BIST test can be incorporated as part of the manufacturing test for the identification of defective parts in the chip factory.

At the chip-level, testability is improved by adding I/O pins to probe the internal nodes of the chip. Connected to the critical paths in the chip core, these pins allow the designers to monitor the internal operation of the device. Observability is thereby improved; identification and location of circuit faults become easier. Of the eight I/O pins dedicated to internal probing on the MSK modem chip, four access the two carrier synchronizers, and the other four access the bit synchronizer.

For higher controllability, a RESET pin is provided. By asserting this pin high for a few system clock cycles, one can synchronously clear all on-chip flip-flops, counters, and registers. This not only serves for system reset purpose but also is useful for test sequence initialization.

Finally, the internal loop-back feature of the modem chip contributes to system-level testability. This feature permits an end-user to establish an internal loopback cascading the modulator and demodulator. With this connection in place, the DTE can send data to itself, thus enabling the end-user to perform two-way testing of communication protocols in the absence of a channel and/or receiving node.

6.2.2 Clock Distribution

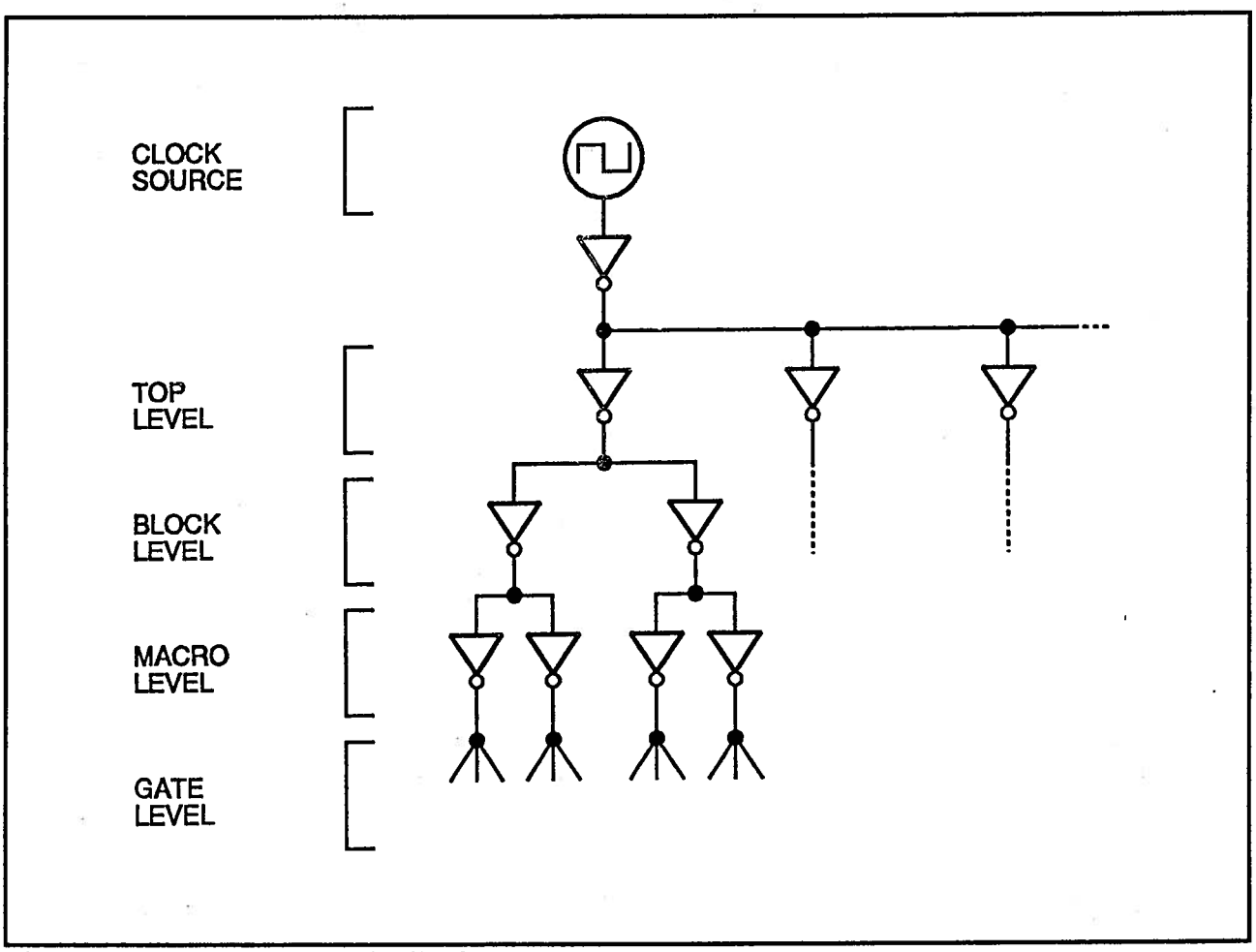


Figure 6.2: System clock distribution tree.

In a synchronous system, the system clock has to be distributed to flip-flops and other edge-sensitive elements. On its way, the clock's edges are delayed, and its rise and fall times slowed. Owing to variability in path length and path loading, the clocks arriving at different parts of the circuit are, in varying degree, skewed relative to one other. Such skewing might lead to timing problems that could be detrimental if left unattended, especially in systems where the clock width is in the same order of magnitude as one gate-level delay. A large clock skew may also undermine synchronizability. Therefore, the on-chip clock distribution network must be carefully designed to minimize clock skew.

The clock distribution network in the modem chip delivers the system clock to all parts of the chip in an organized, balanced, and hierarchical fashion. As shown in Figure 6.2, it has a

tree-like topology. In this clock tree, each branch corresponds to a distribution path. Inverters are used as "repeaters" in each branch to buffer and drive the clock signal. Basically, for delay balancing purpose, each top-level block in the modem chip is fed by one branch. Then, within each top-level block, the clock signal is split into several branches feeding the subblocks. The same is done in each subblock to send the clock to the submacros. Simulation results indicate that the maximum clock skew in the modem chip is approximately 5 ns.

6.2.3 Power/Ground Allocation

Power is provided to the chip via power and ground pins. The required number of power/ground pins depends on the level of ground noise the circuit can withstand. If insufficient power/ground pins are provided, the chip may malfunction from excessive ground noise. The amount of ground noise generated is determined by a number of factors, including gate count, switching speed, output load capacitance, and current requirement of the output pads. Taking these factors into consideration, it is possible to estimate the ground noise level. Then, based on this estimate, one can determine the required number of power/ground pins. Alternatively, CMC recommends that, as a rule of thumb, for 1.2 μm CMOS technology, one power/ground pair is needed for every 3000 gates in the chip core [52].

The MSK modem chip contains about 2200 gates, which suggests at least one power/ground pair. To allow for a large margin of error, five power/ground pins are actually used on the modem chip. These pins are distributed relatively evenly around chip periphery, with power and ground pins alternating.

6.3 Detailed Circuit Description

The circuit schematics of the MSK modem chip (a total of 20 sheets) are contained in the Appendix. This section describes the schematics from top to bottom, relating functions to structures.

6.3.1 Top-level

An overview of the I/Os, internal signal flow, and block-level organization of the MSK modem chip is shown on the top-level schematic (sheet 1).

Placed on the border are thirty-six pads, each of which corresponds to one pin on the chip. There are four types of pads: input, output, power, and ground. Input or output pads, which are unidirectional, buffer and protect signals entering or leaving the core.

Resided in the core are six interconnected functional blocks. A digital circuit in its own right, each block has a well defined set of I/Os and performs a specific function in synchrony with other blocks.

Pads

The MSK modem chip has a total of 36 pads: 11 inputs, 15 outputs, and 5 pairs of power/ground pads. A descriptive list of the pinouts is given in Section 4.2. Of the 26 I/O pins, only 18 are for operational use; the rest are used as test points probing internal nodes for performance monitoring and debugging purposes.

Core

Signal processing activities of the modem chip take place in the MOD, DMDV, CDT, and TEST blocks, under control and support of the CNTL and TMG blocks.

MOD generates the carrier wave and frequency modulates it with binary data from the host, while DMDV acts as a bit-by-bit semi-coherent MSK demodulator retrieving information from signals received from the channel. CDT monitors the receive input for presence of carrier signals. TEST specializes in built-in self-test of the modulator and demodulator. Timing clocks and strobes required for proper coordination and synchronization of these four blocks are generated by TMG. CNTL is responsible for setting up the internal configuration of the modem.

Tabulated in Table 6.1 are the gate/transistor count figures of these six top-level blocks.

6.3.2 Block Level

Table 6.1 contains an alphabetical listing of all the macro blocks used in this design. Among them are the six top-level functional blocks, made up of random logic, flip-flips, and other sub-blocks. The operation and digital circuitry in each of these top-level blocks are explained below.

CNTL

Block Name	Description
nMX2	n-bit 2 to 1 multiplexer
ADDn	n-bit full adder
CnBE	n-bit synchronous counter
CnBA	n-bit asynchronous counter
CDT	carrier detector
CMPn	n-bit comparator
CNTL	configuration controller
CRL0	carrier synchronizer - space frequency
CRL1	carrier synchronizer - mark frequency
DFFn	n-bit D-flip-flop
DIV12	divide-by-12 circuit
DIV48	divide-by-48 circuit
DMDV	demodulator
DVCO0	numerically controlled oscillator - space
DVCO1	numerically controlled oscillator - mark
LPP	majority loop filter
MOD	modulator
NCOV	numerically controlled oscillator - bit
NORM	magnitude calculator
PHD	carrier phase detector
PLLP	3-level loop filter
SPDV	bit clock phase detector
STORE	8-bit resettable register
STRV	symbol timing recovery unit
TEST	self-tester
TMG	timing generator

Table 6.1: Macro blocks in the modem chip.

MODE #	MODE1	MODE0	Description	LOOP	QUAD	TEST
A	0	0	normal - binary	0	0	0
B	0	1	normal - 4-bit	0	1	0
C	1	0	loopback	1	0	0
D	1	1	self-test	1	0	1

Table 6.2: Mode select truth table.

CNTL controls the modem configuration which depends on user selection of one of the four modes via the MODE1 and MODE0 pins. In both mode-A (MODE1 = MODE0 =low) and mode-B (MODE1 = low, MODE = high), the modem is set for half-duplex data transmission and reception. The difference between these two modes lies in their digitization requirement of

receive signal. For mode-A, the receive signal needs only to be 2-level quantized (e.g. using a hardlimiter). For mode-B, it has to be 16-level digitized (e.g. using a 4-bit ADC) because, in this mode, carrier synchronization relies on a multi-bit sampling scheme. In mode-C (MODE1 = high, MODE0 = low), the output of the modulator is directly fed to the input of the demodulator; this loopback connection facilitates off-line modem testing. Mode-D (MODE1 = MODE0 = 1) is used for built-in self-test: in this mode, loopback is established, and upon reset, the device automatically conducts a test to check the integrity of the modulation/demodulation circuitry.

Three active-high internal control signals from CNTL are used to configure the modem according to its mode of operation. These signals, called TEST, LOOP, and QUAD, are decoded from MODE1 and MODE0. The decoding logic is shown on sheet 2, and the corresponding truth table given in Table 6.2. TEST activates the TEST block and instructs the MOD block to accept test data from the TEST block. LOOP establishes loopback. When QUAD is asserted, the two carrier synchronizers within the DMDV block enter multi-bit mode of operation.

TMG

TMG, the "timing" block, supports, coordinates, and synchronizes the signal processing actions in other blocks. As shown in its block diagram in Figure 6.3, TMG generates several timing waveforms, their relationships illustrated in Figure 6.4. Both C44 and ADCCK are buffered versions of the externally supplied system clock (SYSCK). C44 is used to clock the demodulator, while ADCCK is sent off-chip to sample the receive signal. Other timing waveforms are derived from a branched timing chain driven by SYSCK. First, a divide-by-2 circuit is used to generate C22, that clocks the modulator. Then dividing C22 by 66 and subsequently by 2 yields C19. Pulse BP is obtained by gating the output of the divide-by-66 circuit with C19. Both C19 and BP are used for bit timing control in the modulator. Next, dividing C19 by 16 gives CCD, that defines the carrier detection interval. A divide-by-4 circuit is utilized to derive C9 from SYSCK. C9 provides the time base for symbol timing recovery. Shown on sheet 3 is the detailed schematic of TMG. It contains four frequency dividers, each made up of a counter or flip-flop and a few logic gates. Finally, TMG is also responsible for buffering and distributing the chip-reset input, RESET.

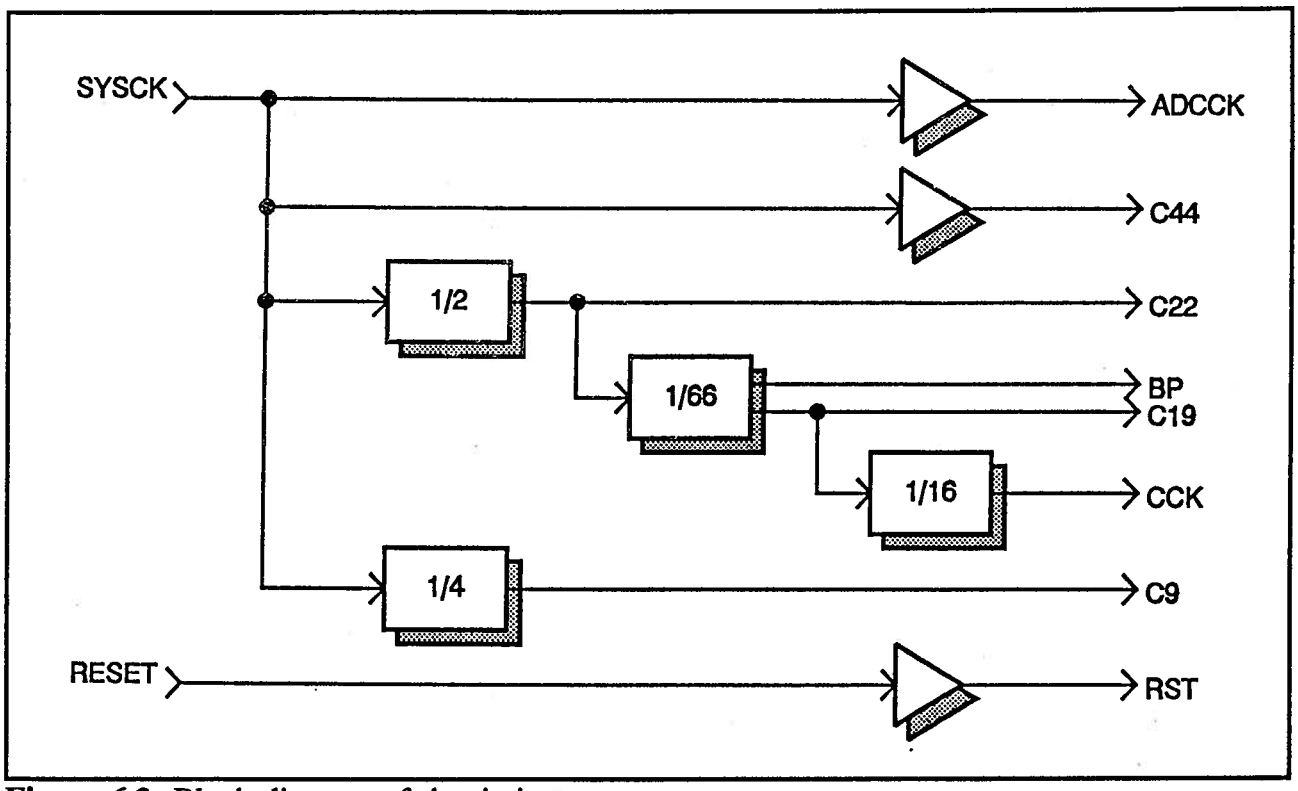


Figure 6.3: Block diagram of the timing generator.

MOD

MOD, the "modulator" block, encodes binary information onto a square wave carrier according to the MSK modulation scheme, with phase continuity maintained at bit boundaries. As shown on the schematic of MOD (sheet 4), the carrier is derived from C22 using a counter, decoder, and flip-flop. C22 clocks the counter. Its count is decoded to determine when to clear itself and to toggle the flip-flop. In this way, the flip-flop outputs a square wave, the frequency of which depends on the decoding threshold. MSK modulation is accomplished by adjusting the threshold according to the transmit binary data latched in. A space bit will set the threshold at 11; a mark bit will change the threshold to 10. Synchronization between the modulator and incoming bit stream is maintained by periodically resetting the counter with BP. This mechanism helps to ensure phase continuity at bit boundaries.

DMDV

DMDV, the "demodulator" block, is a one-bit digital implementation of the semi-coherent

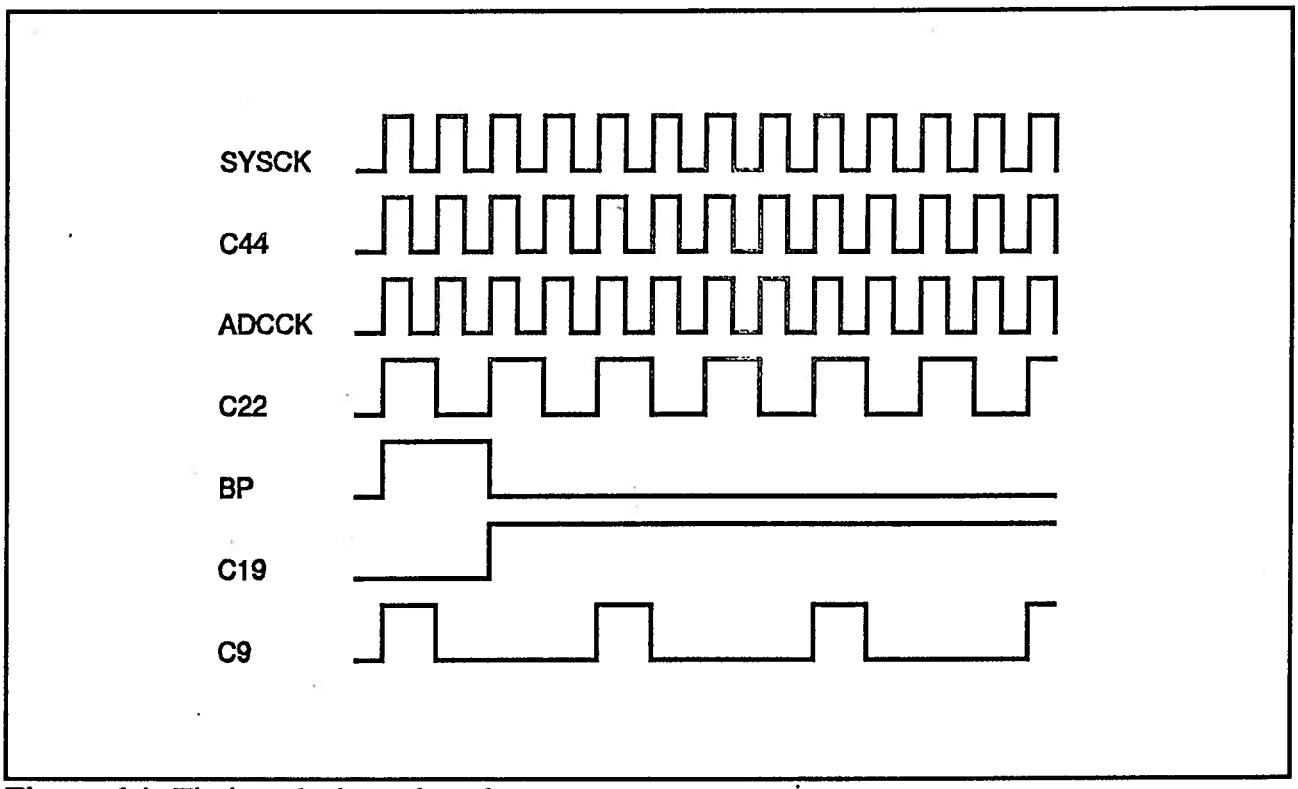


Figure 6.4: Timing clocks and strobes.

MSK receiver. First, the received signal is multiplied with each of the two carrier waveforms, generated by two carrier synchronizers. The products are then processed with two integrate-and-dump filters based on bit timing recovered by the bit synchronizer. Finally, a decision device determines the digital output on a bit-by-bit basis.

Shown on sheet 5 is the block-level schematic of DMDV. CRL0 and CRL1 each contain a digital phase-locked loop designed to recover from the receive signal the two suppressed carriers, respectively. Normally, CRL0 and CRL1 requires the receive signal to be 4-bit digitized in two's complement representation. However, if the receive signal is hardlimited (i.e. in mode-A), then only one bit, indicating the polarity, is available. In this case, this 1-bit signal is input into CRL0 and CRL1 via the most significant bit of the receive input, and the other three bits are controlled as follows to render the corresponding two's complement representation:

1. bit 0: set to 0
2. bit 1: set to 1
3. bit 2: set to be the same as bit 3

This conversion is the function of the logic circuit preceding CRL0 and CRL1. When QUAD is high (4-bit sampling mode), all four bits of the received signals are unchanged; however when QUAD is low (1-bit sampling), only bit 3 is taken as is, and the other three bits are changed in the manner just described.

The carrier waveforms recovered by CRL0 and CRL1 are then used to correlate the received signal through two XOR gates (i.e. modulo-2 multiplication). Then the products are fed into STRV, a special data-aided digital phase-locked loop. STRV concurrently performs three functions: 1) digital integrate and dump, 2) bit-by-bit data extraction, and 3) symbol timing recovery. The internal operations of sub-blocks CRL0, CRL1, and STRV are described below in detail.

CRL0

CRL0 functions to regenerate and track the phase of the suppressed space carrier from the received signal. Because MSK waveforms contain no discrete components at carrier frequencies, CRL0 first recovers the 2nd harmonic with a first order DPLL, and then divides it by two to obtain the original carrier waveform.

As shown on sheet 6, CRL0 itself is made up of six building blocks. Phase detection is done by PHD in conjunction with the five flip-flops preceding it. ADD8, STORE, and PLLP collectively play the role of a loop filter. DVCO0 is equivalent to a numerically controlled oscillator, and included in it is a frequency divider required for regenerating the carrier from its 2nd harmonic. Lastly, DIV48 produces timing strobes that synchronize loop operation.

For phase detection, the 4-bit received signal, in two's complement representation, is first sampled on the rising edge of the 2nd harmonic by four flip-flops, and its sign bit is sampled again on the falling edge by another flip-flop. Then the signs of the two samples are compared to determine whether the 2nd harmonic is leading or lagging the carrier embedded in the received signal. If the two samples have the same sign, the 2nd harmonic is lagging; otherwise, the 2nd harmonic is leading. Inside PHD (sheet 7) is a group of logic gates that two's complement the sampled word, and a 4-bit multiplexer that selects either the first sample or its two's complement, depending on the sign of the sample and the lead/lag decision reached. For example, if the sample is positive (negative) and the 2nd harmonic is lagging (leading), then the two's

complement will be selected, and vice versa. As a result, the output of PHD is a 4-bit number, in two's complement representation, with its sign indicating the lead/lag condition and its absolute value corresponding to the magnitude of the phase error.

PHD outputs one phase error datum per 2nd harmonic cycle. The data are accumulated by STORE and ADD8. STORE (sheet 8) is an 8-bit resettable register, and ADD8 (sheet 9) is an 8-bit full adder built from two cascadable 4-bit full adders. Every 48 cycles, the sum is decoded by PLLP, and STORE is subsequently cleared. PLLP (sheet 10) decides what kind of corrective action is needed in DVCO0 according to the following rules:

1. If abs(sum)<2, no correction is needed.
2. If 2<abs(sum)<32, and if sum>(or <)0, then advance (or retard) carrier phase by one C44 step.
3. If abs(sum)>32, and if sum>(or <)0, then advance (or retard) carrier phase by two C44 steps.

The decision is then conveyed to DVCO0 via two control signals: IDLE and UPDN.

DVCO0 (sheet 11), the numerically controlled oscillator, divides down C44 to generate the 2nd harmonic of the space carrier (CKS). DVCO0 accomplishes this with a correctable counter, a count decoder, and a flip-flop. The counter is clocked by C44. Every time its count reaches 10, it is reset, and the flip-flop toggles once. This creates the 2nd harmonic which is then divided by 2 to generate the space carrier. Phase adjustment is actuated via IDLE and UPDN, controlled by PLLP. With IDLE held low and UPDN held high for one C44 cycle, the count will increase by two instead of one, thus advancing the phase of CKS by one C44 step. On the other hand, when both IDLE and UPDN are held low for one C44 cycle, the count will remain constant, thus retarding CKS by one C44 step.

To synchronize the operation of the DPLL, two timing strobes, R and L, are needed. Both signals goes active once every 48 CKS cycles. R resets STORE, while L enables PLLP to issue a phase correction command. To generate R, DIV48 (sheet 12) divides CKS with a 6-bit counter and decoding logic, and obtains L simply by gating R retimed once by C44 with R itself.

CRL1

CRL1 (sheet 13) functions to recover the mark carrier. Its structure and operation are

identical to those of CRL0, except that DVCO1 is used in place of DVCO0. In DVCO1 (sheet 14), the output flip-flop toggles whenever the count reaches 10, not 11, to produce the 2nd harmonic of the mark frequency.

STRV

The STRV block is responsible for 1) integration of demodulated streams, 2) data extraction, and 3) symbol timing recovery. Like CRL0 and CRL1, STRV is a first-order digital phase-locked loop. As shown on sheet 15, it contains 4 sub-blocks: SPDV, LPP, NCOV, and DIV12. SPDV not only detects phase error, but also performs data integration and extraction. LPP serves as a loop filter controlling NCOV, the numerically controlled oscillator. Loop timing is provided by DIV12..

The phase detection technique used in STRV is different from that used in CRL0 or CRL1. In CRL0 or CRL1, it is done by comparing the polarities of the received signals sampled on the rising and falling edges of the local signal. The same can not be done for symbol timing recovery because, 1) timing information is carried in not one, but two demodulated streams, and 2) no well-defined state transition edges are available due to non-zero phase difference between the received signal and local carrier. Instead a data-aided approach based on early-late timing is adopted in SPDV (sheet 16), which makes use of three pairs of digital integrate-and-dump's. Both data extraction and phase detection are using the same circuit.

The implementation of this scheme requires not only the regular bit clock, but also an early and a late version of it. These clocks, supplied to SPDV by NCOV, control the interval of integration on three pairs of counters, acting as digital integrate-and-dump's. The middle pair integrates the two demodulated streams over the bit interval. The top pair does the same over an earlier interval using the early clock, and the bottom pair over a later interval using the late clock. The final count value on each counter is a measure of the correlation between the receive signal and one of the local carriers over the selected integration interval. Each counter is followed by a block called NORM (sheet 17) which decodes the count to yield a measure of the absolute correlation between the receive signal and the local carrier over the integration interval.

First, data extraction is done simply by comparing the correlation values obtained from the middle pair of counters using a 7-bit magnitude comparator (CMP7) made from two 4-bit

comparators (CMP4). If the lower counter, which monitors the mark carrier demodulated stream, presents a higher correlation, a "1" is detected; otherwise "0" is assumed. Second, to determine the phase error, the greater of the two correlation values from the middle pair is compared to corresponding results obtained by the other two pairs of counters over an early and late interval. For example, if the lower count exceeds the upper count over the nominal interval, then the three lower counts will be selected for phase error consideration. In essence, the selection is based on the data detected. Hence this scheme can be referred to be data-aided. The selected set is latched and then compared to determine the phase error according to the following rules:

1. If |early correlation| > |nominal correlation| > |late correlation| => lagging.
2. If |late correlation| > |nominal correlation| > |early correlation| => leading.
3. Otherwise => inconclusive.

These rules are based on the premise that the more accurate the bit clock is, the higher the correlation becomes. They are realized with hardwired logic including two 7-bit comparators (CMP7) and two AND gates.

Using the scheme just mentioned, SPDV extracts a datum and makes a lead/lag decision for each bit interval. The data, along with the bit clock, are exported to the host. Phase decisions are conveyed to the loop filter (LPPL) via two active-high signals: LEAD and LAG. LPPL (sheet 18), a binary sequential filter, functions to determine the ensemble average of the phase error over 12 bit intervals. Its implementation includes two 4-bit counters, one monitoring the LEAD input, and the other the LAG input. The counters are reset by R once every 12 bit intervals. At the end of each reset interval, the counts stored in the two counters are compared using a 4-bit comparator (CMP4). The majority rule applies here. If the LEAD count exceeds the LAG count, ADD will be asserted to retard the bit clock; or if vice versa, DEL will be asserted to advance the bit clock.

NVCO (sheet 19), the numerically controlled oscillator, is driven by C9. It is structurally similar to DVCO0 or DVCO1 used for carrier synchronization. First, the early clock is generated from a divide-by-66 circuit which features a 7-bit correctable counter. Second, a 15-bit shift register is employed to delay the early clock to produce the nominal clock. Third, the nominal clock is, in turn, delayed on another 15-bit register to render the late clock. The clock phase is adjusted via ADD and DEL. When DEL is asserted, the counter will skip a cycle, thus shifting

the clocks backward by one C9. On the contrary, asserting ADD will doubly increment the counter and as a result shift the clocks forward by one C9.

The operation of this DPLL is synchronized with two timing strobes: R and L. Strobe R resets the sequential filter (LPPL) once every 12 C44 clock cycles. Strobe L enables the ADD/DEL output of LPPL periodically. Both R and L originates from DIV12 (sheet 20). R is generated by dividing down the bit clock by 12 with a 4-bit counter, and L is obtained by gating R delayed by one C44 with R itself.

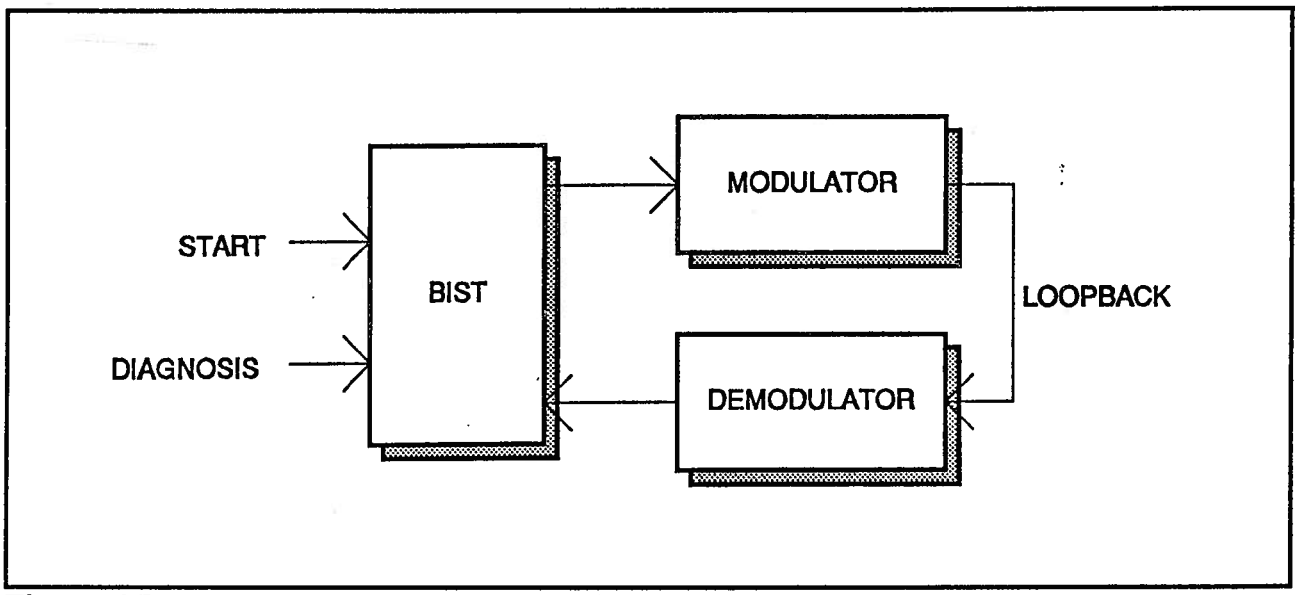


Figure 6.5: Loopback configuration for self-test.

CDT

Shown on sheet 21 is the schematic of the CDT block which performs carrier detection. It contains an 8-bit up-counter that is reset by CCD. The clock input of this counter is connected to the receive line (RXD). In the presence of a carrier signal, RXD will toggle and increment the count value. At the end of each reset interval, the counter is decoded to determine if there is activity on RXD. The result is updated on a flip-flop. Under normal on-line condition, the count should reach some value in the neighbourhood of 90. But taking into consideration of channel impairments on the receive line, an arbitrarily low decision threshold of 8 is chosen. That is, if the count exceeds 8, then carrier presence is assumed.

TEST

TEST, the "test" block, performs automatic testing and functional verification of the on-chip modulator and demodulator. As shown in Figure 6.5, when the modem is in self-test mode, test data is looped from TEST to MOD, to DMDV, and then back to TEST. The schematic of TEST is shown on sheet 22. A 7-bit pseudo random shift register is used to generate the test pattern, each frame of which is 127 bits long. Data received from the demodulator is compared with data submitted to the modulator on a bit-by-bit basis using a XOR gate. Any occurrence of a compare error will be flagged on the error register. Timing control is provided by a counter that keeps tracks of the number of transmitted data frames. It ensures that the compare circuit is not activated until five frames of test data have been transmitted, because the modem takes a substantial amount of time to acquire carrier and symbol synchronization. After one frame of comparison, the test is terminated, and the outcome is indicated on the GOOD line.

7. THE MAKING OF A POWERLINE MODEM

To illustrate the application of the MSK modem chip designed in this thesis, a high speed modem unit based on the modem chip is built. The unit facilitates half-duplex data transmission between two data terminal equipment (DTE) via intrabuilding AC powerlines. After a brief review of the transmission and noise characteristics of powerlines, this chapter presents the board-level design of this compact almost-all-digital MSK powerline modem, including descriptions of the DTE and powerline interface circuits.

7.1 Powerlines As Communication Channels

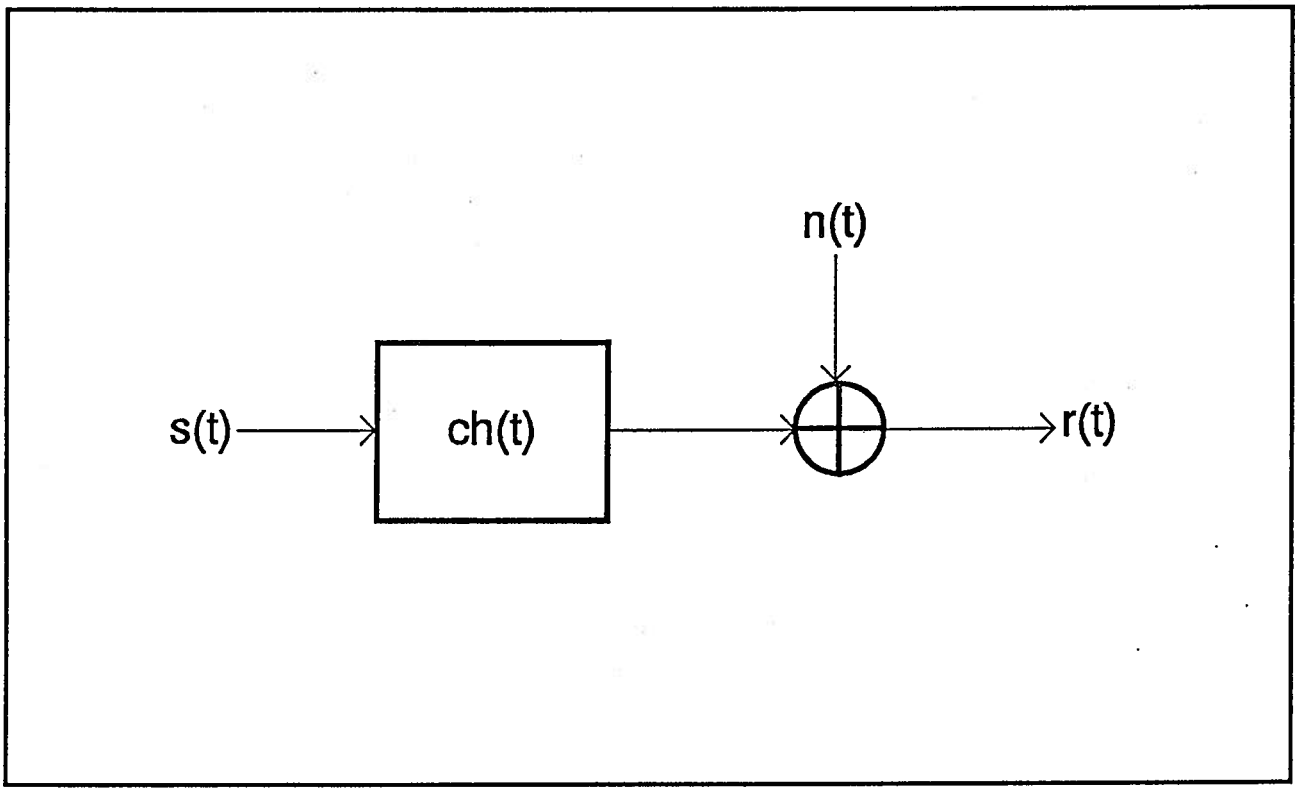


Figure 7.1: Model of intrabuilding powerline channels.

The channel model of intrabuilding powerlines appears in Figure 7.1. A signal *s(t)* injected into the powerline by the transmitter will be received as *r(t)* at the receiver. A transformed and corrupted version of *s(t)*, *r(t)* is given by

$$r(t) = s(t) \otimes ch(t) + n(t) \qquad \text{<7.1>}$$

where *ch(t)* is the impulse response of the physical channel, and *n(t)* stands for noise interference.

Channel function *ch(t)* accounts for the impedance and signal attenuation effects of the channel. It is time-varying, and depends not only on the signal frequency but also on the position of the transmitter and receiver, and the load profile of the powerline circuit. Topology and physical characteristics of intrabuilding power circuits are discussed in [8, 12]. Nicholson and Malack [53], and Vines, etc. [54] measured the input impedance of powerlines in commercial buildings. This is the driving-point impedance into which the transmitter sends a signal and from which the receiver extracts a signal. It is attributed to distribution transformer secondary, copper wiring, and electrical loads present in a powerline network. Chan [55] investigated the attenuation of signals propagating across intrabuilding powerline networks. Attenuation, in this case, is defined as the ratio between the received signal amplitude and transmitted signal amplitude. The severity of attenuation depends, to some degree, on the phase relationship between the transmit and receive points of access to the powerline circuit. In addition, attenuation level may also fluctuate rapidly and periodically with time, giving rise to signal fading. Signal fades of 120 kHz are observed on powerline channels. This effect is in part caused by time variation in driving-point impedance at the transmitter and receiver as a result of load switching (e.g. rectifier circuits in power supplies). Due to the complexity and unpredictability of powerline networks, explicit representation of *ch(t)* is not possible. Generally it has the following characteristics:

1. It presents an impedance of about 10 Ω to the transmitter and receiver in the 10 - 200 kHz range.
2. It behaves like a low-pass filter; any frequencies above 150 kHz are severely attenuated by up to as much as 50 dB.
3. Signal attenuation on opposite-phase and cross-phase paths is greater than on in-phase paths (Figure 7.2).

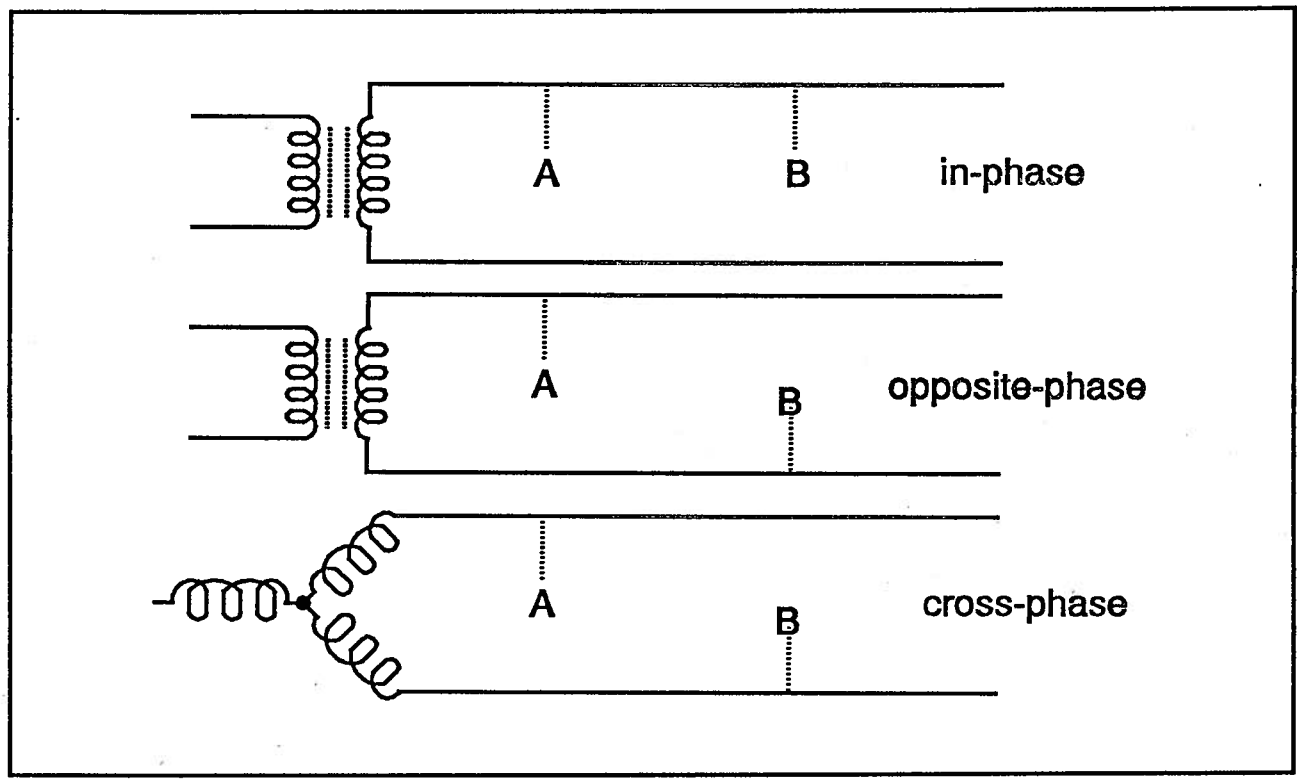


Figure 7.2: Intrabuilding powerline transmission paths.

Noise function *n(t)* accounts for noises inherent in a powerline channel. Like *ch(t)*, *n(t)* is very much time varying. Performing spectral density measurements, Smith [56] found that the background noise intensity of powerlines decreases at approximately 29 dB/decade over the 10 - 100 kHz range. Vines, etc. [57] characterized different types of noise sources on residential powerlines over the 5 - 100 MHz range. Powerline noise can generally be regarded as a combination of background noise *b(t)* and impulse noise *i(t)*. Trussel and Wang [58] verified that *b(t)* is typically Gaussian. The time domain characteristics, including amplitude, width, and interarrival time of *i(t)* have recently been measured by Chan [59]. Depending on which noise sources and their proximity to the receiver, impulse strength can be as much as 10 - 40 dB above background noise level. Impulse frequency is dominantly 120 Hz. Impulse width can vary up to a few percent of the period of a 120 Hz signal. It is the presence of *i(t)* that limits the on-line bit error performance of powerline modems, especially in high speed transmission where data bit duration is comparable to or less than the impulse width.

7.2 Modem System Architecture

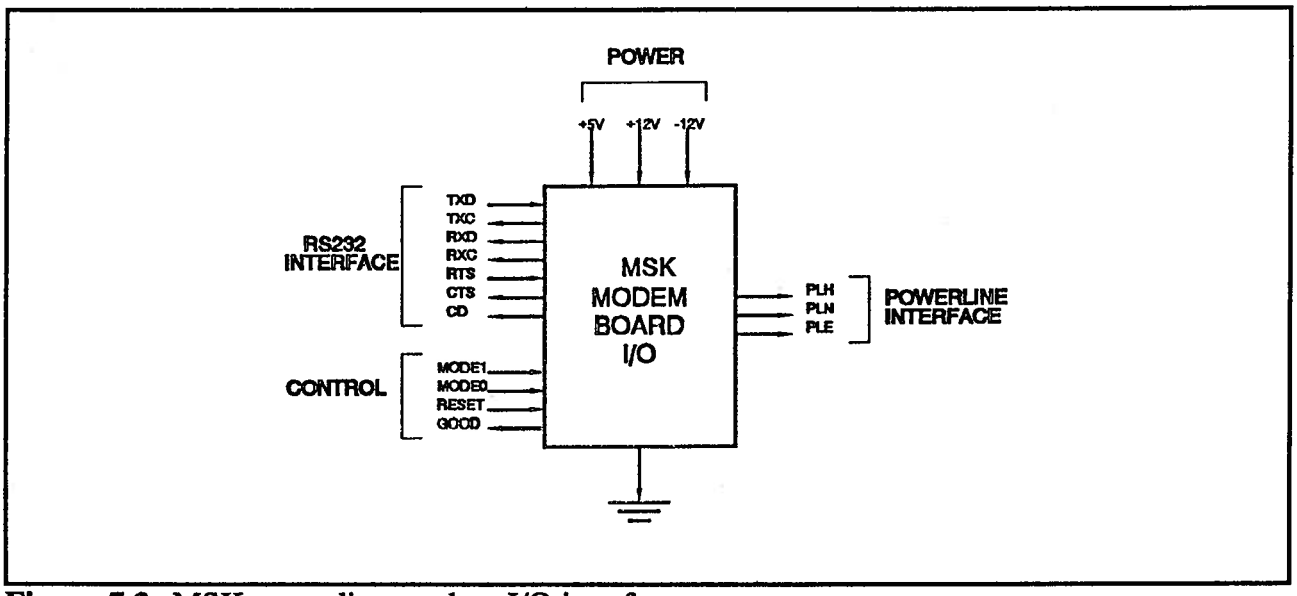


Figure 7.3: MSK powerline modem I/O interface.

Pin Name	Type	Speed	Description
TXD	I	9.6 kHz	transmit data from DTE
TXC	O	19.2 kHz	transmit clock to DTE
RXD	O	9.6 kHz	receive data to DTE
RXC	O	19.2 kHz	receive clock to DTE
RTS	I	async	Request_To_Send
CTS	O	async	Clear_To_Send
DCD	O	async	Data_Carrier_Detect
MODE1	I	DC	mode control -- bit 1
MODE0	I	DC	mode control -- bit 0
RESET	I	DC	synchronous reset
GOOD	O	DC	on-board ASIC diagnosis
PLH	I/O	analog	connect to hot wire
PLN	I/O	analog	connect to neutral wire
PLE	I/O	analog	connect to earth
+5V	power	DC	+5V DC supply
+12V	power	DC	+12V DC supply
-12V	power	DC	-12V DC supply
GND	ground	DC	ground reference

Table 7.1: I/Os of the MSK powerline modem board

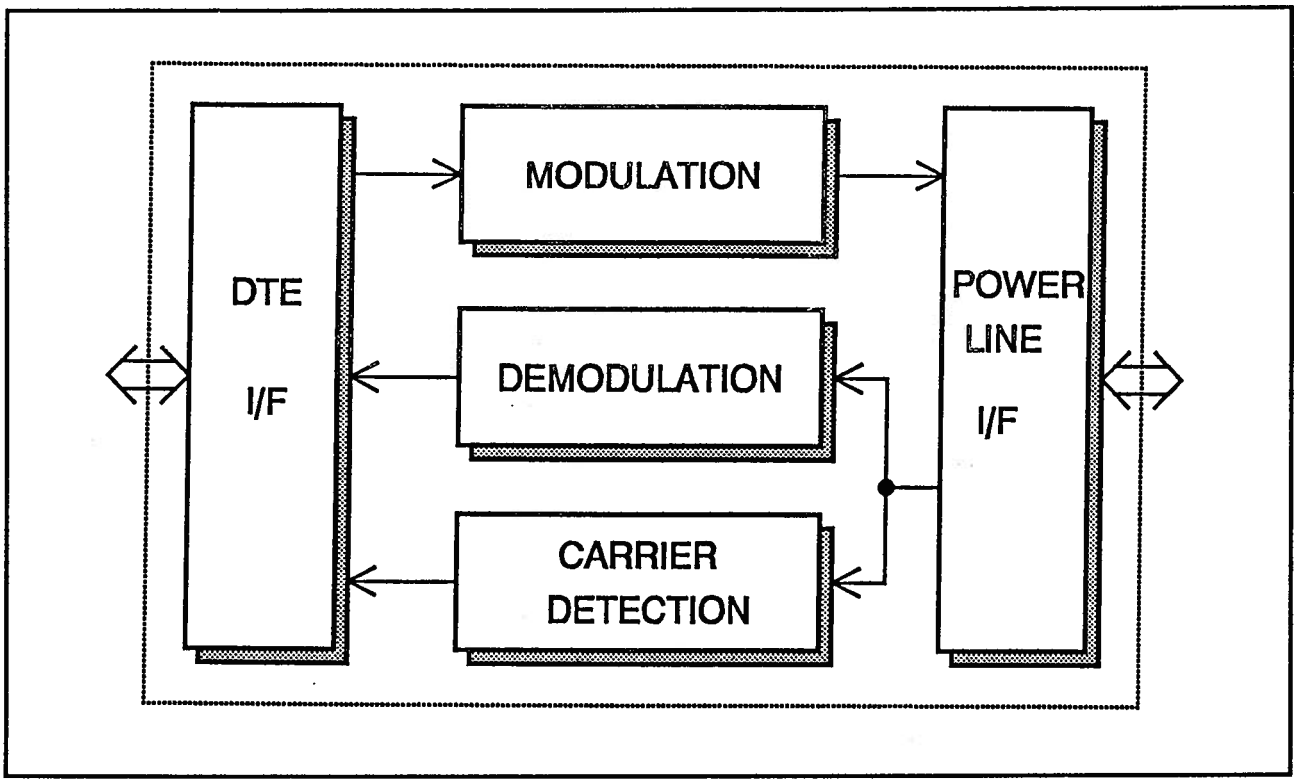


Figure 7.4: Functional block diagram of the powerline modem.

The powerline modem board supports two-way data transfer at 19.2 kbps in half-duplex mode. Its I/O is shown in Figure 7.3 and specified in Table 7.1. Communication between the modem and DTE is facilitated by a synchronous serial interface in compliance with RS232 specifications [60, pp. 421-429]. At this interface, transmit and receive data are NRZ formatted, and are timed by bit clocks originated from the modem. Connection of the modem to the powerline is achieved with a line coupling network. In transmit mode, an 8 V_{pp} sinusoidal MSK carrier wave is emitted from the modem board into the powerline. The output power of the transmitter is rated at 3 W. Depending on input data, carrier frequency is switched between 105.6 kHz (space) and 115.2 kHz (mark). This corresponds to a centre carrier frequency to bit rate ratio of 5.75. The spectrum of the transmitted signal centres at 110.4 kHz and has a bandwidth of about 23 kHz, which is within the passband of typical intrabuilding powerlines. In receive mode, the modem extracts MSK signal from the powerline. For proper reception, the signal arriving at the receive input is required to have an amplitude of at least 0.1 V_{pp}, which corresponds to the quantization threshold of the modem's input stage.

Figure 7.4 shows the functional block diagram of the modem. In addition to modulation, demodulation, and carrier detection, two auxiliary functions are needed: DTE interfacing and powerline interfacing. First, based on the synchronous RS232 protocol [60, pp. 421-429], the DTE interface is responsible for the followings:

1. Serial transfer of digital data and bit clocks between the modem and DTE.
2. Conditioning of interface signals to meet RS232 electrical specifications.
3. Handshaking with the DTE to establish the transmit/receive status of the modem.

Second, the powerline interface serves the following purposes:

1. Filtering and power amplification of transmit waveforms.
2. Filtering and digitization of receive waveforms.
3. Two-way AC coupling of modulated signal between modem and powerline.
4. Isolation of modem from 120 V AC voltage.

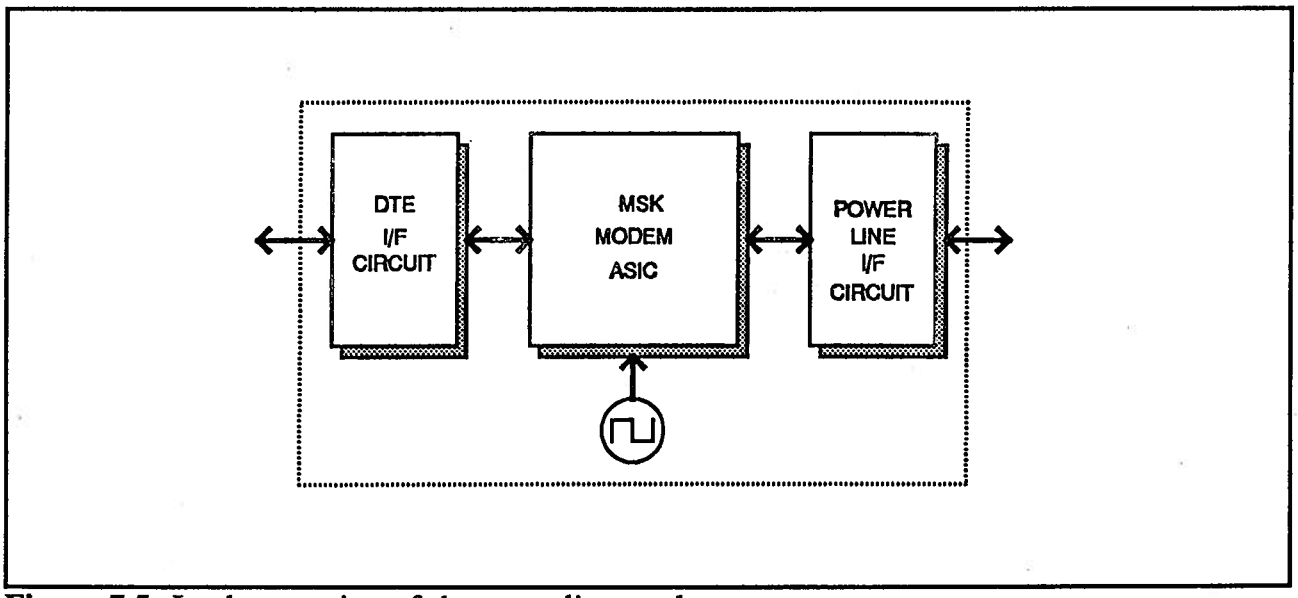


Figure 7.5: Implementation of the powerline modem.

5. Provision of impedance matching and surge protection.

Physically, the modem board contains two subcircuits, a semicustom ASIC, and a crystal oscillator, as shown in Figure 7.5. Both subcircuits are made up of off-the-shelf components. Subcircuit 1, which is partly analog and partly digital, functions as the DTE interface, and subcircuit 2, which is all analog, as the powerline interface. Modulation, demodulation, and carrier detection are handled by the MSK modem chip, the heart of the modem unit. This chip

operates in synchronism with the 5.0688 MHz (as determined below) clock supplied by the crystal oscillator that has an accuracy of 0.01%. In this design, because most of the signal processing functions, including carrier and bit synchronization, are implemented digitally, such problems as temperature drift and component aging are largely avoided. Furthermore, by means of VLSI implementation, the physical size, power consumption, and manufacturing cost of the modem are considerably reduced.

7.3 Modem Chip Application

With the bit rate and carrier frequencies specified, the modem chip's operational characteristics can be computed by using the design equations presented in previous chapters:

1. The modem chip should be driven at 5.0688 MHz in order to render 19.2 kbps transmission on 105.6 kHz and 115.2 kHz carriers (equations <5.4-6>).
2. With a system clock stability of 0.01%, the absolute and percentage phase jitter of the modulated output are approximately 7.8 Hz and 0.0071%, respectively (equations <3.1-2>).
3. The two on-chip carrier synchronizers have a lock range of 6.8 kHz. (equation <4.23>). This range is adequate because tone spacing is only 9.6 kHz.
4. The lock range of the on-chip bit synchronizer is approximately 0.05 kHz (equation <4.31>).
5. Carrier detection delay is $\approx 1.5 \times 16 \times 19200^{-1} = 1.25 \times 10^{-3}$ second (Section 3.3).

For decoupling purpose, several 0.1 μF capacitors are connected across power and ground in the proximity of the modem chip. In order to avoid CMOS latch-up [50], all unused input pins of the chip are pulled down via 10 kΩ resistors.

7.4 DTE Interface

Digital information is serially transferred between the DTE and modem chip via the DTE interface (subcircuit 1). Shown in Figure 7.6 is the schematic of this interface (adapted from R. Jeffery's work [61]). A hybrid analog/digital circuit built with off-the-shelf components, the interface provides the functions of RS232 signal conditioning and handshaking.

A universally accepted standard, RS232 specifies the electrical and mechanical details of the serial interface. The bipolar signal levels used in the RS232 standard are not at all compatible with CMOS levels, which are unipolar. Therefore it is necessary to convert those signals going

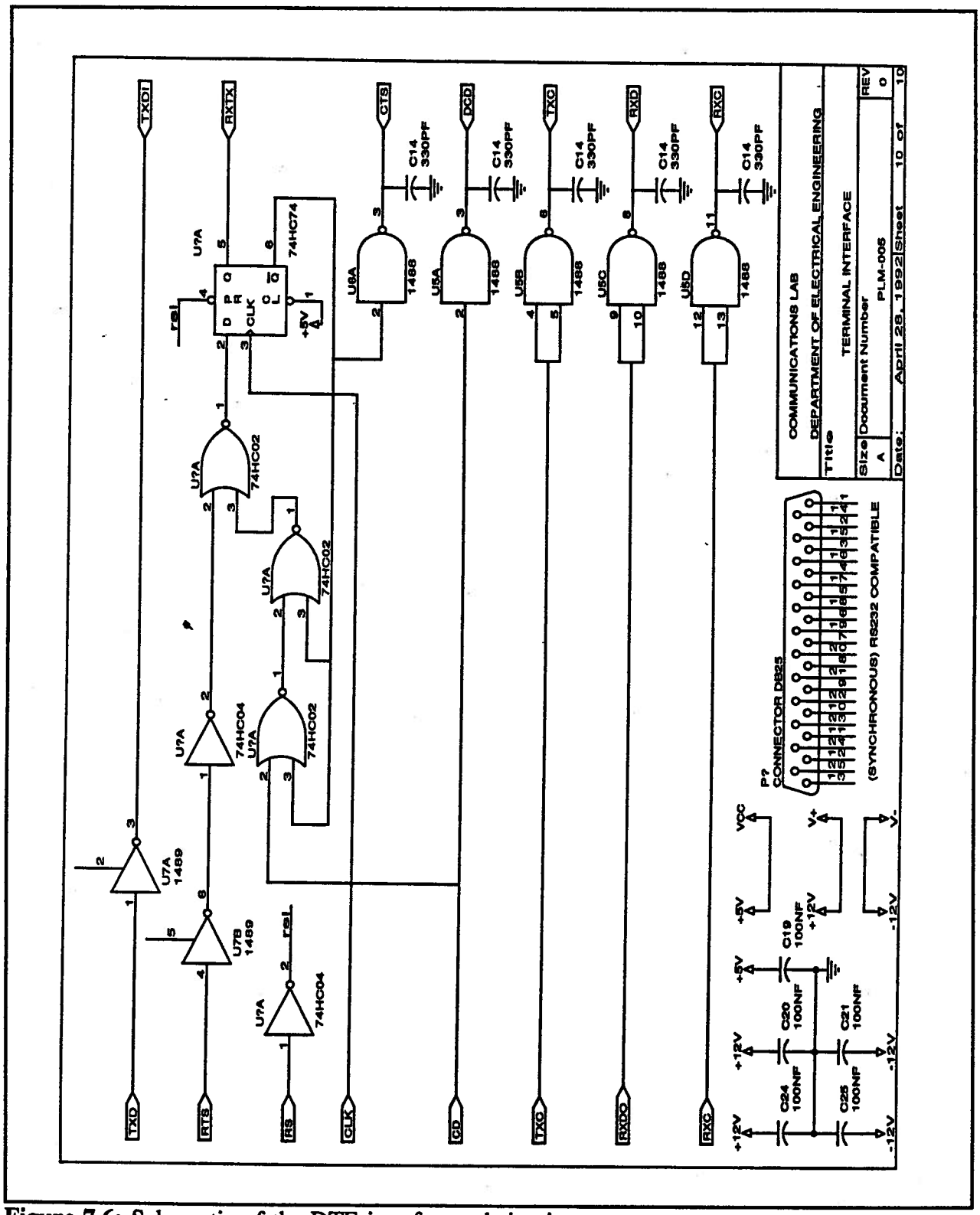


Figure 7.6: Schematic of the DTE interface subcircuit.

from the DTE to the modem from RS232 level to CMOS level, and vice versa for those signals going in the opposite direction. This two-way signal conditioning function is achieved in the subcircuit with the 1N14C88 driver ICs and 1N14C89 receiver ICs.

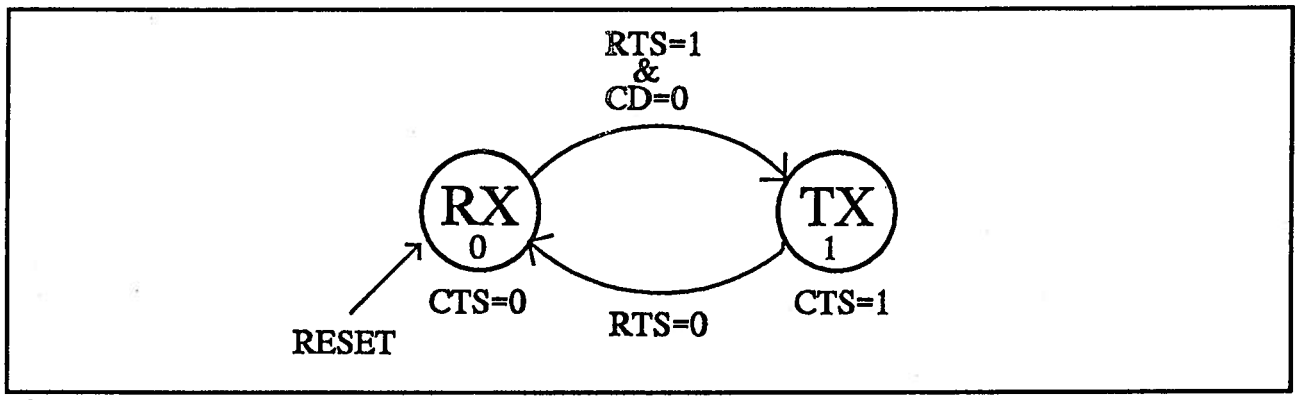


Figure 7.7: State diagram for RS232 interfacing.

With RS232, data transfer between the DTE and modem is coordinated with two signals: Request_To_Send (RTS) and Clear_To_Send (CTS). When the DTE has data to transmit, it asserts RTS high. Then, if the channel is sensed to be idle, the modem will assert CTS high to permit the DTE to start a transmission. On the other hand, if carrier presence is detected, CTS will remain inactive thus forbidding the DTE to transmit. This kind of handshaking is controlled in the DTE interface with a simple one-flip-flop-based state machine. Figure 7.7 shows the corresponding state diagram. Basically, the circuit sets CTS according to the status of RTS, and Carrier_Detect (CD). The latter, originating from the modem chip, is an active high signal indicating carrier presence. CTS is asserted high if and only if RTS is high and CD is low. CTS is reset when RTS is released at the end of a transmission. CTS also reflects the transmit/receive status of the modem: when CTS is high, the modem transmits; otherwise, the modem receives, which is the default state.

7.5 Powerline Interface

Figure 7.8 shows the schematics of the powerline interface (originally designed by R. Jeffery [61]). Made up of off-the-shelf analog components, the interface includes a line coupling network, a relay, a transmit signal processing circuit, and a receive signal processing circuit. The line coupling network consists of a 1:1 transformer, a zener diode, and two capacitors. The

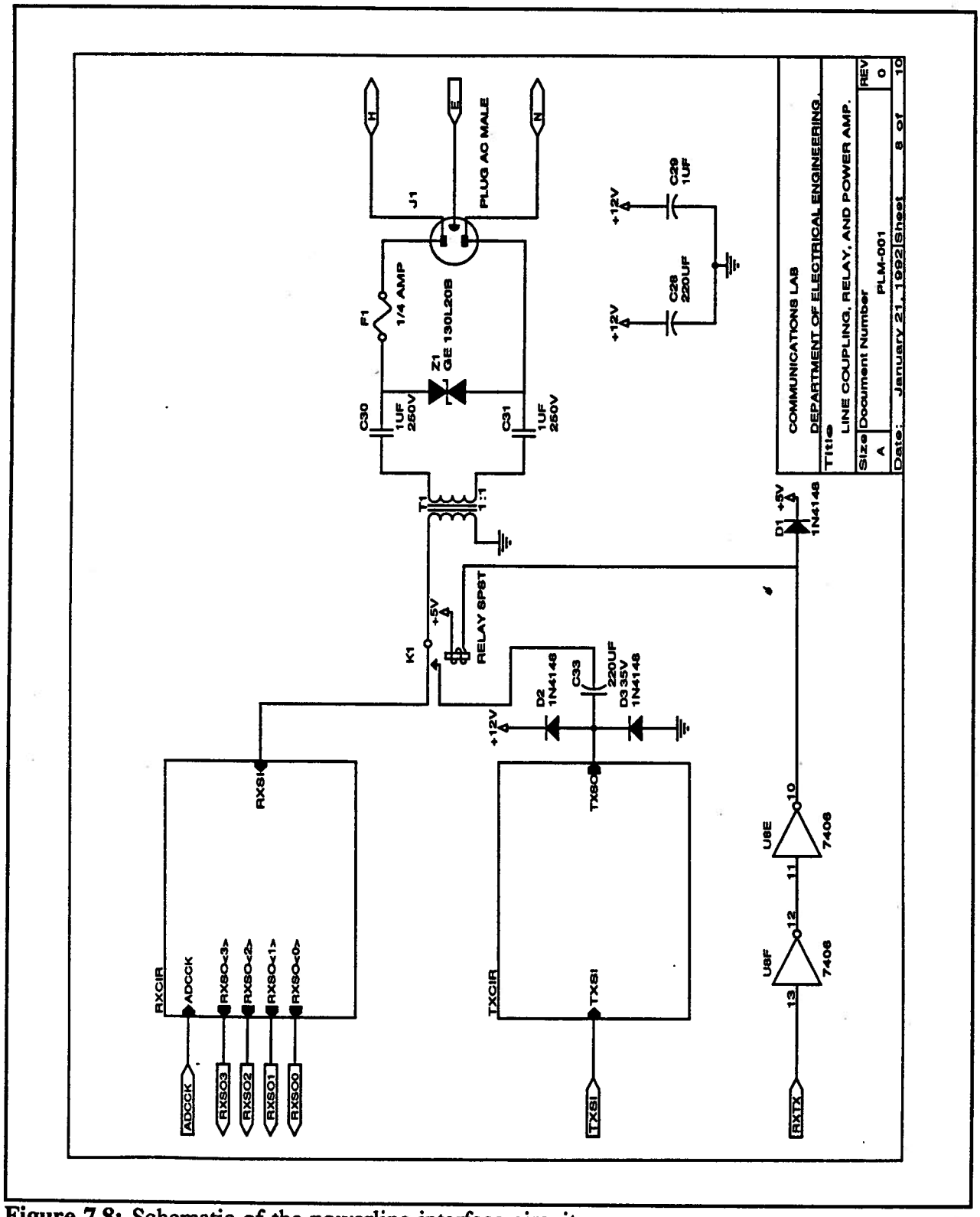


Figure 7.8: Schematic of the powerline interface circuit.

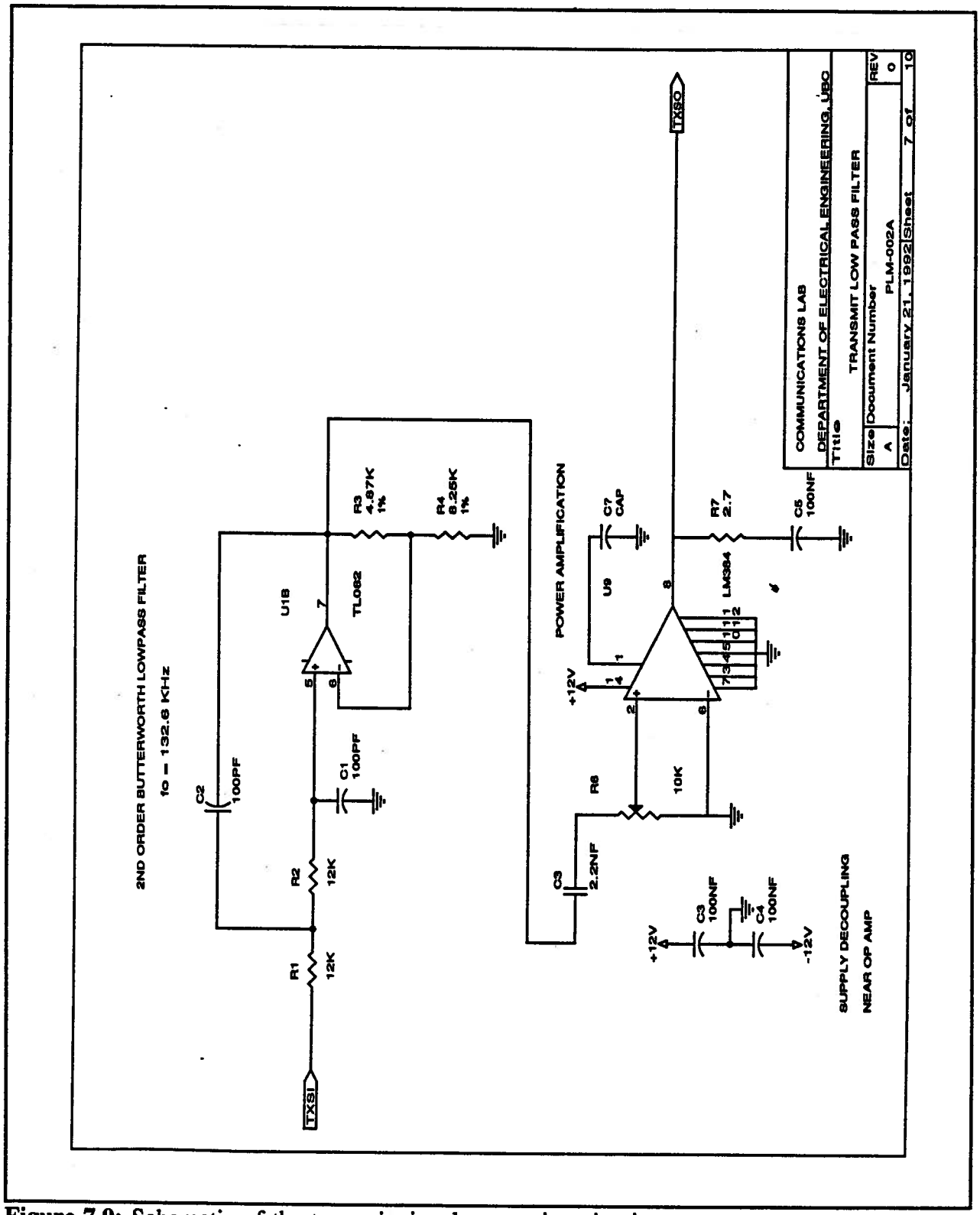


Figure 7.9: Schematic of the transmit signal processing circuit.

coupling network facilitates AC coupling of carrier signal to and from the powerline while isolating the rest of the modem from 120 V AC. In addition, it provides impedance matching and surge protection. The transmit and receive circuits access the line coupling network through the relay. This relay is controlled by the CTS signal from the DTE interface: when CTS is high, the relay goes on, connecting the output of the transmit circuit to the line coupling network; when CTS is low, it goes off, connecting the output of the receive circuit to the line coupling network.

In the transmit circuit (Figure 7.9), the modulated square wave carrier output of the modem chip is filtered by a 2nd-order bandpass filter, that has a bandwidth of 100 kHz, centring at 90 kHz. Before being relayed to the line coupling network, the resulting sinusoidal waveform is amplified with an audio power amplifier (LM384) that has a voltage gain of 50. The bandpass filter also helps to suppress any spurious components generated by the modulator.

In the receive direction (Figure 7.10), the analog signal received from the powerline via the line coupling network is filtered by a 4th-order Butterworth bandpass filter to extract the MSK waveforms. This bandpass filter also prevents possible overloading of the received input signal by noise. The filter bandwidth is 40 kHz, centred at 110 kHz. Its output is amplified with LF356 by a factor of 20. Subsequently, a comparator (LM339) hardlimits the signal so that it can be input to the modem chip for demodulation. Alternatively, one may use a 4-bit A/D converter to digitize the signal because, as mentioned in Section 4.2, the received input to the modem chip can be either a 1-bit or 4-bit word.

7.6 System-Level Design

Figure 7.11 contains the board-level modem schematic showing interconnections among the DTE interface subcircuit, the modem chip, and the powerline interface subcircuit. The modem board requires +5 V, +12 V, and -12 V DC supplies, and has a maximum power rating of 3.5 W. Also, it uses a 25-pin D-connector to communicate with the DTE, and a three-prong plug to access the powerline. For instance, in the case of a PC host, one end of the modem will be connected to the serial port of the PC, and the other end plugged into an AC outlet. To utilize this powerline modem, a DTE must be equipped with a synchronous RS232 serial card or its equivalent. In addition, it is the DTE's responsibility to append, probably via software, a preamble sequence to the beginning of each transmit data packet. This preamble should consist

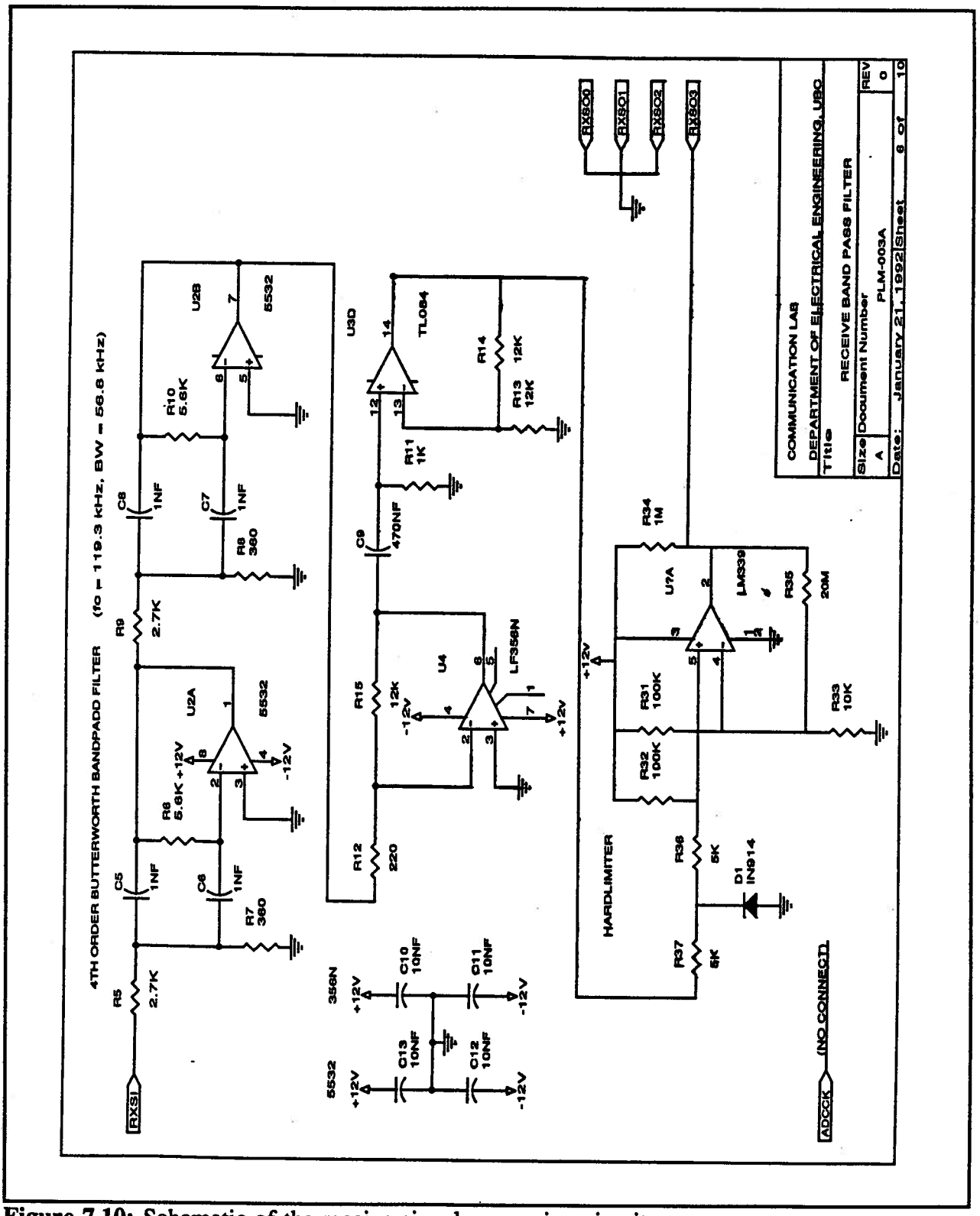


Figure 7.10: Schematic of the receive signal processing circuit.

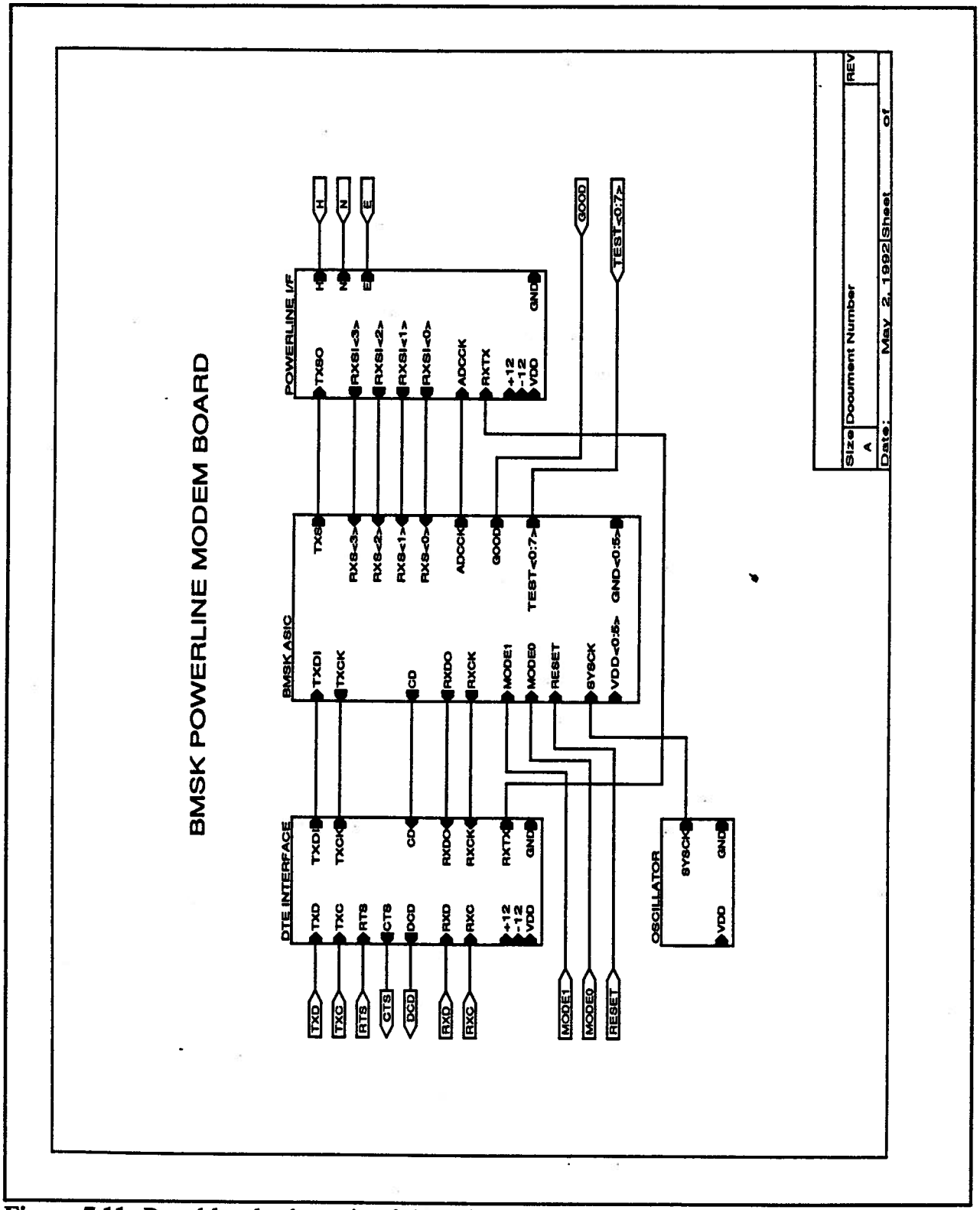


Figure 7.11: Board-level schematic of the MSK powerline modem.

of two segments: a reversal sequence and a sync word. The former, a sequence of alternating 0's and 1's, is recommended to be at least 236 bits long (see Section 5.4.5). It trains the receiving modem. The latter, also known as the frame marker, is usually less than 30 bits long. It is required for frame synchronization by the receiving DTE. Because of their special autocorrelation property, the Barker sequences and Willard sequences, among others, are good sync word selections [18].

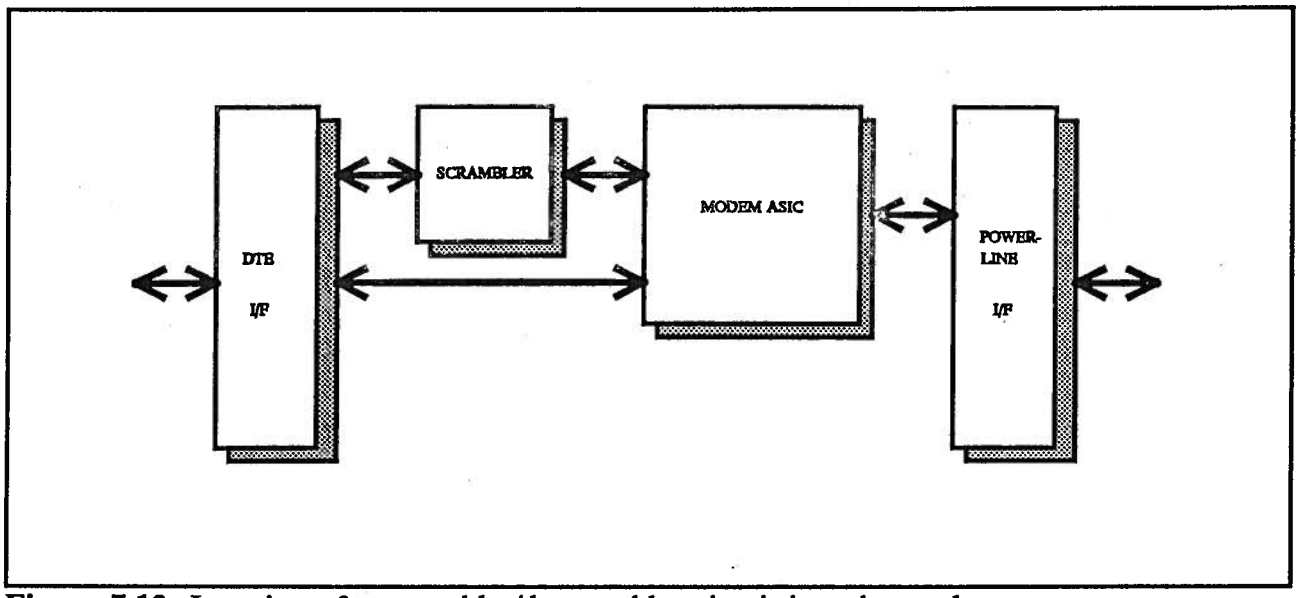


Figure 7.12: Insertion of a scrambler/descrambler circuit into the modem.

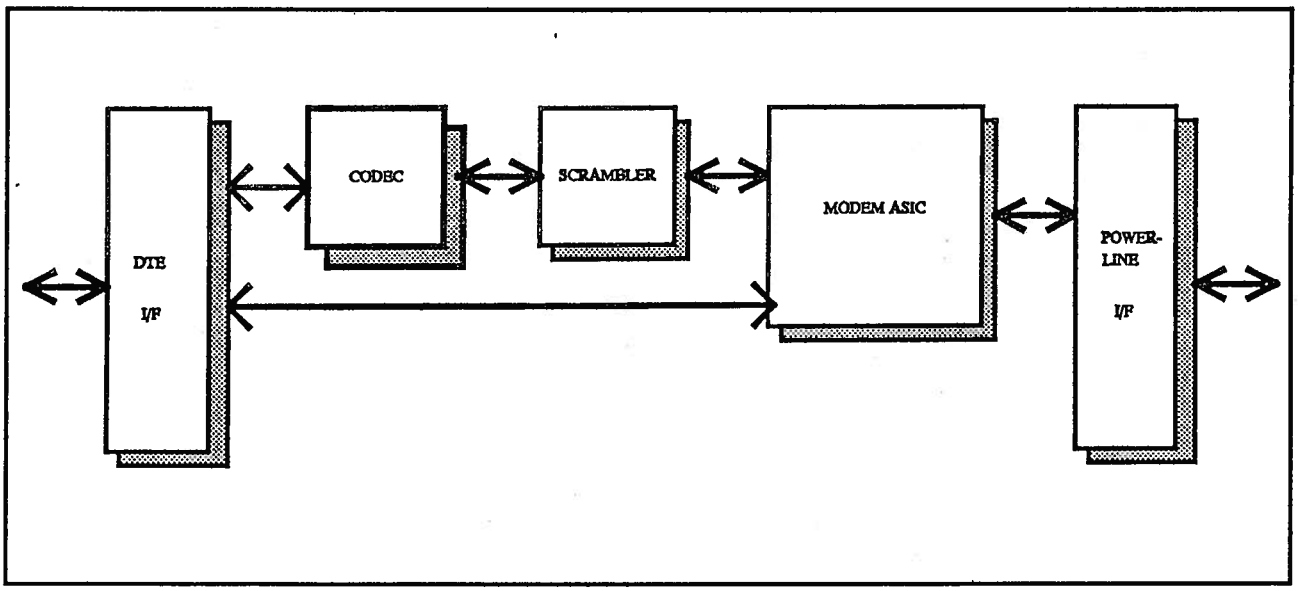


Figure 7.13: Enhanced modem with built-in scrambler/descrambler and codec.

The modem board can easily be modified to accommodate additional functions in the physical layer. One possibility is the insertion of a data scrambler between the DTE interface subcircuit and the modem chip (Figure 7.12). Data scrambling is highly recommended [62] because it has the merits of providing some communication security and preventing the receiver from loss of bit synchronization caused by long sequences of 0's and 1's in the data pattern. Another possible enhancement is to add a FEC codec chip in the data path (Figure 7.13). Convolutional coding and bit interleaving techniques are proved useful in combating impulse noise inherent in powerlines [63]. General purpose FEC chips are now commercially available [64, 65, 66]. As well, a special purpose FEC chip with bit interleaving capability is currently being developed at the University of British Columbia to accompany the MSK modem chip as part of a chip set for powerline LAN implementation.

8. TESTING AND PERFORMANCE EVALUATION

In this chapter, the design and performance of the MSK modem chip are tested and evaluated. This includes, first, functional verification of the integrity and operation of the chip, and, second, determination of the bit error rate, block error rate, and packet error rate of the powerline modem unit over an AWGN channel as well as actual intrabuilding powerlines. In addition, the modem's output spectrum, carrier phase and bit timing error characteristics are measured.

8.1 Functional Verification Of Modem Chip

Five modem chip samples are produced. To verify that they are properly fabricated and meet design specifications, three different tests are performed: BIST test, loopback self-test, and point-to-point test. The first of these is a pass/fail test which exercises the on-chip diagnostic circuit. In the latter two tests, the bit error performance of the chip is measured; moreover, its test pins are probed to check the internal signals as well as to measure the carrier phase and bit timing error of the on-chip demodulator.

8.1.1 Built-In Self-Test

As explained in Section 3.4, the BIST feature provides a quick and automatic means of testing the integrity of on-chip modulator and demodulator without using special test equipment. To run this test, the chip is first programmed into test mode (MODE1=MODE0=1), and the voltage level of the "GOOD" pin, which indicates test outcome, is displayed on an oscilloscope. Then BIST is activated by issuing a hardware reset (via the RESET pin). At the end of the test which lasts about 0.05 ms, GOOD should remain high if no errors are detected.

The BIST test is run on each of the five samples of the MSK ASIC. All give a positive result.

8.1.2 Loopback Self-Test

The setup for this test is depicted in Figure 8.1. With the chip in loopback mode

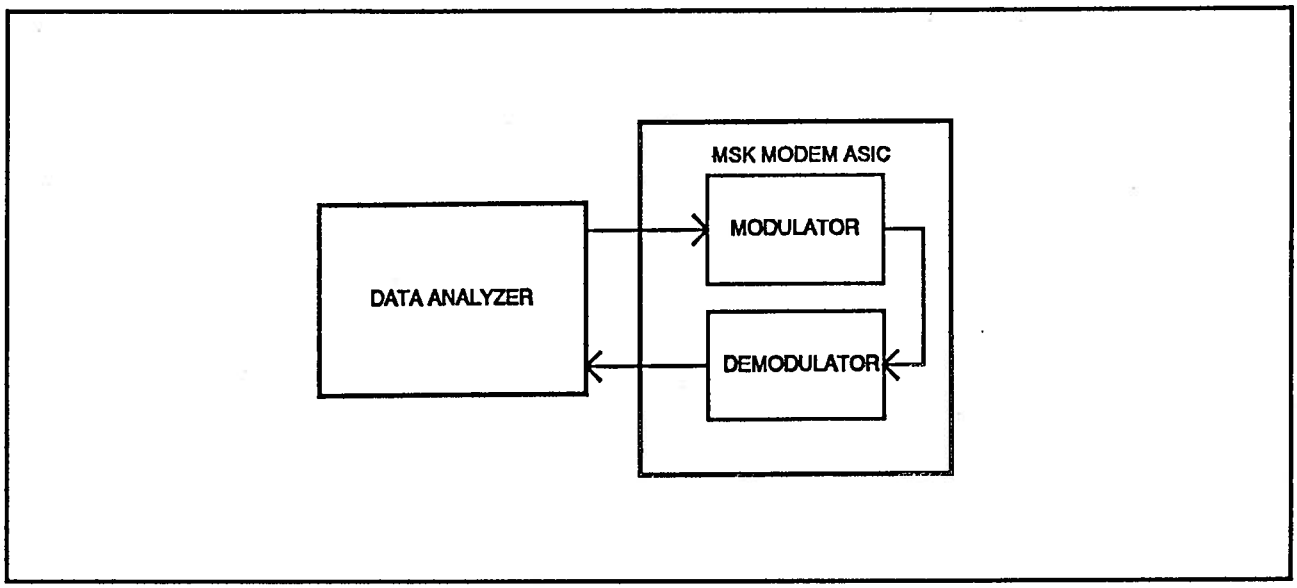


Figure 8.1: Chip-level loopback BER test.

(MODE1=1, MODE0=0), a HP 1645A data error analyzer is used to measure the bit error probability of the "noiseless" loopback connection. The analyzer injects pseudo-random test data into the modulator and monitors the resulting output of the demodulator for errors. After running the test at 19.2 kbps continuously for about 15 hours, the bit error probability is found to be less than 10^{-9}.

During this loopback self-test, the signals on the eight test pins of the chip (see Section 4.3) are examined with an oscilloscope. UD0 and UD1 give a good indication of the properness of the carrier synchronizing loops. One can tell whether the bit timing recovery loop is in lock or not by inspecting the ADD and DEL signals. MAXM and MAXP are the early and late versions of the locally recovered bit clock. SIG0 and SIG1 carry the demodulated subbit streams.

In addition, the carrier phase error of the demodulator is determined by measuring the minimum pulse width of the SIG0 and SIG1 signals. This pulse width is observed to be about 0.5 μs, which corresponds to a carrier phase error of ±3%.

To measure the bit timing jitter of the demodulator, the transmit clock generated by the modulator and the receive clock recovered by the demodulator are simultaneously displayed on a dual-trace oscilloscope. The waveforms indicate a received bit clock jitter of ±0.35 μs, which is approximately ±4% of the period of a 19.2 kHz clock.

8.1.3 Point-To-Point Transmission Test

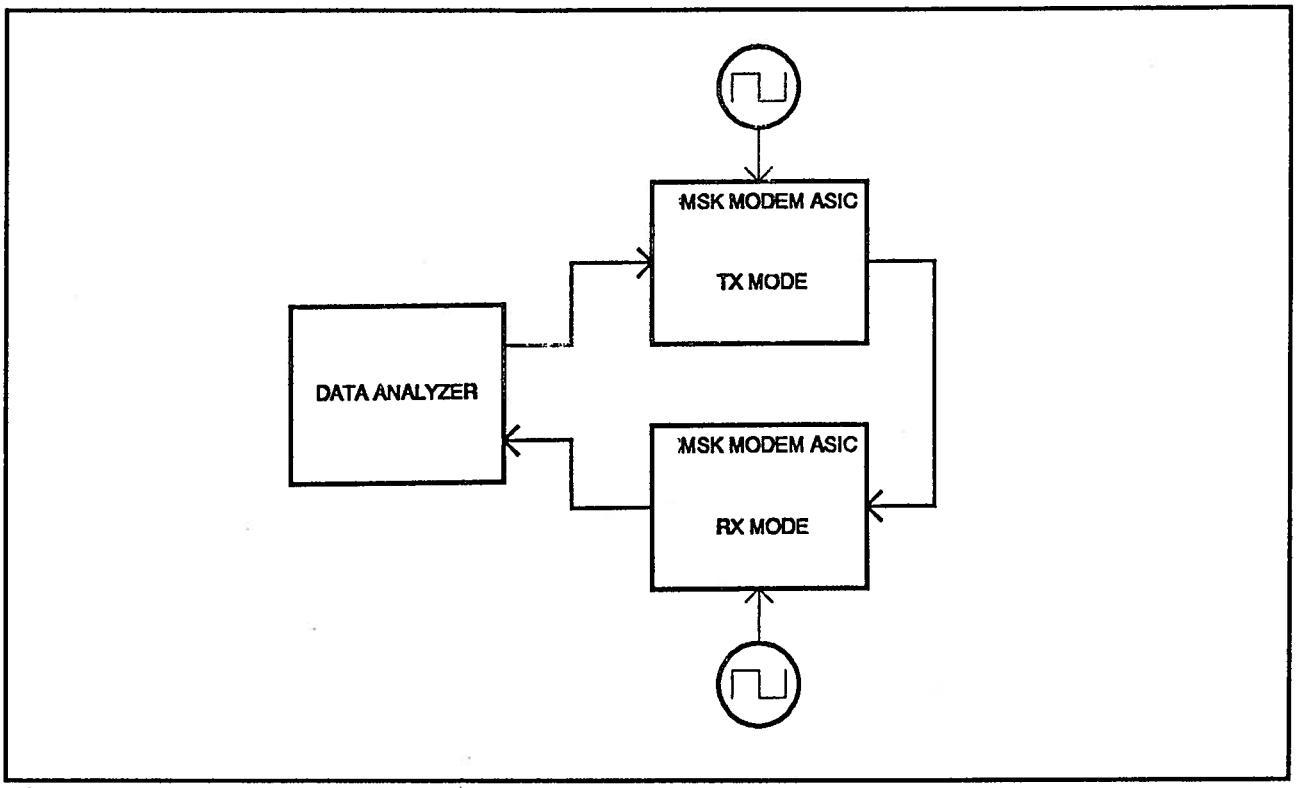


Figure 8.2: BER monitoring for inter-chip communications.

Shown in Figure 8.2 is the setup for the point-to-point transmission test. Again, the HP 1645A data error analyzer is used, but this time it determines the bit error probability of data transmitted from one chip to another via a copper wire approximately one foot long. The bit error probability of this system is measured to be less than 10^{-8}, thus validating the operation of the two chips.

During this point-to-point BER test, the test pins are probed to observe the operation of some internal circuitry. The average carrier phase error and bit timing error of the receiver are measured to be ±3% and ±4%, respectively.

8.2 Modem Performance In A Controlled Environment

In this section, the observed signal spectra and bit error rate (BER) of the MSK powerline modem unit in a controlled environment are reported.

8.2.1 Signal Quality

To measure signal quality, a modem board is set up to transmit pseudorandom data, generated by a data error analyzer, to another modem board at 19.2 kbps via a piece of one-foot-long copper wire.

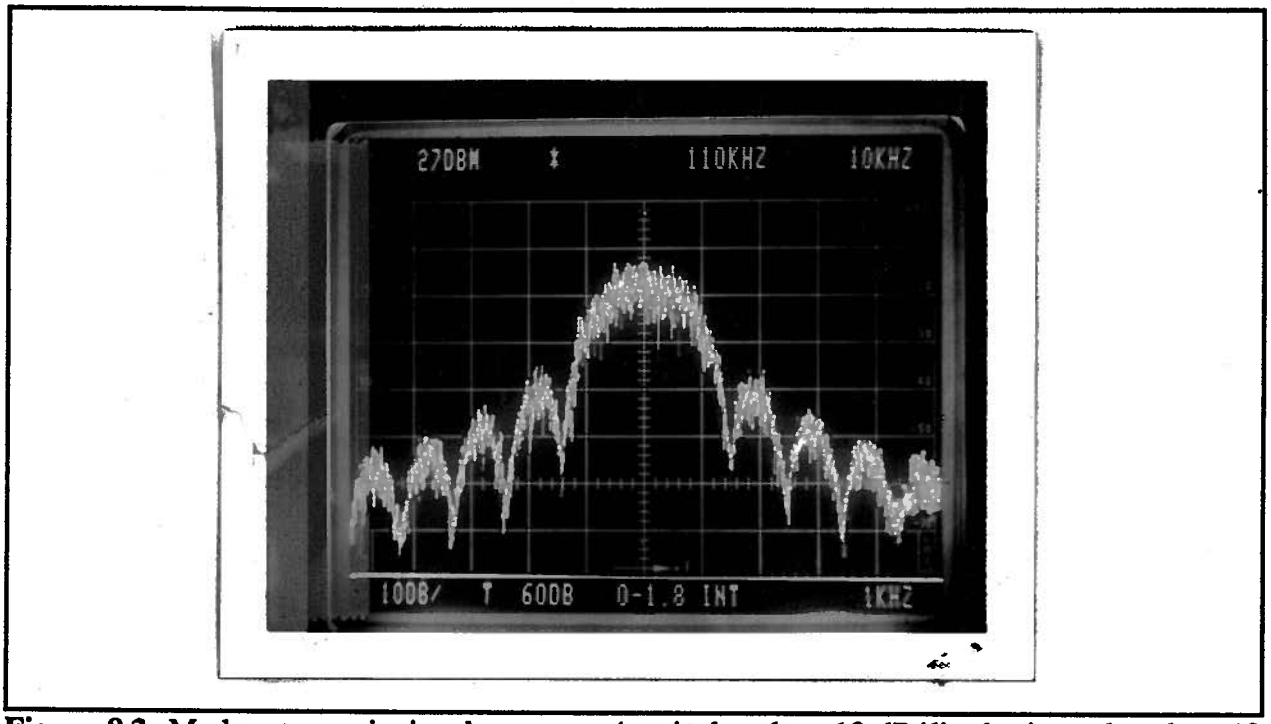


Figure 8.3: Modem transmit signal spectrum (vertical scale = 10 dB/div, horizontal scale = 10 kHz/div).

First, the frequency spectrum of the transmitted signal is obtained using a HP 497P spectrum analyzer, and it is shown in Figure 8.3.

Next, the timing jitter and frequency spectra of the 19.2 kHz receive clock signal are measured. The results appear in Figures 8.4 and 8.5.

Finally, by examining the SIG0, SIG1, and RXCK signals from the modem chip on the receive modem, the carrier phase error and bit clock jitter of the receiver are estimated to be ±4.5% and ±5%, respectively.

8.2.2 Performance In AWGN Environment

By using the setup shown in Figure 8.6, the bit error probability of the powerline modem

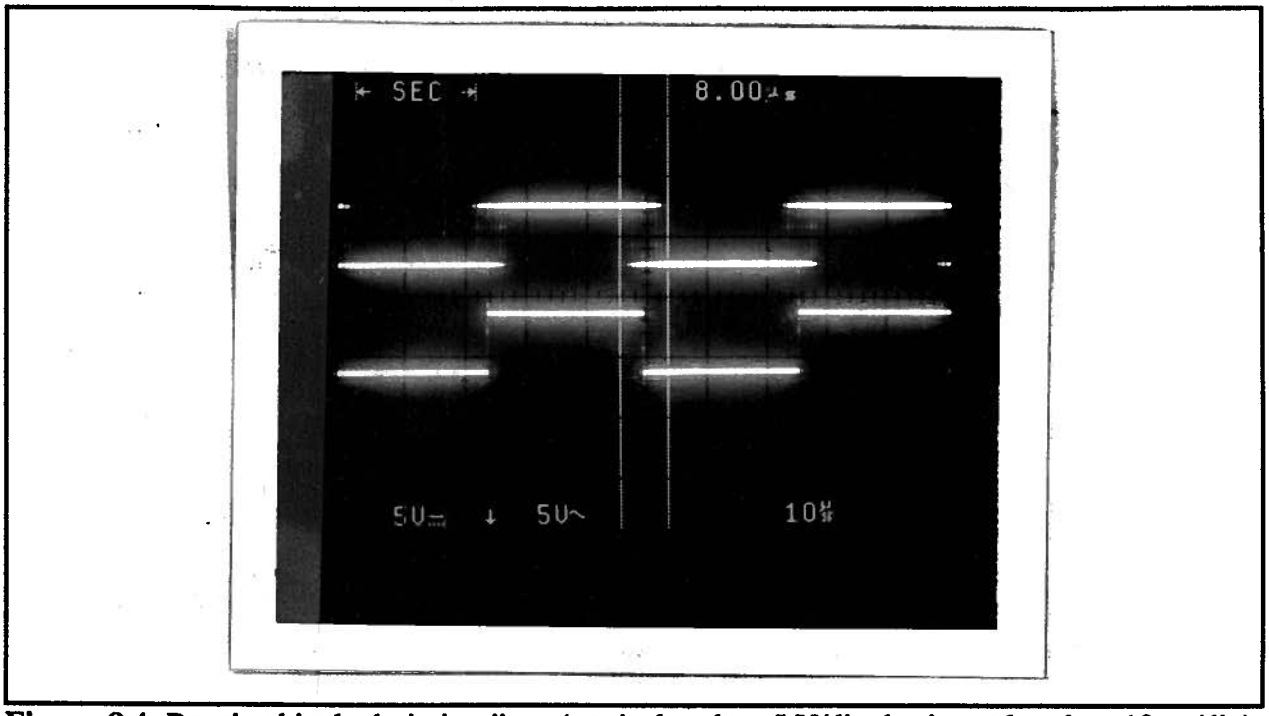


Figure 8.4: Receive bit clock timing jitter (vertical scale = 5 V/div, horizontal scale = 10 μs/div).

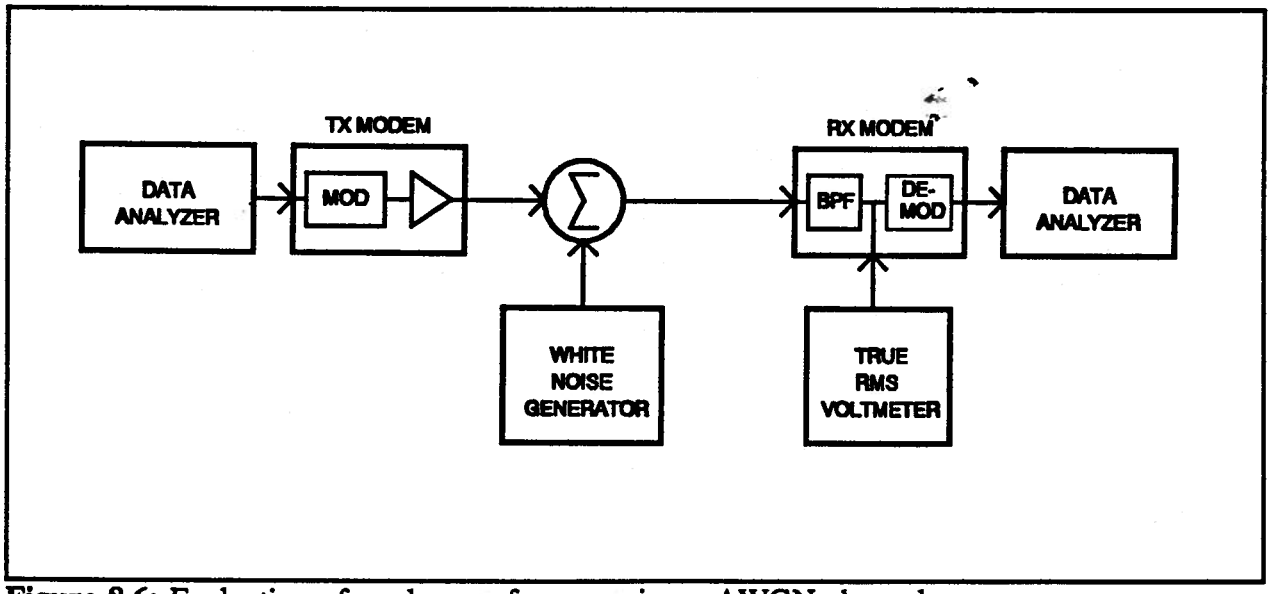


Figure 8.6: Evaluation of modem performance in an AWGN channel.

board over an AWGN channel is determined as a function of the received energy to noise ratio (E/N). To simulate an AWGN channel, white noise (from a Bruel & Kjaer 1405 noise generator) is added (using an op-amp) to the transmitted signal before it is sent to the receive modem over a one-foot-long copper wire. At the transmit end, test data is supplied to the transmit modem by

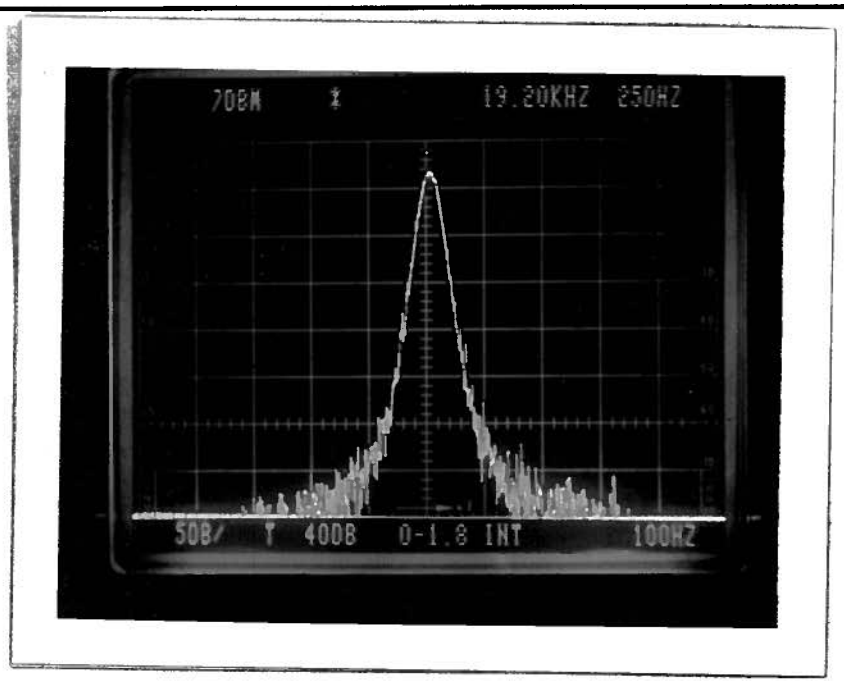


Figure 8.5: Spectral line at receive bit clock frequency (vertical scale = 5 dB/div, horizontal scale = 250 Hz/div).

a data error analyzer; at the receive end, another data error analyzer is employed to detect and count errors in the demodulated bit streams.

The output of the receive bandpass filter is monitored with a true rms voltmeter. Energy per bit, E, is given by:

$$E = K\frac{(V_{rms,s})^2}{R} \qquad \text{<8.1>}$$

where K = constant of proportionality, $V_{rms,s}$ = voltmeter reading with the white noise generator disabled, and R = bit transfer rate. In this case, R equals to 19.2 kbps. The noise density, N, is given by:

$$N = K\frac{(V_{rms,n})^2}{B_{eq}} \qquad \text{<8.2>}$$

where $V_{rms,n}$ = voltmeter reading with the transmitter switched off, and B_{eq} = equivalent noise bandwidth of the receive bandpass filter. By integrating the area under the frequency response curve of the filter, B_{eq} is found to be about 85 kHz.

Therefore from <8.1> and <8.2>,

$$\frac{E}{N} = \left(\frac{V_{rms,s}}{V_{rms,n}}\right)^2\left(\frac{B_{eq}}{R}\right) \qquad \text{<8.3>}$$

As a parameter, *E/N* is varied by adjusting the output level of the white noise generator while holding $V_{rms,s}$ fixed. For accuracy and precision, several BER measurements are taken for each *E/N* setting, with each BER measurement calculated from an error count of at least 100, if possible.

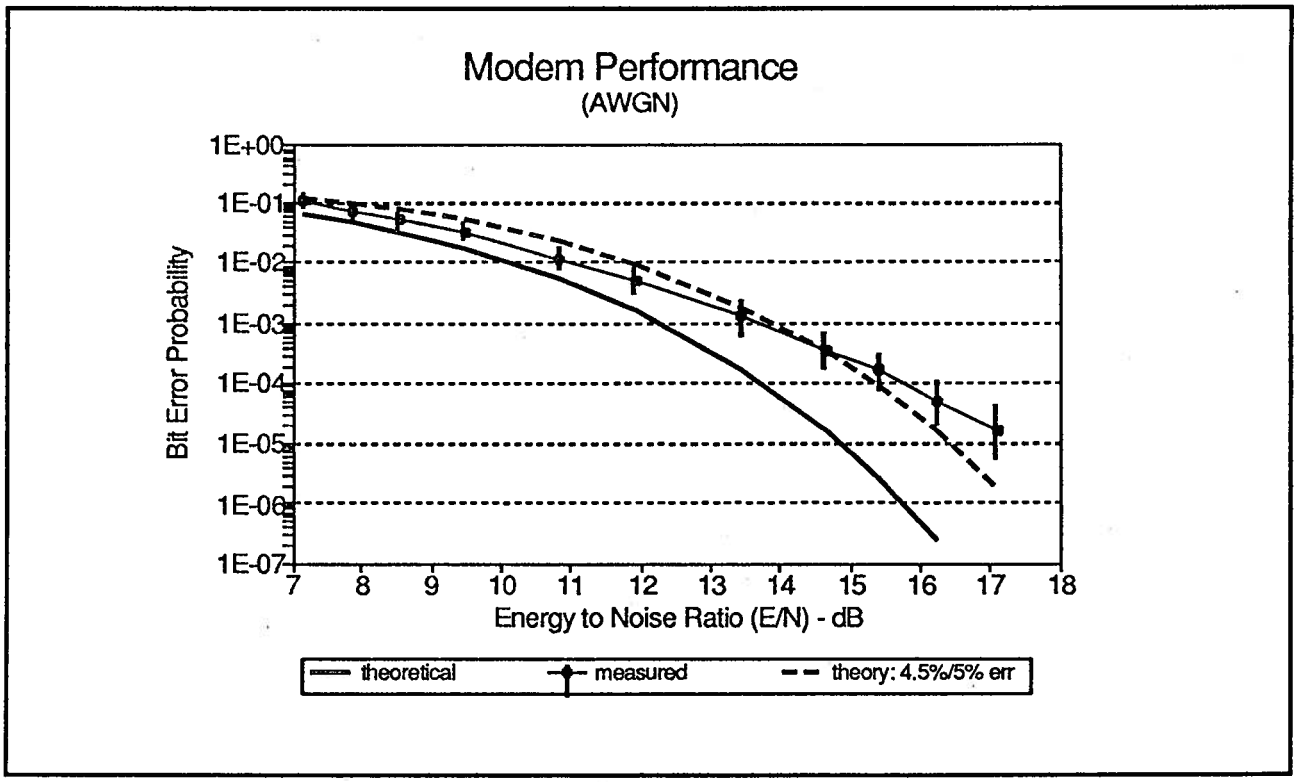


Figure 8.7: BER performance of the MSK modem in an AWGN environment.

The results of this experiment are plotted in Figure 8.7. Also shown in the figure are two theoretical BER curves computed using formula derived in Chapter 5. The first curve predicts the AWGN performance of the binary partial decision MSK demodulator under ideal condition (i.e. perfect synchronization). The second curve takes into account of the effects of carrier phase error and bit timing error, which are observed to be approximately ±4.5% and ±5%, respectively. The measured BER values are approximately 2 dB higher than the first curve, but are in close agreement with the second curve. Thus the modem's performance degradation in AWGN can be attributed primarily to imperfect carrier and bit synchronization.

8.3 Modem Performance On Powerline Channels

To evaluate the performance of the powerline modem over intrabuilding powerlines, its bit error rate (BER), block error rate (BLKER), and packet error rate (PKTER) for data transmission between two points in an actual intrabuilding powerline network are measured. The tests are conducted in the Macleod Building (Department of Electrical Engineering) located on the University of British Columbia campus. It is a large multi-use commercial building with four floors including a basement. A wide variety of loads are present, including industrial machinery, computers, and office equipment. This intrabuilding powerline network should be representative of those found in other commercial or industrial premises.

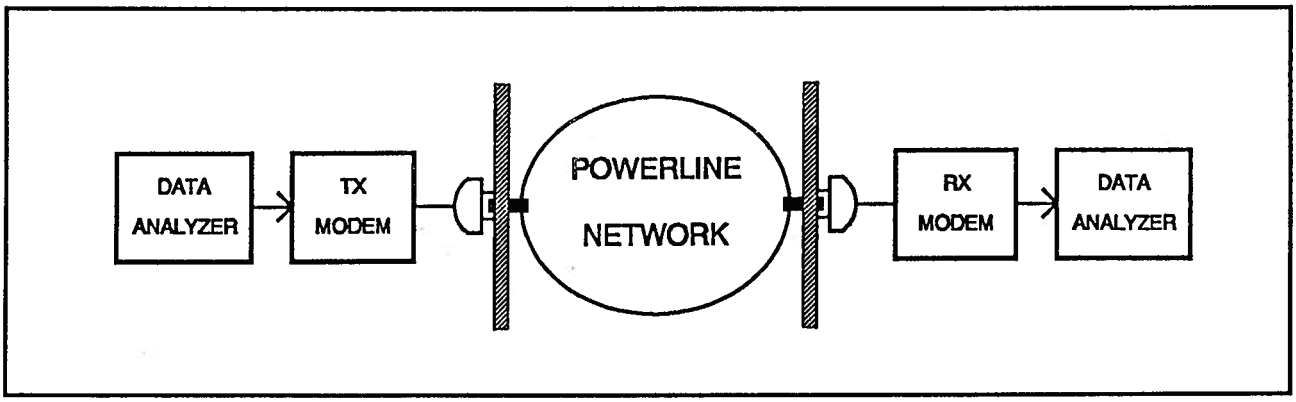


Figure 8.8: BER/BLKER measurement over intrabuilding powerlines.

The BER/BLKER test setup is diagrammed in Figure 8.8. Two modems, one as a transmitter and the other as a receiver, are plugged into separate AC outlets to access the powerline channel. At the transmit end, test data is supplied to the transmit modem by a data analyzer. At the receive end, demodulated data from the receive modem is submitted to another data error analyzer which measures the bit error rate and block error rate. Here the block error rate is defined as follows:

$$BLKER = \frac{(number\ of\ received\ blocks\ containing\ bit\ errors)}{(total\ number\ of\ transmitted\ blocks)} \qquad <8.4>$$

Each data block is 10000 bits in length.

In order for a data communication system to successfully receive a data packet, the following conditions must be satisfied:

(1) proper training of the receiving modem;

(2) recognition of the opening flag of the packet;

(3) recognition of the closing flag of the packet;

(4) no detected errors in data-carrying segment of the packet.

If any one of (1), (2) and (3) is not met, the transmitted packet will be lost. If (4) is violated, the received packet will be discarded. Thus, one can define the packet error rate as follows:

$$PKTER = \frac{(no.\ of\ lost\ packets) + (no.\ of\ received\ erroneous\ packet)}{(no.\ of\ transmitted\ packets)} \qquad <8.5>$$

While the block error rate is strictly attributed to noise-induced bit errors, the packet error rate depends on a number of additional factors, which include modem synchronization, frame synchronization, and data link control protocol. The packet error rate therefore a better and more realistic indication of overall transmission efficiency.

PKTER measurement is facilitated by specialized PC-based modem testing software developed at the Electrical Engineering Communications Laboratory in the University of British Columbia. In each test run, data packets of 1000-bit long are transmitted across the powerline from one PC to another; after 1000 packets are received, the test is terminated, and the

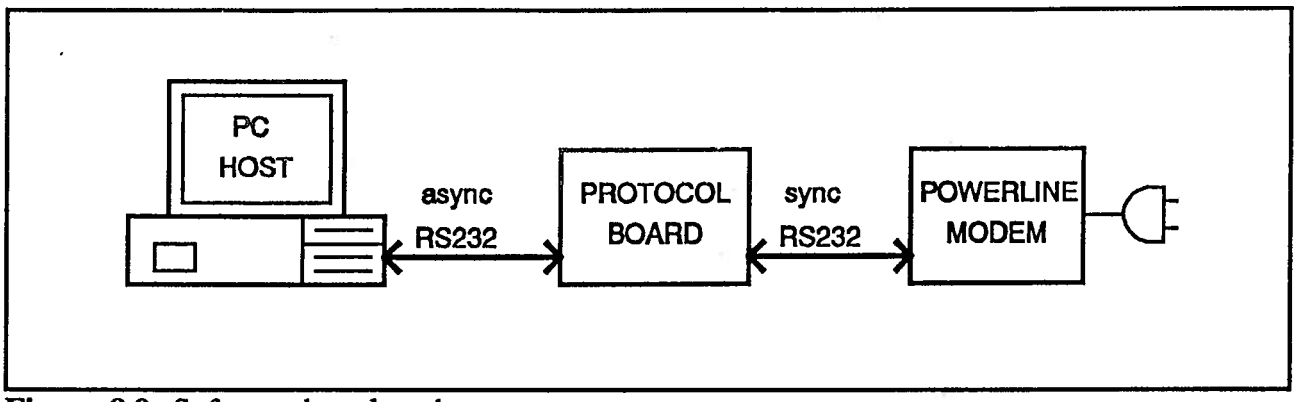


Figure 8.9: Software-based packet error rate measurement.

percentage of transmitted packets that are lost and the percentage of received packets containing bit error(s) are determined. Because the modem testing software is designed to operate with the asynchronous RS232 serial port of a PC, the modem board which supports only synchronous RS232 interface cannot be directly connected to the PC's serial port. This incompatibility is reconciled with the use of a protocol board (courtesy of Aries Wong), as shown in Figure 8.9. Having an asynchronous interface on its host side and a synchronous interface on its modem side, the protocol board performs frame synchronization and packet buffering.

8.3.1 Performance Over A Small Area

The BER, BLKER, and PKTER of the powerline modem for data communication within a room in the building are determined.

BER/BLKER Vs Transmitted Signal Level

First, the performance of the powerline modem over actual powerline channels is determined as a function of the rms output level of the transmitter (V_s). V_s is measured in units of dBmV:

$$dBmV = 20 \log[\frac{rms\ signal\ level\ in\ volts}{0.001}] \qquad \text{<8.6>}$$

Values of V_s range from 0 to 70 dBmV.

Two sets of measurements are made within Room 458, a research laboratory in the

building. In this room, there are ten Sun workstations, five PCs, as well as several electrical instruments such as oscilloscopes and function generators.

In the first set of measurements, the transmitter and receiver access the X, Y, and Z phases of the powerlines via outlets on two separate power-bars approximately 50 feet apart. The corresponding BER and BLKER results, as shown in Figure 8.10, indicate that transmissions in and between the X and Y phases are reasonably reliable. Their BERs are 10^{-5} or lower when V_s is above 55 dBmV. Performance increases with V_s, with in-phase transmission having a 10 dBmV advantage over cross-phase transmission. Conversely, for those transmissions involving the Z phase, be they in-phase or cross-phase, the BERs are very high ($\sim 10^{-1}$) for all V_s values. This implies that the Z phase of the powerline is relatively noisy; indeed, most workstations in the room draw power from this phase.

In the second set of measurements, the transmitter and receiver are side-by-side, accessing the powerlines via outlets on a single power-bar. Figure 8.11 shows the results obtained for this set of measurements. They are very similar to those of the first set of measurements, except that considerably better performance is attained for in-phase transmission over the Z phase. This improvement can be attributed to the fact that the corresponding transmission segment is short and localized.

Packet Error Rate

Power Phase	Packet Error Rate	Packet Loss Rate
X -> X	~ 0%	~ 0 %
X -> Y	~ 0%	~ 0 %
X -> Z	~100%	~80 %

Table 8.1: Packet error/loss rate for transmissions between two power-bars 50 feet apart in the laboratory.

With the transmitter output fixed at 70 dBmV (8 V_{pp})., the packet error rates of the MSK modem for transmission between those two power-bars that are 50 feet apart are determined. Data are sent from the X phase of the first power-bar to the X, Y, and Z phases of the second power-bar. The measured PKTERs of these transmissions are listed in Table 8.1. Also tabulated there

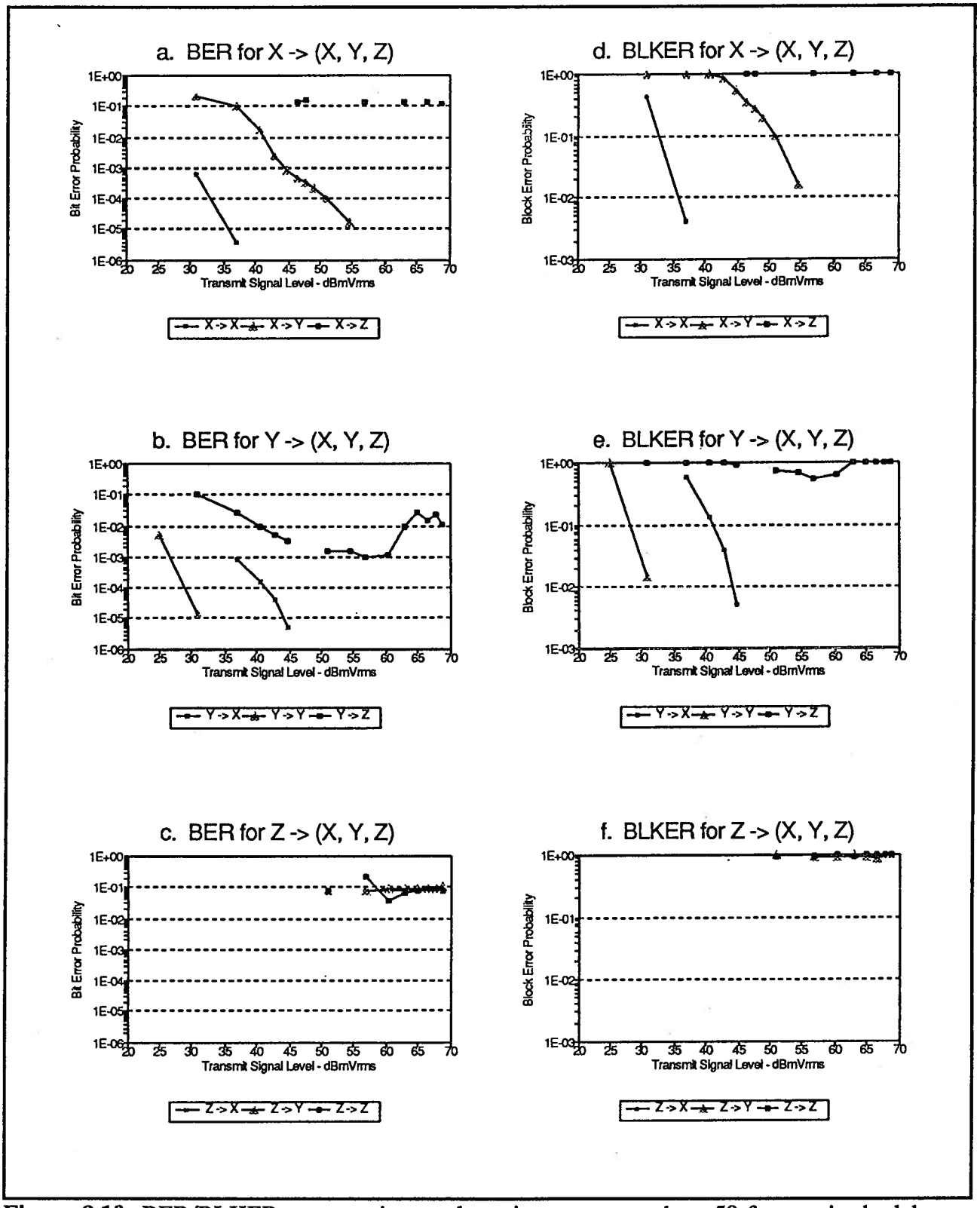


Figure 8.10: BER/BLKER -- transmitter and receiver on power-bars 50 ft apart in the lab.

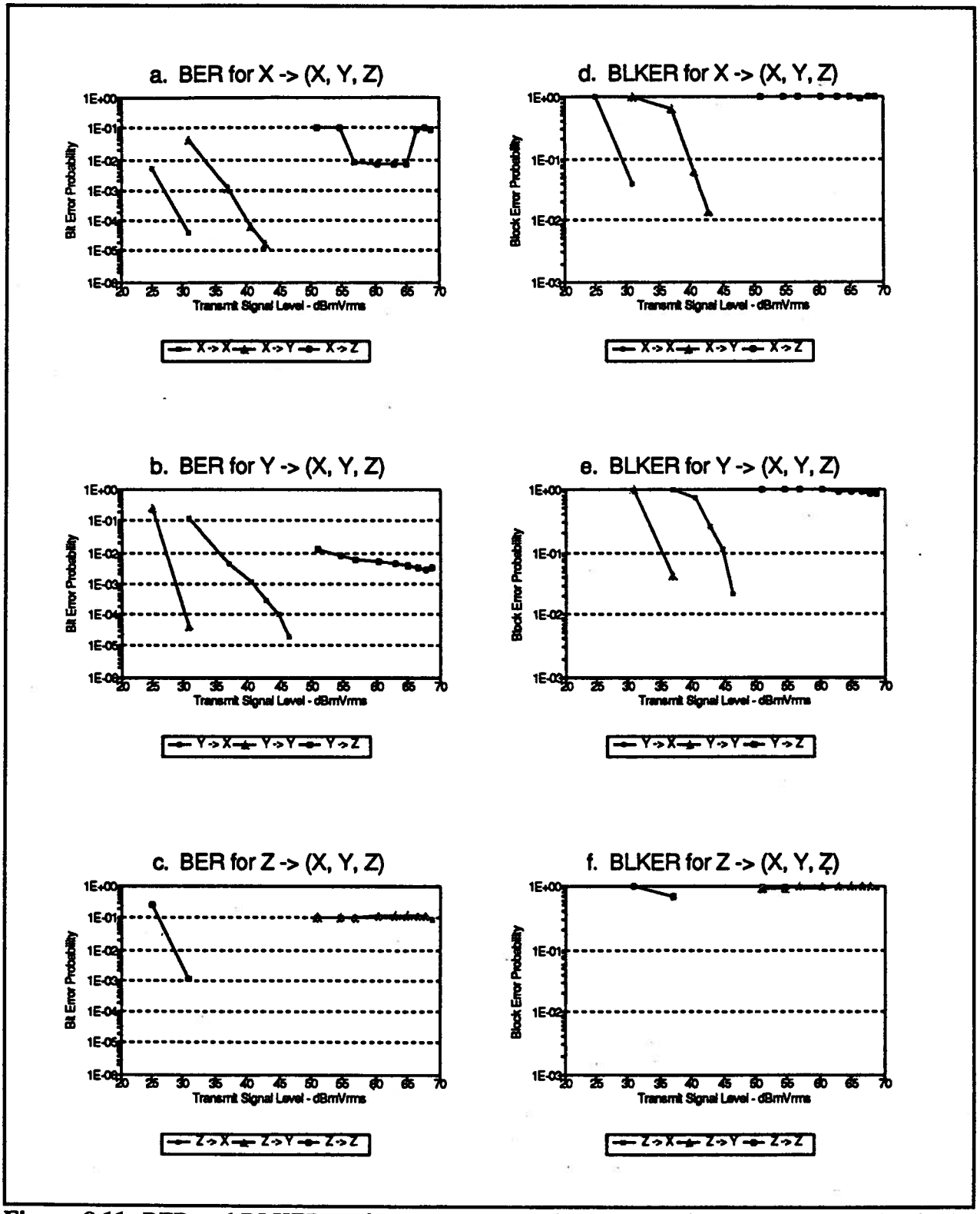


Figure 8.11: BER and BLKER performance -- transmitter and receiver on one power-bar in the laboratory.

are the corresponding packet loss rates (PKTLR), namely, the percentage of packets that are transmitted but not received.

As expected, the PKTER of a transmission is correlative with its BER/BLKER. Over a "good" link (BER $\approx 10^{-7}$ or lower), the PKTER is close to zero. Conversely, over a "poor" link (BER $\approx 10^{-2}$ or higher), the PKTER and PKTLR can reach as high as 100% and 80%, respectively.

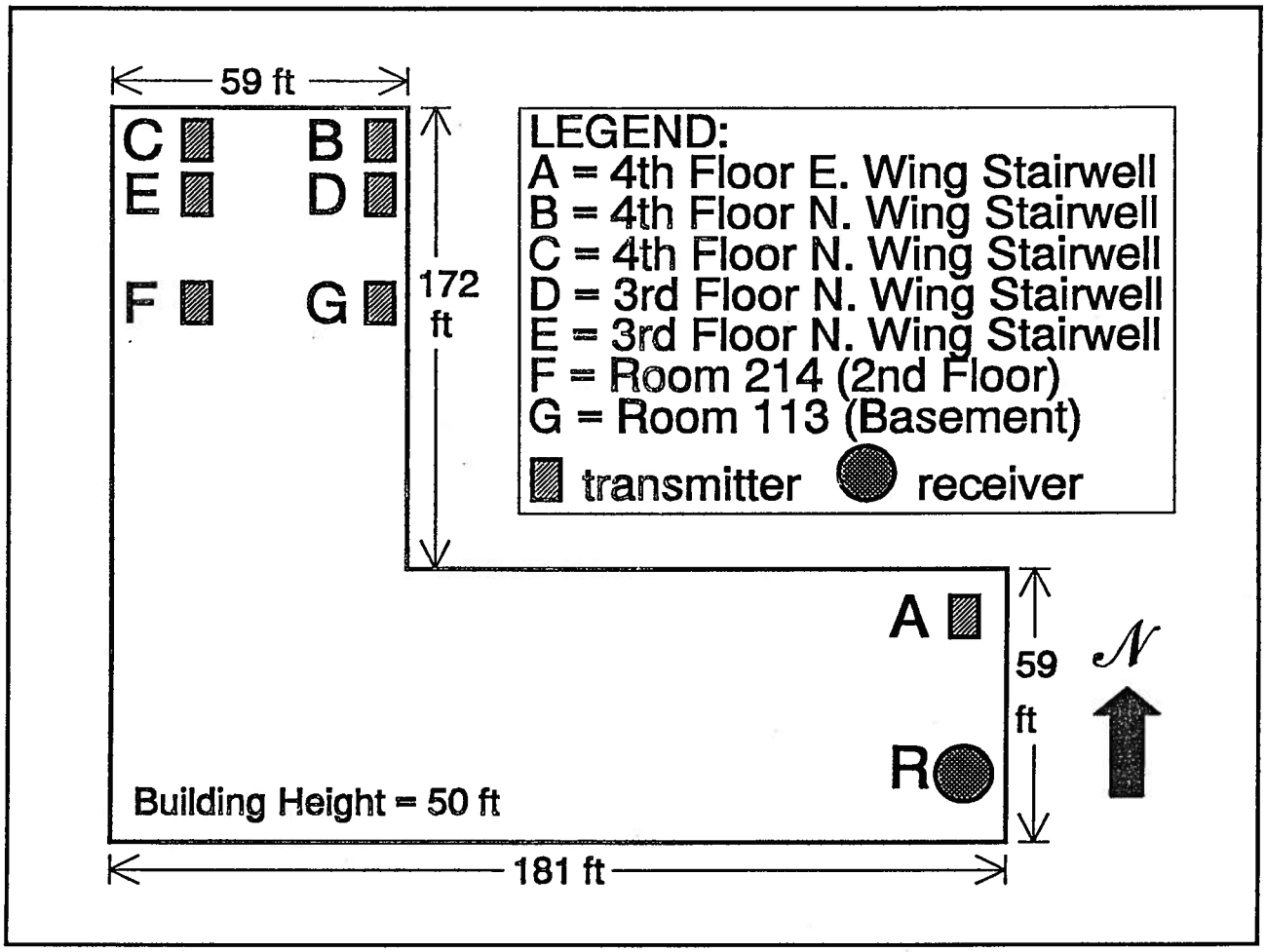


Figure 8.12: Locations of various access points in the building.

8.3.2 Performance Over A Large Area

Described below are the measured BER, BLKER, and PKTER of the powerline modem for data communications across the building.

Designation	Location	Power Phase
A	4th Floor East Wing Stairwell	Y
B	4th Floor North Wing Stairwell	X
C	4th Floor North Wing Stairwell	Z
D	3rd Floor North Wing Stairwell	X
E	3rd Floor North Wing Stairwell	Z
F	Room 214 (2nd Floor)	Y
G	Room 113 (Basement)	Z

Table 8.2: Power phase on various AC outlets in the building.

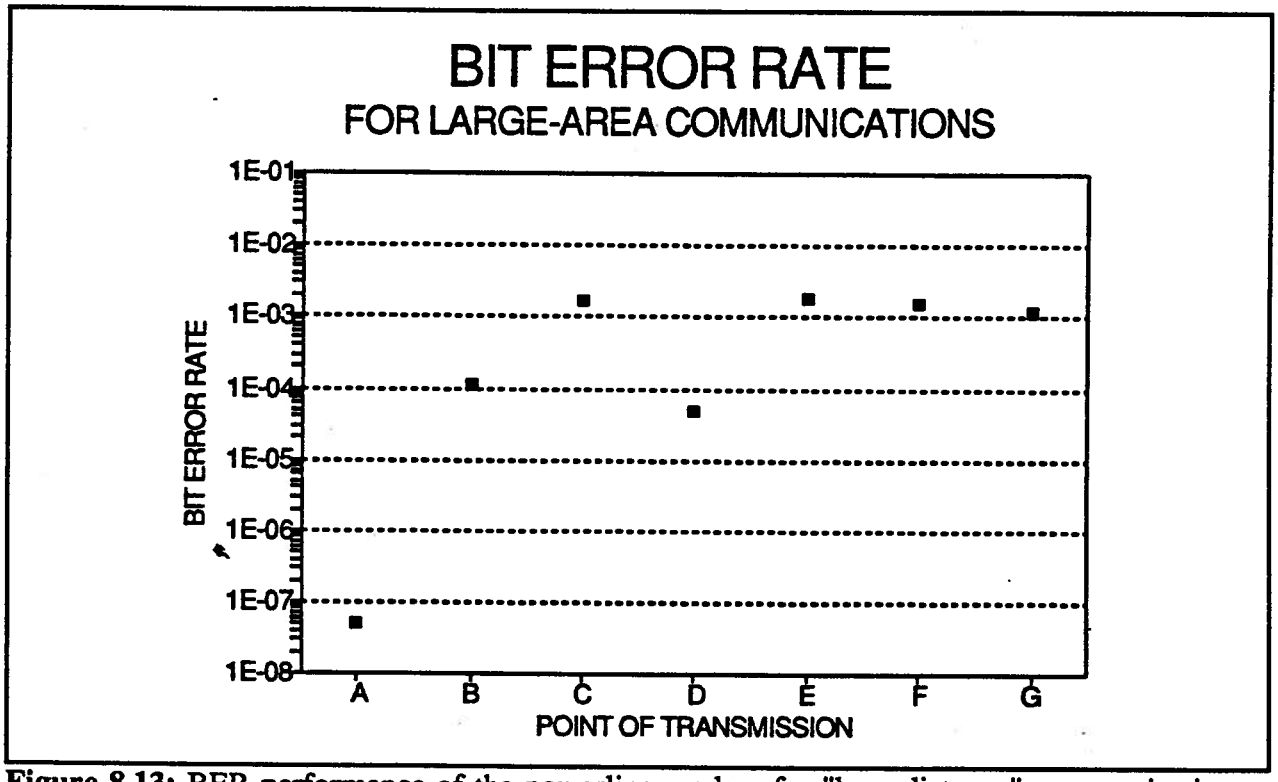


Figure 8.13: BER performance of the powerline modem for "long-distance" communications.

BER/BLKER Vs Modem Separation

With the transmitter output fixed at its maximum level of 70 dBmV, the bit error rate and block error rate of the modem over powerline channels linking different areas of the building are determined. Four groups of measurements are taken:

1. intra-floor-44: transmission between two points on the third floor;
2. inter-floor-34: transmission from an AC outlet on the second floor to one on the third floor;

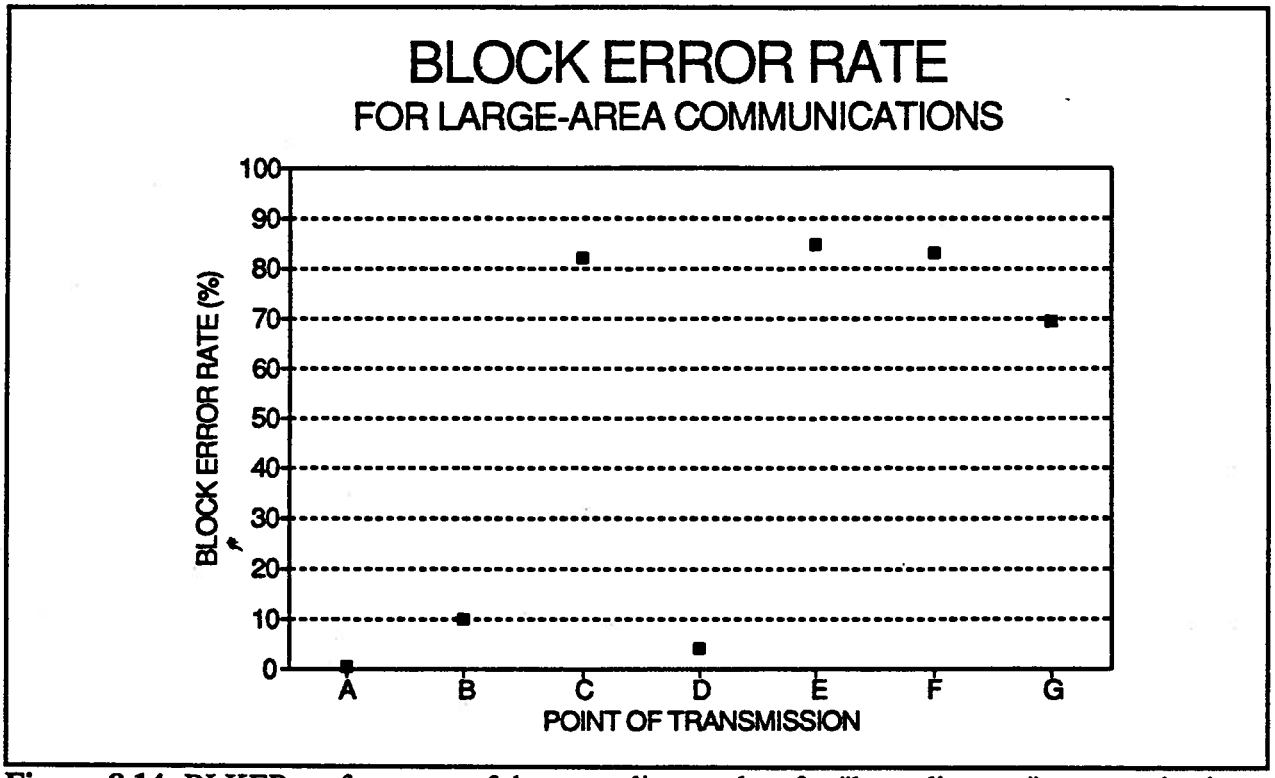


Figure 8.14: BLKER performance of the powerline modem for "long-distance" communications.

3. inter-floor-24: transmission from an AC outlet on the first floor to one on the third floor;
4. inter-floor-14: transmission from an AC outlet in the basement to one on the third floor.

Shown in Figure 8.12 is a map indicating the locations of the AC outlets used in these measurements. The power phases of the outlets are identified in Table 8.2.

The modem's BER and BLKER over each link are determined by averaging values obtained from several consecutive test runs, each having at least 100 accumulated bit errors. The results are presented in Figures 8.13 and 8.14.

For thoroughness, additional BER tests are conducted using several other transmit points (unidentified in Figure 8.12) throughout the building, and the outcomes are summarized in Figure 8.15.

Overall, the BER performance of the MSK powerline modem ranges from 10^{-2} to less than 10^{-7}, and is fairly independent of the physical separation of the transmitter and receiver. Instead, BER depends on other factors, which, in order of importance, include:

1. whether the transmission path is in-phase or cross-phase;

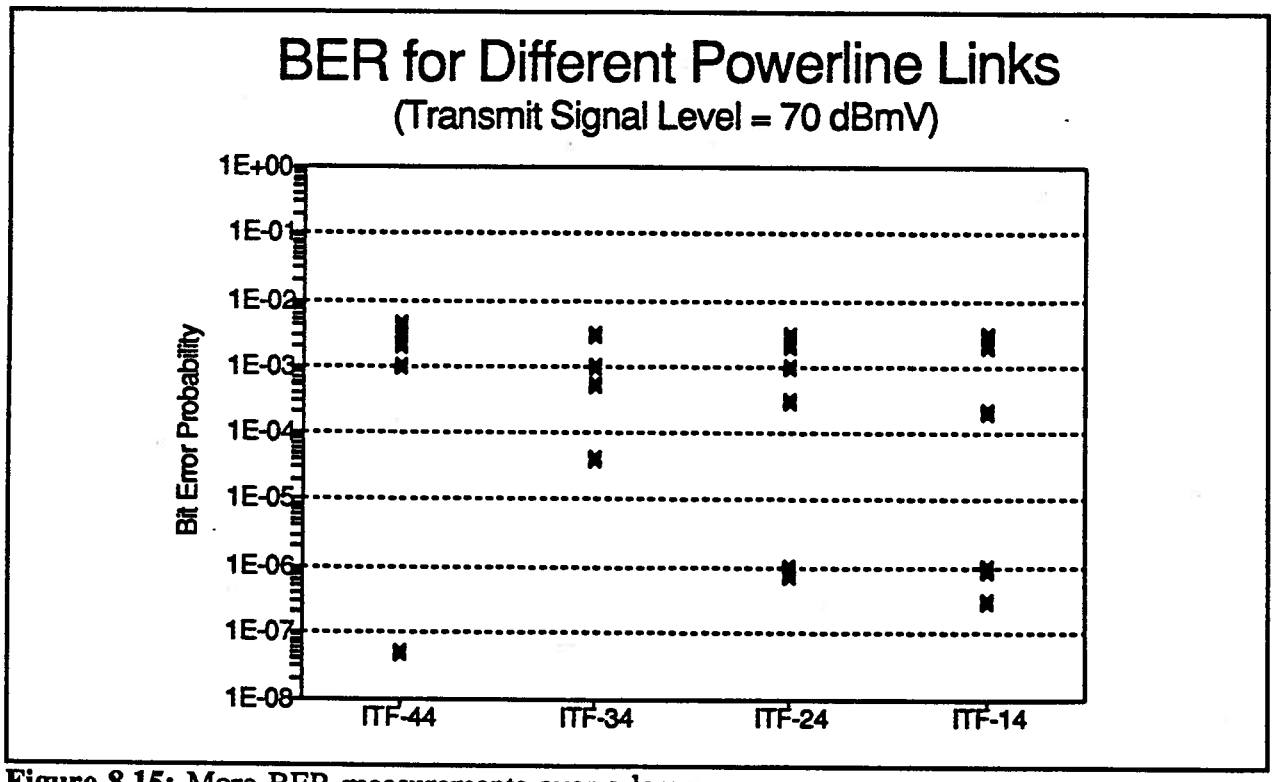


Figure 8.15: More BER measurements over a large area.

2. the loading profile of the channel;

3. the time and day on which the measurement is taken.

In general, for "large-area" communication, better performance can be achieved over an in-phase path than an cross-phase path. The BER of transmission over an in-phase path usually falls into the range from 10^{-5} to less than 10^{-7}. When switched over to an cross-phase path, the BER is degraded by approximately two to three order of magnitude and ranges from 10^{-2} to 10^{-5}. There are exceptions, however; for example, in some inter-floor in-phase transmissions, the observed BERs are in the neighbourhood of 10^{-3}.

Packet Error Rate

With the transmitter output fixed at 70 dBmV, the packet error rates of the powerline modem for transmission over a large area are determined. The same access points as those identified in Figure 8.12 are chosen for transmission and reception. The results are graphed in Figure 8.16, indicating both the packet error rates and the percentages of lost packets. Over a link

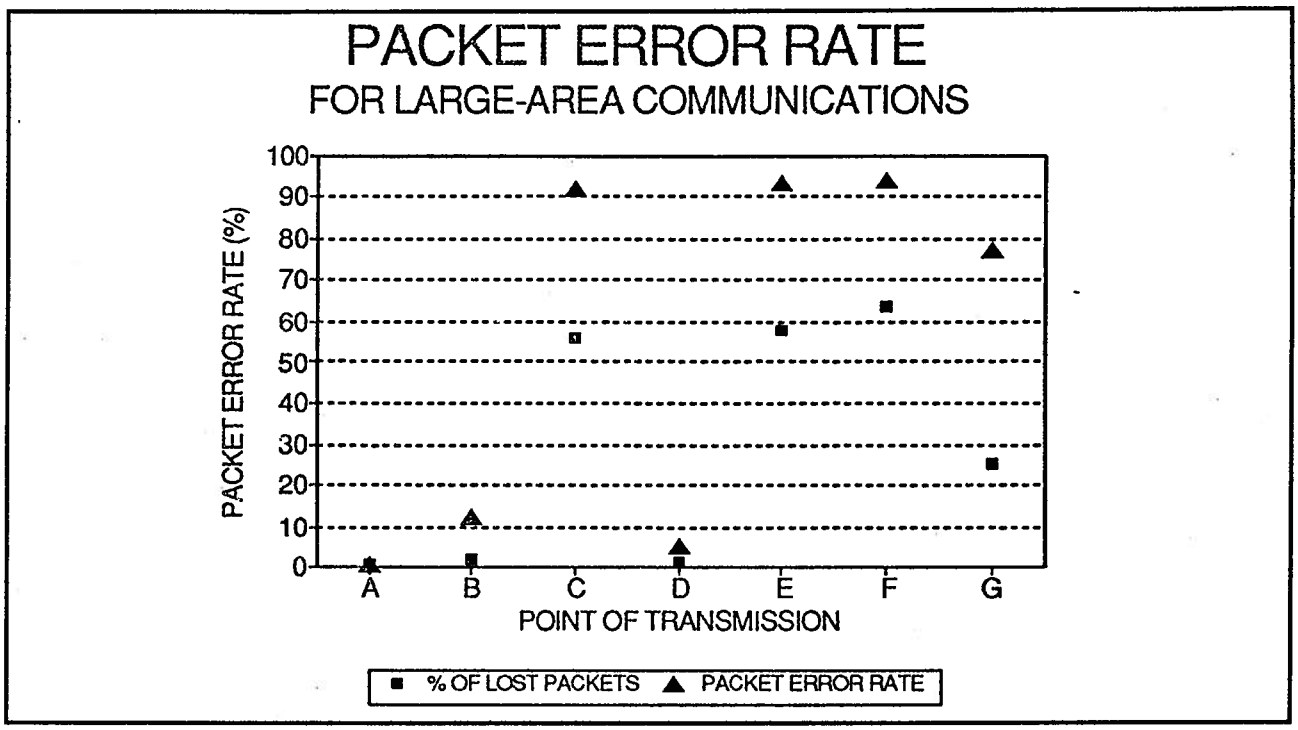


Figure 8.16: Packet error/loss rate for long-distance communications using the powerline modem.

with a BER of 10^{-5} or less, the packet error rate is typically below 15%. But, if the link's BER is above 10^{-3}, the packet error rate may exceeds 90%, which is highly unacceptable. However, forward error correction can substantially reduce this packet error rate [63]. As well, further reduction may be obtained by using novel data link protocols [67].

9. CONCLUSIONS AND DISCUSSIONS

9.1 Conclusions

This dissertation documents the research work which involves the design, implementation, analysis, and testing of an all-digital VLSI MSK modem chip with novel synchronization capability. On-chip functions include: MSK modulation with a centre carrier frequency to bit rate ratio of 5.75; semi-coherent MSK demodulation over a one-bit observation interval; and carrier detection. Fabricated with 1.2 μm CMOS technology, the chip is capable of MSK signalling at 0.19 Mbps maximum.

A standard-cell-based design (Chapter 6), the modem chip contains approximately 8500 transistors, and has a total of 36 pins, including 5 pairs of power/ground pins and 8 test pins for internal probing. In addition, to augment testability, a loopback self-test circuit is built into the chip. Design specifications of the chip are given in Chapter 5, and circuit schematics are described in Chapter 6.

Modulation is performed with a simple but reliable data-controlled digital square wave synthesizer without using any on-chip RAM (Chapter 3). A very high level of output phase stability is achieved.

The on-chip demodulator is implemented as a discrete-time correlation-receiver, with bit decision based on a one-bit observation interval. The theoretical performance of this demodulator in AWGN, as analyzed in Chapter 3, is about 2 dB poorer than that of a continuous-time realization, which is reviewed in Chapter 2. Also, the demodulator's susceptibility to imperfect carrier and bit synchronization is also formulated in Chapter 3.

A novel digital phase-locked loop (DPLL) is designed for suppressed carrier recovery. Unlike other Nth-order DPLLs, this DPLL obviates the need of any external zonal filter. This merit is largely owing to a proprietary polarity-based phase detection algorithm. Bit synchronization is carried out with another innovative DPLL which features a maximum-seeking phase detection technique. The phase error performance of these newly developed carrier and bit synchronizing structures are analyzed using Markov theory in Chapter 4.

To demonstrate its operation, the modem chip is applied to facilitate data communications

over intrabuilding powerlines at 19.2 kbps using 105.6 kHz and 115.2 kHz carriers. In addition to the modem chip, the resulting compact MSK powerline modem unit includes a DTE interface circuit and a powerline interface circuit. The former, which is mixed analog-digital, provides RS232 signal conditioning and coordinates the synchronous serial transfer of data between the modem and host, while the latter, which is all-analog, injects and extracts carriers to and from the powerlines.

After fabrication, the modem chip is functionally verified by means of a BIST test, an external loopback self-test, and an inter-chip data transfer test (Chapter 7). The performance, including bit error rate (BER), block error rate, and packet error rate, of the powerline modem unit is also evaluated. Its BER performance in AWGN is found to be about 2 dB poorer than theoretical prediction. Degradation is caused by hardware limitations, especially imperfect carrier and bit synchronization. When used for data transmission over actual intrabuilding powerlines, the modem achieves a BER in the range of 10^{-2} to 10^{-7} or less. In general, transmission on in-phase channels is more reliable than on cross-phase channels. For large area communication (i.e. >100 ft), modem performance is fairly independent of channel length.

In summary, an versatile all-digital VLSI MSK modem chip with novel synchronization means has been successfully designed and implemented.

9.2 Discussions

In the following discussion, the technological limit and baud rate selectivity of the all-digital MSK modem architecture are explored, the shortcomings of the design are identified, and some possible improvements as well as further investigations are suggested.

9.2.1 Technological Limit

In theory, the principle of the all-digital MSK modulation-demodulation technique introduced in this thesis can be applied to the implementation of any other FSK-like systems. In practice, feasibility depends on whether the required system clock speed (f_s) in the modem is within the limit of the selected digital technology. Clock speed f_s is dictated by the centre frequency (f_c) and bit rate (R) of the modem, as specified in equation <5.2>. Basically, f_s has to be high enough to resolve the closely spaced mark and space carrier frequencies. For example,

in the case of 19.2 kbps MSK signalling over powerline network using carrier frequencies of 105.6 kHz and 115.2 kHz, the digital modem only has to operate at 5.0688 MHz, which is well below the 100 MHz limit of current CMOS technology [50].

With the assumption of a center carrier frequency to bit rate ratio α of 5.75 and state-of-the-art CMOS implementation, the real-time digital modem processing technique developed in this project can be used to implement any MSK system whose centre frequency and bit rate are below 2.2 MHz and 0.38 Mbps, respectively. In the limit of α = 1.25, the upper bounds reach 10.4 MHz and 8.3 Mbps. Of course, the faster the chosen technology (e.g. ECL, GaAs), the higher the upper bounds.

9.2.2 Baud Rate Selectivity

In the design, the modem's centre carrier frequency to bit rate ratio α is internally fixed at 5.75. However, especially when channel condition is highly unpredictable, it is desirable to step down the baud rate in multiples of 2 while keeping f_0 and f_1 fixed (i.e. lower the bit rate by increasing the modulation index). For example, one way to improve the packet error performance of the powerline modem is by reducing the transmission rate [10]. With the present modem architecture, this kind of baud rate selectivity can easily be accommodated. Only three modifications are needed. First, add a selectable divide-by-1,2,4,8 circuit to control the transmit clock frequency. Second, provide the same to adjust the receive clock frequency. Third, increase the bit length of the digital integrate and dump's and the decision comparators to accommodate the increase in the number of subbit samples resulting from the rate reduction.

Actually, a second version of the MSK modem chip with the above modifications has been fabricated and functionally tested. Its baud rate is controlled via two new input pins. When driven at 5.0688 MHz, the chip can transmit at 19.2, 9.6, 4.8, or 2.4 Mbps. Performance evaluation of this modem chip at those lower baud rates over powerline channels is encouraged.

9.2.3 Design Shortcomings and Remedies

While the modem chip presented here has the merits of simplicity, reliability, and low space and power requirement, it has a few shortcomings. These are identified below in order of increasing importance.

1. Modem performance depends very much on the accuracy and precision of the system clock. Currently, crystal oscillators of very high quality (+/- 0.01% accuracy) are readily available. Consequently, this shortcoming is not a real threat.
2. The duty cycle of the digitized MSK signal at the receiver must be maintained to be as close to 50/50 as possible. Otherwise, significant BER performance degradation will be incurred as a result of two ramifications. First, by design, the locally generated carrier waveform always has a 50/50 duty cycle. When the duty cycle of the digitized input is not symmetrical, perfect correlation between the input and local carrier will not be possible, and this will give rise to systematic error the effect of which is similar to that of carrier phase error. Second, the zero-crossing-based phase detection algorithm employed for suppressed carrier recovery is sensitive to the duty cycle of the digitized input. Any duty cycle distortion will increase the probability of phase detection error, thus reducing carrier synchronization accuracy.
3. Due to the relatively slow acquisition behaviour of the newly designed bit synchronizer, a relatively long preamble is needed for modem synchronization purpose. For example, a preamble of at least 256 bits long is recommended for the MSK modem chip. The obvious remedy is to speed up the lock acquisition time of the bit synchronizer. This speed increase can be achieved in two ways: a) by increasing the phase update frequency, b) by increasing the step size of phase correction. However, both of these modifications will worsen the steady-state performance of the synchronizer. In light of this trade-off, a better strategy is to enhance the synchronizer's controllability such that two modes of operation are available: in the acquisition mode, a higher clock update frequency and/or larger phase correction step size are selected; in the tracking mode, these parameters are reduced to ensure a reasonably small steady-state bit timing error.

9.2.4 Other Improvements and Further Investigations

The modem chip designed in this thesis performs modulation, demodulation, and carrier detection. An increased level of system integration can be attained by adding to the chip some other digitally implemented functions involved in the physical layer of a data communication system. These functions include: a) RS232 handshaking, b) preamble generation/removal, c) data

scrambling/descrambling, d) FEC coding/decoding, and e) bit interleaving/deinterleaving.

From a theoretical standpoint, it is interesting to systematically study the effects of signal quantization and sampling frequency on the BER performance of the all-digital demodulator. Along with imperfect carrier and bit synchronization, these are the major sources of errors leading to significant performance degradation.

The carrier synchronizer and bit synchronizer on the modem chip are designed in a somewhat ad-hoc manner. Their performance depends on a few factors, including phase update frequency, phase correction step size, and loop filtering algorithm. A further detailed investigation of the effects of these factors on synchronizer performance is highly recommended.

Finally, attempt should be made to apply and test the MSK modem chip in other transmission environments.

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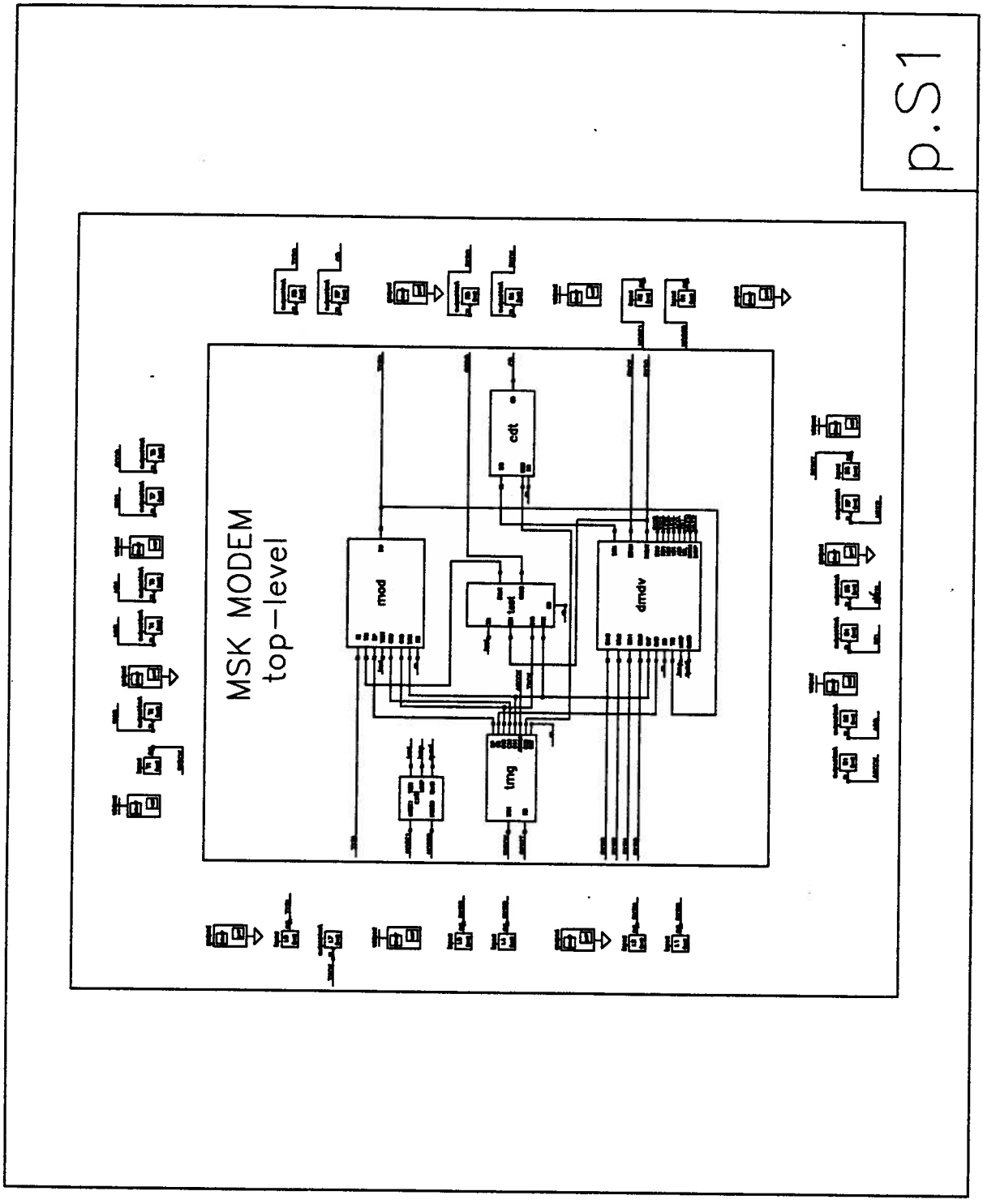
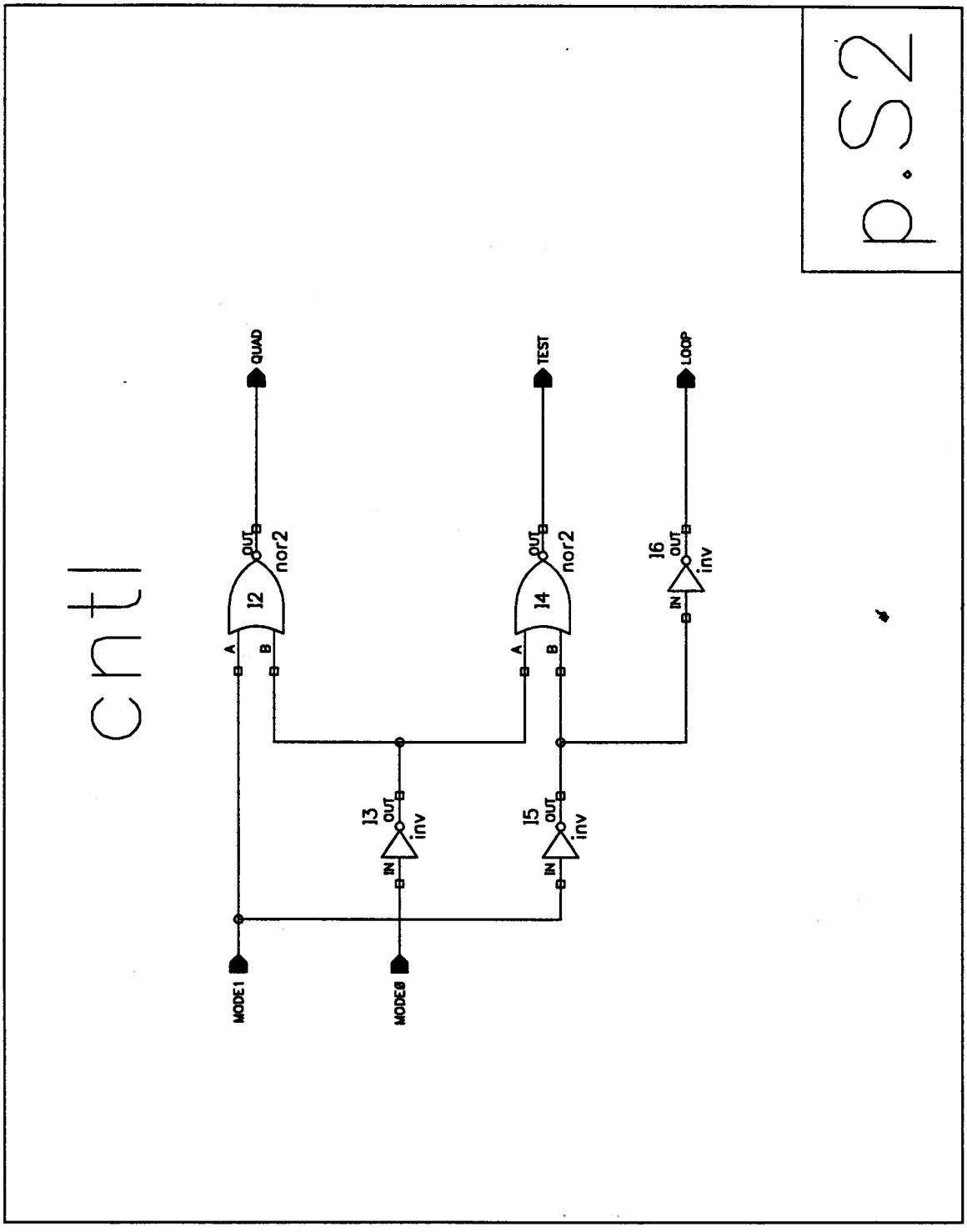
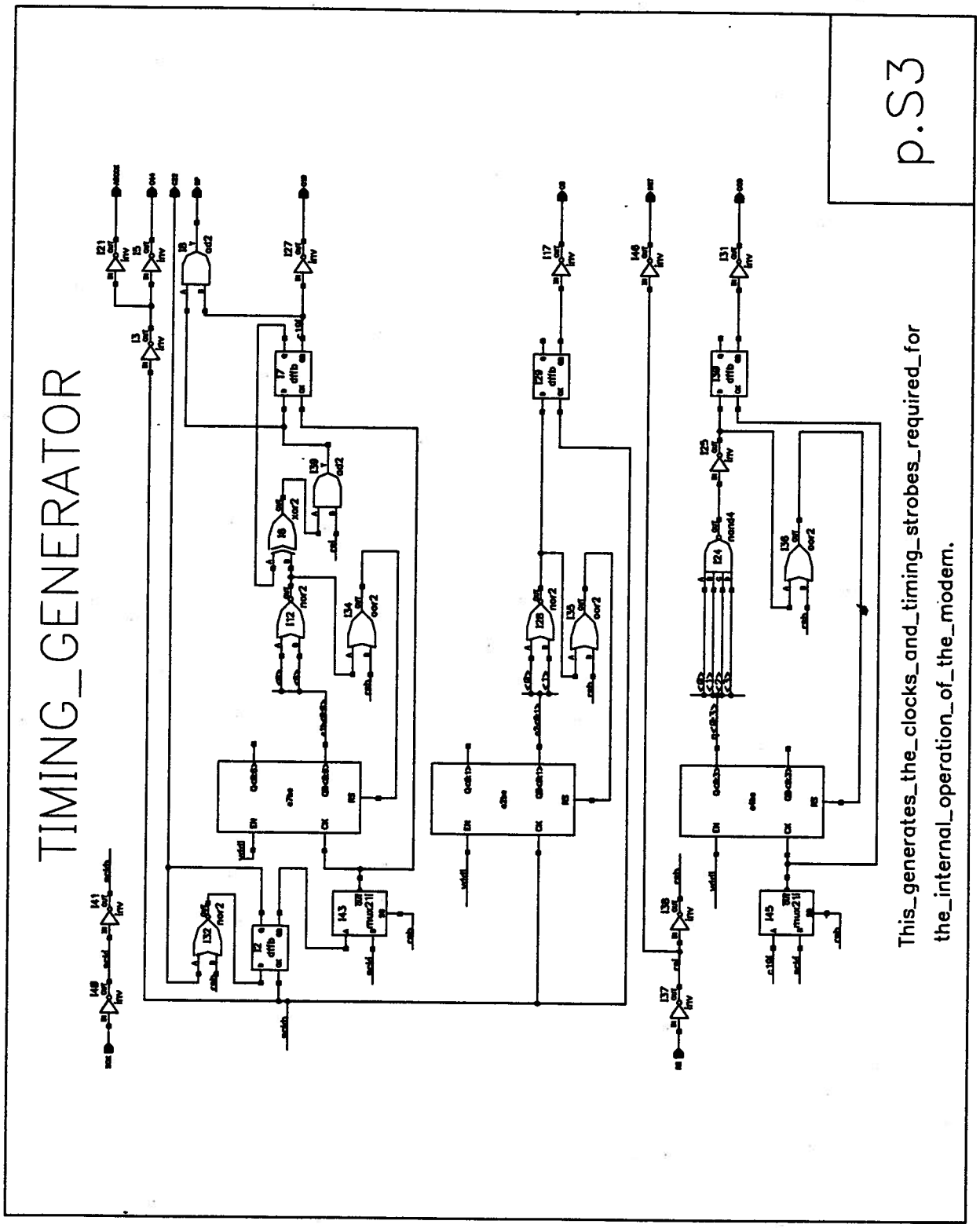
APPENDIX: SCHEMATICS OF MODEM CHIP

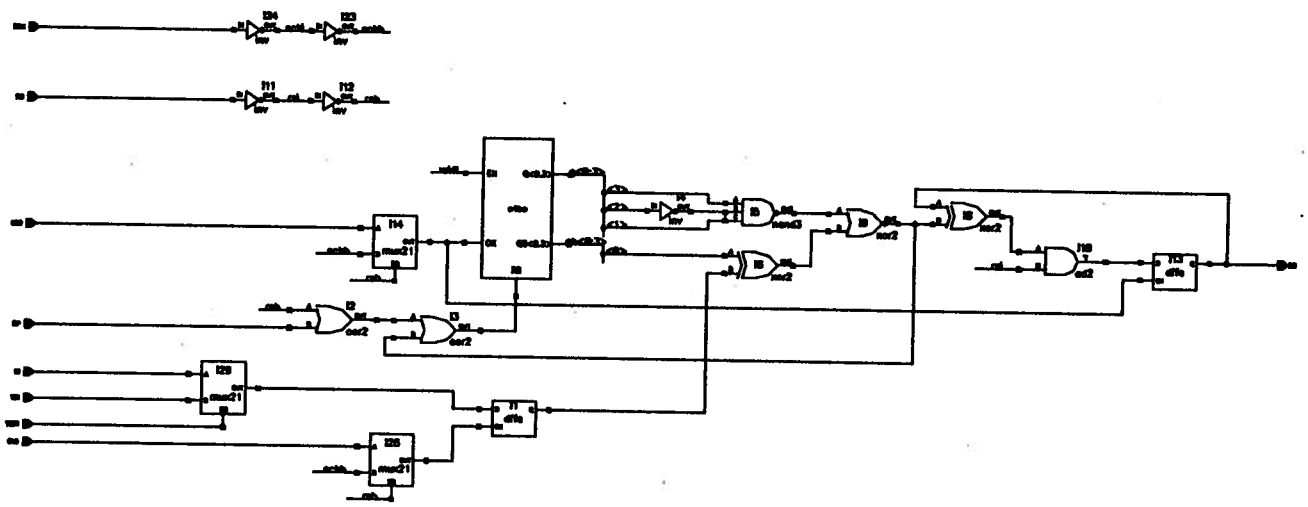
Sheet 1: Top-level chip architecture.
Sheet 2: Modem control logic.
Sheet 3: Timing generator.
Sheet 4: MSK modulator.
Sheet 5: MSK demodulator.
Sheet 6: Carrier synchronizer -- space frequency.
Sheet 7: Zero-crossing phase detector.
Sheet 8: 8-bit resettable register.
Sheet 9: 8-bit full adder.
Sheet 10: Averaging loop filter.
Sheet 11: Numerically controlled oscillator -- space frequency.
Sheet 12: Divide-by-48 clock divider.
Sheet 13: Carrier synchronizer -- mark frequency.
Sheet 14: Numerically controlled oscillator -- mark frequency.
Sheet 15: Bit synchronizer.
Sheet 16: Early/late phase detector.
Sheet 17: Absolute value converter.
Sheet 18: Majority loop filter.
Sheet 19: Numerically controlled oscillator -- bit clock.
Sheet 20: Divide-by-12 clock divider.
Sheet 21: Carrier detector.
Sheet 22: BIST controller.


p.S1
MSK MODEM
top-level
mod
dmdv
cdt
lmg


p.S2
cntl
QUAD
TEST
LOOP
12
nor2
14
nor2
16
inv
13
inv
15
inv
OUT
A
B
IN
MODE1
MODE0

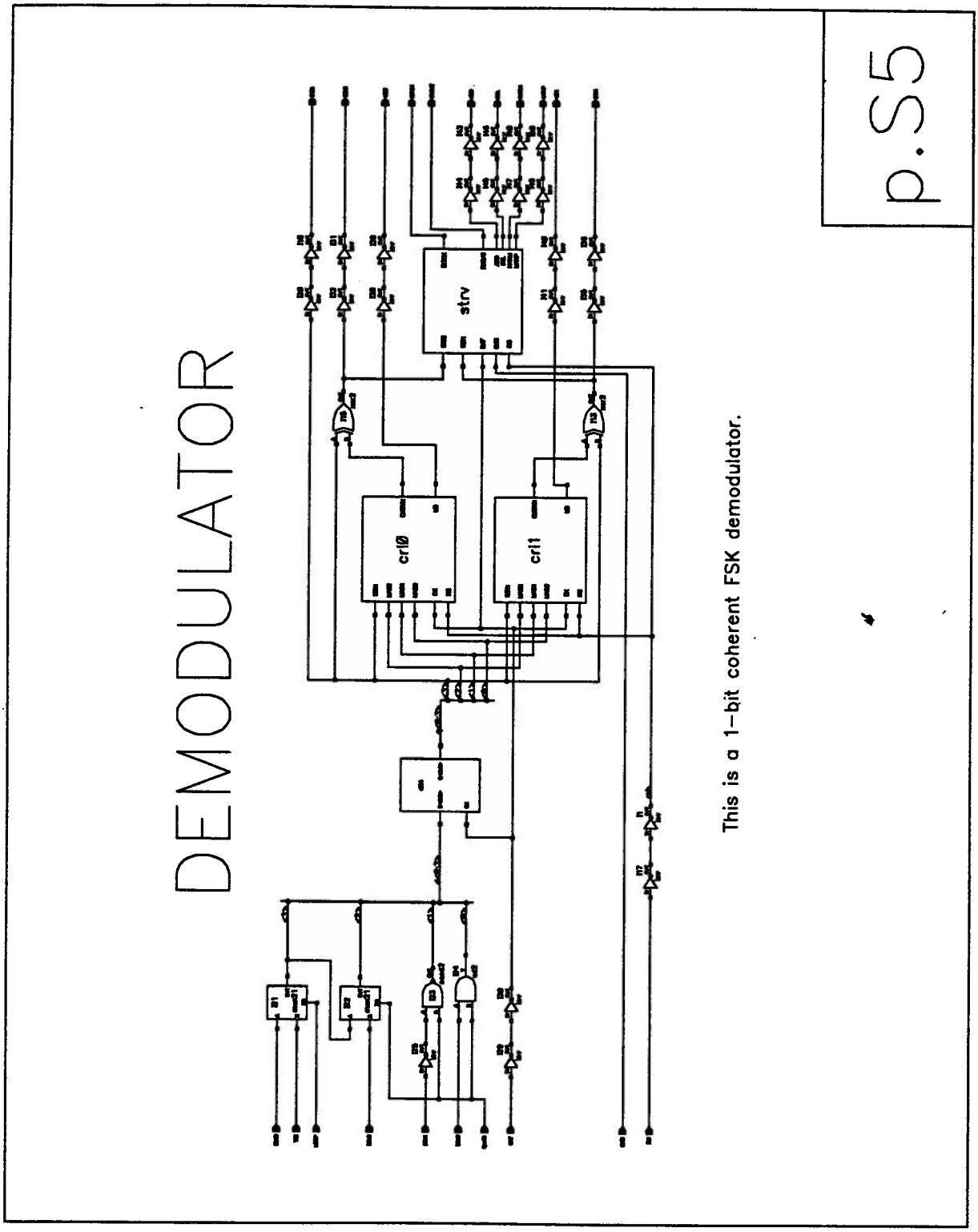

TIMING_GENERATOR
p.S3
This_generates_the_clocks_and_timing_strobes_required_for
the_internal_operation_of_the_modem.

MODULATOR

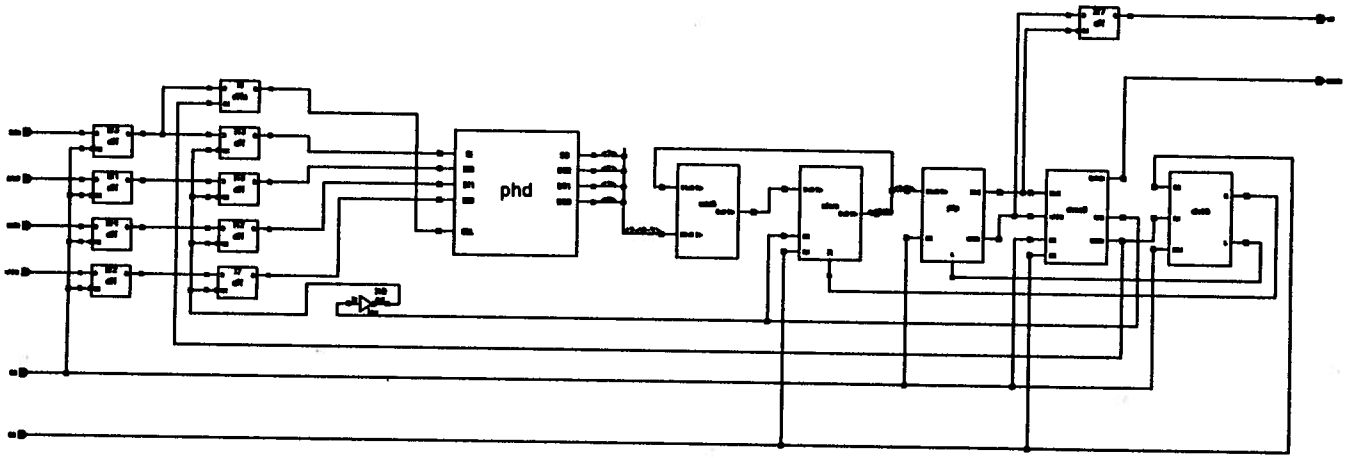


Minimum Shift Keying (MSK) modulation;
square wave output;
space: clock frequency / 48; mark: clock frequency /44
bit rate = clock frequency / 264

p.S4

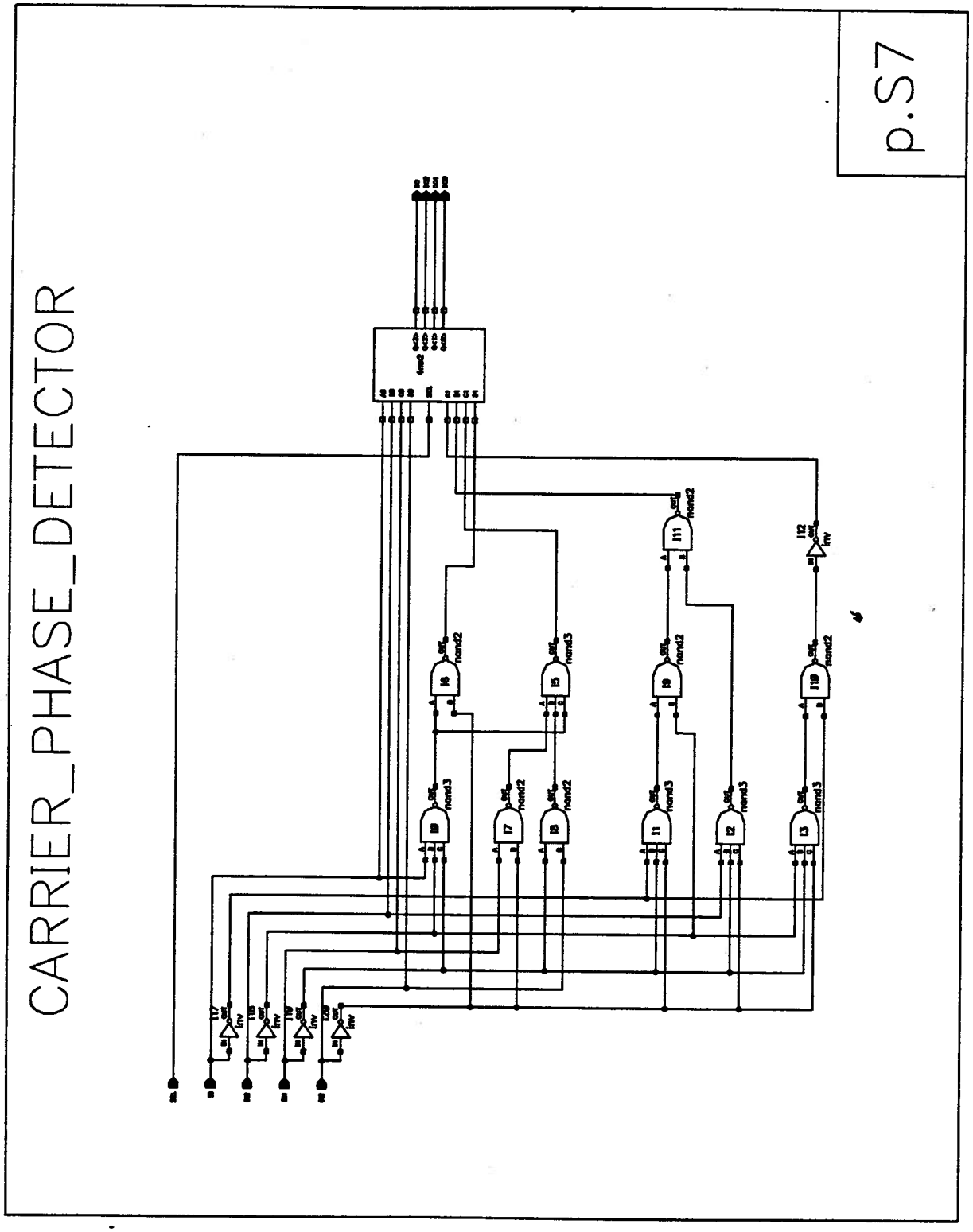

DEMODULATOR
P.S5
strv
cr10
cr11
This is a 1-bit coherent FSK demodulator.

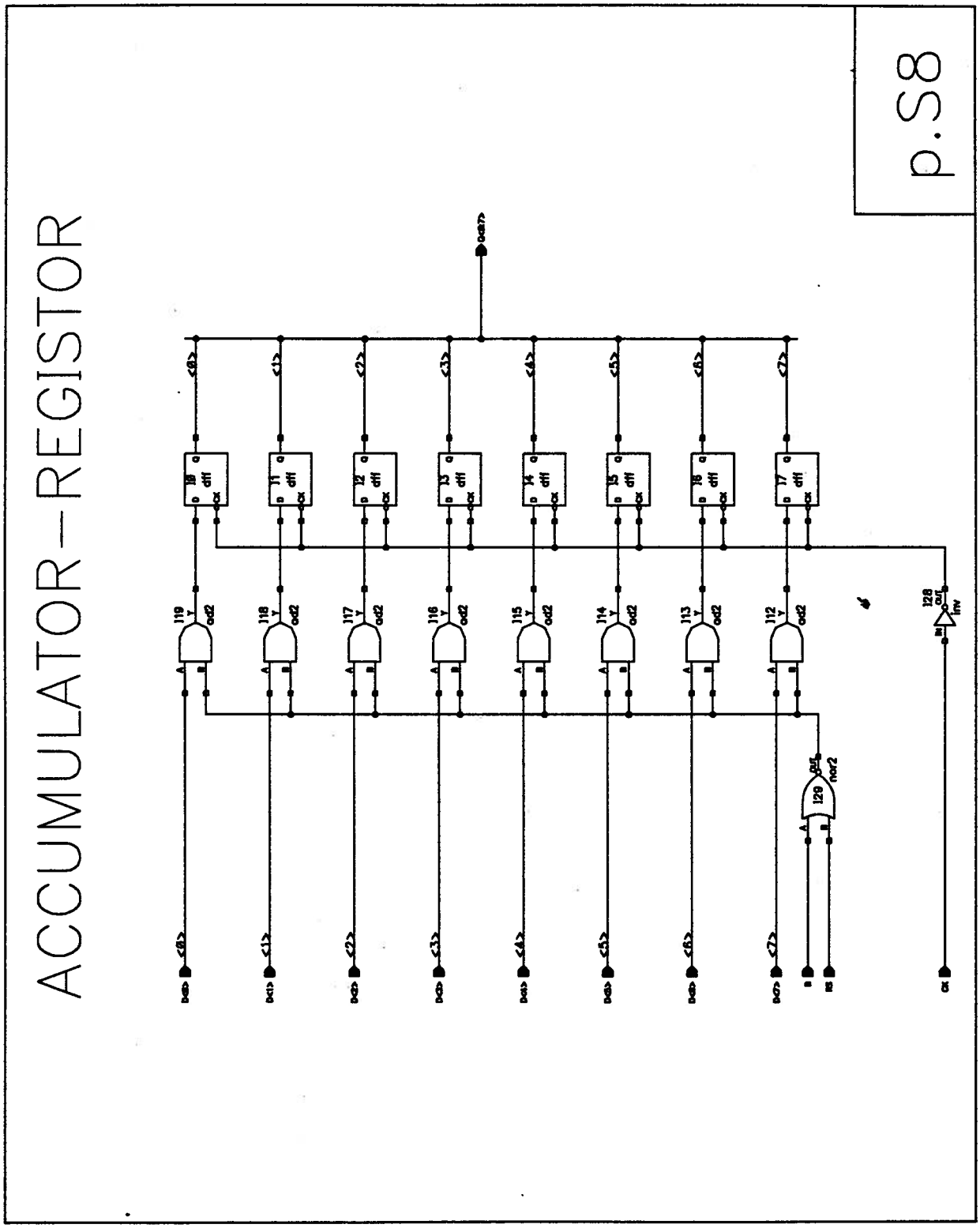
CARRIER-SYNC Ver.Ø

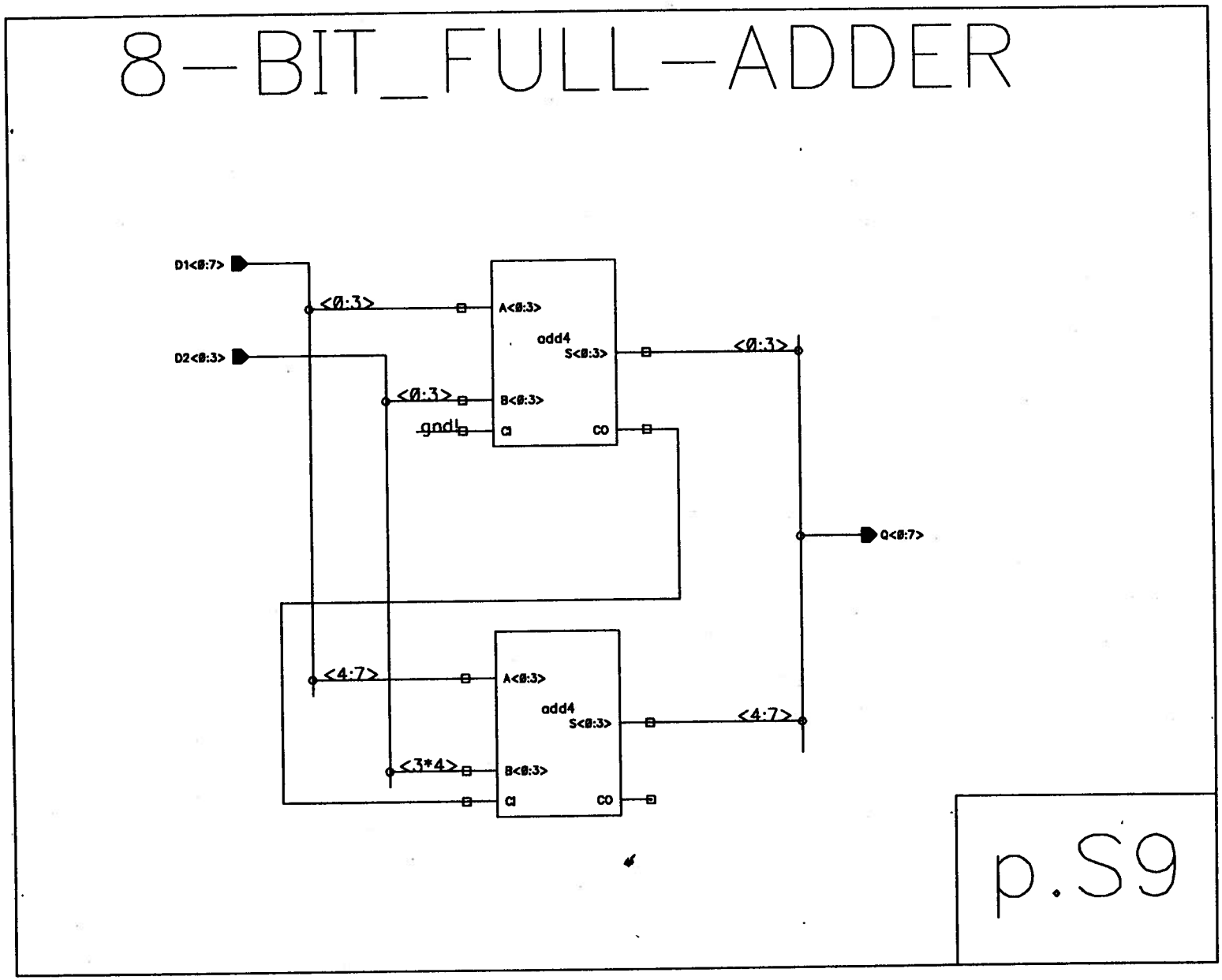


space frequency suppressed carrier synchronizer

p.S6


CARRIER_PHASE_DETECTOR
P.S7


ACCUMULATOR-REGISTOR
p.S8


8-BIT_FULL-ADDER
D1<0:7>
D2<0:3>
<0:3>
A<0:3>
add4
S<0:3>
<0:3>
<0:3>
B<0:3>
gnd
CI
CO
<0:3>
Q<0:7>
<4:7>
A<0:3>
add4
S<0:3>
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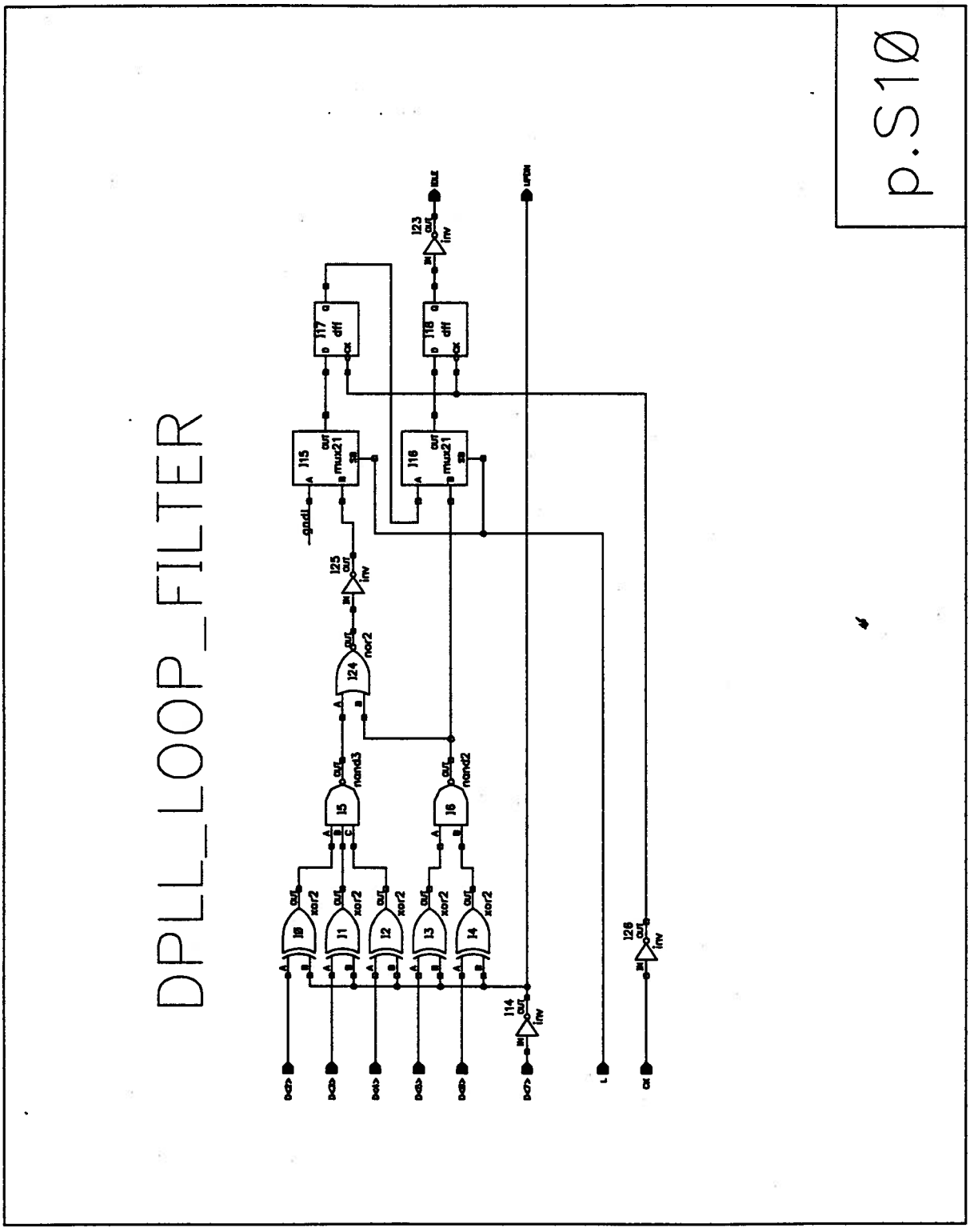
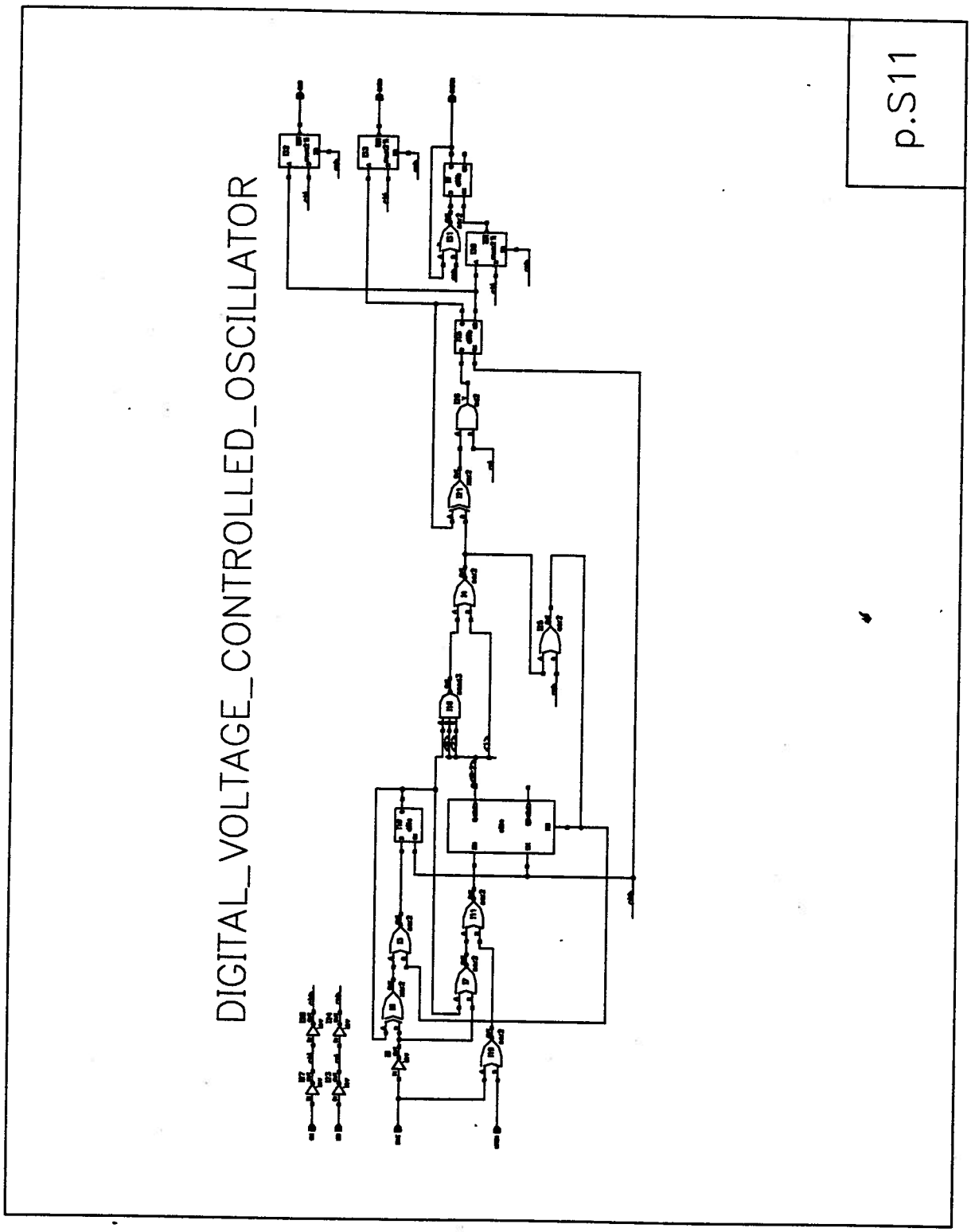
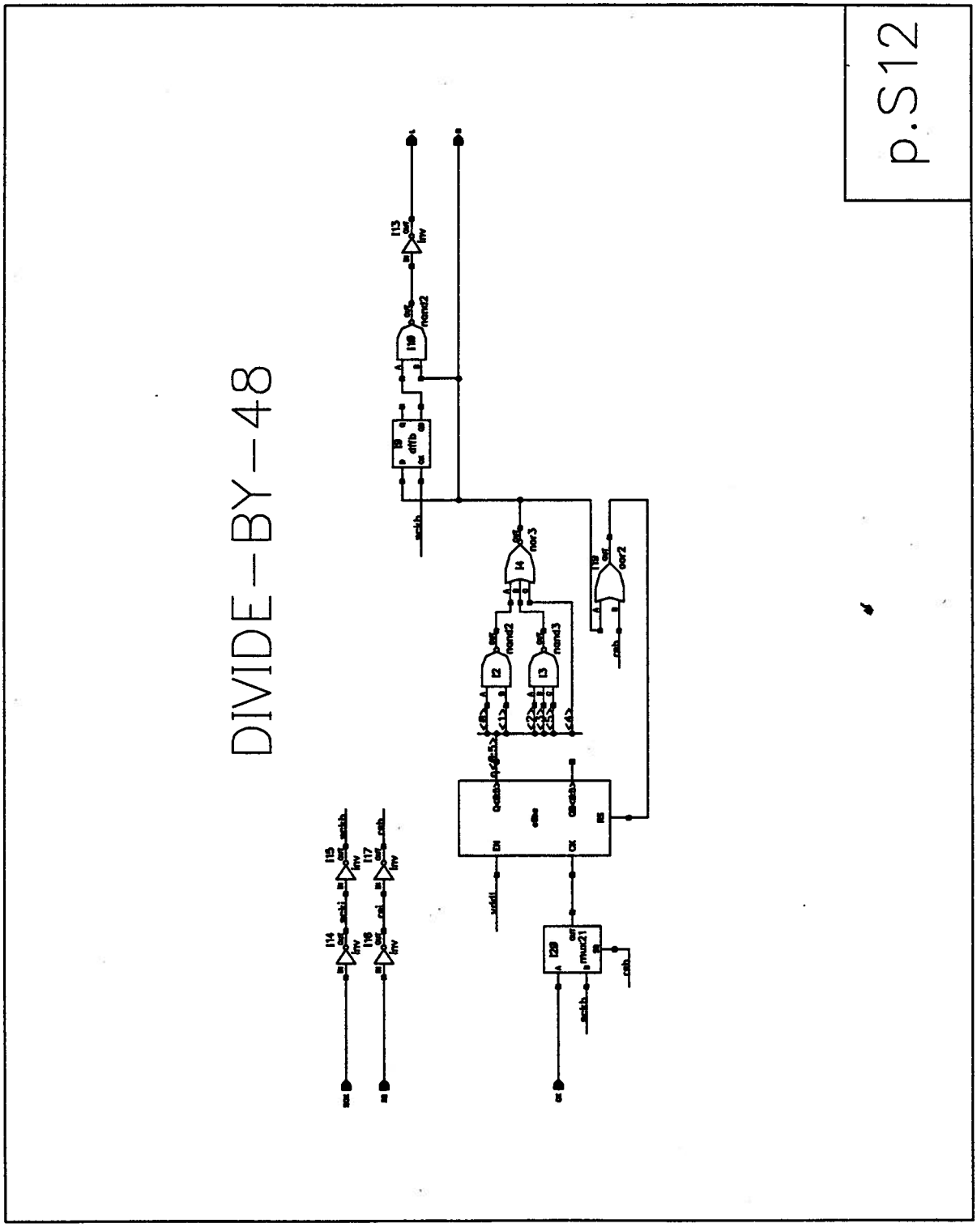
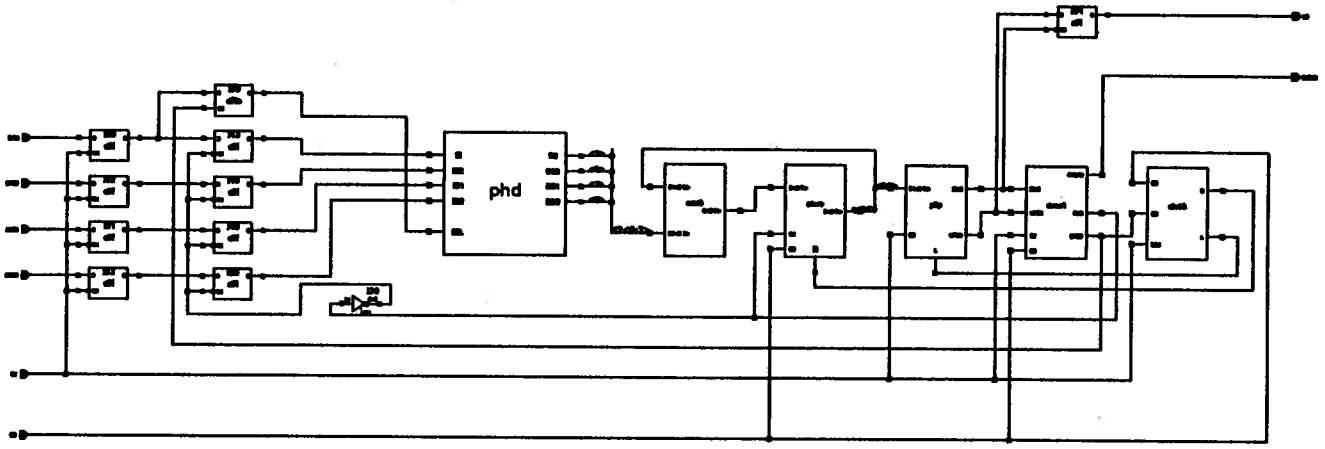
<3*4>
B<0:3>
CI
CO
p.S9


DPLL_LOOP_FILTER
p.S10


DIGITAL_VOLTAGE_CONTROLLED_OSCILLATOR
p.S11

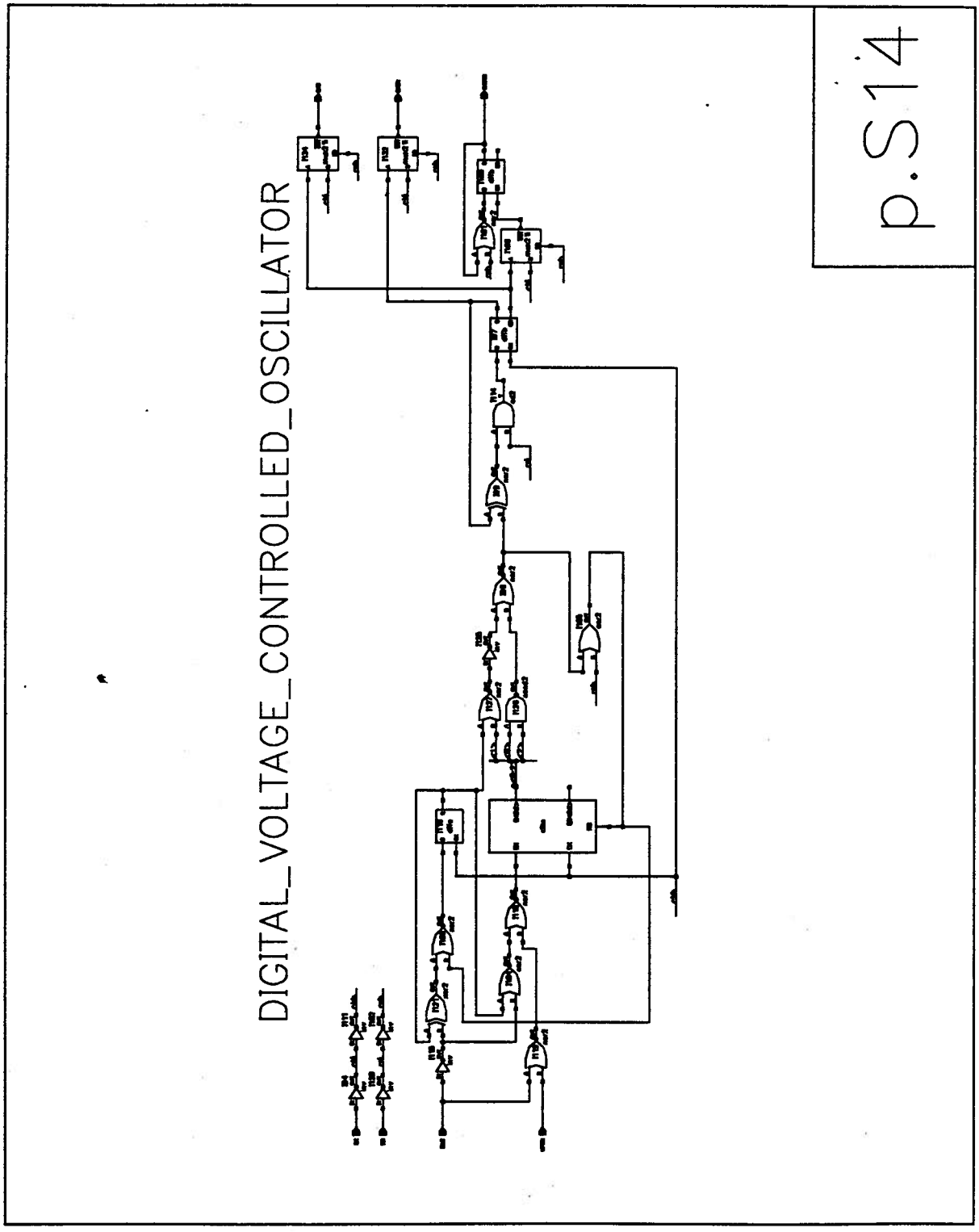

DIVIDE-BY-48
p.S12

CARRIER-SYNC Ver.1

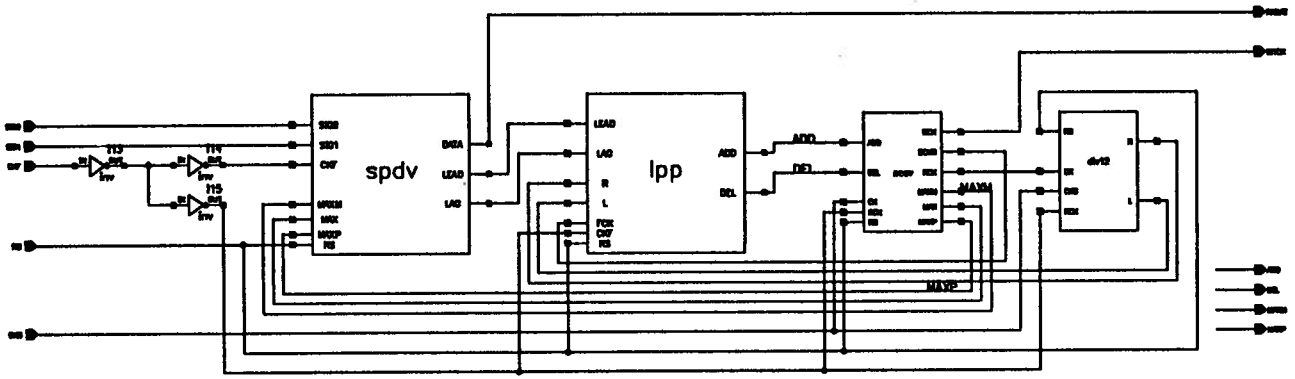


115.2kHz suppressed carrier synchronizer

p.S13

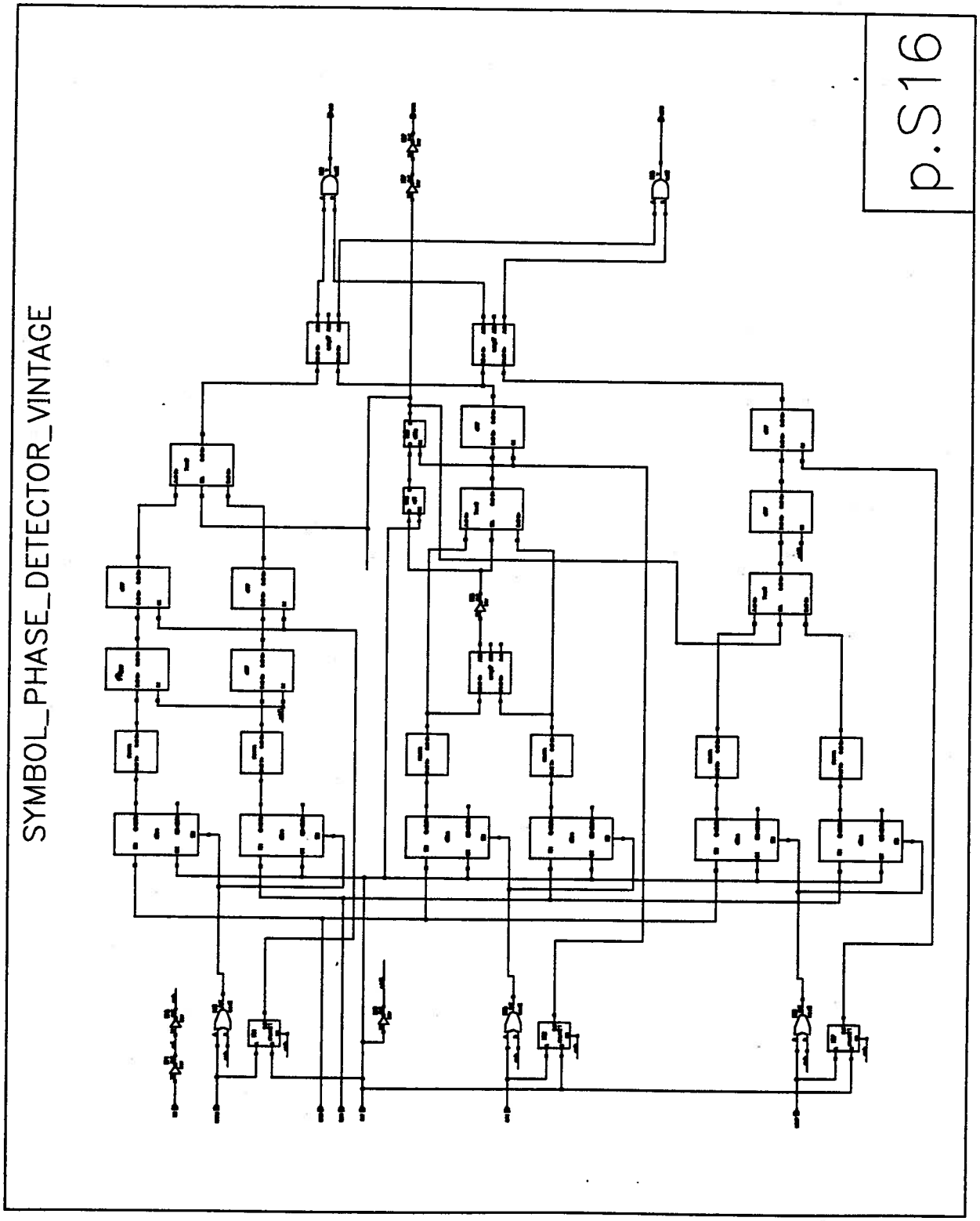

DIGITAL_VOLTAGE_CONTROLLED_OSCILLATOR
p.S14

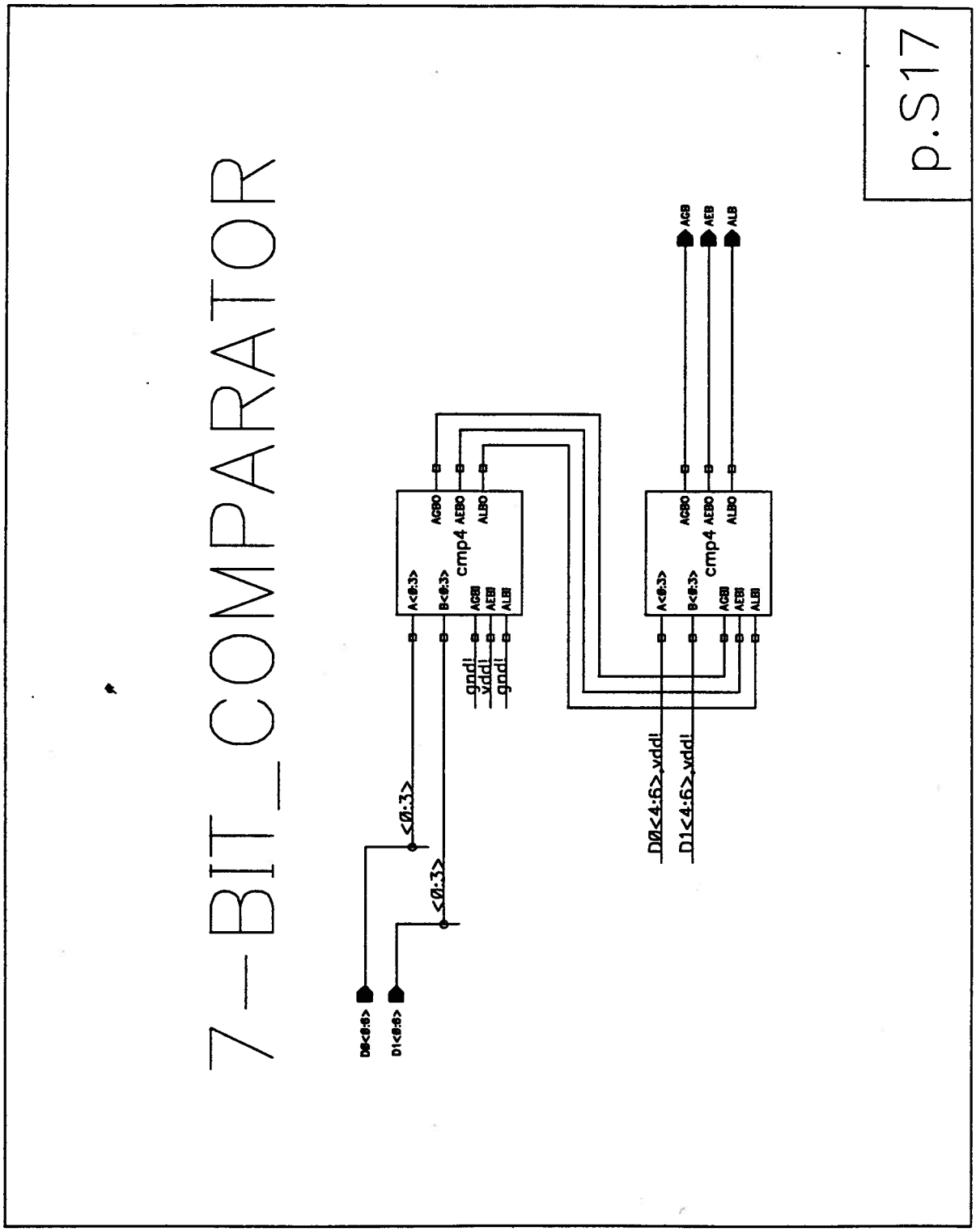
SYMBOL_TIMING_RECOVERY_VINTAGE

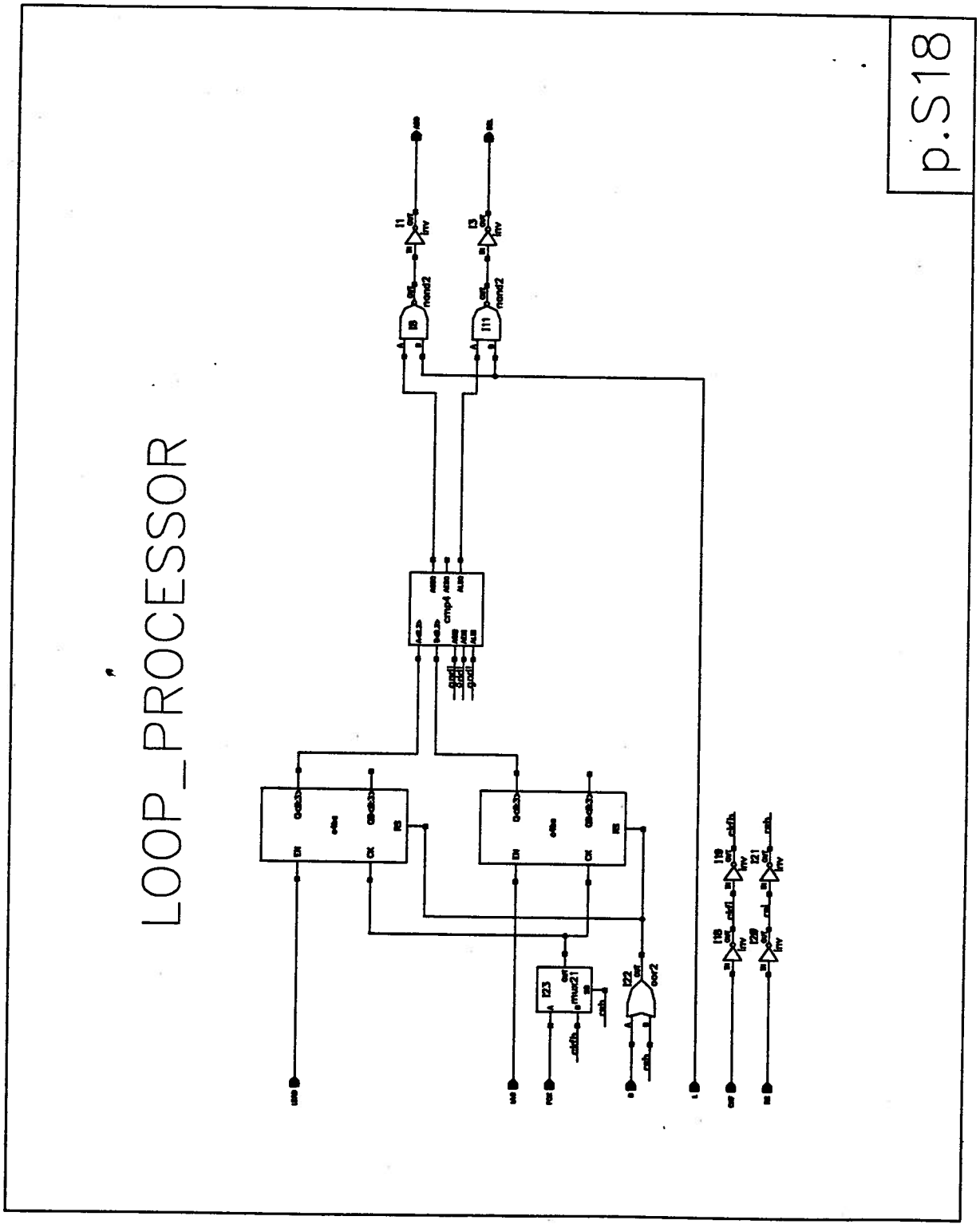


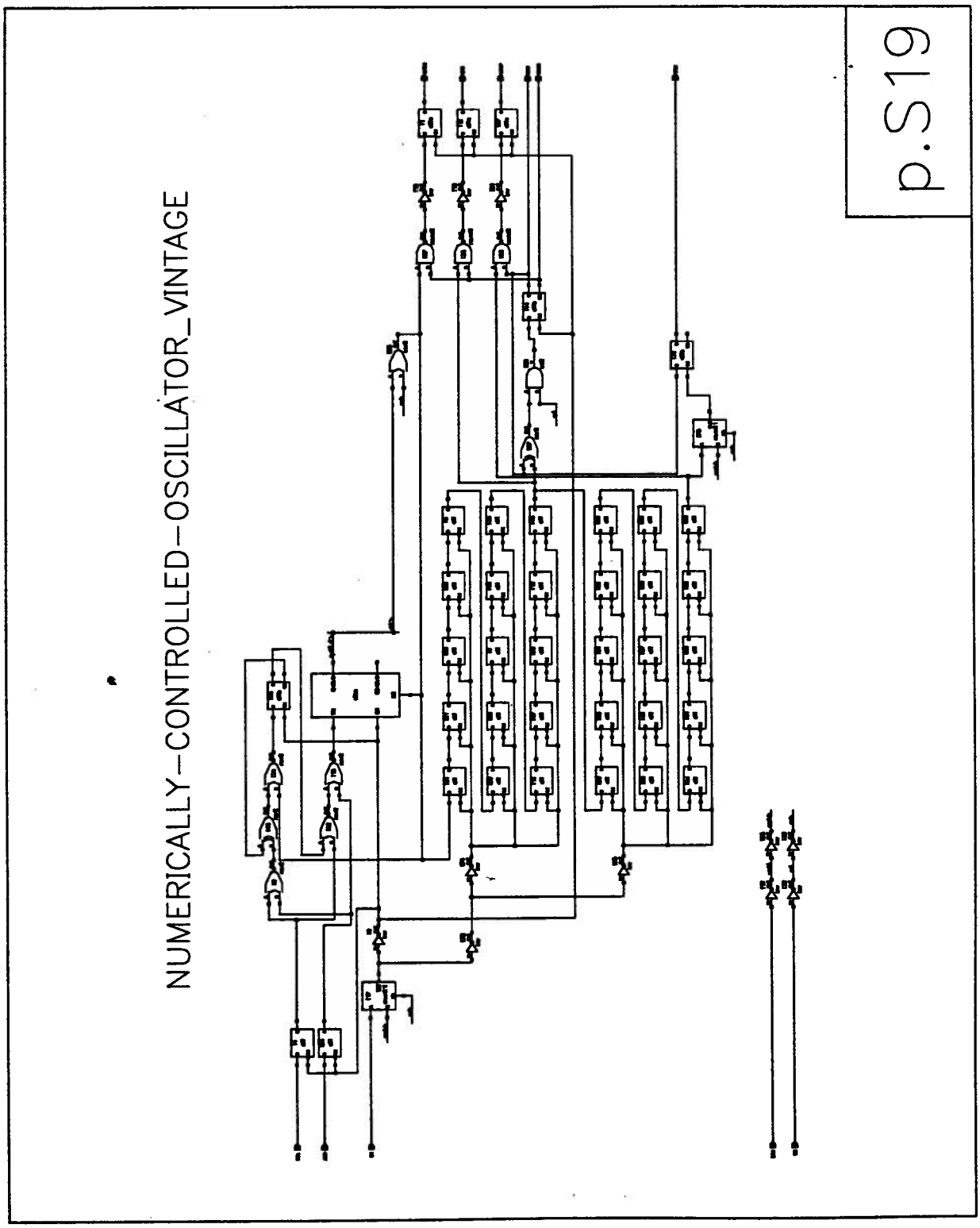
19.2kHz Bit SYnchronizer

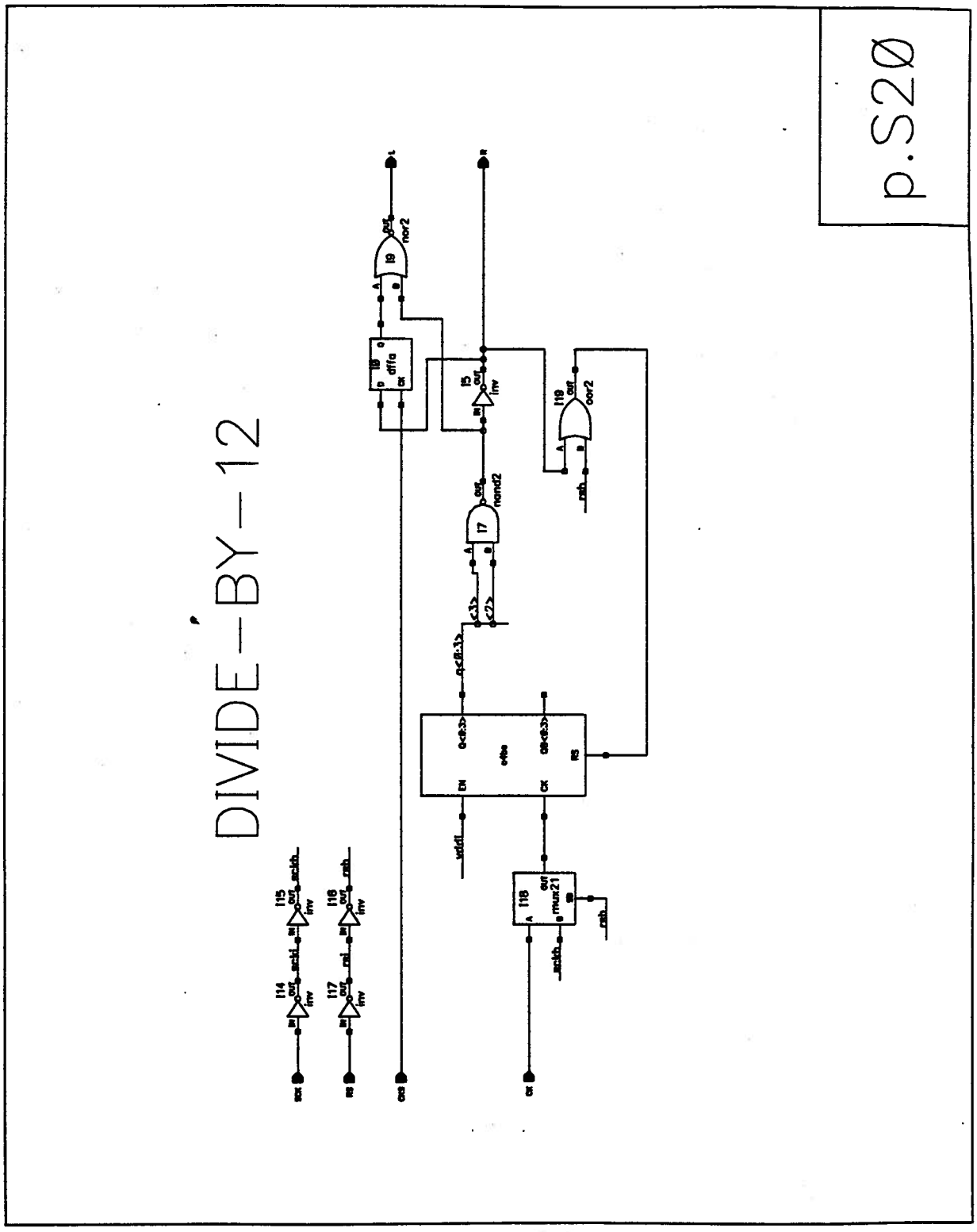
p.S15


SYMBOL_PHASE_DETECTOR_VINTAGE
p.S16

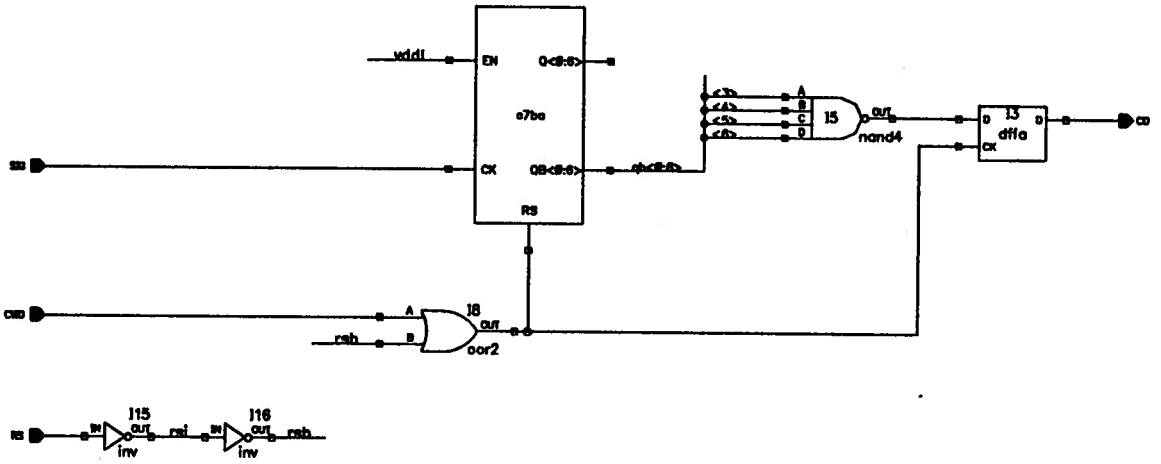

7 — BIT _ COMPARATOR
p.S17
cmp4
A<0:3>
B<0:3>
AGBO
AEBO
ALBO
AGBI
AEBI
ALBI
gnd!
vdd!
gnd!
<0:3>
<0:3>
D0<0:6>
D1<0:6>
D0<4:6>,vdd!
D1<4:6>,vdd!
AGB
AEB
ALB


p.S18
LOOP_PROCESSOR


NUMERICALLY-CONTROLLED-OSCILLATOR_VINTAGE
p.S19

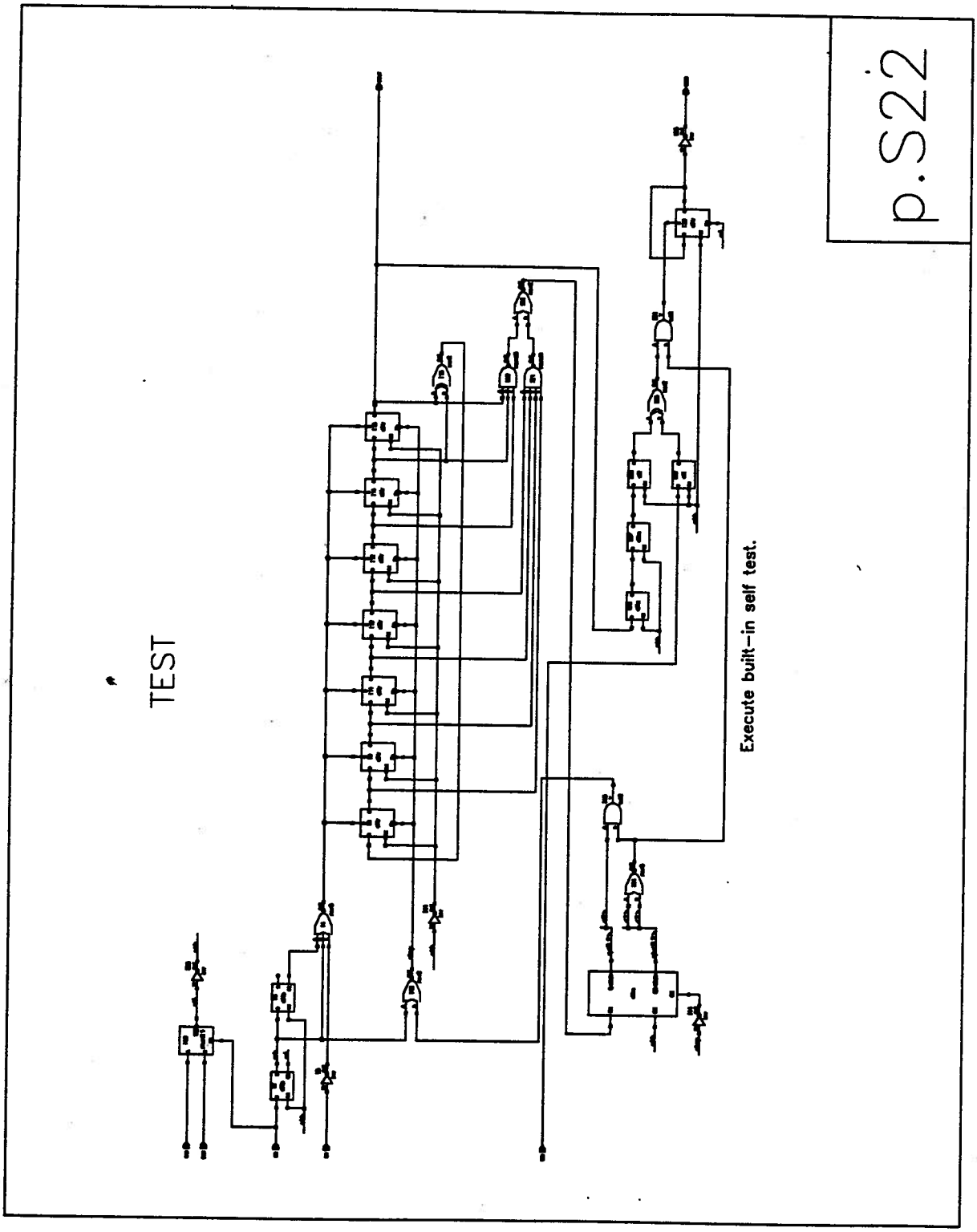

p.S20
DIVIDE-BY-12

CARRIER_DETECT



Monitor RX input for carrier presence.

p.S21


p.S22
TEST
Execute built-in self test.