Testing for Floating Gates Defects in CMOS Circuits

By

Sumbal Rafiq

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Department of _Electrical & Computer Engineering_

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Abstract

This thesis studies the detectability of MOS floating gate transistor faults considering classical Static Voltage, Dynamic Voltage and Static Current testing strategies. The behavior of the defect depends on two classes of parameters: the predictable and unpredictable parameters. A floating gate fault can induce abnormal logic values, additional delays, or increased power supply current. Consequently, classical test strategies can only detect floating gate faults for a given range of the unpredictable parameter. Here, a new test scheme is proposed, which allows a considerable current to flow in the faulty logic gate in stable state, making the circuit with a floating gate I_{DDQ} testable. It is shown that a combination of voltage and current testing can ensure complete detection of the floating gate defects, i.e., regardless of the unpredictable parameters. Analysis with increasing initial charge on the floating gate transistor shows how the detectability intervals become smaller for the voltage testing strategies and increase for the static current strategy.

Keywords: Floating gate testing, I_{DDQ} testing, gate opens, floating gate defect model.

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Chapter 1

Introduction

1.1 The Need for Testing

Very Large Scale Integration (VLSI) has enabled us to implement very complex circuits on a single chip. Complementary Metal Oxide Semiconductor (CMOS) technology has played a dominant role in allowing this to happen. The advantages of VLSI circuits are obvious. However, they do pose a problem. The problem is how do we test VLSI chips to ensure that they function as they are supposed to. With chips containing million or more transistors, testing has become an increasing part of the time it takes from conception to marketing of a chip. The problem can only become severe in the future.

The yield of a particular IC is the number of good die divided by the total number of die per wafer [38]. Due to the complexity of the manufacturing process not all die on the wafer correctly operate. Small imperfections in starting material, processing steps, or in

photomasking may result in bridged connections or missing features. It is the aim of a test

procedure to determine which die are good and should be used in end systems.

Testing a die (chip) can occur:

- at the wafer level

- at the packaged-chip level

- at the board level

- at the system level

- in the field.

If the faults can be detected at the wafer level, the cost of manufacturing is kept the

lowest. In some circumstances, the cost to develop adequate tests at the wafer level,

mixed-signal requirements, or speed considerations may require that further testing be

done at the packaged-chip level or the board level. A component vendor can only test at

the wafer or chip level. Special systems, such as satellite-borne electronics, might be

tested exhaustively at the system level.

IC tests may fall into two main categories. The first set of tests verifies that the chip

performs its intended function; e.g., that it performs a digital filter function, acts as a

microprocessor, or communicates using a particular protocol. In other words, these tests

assert that all the gates in the chip, acting in concert, achieve a desired function. These

tests are usually used early in the design cycle to verify the functionality of the circuit.

These are called the functionality tests. They may be lumped into the verification activity.

The second set of tests verifies that every gate and the register in the chip functions correctly. These test are used after the chip is manufactured to verify that the silicon is intact. They are called manufacturing tests. In many cases these two set of tests may be one and the same, although the natural flow of design usually has a designer considering function before manufacturing concerns.

CMOS has been the dominant technology for the last few years and is expected to remain dominant for many years to come. However, CMOS poses many new challenges in the area of testing. Overcoming these challenges is essential to the well-being of the semiconductor industry [39].

1.2 What is Testing ?

Testing in the context of digital systems is defined to be the process by which a defect in the system can be exposed. The defect can occur at the time of manufacture or when the system is in the field. In Figure 1.1 a device under test (DUT) is shown to which test vectors are applied. The resulting response from the device is monitored. If the correct response is known then we can determine if the DUT has a defect or not by comparing the responses.

Test Vectors ———————▶ DUT ———————▶ Response
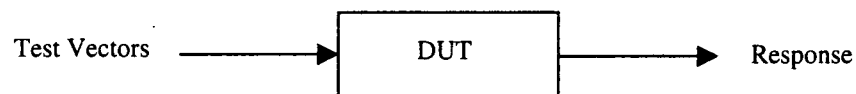
Figure 1.1   Testing of a device

Of course, it is assumed that one of the test vectors exposes the defect. For this assumption to be reasonable, the set of test vectors should include vectors for most, if not all, of the defects that are likely to occur.

1.3 Faults and Errors

A fault is an actual defect that occurs in the device. When a vector is applied to the faulty device which produces an incorrect response, an error is said to have occurred. For example, if a line in a chip breaks, a fault has occurred. When this fault is exposed at the circuit outputs by some input vector, an error results. In this case the error is manifested as an incorrect logic value at one or more of the circuit outputs [32]. However, monitoring the logic values is not the only way to determine if an error has occurred. There may be faults which cause the circuit to draw excessively large current when a particular vector is applied, but they may not result in an incorrect logic value at the outputs. In this case the error is manifested as a drastic change in the value of the current [10].

A fault which can change the logic value on a line in the circuit from logic 0 to logic 1 or vice versa is called a logical fault. On the other hand if the fault causes some parameters of the circuit to change, such as the current drawn by the circuit, then it is termed parametric [19].

A fault can also be categorized on the basis of duration for which it lasts. The three broad categories are (a) transient, (b) intermittent, and (c) permanent. A fault is called transient if it is only present for a small duration. A fault is intermittent if it appears regularly but is not present continuously. If a fault is present continuously, it is called permanent.

1.4 Fault Models

In order to deal with the existence of good and bad ICs it is necessary to propose a fault model, i.e., a model for how faults occur and their impact on circuits. If we try to derive test vectors for every possible physical failure in a VLSI chip, the problem would soon become unmanageable. To successfully tackle the problem, we represent the physical failures in a chip at a higher level with the help of a fault model.

Any one fault from the fault model may represent many physical failures. Thus, the use of fault models speeds up the test generation process. The fault models most commonly used for CMOS circuits are (a) Stuck-at fault model, and (b) Short-Circuit and Open-circuit fault model [39]. Another fault model which is increasingly being paid attention is the delay fault model [7].

1.4.1 Stuck-at Fault Model

The fault model which has found the most widespread use in the industry is the stuck-at fault model [2]. In this model it is assumed that the fault causes a line in the circuit to

behave as if it is permanently at logic 0 or logic 1. If the line is permanently at logic 0, it is said to be stuck-at 0 (s-a-0), otherwise if it is permanently at logic 1 it is said to be stuck-at 1 (s-a-1).

Consider the two-input static CMOS NAND gate in Figure 1.2.
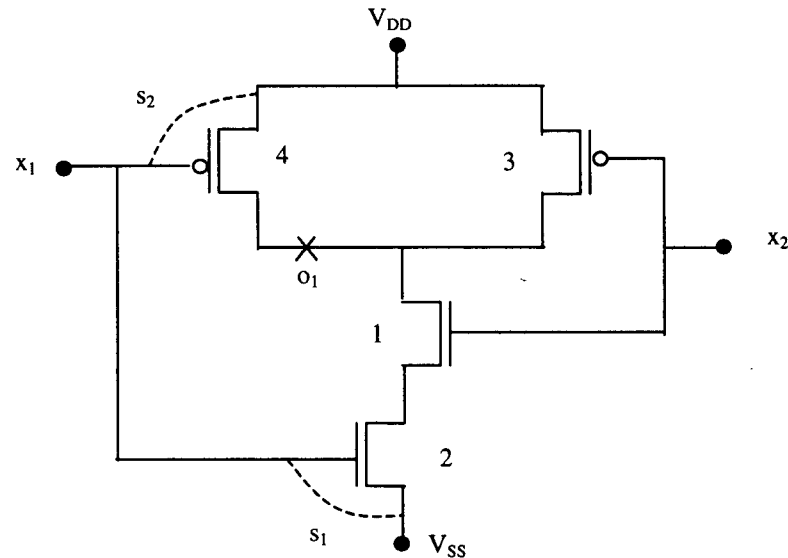
Figure 1.2   A two-input CMOS NAND gate

Let us first examine the short denoted s_1. This short forces the line fed by input x_2 to behave in a s-a-0 fashion. Similarly, the short denoted by s_2 forces the line fed by input x_1 to behave in a s-a-1 fashion. In Table 1.1 the fault-free output is denoted as f whereas the outputs in the presence of shorts s_1 and s_2 are denoted as f_1 and f_2 respectively. From this table one can see that the vectors $(x_1, x_2) = 11$ detects short s_1 and the vector $(x_1, x_2) = 01$ detects short s_2.

x_1	x_2	f	f_1	f_2
0	0	1	1	1
0	1	1	1	0
1	0	1	1	1
1	1	0	1	0

Table 1.1 Truth table for the NAND gate

1.4.2 Short-Circuit and Open Circuit Fault Models

Other fault models include "stuck-open" or "shorted" models [38, 39]. If a fault causes a transistor to conduct continuously, the transistor is said to be "stuck-on". When a transistor is rendered non-conducting by a fault, it is said to be "stuck-open". Consider the break denoted by o_1 in Figure 1.2. This break prevents transistor 4 from conducting. Thus, it results in a stuck-open fault in transistor 4. Suppose that the vectors shown in Table 1.1 are applied in the order shown. Even when o_1 is present the resultant output will still be the same as fault-free output f. This can be verified as follows. When 00 and 01 are applied, transistor 3 conducts, resulting in f = 1. When the third vector 10 is applied, neither the p-MOS network nor the n-MOS network can conduct. Therefore, the previous logic value is retained at the output node. Finally, when 11 is applied, the n-MOS network conducts and f becomes 0.

A stuck-open fault may cause even a combinational circuit to behave in a sequential fashion [20, 23]. Thus, in order to detect a stuck-open fault, a sequence of vectors is required. The reason the stuck-open fault in transistor 4 did not get detected above is that the proper sequence of vectors was not fed to the circuit. It usually requires a sequence of two vectors to detect a stuck-open fault. The first vector is called an initialization vector and the second vector is called the test vector. The sequence of these two vectors is referred to as the two-pattern test [16]. The two-pattern test for the stuck-open fault in transistor 4 is <11,10>. The vector 11 initializes the output node to 0. When 10 is applied next, the output node remains at 0 and the fault is detected.

It should be mentioned that the two-pattern tests should be applied at a rate higher than that associated with the leakage current time constants. Otherwise, a correct transition may be observed at the output even in the presence of the fault [23]. Opens such as o_1 in Fig. 1.2, do not make the transistor permanently non-conducting. Due to the leakage currents, the node f may eventually charge to logic 1. However, the more important point is that if the two-pattern test is applied rapidly, the open o_1 will still be detected. So it is not necessary to assume that the transistor is permanently non-conducting for the success of two-pattern testing.

1.4.3 Bridging Fault Model

A bridging fault is generally defined to be a short among two or more signal lines in the circuit [11, 32, 33]. Such a short could occur, for example, due to defective masking or etching, aluminum migration, breakdown of insulators, etc. A bridging fault can be broadly classified as either (a) feedback bridging fault, or (b) non-feedback bridging fault. If a bridging fault creates one or more feedback loops, it is referred to as a feedback bridging fault, otherwise it is referred to as a non-feedback bridging fault.

1.4.4 Delay Fault Model

Even if a circuit is free of structural defects, it may not propagate a signal in the time allowed. This gives rise to a delay fault [39]. The voltage on the faulty line could either be slow-to-rise (STR) or slow-to-fall (STF). Two types of delay fault models are generally used: (a) gate delay model, and (b) path delay model. The gate delay model models defects at the inputs or the outputs of a gate. On the other hand, the path delay model models those defects which cause cumulative propagation delays along a circuit path to exceed the specified value. Each model has its own advantages and disadvantages. The path delay model requires the enumeration of circuit paths from all primary inputs to all circuit outputs. This causes an explosion in the number of paths that have to be considered, thereby increasing the number of tests and the test generation time.

The gate delay model does not have this problem. However, it can not model delay defects which are not necessarily localized to single gates.

1.5 Test Strategies

With today's manufacturing technology, it is not possible to eliminate all defects and ensure that every manufactured unit is perfect. Instead, each manufactured unit must be tested so that defective parts are not shipped to the customer. Most companies adopt individual approaches since there is not yet general agreement on an optimal (low defect level) test strategy that can be quantified and accepted by both customer and supplier. Most companies use some but not all of the following three test strategies [6]:

1. Static Voltage Strategy (SV strategy)

2. Dynamic Voltage Strategy (DV strategy)

3. Static Current Strategy (SC strategy)

The decision to use some of these three strategies is usually done according to the classical cost / efficiency trade-off.

1.5.1   Static Voltage Strategy (SV Strategy)

The Static Voltage strategy (SV strategy) refers to any test using voltage sensing for verifying logic functionality regardless of clock frequency. SV tests provide boolean controllability (a measure of the ease of setting the node to a 1 or 0 state) and observability (the degree to which one can observe that node at the outputs of an integrated circuit) of the considered fault.

1.5.2   Dynamic Voltage Strategy (DV Strategy)

The Dynamic Voltage or Delay strategy (DV strategy) refers to any test using voltage sensing but taking into account the clock frequency. The DV technique works on a gate level description and uses two vector pairs to measure circuit propagation delays. The first vector (initialization vector) sets the logic output and the second one (state change vector) provides controllability and observability for the targeted path or gate.

1.5.3   Static Current Strategy (SC Strategy)

The Static Current Strategy (SC strategy) measures the quiescent V_{DD} power supply current of the IC. This relies on the fact that when a complementary CMOS logic gate is not switching, it draws no DC current (except for leakage) [1]. When a fault such as a short occurs, for some combination of input conditions a measurable DC I_{DD} will flow.

Testing consists of applying the normal vectors, allowing the signals to settle, and then measuring I_{DD}. To be effective any circuits that draw DC power such as pseudo-nMOS gates or analog circuits have to be disabled. Because many circuits now require SLEEP modes to reduce power, this may not be a substantial overhead [1, 10, 16].

Because current measuring is slow, the test must be run slower than normal, thus increasing test time. However, this technique gives a form of indirect massive observability at little circuit overhead. The SC test, therefore, just has to provide the boolean controllability of the considered fault because observability is inherently guaranteed.

1.6 Fault Coverage

A measure of goodness of a test program is the amount of fault coverage it achieves; that is, for the vectors applied, what percentage of the chip's internal nodes were checked. Conceptually, the way in which the stuck fault coverage is calculated is as follows. Each circuit node is taken in sequence and held to 0 (s-a-0), and the circuit is simulated, comparing the chip outputs with a known "good machine" – a circuit with nodes artificially set to 0 (or 1). When a discrepancy is detected between the "faulty machine" and the good machine, the fault is marked as detected and the simulation is stopped [38, 39]. This is repeated for setting the node to 1 (s-a-1). In turn, every node is thus stuck at 1 and 0, sequentially. The total number of nodes that, when set to 0 or 1, do result in the

detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage. This method of fault analysis is called sequential fault grading.

1.7 Thesis Motivation

The quality of a test set largely depends on the "realistic" characteristics of the fault model. It was found that a test with 100% fault coverage will only provide as little as 10% fault coverage if another fault model is used [5]. In the last decade, it became clear that the knowledge of the electrical and physical mechanisms that cause faults must be taken into account on establishing accurate fault models [32], while the traditional stuck-at fault models are not sufficient to model behavior of faults in MOS circuits [3,8,12,17,33].

The fault models with the insight into the physics of processing defects and mask layouts sometimes are referred to as Realistic Fault Models [34]. Currently, there are a few methods and systems available which can be used to analyze the realistic faults for a given layout. Most of the effort has been put into the study of shorts / bridging faults. However, it seems that the analysis of realistic opens attracts less attention. The importance of the opens should be recognized, however, by the following facts:

1. Although opens are not as frequent as bridges [28], the probability of the occurrence of opens can be large [8, 17, 19]. For instance, missing contacts causing opens are one of the most likely defect mechanisms.

2. The random defects cause opens more likely than bridges in one products than in other products [29, 30] or in one period of time than in rest of the time [2]. It is reported experimentally that chips passed single stuck-at (SSA), I_{DDQ} or even delay test pattern sets still not function correctly. One of the reasons is opens on the conducting paths [2, 31].

Furthermore, the type of defects and failure mechanisms in CMOS ICs are dependent on the design, layout, and process technology and therefore can vary not only from vendor to vendor but from wafer lot to wafer lot. Hence for one process, bridge defects may dominate while, for a different process, open circuits may prevail.

In general, the type of an open fault in terms of a transistor may be one of (a) floating gate, (b) open source, and (c) open drain. Many research works showed that the floating gate fault is the most complex and hard-to-detect fault in IC test [5, 7, 12]. Although single transistor stuck-on and stuck-open fault models have been introduced at the switch level, the models are still not sufficient to describe the floating gate behavior. In fact, as will be described later, the behavior of a transistor with floating gate transistor depends on the exact site of the occurrence of the open. It is not possible to model a floating gate

transistor without the information of the open site, since the same floating gate transistor may act completely different if the open sites are different. The floating gate acquires a voltage that depends on the coupling capacitances of the transistor device and on the surrounding circuitry [5, 14, 16]. Gate oxide trapped charges may play an important role in the floating gate transistor (FGT) as well [17].

The significance of the floating gate fault has been investigated by defect simulation by several workers. Shen *et al.* [19] used a procedure called Inductive Fault Analysis (IFA) to investigate the susceptibility of the layout of a logic cell to photolithography defects. In IFA, random defects are generated on the cell layout and their effect was automatically assessed. They found that 25 % of defects generated for an n-MOS logic cell produce floating gate faults.

Similar results have been obtained by Johnson [17], in defect simulations of CMOS cells. Photolithography defect simulations were performed on a selection of hand-crafted and semi-custom cells. Other forms of defects, such as incomplete contact etching were not included in their calculation. To maintain generality in their results, defect distributions from specific process lines were not used. A generally accepted distribution was used for the defect diameter [35], and equal distributions of extra and missing material resulting from photolithography defects were used in the simulations. In these simulations, a total of 16100 defects were scattered over three typical CMOS cells and the effects of the defects were analyzed. The defects produced 930 faults and 27% of these were floating

gates. The floating gate is clearly a significant form of fault that can arise from photolithography defects in CMOS circuits.

Hua *et al.* [8], performed the probability analysis for CMOS floating gate faults on ISCAS '85 benchmark layouts. The defect with size 5 micron was chosen to analyze the open faults and their critical areas. The results clearly showed that the probability of the occurrence of the floating gate fault is the highest one among the various open faults. The percentage of the floating gate faults in terms of the number of faults was 73 % on average, out of the total number of possible open faults. On the other hand, in terms of the critical area (defined as the area in which the center of a defect must fall to cause a fault), which is proportional to the probability of the occurrence of the fault, the percentage of the floating gate fault reached as high as 91 % out of the total number of possible open faults.

In addition to photolithography defects, poor contact or via processing is likely to be an increasing cause of floating gate faults. The use of stacked vias in submicron, three or more layer metal processes results in via and contact holes which are difficult to etch. This can result in high resistance or open circuit contacts and hence floating gate faults.

1.8 Scope of the Thesis

Recognizing the complexity and high probability of occurrence of the floating gate faults, this dissertation analyses the detectability of FGTs using the three conventional test strategies, viz.,

1. The Static Voltage strategy (SV strategy)

2. The Dynamic Voltage or Delay strategy (DV strategy)

3. The Static Current (I_{DDQ}) strategy (SC strategy)

It is shown that the behavior of the floating gate defect depends on two classes of parameters, i.e., the predictable and the unpredictable parameters. Predictable parameters include both technological information from the process and topological information from the layout [5]. The unpredictable parameters include the random information coming from the size, location, and nature of the fault. It is shown that the metal-poly capacitance C_{mp}, and the metal potential V_m, together with the unpredictable poly-bulk capacitance C_{pb} and Q_o, play an extremely important role in determining the final output voltage and the steady state current of a logic gate subject to a floating gate defect.

Chapter 2 is devoted to the analysis of the electrical behavior of a floating gate transistor. It is mentioned that the equivalent gate potential V_{gs} of the faulty transistor depends on its own drain to source voltage V_{ds}, the influence of an overlapping metal track V_m, and

different technological and topological parameters [5, 14, 16]. It is shown that the induced voltage on the defective transistor decreases for higher values of the poly-bulk capacitance C_{pb} and increases for the lower values of the same. A strong relationship between the crossing-metal potential V_m together with the corresponding metal-poly capacitance value C_{mp}, and the induced voltage on the gate is also presented in detail.

Using these relationships, Chapter 3 analyses the detectability of the floating gate fault using the three classical test strategies. Detectability is discussed according to the unpredictable polysilicon-to-bulk capacitance C_{pb}. A new testing technique for the Static Current strategy is proposed based on the induction of voltage on the gate of the faulty transistor, through a crossing metal wire. It is shown that if the voltage at the floating gate of an n-MOS transistor in a logic gate assumes a value between V_{TN} and V_{DD} (V_{PT} and V_{SS} for a p-MOS transistor), a quiescent current path in the logic gate can be created. This current can easily be sensed by the static current strategy. Complete analysis is given by considering an example of a two input NOR gate.

Chapter 4 compares the detectability intervals for the three test strategies SV, DV and SC. It is shown that the range is larger for the Dynamic Voltage technique than for the Static Voltage technique. The Static Current strategy exhibits a complementary interval with respect to both the SV and DV strategies. A combination of either one of the voltage strategies and the Static Current strategy using the proposed technique, can ensure complete coverage of the floating gate faults.

Finally, it is analyzed how the detectability intervals change with the amount of initial charges trapped on the floating gate transistor. It is shown that a greater value of initial trapped charges decreases the detectability interval for the SV and DV strategies, whereas the interval increases for the Static Current strategy. Similarly, the effect of the overlapping metal potential and the corresponding metal-poly capacitance is also presented in detail.

Chapter 2

Electrical Analysis of a Floating Gate Transistor

It is widely assumed that an open gate fault in a MOS transistor is equivalent to a stuck-at fault. In this chapter we demonstrate that a floating gate transistor (FGT) is influenced by its topological environment. It is shown that the equivalent gate potential V_{gs} of the faulty transistor depends on its own drain to source voltage V_{ds}, the influence of an overlapping metal track V_m, and different technological and topological parameters. It is shown that the induced voltage on the defective transistor decreases for higher values of the poly-bulk capacitance C_{pb} and increases for the lower values of the same. A strong relationship between the crossing-metal potential V_m together with the corresponding metal-poly capacitance value C_{mp}, and the induced voltage on the gate is also presented in detail.

2.1   The Floating Gate Transistor Fault

A floating gate fault will occur when the connection between the gate terminal of a MOS transistor and the driving source is open circuited. In such a configuration, a voltage is induced at its gate with values depending on the coupling capacitances of the transistor and of the surrounding circuitry, and by the gate oxide trapped charges. Consider the n-transistor shown in Figure 2.1.
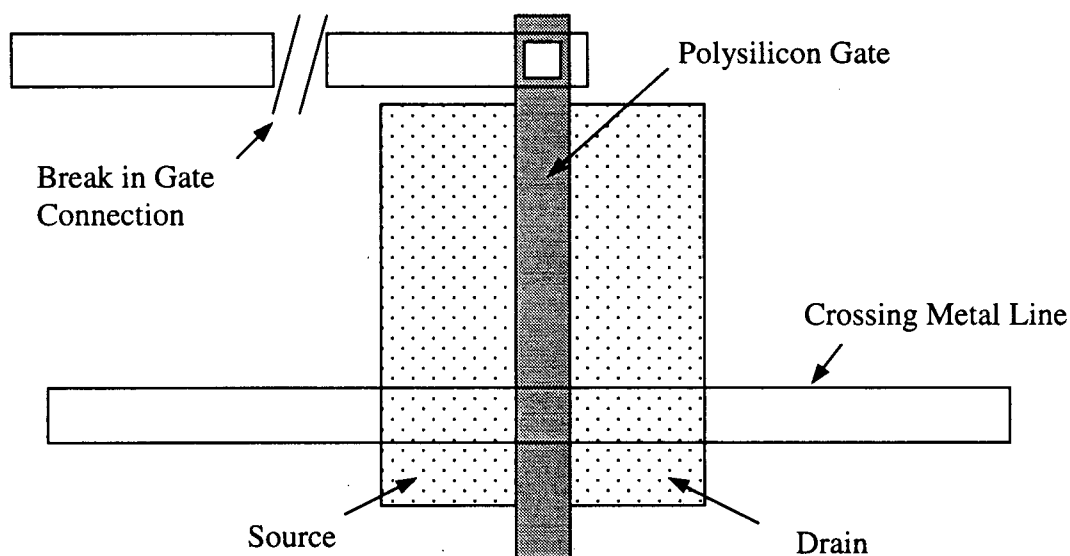
Figure 2.1. A floating gate transistor (FGT).

The gate connection of the transistor is open, i.e., not connected to the gate control node through a "good" ohmic connection, i.e., low resistance; hence the potential of the gate is floating.

A floating gate transistor fault can result from one of the following probable causes:

i)   Layout design errors

ii)   Photolithography defects

iii)   Poor contact / via processing

iv)   Migration phenomena in tracks or contacts

v)   Corrosion.

One of the most probable causes of those listed above is the photolithographic defect [17]. Defects in any of the interconnect or contact layers, which result in missing material, can also produce floating gate faults. As will be discussed later in this chapter, the location of a defect in the circuit layout will have a significant effect on the fault behavior produced.

2.2   Electrical Analysis of a Floating Gate Fault

The electrical environment of an FGT consists of potentials and capacitances [5, 14]. The different potentials are the source potential (V_s), bulk potential (V_b), and the drain potential (V_d). In addition, we assume that a metal track crosses the gate. The corresponding potential is V_m. Finally, we assume that charges Q_0 can be trapped in the silicon dioxide. Many well-known origins such as hot electrons, photons, and technological processes can induce charges in the silicon dioxide [17]. The different capacitances are as follows:

- the gate to source capacitance C_{gs}

- gate to bulk capacitance C_{gb}

- gate to drain capacitance C_{gd}

- gate to source overlap capacitance C_{gso}

- gate to drain overlap capacitance C_{gdo}

- metal to gate overlap capacitance C_{mp}, and

- polysilicon on thick oxide to bulk capacitance C_{pb}

The question is how this electrical environment (V_s, V_d, V_m, Q_o) will affect the potential V_{fg} of the floating gate. The resulting electrical equivalent circuit for an n-MOS transistor is given in Figure 2.2 (a).
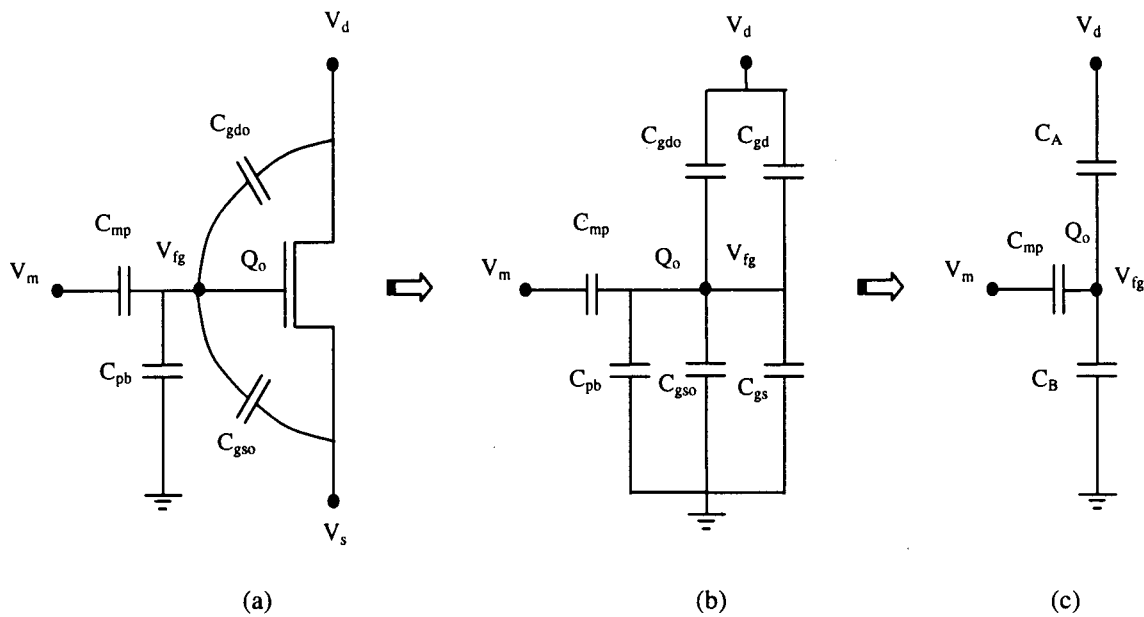
Figure 2.2. Floating gate n-MOS transistor model.

Of course, the source and the drain terminals are physically symmetrical. For the n-channel MOS the bulk is grounded and the terminal labels are assigned so that drain-to-source voltage V_{ds} is normally positive. For the sake of convenience, the source is considered to be grounded and used as a reference. The resulting equivalent circuit of Figure 2.2 (a) is given in Figure 2.2 (b).

In Figure 2.2 (b), capacitances C_{gd} and C_{gdo} are in parallel. Similarly, C_{gs}, C_{gso} and C_{pb} are in parallel as well. It is to be recalled that when capacitors are connected in parallel, the effective plate area increases, and the total capacitance is the sum of the individual capacitances, i.e., capacitors add in parallel. In Figure 2.2 (c), C_A and C_B represent the equivalent capacitance of the floating gate transistor model of Figure 2.2 (b) and are equal to $C_A = C_{gdo} + C_{gd}$ and $C_B = C_{pb} + C_{gso} + C_{gs}$. The capacitance C_{mp} is not added in C_A or C_B, as it depends on the potential V_m. If $V_m = Vd$, C_{mp} comes in parallel to C_A. On the other hand, if $V_m = V_{SS}$, C_{mp} comes in parallel to C_B.

Figures 2.3 (a) and (b) show different situations with $V_m = V_{SS}$ and $V_m = V_d$ respectively. In Figure 2.3 (a) $C_1 = C_A$ and $C_2 = C_B + C_{mp}$; whereas in Figure 2.3 (b), $C_1 = C_A + C_{mp}$ and $C_2 = C_B$.
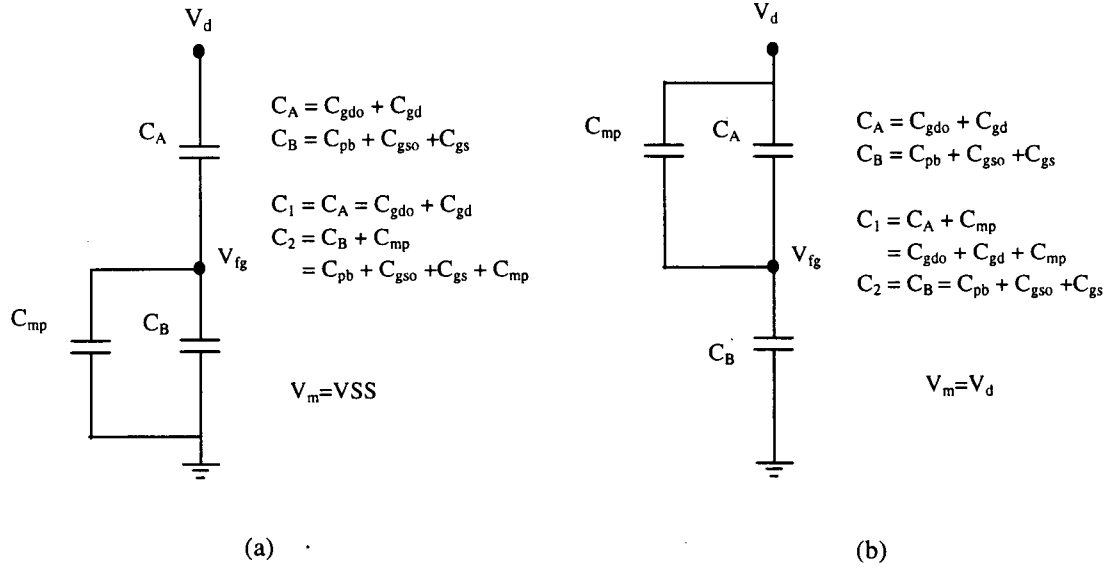
Figure 2.3. Equivalent model of a floating gate transistor with $V_m = V_{SS}$ and $V_m = V_d$, respectively.

A series connection of the charged capacitors acts as a voltage divider. The voltage across each capacitor in series is inversely proportional to its capacitance ($V = Q/C$). Since the charge on any capacitor in series is the same as the total charge (in a series circuit the current must be the same at all points, and since current is the rate of flow of charge, the amount of charge stored by each capacitor is equal to the total charge), hence:

$$Q_{Total} = Q_1$$

$$C_2 V_{fg} = C_{Total} V_d + Q_o \qquad where, \quad C_{Total} = \frac{C_1 C_2}{C_2 + C_2}$$

$$V_{fg} = \frac{C_{Total} V_d}{C_2} + \frac{Q_o}{C_2}$$

$$V_{fg} = \frac{C_1}{C_1 + C_2} V_d + \frac{Q_o}{C_2} \qquad \text{.............} \qquad (2.1)$$

Where

$$C_1 = C_{gdo} + C_{gd}$$

$$C_2 = C_{pb} + C_{gso} + C_{gs} + C_{mp} \quad for \ V_m = V_{SS}$$

and

$$C_1 = C_{gdo} + C_{gd} + C_{mp}$$

$$C_2 = C_{pb} + C_{gso} + C_{gs} \qquad for \ V_m = V_d$$

From equation (2.1) it is clear that the behavior of a transistor is strongly dependent on the drain voltage. Champac et. al. [16] made experimental measurements from fabricated n-MOS transistors with floating gate defects. The experimental data showed that the defective transistors might still work in the saturation region for high drain voltages. The induced voltage at the floating gate V_{fg} decreases as the drain voltage decreases. For a certain drain voltage, the transistor begins to work in cut-off ($V_{fg} \approx V_{TN}$). Then, the floating gate transistor is not completely turned off but rather works in the sub-threshold region, low current levels flow through the defective transistor and the transistor can be considered as *slightly* ON.

From equation (2.1), it is also clear that the induced voltage on the defective transistor decreases for higher values of C_{pb} and increases for lower values of the same. Similarly, with $V_m = V_{DD}$, the induced voltage at the gate of a transistor increases for higher values of C_{mp} and decreases with a lower value. With $V_m = 0$, the induced voltage at the gate

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decreases for a higher value of C_{mp} and increases with a lower value. Similar relationships of C_{mp} and C_{pb} were observed by Champac and Figueras [15].

The metal-polysilicon capacitance C_{mp} is an overlap capacitance whose value depends on the gate capacitor area and the metal-to-poly capacitance per unit area [3, 5, 14, 16]. The area can be extracted from the circuit layout and the value per area unit is a known technological parameter. Consequently, the C_{mp} value for a given defect can be predicted. In the same way, by using the layout and the technological parameters, the C_{gd} and C_{gs} capacitances can be computed. All the capacitances of the interconnect open defect appear being predictable except the polysilicon on thick oxide capacitance C_{pb}. Indeed, the value per area unit is perfectly known, but the same depends on the location of the open on the line, which is purely random. So, for the interconnect open, the C_{pb} capacitance must be viewed as an unpredictable parameter. The quantity of the trapped charges Q_o on an FGT is a technological specificity that is not commonly given [6]. The effect of Q_o on the behavior of an FGT will be studied later in chapter 4.

The above analysis has been centered on an n-MOS transistor. A similar analysis can be carried out for a p-MOS transistor.

Chapter 3

Floating Gate Fault Detection

3.1 Introduction

In this chapter we analyze the detectability of the floating gate faults using the three classical test strategies viz., Static Voltage (SV), Dynamic Voltage (DV), and Static Current (SC) testing strategies. Detectability is discussed according to the unpredictable polysilicon-to-bulk capacitance C_{pb}. A new testing technique for the Static Current strategy is proposed based on the induction of voltage on gate of the faulty transistor, through a crossing metal wire. We show later that if the voltage at the floating gate of an n-MOS transistor in a logic gate assumes a value between V_{TN} and V_{DD} (V_{PT} and V_{SS} for a p-MOS transistor), a quiescent current path in the logic gate can be created. This current can easily be sensed by the Static Current testing strategy. Complete analysis is given by considering an example of a two input NOR gate.

3.2   Detection of a Floating Gate Fault

The circuit in Figure 3.1, composed of a NOR gate and an inverter illustrates an interconnect open. In the NOR gate, the gate of the n-MOS transistor on input V_{in1} is disconnected. Hence this transistor is a floating gate transistor. In this Section we examine the behavior of the floating gate fault with respect to the Static Voltage, Dynamic Voltage, and Static Current test strategies. In each case, it is demonstrated that the detection depends on the unpredictable parameter C_{pb}.
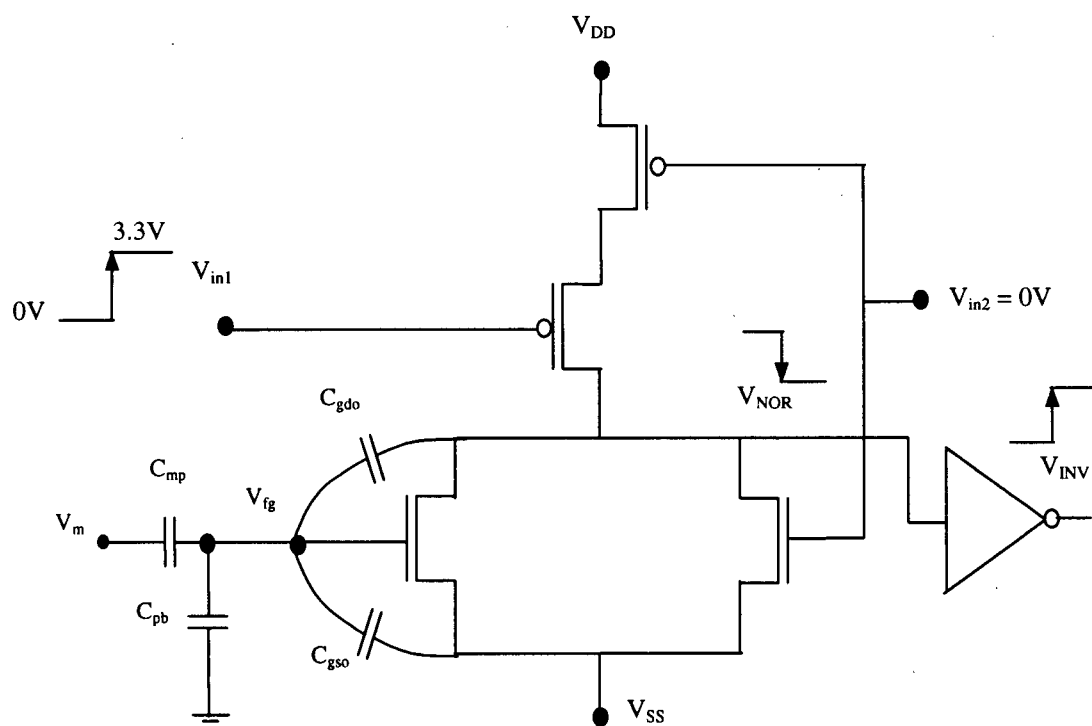
Figure 3.1. An interconnect open in a NOR gate.

Figure 3.2 gives the Cadence Spectre simulation results of the NOR gate of Figure 3.1 using a standard 0.5 micron, 3.3V technology. It is assumed for these simulations that there is no initial charge Q_o on the floating gate transistor. The behavior of the circuit with initial charge consideration will be discussed later in Chapter 4. The first NOR gate input V_{in1} performs a rising transition from 0 to 3.3V, while the second NOR gate input V_{in2} is equal to 0V. In the fault-free circuit, the output of the NOR gate obviously switches from 3.3V to 0V. The behavior of the faulty NOR gate output V_{NOR} is given in Figure 3.2 for different C_{pb} values.
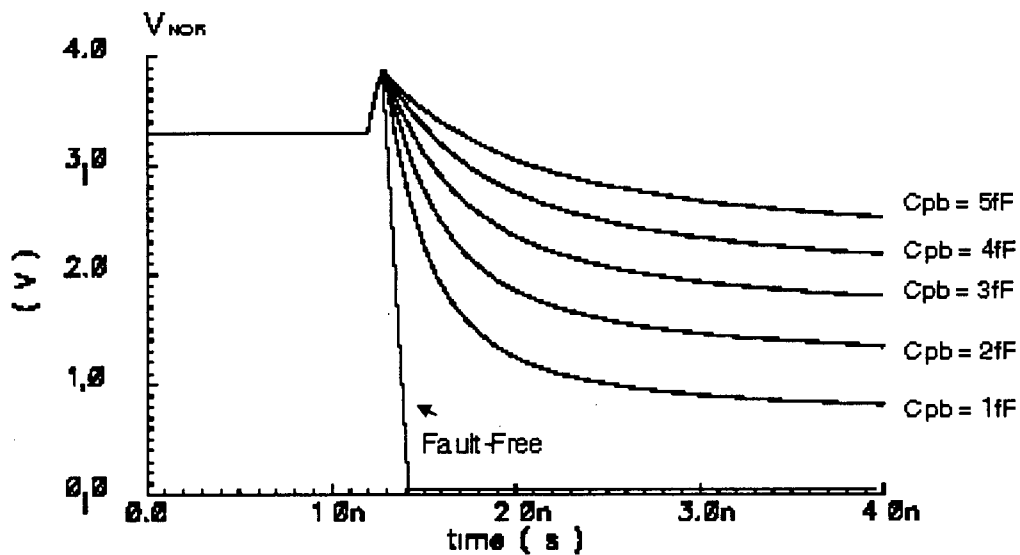
Figure 3.2: Faulty behavior of the NOR gate

To analyze the plots in Figure 3.2, we have to detail the behavior of the floating gate transistor. The charges trapped in the gate oxide, plus the influence of the crossing metal

line and the influence of the drain voltage create an induced voltage on the floating gate in such a way that the faulty transistor is in a so-called 'slightly' ON state [3, 5, 14].

When V_{in1} = 0V, the p-MOS transistor is ON and the faulty n-MOS transistor is *slightly* ON. In this situation, we have two fighting conducting transistors. Due to the very different conduction of these two transistors, the output of the NOR gate is $V_{NOR} \approx 3.3V$, which is the correct value. It is important to note that the difference of degree of conduction is so large that the output is equal to 3.3V whatever the parameters of the defect: C_{mgo}, C_{pb}, C_{gd}, etc. The inverter controlled by a high output produces a low output V_{inv} = 0V. The current flowing through the p and n-transistor is negligible due to the low degree of conduction of the floating n-MOS transistor.

When the input rises to V_{in1} = 3.3V, the p-MOS transistor is turned off, and the faulty n-MOS transistor remains slightly ON. In this situation, we no longer have two fighting transistors but only one slightly conducting n-MOS transistor. Consequently, the floating n-MOS transistor starts to slowly discharge the output node V_{NOR}. The output voltage V_{NOR} slowly decreases as illustrated in Figure 3.2. But the voltage induced on the floating gate depends on the drain voltage, which is V_{NOR}. So the voltage induced on the floating gate decreases as V_{NOR} decreases. For a certain V_{NOR} = V_{final}, this floating gate voltage is equal to threshold voltage V_{TN} and the transistor is turned OFF as described by Champac and Figueras [14]. In this new situation we have two OFF transistors, the NOR gate output is in a high impedance state and the final voltage V_{final} is memorized on the output.

It is now important to note that the final voltage V_{final} strongly depends on the defect parameters including the unpredictable parameter C_{pb} as illustrated in Figure 3.2.

3.2.1 Static Voltage (SV) Testing Strategy

Considering a Static Voltage strategy, it clearly appears in Figure 3.2 that the circuit operates correctly when the input $V_{in1}=0V$ (the effect of the crossing metal potential in this situation, will be discussed in Chapter 4). When $V_{in1} = 3.3V$, the final NOR gate output voltage is V_{final}. If V_{final} is greater than the logic threshold Vth_{inv} of the inverter, this voltage is recognized as a faulty logic '1' and a faulty value can be propagated through the circuit, to a primary output.

V_{final} depends on the transistors' technological and topological parameters: C_{ox}, V_T, μ_n, μ_p, W_n, W_p, L_n, L_p, C_{mp}, C_{gd}, including the trapped charges Q_o [6]. But it is of prime importance to remark that this voltage also depends on the unpredictable poly-to-bulk capacitance value: C_{pb}. Due to the presence of the unpredictable capacitance value, it is not possible to predict the V_{final} in case of a fault. Consequently, the static voltage strategy is not able to unconditionally detect floating gate faults.

However, it is useful to study the variations of the faulty behavior according to the values of the unpredictable parameter. From circuit simulations, we can plot the Static Voltage V_{final} versus C_{pb} characteristics as illustrated in Figure 3.3. In this Figure, V_{final}
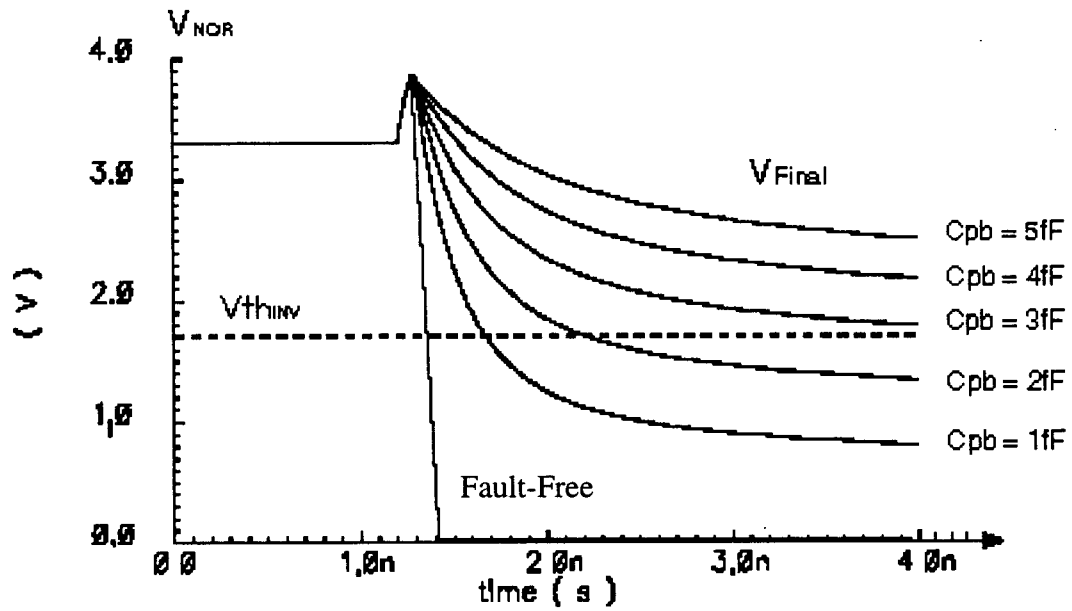
(a)
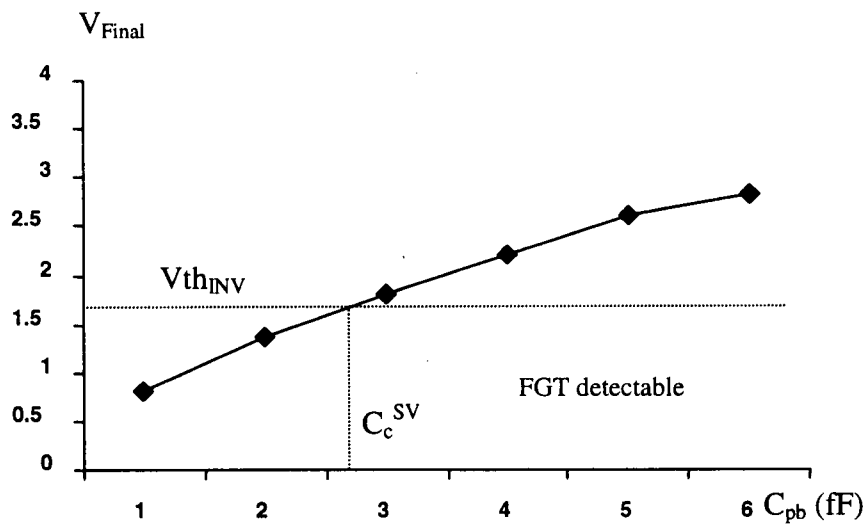
(b)

Figure 3.3: Static Voltage behavior of a floating gate transistor.

increases when C_{pb} increases. V_{final} is greater than the logic threshold voltage Vth_{INV} of the driven gate if the unpredictable parameter C_{pb} is greater than a critical capacitance C_c^{SV}. This small example illustrates that a critical value of the unpredictable parameter can be defined for the FGT fault. An FGT fault can be detected using a Static Voltage test if the unpredictable parameter C_{pb} falls into the interval $[C_c^{SV}, \infty]$. In this case, the logic fault model associated to the interconnect open corresponds to what is commonly called a 'Stuck-Open' transistor fault [2].

3.2.2 Dynamic Voltage (DV) Testing Strategy

When V_{in1} rises from 0 to 3.3V, the faulty NOR gate output falls from 3.3V to V_{final}. It can be noted that this falling transition is delayed due to the low degree of conduction of the floating gate transistor. If this delay D is greater than the slack time SL of the node, a faulty value will be captured on the circuit output. It is clear that the resulting delay D depends on transistor technological and topological parameters and on the poly-bulk capacitance C_{pb}. As for the static voltage detection, due to the presence of the unpredictable poly-bulk capacitance value, it is not possible to compute a priori the delay D. Consequently, the Dynamic Voltage strategy is not able to unconditionally predict the detection of a floating gate fault.

Here again, we can study the variation of the faulty behavior according to the values of the unpredictable parameter C_{pb}. Using Spectre simulations, Figure 3.4 gives the delay

versus C_{pb} characteristics where the delay increases when C_{pb} increases. The delay D is

greater than the slack time SL if the unpredictable parameter C_{pb} is greater than a critical

capacitance C_c^{DV}. It is interesting to note that the delay D becomes infinite when V_{final}

becomes greater than the logic threshold Vth_{INV} of the inverter. Indeed, in this case there

is no switching and the delay fault behaves as a stuck-open fault which may be viewed as

a particular case of a delay fault. Consequently, this faulty dynamic behavior includes the

faulty static behavior and we have $C_c^{DV} < C_c^{SV}$. This small example illustrates that a FGT

fault can be detected using a Dynamic Voltage test if the unpredictable parameter C_{pb}

falls into the interval $[C_c^{DV}, \infty]$.
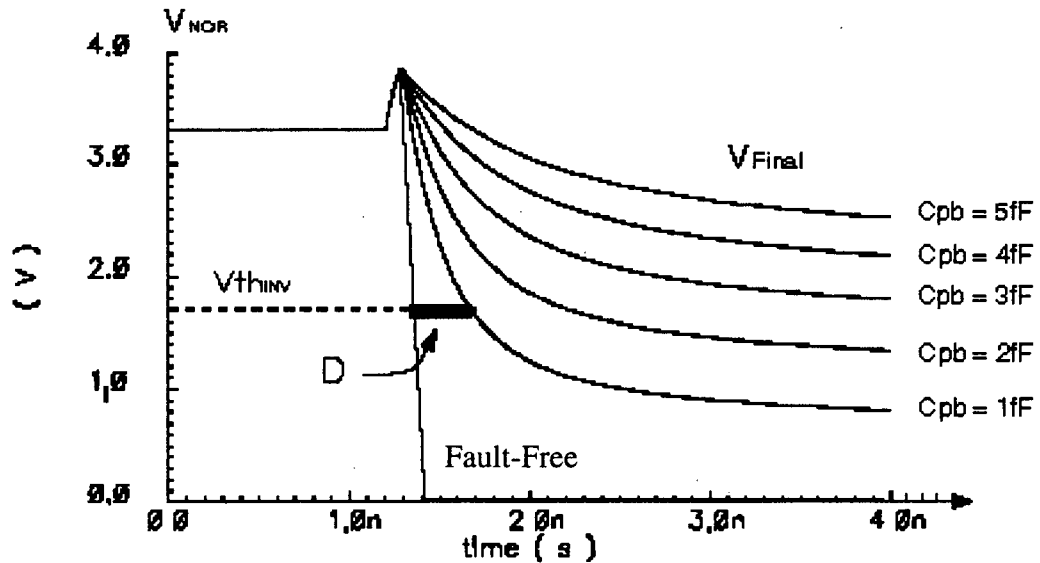
Figure 3.4 (a). Dynamic behavior of an FGT
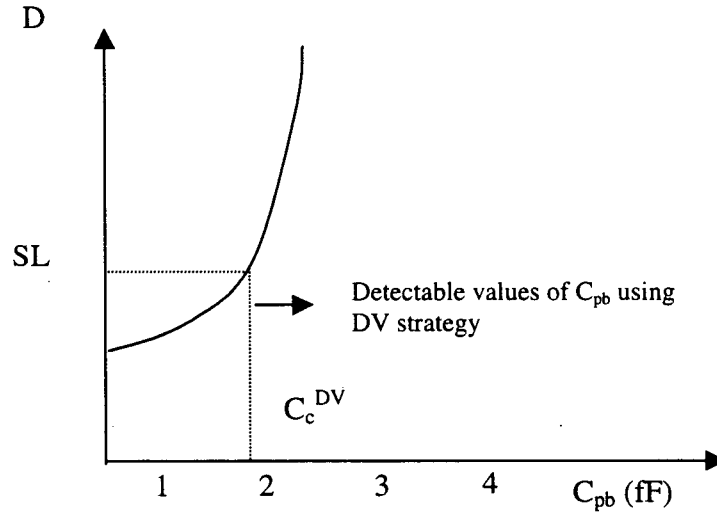
(b)

Figure 3.4: Dynamic behavior of an FGT.

3.2.3 Static Current (SC) Testing Strategy

Due to the low degree of conduction of the floating gate transistor (*slightly* ON state), the current in the NOR gate is negligible. No current detection of the floating gate is possible by giving a rising transition on V_{in1} keeping $V_{in2} = 0$ while only considering the current flowing in the NOR gate. This detection might become possible if we consider the current flowing in the driven inverter gate. That is, when $V_{in1} = 0V$, the output of the NOR gate is equal to V_{final} which is an intermediate voltage between V_T and $V_{DD}-V_T$. In such conditions, the two transistors of the driven inverter are 'ON' (with different degrees of conduction) and a current I_{DDQ} flows in the inverter from V_{DD} to GND during the steady state [6,9,11,16]. But generally, this is not a valid test strategy for I_{DDQ}, as the

situation might become entirely different if instead of an inverter, a complex gate was driven by the output of the faulty NOR gate.

The following details a proposed technique which makes floating gates I_{DDQ} testable independently of current in the driven gate, by controlling the potential V_m, of a crossing metal wire. The behavior of the circuit with different metal-poly capacitance is described first, followed by the analysis for behavior with the unpredictable parameter C_{pb}.
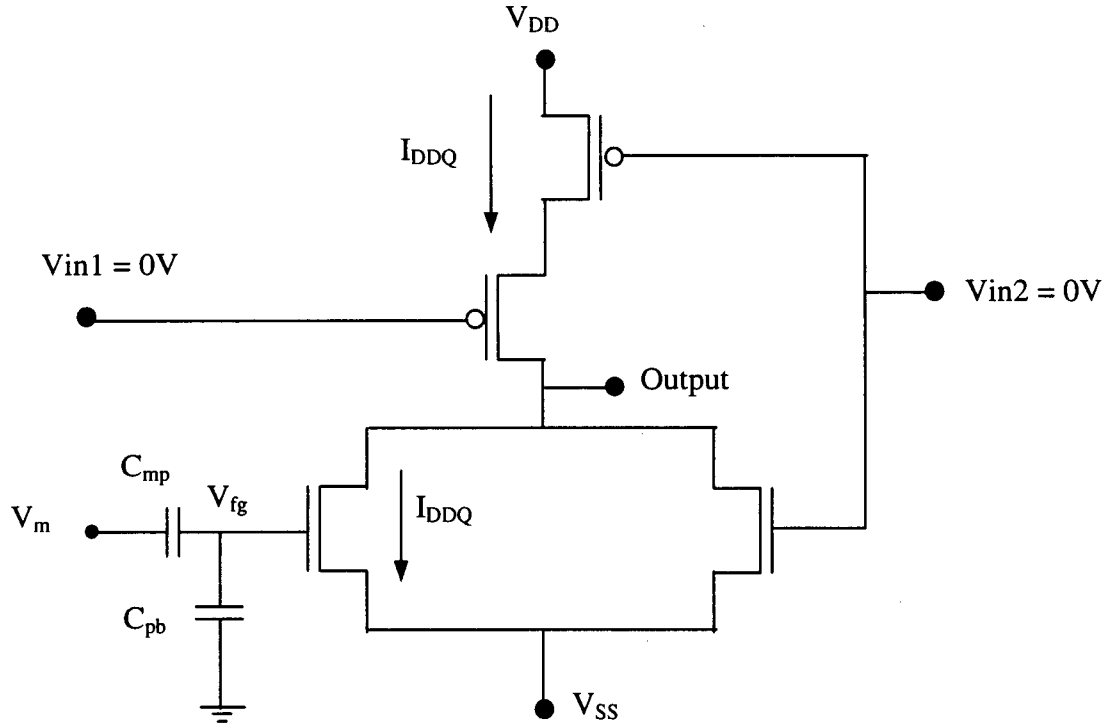
Figure 3.5 (a): A faulty NOR gate circuit.

From Fig. 3.5 (a), when $V_{in1} = 0V$ and $V_{in2} = 0V$, a high impedance path from the power supply to ground through the defective transistor is created (as the defective n-MOS

transistor is *slightly* ON). If the voltage at the floating n-MOS gate assumes a value

between V_{TN} and V_{DD}, an increased quiescent current I_{DDQ} flows through the NOR gate.

This increase in the quiescent current can be used to detect the floating gate defect by

I_{DDQ} testing, independent of the current in the driven gate. As mentioned in Chapter 2, for

$V_m = V_{DD}$, the induced voltage at the gate of the transistor is directly proportional to C_{mp},

while for $V_m = 0$, the induced voltage at the gate becomes inversely proportional to C_{mp}.

Using this relationship, it is clear that by increasing the voltage at V_m, we can increase

the voltage at the gate of the transistor. Several Spectre simulations were conducted with

$V_{in1} = V_{in2} = 0V$, by giving a rising transition at V_m from 0 to 3.3V for the NOR gate in

Figure 3.5 (b).

Figure 3.5 (b): Current testing (SC) for FGT NOR gate.

When $V_{in1} = V_{in2} = 0V$ and $V_m = 0V$, both p-MOS transistors conduct. Assuming the extreme case, i.e., when there are no trapped charges on the floating gate transistor, the floating gate acquires a voltage depending only on its electrical environment from the drain voltage V_d, through capacitances C_{gd}, C_{gs}, C_{pb}, C_{mp}. This voltage strongly depends on the C_{pb} and C_{mp} values 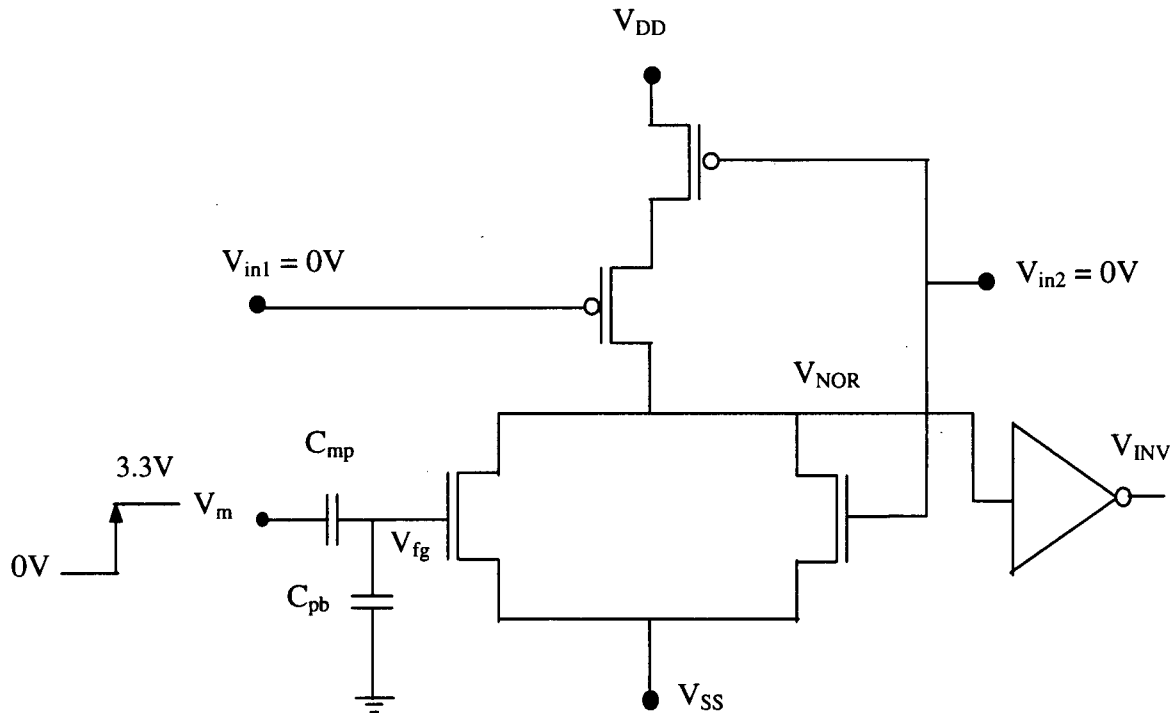[11]. As stated in Chapter 2, when $V_m = 0V$, the value of C_{mp} is added to C_{pb} ($C_2 = C_{pb} + C_{gso} + C_{gs} + C_{mp}$; capacitors in parallel). In that case, the induced voltage on the gate of the defective transistor (V_{fg}) decreases for higher values of C_{pb}, the floating gate acquires a smaller value with $V_m = 0V$. However, when the voltage V_m rises to 3.3 volts, the effective value of C_2 ($C_2 = C_B = C_{pb} + C_{gso} + C_{gs}$) decreases and the effective value of C_1 ($C_1 = C_A + C_{mp} = C_{gdo} + C_{gd} + C_{mp}$) increases. As a result, the voltage on the floating gate also increases. If the values of capacitors are such that V_{fg} rises above the threshold voltage V_{th} of the transistor, the transistor starts conducting and allows a quiescent current to flow through it making the faulty gate I_{DDQ} testable.

Figure 3.6 shows plots obtained by sweeping C_{pb}, with $C_{mp} = 250aF$. A NOR cell with an n-MOS floating gate transistor on V_{in1}, was laid out using a standard 0.5 micron technology, with the n-MOS transistors of dimension 0.6 μ by 2μ, and p-transistors of dimension 0.6μ by 3μ. A crossing metal wire of length 110μ in metal 2 gave $C_{mp} = 422aF$. A value of 250aF for C_{mp} is therefore a reasonable value to plot the current versus C_{pb} characteristics. Similarly, to get a critical value for I_{DDQ} testing, a circuit of 10,000 gates was laid out using the same 0.5-micron technology. An I_{DDQ} current of 0.34 μA was observed for these 10,000 gates. Allowing for a margin of one order of magnitude yields

3.4 μA as a critical current for I_{DDQ} testing. The plots indicate that by increasing C_{pb}, the floating gate acquires a smaller voltage and consequently the current in the faulty gate decreases.
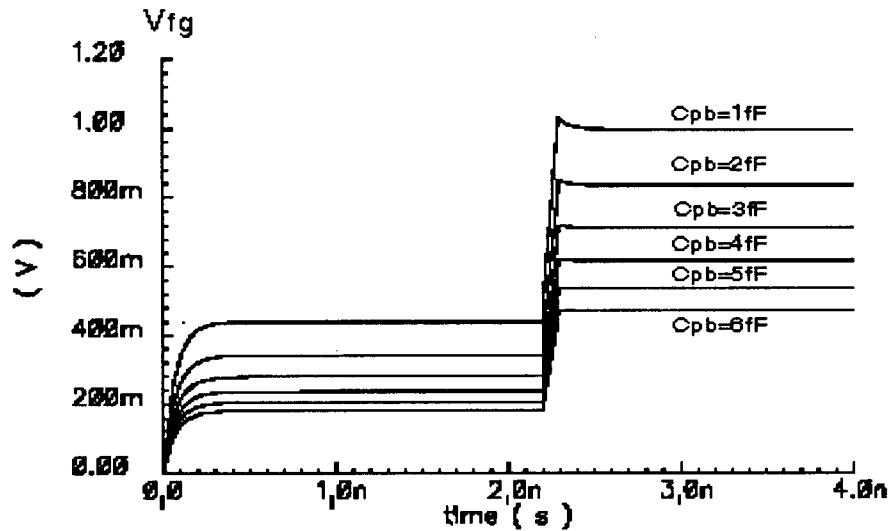
(a)
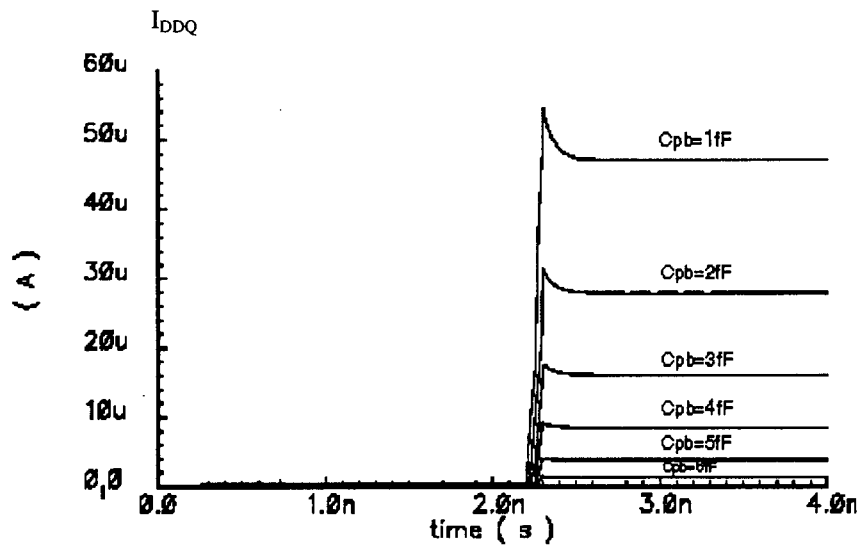
(b)

Figure 3.6: Change in the floating gate voltage and current by sweeping C_{pb}; C_{mp}=250aF

Figure 3.7 gives the current versus C_{pb} characteristics where the current decreases when C_{pb} increases. So, the current is greater than the minimum required if the unpredictable parameter C_{pb} is smaller than a critical capacitance C_c^{SC}. A floating gate transistor fault can be detected using Static Current test if the unpredictable parameter C_{pb} falls into the interval $[0, C_c^{SC}]$.
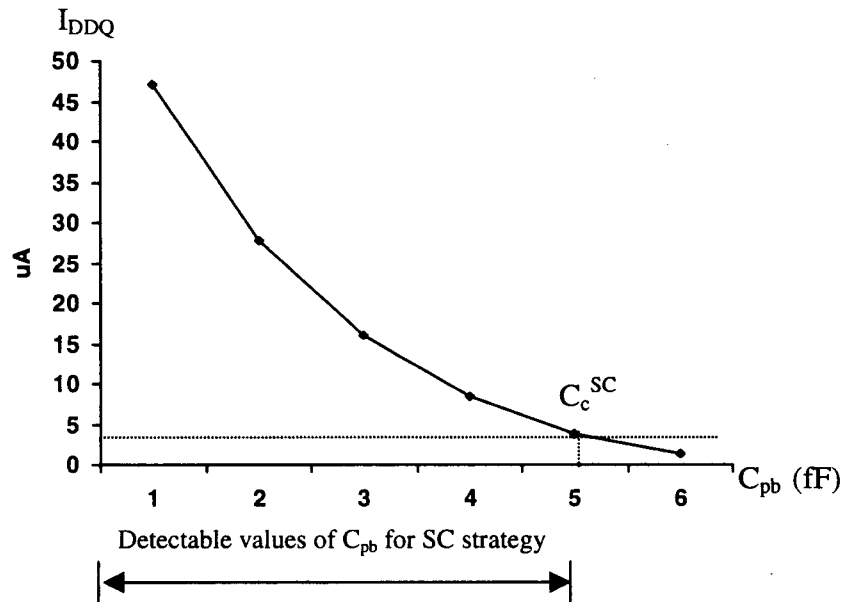
Figure 3.7: Current versus C_{pb} characteristics of an FGT.

Chapter 4:

Test Strategy Detectability Intervals for the

Floating Gate Transistor Fault

4.1   Introduction

This chapter compares the detectability intervals for the three test strategies SV, DV and

SC. It is shown that the range is larger for the Dynamic Voltage technique than for the

Static Voltage technique. The Static Current strategy exhibits a complementary interval

with respect to both SV and DV strategies. A combination of either one of the voltage

strategies and the Static Current strategy using the proposed technique, can ensure

complete coverage of the floating gate faults. Moreover, we analyze how the detectability

intervals change with the amount of initial charges trapped on the floating gate transistor.

It is shown that a greater value of initial trapped charges decreases the detectability

interval for the SV and DV strategies, whereas the interval increases for the Static

Current strategy. This again suggests a combination of both the current and voltage testing strategies to ensure a complete coverage of the floating gate faults. The effect of metal-poly capacitance C_{mp}, and metal potential V_m on the detectability intervals is also studied in detail.

4.2   Test Strategy Sensitivity to Floating Gate Fault Parameter

In the Chapter 3, the detection of floating gate faults has been analyzed using three different test strategies, viz., Static Voltage, Dynamic Voltage and Static Current. This analysis can now be used to clarify the relationships between these test strategies.

First , the main remark coming from the previous study is that the behavior of a defect clearly depends on unpredictable parameters. Second, for a given test strategy, the detection of a floating gate defect can never be guaranteed due to the presence of the associated unpredictable parameter. However, the defect can be detected by a given test strategy if its unpredictable parameter falls within a specific interval. More formally, each couple (Defect, Test Strategy) is associated with a given interval.

As indicated above, a defect cannot be simply unconditionally declared as detected or un-detected. So the efficiency of a test strategy cannot be evaluated using the oversimplified concept of detection or non-detection. Consequently, the unpredictable parameter interval represents a reasonable criterion that can be used to evaluate the efficiency of a Test

Strategy as well as to compare the efficiency (the global ability to detect realistic defects rather than faults) of different test strategies. Figure 4.1 shows the detectability intervals for Static Voltage, Dynamic Voltage and Static Current strategies for FGT faults.

Static Voltage

Dynamic Voltage

Static Current

Zn 1   Zn 2   Zn 3   Zn4
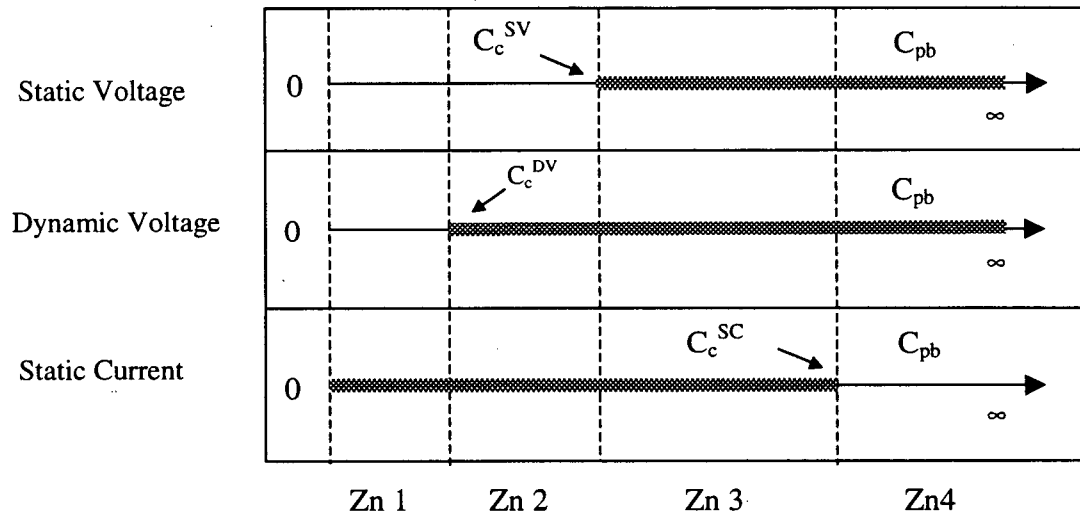
Figure 4.1: FGT Fault Detectability Intervals.

The global consideration of Figure 4.1 shows that all three test strategies are able to detect the considered defect. In each case, we observe a non-empty interval. Using the oversimplified 'detection' versus 'non-detection' concept, the three test strategies appear as equivalent. Of course, this is not the case when considering the size of the interval. Indeed, it seems clear that larger interval means a higher probability of defect detection, and so a higher efficiency. The Static Voltage strategy presents an interval smaller than the Dynamic Voltage since C_c^{SV} is always greater than C_c^{DV}. Consequently, we can say that DV (zone 2,3,4) is more efficient than SV testing (zone 3, 4). The Static Current Strategy presents a complementary interval with respect to the Static and Dynamic

Voltage strategies (zone 1, 2, 3), but overlaps with both Static Voltage and Dynamic Voltage test strategies. It is evident that a combination of either one of the voltage strategies and the Static Current strategy can ensure complete coverage of the floating gate fault.

4.3   Effect of the FGT Initial Charge on the Detectability Intervals

All the simulation results in chapter 3 were generated by considering the extreme case scenario, with no initial charge on the faulty transistor. In this sub-section we will explain how the detectability intervals change with the amount of charge Q_o trapped on the floating gate transistor.

4.3.1   The Source of Residual Charge

Potential residual charge is most likely to result from the processing of the ICs as the devices had been stored unpowered before testing. Johnson [17] suggests that one possible source of charge is the plasmas that are used in IC fabrication for the etching of various layers and resists. Consider, for example, the patterning of polysilicon by reactive ion etching. The ions at the surface of the sample are positive as the sample is placed on the cathode of the etching system. Interaction of the plasma with the polysilicon as it etches the layer will therefore result in the transfer of charge into the material. At this point the charge density will be roughly uniform within the sheet. Completion of the etch will result in a set of isolated polysilicon tracks and gates which all contain positive

charge. It is probable that the photoresist layer would then be removed by a further dry etching process during which the isolated polysilicon tracks are exposed to further positive charge. Subsequent exposure of the wafer to oxygen or nitrogen atmospheres will produce a silicon dioxide or a silicon nitride coating on all polysilicon surfaces which will trap the residual charge [17]. Later stages of the processing will connect all fault free polysilicon tracks to metal tracks providing a conducting path for the tracks to be discharged. Polysilicon gates that remain isolated will retain their positive charge, and this is seen as the unbiased floating gate potential when devices are used.

The analysis presented so far suggests that the charge density will be approximately uniform throughout the polysilicon tracks. Johnson [17], however, made experimental measurements of the floating gate potential in which this is not seen to be the case. A possible cause for this variation can be seen by considering further stages of processing. The first stage of the charge deposition during the reactive ion etch of the polysilicon should result in a uniform charge distribution. The polysilicon layer is a single conducting sheet until the etch is complete, and so for most of the etch a uniform charge distribution will occur. The situation is different during the removal of photoresist. For most of this process, each isolated polysilicon track is exposed to the plasma only along its perimeter. One might therefore assume that the amount of charge accumulating on each track should be determined by the length of the track perimeter. This would result in higher values of residual charge for longer or wider tracks or devices.

4.3.2   Detectability Intervals with an Initial Charge on the FGT

Figure 4.2 shows the behavior of the NOR gate output voltage V_{final}, when the initial charge Q_o on the floating gate increases. It is evident that as the initial charge on the floating gate increases, the voltage at the output of the faulty gate decreases. Hence the detectability intervals for Static Voltage and Dynamic Voltage strategies decrease too.
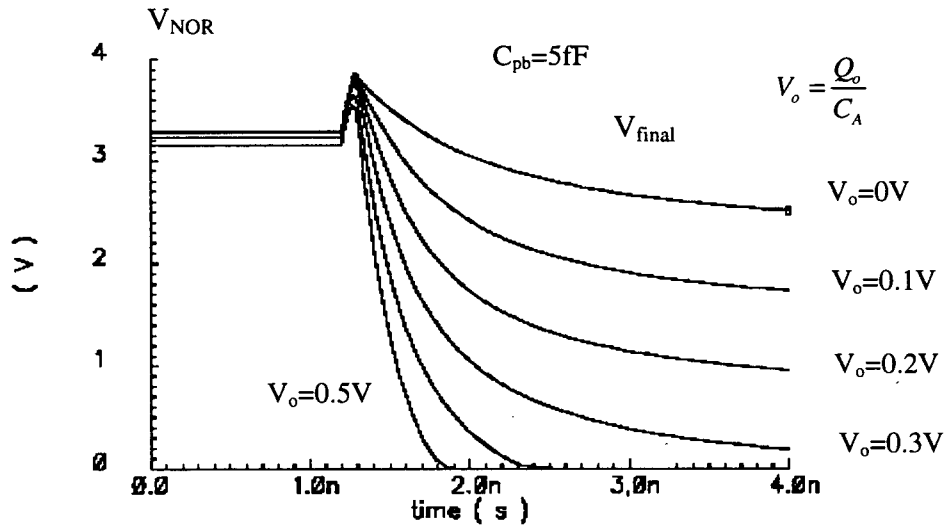
Figure 4.2: Change in the output voltage of the NOR gate with an increased initial charge Q_o.

Figures 4.3 and 4.4 show the detectability intervals for the Static Voltage and Dynamic Voltage strategies with an increased initial floating gate voltage of V_o=0.4V (V_o=Q_o/C_A). The critical capacitances C_c^{SV} and C_c^{DV} for both the strategies increase, giving a lower range of detectability intervals.

V_{Final}

Vth$_{INV}$

$V_o=0V$

$V_o=0.4V$

C_c^{SV}

C_{pb}

Detectable
values of C_{pb}
for SV strategy

$V_o=0V$
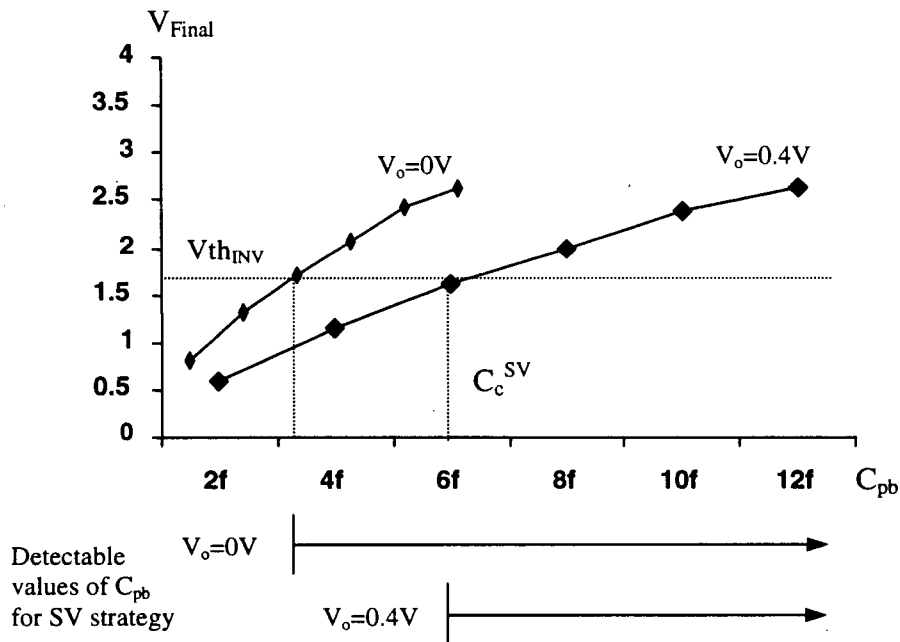
$V_o=0.4V$

Figure 4.3: Detectability intervals for Static Voltage strategy with $V_o=0.4V$

D

SL

C_c^{DV}

C_{pb}

Detectable
values of C_{pb}
for DV strategy

$V_o=0V$
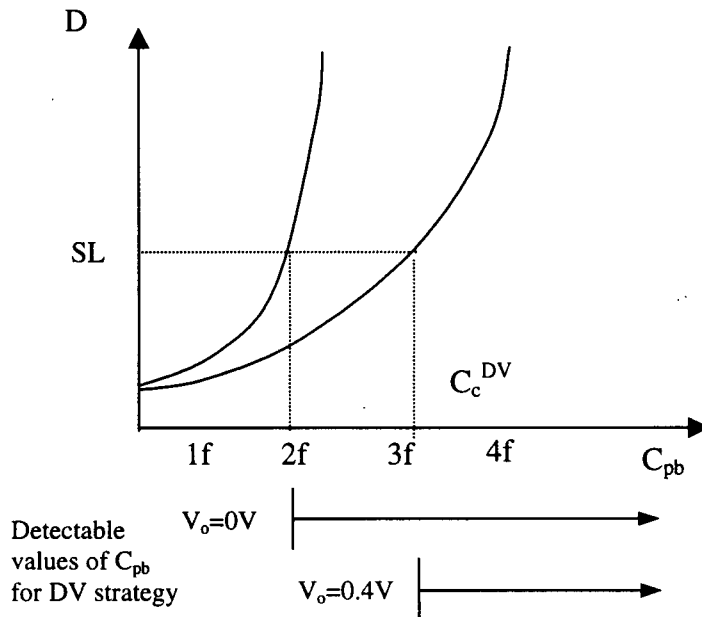
$V_o=0.4V$

Figure 4.4: Detectability intervals for Dynamic Voltage strategy with $V_o=0.4V$

As for the Static Current strategy, a higher V_{fg} means a higher current through the faulty transistor. Figure 4.5 shows the change in current through the floating gate transistor when the value of initial charge on the floating gate Q_o increases for $C_{pb} = 5$ fF. With $V_o = 0$V, $C_{pb} = 5$ fF gave a current value of 3.1uA, which was below the critical current of 3.4 uA. However, with a slight increase in the initial charge ($V_o=0.1$V), the current increases above the threshold current bringing $C_{pb} = 5$ fF in the SC strategy's detectable range.
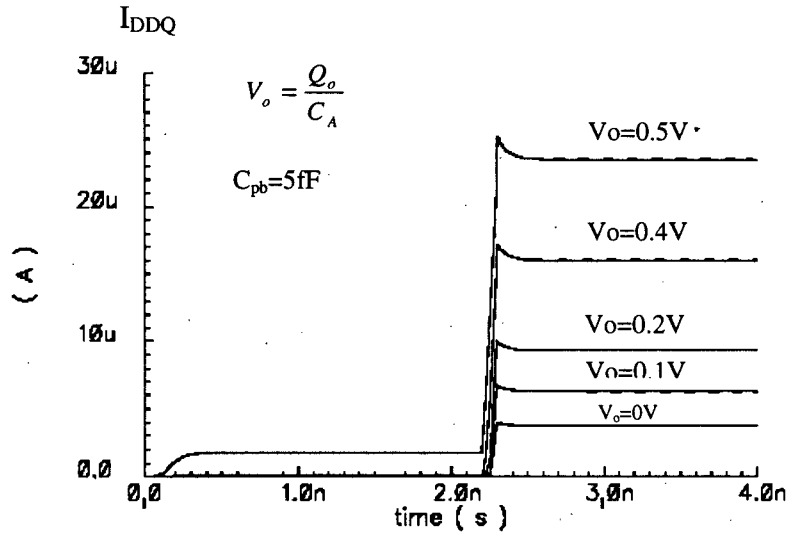
Figure 4.5: Change in I_{DDQ} current by an increase in initial charge on the floating gate.

The detectability behavior for the Static Current strategy with an increased initial floating gate voltage of $V_o = 0.4$V is shown in Figure 4.6.
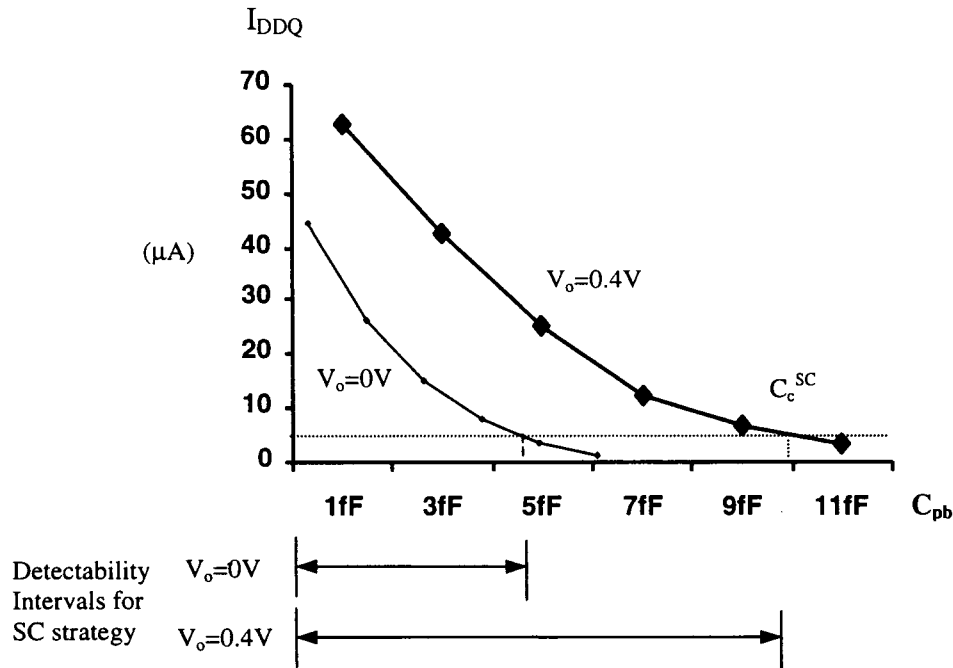
Figure 4.6: Change in the detectability interval for Static Current Strategy with V_o=0.4V

Figure 4.7 shows the changed detectability intervals for the three test strategies. It is evident that with the increase in the initial charge on the floating gate, the detectability interval of Static Current strategy changes more than for the voltage strategies. Hence the overlap between current and voltage strategies increases with the increase in the initial charge at the floating gate. However, it is important to note that the detectability interval for the voltage techniques decreases, hence conducting only the voltage test (even Dynamic Voltage) does not ensure a complete coverage of the floating gate fault. Therefore, it is necessary to conduct both current and either of the voltage strategies for guaranteed detection of the floating gate fault.
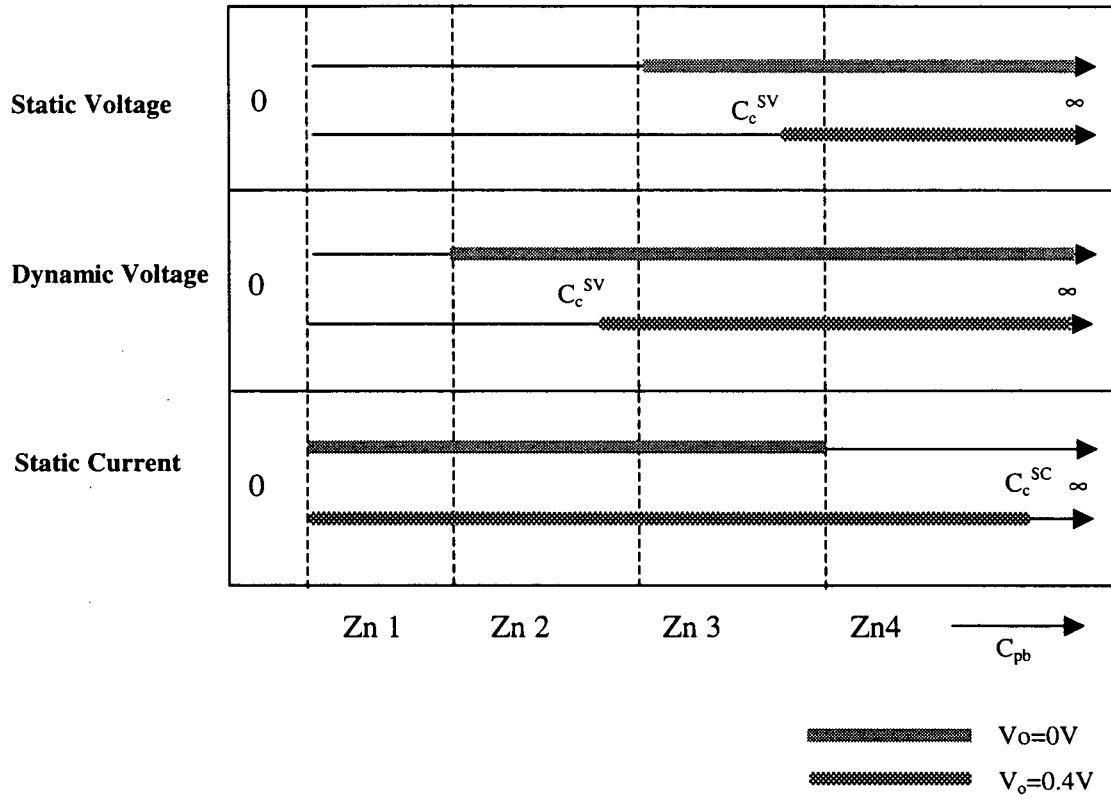
Figure 4.7: Change in the fault detectability intervals by trapped charges Q_0 on the FGT.

4.4   Effect of the Metal-Poly Capacitance C_{mp} and Metal Potential V_m on the Detectability Intervals

In this section, we will analyze how a crossing metal wire over a floating gate transistor affects the detectability intervals for the different test strategies. Two parameters are of prime importance while considering the effect of the metal, viz., (a) the value of the capacitance C_{mp}, and (b) the corresponding metal potential V_m. Electrical analysis of the

floating gate transistor with respect to V_m and C_{mp}, will be presented first followed by the study of influence of V_m and C_{mp}, on the detectability intervals.

4.4.1   Electrical Analysis of the Floating Gate Transistor for C_{mp} and V_m

To study the influence of C_{mp} and V_m on the FGT, we need to deduce an expression for V_{final} that will give a relationship between V_{final} and C_{mp} / V_m. Consider the electrical equivalent circuit for the floating gate n-MOS transistor of the faulty NOR gate of Figure 3.1 as follows:

For $V_m = VSS$
$$C_1 = C_{gdo} + C_{gd}$$
$$C_2 = C_{pb} + C_{gso} + C_{gs} + C_{mp}$$

For $V_m = VDD$
$$C_1 = C_{gdo} + C_{gd} + C_{mp}$$
$$C_2 = C_{pb} + C_{gso} + C_{gs}$$
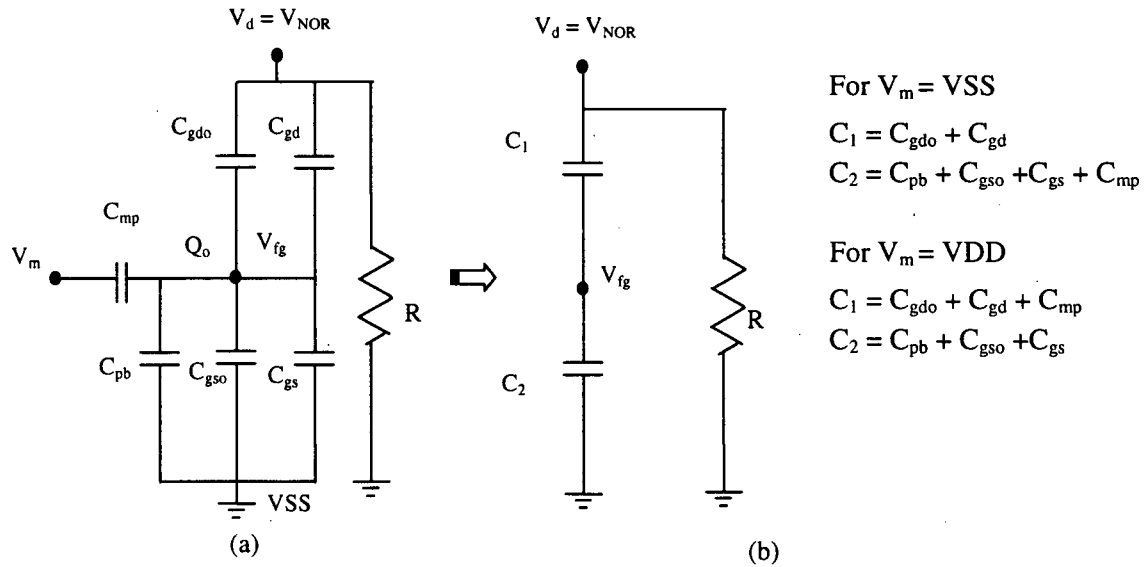
Figure 4.8: Electrical equivalent circuit of the n-MOS FGT of a faulty NOR gate

In the NOR gate of Figure 3.1, when $V_{in1} = V_{in2} = 0$ V, the drain voltage V_d of the FGT is at V_{DD}, which is the correct value as discussed in section 3.1. When V_{in1} rises to V_{DD}, the p-MOS transistor is turned off, and the faulty n-MOS transistor remains slightly ON. In

this situation, we have one slightly conducting n-MOS transistor. Consequently, this floating transistor starts to slowly discharge the output node V_{NOR}. But the voltage induced on the floating gate depends on the drain voltage, which is V_{NOR}. So, the voltage induced on the floating gate decreases as V_{NOR} decreases. For a certain $V_{NOR} = V_{final}$, this voltage is equal to threshold voltage V_{TN} of the FGT, and the transistor is turned OFF. In this new situation we have two OFF transistors, the NOR gate output is in a high impedance state and the final voltage V_{final} is memorized on the output. In Figure 4.8 (b) with $V_{fg} > V_{TN}$, the drain voltage of the n-MOS transistor V_d (=V_{NOR}), can be written as:

$$V_{NOR} = V_{DD} e^{-t/\tau}$$

where

$$\tau = R.\frac{C_1 C_2}{C_1 + C_2}$$

Taking a first order approximation V_{NOR} can be written as follows:

$$V_{NOR} = V_{DD}\left(1 - \frac{t}{R.(C_1 C_2)/(C_1 + C_2)}\right) \qquad \text{....... (4.1)}$$

Assuming no initial charge on the floating gate, the voltage at the gate of the n-MOS transistor is

$$C_2 V_{fg} = C_{Total} V_{NOR} \qquad\qquad where \quad C_{Total} = \frac{C_1 C_2}{C_2 + C_2}$$

$$\Rightarrow \quad V_{fg} = \frac{C_{Total}V_{NOR}}{C_2}$$

$$\Rightarrow \quad V_{fg} = \frac{C_1}{C_1 + C_2}V_{NOR} \qquad \text{.................} \qquad (4.2)$$

By inserting the value of V_{NOR} from Equation 4.1 into Equation 4.2, we get

$$V_{fg} = \frac{C_1}{C_1 + C_2}.V_{DD}\left(1 - \frac{t}{R.(C_1C_2)/(C_1 + C_2)}\right)$$

V_{final} will be reached when $V_{fg} = V_{TN}$. Hence,

$$V_{TN} = \frac{C_1}{C_1 + C_2}.V_{DD}\left(1 - \frac{t_{OFF}}{R.(C_1C_2)/(C_1 + C_2)}\right)$$

Re-arranging the above equation

$$\left(\frac{V_{TN}}{V_{DD}}.\frac{C_1 + C_2}{C_1}\right) - 1 = -\frac{t_{OFF}}{R.(C_1C_2)/(C_1 + C_2)}$$

$$t_{OFF} = \frac{R.C_1C_2}{C_1 + C_2} - \frac{R.C_2V_{TN}}{V_{DD}} \qquad \text{......} \quad (4.3)$$

At t_{OFF}, $V_{final} = V_{NOR}$. Hence

$$V_{final} = V_{DD}\left(1 - \frac{t_{OFF}}{R.(C_1C_2)/(C_1 + C_2)}\right) \qquad \text{........} \quad (4.4)$$

Inserting the value of t_{OFF} from Equation 4.3 into Equation 4.4 yields

$$V_{final} = V_{TN} \cdot \left(\frac{C_1 + C_2}{C_1} \right) \qquad \ldots \ldots \ (4.5)$$

As described in Chapter 2, for $V_m = V_{SS}$

$$C_1 = C_{gdo} + C_{gd}$$

$$C_2 = C_{pb} + C_{gso} + C_{gs} + C_{mp}$$

whereas for $V_m = V_{DD}$

$$C_1 = C_{gdo} + C_{gd} + C_{mp}$$

$$C_2 = C_{pb} + C_{gso} + C_{gs}$$

Writing equation 4.5 for the two cases, i.e., with $V_m = V_{SS}$, and $V_m = V_{DD}$, we have

$$V_{final} = V_{TN} \cdot \left(\frac{C_{gdo} + C_{gd} + C_{pb} + C_{gso} + C_{gs} + C_{mp}}{C_{gdo} + C_{gd}} \right) \qquad for\ V_m = V_{SS}$$

$$V_{final} = V_{TN} \cdot \left(\frac{C_{gdo} + C_{gd} + C_{pb} + C_{gso} + C_{gs} + C_{mp}}{C_{gdo} + C_{gd} + C_{mp}} \right) \qquad for\ V_m = V_{DD}$$

From the above two equations, we can see that for both $V_m = V_{SS}$ and $V_m = V_{DD}$, the numerator remains the same. However, the value of the denominator increases in the case when $V_m = V_{DD}$. Hence, we can make the following inferences:

a)   Keeping C_{mp} constant, the value of V_{final} is higher for the case when $V_m = V_{SS}$, as compared to the value when $V_m = V_{DD}$. This is due to an additional term in the denominator when $V_m = V_{DD}$.

b)   When $V_m = V_{SS}$, V_{final} is directly proportional to C_{mp}.

c)   When $V_m = V_{DD}$, V_{final} is inversely proportional to C_{mp}.

4.4.2   Dependence of V_m on the Detectability Intervals

In the previous analysis for the two voltage strategies, a two vector set sequence was applied to the NOR gate circuit with an FGT in order to excite the fault. The first input vector was an initialization vector (00) that sets the output of the NOR gate to a correct logic '1'. The second input vector (10) tries to set the output of the NOR gate to a logic '0' but an intermediate voltage V_{final} is achieved in case a floating gate transistor is present. In the previous analysis in Chapter 3, it was assumed that the crossing metal wire also receives a rising transition, i.e., a logic level '1', at the same time the second vector is applied to the NOR gate.
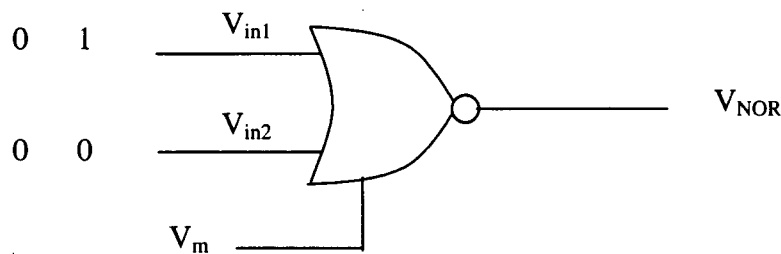
Figure 4.9: Input vectors for the faulty NOR gate

In this sub-section we will analyze four different situations for V_m, viz.,

a) V_m is '0' at the application of first vector, and remains '0' at the application of second vector.

b) V_m is '0' at the application of the first vector, and becomes '1' for the second vector.

c) V_m is '1' at the application of first vector, and remains '1' at the application of the second vector.

d) V_m is '1' at the application of first vector, and changes to '0' for the second vector.

Figure 4.10 shows the plots for the four cases described above for a poly-bulk capacitance of 5 fF.

In Figure 4.10 (a), $V_m = V_{SS}$ when the first vector 00 is applied at the inputs. The floating gate voltage is such that a correct value of 3.3 V is observed at the output. At the application of the second vector '10', V_m remains 0V, and the increase in voltage at the floating gate is not sufficient to turn the faulty transistor ON. Hence, the output voltage does not discharge and an increased V_{final} is stored at the output. In Figure 4.10 (b), V_m changes to 3.3V at the application of the second vector. The floating gate acquires a voltage greater than the transistor threshold and the output node discharges to V_{final}. This is precisely in accordance to the analysis presented earlier.

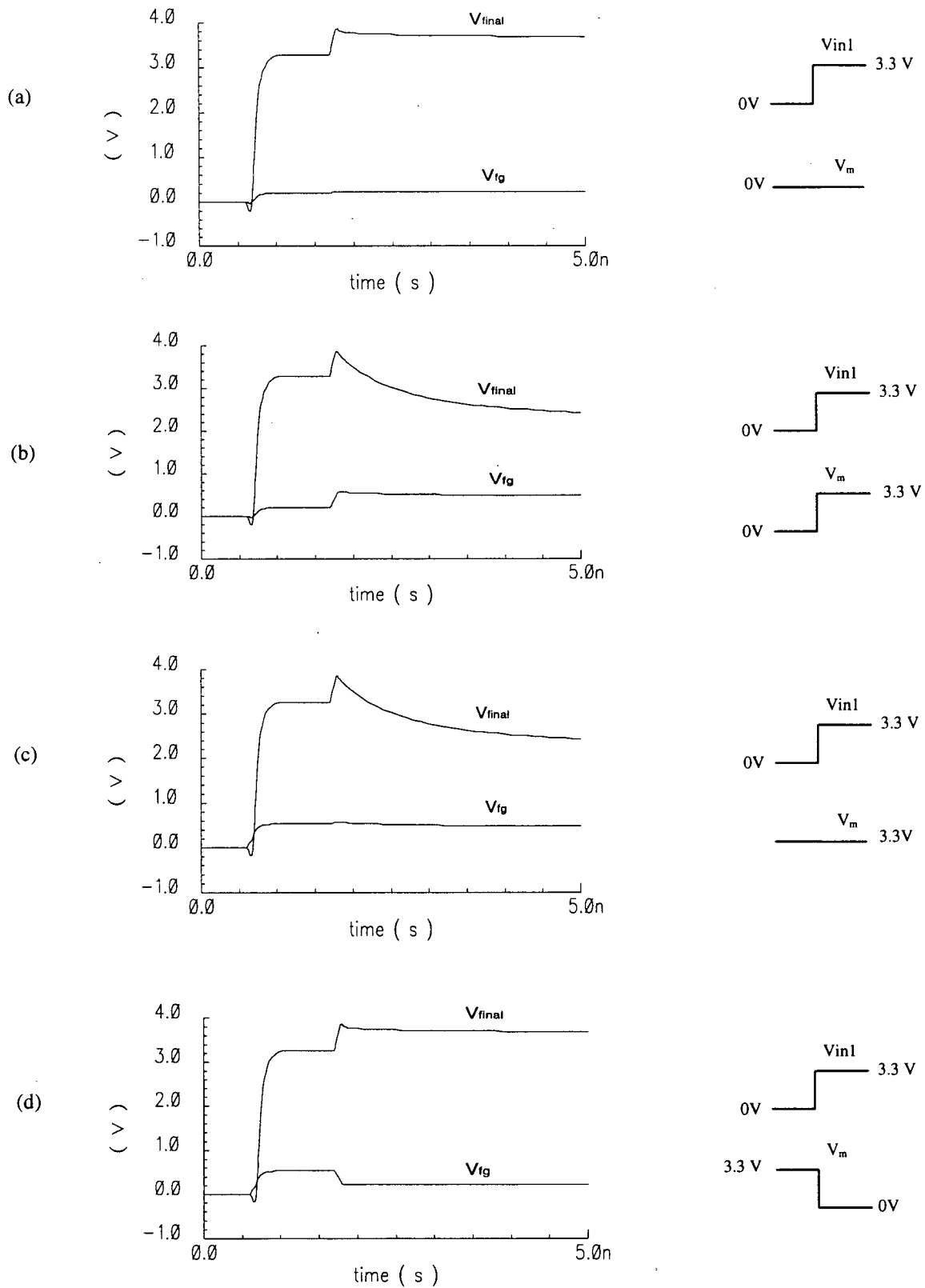Figure 4.10: V_{final} and V_{fg} plots with the application of V_m at different instances

In Figure 4.10 (c), $V_m = V_{DD}$ at the application of first vector. This value remains the same when the second vector is applied. The floating gate acquires a voltage greater than its threshold and the output discharges to a lower V_{final}. In Figure 4.10 (d), V_m drops to V_{SS}. Consequently the value of V_{fg} decreases and the output node does not discharge. Hence, from the simulations in Figure 4.10 we can infer the following: Figure 4.10 (a) and (d) indicate that with $V_m = V_{SS}$, at the application of the second vector, i.e., when V_{in1} transitions from zero volts to V_{DD}, a lower V_{fg} is achieved. Consequently the final value of the output V_{final} , acquires a higher value. Whereas, Figure 4.10 (b) and (c) indicate that a higher V_{fg} is achieved if $V_m = V_{DD}$, when the second vector is applied. This gives a smaller value of V_{final}. Therefore, we can say that for given values of C_{pb} and C_{mp}, the detectability range for the Static Voltage and Dynamic Voltage techniques increases by keeping the metal potential equal to V_{SS} as compared to the case when $V_m = V_{DD}$.

Figure 4.11 shows the increased detectability intervals for the voltage techniques by controlling the metal potential and maintaining it at V_{SS}. The interval for the Static Current technique is not considered, as the testing strategy for the same depends on providing a rising transition at V_m.
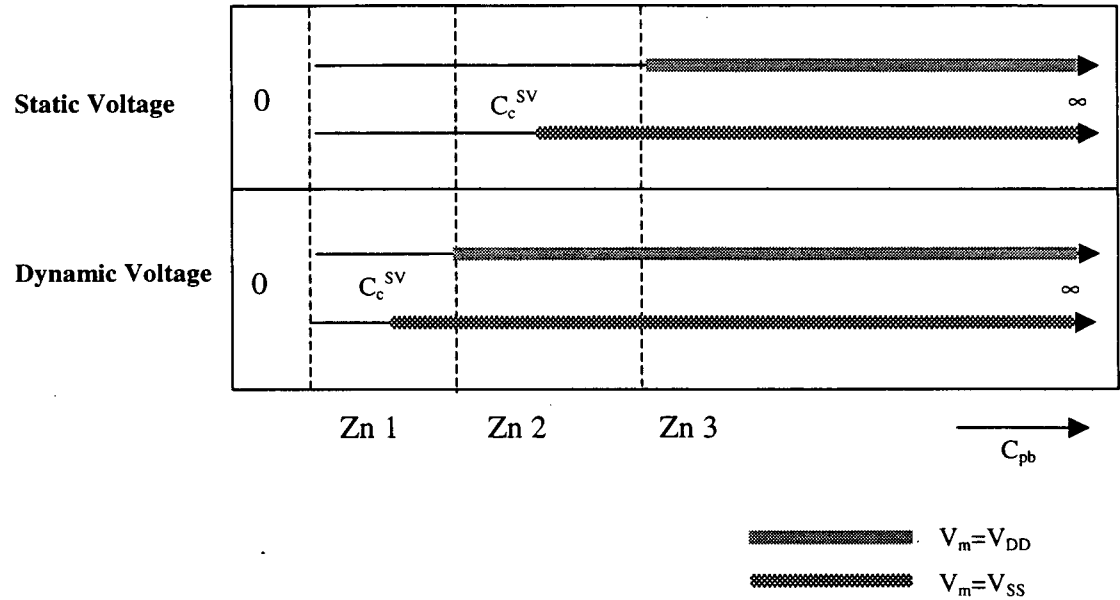
Figure 4.11: Increase in the detectability intervals by controlling V_m to V_{SS} volts.

4.4.3   Dependence of the Detectability Intervals on C_{mp}

The detectability intervals for the voltage and current testing strategies will be considered separately in the following analysis.

4.4.3.1 Detectability Intervals for SV and DV Test Strategies

Consider the following equations

$$V_{final} = V_{TN} \cdot \left(\frac{C_{gdo} + C_{gd} + C_{pb} + C_{gso} + C_{gs} + C_{mp}}{C_{gdo} + C_{gd}} \right) \qquad for\ V_m = V_{SS}$$

and

$$V_{final} = V_{TN} \cdot \left(\frac{C_{gdo} + C_{gd} + C_{pb} + C_{gso} + C_{gs} + C_{mp}}{C_{gdo} + C_{gd} + C_{mp}} \right) \qquad \text{for } V_m = V_{DD}$$

$$\Rightarrow \quad V_{final} = V_{TN} \cdot \left(1 + \frac{C_{pb} + C_{gso} + C_{gs}}{C_{gdo} + C_{gd} + C_{mp}} \right) \qquad \text{for } V_m = V_{DD}$$

From the above equations, it is clear that when $V_m = V_{SS}$, V_{final} is directly proportional to C_{mp}, whereas when $V_m = V_{DD}$, V_{final} is inversely proportional to C_{mp}. Figure 4.12 shows the simulation results for NOR gate of Fig. 3.1 with $C_{pb} = 5fF$ and different values of C_{mp} when $V_m = V_{DD}$.
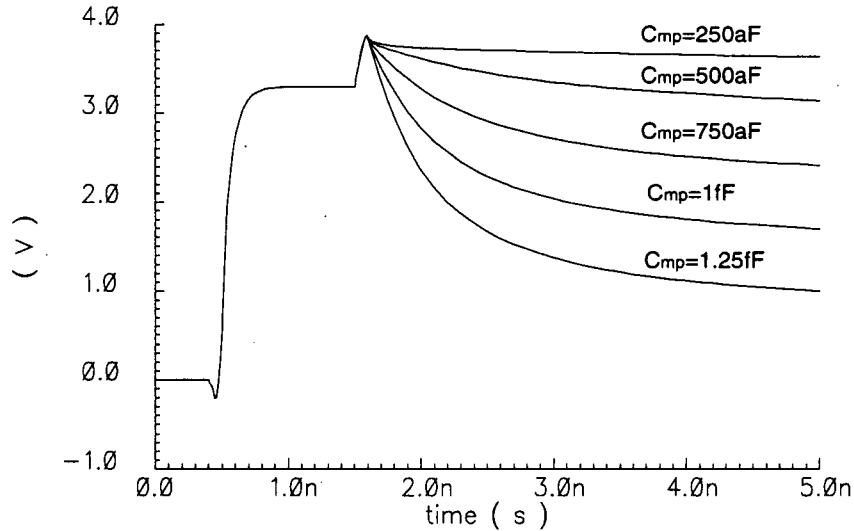
Figure 4.12: V_{final} variation of a faulty NOR gate for different values of C_{mp} ($C_{pb} = 5fF$)

From Figure 4.12, it is evident that a small variation in C_{mp} has a considerable effect on the output voltage V_{final}, of the NOR gate. For higher metal-poly capacitances, a lower value of V_{final} is achieved and vice versa. A lower V_{final} means a lower detectability interval for both SV and DV testing strategies. Hence, with $V_m = V_{DD}$, as the value of C_{mp} increases, the detectability intervals for the voltage strategies decrease. Figure 4.13 illustrates the C_{mp} and C_{pb} relationship curves with V_{final} ($V_m = V_{DD}$), for the Static Voltage technique.

The case is, however, different when $V_m = V_{SS}$. In this case, V_{final} is inversely proportional to C_{mp} and an increased value of C_{mp} means increased detectability intervals for SV and DV strategies. Therefore, an ideal case to achieve maximum coverage for the Voltage strategies would be a high value of C_{mp} with $V_m = V_{SS}$.
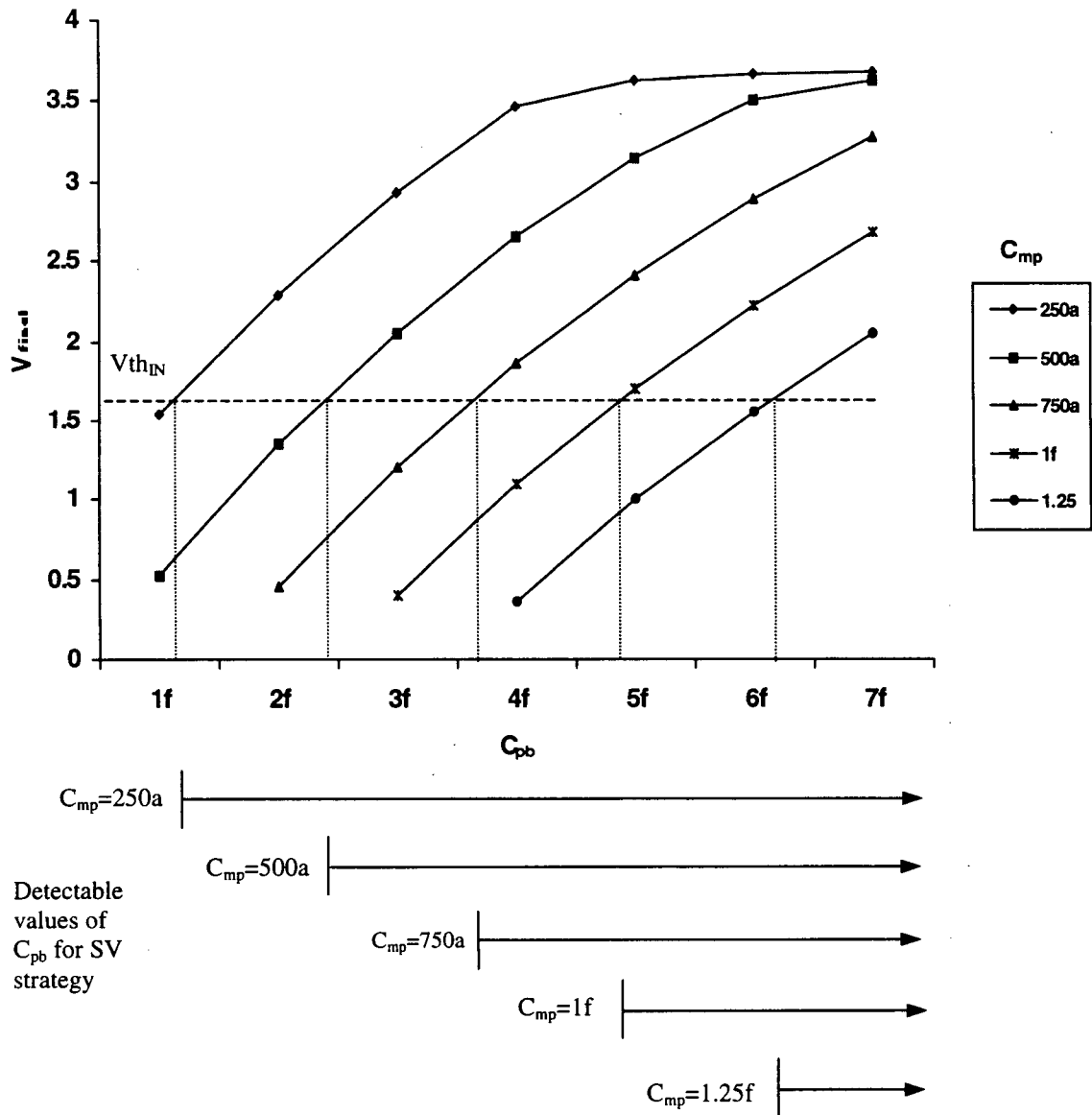
Figure 4.13: V_{final} versus C_{mp} and C_{pb} for faulty NOR gate ($V_m = V_{DD}$)

4.4.3.2 Detectability Intervals for SC Test Strategy

For the Static Current testing technique from simulations, by controlling the metal potential and by giving a rising transition at V_m, a greater C_{mp} ensures a greater voltage induced on the floating gate. Consequently, the conduction of the transistor increases and an increased current flows through the faulty logic gate. Hence the detectability interval increases with an increase in C_{mp}.
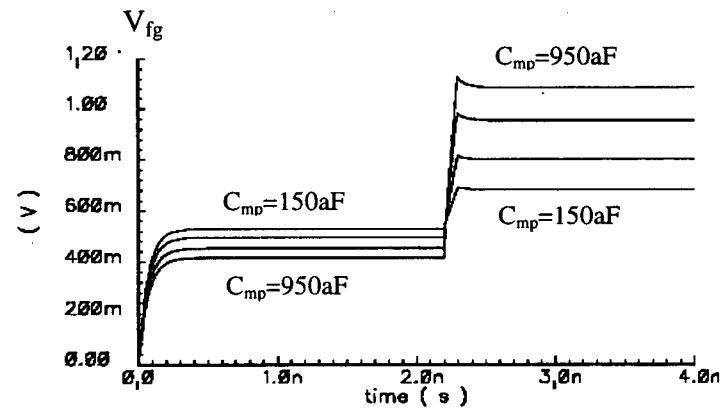
(a)
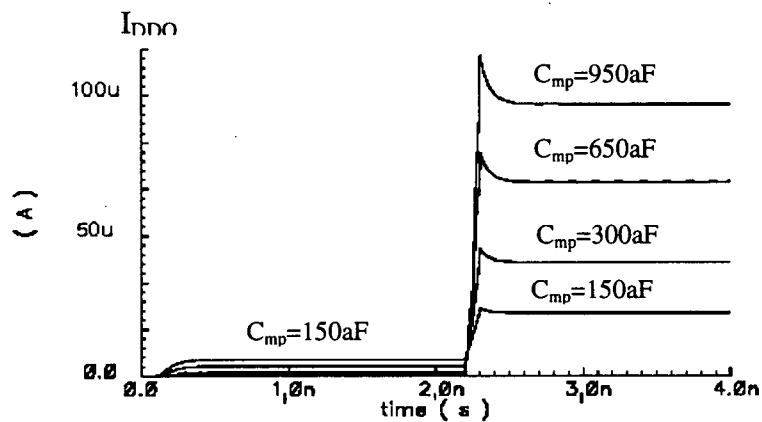
(b)

Figure 4.14: V_{fg} and I_{DDQ} simulation results for different C_{mp} values.

Figure 4.14 (a) shows the voltage acquired by the floating gate for the circuit presented in Fig. 3.5. It clearly appears that when $V_m = V_{SS}$, V_{fg} acquires a larger value with $C_{mp}=150aF$ as compared to $C_{mp} = 300aF$, $650aF$, $950aF$, etc., i.e., the higher the value of C_{mp} the lower the value of V_{fg} (refer to the first half of the simulation). When V_m rises to V_{DD} (the second half of the simulation), the voltage on the floating gate also increases, i.e., the higher the C_{mp}, the higher the V_{fg}.

Figure 4.14 (b) shows the I_{DDQ} current flowing through the floating gate transistor. The plots indicate that when $V_m = V_{SS}$, the current is inversely proportional to C_{mp}. This is because the floating gate acquires a larger voltage with a smaller C_{mp} when $V_m = V_{SS}$. But when V_m jumps to V_{DD}, the current becomes directly proportional to C_{mp}. Hence, for the proposed technique for SC test strategy (by giving a rising transition at V_m, as per section 3.2.3), the detectability interval increases with an increase in C_{mp}.

Figure 4.15 depicts that as C_{mp} is increased, an increased C_{pb} value is required to maintain the same amount of I_{DDQ} current. Hence, a higher detectability interval is achieved for the Static Current testing technique when C_{mp} is increased.
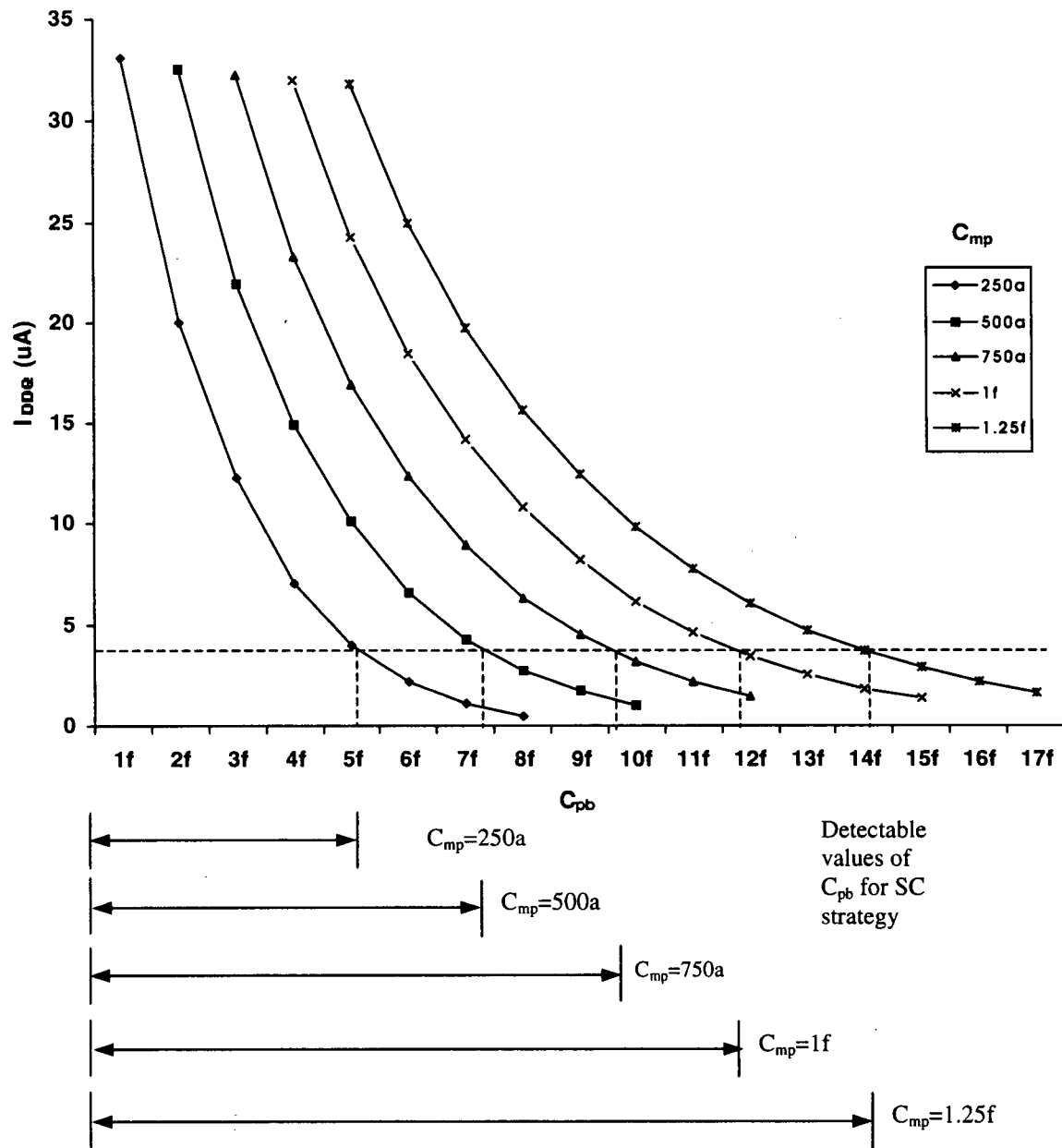
Figure 4.15: I_{DDQ} versus C_{pb} for varying C_{mp} of a faulty NOR gate.

The analysis for the effects of V_m and C_{mp} can be summarized as follows. For V_m, we can infer that by keeping the metal potential V_m at V_{SS} increases the fault detectability intervals for the Static Voltage and Dynamic Voltage test strategies (section 4.4.2). As for the Static Current strategy, applying a rising transition at V_m provides a method to monitor the I_{DDQ} current in the faulty transistor (described in section 3.3).

For the capacitance C_{mp}, Section 4.4.3 suggests that with $V_m = V_{DD}$, an increase in C_{mp} decreases the detectability intervals for the DV and SV testing techniques, while the intervals increase for the same with an increase in C_{mp} when $V_m = V_{SS}$. As for the Static Current technique, a higher detectability interval is achieved for the Static Current testing technique when C_{mp} is increased with a rising transition at V_m. The results for V_m and C_{mp} are summarized in table 4.1.

No.	Test Strategy	V_m	C_{mp}	Detectability
1.	Static Voltage	V_{DD}	↑	↓
		V_{SS}	↑	↑
2.	Dynamic Voltage	V_{DD}	↑	↓
		V_{SS}	↑	↑
3.	Static Current	V_{DD}	↑	↑
		V_{SS}	↑	↓

Table 4.1   Summary of the results for V_m and C_{mp}

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this thesis, the detection of floating gate faults is studied using Static Voltage, Dynamic Voltage and Static Current strategies. It is shown that the behavior of the defect depends on two classes of parameters, i.e., the predictable and the unpredictable parameters. Predictable parameters include both technological information from the process and topological information from layout. The unpredictable parameters include the random information coming from the size, location and nature of the fault. Furthermore, it is shown that the metal-poly capacitance C_{mp} and the metal potential V_m together with the unpredictable poly-bulk capacitance C_{pb}, play an extremely important role in determining the final output voltage and the steady state current of a faulty gate.

We demonstrated that the three test techniques (namely, the SV, DV and SC testing strategies) are each able to detect floating gate faults for a given range of the unpredictable parameter. The Static Current strategy presents a complementary interval with respect to Static and Dynamic Voltage strategies. It is shown that a combination of a voltage and current test strategies can ensure 100% detection of the floating gate defect.

The effect of initial charge on the floating gate was also analyzed. It is shown that with an increase in the initial charge at the floating gate, the detectability intervals for the voltage strategies decrease, while the detectability interval for the current strategy increases. This again suggests a combination of both the current and voltage testing strategies to ensure a complete coverage of the floating gate faults.

Similarly, the effect of the overlapping metal potential and the corresponding metal-poly capacitance is also presented in detail. It is shown that keeping the metal potential at V_{SS} increases the fault detectability intervals for the Static Voltage and Dynamic Voltage testing strategies. For the metal-poly capacitance, an increase in the same decreases the detectability intervals for the DV and SV testing strategies when $V_m = V_{DD}$, while the intervals increase for the SC strategy (using the proposed technique) with an increase in C_{mp}. It can be therefore, concluded that to achieve complete coverage of the floating gate fault, it is mandatory to conduct both current and either of the voltage testing strategies.

5.2   Future Work

The results in this dissertation strongly suggest that the detectability intervals are adversely affected by the initial charge on the floating gate transistor. Though it has been shown that no matter how much initial charge is present at the FGT, a combination of both the current and voltage strategies provides 100% fault coverage. However, for the cases when it is not possible to conduct both the tests due to the classical cost / efficiency trade off, the amount of initial charge on the gate becomes an extremely important factor in determining the detectability interval of the floating gate defect coverage. Further work needs to be done in this regard to determine the initial charge on the gate.

A new technique for I_{DDQ} current monitoring was presented in this thesis assuming that the potential of the crossing metal wire is controllable. However, it was not shown how could that be achieved. Obviously, this is another design area that needs more investigation.

6. References

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Appendix A: Model Parameters for the Transistors Used in Simulations

```
# OPT("/I7/M0","??")
ids = -861.1e-15     vgs = -3.3          vds = -1.193e-9
vbs = -1.193e-9      vth = -863.8e-3
vdsat = -2.001       gm = 245.4e-15      gds = 212e-6
gmbs = 51.09e-15     gameff = 390.6e-3
betaeff = 87e-6      cbd = 2.091e-15     cbs = 2.091e-15
cgs = 1.624e-15      cgd = 1.624e-15
cgb = 199.1e-18      ron = 1.385e3       id = -861.1e-15
ibulk = 11.34e-21    pwr = 1.027e-21
gmoverid = -285e-3   isub = 0            stress = 0
age = 0              he_vdsat = 0
```

```
# OPT("/I7/M2","??")
ids = -25.19e-18     vgs = -1.193e-9     vds = -886.3e-3
vbs = -1.193e-9      vth = -830.8e-3
vdsat = -35.13e-3    gm = 635.4e-18      gds = 23.78e-18
gmbs = 202.4e-18     gameff = 390.6e-3
betaeff = 124.4e-6   cbd = 1.526e-15     cbs = 2.091e-15
cgs = 325.9e-18      cgd = 325.9e-18
cgb = 1.48e-15       ron = 35.19e15      id = -10.03e-15
ibulk = 10e-15       pwr = 8.885e-15
gmoverid = -25.23    isub = 0            stress = 0
age = 0              he_vdsat = 0
```

```
# OPT("/I7/M1","??")
```

```
ids = 2.442e-12      vgs = 0              vds = 2.414
vbs = 0              vth = 446.3e-3
vdsat = 34.67e-3     gm = 59.17e-12       gds = 3.861e-12
gmbs = 21.99e-12     gameff = 512.9e-3
betaeff = 465.5e-6   cbd = 319.5e-18      cbs = 629.6e-18
cgs = 369.5e-18      cgd = 369.5e-18
cgb = 1.03e-15       ron = 988.6e9        id = 2.452e-12
ibulk = -10e-15      pwr = 5.918e-12
gmoverid = 24.23     isub = 0             stress = 0
age = 0              he_vdsat = 0


# OPT("/I7/floating_nmos","??")
ids = 280.3e-9       vgs = 480.8e-3       vds = 2.414
vbs = 0              vth = 446.3e-3
vdsat = 34.67e-3     gm = 6.793e-6        gds = 443.3e-9
gmbs = 2.021e-6      gameff = 512.9e-3
betaeff = 465.5e-6   cbd = 319.5e-18      cbs = 629.6e-18
cgs = 369.5e-18      cgd = 369.5e-18
cgb = 826.7e-18      ron = 8.61e6         id = 280.3e-9
ibulk = -10.02e-15   pwr = 676.6e-9
gmoverid = 24.23     isub = 0             stress = 0
age = 0              he_vdsat = 0
```

Appendix B: Hspice Netlist

The Hspice netlist for the Faulty NOR gate in Figure 3.1:

```
* # FILE NAME: /NFS/ABAN/INT1-
6/HOME2/SUMBALR/CAD/CDS/CMOSIS5/SIMULATION/
* FG_nr2_layout_sim_org2/spectreS/schematic/netlist/
* FG_nr2_layout_sim_org2.C.raw
* Netlist output for spectreS.
* Generated on May 11 22:54:07 1998


* global net definitions
.GLOBAL vdd\! vss\!


simulator lang= spectre
* File name:
floating_Gate_simualtion_FG_nr2_layout_sim_org2_schematic.s.
* Subcircuit for cell: FG_nr2_layout_sim_org2.
* Generated for: spectreS.
* Generated on May 11 22:54:09 1998.




* vpwl Instance V5 = spectreS device v5
v5 (ip1 vss\!)  vsource  type= pwl wave= [ 400e-12 3.3 500e-12
0.0 1.5e-9 0.0
+1.6e-9 3.3  ]


* vpwl Instance V4 = spectreS device v4
v4 (net10 vss\!)  vsource  type= pwl wave= [ 400e-12 0.0 500e-12
0.0 1.5e-9
```

```
+0.0 1.6e-9 3.3   ]


* hnr2_type2 Instance I7 = spectreS device xi7

* Instance of Lib: FloatingGates,  Cell: hnr2_type2,  View:
schematic

xi7 (vdd\! vss\! vfg ip1 in2 output) hnr2_type2_g1


* tiedown Instance I4 = spectreS device xi4

* Instance of Lib: cmosis5,  Cell: tiedown,  View: schematic

xi4 (vss\!) tiedown_g2


* vdc Instance Vin2 = spectreS device vin2

vin2 (in2 vss\!)  vsource  type= dc dc=0.0


* vdc Instance V1 = spectreS device v1

v1 (vdd\! vss\!)  vsource  type= dc dc=+3.30000000E+00


* cap Instance C11 = spectreS device c11

c11 (vfg net10)  capacitor c=750e-18 m=1.0


* cap Instance Cgd = spectreS device cgd

cgd (output vfg)  capacitor c=100e-18 m=1.0


* cap Instance Cpb = spectreS device cpb

cpb (vfg vss\!)  capacitor c=+5.00000000E-15 m=1.0
ic=+0.00000000E+00


simulator lang= spice
```

simulator lang= spectre

simulator lang= spice

*Model definitions

* File name: cmosis5_tiedown_schematic.s.

* Subcircuit for cell: tiedown.

* Generated for: spectreS.

* Generated on May 11 22:54:09 1998.

simulator lang= spectre

* terminal mapping: gndPoint = gndpoint

subckt tiedown_g2 gndpoint

* resistor Instance R3 = spectreS device r3

r3 (0 gndpoint) resistor r=1.0 m=1.0

simulator lang= spice

simulator lang= spectre

* End of subcircuit definition.

ends tiedown_g2

simulator lang= spice

* File name: FloatingGates_hnr2_type2_schematic.S.

* Subcircuit for cell: hnr2_type2.

* Generated for: spectreS.

```
* Generated on May 11 22:54:08 1998.


simulator lang= spectre
* terminal mapping: VDD! = vdd\!
*                   VSS! = vss\!
*                   fin = fin
*                   ip1 = ip1
*                   ip2 = ip2
*                   op = op
subckt hnr2_type2_g1 vdd\! vss\! fin ip1 ip2 op


* nfet3 Instance floating_nmos = spectreS device mfloating_nmos
mfloating_nmos (op fin vss\! vss\!)   CMOSN   region= triode
w=800e-9 l=600e-9
+as=+8.00000000E-13 ad=+8.00000000E-13 ps=+3.60000000E-06
pd=+3.60000000E-06
+nrd=+1.25000000E+00 nrs=+1.25000000E+00 m=1.0


* nfet3 Instance M1 = spectreS device m1
m1 (op ip2 vss\! vss\!)   CMOSN   region= triode w=800e-9 l=600e-9
+as=+8.00000000E-13 ad=+8.00000000E-13 ps=+3.60000000E-06
pd=+3.60000000E-06
+nrd=+1.25000000E+00 nrs=+1.25000000E+00 m=1.0


* pfet3 Instance M2 = spectreS device m2
m2 (op ip1 net14 vdd\!)   CMOSP   region= triode w=1e-6 l=600e-9
+as=+1.00000000E-12 ad=+1.00000000E-12 ps=+4.00000000E-06
pd=+4.00000000E-06
+nrd=+1.00000000E+00 nrs=+1.00000000E+00 m=1.0
```

```
* pfet3 Instance M0 = spectreS device m0
m0 (net14 ip2 vdd\! vdd\!)   CMOSP  region= triode w=1e-6 l=600e-
9
+as=+1.00000000E-12 ad=+1.00000000E-12 ps=+4.00000000E-06
pd=+4.00000000E-06
+nrd=+1.00000000E+00 nrs=+1.00000000E+00 m=1.0
simulator lang= spice




simulator lang= spectre
* End of subcircuit definition.
ends hnr2_type2_g1
simulator lang= spice




simulator lang= spectre
simulator lang= spice


* Include files



save xi7.m45:vth
save xi7.m47:vth
save xi7.m43:vth
save xi7.m41:vth
save xi7.mfloating_nmos:cbs
save xi7.mfloating_nmos:cgs
save xi7.mfloating_nmos:cgd
save xi7.mfloating_nmos:cgb
```

```
save xi7.mfloating_nmos:cbd

save xi7.mfloating_nmos:vth

save xnmosvin1:vth



*Only one library can be selected in a time.

*

*

*#define anyDesiredLibrary

* n5bo being the default


#define n5bo


*#include anyDesiredModelFile

* There are cmosis5.level3 and cmosis5.bsim1

* cmosis5.level3 being the default


#include "cmosis5.level3"


*#undef theUsedLibrary


#undef n5bo


simulator lang= spectre


* End of Netlist

*

simulator lang=spectre

simOptions options

*        rawfmt=psfbin rawfile="%C:h/../psf"
```

```
+          currents=all
+          gmin=  1.00000000E-15
+          reltol=  1.00000000E-03
+          scale=   1.0000000
+          scalem=   1.0000000
+          vabstol=  1.00000000E-06
+          iabstol=  1.00000000E-12
+          temp=   27
+          tnom=   27
+          rforce=   1.0000000
+          maxwarns=    5
+          digits=    5
+          cols=    80
+          pivrel=  1.00000000E-03
+          ckptclock= 1800
+          save=allpub
modelParameter   info   what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
timeSweep tran  stop= 5.00000E-09
+          write="spectre.ic"
+          writefinal="spectre.fc"
+          annotate=status
+          compression=no
+          maxiters=    5
finalTimeOP info what=oppoint where=rawfile
```