Built-in Jitter Test Schemes for Mixed-Signal Integrated Circuits

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Abstract

Recent years have seen an unparalleled growth in the speed and complexity of VLSI circuits. Analog and mixed-signal circuits are going through a resurgence and continue to pose new challenges to VLSI test engineers. The state-of-the-art in the mixed-signal and analog test domain is to use application-specific test methodologies to tackle individual problems. The same is true for testing the high-speed clock signals used in present day integrated circuits (ICs) for their analog attributes. Jitter is one of the ways of quantifying the accuracy of a clock signal. Present day digital automatic test equipment (ATE) does not possess enough resolution to be suitable for jitter tests of high-speed clock signals such as SONET's (Synchronous Optical Network) 155.52 MHz and 622.08 MHz. In this thesis, the jitter test problem of high-speed clocks is approached with a built-in self-test (BIST) perspective. A BIST scheme is presented for the jitter tolerance test of clock and data recovery units typically found in data transceiver ICs. A cost-effective scheme based on the utilization of existing components for test purposes is presented. Some possible variations of the presented scheme are discussed. A second BIST scheme, focused on jitter testing of clock signals in a sampling-based digital signal processing (DSP) environment, is presented. Again, the focus is on the re-use of typically existing blocks on such ICs.

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Acknowledgments

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Kamal Dalmia

Chapter 1
Introduction

Testing for manufacturing defects and fault diagnosis are vital for the quality assurance of electronic components. With the rapid advancement in integrated circuit technology, these aspects have become critical in determining the overall cost of the components and systems. Over the years, testing has become a major factor in determining the *time to market* for Very Large Scale Integration (VLSI) circuits. Historically, the focus of the test community has been biased towards digital circuits due to their sheer abundance. However, this scenario is changing rapidly with the increasing integration of analog and digital functions on single integrated circuits. The class of integrated circuits (ICs) with both analog and digital components is commonly referred to as mixed-signal. This integration of analog and digital components is posing new challenges to VLSI test engineers. The primary reason for this is the fact that the automatic test equipment (ATE) that has been traditionally employed and designed for testing purely digital circuits is incapable of meeting the stringent demands of mixed-signal testing [Meh93]. In recent years, some ATE vendors have introduced test equipment with mixed-signal test capabilities. However, most of these testers are either incapable of meeting the application-specific requirements of analog components, or are too expensive to be cost-effective in a volume-production environment [Ton93]. Other factors that render mixed-signal testing a difficult task are the limited pin counts of chips and the restricted controllability and observability of internal nodes. The recognition of these

difficulties has caused IC designers to more seriously consider test issues and adopt *design-for-testability* techniques [Bar87].

Built-in self-test (BIST) is a well known design for testability technique [Ton93] [Ter93]. BIST techniques alleviate some of the problems associated with internal testing. A typical BIST methodology involves the generation of test stimuli and the evaluation of test responses by adding special circuitry to the basic IC. Fig. 1.1 depicts the basic methodology of a BIST scheme.

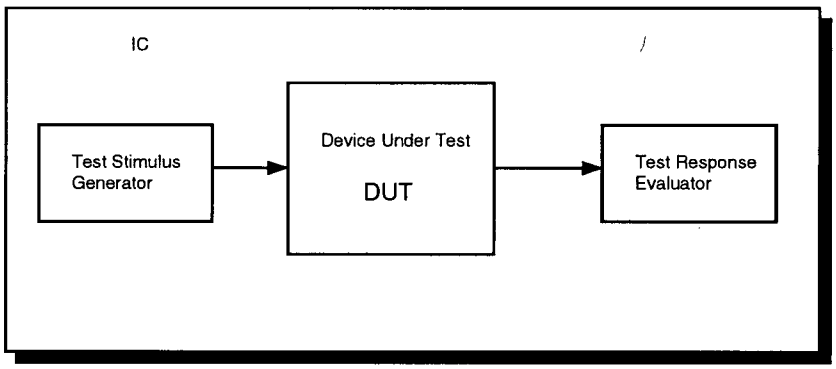

Figure 1.1 The BIST methodology.

The test stimulus and the test response evaluator are often realized using linear feedback shift registers (LFSR) [Bar87]. BIST techniques for testing digital circuits have reached a level of sufficient maturity. However, analog and mixed-signal BIST research is still in its infancy. Present day BIST techniques for analog and mixed-signal ICs are essentially *application specific*, i.e., the test circuitry is designed for testing a specific category of circuits and cannot be employed for other circuits in general. The significant advantages of a BIST scheme over the conventional ATE based schemes are the following :

a. Low cost : If a BIST scheme is carefully designed with optimum area overhead, the result is substantial savings in the overall cost of the testing. The savings in the total cost, in turn, result from the savings in the external test equipment and the overall test time.

b. Test time : In general, the external test equipment requires a longer setup time than the circuitry present on the IC. In the case of a BIST scheme, the test circuitry is present on the IC itself and hence results in a shorter test time.

c. Cable parasitics : In high-speed testing, the cables that run from the tester to the DUT can cause significant parasitics to alter the results of a test. It is always desirable to keep the cable lengths to a minimum. The BIST technique alleviates this problem to a significant extent as the high-speed paths are usually on the chip itself.

d. Upgrade with technology : As the speed of the ICs advances, faster testers are required to meet the demands of newer generation of ICs. In a BIST scheme, the technology and the speed of the test circuitry advances with that of the DUT, resulting in savings in the capital expenditure of tester upgrades.

Though the popularity of the BIST methodology is growing at a fast rate, test engineers often have to tackle the limitations of the BIST methodology. The significant limitations of the BIST scheme are the following :

a. Area-overhead : The test circuitry added to the basic circuit is duplicated on every IC for a BIST scheme. If the test area overhead is excessive, the product yield may drop resulting in higher overall cost of the IC.

b. Performance degradation : In some cases such as high-speed digital circuits and analog circuits, added circuitry may introduce noise into the high-speed paths resulting in an

overall performance degradation.

c. Limited test capabilities : Due to the limitation of the test resources that may be added to an IC, in most BIST cases, only a limited set of tests may be performed as compared to the tests possible with ATEs.

Clocking is an integral part of all synchronous circuits. Clock accuracy is crucial in many computer, telecommunication, and signal processing applications. The clock accuracy, in particular with respect to the occurrence time of clock edges, is becoming increasingly difficult to achieve with increasingly fast clock rates. The timing precision required for the clocks in the range of megahertz is of the order of picoseconds. Various attributes such as frequency stability and skew are used to quantify the accuracy of clock signals. One of the standard ways of quantifying the accuracy of a clock signal is through jitter specifications. Jitter is defined as the short-term variations of the significant instants of a digital signal from their ideal position in time [Syn94]. Like other noise forms, jitter can affect system performance, e.g., by introducing bit errors in a digital telecommunication application or by degrading the signal to noise ratio (SNR) in a sampling-based system. With the advent of high-speed information-based systems, there is increasing interest in the systematic measurement of jitter. With digital systems operating at a speed of hundreds of megahertz, commonly available ATEs prove to be incapable of being effectively utilized for testing telecommunication ICs as they are limited to 100–200 MHz clock speeds [Hot92].

Another jitter related problem, mainly associated with clock and data recovery applications, is the production-stage testing for jitter tolerance of clock recovery units (CRU). Common applications which find widespread use of CRUs are data telecommunication ICs,

disk drive storage systems, compact disk players and satellite link communications [Ram94] [Wol91]. Jitter tolerance is a receiver's ability to recover data without errors in the presence of jitter. In general, a typical digital ATE is incapable of generating jittered data with the required precision (picosecond range for SONET/SDH [Syn94]). Hence, dedicated jitter generators and analyzers are used for jitter tolerance tests. Most dedicated jitter generators are designed for characterization tests and are expensive and unsuitable for production-stage testing due to long setup and operational delays. Hence, neither ATEs nor dedicated characterization test equipment provide for low cost and efficient volume-production testing. Moreover, there is no published BIST technique for jitter tolerance testing.

1.1 Scope of Thesis

Recognizing the limitations of generic digital ATE's with respect to the measurement of analog signals in general and the clock attributes in particular, this thesis approaches the jitter test problem from a BIST perspective. Most digital integrated circuit designers are familiar with the time domain representation of jitter. The time domain measurements are usually easier and faster than the frequency domain measurements. However, time domain treatment is often insufficient for phase locked loops (PLLs). PLLs are the most commonly used components in clock generation and clock recovery applications. For PLLs, some particular frequencies may be more offensive than others. Due to this, the study of the spectral content of clock signals is important. Hence, a frequency domain approach has been adopted in this thesis to tackle the problem.

As a first step towards the attempt to solve the jitter test problem, a comprehensive overview of jitter is provided in Chapter 2. The formal definition of jitter is presented,

followed by a discussion on the sources and effects of jitter in sampling-based environments and high-speed data transceiver ICs. Since modern high-speed data telecom equipment must comply with international standards and specifications to ensure compatibility between the equipment manufactured by different vendors and subsequent successful implementation of networks, IC manufacturers must test their components against a variety of applicable jitter specifications. Test engineers dealing with jitter must have a thorough understanding of the specifications. Recognizing this, an overview of Synchronous Optical Networks (SONET) specifications is also presented in this chapter.

Chapter 3 describes a novel BIST scheme for the jitter tolerance test of clock and data recovery units (CRUs) commonly found in the receiver section of high-speed data transceiver ICs. The BIST scheme is designed to test a CRU against SONET jitter tolerance specifications. An overview of typical SONET nodes is presented. Following this, conventional jitter tolerance test schemes are discussed. The requirement that a CRU be tested for jitter tolerance in the presence of a broad range of jitter amplitudes and frequencies make the "traditional" jitter tolerance test very time-consuming and cumbersome. The presented BIST scheme effectively tackles the problem. The flexibility of the methodology leads to some variations in implementation which are discussed at the end of the chapter.

With ever-increasing clock speeds, the jitter constraints become increasingly stringent. To measure low amounts of jitter the test equipment must have superior resolution. A direct implication of this requirement is high cost. Chapter 4 presents a BIST scheme for jitter measurement of clock signals in a sampling based IC. The presented scheme is applicable to the class of circuits which constitute a sampling circuit such as an analog-to-digital convertor

(ADC) and a digital signal processing (DSP) core capable of performing Discrete Fourier Transforms (DFT). Mathematical analysis leading to the concept underlying the BIST scheme is also presented.

The BIST schemes presented in this thesis are a step towards increasing the awareness and recognition of the feasibility of the 'self-test' philosophy in those applications which are traditionally considered unsuitable for a self-test approach. This thesis addresses various aspects of jitter testing, such as, jitter measurement and the jitter tolerance test, but the problem is by no means completely solved. Some possible variations of the presented scheme are mentioned for future work, along with conclusions, in Chapter 5.

Chapter 2
Jitter

2.1 Definitions

Jitter is defined as the short term variation of the significant instants of a digital signal from their ideal position in time [Syn94]. In other words, jitter is the short term variation of the significant edges of a digital signal from an ideal clock running at an average rate equal to that of the signal itself [You94]. Jitter is also defined as undesired phase variation of the signal, or in other words, as the phase noise [You94]. Fig. 2.1.1 illustrates the concept of jitter in the time domain.

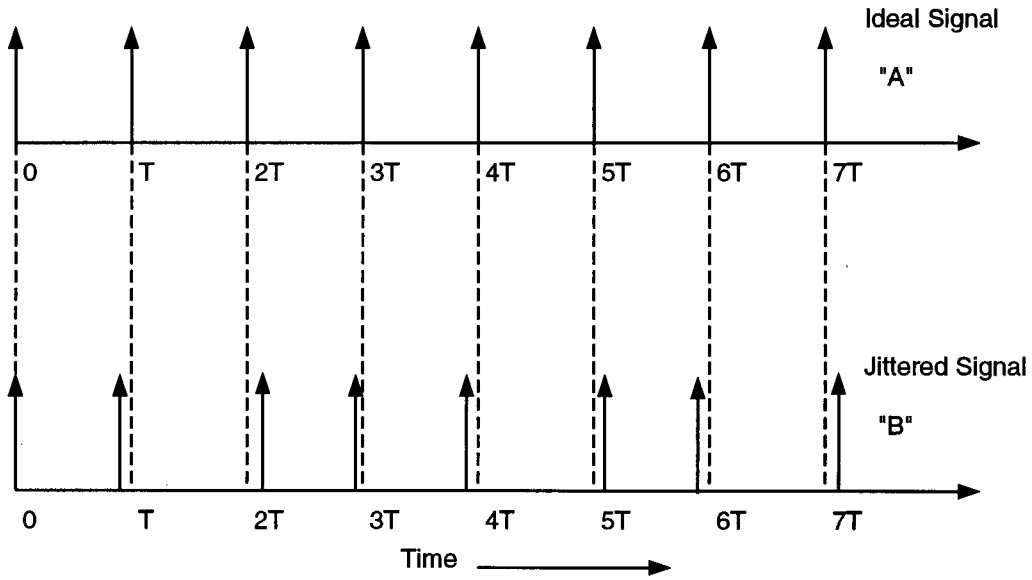

Figure 2.1.1 Illustration of jitter in the time domain.

In Fig. 2.1.1, 'A' represents an ideal pulse stream and 'B' represents the jittered version of signal 'A'. Significant edges of the signal 'A' are ideally spaced in time while the edges of signal 'B' are shifted from their ideal position and hence said to be jittered.

2.2 Effects of Jitter

Like other forms of noise, jitter is undesirable due to its negative effect on a system's performance. In a typical digital telecommunication system, bit streams are transmitted serially. Most often, it is not practical to transmit a reference clock along with the data. Hence, a receiver is required to recover the clock from the received data and re-time the data using the recovered clock. In real systems, the received data is jittered due to various stages of regeneration and the non-ideal behavior of network components. The jitter on the received data may lead to bit-errors during the recovery. If the number of the bits in error is beyond the capabilities of error detection and correction circuits, the data becomes useless.

In a sampling-based system which deploys the conversion of continuous time analog signals into discrete time signals, jitter on the sampling clock leads to the addition of random noise to the discretised signal. Such noise degrades the signal-to-noise ratio of the signal. The major factors which limit the accuracy and speed of analog-to-digital convertors are jitter, harmonic distortion, and non-linearity [Shi90]. However, some other factors such as temperature may be important in some particular applications. Hence, the control and measurement of jitter is extremely important in such systems.

2.3 Sources of Jitter

2.3.1 Telecom Systems

The primary sources of jitter in a digital telecommunication system are regenerators and multiplexors [Tri89]. In a typical data transceiver, a 'clean' clock signal is synthesized by the transmitter section. This clock signal is used to transmit the data in a bit-serial manner. The transmitted data, on its way to the receiver, passes through various regenerators and multiplexors which introduce jitter into the signal. Commonly available regenerators use clock extraction and re-transmission using the extracted clock [Tri89]. The process of clock extraction and re-transmission is rather imperfect and involves timing non-idealities. Due to cascading of regenerators in most systems, jitter accumulation takes place and results in a higher net jitter faced by the receiver.

In the preceding discussion it was mentioned that the signal at the output of a transmitter is a 'clean' signal. However, this does not imply that the transmitted signal is jitter-free. Instead, it means that the signal contains acceptably low amounts of jitter. Standards such as ANSI T1.105.03–1994 [Syn94] specify the limits of acceptable jitter at the output of transmitters. Typically, transmitters use some form of clock multiplier or synthesizer that generates a line rate clock using a phase-locked loop (PLL) and a crystal reference. PLL clock synthesizers are prone to introduce their internal phase noise to the generated clock signal in the form of jitter. This property is often referred to as 'jitter generation'. Primary sources of a PLL's internal phase noise are the input phase noise and the voltage controlled oscillator (VCO) phase noise. A comprehensive treatment of PLL internal noise can be found in [Wol91].

2.3.2 Sampling Systems

A sampling system typically comprises an analog-to-digital convertor, an analog signal source, and a digital signal processing circuit. Most analog-to-digital convertors can be thought of as a combination of a sampling circuit, a quantization circuit, and a digitization circuit. In such a sampling system, the primary sources of timing jitter are – (a) the sampling clock jitter, (b) the sampling circuit jitter and (c) the input signal jitter [Shi90]. As described earlier, when a clock is synthesized using a PLL, it constitutes the internal phase noise of the PLL in the form of jitter. When such a clock is used in a sampling system, it is viewed as the sampling clock jitter ((a) above). With a jittered sampling clock, the analog signal is sampled at non-ideal time instants. This leads to unintended amplitudes of the analog signal being recorded and hence results in amplitude noise being added to the signal. Thermal noise in the sampling circuit also leads to inaccuracy in timing and subsequently to further jitter being added to the signal. This form of noise is referred to as the sampling circuit jitter ((b) above). Normally, the signal being sampled has its own jitter and is reffered to as the input signal jitter ((c) above). Though band-limiting is inherent in sampling and it reduces the signal generator jitter (input signal jitter), substantial jitter can be contributed to the overall jitter by this component. Shinagawa et al. [Shi90] present a method for separately estimating the three forms of jitter in a sampling system.

2.4 Jitter Characterization

Jitter is a form of noise and is generally random in nature. Some forms of jitter such as pattern dependent jitter [Wol91] in clock recovery applications are input specific. However,

since a typical input to such systems is often random or pseudo-random serial data, pattern dependent jitter can also be classified as random jitter. Similar to many noise forms, the Gaussian distribution function is the most commonly used function to represent jitter for analytical purposes [Shi90][Wag91][Wag90].

The jitter tolerance specification for SONET network elements is an exception to the practice of using a Guassian distribution function. SONET jitter tolerance specifications require that the clock signal be modulated by a sequence of single frequency sinusoids be used for testing as opposed to a signal containing broadband noise. The jitter tolerance specifications for SONET are discussed in detail in the next section.

2.5 Jitter Specifications

SONET is a digital hierarchy interface based on a basic unit of 51.84 Mbps as the transmission rate. SONET was initially deployed in North America. Later on, Synchronous Digital Hierarchy (SDH) was introduced as an international version of SONET. SDH is designed to support the European digital data networks. SDH provides for traffic interfaces which are vendor-independent. The basic rate of 51.84 Mbps is known as OC-1 or STS-1 (Optical Carrier at level 1 or Synchronous Transport Signal at Level 1). Subsequently, the higher rates are known as OC-N or STS-N [Fer94] [Hot92]. At 155.52 Mbps (OC/STS-3), the jitter specifications are defined for optical and electrical interfaces. For higher rates, they are defined for optical interfaces only. The following is an overview of SONET/SDH jitter specifications for a network element.

2.5.1 Jitter Tolerance

Input jitter tolerance is the peak-to-peak (p-p) amplitude of sinusoidal jitter applied on the input of an OC-N equipment interface that causes an equivalent 1 dB optical or electrical power penalty [Syn94].

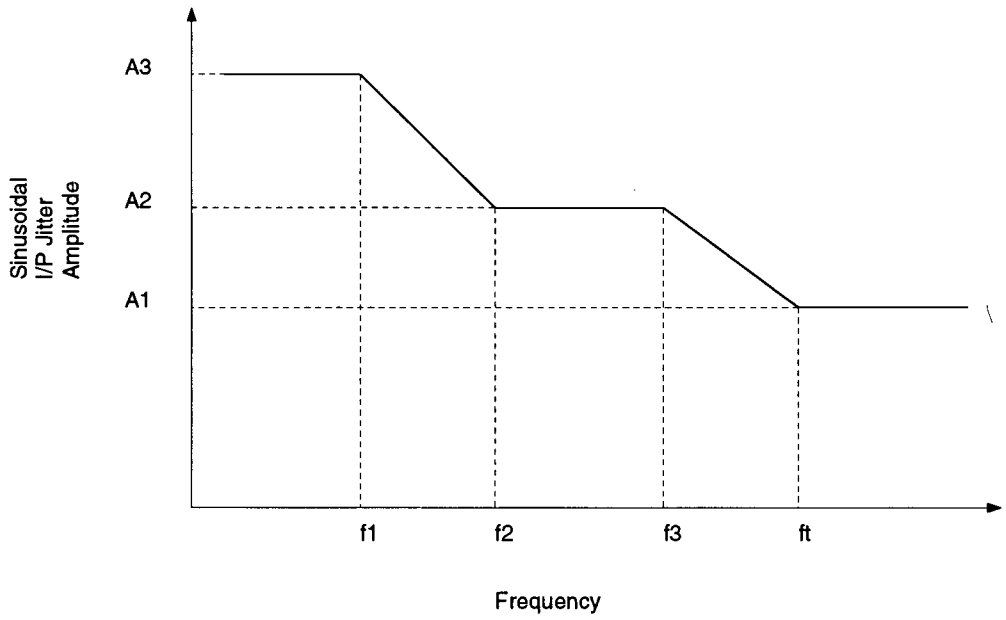

Figure 2.5.2 Input jitter tolerance specification [Syn94].

Table 2.5.1 Jitter tolerance Specification [Syn94].

OC/STS level	fo (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)	A1 (UI p-p)	A2 (UI p-p)	A3 (UI p-p)
1	10	30	300	2	20	0.15	1.5	15
3	10	30	300	6.5	65	0.15	1.5	15
12	10	30	300	25	250	0.15	1.5	15

For practical purposes, the jitter tolerance template specifies the minimum jitter that a network element must be able to sustain without producing any bit errors. Jitter tolerance

applies specifically to clock and data recovery units. An interesting feature of this jitter tolerance specification is that it requires CRUs to be able to recover clock and data satisfactorily from a modulated bit stream which has been modulated using a sequence of sinusoids of single frequency and constant amplitude. The range of frequency-amplitude pairs over which the procedure must be repeated is given by the template shown in Fig. 2.5.2. The jitter amplitudes and frequencies are specified in Table 2.5.1. In reality, a jittered data stream is seldom modulated by an individual sinusoid. Almost always, in real systems, the jitter present on a data stream is random in nature with a broadband jitter spectrum [Bla95]. The requirement of sinusoidal modulation has both advantages and disadvantages. On one hand, it makes the testing procedure deterministic and repeatable. On the other hand, it requires long test times as the test must be repeated a number of times for various amplitude-frequency pairs specified in the template. Theoretically, the number of points is infinite. However, for practical purposes a reasonable spacing between the frequency points is chosen by the test engineer depending on the time, accuracy, and cost requirements. A reasonable number of points can be between 10 to 20. Since jitter tolerance specifications require that the jitter for the test purposes be sinusoidal, next, we investigate the jitter parameters in terms of conventional angle-modulation parameters.

Jitter as a Case of Angle Modulation Phase modulation (PM) is a form of angle modulation in which the angle of the carrier is varied linearly with the modulating signal [Hyk92]. Let $x_c(t)$, given by

$$x_c(t) = cos(\omega_c t), \tag{2.1}$$

denote an unmodulated carrier whose angular frequency is ω_c. The zero crossing instances of this signal are assumed to be the time instances corresponding to the clock signal edges under test. Let $x_m(t)$, given by

$$x_m(t) = A_m cos(2\pi f_m t), \tag{2.2}$$

be the modulating signal used to phase-modulate the carrier $x_c(t)$. f_m is the frequency and A_m is the amplitude of the modulating signal. Then, the PM wave is given by

$$x_{pm}(t) = cos\{\omega_c t + k_p x_m(t)\}, \tag{2.3}$$

where k_p is the phase sensitivity of the modulator. If the angle of the unmodulated carrier is considered to be the reference, the angle of the modulated signal, $\theta_o(t)$, varies proportionally with the amplitude of the modulating signal, i.e., $\theta_o(t) = k_p x_m(t)$. The phase deviation resulting from the modulation is the jitter.

A phase-modulated signal is shown in Fig. 2.5.3. Due to the modulation, there is a difference in the time instants at which the edges of the unmodulated and modulated signals happen. The case shown here is the case of sinusoidal jitter.

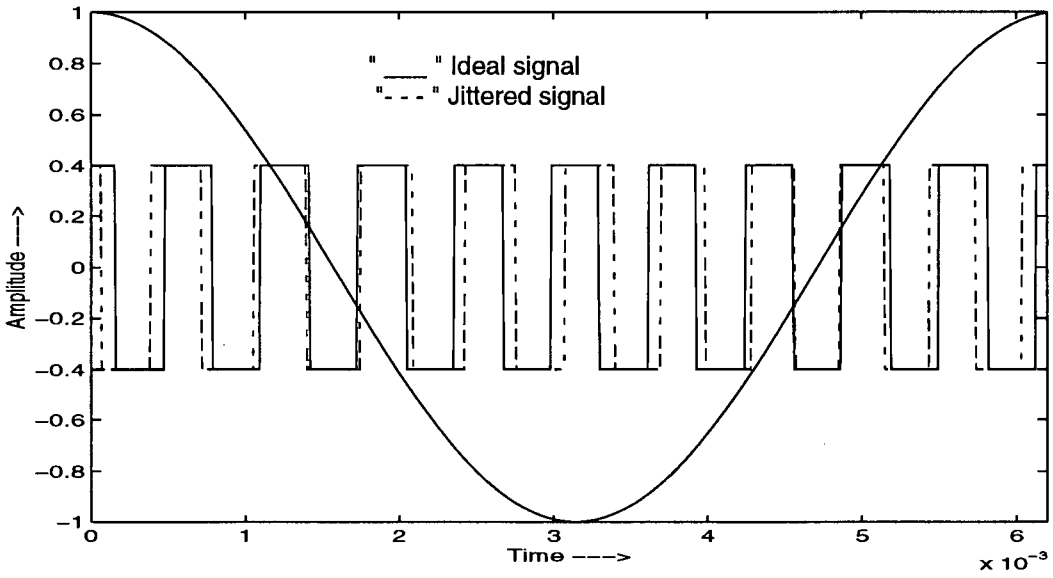

Figure 2.5.3 Phase Modulation.

Jitter can also be considered a case of frequency modulation (FM), as frequency and phase modulation are closely related. A frequency modulated wave corresponding to the phase modulated wave in Eq.2.3 is given by

$$x_{fm}(t) = cos\{\omega_c(t) + k_f sin(2\pi f_m t)\} \tag{2.4}$$

where k_f is frequency modulation index given by $k_f = \Delta f / f_m$. Δf is the maximum frequency deviation due to FM and f_m is the modulating signal frequency. Fig. 2.5.4 [Hyk92] depicts the relationship between PM and FM. PM and FM blocks shown in the figure denote a phase modulator and a frequency modulator, respectively.

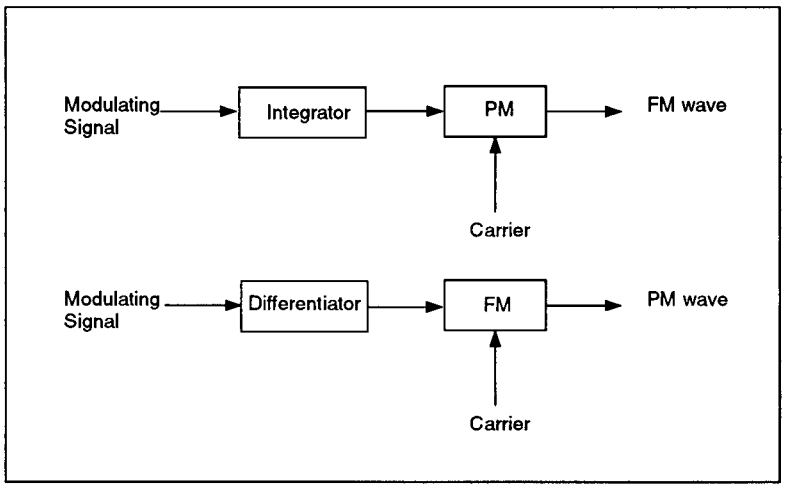

Figure 2.5.4 Relation between PM and FM.

In the physical sense, k_f represents the phase deviation of the wave in Eq.2.4. If the maximum values of the deviations in angle for FM and PM are considered, then,

$$|\{k_p \times \cos(\omega_m t)\}|_{max} = |\{\Delta f/f_m \times \sin(\omega_m t)\}|_{max}. \tag{2.5}$$

UI (unit interval) is a standard way of jitter representation in terms of the part of the total bit interval. If J_{pp} is the peak to peak jitter in UI, then, its angle equivalent is equal to J_{pp} x 2π. However, due to the cosine function in the angle argument of the angle modulated wave, we replace $\Delta f/f_m$ by J_{pp} x π and not by J_{pp} x 2π, as the excursions of a sinusoid are from – 1 to + 1. Hence, the jitter in UI is related to the modulation index as given by

$$J_{pp} \times \pi = \Delta f/f_m. \tag{2.6}$$

Eq. 2.6 is the relation between the frequency modulation parameters and the jitter. This equation is used to translate input jitter tolerance template specifications to frequency deviations. However, the above relations hold for low values of angle modulation indices (<0.8) as the higher modulation indices result in wideband angle modulation [Hyk92].

A numeric example provides better insight into the specifications. Consider one of the points on the template, say, 0.15 UI maximum jitter at 250 kHz for an OC-12 (622.08 MHz) network element. These two numbers provide a complete specification of jitter at the given frequency. 0.15 UI maximum jitter at 250 kHz means that the edges of the jittered signal are shifting away from their corresponding edges of the non-jittered signal at a rate of 250 kHz. Since the modulating signal is assumed sinusoidal, the jitter reaches a maximum at $\pi/2$. At this point the corresponding edges are apart by 0.15 UI. In the time domain this means that the edges are apart by 241 ps (0.15 x 1.6075 ns), as the time period of a 622 MHz clock is 1.6075 ns. In the frequency domain, this implies that the instantaneous frequency at this point is (622.08+0.1178) MHz (using Eq. 2.6). Clearly, the control and measurement of time in the order of picoseconds is difficult and cumbersome especially at high frequencies.

There are other jitter specifications that are not relevant to the clock and data recovery units. Since, they do not relate to CRUs, they are not discussed in detail in this thesis. However, a brief overview is provided in Appendix F for the sake of completeness.

Chapter 3
A BIST Scheme For the Jitter Tolerance Test of a Clock and Data Recovery Unit

This chapter deals with the jitter tolerance test of the CRUs found in data transceiver ICs. A SONET clock and data recovery unit is adopted as an example. First, an overview of a typical SONET node is presented. Following this, the theory of jitter tolerance of a generic PLL is presented. This is followed by a discussion of present-day industry standard methods of performing jitter tolerance tests. A novel BIST scheme is presented along with simulation and experimental results. Finally, some possible variations of the presented BIST scheme are discussed.

3.1 A SONET Node

The requirement of higher bit rates than the existing integrated services digital network (ISDN) [Onv94], for supporting applications such as interactive multimedia and interconnection of local area networks, has led to the introduction of broadband ISDN (B-ISDN). Asynchronous Transfer Mode (ATM) is a transport mode of choice for future B-ISDN. A transfer mode defines how information supplied by network users is eventually mapped onto the physical network [Onv94]. SONET has been chosen as the preferred physical medium for ATM networks [Bla95].

SONET is an interface that provides a physical envelope through a framing structure to transport ATM cells. Fig. 3.1.1 shows a typical SONET network element. The clock and data recovery unit (CRU) in the receiver section of this SONET node recovers the clock signal from the received serial data. The data is recovered with the help of the recovered clock. The recovered data is stored on the IC in the form of bytes. Hence, a serial-to-parallel conversion is performed using the serial-to-parallel block. The parallel data is processed for section, line, and path overhead by the OHP (overhead processor) block. Error checking and delineation is also performed on the cells by this block. The legitimate cells are then written to a first-in first-out (FIFO) buffer. The switching section processes the frames and routes the data. The clock synthesis unit (CSU) in the transmitter section synthesizes a line rate clock using a local reference. Prior to the transmission, the parallel data stored in the FIFO is appended with line and section overhead by the OHP. Then, the parallel data is converted into a serial bit stream by the parallel-to-serial convertor. The SONET/SDH frames are finally transmitted via a serial data stream at the line rate.

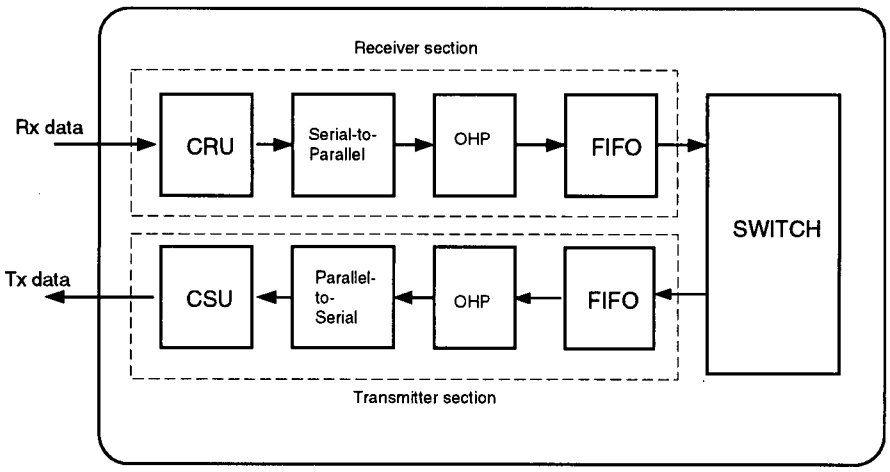

Figure 3.1.1 A typical SONET node.

The present day level of system integration has made it possible to integrate CRU, CSU, serial-to-parallel, parallel-to-serial, OHP, and FIFOs blocks on a single IC. An example of such an IC is PM5346 [Sun95]. The receiver section of such an IC typically constitutes a clock and data recovery unit (CRU) based on a PLL. The transmitter section also contains a PLL-based clock synthesizer.

3.2 Theory of Jitter Tolerance

A PLL is a feedback control loop whose frequency is locked onto some frequency component of an input signal. The basic architecture of a PLL is illustrated in Fig. 3.2.2. A phase detector (PD) is used to compare the phase difference between the input signal and the signal generated by a voltage controlled oscillator (VCO). The phase-difference signal at the output of the phase detector is filtered by a low-pass filter to generate the control voltage for the VCO. Thus, through negative feedback, the phase and the frequency of the VCO are "locked" to the phase and frequency of the input signal. Example references on PLLs are [Wol91], [Ega81] and [Gar79].

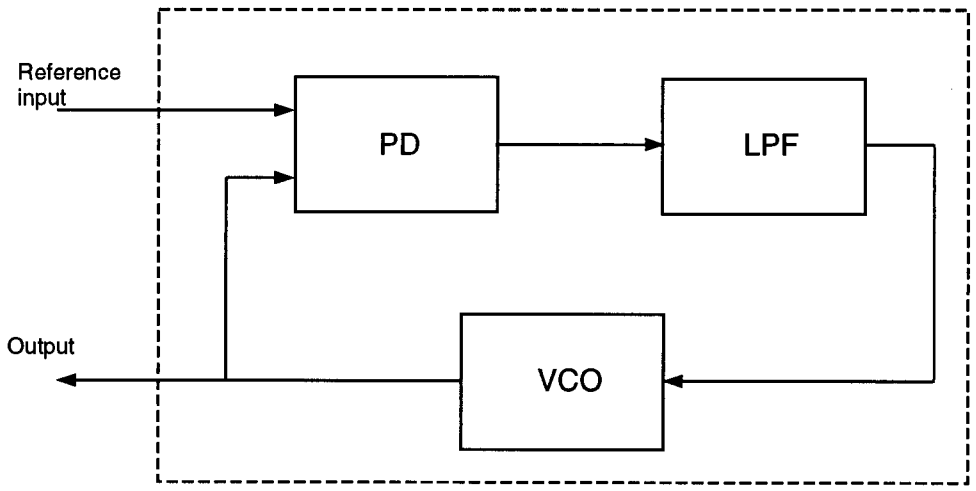

Figure 3.2.2 Block diagram of a PLL.

To study the jitter tolerance of a PLL, a linear ac model of the PLL is used. The linear ac model shown in Fig. 3.2.3 [Wol91] represents a generic phase-locked loop comprising of an active loop filter. The ac model of the PLL is used, as opposed to the complete linear model with dc parameters, since the jitter tolerance is directly related to the dynamic behavior (frequency response) of a PLL.

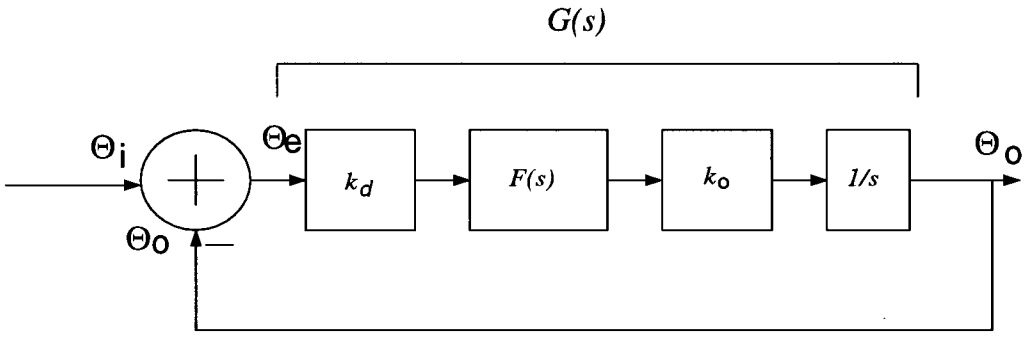

Figure 3.2.3 Linear ac model of a PLL [Wol91]

In Fig. 3.2.3, *F(s)* is the frequency response of the loop filter, k_d is the gain factor of the phase detector, and k_o is the VCO gain. Let $\Theta_i(s)$ be the phase of the input signal, $\Theta_o(s)$ be the phase of the signal generated by the VCO, and $\Theta_e(s)$ be the error signal or the phase difference between the input signal and the VCO output. The forward gain of the PLL, *G(s)*, is then given by

$$G(s) = \frac{\Theta_o(s)}{\Theta_e(s)} = \frac{k_d k_o F(s)}{s} \tag{3.1}$$

From the ac model shown in Fig. 3.2.3,

$$\Theta_e(s) = \Theta_i(s) - \Theta_o(s), \tag{3.2}$$

and

$$\Theta_o(s) = \Theta_e(s) \times G(s) \tag{3.3}$$

Hence, on replacing $\Theta_o(s)$ in Eq. 3.2 with its value from Eq. 3.3 , we obtain

$$\Theta_e(s) = \Theta_i(s) - \Theta_e(s)G(s) \tag{3.4}$$

or,

$$\frac{\Theta_e(s)}{\Theta_i(s)} = \frac{1}{1+G(s)} \tag{3.5}$$

The term $\frac{\Theta_e(s)}{\Theta_i(s)}$ is known as the phase error response $H_e(s)$ [Wol91]. In a general sense, the jitter tolerance of a PLL is its ability to maintain lock. An implication of this statement is that the phase error remains within the linear (useful) range of the phase detector. Hence, the jitter tolerance response, $J(s)$, of a PLL is the inverse of the phase error response $H_e(s)$, i.e.,

$$J(s) = \frac{1}{H_e(s)} \tag{3.6}$$

Next, we investigate the various response functions discussed in this section i.e., $H_e(s)$, $J(s)$, $F(s)$, and $G(s)$, for an example PLL. The PLL under consideration is based on an active loop filter and a multiplier type PD. The details of the PLL are as follows.

Loop Filter : The loop filter is shown in Fig. 3.2.4. The filter is an active RC filter with poles at 0 and ω_3 and a zero at ω_2. The filter uses passive elements used for a PLL in [Sun95]. The transfer function of the filter is given by

$$F(s) = k_h \frac{(s+\omega_2)}{s(s/\omega_3+1)} \tag{3.7}$$

where, $k_h = \frac{R_2}{R_1}$, $\omega_2 = \frac{1}{R_2 C}$ and $\omega_3 = \frac{4}{R_1 C_3}$. The passive components used for the filter are

- R_1 = 53.2 k Ω

- R_2 = 200 Ω
- C = 0.47 μF
- C_3 = 13.5 pF

Hence, the frequencies of interest are

- ω_2 = 2π x 1.693 kHz
- ω_3 = 2π x 886.41 kHz
- k_h = 0.003759

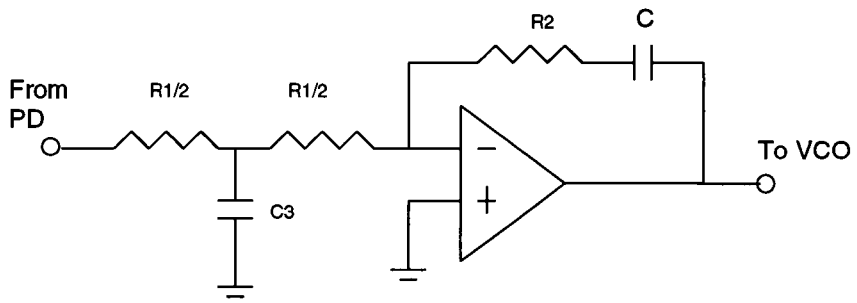

Figure 3.2.4 Loop Filter.

The frequency response of the filter plotted using MATLAB [Mat94] is shown in Fig. 3.2.5.

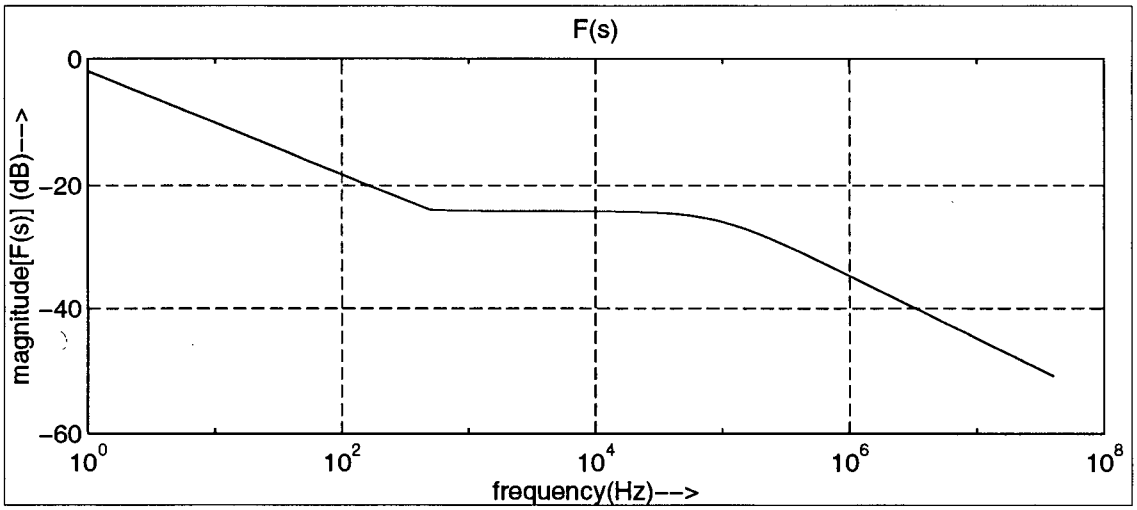

Figure 3.2.5 Frequency response of the loop filter.

Phase Detector : The phase detector used for the PLL is a multiplier-type phase detector [Wol91]. The block diagram of the phase detector is shown in Fig. 3.2.6. The phase detector comprises a four-quadrant multiplier and a limiter. Such a phase detector features a triangular characteristics as shown in Fig. 3.2.7. For a multiplier-type phase detector, the

Figure 3.2.6 Multiplier type phase detector

gain is given by [Wol91]

$$k_d = \frac{V_{dm}}{\pi/2}. \tag{3.8}$$

In our case, V_{dm} is chosen to be 2.5 V. Hence, k_d = 0.398 V/rad.

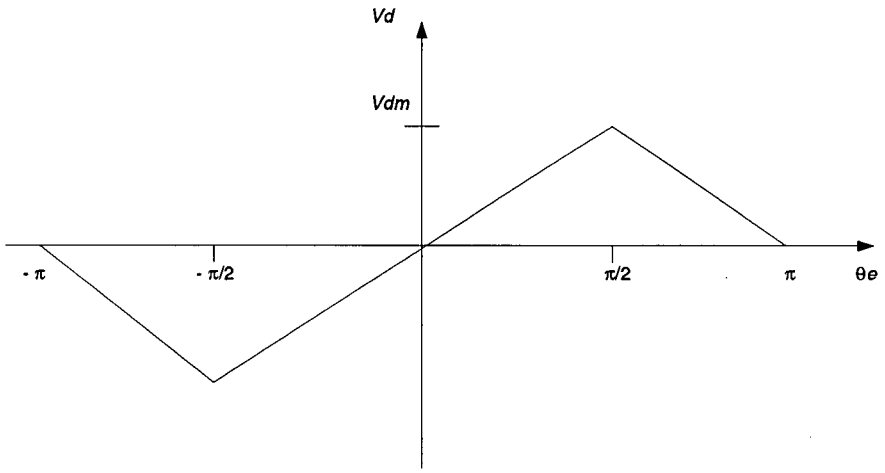

Figure 3.2.7 Phase detector characteristics.

Voltage Controlled Oscillator : The VCO model chosen for the PLL is assumed to be linear with the gain k_o = 100 MHz/V.

From the ac model of the PLL, the closed loop transfer function H(s) is given by

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{G(s)}{1 + G(s)}. \tag{3.9}$$

For the PLL under consideration, the open loop transfer function, or, the forward loop gain is

$$G(s) = k\frac{(s + \omega_2)}{s^2(s/\omega_3 + 1)} \tag{3.10}$$

where k is referred to as the PLL bandwidth [Wol91] and is given by $k = k_h k_o k_d$. Hence, the closed-loop transfer function is given by

$$H(s) = \frac{ks + k\omega_2}{s^3/\omega_3 + s^2 + ks + k\omega_2}. \tag{3.11}$$

MATLAB plots of functions H(s) and G(s) are shown in Fig. 3.2.8 and 3.2.9 respectively.

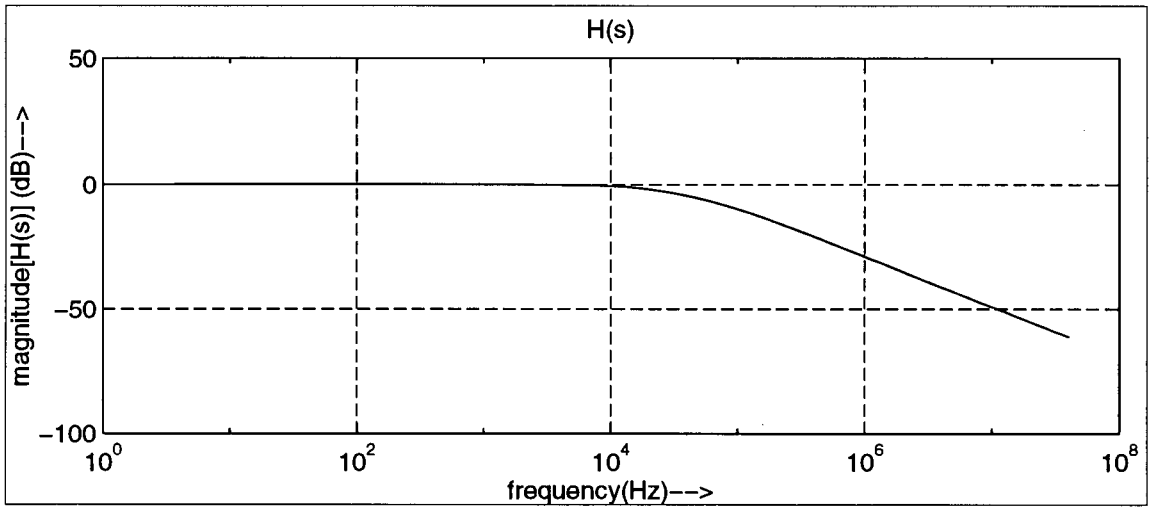

Figure 3.2.8 Closed-loop response of the PLL.

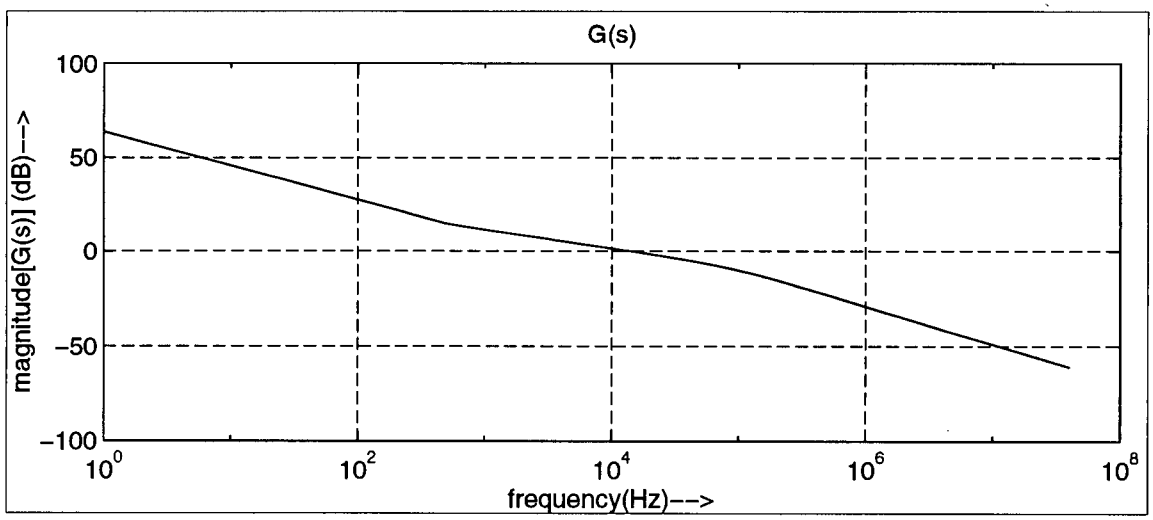

Figure 3.2.9 Open-loop response of the PLL.

The jitter tolerance function J(s) is given by

$$J(s) = 1 + k\frac{(s+\omega_2)}{s^2(s/\omega_3+1)}. \tag{3.12}$$

J(s) for the PLL under consideration is plotted in Fig. 3.2.10.

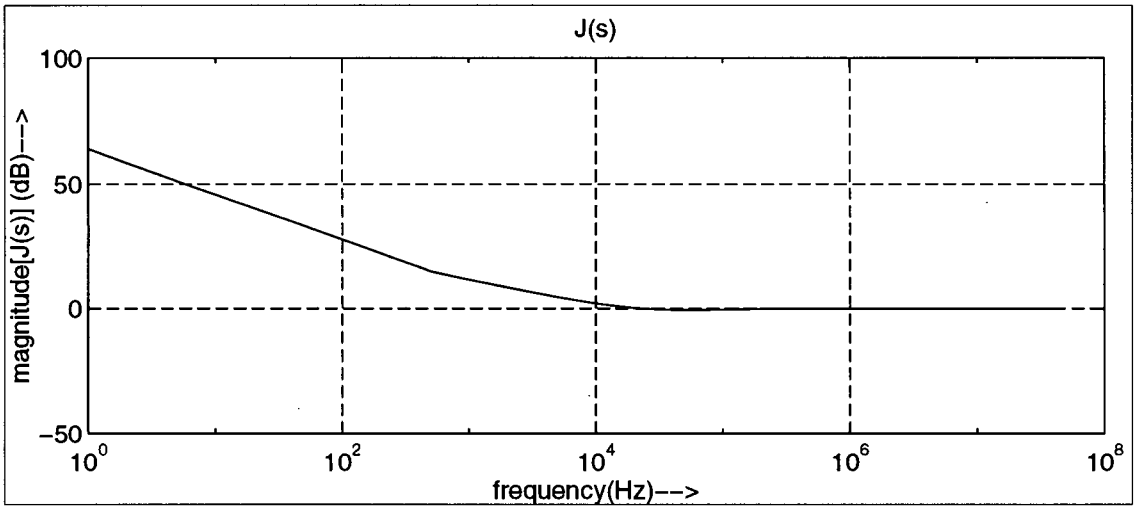

Figure 3.2.10 Jitter tolerance of the PLL.

The above plots are used to observe the correlation between the PLL parameters and the theoretical jitter tolerance of the PLL. The jitter tolerance is the inverse of the phase error response and is essentially a function of the PLL's open-loop and closed-loop response. This provides a design guideline for a PLL with required jitter tolerance. The calculated jitter tolerance (theoretical) of the PLL, obtained in this section, is used as a comparative measure for the simulations in section 3.4.1.

3.3 Conventional Jitter Tolerance Test Schemes

A conventional method of performing a jitter tolerance test is to use dedicated expensive test equipment that can impose a given jitter on a data stream generated by a data generator. The jittered stream produced by the jitter generator is supplied to the DUT. The bits recovered by the DUT from the jittered data stream are fed to a bit-error rate tester (BERT). The non-jittered data stream is also fed to the BERT. The BERT generates an output indicating the bit error rate of the DUT. The magnitude of jitter at which the bit-error rate (BER) exceeds the

pre-defined bound specified in the jitter tolerance specifications determines the jitter tolerance of the DUT. An example of an instrument capable of being used for a jitter tolerance test is the industry-standard Microwave Logic SONET/SDH SJ-300 Jitter and Wander Analyzer [Mic95].

A non-SONET-specific example of a jitter tolerance test equipment can be found in [Bla95]. The methodology is based on the generation of jittered data using a jitter source created using precision delay lines. The recovered clock is analyzed by plotting its eye-diagram on an oscilloscope. The jitter tolerance methodology is aimed at jitter tolerance tests of fibre channel equipment and does not specify the spectral content of the clock generated by the jitter source. Since SONET jitter tolerance tests must be carried out in the presence of sinusoidal jitter, the above method is not suitable for SONET tests.

Another example of a jitter clock source based on direct digital synthesis waveform theory has been proposed in [LaM89]. The presented jitter clock source is capable of generating a clock signal with a wide range of jitter amplitudes and frequencies. However, the method requires a very high frequency clock signal for the synthesis of a programmable low frequency signal. This is due to the fact that the method is based on discrete time approximation. For SONET frequencies (MHz range), the method will require a base frequency in the range of GHz for generating a clock with required jitter characteristics. Since such a high frequency clock signal (GHz) is not available in normal circumstances, this method is also not appropriate for jitter tolerance test at SONET frequencies in the range of MHz or higher.

The above methods of performing jitter tolerance tests are either unsuitable for SONET frequencies (hundreds of MHz or higher), or are only applicable for either characterization

tests or volume production-stage tests of expensive parts that can tolerate long test times, using dedicated expensive test equipment that can generate data streams with controlled amounts of jitter. Hence, the major drawbacks of the aforementioned jitter tolerance test methodologies are :

(a) high cost - the requirement for expensive test equipment that must have the same or superior speed and accuracy specifications as the CRU under test.

(b) long test times - normally, the setup and operational time of dedicated equipment is very long and results in overall long test times. The setup time is a applicable once, while the operational delays are recurrent.

(c) frequency limitations - most apparatus of applying jitter to the clock are limited to 1 to 5 MHz jitter frequency and cannot source enough jitter to make the parts fail the test.

With the rapidly increasing speeds of clock rates resulting from the advances in the IC technology, these drawbacks become increasingly significant, especially for performing volume-production stage testing of CRU jitter tolerance.

3.4 The BIST Scheme

Recognizing the demerits of conventional jitter tolerance test methodologies and the need for more efficient techniques, this section presents a BIST scheme for the jitter tolerance test of the CRUs found on high speed data transceivers that belong to the class of ICs described in the beginning of this chapter. In particular, the availability of a PLL-based clock synthesizer is assumed which is normal for the types of ICs considered.

Fig. 3.4.11 shows a block diagram that illustrates the concept underlying the novel CRU test method. CRU is the block under test. The data generator, Clock Synthesis Unit (CSU), bit-error rate tester, signal generator, and the coupling capacitor together constitute the circuitry required for realizing the CRU tests. The following describes the functionality of these blocks and how it is used towards the realization of the novel test method. It is desirable to have all the blocks integrated on the same IC, and thereby provide for a complete and true BIST scheme. However, the CRU frequency and jitter tolerance tests can still be realized if any one or more of the blocks in Fig. 3.4.11 reside externally (off-chip) to the CRU under test.

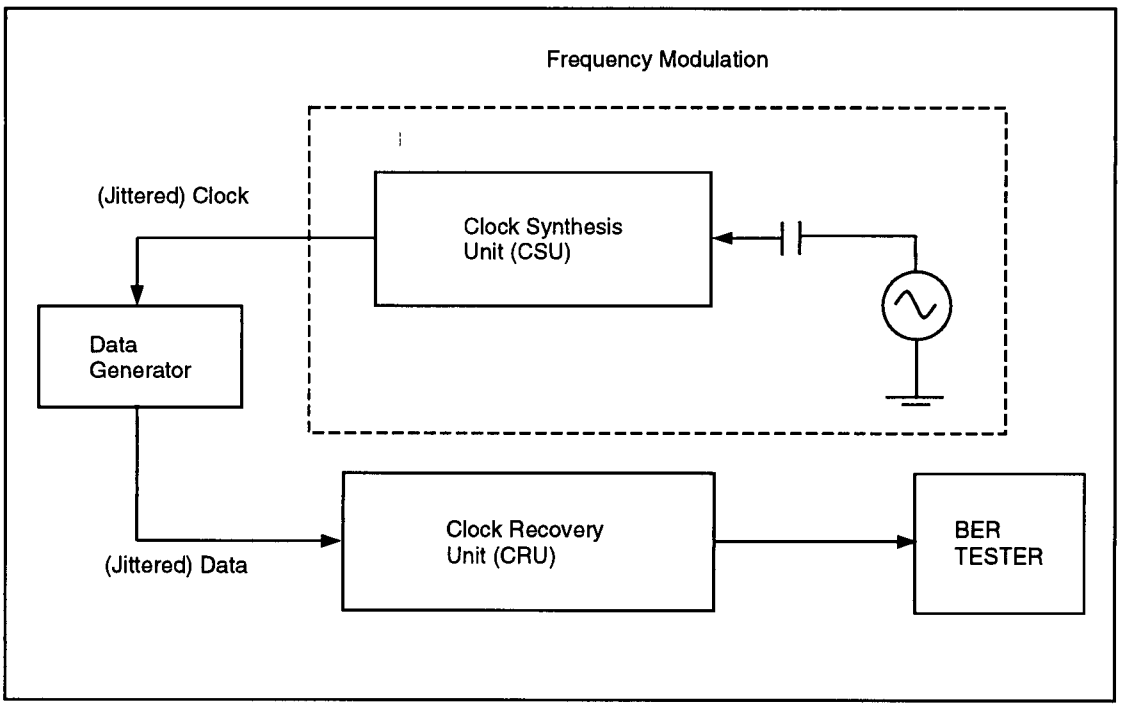

Figure 3.4.11 Jitter tolerance BIST scheme.

The requirement for a CRU jitter tolerance test is to verify that the CRU can correctly recover the data from an arbitrary (pseudorandom) data stream that is itself generated from

a specifically jittered clock. The test method here performs just that through the following steps: (1) a jittered clock is generated, (2) the jittered clock is used to generate a test data stream, (3) the test data stream is fed to the CRU under test, (4) the bit error rate tester determines the number of bit errors that arise in the CRU's recovered data stream, thereby establishing the CRU's jitter tolerance or lack of. The following describes the steps of the BIST scheme in detail.

STEP I : Frequency modulation is performed to impose a jitter of known characteristics (amplitude and frequency) on the clock signal generated by the CSU. In the normal mode of operation, the CSU on typical data transceiver ICs is used to synthesize a line rate clock from a local reference. Fig. 3.4.12 shows the structure of a typical phase-locked loop (PLL)-based CSU and the arrangement for performing such frequency modulation.

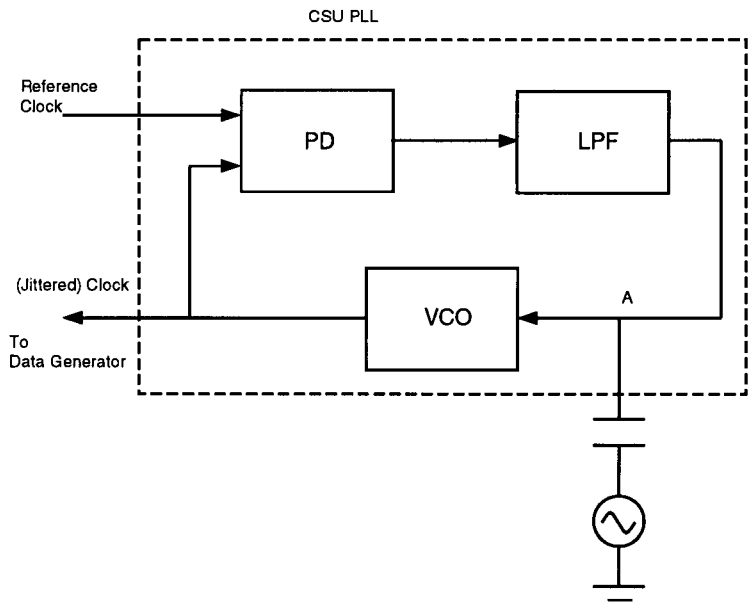

Figure 3.4.12 Generation of jittered clock.

Let k_f be the gain of the voltage controlled oscillator (VCO) in the CSU PLL and A_m

be the amplitude of the modulating signal. The deviation in output frequency of the VCO is given by

$$\Delta f = k_f \times A_m. \tag{3.13}$$

Then, the amplitude of the modulating signal required to impose a jitter of value J_{pp} on the clock is obtained using Eqs. 3.13 and 2.6, and is given by

$$J_{pp} = \frac{k_f \times A_m}{\pi \times f_m}. \tag{3.14}$$

Thus, a sinusoid with a frequency of f_m and amplitude A_m will impose a desired jitter of J_{pp} UI at frequency f_m on a carrier given by Eq. 2.1.

Since the CSU used in this test method has a normal mode of operation and purpose other than testing the CRU, it is crucial that the test circuitry added to it for the CRU test purposes not have any significant negative performance impact on the CSU's normal mode of operation. As the normal mode of operation of the CSU results in the VCO input to be (when in-lock) a dc or very low-frequency signal, it is generally acceptable to add capacitance to this node without incurring any significant negative performance impact. Therefore, as the normal VCO input is a dc signal, an effective way of generating a frequency modulated signal at the CSU output is to provide a modulating signal of specific amplitude and frequency to the VCO-input (node A). In turn, a simple way of superimposing a relatively high frequency (MHz range) ac-signal (modulating signal) onto a dc signal is through ac-coupling, i.e., coupling the modulating signal source to the VCO - control input through a capacitor.

Often the output of the loop filter is a low impedance node and the input of the VCO is a high impedance node. If a signal is ac-coupled into such a node, the relative impedances

and their impact on the effective control voltage to the VCO must be taken into account. Fig. 3.4.13 depicts the approximate scenario at the control input node of the VCO.

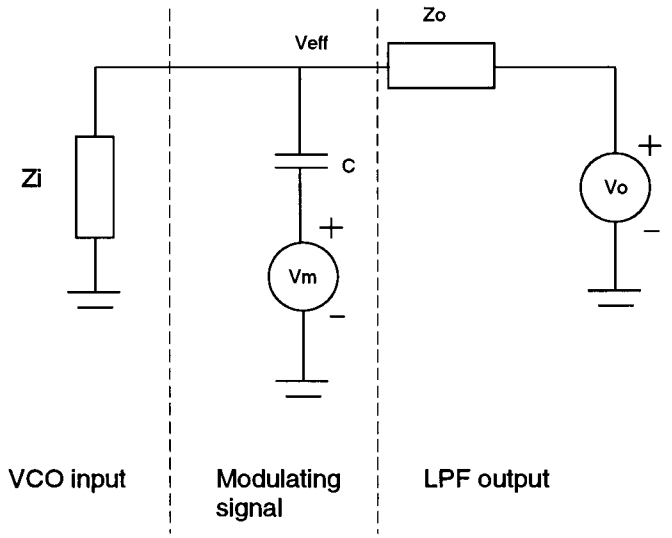

Figure 3.4.13 AC coupling.

Z_i is the high input impedance of the VCO (M Ω range), Z_o is the output impedance of the LPF and V_o represents the voltage at the output of the LPF. V_m and C represent the modulating source and the coupling capacitor, respectively. The impedance of the capacitor is given by Z = 1/sC. Then, the effective voltage, V_{eff}, at the control input of the VCO is given by

$$V_{eff} = \frac{V_o}{\left(\frac{Z_o}{Z_i} + \frac{Z_o}{Z} + 1\right)} + \frac{V_m}{\left(\frac{Z}{Z_i} + \frac{Z}{Z_o} + 1\right)}. \tag{3.15}$$

If $|Z_i| >> |Z_o|$ and $|Z_i| >> |Z|$, then V_{eff} is given by

$$V_{eff} \approx \frac{V_o}{(Z_o/Z + 1)} + \frac{V_m}{(Z/Z_o + 1)}. \tag{3.16}$$

In order to make V_m the determining factor for V_{eff}, the ac impedance Z must be small compared to R_o. If $|Z| << |Z_o|$, then from Eq. 3.15,

$$V_{eff} \approx Vm. \tag{3.17}$$

In some cases, the condition $|Z| << |Z_o|$ may imply a large capacitor which may be unacceptable. However, if the PLL is designed such that V_o is approximately equal to 0 V in the 'locked' condition, a smaller capacitor can be used. In that case, V_{eff} is given by

$$V_{eff} \approx \frac{V_m}{\left(\frac{Z}{Z_o} + 1\right)}. \tag{3.18}$$

The amplitude of the modulating signal should be determined taking Eq. 3.18 into account.

If the capacitor scenario is found unsuitable for a particular application, the capacitor can be replaced by an adder (eg., op-amp based adder) or a simple resistor. When an adder is used instead of a capacitor to add the modulating signal to the VCO input, it provides better control over the modulation as the magnitude of the coupled signal is not dependent on the frequency of the modulating signal. However, the price to be paid is the added cost of the adder. If a resistor is used instead of the capacitor it will also make the magnitude of the coupled signal independent of the frequency of the modulating signal.

The sinusoidal modulating signal is provided by a sinusoidal signal generator. This sinusoidal signal generator can be realized on the same IC as the CRU under test. Examples of such integrable signal generators can be found in [Ton93][Lu94]. Some jitter specifications may require that the source generate a sinusoid of precise amplitude and frequency. The precise amplitude requirement may not allow an on-chip signal source in most current cases

due to the relatively large area that would be required to realize such a source. As such sources are not necessarily found on the types of ICs such as transceiver ICs where CRUs are found, the required area for integrating the signal source may not be easily justified. In that case, one would resort to an external signal source. Though the external signal source scenario does not comply with the requirements of a true BIST scheme, it provides an economical solution as compared to the one provided by mixed-signal ATEs. Another advantage of the external signal source is that, in general, it is more precise than the on-chip generator.

For example, to impose 0.15 UI jitter on a 622.08 MHz clock signal, frequency modulation is performed with a sinusoid of 250 kHz frequency. The amplitude of the sinusoid is determined by the maximum value of angle deviation. The corresponding value of maximum angle deviation is $0.15 \times \pi = 0.4712$ rad. This corresponds to $\Delta f/f_m$. Hence, the value of Δf is 117.8 kHz. Assume that the gain of the VCO is 100 MHz/V. The required amplitude of the sinusoid is then obtained from Eq. 2.6. In this case, the amplitude will be 1.178 mV. The amplitude of the sinusoid can be directly obtained from Eq. 3.14 also. Hence, a sinusoid with a frequency of 250 kHz and amplitude 1.178 mV will impose a desired jitter of 250 kHz and 0.15 UI on a 622.08 MHz clock signal. In such cases, due to the noise factors, the amplitude in the order of mV may require an external generator.

STEP II : The realization of Step (II) of the BIST, requires that the jittered clock signal from the CSU be fed to the data stream generator block that in turn generates the data stream against which the CRU is tested for clock recovery and tolerance to jitter. Such a data generator is usually chosen to be a digital pseudo-random data generator realized as a digital finite state machine with feedback. A well-known example of a pseudo-random

data generator is a Linear Feedback Shift Register (LFSR) [Bar87]. However, this does not preclude the clock being fed to other data sources, such as digital logic producing specific protocol data formats, like SONET frames. SONET interface ICs like PM 5346 [Sun95] normally include such digital circuitry to produce protocol specific data. Thus, supplying the jittered clock obtained through Step (I) to the data generator results in a data stream that has same jitter characteristics as the clock.

STEP III : The data stream with imposed jitter, obtained through Step (II) is then fed as a test input stream to the CRU. The CRU recovers the clock and data from the input data stream typically using a PLL.

STEP IV : The recovered data from CRU is fed to a bit-error rate detection circuit (e.g., BERT). The error detector circuit checks the recovered data stream for BER. The output of this block is an indication of the number of bits in error. Several realizations of such error detectors can be found in practice [Pal95]. In our case (IC PM5346), the transmitter section of the IC contains resources to generate pseudo-random data in one of its normal modes of operation. Also, the receiver section is capable of processing the data for bit errors. Hence, a test-dedicated data generator and a bit error detector were not needed, rendering the implementation more economical. The output of the error detector circuit is used to generate a pass/fail signal for the CRU block.

The total area overhead of the BIST scheme is minimal. The scheme requires essentially four blocks, i.e., a CSU, a data generator, a BERT, and a modulating signal generator. In addition to this, a coupling capacitor is also required. As mentioned earlier, the CSU is normally present on the IC. As for the data generator and BERT, these simple circuits can

easily be implemented using known techniques [Bar87, Pal95], and thus do not constitute overhead per se. Regarding the signal generator, if the integration of the latter is judged excessive, the scheme can still be implemented using a readily available external generator. On the basis of the block diagram level description of the scheme, the control required for implementing the BIST scheme is likely to be simple and is not likely to incur any significant overhead. Another major advantage of the BIST scheme is high speed of operation as compared to the conventional test methods. The exact cost of the BIST is highly dependent on the implementation. Since the implementation of the BIST is not done on a transistor level, the exact overhead of the scheme is not known. However, based on the other similar implementations found in literature, such as the BIST scheme presented in [Ton93], it can be stated that the area overhead and hence the overall cost is not likely to be excessive.

A potential drawback in the presented scheme is that it relies on the knowledge of the VCO gain for control over the jitter amplitude being supplied to the DUT. Typically, when an IC is designed and fabricated, a thorough characterization is performed on the sample parts. Through characterization, various parameters and their variations are determined. For the BIST scheme, the VCO gain needs to be determined. Because of process variations and other factors such as temperature and transistor size mismatching, the VCO gain may vary from its nominal value. Hence, a careful characterization of VCO gain margins is required prior to the production stage deployment of the methodology. Precise knowledge of other parameters affecting the modulation such as the impedances associated with the control input node of the VCO is not as critical as the VCO gain as long as the conditions on the size of the coupling capacitor, as described earlier, are satisfied. The test guard bands

must be determined using the variation limits determined through characterization. If the parametric variation of the VCO gain is found to be excessive, the BIST scheme cannot be used effectively for production stage testing. However, an excessive variation itself would call for the modification of the basic design.

3.4.1 Simulation

The presented scheme was simulated in "Cadence Analog-Artist" environment [Ana94]. The block diagram shown in Fig. 3.4.11 was implemented using both digital and analog components. The simulations were performed using a mixed-mode simulator 'SpectreVerilog' [Spr94] [Ver90]. The CSU and CRU were implemented using macromodels of PLLs. Two models of the PLLs were made using building blocks from the 'Functional' library for the CRU and the CSU separately. These building blocks have been realized using controlled sources. The schematic for the overall BIST scheme is shown in Fig. B.6 (Appendix B).

The PLL macromodel used for the CSU is shown in Fig. B.4. The PLL uses a passive loop filter and a multiplier type phase detector. The VCO from the library was used along with a comparator to obtain a square-wave VCO. The phase detector was realized using an analog multiplier and a comparator. An attempt was made to imitate the scenario that would be seen in an actual circuit, with respect to the impedances. For example, the control input net of the VCO, which is a critical node from the point of view of the BIST scheme, was carefully modeled by putting an extra op-amp based unity gain buffer to simulate a high input impedance. Similarly, the output impedance of the LPF was modeled by the output of another op-amp based unity gain buffer.

The following is a list of parameters defined for the various components of the CSU PLL. The parameters chosen here are of the order used for SONET OC–3 CMOS ICs such as the IC PM 5346.

- VCO gain = 100 MHz/V;
- Phase detector gain = $5/\pi$ V/rad;
- Loop filter

  a. k_h = 0.34;

  b. Cut-off frequency = 120 kHz.

The PLL macromodel for the CRU is shown in Fig. B.3 (Appendix B). The loop filter used for this PLL is an active filter implemented using an op-amp macro from the library and the passive components. The VCO used for this filter is exactly the same as the VCO for the CSU PLL. The basic phase detector used for this PLL is also the same as the PD of the CSU. However, a module to convert non-return to zero (NRZ) data generated by the data generator into a return to zero (RZ) type format [Wol91] is added before the PD to simplify the design and performance of the basic PLL. The functionality of the NRZ to RZ type convertor is depicted in Fig. 3.4.14. By virtue of this conversion, a frequency component is created in the RZ-like data which helps in clock recovery. The module consists of a delay element and an XOR gate. The delay element shown in the schematic in Fig. B.6 is written in the 'Verilog' hardware description language (HDL) [Ver90]. The code for this module is given in Appendix D.

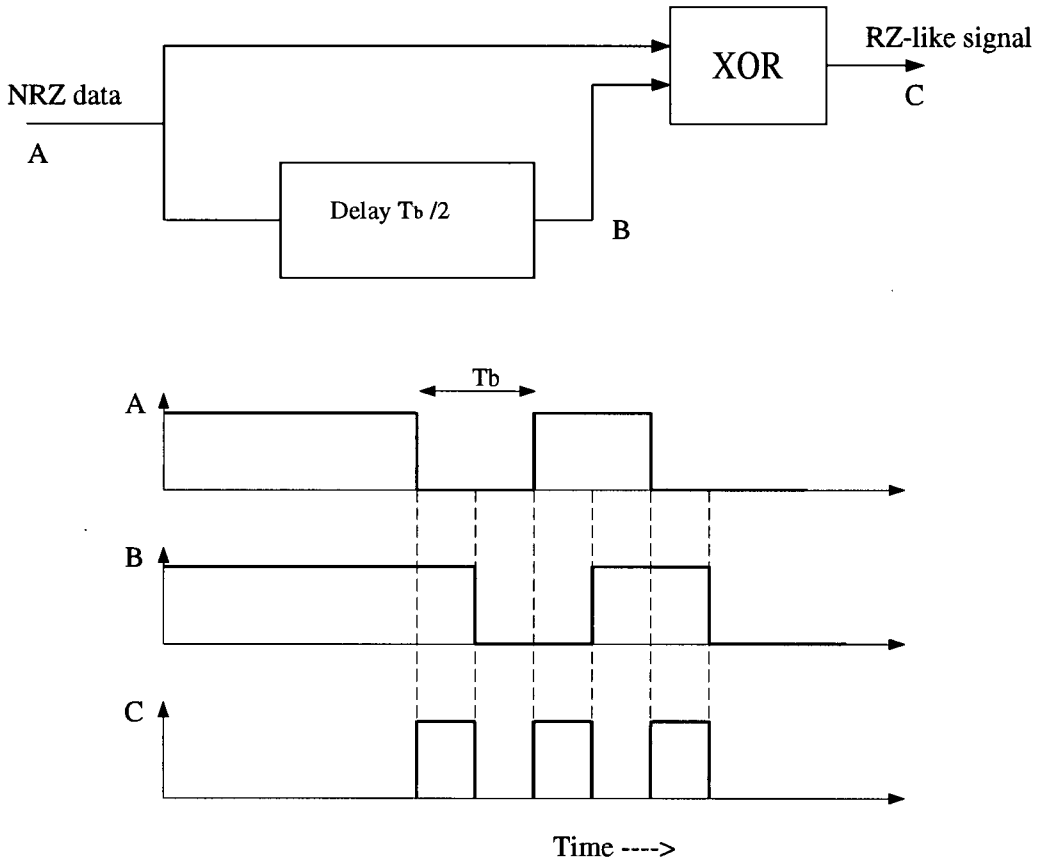

Figure 3.4.14 Conversion of NRZ data to RZ-like data.

The two PLLs (CSU and CRU) were designed for generating clocks with -2.5 and 2.5 V as low and high amplitudes respectively. This simplifies the design without any impact on performance or functionality. In this particular case, the time instants of the clock and data signals are of importance as opposed to the amplitude levels of the signals. Hence, no performance impact occurs due to the chosen amplitudes. Moreover, since the clock generated by the CSU has a swing of -2.5 to 2.5 V, those levels are shifted 'up' using a level shifter from the library before feeding it to the data generator which accepts signals between the 0 and 5 V rails. A delay of one quarter of the time period of the CSU clock (i.e. $T_b/2$)

is supplied to the recovered clock to compensate for the inherent phase characteristics of the multiplier type phase detector. The data generator description was also written in Verilog. An arbitrary data sequence was chosen for the data from the generator. The simulations were divided into two parts. In Part I of the simulations the functionality of the BIST scheme was simulated. In Part II of the simulations, the behavior of the example PLL was investigated in the presence of various modulating signals.

Part I : The BIST scheme was simulated for Part I of the simulations. The schematic used for the simulations is shown in Fig. B.6. The aim of the simulations was to determine the jitter tolerance of the PLL described in Section 3.2. The jitter tolerance of the CRU PLL was determined by gradually increasing the jitter (by increasing the amplitude of the modulating signal) until any bit error was observed. The occurrence of bit errors was checked by observing the phase relation between the input data and the output clock. Detailed results are shown in Appendix C. The simulation results are summarized in Table 3.4.1. The

Table 3.4.1 Simulation and theoretical results.

V_m (V)	V_{eff} (mV)	f_m	J_{pp} (simulation) (UI)	J_{pp} (theoretical) (UI)
32.706	4.115	10 kHz	13.100	14.1894
2.252	2.83	100 kHz	0.901	0.9246
2.466	31.00	1 MHz	0.987	1
2.477	62.27	2 MHz	0.991	1
2.482	155.98	5 MHz	0.993	1

simulation results are obtained using Eq 3.14 at the amplitudes of the modulating signal at which bit errors are observed. The theoretical results are obtained using the MATLAB

code given in Appendix E. The theoretical and simulated jitter tolerance curves are shown in Fig. 3.4.15.

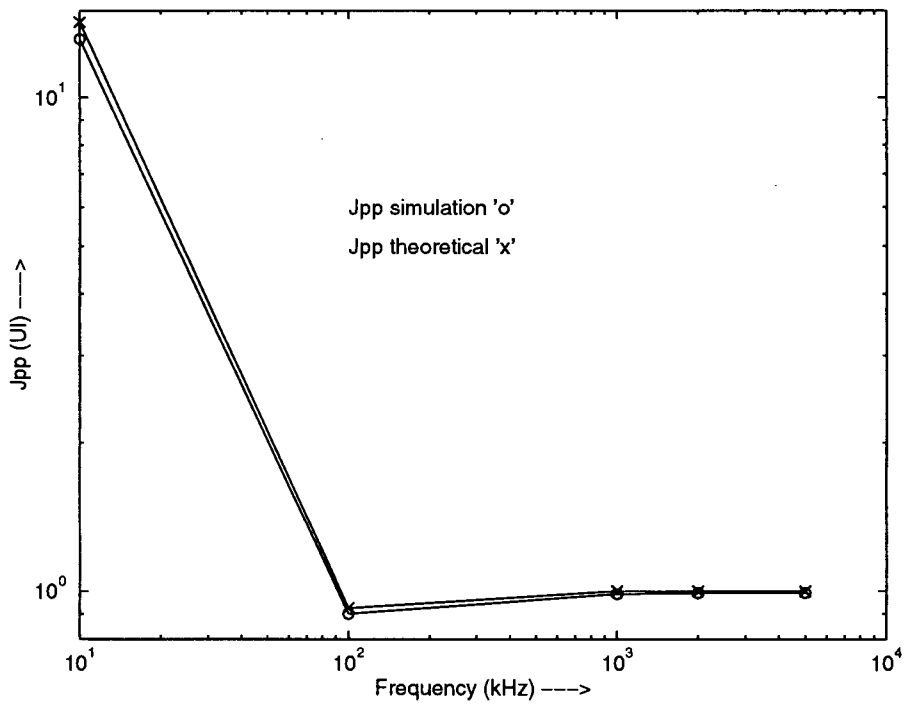

Figure 3.4.15 Simulated and theoretical jitter tolerance.

Part II : In part II of the simulations, only the stimulus part of the scheme was simulated with the aim of investigating the capability of a PLL to provide a jittered clock in the presence of different modulating signals like a triangular wave, a square wave and a step input signal. Different signals were ac-coupled into the VCO input node of the CSU PLL and the outputs of VCO and loop filter were observed.

1. **Sine wave input** - When sine waves are coupled into the VCO input, frequency modulation takes place. The output frequency is directly proportional to the amplitude

of the coupled signal as given by Eq. 3.13 (Fig. C.6).

2. **Triangular input** - When a triangular signal is supplied to the VCO through the coupling capacitor, the waveform at the filter output is as shown in Fig. C.7. The PLL lock behavior depends on the slope and amplitude of the ramp signal.
3. **Square-wave input** - A square wave applied to the coupling capacitor throws the PLL out of the lock. This simulates a random jitter scenario. (Fig. C.8).
4. **Step input** - The basic coupling scheme is altered to supply the step input to the PLL. An adder is required to add the LPF output and coupled signal. The output of the adder is connected to the VCO input. The PLL response is as expected. The PLL is first thrown out of lock and then the lock is achieved at a different frequency. This frequency corresponds to the new amplitude of input to the VCO. The waveforms are shown in Fig. C.9.

3.4.2 Hardware Verification

It was not feasible to design a circuit on the transistor level and get it fabricated for the verification of the concept underlying the BIST scheme. Nevertheless, we verified the concept by using an existing IC PM 5346 [Sun95] provided by PMC-Sierra, Inc. The hardware verification was done on a S/UNI-Lite Optical Reference Design (SORD) board [Sor95]. Since, the IC PM 5346 is not designed with the intent of the implementation of the particular BIST scheme, only the most critical aspect of the scheme, i.e., the generation of the jittered clock could be verified. The underlying assumption is that the digital components required for the BIST scheme can be easily implemented using well-known digital design techniques. The IC PM 5346 has an architecture very similar to the SONET node shown in

Fig. 3.1.1, with the exception of the switch. The IC does not include a switching section. This did not affect the experiment as the switch is not used for the BIST scheme. Moreover, only the jittered clock generation part of the scheme was verified which does not require the use of other digital circuitry present on the IC.

The CSU on the IC is designed such that the CSU-PLL cannot be put in a free running mode with the VCO input being accessible. This means that the CSU-PLL could not be used for the modulation. Due to this restriction, it was decided to use the CRU-PLL for performing the jitter modulation. In the mode of operation of the IC that was used for the experiment, the CRU-PLL is locked to an external 19.44 MHz reference clock signal generated by a crystal source. The PLL generates a 155.52 MHz clock using the reference clock signal. However, the synthesized 155.52 MHz clock signal is not available at an external pin for analysis. Instead, a 'divide-by-8' of the synthesized clock is available at an external pin.

A sinusoidal signal was ac-coupled into the VCO-control input node of CRU-PLL using a Marconi – 2022D signal generator and an external 0.47 μF capacitor. The spectrum of the 'divide-by-8' clock was observed on a spectrum analyzer. The spectrum of a narrow band FM wave consists of a peak at the carrier frequency f_c. The two side bands are present at f_c +/- f_m. It was observed that the modulation sidebands and the carrier signal were prominently distinguishable. The experimental value of jitter was obtained as follows. If V_n is the amplitude of the sideband and V is the amplitude of the carrier, it is known from the theory of angle modulation [Hyk92] that the relation between modulation index and the amplitudes is given by

$$V_n/V = \Delta f/f_m. \tag{3.19}$$

From Eq. 2.6 we know that

$$J_{pp}\pi = \Delta f / f_m. \tag{3.20}$$

Hence,

$$J_{pp}\pi = \frac{V_n}{V}. \tag{3.21}$$

Since, the readings on the spectrum analyzer were taken in the form of a difference between the amplitudes of the carrier and the sideband (Δ) in dB, Δ is given by

$$\Delta = 20 \log_{10} \frac{Vn}{V} \tag{3.22}$$

or,

$$\frac{V_n}{V} = 10^{\frac{\Delta}{20}}. \tag{3.23}$$

Replacing V_n/V in Eq. 3.23 with Eq. 3.19, yields

$$J_{pp}\pi = 10^{\frac{\Delta}{20}} \tag{3.24}$$

Since, the observed signal is the 'divide-by-8' of the original clock signal, Eq. 3.24 must be modified as

$$J_{pp} = \frac{8 \times 10^{\frac{\Delta}{20}}}{\pi} \tag{3.25}$$

to obtain the jitter on the original clock signal [Ega81]. Eq. 3.25 gives the experimental value of jitter in the p-p form directly from the spectrum analyzer reading of Δ. For the verification of the jitter generation concept, the experimental readings obtained from Eq. 3.25 are compared against the theoretical value obtained using Eq. 3.14, i.e.,

$$J_{pp} = \frac{k_f \times A_m}{\pi \times f_m}. \tag{3.26}$$

Tables 3.4.2, 3.4.3, and 3.4.4 summarize the modulation results at jitter frequencies 5, 2 and 1 MHz respectively. The difference in the theoretical and experimental results can be attributed to the approximations involved in the calculation. For example, it has been assumed that the impedance of the coupling capacitor is very small compared to the output impedance of the LPF, and hence, there is a negligible voltage drop across the capacitor. Since, the output impedance of the LPF is not known precisely, the assumptions leads to some error. The average error in this case is 4.6 %. In a production stage deployment of the scheme, the test limits need to be determined using the results obtained in this section.

Table 3.4.2 Jitter generation comparing predicted and measured values for f_m = 5 MHz.

Modulating Sine Wave Amplitude (rms) (mV)	Δ (dB)	Experimental J_{pp} (UI)	Theoretical J_{pp} (UI)
10	-27.37	0.109	0.113
11	-26.39	0.122	0.123
12	-25.58	0.134	0.135
13	-25.25	0.139	0.146
14	-24.48	0.152	0.157
15	-23.98	0.161	0.169
16	-23.36	0.173	0.180

Table 3.4.3 Jitter generation comparing predicted and measured values for f_m = 2 MHz.

Modulating Sine Wave Amplitude (rms) (mV)	Δ (dB)	Experimental J_{pp} (UI)	Theoretical J_{pp} (UI)
1	-39.80	0.026	0.028
2	-33.96	0.051	0.056
3	-30.16	0.079	0.084
4	-27.29	0.110	0.113
5	-25.38	0.137	0.140
6	-24.48	0.152	0.169
7	-22.63	0.188	0.197

Table 3.4.4 Jitter generation comparing predicted and measured values for f_m = 1 MHz.

Modulating Sine Wave amplitude (rms) (mV)	Δ (dB)	Experimental J_{pp} (UI)	Theoritical J_{pp} (UI)
1	-33.47	0.054	0.0562
2	-27.00	0.113	0.1125
3	-24.48	0.152	0.1688

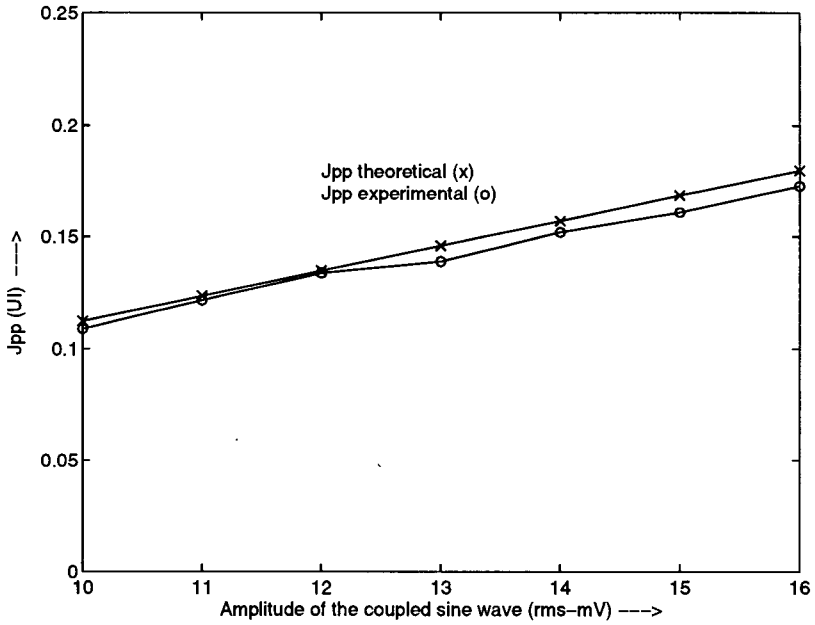

Figure 3.4.16 Experimental vs. theoretical results (5 MHz).

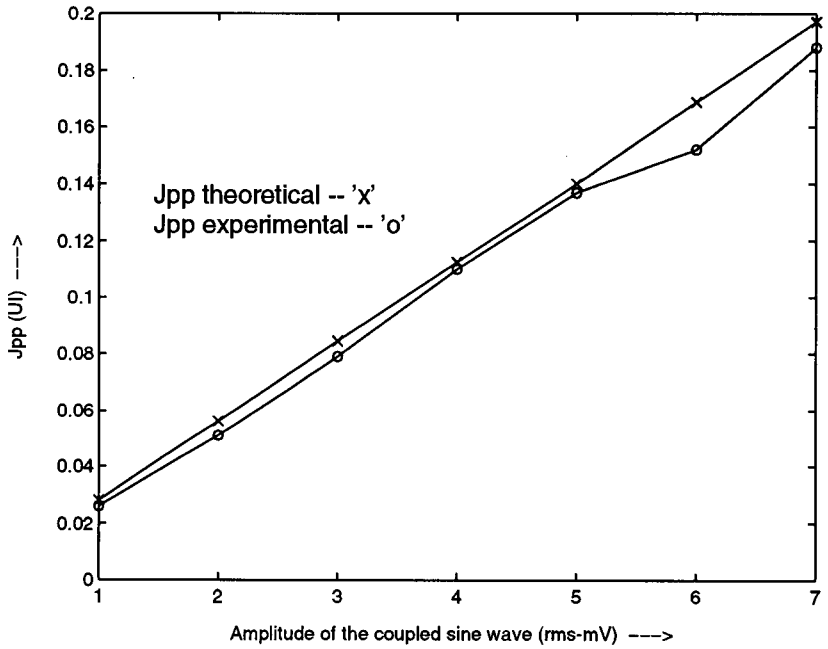

Figure 3.4.17 Experimental vs. theoretical results (2 MHz).

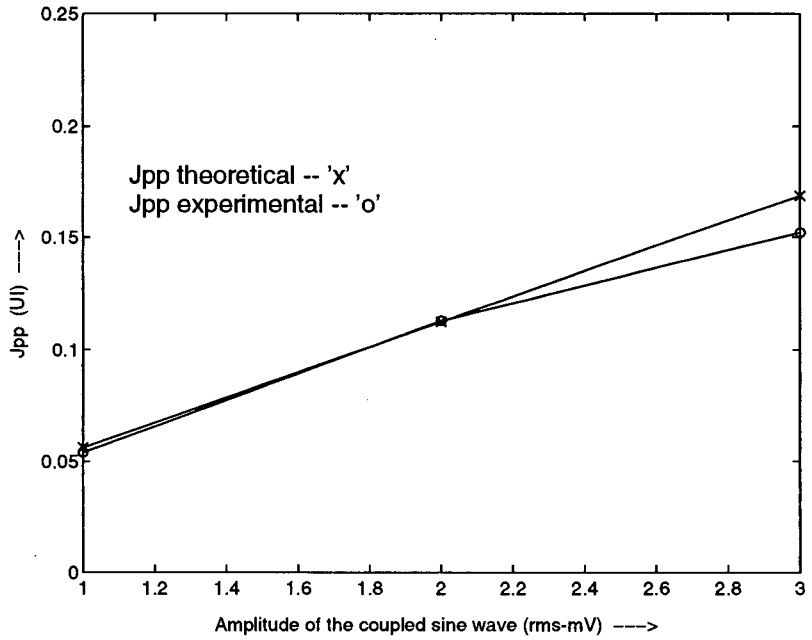

Figure 3.4.18 Experimental vs. theoretical results (1 MHz).

3.5 Variations of the BIST Scheme

The proposed scheme can be varied to suit the implementation needs. Some possible variations of the scheme are described below. Another variation of the scheme in the form of a frequency test is presented in Appendix G.

3.5.1 A Reduced-Set Jitter Tolerance Test

The basic BIST scheme presented so far in this chapter is designed to mimic the natural and straight-forward test flow that would be carried out with the external test equipment. The major difference between the testing using external test equipment and the BIST scheme is not in the basic procedure, but in the location of test components and the speed of overall operation. Even with the presented BIST scheme, one is required to test the DUT for the complete range of frequencies and jitter amplitudes specified in the SONET template. This

may still be unacceptable due to long test times implied by the low jitter frequencies. For example, a single test at a frequency of 100 Hz requires a minimum of 10 ms (1 period) plus the setup time of the test equipment.

In this section, we develop an algorithm to decrease the number of test sets for a complete jitter tolerance test. First of all, we observe that a PLL is able to maintain lock in the presence of sinusoidal modulation at its input as long as the maximum frequency deviation ($\Delta\omega_i$) at the input does not exceed the lock-in range of the PLL [Wol91], i.e.,

$$\Delta\omega_i \leq \omega_L. \tag{3.27}$$

For a multiplier type PD, the relation between the lock-in range and the bandwidth k is given by

$$\omega_L = k\frac{\pi}{2}. \tag{3.28}$$

Hence, Eq. 3.27 can be rewritten as

$$\Delta\omega_i = k\frac{\pi}{2}. \tag{3.29}$$

Eq. 3.29 implies that the PLL will be able to track any frequency modulation producing a maximum frequency deviation less than or equal to $k\pi/2$. For jitter tolerance tests, jitter on the clock is essentially angle modulation. Hence, if a test were performed at a certain jitter amplitude and frequency that produced a given frequency deviation $\Delta\omega$, the particular test would cover all the jitter amplitude-frequency pairs which produce a deviation less than $\Delta\omega$.

Next, we calculate the frequency deviations at various points in the jitter tolerance template for SONET OC-3. The obtained values are shown in Table 3.5.5.

Table 3.5.5 Calculation of the maximum frequency deviation.

Jitter amplitude (UI-pp)	Jitter frequency	Δf ($\Delta\omega/2\pi$)
15	10 Hz	471 Hz
15	30 Hz	1413.7 Hz
1.5	300 Hz	1413.7 Hz
1.5	6.5 kHz	30.63 kHz
0.15	65 kHz	30.63 kHz
0.15	1 MHz	471 kHz
0.15	5 MHz	2.356 MHz

It is observed that the jitter amplitude-frequency pair of 1.5 UI at 6.5 kHz produces a frequency deviation of 30.63 kHz. The jitter amplitude-frequency pair of 0.15 UI at 65 kHz also produces a frequency deviation of 30.63 kHz. At frequencies lower than 65 kHz, all the amplitude-frequency pairs produce a maximum frequency deviation of less than or equal to 30.63 kHz. This suggests that the test at the amplitude-frequency pair of 65 kHz and 0.15 UI jitter will cover all the frequencies lower than 65 kHz. It can be noted that the frequency amplitude pair at 5 MHz and 0.15 UI jitter produces the maximum frequency deviation among the values considered in Table 3.5.5 but it is not chosen as the test point that can cover all frequencies lower than 5 MHz due to the reason explained below.

Most practical PLLs designed for clock recovery applications at the clock speeds under consideration are narrow-band PLLs and do not have the bandwidth in the order of MHz [Wol91]. This essentially means that they will not track the modulation at frequencies in the MHz range for the amplitudes specified in the template. However, this does not cause any bit errors as the PLL is not required to track the modulation in order to achieve zero bit errors as long as the jitter amplitude is less than 1 UI. In the case of jitter amplitude less than 1 UI, the bit error depends on the useful range of the phase-detector. The concept is better understood by observing the error response of the PLL, which is given by

$$\frac{\Theta_e(s)}{\Theta_i(s)} = H_e(s) = 1 - H(s) = \frac{1}{1 + G(s)}. \tag{3.30}$$

The phase error function, $H_e(s)$, is plotted for the PLL under consideration in Fig. 3.5.19. It is observed that the magnitude of $H_e(s)$ is approximately equal to 1 for all frequencies higher than the PLL bandwidth. This means that, for these frequencies,

$$|\Theta_e| \approx |\Theta_i|. \tag{3.31}$$

An interpretation of Eq. 3.31 is that the PLL is not able to decrease the phase error by tracking the input phase and all of the input phase is appearing as the phase error at the output of phase detector. There will be no bit errors as long as the phase error does not exceed the linear range of the phase detector. Hence, from a PLL's point of view, a given jitter amplitude at all frequencies greater than the PLL bandwidth displays the same behavior, i.e., the behavior of the PLL is given by Eq. 3.31. This, in turn, indicates that a test at any frequency much higher than the PLL bandwidth will cover all the frequencies in that

range. This is the most likely reason behind the fact that the jitter tolerance template does not specify the highest frequency at which the tests should be carried out.

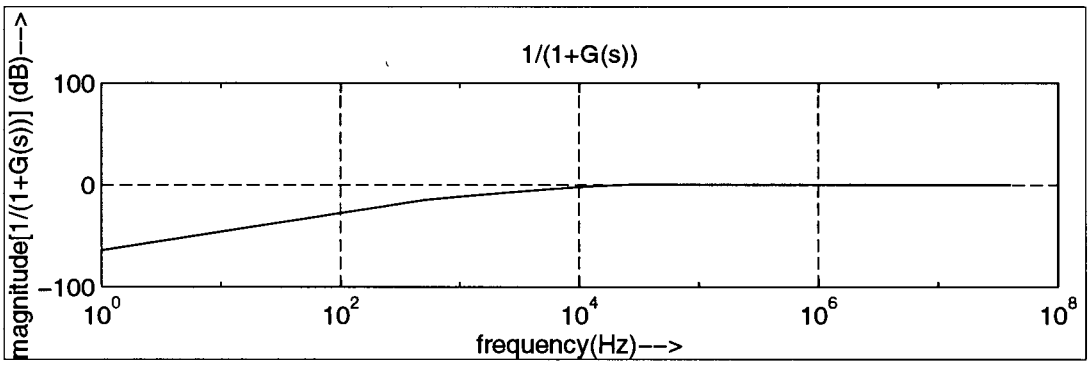

Figure 3.5.19 Phase error response of the PLL.

Thus, by choosing two points on the template, one at jitter amplitudes greater than 1 UI and producing the highest frequency deviation in that range, and another point at an arbitrary frequency higher than the PLL bandwidth, the complete template can be covered. In the particular case of OC-3, the highest frequency deviations for the jitter amplitude-frequency pair of 1.5 UI at 6.5 kHz and 0.15 UI at 65 kHz happen to produce the same maximum frequency deviation (30.63 kHz from Table 3.5.5). Hence, instead of choosing the first point in the amplitude range > 1 UI, the 65 kHz point can be chosen as the first point. This will result in a faster test as the time required for a test at 65 kHz is lesser than the time required for a 6.5 kHz test due to the longer time period of a 6.5 kHz signal.

The preceding discussion holds for overdamped and critically damped PLLs [Wol91] [Gar79] and may hold for some PLLs with a low degree of underdamping. If the PLL is highly underdamped, the peaking behavior [Wol91] of the closed-loop system becomes prominent and causes the PLL to be less tolerant to jitter in the vicinity of the peaking

frequency as compared to the jitter at neighboring frequencies. If a test is not performed in the vicinity of the peaking frequency, the results of the overall test may be misleading. Hence, the above methodology may not hold for some PLLs. A discussion on the damping behavior of PLLs can be found in [Wol91], [Gar79] and [Bes84].

3.5.2 Lock-in Range Test

As mentioned in the previous subsection, a PLL can maintain lock in the presence of a sinusoidal FM if the condition in Eq. 3.27 is satisfied [Wol91], i.e.,

$$\Delta\omega_i \leq \omega_L \tag{3.32}$$

where $\Delta\omega_i$ is the input frequency deviation due to modulation, and ω_L is the lock-in range of the PLL. Hence, if the lock-in range of the PLL is known, the maximum frequency deviation that the PLL can sustain can be determined. The maximum frequency deviation can, in turn, be used to calculate the jitter tolerance of the PLL for jitter amplitudes higher than 1 UI, as explained in Section 3.5.1. A complete jitter tolerance test can be performed by performing a test that determines the lock-in range of the PLL (and the jitter tolerance for jitter > 1UI) and a second test same as the high frequency test explained in the previous subsection. The lock-in range test can be easily performed by supplying the CRU with data at a higher rate than the nominal frequency and observing the bit-errors at its output. The highest frequency at which the PLL acquires lock without bit-errors is its lock-in range.

The data at a higher frequency than the nominal frequency can be obtained by adding a dc signal to the VCO input of a CSU PLL. However, the capacitive coupling used for the BIST scheme cannot be used for adding the dc signal to the VCO input as a capacitor blocks

the dc signal. The dc signal can be added to the VCO by using an op-amp based adder. The cost of the adder can be justified by the fact that now only dc signals are required as opposed to the sinusoidal signal at low frequencies.

3.5.3 Conclusions

The following summarizes the relative hardware requirements and the merits and demerits associated with the basic BIST scheme and its variations.

(a) The basic BIST scheme : The basic BIST scheme requires the longest test time and the largest area overhead among the presented schemes. However, the basic scheme meets the formal requirements of a jitter tolerance test (SONET jitter tolerance test as specified by [Syn94]).

(b) The reduced-set BIST scheme : The reduced-set jitter tolerance scheme requires the same amount of hardware overhead as the basic scheme, but a significant reduction in the overall test time is achieved. The scheme is not the formal jitter tolerance test. However, it can be used as a production stage jitter tolerance test and is a promising alternative to the basic BIST scheme.

(c) The lock-in range test : The lock-in range test requires the overhead of an adder and a variable dc voltage source. The area overhead for this test is slightly less than previous two schemes and this also is not the formal jitter tolerance test.

Chapter 4
A BIST Scheme for Jitter Measurement in DSP-Based Mixed-Signal ICs

The majority of mixed-signal systems being integrated onto single ICs are digital signal processing (DSP) based systems [Meh93]. Examples of such mixed-signal DSP-core ICs are coder-decoders (CODECs) and single chip modulator-demodulators (MODEMs) [Ter93]. With the increasing integration and emergence of new challenges for test engineers, the attention of researchers has been drawn towards the development of test methodologies for this class of circuits [Ton93] [Meh93] [Ter93]. Teroaka et al. [Ter93] presented a BIST scheme for testing analog-to-digital convertors (ADCs) found in a CODEC IC consisting of a 24–bit floating point DSP-core, a 13–bit ADC, a 13–bit DAC (digital-to analog convertor), a 6K-word read only memory (ROM) and a 3.5K-word random access memory (RAM). Toner et al. [Ton93] presented a BIST scheme for the SNR test of a generic mixed-signal IC with a DSP-core. Fig. 4.1 shows a generic mixed-signal DSP-core IC. Typically, over 60% of the total IC area in such ICs is occupied by digital circuits [Meh93]. The major analog and mixed-signal components on these ICs tend to be analog-to-digital and digital-to-analog convertors, PLLs, op-amps and filters. Sampling is an integral and important part of these systems. The sampling accuracy plays a major role in the functionality of these ICs, and, is in turn, highly dependent on the accuracy of the sampling clock.

Issues such as frequency stability and accuracy of the clock signal determine the quality of measurements in DSP-based systems [Meh93]. Hence, testing for clock accuracy is critical for such systems. This chapter presents a BIST scheme for measuring the jitter of clock signals in DSP-core mixed-signal ICs. First, a review of the prevalent methods of the analysis of jitter in sampling-based systems is presented. Following this, the concept underlying the proposed BIST scheme is established. Finally, the BIST scheme is described, along with simulation and hardware experiment results.

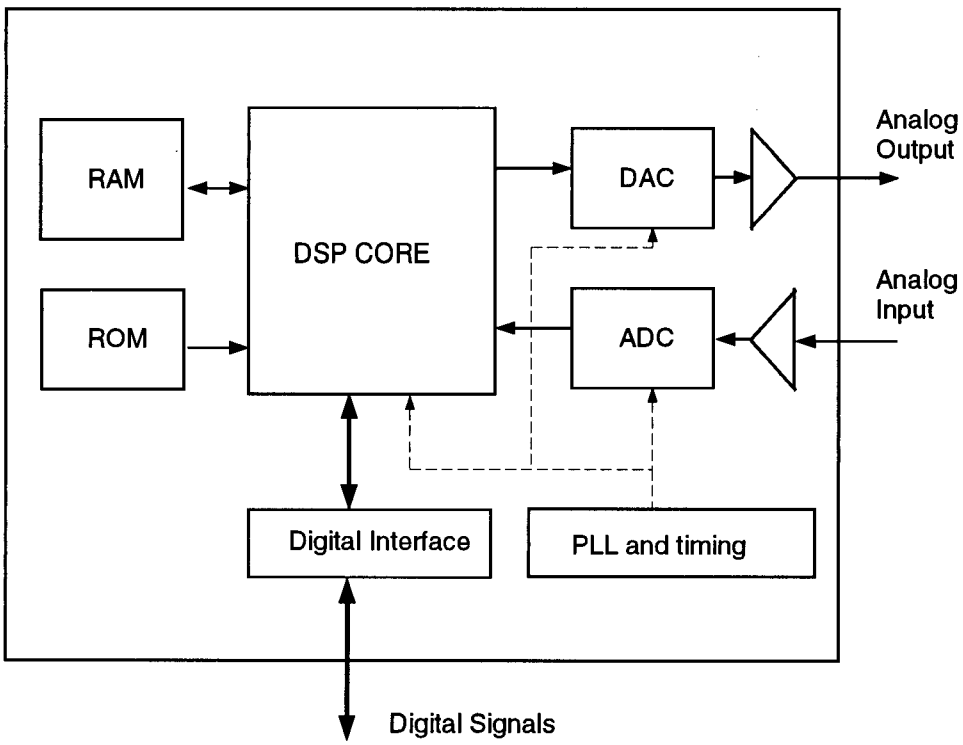

Figure 4.1 A DSP-based mixed-signal IC.

4.1 Jitter Characterization

Most of the recent efforts towards the analytical characterization of jitter in a sampling-based system are based on the time domain representation of jitter. These efforts can be

broadly classified into two categories: jitter represented as a case of (i) uniform, and (ii) non-uniform sampling. Jenq [Jen188, Jen288 and Jen90] treats the analysis of jitter as a case of non-uniform sampling. Wagdy et al. [Wag90], and Souders et al. [Sou90] treat jitter as a case of uniform sampling. Wagdy et al. [Wag91] presented a comparison of jitter characterization using uniform and non-uniform sampling approaches. Both of these approaches are based on characterizing jitter by an arbitrary probability distribution function. In most cases, jitter has been assumed to be a random variable with a symmetrical distribution. Next, we present a brief review of these two methods of jitter analysis.

As the names suggest, the two methods of analysis of jitter primarily differ in their representation of the sampling and the sampled signals. Non-uniform sampling is a more intuitive approach for representing jitter as a jittered clock essentially has non-uniform time periods. Jenq [Jen188] presents a comprehensive analysis of jitter using the non-uniform sampling representation. He presents a generic expression for the spectral representation of non-uniformally sampled signals. From the spectral representation, he derives expressions for the SNR of the sampled signal. If r_m is the jitter on the m^{th} sampling edge of a sampling signal with a frequency f_s or a nominal time period T, then r_m in UI is given by

$$r_m = \frac{\Delta t_m}{T} = \frac{mT - t_m}{T} \tag{4.1}$$

where t_m is the actual time instant corresponding to the significant edge of the m^{th} time interval [Jen188 & Jen90]. Fig. 4.1.2 illustrates the representation for the case of random jitter.

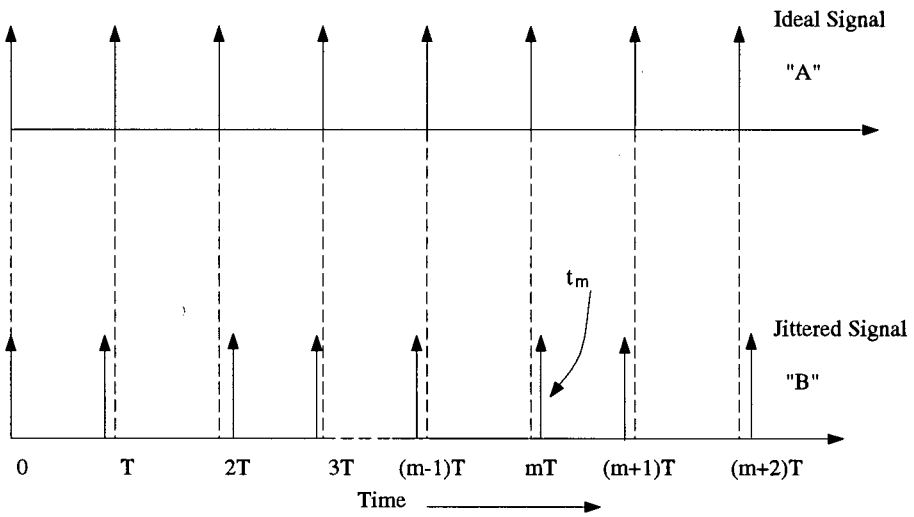

Figure 4.1.2 Illustration of jitter on the m[th] sampling edge.

For the treatment of jitter as a case of uniform sampling, the jittered clock is treated as though it were ideal and the jitter is added to the phase component of the sampled signal. If the sampled signal is a sinusoid, then the n^{th} sample of the signal, v_n, is given by

$$v_n = sin\left(\frac{2\pi n}{M} + J_n\right) \tag{4.2}$$

where J_n is the jitter on the n_{th} sample and M is the number of samples per cycle [Wag91]. For the particular case of a sinusoid $\left(e^{j\omega_0 t} - e^{-j\omega_0 t}\right)/2$ being the sampled signal, where ω_o is the angular frequency of the sinusoid, it has been shown by Wagdy et al. [Wag91] that for a jitter J_n with zero mean and symmetrical distribution, the SNR is given by

$$SNR = \frac{N}{(N-2)\sigma^2} \tag{4.3}$$

where N is the number of samples in the FFT and σ is the standard deviation of the jitter.

It has been further shown by Wagdy et al. [Wag91] that for the same sinusoid, the non-uniform sampling representation as described earlier also results in the SNR given by Eq. 4.3. The two approaches discussed above, i.e., the uniform and the non-uniform sampling approach, have been used to calculate the SNR and the variation of the jitter from the calculated SNR. In the cases where peak-to-peak jitter measurement is desired, the above approaches cannot be used directly.

4.1.1 The Basis of the BIST Scheme

Recognizing the drawbacks of the above mentioned approaches for the measurement of peak-to-peak jitter, we analyze the sampling clock jitter in terms of the angle modulation. Let a sinusoid given by

$$v_{ref}(t) = A_{ref} \cos\left(2\pi f_{ref} t\right) \tag{4.4}$$

where A_{ref} is the amplitude and f_{ref} is the frequency, be sampled using a jittered clock. Let the nominal frequency of the jittered clock be f_s and the nominal time period be T. Let the clock be jittered by a sinusoid such that the n^{th} sampling time instant, nT', be given by

$$nT' = nT + k\cos\left(2\pi f_j nT\right) \tag{4.5}$$

where f_j is the jitter frequency and k is a constant. When the jittered clock represented by Eq. 4.5 is used to sample the sinusoid in Eq. 4.4, the n^{th} sample of the sinusoid is given by

$$v_{ref}\left(nT'\right) = A_{ref} \cos\left(2\pi f_{ref} nT'\right) \tag{4.6}$$

Replacing the value of nT' from Eq. 4.5 into Eq. 4.6, we get

$$v_{ref}\left(nT'\right) = A_{ref} \cos\left(2\pi f_{ref} nT + k2\pi f_{ref} \cos\left(2\pi f_j nT\right)\right) \tag{4.7}$$

If the constant $k.2\pi.f_{ref}$ is represented by another constant k', then the Eq. 4.7 can be rewritten as

$$v_{ref}\left(nT^{'}\right) = A_{ref}\cos\left(2\pi f_{ref}nT + k^{'}\cos\left(2\pi f_j nT\right)\right) \tag{4.8}$$

Now, let us consider another angle modulated sinusoid

$$v_{ref'}(t) = A_{ref}\cos\left(2\pi f_{ref}t + k_a\cos 2\pi f_j t\right) \tag{4.9}$$

with a frequency f_{ref} and the modulating frequency f_j. k_a is the phase modulation index. If the signal in Eq. 4.9 is sampled using an ideal clock with a nominal time period T, then the n^{th} sample of the signal is given by

$$v_{ref'}(nT) = A_{ref}\cos\left(2\pi f_{ref}nT + k_a\cos\left(2\pi f_j nT\right)\right). \tag{4.10}$$

From Eqs. 4.8 and 4.10, it is evident that they both represent an angle modulated signal sampled with an ideal clock. This indicates that when a pure sinusoid is sampled with an angle modulated clock, the sampled version of the sinusoid represents an angle modulated sinusoid sampled with an ideal clock. However, the relation between the constants determines the amplitude of the jitter on the sampled signal. Thus, if the relation between the angle modulation constants is known, the modulation of the clock signal can be calculated from the modulation information of the sampled signal. In a sampling process, frequency division is inherent [Ega81]. Since the phase of the modulated sampling signal is transferred to the output only at sampling instants, similar to the process of frequency division, the low frequency modulation is transferred to the sampled signal. Hence, if the sampling clock is modulated with a low frequency signal, the sampled signal gets modulated by the signal of

the same frequency. Due to the inherent frequency division, the modulation index of the sampled signal is decreased by a factor equal to the ratio of the sampled frequency to the sampling frequency [Ega81]. Hence, by measuring the frequency modulation parameters of the sampled sinusoid, the modulation of the clock can be calculated. The BIST scheme presented next relies on this principle.

4.2 The BIST Scheme

A BIST scheme proposed in [Ton93] makes use of an on-chip analog stimulus generator and on-chip DSP resources to perform the SNR test of an ADC. An on-chip stimulus generator is used to obtain a known signal which is sampled using an ADC and a system clock. A Fast Fourier Transform (FFT) is performed on the sampled signal to obtain the SNR. This SNR serves as a figure of merit for the ADC. In such an SNR calculation, the jitter information is lost due to the summation of frequency contents other than the signal frequency. Our BIST scheme is based on analysis of the FFT results from the point of view of angle modulation and thus yields jitter information.

The BIST is conducted through the following steps - (I) the digital circuitry of the IC is tested using conventional digital BIST or tester–based techniques, (II) a low frequency signal is generated using a stimulus generator, (III) the low frequency signal is sampled by an ADC, (IV) an FFT is performed on the sampled signal, (V) a peak search is performed on the FFT results to identify signal and highest jitter components, (VI) p-p value of jitter is calculated. The block diagram of the BIST scheme is shown in Fig. 4.2.3.

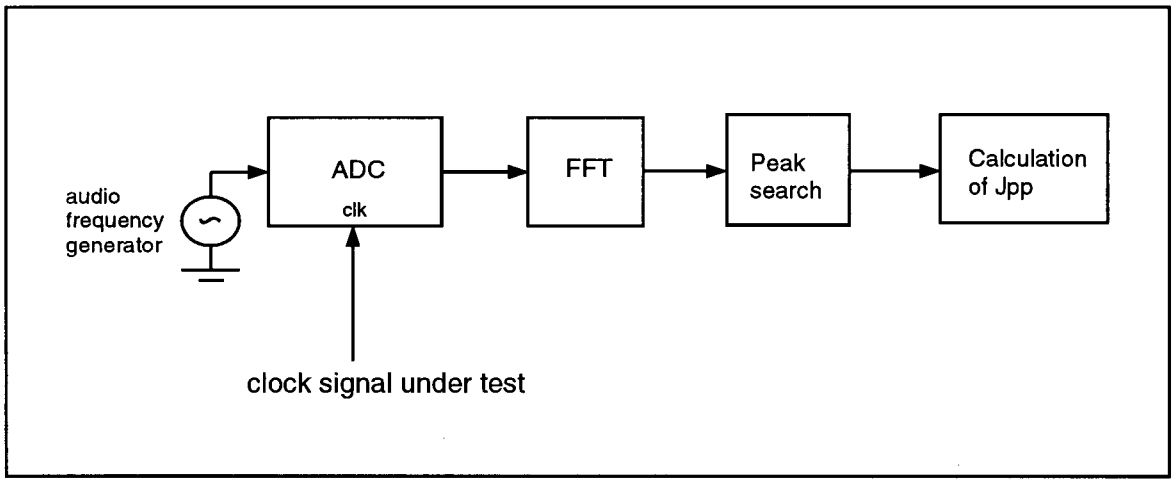

Figure 4.2.3 The block diagram for BIST.

The following describes the steps involved in the BIST in detail.

STEP I : The digital circuitry on the IC is tested before the actual jitter test is performed. This is necessary as the BIST scheme makes use of the digital components of the IC. The digital circuitry can be tested using a number of well established techniques such as scan and digital BISTs using pseudo-random test patterns [Wil82]. The digital circuitry can also be tested using ATEs commonly found in the industry.

STEP II : A sinusoid of known amplitude and frequency is generated on chip. The generation of such stimulus is now possible on the chip itself with the introduction of architectures focused on testing. An example of such a generator can be found in [Lu94]. Lu et al. have presented a signal generator designed specifically for mixed-signal testing.

STEP III : The stimulus (sinusoid) generated by the on-chip generator is supplied to the analog input of the ADC. The sampling clock of the ADC is chosen to be the clock signal under test. The samples of the sampled sinusoid are stored in the on-chip RAM. As mentioned earlier, a RAM is normally found on the class of ICs being considered.

STEP IV : An FFT is performed on the sampled waveform stored in the RAM in Step III. Again, most programmable DSP based ICs are capable of performing an FFT [Ter93]. The results of the FFT are stored in the RAM.

STEP V : A peak search is performed on the results of the FFT stored in the RAM (from Step IV). The highest magnitude among the stored results normally corresponds to the frequency of the sampled signal. The next highest magnitude corresponds to the peak jitter frequency. These two magnitudes are recorded in the memory. The sampled waveform record and the other magnitudes obtained as a result of the FFT are discarded.

STEP VI : The peak jitter on the sampling clock is calculated from the amplitudes recorded in Step V as follows.

Let the sampled sinusoid be the reference sinusoid with a frequency f_{ref} and a unity amplitude. From Chapter 3, for a case of sinusoidal jitter, J_{ppref}, the p-p jitter on the reference signal (sampled signal) in UI (unit interval), is given by

$$J_{pp_{ref}} = \frac{\Delta f_{ref}}{\pi f_j} \tag{4.11}$$

where Δf_{ref} is the peak frequency deviation of the carrier (sampled signal) and f_j is the jitter frequency. Eq. 4.11 can be used to obtain the magnitude of jitter on the sampled signal in the peak-to-peak form. Also, it is known from the theory of angle modulation that, for small values (<0.8) of β (modulation index), the relation between β and the amplitudes of the sidebands is given by [Hyk92]

$$\beta = \frac{\Delta f_{ref}}{f_j} = \frac{V_p}{V} \tag{4.12}$$

where V_p is the amplitude of the sideband and V is the amplitude of the carrier frequency component. From Eqs. 4.11 and 4.12, we obtain

$$J_{pp_{ref}} = \frac{V_p}{\pi V}. \tag{4.13}$$

Eq. 4.13 is used to obtain the amplitude of jitter on the reference signal, from the results of the FFT. To obtain the jitter parameters for the clock signal under test, the process of frequency division must be taken into account, as explained in the previous section. Hence, to account for the frequency division, multiplying the jitter in Eq. 4.13 by f_s/f_{ref} gives the jitter on the sampling clock, i.e.,

$$J_{pp} = J_{pp_{ref}} \times \frac{f_s}{f_{ref}} \tag{4.14}$$

or,

$$J_{pp} = \frac{V_p}{\pi V} \times \frac{f_s}{f_{ref}}. \tag{4.15}$$

The experimental peak-to-peak jitter is calculated from Eq. 4.15. V_p and V are obtained from the results of the FFT by performing a peak search (Step V above). f_s and f_{ref} are known constants. Since, the scheme is targeted towards the measurement of the peak value of jitter, only the highest jitter amplitude is considered and other frequency (jitter) components are not considered.

The overhead required for the BIST scheme includes the signal generator, the control circuitry, and the ROM area for storing the test routine. The overhead of the signal generator

can be justified by the recognition of the fact that the generator can be shared by other tests such as the signal-to-noise ratio (SNR) test presented in [Ton93]. The control circuitry required for the BIST is not likely to be excessive. The ROM area for storing the test routine can be justified if the FFT routine is considered a part of normal functionality of the IC. If this is the case, the peak search routine will be the ROM overhead. The peak search routine is normally simple and does not require unacceptable overhead. The total overhead is specific to the implementation and depends on the size of the basic IC. With the above restrictions, the presented scheme can be used as a production stage BIST. However, the presented BIST scheme does not apply to the cases which include excessive noise from other sources such as amplitude noise and quantization noise. In such cases, the noise from other sources may be mistaken for jitter.

4.2.1 Simulation

To verify the scheme, a relatively new method of simulation was chosen. The circuit shown in Fig. 4.2.4, comprised of two types of models, was used to simulate the scheme. The ADC block was written in an analog hardware description language (AHDL) [Spt94]. The voltage-controlled oscillator (VCO) and sinusoidal generators were taken from the "Functional" library in Cadence [Ana94]. These blocks have been realized using controlled sources. The circuit was simulated using the Spectre simulator [Spr94]. The FFT was performed using the built-in Discrete Fourier Transform (DFT) capability of the Analog Artist simulation interface [Ana94].

Frequency modulation was performed using the VCO to simulate a clock with known jitter. The modulating signal was supplied as the control voltage to the VCO. The detailed

circuit diagram is given in Appendix B, Fig. B.5.

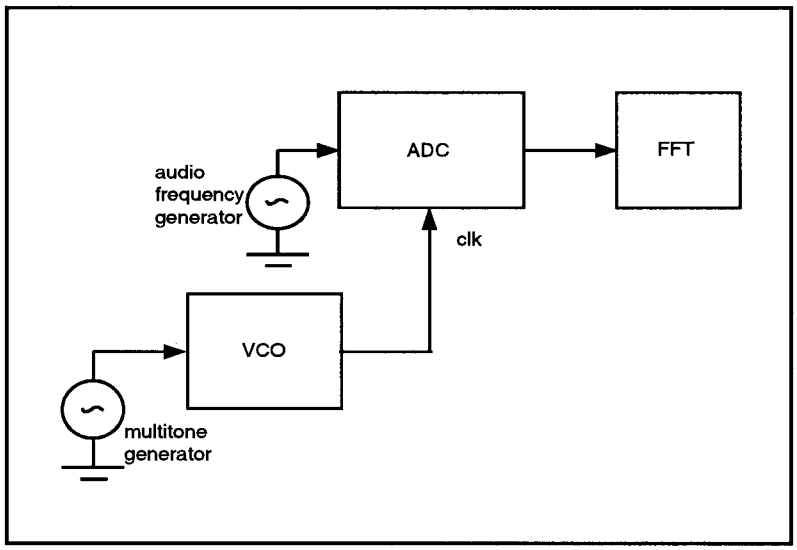

Figure 4.2.4 The simulation block diagram.

Fig. 4.2.5 shows an FFT plot of the reference signal sampled by the jittered clock. In this case, the frequency of the reference sinusoid is 10 MHz. The jitter frequency was chosen to be 200 kHz. The clock frequency was chosen to be 100 MHz. It is observed that the jitter components at 10.2 and 9.8 MHz are discernible. The VCO gain was 10 MHz/V and the length of the FFT was 1024. The amplitudes of 200 kHz signal was chosen to be 10 mV. The corresponding β is 0.5.

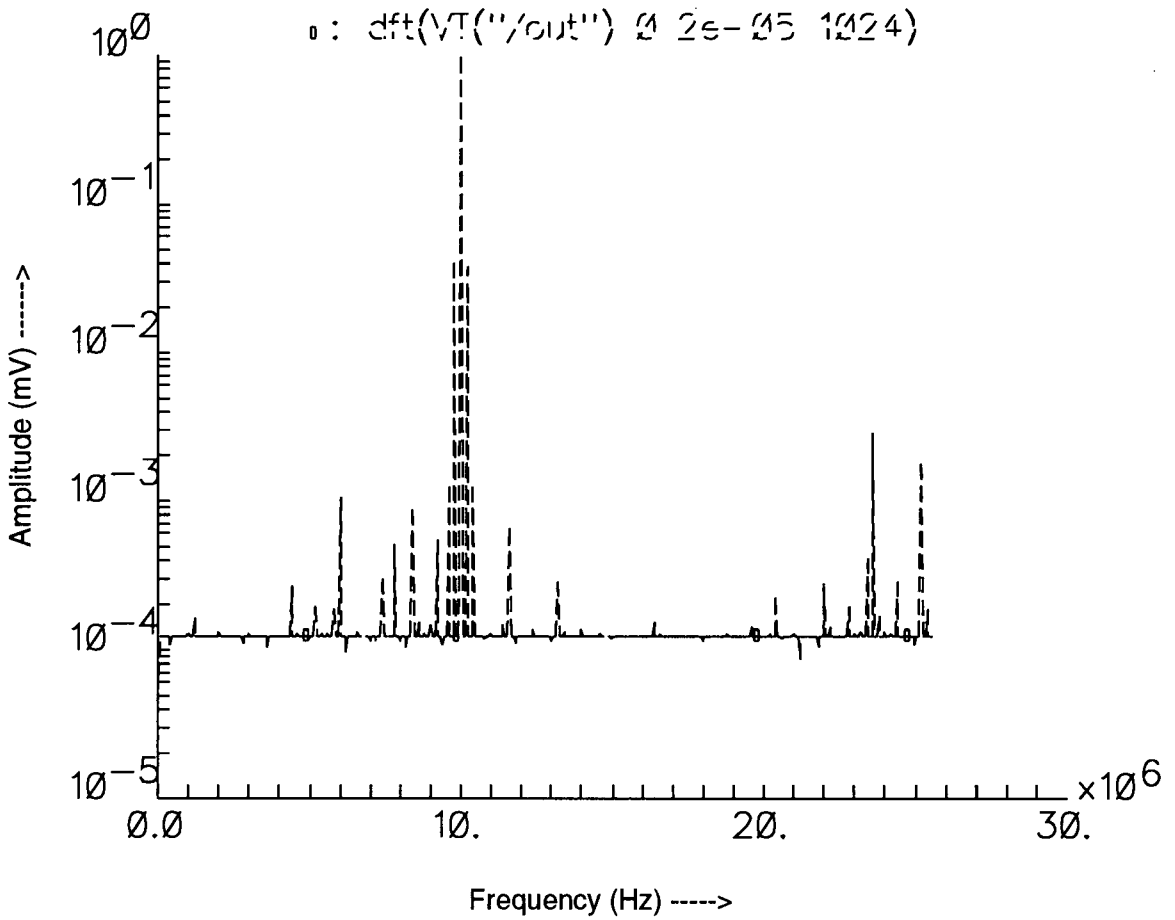

Figure 4.2.5 Jitter spectrum with AHDL simulation.

4.2.2 Hardware Verification

The experimental verification of the BIST scheme was done on HP75000 D20 system using the VEETEST mixed-signal test environment [Vee95, D2092]. Fig.4.2.6 shows the setup used to perform the experiment. The ADC used was the HP a1430 [Adc94] module. The reference signal was supplied by the HP E1445a function generator which is a part of the HP75000 D20 system. The frequency modulated clock signal was obtained directly from an HP 33120a function generator. A separate FFT block was not required for this case

as the spectrum display block includes the FFT processing. The external generator is not shown in Fig. 4.2.6.

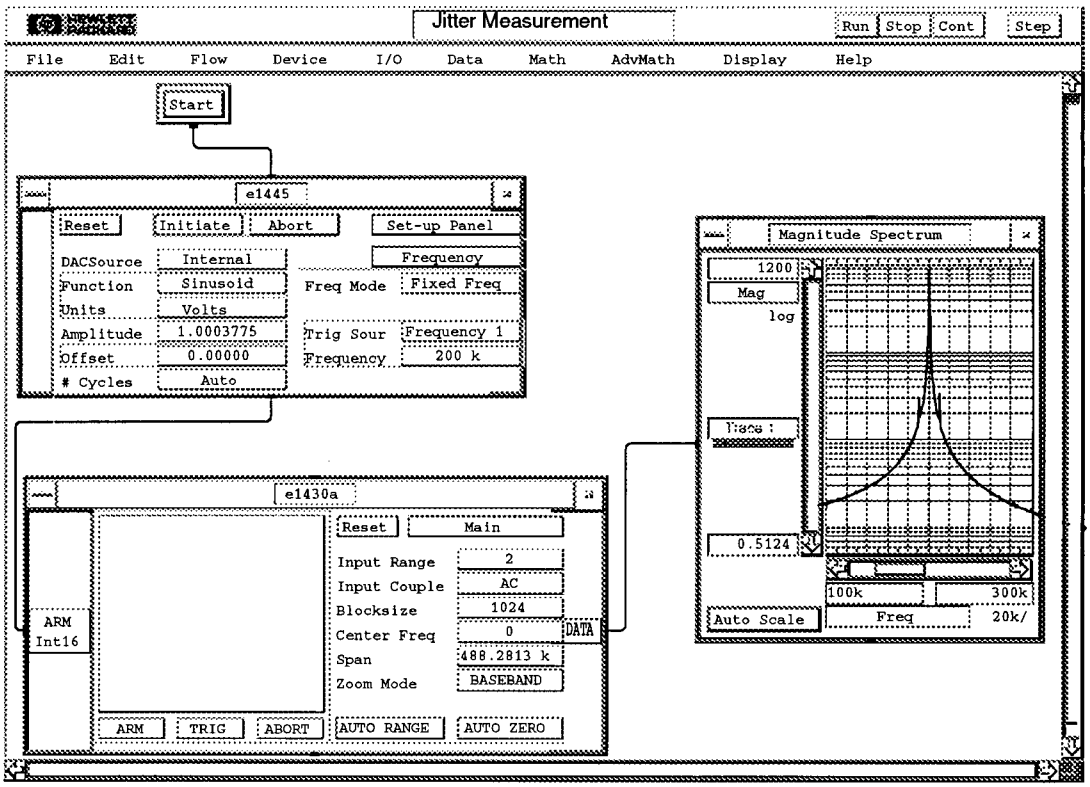

Figure 4.2.6 Experimental setup for the BIST scheme.

A sinusoid of unity amplitude and a frequency of 200 kHz was sampled using the system's ADC with a jittered clock signal. A frequency modulated clock signal was supplied to the ADC as a jittered clock. The unmodulated clock frequency was 10 MHz. The modulation of the clock signal was performed using a sinusoid of 10 kHz frequency for various values of Δf. The experimental jitter amplitude is obtained from Eq. 4.15 and is compared with the theoretical amplitude calculated using Eq. 3.14, i.e.,

$$J_{pp} = \frac{k_f \times A_m}{\pi \times f_m} \tag{4.16}$$

The experimental and theoretical amounts of jitter are summarized in Table 4.2.1. It is

Table 4.2.1 Experimental results

fc (MHz)	Δf (kHz)	fm (kHz)	V (mV)	Vp (mV)	calculated Jpp (UI)	experimental Jpp (UI)
10	10	10	998	18.9	0.318	0.301
10	15	10	998	30.1	0.477	0.480
10	20	10	998	39.6	0.636	0.631
10	25	10	998	47.9	0.796	0.763
10	30	10	998	54.7	0.955	0.872

observed that the theoretical and experimental results are in close agreement. It is also observed that at higher jitter amplitudes, the amount of error is more than the lower amplitudes. This is due to the fact that the calculations presented in this chapter are not valid for the high values of angle-modulation index (>0.8) due to the side bands that result at higher modulation indices [Hyk92]. The results are plotted in Fig. 4.2.7. The FFT plot obtained by sampling the sinusoid with a frequency modulated clock signal is shown in Fig. 4.2.8. The modulation sidebands are easily separable from the rest of noise. In the case shown here, the reference frequency was 200 kHz, the modulation frequency was 10 kHz and frequency deviation was 30 kHz.

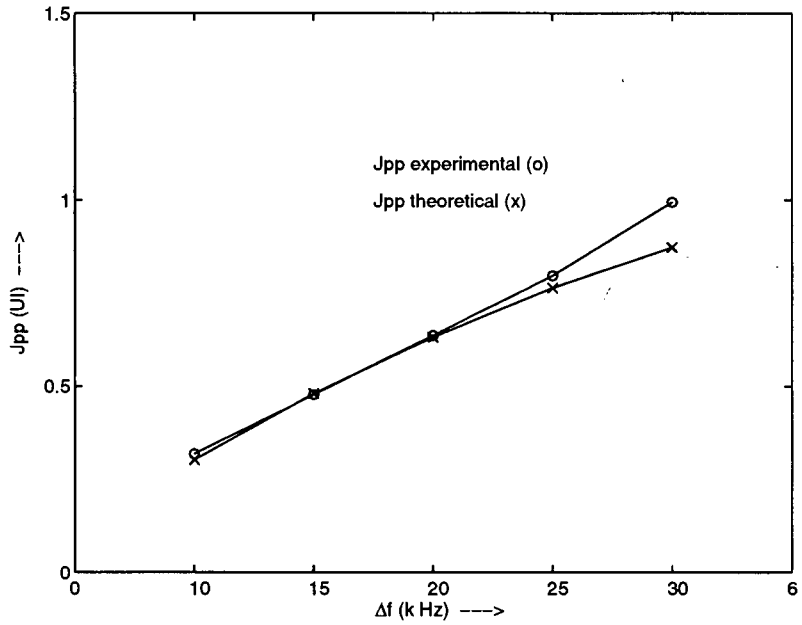

Figure 4.2.7 Theoretical vs. experimental results.

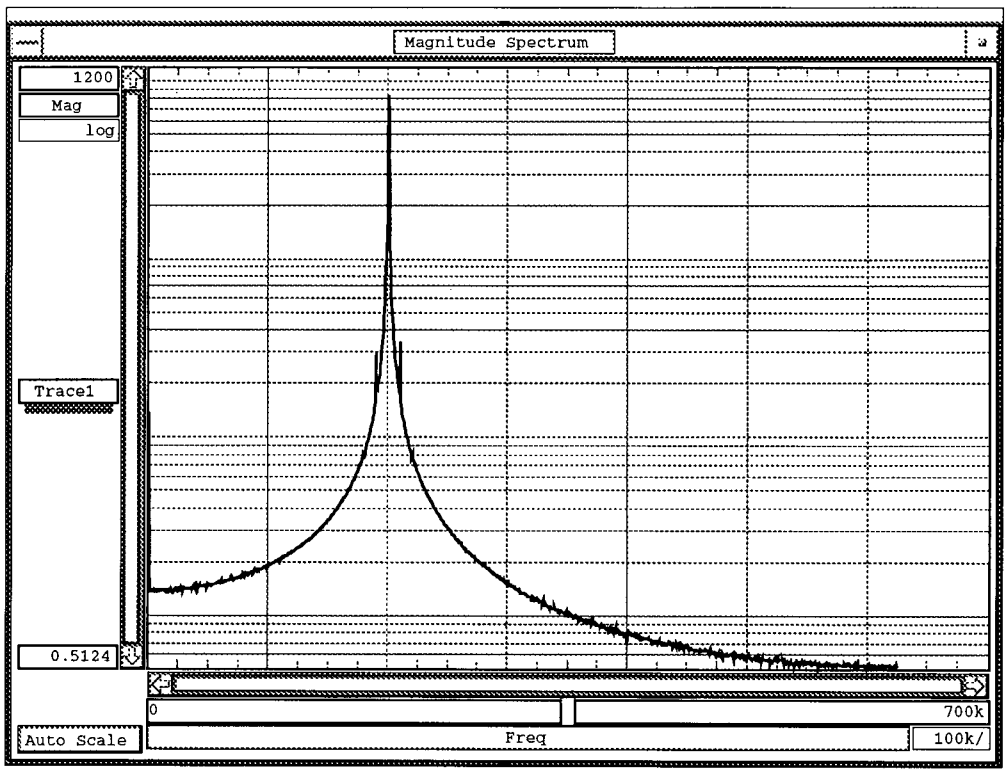

Figure 4.2.8 FFT plot of the sampled sinusoid.

Chapter 5
Conclusions and Future Work

5.1 Conclusions

In this thesis, the problems and issues that beset clock jitter testing of ICs have been outlined. Along with an overview of jitter, two non-traditional and novel BIST schemes have been presented. The thesis focuses on developing test schemes to overcome the limitations of ATEs.

A novel method of performing a jitter tolerance test of clock and data recovery units is presented. The scheme uses low overhead. The approach is to use the pre-existing blocks on an IC for the test purposes. Specifically, it has been demonstrated that the clock synthesis units, in conjunction with a pseudo-random data source, can be used as an effective source of jittered data. The method provides easy control over the jitter supplied to the CRU. In a specific case, it has been shown that the scheme can be implemented with the overhead of a signal generator and a capacitor.

The results obtained through theoretical calculations and simulations of the BIST scheme have been found to be in close agreement with each other, thus providing a proof of concept. The most critical aspect of the presented scheme, i.e., the generation of the jittered clock, was verified in hardware. The results demonstrate the effectiveness of the method for generating jittered clock signals. Variations of the principal method in the forms of the reduced-set jitter tolerance test, the lock-in range test and the frequency test (Appendix G) have also

been presented. The mathematical analysis and a numeric example have been used to substantiate the viability of the lock-in range test. However, a separate mathematical analysis or simulation was not performed to support the frequency test variation.

A second BIST scheme for the jitter measurement of the clock signal in DSP-based mixed-signal ICs has been presented. The BIST is designed to measure the peak-to-peak jitter on the sampling clock used in DSP-based ICs. It has been shown that the BIST scheme is suitable for the specific class of ICs considered. Further, the presented scheme is suitable for the cases where jitter is the prominent source of the overall noise. Simulation and experimental results have been provided in support of the presented scheme.

The feasibility of both the BIST schemes presented in this thesis rely on the availability of a number of components as parts of normal functionality of the ICs being tested. This makes the BIST schemes essentially application-specific. Nevertheless, it has been demonstrated that the BIST for jitter testing is feasible for the applications that have been traditionally considered unsuitable for BIST techniques.

5.2 Future Work

It is by no means claimed that the jitter test problem has been completely solved in this thesis. Since this work is a first step towards the BIST techniques for jitter tests, there is certainly room for improvement and further development of the presented ideas. The variations of the BIST for CRUs should be explored further as they have the potential to reduce the test overhead without compromising the quality. In particular, a generic test algorithm for reduced-set jitter-tolerance test for generic PLLs should be explored as

the methodology presented in this thesis is applicable only to critically and overdamped PLLs. More work is needed to extend the methodology to the under-damped PLLs. Use of various waveforms other than sinusoidal waveforms should also be studied in a more detailed manner. In addition to this, since optical-to-electrical and electrical-to-optical conversions are always involved in typical SONET/SDH networks, the jitter allocation to the conversions must be taken into account to determine the test parameters. This will depend on the jitter characteristics of the individual convertors used and is specific to the application.

The BIST scheme for the jitter measurement of DSP-based ICs is suitable for applications where jitter is the dominating source of noise as compared to other noise sources. The improvement of the presented methodology should be sought to take other noise sources into account. Also, the analysis leading to the concept underlying the BIST scheme is inductive. A more formal proof of concept is desirable.

The BIST scheme for the CRU exploits a PLL's capability of performing angle modulation. This capability has been used to generate a jittered clock. Noting that a PLL can be used to demodulate an angle-modulated signal, possibilities of using a PLL for jitter measurement in BIST schemes should be sought. It is generally required to measure the jitter on the clock signal generated by a CSU on data transceiver ICs. If the CRU PLL is used to measure jitter by demodulation, the resulting scheme would result in a low overhead BIST scheme.

References

[Adc94] HP E1430A VXI ADC Operator's Guide, Hewlett Packard Company, 1994.

[Ana94] Analog Artist Mixed-Signal Reference, Cadence Design Systems, Inc. March 1994.

[Bar87] P. H. Bardell, W. McAnney and J. Savir, *Built-In Test for VLSI : Pseudorandom Techniques.* John Wiley and Sons, New York, 1987.

[Bes84] R. E. Best, *Phase-locked Loops.* McGraw-Hill, New York, 1984, Chapter 3.

[Bla95] A. Black and J. Bostak, "Jitter and Wander in Emerging Gigabit Networks," *Digital Communication Design Conference*, 1995.

[Cor94] GR-253–CORE, "SONET Transport Systems: Common Criteria, Network Element Architectural Features," Issue 1, 1994.

[D2092] HP 75000 D20, User's Manuals, Hewlett Packard Company, September 1992.

[Ega81] F. W. Egan, *Frequency Synthesis by Phase Lock.* John Wiley and Sons, New York,1981, Chapter 4.

[Enc93] J. B. Encinas, *Phase Locked Loops.* Chapman and Hall, London, 1993, Chapter 2.

[Fer94] S. P. Ferguson, "Implications of SONET and SDH," in *Electronics and Communication Engineering Journal,* pp. 133–142, 1994.

[Gar79] F. M. Gardner, *Phase Lock Techniques.* John Wiley and Sons, 1979, Chapters 1 and 2.

[Hot92] R. Hotler, "SONET- New Technology With New Management Requirements," in *SUPERCOMM/ICC '92,* pp. 1810–1814, 1992.

[Hyk92] S. Haykin, *Communications Systems.* Wiley, New York, 1992, Chapter 4.

[Jen90] Y. Jenq, "Digital Spectra of Non-uniformly Sampled Signals : Theories and Applications. Part IV – Measuring Clock/Aperture Jitter of an A/D system," in *Instrumentation and Measurement Technology Conference,* pp. 145–147, 1990.

[Jen188] Y. Jenq, "Digital Spectra of Non-uniformly Sampled Signals : Theories and Applications. Part I – Fundamentals and High Speed Waveform Digitizers," in *Instrumentation and Measurement Technology Conference,* pp. 391–398, 1988.

[Jen288] Y. Jenq, "Digital Spectra of Non-uniformly Sampled Signals : Theories and Applications. Part II – Digital Look-up Tunable Sinusoidal Oscillators," in *IEEE Transactions on Instrumentation and Measurement,* vol. 37, pp. 358–362, 1988.

[Kim93] S. Kimura, M. Kimura, T. Nakatani and M. Sugai, "A New Approach for PLL Characterization on Mixed Signal Tester," in *Proceedings of International Test Conference,* pp. 697–704, 1993.

[LaM89] J. LaMay and D. C. Caldwell, "A Telecommunication Line Interface Test System Architecture," in *Instrumentation and Measurement Technology Conference,* pp. 216–221, 1989.

[Lu 94] A. K. Lu, G. W. Roberts and D. A. Jones, "A High-Quality Analog Signal Oscillator Using Oversampling D/A Conversions Techniques ," in *IEEE Transactions on Circuits and Systems II : Analog and Digital Signal Processing,* vol. 41, pp. 437–444, 1994.

[Mat94] MATLAB, User's Manual, The MathWorks Inc. 1994.

[Meh93] R. Mehtani, B. Atzena, "Mixtest : A Mixed-Signal Extension to a Digital Test System," in *Proceedings of International Test Conference,* pp. 945–953, 1993.

[Mic95] *Microwave Logic SJ-300 SONET/SDH Jitter and Wander Analyzer, User's Guide, March 1995.*

[Onv94] R. O. Onvural, *Asynchronous Transfer Mode Networks : Performance Issues.* Artech House, 1994.

[Pal95] P. Palacharla, J. Chrostowski and R. Neumann, "Techniques for Accelerated Measurement of Low Bit Error Rates in Computer Data Links," in *Computers and Communications, 1995 International Phoenix Conference*, 1995, pp. 184–189.

[Ram94] S. C. Ramon and J. Mullighan, "Optimization of PLL Performance in Data Recovery Systems," in *IEEE Journal of Solid-State Circuits,* vol. 29, pp. 1022–1034, Sept. 1994.

[Shi90] A. Y. Shinagawa, M. and T. Wakimota, "Jitter Analysis of High–speed Sampling Systems," in *IEEE Journal of Solid-State Circuits,* vol. 25, pp. 220–224, 1990.

[Sou90] T. M. Souders, D. R. Falch, C. Hagwood and G. L. Yang, "The Effect of Timing Jitter in Sampling Systems," in *IEEE Transactions on Instrumentation and Measurement,* vol. 39, pp. 80–85, 1990.

[Sor95] SUNI-Lite Optical Reference Design Board : PMC-Sierra, Inc., 1995.

[Spt94] SpectreHDL Reference Manual, Cadence Design Systems, Inc. Sept. 1994.

[Spr94] Spectre Reference Manual, Cadence Design Systems, Inc. March 1994.

[Sun95] SUNI-155–LITE, PM 5346; SATURN User Network Interface: PMC-Sierra, Inc., 1995.

[Syn94] "Synchronous Optical Network (SONET) – Jitter at Network Interfaces," Tech. Rep. ANSI T1.105.03–1994, American National Standard for Telecommunications.

[Ter93] E. Teraoka, T. Kengaku, I. Yasui, K. Ishikawa, T. Matsuo, H. Wakada, N. Sakashita, Y. Shimazu and T. Tokuda, "A Built-in Self-test for ADC and DAC in a Single Chip Speech Codec," in *Proceedings of International Test Conference,* pp. 791–796, 1993.

[Ton93] M. F. Toner and G. Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC," in *Proceedings of International Test Conference,* pp. 805–814, 1993.

[Tri89] P. R. Trischitta and E. L. Varma, *Jitter in Digital Transmission Systems.* Artech House: Norwood, Mass., 1989, Chapter 1.

[Vee95] HP VEE, Reference Manual, Hewlett Packard Company, Jannuary 1995.

[Ver90] Verilog XL Reference Manual, Volume 1, Version 1.2b, Cadence Design Systems, Inc. Nov. 1990.

[Wag90] F. Wagdy and S. Awad, "Effects of Sampling Jitter on Some Sine Wave Measurements," in *IEEE Transactions on Instrumentation and Measurement,* vol. 39, pp. 86–89, 1990.

[Wag91] F. Wagdy and S. Awad, "More on Jitter Effects on Sinewave Measurements," in *IEEE Transactions on Instrumentation and Measurement,* vol. 40, pp. 549–552, 1991.

[Wes85] N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design, A Systems Perspective*, 2nd ed. Addison-Wesley, Reading Mass., 1985, Chapter 3.

[Wil82] T. W. Williams and K. P. Parker, "Design for Testability – A Survey," in *IEEE Transactions,* vol. 31, pp. 2–15, 1982.

[Wol91] D. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice Hall, Englewood Cliffs, N.J., 1991.

[You94] J. Young, "Jitter Considerations in High Bit Rate Digital Video Signals," in *IEEE Transactions on Broadcasting,* vol. 40, pp. 82–90, 1994.

Appendix A. List of Acronyms

ac	Alternating Current
ADC	Analog-to-digital Convertor
AHDL	Analog Hardware Description Language
ANSI	American National Standards Institute
ASIC	Applications Specific Integrated Circuit
ATE	Automatic Test Equipment
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BERT	Bit Error Rate Tester
B-ISDN	Broadband Integrated Services Digital Network
BIST	Built-in Self-test
CMOS	Complimentry Metal Oxide Semiconductor
CRU	Clock Recovery Unit
CSU	Clock Synthesis Unit
DAC	Digital-to-analog Convertor
DC	Direct Current
dB	decibel
DFT	Discrete Fourier Transform
DSP	Digital Signal Processing
DUT	Device Under Test
FFT	Fast Fourier Transform
FIFO	First In First Out
FM	Frequency Modulation
GHz	Giga Hertz
GPIB	General Purpose Interface Bus

I/O	Input/Output
ISDN	Integrated Services Digital Network
kHz	Kilo Hertz
LFSR	Linear Feedback Shift Register
LPF	Low Pass Filter
Mbps	Mega bits per second
MHz	Mega Hertz
NE	Network Element
nS	nanoSecond
OC-N	Optical Carrier at level N
PD	Phase Detector
PLL	Phase Locked Loop
PM	Phase Modulation
p-p	peak-to-peak
pS	picoSecond
rms	root mean square
SDH	Synchronous Digital Hierarchy
SNR	Signal to Noise Ratio
SONET	Synchronous Optical Network
SORD	Synchronous Optical Reference Design
STS-N	Synchronous Transport Signal at level N
UI	Unit Interval
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration

Appendix B. Schematics

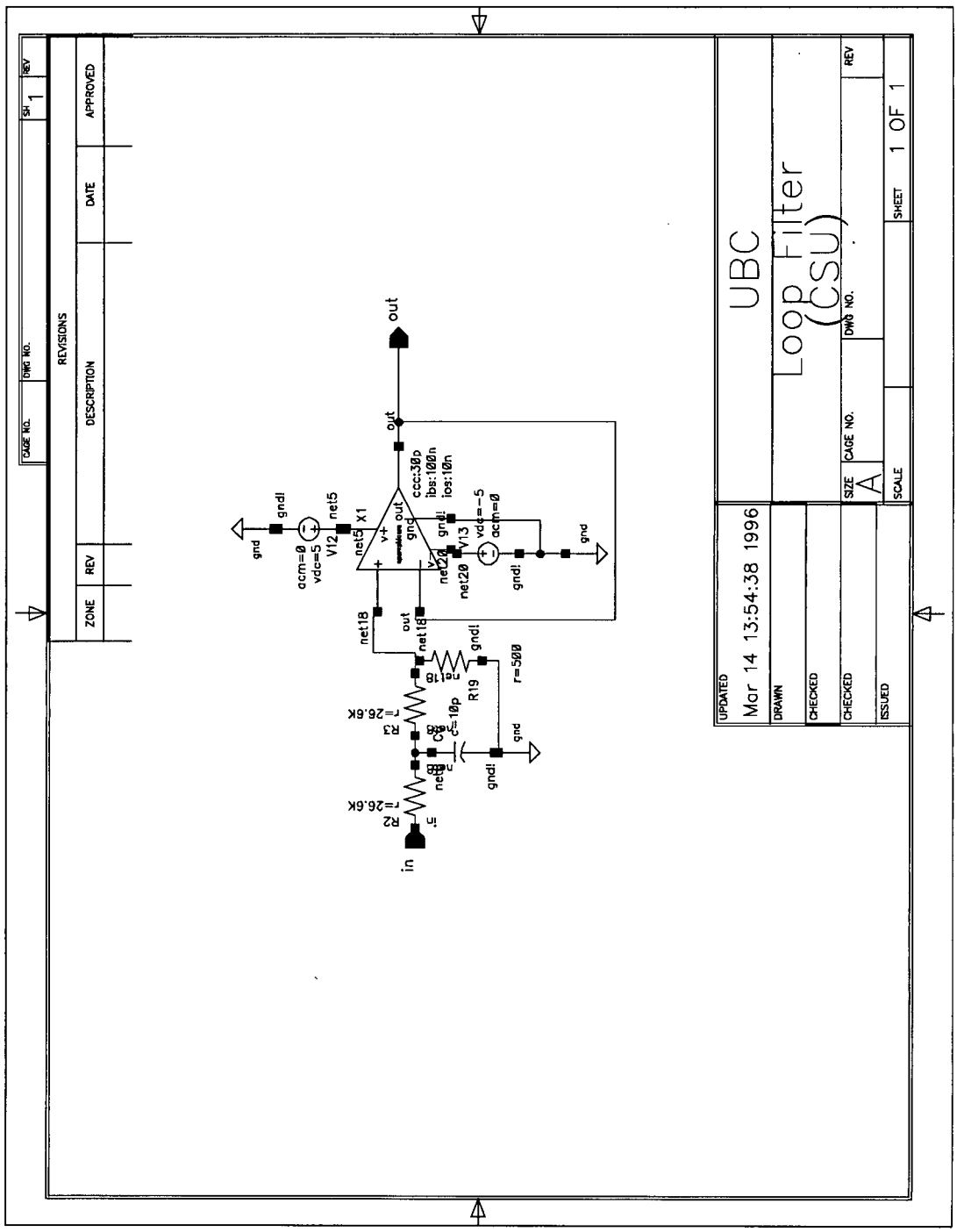

Figure B.1 Low pass filter for CSU.

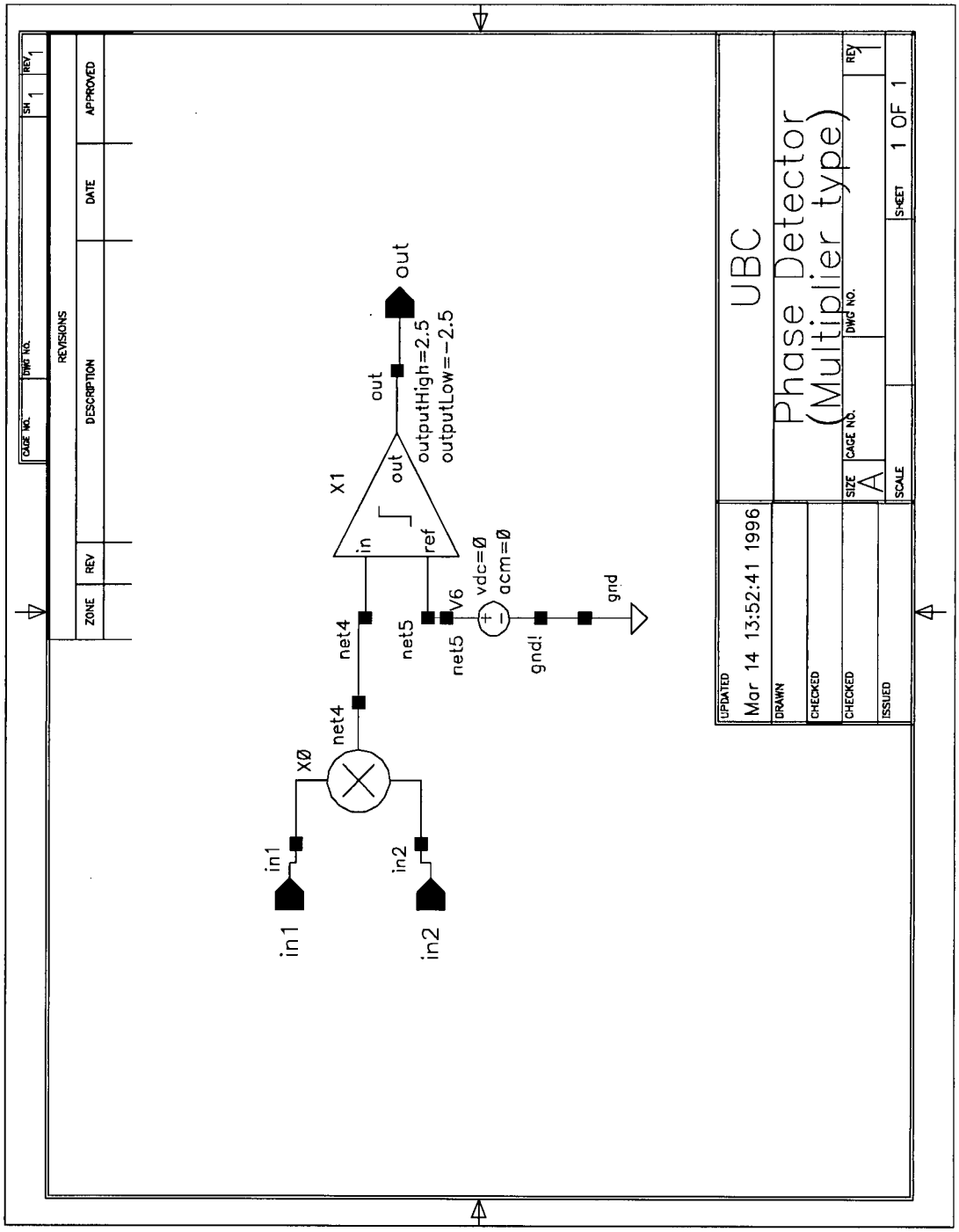

Figure B.2 Phase detector used in CRU and CSU.

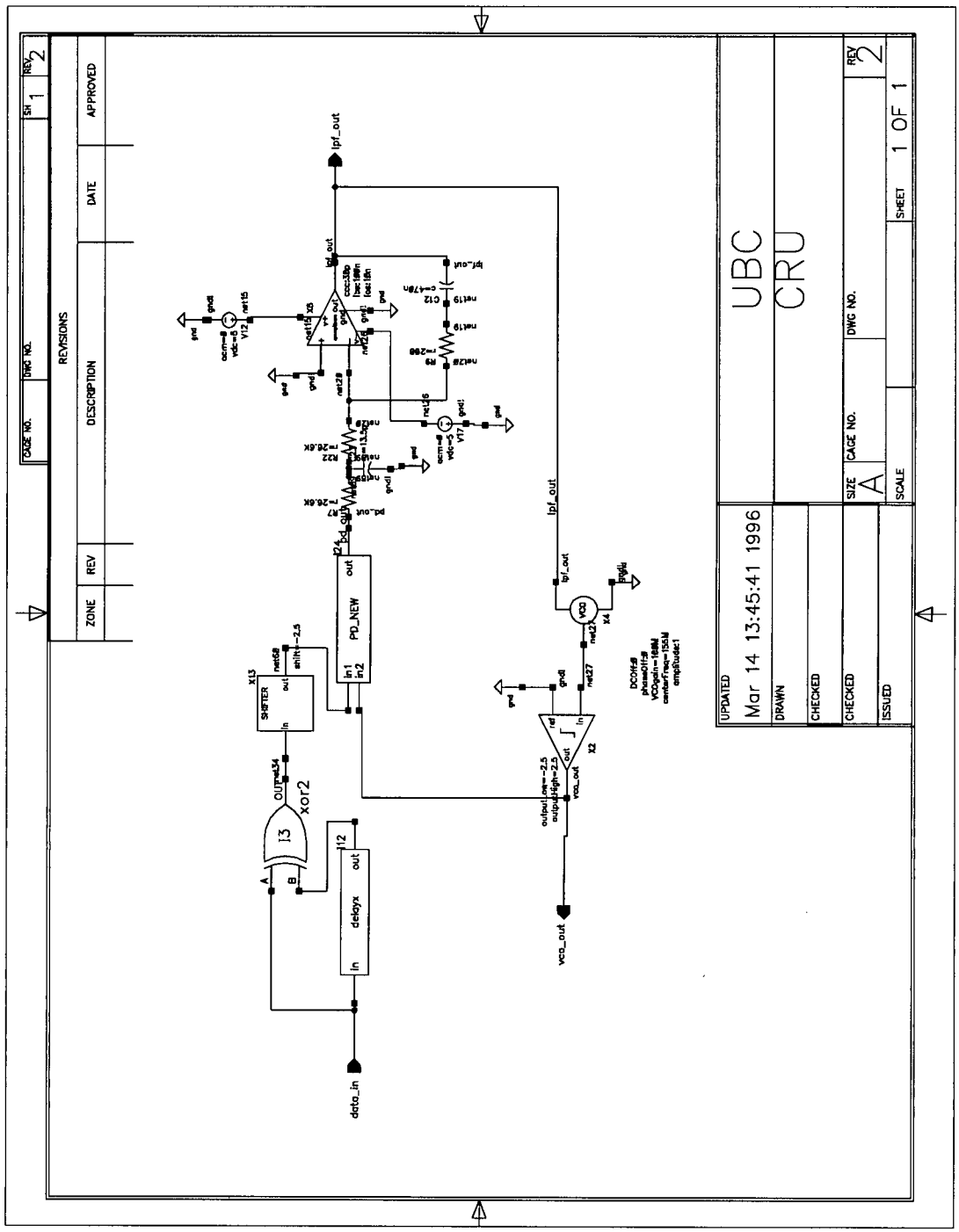

Figure B.3 The Clock and data recovery unit (CRU).

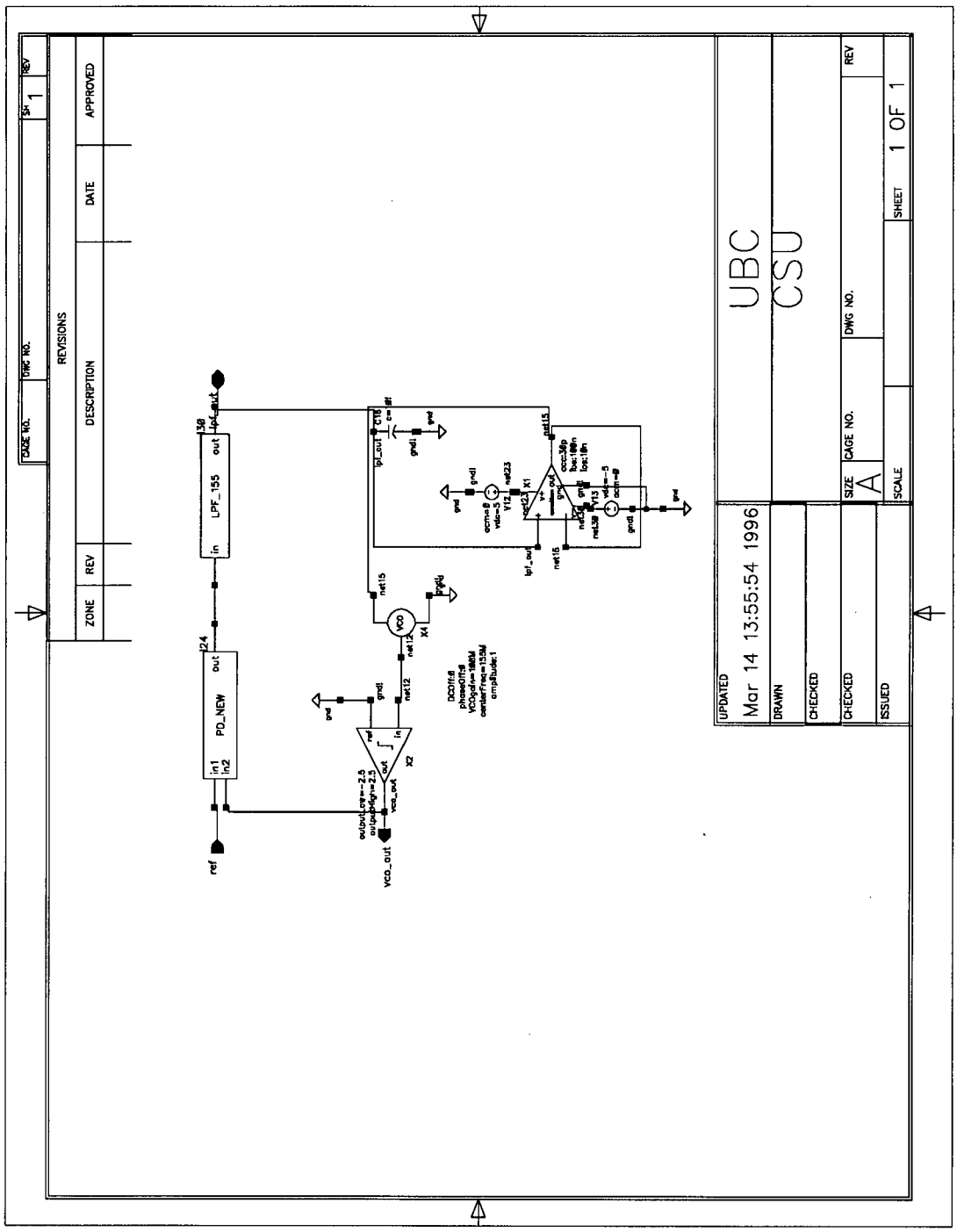

Figure B.4 The Clock synthesis unit (CSU).

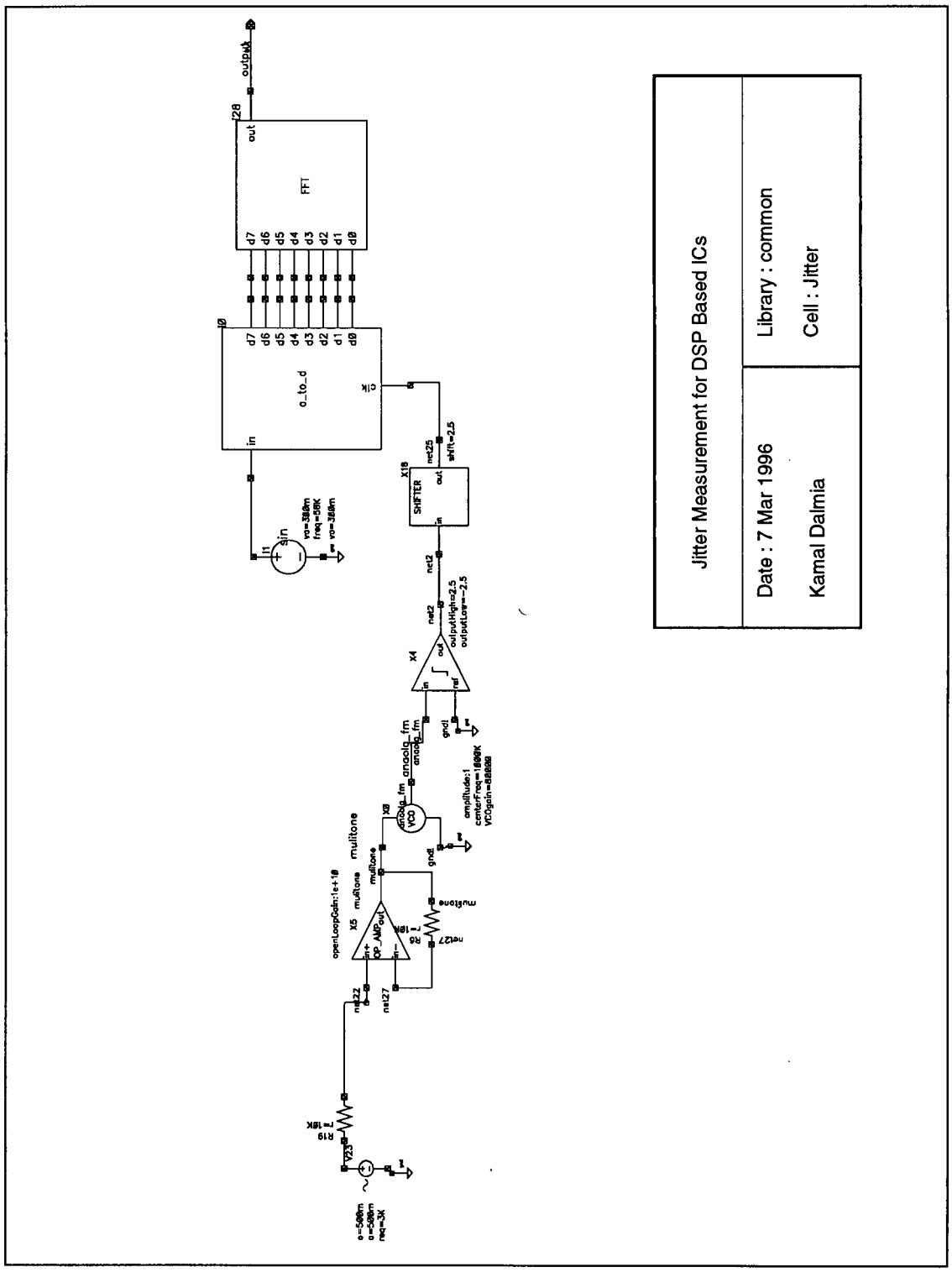

Figure B.5 BIST scheme for DSP-based ICs.

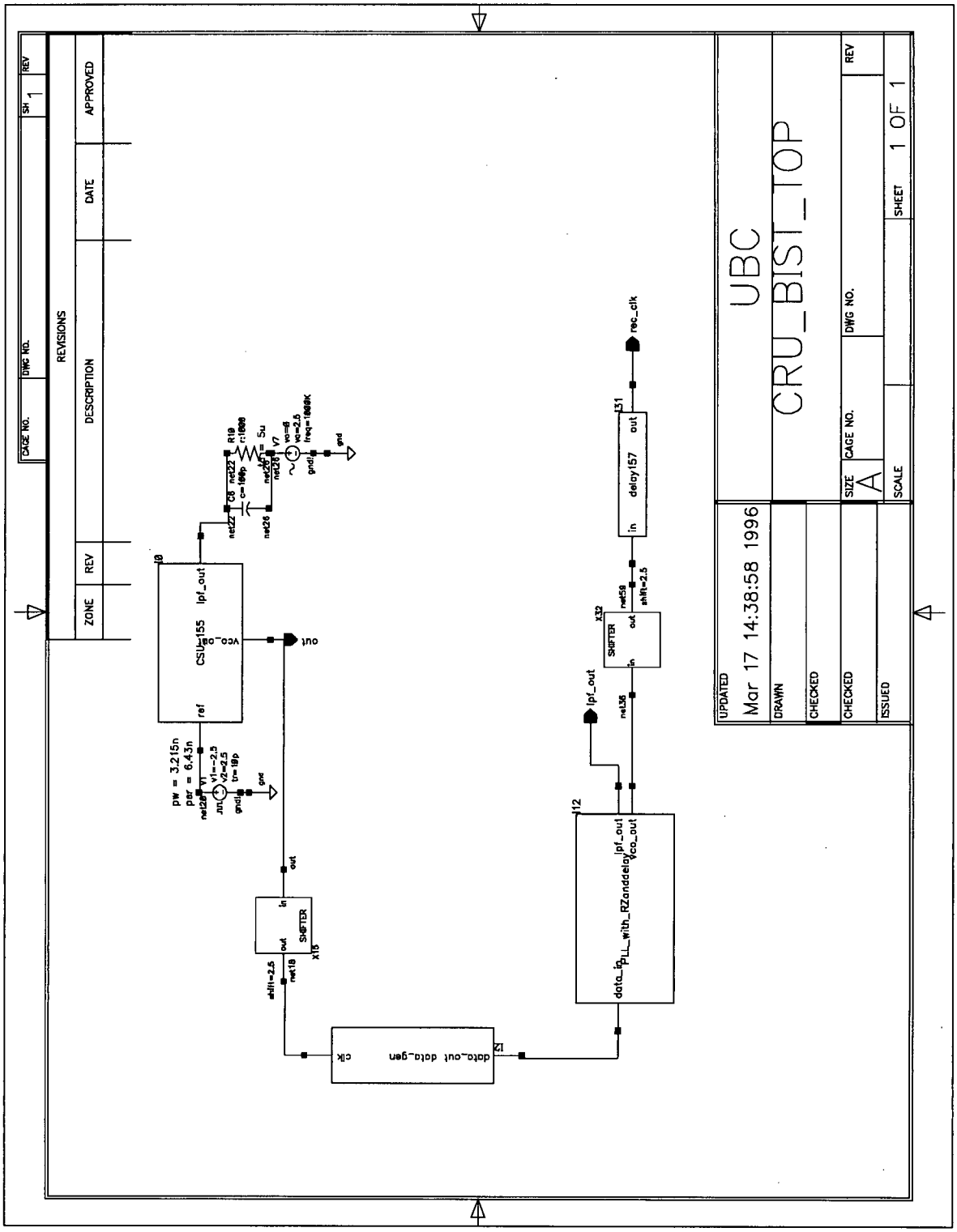

Figure B.6 BIST scheme for jitter tolerance test.

Appendix C. Simulation Results

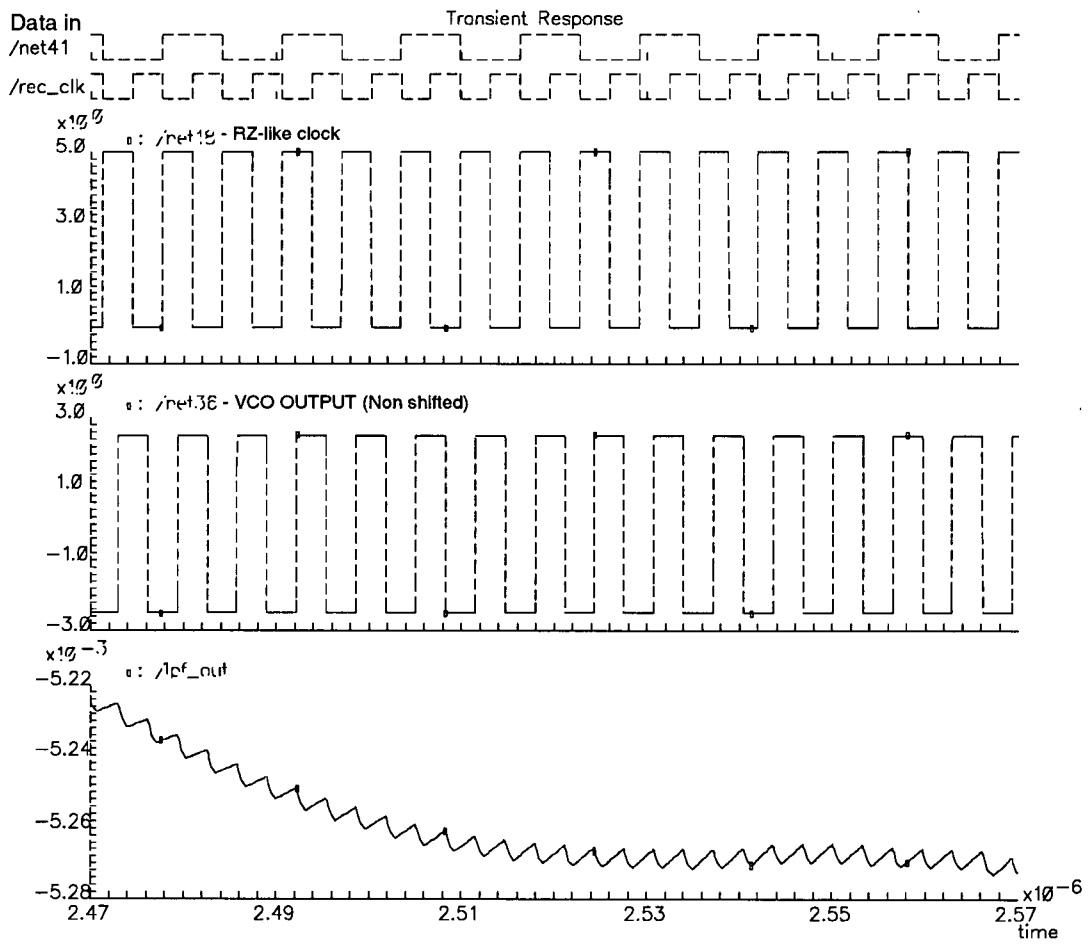

Figure C.1 No bit in error, data transition density = 100 %.

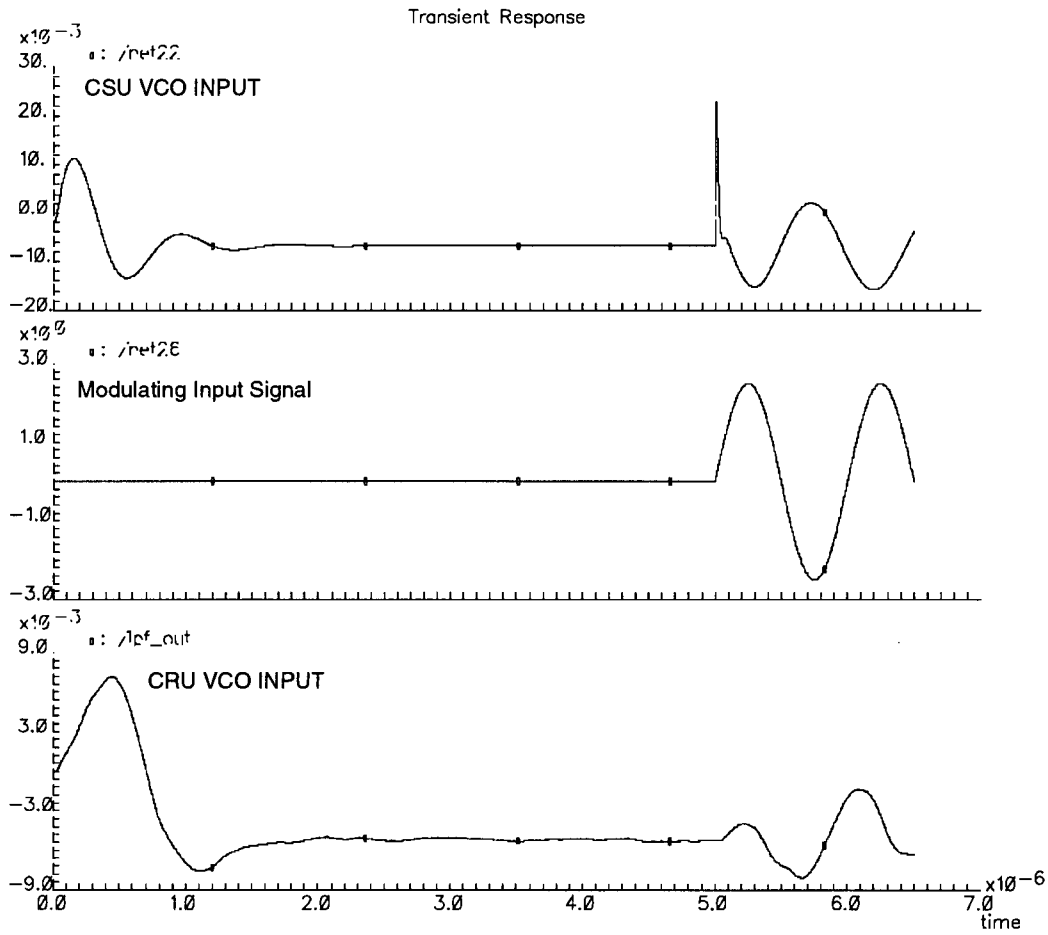

Figure C.2 Various wavefroms with data transition density = 100 %.

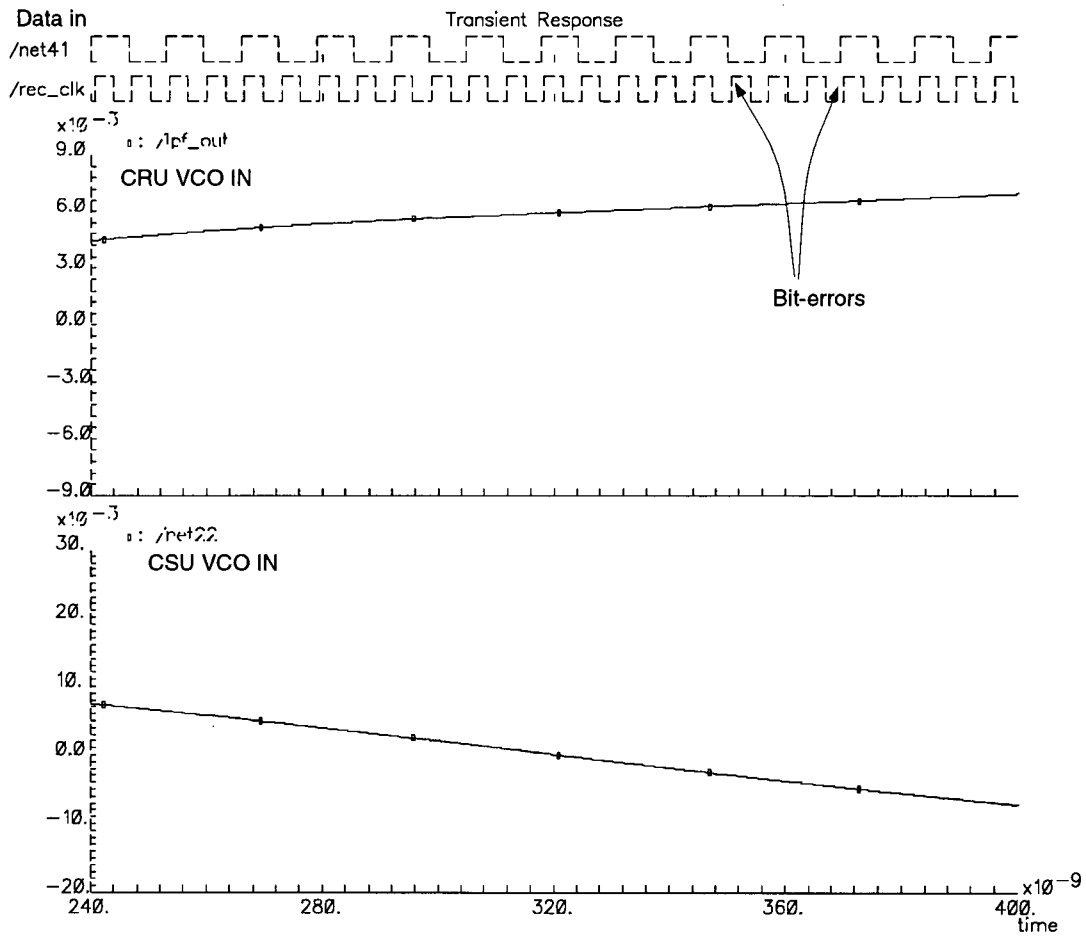

Figure C.3 Bits in error with data transition density = 100 %.

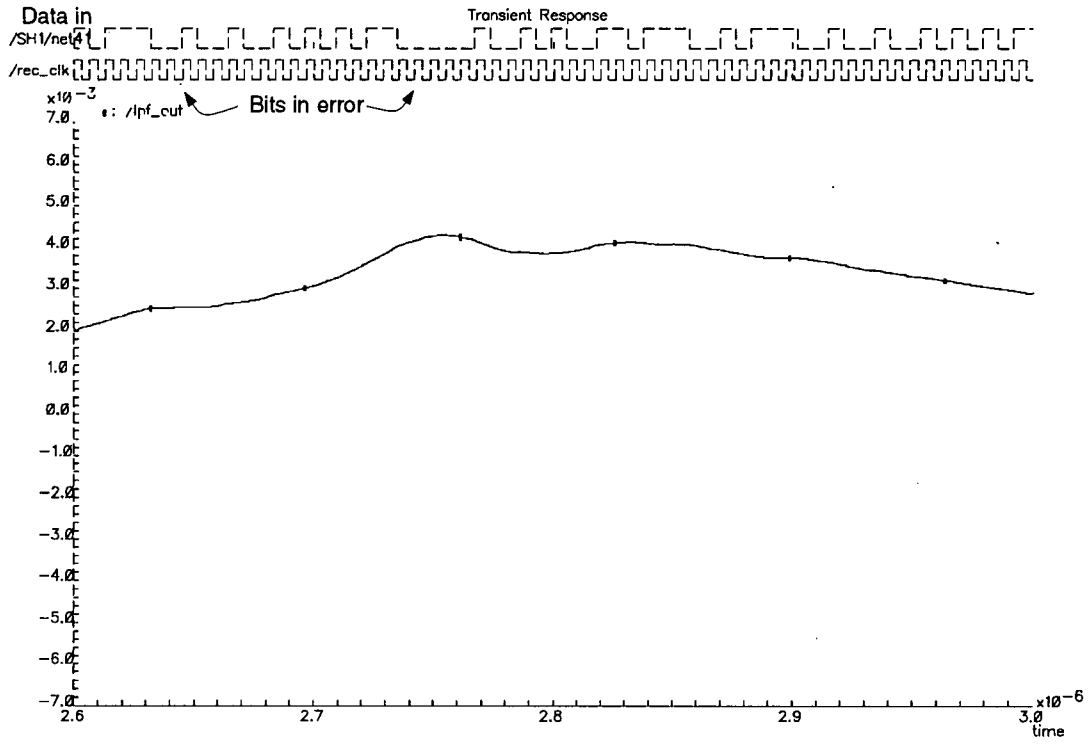

Figure C.4 Bits in error with pseudo-random data

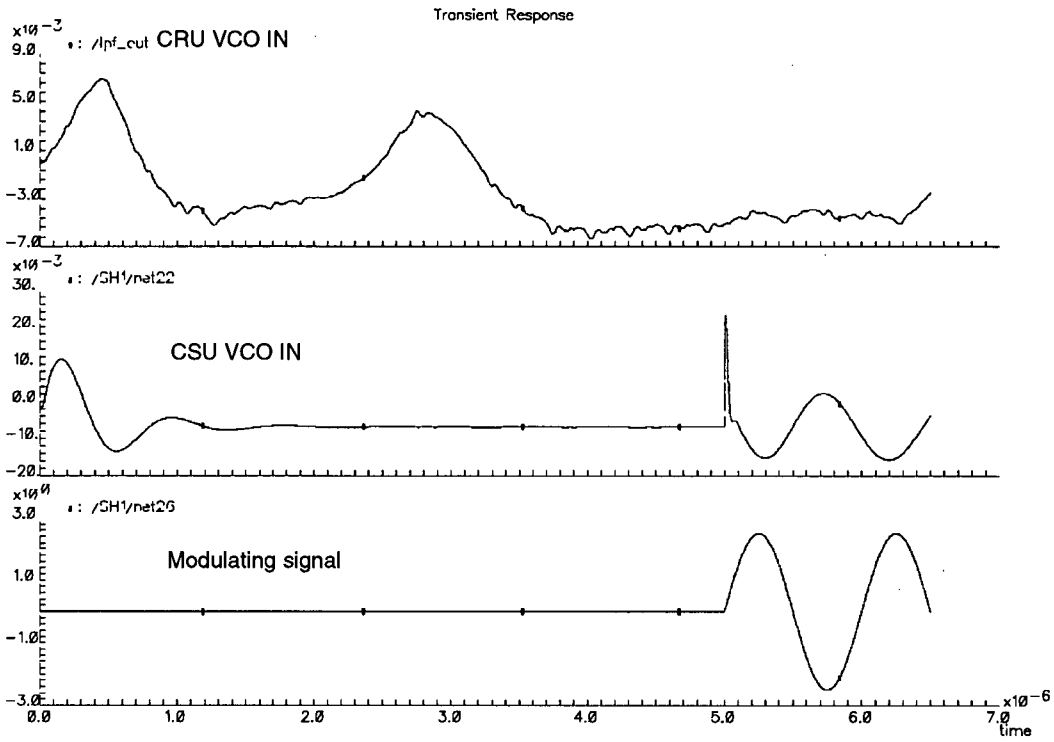

Figure C.5 Various waveforms with pseudo-random data.

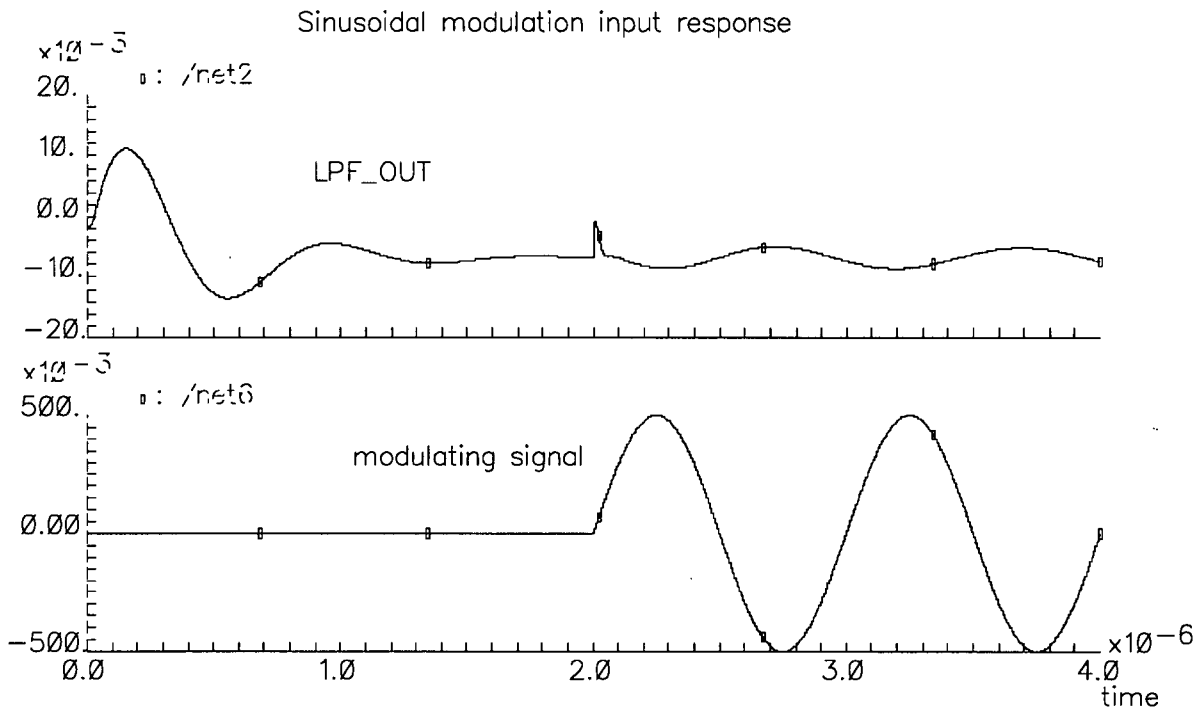

Figure C.6 Jitter generation with sinusoidal input.

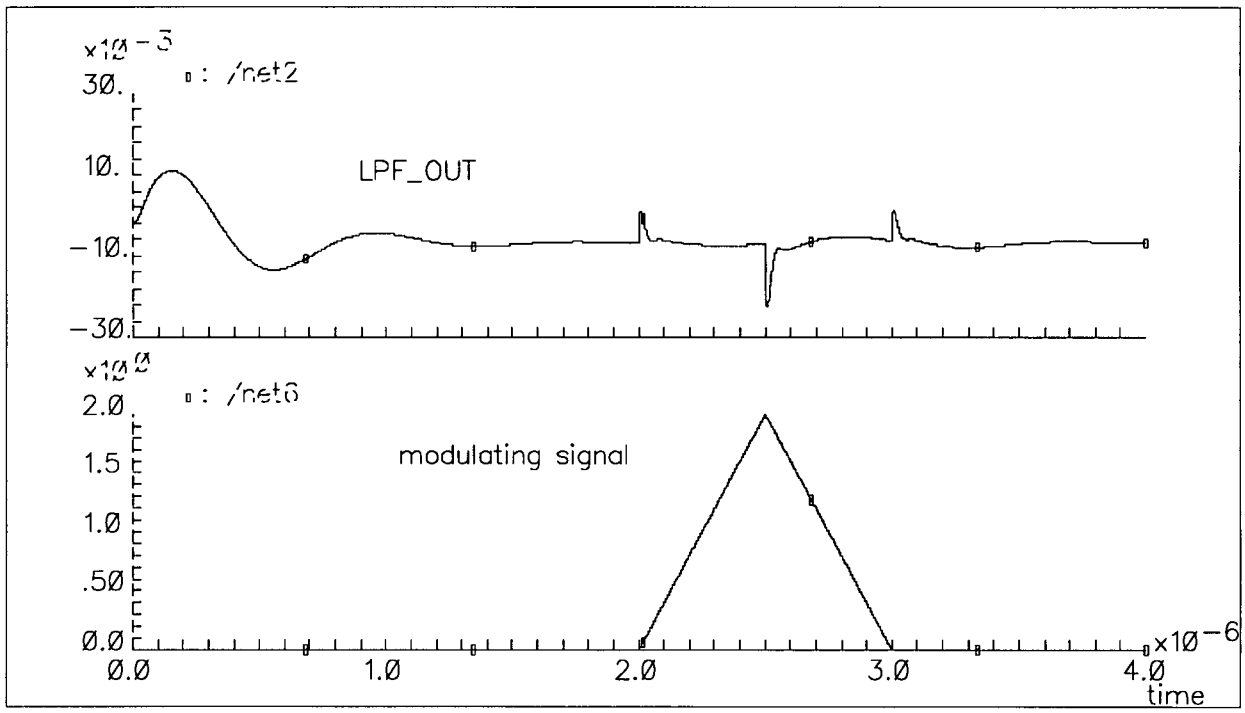

Figure C.7 Jitter generation with triangular input.

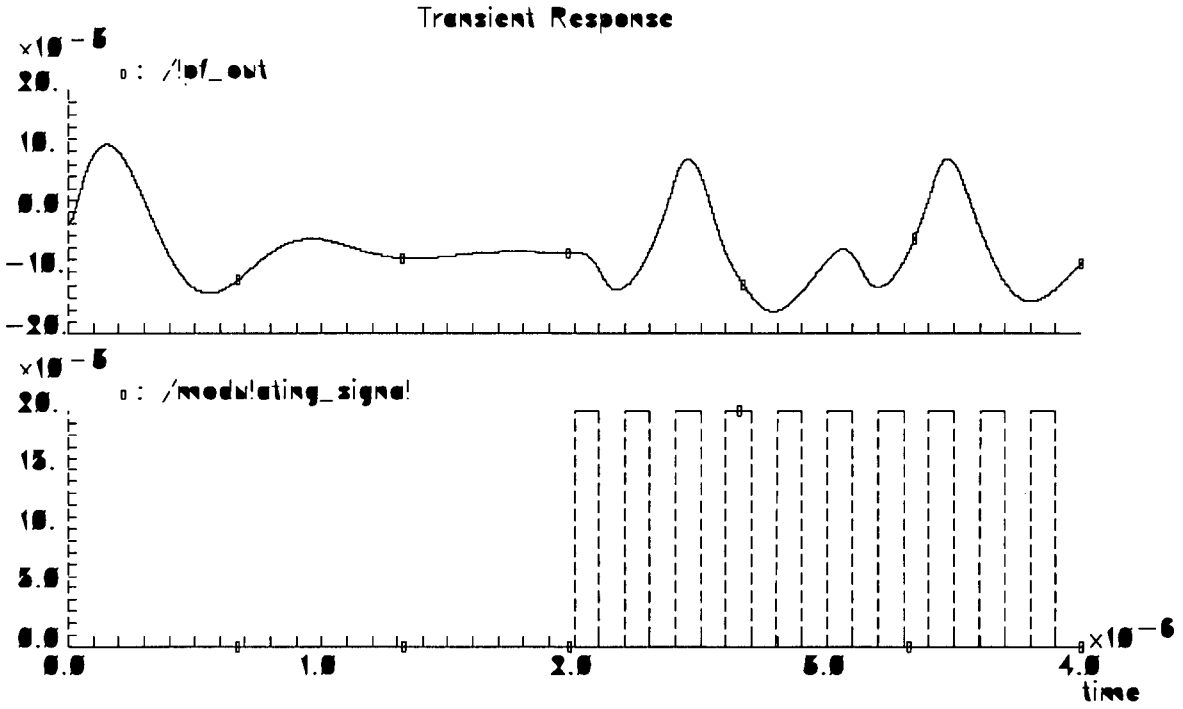

Figure C.8 Jitter generation with square wave input.

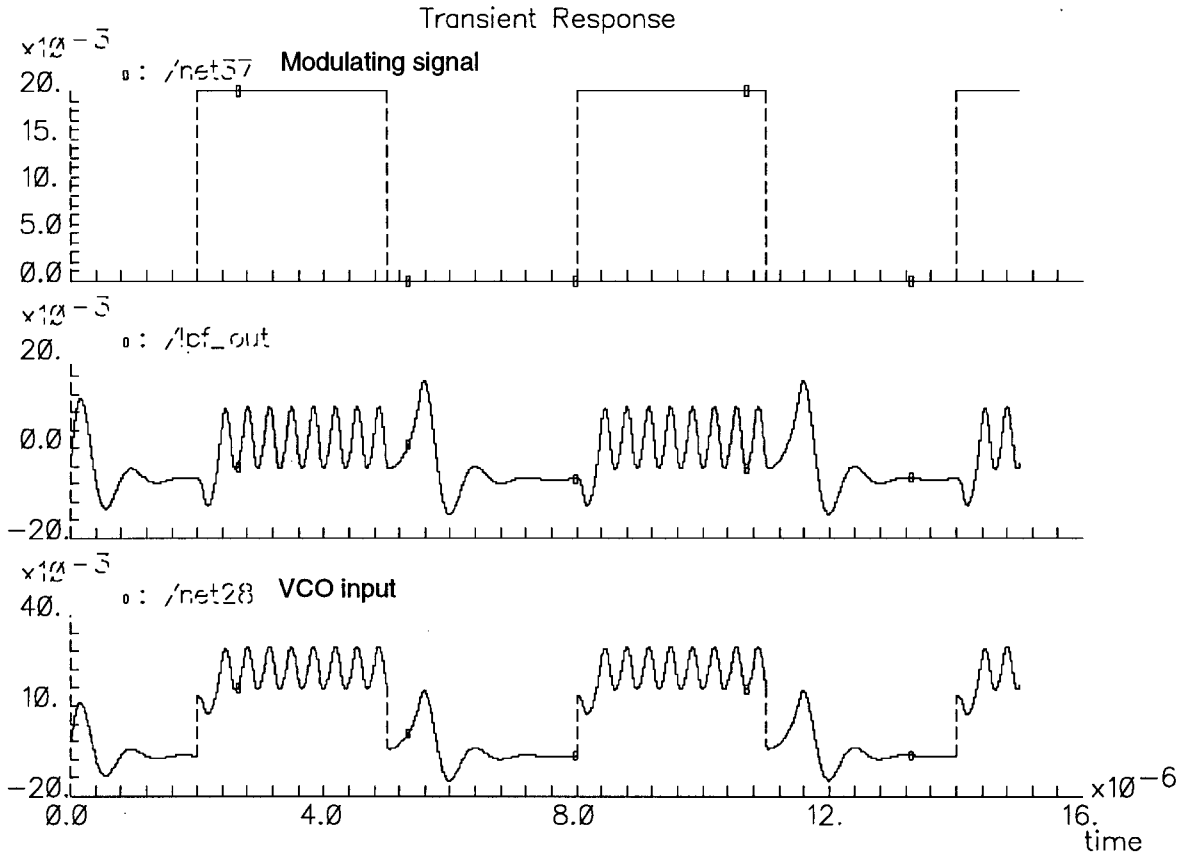

Figure C.9 Jitter generation with square wave input added to VCO control net.

Appendix D. HDL Codes

1. The Verilog code for the data generator.

```
// Verilog HDL for "data_gen" "_functional"

`timescale 1 ps/1ps

module data_gen (clk,data_out) ;

input clk;
output data_out;
reg mem[0:1090];
reg data_out;

initial $readmemb ("prbs23.data", mem);

integer i;

initial
 begin
  i=0;
 end
```

```
always @(posedge clk)
      begin
    data_out=mem[i];
   end

always @(negedge clk)

   begin

    if (i==1090)
     begin
      i=0;
     end
    else
     begin
      i=i+1;
     end
   end
endmodule
```

2. The Verilog code for the delay element.

```
// The Verilog code for the Delay element



// Verilog HDL for "common", "delayx" "_functional"


`timescale 1 ps/1 ps


module delayx (in,out) ;


input in;

output out;

reg out;


always @(in)

 begin

   out = #3215 in;

 end

endmodule
```

3. The AHDL code for the analog-to-digital convertor.

```
module a_to_d (d7, d6, d5, d4, d3,
 d2, d1, d0, in, clk) (risetime, falltime)
node [V, I] d7, d6, d5, d4, d3, d2, d1, d0, in, clk;
parameter real risetime = 0.01n from (0:inf);
parameter real falltime = 0.01n from (0:inf);
{
  real x;
  const real halfref = 0.5;
  real out7, out6, out5, out4, out3, out2, out1, out0;

   analog {
    if ($threshold(V(clk)-2.5, 1.0)){
      out7 = 0;
      out6 = 0;
      out5 = 0;
      out4 = 0;
      out3 = 0;
      out2 = 0;
      out1 = 0;
      out0 = 0;
      x = V(in);
```

```
      if (x > halfref) { out7 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out6 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out5 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out4 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out3 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out2 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out1 = 5.0; x -= halfref; } x *= 2.0;
      if (x > halfref) { out0 = 5.0; }
    }
    V(d7) <- $transition( out7, 0, risetime, falltime );
    V(d6) <- $transition( out6, 0, risetime, falltime );
    V(d5) <- $transition( out5, 0, risetime, falltime );
    V(d4) <- $transition( out4, 0, risetime, falltime );
    V(d3) <- $transition( out3, 0, risetime, falltime );
    V(d2) <- $transition( out2, 0, risetime, falltime );
    V(d1) <- $transition( out1, 0, risetime, falltime );
    V(d0) <- $transition( out0, 0, risetime, falltime );
  }
}
```

Appendix E. MATLAB Code

The MATLAB code for plotting various PLL parameters.

```
clear;

f=1 : 500 : 4*10e6;

R1=2*26.6*1000;

R2=200;

C3=13.5*10e-12;

C=0.47*10e-6;

%%%%%%%%%%%%%%%% LPF, VCO and PD parameters

kd=5/(pi);

ko=100*2*pi*10e6;

kh=R2/R1;

%%%%%%%%%%%%%%%%%%%%%

w=2*pi*f;

w2=1/(R2*C);

w3=4/(R1*C3);

%%%%%%%%%%%%%%%%%%%%%

Fs=kh.*((j*w+w2)./((j*w).*(j*w/w3 +1)));

Gs=ko*kh*Fs./(j*w);

Js=1+Gs;

Hs=Gs./(1+Gs);
```

```
%%%%%%%%%%%%%%%%%%%%%%
magHs=abs(Hs);magGs=abs(Gs);
magJs=abs(Js);
magFs=abs(Fs);
%%%%%%%%%%%%%%%%%%%%%%  plots
log_Hs=10*log10(magHs);
subplot(3,1,1)
semilogx(f,log_Hs);
grid;
title('H(s)');
xlabel('frequency(Hz)-->');
ylabel('magnitude[H(s)] (dB)-->');
print log_hs

figure(2);
log_Gs=10*log10(magGs);
subplot(3,1,1)

semilogx(f,log_Gs);
grid;
title('G(s)');
xlabel('frequency(Hz)-->');
```

```
ylabel('magnitude[G(s)] (dB)-->');
print log_gs

figure(3);

log_Js=10*log10(magJs);subplot(3,1,1)

semilogx(f,log_Js);
grid;
title('J(s)');
xlabel('frequency(Hz)-->');
ylabel('magnitude[J(s)] (dB)-->');
print log_js

figure(4);

log_Fs=10*log10(magFs);
subplot(3,1,1)

semilogx(f,log_Fs);
grid;
title('F(s)');
```

```
xlabel('frequency(Hz)-->');
ylabel('magnitude[F(s)] (dB)-->');
print log_fs
```

Appendix F. SONET Jitter Specifications

F.1 Jitter Transfer :

Jitter transfer is the ratio of jitter on the output of an OC-N/STS-N signal to the jitter applied on the input of an OC-N/STS-N signal versus frequency. Fig. F.1.1 and Table F.1.1 show the jitter transfer curve applicable to OC-N network interfaces. In general, jitter transfer does not apply to transmitters and receivers. It mainly applies to regenerators [Syn94].

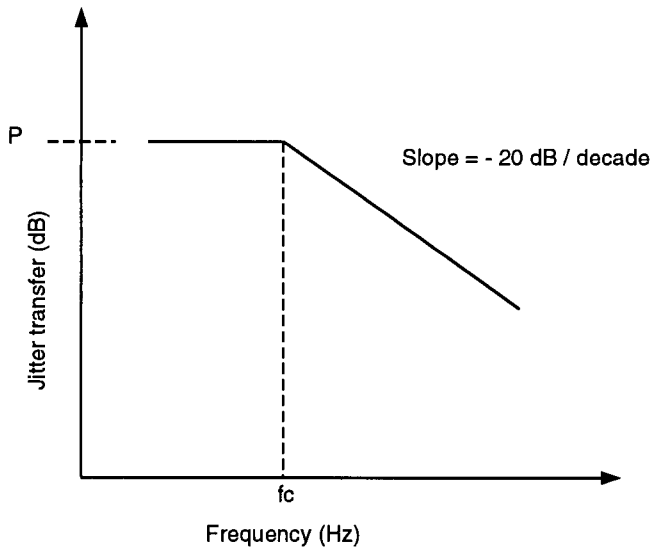

Figure F.1.1 Jitter transfer specification [Syn94].

Table F.1.1 Jitter transfer specification [Syn94].

OC/STS level	fc (kHz)	P (dB)
1	40	0.1
3	130	0.1
12	500	0.1

F.2 Output Jitter :

Jitter generation or "output jitter" specifies the acceptable phase noise level from a SONET transmitter. Current requirements for a SONET network element is that the maximum jitter be less than 0.01 UI rms (root mean square) and 0.1 UI p-p when measured with a high pass filter having a cut-off of 12 kHz and a low pass having a minimum cut-off of 5 MHz [Syn94][Cor94].

Appendix G. Frequency Test

The basic BIST scheme for jitter tolerance test and the variations of the scheme discussed in Chapter 3 use some kind of function generator to supply a signal to the VCO input. If none of the discussed variations is feasible, then, a plain frequency test can be performed without the need of a function generator. This can be done by a simple loop-back operation of the CRU and CSU. The CSU can be used to generate a line rate clock signal. This clock is then used in conjunction with a data generator to feed data to the CRU. The recovered data from CRU is checked for bit-errors. This is a functional test of both the CRU and the CSU. This test does not take jitter into account. The block diagram is shown in Fig. G.1.

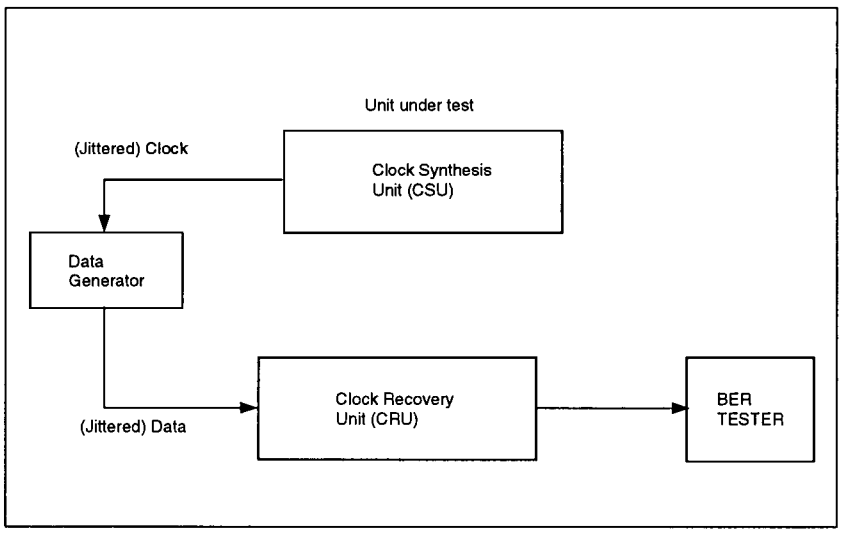

Figure G.1 Frequency test.