LOW HARMONIC CONTENT
THREE-PHASE-TO-DC-CONVERSION
USING AC-SIDE SWITCHES
AND DISCONTINUOUS CONDUCTION MODE

by

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ABSTRACT

The quality of AC power is affected by the large number of nonlinear loads, particularly power converter systems. One way of improving the power factor of AC-DC converters in the 3-100 kW power range is by using Pulse Width Modulation rectifiers with low effects on the mains. The three-phase Power Factor Correction circuits process the whole amount of power transferred, using inductors whose current is controlled at switching frequencies above 20 kHz. Based on the inductor energy being fully or partially transferred to the output within a switching cycle, the operation is called Discontinuous or Continuous Conduction Mode. The definition comes from the shape of the inductor current, whether or not it reaches zero every switching cycle.

The present work brings a contribution to the knowledge about three-phase Power Factor Correction in the Discontinuous Conduction Mode. These circuits are characterized by the small size of the inductors and simple voltage follower control with the downside of higher component stress and large input filters.

The thesis investigates the performance features of circuits with AC-side switches. Two new circuits, the boost-delta and boost-star, with very competitive features emerge. The possibility of using bi-directional and quasi tri-directional switches is explored.

New analytical tools are developed for the study of circuits operating in Discontinuous Conduction Mode. The average current space vector method brings a new insight into the operation of the circuits. Thus, the development of modulation techniques which improve the Total Harmonic Distortion down to zero becomes possible. Moreover, a sinusoidal current waveform in lightly unbalanced voltage systems is achievable.

New circuits using two boost stages, series connected, are proposed. Advantageous features are derived without any compromise. The SEPIC converter with AC-side switches is also analyzed. A comparison is drawn among the investigated circuits. The possibility of staggered operation of several stages, which reduces the amount of ripple on the input is analyzed in this context.
The contribution of the thesis consists in finding theoretically viable options for achieving high power factors with very low harmonic content in Discontinuous Conduction Mode.
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To my father, who has taught me to seek out knowledge,

and to share it for the benefit of all.
CHAPTER 1

INTRODUCTION

In this chapter the historical background and available topologies for three-phase power factor correction are described. A general classification and the advantages and disadvantages of various types of circuits are discussed. The contribution of this thesis is presented in the context of the previous work. The assumptions underlying the calculations are given.
1.1. Harmonics – Historical Context

Power system harmonic distortion is not a new phenomenon - efforts to limit it to acceptable proportions have been a concern of power engineers from the early days of utility systems. At that time, the distortion was typically caused by the magnetic saturation of transformers or by certain industrial loads, such as arc furnaces or arc welders. The major concerns were the effects of harmonics on synchronous and induction machines, telephone interference, and power capacitor failures. In the past, harmonic problems could often be tolerated because equipment was of conservative design and grounded wye-delta transformer connections were used judiciously.

Power system problems that were associated with harmonics began to be of general concern in the 1970s, when two independent developments took place. The first was the oil embargo, which led to price increases in electricity and the move to save energy. Industrial consumers and utilities began to apply power factor improvement capacitors. Capacitors reduce MVA demand from the utility grid systems by supplying the reactive power portion of the load locally. As a result, losses are reduced in the industrial plant and the utility network. The move to power factor improvement resulted in a significant increase in the number of capacitors connected to power systems. As a consequence, there has been an equally significant increase in the number of tuned circuits in plant and utility networks.

The second involved the coming of age of low voltage thyristor technology. In the 1960s, thyristors were developed for dc motor drives and then extended to include adjustable-speed ac motor drives in the 1970s. This resulted in a proliferation of small, independently operated converters usually without mitigation techniques employed.

The increase in the use of static converters both in industrial control equipment and in domestic applications, combined with the increase in use of power factor improvement capacitors, created widespread problems.

The quality of distributed electrical power has become a critical concern in recent years. This concern has grown with the advent of positive industry trends to improve electrical product efficiency as well due to the proliferation of electronic equipment in households and commercial environments. Interestingly enough, the very technology that allows for more efficient use of electrical energy, switch-mode power conversion technology, is also a culprit that can negatively impact power quality. Switch-mode power supplies can
draw high harmonic currents from the AC mains, which can cause a variety of undesirable effects in the ac power distribution system. The end result for electronic products connected to the ac mains can be improper operation, over-stressed ac input components and product failure. There are a number of areas of new and continuing concern related to the effect of harmonics:

- sensitivity of computers, computer-controlled machine tools, and various types of digital controllers;
- damaging dielectric heating in underground cables;
- insulation stress in capacitors, fuse blowing in capacitor banks;
- metering errors;
- rotating machines and transformers heating problems;
- communication systems interference;
- thyristor firing errors, false tripping of protective devices.

The presence of harmonic distortion on the utility system results in incremental costs in the operation of the system. The most important cost component is likely to be the costs associated with applying mitigation measures, such as harmonic filtering, to reduce harmonic levels. Based on the incremental costs alone, substantial investment in mitigating harmonic generation in the end use equipment could be justified. This philosophy of controlling harmonic distortion levels by applying limits at the end use equipment level has been adopted in IEC 1000-3-2.

On the other hand the North American approach is emphasized in the recommendations given in IEEE Std 519-1992, where the harmonic limits are given at the point of common coupling, i.e. the electrical connecting point between utility and customers distribution systems.
1.2 Classification and related issues

Classification

Power Factor Correction (PFC) has been an active research topic in power electronics, motivated by forthcoming stringent power quality regulations. The single-phase PFC is already a common practice, and the industrial application of three-phase PFC techniques has also emerged.

Up to this point the research of three-phase converter techniques has been heavily focused on inverter applications. Although most techniques developed in the inverter area can be used in PFC applications, a PFC circuit has its unique characteristics, and therefore deserves some special treatment. The primary differences between PFC and inverter applications include the following aspects:

- Special attention has to be paid to the quality of input current and electromagnetic interference (EMI) emissions in PFC, which makes control design more difficult;
- Very high switching frequencies are desirable to reduce the size and weight of reactive components (especially inductors), and to improve current control performance. The effect of soft-switching techniques is therefore very prominent in PFC applications;
- The input currents are generally in phase with input voltages, and bi-directional power flow is usually not required in PFC circuits. These aspects provide some flexibility to develop soft-switching and control techniques specific for PFC converters.

There are two basic approaches to controlling power in a power conditioning system, as shown in Fig. 1.1. The first approach is a single stage conversion, which integrates input current control, load voltage regulation, and possibly input/output isolation into one power stage. The second approach is the traditional two-stage scheme, where the input stage (i.e. a PFC converter) controls the input currents and provides a coarsely regulated output voltage, while the load regulation is performed by the second stage.

Active conditioning circuits are the only practical option available to the design engineer. Passive circuits are characterized by poor performance in addition to their notable size and weight. Conversely, so many different active methods have been described that it becomes a task to simply attempt a classification. The
most apparent differentiating attribute is probably the type of the processed power signal, from which
derives the distinction between voltage loaded and current loaded topologies. This nomenclature is
borrowed from inverter circuit theory, and, in the context of rectification, the relevant difference is most
properly characterized by the type of output storage element. A capacitive loaded topology is usually
closely associated with the boost converter as its single phase equivalent. An inductive loaded topology
will be associated with the buck converter.

Fig. 1.1 Basic approaches to obtaining power factor correction.

Capacitive loaded topologies come in many varieties for different applications. They can usually be
understood, schematically, as voltage sourced inverters utilized as loads rather than generators. Note that
under balanced conditions and assuming identical switching behavior for the three rectifying legs, the
output voltage \( V_n \) is guaranteed to be DC and free of low frequency harmonics even with low values of
output capacitance. This is due to the uniform power transfer which characterizes balanced three phase
sources.

The technical conditions for developing of self-commutated PWM rectifiers with low effects on the mains
have been established by the availability of turn-off power semiconductors with low switching power loss
(power MOSFETs, IGBTs and GTOs) and of digital signal processors.

Besides reducing the effects on the mains, this also gives (as compared to conventional line-commutated
rectifier systems) the possibility of a highly dynamic control of the power flow, the generation of an output
voltage being constant independently of the mains voltage and the load and the reduction of the rated power
and the weight of the rectifier unit. The constant output voltage feature also gives the possibility of an
adjustment to a wide input voltage region and a maximum utilization of the rated power of the converter
connected in series on the DC side.
Fig. 1.2. Classification of three-phase rectifier systems for low and medium power
The aim of this chapter is to give a classification of the circuit concepts of three-phase PWM rectifier systems as given in literature and to give an overview over the technical possibilities and the most important trends of the presently very dynamic developments in the area of self commutated rectifier systems. The main attention will be paid to PWM converters (with low and medium power) to be operated from the public low-voltage mains. This means that area which seems to be most likely affected (due to its high application diversity) by future stricter standards concerning effects on the mains of power converter systems.

Fig. 1.2 shows a classification developed in [1] for low and medium power three-phase rectifier systems. For a detailed reference list of the circuits mentioned, [1] represents a source of information rigorously and exhaustively developed. Based on the number of pertinent publications the main focus of the development is now in the area of self commutated and hybrid circuit concepts. (The latter denotes the series and/or parallel connection of a line-commutated and a self-commutated converter). In connection with hybrid systems we also have to point out the future high importance of active filters (besides the concepts discussed here) in the area of energy distribution. Due to the much broader application of pulse rectifier systems with impressed output voltage (voltage DC link pulse rectifier systems) as compared to current DC link pulse converters (e.g. for electrical drive systems) also current DC link pulse rectifiers are omitted from the considerations here. In the following several examples of three-phase PFC will be given, based on presentations such as [1-3].

Three single-phase boost rectifiers

A simple way to implement a three-phase PFC converter is to combine three single-phase boost rectifiers at the input side, one for each phase and each followed by a dc-dc converter, as shown in Fig. 1.3. This configuration is simplified in [4] by directly coupling the outputs of the three PFC converters, so only one dc-dc converter is required. The advantage of the configuration is that well-known single-phase PFC techniques can be used directly, so little development effort is required. In addition, certain redundancy is inherent in this arrangement, since the three converters operate independently. The disadvantages are that more components are added in the main power path, and that the interference among the single-phase PFC converters cannot be avoided completely [4]. Due to its relatively low efficiency, this topology is
not recommended for high power applications.

For high power applications, especially when high performance is required, the continuous current mode (CCM) boost rectifier, shown in Fig. 1.4, is usually used, due to its high efficiency, good current quality and low EMI emissions. The high conversion efficiency results from the use of unidirectional blocking switches such as a single MOSFET or IGBT and its intrinsic antiparallel body diode. It must be noted that, in most cases (i.e. small duty ratio operation), it is the diode that carries most of the current so that the total conduction losses truly approach those of the equivalent natural commutation diode bridge.

The converter is controlled by an output voltage loop and inner current loops which shape the input currents according to their sinusoidal references. Due to the existence of multi-loop control, excellent

Fig. 1.3 Three single-phase boost rectifiers circuit.
current characteristics can be achieved if output voltage is higher than the input line voltage amplitude. EMI emissions and switch conduction loss are also kept low due to the continuous input current. Due to severe diode reverse recovery problem, the major part of the switching loss in a CCM boost converter is the turn-on loss. Several zero-voltage switching techniques have been proposed to reduce or eliminate the switch turn-on loss while alleviating the turn-off loss indirectly by the use of snubber capacitors. Great simplicity can be achieved if the soft switching mechanism is applied to the dc link instead of applying it on the ac side, as in the resonant dc-link (RDCL) [5,6] and other dc link commutated converters [7-10]. Although device switching losses are significantly reduced, the conduction loss in the auxiliary circuit is quite high. RDCL converters also suffer from high voltage stress, high circulating energy and complex but not very effective discrete pulse modulation.

The control section design presents additional difficulties since it must provide for the evaluation of the proper duty cycle, and the suitable power angle simultaneously in order to regulate the output. This increases the controller’s complexity and difficulty of analysis. Furthermore, the small signal behavior is characterized by a RHP zero, if used in continuous mode, complicating further the realization of a stable system within large operating ranges. All of the above reasons would certainly restrain most power engineers from adopting such a topology if it were not for the notable benefits it provides.

![Fig. 1.4 Boost rectifier circuit in CCM.](image-url)
Single switch boost converter

An example of voltage loaded rectifier which is unusually simple yet effective in reducing input current harmonics is the single switch topology [11], shown in Fig. 1.5. Control is simply managed by changing the duty cycle for the switch. Under steady state conditions the duty cycle is constant and only dependent on output power; the output voltage is regulated and ripple-free under balanced line conditions. The main limitation of such a scheme is that it provides sinusoidal fundamentals at the rectifier's input only when run in discontinuous mode; failure to do so results in unacceptably distorted input currents. Although the input current peak is proportional to the sinusoidal input voltage, the average input current is distorted by the inductor current during the discharging state, whose duration is determined by the difference between output and input voltages. To reduce the distortion, the output voltage has to be sufficiently high to limit the duration of the discharging state. Since high output voltage causes higher conduction loss and switch stress in the PFC as well as downstream DC-DC converters, and requires higher boost inductance, the maximum applicable power is practically limited by the trade-off between output voltage and converter performance. The input current THD can be reduced by variable duty cycle or variable switching frequency [12] and by harmonic injection [13]. Because of the DCM operation, the switch is always turned on with zero current, and therefore has very low turn-on loss. However, it is turned off with high current, and thus has high turn-off loss. Rectifier systems of this group have intrinsic resistive fundamental mains behavior. The single switch boost converter does not generate a Right Half Plane (RHP) zero and eases stresses on the boost diode.

Fig. 1.5 Single switch boost circuit with DC-side switch.
SEPIC and Cuk circuits

By changing the output stage of the boost topology, several other topologies have been proposed in [14-15], one example being shown in Fig. 1.6. In the SEPIC and Cuk topologies, the voltage gain can be reduced to facilitate the dc-dc converter in the second stage. However, the switch as well as the intermediate bulk capacitor in the PFC stage are exposed to high voltage stress, and the conduction loss is increased due to the increased circulating current. All these converters suffer from decreased efficiency.

Fig. 1.6 PFC circuit with DC-side SEPIC network.

Buck converter

Three phase inductive loaded rectifiers, such as the one shown in Fig. 1.7, can usually be associated to the single phase buck converter. The general idea is to gate the power bridge switches properly so as to reflect a pulse width modulated version of the DC inductor current on the AC lines. Assuming the same PWM pattern on all three rectifier legs, voltage $V_D$ contains no low frequency line harmonics due to the constant delivery of power. As a consequence, the steady state inductor current is also DC and ripple-free. Because of this feature, the harmonic content of the generated input current is identical in relative magnitude and phase to that of the chosen gating pattern. Note that, once the gating pattern is synchronized with the line, the system only needs one loop to operate for output regulation; this loop simply controls the modulation index $M$ (the average duty cycle) as a means to control the power transferred to the DC output. The most prominent features of this type of rectifiers are:

- the output voltage is lower than in a boost rectifier, so the second stage can use lower voltage devices;
• the input currents can be controlled in open loop and much wider voltage loop bandwidth can be achieved.

• more resilient to switch “misfiring” problems. Momentary “shoot-throughs” result in no damage; they are actually often utilized as part of the gating technique implementation.

• the inrush current at start up can be easily controlled by limiting switch duty cycles;

• less efficient than the voltage loaded type due to the series blocking diodes;

• a freewheeling diode can be used on the dc side to reduce the conduction loss.

Generally, a buck rectifier has similar switching loss, but higher conduction loss than its boost counterpart. Due to the series diodes and consequently its lower efficiency, the buck rectifier is not used as widely as the boost rectifier.

![Inductively loaded buck rectifier circuit](image)

**Fig. 1.7** Inductively loaded buck rectifier circuit

**Active filters**

The active filter concept uses power electronics to produce harmonic components which cancel the harmonic components from the nonlinear loads. These active filters are relatively new and a number of different topologies are being proposed. Within each topology, there are issues of required component ratings and methods of rating the overall filter for the loads to be compensated. The most common active filter configuration is shown in Fig. 1.8 and is based on a PWM voltage source inverter that interfaces to the system through a system interface filter. In this configuration, the filter is connected in parallel with the load being compensated. Therefore, the configuration is often referred to as an active parallel filter.
Phase Sequence, lightning protection and input filter interaction

In a practical situation, some relevant considerations deserve attention. For example, it is important to point out that controlled rectifiers are naturally sensitive to phase sequence. Circuitry must be added to remove such sensitivity in order to avoid cumbersome line measurements at installation.

Another matter of concern is lightning protection which becomes more difficult to implement, as nominal input voltages increase. It is usually inadequate, in fact, to use simple varistor based circuits in high line applications since even large sized varistor which will normally operate at 440VAC will only clamp the 3000A surge prescribed by VDE if its voltage reaches values of 1.5 kV typically. This is usually higher than the rating of available power switches for the rectifier bridge.

The system interaction between the converter and the input filter (including line impedance) is an important and complex issue. However, much more research is needed to obtain a general, theoretically justified, and practical criterion for stability at the three-phase interface. Since a three-phase converter is intended for high power applications, it is characterized by low input impedance. On the other hand, the output impedance of the input filter cannot be reduced arbitrarily since its capacitance is limited by displacement factor requirements [16]. As a result, the filter output impedance and converter input impedance usually overlap over a certain frequency range and system interaction may occur. The interaction at the dc link is also a critical issue for two-stage PFC converters, since the second stage presents to the front-end rectifier a constant power load (negative resistance in small signal sense) due to its tight output voltage regulation. As a general guideline, the converter should be designed with enough input inductance and output capacitance to sufficiently increase the input impedance and lower the output impedance at higher frequencies. The
pulse frequency of the rectifier system has to be set sufficiently above the resonance frequency of the filter in order to obtain sufficient damping of the current harmonics with switching frequency. However, also in this case a resonance condition can result if periodic load changes occur.

Soft-switching

Soft-switching techniques are very important for increasing the power density and reducing the EMI emissions of a PFC circuit. They reduce the switching loss and switch stresses of power devices, and thus makes high switching frequency operation feasible. Most soft-switching techniques originate in dc-dc converters, and have evolved from quasi-resonant converters (QRC), multi-resonant converters (MRC), quasi square-wave PWM converters and soft transition PWM techniques, which include zero-voltage-transition (ZVT) and zero-current-transition (ZCT). The soft transition techniques combine the advantages of soft-switching and PWM control with a low power auxiliary circuit, which is actuated only for a short time prior to switch transition. For most PFC applications, soft transition techniques are more efficient than other soft-switching techniques.

Control

The control of power converters usually can be divided into three functions: modulation, current control, and regulation of an output variable (the output voltage in rectifiers). In the three phase inverter applications, the system dynamics is usually dominated by the slow electromechanical and/or large reactive components, so that the inverter dynamic performance is not very critical. Additionally, accurate ac current control is not very important in many inverter applications (except for field-oriented drives). On the contrary, high quality current control, without the use of large reactive components, is the major objective in PFC applications. With high switching frequencies, which is made possible through the use of soft-switching techniques, high performance and very wide bandwidth control now can be designed.

All standard modulation techniques developed for inverters could be used in rectifier applications. An excellent survey of these techniques can be found in [17]. Sinusoidal PWM (SPWM) is well suited for analog implementation [18] but causes higher switching losses and current ripple [19]. In boost rectifiers, SPWM can be used with third harmonic injection to decrease the minimum output voltage by 15%. The
same effect is automatically achieved with space vector modulation (SVM) [35] which also significantly reduces switching loss and high frequency current ripple. Many of the soft switching techniques often require the use of completely different modulation strategies [20] or modifications of the standard PWM schemes [19,21,22].

The simplest analog current control for boost rectifiers is the hysteresis control [18] which combines the modulation and current control in a single function. It also provides the widest current loop bandwidth of all schemes. The major problems with the hysteresis control are the load dependence of the switching frequency, and the interference among phases resulting in irregular converter operation and uneven current waveforms. These problems can be remedied by controlling two line-to-line currents (differences between phase currents).[23-24]

Average current control is widely used in three-phase rectifiers and can be implemented either with analog or digital hardware. The SVM sequence is often adjusted such that the switches in the phase carrying the highest current are disabled, so the switching loss is reduced to 50%. In digital implementations, two current compensators in rotating coordinates are used [25]. The advantage of the digital implementation is that all control variables are constant in steady state for a balanced system. Conversely, in the analog current control, the control variables are time-varying, and the ideal control voltages may be even discontinuous at the current zero-crossing. Therefore, very fast analog controllers have to be used to achieve good current control, and the current distortion is usually higher than with the digital controllers due to finite controller gains at line frequency [26]. Similarly as in dc-dc converters, the output voltage loop bandwidth for boost rectifiers is severely limited by the presence of the RHP zero in the control-to-output-transfer function [25, 27]. For digital control implementations, the bandwidth is limited even more by the computational and sampling delays.

In the buck rectifiers, due to topological restrictions, three phases cannot operate independently. This prevents the use of hysteresis input current controllers. Instead, SVM or modified SPWM techniques are usually used [28-29]. Excellent input current quality can be easily achieved with open loop control [30].
Future trends

Concerning the effects on the mains with the switching frequency caused by pulse rectifier systems, attempts are being made to obtain a wider distribution of harmonic power and/or a reduction of the amplitudes of single frequency components by varying the pulse frequency (e.g. random pulse width modulation). In this area, a clarification would be advantageous in connection with the standards being prepared for the frequency region 2 ... 9 kHz regarding the admissible harmonic stress on the mains; this should make clear that an even distribution of the harmonic power within a frequency band (and, therefore minimum harmonic stress on the mains for discrete frequencies) should be preferred as compared to a concentration of the harmonic power around multiples of the mains frequency.

Assuming a wider application in the future of pulse converter systems with low effects on the mains and/or of power electronic energy converters, in general, we have to point out the deterioration of the damping conditions to be expected due to the constant power characteristic of these systems. Therefore, under further consideration of the efficiency reduction (2...3% as compared to simple diode rectification) resulting typically for connecting a power factor correction stage in front of each single power electronic load, one has to pose the question in general how a technically and economically optimal solution of the problem area of effects on the mains can be achieved (e.g. by a combined application of "mains-friendly" pulse rectifier systems and centrally located active or hybrid filters).

1.3 Contribution

The thesis proposes a new family of PFC circuits operating in DCM. The distinctive feature is the presence of switches on the AC side of the rectifying bridge unlike the circuits presented in the literature, where they are on the DC-side.

One important consequence is the fact that the switches have to be bi-directional or as it will further be proposed, quasi tri-directional. While this can be seen as an increase of the semiconductors number, the sharing of the dissipated heat can be a reasonable trade-off. New areas of research will evolve by the use of bi-directional switches, both in semiconductor fabrication as well as in soft-switching circuitry.
Fig. 1.9. Classification of the proposed three-phase power factor correction circuits.
The single-switch boost circuit operating in DCM has the disadvantage of poor performance at low voltage transfer ratios. The circuits proposed reduce the THD significantly while maintaining a simple voltage follower control. As a continuation of the general classification given in Fig. 1.2, Fig. 1.9 shows the circuits operating in DCM and includes in the dotted area the contribution of the present thesis. A short description of the circuits will be given here while the schematics and analysis of features will be dealt with in further chapters.

The introduction of three bi-directional switches on the ac-side will give a new degree of freedom to the single-switch boost circuit. The circuit still has a single voltage follower loop, however a phase dependent modulation will reduce in this case the harmonics down to zero. The degree of reduction is dependent on the level of approximation of theoretically determined curves.

By connecting the switches in delta rather than in star as in the previously described circuit, a new set of features is obtained. The boost delta will be phase sequence sensitive and its harmonic content will be comparable to the single switch circuit. However two parallel circuits with the switches connected reverse sequence and staggered operation will achieve both a dramatic reduction of the harmonics as well as an improved ripple on the input. While the staggered operation of the DC-side switch PFC will improve the ripple to an equal extent, the harmonics will stay the same due to phase sequence insensitivity.

Both circuits described so far, will be dealt with in Chapter 3 and are characterized by a single set of boosting inductors. In contrast, Chapter 4 is dedicated to the analysis of circuits having two sets of boosting inductors and AC-side switches. A variety of properties will characterize the boost star – flyback, boost delta – flyback, boost star – boost delta and boost delta – boost delta circuits. The degree of reduction of the harmonics is a trade-off with the displacement angle, switches stress and number.

In Chapter 5, SEPIC derived circuits are studied. They are a natural consequence of the presence of the switches on the AC-side, and are characterized by shifting the L-C-L networks on the AC-side as well. The well known trade-offs of high switch stress and the need for capacitors vs. low harmonics, simple voltage follower control and very good transient performance are present here as in all other SEPIC circuits. However a better power sharing and the quasi tri-directional switch become available options.
1.4 Assumptions

The following assumptions have been used in the determination of the properties of the proposed circuits:

- the utility source is ideal with a zero internal impedance;
- the requirement on power flow is unidirectional;
- the components are ideal, unless specified otherwise;
- variations in the utility source voltage are ignored;
- the switching frequency is constant;
- the switching frequency is much higher than the line frequency;
- the ripple in the output voltage is neglected in comparison to its average value.

The diodes and the output dc capacitors are not included in the evaluation of component ratings, since the diodes are relatively inexpensive and the output dc capacitors are needed in all schemes.
CHAPTER 2
NEW ANALYSIS TOOLS

In this chapter an average current space vector technique is proposed which makes possible a complete analysis of the three-phase power factor correction circuit in the discontinuous conduction mode. The theoretical analysis of various switching combinations allows the determination of the modulation needed for very low Total Harmonic Distortion, down to zero. A technique previously applied for determining the harmonics of the line current is further extended for the calculation of the switching frequency component of the boost inductor currents.
2.1. Average Current Space Vector Technique

2.1.1. Introduction

The boost three-phase Power Factor Correction (PFC) circuit operating in Discontinuous Conduction Mode (DCM), shown in Fig. 1.5, is a popular topology. The input current waveforms have been determined for various voltage transfer ratios, M in [31] and are reproduced here in Fig. 2.1 where M, the voltage transfer ratio is defined as follows:

\[ M = \frac{V_D}{\sqrt{3}V_{LN}} \]  

(2-1)

where:

- \( V_D \) = output DC voltage,
- \( V_{LN} \) = phase peak voltage.

The main limitation of the circuit is that a high output voltage or reduced output power are needed in order to meet the requirements of IEC 1000-3-2 in regards to the harmonic content.

A space vector analysis method which uses averaged currents over a switching cycle is proposed. The method will be used in order to analyze the harmonic content of the line current for the PFC circuit with DC-side switch, shown in Fig. 1.5. The new method will demonstrate that no possible modulation can reduce the THD substantially for the particular circuit studied.

![Fig. 2.1 Normalized current waveforms vs. phase angle for the boost-star circuit, at various voltage transfer ratios M.](image-url)
The method will be applied in further chapters to the proposed family of PFC circuits with switches on the AC side. A theoretical determination becomes therefore possible for the modulation of various schemes, in order to obtain very low, down to zero, harmonic content in the input current.

2.1.2. Space vector technique

PFC circuits operating in CCM have been studied using the space vector technique, as in [32]. The method relies on the creation of a variable voltage at the legs of the three-phase controlled rectifier, in such way as to obtain a sinusoidal current in the boost inductors. To this end, the phase angle will determine the combination of on/off switches.

The space vector method as a general application to instantaneous voltages is based on the following formula:

\[ v(t) = \frac{2}{3} \left[ v_A(t) + a_v B(t) + a^2 v_C(t) \right] \]  \hspace{1cm} (2-2)

where:

Fig. 2.2 Space vector technique: decomposition of the vector into its three-phase components.

Fig. 2.3 Space vector technique: decomposition of the vector into its fundamental and harmonics.
\[ 1 = e^{j0} = (\cos(0) + j \sin(0)) = 1 \]  
\[ a = e^{j2\pi/3} = (\cos(2\pi/3) + j \sin(2\pi/3)) = -1/2 + j\sqrt{3}/2 \]  
\[ a^2 = e^{-j2\pi/3} = (\cos(-2\pi/3) + j \sin(-2\pi/3)) = -1/2 - j\sqrt{3}/2 \]

An example of the application of formula (2-2) to phase and line three phase voltage systems is given in the following:

\[ V_{\text{phase}}(t) = V_m e^{j(\omega t - \pi/2)} \]  
(2-4)

where:

\[ V_a = V_m \sin(\omega t), \quad V_b = V_m \sin(\omega t - 2\pi/3), \quad V_c = V_m \sin(\omega t + 2\pi/3) \]

\[ V_{\text{line}}(t) = \sqrt{3} V_m e^{j(\omega t - \pi/3)} \]  
(2-5)

and:

\[ V_{ab} = V_a - V_b = \sqrt{3} V_m \sin(\omega t + \pi/6) \]

\[ V_{bc} = V_b - V_c = \sqrt{3} V_m \sin(\omega t - \pi/2) \]

\[ V_{ca} = V_c - V_a = \sqrt{3} V_m \sin(\omega t + 5\pi/6) \]

The interpretation of formula (2-2) can be seen in Fig. 2.2, where the projections of the space vector onto the three axes gives the instantaneous values of the phase voltages. When the space vector is of constant amplitude, its trajectory describes a circle, and consequently its projections onto the axes A,B,C are three sinusoidal components, phase shifted by 120° electric. In Fig. 2.3 an exemplification of the situation where \( V \) is the space vector for a signal where harmonics are present, shows that the trajectory is distorted from its circular shape. A Fourier decomposition yields harmonics which can be represented by vectors of constant amplitude, a given phase angle and a rotation speed of \( n\omega t \). While the space vector technique has been exemplified for voltages, it can be equally applied to currents.
2.1.3. Space vector technique using average currents

An averaging technique which determines analytically the properties of the circuit in Fig. 1.5 has been proposed in [31]. Here this method is extended to a space vector representation of the averaged current over a switching cycle. An analytical determination carried out in [31] has shown that the waveforms of the three phase instantaneous currents, look like those in Fig. 2.3 during a switching cycle. The expressions describing this waveforms for each phase are given in Appendix A and are functions of \( x \), the time parameter. The time points where change occurs in the functions are determined in [31] and given below:

\[
t_1 = \frac{3V_A}{V_D - 3V_A} T_{ON}
\]

\[
t_2 = \frac{2V_D(V_C - V_A)}{(V_D - 3V_A)(V_D + V_B - V_C)} T_{ON}
\]

\[
T_{SW} = \frac{M}{M-1} T_{ON}
\]

An attempt to apply the space vector method to instantaneous currents, has resulted in [12] in the determination of the trajectory of the instantaneous current space vectors, such as shown in Fig. 2.5b. The trajectory is based on the formulas given in Appendix A. This method will not give a visual representation of the features of the circuit and consequently little insight is brought.

The space vector method using instantaneous currents is based on the formula (2-7). Its application for average currents will be described by (2-8) which was derived for the boost-star PFC circuit in [31].

\[
i(t) = \frac{2}{3} \left( i_A(t) + \alpha i_B(t) + \alpha^2 i_C(t) \right)
\]

(2-7)

\[
i_{sv} = \frac{1}{2T_{sw}} \left[ i(T_{on})I_{on} + i(T_{on} + t_i)I_{on} + i(T_{on} + t_i)I_{on} \right]
\]

(2-8)

The average current for each time point where \( di/dt \) changes occur, as well as the average over the switching cycle have been calculated and the results are shown in (2-9) and (2-10).

\[
i(T_{on}) = \frac{V_m}{L} \frac{T_{on}}{2} e^{j(\omega t - \pi/2)}
\]

(2-9)
\[
\begin{align*}
\dot{i}(T_{ON} + t) &= \frac{V_m}{L} (T_{ON} + t_1) e^{j(\omega r + \pi/2)} + \frac{2V_D}{3L} t e^{j2\pi/3} \\
\dot{i}(T_{ON} + t_1 + t_2) &= 0 \\
\dot{i}(t_1 + t_2) &= \frac{V_m}{L} e^{j(\omega r + \pi/2)} (T_{ON} + t_1) (T_{ON} + t_2) + \frac{2V_D}{3L} t_1 (t_1 + t_2) \\
&= 2T_{SW} \tag{2-10}
\end{align*}
\]

Fig. 2.4 Phase current waveforms for the boost-star PFC circuit with DC-side switch.

Fig. 2.5 a) Average current space vector and its components, b) Trajectory of the instantaneous current space vector and its resultant average current space vector.
As can be seen by analyzing formula (2-10) and its visual representation in Fig. 2.5, except at the extremities of the studied interval \([0, \pi /6]\), the resultant vector is always behind the voltage vector, and has a variable amplitude. That can be also assessed by looking at the plots of the average current as determined in [31] and reproduced in Fig. 2.1 where for the interval \((0, \pi /6)\) the current amplitude is always smaller than that corresponding to a sinusoidal wave.

The non-circular trajectory implies that the resultant vector is composed of a fundamental and harmonic vectors. A space vector which describes a circle with the speed of \(\omega t\) has a constant amplitude and its projection onto the three axes gives the instantaneous amplitude of the three phases.

When a vector has a non-circular trajectory, it is equivalent to a three-phase system with fundamental and harmonics. Consequently this trajectory is the summation of the vectors representing the fundamental and its harmonics which have particular amplitudes and phase shifts. The vector corresponding to the \(n\)-th harmonic rotates \(n\)-times faster, i.e. with a speed \(n\omega t\). The simplest way to determine their amplitude and phase is by using an analytical rather than graphical method, based on the formulas presented in [31].

It is now easy to show how larger voltage transfer ratios reduce the harmonic component by comparing the overall contribution of the two component vectors from (2-10):

\[
\frac{2V_D}{3L} \frac{t_1(t_1 + t_2)}{2T_{sw}} \frac{V_m}{L} \left[ \frac{T_{on} + t_1}{2T_{sw}} \right] = \frac{2V_m(V_C - V_A)}{V_m V_D} = \frac{\sin(2\omega t)}{M}
\]

The formula proves that the relative size of the vector \(e^{j2\pi/3}\) becomes smaller with higher voltage transfer ratio and consequently the resultant vector is more aligned with the voltage vector, i.e. the harmonics will be smaller.

The vector diagram shown in Fig. 2.5 lets us draw an important conclusion, that it is impossible to obtain zero THD regardless of the modulation scheme used due to the fact that the vector \(e^{j2\pi/3}\) will always have some distorting effect.

Let us now analyze the variation of the resultant vector over the \((0, \pi /6)\) interval.

The average current vector can be written as:
\[ i_{AV} = V e^{i(\omega t - \pi/12)} + V e^{i2\pi/13} \frac{\sin(2\omega t)}{M} \]  

(2-12)

where:

\[ V = \frac{V_m (T_{ON} + t_1) T_{ON} + t_1 + t_2)}{2T_{SW}} \]  

(2-13)

For a simpler calculation the system of axes can be rotated as follows:

\[ i_{AV-R} = V + V e^{i(\pi/12 - \omega t)} \frac{\sin(2\omega t)}{M} \]  

(2-14)

In order that no harmonics be present the following should hold true:

\[ \text{Re}(i_{AV-R}) = ct. \]  

(2-15)

\[ \text{Im}(i_{AV-R}) = 0 \]

As mentioned before meeting the conditions in (2-15) is not possible for this circuit, however it is interesting to study the variation of these components in order to see what duty cycle modulation would reduce the harmonic content.

\[ \text{Re}(i_{AV-R}) = V \left(1 + \frac{\sin(2\omega t)}{M} \cos(7\pi/6 - \omega t) \right) \]  

(2-16)

\[ \text{Im}(i_{AV-R}) = V \frac{\sin(2\omega t)}{M} \sin(7\pi/6 - \omega t) \]

The plots are given in Figs. 2.6 and 2.7 for \( M = 1.5 \) and a normalizing factor \( V_m T_{ON} / 2L \). It can be seen that a significant variation of the amplitude of the two components occurs.

Since \( \text{Re}(i_{AV-R}) \) must be brought closer to a constant value and \( \text{Im}(i_{AV-R}) \) closer to zero, several papers [33-35] have proposed a modulation \( T_{ON} (1 + m \sin(6\omega t + 3\pi/2)) \) in order to achieve just that.
Fig. 2.6 Amplitude of $\text{Re}(i_{AV-R})$ vs. phase angle for the interval $(0, \pi / 6)$.

Fig. 2.7 Amplitude of $\text{Im}(i_{AV-R})$ phase angle for the interval $(0, \pi / 6)$.
2.2. Current calculation method for DCM circuits

2.2.1. Determination of the rms currents in DCM

The Discontinuous Conduction Mode (DCM) is one of the viable modes of operation for three-phase Power Factor Correction (PFC) circuits. In this operating mode, the current in the inductors reaches zero in every switching cycle and creates a significant influence of the switching frequency fundamental and harmonics on the rating of the passive components.

The average and rms values of the current during a switching period are calculated with the following formulas:

\[ i_{ave_{SW}}(t) = \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i(t) dt \]  
\[ i_{rms_{SW}}(t) = \sqrt{\frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i^2(t) dt} \]

where:

- \( i_{ave_{SW}}(t) \) = average value over a switching period;
- \( i_{rms_{SW}}(t) \) = rms value over a switching period;
- \( i(t) \) = instantaneous value.

The averaging method proposed in [31] calculates the average per switching cycle, as given by the following formula:

\[ I_{RMS_{LINE}} = \sqrt{\frac{1}{T_{LINE}} \int_{0}^{T_{LINE}} i_{ave}^2(t) dt} = \sqrt{\frac{1}{T_{LINE}} \int_{0}^{T_{LINE}} \left( \frac{1}{T_{SW}} \int_{t}^{t+T_{SW}} i(t) dt \right)^2 dt} \]  

Since the assumption \( f_{SW} >> f_{LINE} \), the average value determined over a switching cycle is seen as an 'instantaneous' value of the current at line frequency.

In the present thesis, the method is extended to the determination per switching cycle not only of the average value of the current, but also of the rms value. Further on, it is considered that for a small number of switching cycles the waveform of the current is repeatable and consequently the Fourier analysis can be
applied. Consequently, the switching frequency fundamental and its harmonics can be analytically determined for every phase angle. Normalized currents are used in the calculations.

The total rms current can be determined over a period at the line frequency by integrating the instantaneous rms currents as shown in the following:

\[ I_{\text{RMSTOT}} = \frac{1}{T_{\text{LINE}}} \int_{0}^{T_{\text{LINE}}} i_{\text{rms}}(t)^{2} dt = \frac{1}{T_{\text{SW}}} \int_{0}^{T_{\text{SW}}} \left( \frac{1}{T_{\text{SW}}} \int_{-T_{\text{SW}}}^{T_{\text{SW}}} i(t)^{2} dt \right) dt \]  

(2-20)

where:

- \( i_{\text{rms}}(t) \) = rms value over a switching period;
- \( i(t) \) = instantaneous value.
- \( I_{\text{RMSTOT}} \) = total rms value.

The rms contribution of the switching frequency component is determined as follows:

\[ I_{\text{RMSfsw}} = \sqrt{I_{\text{RMSfsw}}^{2} - I_{\text{RMSfline}}^{2}} \]  

(2-21)

where:

- \( i_{\text{avg}}(t) \) = average value over a switching period;
- \( I_{\text{RMSfline}} \) = total rms value of the line frequency fundamental and its harmonics ;
- \( I_{\text{RMSfsw}} \) = total rms value of the switching frequency fundamental and its harmonics.

On the other hand we can write:

\[ I_{\text{RMSfsw}} = \sqrt{I_{\text{RMSfsw}}^{2} - i^{2}_{fsw-nh} + I_{\text{RMSfsw}}^{2} - i^{2}_{fsw-2nh} + I_{\text{RMSfsw}}^{2} - i^{2}_{fsw-3nh} + \ldots} \]  

(2-22)

where:

\[ I_{\text{RMSfsw-nh}} = \frac{1}{T_{\text{LINE}}} \int_{0}^{T_{\text{LINE}}} i_{fsw-nh}^{2}(t) dt \]  

(2-23)

\[ i_{fsw-nh}(t) = \sqrt{i_{fsw-nh-\sin}^{2}(t) + i_{fsw-nh-\cos}^{2}(t)} \]

\[ i_{fsw-nh-\sin}(t) = \frac{1}{T_{\text{SW}}} \int_{-T_{\text{SW}}}^{T_{\text{SW}}} i(t) \sin(n \omega t) dt \]
Due to the popularity of the boost-star, the generalized formulas used to calculate the switching frequency harmonics for this circuit are given in Appendix A (A4-A9) for the \(0, \pi / 3\) interval. They have been obtained by substituting the functions describing the current waveforms, Appendix A (A1-A3), into the expressions (2-19, 2-20, 2-23).

In plotting the waveform for the whole line period, the following symmetry conditions have been used:

\[
\begin{align*}
0 < \omega t < \pi / 6 & \quad \quad i_A(\omega t) = i_A(\pi - \omega t) = -i_A(\pi + \omega t) = -i_A(2\pi - \omega t) \\
\pi / 6 < \omega t < \pi / 3 & \quad \quad i_A(\omega t) = i_C(\pi / 3 - \omega t) \\
\pi / 3 < \omega t < \pi / 2 & \quad \quad i_A(\omega t) = -i_b(\omega t - \pi / 3)
\end{align*}
\]

(2-24)

Once formulas have been developed for the 'instantaneous' rms, average, switching frequency fundamental and its harmonics, their overall contribution can be calculated by determining the rms values over the line frequency cycle. It must be specified that where rms contribution is mentioned, the square of the rms currents is meant, in such way that their sum is equal to 100%.

The current waveforms during the switching cycle are different for various PFC circuits, so the formulas have to be determined for each of them. In the case of the boost-star PFC circuit, the plots of the line frequency rms and average values, as well as switching frequency and its harmonics rms currents are given in Fig. 2.8 vs. the phase angle. The normalizing current for the inductor is \(V_n T_{on} / 2L\).
The total rms contribution shown in Fig. 2.9 varies with the duty cycle for a fixed voltage transfer ratio M. The fact that the rms contribution of the switching frequency fundamental and harmonics is maximum at less than the maximum duty cycle will help in the estimation of the heat losses in the inductors. A separation of the copper losses due to the line frequency component and due to the skin effect at the switching frequency and its harmonics is thus possible for the inductor winding.

By inspecting Fig. 2.10 it can be seen that at maximum duty cycle and variable M, the main contributors to the total rms are the line and switching frequency components. The duty cycle is defined as $D = \frac{T_{on}}{T_{sw}}$ and depends on M, when the criteria of maximum power throughput is chosen.
CHAPTER 3

BOOST, SINGLE-STAGE CIRCUITS

Two circuits, the boost-star and boost-delta PFC are proposed in the present chapter. The location of the switches on the AC-side allows a superior performance when compared with the circuits previously available in DCM. A complete analysis of the circuit properties is carried out using the tools developed in the previous chapter. For the boost-delta, the improvement of the performance is investigated for the case of sixth harmonic injected into the duty cycle.
3.1. Boost-star circuit with AC side switches

3.1.1. Introduction

The limitations of the boost-star circuit with DC-side switch have been shown in Section 2.1. The possibility for the individual control of the current waveform in each phase is not available due to the existence of a single switch. If switches are placed on the AC rather than the DC side, the circuit in Fig. 3.1 is obtained and different modulation possibilities are achieved. Such a circuit can be implemented with three delta-connected bi-directional switches or a ‘quasi tri-directional switch’ as will be shown in Section 3.1.4.

By introducing modulation, i.e. switch ON-times starting at different time points and/or of different lengths, it becomes possible to influence the evolution of the current waveform for each phase. The independent control of the component switches gives a much wider flexibility of operation and leading or lagging current can be obtained.

As it can be seen in Fig. 3.1 the voltage follower control loop is present like in all other PFC circuits operating in DCM. The voltage compensator block adjusts $T_{on}$ based on the voltage transfer ratio, $M$, which in turn depends on the amount of power processed. The control addition consists in the phase detector block. Its output, the phase angle $\omega t$, will determine the modulation parameters $t_a$ and $T_{sw}$, as it will be shown in this chapter.

There are many modulation possibilities, some of which are shown in Figs. 3.2-3.3: at the beginning of the on interval and at the end of the on interval. Another possibility is to keep the on-time and duty cycle constant for all three switches and have every few cycles only two switches turned on. Since the switching frequency is considered much higher than the line frequency, the average current over a few cycles can be considered as an instantaneous value at the line frequency. Here the first two modulation types mentioned will be analyzed. It will be shown that zero THD and unity power factor are possible with a certain analytically determined modulation of the ON-time and switching period. A simpler practical implementation could use an approximation of the analytical results and obtain very good performance.
Fig. 3.1 Boost-star PFC circuit with AC-side switch.

Fig. 3.2 Modulation at the end of the ON-interval.

Fig. 3.3 Modulation at the beginning of the ON-interval.
3.1.2. Modulation at the beginning of the ON-interval

The equations describing the current evolution in each phase are given in the Appendix B in formulas (B11-B16) for various combinations of switch turn-offs at the beginning of the ON-interval. A simple strategy for obtaining a low harmonic current is to modulate during one switching cycle only one set of the available space vectors.

Applying the formula (2-13) for the case of the boost circuit with AC-side switches, we obtain:

\[ i_{\text{sw}} = \frac{1}{2T_{\text{sw}}} \left[ \left( t_{\text{sw}} \right) \eta + i(t_{\text{sw}}) T_{\text{sw}} + i(t_{\text{sw}} + T_{\text{sw}}) \eta + i(t_{\text{sw}} + T_{\text{sw}} + t_{\text{sw}}) \eta + i(t_{\text{sw}} + T_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}}) \eta \right] \]  

(3-1)

equivalent to:

\[ i_{\text{sw}} = i(t_{\text{sw}}) \eta + i(t_{\text{sw}} + T_{\text{sw}}) \eta + i(t_{\text{sw}} + T_{\text{sw}} + t_{\text{sw}}) \eta + i(t_{\text{sw}} + T_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}}) \eta \]  

(3-2)

We obtain:

\[
i_{\text{AV}} = \frac{\sqrt{3}(V_{A} - V_{B})}{3L} e^{-j(t_{\text{sw}} + t_{\text{sw}})} t_{\text{sw}} + \frac{V_{m}}{L} e^{j(t_{\text{sw}} + t_{\text{sw}})} \left( T_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} \right) + \frac{2V_{D}}{3L} e^{j2\pi t_{\text{sw}}} t_{\text{sw}} (t_{\text{sw}} + t_{\text{sw}}) \]

(3-3)

\[
i_{\text{AV}} = \frac{\sqrt{3}(V_{C} - V_{A})}{3L} e^{-j(t_{\text{sw}} + t_{\text{sw}})} t_{\text{sw}} + \frac{V_{m}}{L} e^{j(t_{\text{sw}} + t_{\text{sw}})} \left( T_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} \right) + \frac{2V_{D}}{3L} e^{j2\pi t_{\text{sw}}} t_{\text{sw}} (t_{\text{sw}} + t_{\text{sw}}) \]

(3-4)

\[
i_{\text{AV}} = \frac{\sqrt{3}(V_{B} - V_{C})}{3L} e^{j(t_{\text{sw}} + t_{\text{sw}})} t_{\text{sw}} + \frac{V_{m}}{L} e^{j(t_{\text{sw}} + t_{\text{sw}})} \left( T_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} + t_{\text{sw}} \right) + \frac{2V_{D}}{3L} e^{j2\pi t_{\text{sw}}} t_{\text{sw}} (t_{\text{sw}} + t_{\text{sw}}) \]

(3-5)

By inspecting the formulas it becomes clear that for the interval \((0, \pi/6)\) the only modulation possible for obtaining a sinusoidal current in phase with the voltage is 110. As can be noticed, in this case a leading power factor could be obtained by modulating 110 and a lagging power factor by adjusting the 101 or 011 vectors.
A space vector diagram can be drawn in order to give a graphical representation of the reason why the 110 modulation is useful. The amplitude of the component vectors from (3-3), represented in Fig. 3.5, is given below:

\[ I_1 = \frac{V_m}{L} \left( \frac{T_{ON} + t_1}{2T_{SW}} \right) \]

\[ I_2 = \frac{\sqrt{3}(V_A - V_B)}{3L} t_a \left( t_a + 2T_{ON} + 2t_1 + t_2 \right) \frac{1}{2T_{SW}} \]

\[ I_3 = \frac{\sqrt{3}(V_C - V_A)}{3L} t_a \left( t_a + 2T_{ON} + 2t_1 + t_2 \right) \frac{1}{2T_{SW}} \]

\[ I_4 = \frac{\sqrt{3}(V_B - V_C)}{3L} t_a \left( t_a + 2T_{ON} + 2t_1 + t_2 \right) \frac{1}{2T_{SW}} \]

\[ I_5 = \frac{2V_D}{3L} \frac{t_1(t_1 + t_2)}{2T_{SW}} \]

In Fig. 3.5 the alignment of the average current vector to the input voltage vector is detailed. In Fig. 3.5b it can be seen how by using the 110 modulation the vector components give a resultant average current in phase with the voltage. In order to have a more visual representation, Fig. 3.5a shows how the current flows initially only in phases A and B until time \( t_a \). The trajectory of the instantaneous current space vector during a switching cycle is shown in Fig. 3.5c with dotted lines.

Let us rotate the reference axis by \( (\pi / 2 - \omega t) \) for simplicity of calculation:

\[ i_{AV} = \frac{\sqrt{3}(V_A - V_B)}{3L} e^{j(\pi / 3 - \omega t)} t_a \left( t_a + 2T_{ON} + 2t_1 + t_2 \right) \frac{V_m}{L} \left( \frac{T_{ON} + t_1}{2T_{SW}} \right) \left( \frac{T_{ON} + t_1}{2T_{SW}} \right) \frac{2V_D}{3L} e^{j(\pi / 2 - \omega t)} \frac{t_1(t_1 + t_2)}{2T_{SW}} \]

The contribution of the \( e^{j2\pi / 3} \) and \( e^{-j\pi / 6} \) must cancel each other.

\[ \text{Re}(i_{AV}) = ct. \quad \text{Im}(i_{AV}) = 0. \]

This system of equations can be solved by varying \( t_a \) in order to obtain \( \text{Im}(i_{AV}) = 0 \) and \( T_{SW} \) for \( \text{Re}(i_{AV}) = ct. \) From \( \text{Im}(i_{AV}) = 0 \) we obtain:

\[ t_a \left( t_a + 2T_{ON} + 2t_1 + t_2 \right) \sin(\pi / 3 - \omega t) = t_1(t_1 + t_2) \frac{2V_D}{\sqrt{3}(V_A - V_B) \sin(\pi / 6 - \omega t)} \]

From \( \text{Re}(i_{AV}) = ct. \) we obtain:
Fig. 3.5 a) Phase current waveforms for the boost-star PFC circuit with AC-side switches and 110 modulation, b) Average current space vector, c) Instantaneous current space vector trajectory.
Given a fixed $T_{ON}$ and $t_{w-r}$ to meet $\text{Im}(i_{AV}) = 0$, now $T_{SW}$ can be determined for $\text{Re}(i_{AV}) = ct$.

The average current can be written as:

$$i_{AV} = \frac{V_m T_{ON}}{2L} \cdot \frac{f(\omega t)}{T_{SW-\omega}(\omega t)} = ct. \quad (3-14)$$

where:

$$T_{SW-\omega}(\omega t) = \frac{T_{SW}(\omega t)}{T_{ON}} \quad (3-15)$$

$$T_{sw}(\omega t) = T_{ON} + t_a(\omega t) + t_{t_1}(\omega t) + t_2(\omega t) \quad (3-16)$$

It has been proven through MATLAB simulations that:

$$T_{SW}(\omega t) > T_{sw}(\omega t) \text{ for } 0 < \omega t < \pi / 6 \text{ and,} \quad (3-17)$$

$$T_{SW}(\omega t) = T_{sw}(\omega t) \text{ for } \omega t = \{0, \pi / 6\} \text{.}$$

This makes it possible to choose:

$$T_{SW-\omega}(\omega t) = f(\omega t) \text{ resulting in:} \quad (3-18)$$

$$i_{AV} = \frac{V_m T_{ON}}{2L} \cdot \frac{f(\omega t)}{T_{SW-\omega}(\omega t)} = 1$$

One important consequence of choosing $T_{SW-\omega}(\omega t)$ in this way is a maximization of the power throughput of the rectifier.

The solutions to the equation in (3-32) are given in Appendix B in formulas (B17-B21). The results for $t_a$ and $T_{SW}$ have been determined using MATLAB and are shown in Figs. 3.6-3.12. The plots given in the following are an illustration for $M=1.4$.
Fig. 3.6 The positive and negative roots of $t_a$ vs. phase angle. Interval $(0, \pi / 6)$.

Fig. 3.7 Diagram showing phase A goes out of conduction before phase C. $(0, \pi / 6)$ interval.

Fig. 3.8 The positive root of $t_a$ vs. phase angle. Interval $(0, \pi / 6)$.

Fig. 3.9 Times $T_{\text{in}}$ and $T_{\text{SW}}$ normalized to $T_{\text{ON}}$ vs. phase angle. Interval $(0, \pi / 6)$.

Fig. 3.10 Maximum $t_{\text{in}, R}$ vs. voltage transfer ratio.

Fig. 3.11 Maximum and minimum $T_{\text{SW}, R}$ vs. voltage transfer ratio.
It may be necessary in practice that an approximation of the ideal modulation be implemented, for sake of simplicity. An example is given in the following:

\[ M = 1.4, \quad T_{ov} = 1 \]

\[ i_a(\omega t) = 0.3 \sin(6\omega t) \quad \text{for} \quad 0 < \omega t < \pi / 6 \]  \hspace{1cm} (3-19)

\[ T_{sw}(\omega t) = 3.5 - 0.03(\omega t/2\pi) + 0.95\sin(6\omega t) \quad \text{for} \quad 0 < \omega t < \pi / 6 \]  \hspace{1cm} (3-20)

The normalized waveform obtained is presented in Fig. 3.13.

The resulting harmonics meet the IEC 1000-3-2 throughout the whole range of power:

\[ i_{w5} = 0.3929\% , \quad i_{w7} = 0.7278\% , \quad i_{w11} = 0.5444\% , \quad i_{w13} = 0.3276\% , \quad i_{w17} = 0.4199\% , \quad i_{w19} = 0.0375\% . \]

The interval studied was \( 0 < \omega t < \pi / 6 \). In order to give a picture of the way the modulation would occur at line frequency, the sequence of switches with duty cycle modulation is shown in Fig. 3.14. The amount of modulation is the same as for the interval studied, based on the phase angle.

Fig. 3.14 Sequence of switches with duty cycle modulation during a line period.
3.1.3. Modulation at the end of the ON-interval

The equations describing the current evolution in each phase are given in the Appendix B in formulas (B1-B6) for various combinations of switch turn-offs at the end of the ON-interval. A simple strategy for obtaining a low harmonic current is to modulate during one switching cycle only one set of the available space vectors.

Applying formula (2-13) for the case of the boost circuit with AC-side switches, we obtain:

\[ i_{AV} = \frac{1}{2T_{SW}} \left[ i(T_{ON}) T_{ON} + i(t_a) T_{ON} + i(t_1) T_{ON} + i(t_2) T_{ON} \right] \]

\[ i_{AV} = i(T_{ON}) T_{ON} + i(t_a) \frac{T_{ON} + t_1}{2T_{SW}} + i(t_1) \frac{T_{ON} + t_2}{2T_{SW}} \]

We obtain:

110 (SW1=on SW2=on SW3=off)

\[ i_{AV} = \frac{V_m}{L} e^{j(\omega t-\pi/2)} \left( T_{ON} + t_a + t_1 \right) \left( T_{ON} + t_a + t_1 + t_2 \right) + \frac{2V_D}{3L} e^{j\pi/3} \frac{t_a + 2t_1 + t_2}{2T_{SW}} + \frac{2V_D}{3L} e^{j2\pi/3} \frac{t_1}{2T_{SW}} \]

000, 101 (SW1=off SW2=off SW3=off), (SW1=on SW2=off SW3=on)

\[ i_{AV} = \frac{V_m}{L} e^{j(\omega t-\pi/2)} \left( T_{ON} + t_a + t_1 \right) \left( T_{ON} + t_a + t_1 + t_2 \right) + \frac{2V_D}{3L} e^{j\pi/3} \frac{t_a + 2t_1 + t_2}{2T_{SW}} + \frac{2V_D}{3L} e^{j2\pi/3} \frac{t_1}{2T_{SW}} \]

011 (SW1=off SW2=on SW3=on)

\[ i_{AV} = \frac{V_m}{L} e^{j(\omega t-\pi/2)} \left( T_{ON} + t_a + t_1 \right) \left( T_{ON} + t_a + t_1 + t_2 \right) + \frac{2V_D}{3L} e^{j\pi/3} \frac{t_a + 2t_1 + t_2}{2T_{SW}} + \frac{2V_D}{3L} e^{j2\pi/3} \frac{t_1 + t_2}{2T_{SW}} \]

By inspecting the formulas it becomes clear that for the interval \((0, \pi/6)\) the only modulation possible for obtaining a sinusoidal current in phase with the voltage is 110. As can be seen, in this case a leading power factor could be obtained by modulating 110 and a lagging power factor by adjusting 101 or 011 vectors. A space vector diagram can be drawn in order to give a graphical representation of the reason why the 110 modulation pattern is useful. The amplitude of the vectors shown in Fig. 3.15 is given below:
Let us rotate the reference axis by \((\pi / 2 - \omega t)\) for simplicity of calculation:

\[
i_{av} = \frac{V_m}{L} \left( \frac{(T_{ON} + t_a + t_1)(T_{ON} + t_a + t_2)}{2T_{SW}} + \frac{2V_D}{3L} e^{j(\pi / 6 - \omega t)} \frac{t_a(t_a + 2t_1 + t_2)}{2T_{SW}} + \frac{2V_D}{3L} e^{j(\pi / 6 + \omega t)} \frac{t_1(t_1 + t_2)}{2T_{SW}} \right)
\]  

(3-29)

The contribution of the \(e^{j2\pi / 3}\) and \(e^{j\pi / 3}\) must cancel each other.

\[\text{Re}(i_{av}) = ct. \quad \text{Im}(i_{av}) = 0\]

(3-30)

This system of equations can be solved by varying \(t_a\) in order to obtain \(\text{Im}(i_{av}) = 0\) and \(T_{SW}\) for \(\text{Re}(i_{av}) = ct.\)

With \(\text{Im}(i_{av}) = 0\) yields:

\[t_a(t_a + 2t_1 + t_2)\sin(\pi / 6 + \omega t) = t_1(t_1 + t_2)\sin(\pi / 6 - \omega t)\]

(3-31)

Therefore with \(\text{Re}(i_{av}) = ct.\) we obtain:

\[
i_{av} = \frac{V_m}{L} \left( \frac{(T_{ON} + t_a + t_1)(T_{ON} + t_a + t_2)}{2T_{SW}} \right)
\]

(3-32)
\[ + \frac{2V_D}{3L} \cos\left(\frac{5\pi}{6} - \omega t\right) \frac{t_a}{2T_{SW}} \left( t_a + 2t_1 + t_2 \right) + \frac{2V_D}{3L} \cos\left(\frac{7\pi}{6} - \omega t\right) \frac{t_i}{2T_{SW}} \left( t_1 + t_2 \right) = ct \]

Given a fixed \( T_{ON} \) and \( t_{a,r} \) to meet \( \text{Im}(i_{AV}) = 0 \), now \( T_{SW} \) can be determined for \( \text{Re}(i_{AV}) = ct \).

The average current can be written as:

\[ i_{AV} = \frac{V_m T_{ON}}{2L} \frac{f(\omega t)}{T_{SW-}\((\omega t)\)) = ct \tag{3-33} \]

where:

\[ T_{SW-}\((\omega t)\) = \frac{T_{SW}(\omega t)}{T_{ON}} \tag{3-34} \]

\[ T_{sw}(\omega t) = T_{ON} + t_a(\omega t) + t_i(\omega t) + t_2(\omega t) \tag{3-35} \]

It has been proven through MATLAB simulations that:

\[ T_{SW}(\omega t) = T_{sw}(\omega t) \text{ for } \omega t \in [0, \pi/6] \tag{3-36} \]

That makes it possible to choose:

\[ T_{SW-}(\omega t) = f(\omega t) \text{ resulting in:} \tag{3-37} \]

\[ i_{AV} = \frac{V_m T_{ON}}{2L} \frac{f(\omega t)}{T_{SW-}(\omega t))} = 1 \]

One important consequence of choosing \( T_{SW-}(\omega t) \) in this way is a maximization of the power throughput of the rectifier. The solutions to the equation in (3-11) are given in Appendix B in formulas (B7-B10). The results for \( t_a \) and \( T_{SW} \) have been determined using MATLAB and are shown in Figs. 3.16-3.22. The plots given in the following are an illustration for \( M=1.4 \).

Fig. 3.16 The positive and negative roots of \( t_a \) vs. phase angle. \((0, \pi/6)\) interval.

Fig. 3.17 Diagram showing phase A goes out of conduction before phase C. \((0, \pi/6)\) interval.
Fig. 3.18 The positive root of $t_a$ vs. phase angle. $(0, \pi/6)$ interval.

Fig. 3.19 Times $T_{OH}$ and $T_{SW}$ normalized to $T_{ON}$ vs. phase angle. $(0, \pi/6)$ interval.

Fig. 3.20 Maximum $t_{a-R}$ vs. voltage transfer ratio $M$.

Fig. 3.21 Maximum and minimum $T_{SW-R}$ vs. voltage transfer ratio $M$.

Fig. 3.22 Ratio maximum/minimum $T_{SW}$ vs. voltage transfer ratio $M$.

Fig. 3.23 Current waveform with approximating modulation vs. phase angle. $(0, 2\pi)$ interval.
Maximum ratio $I_{av} / T_{SW} = 1$.

It may be necessary in practice that an approximation of the ideal modulation be implemented with analog circuitry. An example is given in the following:

$M=1.4$, $T_{ov} = 1$

\begin{align*}
    t_a(\omega t) &= 0.2\sin(6\omega t) + 0.167\sin(12\omega t) \quad \text{for } 0 < \omega t < \pi / 12 \\
    t_a(\omega t) &= 0.2\sin(6\omega t) \quad \text{for } \pi / 12 < \omega t < \pi / 6 \\
    T_{SW}(\omega t) &= 3.7 - 0.035(\omega t / 2\pi) \quad \text{for } 0 < \omega t < \pi / 6
\end{align*}

(3-38) (3-39) (3-40)

The normalized waveform obtained is presented in Fig. 3.23.

The resulting harmonics meet the IEC 1000-3-2 throughout the whole range of power:

\[ i_{\omega 5} = 3.1078\% , \quad i_{\omega 7} = 0.5637\% , \quad i_{\omega 11} = 1.4032\% , \quad i_{\omega 13} = 1.2751\% , \quad i_{\omega 17} = 0.7924\% , \quad i_{\omega 19} = 0.4006\% . \]

The sequence of switches with duty cycle modulation is the same as presented in Fig. 3.14.

### 3.1.4. The Quasi Tri-directional Switch

A new 'quasi tri-directional switch' is proposed for application in three-phase Power Factor Correction (PFC) circuits. In regards to the implementation, a 'quasi tri-directional' switch can be used as an AC-side switch. The term 'quasi' comes from the fact that the current flow can be controlled in one direction, of the IGBT, but it is independent of the gating in the opposite direction, of the diode.

The 'quasi tri-directional' switch consists of three IGBTs with anti-parallel diodes and common-emitter connected. The gating signals have thus a common point for all three IGBTs. A reduction of the number of transistors is obtained by implementation in circuits formerly using three bi-directional switches, without any compromise on the performance.

The bi-directional switch shown in Fig. 3.24a has been applied in various three-phase PFC circuits [37,38].

The practical implementation of this switch can be done with today’s components as in Figs. 3.24b and 3.24c. On the other hand an Insulated Gate Bipolar Transistor (IGBT) with anti-parallel diode, shown in Figure 3.24d, can be seen as a 'quasi bi-directional switch'.
In three phase PFC circuits [37,39] the bi-directional switch has been used in delta and star configurations, as shown in Figs. 3.25a and 3.25b. The present thesis proposes the use of the star connected ‘quasi tri-directional switch’, Fig. 3.25c, instead of three bi-directional switches. The advantage is that the number of IGBTs is reduced to half and at the same time a common emitter allows easy gate control.

The quasi tri-directional switch can be used both in continuous and discontinuous conduction mode PFC circuits. Many of the circuits proposed in the thesis could use this type of switch, including the one studied in the present chapter. In the comparison section 7.1, Table 7.1 shows the voltage and current rating of the IGBTs for the circuits where two alternatives are applicable: quasi tri-directional and three bi-directional switches.
3.2. Boost-delta circuit

3.2.1. Introduction

A new PFC circuit operating in DCM is proposed. The circuit is called boost-delta and is shown in Fig. 3.26. The difference between the boost-star and boost-delta PFC circuits consists in the way the boost inductors are connected during the switches' on-time. As the names indicate, in the first case the inductors are star connected across the supply, while in the second case they are delta connected. That makes the current build-up in the inductors proportional to the instantaneous voltages as follows: phase-to-neutral for the boost-star and phase-to-phase for the boost-delta. During the off time, the inductors are series connected with the supply in both cases, dumping their energy into the load.

Three bi-directional switches with simultaneous triggering are needed for the implementation of the boost-delta PFC. The circuits harmonic content is determined, and compared with the performance of the boost-star with a DC-side switch.

![Fig. 3.26 Boost-delta 3-phase 3-switch PFC circuit.](image)

3.2.2. Analysis of the boost-delta PFC

In order to analyze the new PFC circuit, it is sufficient to consider one sixth of the line period, e.g. the \((0, \pi/3)\) interval. The whole analysis is carried out in Appendix C. Only the results are presented here.
Fig. 3.27 Proposed circuit. Switches closed.

Fig. 3.28 Proposed circuit for the interval $(0, \pi / 3)$ when current flows in three inductors.

Fig. 3.29 Proposed circuit for the interval $(0, \pi / 3)$, when current reaches zero first in inductor $L_1$.

Fig. 3.30 Proposed circuit for the interval $(0, \pi / 3)$, when current reaches zero first in inductor $L_3$.

Fig. 3.31 Phase current vs. phase angle over one period, at various voltage transfer ratios $M$. Boost-delta circuit.

Fig. 3.32 Average inductor current vs. phase angle over one period, at various voltage transfer ratios $M$. Boost-delta circuit.
The equivalent circuits for the period when current is flowing in the inductors are presented in Fig. 3.27-3.30. Simulations carried out show that up to a certain angle, dependent on \( M \), the current in inductor 1 is the first to reach zero, beyond that point the current in inductor 3 reaches zero first. The angle is dependent on the voltage transfer ratio \( M \), and is given in Fig. 3.33, resulting from the expressions (C-6) developed in Appendix C.

![Fig. 3.33 Plot showing the times (normalized to \( T_{on} \)) at which the current through the inductors reaches zero vs. phase angle. \((0, \pi / 6)\) interval. Voltage transfer ratio \( M=3 \).](image)

![Fig. 3.34 Phase current waveforms during a switching cycle.](image)

Based on the derived analytical expressions, MATLAB has been used for obtaining the plots of the normalized phase and inductor currents, as shown in Figs. 3.31 and 3.32. The phase voltage reference was plotted in order to show the angle between the phase voltage and current and its amplitude has no significance in the context. A note should be made that for the boost-delta circuit, due to calculation reasons, the phase angle of the plots starts from the zero crossing of the phase-to-phase voltage rather than the phase-to-neutral as for the boost-star circuit.
The displacement angle can be determined by making the phase A average current equal to zero. Solving numerically for various M, it has been determined that the phase current is leading the phase voltage by an angle as shown in Fig. 3.36.

3.2.3. Component ratings

The study of the interval \((0, \pi / 6)\) is sufficient for the determination of the maximum voltage across the switch. For the period when all three inductors have a current flow:

\[
V_{sw1} = V_a - \frac{V_o}{3}
\]

\[
V_{sw2} = V_c + \frac{2V_o}{3}
\]

\[
V_{sw3} = V_d - \frac{V_o}{3}
\]

It has been determined that the maximum voltage happens across switch 2:

\[
\max(V_{sw2}) = V_{in}(1 + \frac{2\sqrt{3}M}{3})
\]

For the period when only two inductors have a current flow, it can be shown that the voltage is less than the value determined above. This result is confirmed by time-domain simulation results.

The peak inductor current is given by the expression:

\[
\max(i_{pk}) = \max(\frac{V_{ab} T_{ox}}{L}) = \frac{\sqrt{3} V_{in} T_{ox}/L}{L}
\]

The peak switch current is given by the expression:

\[
\max(i_{sw-pk}) = \max(\frac{V_{ab} T_{ox}}{L}) = \frac{\sqrt{3} V_{in} T_{ox}}{L}
\]

The average instantaneous switch current is:

\[
i_{av-sw}(t) = \frac{V_{ab} T_{ox}}{L} \frac{T_{ox}}{2t} = \frac{V_{ab} T_{ox}^2}{2Lt} = \frac{\sqrt{3} V_{in} T_{ox}^2}{2Lt} \sin(\omega t)
\]

The time-domain simulation of the circuit has been done using PSIM. A comparison of the theoretical calculations, time-domains simulations and experimental measurements has been carried out in Chapter 6.
3.2.4. Harmonic Injection

The boost-star circuit [11], has been extensively studied. Inherently, the circuit has a high 5th harmonic component and a high Total Harmonic Distortion (THD) at low voltage transfer ratios M and fixed duty-cycle operation. Consequently, in [13,33-35], various harmonic injection techniques which modulate the duty cycle have been proposed.

The properties of the boost-delta circuit are further investigated in regards to harmonic reduction. The 5th and 7th harmonics are determined for various voltage transfer ratios and so is the phase angle by which the current leads the voltage. A harmonic injection technique is proposed in order to reduce the THD.

A comparison is made between the boost-delta and the boost-star circuits, with and without harmonic injection. The criterion is the maximum power handling capability in light of the requirements of the IEC 1000-3-2 standard.

The 5th and 7th harmonics of the phase currents for the two circuits are presented in Fig. 3.35. The boost-delta shows a slightly better performance than the boost-star circuit.

![Fig. 3.35 5th and 7th harmonics (%) vs. voltage transfer ratio M.](image1)

![Fig. 3.36 Leading angle of phase current vs. voltage transfer ratio M. Boost-delta circuit.](image2)

An interesting property of the boost-delta is that, unlike the boost-star where the current fundamental is in phase with the voltage, here the current is leading the voltage (for a certain phase sequence). The leading
angle is dependent on the voltage transfer ratio $M$ as shown in Fig. 3.36. The same plot shows the current zero crossing angle which is different from the leading angle mentioned above due to the asymmetry of the waveform.

Analyzing Fig. 3.35 it can be seen that the $5^{th}$ harmonic, in particular, is quite large at low voltage transfer ratios. This limits the power capability of the circuits which have to meet the absolute harmonic values stipulated by the IEC 1000-3-2 standard. The various harmonic injection techniques proposed in [13,33-35] revolve around the idea of introducing a $6^{th}$ harmonic component in the duty cycle, one example being the formula in [34]:

$$d = d_{\text{max}} - m(1 + \cos(6\omega_t))$$

(3-46)

where: $m =$ injected harmonic amplitude.

A harmonic injection technique which improves the performance of the boost-delta circuit is proposed in the following. It is also based on the modulation of the duty cycle with a $6^{th}$ harmonic of the line frequency. However, the modulation is done with a sine term rather than a cosine as in the boost-star circuit:

$$d = d_{\text{max}} - m(1 + \sin(6\omega_t))$$

(3-47)

MATLAB has been used for the determination of the optimum amplitude of the injected harmonic in order to maximize the power capability. As an example of the improvement possibility, the shape of the phase current is shown in Fig. 3.37 for a voltage transfer ratio $M=1.5$ with and without harmonic injection.

![Graph](image-url)

*Fig. 3.37 Normalized phase current vs. phase angle over one period. Boost-delta circuit. $M=1.5$*
A comparison is drawn between the boost-star and boost-delta circuits, with and without harmonic injection. The optimization criterion is maximum power throughput while satisfying the IEC 1000-3-2 requirements.

A short presentation of the IEC 1000-3-2 will be made in the following:

- the voltage at which the measurements are made is 3 phase 400V, 50Hz;
- the absolute rms value of the line current and its harmonics are given: fundamental current, 16 A; 5th harmonic, 1.14 A; 7th harmonic, 0.77 A; 11th harmonic, 0.33 A; 13th harmonic, 0.21 A.
- the maximum power to which the standard applies is:

\[ P_{\text{max}} = \sqrt{3} \times 400V \times 16A = 11,072W \]  

(3-48)

- the relative values of the harmonics are:

\[ \text{5th harmonic } \frac{114}{16} \times 100 = 7.125\% ; \quad \text{7th harmonic } \frac{77}{16} \times 100 = 4.812\% \]  

(3-49)

\[ \text{11th harmonic } \frac{33}{16} \times 100 = 2.062\% ; \quad \text{13th harmonic } \frac{21}{16} \times 100 = 1.312\% \]

- the harmonics ratio:

\[ \frac{5^\text{th}}{7^\text{th}} = 1.481, \quad \frac{5^\text{th}}{11^\text{th}} = 3.455 \]  

(3-50)

The maximum power handled by the PFC circuits analyzed is determined based on the following optimization criteria:

a - for high voltage transfer ratios, the maximum power can be handled without harmonic injection, since the relative values of the harmonics are below the standard limits;

b - at lower voltage transfer ratios, harmonic injection is used in such way that the relative values of the harmonics are still below the standard limits and maximum power can be processed;

c - at very low voltage transfer ratios, the harmonic injection amplitude can be chosen in such a way that the harmonics ratios 5th/7th and 5th/11th are close to the standard limit. In this way, the power transferred is below the standard limit but it is maximized with respect to the absolute harmonic components acceptable.

The application of these criteria will be illustrated in Tables 3.1-3.4, which show the performance of the boost-star and boost-delta PFC circuits with and without harmonic injection.
Based on the results presented in Tables 3.2 and 3.4, the plots of the optimized amplitude of the injected sixth harmonic are shown in Fig. 3.38. Further on, the information in the tables is shown in a chart type comparison of the $5^{th}$ harmonic, THD and maximum power in Figs. 3.39-3.41.

The overall result is that the boost-delta has slightly better performance than the boost-star in terms of harmonics. By introducing harmonic injection, a significant reduction of the harmonics occurs for both circuits, while the boost-delta still preserves its small advantage.

Fig. 3.38 Injected harmonic amplitude vs. voltage transfer ratio, $M$ for the boost-star and boost delta circuits.

Fig. 3.39 $5^{th}$ harmonic vs. voltage transfer ratio. 
- a - boost-star without harmonic injection,
- b - boost-star with harmonic injection,
- c - boost-delta without harmonic injection,
- d - boost-delta with harmonic injection.

Fig. 3.40 Total Harmonic Distortion vs. voltage transfer ratio $M$.
- a - boost-star without harmonic injection,
- b - boost-star with harmonic injection,
- c - boost-delta without harmonic injection,
- d - boost-delta with harmonic injection.

Fig. 3.41 Maximum power based on harmonic content required by IEC 1000-3-2 vs. voltage transfer ratio $M$.
- a - boost-star without harmonic injection,
- b - boost-star with harmonic injection,
- c - boost-delta without harmonic injection,
- d - boost-delta with harmonic injection.
Table 3.1 Performance of the boost-star circuit without harmonic injection

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Table 3.2 Performance of the boost-star circuit with harmonic injection

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Table 3.3 Performance of the boost-delta circuit without harmonic injection

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<td>7.95</td>
<td>1.67</td>
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<td>0.40</td>
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<td>1.9</td>
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<td>0.76</td>
<td>0.36</td>
<td>7.53</td>
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<tr>
<td>2.0</td>
<td>0.781</td>
<td>6.80</td>
<td>1.52</td>
<td>0.68</td>
<td>0.33</td>
<td>7.01</td>
<td>11,072</td>
<td></td>
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Table 3.4 Performance of the boost-delta circuit with harmonic injection

<table>
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<th>M</th>
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<td>19.47</td>
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<td>5.21</td>
<td>0.91</td>
<td>24.81</td>
<td>0.0063</td>
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<td>2.60</td>
<td>1.12</td>
<td>0.47</td>
<td>7.70</td>
<td>0.0052</td>
<td>11,072</td>
<td>b</td>
<td></td>
<td></td>
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<tr>
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<td>0.78</td>
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<td>0.0008</td>
<td>11,072</td>
<td>b</td>
<td></td>
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<td>2.0</td>
<td>0.781</td>
<td>6.80</td>
<td>1.52</td>
<td>0.68</td>
<td>0.33</td>
<td>7.01</td>
<td>0</td>
<td>11,072</td>
<td>c</td>
<td></td>
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</tr>
</tbody>
</table>
3.2.5. Average current space vector analysis

Individual modulation of the switches is not possible due to the fact that after turn-off the three phase currents don’t add up to zero.

The averaged current space vector for the boost-delta circuit is calculated based on the method in Section 2.1. The resulting formulas, given below for the regular phase sequence, are visually represented in Fig. 3.42.

\[ I_{av} = \frac{1}{2T_{sw}} \left[ i(T_{on}) + i(T_{off}) + i(T_{on}) + i(T_{off}) \right] \]  

\[ I_{av} = \frac{V_m}{L} e^{j(0.7\pi/3)} \left( \frac{3T_{on}^2}{2T_{sw}} + \frac{t_1}{2T_{sw}} \right) + \frac{V_m}{L} e^{j(0.7\pi/3)} \frac{\sqrt{3}T_{on}(2t_1 + t_2)}{2T_{sw}} + \frac{2V_D}{3L} e^{j\pi/3} t_1(t_1 + t_2) \]  

\[ I_{av} = \frac{V_m}{L} e^{j(0.7\pi/3)} \left( \frac{3T_{on}^2}{2T_{sw}} + \frac{t_1}{2T_{sw}} \right) + \frac{V_m}{L} e^{j(0.7\pi/3)} \frac{\sqrt{3}T_{on}(2t_1 + t_2)}{2T_{sw}} + \frac{2V_D}{3L} e^{j\pi/3} t_1(t_1 + t_2) \]  

When two phases are reversed or the switches are connected in reverse sequence, the formula becomes (3-53) and the vectorial representation is as shown in Fig. 3.43.

\[ I_{av} = \frac{V_m}{L} e^{j(0.7\pi/3)} \left( \frac{3T_{on}^2}{2T_{sw}} + \frac{t_1}{2T_{sw}} \right) + \frac{V_m}{L} e^{j(0.7\pi/3)} \frac{\sqrt{3}T_{on}(2t_1 + t_2)}{2T_{sw}} + \frac{2V_D}{3L} e^{j\pi/3} t_1(t_1 + t_2) \]  

For the case where two boost-delta circuits, one non-reversed and one reversed are run in parallel, the formula is:

\[ I_{av} = \frac{V_m}{L} e^{j(0.7\pi/3)} \left( \frac{3T_{on}^2}{2T_{sw}} + \frac{t_1}{2T_{sw}} \right) + \frac{V_m}{L} e^{j(0.7\pi/3)} \frac{\sqrt{3}T_{on}(2t_1 + t_2)}{2T_{sw}} + \frac{2V_D}{3L} \left( e^{j\pi/3} t_1(t_1 + t_2) + e^{j\pi/3} t_2(t_1 + t_2) \right) \]  

After rotating the axes of coordinates by \((0.7\pi/2)\) the vector becomes:

\[ I_{av} = \frac{V_m}{L} \left( \frac{3T_{on}^2}{2T_{sw}} + t_1(t_1 + t_2) + t_2(t_1 + t_2) \right) + \frac{V_m}{L} \frac{\sqrt{3}T_{on}}{2T_{sw}} \left( e^{j\pi/6}(2t_1 + t_2) + e^{-j\pi/6}(2t_1 + t_2) \right) + \frac{2V_D}{3L} \left( e^{j(5\pi/6)\omega} t_1(t_1 + t_2) + e^{j(5\pi/6)\omega} t_2(t_1 + t_2) \right) \]  

The indexes \( n \) and \( r \) are used for the non-reversed and reversed phase sequence boost-delta circuits.
As it was mentioned in previous sections of this chapter the performance of a boost-delta PFC is comparable with the boost-star. However, when connecting two boost-delta circuits in parallel and their phase connections are reversed, the performance is significantly improved. The explanation is that the vectorial components not in phase tend to cancel each other, as can be seen by comparing Figs. 3.42 and 3.43.

The effect is presented in Fig. 3.44 where a dramatic reduction of the 5th harmonic occurs, particularly for M=1.4. This is the area of most interest due to the practical applicability: \( V_m = 208 V \), \( V_{ac} = 420 V \) for North America and \( V_m = 380 V \), \( V_{ac} = 750 V \) for Europe. Where perfectly sinusoidal current waveform must be obtained, two boost-delta circuits must be connected in parallel, with reversed phase sequence. An individual modulation of the duty cycle of each stage will make the circuit behave more inductively or capacitively, as needed. Then a sinusoidal current can be achieved, even if the input voltage has some distortion, by meeting the conditions given in formula (3-10).

3.2.6. Current calculations

Since the current waveforms during the switching cycle are different when compared with the boost-star circuit, the formulas are determined for the boost-delta as well. The formulas (2-19, 2-20, 2-23) are applied. The resulting plots are drawn in Figs. 3.45-3.47 for the inductor currents, at various voltage transfer ratios M and maximum duty cycle, as well as for fixed M and variable duty cycle. The total rms contribution shown in Fig. 3.46 varies with the duty cycle for a fixed voltage transfer ratio M. The fact that the rms contribution of the switching frequency fundamental and harmonics is maximum at less than the maximum duty cycle will help in the estimation of the heat losses in the inductors. A separation of the copper losses due to the line frequency component and due to the skin effect at the switching frequency and its harmonics is thus possible for the inductor winding.

By comparing the plots in Figs. 2.10 and 3.47, showing the rms contribution of the various harmonics at maximum duty cycle and variable M, it can be seen that the difference between the boost-star and boost-delta is small.
Fig. 3.42 Average current space vectors for boost-delta circuit.

Fig. 3.43 Average current space vectors.

Fig. 3.44 Boost-delta. One stage vs. two reverse connected. 5th and 7th harmonics (%) vs. voltage transfer ratio M.

Fig. 3.45 Normalized inductor currents vs. phase angle for the boost-delta circuit. M=1.5

Fig. 3.46 Total rms contribution (%) vs. duty cycle D for capacitor currents in the boost-delta circuit. M=1.5

Fig. 3.47 Total rms contribution vs. voltage transfer ratio M for the inductor currents. Boost-delta circuit. Max. duty cycle.
In this chapter PFC circuits with two boost stages are studied. Since the first stage can be a boost-star or a boost-delta, and the second stage a flyback or a boost-delta, four combinations become possible. The resulting circuits are analyzed using the average current space vector technique where possible, and a sequence of diode conducting stages in the other cases. The principles underlying the improvement of harmonic content in DCM are exposed. The advantages and disadvantages of n-stage PFC circuits are investigated.
4.1. ‘STARFLY’ Circuit

4.1.1. Introduction

A new family of PFC circuits operating in Discontinuous Conduction Mode is analyzed in this Chapter. The focus will be on two-stage circuits where two sets of inductors are used for boosting. A brief mention will be made about the features of n-stage circuits. Bi-directional and/or quasi tri-directional switches are needed for the implementation of these PFC circuits.

The Starfly is composed of a boost and a flyback stages, where the boost is directly in series with the input lines. A combination of the features of the boost and flyback is possible by changing the inductance ratio of two sets of inductors. A theoretical analysis is made in regards to the properties of the circuit. Design recommendations in light of the IEC 1000-3-2 requirements are given.

The Starfly circuit uses three bi-directional switches as shown in Fig. 4.1. The \( L_1 \) and \( L_2 \) sets of inductors are characteristic to the boost, and flyback PFC circuits, respectively the \( L_f \) and \( C_f \) components shown in Fig. 4.1 represent a low pass filter which eliminates the switching frequency fundamental and its harmonics from the line current. An analysis based on the method in [31] is presented for the Discontinuous Conduction Mode (DCM) operation.

![Fig. 4.1 'Starfly' PFC circuit.](image-url)
4.1.2. Analysis of the ‘Starfly’ Three-Phase PFC Circuit

The circuit proposed is analyzed with respect to its DCM operation. The three switches are simultaneously either on or off. The switching period is chosen in such way that the currents in both the boost and flyback parts of the circuit reach zero before the next turn-on of the switches. A voltage follower control is used for the switches, where the on time and switching period are fixed.

In order to analyze the circuit, it is sufficient to consider one twelfth of the line period, e.g. the interval \( (0, \pi / 6) \).

The inductance ratio is:

\[
T = \frac{L_2}{L_1}, \quad (4-1)
\]

The proposed starfly PFC stage has as particular cases the boost-star circuit with DC-side switch when \( T = 0 \), respectively flyback when \( T = \infty \).

While the boost circuit has a high Total Harmonic Distortion (THD) at low voltage transfer ratios, the flyback with zero THD suffers from high switch currents. The Starfly circuit alleviates these problems by compromising on the characteristics of the boost and flyback. That makes the circuit particularly interesting for the cases where low fifth and seventh harmonics, as well as THD are desirable at low voltage transfer ratios, i.e. \( M=1.3-1.5 \).

In practical applications that would allow the use of 1200V semiconductor devices for the European 380 V input voltage and 600V devices for the North American 208V, without the need for modulation of the duty cycle [13,33-35].

Other benefits are the reduced switch current as well as the smaller size of the inductors. This is achieved at the expense of the introduction of a second three-phase bridge of ultrafast recovery diodes.

With the assumption: \( f_{sw} \gg f_{line} \), the analysis method given in [1] can be applied. The equivalent circuit looks like Fig. 4.2 during the switch on time and like Fig. 4.3 during the off time.

The equations for the interval \( (0, \pi / 6) \) are given in Appendix D. The current waveforms during a switching cycle are shown in Figs. 4.4 and 4.5 for the inductor sets \( L_1 \) respectively \( L_2 \).
The line current is obtained by averaging the inductor current over each switching cycle and plotting these values for the entire line period.

The following formulas have been used in the analysis:

- the normalizing current:

\[
i_N = \frac{3V_{LN}}{3L_1 + L_2} T_{SW}
\]

(4-2)

- the normalizing power:

\[
P_N = \frac{9V_{LN}^2}{2(3L_1 + L_2)} T_{ON}
\]

(4-3)

where:

- \(T_{ON}\) = switch on time,
- \(T_{SW}\) = switching period.

- the normalized value of the fifth harmonic:

\[
\frac{I_5}{I_1} \times 100
\]

(4-4)

- the normalized value of the seventh harmonic:

\[
\frac{I_7}{I_1} \times 100
\]

(4-5)

- the Total Harmonic Distortion:

\[
THD(\%) = \sqrt{\frac{\sum_{n=1}^{16} I_n^2}{\frac{5}{2} I_1^2}} \times 100
\]

(4-6)

where:

- \(I_n\) = the \(n^{th}\) harmonic of the line current obtained by Fourier series decomposition.

The parameters which give a qualitative description on the performance of the circuit are defined as follows:

- the current ratio \(\hat{i}_1\): \(L_1\) global peak /peak of the phase fundamental:
\[
\frac{3V_{LN} T_{ON}}{3L_1 + L_2} \frac{3L_1 + L_2}{3L_1 + L_2} = \frac{T_{ON}}{T_{SW i_{1N}}} \tag{4-7}
\]

- the current ratio \( i_L : \) global peak /peak of the phase fundamental:

\[
\frac{\sqrt{3} V_{LN} T_{ON}}{3L_1 + L_2} \frac{3L_1 + L_2}{3L_1 + L_2} = \frac{T_{ON}}{\sqrt{3} T_{SW i_{1N}}} \tag{4-8}
\]

- the active power:

\[
P = \frac{9V_{LN}^2}{2(3L_1 + L_2)} T_{SW i_{1N}} \tag{4-9}
\]

- the ratio inductors energy/transmitted energy:

\[
\frac{\max \left( \frac{L_1 i_1^2}{2} \right) + \max \left( \frac{L_2 i_2^2}{2} \right)}{P_{av} T_{sw}} = \frac{T_{ON}^2}{3T_{SW i_{1N}}} \tag{4-10}
\]

where:

\( i_1 = \) instantaneous current through inductor \( L_1, \)

\( i_2 = \) instantaneous current through inductor \( L_2, \)

\( i_{1N} = \) peak of the fundamental of the average phase current,

\( P_{av} = \) average active power.

By looking at Figs. 4.6-4.8 it can be seen how by increasing \( T \) the line current waveforms are closer to sinusoids. The plots of the fifth and seventh normalized harmonics as well as the THD shown in Figs. 4.9-4.11 indicate an improvement with the increase of the inductance ratio \( T. \)

On the other hand higher \( T \) increases the switch current and deteriorates the performance indicators of the circuit, presented in Figs. 4.12-4.15.
Fig. 4.2 Equivalent circuit diagram of the proposed circuit when all switches are closed.

Fig. 4.3 Equivalent circuit diagram of the proposed circuit when all switches are opened.

Fig. 4.4 Inductor $L_1$ currents during a switching cycle.

Fig. 4.5 Inductor $L_2$ currents during a switching cycle.
Fig. 4.6 Normalized average phase current for boost circuit \((T = 0)\) over one period.

Fig. 4.7 Normalized average phase current for flyback circuit \((T = \infty)\) over one period.

Fig. 4.8 Normalized average phase current for starfly circuit \((T = 6)\) over one period.

Fig. 4.9 Normalized fifth harmonic (percentage) vs. voltage transfer ratio \(M\).

Fig. 4.10 Normalized seventh harmonic (percentage) vs. voltage transfer ratio \(M\).

Fig. 4.11 Total Harmonic Distortion (percentage) vs. voltage transfer ratio \(M\).
Fig. 4.12 Current ratio $i_2$ : $L_1$ global peak /peak of the phase fundamental vs. voltage transfer ratio $M$.

Fig. 4.13 Current ratio $i_2$ : $L_2$ global peak /peak of the phase fundamental vs. voltage transfer ratio $M$.

Fig. 4.14 Normalized active power vs. voltage transfer ratio $M$.

Fig. 4.15 Ratio inductors/transmitted energy vs. voltage transfer ratio $M$.

Fig. 4.16 Line current. Time domain simulation.

Fig. 4.17 Voltage transfer ratio $M$ vs. inductor ratio $T$ for meeting IEC 1000-3-2 requirements at various power levels.
4.1.3. Design Related Issues

The component ratings are determined theoretically and they are matched by the results of the time-domain simulation using PSIM. By inspection of the circuit the following component ratings can be determined:

- peak voltage across the switches and diodes:

\[
\max(V_{sw}) = V_D
\]  

(4-11)

- peak current through the switches and diodes:

\[
\max(i_{sw}) = \frac{3V_{IN}T_{ON}}{3L_1 + L_2}
\]  

(4-12)

- peak inductor \(L_1\) current:

\[
\max(i_{L1}) = \frac{3V_{IN}T_{ON}}{3L_1 + L_2}
\]  

(4-13)

- peak inductor \(L_2\) current:

\[
\max(i_{L2}) = \frac{\sqrt{3}V_{IN}T_{ON}}{3L_1 + L_2}
\]  

(4-14)

The time domain simulation was done with the following values:

\(V_{sin} = 400V / 50Hz\), \(V_D = 800V\), \(R = 59\Omega\), \(P_{out} = 10,850W\), \(L_1 = 35\mu H\), \(L_2 = 270\mu H\), \(T_{sw} = 40\mu s\), \(T_{ON} = 22.11\mu s\), \(T_{prop} = 0.1\mu s\), \(T_{total} = 0.035\) s.

For the sake of brevity only the line current, with the switching frequency and its harmonics filtered out, is shown in Fig. 4.16.

The requirements of IEC 1000-3-2 refer to absolute limits for the line frequency harmonics, for currents up to 16 A per phase.

By inspection of Figs. 4.9 and 4.10 it can be seen that only the 5th harmonic has a significant value. Based on the standard, the limit for the 5th harmonics relative value can be calculated as follows:

\[
\frac{I_5}{I_1} \times 100 = \frac{1.14}{16} \times 100 = 7.125\%
\]  

(4-15)

at maximum power throughput, i.e.:

\[
\sqrt{3} \times 400V \times 16A = 11,072W
\]  

(4-16)
Fig. 4.17 shows the inductance ratio T which allows various power throughput levels, while meeting the standard requirements. It can be seen that for the same M and lower powers T will be smaller. These plots can be a very helpful tool in the design, where after establishing the maximum throughput power, the output voltage and the voltage transfer ratio range, the minimum inductance ratio T allowable can be determined. In this way the peak current stress on the switches will be reduced most.

The features of the circuit can be seen in an overall comparison with other two-stages PFCs in Section 7.1.

4.1.4. Average current space vector analysis

The method developed in Section 2.1 can be applied for the analysis of the properties of the Starfly PFC circuit. The circuit represents in fact a boost-star PFC with AC-side switches interconnected with a flyback stage. For this reason the analysis is similar to the one carried out in Section 3.1 and the final equations are given in Appendix D. As expected, the modulation options are similar with those in Section 3.1

The average current space vector for the line is given by the following formula:

\[
i_{aL} = \left[ \frac{3V_m}{3L_1 + L_2} \frac{(T_{ON} + t_1)(T_{ON} + t_1 + t_2)}{2T_{SW}} + \frac{V_m L_2}{L_1(3L_1 + L_2)} \frac{t_1(t_1 + t_2)}{2T_{SW}} \right] e^{j\phi} + \frac{2V_m}{3L_1} \frac{t_1(t_1 + t_2)}{2T_{SW}} e^{j2\phi} \tag{4-17}
\]

The inductance \( L_2 \) appears this time in the expressions, and it is quite easy to prove that the ratio of the vector component out of phase to the one in phase is decreasing with the increase of the inductors ratio T.

As it was already shown in Section 4.1.2, and proven here by formula (4-17) the inductance of \( L_2 \) plays a harmonic reduction role. For sake of completeness the space vector formulas are given for modulation in the case of the Starfly. However, the relative complexity of the circuit would encourage a mitigation of the harmonic content based on the inductance ratio alone, and preservation of a fixed duty cycle, rather than on modulation.
4.2. ‘DELTAFLY’ Circuit

4.2.1. Introduction

A new three-phase three-switch Power Factor Correction (PFC) circuit operating in Discontinuous Conduction Mode (DCM), shown in Fig. 4.18, is proposed. The ‘Deltafly’ circuit consists of two stages, a boost-delta and a flyback, where the boost-delta is directly in series with the input line. The boost-delta circuit has a relatively high harmonic content and a leading/lagging current based on the phase sequence and voltage transfer ratio. While the flyback has zero Total Harmonic Distortion (THD) and in-phase current, high current/voltage stress on the switches limits its application. Just like in the case of the ‘Starfly’, a proportional combination of the features of the two stages is possible by changing the inductance ratio of the two sets of inductors.

The following analysis refers to the boost-delta operating with a leading current. The results for the lagging current situation, occurring for a reversed phase sequence, are determined in a similar way, based on the results in Section 3.2.

The ‘Deltafly’ circuit uses six bi-directional switches. The quasi tri-directional switches presented in Section 3.1.4 could replace two adjacent bi-directional switches by simply connecting the three independent nodes of the circuit. The gating becomes easier due to the common emitter point. There are two levels of complexity with regards to the operation of the switches. In the simplest, the switches are turned simultaneously on/off, and a proportional combination of the features of the boost-delta and flyback is obtained based on the inductance ratio. The possibility of cycle-by-cycle, interleaved boost-delta and boost-star connection, by triggering the appropriate switches, could be implemented. In this way a reduction of the harmonic content is possible, at the cost of power reduction throughput and slightly higher control complexity. The latter implementation is a variation of the basic scheme, and will not be further investigated here.

The high conduction losses and switching losses associated with the high number of semiconductors is a trade-off for the simple voltage follower control and low Total Harmonic Distortion (THD).
An analysis based on the method in [31] is presented for the Discontinuous Conduction Mode. The determination of circuit components ratings is then performed. The average current space vector is applied, in order to give a synthetic picture of the analytical results.

![Proposed 'deltafly' three-phase, three-switch Power Factor Correction circuit.](image)

Fig. 4.18 Proposed ‘deltafly’ three-phase, three-switch Power Factor Correction circuit.

### 4.2.2. Analysis of the Deltafly Three-Phase PFC Circuit

The analysis is carried out using the method in [31], where the switching frequency is considered much higher than the line frequency, and consequently the averaged current over a switching cycle is taken as an instantaneous value at the line frequency.

In order to analyze the circuit, it is sufficient to consider one sixth of the line period, e.g. the interval $(-\pi/6, \pi/6)$.

The inductance ratio is given in formula (4-1).

The proposed deltafly PFC stage has as particular cases the boost-delta circuit [40], when $T = \infty$, respectively flyback when $T = 0$.

The following formulas have been used in the analysis:

- the normalizing current:
\[ i_n = \frac{V_{LN}}{2L_1} T_{SW} \quad (4-18) \]

- the normalizing power:

\[ P_n = \frac{3V_{LN}^2}{2L_1} T_{SW} \quad (4-19) \]

where:

\[ T_{ON} = \text{switches on time}, \]

\[ T_{SW} = \text{switching period}. \]

The parameters which give a qualitative description on the performance of the circuit are defined as follows:

- the current ratio \( \hat{i}_1 \): \( L_1 \) global peak/peak of the phase fundamental:

\[ \frac{\sqrt{3}V_{LN} T_{ON}}{L_1} \frac{2L_1}{V_{LN} T_{SW} i_{1N}} = \frac{2\sqrt{3}T_{ON}}{T_{SW} i_{1N}} \quad (4-20) \]

- the current ratio \( \hat{i}_2 \): \( L_2 \) global peak/peak of the phase fundamental:

\[ \frac{\sqrt{3}V_{LN} T_{ON}}{L_2} \frac{2L_2}{V_{LN} T_{SW} i_{2N}} = \frac{2\sqrt{3}T_{ON}}{T_{SW} i_{2N}} \quad (4-21) \]

- the active power:

\[ P = \frac{3V_{LN}^2}{2L_1} T_{SW} i_{1N} \cos \phi_i \quad (4-22) \]

- the ratio inductors energy/transmitted energy:

\[ \frac{\max \left( \frac{L_1 i_1^2}{2} \right) + \max \left( \frac{L_2 i_2^2}{2} \right)}{P_n T_{SW}} = \frac{T_{ON}^2}{T_{SW} i_{1N} \cos \phi_i \left( 1 + \frac{L_1}{L_2} \right)} \quad (4-23) \]

where:

\[ i_1 = \text{instantaneous current through inductor } L_1, \]

\[ i_2 = \text{instantaneous current through inductor } L_2, \]

\[ i_{1N} = \text{peak of the fundamental of the average phase current}, \]
The equivalent circuits during the switches on-time and off-time are shown in Figs. 4.19 and 4.3. The equations resulting from the analysis of the circuit are based on Appendix C for the boost-delta stage and Appendix D for the flyback stage. The current waveforms during a switching duty cycle are presented in Figs. 4.20-4.22 for the line, inductor $L_1$ and $L_2$ currents. Based on those results, the plots defining the performance of the circuit are given below. In Fig. 4.23 the shape of the line currents shows clearly how the inductance ratio makes the circuit look more like a flyback ($T$ close to zero) or boost-delta ($T$ large). The same idea is reflected by the plots in Figs. 4.24 and 4.25 where the relative value of the 5th and 7th harmonics are given vs. the voltage transfer ratio $M$. While the boost-delta presents a current leading/lagging phase-angle, the proposed circuit makes possible a reduction of this angle, as shown in Fig. 4.26.

4.2.3. Design related issues

The voltage, current and power rating utilization factor of the components will be given. The component ratings are determined theoretically and they are matched by the results of the time-domain simulation using PSIM.

By inspection of the circuit the following component ratings can be determined:

- peak voltage across the diodes:

$$\max(V_{d1}) = \max(V_{d7}) = V_D$$ (4-24)

- peak voltage across the switches:

$$\max(V_{sw1}) = V_{ln} + \frac{2V_D}{3}, \max(V_{sw4}) = V_D, \max(V_{sw-3-IGBT}) = V_{ln} + \frac{2V_D}{3}$$ (4-25)

- peak current through the diodes:

$$\max(i_{ln}) = \frac{\sqrt{3}V_{ln}T_{ON}}{L_1}, \max(i_{d7}) = \frac{3V_{ln}T_{ON}}{L_2}$$ (4-26)

- peak current through the switches:
max\(i_{SW_1}\) = \(\max\left(\frac{V_a - V_b}{L_1} T_{ON} - \frac{3V_B}{L_2} T_{ON} \right)\), \(\max(i_{SW_4}) = \frac{3V_L}{L_2} T_{ON}\)

max\(i_{SW-3-IGBT}\) = \(\max\left(\frac{V_a - V_b}{L_1} T_{ON} - \frac{3V_B}{L_2} T_{ON} \right)\), \(\max(i_{SW-3-IGBT_2}) = \frac{\sqrt{3}V_L}{L_1} T_{ON}\)

max\(i_{SW-3-IGBT_3}\) = \(\frac{3V_L}{L_2} T_{ON}\)

- peak inductor \(L_1\) current:

\[\max(i_{i_1}) = \frac{\sqrt{3}V_L T_{ON}}{L_1}\]

- peak inductor \(L_2\) current:

\[\max(i_{i_2}) = \frac{\sqrt{3}V_L T_{ON}}{L_2}\]

A comparison will be drawn with the boost-delta and flyback circuits. A practical example is simulated with the values given below:

\(V_{\sin} = 400V / 50Hz\), \(V_D = 800V\), \(R = 59\Omega\), \(C = 4.700\mu F\), \(P_{on} = 10,850W\), \(L_1 = 135\mu H\), \(L_2 = 135\mu H\), \(T_{SW} = 40\mu s\), \(T_{ON} = 8.14\mu s\), \(T_{swp} = 0.2\mu s\), \(T_{total} = 0.04s\).

The time-domain plots are shown to match the analytical results. In Fig. 4.27 the average line current is given for an inductance ratio \(T=1\). The inductors and semiconductors averaged currents are presented in Figs. 4.28 and 4.29.

### 4.2.4. Average current space vector analysis

The space vector method presented in Section 2.1 is applied to the expressions given in Appendix E. As a result the following expression is obtained for the line current:

\[i_{AV} = \frac{V_m}{L_1} e^{j(\omega_t \pi / 2)} \left[ \frac{3T_{ON}^2}{2T_{SW}} \left(1 + \frac{L_1}{L_2}\right) + \frac{t_1(t_1 + t_2)}{2T_{SW}} \right] + \frac{V_m}{L_1} e^{j(\omega_t \pi / 3)} \sqrt{3}T_{ON} \left(2t_1 + t_2\right) + \frac{2V_D}{3L} e^{j2\pi / 3} t_1(t_1 + t_2) / 2T_{SW}\]  

(4-31)
Fig. 4.19 Equivalent circuit diagram of the proposed circuit when all switches are closed.

Fig. 4.20 Line currents during a switching cycle.

Fig. 4.21 Inductor $L_1$ currents during a switching cycle.

Fig. 4.22 Inductor $L_2$ currents during a switching cycle.
Fig. 4.23 Line current vs. time, for various voltage transfer ratios, M and inductance ratios.

Fig. 4.24 5th harmonic (%) vs. voltage transfer ratio M, for various inductance ratios.

Fig. 4.25 7th harmonic (%) vs. voltage transfer ratio M, for various inductance ratios.

Fig. 4.26 Current leading angle vs. voltage transfer ratio, M for various inductance ratios.

Fig. 4.27 Average line current vs. time.

Fig. 4.28 Average inductor currents vs. time.

Fig. 4.29 Average semiconductor currents vs. time.
As it can be seen by analyzing (4-31) and its visual representation in Fig. 4.30, over the studied interval 
$[-\pi/6, \pi/6]$, the resultant vector is always leading the voltage vector. This result is simply confirming the plots in Fig. 4.23. The formula proves that the relative size of the vector $e^{j2\pi/3}$ becomes smaller with a higher voltage transfer ratio and consequently the resultant vector is more ‘aligned’ with the voltage vector, i.e. the harmonics will be smaller. The smaller the ratio $T$, i.e. features more closer to a flyback, the greater the weight of the $e^{j(\alpha-\pi/2)}$ current component, in phase with the voltage space vector.

The resultant vector is the sum of a fundamental and harmonics vectors. The simplest way to determine their amplitude and phase is in an analytical rather than graphical way, based on the formulas in Appendix C and D.

In order to align the resultant current space vector to the $e^{j(\alpha-\pi/2)}$ component, and consequently improve the harmonic content, schemes could be used where the switches SW4-SW6 and SW1-SW6 are cycle-by-cycle triggered. In that case the circuits behavior would have mixed features of a boost-star and Deltafly. For such an implementation the average current space vector technique proves to be an indispensable tool.

Fig. 4.30 Space vector representation of the averaged phase current for the boost-delta circuit.

a) $\alpha = -\pi/6$, b) $\alpha = 0$, c) $\alpha = \pi/6$. 

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4.3. ‘STAR-DELTA’ Circuit

4.3.1. Introduction

A new three-phase three-switch Power Factor Correction (PFC) circuit operating in Discontinuous Conduction Mode (DCM), shown in Fig. 4.31, is proposed. The switches are bi-directional, operate simultaneously on/off, and could be implemented as in Section 3.1.4. The circuit consists of two stages, a boost-star and a boost-delta, where the boost-star is directly in series with the input line. A proportional combination of the features of the two stages is possible by changing the inductance ratio of the two sets of inductors.

![Fig. 4.31 ‘Star-delta’ three-phase, three-switch Power Factor Correction circuit.]

4.3.2. Analysis of the Star-Delta Three-Phase PFC Circuit

An original method of analysis is proposed for describing the performance parameters of the circuit. At the moment when the switches turn off, six diodes are initially conducting. The sequence in which the diodes come out of conduction is important for determining the shape of the currents in the inductors, as exemplified in Fig. 4.32. The equations are written for the current in the inductors and the six nodes corresponding to the two bridge rectifiers.
A detailed analysis is carried out in Appendix E. The same parameters are used as for the ‘Starfly’ circuit. The results are synthetically presented in the following. In Figs. 4.33 and 4.34, the shape of the line currents and maximum duty cycle show clearly how the inductance ratio makes the circuit look more like a boost-star ($L_2/L_1$ close to zero) or boost-delta ($L_2/L_1$ large). Both boost-star and boost-delta circuits have, at the same voltage transfer ratio, approximately equal harmonic content and Total Harmonic Distortion as seen in Fig. 4.35. While the boost-delta presents a current leading phase-angle, the proposed circuit makes possible a reduction of this angle to the desired value, as shown in Fig. 4.36. In Fig. 4.37 the ratio of the conduction losses in the two sets of diodes can be seen for various voltage transfer ratios $M$.

Fig. 4.32 Time-domain simulation showing the currents for the inductor sets $L_1$ and $L_2$ during a switching cycle.
Fig. 4.33 Line current vs. time, for various voltage transfer ratios, M and inductance ratios.

Fig. 4.34 Maximum duty cycle vs. voltage transfer ratio, M for various inductance ratios.

Fig. 4.35 Total Harmonic Distortion vs. voltage transfer ratio M, for various inductance ratios.

Fig. 4.36 Current leading angle vs. voltage transfer ratio, M for various inductance ratios.

Fig. 4.37 Diode set 1/(Diode set 1 + Diode set 2) average current vs. inductance ratio for various voltage transfer ratios, M.
4.3.3. Design related issues

The component ratings are determined theoretically and they are matched by the results of the time-domain simulation using PSIM.

By inspection of the circuit the following component ratings can be determined:

- peak voltage across the diodes:
  \[ \text{max}(V_{D1}) = \text{max}(V_{D2}) = V_D \]  
  \[ \text{(4-32)} \]

- peak voltage across the switches:
  \[ \text{max}(V_{SW}) = V_D \]  
  \[ \text{(4-33)} \]

- peak current through the diodes:
  \[ \text{max}(i_{D1}) = \text{max}(i_{D2}) = \frac{\sqrt{3} Y_{LN} T_{ON}}{3 L_1 + L_2} \]  
  \[ \text{(4-34)} \]

- peak current through the switches:
  \[ \text{max}(i_{SW}) = \frac{\sqrt{3} Y_{LN} T_{ON}}{3 L_1 + L_2} \]  
  \[ \text{(4-35)} \]

- peak inductor \( L_1 \) current:
  \[ \text{max}(I_{L1}) = \frac{3 Y_{LN} T_{ON}}{3 L_1 + L_2} \]  
  \[ \text{(4-36)} \]

- peak inductor \( L_2 \) current:
\[
\max(i_s) = \frac{\sqrt{3}V_{in}T_{sw}}{3L_1 + L_2}
\]

A comparison will be drawn in Section 7.1 with the other PFC circuits proposed. A practical example is simulated with the values given below:

\[V_{\text{in}} = 400V \, / \, 50\, \text{Hz} \, , \, V_D = 800V \, , \, R = 59\, \Omega \, , \, C_{\text{out}} = 500\, \mu\text{F} \, , \, P_{\text{out}} = 10,850W \, , \, L_1 = 25.5\, \mu\text{H} \, , \]

\[L_2 = 76.5\, \mu\text{H} \, , \, f_{\text{sw}} = 25kHz \, , \, D = 0.2445 \, , \, T_{\text{on}} = 0.3\, \mu\text{s} \, , \, T_{\text{off}} = 0.03s \, .\]

The time-domain plots are shown to match the analytical results. The inductors and semiconductors averaged currents are presented in Figs. 4.38 and 4.39.
4.4. ‘Delta-Delta’ Circuit

4.4.1. Introduction

A new three-phase Power Factor Correction (PFC) circuit operating in Discontinuous Conduction Mode (DCM), shown in Fig. 4.40, is proposed. The two sets of inductors are delta-connected across the line during the on-time. After turning off the switches, the inductors are series connected, similarly with the circuit in Section 4.3. The circuit belongs to the family of two-stage PFC circuits presented in this chapter. The inductance and rectifying capability needed for boosting are split, which allows smaller individual size and better cooling. A higher number of semiconductors is the trade-off for a simple voltage follower control and very low THD, even at voltage transfer ratios of 1.3-1.5. The implementation is in applications which need to meet the IEC 1000-3-2 requirements in the upper half of the power range, i.e. 5-11 kW.

![Diagram of Delta-Delta three-phase, three-switch Power Factor Correction circuit](image)

Fig. 4.40 Proposed delta-delta three-phase, three-switch Power Factor Correction circuit.

4.4.2. Analysis of the proposed circuit

The following analysis refers to the boost-delta operating with a leading current. The situation where the current is lagging, which occurs for a reversed phase sequence, can be studied in a similar way.
The analysis is carried out using the method in Section 4.3. The assumption is made that the switching frequency is much higher than the line frequency, and consequently the averaged current over a switching cycle is taken as an instantaneous value at the line frequency. During off-time there are initially six diodes conducting. They come consecutively out of conduction pending on the node currents at the legs of the three-phase rectifiers. The phase angle, voltage transfer ratio and inductance ratio are factors which will influence the switching period and the averaged phase and inductor currents. A chart of all the possible combinations has been devised and MATLAB has been used for solving the system.

The normalizing current used in the analysis is:

\[ i_N = \frac{V_{LN}}{2L_1} T_{sw} \]  \hspace{1cm} (4-38)

where;

\[ T_{sw} = \text{switching period}. \]

The analysis is carried out in Appendix F and some of the results are given in the following. The plots in Figs. 4.41-4.43 show the variation of the 5th, 7th harmonics (percent of the fundamental) and current fundamental leading angle vs. the inductance ratio, T for various M. The same plots are then presented vs. voltage transfer ratio M, for various T, in Figs. 4.44-4.45.

4.4.3. Design related issues

The component ratings are determined theoretically and they are matched by the results of the time-domain simulation using PSIM.

By inspection of the circuit the following component ratings can be determined:

- peak voltage across the diodes:

\[ \max(V_{D1}) = \max(V_{D7}) = V_D \]  \hspace{1cm} (4-39)
- peak voltage across the switches:

\[ \max(V_{SW1}) = V_{LN} + \frac{2V_D}{3}, \quad \max(V_{SW4}) = V_D \]  \hspace{1cm} (4-40)

\[ \max(V_{SW3-IGBT}) = V_{LN} + \frac{2V_D}{3} \]  \hspace{1cm} (4-41)

- peak current through the diodes:

\[ \max(i_{Di}) = \max\left(\frac{V_A - V_B - V_C}{L_1} T_{ON}\right) T_{ON}, \quad \max(i_{D7}) = \frac{\sqrt{3} V_{LN} T_{ON}}{L_2} \]  \hspace{1cm} (4-42)

- peak current through the switches:

\[ \max(i_{SW1}) = \max\left(\frac{V_A - V_B - V_C}{L_1} T_{ON}\right) T_{ON}, \quad \max(i_{SW4}) = \frac{3V_{LN} T_{ON}}{L_2} \]  \hspace{1cm} (4-43)

\[ \max(i_{SW3-IGBT}) = \max\left(\frac{V_A - V_B - V_C}{L_1} T_{ON}\right) T_{ON}, \quad \max(i_{SW3-IGBT2}) = \max\left(\frac{V_A - V_B - V_C}{L_2} T_{ON}\right) \]  \hspace{1cm} (4-44)
\[
\text{max}(i_{\text{SW-3-IGBT}}) = \frac{\sqrt{3}V_{\text{IN}}}{L_2} T_{\text{ON}}
\]
- peak inductor \( L_1 \) current:
\[
\text{max}(i_{L_1}) = \frac{\sqrt{3}V_{\text{IN}}}{L_1} T_{\text{ON}}
\] (4-45)
- peak inductor \( L_2 \) current:
\[
\text{max}(i_{L_2}) = \frac{\sqrt{3}V_{\text{IN}}}{L_2} T_{\text{ON}}
\] (4-46)

A comparison will be drawn in Section 7.1 with the other PFC circuits proposed. A practical example is simulated with the values given below:

\[
V_{\text{sin}} = 400V / 50\text{Hz} , \quad V_D = 800V , \quad R = 62.5\Omega , \quad C = 500\mu F , \quad P_{\text{out}} = 10,240W , \quad L_1 = 162\mu H , \quad L_2 = 54\mu H ,
\]
\[
T_{\text{sw}} = 40\mu s , \quad T_{\text{on}} = 6.55\mu s , \quad T_{\text{up}} = 0.2\mu s , \quad T_{\text{wait}} = 0.03s .
\]

PSIM has been used for the plots in Figs. 4.47-4.49. In Fig. 4.47 the average line current is given for an inductance ratio \( T=0.33 \). The harmonic values as determined using PSIM correspond to those expected from Figs. 4.44 and 4.45. The improvement of the phase current harmonic content can also be easily seen by comparing Fig. 4.47 with Fig. 2.1 for an \( M=1.4 \). The inductors and semiconductors averaged currents are presented in Figs. 4.48 and 4.49.
4.5. N-level circuits

4.5.1. Harmonic reduction techniques for DCM operation

A generic drawing of the shape of the line current in a PFC circuit operating in DCM is given in Fig. 4.50. The waveform does not have continuity due to the possible change of the amplitude based on the configuration of the switches.

![Generic line current during a switching cycle.](image)

Fig. 4.50 Generic line current during a switching cycle.

An inspection of the waveform results in the conclusion that, when $T_{ON}$, $T_{SW}$ are constant, there are three sets of variables which could make the current more sinusoidal. By keeping two criteria constant and varying the third one, a direct influence on the harmonic content can be achieved, as shown below:

- for $i(T_{ON-}) = i(T_{ON+})$ and $L_1 = L_2$:

$$V_D >> V_{ph}$$

- for $i(T_{ON-}) = i(T_{ON+})$ and $V_D \approx V_{ph}$

$$L_1 >> L_2$$

- for $V_D \approx V_{ph}$ and $L_1 = L_2$

$$i(T_{ON-}) >> i(T_{ON+})$$

In the drawing $k$ is a sub-unitary coefficient.
$V_D >> V_{ph}$ is equivalent to $M >> 1$.

Another way of reducing the harmonics is when:

$$i(T_{ON-}) = i(T_{ON+}), \quad L_1 = L_2, \quad V_D \approx V_{ph},$$

and a variable $T_{ON}, T_{SW}$ are used, such as it was the case with the boost-star with AC-side switch.

### 4.5.2. Features of the N-level circuits

The PFC circuits studied in the present chapter have as a common characteristic the use of two boost stages connected in series during the ON-time and in series/parallel during the OFF-time. These circuits take advantage of the harmonic reduction criteria presented in Section 4.5.1. The building blocks for the development of these circuits are boost-star, boost-delta for the input, and flyback and boost-delta for the second stage, as shown in Figs. 4.51-4.54. One more variation is possible in the phase sequence for the boost-delta stages, as explained in Section 3.2. In the alternative of N-connected stages various combinations could be made with one input and (N-1) follow-up boosting stages.

Besides this type of connection, several networks of parallel running circuits could also be connected to the same DC output rail. An example can be given in the two boost-delta with reverse connection sequence, as presented in Section 3.2.5. Also the interconnection of several parallel and series networks can be made on the AC-side with the use of bi-, tri- or N-directional switches.

As a general rule little benefit is seen in connecting more than two stages. This is due to the added complexity, reduced improvement over two stages, and particularly difficult layout with largely sized inductors. In order that such circuits receive more interest, layouts must be developed where the ratio of inductor size and interconnection length is large.

Some of the problems specific to N-series connected circuits are underlined below:

- Interleaved switching pattern of the stages for a reduction of the EMI/filtering requirements is not possible; a parallel structure must be available for that purpose;

- switch's current is highest close to the supply and decreasing toward the DC side. The same trend is valid for the first set of line inductors depending on the number of switches series connected.
Fig. 4.51 Boost-star input stage.

Fig. 4.52 Boost-delta input stage.

Fig. 4.53 Flyback stage.

Fig. 4.54 Boost-delta stage.
CHAPTER 5
SEPIC-DERIVED CIRCUITS

The location of the switches on the AC-side, allows the development of SEPIC (Single-Ended-Primary-Inductor-Circuit) networks across the three phases. Due to the star-delta nature of three-phase, two new circuit topologies become possible: the star-SEPIC and delta-SEPIC. It is shown that the general properties of the SEPIC are carried over, while the power distribution across three sets of components allows a more manageable size.
5.1. Star-SEPIC

5.1.1. Introduction

The present chapter extends the SEPIC topology, first developed in [41] to a three-phase three-switches power factor correction (PFC) stage operating in DCM. Unlike previous work [42,43] where the SEPIC topology is placed on the DC side, in the proposed circuit it is placed on the AC side, i.e. before the rectifying bridge. The circuit consists of three bi-directional switches and three SEPIC characteristic L-C networks as shown in Fig. 5.1.

For DCM operation a possible implementation of the three bidirectional switches is by using three IGBTs with antiparallel diodes, star-connected with a common emitter. This way the gating signals for all the controllable switches of the circuit have a common reference.

It is known that in the case of the SEPIC converter the DCM can occur with inductor current reaching zero every switching period or following a base line at the supply frequency. In the present work the mode in which the current of the inductors always reaches zero is studied. As documented in [44] in this case the energy stored in the inductors is the smallest.

The results reported here are the outcome of an analytical investigation of the circuit’s steady state behavior. The theoretical analysis has its roots in the previous work developed for single-phase PFC [45-48] and the averaging method proposed in [31]. The normalized current waveforms, harmonics, THD and design optimization criteria are determined. Time domain simulations which confirm the analytical results are shown.

Several disadvantages present in the popular DCM boost topology, like:

- difficult implementation of input-output isolation;
- difficult to control overload and start-up overcurrents;
- need of a high voltage transfer ratio or duty cycle modulation for the reduction of the 5th and 7th harmonics;

can be easily eliminated due to the intrinsic properties of the SEPIC converter. In addition, for the same power level the inductor volume for the SEPIC and boost DCM PFC stages stays approximately the same with the advantage of having split inductors in the first case.
Fig. 5.1 Proposed SEPIC 3-phase 3-switch power factor correction circuit.

On the other hand some disadvantages characteristic to the SEPIC converter, are also present:

- high switch voltage and current stress;
- additional capacitors needed.

The general features characteristic to all PFC converters working in DCM such as simple voltage follower control and bigger EMI filters are applicable in this case as well.

5.1.2. Circuit Analysis

The proposed circuit is analyzed in respect to its DCM operation, where only two switching states are possible: 000 or 111.

The following parameters, specific to this circuit’s analysis, are defined:

- the normalized phase and inductor $L_1$ current:

$$i_{AN} = \frac{i_A}{i_{N_{L1}}} ,$$

(5-1)

where: $i_A = \text{phase current}$, $i_{N_{L1}} = \frac{V_{LN}T_{SW}}{2L_1} = \text{normalizing } L_1 \text{ current};$

- the normalized inductor $L_2$ current:
\[ i_{L_2} = \frac{i_1}{i_{L_2}} \]  

(5-2)

where: \( i_1 \) = inductor \( L_2 \) current, \( i_{L_2} = \frac{V_{LN} T_{SW}}{2L_2} \) = normalizing \( L_2 \) current;

- the normalized capacitor \( C \) current:

\[ i_{C1N} = \frac{i_{C1}}{i_{C2}} \]  

(5-3)

where: \( i_{C1} \) = capacitor \( C \) current, \( i_{C2} = V_{LN} T_{SW} \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \) = normalizing \( C \) current;

- the inductors ratio:

\[ a = \frac{L_2}{3L_1} \]  

(5-4)

In order to analyze the new PFC circuit, it is sufficient to consider one twelfth of the line period, e.g. \((0, \pi / 6)\) interval, due to symmetry.

For the time interval \((0, T_{ON})\) all the switches are closed (111) and the equivalent circuit looks like in Fig. 5.2. During the off time of the switches (000), the current flow is dependent on the instantaneous values of the currents (proportional to the instantaneous voltages). There are two time intervals: \((T_{ON}, t_1)\) when current flows in three diodes and \((t_1, t_2)\) when current flows in two diodes, as shown in Fig. 5.3 and 5.4.

The shape of the currents in the inductors, capacitors, diodes and switches during a switching cycle is presented in Fig. 5.5-5.9, where absolute values are given for the times \( T_{ON} \), \( t_1 \) and \( t_2 \).

The total time in which current flows through the \( L_1 \) inductors can be determined as:

\[ t_{SW} = T_{ON} + t_1 + t_2 = T_{ON} \left( 1 + \frac{3V_A}{V_D} + \frac{2(V_C - V_A)}{V_D} \right) = T_{ON} \frac{V_D + (V_C - V_B)}{V_D} \]  

(5-5)

For fixed frequency operation the switching period and duty-cycle are determined as:

\[ T_{SW} = \max(t_{SW}) = T_{ON} \frac{V_D + \sqrt{3V_{LN}}}{V_D} = T_{ON} \frac{M + 1}{M} \]  

(5-6)

\[ D = \frac{T_{ON}}{T_{SW}} = \frac{V_D}{V_D + \sqrt{3V_{LN}}} = \frac{M}{M + 1} \]
Fig. 5.2 Proposed circuit. Switches closed (111).

Fig. 5.3 Proposed circuit. Switches opened (000). Current flowing in three diodes.

Fig. 5.4 Proposed circuit. Switches opened (000). Current flowing in two diodes.

Fig. 5.5 Inductor $L_1$ current waveforms during a switching period.

Fig. 5.6 Inductor $L_2$ current waveforms during a switching period.

Fig. 5.7 Rectifying diodes current waveforms during a switching period.
5.1.3. Analytical Determination of Circuit Parameters

For the rating of the rectifying diodes, switches and capacitors the maximum voltage will be determined:

- rectifying diodes:
  \[ V_{D_{\text{MAX}}} = V_D \]  \hspace{1cm} (5-7)

- switches maximum voltage:
  \[ V_{SW_{\text{MAX}}} = V_D + \max(V_B - V_C) = V_D + \sqrt{3}V_{L_{N}} = V_D \frac{M+1}{M} \]  \hspace{1cm} (5-8)

- capacitor maximum voltage:
  \[ V_{C_{\text{MAX}}} = V_{L_{N}} + V_{\text{ripple}} \]  \hspace{1cm} (5-9)

In Section 2.2, a method has been introduced for the analytical determination of the average and rms currents, both at line and switching frequency.
By applying the formulas (2-19, 2-20, 2-23) to the current shapes given in Fig. 5.5, the closed form expressions for the inductor $L_1$ rms currents are determined for each phase as follows:

$$i_{A_{rms}} = \frac{T_{ON}}{L_1} \sqrt{ \frac{T_{ON}}{3 T_{SW}} \left( V_s^2 + \frac{3V_s}{V_o} V_s^2 \right) } ;$$

$$i_{B_{rms}} = \frac{T_{ON}}{L_1} \sqrt{ \frac{T_{ON}}{3 T_{SW}} \left( V_s^2 + \frac{3V_s}{V_o} \left(V_s + V_o (V_s - V_o) + (V_s - V_o)^2 \right) \right) } \frac{2(V_c - V_o)^2}{V_o} ;$$

$$i_{C_{rms}} = \frac{T_{ON}}{L_1} \sqrt{ \frac{T_{ON}}{3 T_{SW}} \left( V_s^2 + \frac{3V_s}{V_o} \left(V_s + V_o (V_s - V_o) + (V_s - V_o)^2 \right) \right) } \frac{2(V_c - V_o)^2}{V_o} .$$

The average current space vector method, developed in Section 2.1.3. can also be applied to the input phase currents. Using formulas (2-7, 2-8) and Fig. 5.5 the space vector and its components are determined as:

$$i(T_{ON}) = \frac{V_m}{L_1} T_{ON} e^{j(\omega t - \pi/2)}$$

$$i(t_1) = \frac{V_c - V_o}{L_1} T_{ON} e^{-j\pi/2}$$

$$i_A' = \frac{V_m}{L_1} \left( T_{ON} + t_1 \right) e^{j(\omega t - \pi/2)} + \frac{2\sqrt{3}}{3} \frac{V_c - V_o}{L_1} T_{ON} \left( t_1 + t_2 \right) e^{-j\pi/2}$$

Since in the case of the SEPIC converter no modulation is needed, due to the intrinsic low harmonic content, the average current space vector will not be further used.

Using the general formulas (2-24, 2-25, 2-28), plots have been drawn for the normalized rms and average inductor $L_1$ currents in Fig. 5.10 and 5.11 and the rms normalized inductor $L_2$ and capacitor $C_1$ currents, in Fig. 5.12 respectively 5.13.

By studying Fig. 5.14 it can be seen an important advantage of the SEPIC converter, that good 5th, 7th harmonics and THD can be achieved even at low voltage transfer ratios $M$. In Fig. 5.15 the contribution of the high frequency rms component to the total rms for inductor $L_1$ is shown to be dependent on $M$. 

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Fig. 5.10 Normalized average phase current vs. phase angle during a line period.

Fig. 5.11 Normalized inductor $L_1$ rms current vs. phase angle during a line period.

Fig. 5.12 Normalized inductor $L_2$ rms current vs. phase angle during a line period.

Fig. 5.13 Normalized capacitor $C_1$ rms current vs. phase angle during a line period.

Fig. 5.14 Normalized 5th, 7th harmonics and THD (%) of the average inductor $L_1$ current vs. voltage transfer ratio $M$.

Fig. 5.15 Ratio (%) of the high frequency/total inductor $L_1$ rms current vs. voltage transfer ratio $M$. 

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5.1.4. Design Notes and Time Domain Simulations

As it has been shown in [48] the SEPIC converter used as a single-phase power factor correction stage has
to meet a certain condition for the inductors ratio $L_1/L_2$ so that the base line of the current in $L_1$ will
have the same sign with the phase voltage during the whole period.

For three-phase the same condition will be determined in the following. The energy drawn by the circuit
during one switching period is:

$$
E = L_1 \left( I_{Ax}^2 - I_{Ay}^2 \right) + L_2 \left( I_{Bx}^2 - I_{By}^2 \right) + L_1 \left( I_{Cx}^2 - I_{Cy}^2 \right) + L_2 \left( I_{Dx}^2 - I_{Dy}^2 \right) + L_2 \left( I_{Ex}^2 - I_{Ey}^2 \right) + L_2 \left( I_{Fx}^2 - I_{Fy}^2 \right) = 
$$

$$
= \frac{3V_{LN}^2}{4} T_{ON} \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \tag{5-12}
$$

where:

$I_{Ax}, I_{Ay}, I_{Cn} =$ currents in the $L_1$ inductors at the beginning of the switching period;

$I_{Bx}, I_{By}, I_{Cn} =$ currents in the $L_2$ inductors at the beginning of the switching period;

$I_{Axk}, I_{Byk}, I_{Cpk} =$ currents in the $L_1$ inductors at $T_{ON}$;

$I_{Axk}, I_{Byk}, I_{Cpk} =$ currents in the $L_2$ inductors at $T_{ON}$.

At the same time the energy can be written as:

$$
E = (V_A I_{Ax} + V_B I_{By} + V_C I_{Cy} ) T_{SW} \tag{5-13}
$$

Making the two expressions (17) and (18) equal and taking into consideration:

$$
V_A I_{Ax} + V_B I_{By} + V_C I_{Cy} \geq 0 \tag{5-14}
$$

we obtain:

$$
\frac{L_1}{L_2} \geq \frac{3V_A^2 + 2V_B V_D^2 - 4V_B V_C^2 - V_C V_A^2}{2V_B V_{LN}^2} \tag{5-15}
$$

Since the above inequality should hold for any angle in the interval $(0, \pi/6)$ we obtain:

$$
\frac{L_1}{L_2} \geq \frac{1}{3M} \tag{5-16}
$$
In terms of the load, the boundary condition for having discontinuous conduction mode is based on the method in [48] and results in the following:

\[ R \geq \frac{V_D}{I_{sw}} = \frac{V_D^2}{2V_c^2 + 2V_c^2 + 2V_A^2} \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \frac{2T_{sw}}{T_{on}} \]  

\( (5-17) \)

The discontinuous conduction mode is guaranteed for the whole period when:

\[ \frac{1}{\left( \frac{1}{L_1} + \frac{3}{L_2} \right) RT_{sw}} \leq \frac{1}{4(M + 1)^2} \]  

\( (5-18) \)

The capacitor voltage has two constraints: to have a nearly constant value during a switching period and to follow the input voltage in a line period. Its value has a great influence on the input current waveform. The resonant frequency of \( C_1, L_1 \) and \( L_2 \) must be much greater than the line frequency, to avoid input current oscillations each half-cycle. Besides, if the resonant frequency is near the switching frequency, the characteristic of good power factor is lost and distorted waveforms are generated. As a general rule, based on the recommendation in [48], we can use:

\[ \omega_{sw}^2 >> \frac{1}{C_1 \left( \frac{L_1 + L_2}{3} \right)} >> \omega_{line}^2 \]  

\( (5-19) \)

The energy transfer between the inductor and capacitor networks during each switching cycle must keep the capacitor voltage ripple within reasonable limits.

Therefore, the following design rules can be derived, based on energy considerations:

\[ C_1 > \frac{3}{L_2} T_{on}^2 \quad \text{and} \quad C_1 > \frac{1}{L_1} T_{on}^2 \]  

\( (5-20) \)

As an example a 3-phase 3-switches PFC stage was designed and simulated using PSIM. The following values have been chosen:

\[ V_{line} = 208V, \quad f_{line} = 60Hz, \quad L_1 = 90\mu H, \quad L_2 = 540\mu H, \quad C_1 = 9.4\mu F, \quad C_{out} = 4.700\mu F, \]

\[ R = 58.5\Omega, \quad V_{out} = 600V, \quad f_{sw} = 25KHz, \quad D = 0.64, \quad T_{step} = 1\mu sec., \quad T_{off} = 0.3sec., \quad P_{out} = 6.15KW. \]

The phase current at the input of the high frequency filter and the capacitor \( C_1 \) voltage are given in Fig. 5.16 and 5.17.
5.1.5. Conclusions

A new 3-phase 3-switch Power Factor Correction circuit based on three SEPIC networks has been analyzed relative to its DCM operation. When output isolation is required as well as over-current and start-up protection the proposed SEPIC converter is a good solution. Some other advantages are: operation at constant frequency and duty cycle even at low voltage transfer ratios, no need of current loop, soft turn-on of the switches, split inductor volume.

The main disadvantages are: switch voltage and current stresses, bigger EMI. Other disadvantages present are: capacitors required, high rms current in the inductors and capacitors. Nonetheless a good design and implementation can overcome these problems.

An extension of the method for the calculation of the instantaneous average current is proposed for the instantaneous rms current. As a consequence the content of high frequency harmonics can be determined. This helps in the design of the components and can be applied to all PFC circuits operating in DCM.
5.2. Delta-SEPIC

5.2.1. Introduction

This circuit represents a variation on the SEPIC presented in Section 5.1. The first set of inductors is connected this time in delta, rather than in star, during the switches' on-time. This changes the large signal transfer function of the circuit. Another difference is that a small phase shift between the phase voltage and current will occur. The mode in which the current of the inductors always reaches zero is studied. As documented in [44], in this case, the energy stored in the inductors is the smallest.

![Fig. 5.18 Proposed Delta-SEPIC 3-phase 3-switch power factor correction circuit.](image)

The work reported here is the result of an analytical investigation of the steady state behavior of the circuit, and is pursued with the same techniques as for the Star-SEPIC PFC. The normalized current waveforms, harmonics, THD and design optimization criteria are determined. Time domain simulations which confirm the analytical results are shown.

The general advantages and disadvantages characteristic to SEPIC converters have been shown in section 5.1.1. and are applicable to this circuit as well.
5.2.2. Circuit Analysis

The proposed circuit is analyzed in respect to its DCM operation, where only two switching states are possible: 000 or 111.

The following parameters, specific to this circuit’s analysis, are defined:

- the normalized phase current:

\[ i_{AN} = \frac{i_A}{i_{N,\text{ph}}} \]  \hfill (5-21)

where \( i_A \) = phase current, \( i_{N,\text{ph}} = V_{LN} T_{SW} \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \) = normalizing phase current;

- the normalized inductor \( L_1 \) current:

\[ i_{L1} = \frac{i_L}{i_{N,L1}} \]  \hfill (5-22)

where: \( i_L \) = inductor \( L_1 \) current, \( i_{N,L1} = V_{LN} T_{SW} \frac{1}{2L_1} \) = normalizing \( L_1 \) current;

- the normalized inductor \( L_2 \) current:

\[ i_{L2} = \frac{i_L}{i_{N,L2}} \]  \hfill (5-23)

where: \( i_L \) = inductor \( L_2 \) current, \( i_{N,L2} = V_{LN} T_{SW} \frac{1}{2L_2} \) = normalizing \( L_2 \) current;

- the normalized capacitor \( C_1 \) current:

\[ i_{CN} = \frac{i_C}{i_{N,C1}} \]  \hfill (5-24)

where: \( i_C \) = capacitor \( C_1 \) current, \( i_{N,C1} = V_{LN} T_{SW} \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \) = normalizing \( C_1 \) current;

- the inductors ratio:

\[ a = \frac{L_2}{\sqrt{3} L_1} \]  \hfill (5-25)

The following assumption is made:
where: \( f_{SW} = \) switching frequency, \( f_{LINE} = \) line frequency.

This makes it possible to consider the average, rms, and high frequency components of the current over a switching cycle as ‘instantaneous’ values seen at the line frequency. In the following, where plots or formulas refer to line frequency, the ‘instantaneous’ values are used.

In order to analyze the new PFC circuit, it is sufficient to consider one twelfth of the line period, e.g., \( (\pi/6, \pi/3) \) interval, due to symmetry, as shown below:

\[
i_A(\omega t) = i_A(\pi - \omega t) = -i_A(\pi + \omega t) = -i_A(2\pi - \omega t)
\]

\[
i_A(\omega t) = i_C(\pi/3 - \omega t) \quad \text{for } 0 < \omega t < \pi/3;
\]

\[
i_A(\omega t) = -i_B(2\pi/3 - \omega t) \quad \text{for } \pi/3 < \omega t < \pi/2.
\]

For the time interval \( (0, T_{ON}) \) all the switches are closed (111) and the equivalent circuit looks like in Fig. 5.19. During the off time of the switches (000), the current flow is dependent on the instantaneous values of the currents (proportional to the instantaneous voltages). There are two time intervals: \( (T_{ON}, t_1) \) when current flows in three diodes and \( (t_1, t_2) \) when current flows in two diodes, as shown in Fig. 5.20 and 5.21.

The shape of the currents in the line, inductors, capacitors, diodes, and switches during a switching cycle is presented in Figs. 5.22-5.27.

The total time in which current flows through the \( L_i \) inductors can be determined as:

\[
t_{SW} = T_{ON} + t_1 + t_2 = T_{ON} \left( 1 + \frac{3(V_A - V_C)}{V_D} + \frac{6V_C}{V_D} \right) = T_{ON} \frac{V_D - 3V_B}{V_D}
\]

For fixed frequency operation, the switching period and duty-cycle are determined as:

\[
T_{SW} = \text{max}(t_{SW}) = T_{ON} \frac{V_D + 3V_{LN}}{V_D} = T_{ON} \frac{M + \sqrt{3}}{M}
\]

\[
D = \frac{T_{ON}}{T_{SW}} = \frac{V_D}{V_D + 3V_{LN}} = \frac{M}{M + \sqrt{3}}
\]
Fig. 5.19 Proposed circuit. Switches closed (111).

Fig. 5.20 Proposed circuit. Switches opened (000). Current flowing in three rectifier diodes.

Fig. 5.21 Proposed circuit. Switches opened (000). Current flowing in two rectifier diodes.

Fig. 5.22 Inductor $L_1$ current waveforms during a switching period.

Fig. 5.23 Inductor $L_2$ current waveforms during a switching period.

Fig. 5.24 Capacitor $C_1$ current waveforms during a switching period.
5.2.3. Analytical Determination of Circuit Parameters

For the rating of the rectifying diodes, switches, and capacitors, the maximum voltage will be determined:

- rectifying diodes maximum voltage:

\[ V_{\text{d,MAX}} = V_D \]  \hspace{1cm} (5-30)

- switches maximum voltage:

\[ V_{\text{SW,MAX}} = \frac{2V_D}{3} + \max(V_B - V_C) = \frac{2V_D}{3} + \sqrt[3]{3}V_{\text{LN}} = V_D \frac{2M + 3}{3M} \]  \hspace{1cm} (5-31)

- capacitor maximum voltage:

\[ V_{\text{C,MAX}} = V_{\text{LN}} + V_{\text{ripple}} \]  \hspace{1cm} (5-32)

The result of the application of formula (2-20) is given below for the interval \((\pi / 6, \pi / 3)\). Based on the current shapes in Fig. 5.22 and 5.27 the closed form expressions are calculated in (5-33, 5-34).
Phase ‘instantaneous’ average currents:

\[ i_{A_{av}} = \frac{T_{ON}^2}{2T_{SW}} \left[ \frac{1}{L_1} \left( 3V_A + \frac{3(V_A - V_B)}{V_D} (V_A - V_C) + \frac{3(V_A - V_B)}{L_2} \right) \right] \]  

(5-33)

\[ i_{B_{av}} = \frac{T_{ON}^2}{2T_{SW}} \left[ \frac{1}{L_1} \left( 3V_B + \frac{3(V_A - V_C)}{V_D} (V_B - V_A - 3V_C) - \frac{6V_C}{V_D} 3V_C \right) + \frac{3(V_B - V_C)}{L_2} \right] \]

\[ i_{C_{av}} = \frac{T_{ON}^2}{2T_{SW}} \left[ \frac{1}{L_1} \left( 3V_C + \frac{3(V_A - V_C)}{V_D} (V_C - V_B + 3V_C) + \frac{6V_C}{V_D} 3V_C \right) + \frac{3(V_C - V_A)}{L_2} \right] \]

Inductor \( L_1 \) ‘instantaneous’ rms currents:

\[ i_{A_{rms}} = \frac{T_{ON}}{L_1} \sqrt{\frac{T_{ON}}{3T_{SW}}} \left( \frac{V_A - V_C}{V_D} \right)^2 + \frac{3(V_A - V_C)}{V_D} (V_A - V_C)^2 \]

\[ i_{B_{rms}} = \frac{T_{ON}}{L_1} \sqrt{\frac{T_{ON}}{3T_{SW}}} \left( \frac{V_B - V_A}{V_D} \right)^2 + \frac{3(V_A - V_C)}{V_D} (V_B - V_A)^2 + \frac{(-3V_C)(V_B - V_A) + (3V_C)^2}{V_D} + \frac{6V_C}{V_D} (3V_C)^2 \]

\[ i_{C_{rms}} = \frac{T_{ON}}{L_1} \sqrt{\frac{T_{ON}}{3T_{SW}}} \left( \frac{3V_C}{V_D} + \frac{3(V_A - V_C)}{L_2} \right)^2 + \frac{3(V_A - V_C)}{V_D} (V_C - V_B)^2 + (V_C - V_B)(3V_C + (3V_C)^2) + \frac{6V_C}{V_D} (3V_C)^2 \]

The average current space vector method, developed in Section 2.1.3, can also be applied to the input phase currents. Using formulas (2-7, 2-8) and Fig. 5.27 the space vector and its components are determined as:

\[ i(T_{ON})_A = \frac{3V_m}{L_1} \frac{T_{ON}}{L_1} e^{j(\alpha_{r} - \pi/2)} + \frac{3V_m}{L_2} \frac{T_{ON}}{L_2} e^{j(\alpha_{r} - \pi/2)} + \frac{3V_m}{L_2} \frac{T_{ON}}{L_2} e^{j(\alpha_{r} - \pi/2)} e^{j\pi/3} \]  

(5-35)

\[ i(T_{ON})_B = \frac{V_m}{L_1} \frac{T_{ON}}{L_1} e^{j(\alpha_{r} - \pi/2)} + \frac{V_m}{L_1} \frac{T_{ON}}{L_1} e^{j(\alpha_{r} - \pi/2)} e^{-j\pi/3} \]

\[ i(t_1) = \frac{3V_m}{L_1} \frac{T_{ON}}{L_1} e^{-j\pi/2} \]

\[ i_{AV} = \frac{V_m}{2T_{SW}} \left[ \frac{T_{ON}^2}{L_1} \left( \frac{1}{L_1} + \frac{1}{L_2} \right) + \frac{T_{ON} t_1}{L_1} \right] e^{-j\pi/2} \]

\[ + \frac{V_m}{2T_{SW}} \left[ \frac{T_{ON}^2}{L_2} \left( \frac{1}{L_2} + \frac{T_{ON} t_1}{L_1} \right) e^{-j\pi/2} \right] e^{j\pi/3} + \frac{2\sqrt{3}V_C}{L_1} \frac{T_{ON} (t_1 + t_2)}{2T_{SW}} e^{-j\pi/2} \]

Since in the case of the SEPIC converter no modulation is needed, due to the intrinsic low harmonic content, the average current space vector will not be further used.
Applying formula (5-33) and using the symmetry of the waveform, the plots have been drawn in Fig. 5.28 for the normalized average phase current at various voltage transfer ratios. This current is what will appear on the line, due to the averaging effect of the input filter. The normalized rms currents for the inductors \( L_1 \), inductors \( L_2 \), and capacitors \( C_1 \) are obtained using the same technique and are shown in Figs. 5.29-5.31. MATLAB has been used for the calculation of the 5th, 7th harmonics, and THD of the normalized average phase current. By studying Fig. 5.32, an important advantage of the SEPIC converter can be seen, that low harmonic content can be achieved even at low voltage transfer ratios \( M \).

In Fig. 5.33, the contribution of the high frequency component to the total rms current for inductor \( L_1 \) is shown. It must be specified that where rms contribution is mentioned, the square of the rms currents is meant, in such way that their sum is equal to 100%. The conclusion is that the voltage transfer ratio has little effect on the high frequency/total rms current ratio.

5.2.4. Design Notes and Time Domain Simulations

As it has been shown in [48], the SEPIC converter used as a single-phase power factor correction stage has to meet a certain condition for the inductors ratio \( L_1 / L_2 \) so that the base line of the current in \( L_1 \) will have the same sign with the phase voltage during the time interval \( (t_2, T_{sw}) \).

For three-phase, the same condition will be determined in the following. The energy drawn by the circuit during one switching period is:

\[
E = L_1 \frac{(i_{1_{bc}}^2 - i_{1_{bc}}^2)}{2} + L_1 \frac{(i_{2_{bc}}^2 - i_{2_{bc}}^2)}{2} + L_1 \frac{(i_{3_{bc}}^2 - i_{3_{bc}}^2)}{2} + \\
+ L_2 \frac{(i_{1_{bc}}^2 - i_{1_{bc}}^2)}{2} + L_2 \frac{(i_{2_{bc}}^2 - i_{2_{bc}}^2)}{2} + L_2 \frac{(i_{3_{bc}}^2 - i_{3_{bc}}^2)}{2} = \frac{9V_{EN}^2}{4} T_{SW}^N \left( \frac{1}{L_1} + \frac{3}{L_2} \right) \tag{5-36}
\]

where:

\( I_{A_0}, I_{B_0}, I_{C_0} \) = currents in the \( L_1 \) inductors at the beginning of the switching period;

\( I_{B_0}, I_{Z_0}, I_{Y_0} \) = currents in the \( L_2 \) inductors at the beginning of the switching period;

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Fig. 5.28 Normalized average phase current vs. phase angle over one period.

Fig. 5.29 Normalized inductor $L_1$ rms current vs. phase angle over one period.

Fig. 5.30 Normalized inductor $L_2$ rms current vs. phase angle over one period.

Fig. 5.31 Normalized capacitor $C_1$ rms current vs. phase angle over one period.

Fig. 5.32 Normalized $5^{th}$, $7^{th}$ harmonics, and THD (%) of the average phase current vs. voltage transfer ratio $M$.

Fig. 5.33 Ratio (%) of the high frequency/total rms currents in inductor $L_i$ vs. voltage transfer ratio $M$. 

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\( I_{A_{PK}}, I_{B_{PK}}, I_{C_{PK}} \) = currents in the \( L_1 \) inductors at \( T_{ON} \);

\( I_{1_{PK}}, I_{2_{PK}}, I_{3_{PK}} \) = currents in the \( L_2 \) inductors at \( T_{ON} \).

At the same time, the energy can be written as:

\[
E = (V_A I_{A_{av}} + V_B I_{B_{av}} + V_C I_{C_{av}}) T_{SW} \tag{5-37}
\]

where:

\( I_{A_{av}}, I_{B_{av}}, I_{C_{av}} \) = "instantaneous" average phase currents at line frequency;

Making the two expressions (5-36) and (5-37) equal and taking into consideration:

\[
V_A I_A + V_B I_B + V_C I_C \geq 0 \tag{5-38}
\]

we obtain:

\[
\frac{L_1}{L_2} \geq \frac{4}{27 V_0 V_{LH}^2} \left[ V_A [3(V_A - V_C)(V_A - V_C)] + V_B [3(V_A - V_C)(V_B - V_A - 3V_C) - 18V_C^2] + V_C [3(V_A - V_C)(V_C - V_B + 3V_C) + 18V_C^2] \right] \tag{5-39}
\]

Since the above inequality should hold for any angle in the interval \((\pi/6, \pi/3)\), we obtain:

\[
\frac{L_1}{L_2} \geq \frac{1}{\sqrt{3M}} \tag{5-40}
\]

In terms of the load, the boundary condition for having discontinuous conduction mode is based on the method in [48] and results in the following:

\[
R \geq \frac{V_D}{I_{b_{av}}} = \frac{V_D^2}{([V_B - V_A - 3V_C]3(V_A - V_C) - 18V_C^2) \left( \frac{1}{L_1} + \frac{3}{L_2} \right) T_{SW}^2 T_{ON}^2} \tag{5-41}
\]

The discontinuous conduction mode is guaranteed for the whole period when:

\[
\left( \frac{1}{L_1} + \frac{3}{L_2} \right) R T_{SW} \leq \frac{3}{4(M + \sqrt{3})^2} \tag{5-42}
\]

The capacitor voltage has two constraints: to have a nearly constant value in a switching period and to follow the input voltage in a line period. Its value has a great influence on the input current waveform.
The resonant frequency of $C_1$, $L_1$, and $L_2$ must be much greater than the line frequency, to avoid input current oscillations each half-cycle. Besides, if the resonant frequency is near the switching frequency, the characteristic of good power factor is lost and the waveforms are distorted. As a general rule, based on the recommendation in [48], we can use:

$$\omega_{SW}^2 \gg \frac{1}{C_1 \left( \frac{L_1 + L_2}{\sqrt{3}} \right)} \gg \omega_{LINE}^2$$ (5-43)

The energy transfer between the inductor and capacitor networks during each switching cycle must keep the capacitor voltage ripple within reasonable limits. Therefore, the following design rules can be derived, based on energy considerations:

$$C_1 > \frac{9}{L_2} T_{ON}^2 \quad \text{and} \quad C_1 > \frac{3}{L_1} T_{ON}^2$$ (5-44)

As an example, a 3-phase 3-switches PFC stage was designed and simulated using PSIM. The following values have been chosen:

$$V_{LINE} = 208V, \quad f_{LINE} = 60Hz, \quad V_{OUT} = 600V, \quad P_{OUT} = 12.15KW, \quad L_1 = 90\mu H, \quad L_2 = 310\mu H,$$

$$C_1 = 14.1\mu F, \quad C_{OUT} = 4.700\mu F, \quad R = 29.6\Omega, \quad f_{SW} = 25KHz, \quad D = 0.47, \quad T_{STEP} = 1\mu sec., \quad T_{TOT} = 0.3\sec.$$ The phase current at the input of the high frequency filter and the capacitor $C_1$ voltage are given in Figs. 5.34 and 5.35. By inspection, it can be seen that the time domain simulation confirms the analytical results.

Fig. 5.34 Phase current at the input of the high frequency filter vs. time.

Fig. 5.35 Capacitor $C_1$ voltage vs. time.
5.2.5. Conclusions

A delta-SEPIC 3-phase 3-switch Power Factor Correction circuit based on the characteristic L-C-L networks has been analyzed relative to its DCM operation.

The same comments are valid as for the star-SEPIC circuit, in respect to advantage and disadvantages. The differences in between the star-SEPIC and delta-SEPIC are summarized in Table 5.1. As it can be seen the switch voltage is significantly lower for the delta-SEPIC circuit, but the trade-off is that ripple steering can no more be achieved. In terms of harmonic content, both circuits are well bellow the requirements of IEC 1000-3-2.

Table 5.1 Comparison between Delta-SEPIC and Star-SEPIC PFC circuits

<table>
<thead>
<tr>
<th>Type of circuit</th>
<th>Delta-SEPIC</th>
<th>Star-SEPIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD</td>
<td>5%</td>
<td>2.5%</td>
</tr>
<tr>
<td>Switch Voltage</td>
<td>( \frac{2V_P}{3} + \sqrt{3}V_{LN} )</td>
<td>( V_D + \sqrt{3}V_{LN} )</td>
</tr>
<tr>
<td>Number of switches</td>
<td>3</td>
<td>3/1</td>
</tr>
<tr>
<td>Switches type</td>
<td>Bi-directional</td>
<td>Bi-directional/quasi tri-directional</td>
</tr>
<tr>
<td>Ripple steering by inductors coupling</td>
<td>Not possible</td>
<td>Possible</td>
</tr>
</tbody>
</table>
CHAPTER 6
EXPERIMENTAL RESULTS

A proof of concept circuit has been built for the boost-delta PFC. Since the boost-delta is a phase sequence sensitive circuit. The circuit features for both phase sequence cases, ABC and ACB, are investigated. The properties of two parallel running boost-delta circuits with reverse phase sequence are studied. The results obtained analytically and in time-domain simulations are found to be in good agreement with the experimental data. Photos of the experimental set-up are presented.
6.1. Circuit Description

The experimental validation has been carried out for one of the circuits analyzed in the present thesis. The boost-delta circuit has been chosen due to the relative straightforward implementation, good performance and simplicity of control.

The test has been conceived on a proof-of-concept basis. Therefore the components have been chosen based on their off-the-shelf availability rather than an accurate design for a specific application.

The circuit diagram for the tested circuit is given in Fig. 6.1. Since the circuit is phase sequence sensitive (A-B-C and A-C-B), both possible cases have been studied.

![Fig. 6.1 Boost-delta PFC circuit.](image)

As was explained in Section 3.2, by connecting two boost-delta circuits in parallel, as in Fig. 6.2, each supplied with a different sequence, the harmonic content and THD decrease dramatically. A further advantage is the possibility of staggered operation, where one of the circuits is triggered during the interval \((0, T_{ON})\) and the other one during \((T_{SW} / 2, T_{SW} / 2 + T_{ON})\). By running two circuits in parallel, the number of components will increase, however their rating will be smaller and reduced heat dissipation will be achieved.
Fig. 6.2 Boost-delta PFC. Two circuits running in parallel, with reverse input phase connections.
Fig. 6.3 shows a possible way of implementing a bi-directional switch. The gate driving and PWM circuits have been implemented with circuits readily available in Xantrex and their schematics are shown in Figs. 6.4 and 6.5. The gating signals generated by the circuit in Fig. 6.5 are sent to the input of the circuit in Fig. 6.4. Isolation is then achieved and the output signals from the circuit in Fig. 6.4 are connected to gates of the bi-directional switches, as represented in detail in Fig. 6.3. The lists of components and other equipment used in the experimental part are given in Appendix G.

6.2. Theoretical and experimental results

The approach taken is to use MATLAB to determine analytically the current waveforms, the harmonic content and THD for a voltage transfer ratio $M=1.4$.

PSIM is then used for time-domain simulations. The experimental values are given in the following:

One stage (Fig. 6.1)

\[ V_{\text{Phase}} = 44V, f_{\text{LINE}} = 60Hz, L_1 = L_2 = L_3 = 87.5\mu H, L_4 = L_5 = L_6 = 180\mu H, C_1 = C_2 = C_3 = 8\mu F, \]
\[ C_7 = 4.480\mu F, R = 47.7\Omega, V_{\text{OUT}} = 151V, f_{\text{SW}} = 24KHz, D = 0.2, T_{\text{STEP}} = 1\mu \text{sec.}, T_{\text{TOT}} = 0.1\text{sec.}, \]
\[ P_{\text{OUT}} = 478W. \]

Two stages running in parallel (Fig. 6.2)

The values are the same as above, but $R = 24.4\Omega$, $P_{\text{OUT}} = 934W$. The following additions are made:

\[ L_7 = L_9 = L_8 = 87.5\mu H, L_{10} = L_{11} = L_{12} = 180\mu H, C_4 = C_5 = C_6 = 8\mu F \]

A practical implementation with the values used in the simulation is the final way of proving the concept. In order to illustrate the bench setup and circuit layout, several pictures have been taken and are presented in Section 6.4.
Fig. 6.3 Practical implementation of a bi-directional switch.

Fig. 6.4 Gate driving circuit.
Fig. 6.5 PWM and drivers circuit.
There are two ways in which a confirmation of the analytical results is performed. Firstly, a comparison of
the waveforms obtained by MATLAB, PSIM and the experiment is made. Secondly, the values of the
harmonics content and THD obtained with the three methods are compared.

The plots which show the performance of the single/double PFC circuits with/without phase sequence
reversal are shown as a first set. The line current is presented in Figs. 6.6-6.8 as obtained from MATLAB,
and PSIM. In practice, an input filter is necessary for removing the high frequency components from the
line current. For this reason, the PSIM simulation is carried out for this situation as well, and a good
confirmation of the experimental results can be seen in Figs. 6.9-6.11.

The inductor, switch, diode and capacitor currents are shown in Figs. 6.12-6.19 as obtained with PSIM and
experimentally. A close match of the waveforms can be noticed, at the line and switching frequencies.

In regards to switch, filter capacitor and output capacitor voltages, they are presented in Figs. 6.20-6.24.

The waveforms are shown at line and switching frequency.

For sake of comparison a test has been performed with the switches turned off, in which case the circuit
becomes a three-phase bridge rectifier. The PSIM simulation has been performed with a line impedance of
300 \( \mu \)H and the measurements have confirmed the theoretical shape as seen in Fig. 6.25 and 6.26. The
output voltage ripple for this case also shows a close match between theory and practice.

Notes:

- All experimental data has been taken with a current probe setting of 5A/10mV, except those in Figs.
  6.9 and 6.10 where 2A/10mV has been used. The voltage scale is given individually for each plot by
  the scope reading.

- The MATLAB plots use normalized values. The scale for the PSIM plots should be read: Volts for the
  voltage and Amperes for the current. The voltage measurements have somewhat been affected by noise
  since the experimental layout was not very compact.

- Fig. 6.23. The resolution of the scope could not be further expanded for the experimental
  measurement.

- Fig. 6.26. The superimposed oscillation in the experimental result is assumed to be due to the slight
  voltage imbalance of the supplying variac.
Fig. 6.6 Boost-delta PFC circuit. a) Line current vs. phase-angle. MATLAB simulation. b) Line current and voltage vs. time. PSIM simulation.

Fig. 6.7 Boost-delta PFC circuit with reversed phase sequence. a) Line current vs. phase-angle. MATLAB simulation. b) Line current and voltage vs. time. PSIM simulation.

Fig. 6.8 Boost-delta PFC circuit with two stages. a) Line current vs. phase-angle. MATLAB simulation. b) Line current and voltage vs. time. PSIM simulation.
Fig. 6.9 Line current and voltage vs. time for the boost-delta PFC with input filter:
a) PSIM, b) experimental, 2A/10mV scale.

Fig. 6.10 Line current and voltage vs. time for the boost-delta PFC with reversed phase sequence and input filter:
a) PSIM, b) experimental, 2A/10mV scale.

Fig. 6.11 Line current and voltage vs. time for the boost-delta PFC with two stages and input filter:
a) PSIM b) experimental, 5A/10mV scale.
Fig. 6.12 Inductor current vs. time at line frequency a) PSIM, b) experimental, 5A/10mV scale.

Fig. 6.13 Inductor current vs. time at switching frequency a) PSIM, b) experimental, 5A/10mV scale.

Fig. 6.14 Bi-directional switch current vs. time at line frequency:
a) PSIM, b) experimental, 5A/10mV scale.
Fig. 6.15 Bi-directional switch current vs. time at switching frequency:
   a) PSIM, b) experimental, 5A/10mV scale.

Fig. 6.16 Diode current vs. time at line frequency: a) PSIM, b) experimental, 5A/10mV scale.

Fig. 6.17 Diode current vs. time at switching frequency: a) PSIM, b) experimental, 5A/10mV scale.
Fig. 6.18 Filter capacitor current vs. time at line frequency: a) PSIM, b) experimental, 5A/10mV scale.

Fig. 6.19 Filter capacitor current vs. time at switching frequency: a) PSIM, b) experimental, 5A/10mV.

Fig. 6.20 Bi-directional switch voltage vs. time at line frequency: a) PSIM, b) experimental (inverted waveform).
Fig. 6.21 Bi-directional switch voltage vs. time at switching frequency: a) PSIM, b) experimental.

Fig. 6.22 Filter capacitor voltage vs. time at line frequency: a) PSIM, b) experimental.

Fig. 6.23 Filter capacitor ripple voltage vs. time at switching frequency: a) PSIM, b) experimental.
Fig. 6.24 Output capacitor ripple voltage vs. time at line frequency: a) PSIM, b) experimental.

Fig. 6.25 Input phase voltage and current of three-phase rectifying bridge vs. time:
a)PSIM, b) experimental.

Fig. 6.26 Output voltage ripple of three-phase rectifying bridge vs. time: a)PSIM, b) experimental.
Table 6.1 shows a comparison of the harmonic contents and THD for the single and double stage PFC circuits as given by MATLAB and PSIM. As can be seen a very good match occurs between the two types of theoretical determinations.

Table 6.1 Harmonics comparison of MATLAB and PSIM results

<table>
<thead>
<tr>
<th>Simulation</th>
<th>Boost-delta circuit</th>
<th>Two boost-delta circuits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MATLAB</td>
<td>PSIM</td>
</tr>
<tr>
<td>Input filter</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Phase sequence</td>
<td>ABC or ACB</td>
<td>ABC</td>
</tr>
<tr>
<td>5\textsuperscript{th} (%)</td>
<td>12.49</td>
<td>11.66</td>
</tr>
<tr>
<td>7\textsuperscript{th} (%)</td>
<td>2.47</td>
<td>2.41</td>
</tr>
<tr>
<td>11\textsuperscript{th} (%)</td>
<td>1.50</td>
<td>1.67</td>
</tr>
<tr>
<td>13\textsuperscript{th} (%)</td>
<td>0.59</td>
<td>0.56</td>
</tr>
<tr>
<td>THD (%)</td>
<td>12.85</td>
<td>12.04</td>
</tr>
</tbody>
</table>

The experimental results are shown in Table 6.2 and have been determined using a three-phase power analyzer. The experimental THD value of the PFC circuits is presented in Table 6.2, and when compared with the theoretical values given in Table 6.1 shows a close match. The influence of the input filter is shown by the difference in the harmonic content of the PSIM simulations and the theoretical MATLAB calculations. By inspecting the results it can also be seen that two stages running in parallel is the best solution in terms of power factor and harmonic content. For sake of comparison, the results are given also for the case where only a three phase bridge is used. The measurement can be performed very easily, by turning off the gating signal from the bi-directional switches. It can be seen how much better the performance of the power factor stage is, for a penalty in efficiency of about 3%. Generally speaking the efficiency of the PFC stage can be improved by using a soft- rather than hard-switching method, and designing the boost inductors for a lower ac resistance.
Table 6.2 Experimental measurements for the boost-delta PFC circuit

<table>
<thead>
<tr>
<th></th>
<th>Boost-delta circuit ABC sequence</th>
<th>Boost-delta circuit ACB sequence</th>
<th>Two boost-delta circuits ABC and ACB sequence</th>
<th>Three-phase rectifying bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output Voltage (V)</strong></td>
<td>151.1</td>
<td>151.5</td>
<td>152.3</td>
<td>150.3</td>
</tr>
<tr>
<td><strong>AC Phase Voltage (V)</strong></td>
<td>43.80</td>
<td>43.88</td>
<td>43.45</td>
<td>64.40</td>
</tr>
<tr>
<td><strong>AC Input Current (A)</strong></td>
<td>3.98</td>
<td>4.30</td>
<td>7.94</td>
<td>3.47</td>
</tr>
<tr>
<td><strong>Power Factor</strong></td>
<td>0.984</td>
<td>0.926</td>
<td>0.994</td>
<td>0.740</td>
</tr>
<tr>
<td><strong>Output Power (W)</strong></td>
<td>478.6</td>
<td>481.2</td>
<td>1028.8</td>
<td>473.6</td>
</tr>
<tr>
<td><strong>Input Power (W)</strong></td>
<td>514.6</td>
<td>524.2</td>
<td>950.2</td>
<td>496.8</td>
</tr>
<tr>
<td><strong>Efficiency (%)</strong></td>
<td>93.0</td>
<td>91.8</td>
<td>92.4</td>
<td>95.3</td>
</tr>
<tr>
<td><strong>Output Load (Ω)</strong></td>
<td>47.7</td>
<td>47.7</td>
<td>24.4</td>
<td>47.4</td>
</tr>
<tr>
<td><strong>Voltage Transfer Ratio</strong></td>
<td>1.41</td>
<td>1.41</td>
<td>1.44</td>
<td>0.95</td>
</tr>
<tr>
<td><strong>THD (%)</strong></td>
<td>11.45</td>
<td>11.57</td>
<td>5.70</td>
<td>79.97</td>
</tr>
</tbody>
</table>
6.3. Experimental Set-up Pictures

Photo 6.1 Bench set-up for testing the PFC circuit

Photo 6.2 Measurement equipment with test readings
Photo 6.3 PFC Circuit layout

Photo 6.4 Bi-directional switches and rectifying diodes
Photo 6.5 PWM circuit

Photo 6.6 Boost inductor and input filtering stage
CHAPTER 7

CONCLUSIONS

A comparison is carried out for all the circuits proposed in the present thesis. Conclusions are drawn as to their suitability for various applications. Recommendations are given and future work directions are outlined.
7.1. Comparison and Recommendations

The work covered in this thesis has dealt so far with the in-depth analysis of the properties of proposed PFC circuits. In order to have an overall view, whereby a comparison becomes more straightforward, the main features of the circuits are presented in Table 7.1 at page 139.

The switches column shows the voltage and current stress. Switches could be one of three types: uni-directional, bi-directional or quasi tri-directional. All of them, even if composed of several transistors, have a common emitter and consequently gating point. The triggering can be of two types: simultaneous, or modulation, where slight deviations from a simultaneous signal are used for individual switches. Where simultaneous–staggered appears in the Table, two parallel running boost stages, each one with simultaneous switching but staggered triggering in between circuits is meant.

The diodes column shows the number of three-phase bridges needed for the operation of the circuit. A common characteristic to all circuits is that the diodes see as maximum reverse voltage \( V_D \). The peak current is given for each three-phase diode bridge, and is characteristically high due to the operation in DCM. \( \Delta I_{\text{mod}} \) represents the amount of extra current due to the modulation and is proportional to the time \( t_{\text{mod}} \) and the current slope \( V/L \).

All the circuits studied in the present thesis are operating in boost mode. The number of passive components varies, being a characteristic which defines the type of circuit. The boost-star and boost-delta use only one set of inductors for obtaining PFC. Two sets of inductors are needed for the star-flyback, delta-flyback, star-delta and delta-delta PFCs. The SEPIC circuits are characterized by L-C-L networks, just like their single phase or DC-DC implementations. Table 7.1 shows the peak current in the inductors and the peak voltage across the capacitors, which are important parameters for the design.

In order to obtain a consistent comparison, the harmonics and THD of the analyzed circuits are given for a voltage transfer ratio \( M=1.4 \). Since some of the circuits are phase sequence sensitive and characterized by a displacement factor, this parameter is also shown. For circuits with two sets of inductors, their ratio influences the harmonic content. The comments column shows the ratios chosen, and they are based on the principle of equal amounts of stored energy and consequently equal physical size of the two inductors.
It can be seen in general that a complex trade-off of the performance parameters occurs. There is no universal solution and different approaches can be used for various applications. A short description of the advantages and limitations are given below for each of the proposed circuits:

- **Boost-Star DC side switch**

The simplicity of the circuit makes it a favorite in many practical applications. While the uni-directional switch and rectifying diode are operating under DC conditions, which simplifies the implementation of soft-switching, their power stress is very high and often several components must be paralleled. The content of harmonics cannot be reduced substantially for \( M=1.4 \) which limits the application to 5 KW for meeting IEC 1000-3-2, unless harmonic injection schemes are implemented. Several circuits running in parallel can have staggered operation, which will reduce the EMI requirements for the input filter, but no improvement will be achieved in regards to the harmonic content.

- **Boost-Star AC side switch**

The circuit can be implemented with either three bi-directional or a single quasi tri-directional switch. Since three independent triggering signals are now available, a certain amount of modulation can reduce the harmonics down to zero. The degree of approximation of the analytically determined modulation will determine the amount of harmonic reduction in practice. The modulation is dependent on \( M \), the output power as well as the phase angle. Consequently the control will be somewhat more complicated than in the case of the boost-star with DC side switch. For this circuit as well as for all the other ones further described, the soft switching/snubbering of bi-directional switches under AC conditions has been little developed and presents new opportunities for research.

- **Boost-Delta**

By connecting the switches in a delta rather than a star configuration, a new set of properties is obtained. The circuit will bring a small benefit when compared with the Boost-Star DC-side switch. However, the situation changes when two circuits with reverse switch connection sequence are running in parallel. The
amount of reduction of harmonics is dramatic and practically the requirements for the whole range covered by IEC 1000-3-2 are met. In addition staggering is possible, relieving the EMI/RFI filter of some of the performance requirements. The fact that the transistor's emitters are at different potentials is one of the drawbacks, but it is compensated by the simultaneous operation and possibility of having a single pulse transformer with three isolated secondaries for driving. Another disadvantage is the relatively high number of semiconductors of the circuit, but in fact this is just a redistribution of the semiconductor area in more components. If the properties of the circuit seem to justify it, the semiconductor manufacturers could assemble the three bi-directional switches in a compact package.

- Starfly
This circuit has two sets of boosting inductors, series connected during the on-time and parallel running during the off-time. It is a combination of a Boost-Star and a Flyback, whereby a trade-off between the characteristics of the two circuits is achieved, pending on the inductors ratio. Three bi-directional switches with the emitter at various potentials and simultaneous triggering are used. The advantages are split inductors and switching bridges, improved harmonic content. Due to the topological similarity to the Boost-Star with AC-side switch, in this case too, zero harmonic content can be achieved by modulation. The main disadvantages are higher component number and a moderately high switching stress for a significant harmonic reduction.

- Deltafly
A similar combination as the circuit previously described, this time a Boost-Delta and a Flyback are connected together. A characteristic common to all circuits with two inductor sets is the relative large number of components which makes staggered operation with another similar circuit a complex implementation. Since the boost-delta is phase sequence sensitive, this feature is conveyed to the new circuit. The harmonic content and displacement angle are alleviated as compared to the original boost delta, depending on the inductance ratio, just like in the case of the Star-Flyback. However, while the mentioned
circuit has three bi-directional switches, the DeltaFly has to use six bi-directional or three quasi tri-directional switches. This represents a heavy toll on semiconductor components.

- Star–Delta

Three bi-directional switches are needed to implement this circuit. The reasonable number of semiconductors is offset by the relatively low improvement in performance over the Boost-Star with DC side switch. The displacement angle, characteristic to the boost-delta, is a property carried over even though it is significantly reduced.

- Delta–Delta

As in the Delta–Flyback circuit, six bi-directional switches or three quasi tri-directional switches are needed for implementation. The high number of semiconductors and a displacement angle of about nine degrees are the price to pay for a very good harmonic performance.

- SEPIC-Star

As is the case with all the other SEPIC circuits, in this case too a high switch stress and current ripple are the major drawbacks in a practical implementation. On the other hand, very good transient performance and very low harmonic content are achieved. A quasi tri-directional switch could be used with a simple, simultaneous triggering of its three transistors. Ripple current steering can be obtained, giving the circuit CCM type of current waveforms with a simple voltage follower control.

- SEPIC-Delta

This circuit represents a variant of the SEPIC-Star. The switches are delta rather then star connected and consequently their voltage stress is significantly reduced, from about 170% to 130% of the DC rail. An insignificant displacement angle will appear and the harmonics will be very small. As a trade-off this time three bi-directional switches must be used with isolated gate drives. In addition, ripple current steering is
no more possible. In general the SEPIC-derived circuits will not be interesting for a practical implementation, unless some particular features of the SEPIC are required by the application.

It is expected that the proposed circuits using a single set of inductors will be the most attractive in practice. The circuits using two sets of inductors could be interesting for particular applications where splitting the inductors and rectifying bridges becomes a layout advantage or the power level requires it. Except of the Star-Flyback, all the circuits in the two inductors category would have to be used where a small displacement angle is acceptable, and/or can be offset to some extent by the EMI/RFI input filter.

7.2. Conclusions and Future Work

The work done in the present thesis lays the theoretical basis for obtaining power factor correction with lower harmonic content than any other circuits operating in Discontinuous Conduction Mode. The practical implementation in successful applications is based on further research in the technological aspects, such as high efficiency bi-directional switches and good techniques for soft-switching in AC.

A wide selection of new circuits has been proposed, allowing the flexibility of choice based on specific application requirements. Experimental results have shown a close match with the expected performance, as determined analytically with MATLAB and in time domain simulations with PSIM.

The PFC circuits presented bring a significant contribution in regards to new schematic and control solutions. While the general properties have been covered in the thesis, the author deems further research necessary, particularly in the following areas:

- Small Signal Modeling,
- Operation with other loads then a voltage source,
- Operation under unbalanced/distorted voltage condition,
- Influence of the unequal value of the inductors,
- Noise Reduction with Random Pulse Width Modulation,
• Interaction between EMI filter and PFC stage,
• Soft-switching of bi-directional switches in AC.

In regards to the future prospects, it can be expected that the use of three-phase PFC circuits will grow substantially. The growth will be most prominent in applications such as telecommunications, autonomous ac power systems (e.g. aircraft and ships) and other applications where performance and/or power density are critical. In the consumer and industrial markets, the growth will be mainly conditioned by new power quality regulations due to the significant add-on cost of active PFC when compared to diode rectification and bulky passive filter. For the low power applications, the simple three-phase PFC circuits may provide a cost effective solution with satisfactory performances. At the high power end, the trade-off between passive harmonic filtering and the active PFC tends to be in favor of the active circuits.

The issues of high frequency operation, input current quality, EMI filtering, high efficiency and power density remain the driving force in the development of PFC circuits. Because the performance requirements in the PFC applications are much less diversified and complicated than that in the motor drive applications, development of standardized, low cost, single-chip digital controllers could be expected soon. Many of these results will also benefit three-phase inverter design, especially in applications such as three-phase distributed power systems and uninterruptible power supplies.
BIBLIOGRAPHY


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APPENDIX A

Determination of the closed form expressions for the switching frequency and harmonic components of the inductor current in the boost-star PFC circuit with DC-side switch

The phase current waveforms for the boost-star PFC circuit are shown in Fig. 2.3 and are described by the following expressions over a switching cycle:

\[ 0 < x < T_{ON} \]
\[ f_A(x) = \frac{V_c}{L} x \quad \text{(A-1)} \]

\[ T_{ON} < x < t_1 \]
\[ f_A(x) = \frac{V_c}{L} T_{ON} + \frac{V_c - V_D / 3}{L} (x - T_{ON}) \]

\[ t_1 < x < T_{SW} \]
\[ f_A(x) = 0 \quad \text{(A-2)} \]

\[ 0 < x < T_{ON} \]
\[ f_B(x) = \frac{V_B}{L} x \]

\[ T_{ON} < x < t_1 \]
\[ f_B(x) = \frac{V_B}{L} T_{ON} + \frac{V_B + 2V_D / 3}{L} (x - T_{ON}) \]

\[ t_1 < x < t_2 \]
\[ f_B(x) = \frac{V_B(V_A - V_C)}{(V_D - 3V_A)L} T_{ON} + \frac{V_D + V_B - V_C}{2L} (x - t_1) \]

\[ t_2 < x < T_{SW} \]
\[ f_B(x) = 0 \]

The phase current waveforms for the boost-star PFC circuit are shown in Fig. 2.3 and are described by the following expressions over a switching cycle:

\[ 0 < x < T_{ON} \]
\[ f_C(x) = \frac{V_C}{L} x \quad \text{(A-3)} \]

\[ T_{ON} < x < t_1 \]
\[ f_C(x) = \frac{V_C}{L} T_{ON} + \frac{V_C - V_D / 3}{L} (x - T_{ON}) \]

\[ t_1 < x < t_2 \]
\[ f_C(x) = \frac{(V_C - V_A) V_D}{(V_D - 3V_A)L} T_{ON} + \frac{V_C - V_B - V_D}{2L} (x - t_1) \]

\[ t_2 < x < T_{SW} \]
\[ f_C(x) = 0 \]

The generalized formulas for the switching frequency harmonics have been calculated based on formulas (2-24, 2-25, 2-28) and are given below for the particular case of the boost-star PFC circuit.

\[ i_{A-f_{sw-nth-sin}} = \frac{1}{\pi} \int_0^{\pi/n} f_A(x) \sin nA \, dx = \]
\[ = \frac{1}{n^2 \pi} \left[ \frac{V_A}{L} \left( \sin n\alpha - n\alpha \cos n\alpha \right) + n\alpha \left( \frac{V_D / 3}{L} \right) \left( \cos n\alpha - \cos n\beta \right) + \right. \]
\[ \left. + \frac{V_A - V_D / 3}{L} \left( \sin n\beta - \sin n\alpha - n\beta \cos n\beta + n\alpha \cos n\alpha \right) \right] \quad \text{(A-4)} \]

\[ i_{A-f_{sw-nth-cos}} = \frac{1}{\pi} \int_0^{\pi/n} f_A(x) \cos nA \, dx = \]
\[ = \frac{1}{n^2 \pi} \left[ \frac{V_A}{L} \left( \cos n\alpha - 1 + n\alpha \sin n\alpha \right) + n\alpha \left( \frac{V_D / 3}{L} \right) \left( \sin n\beta - \sin n\alpha \right) + \right. \]

\[ \left. + \frac{V_A - V_D / 3}{L} \left( \cos n\beta - \cos n\alpha - n\beta \cos n\beta + n\alpha \cos n\alpha \right) \right] \]
\[ + \frac{V_s - V_D/3}{L} \left( \cos \beta + n \beta \sin \alpha - \cos \gamma - n \alpha \sin \gamma \right) \]

\[ i_{\beta-fa-nth-sin} = \frac{1}{\pi} \int_{\alpha}^{\beta} f_B(x) \sin nxdx = \]

\[ = \frac{1}{n^2 \pi} \left( \frac{V_B}{L} \left( \sin \alpha - \alpha \cos \alpha \right) + n \alpha \left( -\frac{2V_D/3}{L} \right) \left( \cos \alpha - \cos \beta \right) + \right. \]

\[ + \frac{V_B + 2V_D/3}{L} \left( \sin \beta - \sin n \alpha - \beta \cos n \alpha + n \alpha \cos n \alpha \right) + \]

\[ + \frac{V_B + V_C}{2L} \left( \cos \gamma - \sin n \beta - \gamma \cos n \beta + n \beta \cos n \beta \right) \]

\[ i_{\beta-fa-nth-cos} = \frac{1}{\pi} \int_{\alpha}^{\beta} f_B(x) \cos nxdx = \]

\[ = \frac{1}{n^2 \pi} \left( \frac{V_C}{L} \left( \sin \alpha - \alpha \cos \alpha \right) + n \alpha \left( \frac{V_D/3}{L} \right) \left( \cos \alpha - \cos \beta \right) + \right. \]

\[ + \frac{V_C - V_D/3}{L} \left( \sin \beta - \sin n \alpha - \beta \cos n \alpha + n \alpha \cos n \alpha \right) + \]

\[ + \frac{V_C - V_B - V_D}{2L} \left( \cos \gamma - \sin n \beta - \gamma \cos n \beta + n \beta \cos n \beta \right) \]

\[ i_{\beta-fa-nth-cos} = \frac{1}{\pi} \int_{\alpha}^{\beta} f_C(x) \cos nxdx = \]

\[ = \frac{1}{n^2 \pi} \left( \frac{V_C}{L} \left( \sin \alpha - \alpha \cos \alpha \right) + n \alpha \left( \frac{V_D/3}{L} \right) \left( \cos \alpha - \cos \beta \right) + \right. \]

\[ + \frac{V_C - V_D/3}{L} \left( \cos \beta - \cos \gamma - \beta \sin n \beta + n \alpha \sin n \alpha \right) + \]

\[ + \frac{V_C - V_B - V_D}{2L} \left( \cos \gamma - \sin n \beta - \gamma \cos n \beta + n \beta \cos n \beta \right) \]

\[ \left( A-6 \right) \]

\[ \left( A-7 \right) \]

\[ \left( A-8 \right) \]

\[ \left( A-9 \right) \]

\[ \left( A-10 \right) \]

\[ \alpha = \frac{T_{ON}}{T_{SW}} 2\pi \ ; \ \beta = \frac{T_{ON} + t_1}{T_{SW}} 2\pi \ ; \ \gamma = \frac{T_{ON} + t_1 + t_2}{T_{SW}} 2\pi \]
APPENDIX B

Formulas for the determination of the optimum modulation of boost-star PFC circuits with AC-side switches

Modulation at the end of the ON-interval

The equations for various combinations of switch turn-offs at the end of the ON-interval are determined as follows:

\[
\frac{di}{dt} = \begin{cases} 
\frac{V_A}{L}, & \text{if } (B-1) \\
\frac{V_B + V_D/3}{L}, & \text{if } (B-2) \\
\frac{V_A - V_D/3}{L}, & \text{if } (B-3) \\
\frac{V_A - 2V_D/3}{L}, & \text{if } (B-4) \\
\frac{V_C - V_D/3}{L}, & \text{if } (B-5) \\
\end{cases}
\]

\[
V_{L_{\text{ABC}}} = \frac{V_m}{L} e^{j(\omega t - \pi/2)}
\]

\[
V_{L_{\text{ABC}}} = \frac{V_m}{L} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L} e^{-j\pi/3}
\]

\[
V_{L_{\text{ABC}}} = \frac{V_m}{L} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L} e^{j\pi/3}
\]

\[
V_{L_{\text{ABC}}} = \frac{V_m}{L} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L} e^{j\pi/3}
\]

000

The operation in this interval can be split into two:

- current flowing in three rectifying diodes:

\[
\frac{di}{dt} = \begin{cases} 
\frac{V_A - V_D/3}{L}, & \text{if } (B-5) \\
\frac{V_B + 2V_D/3}{L}, & \text{if } (B-5) \\
\frac{V_C - V_D/3}{L}, & \text{if } (B-5) \\
\end{cases}
\]

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\[ V_{L,ABC} = \frac{V_u}{L} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L} e^{j\pi/3} \]

- current flowing in two rectifying diodes:

\[
\frac{di_a}{dt} = 0, \quad \frac{di_b}{dt} = \frac{V_B - V_C + V_D}{2L}, \quad \frac{di_c}{dt} = \frac{V_C - V_B - V_D}{2L} \quad (B-6)
\]

\[ V_{L,ABC} = \frac{\sqrt{3}(V_B - V_C)}{3L} e^{j\pi/2} + \frac{\sqrt{3}V_D}{3L} e^{j\pi/2} \]

This equation is valid under the condition: \( i_c(t_a) > i_a(t_a) = 0 \).

Determination of \( t_a \) for modulation at the end of the ON-interval

From \( \text{Im}(t_{AV}) = 0 \) it results:

\[
t_a(t_a + 2t_1 + t_2) \sin(\pi/6 + \omega t) = t_1(t_1 + t_2) \sin(\pi/6 - \omega t) \quad (B-7)
\]

where:

\[
t_1 = \frac{V_A}{V_D/3 - V_A} T_{ON} + \frac{V_D/3 + V_A}{V_D/3 - V_A} t_a \quad (B-8)
\]

\[
t_2 = \left[ \frac{2V_B}{V_C - V_B - V_D} + \frac{2V_A(V_B + 2V_D/3)}{V_C - V_B - V_D(V_D/3 - V_A)} \right] T_{ON} + \left[ \frac{2(V_B + V_D/3)}{V_C - V_B - V_D} + \frac{2(V_B + 2V_D/3)(V_D/3 + V_A)}{V_C - V_B - V_D(V_D/3 - V_A)} \right] t_a
\]

By writing:

\[
t_1 = A + Bt_{a-r} \quad (B-9)
\]

\[
t_2 = C + Dt_{a-r}
\]

\[
E = \frac{\sin(\pi/6 - \omega t)}{\sin(\pi/6 + \omega t)}
\]

\[
F = 1 + 2B + D - BE(B + D)
\]

\[
G = 2A + C - E(BA + BC + AB + AD)
\]

\[
H = -AE(A + C)
\]

\[
t_{a-r} = \frac{t_a}{T_{ON}}
\]

we obtain the following equation:

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Simulations using MATLAB show that the equation has only one positive root over the \((0, \pi/6)\) interval.

Also through simulation it is checked that the resulting \(i_a(t)\) maintains \(i_c(t) > i_a(t) = 0\).

Modulation at the beginning of the ON-interval

The equations for various combinations of switch turn-ons at the beginning of the ON-interval are determined as follows:

\[ \frac{di_a}{dt} = \frac{V_A}{L}, \quad \frac{di_b}{dt} = \frac{V_B}{L}, \quad \frac{di_c}{dt} = \frac{V_C}{L}, \quad V_{L,ABC} = \frac{V_m}{L} e^{j(\alpha - \pi/2)} \]  

(B-11)

\[ \frac{di_a}{dt} = \frac{V_A - V_B}{2L}, \quad \frac{di_b}{dt} = \frac{V_A - V_B}{2L}, \quad \frac{di_c}{dt} = 0, \quad V_{L,ABC} = \frac{\sqrt{3}(V_A - V_B)}{3L} e^{-j\pi/6} \]  

(B-12)

\[ \frac{di_a}{dt} = \frac{V_C - V_A}{2L}, \quad \frac{di_b}{dt} = 0, \quad \frac{di_c}{dt} = \frac{V_A - V_B}{2L}, \quad V_{L,ABC} = \frac{\sqrt{3}(V_C - V_A)}{3L} e^{-j\pi/6} \]  

(B-13)

\[ \frac{di_a}{dt} = 0, \quad \frac{di_b}{dt} = \frac{V_B - V_C}{2L}, \quad \frac{di_c}{dt} = -\frac{V_B - V_C}{2L}, \quad V_{L,ABC} = \frac{\sqrt{3}(V_B - V_C)}{3L} e^{j\pi/2} \]  

(B-14)

The operation in this interval can be split into two:

- current flowing in three rectifying diodes:
  \[ \frac{di_a}{dt} = \frac{V_A - V_D/3}{L}, \quad \frac{di_b}{dt} = \frac{V_B + 2V_D/3}{L}, \quad \frac{di_c}{dt} = \frac{V_C - V_D/3}{L}, \quad V_{L,ABC} = \frac{V_m}{L} e^{j(\alpha - \pi/2)} + \frac{2V_D}{3L} e^{-j\pi/3} \]  

(B-15)

- current flowing in two rectifying diodes:
  \[ \frac{di_a}{dt} = 0, \quad \frac{di_b}{dt} = \frac{V_B - V_C + V_D}{2L}, \quad \frac{di_c}{dt} = \frac{V_C - V_B - V_D}{2L}, \quad V_{L,ABC} = \frac{\sqrt{3}(V_B - V_C)}{3L} e^{j\pi/2} + \frac{\sqrt{3}V_D}{3L} e^{j\pi/2} \]  

(B-16)

This equation is valid under the condition: \(i_c(t_1) > i_a(t_1) = 0\).
Determination of \( t_a \) for modulation at the beginning of the ON-interval

From \( \text{Im}(i_{AV}) = 0 \) it results:

\[
t_a(t_a + 2T_{ON} + 2t_1 + t_2)\sin(\pi/3 - \omega t) = t_1(t_1 + t_2)\frac{2V_D}{\sqrt{3(V_A - V_B)}}\sin(\pi/6 - \omega t)
\]  \hspace{1cm} (B-17)

where:

\[
t_1 = \frac{V_A}{V_D/3 - V_A}T_{ON} + \frac{2(V_A - V_B)}{2(V_D/3 - V_A)}t_a
\]  \hspace{1cm} (B-18)

\[
t_2 = \left[ \frac{2V_B}{V_C - V_B - V_D} + \frac{2V_A(V_B + |2V_D/3|)}{(V_C - V_B - V_D)(V_D/3 - V_A)} \right]T_{ON} + \left[ \frac{V_B - V_A}{V_C - V_B - V_D} + \frac{(V_B + 2V_D/3)(V_A - V_B)}{(V_C - V_B - V_D)(V_D/3 - V_A)} \right]t_a
\]  \hspace{1cm} (B-19)

By writing:

\[
t_1 = A + Bt_{a-r}
\]  \hspace{1cm} (B-20)

\[
t_2 = C + Dt_{a-r}
\]

\[
E = -\frac{2V_D}{\sqrt{3(V_A - V_B)}}\sin(\pi/6 - \omega t)
\]

\[
F = 1 + 2B + D - BE(B + D)
\]

\[
G = 2A + C - E(BA + BC + AB + AD)
\]

\[
H = -AE(A + C)
\]

\[
t_{a-r} = \frac{t_a}{T_{ON}}
\]

we obtain the following equation:

\[
Ft_{a-r} + Gt_{a-r} + H = 0
\]  \hspace{1cm} (B-21)

Simulations using MATLAB show that the equation has only one positive root over the \((0, \pi/6)\) interval.

Also through simulation it is checked that the resulting \( t_{a-r} \) maintains \( i_C(t_1) > i_A(t_1) = 0 \).
APPENDIX C

Formulas for the determination of the current waveforms for the boost-delta PFC circuit

The following parameters have been used for describing the performance of the circuits:

- the normalized phase current: 

\[ i_{A_N} = \frac{i_A}{i_{N_t}} \]  

where: \( i_A \) = phase current, 

\[ i_{N_t} = \frac{V_{LN} T_{SW}}{2L} \] = normalizing L current.

There are two possible states of the three switches: 000 or 111. When all the switches are closed (111) the circuit looks like in Fig. 3.27 and the following equations can be written:

\[ i_1(T_{ON}) = \frac{V_{ab} T_{ON}}{L}, \quad i_2(T_{ON}) = \frac{V_{bc} T_{ON}}{L}, \quad i_3(T_{ON}) = \frac{V_{ca} T_{ON}}{L} \]  

\[ i_{m1}(T_{ON}) = \frac{(V_{ab} - V_{ca}) T_{ON}}{L}, \quad i_{m2}(T_{ON}) = \frac{(V_{bc} - V_{ab}) T_{ON}}{L}, \quad i_{m3}(T_{ON}) = \frac{(V_{ca} - V_{bc}) T_{ON}}{L} \]  

where \( i_1(T_{ON}), i_2(T_{ON}), i_3(T_{ON}) \) are the currents through the inductors and \( i_{m1}(T_{ON}), i_{m2}(T_{ON}), i_{m3}(T_{ON}) \) are the phase currents at the end of the ON interval.

During the off time of the switches (000) the current flow is dependent on the instantaneous values of the currents (proportional to the instantaneous voltage). For the equivalent circuit presented in Fig. 3.28 the following equations can be written:

\[ V_a - L \frac{di_a}{dt} = V_c - L \frac{di_c}{dt} = V_b - L \frac{di_b}{dt} + V_d \]  

\[ V_a + V_b + V_c = 0 \]

\[ i_a + i_c + i_b = 0 \]

Solving the system the following solution is obtained:

\[ i_1(t) = \frac{V_{ab} T_{ON}}{L} + \frac{V_a - \frac{1}{3} V_d}{L} (t - T_{ON}) \]
The time at which the current would reach zero in the three inductors is determined as:

\[ t_{\text{on}} = T_{\text{on}} \frac{V_D - 3V_A}{V_D - 3V_A} \]

\[ t_{\text{on}} = T_{\text{on}} \frac{2V_D + 3V_C}{2V_D + 3V_A} \]

\[ t_{\text{on}} = T_{\text{on}} \frac{V_D - 3V_A}{V_D - 3V_C} \]

Since the beginning of the interval studied is taken as the zero crossing of \( V_{ab} \) the phase voltages are written as:

\[ V_A = V_{LN} \sin(\omega t - \frac{\pi}{6}) \]

\[ V_B = V_{LN} \sin(\omega t - \frac{5\pi}{6}) \]

\[ V_C = V_{LN} \sin(\omega t + \frac{\pi}{2}) \]

\[ V_D = V_{LN} M \sqrt{3} \]

After the time point where one of the currents becomes zero, the analysis must be carried out for two intervals:

Interval \((0, \alpha)\)

\[ i_L(t_{\text{in}}) = 0 \]

\[ i_L(t_{\text{in}}) = -i_L(t_{\text{in}}) = \frac{V_{D}T_{\text{on}}}{L} + \frac{1}{3} \frac{V_D}{L} (T_{\text{on}} V_D - 3V_A - T_{\text{on}}) \]
After \( t_{i1} \) the current in inductors 2 and 3 is equal and of opposite sign. The equivalent circuit is shown in Fig. 3.29 and the following equations describe the circuit:

\[
V_c - L \frac{di_2}{dt} = V_a - L \frac{di_3}{dt} + V_d
\]

\( i_2 + i_3 = 0 \)

By solving:

\[
i_2(t) = i_2(t_{i1}) + \frac{1}{L} (V_c - V_a - V_d) \left( t - t_{i1} \right)
\]

The time \( t_2 \) at which the current through inductors 2 and 3 will become 0 is determined as:

\[
t_2 = t_{i1} - \frac{i_2(t_{i1})L}{\frac{1}{2}(V_c - V_a - V_d)}
\]

\( i_2(t_2) = 0 \)

The instantaneous currents in the three phases and inductors are shown in Fig. 3.34.

The average current in the inductors over a switching period can be calculated as follows:

\[
i_{k1} = \frac{1}{2t_2} i_k(T_{ON})t_{i1}
\]

\[
i_{k2} = \frac{1}{2t_2} \left\{ i_k(T_{ON})T_{ON} + (t_{i1} - T_{ON})[i_k(T_{ON}) + i_k(t_{i1})] + (t_2 - t_{i1})i_k(t_{i1}) \right\}
\]

\[
i_{k3} = \frac{1}{2t_2} \left\{ i_k(T_{ON})T_{ON} + (t_{i1} - T_{ON})[i_k(T_{ON}) + i_k(t_{i1})] + (t_2 - t_{i1})i_k(t_{i1}) \right\}
\]

The average current in the phases over a switching period can be calculated as follows:

\[
i_{ph1} = \frac{1}{2t_2} \left\{ i_{ph1}(T_{ON})T_{ON} + (t_{i1} - T_{ON})i_1(T_{ON}) \right\}
\]

\[
i_{ph2} = \frac{1}{2t_2} \left\{ i_{ph2}(T_{ON})T_{ON} + (t_{i1} - T_{ON})[i_2(T_{ON}) + i_2(t_{i1})] + (t_2 - t_{i1})i_2(t_{i1}) \right\}
\]

\[
i_{ph3} = \frac{1}{2t_2} \left\{ i_{ph3}(T_{ON})T_{ON} + (t_{i1} - T_{ON})[i_3(T_{ON}) + i_3(t_{i1})] + (t_2 - t_{i1})i_3(t_{i1}) \right\}
\]
Interval \((\alpha, \pi/3)\)

\[ i_j(t_{13}) = 0 \quad (C-14) \]

\[ i_i(t_{13}) = -i_j(t_{13}) = \frac{V_{\alpha}T_{on}}{L} + \frac{V_{\alpha} - V_B}{3L}(T_{on} \frac{V_B - 3V_d - V_{on}}{V_B - 3V_c}) \]

After \(t_{11}\) the currents in inductors 1 and 2 are equal and of opposite sign. The equivalent circuit is shown in Fig. 3.30 and the following equations describe the circuit:

\[ V_{\alpha} - L \frac{di_1}{dt} = V_{\beta} - L \frac{di_2}{dt} + V_{\beta} , i_1 + i_2 = 0 \quad (C-15) \]

By solving:

\[ i_1(t) = i_1(t_{13}) + \frac{1}{L} \left( V_{\alpha} - V_{\beta} - V_{\beta} \right) \left( t - t_{13} \right) \]

\[ i_i(t_{13}) = 0 \quad (C-16) \]

The time \(t_{12}\) at which the current through inductors 1 and 2 will become 0 is determined as:

\[ t_{12} = t_{13} - \frac{i_i(t_{13})L}{\frac{1}{2} \left( V_{\alpha} - V_{\beta} - V_{\beta} \right)} \quad (C-17) \]

The average of the current in the inductors over a switching period can be calculated as follows:

\[ i_{L1} = \frac{1}{2t_{2}} \{ i_i(T_{on})T_{on} + (t_{13} - T_{on})[i_i(T_{on}) + i_i(t_{13})] + (t_{2} - t_{13})i_i(t_{13}) \} \]

\[ i_{L2} = \frac{1}{2t_{2}} \{ i_2(T_{on})T_{on} + (t_{13} - T_{on})[i_2(T_{on}) + i_2(t_{13})] + (t_{2} - t_{13})i_2(t_{13}) \} \]

\[ i_{L3} = \frac{1}{2t_{2}} i_i(T_{on})t_{13} \]

The average of the current in the phases over a switching period can be calculated as follows:

\[ i_{PH1} = \frac{1}{2t_{2}} \{ i_{ph1}(T_{on})T_{on} + (t_{13} - T_{on})[i_i(T_{on}) + i_i(t_{13})] + (t_{2} - t_{13})i_i(t_{13}) \} \]

\[ i_{PH2} = \frac{1}{2t_{2}} \{ i_{ph2}(T_{on})T_{on} + (t_{13} - T_{on})[i_2(T_{on}) + i_2(t_{13})] + (t_{2} - t_{13})i_2(t_{13}) \} \]

\[ i_{PH3} = \frac{1}{2t_{2}} \{ i_{ph3}(T_{on})T_{on} + (t_{13} - T_{on})i_i(T_{on}) \} \]
APPENDIX D

Determination of the currents in the ‘Starfly’ PFC circuit operating in DCM

State 111

During this state all the switches are on, the inductors are building up energy and no power transfer occurs to the DC side. As it can be seen in the Fig. 4.2 we have the two sets of inductors, $L_1$ and $L_2$, in a star-delta configuration across the input three-phase voltage system.

While $0 < t < T_{on}$ the inductor currents, as shown in Figs. 4.2, 4.4 and 4.5, have the following expressions:

\[ i_1(t) = \frac{3V_A}{3L_1 + L_2} - t \text{, } i_2(t) = \frac{3V_B}{3L_1 + L_2} - t \text{, } i_3(t) = \frac{3V_C}{3L_1 + L_2} - t \]  \hspace{1cm} (D-1)

\[ i_1(t) = \frac{V_A - V_B}{3L_1 + L_2} - t \text{, } i_2(t) = \frac{V_B - V_C}{3L_1 + L_2} - t \text{, } i_3(t) = \frac{V_C - V_A}{3L_1 + L_2} - t \]  \hspace{1cm} (D-2)

At the end of the interval the following currents have been reached in the inductors:

\[ i_1(T_{on}) = \frac{3V_A}{3L_1 + L_2} - T_{on} \text{, } i_2(T_{on}) = \frac{3V_B}{3L_1 + L_2} - T_{on} \text{, } i_3(T_{on}) = \frac{3V_C}{3L_1 + L_2} - T_{on} \]  \hspace{1cm} (D-3)

\[ i_1(T_{on}) = \frac{V_A - V_B}{3L_1 + L_2} - T_{on} \text{, } i_2(T_{on}) = \frac{V_B - V_C}{3L_1 + L_2} - T_{on} \text{, } i_3(T_{on}) = \frac{V_C - V_A}{3L_1 + L_2} - T_{on} \]  \hspace{1cm} (D-4)

State 000

During this state all the switches are off and the inductors are transferring energy to the DC side. As it can be seen in Fig. 4.3 the boost and the flyback stages are running independently.

Boost stage.

While $T_{on} < t < t_1$ the $L_1$ inductor currents, as shown in Figs. 4.3, 4.4 and 4.5, have the following expressions:

\[ i_1(t) = \frac{3V_A}{3L_1 + L_2} - T_{on} + \frac{V_A - V_D}{L_1} - t \]  \hspace{1cm} (D-5)
It can be shown that the current in phase A reaches first zero, at a time $t_1$ as given by the following expression:

$$i_b(t) = \frac{3V_B}{3L_1 + L_2} - \frac{2V_D}{3L_1 + L_2} - t$$

$$i_c(t) = \frac{3V_C}{3L_1 + L_2} - \frac{V_D}{3L_1 + L_2} - t$$

The currents in the $L_1$ set of inductors reach the following values:

$$i_a(t_1) = 0$$

$$i_b(t_1) = \frac{3T_{ON}}{3L_1 + L_2} \frac{V_D(V_A - V_C)}{V_D - 3V_A}$$

$$i_c(t_1) = \frac{3T_{ON}}{3L_1 + L_2} \frac{V_D(V_C - V_A)}{V_D - 3V_A}$$

The current equations after $t_1$, i.e. $t_1 < t < t_2$ become:

$$i_a(t) = 0$$

$$i_c(t) = -i_a(t) = \frac{3T_{ON}}{3L_1 + L_2} \frac{V_D(V_C - V_A)}{V_D - 3V_A} + \frac{V_C - V_B - V_D}{2L_1} - t$$

The current reaches zero in all three phases at $t_2$:

$$t_2 = \frac{3T_{ON}}{3L_1 + L_2} \frac{V_D(V_C - V_A)}{V_D - 3V_A} + \frac{2L_1}{V_D + V_B - V_C}$$

In the interval $t_2 < t < T_{sw}$ no current flows in the inductors:

$$i_a(t_2) = i_b(t_2) = i_c(t_2) = 0$$

The total time in which current flows through inductors of the boost star stage is:
\[ T_{\text{sel-star}} = T_{\text{ON}} + t_1 + t_2 = T_{\text{ON}} \left( 1 + \frac{3L_1(V_C - V_B)}{(3L_1 + L_2)(V_D + V_B - V_C)} \right) \]  

Flyback stage.

While \( T_{\text{ON}} < t < t_3 \), the currents, as shown in Figures 3, 4 and 5, have the following expressions:

\[ i_A(t) = -\frac{3V_A}{3L_1 + L_2} T_{\text{ON}} + V_D \frac{t}{L_2} \]

\[ i_B(t) = -\frac{3V_B}{3L_1 + L_2} T_{\text{ON}} - 2V_D \frac{t}{L_2} \]

\[ i_C(t) = -\frac{3V_C}{3L_1 + L_2} T_{\text{ON}} + V_D \frac{t}{L_2} \]

\[ i_1(t) = \frac{V_A - V_B}{3L_1 + L_2} T_{\text{ON}} - V_D \frac{t}{L_2} \]

\[ i_2(t) = \frac{V_B - V_C}{3L_1 + L_2} T_{\text{ON}} + V_D \frac{t}{L_2} \]

\[ i_3(t) = \frac{V_C - V_A}{3L_1 + L_2} T_{\text{ON}} \]

It can be shown that the current in phase A reaches first zero. Consequently:

\[ t_2 = \frac{3V_A}{3L_1 + L_2} \frac{L_2}{V_D} T_{\text{ON}} \]

\[ i_A(t_2) = 0 \]

\[ i_C(t_3) = -i_B(t_3) = \frac{3T_{\text{ON}}(V_A - V_C)}{3L_1 - L_2} \]

\[ i_1(t_3) = i_3(t_3) = \frac{V_C - V_A}{3L_1 + L_2} T_{\text{ON}} \]

\[ i_2(t_3) = \frac{2V_A - 2V_C}{3L_1 + L_2} T_{\text{ON}} \]

The current equations after \( t_3 \) become:
\[ i_A(t) = 0 \]  
\[ i_C(t) = -i_B(t) = \frac{3T_{ON}(V_A - V_C)}{3L_1 - L_2} + \frac{3V_D}{2L_2} t \]  
\[ i_1(t) = i_2(t) = \frac{V_C - V_A}{3L_1 + L_2} T_{ON} - \frac{V_D}{2L_2} t \]  
\[ i_2(t) = \frac{2V_A - 2V_C}{3L_1 + L_2} T_{ON} + \frac{V_D}{L_2} t \]  

The current reaches zero in all three phases at \( t_A \):

\[ t_A = \frac{L_2}{3L_1 + L_2} \frac{2(V_C - V_A)}{V_D} T_{ON} \]  

\[ i_1(t_A) = i_2(t_A) = i_3(t_A) = 0 \]  

The total time in which current flows through inductors of the flyback stage is:

\[ T_{int-fy} = T_{ON} + t_3 + t_4 = T_{ON} \left( 1 + \frac{L_2(V_C - V_B)}{(3L_1 + L_2)V_D} \right) \]  

Phase currents

The instantaneous switching period is chosen as:

\[ T_{SW} = \max(T_{int-star}, T_{int-fy}) \]  

The averaged instantaneous phase currents for the interval \( (0, \pi / 6) \) are given by the following formulas:

\[ i_{a-av} = \frac{i_a(T_{ON})(T_{ON} + t_1)}{2T_{SW}} \]  
\[ i_{b-av} = \frac{i_b(T_{ON})(T_{ON} + t_1) + i_b(t_1)(t_1 + t_2)}{2T_{SW}} \]  
\[ i_{c-av} = \frac{i_c(T_{ON})(T_{ON} + t_1) + i_c(t_1)(t_1 + t_2)}{2T_{SW}} \]  

In phase A the current can be expressed for the interval \( (\pi / 6, \pi / 2) \) as:
Once the current in phase A has been determined for the interval \((0, \pi/2)\), the current for the whole period can be written as:

\[
i_a(\omega t) = i_a(\pi - \omega t), \quad \text{for} \quad \pi/2 < \omega t < \pi
\]  
\[
i_a(\omega t) = -i_a(\omega t - \pi), \quad \text{for} \quad \pi < \omega t < 2\pi
\]

Average current space vectors determination for the ‘Starfly’ PFC circuit

For the modulation at the beginning of the ON-interval, the space vectors are given in formulas \((D-28)/D-30)\) and the diagram of Fig. 3.15 is valid with the values given by \((D-31)/D-35)\).

\[
\left(\frac{di}{dt}\right)_{ABC} = \frac{\sqrt{3}(V_A - V_B)}{3L_1 + L_2} e^{-j\pi/6}
\]  
\[
\left(\frac{di}{dt}\right)_{ABC} = \frac{\sqrt{3}(V_C - V_A)}{3L_1 + L_2} e^{-j5\pi/6}
\]  
\[
\left(\frac{di}{dt}\right)_{ABC} = \frac{\sqrt{3}(V_B - V_C)}{3L_1 + L_2} e^{j\pi/2}
\]  
\[
I_1 = \frac{V_m}{L_1} \left[ \frac{3L_1}{3L_1 + L_2} T_{ON} \left( T_{ON} + 2t_1 + t_2 \right) + \frac{t_1(t_1 + t_2)}{2T_{SW}} \right]
\]  
\[
I_2 = \frac{\sqrt{3}(V_A - V_B)}{3L_1 + L_2} \frac{t_a(2T_{ON} + 2t_1 + t_2)}{2T_{SW}}
\]
\[ I_3 = \frac{\sqrt{3}(V_C - V_A) t_a (t_a + 2T_{ON} + 2t_1 + t_2)}{3L_1 + L_2} \frac{1}{2T_{SW}} \]  
\[ I_4 = \frac{\sqrt{3}(V_B - V_C) t_a (t_a + 2T_{ON} + 2t_1 + t_2)}{3L_1 + L_2} \frac{1}{2T_{SW}} \]  
\[ I_5 = \frac{2V_D}{3L_1} \frac{t_1 (t_1 + t_2)}{2T_{SW}} \]  

For the modulation at the end of the ON-interval, the space vectors are given in formulas (D-36/D-38) and the diagram of Fig. 3.5 is valid with the values given by (D-39/D-41).

\[ \frac{di}{dt}_{ABC} = \frac{3V_m}{3L_1 + L_2} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L_1 + L_2} e^{j\pi/3} \]  
\[ \frac{di}{dt}_{ABC} = \frac{3V_m}{3L_1 + L_2} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L_1 + L_2} e^{j2\pi/3} \]  
\[ \frac{di}{dt}_{ABC} = \frac{3V_m}{3L_1 + L_2} e^{j(\omega t - \pi/2)} + \frac{2V_D}{3L_1 + L_2} e^{j\pi} \]  

\[ I_1 = \frac{V_m}{L_1} \left[ \frac{3L_1}{3L_1 + L_2} \frac{(T_{ON} + t_a)(T_{ON} + t_a + 2t_1 + t_2)}{2T_{SW}} + \frac{t_1 (t_1 + t_2)}{2T_{SW}} \right] \]  
\[ I_2 = \frac{2V_D}{3L_1 + L_2} \frac{t_a (t_a + 2t_1 + t_2)}{2T_{SW}} \]  
\[ I_3 = \frac{2V_D}{3L_1} \frac{t_1 (t_1 + t_2)}{2T_{SW}} \]
APPENDIX E

Determination of the currents in the Star-Delta PFC circuit operating in Discontinuous Conduction Mode

The general equations describing the evolution of the current in the boost inductors and the rectifying bridges legs are given below:

\[ \frac{di_a}{dt} = \frac{di_b}{dt} + \frac{di_c}{dt}, \quad \frac{di_{b2}}{dt} = \frac{di_b}{dt} = \frac{di_c}{dt} = \frac{di_{c3}}{dt} \]  \hspace{1cm} (E-1)

\[ i_{ja} = \frac{di_j}{dt} t_{ON}, \quad i_{ja} = i_{ja} + \frac{di_j}{dt} t_6, \quad i_{ja} = i_{ja} + \frac{di_j}{dt} t_5, \]  \hspace{1cm} (E-2)

\[ i_{ja} = i_{ja} + \frac{di_j}{dt} t_4, \quad i_{ja} = i_{ja} + \frac{di_j}{dt} t_3, \quad i_{ja} = i_{ja} + \frac{di_j}{dt} t_2. \]  \hspace{1cm} (E-3)

\[ \frac{di_j}{dt} \text{ varies with the interval.} \]

\[ j \in \{a, b, c, 1, 2, 3, a1, b2, c3\} \]

\[ T_{on} = T_{ON} + t_6 + t_4 + t_2 \]  \hspace{1cm} (E-4)

\[ T_{sw} = \max(T_{on}) \]

\[ i_{ja}, \text{ } = \frac{1}{T_{sw}} \left( \frac{0 + i_{ja} T_{ON}}{2} + i_{ja} + t_6 + \frac{i_{ja} + i_{ja} t_6}{2} + i_{ja} + \frac{i_{ja}}{2} t_4 + \frac{i_{ja} + i_{ja} t_4}{2} t_2 \right) \]  \hspace{1cm} (E-5)

Immediately after turning off the switches, there are six diodes conducting, three in each bridge. They eventually come out of conduction, one by one, changing the current slope of the inductors. The inductance and voltage transfer ratios are determining the set of equations that can be written, and consequently the current evolution. A visual representation of the current in the input inductors is given in Fig. 4.32, based on a time domain simulation with the values given in Section 4.3.

The analysis starts by determining which diodes are conducting at the end of the ON-interval. Table E-1 shows that information for the analyzed interval. As an example of the current evolution, when an inductor of the \( L_z \) set has diodes at both ends conducting onto the same bus, the voltage across it is zero, and its current maintains a constant value. It is identified which possible sequence of diodes coming out of
conduction can occur. This is based on the calculation of the times in which the current in the rectifier bridges legs would reach zero, for a given set of equations. Then the minimum time is determined, and the new set of equations, characteristic to the new current flow is written. The possible states are identified with letters and figures, where the latter shows the number of diodes in conduction. In Table E-2 the times which lead to the occurrence of each state are given. The complete set of equations for each particular state is given in Tables E-3 and E-4.

<table>
<thead>
<tr>
<th>Currents</th>
<th>Phase Angle</th>
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<tbody>
<tr>
<td>Diode bridge 1</td>
<td>(0, π/6)</td>
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<tr>
<td>Diode bridge 2</td>
<td>(π/6, π/3)</td>
</tr>
<tr>
<td>Phase</td>
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</tr>
<tr>
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</tr>
<tr>
<td>(i_b(T_{ON}))</td>
<td>-</td>
</tr>
<tr>
<td>(i_c(T_{ON}))</td>
<td>+</td>
</tr>
</tbody>
</table>

In the following, based on the application of the general equations, the time length for each interval is given.

Interval \((0, T_{ON})\)

\[
i_a(T_{ON}) = \frac{3V_A}{3L_1 + L_2} T_{ON}, \quad i_b(T_{ON}) = \frac{3V_B}{3L_1 + L_2} T_{ON}, \quad i_c(T_{ON}) = \frac{3V_C}{3L_1 + L_2} T_{ON}
\]

(E-6)

Interval \((T_{ON}, T_{ON} + t)\)

\[
i_a(t) = i_a(T_{ON}) + \frac{di_a}{dt} t, \quad i_b(t) = i_b(T_{ON}) + \frac{di_b}{dt} t, \quad i_c(t) = i_c(T_{ON}) + \frac{di_c}{dt} t
\]

(E-9)
\[ i_1(t) = i_1(T_{ON}) + \frac{di_1}{dt} t, \quad i_2(t) = i_2(T_{ON}) + \frac{di_2}{dt} t, \quad i_3(t) = i_3(T_{ON}) + \frac{di_3}{dt} t \]  
(E-10)

\[ i_{a1}(t) = i_a(t) - i_1(t) = i_a(T_{ON}) - i_1(T_{ON}) + \left( \frac{di_a}{dt} - \frac{di_1}{dt} \right) t \]  
(E-11)

\[ i_{b2}(t) = i_b(t) - i_2(t) = i_b(T_{ON}) - i_2(T_{ON}) + \left( \frac{di_b}{dt} - \frac{di_2}{dt} \right) t \]  
(E-12)

\[ i_{c3}(t) = i_c(t) - i_3(t) = i_c(T_{ON}) - i_3(T_{ON}) + \left( \frac{di_c}{dt} - \frac{di_3}{dt} \right) t \]  
(E-13)

It is mathematically shown that:

\[ t_1 = \frac{2V_A + V_B}{3L_1 + L_2} \left( \frac{1}{\frac{3V_A + V_B}{3L_1} - \frac{V_B}{L_2}} \right) \]  
(E-14)

for which:

\[ i_a(t_1) = 0 \]

Interval \((T_{ON} + t_1, T_{ON} + t_1 + t_2)\)

\[ t_2 = \min \left\{ \frac{i_{b2}(T_{ON} + t_1)}{-\frac{di_{b2}}{dt}}, \frac{i_a(T_{ON} + t_1)}{-\frac{di_a}{dt}} \right\} \]  
(E-15)

Interval \((T_{ON} + t_1 + t_2, T_{ON} + t_1 + t_2 + t_3)\)

If:

\[ \frac{i_{b2}(T_{ON} + t_1)}{-\frac{di_{b2}}{dt}} < \frac{i_a(T_{ON} + t_1)}{-\frac{di_a}{dt}} \]

\[ t_3 = \min \left\{ \frac{i_{c3}(T_{ON} + t_1 + t_2)}{-\frac{di_{c3}}{dt}}, \frac{i_a(T_{ON} + t_1 + t_2)}{-\frac{di_a}{dt}} \right\} \]  
(E-16)

If:

\[ \frac{i_{b2}(T_{ON} + t_1)}{-\frac{di_{b2}}{dt}} > \frac{i_a(T_{ON} + t_1)}{-\frac{di_a}{dt}} \]
\[ t_5 = \min \left\{ \frac{i_2(T_{ON} + t_1 + t_2)}{-\frac{di_2}{dt}}, \frac{i_3(T_{ON} + t_1 + t_2)}{-\frac{di_3}{dt}} \right\} \]

Interval \((T_{ON} + t_1 + t_2 + t_3, T_{ON} + t_1 + t_2 + t_3 + t_4)\)

If: \(\frac{i_3(T_{ON} + t_1 + t_2)}{-\frac{di_3}{dt}} > \frac{i_a(T_{ON} + t_1 + t_2)}{-\frac{di_a}{dt}}\)  \hspace{1cm} (E-16)

\[ t_4 = \min \left\{ \frac{i_3(T_{ON} + t_1 + t_2 + t_3)}{-\frac{di_3}{dt}} \right\} \]

If: \(\frac{i_3(T_{ON} + t_1 + t_2)}{-\frac{di_3}{dt}} < \frac{i_a(T_{ON} + t_1 + t_2)}{-\frac{di_a}{dt}}\)  \hspace{1cm} (E-17)

\[ t_4 = \min \left\{ \frac{i_a(T_{ON} + t_1 + t_2 + t_3)}{-\frac{di_a}{dt}}, \frac{i_c(T_{ON} + t_1 + t_2 + t_3)}{-\frac{di_c}{dt}} \right\} \]

If: \(\frac{i_2(T_{ON} + t_1 + t_2)}{-\frac{di_2}{dt}} < \frac{i_3(T_{ON} + t_1 + t_2)}{-\frac{di_3}{dt}}\)  \hspace{1cm} (E-18)

\[ t_4 = \min \left\{ \frac{i_3(T_{ON} + t_1 + t_2 + t_3)}{-\frac{di_3}{dt}} \right\} \]

If: \(\frac{i_2(T_{ON} + t_1 + t_2)}{-\frac{di_2}{dt}} > \frac{i_3(T_{ON} + t_1 + t_2)}{-\frac{di_3}{dt}}\)  \hspace{1cm} (E-19)

\[ t_4 = \min \left\{ \frac{i_2(T_{ON} + t_1 + t_2 + t_3)}{-\frac{di_2}{dt}} \right\} \]
Interval \((T_{ON} + t_1 + t_2 + t_3 + t_4, T_{ON} + t_1 + t_2 + t_3 + t_4 + t_5)\)

\(t_5 = \min \left\{ \frac{i_s (T_{ON} + t_1 + t_2 + t_3 + t_4)}{-\frac{di_s}{dt}} \right\} \) \hspace{1cm} (E-20)

Interval \((T_{ON} + t_1 + t_2 + t_3 + t_4 + t_5, T_{SW})\)

The current in all inductors is zero.
Table E.2 Coordination Table Star-Delta

Interval \((0, \pi/6)\)

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Interval \((\pi/6, \pi/3)\)

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164
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**Table E.3.** Example of a three-phase circuit for the AC/DC circuit (E.3/6).
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Title: E. Tabellarische Konstruktion der quasidiskreten Eichung (\( \gamma / \gamma \))
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APPENDIX F

Determination of the currents in the Delta-Delta PFC circuit operating in Discontinuous Conduction Mode

The general equations describing the evolution of the current in the boost inductors and the rectifying bridges legs are given below:

\[
\begin{align*}
\frac{di_{i4}}{dt} &= \frac{di_{i1}}{dt} - \frac{di_{i4}}{dt} \\
\frac{di_{i25}}{dt} &= \frac{di_{i2}}{dt} - \frac{di_{i36}}{dt} \\
\frac{di_{i3}}{dt} &= \frac{di_{i1}}{dt} - \frac{di_{i6}}{dt}
\end{align*}
\]  \hspace{1cm} (F-1)

\[
\begin{align*}
i_{j6} &= \frac{di_{j6}}{dt} T_{ON} \\
i_{j6} &= i_{j6} + \frac{di_{j6}}{dt} t_6 \\
i_{j6} &= i_{j6} + \frac{di_{j6}}{dt} t_5
\end{align*}
\]  \hspace{1cm} (F-2)

\[
\begin{align*}
i_{j6} &= i_6 + \frac{di_{j6}}{dt} t_4 \\
i_{j6} &= i_6 + \frac{di_{j6}}{dt} t_3 \\
i_{j6} &= i_6 + \frac{di_{j6}}{dt} t_2
\end{align*}
\]

\[
\frac{di_{j}}{dt} \text{ varies with the interval.}
\]

\[
j \in \{1,2,3,4,5,6,14,25,36\}
\]

The analysis is carried out in a similar way as for the Star-Delta circuit in Appendix E. For this reason only the equations are given here, while the procedure remains the same.

The currents immediately after turn-off of the switches are given by the following formulas:

\[
i_1(T_{ON}) = \frac{V_A - V_B}{L_1} T_{ON}, \hspace{0.5cm} i_2(T_{ON}) = \frac{V_B - V_C}{L_1} T_{ON}, \hspace{0.5cm} i_3(T_{ON}) = \frac{V_C - V_A}{L_1} T_{ON}
\]  \hspace{1cm} (F-3)

\[
i_4(T_{ON}) = \frac{V_B - V_C}{L_2} T_{ON}, \hspace{0.5cm} i_5(T_{ON}) = \frac{V_C - V_A}{L_2} T_{ON}, \hspace{0.5cm} i_6(T_{ON}) = \frac{V_A - V_B}{L_2} T_{ON}
\]

\[
i_4(T_{ON}) = 3V_A \left( \frac{1}{L_1} + \frac{1}{L_2} \right) T_{ON}, \hspace{0.5cm} i_5(T_{ON}) = 3V_B \left( \frac{1}{L_1} + \frac{1}{L_2} \right) T_{ON}, \hspace{0.5cm} i_6(T_{ON}) = 3V_C \left( \frac{1}{L_1} + \frac{1}{L_2} \right) T_{ON}
\]  \hspace{1cm} (F-4)

\[
i_4(T_{ON}) = \left( \frac{V_A - V_B - V_C}{L_1} \right) T_{ON}, \hspace{0.5cm} i_5(T_{ON}) = \left( \frac{V_B - V_C - V_A}{L_1} \right) T_{ON}, \hspace{0.5cm} i_6(T_{ON}) = \left( \frac{V_C - V_A - V_B}{L_1} \right) T_{ON}
\]  \hspace{1cm} (F-5)

The analysis starts by determining which diodes are conducting at the end of the ON-interval. Table E.5 shows that information for the analyzed interval.
Table F.1 Sign of the current in the phase and diode bridges for the Delta-delta circuit. Interval \((0, \pi/3)\).

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<th>Inductance ratio</th>
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<th>Diode bridge 2 currents</th>
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The determination of the angles \(\alpha\) and \(\beta\) is given in the following:

\[
0 \leq \alpha \leq \pi/6, \quad \frac{L_1}{L_2} \leq 1, \quad i_{a6} \geq 0
\]

\[
\frac{V_c - V_A}{L_1} - \frac{V_A - V_B}{L_2} \geq 0 \quad \tan \alpha \leq \frac{\sqrt{3} L_2 - L_3}{3 L_2 + L_1} \tag{F-6}
\]

\[
\pi/6 \leq \beta \leq \pi/3, \quad \frac{L_1}{L_2} \geq 1, \quad i_{a5} \leq 0
\]

\[
\frac{V_B - V_C}{L_1} - \frac{V_C - V_A}{L_2} \leq 0 \quad \tan \beta \leq \frac{\sqrt{3} L_2 + 2L_2}{3 L_1} \tag{F-7}
\]

Check-up:

\[
L_1 = L_2
\]

\[
\tan \alpha = 0, \quad \alpha = 0
\]

\[
\tan \beta = \sqrt{3}, \quad \beta = \pi/3
\]

Once the initial current flow has been determined, the sequence of rectifying diodes going out of conduction will be identified with the help of MATLAB. For this purpose all possible states are identified with letters and figures, where the latter shows the number of diodes in conduction. In Table E.6 the times which lead to the occurrence of each state are given. The complete set of equations for each particular state is given in Tables E.7 and E.8.
Table F.2 Coordination Table Delta-Delta.

**Interval \((0, \pi/6)\)**

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172
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APPENDIX G

List of components and equipment for testing the boost-delta PFC circuit operating in Discontinuous Conduction Mode

Power Circuit (Figs. 6.1 and 6.2)

D1-D12: IXYS DSEI 30-06A, 30A/600V

SW1-SW6: see Bi-directional switch parts list

C1-C6: 8 μF/250Vac, 4 parallel 2 μF/250Vac, NISSEI C44205*400B

C7: 4,480 μF/450V, 8 parallel CORNELL DUBILIER 560 μF/450V, 380561 P450 A062


L4-L6, L10-L12: 180 μH, Core MAGENTICS toroid 77083-A7, Cool Mu 60, Copper 45 turns of 6 twisted strands of #26AWG

R1: 47.7/24.4Ω, 10 pcs. parallel connected resistor 500Ω/225W, OHMITE L225 J500. For the two parallel running circuits the following load is parallel connected with the one above: 8 pcs. series connected 6Ω/180W, PACIFIC 180CHN.

Bi-directional switch (Fig. 6.3)

T1-T2: INTERNATIONAL RECTIFIER IRFP 460, 20A/500V

C1-C2: SPRAGUE 1nF/1KV, X7R 10%

D1-D2: MOTOROLA MUR160, 1A/600V

R1-R2: 2 parallel IRC GS3-330, 330Ω/3W, 5%

Gate Driver (Fig. 6.4)

C1: 10 μF/50V; C2: 0.33 μF/25V; C3-C4: 1 μF/35V; R1-R2: 220Ω/0.5W; R3-R4: 10 kΩ/0.25W; R5-R8: 18.6Ω/0.25W; D1-D2: 1N4148; D3-D4: 1N4746 ZENER 18V; T1-T6: RFD14NO5
Tr1: Gating transformer, Core: E2425, Material 3C8, MAGNETICS P42510-EC, Copper: Primary 30 turns #26 AWG, 4 Secondaries 18 turns #26 AWG, Bobbin: E2425 Bobbin PC Mount, MAGNETICS PC-B2510-T1

PWM Circuit (Fig. 6.5)

R1, R5: 10kΩ /0.25W; R2: 2 kΩ /0.25W; R3-R4: 100kΩ /0.25W; R6: 38kΩ /0.25W; R7-R8: 392Ω /0.25W; R9-R12: 3.32Ω /0.25W; P1: 1kΩ ; P2: 10 kΩ ;

C1: 680 pF/25V; C2, C3, C5, C7, C8, C10, C12: 0.33 µF/25V; C4-, C6, C9, C11: 10 µF/50V

D1-D2: MUR160; IC1: THOMPSON SGS 3524A; IC2-IC3: INTERNATIONAL RECTIFIER IR 2110.

Instruments and equipment used for the measurements:

Scope: TEKTRONIX Two Channel, Digital Real-Time Oscilloscope, 100 MHz.

Power Analyzer: YOKOGAWA WT130, Digital Power Meter, Measuring Range 600V/20A, 3 phase

Meter: METEX M-4650

Current Probe: AM503 TEKTRONIX Probe Amplifier

Step-down isolation transformer: 600V/480V, REX MANUFACTURING 45 KVA

Variable auto transformer: 480V/0-560V, SUPERIOR ELECTRIC 30 KVA