TANTALUM PENTOXIDE, A NON CONVENTIONAL

GATE INSULATOR FOR MOS DEVICES

by

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ABSTRACT

Non conventional gate insulators for MOS devices are generally dielectrics that depart considerably from the classic SiO_2 used extensively in this technology. The work presented here reflects the research and development of an existing compound, Ta_2O_5, and its application as a gate insulator for both MOS capacitors and transistors. The oxide is grown both thermally and anodically from pure sputtered tantalum metal over silicon wafers. Succesful dielectrics suitable for gate insulators were obtained using both methods. High relative permittivity ($\simeq 26$-28) being characteristic of tantalum pentoxide, offers considerable advantage over classic silicon dioxide gate insulators, however higher leakage currents (100 to 1000 times greater) were encountered in MOS Capacitor samples at room temperature. A method for processing the tantalum metal was developed using the liftoff technique, and it was successfully applied to both MOS capacitors and field effect transistors. Furthermore, devices were fabricated in the form of MOS Transistors, which exhibited good Id vs. Vds characteristics, with Vgs as a parameter. Gate leakage currents were low, as a double dielectric Ta_2O_5 over SiO_2 structure was used as gate insulator. A small signal model of this class of devices is presented, that takes into account the non zero gate leakage current. Another successful technique, interfacial oxidation of Ta_2O_5 over Si, was used in fabricating MOS Capacitors that yielded also low leakage currents and high specific capacitances.

The purpose of this Thesis is to report the development at the University of British Columbia of the double gate insulator MOSFET technology based on the Tantalum Pentoxide-Silicon Dioxide (Ta_2O_5/SiO_2) heteromorphic structure.

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possible. To all them, I express my deep indebtedness. I dedicate this work to a man that fought many battles in life, but heroically lost the last one: my father.

CHAPTER 1

INTRODUCTION

The term non-conventional dielectrics is used to
describe those which depart considerably from the classic
SiO_2 used in MOS technology as gate insulators, device
isolation, diffusion masking, implant resist and general
surface passivation. Notwithstanding the natural advantages
of the silicon dioxide, numerous authors have followed
research in alternate dielectrics suitable for use in MOS
devices. In the present work, one of such non-conventional
insulators is used, namely Tantalum Pentoxide (Ta_2O_5),
either obtained by thermal or anodic oxidation of tantalum
metal to form MOS capacitors and field effect devices on
silicon substrates.

Large Scale, Very Large Scale Integrated and future
Ultra Large Scale Integrated Circuits will require
technologies and devices capable of performing when scaled
down to 1 micron features and beyond, in order to achieve
the large number of devices per dice (>300,000) if this
microtechnology is to be successful. At this present time
(early 1984), major problem areas seem to have not been
resolved yet, namely the solution to electromigration
induced failures, in which the ions that form the
interconnecting metal lines (usually Aluminium) are
transported by the extremely high current densities, i.e.,
"electron wind", of typically 10,000 A/cm^2 [Black, 1969];
and the subthreshold conduction in MOS transistors, in which

the device does not turn off, i.e., a small, but non-zero drain current still flows despite of the efforts of the applied gate voltage to do so [Troutman, 1974]. The latter is particularly critical to the operation of circuits where low leakage (the device is in the cutoff or OFF condition) currents are required. The subthreshold currents do not scale properly and this presents a problem for very small devices [Dennard et al., 1974]. As a consequence, the reduction of the subthreshold effect is of great importance in attaining successful devices for VLSI and ULSI.

The high permittivity dielectrics presently used in gate insulators for Metal Oxide Semiconductor Field Effect Transistors (MOSFET's) have definitive advantages. A close examination of the equations [Sze, 1969] that relate the drain current with its geometry, threshold voltage and drain voltage, reveals that the former is in direct relation with the insulator relative dielectric constant. A similar effect, and perhaps the most important, is on the device transconductance gm: it is also directly proportional to the gate insulator dielectric constant. Another important parameter, the threshold voltage, is reduced by about the same factor, which is crucial in the design of MOS transistors for analog (linear) applications. The channel conductance, suffers a more complicated change, as it depends on both insulator capacitance (which increases with the dielectric constant) and on the threshold voltage (which decreases). It can be said then, that a general improvement

on the MOSFET device performance can be accomplished by the use of high permittivity gate insulators. Tantalum pentoxide (Ta_2O_5) has a relative dielectric constant of 27, about seven times larger than silicon dioxide (SiO_2). Therefore, in theory, a sevenfold increase in performance should be expected. Because of its negative interface charge density, Ta_2O_5 can help in further reducing the gate threshold voltage [Seki et al., 1984]

Another promising application is in avoiding the gate insulator breakdown by either the internal fixed charge generated field, or the one caused by the application of a gate voltage to the classic gate oxide. As the device is scaled down in its three dimensions, the gate insulator thickness is reduced by the same factor K, hence limiting the maximum applied gate voltage by oxide breakdown. The applied gate voltage has then a lower bound, the turn-on voltage, and a higher bound, the insulator breakdown voltage. This situation can be avoided, if a double dielectric structure is used instead of the single layer, silicon dioxide gate insulator [Angle and Talley, 1978]. If a thick layer of high dielectric constant material (i.e., tantalum pentoxide) is deposited over a thin layer of low dielectric constant material (i.e., silicon dioxide), the latter is protected from breakdown fields, as most of the voltage drop across the compound dielectric will appear in the higher permittivity material, the thicker tantalum pentoxide.

In the double insulator structure, the probability of
pinholes coinciding in the same location is vanishingly
small, thus producing a much better quality insulator.
Amorphous silicon dioxide is structurally porous and has
high permeability to water vapour and migration of alkali
ions. By applying a second outer dielectric onto the inner
one, these effects can be reduced. Tantalum pentoxide has a
much denser structure, and possibly retards the ion
migration. The double dielectric insulating structure is
used in the present work as the gate insulator for both
MOSFET and MOS capacitor devices. The successful devices
proved to be functional transistors, with moderate
transconductance and fast switching pulse response. The MOS
capacitors have good C-V curves and low leakage currents.

It is quite possible that the single dielectric high
permittivity insulator and the double dielectric structure
have direct application in future VLSI and ULSI
technologies. Already, the high dielectric constant tantalum
pentoxide has found use in a VLSI 256/512 kbit dynamic
Random Access Memory (RAM), which aims towards the 1 Mbit
memory Integrated Circuit [Ohta et al., 1980].

The purpose of this Thesis is to present the
measurements and results obtained from experimental MOS
Capacitors fabricated with anodic and thermal tantalum
pentoxide; and from the experimental MOSFET's utilizing a
double dielectric (Ta_2O_5) gate insulator structure, in which
the tantalum oxide was obtained by thermal and anodic

processes.

This Thesis is divided into eight chapters and four appendices. The second chapter contains an overview of the previous work done by several authors in this field. In the third chapter, the theory of the double dielectric insulator is presented, as later on a device will be developed around this technology. The fourth and sixth chapters contain all the information related to the processing of the MOS capacitor and double dielectric device. In the fifth chapter, the measurements performed on the MOS capacitors and results are presented. The seventh chapter contains the measurements made on the double dielectric MOSFET's (MTAOS devices) and the results obtained. In chapter eight, the summary and conclusions of this work are presented.

CHAPTER 2

AN OVERVIEW OF NON CONVENTIONAL INSULATORS

A large number of authors have reported many different properties of non conventional dielectrics. In this chapter, I have attempted to present a summary of published works on the subject. These cover thin and thick films of several compounds used as dielectrics in a non conventional way.

Despite early difficulties in obtaining good counter electrode contacts, successful tantalum pentoxide thin films were first obtained by anodic oxidation of sputtered tantalum metal [Berry and Sloan, 1959], to be used in low value capacitors for printed circuits. Typical capacitance densities of 10 nF/mm^2 and capacitances of 30 nF with leakage currents of 10-100 nA were obtained for samples made on ceramic substrates. Thin films of anodically oxidized aluminium were also produced for the same application and a certain degree of simplicity over the tantalum version was claimed, since Al metal was evaporated instead sputtered and the same was used as contact and for anodic dielectric formation [Huber and Haas, 1960].

A detailed study of the anodic oxides of the so called "valve metals", i.e., the electrolytically formed oxides of Ta, Nb, Al, Zr, Hf, W, Bi, Sb and others, was given concisely in book form by Young in 1961, with great attention devoted to tantalum and the properties of its thin film oxides.

Anodically grown thin films of silicon oxide (SiO), aluminium oxide (Al_2O_3), tantalum pentoxide (Ta_2O_5), zirconium oxide (ZrO_2) and titanium oxide (TiO_2) were fabricated, using evaporation techniques for evaluating their conduction and negative resistance at low frequencies (60 Hz); although the application was not intended for MOS devices, but rather in switching and rectifying [Hickmott, 1962].

A study done on a Metal-Insulator-Metal (MIM) structure of the form Ta-Ta_2O_5-Au revealed that the electronic transport mechanism obeys an Ohmic characteristic at low fields and that at high fields it follows a Poole-Frenkel type emission at room temperatures. At high fields and low temperatures (i.e. 77K), the electronic conduction is governed by a Fowler-Nordheim type emission. Measurements gave an activation energy of 0.1 eV. A discontinuity in the oxide properties was noted around 50 nm [Mead, 1962].

A rather unusual current-voltage characteristics was observed for niobium, titanium and tantalum oxides, when prepared as thin films and their oxides obtained by the thermal process. Regions of negative resistance are found to be current controlled, as opposed to the voltage controlled negative resistance of the Tunnel (Esaki) diode [Chopra, 1963].

Thin film circuits using resistors made of tantalum nitride (TaN) and capacitors made of anodic tantalum oxide were successfully applied in creating the first hybrid circuits, i.e., incorporating discrete bipolar transistors

to a common ceramic substrate, in making both analog and digital circuits [Berry, 1963]. Later a method for producing high value resistors was developed, by sputtering tantalum in a partial atmosphere of argon and oxygen [Pendergast, 1963]. Furthermore, a production style open ended vacuum system for deposition of tantalum films for manufacturing resistors was reported to make 4 million square inches of metal film per year-shift [Balde, Charschan and Dineen, 1964].

Reactive sputtering of tantalum metal with subatmospheric partial pressure gas pressures was used to deposit films of tantalum nitride (TaN), tantalum pentoxide (Ta_2O_5), tantalum carbide (TaC and Ta_2C) titanium nitride (TiN) and oxides (TiO_2), Niobium Nitrides (NbN and Nb_2N); for the fabrication of two dimensional hybrid thin film circuits. It was noted that the introduction of Oxygen as a reactive component, had a drastic effect in the electrical properties of the sputtered films. By controlling its partial pressure, reproducible values of sheet resistivity were obtained. It was found that most nitrides and carbides have superconducting properties and that niobium nitride, NbN, has one of the highest transition temperatures [Gerstenberg, 1964].

The discovery of beta tantalum [Read and Altmann, 1965] sparked more interest in the research of thin films made of this material, as it offered improved electrical properties over its predecessors. It has higher resistivity, a smaller temperature coefficient of resistance and its

superconducting transition temperature is much less. Beta tantalum is formed in a sputtering system when an atmosphere of argon is introduced at a partial pressure of 10 to 30 mTorr and the total pressure (i.e., vacuum quality) of the other gases is 10 μTorr. It was found that a conversion to normal tantalum (body centered cubic structure) takes place, when beta tantalum (tetragonal) is heated in vacuum to about 750 C.

Evidence of photoelectric properties has been found for films made of Nb_2O_5 over metal substrates, as knowledge of the conduction mechanism through the oxide film can be obtained by photoresponse studies [Hickmott, 1966]. Electronic photoconduction is also found in thin films of Ta_2O_5, with sharp increases of conduction current when irradiated with ultraviolet light, in which the increase in current was found to be approximately proportional to the intensity of the light [Young, 1961]. A thin film photocell, using thermally oxidized niobium metal, has been fabricated, and it was found that a linear relation exists between the photocurrent and light intensity, as experimental measurements indicated. However, the transient response is very slow (50-100 sec) and the conversion efficiency is two orders of magnitude below the conventional junction type silicon cells. For Ta and Ti anodic oxides a linear relation exists between photocurrent and photovoltage, although such a characteristic is not desirable in a practical photocell [Chopra and Bobb, 1963].

Chemical vapour deposition techniques (CVD) have been

applied to the fabrication of MOS capacitors, in which films of TiO_2, Ta_2O_5 and Nb_2O_5 were obtained by pyrolysis of the appropiate organo-metal compound. Lead oxide (PbO) films were also deposited, using the same CVD techniques, for use in Vidicons. A wide range of substrates, from silicon to platinum was used [Wang, Zaininger and Duffy, 1970].

Bismuth titanate films ($Bi_4Ti_3O_{12}$) with a very high relative permittivity ($\simeq 160$) have been reported for use in Metal-Insulator-Metal capacitors, in spite of the stoichiometry control problems in the sputtering of this compound. High dissipation factors which depend strongly on frequency and heavy conduction currents were found [Szedon and Takei, 1971].

Tantalum pentoxide (Ta_2O_5) thin films have been considered for application as dielectrics for Microwave Integrated Circuits (MIC's), due to its high relative dielectric constant and moderately high Q ($\simeq 100$) at microwave frequencies. The so called Tantalum System dielectrics for MIC's are based on metal sputtering and later anodic oxidation on an alumina substrate technologies. The guide wavelength λg can be reduced, and the degree of size reduction as well as integration can be increased, if the relative dielectric constant of the substrate is made larger. This is determined by the effective dielectric constant ϵeff, which is a direct function of the relative dielectric constant ϵr of the substrate. Hence, by using substrates with large ϵr (i.e. Ta_2O_5), a larger degree of integration and size reduction can be achieved [Caulton,

1971].

A rather unorthodox approach to a non-conventional gate insulator was applied to a MOSFET voltage divider, in which the gate electrode is made to slide over silicone oil (later glycerine), with the gate oxide being underneath. This formed a capacitive voltage divider, with the MOSFET drain current being a function of the movable gate electrode position [Okamoto and Ugai, 1971].

Thermal oxidation of sputtered tantalum metal over silicon was made feasible in the form of a Si-Ta and Si-Ta-Al structures, placed under heat treatment in different atmospheres of N_2/O_2 and N_2/H_2O mixtures. The kinetics of oxygen incorporation show an approximate square root dependence with time. It was reported that the Ta-Si interface exhibited negligible interdiffusion when annealed. Because of the relatively low temperature process used (525 C), it is said that the tantalum thin films are technologically compatible with the Silicon System. This is due to the stability shown by silicon, the Si-SiO_2 interface and aluminium metal at this temperature [Croset and Velasco, 1971].

A thin film capacitor of silicon dioxide over tantalum pentoxide has been successfully fabricated, in which SiO_2 was sputtered over anodized Ta_2O_5 over a ceramic substrate. The capacitance density is dominated by the silicon dioxide film, because of its smaller dielectric constant as compared with anodic tantalum oxide. This gave a high degree of reproducibility, as the desired capacitance density of the

SiO_2/Ta_2O_5 thin film capacitor is controlled by the thickness of the silicon dioxide film. The temperature coefficient of capacitance (TCC) can be adjusted to compensate the negative temperature coefficient of resistance (TCR) of tantalum nitride resistors (used in RC networks based on the Tantalum System), by proper selection of the silicon dioxide thickness [Sato, Sato and Okamoto, 1973].

Thermal oxidation of tantalum films deposited by electron beam evaporation on silicon, have been prepared in order to study the Si-Ta-{Ta oxide} structure. The criteria of a maxima in the oxide's apparent refractive index was used in deciding the complete oxidation of the tantalum metal. The elapsed time for this maximum value is the oxidation time of the film. It was concluded that some interaction with the Si substrate ocurred during the oxidation of the Ta film, namely the co-oxidation of a small, but non-zero amount of silicon. This interaction at the Si-Ta interface has actually moved into the Si crystal, in a similar fashion as the Si-SiO_2 interface when thermal oxidation takes place. It was claimed that the properties of the oxide film and the Si-{Ta oxide} interface can be controlled by the Si/Ta ratio in the oxide film [Revesz, Allison, Kirkendall and Reynolds, 1974].

An interesting insulator structure is made using evaporated oxide films of tungsten (WO_3) and molybdenum (MoO_3) oxides, sandwiched between orthogonally evaporated Al electrodes. It was established that a Schottky type barrier

exists between the contacts and oxide by verifying the linearity of the $1/C^2$ versus applied voltage plot and it was concluded that a compound barrier, i.e., an insulating layer adjacent to a space charge layer exists between the oxide film and the electrode [Padmanabhan and Sathianandan, 1975].

Another use of tantalum pentoxide is in the field of antireflection coatings for silicon solar cells, since its refractive index (2.23) is very close to the optimum value of 2.3 required in this application. The thermal oxidation of tantalum is a low temperature process that results in a noncrystalline oxide with a Silicon-{Ta oxide} structure of high perfection. This is of great importance if a high quantum yield is desired at short wavelengths, as with a good interface, the carriers generated in its surroundings reach the n-p junction without recombination. Niobium pentoxide has also similar properties with a refractive index of 2.37, close to the optimum [Revesz, Allison and Reynolds, 1976].

MOS capacitance measurements using the C-V plot techniques are helpful in determining the characteristics of the semiconductor- oxide interface, as the density of interface states can be obtained in various ways, in particular by the Terman method [Sze, 1969]. Thermally oxidized samples of sputtered tantalum have been prepared for this purpose, and observing the final oxide thickness, it gave twice that of the original film. It was noted that annealing in forming gas (N_2/H_2 mixture), reduced the density of interface states by a factor of 4, while the

oxide charge remained fixed and negative [Revesz and Allison, 1976].

Ellipsometric observations of the optical properties of thermally oxidized Ta_2O_5 on silicon have shown that a gradient in the optical refractive index exists at the substrate-oxide interface and that the index actually increases slightly from its Si-Ta_2O_5 boundary towards the outer end of the oxide. The existence of this refractive index gradient is somewhat controversial, as in its actual measurement, a thin ($\simeq 10$ nm) layer of oxide was etched at a time, and its index measured by ellipsometry using a multilayer model. Measurements performed on a GaAs substrate show that a gradient with opposite slope exists, as compared with the silicon substrate case. Hence, the gradient in the refractive index (and its slope) of the Ta oxide depends largely on the substrate were they are grown [Revesz, Reynolds and Allison, 1976].

Chemical Vapour Deposition (CVD) is a technique by which an organo-metallic compound is deposited by pyrolysis with the assistance of a carrier gas, usually a mixture which contains oxygen among others. Tantalum pentoxide films have been deposited using this method, with the advantage of being a low temperature (300-500 C) process, that results in oxides with amorphous structures, similar to the thermally grown tantalum oxides. The disadvantages of this approach are mainly in the vast complexity of the deposition equipment and the availability of a suitable tantalum organic compound. Films deposited by CVD show smooth

surfaces and good adhesion, with an index of refraction close to 2.3 and an optical bandgap of 4.4 eV. Capacitance measurements gave a relative dielectric constant of 22-25 and C-V plots indicated that there was no difference among three different crystal orientations of p-silicon substrates, all showing no hysteresis. Some distortion of the C-V curves was attributed to fast surface states. The conduction mechanism at DC was established to be bulk limited, with a Poole-Frenkel emission at low current densities and space charge limited at higher densities. A Schottky plot (log Current vs. Square Root Voltage) revealed a two-slope curve, and from the linear portion (first slope) a dielectric constant of 5.3 was obtained, which fits the optical constant value, but not the one obtained by capacitance measurements. Interestingly, the CVD SiO_2 films also show current saturation, but at much lower currents (six orders of magnitude) than Ta_2O_5 films [Kaplan, Balog and Frohman-Bentchkowsky, 1976].

Further research work on the $Si-Ta_2O_5$ interface has revealed that a significant interaction occurs well below the temperature required to form tantalum silicide ($TaSi_2$) or silicon dioxide (SiO_2). This phenomenon occurs in the deposition of the tantalum metal film, to which silicon incorporates in the process. It is claimed that this interaction is the cause for the refractive index gradient of the Ta oxide film. Gravimetric analysis show that thermally oxidized Ta_2O_5 films contain a significant amount of silicon and the results give a ratio of 0.85 Si-Atom/Ta-

atom in the oxide film. Secondary Ion Mass Spectroscopy (SIMS) analysis seem to strengthen this hypothesis at least in a qualitative sense. The interface interaction is explained by assuming that oxygen facilitates the incorporation of silicon by grain boundary diffusion due to the formation of strong Si-O bonds [Revesz and Kirkendall, 1976].

The Rutherford Backscattering (RBS) analysis technique has been applied to study the Ta{oxide}-Si boundary and the characteristics of the oxide layer itself. In the RBS analysis, light and high energy ions (typical are helium positive ions with an energy of 1-5 MeV) are used to bombard the surface to be studied, and by collecting data from the elastic scattered (i.e. bounced back) energy spectrum, knowledge of the surface and near surface composition can be obtained. A depth concentration profile from the energy spectra is then obtained from the He ions rate of inelastic energy loss. Results from this technique on Ta films show significant impurity effects due to gettering during the electron beam deposition from a high purity source. In partial thermal tantalum oxides, they exhibit substantial oxygen incorporation, and in contrast with anodic Ta_2O_5, there is no sharp boundary between the Ta metal and the tantalum pentoxide layer. It was found that the refractive index varies with the oxide thickness, decreasing slightly with thinner oxides, as reported previously by Revesz et al (1974 and 1976). The formation of Si-O-Ta bonds has been pointed to be responsible for this effect, and the

incorporation of silicon to the Ta_2O_5 is noted for this interaction [Hirvonen, Revesz and Kirkendall, 1976].

Anodic titanium-tantalum films have been prepared for use in capacitor TM (tantalum-tantalum-oxide/metal) structures, by the standard sputtering and anodization method. The films had varying atom fractions of tantalum to titanium and the results gave an increased reliability (lower failure rate) under reverse bias, as compared with the tantalum oxide capacitors. Furthermore, it has been proposed that alloying agents into tantalum have the effect of increasing the symmetry of the DC conductance characteristic at room temperature [Peters and Schwartz, 1977].

A conduction mechanism study of another potential insulator film, vanadium pentoxide (V_2O_5) indicated that for both forward and reverse bias (i.e., the gate is positive under forward bias) the I-V characteristic exhibited a combination of different conduction and emission effects and that no single one could account for the carrier transport in the MOS structure. For example, under reverse bias conditions, the experimental I-V measurements showed that at low voltages (0.4 V) an Ohmic region exists; a Schottky type relation (log I is proportional to the square root of V) between 0.4-0.7 V; and a Square Law area for voltages above 1.25 V and then for higher voltages, a transition region in which the current passes from a Schottky type relation, to a linear one and then to a Square Law one. A similar situation exists under forward bias, with differences in the region

extensions and slopes of the I-V characteristic. Capacitance measurements, C-V plots, also indicate complex relationships with voltage and frequency. It was found that above a certain critical frequency, the capacitance became frequency independent, under both forward and reverse bias conditions. An inverse square law characteristic dominates the C-V relationship, with different slopes under forward or reverse bias, i.e., with forward bias the capacitance decreases with voltage, whereas with reverse bias, it increases with voltage. A certain degree of deviation from this relationship was found at voltages close to zero. A plot of the inverse square of the Capacitance vs. Voltage gave a curve which has a slope, such that when intersected at the ordinate (voltage) axis, gives a value Vb (the barrier height), independent of frequency [Mackus, Suli, Torok and Hevesi, 1977].

Thin film capacitors, fabricated by sputtering tantalum metal over glass substrates and then producing tantalum oxide by the anodization method, which gave a finished capacitor area of 0.1 mm^2, were used in the experimental determination of the AC properties of these. The effect of annealing the capacitors in nitrogen at temperatures between 250-350 C was studied, and the authors established that an improved capacitance stability, lower losses and better temperature coefficient of capacitance (TCC) was obtained after the nitrogen annealing. The metal deposition process, Magnetron Enhanced Sputtering (MES), proved to give better quality films, of lower DC leakage, than those prepared by

the conventional DC Diode sputter equipment [Rottersman, Bill and Gerstenberg, 1978].

Capacitors made of anodically oxidized tantalum nitride (TaN), using thin film technology have also successfully been fabricated on glazed ceramic substrates. Reactive sputtering of TaN is followed by anodic oxidation, with counterelectrodes deposited by evaporation. These capacitors showed superior performance as compared with the previous {Ta-oxide} metal capacitors. Lower TCC and dissipation factors were obtained, with high endurance at to heat treatment and improved reliabilty [Doken, Ohwada, Okamoto and Kamei, 1978].

Tantalum pentoxide also exhibits acousto-optic properties, and Bragg cells using a surface acoustic wave (SAW) have been fabricated for use in integrated optical RF spectrum analyzers. This oxide is representative of a group of materials (namely silicon nitride, zinc oxide and glass) which have low optical loss, refractive indices greater than SiO_2 and can be deposited by conventional techniques. For example, Ta_2O_5 had an optical refractive index of 2.15, an optical loss of 1.5-2.0 dB/cm, a surface acoustic wave velocity of 3500-3700 m/s, and an acoustic loss of 7.0-7.5 dB/cm, when used in a thin film waveguide made on silicon substrates [Hickernell, Davis and Richard, 1978].

Double dielectric structures, which incorporate both Ta_2O_5 and SiO_2 have been analyzed for potential use in nonvolatile memory devices. Anodic and thermal Ta_2O_5 is formed over glass or silicon substrates, and then aluminium

electrodes are deposited for determining the characteristics of the insulator film. Theory predicts that by applying a voltage between the gate electrode and substrate, a charge can be stored at the interface between both insulators. If this structure is used as the gate insulator in a MOS device, the presence of this charge affects the threshold voltage of the transistor. Hence, a memory cell can be constructed, as the presence or absence of the interface charge can define the logical state of the device. The conduction mechanism through the Ta_2O_5/SiO_2 double dielectric is, under high field conditions (i.e., the "write" cycle), Poole-Frenkel. At moderate fields, it is the temperature dependent ohmic component that predominates. Only MOS capacitors of Metal-Ta{oxide}-Si{oxide}-Silicon (MTOS) structure were used in the experimental work [Angle and Talley, 1978].

Thin film transistors, fabricated with anodized Ta_2O_5 as gate insulator have been developed, which replaced the usual Al_2O_3 and eliminated the frequent cleaning of masks during manufacturing. The gate insulator was developed from the anodization of tantalum oxynitride, which was used as the gate electrode. This combination produced matched temperature coefficients between gate insulator and electrode. The resultant anodic tantalum pentoxide had a high relative dielectric constant of 22, which produced devices with high transconductance, thus eliminating the necessity for double gate transistors [Kalfass and Lueder, 1979].

Experimental work of tantalum pentoxide films grown on GaAs substrates showed that good insulating films were obtained for both thermal and anodic oxides. The optical properties of these films indicate that a pronounced interaction takes place during the thermal growth of Ta_2O_5, similar to the interaction on silicon substrates. Better insulating properties were obtained with anodic processing of Ta, as a reduced film-substrate interaction was claimed, due to less incorporation of Ga and/or As into the tantalum pentoxide film. However, it was not possible to obtain MOS capacitance-voltage curves [Nishi and Revesz, 1979].

A microelectrode array, using Ta_2O_5 on sapphire, was developed for production of localized electrical excitation of the fibre bundles in the auditory nerve. The array serves as the interface between the nervous system and the implanted electronics of an auditory cochlear prosthesis. The electrodes are made of tantalum metal, insulated from the conducting medium and from each other by anodically formed tantalum pentoxide, with an overall passivation of silicon nitride. This provided a structure with significant advance in the mechanical and electrical stability required to survive the continous electrical stimulation in the nervous system fluids without metal dissolution due to the inertness of tantalum and its oxides [May, Shamma and White, 1979].

Capacitors made with thin film anodic tantalum oxide were used for studying the efects of humidity on the failure rate of these. Two distinct failure modes were established:

point breakdown caused by randomly distributed weak spots resulting from material processing defects, and edge failures which are localized at the exposed edge of the counterelectrode when only subjected to reverse bias [Adolt and Melroy, 1980].

A Dynamic Random Access Memory (DRAM) using the Quadruply Self Aligned (QSA) MOSFET and a stacked high storage capacitor was developed in the construction of a 256 kbit memory using 1.5 μm double-polysilicon-Si process.The word line is polySi and the bit line is Al. The storage capacitor uses anodic Ta_2O_5 as a high permittivity insulator, which is crucial in realizing the capacitance on the required small area of 7.4 μm^2. The leakage current through the insulator was small enough that it did not affect the operation of memory cell, nor its hold time. Experimental 512 kbits and 1 Mbit integrated circuits have also been designed using the same technology [Ohta, Yamada, Saitoh, Shiraki, Nakamura, Shimizu and Tarui, 1980].

The conduction phenomena in tantalum pentoxide films shows that they obey the Schottky theory at low fields, and at higher fields, the Poole-Frenkel model prevails. However there is experimental evidence that an anomalous Poole-Frenkel conduction takes place at high fields in anodic Ta_2O_5. Heat treatment of samples using anodic tantalum films, reveals that an increase in conductivity takes place after 10 minutes in oxygen or vacuum, and if this time is exceeded in a second heat treatment in oxygen, the conductivity is decreased again. A shift from the anomalous

Poole-Frenkel into the normal one is then observed. These changes were attributed to variations in the donor density to trap density ratio and in the donor level energy [Matsumuto, Susuki and Yabumoto, 1980].

A new kind of thin film transistor (TFT) that uses a rather novel gate insulator, a thin polymer film of polytetrafluoroethylene (i.e., teflon) was fabricated to study the MIS structure using organic insulators. The insulator was applied by electron gun evaporation on a Te semiconductor substrate. However, the device showed instability after a few weeks of been fabricated, caused by slow drift in the insulator- semiconductor interface. This is an improvement over the previous TFT fabricated with the same polymer over a CdSe film, which was quite instable and deteriorated the device in a few days [De Vos and Hindryckx, 1980].

The optical and electrical properties of Ta thermal oxides have been determined by analyzing the films on silicon substrates by ellipsometric, C-V and I-V methods. The oxidation time for the tantalum films in dry oxygen was obtained by examination of the ellipsometric parameters Psi and Delta as a function of time. After a certain amount, they had a very slow rate of change, indicating that a complete conversion from metal to oxide had taken place. Any further change in these parameters could be attributed to annealing effects and slow changes in stoichiometry. In contrast with a previous work by Revesz et al., a tapered refractive index transition layer, represented by five

layers of 1.5 nm thick was found, instead of the graded refractive index through the oxide thickness. The C-V curves indicated the presence of a negative oxide charge at flatband, hysteresis and a relative dielectric constant of 26. The I-V curves revealed a two slope Schottky plot, which is typical of tantalum pentoxide films [Smith and Young, 1981].

Metal-Insulator-Metal (MIM) devices have been developed for use as non-linear devices in multiplexing Liquid Crystal Displays (LCDs). A MIM device, using Ta_2O_5 as the insulator, was optimized for this application, by partially anodizing a sputtered metal film on a glass substrate. A computer program was used to determine the parameters in the Poole-Frenkel conduction model to optimize the performance of the MIM switch. Furthermore, nitrogen doping enhanced the conductivity parameter for better multiplexing [Baraff, Long, MacLaurin, Miner and Streater, 1981].

Waveguide films prepared with tantalum pentoxide over SiO_2 are important, since this class of thin films has a wide range of refractive index with low propagation loss (less than 1 dB/cm at 633 nm wavelength). Irradiation using a CO_2 laser produces a decrease in the refractive index, up to 2%. This decrease is considered to be related to the Ta_2O_5 crystallization process from its amorphous state, when exposed to intense laser radiation. This in turn affects the permittivity of the tantalum oxide [Terui and Kobayashi, 1981].

Bismuth oxide is another insulator material that has

been used in the fabrication of Metal-Insulator-Semiconductor (MIS) capacitors. The film was deposited by reactive ion sputtering and later annealed in air. The Bi_2O_3 capacitor yielded a relative dielectric constant of 25, and a tanδ (loss factor) of 0.002 at 35 kHz, making it useful for production of low frequency capacitors. The C-V curves show a shift in the negative direction with relatively small hysteresis [Raju and Talwai, 1981].

When tantalum films are deposited over silicon substrates by sputtering, a stress field is induced, which produces a curvature of the substrate. A MIS device was used as a photovoltaic cell in order to study the stress effect in its performance. It was found that the induced stress produced large changes in the minority carrier diffusion length and recombination time, as well as the recombination time and capture cross section. Moreover, the short circuit current, open circuit voltage and fill factor were reduced [Lalevic and Murty, 1981].

Indium phosphide, InP, was anodically oxidized to form an gate insulator in a MOSFET accumulation mode device. The oxide had low enough interface state density to be used as gate insulator. No C-V or I-V data was reported, and the oxide required annealing in order to reduce the C-V hysteresis loop. The device had a gate length of 500 μm and a gate width of 2 mm. The measured estimated electron mobility, μeff, was 1500 cm^2/Vs [Yamamoto and Uemura, 1981].

GaAs technology for Microwave Integrated Circuits (MICs) makes use of high quality tantalum oxide capacitors

in interstage coupling of microwave amplifiers. The capacitor has a Metal-Insulator-Metal (MIM) structure and they were integrally sputtered (reactively) on the semi-insulating GaAs substrate. A staircase shape is then formed by lift-off and patterning. Typical capacitances in the range of 50-200 pF were obtained, with an oxide thickness of 150 nm, a relative dielectric constant of 20-25 and a loss factor (tanδ) of 0.03 at 1 MHz. The leakage current had an exponential relation with applied voltage [Elta, Chu, Mahoney, Cerretani and Courtney, 1982].

Anodization of aluminium has also produced dielectrics for MIC capacitors, in the form of Al_2O_3, with a typical value of 30 pF, and a relative dielectric constant of 8. The figure of merit ϵrE, the product of the relative permittivity and the dielectric strength, indicates the quality in terms of bandwidth and area for a given material [Binet, 1982].

Further work in the Ta_2O_5 MIC capacitors indicates that a two stage monolithic IF amplifier, operating in the 1.2 to 2.8 GHz range and using these as coupling elements, is quite feasible. The reactive MIM process produced a capacitance density of 1500 pF/mm², and a very good quality dielectric was obtained with an insertion loss of 1 dB at 16 GHz for a 29 pF capacitor [Chu, Mahoney, Elta Courtney, Finn, Piacentini and Donnelley, 1983].

Ion Sensitive Field Effect Transistors (ISFET's), fabricated with SOS (silicon on sapphire) technology and tantalum pentoxide as gate insulator produced the highest pH

sensitivity among three other dielectrics. ISFETs do not have a metal gate electrode, and it is the electrolyte in which they are immersed which acts as the gate electrode, making them very useful as pH detectors. The Ta_2O_5 gate ISFET exhibits a linear relation between output voltage and the solution pH, with a 90% response time of a few seconds. It was concluded that the Ta_2O_5 film was the most suitable as sensing material for hydrogen activity measurements [Akiyama, Ujihira, Okabe Sugano and Niki, 1982].

Langmuir-Blodgett films are single molecular layers, formed by the removal of a amphiphilic molecule from an aqueous solution with a polar substrate (i.e., aluminium oxide). The amphiphilic molecule is a simple fatty acid, which has a hydrophilic termination immersed in the aqueous solution and a hydrophobic end in the air. The relative permittivity of such a molecule can be selected by choosing a suitable CH_2 chain length and by substituting a divalent ion bond for for the hydrophilic termination. A thin film FET using amorphous silicon and L-B film techniques as gate insulator was developed. The L-B layer not only is pinhole free but also has a high dielectric breakdown strength and exhibits many of the characteristics of an ideal gate insulator. [Pitt, 1983; Lloyd, Petty and Roberts, 1983]

Further analysis of thermal Ta_2O_5 films on silicon substrates show that the amount of silicon incorporated to the oxide depends on the residual pressure during the tantalum metal evaporation. As the vacuum quality is reduced, less amount of silicon is incorporated to the

oxide. Also, it was found that the the relative dielectric constant and the leakage current decrease as the amount of Si increases in the oxide film. [Hasegawa, Ogawa, Wada and Nakano, 1983].

An interesting technique for growing a heteromorphic dielectric layer, Ta_2O_5 over SiO_2, was developed for producing high quality storage capacitors for a VLSI dynamic RAM. The technique is based in the oxidation of a silicon substrate covered with a thin Ta_2O_5 layer. The interfacial oxidation of Si takes place by wet oxidation, and a high quality double dielectric is then produced, thus avoiding separate oxidations of Ta and Si. A memory cell was fabricated using this technique [Kato, Ito, Taguchi, Nakamura and Ishikawa, 1983].

A thin film transistor (TFT) with tantalum pentoxide as gate insulator and deposited by Magnetron Enhanced Sputtering has recently being developed. The device has a p-channel structure, with a fused quartz substrate and Al doped source and drain regions. Reactive Ion Etching (RIE) was used to pattern the Ta_2O_5. The device exhibits a threshold voltage of -2.5 V and a transconductance of $70\mu S$. The fabrication of the device allowed a maximum temperature of 625C, which is compatible with glass substrates and tantalum pentoxide [Seki, Unagami and Tsujiyama, 1984].

CHAPTER 3

THE THEORY OF THE $Ta_2O_5-SiO_2$ DOUBLE

DIELECTRIC STRUCTURE

Considerable amount of work was done in double dielectric insulators, which were based on the Metal-Nitride-Oxide-Silicon (MNOS) system -used in memory devices- such as non-volatile dynamic and static cells in Electrically Programmable Read Only Memories (EPROMs). The MNOS Memory Transistor was studied by Wallmark and Scott (1969), Ross (1969) and Frohman-Bentchkowsky (1970). The theoretical aspects of this device have great importance, as the MNOS and MTAOS behaviour is quite similar, although not identical. They also have in common a thin layer of SiO_2, immediately above the substrate. The electrical performances are similar, and Angle (1976) established that memory devices could also be fabricated using MTAOS technology, which had superior characteristics over the MNOS device.

The double heteromorphic Ta{ox}/Si{ox} dielectric structure has been developed as a result of investigations on large permittivity insulating thin films for applications in MOS Capacitors [Angle, 1976], memory devices [Angle and Talley, 1978] and more recently storage MOS capacitors for dynamic Random Access Memories of VLSI proportions [Ohta et al.,1982].

Generally speaking, the Metal-Double Insulator-Semiconductor (MDIS) structures have similar properties, namely a

dissimilar field distribution in each insulator, different electronic conduction (emission) mechanisms and under certain conditions, a charge retention or memory effect.

Several areas of common interest to microelectronics and the research in double insulating structures are identifiable:

1) The LSI and VLSI densities require increased device scaling.

2) Further scaling in MOS devices requires thinner oxides and insulators.

3) Device scaling decreases the maximum gate voltage due to insulator breakdown.

4) Insulators of large dielectric constant produce the required capacitance in proportionally less area, but in most cases an increase in leakage current is observed.

5) Breakdown of a thin scaled down oxide can be avoided if a larger permittivity insulator is placed between itself and the gate electrode.

6) The large dielectric constant of Tantalum Pentoxide can be combined with the excellent insulating properties of Silicon Dioxide, thus producing a double dielectric with a breakdown voltage governed by the high permittivity oxide thickness, while maintaining a low level of leakage current.

7) In the double insulator structure, the probability of pinholes coinciding in the same location is negligible, thus producing a better quality insulator.

8) Amorphous Silicon Dioxide is structurally porous and it has high permeability to water vapour and migration of alkali ions. The application of a second outer dielectric reduces these effects. Tantalum Pentoxide has a much denser structure, possibly retarding the ion migration through it.

9) Double dielectric stuctures exhibit memory effects, hence they can be used as memory cells if properly designed.

In this work, our main effort is concentrated in the development of a Ta_2O_5/SiO_2 insulator for MOSFET applications as opposed to a memory cell for either RAMs or DRAMs. The MOSFET device that incorporates the tantalum pentoxide-silicon dioxide gate insulator is termed a Metal-Tantalum{Oxide}- Silicon{Oxide}-Silicon device, or MTAOS structure. The inner insulator is immediately above the substrate, and the outer insulator is below the gate contact electrode. Figure 3.1 gives a cross section of such a double dielectric, with the main features and dimensions shown. The critical areas are the interfaces between the Ta_2O_5 and SiO_2 insulators and to a lesser degree, the interface between the top (gate) electrode and the Ta_2O_5. The interface between the SiO_2 and the silicon substrate is well known [Grove et al., 1964; Grove et al., 1965; Gray, 1969] and it is not analyzed here.

Of great importance is the physical model for carrier transport under steady state and transient conditions. The

Gate Contact

Al

Ta$_2$O$_5$

Insulator
Interface

SiO$_2$

n Si

Al

t

s

Substrate
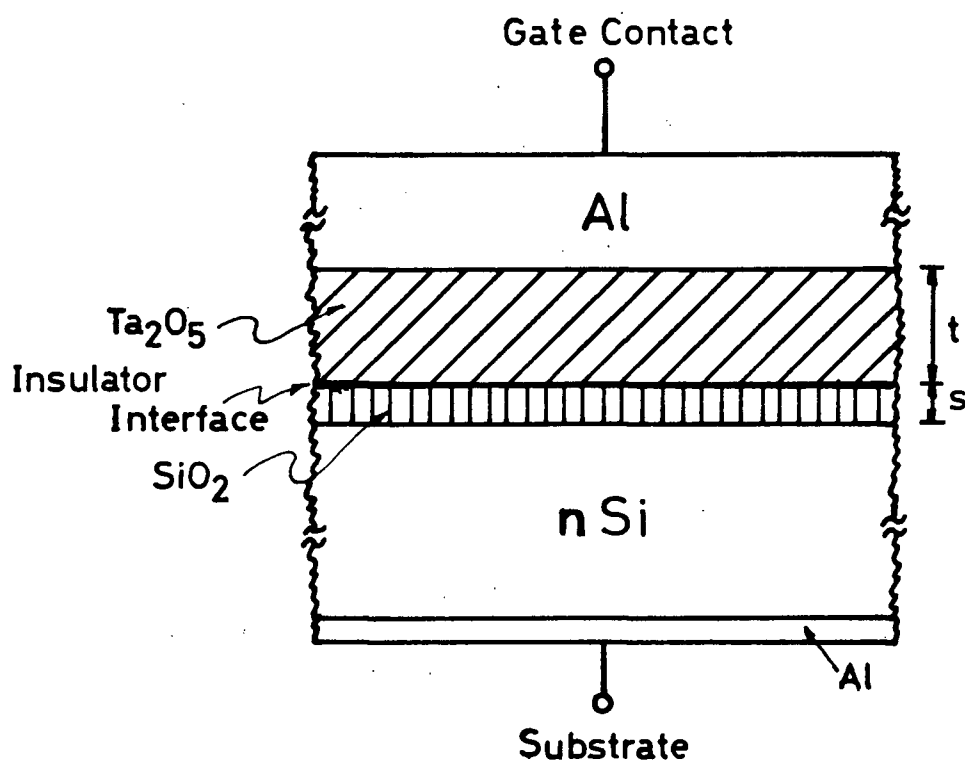
The Al-Ta$_2$O$_5$-SiO$_2$-nSi Structure

s

t

J_s

J_t

t=0

E_s

E_t

V_a
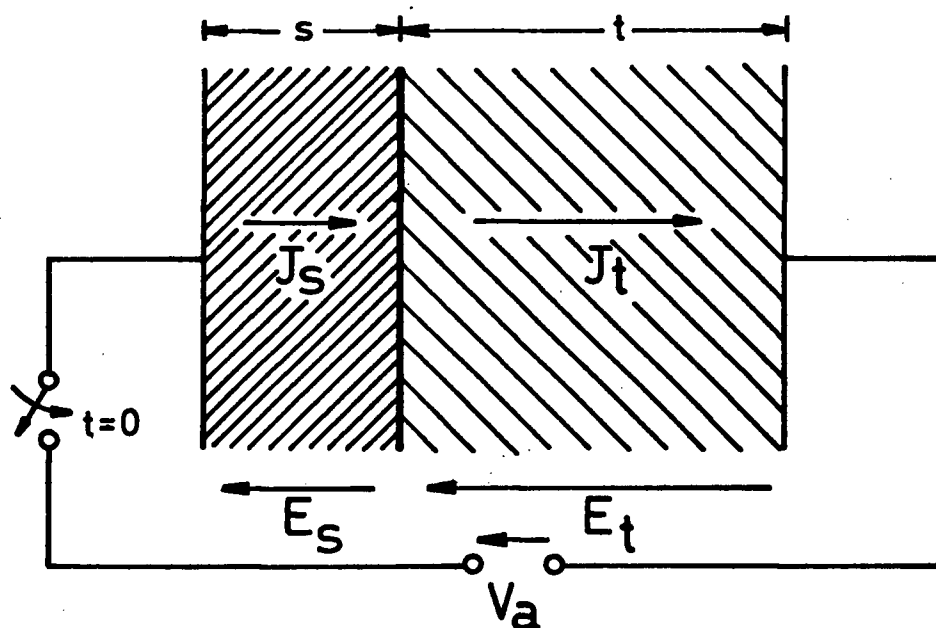
Figure 3.1 The General Double Dielectric Structure.

differences in the composition of each dielectric makes the exact analysis quite complicated, particularly for the transient case. When a voltage is applied to the double insulator structure, conduction currents flow, however, the mechanism that governs these are quite different for the tantalum pentoxide and silicon dioxide. The dominant current transport mechanism for SiO_2 has been established to be electrode limited due to Fowler-Nordheim emission [Lenzlinger and Snow, 1969]. This type of conduction mechanism is caused by tunneling through the barrier into the insulator conduction band. In the case of Ta_2O_5, the carrier transport is bulk limited by Poole-Frenkel type emission [Mead, 1962; Angle, 1976; Angle and Talley, 1978], although it is greatly influenced by the existence of trapping centres. For example, if the trapping density is low, normal Poole-Frenkel conduction takes place, but if it is high (as compared with the donor density), compensated or anomalous Poole-Frenkel emission dominates. Anodic tantalum oxide seems to follow these considerations, however the thermal tantalum oxide exhibits a more complex behaviour, depending on the sign of the applied bias. Angle (1976) explained this complex behaviour by observing that under positive gate bias, normal P-F conduction takes place, but under negative bias space charge limited conduction determines the current flow, attributed to surface states formed at the Al{gate}-Ta_2O_5 interface. The Poole-Frenkel effect represents the increase in electrical conductivity by lowering the Coulombic potential barrier, when it interacts

with ań electric field. Space charge conduction results from carriers injected into the insulator where there is no compensation charge present.

Considering the displacement and conduction current density contributions by virtue of the Ramo-Shockley theorem, the terminal currents for the Ta$_2$O$_5$ and SiO$_2$ insulators can be expressed as:

$$I_t = A_t \left(\frac{\varepsilon_t}{t} \frac{dV_t}{d\tau} + \frac{1}{t} \int_0^t j_t(z)\, dz \right) \quad (3.1a)$$

$$I_s = A_s \left(\frac{\varepsilon_s}{s} \frac{dV_s}{d\tau} + \frac{1}{s} \int_0^s j_s(z)\, dz \right) \quad (3.1b)$$

Where At and As are the cross section areas; εt and εs are the Ta$_2$O$_5$ and SiO$_2$ dielectric constants; t and s are the insulator thicknesses; Vt and Vs are the resulting voltages in each insulator and the variable τ represents time. The term jt(z) is the conduction current density in the tantalum pentoxide, given by the Poole-Frenkel effect, and js(z) is the conduction current density in the silicon dioxide and determined by Fowler-Nordheim tunneling. The dependency on the variable z indicates that a current density distribution exists along that axis.

In the Poole-Frenkel emission, the current density usually can be expressed as:

$$J_t = C_{pf} E_t \exp\left(-\frac{q}{kT} \left(\psi_B - \sqrt{qE_t / \pi \varepsilon_i} \right) \right) \quad (3.2)$$

Where Et is the electric field in the tantalum pentoxide and the quantity ψ_B represents the barrier height.

For the Fowler-Nordheim emission, the current density is expressed as:

$$J_s = C_{fn} E_s^2 \exp(-E_o/E_s) \qquad (3.3)$$

Where Es is the field in the silicon dioxide. The characteristic constants Cfn and Eo depend on the effective mass and barrier height. Notice that in both cases, the current densities are strong functions of the applied field. Furthermore, upon the application of a gate voltage Va to the double insulator structure, an electric field is created in each individual insulator. Gauss' Law prescribes that the continuity of the displacement D at the interface between insulators shall be maintained:

$$\epsilon_t E_t - \epsilon_s E_s = \frac{Q_i}{\epsilon_o} \qquad (3.4)$$

Qi is the charge per unit area at the interface. The sum of the voltage drops across each dielectric has to be equal to the total applied voltage. Then, considering the metal semiconductor work function ϕms, we have:

$$V_a = -t E_t - s E_s + \psi_s + \phi_{ms} \qquad (3.5)$$

The silicon surface potential is represented by ψs and the conventional definition of potential difference (drop) is used.

Finally, the electric charge has to be conserved at all times:

$$J_t - J_s = \frac{\partial Q_i}{\partial \tau} \qquad (3.6)$$

In general, an interface charge Qi will appear between both dielectrics, at the interface. The dependence of this interface charge upon time and geometry of the insulating structure, can be obtained by simultaneous solution of Equations 3.4, 3.5, 3.6, and considering the P-F Ta_2O_5 emission and the F-N mechanism in the SiO_2; not an easy task!

{3.1} STEADY STATE ANALYSIS:

The different conduction mechanisms responsible for the current transport in the SiO_2 and Ta_2O_5 are also the cause for creating an accumulation of carriers at the interface between dielectrics. Upon the application of an external field, caused by the gate voltage, electronic conduction following the Fowler-Nordheim emission takes place in the silicon dioxide and conduction following Poole-Frenkel takes place in the tantalum pentoxide. These being quite different, create a current discontinuity, which leads to a charge accumulation at the interface. This charge

accumulation, in turn, adjusts the electric field distribution, until current continuity is established.

The solution obtained by steady state analysis gives the electric field in each dielectric Et and Es, as well as the charge at the interface Qi. Under steady state conditions, both currents Js and Jt are equal, and therefore, the charge at the interface is negligible. By substituting these conditions in Equations 3.4 and 3.5 above, we obtain the field Es in the SiO_2:

$$E_s = - \frac{(V_a - \psi_s - \phi_{ms})/s}{1 + \frac{t}{s} \frac{\varepsilon_s}{\varepsilon_t}} \qquad (3.7)$$

$$r = \frac{1}{1 + \frac{t}{s} \frac{\varepsilon_s}{\varepsilon_t}} \qquad (3.8)$$

This last equation represents the reduction in the SiO_2 electric field due to the addition of a second dielectric of thickness t and relative permittivity ϵt. Using values of $\epsilon s = 3.8$, $\epsilon t = 27$, s=200 A, and t=1000 A, a reduction factor of 0.587 is obtained.

By similar reasoning we obtain the field Et in the Ta_2O_5:

$$E_t = \frac{(V_a - \psi_s - \phi_{ms})/t}{1 + \frac{s}{t} \frac{\varepsilon_t}{\varepsilon_s}} \qquad (3.9)$$

On the other hand, if the interface charge Qi is non-zero,

the internal electric fields due to this charge, can be calculated in each individual dielectric:

For the Ta_2O_5 insulator:

$$E_t = - \frac{Q_i/\varepsilon_0 + \frac{\varepsilon_s}{s}(\psi_s + \phi_{ms})}{\varepsilon_t + \frac{t}{s}\varepsilon_s} \qquad (3.10)$$

For the SiO_2 insulator:

$$E_s = + \frac{Q_i/\varepsilon_0 + \frac{\varepsilon_t}{t}(\psi_s + \phi_{ms})}{\varepsilon_s + \frac{s}{t}\varepsilon_t} \qquad (3.11)$$

{3.2} TRANSIENT ANALYSIS:

Upon the application of a sudden voltage at the gate, both insulators will have certain fields applied and conduction currents will flow as prescribed before. The Law of Conservation of Charge requires that:

$$\frac{dQ_i(V_a, \tau)}{d\tau} = J_t(V_a, \tau) - J_s(V_a, \tau) \qquad (3.12)$$

The rate of change in the interface charge will be directly proportional to the difference in current density for both dielectrics, at a given applied gate voltage and time. The solution to this partial differential equation of two independent variables can be obtained if more information of the detailed conduction mechanisms is available. For example

Ross and Wallmark (1969) studied the transient behaviour of a MNOS structure, and explained the conduction mechanism at the interface between dielectrics, as a function of trapping centres of the donor type which communicate with the silicon, when a field is applied to the structure. In their mathematical derivation, they assumed a monoenergetic trap level, and the charge transfer was assumed to be through direct tunneling between trap states in the composite insulator. These authors obtained a relation for the transferred charge, that depended logarithmically on the applied gate pulse duration and exponentially on the amplitude of the applied gate pulse.

Considering the fact that the interface charge is a function of applied voltage and time, if Equation 3.4 is substituted in Equation 3.5, the general time varying solution is found for both insulator electric fields:

$$E_t = - \frac{(V_a - \psi_s - \phi_{ms})}{t + s\frac{\epsilon_t}{\epsilon_s}} + \frac{Q_i/\epsilon_o}{\epsilon_t + \frac{t}{s}\epsilon_s} \qquad (3.13)$$

$$E_s = - \frac{(V_a - \psi_s - \phi_{ms})}{t\frac{\epsilon_s}{\epsilon_t} + s} - \frac{Q_i/\epsilon_o}{\frac{s}{t}\epsilon_t + \epsilon_s} \qquad (3.14)$$

Where the relation Qi=Qi(Va,t) is valid for t>to, the instant of gate voltage application.

Then the corresponding voltages across each dielectric are given by:

$$V_t = \frac{(V_a - \psi_s - \phi_{ms})}{\{1 + \frac{s}{t}\frac{\varepsilon_t}{\varepsilon_s}\}} - \frac{Q_i/\varepsilon_o}{\{\varepsilon_s/s + \varepsilon_t/t\}} \qquad (3.15)$$

$$V_s = \frac{(V_a - \psi_s - \phi_{ms})}{\{1 + \frac{t}{s}\frac{\varepsilon_s}{\varepsilon_t}\}} + \frac{Qi/\varepsilon_o}{\{\varepsilon_s/s + \varepsilon_t/t\}} \qquad (3.16)$$

Very little has been published on a solution for the term $Qi = Qi(Va,t)$ under transient conditions. Frohman-Bentchkowsky (1970) analyzed the MNOS case by obtaining a computer solution for Equation 3.12, but he gives no details. Ross and Wallmark (1969) obtained a solution considering a MNOS structure and analyzed the filled trap states using tunneling transition probabilities through a rectangular barrier. Following these last authors, we have:

$$Q_i(\tau) = q\lambda \bar{N}_i(x_o,0)\{0.577 + \ln(t/t_o) - E_i(-t/t_o)\} \qquad (3.17)$$

The function $Ei(-t/to)$ converges rapidly to zero for $t>to$, and λ is quite close to 1 Angstrom.

In the case of the composite dielectric $Ta_2O_5-SiO_2$, more knowledge has to be acquired of the intimate conduction mechanisms at the interface, in order to evaluate Equation 3.12 in a better way. Once again, the interface properties are defining the overall behaviour of a MDIS system.

{3.3}   EFFECT OF THE DOUBLE DIELECTRIC GATE INSULATOR ON THE

MOSFET PERFORMANCE:

In the double insulator structure, an equivalent

insulator thickness di can be defined:

$$d_i = s + \frac{\varepsilon_s}{\varepsilon_t} t \qquad (3.18)$$

This can be verified by considering the capacitors Ct and Cs

in series, and calculating the total capacitance C_T:

$$C_T = \frac{C_s C_t}{C_s + C_t} \qquad (3.19)$$

Also, an equivalent capacitance Ci per unit area that

reflects the combination of both dielectrics can be written

as:

$$C_i = \frac{\varepsilon_s \varepsilon_o}{d_i} \qquad (3.20)$$

Therefore, the total capacitance per unit area in the double

gate insulator is less than each single insulator

capacitance. This is quite obvious, as the insulators can be

represented by two capacitors in series, each with a value

of capacitance per unit area corresponding to each

dielectric.

Of interest are the equivalent capacitance to SiO_2

capacitance ratio:

$$\frac{C_i}{C_s} = \frac{1}{1 + \frac{t}{s}\frac{\varepsilon_s}{\varepsilon_t}}$$ (3.21)

This ratio represents the reduction in capacitance as compared with the silicon dioxide capacitance. For typical values of s=200 A, t=1000 A, εs=3.8 and εt=27, the ratio is 0.587. Therefore, as the electric field across the SiO_2 is reduced, the equivalent capacitance is also reduced by the same factor.

Conversely, an equivalent permittivity can be defined, if the capacitor is considered to have a thickness of t+s units. From the equivalent capacitance expression, Equation 3.20:

$$C_i = \frac{t+s}{s + \frac{\varepsilon_s}{\varepsilon_t}t}$$ (3.22)

Then, the equivalent permittivity can be defined as:

$$\varepsilon_i = \frac{t+s}{s/\varepsilon_s + t/\varepsilon_t}$$ (3.23)

A graph of its function is shown in Figure 3.2, with several curves given for different insulator compounds. Notice that for a large ratio of insulator thicknesses, the equivalent permittivity approaches that of the outer (and larger)

insulator dielectric constant.

The following Equations define the operation of a MOSFET, using the simplified model [Sze, 1969]:

$$I_d = \frac{Z}{L} \mu C_i \{ (V_g - V_T) V_d - \tfrac{1}{2} V_d^2 \} \qquad (3.24)$$

Notice that Id, the drain current, is proportional to Ci, the insulator capacitance.

The threshold voltage is given by:

$$V_T = 2\psi_b + V_{fb} + \{ 2\varepsilon_s q N_{A,D} (2\psi_b) \}^{\tfrac{1}{2}} / C_i \qquad (3.25)$$
$$\psi_b = \frac{kT}{q} \ln\{ N_A/n_i, \; n_i/N_D \}$$

Notice that the threshold voltage V_T, is inversely related to Ci, which is is given by:

$$C_i = \frac{\varepsilon_o \varepsilon_i}{d_i} \qquad (3.26)$$

The device transconductance is:

$$g_m = \frac{Z}{L} \mu C_i V_d \qquad (3.27)$$

Which is directly proportional to Ci.

In the case of the channel conductance, the situation is slightly more complicated:
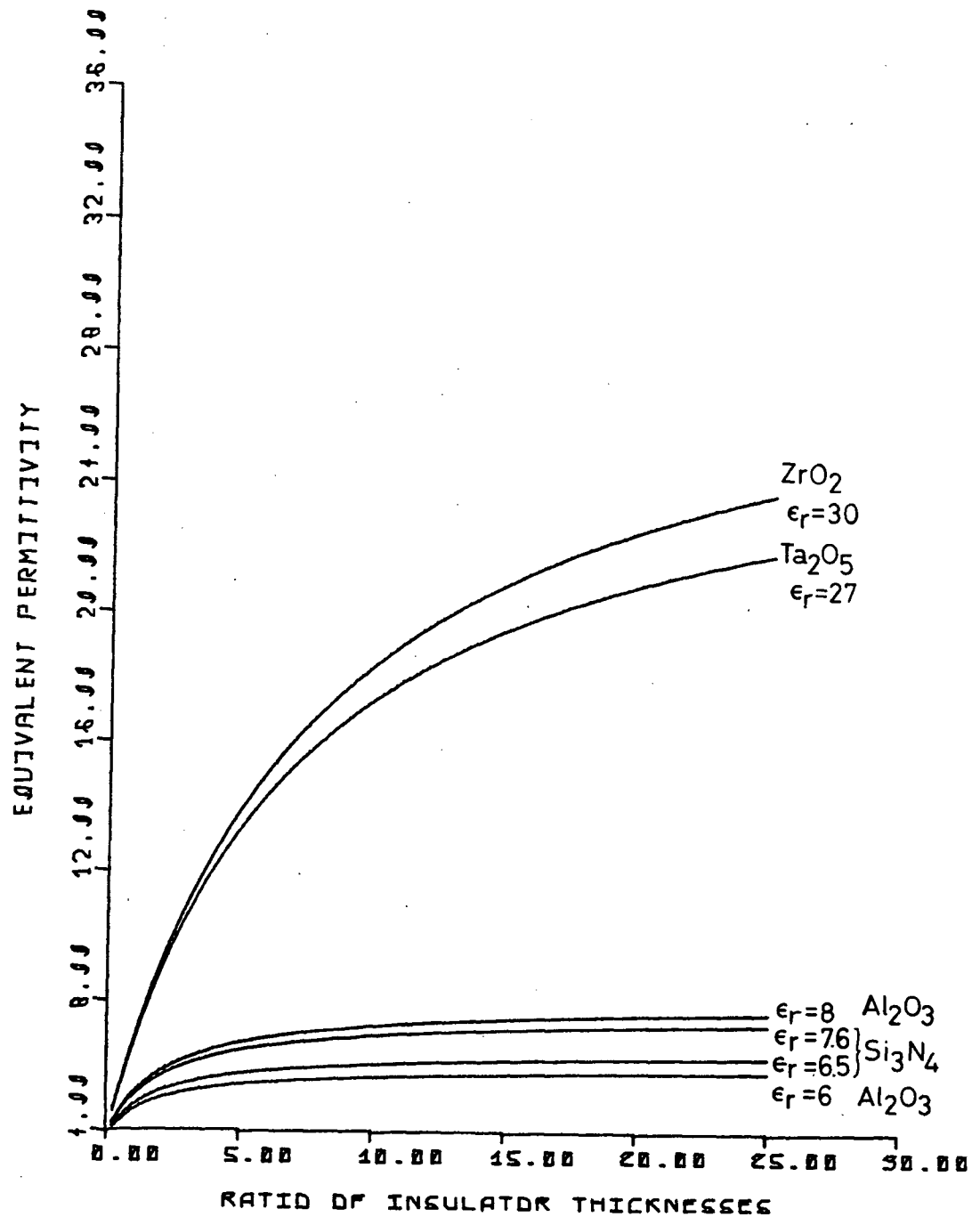
Figure 3.2 Equivalent Permittivity of a Double Insulator
Structure

$$g_d = \frac{Z}{L} \mu C_i (V_g - V_T) \qquad (3.28)$$

The channel conductance remains approximately the same, since C_i has increased, but V_T has decreased.

Based on the above reasoning, Table 3.1 gives the results obtained using the SiO_2 insulator capacitance as reference.

TABLE 3.1

DOUBLE DIELECTRIC MOSFET PARAMETERS

Tantalum Pentoxide on Silicon Dioxide

	t/s=5.0	t/s=2.0	t/s=1.0
Idi/Ids	0.587	0.780	0.877
V_Ti/V_Ts	$\simeq 1.704$	$\simeq 1.282$	$\simeq 1.140$
Ci/Cs	0.587	0.780	0.877
gmi/gms	0.587	0.780	0.877
gdi/gds	$\simeq 1$	$\simeq 1$	$\simeq 1$

The subscripts 's' and 'i' refer to the SiO_2 and equivalent insulator parameters, t and s are the thickness of the tantalum pentoxide and silicon dioxide, respectively.

Notice that the channel conductance gd remains approximately constant as the ratio t/s is varied. The transconductance, insulator capacitance and drain current increase with diminishing t/s. The gate threshold voltage decreases as t/s is reduced.

{3.4} EFFECT OF A HIGH PERMITTIVITY GATE INSULATOR ON THE MOSFET PERFORMANCE:

In the case of a single dielectric layer of gate oxide, which has high relative permittivity, the same previous reasoning is valid for the MOSFET device relations, with the exception that the relative dielectric constant of the Ta_2O_5 is 27, and that of the SiO_2 is 3.8. Using these values the ratio of ϵt to ϵs is then 7.11.

The calculated quantities, for tantalum pentoxide, silicon nitride ($\epsilon r = 7.6$) and aluminium oxide ($\epsilon r = 8$) using the SiO_2 insulator as comparison, are shown in Table 3.2.

TABLE 3.2

SINGLE DIELECTRIC MOSFET PARAMETERS

Tantalum Pentoxide, Silicon Nitride and Aluminium Oxide

	Ta_2O_5/SiO_2 $\epsilon t/\epsilon s=7.11$	Si_3N_4/SiO_2 $\epsilon n/\epsilon s=2.0$	Al_2O_3/SiO_2 $\epsilon a/\epsilon s=2.11$
Idi/Ids	7.11	2.0	2.11
V_Ti/V_Ts	$\simeq 0.141$	$\simeq 0.500$	$\simeq 0.475$
Ci/Cs	7.11	2.0	2.11
gmi/gms	7.11	2.0	2.11
gdi/gds	$\simeq 1$	$\simeq 1$	$\simeq 1$

It quite clear that the high dielectric constant insulator as gate oxide will, with all other parameters remaining equal, increase the transconductance, insulator capacitance and drain current. Notice that the threshold voltage is reduced by the same factor. The channel conductance remains approximately the same.

The ability of the MOS Capacitor to withstand an applied voltage and store a given charge is measured by the figure of merit $\epsilon_0 \epsilon r E$, were E is the maximum (breakdown) electric field. This is the capacitor charge storage factor [Glaser, Subak-Sharpe, 1977; Binet, 1982], it is based on the flat plate capacitor equation and the fact that the best capacitor bandwidth is obtained when the ratio $\epsilon r/t$ is largest. The bandwidth of a capacitor (used for coupling circuits in MIC's) is that in which the impedance shunting effects due to parasitic capacitances is small compared with the system impedance. However, the thickness t is limited by $t = E/Va$, were Va is the maximum applied voltage. Following Binet (1982), Table 3.3 gives the figure of merit for several widely used insulators, in which the maximum (breakdown) field is applied. The tantalum pentoxide insulator has the highest figure of merit, followed by aluminium oxide and silicon nitride.

The use of either single insulator or double insulator structure in a MOS transistor will be a function of the design objectives. In theory, the single, high permittivity Ta_2O_5 gate insulator can offer considerable advantages over

the compound structure, but as we shall see in the following chapters, the electronic conduction (i.e. leakage) currents, impose a serious limitation to the tantalum pentoxide monoinsulator. The double layer insulator, with SiO_2 immediately over the Si substrate, can reduce considerably the electronic conduction, if the thickness of this insulator is such (typically >10 nm) that tunneling through the barrier is avoided.

TABLE 3.3

MOS CAPACITOR INSULATOR FIGURE OF MERIT

Silicon Dioxide, Silicon Nitride, Aluminium Oxide and

Tantalum Pentoxide

MATERIAL	ϵr	Field, E [MV/cm]	ϵrE [MV/cm]	$\epsilon_0 \epsilon rE$ [pfV/mm^2]
SiO_2	3.8	4	15.2	13458
Si_3N_4	7.6	10	76	67290
Al_2O_3	8	10	80	70832
Ta_2O_5	27	4	108	95623

{3.5} ENERGY BANDS OF THE TANTALUM PENTOXIDE INSULATOR:

An effort was made to compile enough data from this insulator as to produce an energy band diagram. Little data is available in the literature regarding the essential parameters such as electron affinity and metal-insulator barrier potentials. Internal photoemission is a powerful tool that is used to obtain the electron affinity of insulators [Goodman, 1968]. However, in the case of Ta_2O_5 no measurements have been made [Goodman, 1984], which confirms the unavailability of published figures. Angle (1976) provides a sketch of a band diagram in his Ph.D. Thesis, but he provides no details or references on his source for the tantalum pentoxide band structure data. The value of his metal-insulator barrier height coincides (0.72 eV) with the one given by Young (1961) of 0.71 eV. Also the value of the bandgap energy (4.2 eV) is coincident with the ones obtained by previous authors [Zaininger et al., 1969; Kaplan et al., 1973; Revesz et al., 1976]. Based on the data provided by Angle, an energy band diagram is presented in Figure 3.3, for an $Al-Ta_2O_5-nSi$ structure in equilibrium (no external gate potential applied).

Figure 3.3 Energy Band Diagram of the Al-Ta₂O₅-nSi Structure

{3.6} DOUBLE DIELECTRIC MOSFET STRUCTURE:

The cross section of this device is shown in Figure 3.4. Its dimensions are typical and reflect the ones used in this work. The transistor has the drain and source p-type junctions on a n-Si substrate, with windows cut in the field oxide to provide adequate contacts. The gate area contains the double insulator structure, bounded by the substrate and the gate metal contact. An inversion p-type channel is formed under the gate, when a negative voltage is applied to the gate, thus providing enhancement mode operation. For proper operation, the drain-source bias has to be negative. The substrate or bulk, has a contact provided by a bottom gold metallization.

Figure 3.4 Double Dielectric MOSFET Structure.
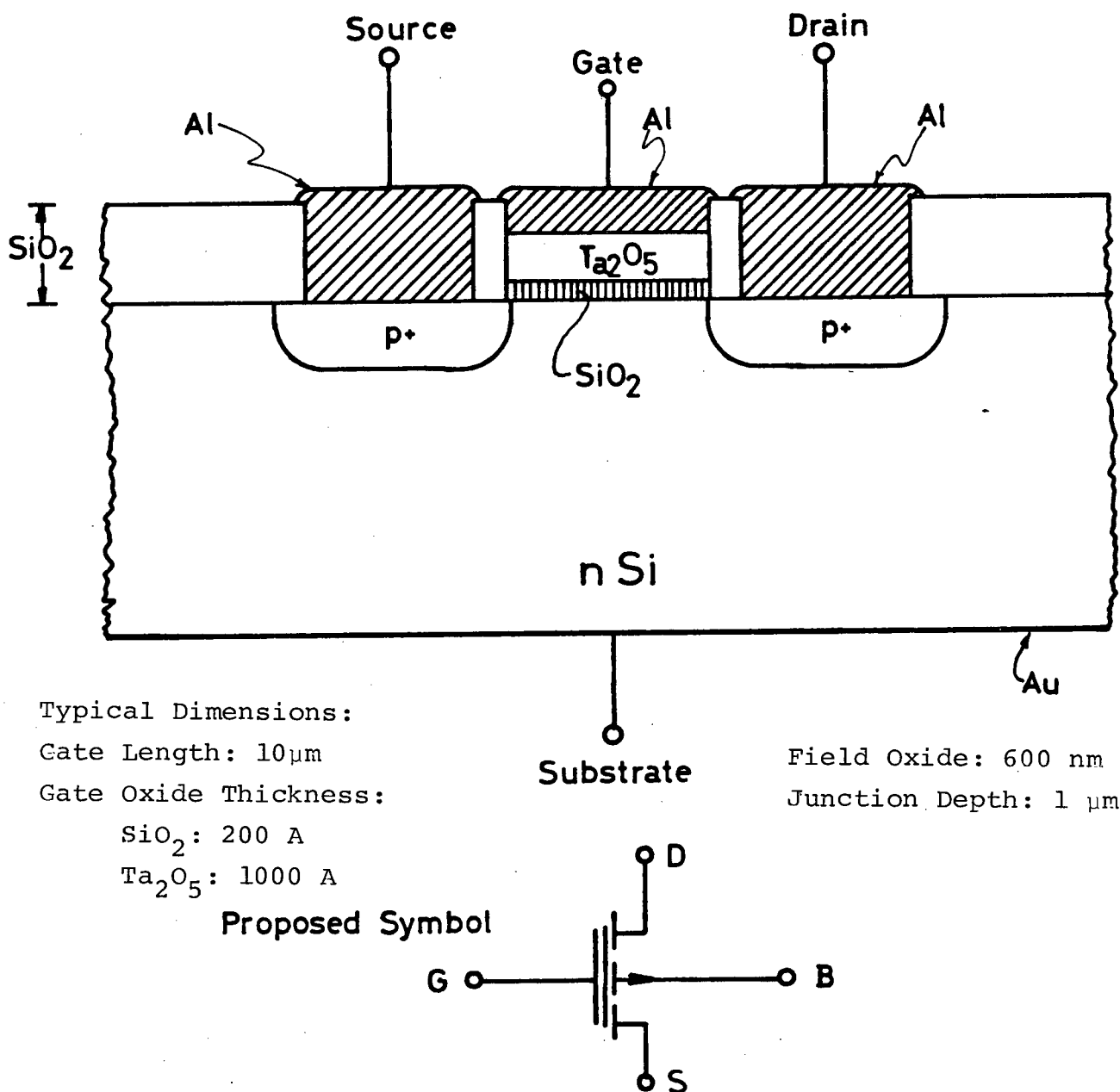
CHAPTER 4

FABRICATION AND PROCESSING OF MOS CAPACITOR DEVICES

Before the final MTAOS structure could be developed, it was necessary to study in great detail the fabrication and processing of tantalum pentoxide single dielectric MOS capacitors. Then a step further could be made into the Ta_2O_5-SiO_2 double dielectric MOS Capacitor fabrication. When these were established as successful processing technologies, the double dielectric MTAOS device could only then be fabricated.

{4.1} MOS CAPACITORS WITH THERMAL Ta_2O_5 AS INSULATOR:

Considerable amount of time was devoted to the processing of MOS Capacitors with a single insulating film of Ta_2O_5, and several techniques for patterning the Ta metal were used. The following general processing steps were followed:

1) Thickness and four point resistivity measurements.

2) Scribing and marking.

3) Peroxide-Acid cleaning using the RCA process.

4) RF Sputtering of tantalum metal.

5) Thermal Oxidation in dry oxygen.

6) Aluminium evaporation for gate electrodes.

7) Patterning of aluminium metal by photolithography.

8) Back contact by aluminium evaporation.

{4.1.1} THICKNESS AND SHEET RESISTIVITY MEASUREMENTS:

Thickness measurements were performed with a Mitutoyo DGS-E Gauge dial caliper. Four Point resistivity measurements were done using a Hewlett-Packard 6186C Current Source, a Fluke 8000A or 8050A Digital Voltmeter and a Kulicke and Soffa Model 3007, No.130, four point probe with an interprobe spacing of 0.025 inches.

{4.1.2} SCRIBING AND MARKING:

Scribing and marking was done with a standard diamond pen, on the wafer's back, immediately above the flat. A special code and date was inscribed, unique to each individual wafer, so that future identification could be made easy. A large amount of samples was prepared, as shown in Table 4.1.

TABLE 4.1

SINGLE DIELECTRIC THERMAL MOS CAPACITORS

SAMPLE NAME	Ta THICKNESS [A]	SUBSTRATE
N1	500	n Type
N2	1000	n Type
BNR500	500	p Type
BNR1000	1000	p Type
SampleA	500	p Type
SampleB	1000	p Type
500ALift	500	p Type
1000ALift	1000	p Type
MOSC1	500	n Type
MOSC2	1000	n Type
MOSC3	500	n Type
MOSC4	1000	n Type
MOSC5	500	n Type
MOSC6	500	n Type
MOSC7	1000	n Type
MOSC8	1000	n Type

{4.1.3} PEROXIDE ACID CLEANING:

Cleaning of the wafers followed the RCA SSEE-100 acid-peroxide process [Kern and Puotinen, 1970], as detailed in the Appendix III. Rinsing in deionized water followed each step, which produced a smooth, shiny and very clean surface.

{4.1.4} RF SPUTTERING:

Radio Frequency Sputtering of Ta metal on the already clean Si substrates, was accomplished using a Perkin-Elmer 3140 Randex single target system, mounted on a NRC 703 Automatic Valve Control High Vacuum System. The sputtering was performed in Argon, with a partial pressure of 26 mTorr. The vacuum system evacuated the chamber to 10^{-6} Torr, as monitored by the baseplate Ionization Gauge (CHA Industries IG-101P Ion Tube and Consolidated Vacuum Corp. G1C-110A Ionization Vacuum Gage). Under these conditions, the sputtering rate was 15 nm/min, which was previously determined by D. Smith using the Sloan Angstrometer method [Smith and Young, 1981].

{4.1.5} THERMAL OXIDATION:

Thermal oxidation of the Ta films was performed in a Thermco Products Corp. Mini Brute resistance heated quartz tube (5 cm) furnace, with a Ana Lock 201 Controller. The temperature in the centre was set to 500 C, with +5 C difference at the edges, in order to compensate for heat loss, thus obtaining a "flat" temperature profile. Dry oxygen was manually regulated by a Brooks R-2-15-A tube

flowmeter, and set to a flow of 1.0 l/min (a Brooks tube reading of 9.4 cm). The oxidation time, a critical parameter, was varied considerably as described below, in order to determine its optimum value in function of the oxide quality.

TABLE 4.2

THERMAL OXIDATION OF TANTALUM ON SILICON

SAMPLE NAME	Ta THICKNESS	TEMPERATURE	TIME
N1	500 A	500 C	60 min
N2	1000 A	500 C	120 min
BNR500	500 A	500 C	93 min
BNR1000	1000 A	500 C	187 min
SampleA	500 A	500 C	3.5 hrs
SampleB	1000 A	500 C	3.5 hrs
500ALift	500 A	500 C	6.5 hrs
1000ALift	1000 A	500 C	10 hrs
MOSC1	500 A	400 C	5 hrs
MOSC2	1000 A	400 C	7 hrs
MOSC3	500 A	600 C	5 hrs
MOSC4	1000 A	600 C	7 hrs
MOSC5	500 A	Broken under processing	
MOSC6	500 A	600 C	5 hrs
MOSC7	1000 A	400 C	1 week
MOSC8	1000 A	600 C	7 hrs

{4.1.6} ALUMINIUM DEPOSITION:

Initially, some samples had an aluminium gate deposited using a Veeco model VE-400 Electron Beam equipment and a stencil metal mask. The bell jar was evacuated to 10^{-5} Torr before deposition took place. This method was replaced by the one described below, since the possibility existed of introducing an unknown factor, namely the high energy radiation from the E-Beam that could implant Al in the oxide, or damage the Si substrate at the interface. In either case, the results would be affected [Miner, 1981]. Aluminium metal was thermally evaporated (as opposed to Electron Beam, which is a high energy process) using a CHA Industries Model SE-600-RP Evaporator with a Auto Tech II controller. High purity 1% silicon aluminium wire (Cominco ALA 1793, 0.045" dia.) was cut into hoops of 2 cm lengths, and hung on the tungsten filaments. The chamber pressure was 10^{-6} Torr, before any evaporation took place. The evaporated thickness ranged between 600 and 1000 nm, as given by a Inficon Model 321 Quartz Crystal Film Thickness Monitor (a density of 2.73 was used for aluminium).

{4.1.7} PHOTOLITHOGRAPHY:

Photolithography was used to pattern the aluminium electrodes, a dot and ring mask was used with a negative photoresist process as described in detail in Appendix III. The dots have an area of 0.7854 mm^2 (1 mm diameter), and the rings provide electrical isolation.

{4.1.8} BACK CONTACT METALLIZATION:

The back contact was made by evaporating aluminium metal, using the same method described above for the gate electrodes. Again thermal evaporation was favored. Gold is the metal usually used in this application, however the large amount of wafers processed indicated that the cost would be prohibitive, thus aluminium proved to be an economical alternative with known processing techniques.

{4.2} MOS CAPACITORS WITH DOUBLE DIELECTRIC STRUCTURE:

The double dielectric Ta_2O_5-SiO_2 was used in a number of samples to evaluate its characteristics. This method of fabrication requires first the formation of a thin silicon oxide layer. Then a layer of tantalum metal is applied, followed by a dry thermal oxidation. After cleaning and marking, the processing steps are as follows:

a) Dry thermal oxidation in oxygen.

b) Tantalum RF sputtering.

c) Aluminium evaporation.

d) Patterning using photolithography.

e) Back contact metallization.

The thermal oxidation was accomplished in the same resistance furnace used for the tantalum oxidation, as described above. Experimentally, it was determined that the oxidation rate was very small [Tarr, 1980], about 1 A/min., for an oxygen flow of 1 l/min. The additional steps used in

this procedure are the same as before. The samples prepared using this technique are:

TABLE 4.3

DOUBLE DIELECTRIC MOS CAPACITORS

SAMPLE NAME	SiO_2 THICKNESS	Ta THICKNESS
20S20T	20 A	20 A
20S50T	20 A	50 A
20S100T	20 A	100 A
20S200T	20 A	200 A
50S100T	50 A	100 A
50S200T	50 A	200 A
50S500T	50 A	500 A
50S1000T	50 A	1000 A

The tantalum metal when fully converted into its oxide, will show an increase in thickness, by a factor of approximately 2, (the "swelling" factor) as detailed in Chapter 6. Hence, the values on the last column will produce a corresponding Ta_2O_5 film thickness twice as large.

{4.3} PROCESS AND FABRICATION COMMENTS:

This method of fabrication produced the required MOS Capacitors for the initial evaluation of the thermal Ta_2O_5 film on silicon substrates. The structure then has a Al-Ta_2O_5-Si configuration.
The conversion of the tantalum metal film into oxide is a rather lengthy process, and although previous authors gave

some indication of the time required for complete thermal oxidation of the metal film [Revesz et al.,1974; Smith and Young, 1981], it was felt that some experimentation should take place to determine the optimum oxidation time in terms of more critical parameters as conduction (leakage) current for a given voltage, and Capacitance-Voltage characteristics. Hence, a large amount of samples was produced, with different oxidation times, which varied from a few minutes (for very thin Ta films) to several hours (for thicker Ta films), and in one case for a few days. Furthermore, in some cases, the temperature was increased from the usual 500 C to 600 C, and in some cases reduced to 400 C, in order to determine the effect of the temperature variations on the C-V and I-V characteristics.

The film final color was purple-blue for the 50 nm samples, and gold-yellow for the 100 nm samples. This color difference was quite helpful in identifying each sample, if the case required. In both cases, the colors are intense and quite striking. The Si substrate was in most cases n type, however p type was also used, in order to establish possible differences in the quality of the Al-Ta oxide-Si capacitors. No attempt was made to use different substrate orientations, as this would have vastly increased the amount of variables in this work, and hence the total time required to complete the project.

In two cases (samples BNR500 and BNR1000), it was possible to obtain Ta films deposited by Magnetron Enhanced Sputtering (MES), in order to evaluate any possible

differences in the performance of the finished MOS capacitors. Silicon wafers were sent to the Solid State Laboratories of Bell Northern Research in Ottawa, Ontario; and processed by MES. A different cleaning method was used, as detailed in Appendix III. Besides this initial difference, the process followed for MOS Capacitors fabrication, was exactly the same as indicated before. Several attempts were made to process the Ta and Ta_2O_5 films in a way that would yield the MOS Capacitors with the oxide film only under the Al gate electrode, and not over the entire substrate. Etching of the Ta or Ta{oxide} film was mandatory, if the present processing technology was to be further extended to the fabrication of MOSFETs. The author had many frustrating experiencies in trying to pattern the Ta metal or Ta oxide film on Si substrates. The chemical solutions used went from the classical 10% HF and Buffered HF, to more stronger mixtures of concentrated hot HF, and even dangerous mixtures like "pirahna etch" (a hot solution of H_2SO_4 and H_2O_2) and "marabunta etch" (a hot solution of HNO_3 and NH_4F), names derived from a species of Amazonian ants, which devour everything upon their passage. The results were very unsatisfying, and in most cases severe damage resulted, either to the photoresist or to the substrate, in particular when the "Amazonian" solutions were used. It was amazing to observe both Ta and Ta_2O_5 films rest untouched by such strong chemicals.

{4.4} THE LIFTOFF TECHNIQUE ON TANTALUM FILMS:

A better processing method was in need, and the use of the Liftoff technique was developed for use with tantalum metal films. It is based on removing chemically (i.e., etching) a thin layer of aluminium metal, deposited first over the Si substrate, then patterned with a negative image of the required final shape. Then the tantalum film is deposited and by etching the underlying aluminium, the final positive pattern is obtained. The deposition methods vary considerably, but in this case, the Aluminium metal was evaporated and the tantalum metal was RF sputtered, using the same methods described above. The following steps were used, after the RCA SSEE100 cleaning step mentioned before:

1. Aluminium evaporation for liftoff.

2. Patterning of Al metal by photolithography, with negative image.

3. RF Sputtering of tantalum metal.

4. Liftoff of unwanted tantalum by aluminium etching.

Then the processing was continued as usual, i.e., the Al metal evaporation for gate electrodes, exactly as described above. The final etching required considerable time, from 60 to 90 minutes, depending on the original Al thickness, which varied from 600 to 1000 nm. Initially, no reaction was noticed, but after 10-20 minutes, gas bubbles appeared on the wafer's surface, indicating that the Al metal was attacked by the etchant solution. Towards the end of this

process, it was noticed that the tantalum metal surface
changed from a smooth appearance to a coarse and wrinkled
texture. The sample(s) then were carefully removed, rinsed
in de-ionized water and gently rubbed with a soft foam swab.
This is done to remove the unwanted wrinkled Ta film.
Interestingly, if the swab was made of cotton (i.e., a
common Q tip sold in drugstores), this one would severely
scratch the tantalum surface, as seen under a standard
optical microscope, or even naked eye. A foam swab (Sof-
Swab, Clean Room Products, Bay Shore, New York) proved to
leave a clean, scratch free surface. It was necessary to
leave the sample(s) in the etching solution for another 30-
45 minutes, in order to remove the residual Al/Ta from the
wafer. The end result was a clean, well defined pattern of
tantalum metal, with no damage to the silicon substrate.
After this, then the process could continue as described
before.

{4.5} MOS CAPACITORS WITH ANODIC Ta_2O_5 AS INSULATOR:

Another possible way of producing tantalum pentoxide
films is by anodic oxidation of a thin layer of Ta metal.
Several authors have reported this method [Berry, 1959;
Young, 1961; Dell'Oca et al., 1971] as a very reliable one
that produces films of superior quality and, of course, much
faster than the dry thermal oxidation of Ta films. However,
the previous work only dealt with insulating substrates (for
example glass or alumina) or conductive ones (a plate of Al
or Ta) which further simplified the problem of making

electrical contact to it. In this case, the substrate was silicon, a semiconductor, and a practical solution had to be found for making a good electrical contact to the Ta film on Si.

A possible solution is to allow the current to flow through the cross section of the silicon substrate, if the proper type is chosen. By taking into account the current direction in the substrate, and noting that the tantalum electrode is the anode, the electronic current flow dictates that a p-Si type substrate is the only possible choice, as this will make the Ta-pSi diode forward biased. If a n-Si substrate is used as the case is, the Ta-nSi diode is then reversed biased and the anodization current will be blocked. Hence, a good direct contact must exist to the silicon surface, if the substrate is p type. This was accomplished by etching a small strip close to the flat, in the wafer's face. Under these conditions, it is then feasible to anodically oxidize a thin layer of Ta metal previously deposited on the silicon substrate. However, care shold be taken NOT to grow an anodic oxide of silicon, which would produce a layer of SiO_2 under the already formed anodic Ta_2O_5. This condition can be detected by monitoring the voltage across the anodization cell, as a function of time, when a constant current flows through it. The rate of voltage increase dV/dt is constant for a constant current density through the electrolyte [Dell'Oca et al., 1971]. The metal will be fully converted into its oxide, when the voltage across the cell reaches Vlimit of the constant current source. At this point the

process is interrupted. Also, any gas escaping from the anode (usually oxygen), indicates that a further change is taking place on the silicon surface: the growth of a SiO_2 layer. It is also known, that by applying a constant voltage to the cell, after the constant current process, it is possible to obtain a better quality oxide film [Young, 1961]. This is based on experimental evidence that a certain "healing" effect takes place on weak spots or areas in the oxide film itself. The anodization cell and associated equipment are shown in Figure 4.1, for both constant current and constant voltage processes.

Based on these principles, the following steps were used in producing anodic tantalum on silicon substrates, after the RCA SSEE100 cleaning process:

1. RF Sputtering of tantalum metal.

2. Back contact by aluminium evaporation.

3. Anodic oxidation at constant current, voltage monitored as a function of time.

4. Application of constant voltage to the cell, current monitored as a function of time.

5. Rinsing in de-ionized water to remove all traces of electrolyte solution.

The processing then continues as before, with the Al evaporation for gate electrodes, being the next step. Table 4.4 gives further details of the wafers and electrolytes used.
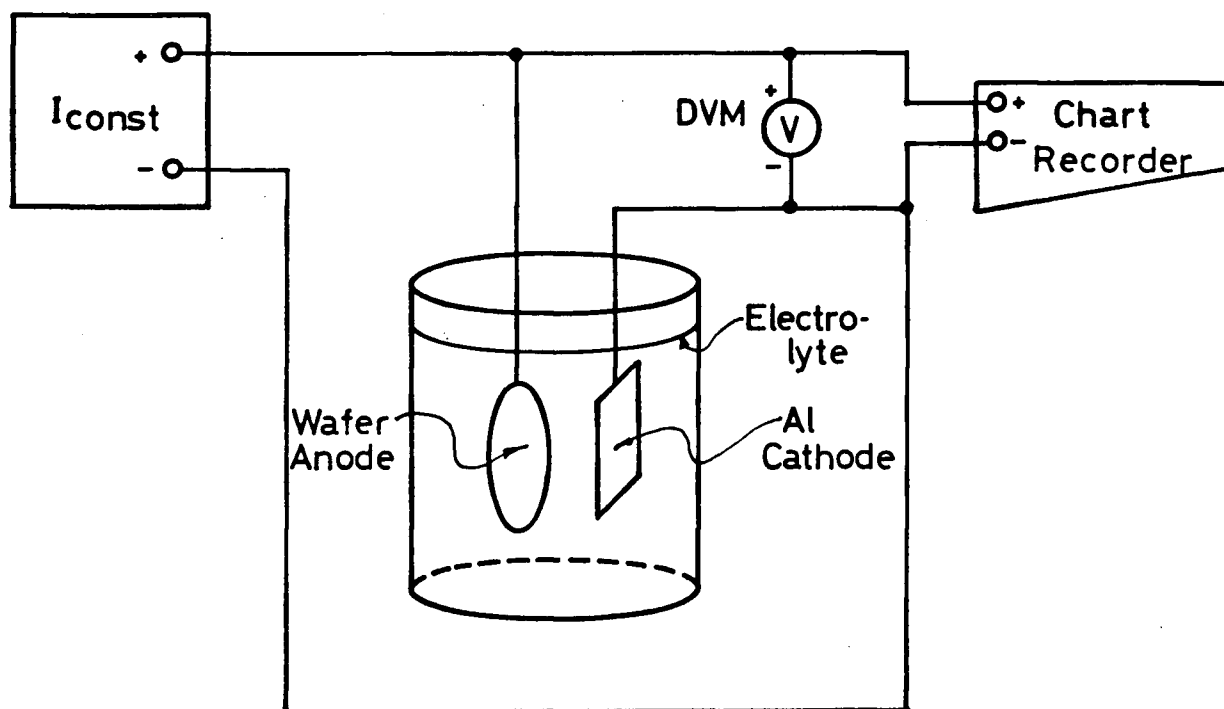
Constant Current Phase

Constant Voltage Phase
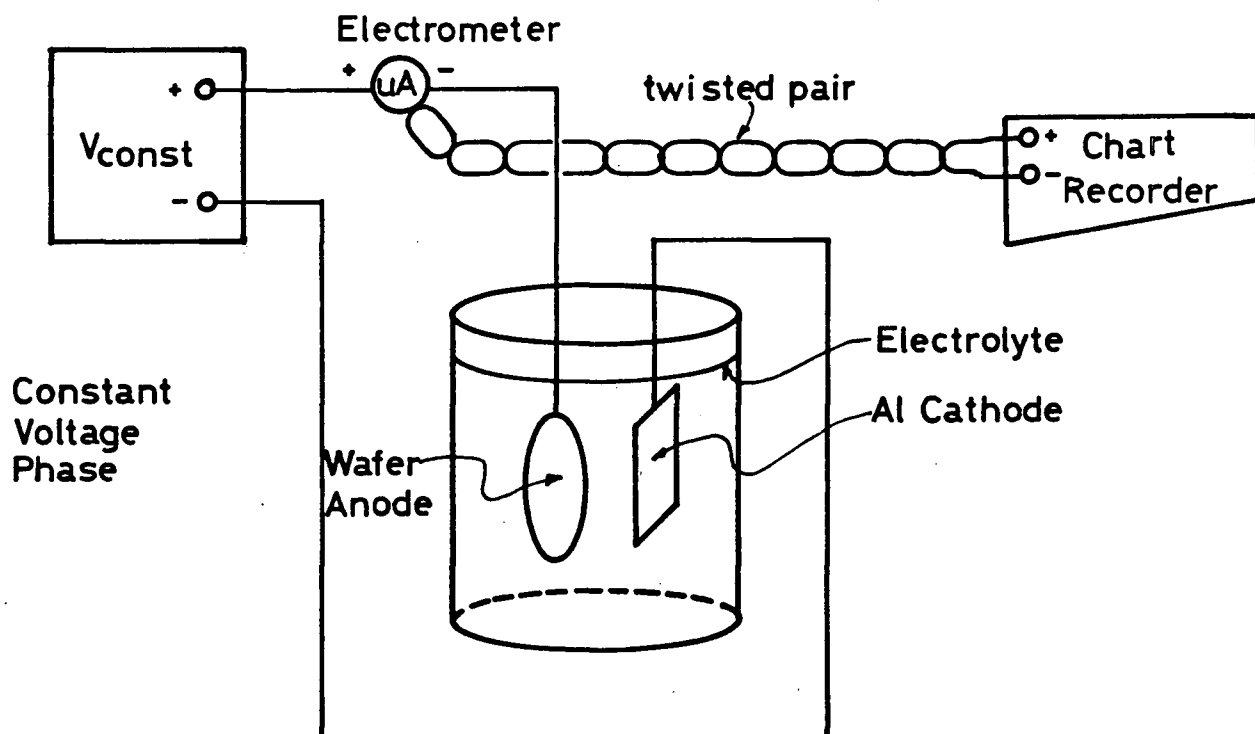
Figure 4.1 Anodization Cell and Equipment

{4.5.1} ANODIZATION IN CITRIC ACID ELECTROLYTE SOLUTION:

A good contact is required to the anode, and the back Al contact performs this function quite well. A current density of 1 mA/cm² was used for the Constant Current process, a value that has been proven to form good quality films [Young, 1961]. The surface area of a standard 2 inch Si wafer is very close to 20 cm², and a current source set to 20 mA was used (Hewlett-Packard 6186C) with a maximum voltage setting of 100 volts. The voltage across the cell was recorded as a function of time, with a chart recorder (Moseley Autograph 7100BM Strip Chart Recorder). The anodic oxidation of tantalum films is a relatively fast process, in 3-5 minutes a film of 100 nm is fully converted to its oxide. The oxidation time is determined from the rate of change of the cell voltage, as explained before. This is in sharp contrast with the time under thermal oxidation, a few hours. It is quite amazing to observe the sudden change in color of the Ta surface, denoting the formation of an oxide film, in the first few seconds. The final color was light blue for a 50 nm Ta sample, and gold for a 100 nm sample, in agreement with the thermal oxide films, for the same tantalum metal thickness. At this point the Constant Current process is interrupted, to be followed by the application of a Constant Voltage for a certain time. The applied voltage corresponds to the operating voltage of the MOS Capacitor, in this case not more than 20 volts. Based on data given by Dell'Oca et al. (1971), 1-3 hrs., is the usual time for this process. Therefore, a constant voltage of 20 V was applied
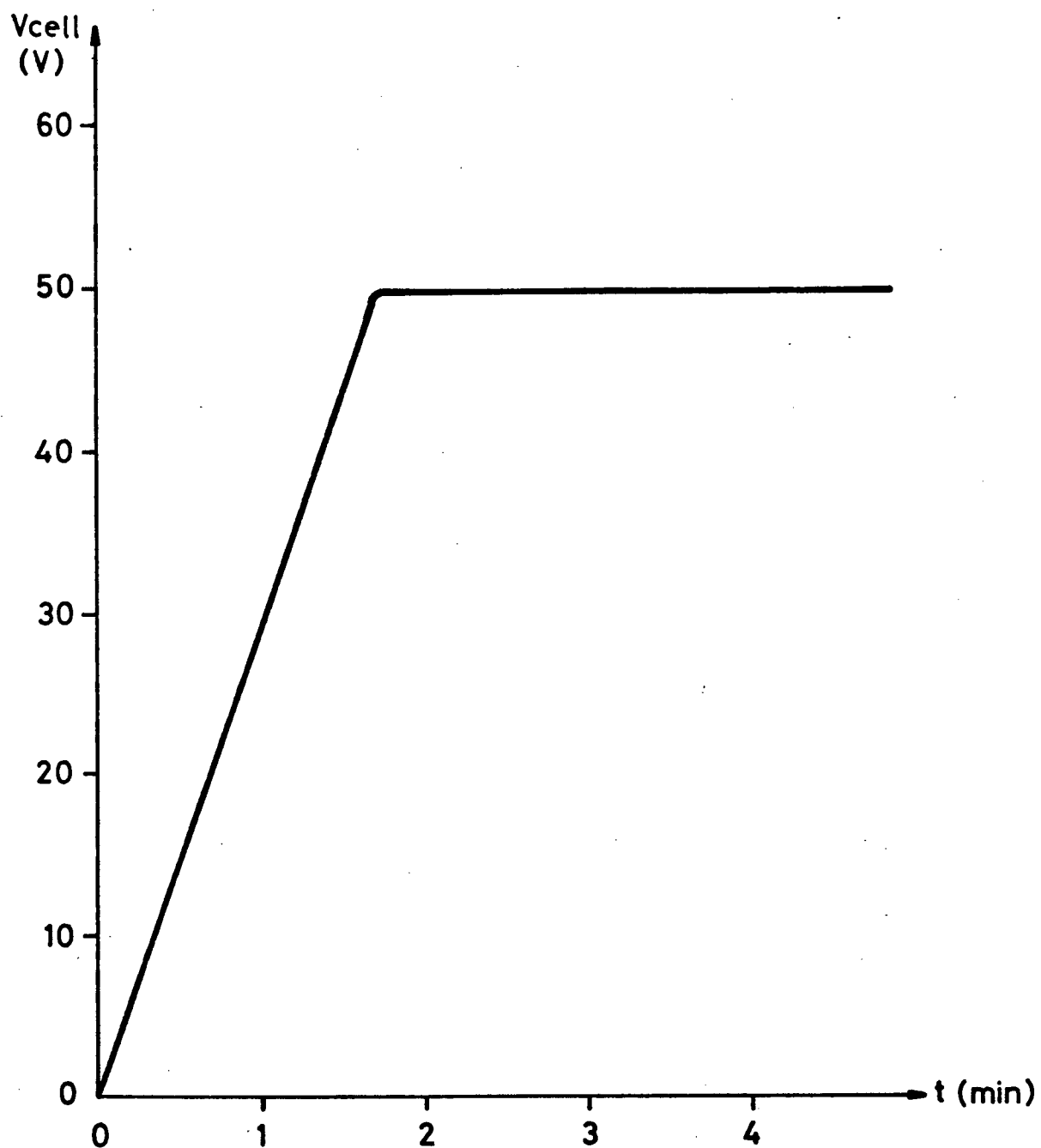
Figure 4.2 Anodization Cell Voltage under Constant Current
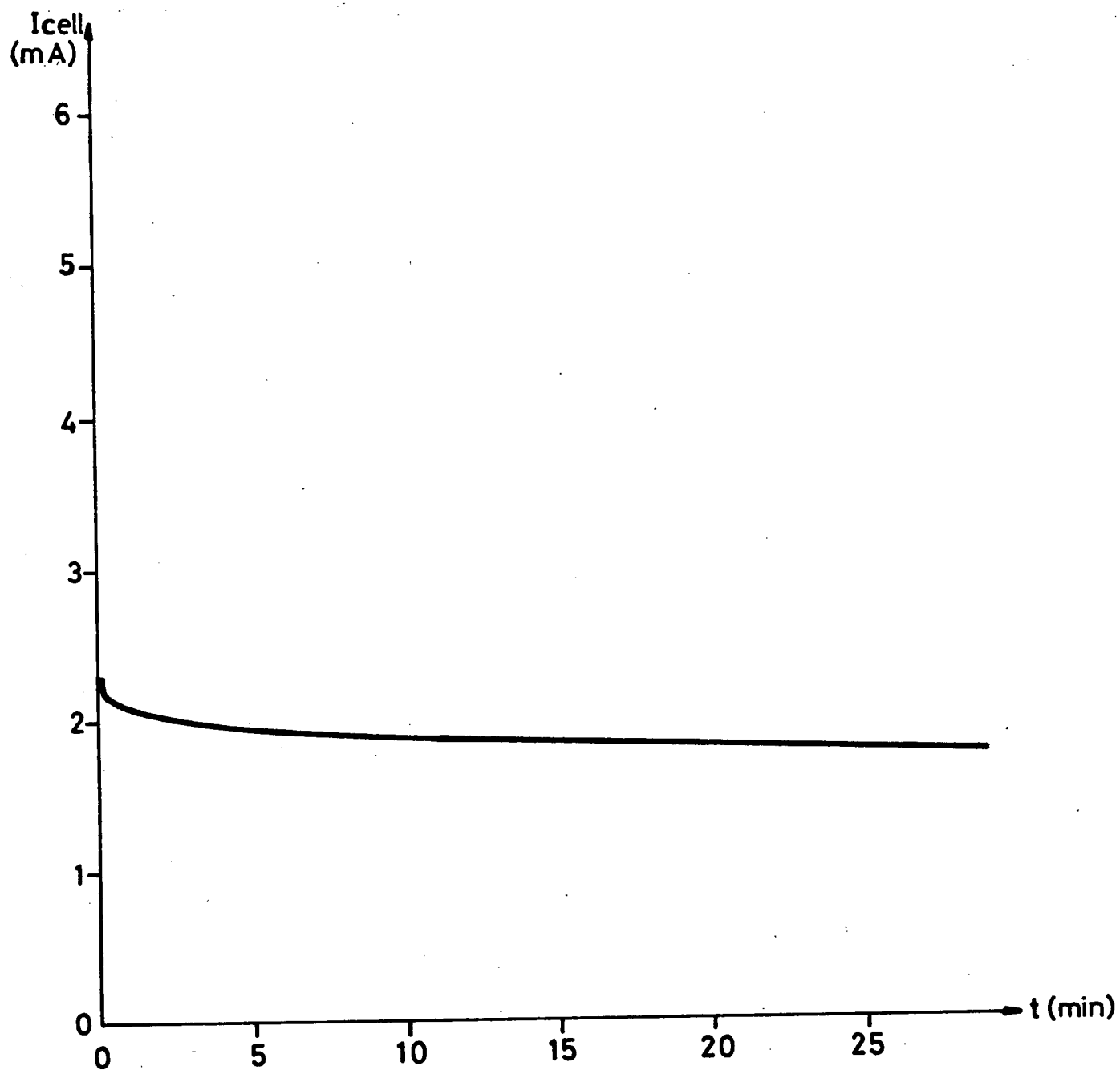
Figure 4.3 Anodization Cell Current under Constant Voltage

to the cell for 1 hr., and the leakage current monitored with an electrometer (Keithley 602) driving a chart recorder. The results of these measurements are shown in Figures 4.2 and 4.3. Note the sharp change of voltage under constant current and the diminishing leakage current under constant voltage.

{4.5.2} ANODIZATION IN H_3PO_4 ELECTROLYTE SOLUTION:

The classic electrolyte for anodic oxidation of tantalum has been an aqueous solution of citric acid [Berry, 1959 and 1963; Young, 1961; McLean, 1966], however it was decided that another electrolyte should be also used in order to compare the film quality and the resulting MOS capacitor performance. The results given by Randall et al. (1965), indicate that an aqueous solution of phosphoric acid produces a better quality film, as it reduces the ionic conductivity in MOS devices that use tantalum oxides. Solutions of 0.1 M were prepared in both cases, as this concentration had produced good results for previous authors [Young, 1961]. Both electrolyte solutions were used, and differences were apparent once the anodic oxidation took place and the V(t) charts (constant current) compared. The anodic samples were then rinsed in de-ionized water, to remove all traces of the electrolyte solutions, and then boiled in isopropyl alcohol to remove any water in the wafers. Appendix III gives these in further detail.

TABLE 4.4

SINGLE DIELECTRIC ANODIC MOS CAPACITORS

SAMPLE NAME	Ta THICKNESS [A]	ELECTROLYTE
MOSC9	500	Citric Acid
MOSC10	500	Citric Acid
MOSC11	1000	Phosphoric Acid
MOSC12	500	Phosphoric Acid
MOSC13	500	Citric Acid
MOSC14	500	Phosphoric Acid
MOSC15	1000	Citric Acid
MOSC16	500	Phosphoric Acid
MOSC17	500	Citric Acid
MOSC18	1000	Citric Acid

{4.6} INTERFACIAL OXIDATION MOS CAPACITORS:

A new technique, Interfacial Oxidation, was used in fabricating MOS capacitors, as this allows the oxidation of silicon through a film of thermally grown tantalum pentoxide. This process departed from the one reported by previous authors [Kato et al., 1983], in which a film of tantalum pentoxide was deposited on silicon substrates, and then followed by a wet oxidation at 800C. The principle behind this procedure is that the oxidizing gases will travel through the outer Ta_2O_5 film and grow a film at the interface of SiO_2. However, no indication was given in their paper on the tantalum pentoxide film and its origins. The insulating structure is then a double dielectric one, with an outer insulator of Ta_2O_5 and an inner insulator of SiO_2.

The procedure followed by this writer and Dr. P. Janega, was slightly different and it has the advantage of growing thermal oxides for both Ta metal and Si. The processing steps are as follows:

1. Thickness and four point resistivity measurements.
2. Scribing and marking.
3. Peroxide-Acid cleaning using the RCA process.
4. RF Sputtering of tantalum metal.
5. Thermal oxidation of tantalum in dry oxygen.
6. Wet oxidation of silicon.
7. Aluminium evaporation for gate electrodes.
8. Patterning of Al metal by photolithography.
9. Back contact by gold evaporation.

The first five steps have already been discussed previously, and they are detailed in Appendix III.

The wafers had 500 A of Ta metal deposited by RFS and were oxidized thermally, following the same method as described before and given in Appendix III, the only difference being an oxygen flow of 1.5 l/min, instead of the usual 1 l/min. The color was deep purple-blue, indicating that the Ta metal was properly oxidized. The wafers were then introduced into the wet oxidation furnace at 800C, for varying periods of time and cycles, in order to determine the effect of oxidation time on the quality of the double dielectric structure. Table 4.5 summarizes the results.

TABLE 4.5

INTERFACIAL OXIDATION OF TANTALUM ON SILICON

SAMPLE	Ta THICKNESS	WET OXIDATION CYCLE
MTJ1	500 A	3-54-3 min.
MTJ2	500 A	3-114-3 min.
MTJ3	500 A	3-54-3 min.
MTJ4	500 A	3-24-3 min.
MTJ5	300 A	None

The wet oxidation gas flows are given in Appendix III, the first digit indicates the time of oxygen flow, the second of oxygen + hydrogen and the last of oxygen only.

Examination of the samples showed that the Ta{oxide} film did not deterioriate during the wet oxidation. Aluminium was deposited by use of the E-Beam technique and later patterned by photolithography using positive photoresist. Gold was deposited on the wafers back using also the E-Beam equipment. The sample marked MTJ1, with electrodes in place, was annealed in nitrogen at 500C for 3 min. The remaining ones had no annealing treatment.

CHAPTER 5

RESULTS AND MEASUREMENTS ON MOS CAPACITORS

Once the MOS capacitors and devices were fabricated, a proper set of systematic mesurement procedures was implemented. In the case of MOS capacitors these consisted of:

1) Ellipsometric Determination of Oxide Thickness.

2) Capacitance-Voltage (C-V) Curves.

3) Current-Voltage (I-V) Curves.

{5.1} ELLIPSOMETRY:

The oxide thickness determination was done using a Rudolf Model 43603-200E Ellipsometer controlled by a PDP8/E Digital Equipment Corporation minicomputer; with a RL-01 disc drive, magnetic tape unit, A/D and D/A converters, running OS/8 under real time and using previously reported techniques [Hopper et al., 1975; Cornish et al., 1973] and software developed by D. Smith (1980). A Spectra Physics Model 133 helium-neon laser, provided the light source, a beam of red color at 632.8 nm. The ellipsometer angle of incidence was 70° and measurements made in zones I and III. The ellipsometric parameters Ψ and Δ were then converted to thickness using the transparent single layer model equations, given the refractive index of the film. Several measurements are usually taken, and these are then averaged.

The software residing in the computer controls the rotation of a pair of small stepper motors, which in turn drive, through reducing gear boxes the Analyzer and Polarizer optics of the Ellipsometer. The angular position of these are accurately given by two resolvers (shaft encoders), coupled via reducing gear boxes to the Analyzer and Polarizer motor driven units. The control system is then a position feedback type and the software resident in the computer attempts to find a balance (null) of the transmitted light as sensed by a photodetector placed at the output of the Analyzer optics. An initial null or balance is initially performed manually, in order to give a good starting point to the computer control software, thus minimizing the posibility of an error and also reducing the measurement time.

{5.2} C-V MEASUREMENTS:

The Capacitance-Voltage (C-V) measurements were obtained also by a computer controlled method [Boyd, 1981]. The measuring system is shown in Figure 5.1. A Boonton Model 71A Capacitance Meter, connected to an optically and electrically shielded test jig box provided the capacitance information to the computer, via the A/D interfacing unit. The biasing voltage is provided by a D/A converter and it is offset by an opposing voltage source, which can be manually adjusted to a desired value. This allows the user to obtain a C-V plot for negative gate voltages, without resorting to special and expensive D/A converters. The biasing voltage is

monitored by a Dana Model 5900 Digital Voltmeter, which in turn serves as a feedback A/D converter. Then by appropiate commands from the computer, the gate bias voltage can be incremented and the capacitance measured. A resident software module, CV.PG was used in obtaining the C-V curves. The source program allows for plotting the experimental data, a theoretical curve, calculating the flatband capacitance and provides calculated values of oxide thickness, surface state density, etc. [Boyd, 1981]. The curves were plotted by a Houston Instrument Complot XY plotter, driven by the PDP8/E minicomputer. This arrangement provided a fast and efficient way to obtain the vast amount of C-V curves from a large amount of samples, which each contained several MOS capacitors.

From the C-V curves, a great amount of information can be obtained. The insulator (oxide) thickness can be calculated from the accumulation layer capacitance, if the capacitor area and insulator permittivity is known. The irregularities in the curve indicate usually the presence of surface states, of the "fast" kind, as they follow the sweep component applied to the Capacitance Meter. The hysteresis, if any, and its orientation can reveal the presence of the mobile charge in the insulator. By comparing with an ideal curve around the origin, the flatband capacitance and voltage can be obtained. The flatband voltage is given by:

$$V_{fb} = \phi_{ms} - Q_f/C_{ox} \qquad\qquad (5.1)$$
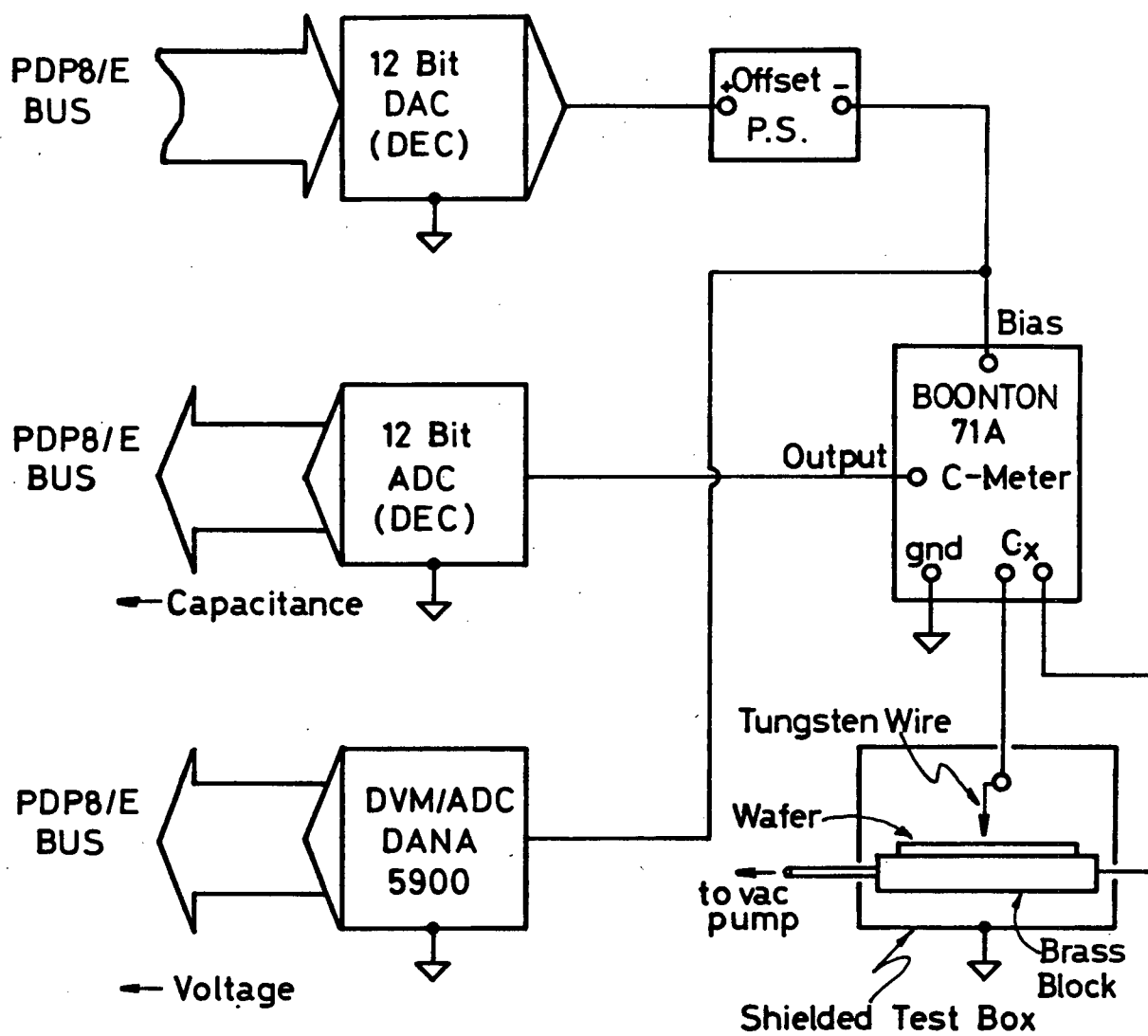
Figure 5.1 C-V Measuring System for MOS Capacitors.

Where the metal to semiconductor work function is given by ϕms and Qf is the net charge at flatband per unit area [Sze, 1969]. Then, the flatband capacitance can be calculated:

$$C_{fb} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{q} \sqrt{kT/\varepsilon_s N_{A,D}}} \qquad (5.2)$$

The slope of the C-V curve can be used to calculate the "fast" surface state density:

$$N_{ss(fast)} = \frac{C_{ox}}{q\phi_F}(\Delta V_a - 2\phi_F) \qquad (5.3)$$

The quantity ΔVa represents the actual slope of the curve and $q\phi_F = Eg/2 + kTln\{ni/Na\}$.

The "slow" surface states, caused by polarization of the insulator and mobile ionic charges, produces hysteresis in the C-V curve. A good estimate of these is given by [North, 1980]:

$$N_{ss(slow)} = \frac{C_{ox}}{3q\phi_F} \Delta V_h \qquad (5.4)$$

Where the hysteresis width around flatband is represented by ΔVh.

The C-V data can be replotted in the form of the inverse of the capacitance squared vs. the gate bias voltage ($1/C^2$ vs V). Linear extrapolation of the replotted data to the

voltage axis gives the diffusion or built-in potential [Sze, 1969]. This method was used in papers by Padmanahban (1975) in relation with WO_3 and MoO_3 films, and by Makus (1977) in their work on V_2O_5.

{5.3} I-V MEASUREMENTS:

The I-V data was obtained by measuring the DC current flow through the MOS capacitors, under both positive (Al electrode) and negative gate voltage. A computer source program was written by this author, that would sequentially increment the gate bias voltage and then read the current flowing in the circuit. Then the data is stored temporarily and the user has the option of plotting a linear (I vs. V) plot or a so called Schottky (log I vs. $\sqrt{V}$). The details of the source program written in FORTRAN IV which runs in the PDP/8E minicomputer, are given in Appendix II. The I-V measuring system is shown in Figure 5.2. A Keithley Model 602 Electrometer is used to measure the leakage current, which in turn is connected to a Keithley Model 399 Isolating (buffer) Amplifier. Then it feeds a Tyco Model 404 DVM-A/D converter, which is interfaced with the computer. The gate voltage is provided by a D/A converter, driven by the resident software in the minicomputer, and it is monitored by a Dana Model 5900, which serves as both indicating DVM and A/D converter. There is a protective current limiting resistor placed directly at the output of the D/A converter, usually set to 100 ohms, which has a negligible effect on the measurements. This arrangement allows use of the

computer and interfacing circuits to acquire I-V data in a fast and efficient way. The software was written so that the user chooses the instrument scales, maximum gate voltage and number of increments, which are entered via keyboard commands into the computer. There is a choice of plotting the data, with and without axes (for several curves in the same sheet), and of a Linear or Schottky graph. All scaling is done automatically and the axes labelled according the type of plot and range of recorded values.

All measurements were made in an electrically and optically shielded box, which contained the test jig. Care was taken to avoid ground loops and noise, as the measured leakage currents were in the nA range. Extensive use of shielded low loss cables was made and the test jig was cleaned with isopropyl alcohol, before each batch of mesurements were taken. This ensured that any surface leakage of the exposed conductors (due to dust, contamination or water vapour) was minimal.

The intention of providing the I-V data in Linear or Schottky form is in the first case to give an overall idea of the I-V characteristic and in the second to obtain more information of the insulator, by examining the slope of log I vs. $\sqrt{V}$. From this one, it is possible to calculate the optical (high frequency) value of the insulator permittivity. However, the classic question of whether the conduction mechanism is Schottky or Poole-Frenkel has to be answered first, otherwise the calculated $\epsilon r(\infty)$ will be in error by a factor of 2. This can be seen from the expression
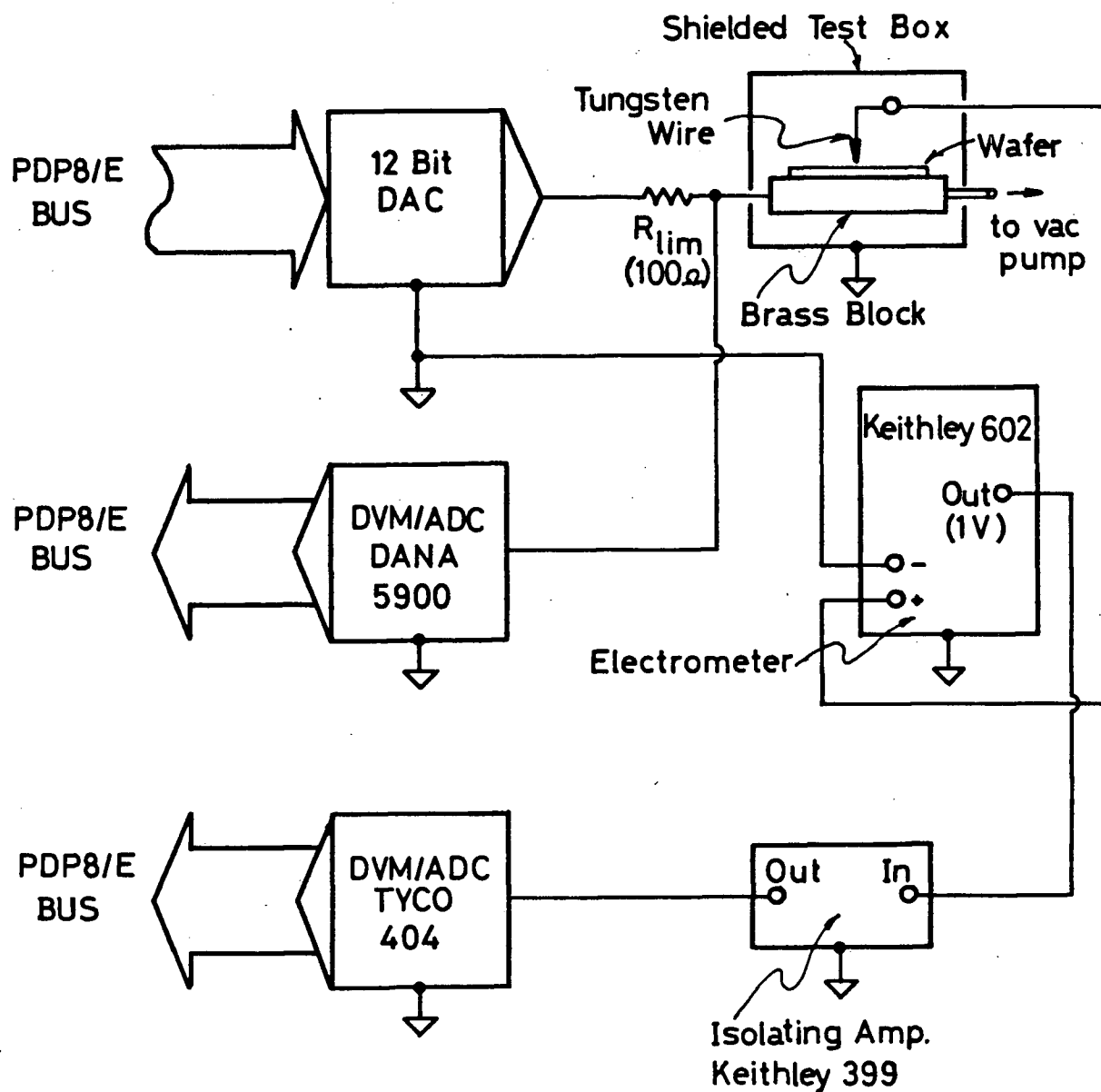
Figure 5.2 I-V Measuring System for MOS Capacitors

of the P-F conduction:

$$J_p = q\mu N_c E \exp(-q\phi_0 + \beta_{pf}\sqrt{E})/kT \qquad (5.5)$$

When this expression is plotted in the Schottky form, and the plot is a straight line, its slope gives the Poole-Frenkel lowering constant βpf:

$$\beta_{pf} = \{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}\}^{\frac{1}{2}} \qquad (5.6)$$

The permittivity can then be calculated from:

$$\varepsilon_r(\infty) = \frac{\pi\beta_{pf}^2}{\varepsilon_0 q^3} \qquad (5.7)$$

On the other hand, the Schottky conduction current density is given by:

$$J_s = A^*T \exp(-q\phi_s + \tfrac{1}{2}\beta_{pf}\sqrt{E})/kT \qquad (5.8)$$

Where A^* is the Richardson constant. The slope, if the Schottky plot is a straight line, is then half of the Poole-Frenkel mechanism. Unfortunately, there is no easy way of determining whether the conduction is P-F or S, from the examination of a straight line plot in the form of log I vs. $\sqrt{V}$. More information from the conduction process is required, and it has been suggested that from internal photoemission measurements [Dell'Oca, et al., 1971], the Frenkel vs. Schottky dilemma can be solved. The

photoemission threshold energy is a function of the applied voltage across the insulator, at the interface between the metal and insulator, hence defining Schottky type emission [Goodman, 1968]. In their now classic paper, Angle and Talley (1978) indicated that the kind of conduction mechanism can be determined by examining the forward (gate positive) and reverse (gate negative) bias Schottky plots. If the slopes are the same and have nearly the same intercept, under both reverse and forward bias, Poole-Frenkel conduction is taking place; i.e., the conduction is bulk-limited and not electrode limited. If Schottky emission is responsible, then the differences in work functions between the Al and the Si substrates will lead to forward and reverse currents of several orders of magnitude different.

As it can be seen later, not all the Ta_2O_5 samples have measured straight line Schottky plots, which suggests that the real conduction mechanism is more elaborate than the already proposed ones. Furthermore, forward and reverse bias plots have large current differences of several orders of magnitude.

{5.4} HILLOCK FORMATION INVESTIGATION:

Through our experimental work, it was found that when Ta metal was RF Sputtered on clean Si substrates, hillocks or "measles" appeared on the surface. These small protuberances are formed probably as a consequence of thermal stresses on the Ta metal during and after deposition

[Miner, 1981]. Close examination with the microscope under dark field (Figures 5.3 to 5.8) reveals a "star sky" or "milky way" pattern, which indicates a relatively high area density of hillocks. However, it was found that this is quite typical of RF Sputtered tantalum [Galeener et al., 1980, Westwood et al., 1975], and an attempt was made to establish a possible link between contamination levels, hillocks and possibly pinhole formation. It is interesting to notice that in the paper by Galeener et al., niobium pentoxide exhibits a similar surface condition, but to a lesser degree. These authors also reported that in silicon nitride, hillocks were not seen. They indicated that these are quite small, in the case of Ta, 100 A is a typical lateral dimension. Hillock growth also appears as an unwanted source of defects in evaporated Al over Si substrates, and they have large dimensions, typically a height of 10 times the deposited thickness. This creates a very serious problem if the passivation or photoresist fails to cover them [Santoro and Tolliver, 1971]. In more recent work [Jakson and Li, 1982], the hillock and void growth on thin films (1 μm or less) deposited on relatively massive substrates is governed by thermal compressive stresses and the growth kinetics are controlled by a bulk process, as opposed to grain boundary diffusion. Under observation, hillocks will grow and shrink with temperature changes, however a certain degree of hysteresis exists, as repeated cycling promotes growth.

In order to quantify the possible effect of contamination

(mainly dust particles), clean and "dirty" glass samples (Corning 7059) were prepared and introduced to the RF Sputtering equipment. Tantalum deposition was done in an argon gas atmosphere at a rate of 100 A/min., under a forward RF power of 120 W. Residual gases indicated a pressure of $1-2\times10^{-6}$ Torr, and the argon partial pressure was 25-30 mTorr. Microscope examination under dark field followed. Only a relative measure is given, as no actual count of the number of hillocks per unit area was done. Results are given in Table 5.1.

TABLE 5.1

RF SPUTTERING OF Ta ON GLASS SAMPLES

SAMPLE NAME	CONDITION	THICKNESS	HILLOCK DENSITY
G100	Clean	100 A	Normal
G500	Clean	500 A	Normal
G500D	Dirty	500 A	High
IG500	Clean	500 A	Normal
310181C	Clean	500 A	Normal
310181D	Dirty	500 A	Normal
040281C	Clean	500 A (*)	Low
040281D	Dirty	500 A (*)	Low
110281C1	Clean	500 A (#)	Very Low
110281C2	Clean	500 A (#)	Very Low
180281C1	Clean	500 A ($)	Low
180281C2	Clean	500 A ($)	Low
180281C1	Clean	1000 A (&)	High
180281C2	Clean	1000 A (&)	High

Notes:

(*) 0.22 μm filter installed in Argon line.

(#) RFS Equipment thoroughly cleaned.

($) Vacuum 10^{-7} Torr.

(&) Sample sputtered again.

It is not conclusive whether the cleanliness of the glass sample is related to the density of hillocks, however there is some correlation beteween the contamination of the RFS equipment and the amount of hillocks. It appears that the effect of cleaning, decontaminating and installing a submicron filter in the Ar gas line produced some positive effects, as the hillock growth diminished. There seems to be also some correlation with the stability of the plasma during sputtering. Experimentally, we observed that when the plasma behaved in an erratic way, with secondary arcs moving randomly, the hillock growth was affected. No conclusive evidence could be found, as the number of samples is too low, the randomness of the secondary arcs cannot be accurately described, and not in all cases was there a noticeable effect. Microscope examination under dark field conditions show no correlation with observations done in a transmission microscope (Union Optical, metallurgical, Model MeC-3Bi) in attempting to find pinholes. The glass samples examined with the transmission unit gave very little pinhole count (10-20) over the entire 2" wafer. Figures 5.3 to 5.8 show the "star sky" pattern for several Ta-RFS glass and Silicon samples, and Ta-MES on silicon. It appears that the MES samples (BNR supplied) have less hillock density, although the magnification is higher. Upon examination under the transmission unit, the pinhole density is less than the RFS samples, which again indicates perhaps a better quality Ta film for the MES samples.
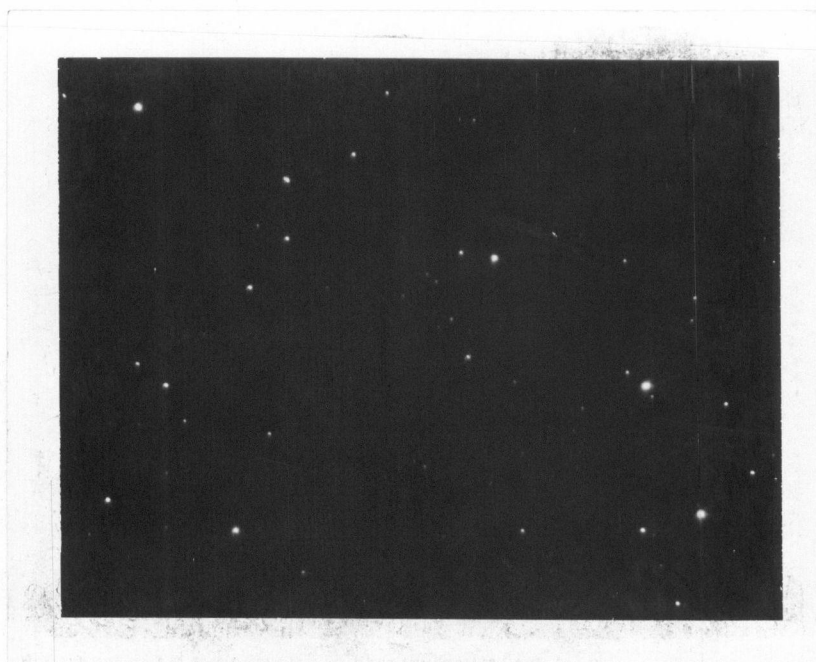
Figure 5.3 Dark Field Photograph (560X), 500 A Ta RF
Sputtered on Glass (sample G500).
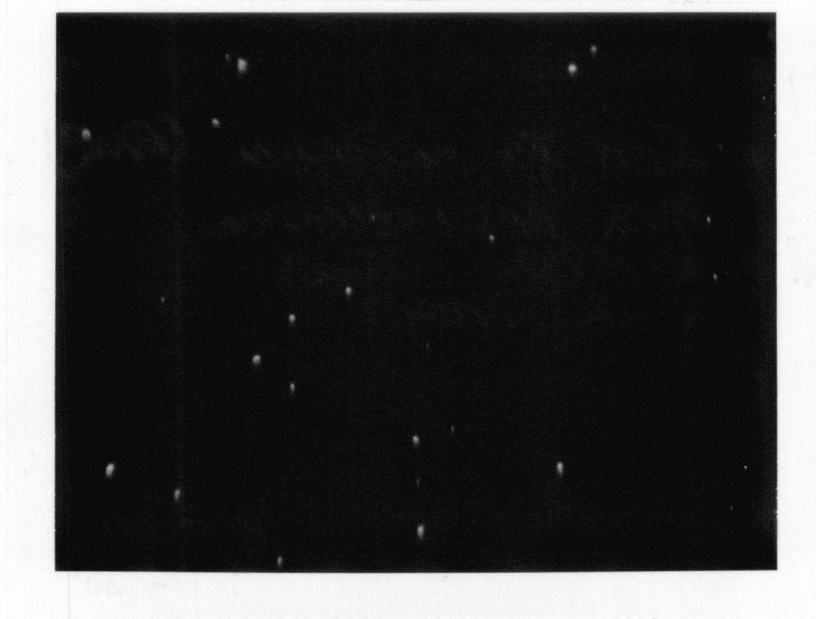
Figure 5.4 Dark Field Photograph (560X), 500 A Ta Magnetron
Enhanced Sputtered on Silicon (sample BNR500).
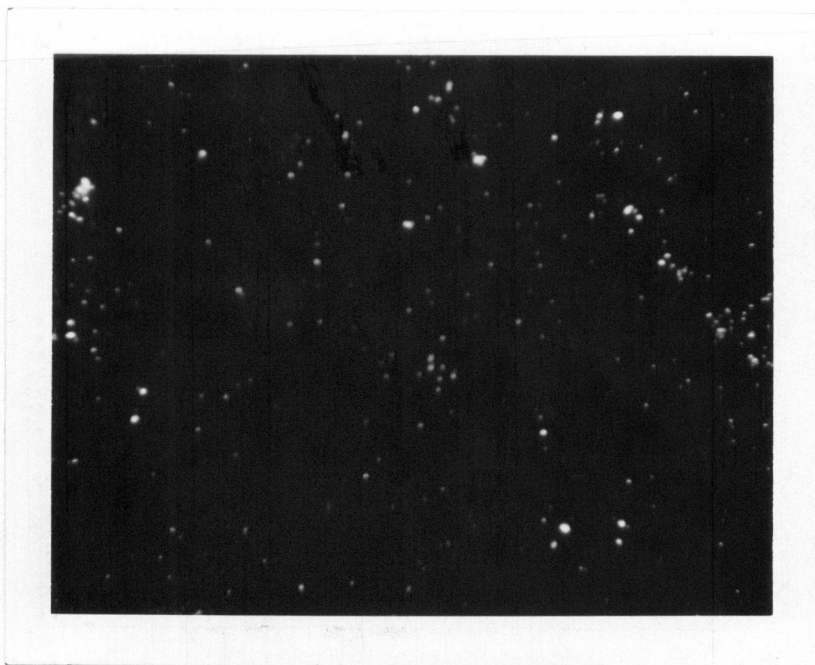
Figure 5.5 Dark Field Photograph (140X), 200 A Ta RF
Sputtered on thin SiO_2 on Silicon (sample 4T6).
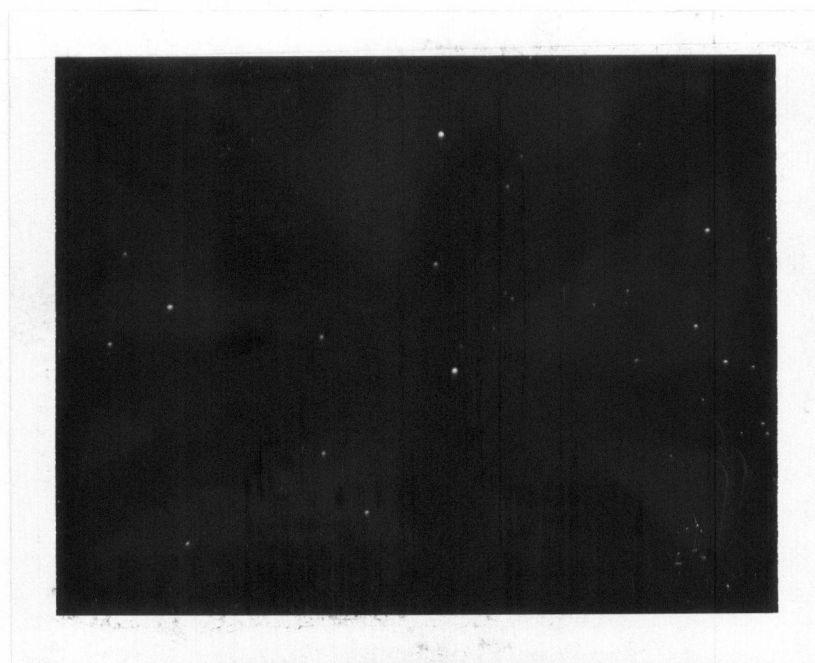
Figure 5.6 Dark Field Photograph (140X), 50 A Ta RF
Sputtered on thin SiO_2 on Silicon (sample 2T6).
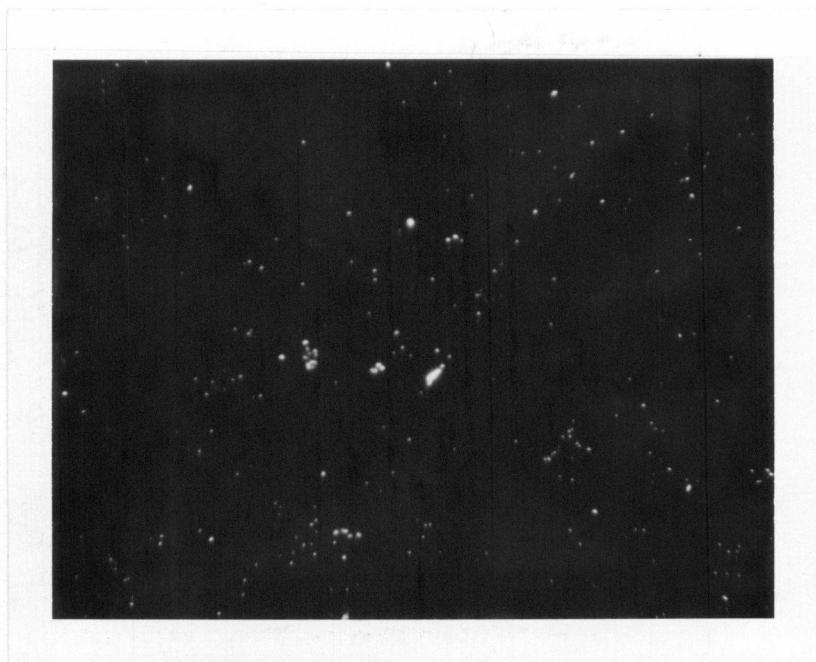
Figure 5.7 Dark Field Photograph (140X), 500 A Ta RF
Sputtered on thin SiO_2 on Silicon (sample 3T7).
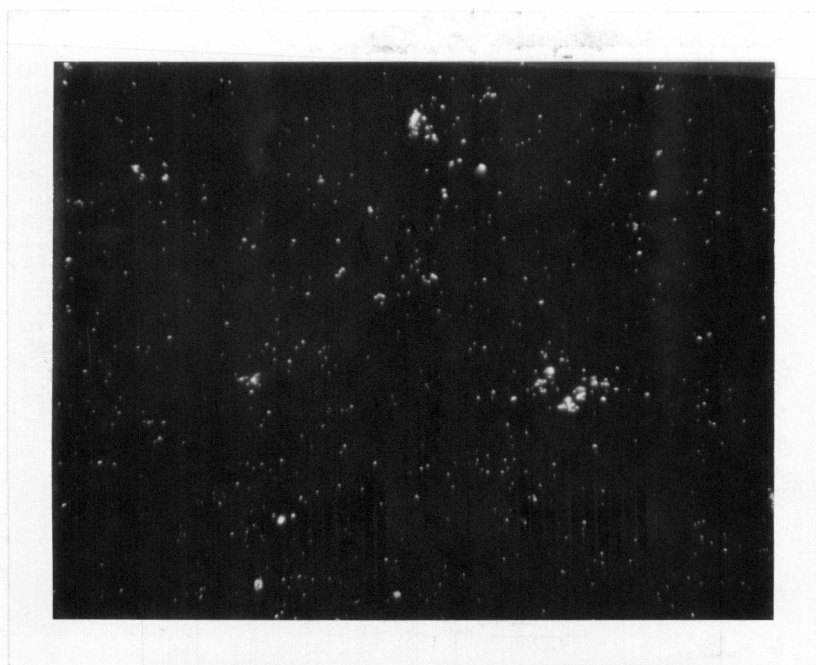
Figure 5.8 Dark Field Photograph (140X), 1000 A Ta RF
Sputtered on thin SiO_2 on Silicon (sample 4T7).

{5.5} DISCUSSION OF RESULTS:

{5.5.1} ELLIPSOMETRY:

Data obtained from the samples BNR500 and BNR1000, in which the ellipsometric parameters Ψ and Δ were periodically measured during the dry thermal oxidation, is shown in graph form in Figure 5.9 and 5.10. Sample BNR500 (500 A Ta thickness) exhibits a rather sharp peak of 48 degrees for Ψ at 15 min, as opposed to a broad peak of 50 degrees but at 60 min oxidation time for for sample BNR1000 (1000 A Ta thickness). The parameter Δ decreases monotonically with increasing time. The apparent discontinuity of the Δ curves is due to its modulo 2π property, i.e., they repeat themselves after 360 degrees.

It is expected that both parameters assume a constant value after long time. Indications of this are apparent from the BNR500 sample curves, and a trend is given in the curves for the sample BNR1000. This indicates that, after a period of time, slow changes take place in the ellipsometric properties of the oxide. Following Smith and Young (1981), this is interpreted as the metal being entirely converted into oxide, with slow changes attributed to changes in stoichiometry and structural annealing. It is interesting to observe that the Ψ and Δ curves vs. time obtained in this work are similar to the ones published by these authors. They report a sharp peak of 46 degrees at 20 min. for the Ψ parameter, for a 400 A thick tantalum film that is thermally oxidized. A similar situation exists for Δ, in which the
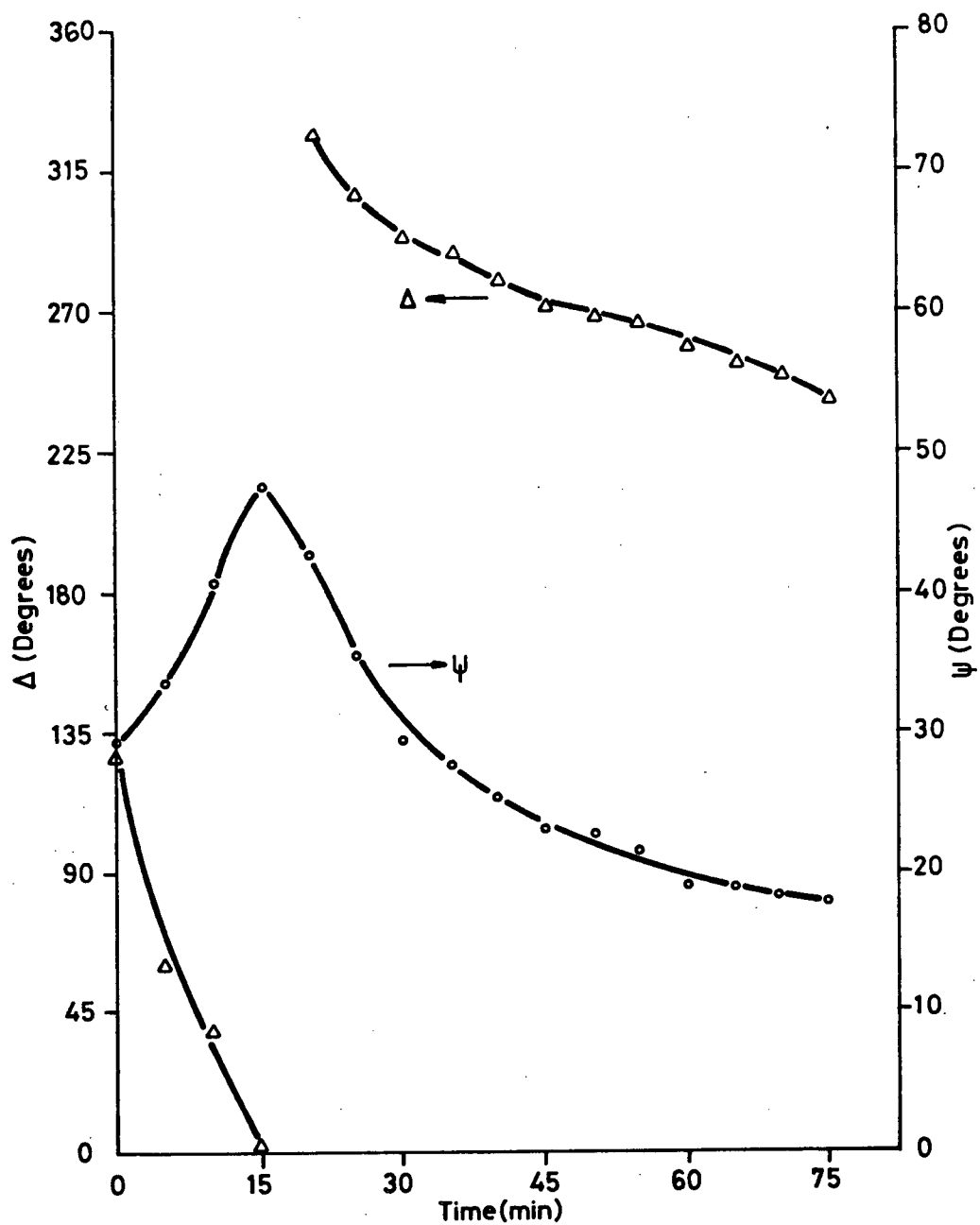
Figure 5.9 Ellipsometric Data vs. Time, Sample BNR500
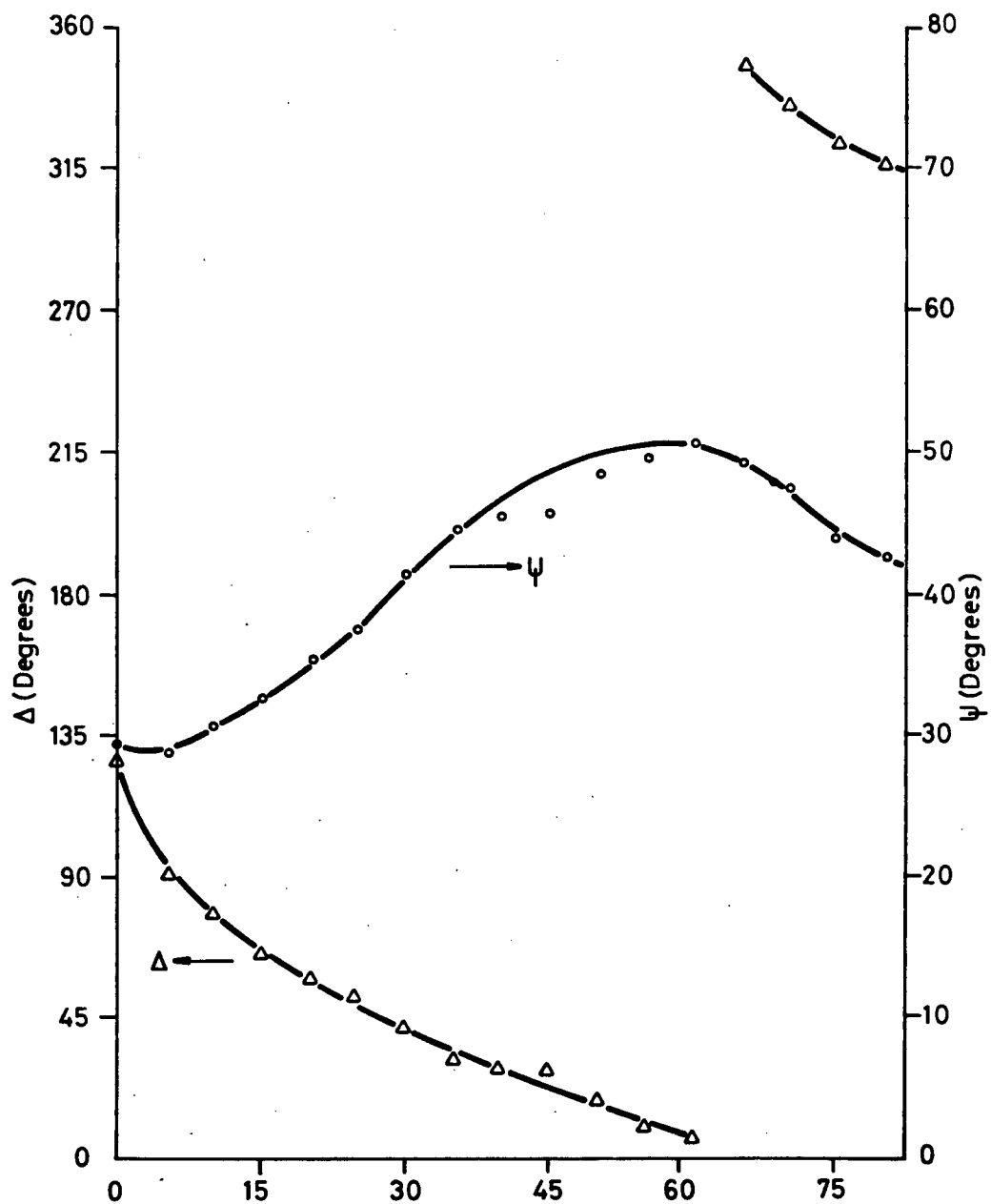
Figure 5.10 Ellipsometric Data vs. Time, Sample BNR1000

starting value is close to 130 degrees, and the curve follows a similar shape. The shift in the BNR1000 curve, as compared with the BNR500 sample, represents the additional time required to fully oxidize a thicker (twice) film of tantalum metal. We can then safely say that a 500 A Ta film will be fully oxidized in the above sense after 75 min., and that a longer time, estimated to be 120 min. is required to oxidize a 1000 A Ta film sample.

Finally, a plot of Δ vs. Ψ was made, as the film is grown in both BNR500 and BNR1000 samples. Figures 5.11 and 5.12 are computer plots of actual data. These graphs can be termed "transient", as the film grows, the ellipsometric parameters approach their final value after a certain time, i.e., the "steady state or permanent" condition. It is interesting to notice that the final values rest on a locus that corresponds to the general shape of the $\Delta-\Psi$ curves for a grown oxide, and that initially large changes of Δ take place with small changes of Ψ. This could be a property peculiar to the growth of thermal tantalum pentoxide that should be further investigated.

Thickness determination of tantalum oxide in silicon substrates was made on several samples. In these, a refractive index of 2.22 for the Ta_2O_5 [Young, 1961; Smith and Young, 1981] with a substrate index of 3.86-j0.025 was used to perform the thickness computation using the program ANALYS [Boyd, 1981], runing in the PDP8/E minicomputer. This program is based on the single layer, optically transparent
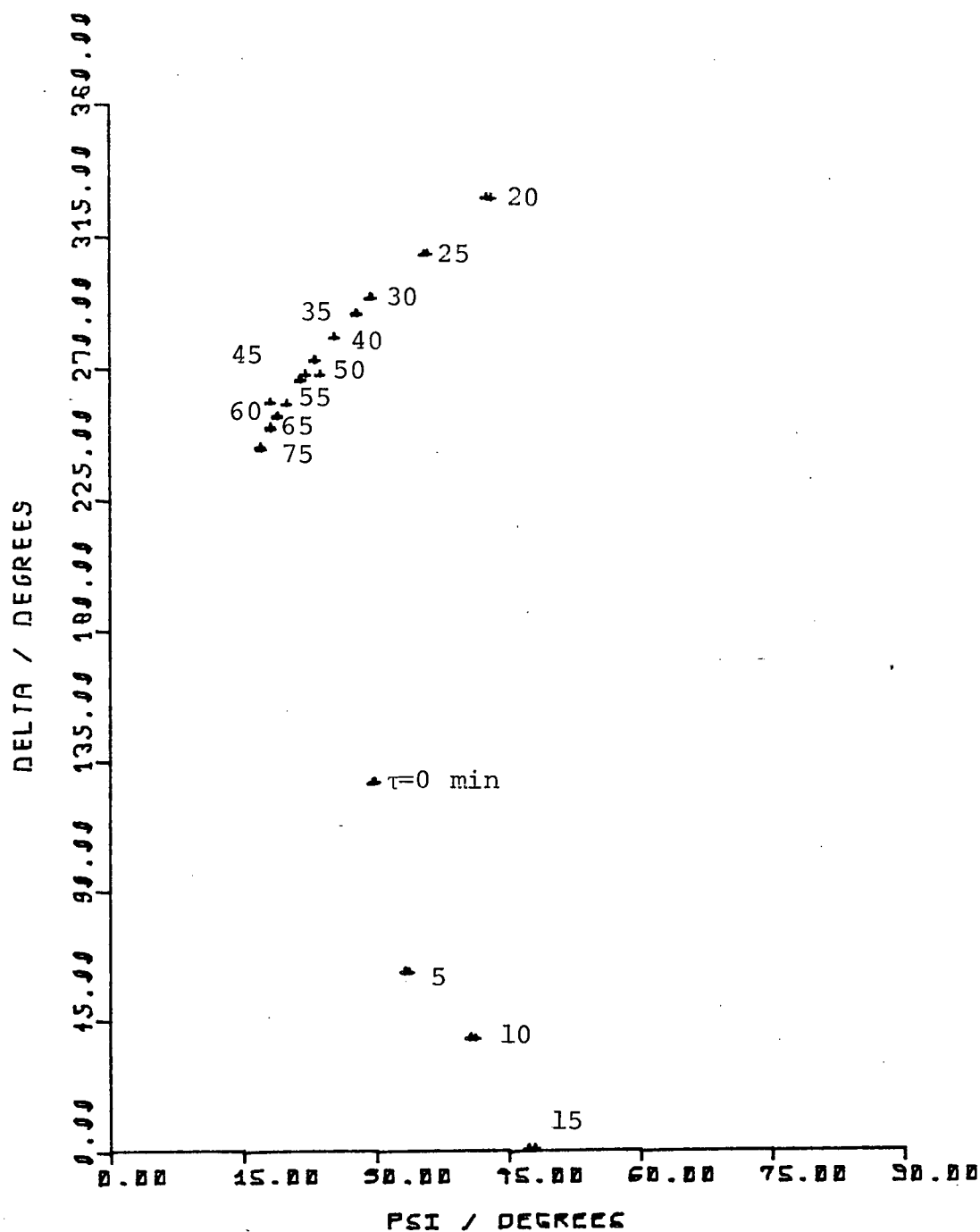
Figure 5.11 Transient Ellipsometry, Sample BNR500
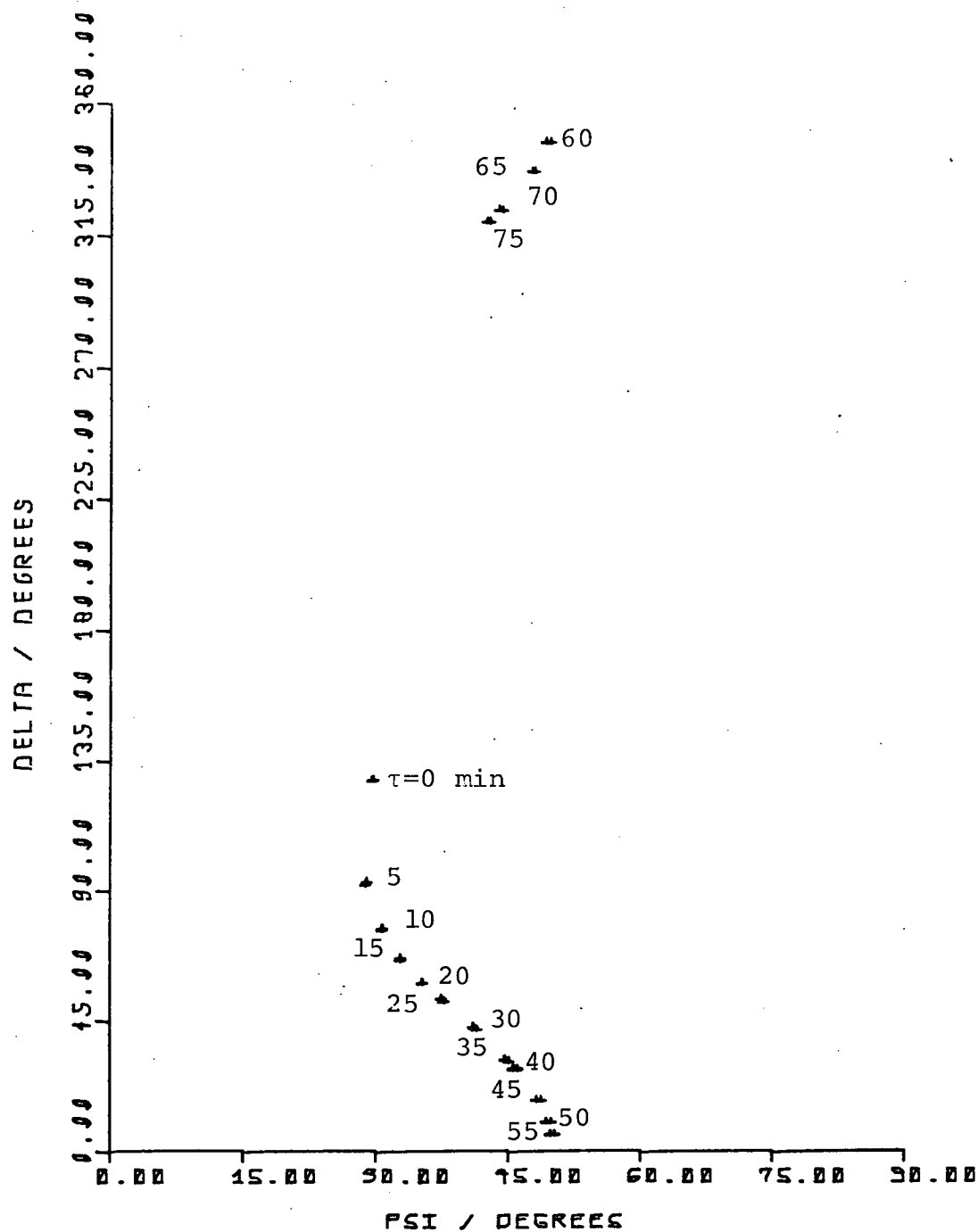
Figure 5.12 Transient Ellipsometry, Sample BNR1000

model and no allowances are made for the transition layer at the interface between the Ta{oxide} and substrate [Revesz et al., 1974 and 1976 (for the graded refractive index model); Smith and Young, 1981 (for the tapered model)]. The results are given in Table 5.2.

TABLE 5.2

OXIDE THICKNESS DETERMINATION BY ELLIPSOMETRY

SAMPLE	Ta THICKNESS	PROCESS	OXIDE THICKNESS
N2	400 A	Thermal	1173.3 A
N3	400 A	Thermal	1173.2 A
MOSC17	500 A	Anodic	890.5 A
MOSC18	1000 A	Anodic	1530.1 A
MTEST.T	500 A	Thermal	792.4 A
MTEST.A	500 A	Anodic	893.3 A

{5.5.2} C-V CURVES

These curves were obtained by the method already described, using the program CV [Boyd, 1981]. The shape of these varied, and it depended on several parameters such as the oxide thickness, whether the oxide is anodic or thermal, substrate, processing, and annealing. In the case of thermal grown oxides, the temperature of oxidation is also a factor. With the anodic oxides, the electrolyte solution also plays a role. Surface states appear in some curves, and they tend to distort its shape, particularly around the inversion region. It was noticed that in the $Al-Ta_2O_5-Si$ samples, the accumulation region was difficult to obtain, independently

of the substrate type. This was not the case in the double dielectric samples, i.e., those with $Al-Ta_2O_5-SiO_2-Si$ structure. However, in some cases, difficulty was encountered in obtaining a defined inversion; i.e., the curve is quite "noisy", indicating the presence of slow surface states (since they follow the relatively slow gate voltage ramp). The fact that accumulation is difficult to obtain in the single dielectric samples, indicates that relatively large conduction (leakage) currents are flowing. This correlates with the obtainable accumulation region in the double dielectric MOS capacitors, in which the SiO_2 layer prevents excessive electronic conduction. Furthermore, examination of the I-V curves, as shown later, corroborates this analysis. Another interesting characteristic of the single dielectric capacitors, is that a reduction of capacitance manifests itself when approaching the accumulation region from a weak inversion. This phenomena is not well understood, and it seems to be related to a decrease in apparent capacitance due to an increase in leakage currents at the onset of accumulation. Similar results were observed by other researchers [Nishioka, 1984].

In some cases, large hysteresis in the C-V curve was observed, probably due to the mobile (ionic) oxide charge in the dielectric. However, the lack of consistency in obtaining curves with hysteresis indicates that this effect is process dependent and not a defined property of the insulator. For example, two anodic grown Ta_2O_5 samples (MOSC 9 and 10) show large hysteresis, but upon fabricating more

samples with the same citric acid process, very little or no hysteresis is observed (samples MOSC 13, 15, 17 and 18). One double dielectric MOS capacitor sample (4T7, 1000 A Ta thickness over 50 A of SiO_2) exhibits a large hysteresis of 5 V, approaching the very large hysteresis curves obtained by Angle and Talley (1978) for their memory capacitors.

Another pecularity pertinent to the single Ta_2O_5 MOS capacitors which were processed thermally at 600C (an increase of 100C above the "normal" temperature of 500C), was the total absence of MOS capacitor behaviour and very large conduction currents. This is possibly due to a change in the crystal structure, from amorphous (i.e., short range order) to crystalline (large range order). Then re-crystallization takes place and the insulator behaves more like a conductor than an insulator. Previous work indicates that Ta_2O_5 recrystallizes at 650-700C for reactively sputtered films annealed in nitrogen [Kimura et al., 1983]. No field effect was observed for sample MOSC 3 and 4 processed at 600C. However, one sample (MOSC6, 500 A Ta) produced a reasonable C-V curve, except that a large decrease in capacitance was recorded at accumulation and that leakage currents were also high.

The C-V results are presented in a summary form in Tables 5.3 5.4 and 5.5, for the MOS Single Dielectric (MOS-SD) thermal the MOS Double Dielectric (MOS-DD) and MOS Single Dielectric Capacitors.

By using the value of capacitance in deep accumulation, which is the oxide capacitance Cox, it is possible to

calculate the relative dielectric constant from:

$$\varepsilon_r = \frac{C_{ox}\, t_{ox}}{A\, \varepsilon_o} \qquad (5.9)$$

The area A in most cases is 0.7854×10^{-6} m², that of a 1 mm diameter dot. The thickness tox, was obtained from ellipsometer measurements or from calculations using the swelling factor. The calculated relative dielectric constant from the C-V curves is given in Tables 5.6 (thermal) and 5.7 (anodic).

The value of the flatband voltage Vfb (i.e., that which makes the surface potential $\psi s=0$, thus producing flatbands), is obtained from the C-V plot by first calculating the flatband capacitance Cfb with the equation that involves the Debye length [Sze, 1969; p.435]:

$$C_{fb} = \frac{1}{1/C_{ox} + (\sqrt{kT/\varepsilon_s N_{A,D}}\, /q)} \qquad (5.10)$$

The value of the substrate doping Na or Nd is obtained from the four point resistivity measurements and Irvin's charts. This value of Cfb is then entered into the C-V curve and a corresponding Vfb is obtained. With the latter it is possible to calculate the fixed charge in the oxide Qfc [Sze, 1969; p.468]:

$$Q_{fc} = \frac{C_{ox}}{q}(\phi_{ms} - V_{fb}) \qquad \text{n type} \quad (5.11)$$

$$Q_{fc} = \frac{C_{ox}}{q}(V_{fb} + \phi_{ms}) \qquad \text{p type} \quad (5.12)$$

This is a straightfoward calculation if the value of ϕms, the metal-semiconductor work function difference is known. However, insufficient data or none is available on the work function properties of metals on Ta_2O_5-Si structures. It is possible to compute the value of ϕms from the expression obtained by analysis of the MIS band diagram [Glaser, Suback-Sharpe, 1977; Sze, 1969]:

$$\phi_{ms} = \phi_m - (\chi + E_g/2q - \psi_F) \qquad \text{n type} \quad (5.13a)$$

$$\phi_{ms} = \phi_m - (\chi + E_g/2q + \psi_F) \qquad \text{p type} \quad (5.13b)$$

Where ϕm and χ are the metal work function and the silicon electron affinity respectively. In the band diagram for the Al-Ta_2O_5-Si structure [Angle, 1976] the following values are used [Sze, 1969]:

$$q\phi m = 4.1 \text{ eV}$$
$$q\chi = 4.45 \text{ eV}$$

The bandgap energy Eg of the silicon semiconductor is taken here to be 1.12 eV. The last quantity ψF is a function of substrate impurity concentration:

$$\psi_F = \frac{kT}{q} \ln(\bar{n}_i/N_D) \qquad \text{n type} \quad (5.14a)$$

$$\psi_F = \frac{kT}{q} \ln(N_A/n_i) \qquad \text{p type} \quad (5.14b)$$

Were ψF is the difference between the Fermi level of the semiconductor substrate and its intrinsic value. Using an average doping concentration of 4.5×10^{14} cm^{-3} and an intrinsic concentration of 1.8×10^{10} cm^{-3}, the calculated value of ψF is -0.263 V for n type and $+0.263$ V for p type substrates. With these quantities, the values of ϕms for n and p material can be calculated:

$$\phi ms = -0.647 \text{ V n-Si substrate}$$
$$\phi ms = -1.173 \text{ V p-Si substrate}$$

Finally, the flatband voltage, capacitance and fixed oxide charge is given in Tables 5.8 (thermal) and 5.9 (anodic).

TABLE 5.3

RESUME OF THERMAL OXIDE MOS-SD CAPACITORS C-V CURVES

SAMPLE/THICKNESS	TEMP/TIME	ACCUMULATION CAP.		COMMENTS
N2/400A	500C/80min	57500	pF/cm^2	Acc.Diff.
N3/400A	500C/320min	8500	pF/cm^2	Acc.Diff.
BNR500/500A	500C/93min	76250	pF/cm^2	Low Hyst.
BNR1000/1000A	500C/187min	94063	pF/cm^2	Acc.Diff.
SampleA/500A	500C/210min	160000	pF/cm^2	Acc.Diff.
SampleB/1000A	500C/210min	84000	pF/cm^2	Acc.Diff.
1000AMOS/1000A	500C/360min	120000	pF/cm^2	Peak Acc.
500ALift/500A	500C/390min	175000	pF/cm^2	Acc.Diff.
MOSC1/500A	400C/300min	n/a	n/a	No MOS Cap.
MOSC2/1000A	400C/420min	n/a	n/a	No MOS Cap.
MOSC3/500A	600C/300min	n/a	n/a	No MOS Cap.
MOSC4/1000A	600C/420min	n/a	n/a	No MOS Cap.
MOSC6/500A	600C/300min	130000	pF/cm^2	Peak Acc.
MOSC7/1000A	400C/1wk	150000	pF/cm^2	Peak Acc.
MOSC8/1000A	600C/420min	98750	pF/cm^2	Peak Acc.

Notes:

1. Acc. Diff.: Accumulation Difficult.

2. Hyst.: Hysterisis.

TABLE 5.4

RESUME OF THERMAL OXIDE MOS-DD CAPACITORS C-V CURVES

SAMPLE/THICKNESS	TEMP/TIME	ACCUMULATION CAP.	COMMENTS
1T6/20S20T A	500C/3min	33875 pF/cm^2	Inv. SS
2T6/20S50T A	500C/7.5min	27032 pF/cm^2	Smooth
3T6/20S100T A	500C/15min	28438 pF/cm^2	Low Hyst.
4T6/20S200T A	500C/30min	28750 pF/cm^2	Inv. SS
1T7/50S100T A	500C/15min	13375 pF/cm^2	Inv. SS
2T7/50S200T A	500C/30min	24000 pF/cm^2	Peak Acc.
3T7/50S500T A	500C/75min	20000 pF/cm^2	Low Hyst.
4T7/50S1000T A	500C/150min	20500 pF/cm^2	Large Hyst.

Notes:

1. Inv. SS: Inversion with Surface States.

TABLE 5.5

RESUME OF ANODIC OXIDE MOS-SD CAPACITORS C-V CURVES

SAMPLE/THICKNESS	PROCESS	ACCUMULATION CAP.	COMMENTS
MOSC9/500 A	Citric Acid	25000 pF/cm^2	Large Hyst.
MOSC10/500 A	Citric Acid	15000 pF/cm^2	Large Hyst.
MOSC11/1000 A	Phosp.Acid	76875 pF/cm^2	Peak Acc.
MOSC12/500 A	Phosp.Acid	87500 pF/cm^2	Peak Acc.
MOSC13/500 A	Citric Acid	43125 pF/cm^2	Acc.Diff.
MOSC14/500 A	Phosp.Acid	70000 pF/cm^2	Acc.Diff.
MOSC15/1000 A	Citric Acid	51875 pF/cm^2	Smooth
MOSC16/500 A	Phosp.Acid	88750 pF/cm^2	Peak Acc.
MOSC17/500 A	Citric Acid	77000 pF/cm^2	Low Hyst.
MOSC18/1000 A	Citric Acid	82750 pF/cm^2	Peak Acc.

TABLE 5.6

CALCULATED RELATIVE DIELECTRIC CONSTANT OF THERMAL Ta_2O_5

SAMPLE	Ta THICKNESS	TEMP/TIME	ϵr
N2	400 A	500C/80min	5.57
N3	400 A	500C/320min	0.82
BNR500	500 A	500C/93min	9.24
BNR1000	1000 A	500C/187min	22.78
SampleA	500 A	500C/210min	19.38
SampleB	1000 A	500C/210min	20.34
1000AMOS	1000 A	500C/360min	29.06
500ALift	500 A	500C/390min	21.20
MOSC6	500 A	600C/300min	15.75
MOSC7	1000 A	400C/1 week	36.32
MOSC8	1000 A	600C/420min	23.91

TABLE 5.7

CALCULATED RELATIVE DIELECTRIC CONSTANT OF ANODIC Ta_2O_5

SAMPLE	Ta THICKNESS	PROCESS	ϵr
MOSC9	500 A	Citric Acid	3.03
MOSC10	500 A	Citric Acid	1.82
MOSC11	1000 A	Phosp.Acid	18.62
MOSC12	500 A	Phosp.Acid	10.60
MOSC13	500 A	Citric Acid	5.22
MOSC14	500 A	Phosp.Acid	8.48
MOSC15	1000 A	Citric Acid	12.56
MOSC16	500 A	Phosp.Acid	10.75
MOSC17	500 A	Citric Acid	9.33
MOSC18	1000 A	Citric Acid	20.04

TABLE 5.8

FLATBAND VOLTAGE, CAPACITANCE AND FIXED CHARGE OF

SINGLE DIELECTRIC Ta_2O_5 MOS CAPACITORS

SAMPLE	TYPE	Cfb [pf/cm^2]	Vfb [V]	Qfc [e/cm^2]
N2	n	28595	+1.85	-8.96×10^{11}
N3	n	7395	-1.67	$+5.43 \times 10^{10}$
BNR500	p	32295	+0.56	-2.92×10^{11}
BNR500	p	35111	+1.35	$+8.22 \times 10^{10}$
SampleA	p	41494	-6.57	-7.73×10^{12}
SampleB	p	33608	-6.49	-4.02×10^{12}
1000AMOS	n	38192	-10.24	$+7.18 \times 10^{12}$
500ALift	p	42437	-8.03	-1.01×10^{13}
MOSC6	n	39151	-2.00	$+1.10 \times 10^{12}$
MOSC7	n	40789	-1.29	$+6.02 \times 10^{11}$
MOSC8	n	35744	-5.00	$+2.68 \times 10^{12}$

TABLE 5.9

FLATBAND VOLTAGE, CAPACITANCE AND FIXED CHARGE OF

DOUBLE DIELECTRIC MOS CAPACITORS

SAMPLE	TYPE	Cfb [pf/cm^2]	Vfb [V]	Qfc [e/cm^2]
1T6	n	21231	−2.95	+4.87×10^{11}
2T6	n	18324	−4.37	+6.28×10^{11}
3T6	n	18863	−9.17	+1.51×10^{12}
4T6	n	18931	−7.67	+1.25×10^{12}
1T7	n	13375	−3.33	+2.24×10^{11}
2T7	n	16741	−8.26	+1.13×10^{12}
3T7	n	16053	−0.24	−5.71×10^{10}
4T7	n	14941	−5.63	+6.34×10^{11}

TABLE 5.10

FLATBAND VOLTAGE, CAPACITANCE AND FIXED CHARGE OF

ANODIC Ta_2O_5 MOS CAPACITORS

SAMPLE	TYPE	Cfb [pf/cm^2]	Vfb [V]	Qfc [e/cm^2]
MOSC9	n	17286	−5.35	$+7.34 \times 10^{11}$
MOSC9	n	17286	+2.28	-4.56×10^{11}
MOSC10	n	11832	−1.13	-4.52×10^{10}
MOSC10	n	11832	+2.16	-2.63×10^{11}
MOSC11	n	32406	−2.24	$+7.64 \times 10^{11}$
MOSC12	n	34155	−2.05	$+7.66 \times 10^{11}$
MOSC13	n	24367	+0.51	-3.11×10^{11}
MOSC14	n	31118	−0.39	-1.12×10^{11}
MOSC15	n	26935	+1.61	-7.30×10^{11}
MOSC16	n	34343	−3.66	$+2.17 \times 10^{12}$
MOSC17	n	32428	−2.21	$+7.51 \times 10^{11}$
MOSC18	n	33406	−4.02	$+1.74 \times 10^{12}$

It can be concluded then, that from the above measurements and calculations that operational MOS capacitors can be fabricated using thermal and anodic processes for obtaining tantalum pentoxide. Furthermore, double dielectric MOS capacitors also show good operational characteristics.

In particular, from the results presented in Tables 5.6 to 5.10, it can be said that:

1. The calculated value of the relative dielectric constant varies according to the thickness of the final Ta_2O_5 film and in the case of the thermal oxide, varies with the oxidation time. With thin oxide films and short oxidation times, the value of ϵr is less. This effect is also noticed by previous authors [Nishioka et al., 1984], and it was attributed to the formation of a very thin layer of SiO_2 at the interface. Revesz et al. (1974) reported that silicon incorporates to the tantalum oxide at the interface, with co-oxidation iteraction during the growth of thermal Ta_2O_5, and as a consequence, the refractive index of the Ta_2O_5 film decreased with the oxide thickness. The thermal oxide samples give a higher dielectric constant than the anodic oxide samples, possibly due to an increase in porosity or inhomogeneity in the film. These are less than the value reported by Young (1961) of 27, for a Metal-Insulator-Metal (MIM) capacitor; by Smith and Young (1981) of 26 for a p-MOS capacitor with thermal Ta oxide; but higher than the ones obtained by Revesz and Allison (1976) of 11.4 for thermal tantalum oxide

on silicon substrates.

2. The flatband voltages are mostly negative, and they vary in magnitude with the type of process and substrate. The thermal oxide sample exhibited the highest flatband voltages, and the anodic oxide samples the lowest. The double dielectric MOS capacitors have flatband voltages between these.

3. The fixed charge in the oxide, Qfc, varies in magnitude and sign, depending on the substrate and the nature of the oxide. The thermal Ta_2O_5 on n type samples have mostly a positive charge and the p type samples exhibit mostly a negative charge, with its magnitude in the range of $2.9x10^{11}$ to $1x10^{13}$ charges/cm^2. In the double dielectric samples, Qfc is mostly positive, with a range of $2.2x10^{11}$ to $1.5x10^{12}$ charges/cm^2. The anodic Ta_2O_5 exhibits mostly a positive charge if the oxide was formed in phosphoric acid, and mostly a negative charge if formed in citric acid, with the same substrate type. Its magnitude is somewhat smaller as compared with the thermal oxides, with a range of $4.5x10^{11}$ to $2.2x10^{12}$ charges/cm^2. Thermal tantalum oxide as reported by previous authors [Revesz and Allison, 1976; Smith and Young, 1981], has a negative charge in the oxide when made on p type substrates. Its magnitude was in the range $6x10^{11}-5x10^{12}$.

{5.5.3} I-V CURVES:

These curves were obtained by the method already

described. From the Schottky graphs, it is possible to obtain the value of the optical relative dielectric constant, which is equal to the square of the index of refraction. By using the Schottky emission model, and by obtaining the slope $\partial \ln J / \partial \sqrt{E}$ in the experimental curves, the $\epsilon r(\infty)$ can be calculated. This assumes that the Schottky plot is a straight line. In most cases however, a best fit to a straight line can be obtained. In other cases, there are several slopes denoting a complex conduction phenomena, which departs considerably from either the Poole-Frenkel or Schottky models. The following expression was used to calculate the Schottky slope:

$$\varepsilon_r = \left\{ \frac{E_1^{\frac{1}{2}} - E_2^{\frac{1}{2}}}{\ln J_1 - \ln J_2} \right\} (\ln E_1^{\frac{1}{2}} - \ln E_2^{\frac{1}{2}}) \frac{q^2}{(kT)^2} \frac{q}{\pi \varepsilon_0} \qquad (5.15)$$

Appropriate conversions were done, as our Schottky plots are given in $\log_{10} I$ vs. $\sqrt{V}$ form. A summary of results is given in Table 5.11.

As already mentioned, most of the Schottky plots are not straight lines, indicating that the emission mechanism cannot be represented by a Poole-Frenkel or Schottky model. Each portion of constant slope can be interpreted as a value of constant optical relative permittivity. The number of slope changes in the Schottky plots provide an indication of how the emission departs from these classical models. These are also given in Table 5.11. From previous authors [Kaplan et al., 1976; Smith and Young, 1981], the typical Schottky plot of Ta_2O_5 on Silicon substrates is a two slope curve,

with a somewhat sharp knee. In it, the high field region has a slope that is close to the optical value of the relative dielectric constant. However, in this work we have found that some samples exhibit two and three slopes. Mead (1962) provides information of his MIM samples and they have three different slopes. In his work, he notes that there is an ohmic region at low fields and a $\exp(\sqrt{V})$ region at higher fields, when the conduction characteristic is plotted in Schottky form.

TABLE 5.11

RESUME OF SCHOTTKY I-V CURVES AND CALCULATED

OPTICAL VALUE OF THE RELATIVE DIELECTRIC CONSTANT

FOR THERMAL Ta_2O_5

SAMPLE/TYPE	PROCESS	$\epsilon r(\infty)$	COMMENTS
N2/n	Thermal/500C	3.032	Curve w/null
N3/n	Thermal/500C	1.925	Two Slopes
N1/n	Thermal/500C	5.455	Two Slopes
BNR500/p	Thermal/500C	8.523	Curve w/null
BNR1000/p	Thermal/500C	21.056	Two Slopes
SampleA/p	Thermal/500C	2.424	Two Slopes
SampleB/p	Thermal/500C	3.867	Two Slopes
1000AMOS/n	Thermal/500C	1.895/1.213	Three Slopes
500ALift/p	Thermal/500C	1.364/1.435	Three Slopes
1000ALift/p	Thermal/500C	1.213	Curve
MOSC6/n	Thermal/600C	50.928	Two Slopes
MOSC7/n	Thermal/400C	174.643	Two Slopes
MOSC8/n	Thermal/600C	3.564	Two Slopes

TABLE 5.12

RESUME OF SCHOTTKY I-V CURVES AND CALCULATED

OPTICAL VALUE OF THE RELATIVE DIELECTRIC CONSTANT FOR ANODIC

Ta_2O_5

SAMPLE/TYPE	PROCESS	$\epsilon r(\infty)$	COMMENTS
MOSC9/n	Citric Acid	3.491	Two Slopes
MOSC10/n	Citric Acid	18.334	Str. Line fit
MOSC13/n	Citric Acid	25.047	Curve
MOSC14/n	Phosp. Acid	17.240	Three Slope
MOSC15/n	Citric Acid	4.378	Three Slope
MOSC16/n	Phosp. Acid	12.732	Curve
MOSC17/n	Citric Acid	6.734	Curve
MOSC18/n	Citric Acid	17.055	Curve

In some samples, the calculated values of $\epsilon r(\infty)$ from the Schottky plots are quite unreasonable. This reinforces the fact that neither a Poole-Frenkel or Schottky emission mechanisms can account for the conduction currents. Mead (1962) proposed three regions with their respective conduction mechanisms: at low applied voltages and high (i.e., room) temperatures, an ohmic characteristic prevails; at high fields and low temperatures, field ionization of trapped electrons in the conduction band is responsible for the current flow, yielding a Fowler-Nordheim type emission; finally at high fields and high temperatures, the current flow is field enhanced by thermal excitation of trapped electrons into the conduction band, producing a Poole-Frenkel type emission. Kaplan, Balog and Frohman-Bentchkowsky (1976) consider a bulk limited P-F emission at low fields, and a transition towards a space charge limited current at higher fields. They provide an empirical relation of the form $J \alpha V^{2.4}$. Angle and Talley (1978) argue that the conduction mechanisms are quite different in the anodic and thermal oxides. From their experimental data, they concluded that under forward bias, P-F type conduction takes place for thermal oxides under forward bias and under reverse bias, a space charge limited conduction mechanism dominates, which is attributed to the surface states at the Al-Ta{oxide} interface formed during processing.

A clear evidence of photoconduction was found in the MOS capacitors. It was noticed that when the samples were illuminated, large variations in conduction current took

place, as detected by the electrometer used in measuring the leakage current. Some samples exhibited more sensitivity to the incident light than others. The light source was a Westinghouse Heat Ray (infrared) lamp, 250 W, 115 V, placed exactly 25 cm above the centre of the sample. Some samples exhibited more sensitivity to the applied light that others, and from the calculated ratios of photocurrent increase, as given in Table 5.11, it suggests that this phenomena is not process dependent, but related to the traps in the oxide's conduction band, to which photo generated electrons use as stepping stones in the insulator bandgap.

TABLE 5.13

PHOTOCONDUCTION IN TANTALUM OXIDE MOS CAPACITORS

SAMPLE	PROCESS	PHOTOCURRENT RATIO AT 5V
N2	Thermal/500C	3.5
1T6	Thermal/500C	3.7
2T6	Thermal/500C	15.8
3T6	Thermal/500C	2.3
4T6	Thermal/500C	1.0
1T7	Thermal/500C	133.3
2T7	Thermal/500C	2.0
3T7	Thermal/500C	3.2
4T7	Thermal/500C	1.3
N1	Thermal/500C	8.0
BNR500	Thermal/500C	6.3
SampleA	Thermal/500C	1.0
SampleB	Thermal/500C	5.6
1000AMOS	Thermal/500C	3.5
500ALift	Thermal/500C	1.2
1000ALift	Thermal/500C	2.0
MOSC6	Thermal/600C	1.5
MOSC7	Thermal/400C	32.0
MOSC8	Thermal/600C	3.2
MOSC14	Anodic/Phosp.	5.5
MOSC15	Anodic/Citric	20.5
MOSC16	Anodic/Phosp.	1.3
MOSC17	Anodic/Citric	11.0
MOSC18	Anodic/Citric	1.8

{5.6} INTERFACIAL OXIDATION MOS CAPACITORS:

Both C-V and I-V curves were obtained for these samples. It was noted that in general the C-V curves are of excellent quality, with well defined accumulation and inversion regions. In the first, the sample had a smooth transition towards accumulation, with none of the difficulties that appeared in the single dielectric Ta_2O_5 MOS capacitors. The acumulation region is also without visible bumps, that indicate the presence of surface states. This indicates that the quality of the double dielectric structure is very good and that the method of growing the SiO_2 layer under the Ta_2O_5 is quite successful.

The results from the I-V curves also indicate that this process is quite successful, as the electronic conduction (leakage) current is quite small, of comparable or smaller magnitude than the previous double dielectric process. Tables 5.12 and 5.13 summarize the results obtained from both C-V and I-V data.

TABLE 5.14

INTERFACIAL OXIDATION MOS CAPACITORS, C-V RESULTS

SAMPLE	WET OX.TIME	INSULATOR	ACCUMULATION CAP.
MTJ1	3-54-3 min	Ta_2O_5/SiO_2	51875 pF/cm^2
MTJ1	3-54-3 min	SiO_2	46500 pF/cm^2
MTJ2	3-114-3 min	Ta_2O_5/SiO_2	76750 pF/cm^2
MTJ2	3-114-3 min	SiO_2	56563 pF/cm^2
MTJ3	3-54-3 min	Ta_2O_5/SiO_2	88750 pF/cm^2
MTJ3	3-54-3 min	SiO_2	75000 pF/cm^2
MTJ4	3-24-3 min	Ta_2O_5/SiO_2	106250 pF/cm^2
MTJ4	3-24-3 min	SiO_2	117500 pF/cm^2
MTJ5	N/A	Ta_2O_5	175000 pF/cm^2

TABLE 5.15

INTERFACIAL OXIDATION MOS CAPACITORS, I-V RESULTS

SAMPLE	INSULATOR	LEAKAGE CURRENT	SCHOTTKY SLOPES
MTJ1	Double	0.52 nA at 10 V	Two
MTJ2	Double	0.30 nA at 10 V	Two
MTJ3	Double	0.52 nA at 10 V	Two
MTJ4	Double	13 nA at 10 V	Two
MTJ5	Ta_2O_5	14.5 μA at 10 V	Three

CHAPTER 6

FABRICATION AND PROCESSING OF MTAOS FIELD EFFECT TRANSISTORS

The MTAOS active devices were fabricated using the already developed techniques for the MOS capacitors, in particular the liftoff process and anodic oxidation of tantalum on silicon substrates. The processing is based on a modified version of the standard p-MOS technology used in the Solid State Laboratory, Electrical Engineering Department, at this University. The objective was to fabricate a Ta_2O_5/SiO_2 double insulator p-Channel Enhancement type MOSFET, and to demonstrate its feasibility as a new active device of the MOS family.

Two main avenues were followed: the thermal and anodic oxidation methods for preparing tantalum pentoxide. This resulted in two groups of n-type Si substrates, each dedicated to the individual preparation method. In order to independently verify the quality of the final double dielectric structure, several substrates were also simultaneously processed for dot and ring MOS capacitors. Further C-V and I-V measurements of these will accurately reveal the insulator performance.

The following general processing steps were followed:

1) Thickness and four point resistivity measurements.

2) Scribing and marking.

3) Peroxide-acid cleaning using the RCA process.

4) Thermal oxidation of substrates, using the "wet"

hydrogen- oxygen method. Field oxide thickness target: 600 nm.

5) Photolithography of source and drain windows on field oxide.

6) Source and drain boron diffusions: predeposition and drive-in.

7) Gate photolithography, window in field oxide.

8) Thermal oxidation, using the "dry" oxygen method, for the thin SiO_2 gate insulator.

9) Peroxide-acid cleaning, excluding the HF step.

10) Aluminium thermal evaporation in preparation for liftoff.

11) Photolithography of aluminium for liftoff.

12) RF Sputtering of tantalum metal.

13) Thermal oxidation of first group in dry oxygen.

14) Anodic oxidation of second group in citric acid.

15) Liftoff patterning of tantalum pentoxide.

16) Inspection of all wafers under microscope.

17) Peroxide-Acid cleaning, excluding the HF step.

18) Drain and source photolithography to remove thin gate oxide.

19) Inspection and photography of all wafers under microscope.

20) Peroxide-Acid cleaning, exluding the HF step.

21) Aluminium evaporation by electron beam technique for source, drain and gate contacts.

22) Photolithography of aluminium source, drain and gate contacts.

23) Thick oxide etching on wafer's back, preparation for substrate (back) contact.

24) Gold evaporation by Electron Beam technique for back contact.

25) Final microscope inspection of all wafers. Photography.

The first three steps were already described in detail under Chapter 4, and they are not repeated here. All wafers were scribed with a code and date, so that they could be easily and uniquely identified. Six MTAOS device wafers were processed, together with three general and one SiO_2 control wafers, a total of ten substrates.

{6.1} SHEET RESISTIVITY DETERMINATION:

The four point resistivity measurements are standard procedure to verify the sheet resistivity and obtain the impurity concentration via Irvin curves for silicon. All wafers were cleaned using the RCA procedure with all its steps. The substrates used were n-type silicon, of the following characteristics:

Manufacturer: Monsanto

Lot No. 4002, Serial No. Di-45640, Date 3/5/76

Dopant: Phosphorous, N type.

Resistivity: 8-10 ohm-cm.

Thickness: 11-12 mils; Diameter: 1.98-2.02 inches.

Two groups of wafers are used in this stage: the ones that will have the tantalum pentoxide thermally grown and those in which the oxide will be grown anodically. These are given in Table 6.1, with the sheet resistivity results.

TABLE 6.1

DEVICE SUBSTRATE MARKING AND MEASURED RESISTIVITY

MARKING	TYPE	RESISTIVITY [ohm-cm]
MTAOS1	Thermal	9.337
MTAOS2	Thermal	10.171
MTAOS3	Thermal	9.528
MTAOS4	Anodic	9.438
MTAOS5	Anodic	9.856
MTAOS6	Anodic	9.221
MOS I	Control	9.976
MOS II	Control	9.259
MOS III	Control	9.044
SiO2 I	SiO_2	9.472
SIO2 II	SiO_2	10.637

{6.2} SILICON THERMAL OXIDATION:

The cleaned wafers were then introduced to a previously conditioned oxidation furnace (Fairchild with Wheelco/Barber Coleman temperature controllers) for thick oxide (target value: 600 nm). The temperature was set to $1100°C\pm5$ with the aid of a previous thermocouple temperature profile and internal regulating system. The gas flows were set as

described in Appendix III. After 2 hrs. 45 min., the samples were removed, cooled for a few minutes and their thickness checked against the Color Chart for silicon oxides and by ellipsometric measurements, using the equipment described before in Chapter 4. The results are the following:

Sample	Ψ	Δ	Thickness [nm]
SiO2I	15.72	122.72	591.1
SiO2II	19.27	108.06	602.8

The color, of the grown film as observed by naked eye was pink. Which, from the Color Chart corresponds to 600 nm.

{6.3} THICK OXIDE PHOTOLITHOGRAPHY:

The mask set used throughout this process was already available, and it contains a sample of several active and passive devices, hence the name "Smorgasbord" attached to it. The devices are:

a) A resistor, p-n diode and MOS capacitor.

b) A MOS Transistor.

c) A Logic Inverter, 2 Input NOR gate and RS Flip-Flop.

Photolithography was used to etch the source and drain windows through the field oxide. Negative photoresist application, exposure, development, etching, and stripping details are given in Appendix III. The wafers were then inspected under a microscope for resolution and under/over etching. They gave excellent results with good line resolution and proper etching.

{6.4} BORON PREDEPOSITION:

The diffusion process has two steps: the predeposition and drive-in of the impurities. Since the substrates are n-type, we are interested in creating two p+ regions for the drain and source. Boron is used as acceptor impurity, in the form of BBr_3, which is passed through the predeposition furnace (Faichild, with Wheelco/Barber Coleman temperature controllers) together with other gases (for details see Appendix III). The furnace is preconditioned ("predoped") for one hour before the slices are introduced, and the temperature carefully set to 1090±5°C. A half-slice, test wafer was used to check the predeposition step, before the device wafers were introduced. After cycling and cooling its resistivity was measured, using the four point probe method. At this point, a certain degree of difficulty was encountered, as the target value of 2.0 ohm-cm could not be achieved. Initilly, the four point probe test gave values that were too high (8-11 Ω-cm), a second iteration gave a value of 6.8 Ω-cm, and finally a third one gave a sheet resistivity of 2.6-2.8 Ω-cm. The measured resistivity was 1.95-1.99 ohm-cm, very close to the target value. Total time was 23 min.

{6.5} BORON DRIVE-IN:

Before the drive-in of impurities, the "boron glass", formed during the previous predeposition step, was removed. It was noted that by placing the wafers in de-ionized water ("wetting") before etching in HF, the results improved

considerably. It appears that the adhered surface water slows the initial reaction, so that there is a slow initial etching rate.

The drive-in furnace (Thermco Pacesetter II) was first set to the proper temperature ($1090 \pm 1°C$), allowed to settle and then profiled with a Pt-Rd thermocouple. The latter was in agreement with the setting. After conditioning, the slices were allowed into the furnace and cycled as detailed in Appendix III. Total time was 2 hrs. The samples showed typical green tracks when examined with naked eye. At this point no smears or evidence of contamination could be seen.

{6.6} GATE PHOTOLITHOGRAPHY:

The gate window now can be cut using photolithography. This required a mask alignment step, performed in a Kasper Instruments Model 17A Mask Aligner, with an ultraviolet light source and adjustable exposure time. Negative photoresist was used, and developed automatically in a Kulicke and Soffa Model 693 Photoresist Spray Developer, etched and stripped as detailed in Appendix III.

{6.7} THIN OXIDE PROCESS SIMULATION USING SUPREM:

After this step, the gate oxidation can be performed. No data was available for accurately growing a thin 200 A thick SiO_2 layer over the silicon substrate, using the furnace equipment available in the Solid State Lab. A process simulation program, SUPREM, runing under MTS, was used to simulate the growth of the silicon dioxide at high

temperatures in an oxidizing atmosphere. Several combinations of temperatures and oxidation time in a dry oxygen atmosphere were used. The results are as follows (details in Appendix IV):

TABLE 6.2

SUPREM SIMULATION RESULTS

Time [min]	Temperature [°C]	Oxide Thickness [A]
3	1000	140
5	1000	200
3	1090	224
3	1090	224
10	1090	349
38.5	1090	754
60	1090	998
80	1090	1198
85	1090	1244
90	1090	1290

For the thin gate oxide, the process selected is then 5 min. in dry oxygen, furnace temperature at 1000 C. Before the device wafers were introduced in the furnace, the cycle was checked using test samples previously prepared and cleaned. The Color Chart available does not provide data below 500 A for silicon, so that only ellipsometric measurements could be carried out.

The above SUPREM results were used as a starting point in determining the right cycle conditions for a target SiO_2

thickness of 200 A. Test wafers were then cleaned and prepared for a sequence of oxidations and ellipsometric measurements, until the proper target value was obtained. When the selected SUPREM value of 5 min. at 1000 C was used, the measured thickness was 110-120 A, which is too low for this application. It is important to note that the actual oxidation cycle used consists of five steps:

    a) 5 min. O_2, Purge.
    b) Samples Introduced.
    c) 3 min. O_2, Passivation.
    d) X min. O_2+HCl, Slow Oxidation.
    e) 20 min. N_2, Annealing.

In step d), the actual time was varied for each individual test wafer (given by the letter X), and then its thickness measured. The results are given in Table 6.3.

TABLE 6.3

DRY THERMAL OXIDATION OF SiO_2

WAFER	O_2+HCl Time [min]	Thickness [nm]
TEST 200A	2	13.74
TEST 200A	5	17.47
TEST 200A	7	20.72
TEST 200A (etched)	7	17.12
TEST 200A (etched)	10	23.95
TEST 200A (etched)	8	21.04

Based on these results, the last entry on Table 6.3 is quite acceptable. The modified cycle is then:

a) 5 min. O_2, Purge.

b) Samples Introduced.

c) 3 min. O_2, Passivation.

d) 8 min. O_2+HCl, Slow Oxidation.

e) 20 min. N_2, Annealing.

The device and control wafers were then introduced to a previously conditioned and profiled furnace (Fairchild with Wheelco/Barber Coleman Controllers), at a temperature of 1000 C.

{6.8} PREPARATION OF DEVICE WAFERS FOR ANODIZATION:

At this point the device wafers were separated into the anodic and thermal groups, as the next processing steps are quite different. Since the anodic device wafers have an overall thin oxide, it is necessary to remove a small area, so to have a direct contact to the silicon substrate for anodic oxidation (this is the same process developed during the anodic MOS capacitor processing in Chapter 4). Photolithography with negative photoresist was used, and a small straight piece of a diamond cut wafer used to cover the flat edge in the device wafer. This slightly reduces the yield, but there is no alternative.

{6.9} PEROXIDE-ACID CLEANING OF ALL WAFERS:

All control and device samples were cleaned using a modified version of the RCA process, which excludes the HF etch, otherwise the thin oxide will be removed.

{6.10} ALUMINIUM EVAPORATION:

Aluminium thermal evaporation followed, as the first step in preparation for Liftoff. This was done in a CHA Evaporator, previously loaded with high purity Al wire, as described in Chapter 4. The monitored final thickness was close to 500 nm. Experimentally, this writer found that when the liftoff Al was too thick (around 1000 nm) the etching time was quite long and underetching took place, as compared with a thinner layer (around 500 nm) of deposited Al. Smaller values can be used, and less etching time will be required, however the resolution can be impaired due to over-etching.

{6.11} PHOTOLITHOGRAPHY FOR LIFTOFF:

The Liftoff pattern was delineated using photolithography with negative photoresist. At this point, a careful examination of the available masks was done. The set did not have an exact opposite (negative mirror image) pattern for our specific application. Instead of designing a new one, with the considerable delay involved, it was discovered that by combining a Gate Contact mask (negative version) with a Gate Window mask, the exact area of evaporated aluminium could be removed. This required a

critical double alignment and exposure, which considering the quality of our Mask Aligner, was not an easy step. A "guinea pig" wafer was used to verify the results and quality of our procedure. A close examination under the microscope confirmed our expectations and revealed that this technique was a good one. Only the device wafers were processed with this method.

{6.12} MICROSCOPE EXAMINATION AFTER LIFTOFF:

Inspection under the microscope revealed that all device wafers had excellent alignment, good resolution and that the double exposure technique worked very well, with good definition around the gate area. Some "ragging" was visible under higher magnification, which will not make the liftoff edge very straight. This suggests perhaps some degree of underetching of the Al metal. Some flaws were evident on the edges (tweezer handling), which are quite normal. Except for these, the device wafers exhibited very good quality.

{6.13} DETERMINATION OF THE SWELLING FACTOR S:

Before the tantalum metal could be deposited by sputtering, it was necessary to determine the thickness required for a target thickness of tantalum pentoxide. In the oxidation process, all the metal will be converted (ideally) into oxide, independently of whether the method is thermal or anodic. The final oxide will be thicker that the original metal film, and it can be said that "swelling"

takes place. Hence a swelling factor S can be defined, and calculated considering the molecular weights, densities, areas and thickness of the initial metal and final oxide films:

$$\frac{^m Ta_2O_5}{^m Ta} = \frac{^\delta Ta_2O_5}{^\delta Ta} \frac{(A_{Ta_2O_5} \, t_{Ta_2O_5})}{(A_{Ta} \, t_{Ta})} \qquad (6.1)$$

Clearly, the areas are equal, and by using m{O}=16 gr and m{Ta}=180.88 gr, the molecular weight m{Ta$_2$O$_5$}=441.76 gr is obtained. From the CRC (Chemical Rubber Company, 57th Edition, 1977) Physics and Chemistry Handbook, the density value of tantalum and from Young (1961) the tantalum pentoxide density are:

$$\delta\{Ta\} = 16.6 \text{ gr/cm}^3 \qquad\qquad \delta\{Ta_2O_5\} = 7.95 \text{ gr/cm}^3$$

Then, the swelling factor S is defined as the ratio of the tantalum pentoxide thickness to the tantalum thickness:

$$S = \frac{t_{Ta_2O_5}}{2 \, t_{Ta}} \qquad (6.2)$$

The factor 2 in the denominator arises from the fact that two atoms of tantalum are required to form Ta$_2$O$_5$, if the stoichiometry is right. By using the above molecular weight figures, the S factor is then:

$$S = \frac{^m Ta_2O_5}{^m Ta} \frac{^\delta Ta}{^\delta Ta_2O_5} = 2.55 \qquad (6.3)$$

It is important to compare this value with experimentally measured ones. Revesz et al. (1976), in his work on thermal tantalum oxides, gave a final oxide thickness of 60 nm for an initial metal film thickness of 28 nm; the S factor is then 2.14. This compares quite favourably with the theoretical value of 2.55. It quite reasonable then to expect doubling the original metal thickness value, when fully converted to oxide.

{6.14} PRELIMINARY RF SPUTTERING OF TANTALUM:

In this work, and from previous MOS Capacitor experience, two standard values of tantalum metal thickness are used: 500 and 1000 A, which when fully oxidized will yield a gate oxide thickness of 1000 and 2000 A for the tantalum pentoxide. In this case only 500 A of Ta film will be used.

Previously clean test wafers were introduced into the RF Sputtering equipment. A good recommended practice, followed through our experimental work, was to preliminary sputter at low power for 10-15 min., in order to eliminate any possiblity of contamination, due to chamber/target impurities. We also recommend that clean glass samples should be placed side by side to the wafer (preferably two). This accomplishes two functions: holds the substrate in place, under the centre of the target, thus eliminating any possiblity of movement due to vibration (particularly when the roughing pump is in action) and by air being removed from under the wafer; secondly the glass receives an equal

amount of deposited metal, hence these can be used for microscope (dark field will show the hillock or measle count, and a transmission one will reveal the pinhole density) examination.

The sputtering rate was determined before by D. Smith (using the Sloan Angstrometer and stepwise etch method). At a forward RF power of 160 W (reflected power <5 W), the rate is 294 A/min. The film thickness of the Ta metal can be determined using ellipsometry, by taking measurements at two or more different ellipsometer angles. Westwood (1975), gives several values for triode sputtered films, all complex with a fairly large imaginary component. Furthermore, these films seem to be quite reflective, and not transparent as the ellipsometric technique requires. Examination either by naked eye or microscope shows a "mirror" like surface, which reflects most of the incident light.

{6.15} PRELIMINARY THERMAL OXIDATION:

A single test wafer was thermally oxidized in a dry Oxygen atmosphere at 500 C, in previously conditioned and stabilized furnace (Minibrute, Thermco Products Corp., with Analock 201 Controllers). The gas flow was set to 1 l/min, and at the furnace ends, the temperature was set to +5C above the centre. The oxidation time was based on previous MOS capacitor work, and a time of 90 min was decided to be optimum for full conversion of metal into oxide. The wafer was then removed and allowed to cool. Its color was bright intense blue, clean with no traces of contamination.

Ellipsometric determination of the film thickness gave a value of 80 nm.

{6.16} PRELIMINARY ANODIC OXIDATION:

Anodic oxidation was performed on another test wafer, with Al deposited by evaporation in the back, to assure a good contact. The electrolyte was a 0.1 M solution of citric acid in de-ionized water. The anodization cell was the same as described in Chapter 4, the same equipment set-up was used and a current density of of 1 mA/cm² was passed through the cell. Because of the O ring that holds the wafer against its back brass contact, the Ta metal at the perimeter is not oxidized, and this acts as a conductor around the wafer, thus assuring that the current will be uniformly distributed on the exposed area. The wafer was carefully rinsed in d.i. water and dried in boiling isopropyl alcohol. Its color was medium dark blue, and some traces of deterioration were evident. Also, some bubbling was noticed during the latter part of anodization, which indicates breakdown by "sparking" [Young, 1961]. Analysis of our procedure revealed that the Constant Current power supply was set to a voltage limit of 100 V, which is too high and as the oxide was grown, some areas (weak spots and probably pinholes) were subject to electric fields beyond breakdown. This experience was invaluable for successfully processing the anodic device wafers. The film thickness, as determined ellipsometrically, gave a value of 90 nm.

{6.17} RF SPUTTERING OF TANTALUM:

After this preliminary experiment, the remaining device wafers could be processed. RF sputtering was accomplished on each wafer individually, as our experience indicated that two or more wafers could not be uniformly covered with Ta, due to a noticeable thickness gradient away from the target centre. Each wafer was introduced accompanied by two previously cleaned (RCA process) and labeled glass samples (Corning 2947). The sputtering is done in argon, with a partial pressure of 26 mT. Residual gases had a measured pressure better than 10^{-6} Torr. Under these conditions the sputtering rate is 294 A/min at 160 W forward and <5 W reflected power. All samples had an estimated deposited thickness of 500 A. Naked eye examination indicates that the surface is mirror-like and free from contamination and impurities.

{6.18} THERMAL OXIDATION OF TANTALUM:

All thermal device samples were introduced to a previously conditioned furnace (already described before) at 500 C, and with a dry oxygen flow rate of 1 l/min. The total oxidation time was 90 min, at which point the wafers were removed and left to cool before further handling. The oxidized Ta surface had a deep blue-purple color in the areas were the Al was etched. The film seems to be transparent, as the Al can be seen quite well, although the bluish film is everywhere.

{6.19} ANODIC OXIDATION OF TANTALUM:

Before the anodic oxidation could proceed, Al metal was thermally evaporated onto the back of each anodic sample. The CHA equipment was used, and a thickness of 7500 A was deposited as indicated by the Thickness Monitor. The anodization process consisted of two main steps:

a) Constant Current Mode: Anodization.

b) Constant Voltage Mode: Healing of weak spots.

The wafers were anodized in a 0.1 M Citric Acid solution at a constant current density of 1 mA/cm^2. The voltage limit on the Constant Current Power Supply was set to 50 V, as this avoids the problems encountered in Section {6.16}. As usual, a chart recorder monitored the voltage V(t) across the anodization cell. At this point, the color of the wafer changed from metallic tantalum, to pale yellow and finally to intense blue. It is quite interesting to observe this color change in a matter of 2-3 min. The graph of V(t) under constant current mode is shown in Figure 6.1, when it reaches Vlimit, the Ta metal is fully converted into oxide. The basic assumption under the constant voltage mode, is that most of the weak spots and pinholes will be "healed", in a not very well understood process [Dell'Oca et al., 1971], but has been experimentally verified to reduce the electronic conduction (leakage current) through the film. A constant voltage of 15 V was applied to the cell, for 60 min., and the current flow I(t) monitored with a chart
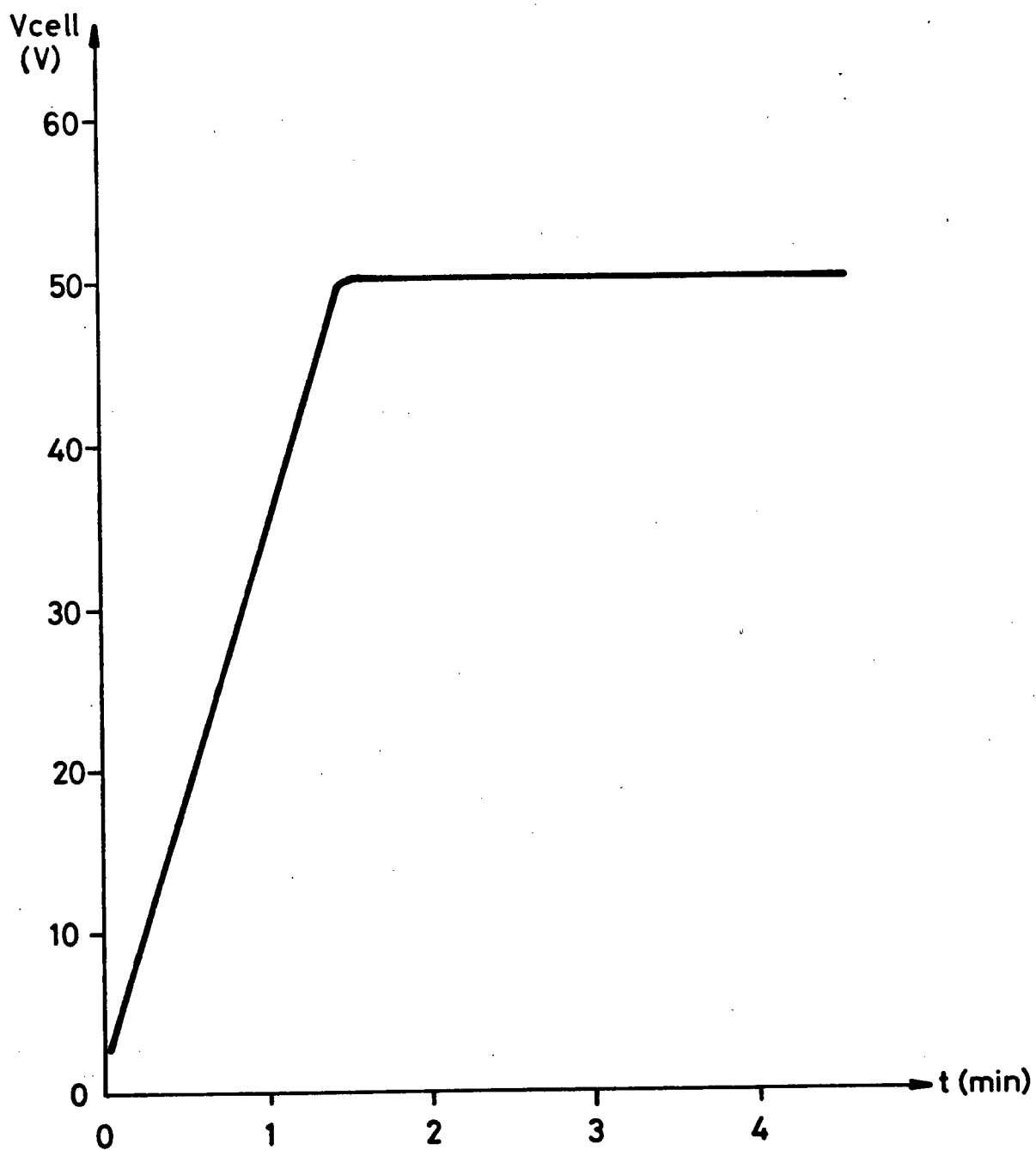
Figure 6.1 MTAOS Anodic Oxidation under Constant Current.
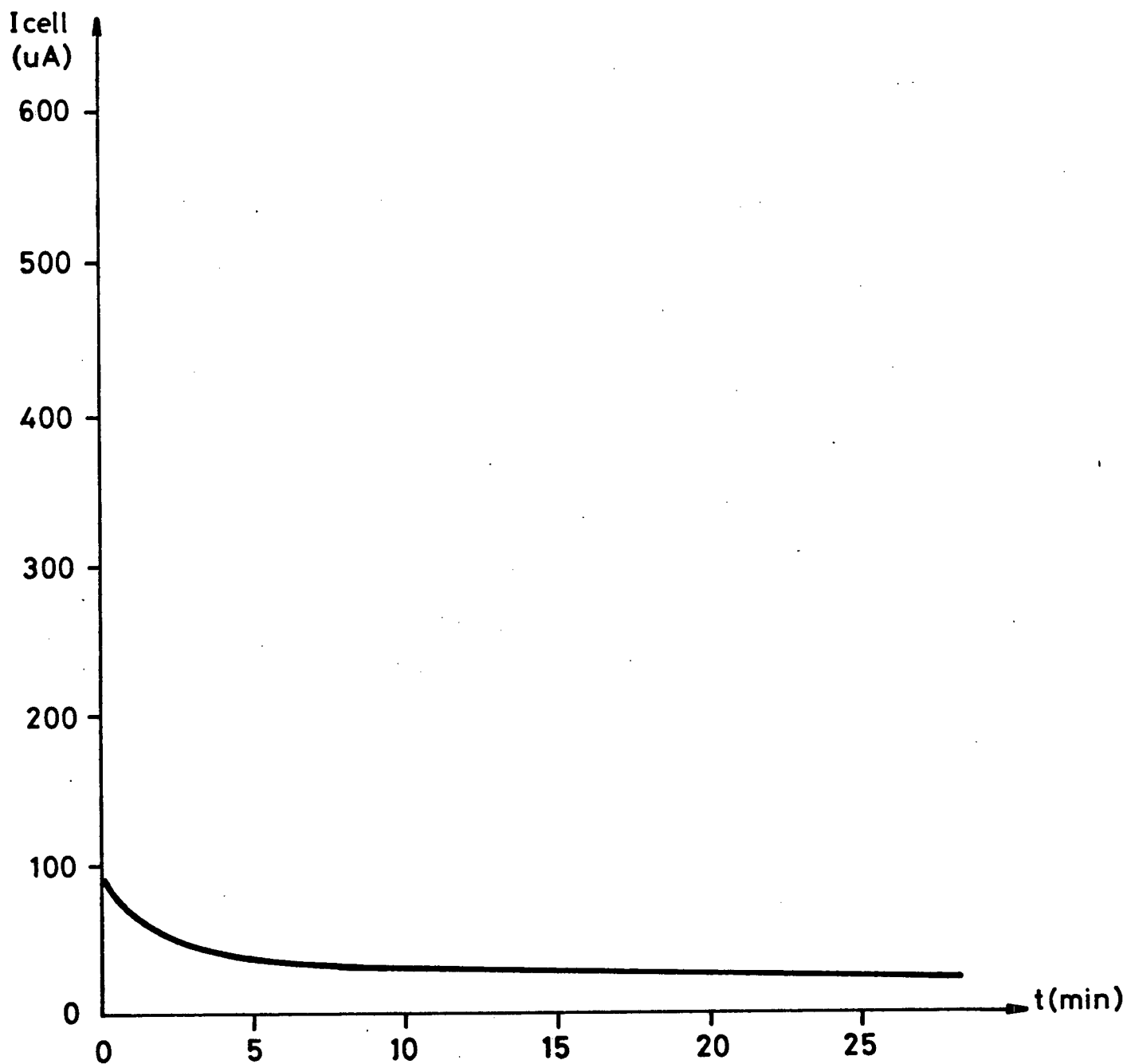
Figure 6.2 MTAOS Anodic Oxidation under Constant Voltage.

recorder, as shown in Figure 6.2. A decrease of current with time is clearly noticed.

After anodization took place, all wafers were thoroughly rinsed in de-ionized water, boiled in isopropyl alcohol and dried in a N_2 jet.

{6.20} PRELIMINARY MICROSCOPE EXAMINATION:

A preliminary examination of all wafers under the microscope revealed that well delineated features are visible, with good resolution and contamination free surfaces. The typical "star sky" or "milky way" on the Ta{oxide} areas, was obtained under dark field revealing the formation of hillocks or "measles". Some "ragging" was evident in the gate area, probably due to Al underetching or underdeveloping of the photoresist. It was noticed that a significant color difference exists between the anodic and thermal oxide wafers. The first ones show a blue/light-blue color and the latter, a deep blue-purple color.

{6.21} LIFTOFF PATTERNING:

A device wafer was introduced into a hot (70 C) etching solution of phosphoric acid and de-ionized water (1:1 ratio), in order to check the quality of the process. After 5 min., a cloud of gas bubbles formed above the wafer. The temperature was closely monitored with a thermometer placed in the beaker containing the solution and wafer. After one hour, the Al shows signs of deterioration and it has actually wrinkled. The wafer was allowed another 30 min. in

the solution, after which was removed, rinsed in d.i. water. A Sof-Swab (Clean Room Products, Bay Shore, New York) was used to remove, with great care, the wrinkled Al with Ta{oxide} on top, procedure mentioned in Chapter 4. If care is taken, the surface can be quickly cleaned, by liberal use of d.i. water rinsing and the action of the Sof-Swab. Any stubborn spots can be removed by placing the wafer back in the etching solution for another 15 min., perhaps for 3-4 times or until required. All device (anodic and thermal) wafers were processed successfully in a similar way.

{6.22} MICROSCOPE EXAMINATION AFTER LIFTOFF:

Under bright field, all device wafers show a clean surface, with no traces of liftoff Al/Ta{oxide}, features such as lines, drains, gates and sources are very well delineated, indicating good resolution. Dark field examination shows the typical "star sky" pattern of hillocks, in the areas in which the tantalum metal was oxidized. For comparison, a clean, bare sample of silicon wafer (of same characteristics as the processed ones) did not reveal the "star sky" or "milky way" pattern, when examined under dark field. It is then quite conclusive, that the deposition of tantalum metal on silicon originates such a pattern. A more extensive discussion on this subject was done in Chapter 5.

{6.23} PEROXIDE-ACID CLEANING:

A modified RCA cleaning process was used, in which the hydrofluoric acid (HF) step was not used, as this would have attacked the very thin (200 A) gate Si oxide.

{6.24} SOURCE AND DRAIN THIN GATE OXIDE REMOVAL:

Since the thin gate oxide was grown everywhere on the wafer surface, it is necessary to remove it from the source and drain, to provide a reliable contact. This was accomplished by photolithography using a negative photoresist process. Etching was performed in a buffered HF solution at a rate of 850 A/min, for a total time of 30 secs.

{6.25} MICROSCOPE PHOTOGRAPHY:

Examination under the microscope revealed that all wafers were in excellent condition. It was decided then to obtain a set of color negative pictures of the devices fabricated. A Wild Model MPS20 Negative Film camera was used in conjunction with a Model M20 Microscope. The combination proved excellent for microphotography work. Figures 6.3 to 6.5 show the different devices captured by the camera. Notice the blue-green color of the tantalum pentoxide, the pink-orange background of the thick field oxide and pale yellow of the source and drain diffusions. The colors are quite striking considering that no contact metallization (Al) has been applied yet.

{6.26} ALUMINIUM DEPOSITION FOR CONTACTS:

The final contact metallization was done by depositing high purity aluminium metal using the Electron Beam method. Previous work [Solomon, 1974; Janega, 1983] indicated that considerable amount of Na can be deposited using the thermal evaporation method, in which Al metal is melted under high vacuum in Tungsten filaments. Apparently, the highly mobile sodium is present in the W filaments. Experimental confirmation was evident by measuring the threshold voltage V of conventional MOSFET's fabricated identically, except for the final contact metallization [Janega, 1983]. The measured V was higher in the devices with thermally evaporated Al than those with E-Beam deposited metal; which indicates the presence of a charge in the gate oxide ,due to mobile ions.

The Electron Beam equipment (Veeco Model VE400) was thoroughly cleaned, its hearth sandblasted, cleaned in hot acetone and isopropyl alcohol. The wafer carriers were inspected and cleaned in a hot 5% solution of HCl and HNO_3, since previous users had deposited titanium and nickel. The entire unit was reassembled and tested for possible leaks. Previously clean samples (using the modified RCA process as in 6.22) were placed in the E-Beam equipment carousel. After a good vacuum was obtained ($<4 \times 10^{-6}$ Torr), 1000 nm of metal was deposited as indicated by the Thickness Monitor. Upon a satisfactory inspection, then the remaining wafers were processed in the same way. Control wafers were also introduced to the E-Beam equipment, to monitor the quality

of the final double insulator structure.

{6.27} DRAIN AND SOURCE CONTACT PHOTOLITHOGRAPHY:

This step required mask alignment, using the contact mask together with the Mask Aligner described before. As one of the final processing steps, great attention was exercized in obtaining a close to perfect alignment. The top metallization (contact) layer was patterned by photolithography using positive photoresist, as per details given in Appendix III. Care was taken to closely monitor the etching process, as neither under or overetching is wanted. The control wafers (dot and ring) etched at a faster rate, than those with the device pattern. This is probably due to the larger exposed surface for the dot and ring pattern, as compared with the device ones. Also, gas bubbles (H_2) form very quickly at the exposed Al surface. This has a more pronounced effect on the very fine device features, slowing the rate of etching.

{6.28} ETCHING ON BACK OF WAFER AND Au DEPOSITION:

Before the Au back contact could be evaporated onto the wafer's back, its back has to be etched very carefully to remove the thick oxide grown in the initial steps. A small Nalgene beaker, with a diameter slightly smaller than the 2" wafer was used. The etching solution was 48% HF, and the wafer was handled very carefully, placed on top of the beaker for 60 secs. The fumes from the strong HF solution are sufficient to remove by etching the thick oxide on the

wafer's back. Thorough rinsing in d.i. water was followed by boiling in isopropyl alcohol to remove any traces of water.

Gold was deposited on the back of each wafer using the thermal evaporation option available in the Veeco VE400 E-Beam equipment. After a good vacuum ($<10^{-5}$ Torr) was obtained, 320 nm of Au was deposited as indicated by the Thickness Monitor.

It was decided that annealing in Nitrogen was not to be done, because from our previous work indications were that the gate leakage current would increase by several orders of magnitude.

{6.29} FINAL MICROSCOPE EXAMINATION:

All device and control wafers were carefully examined under the microscope. This showed that excellent results were obtained and that all wafers exhibited properly etched contact metallization, good alignment and resolution. Photography of most samples was accomplished using the same microscope and negative film camera arrangement described in 6.24. The pictures obtained are shown in Figures 6.6 to 6.12. The aluminium metallization is clearly visible as light grey, under which the source, drain and gate contact windows areas can be seen. The source and drain diffusions are shown in light purple, and the background color is the field (thick) oxide. The pictures also show several areas of the mask, namely the RS Flip-Flop, 2 Input NOR gate and MOS Transistor.
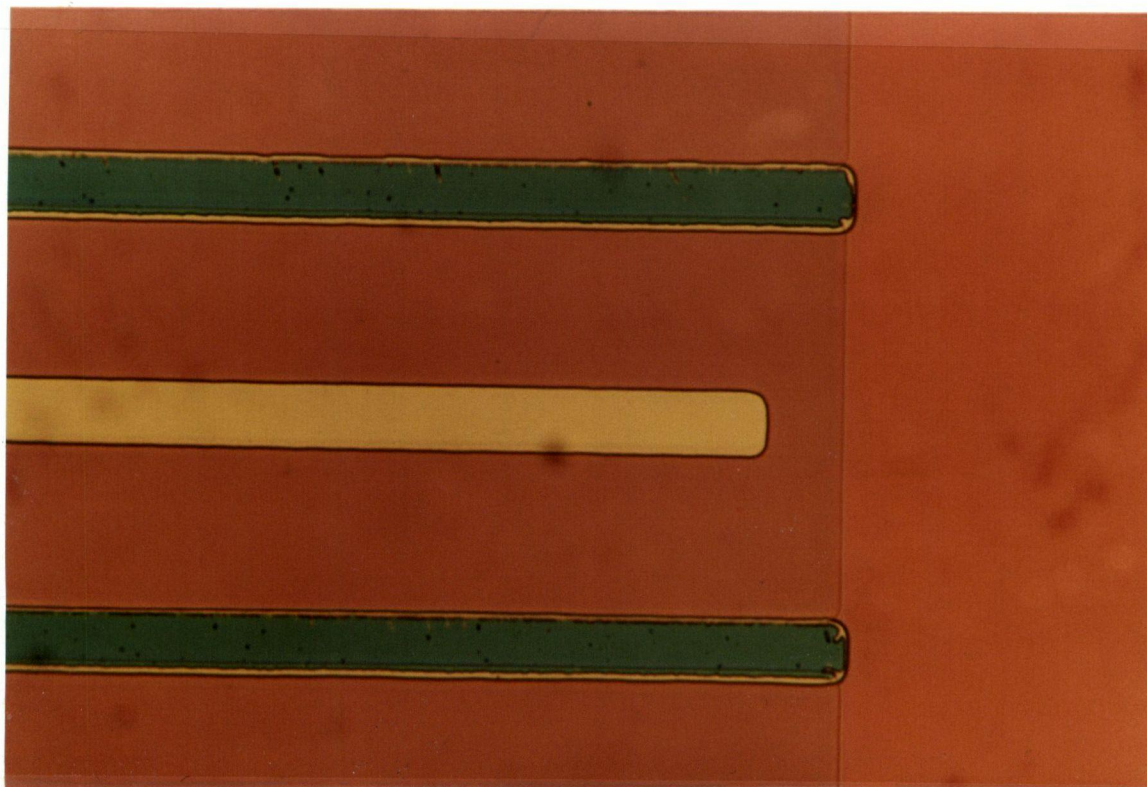
Figure 6.3 MTAOS Transistor; Drain, Source and Gate details.
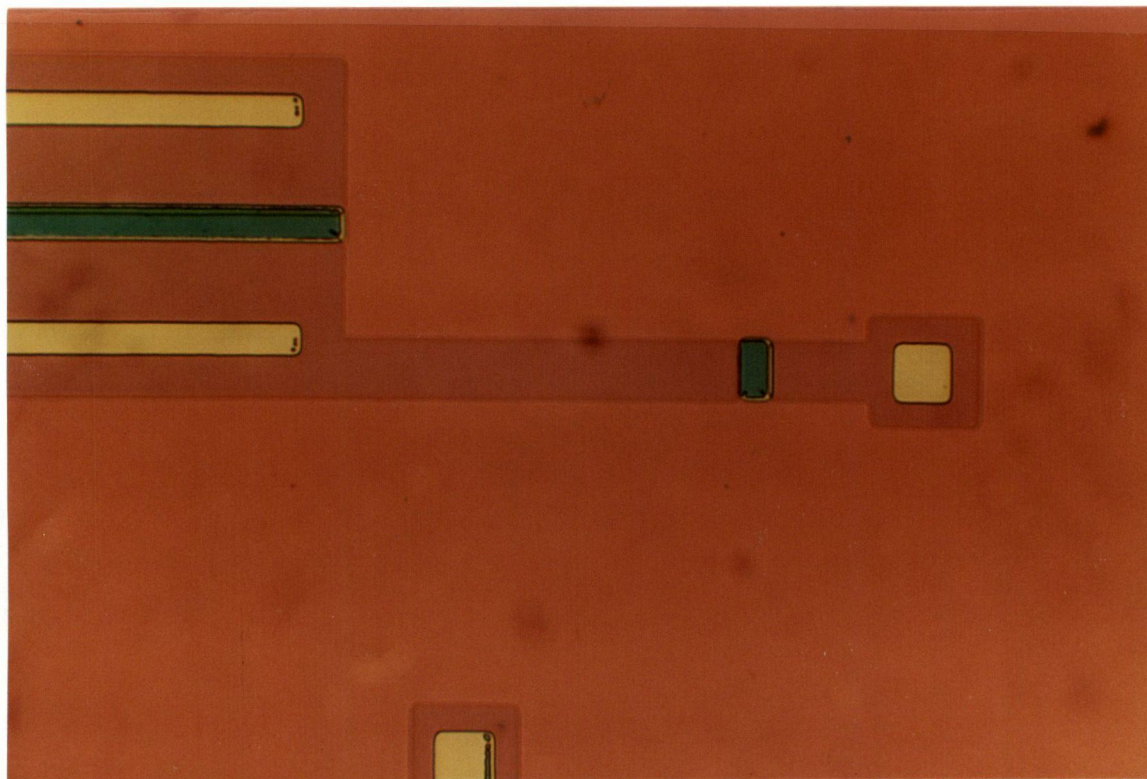
Figure 6.4 MTAOS Transistor, Contact Window area detail.

Figure 6.5 Overall view showing MOSFET and R-S Flip Flop.
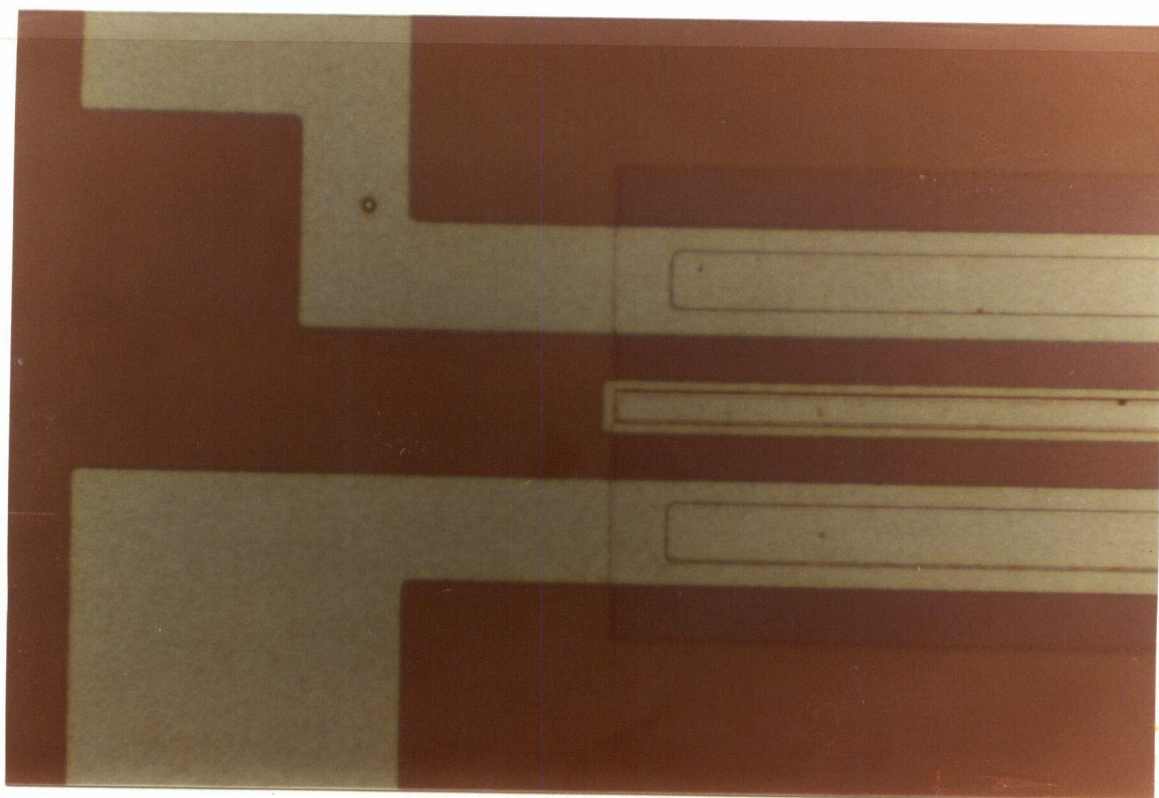
Figure 6.6 MTAOS Transistor Contact Metallization details.
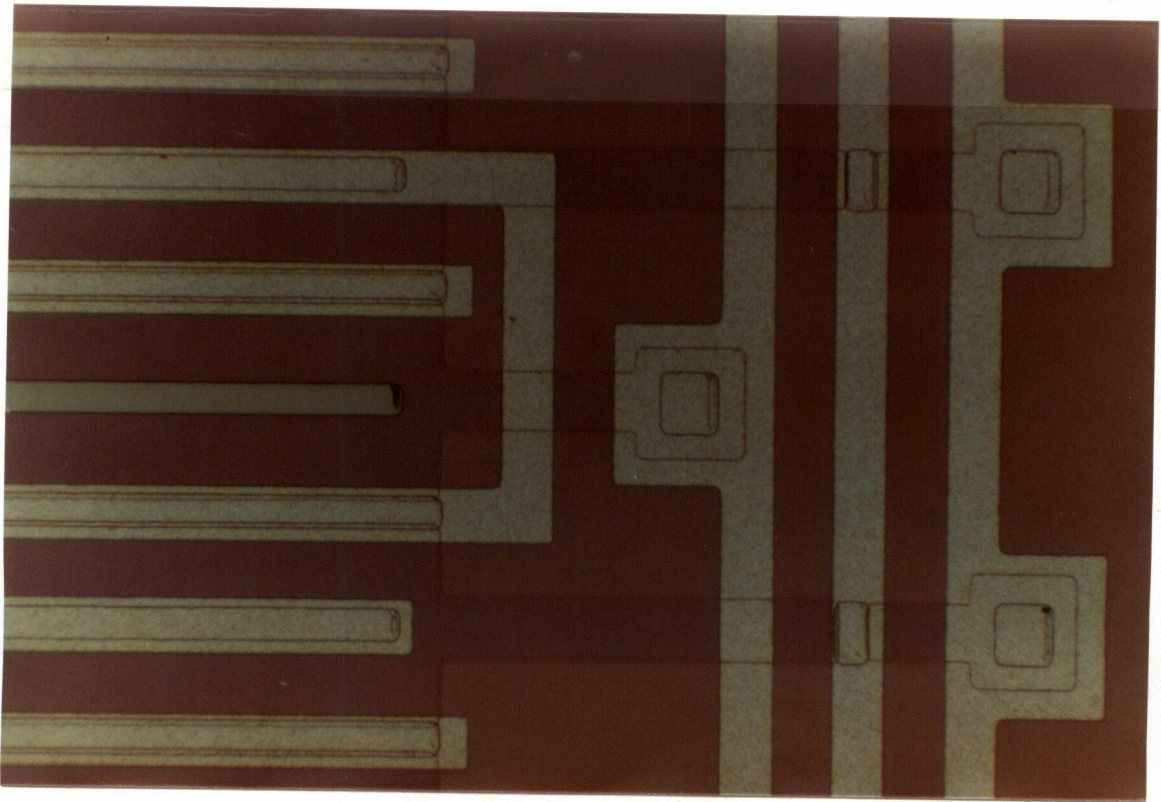
Figure 6.7 R-S Flip Flop Contact Metallization windows.
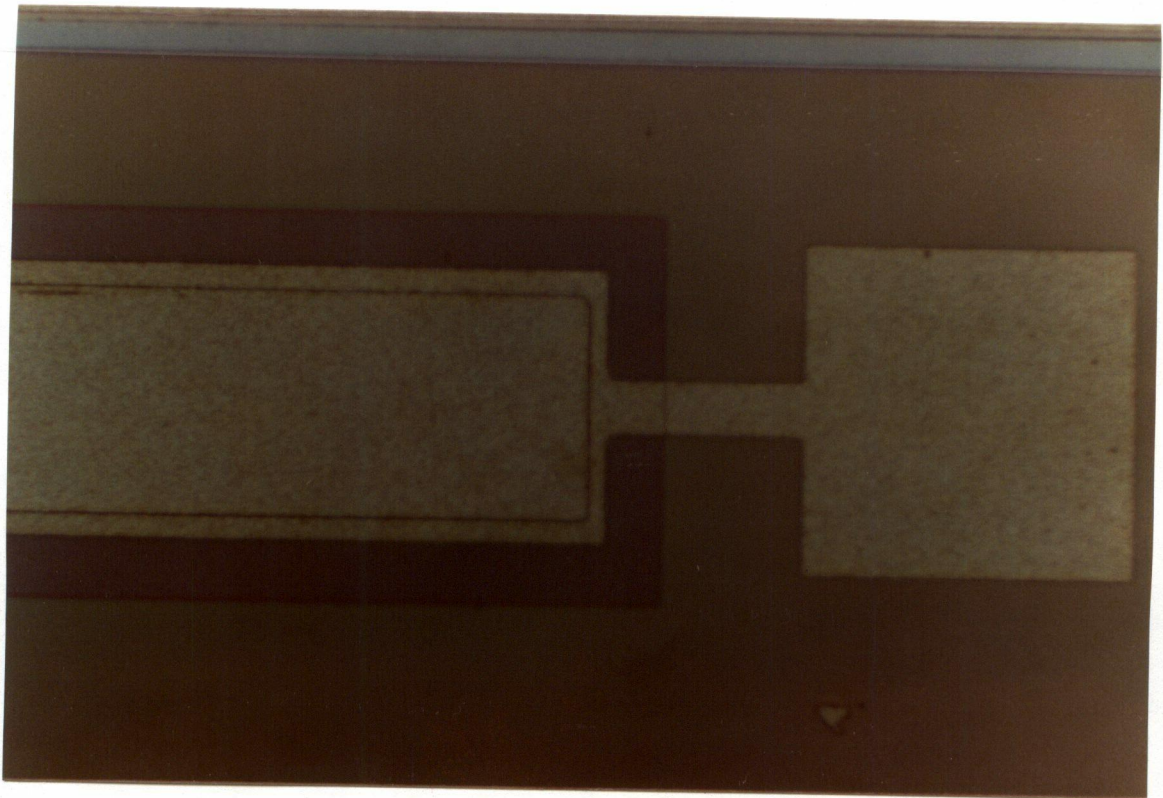
Figure 6.8 MOS Capacitor Area, contact metallization.
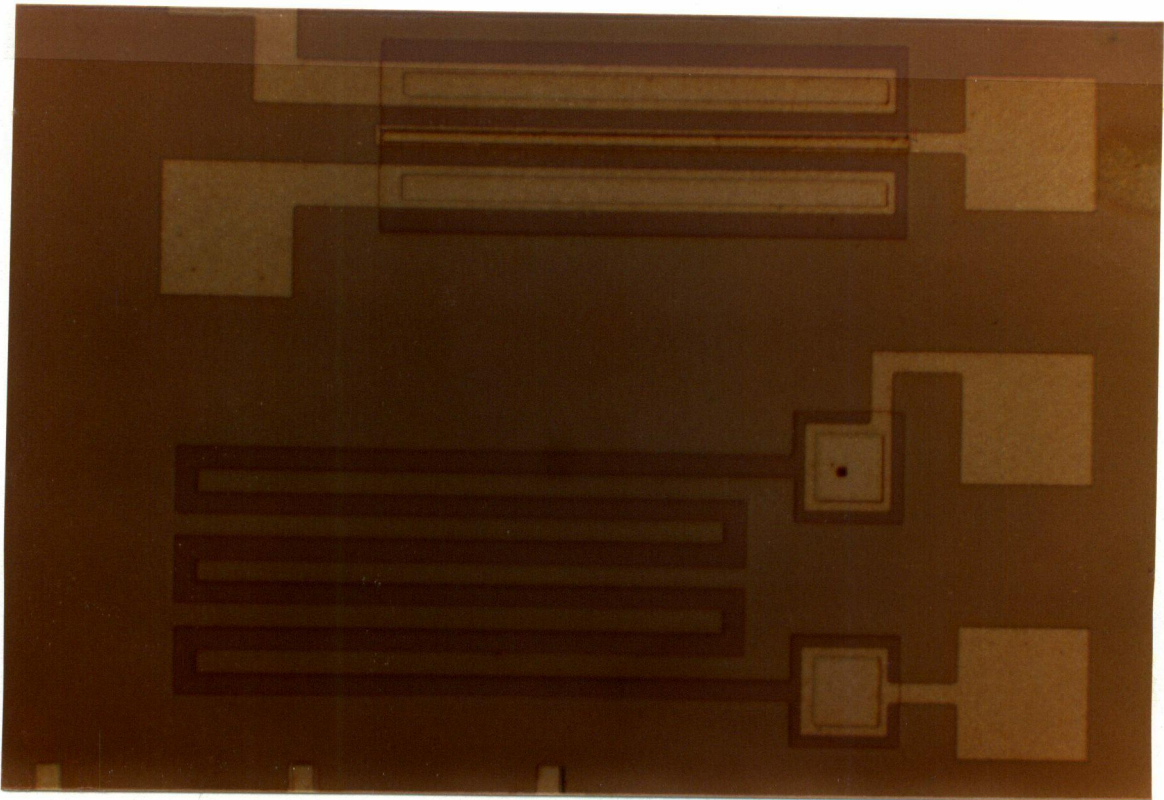
Figure 6.9 Overall view showing MOSFET and diffused
resistor.
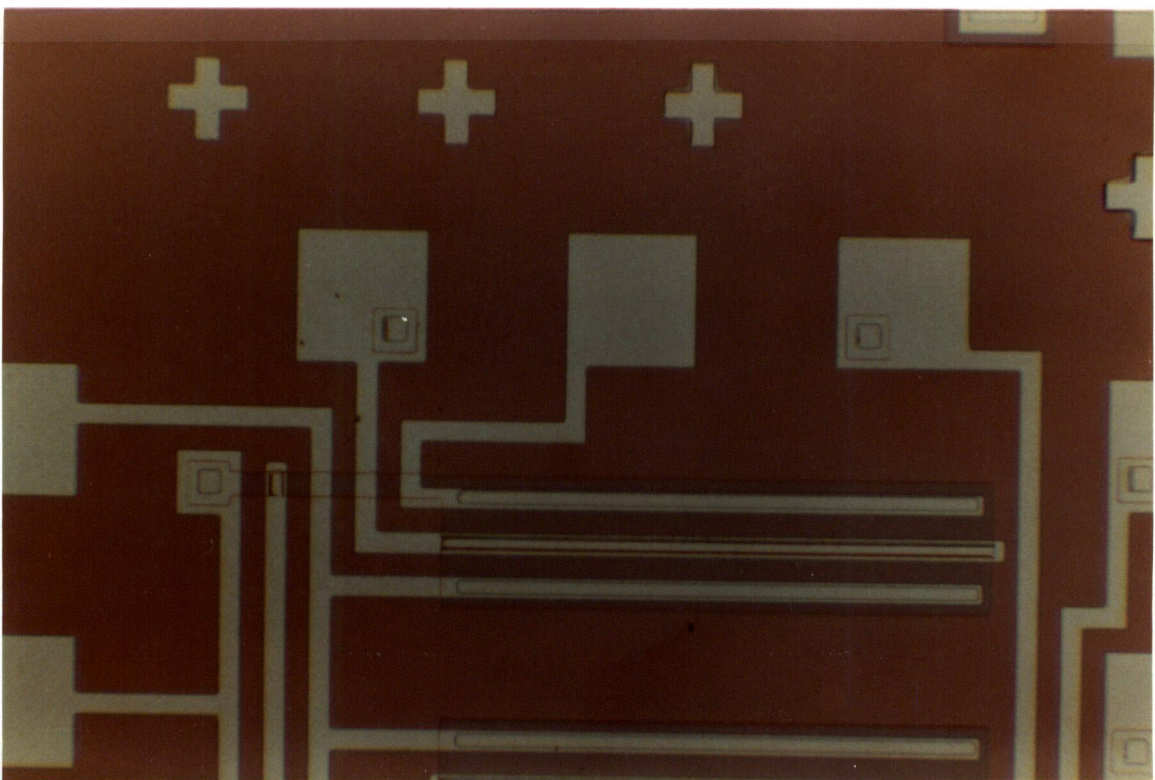
Figure 6.10 Contact pads and alignment markers.
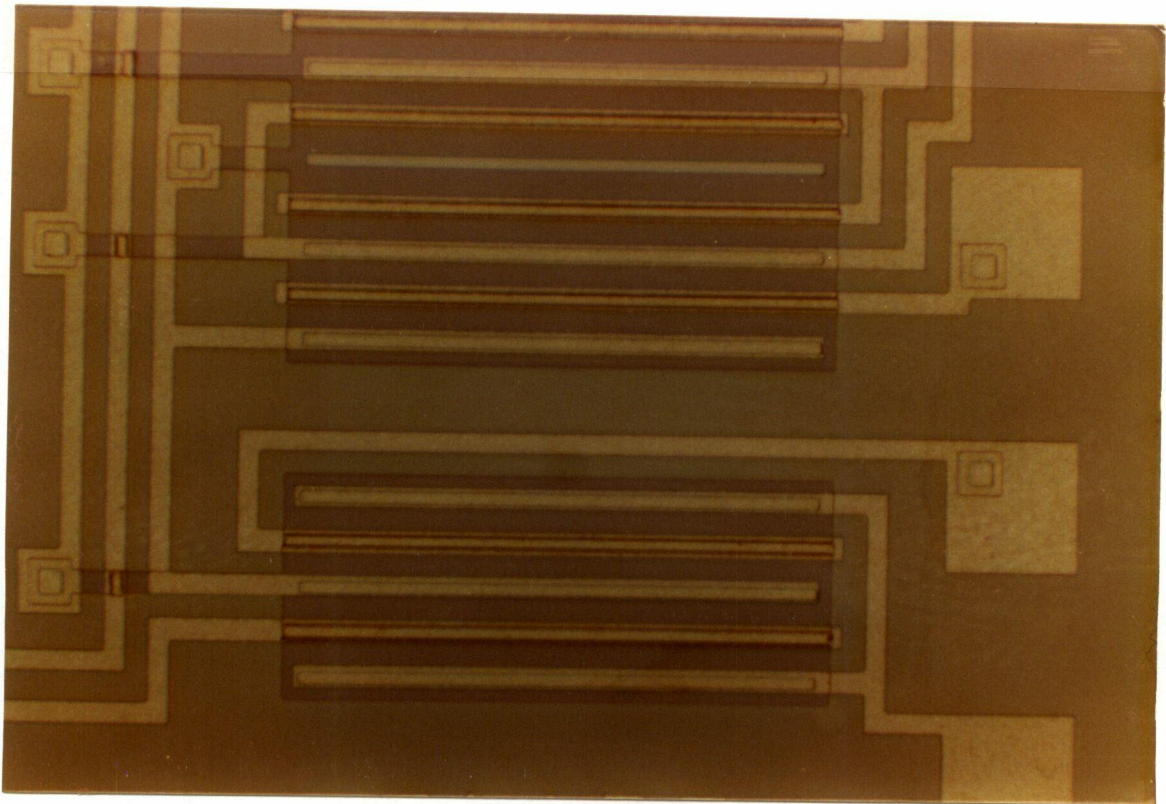
Figure 6.11 NOR Gate and R-S Flip Flop overall view.
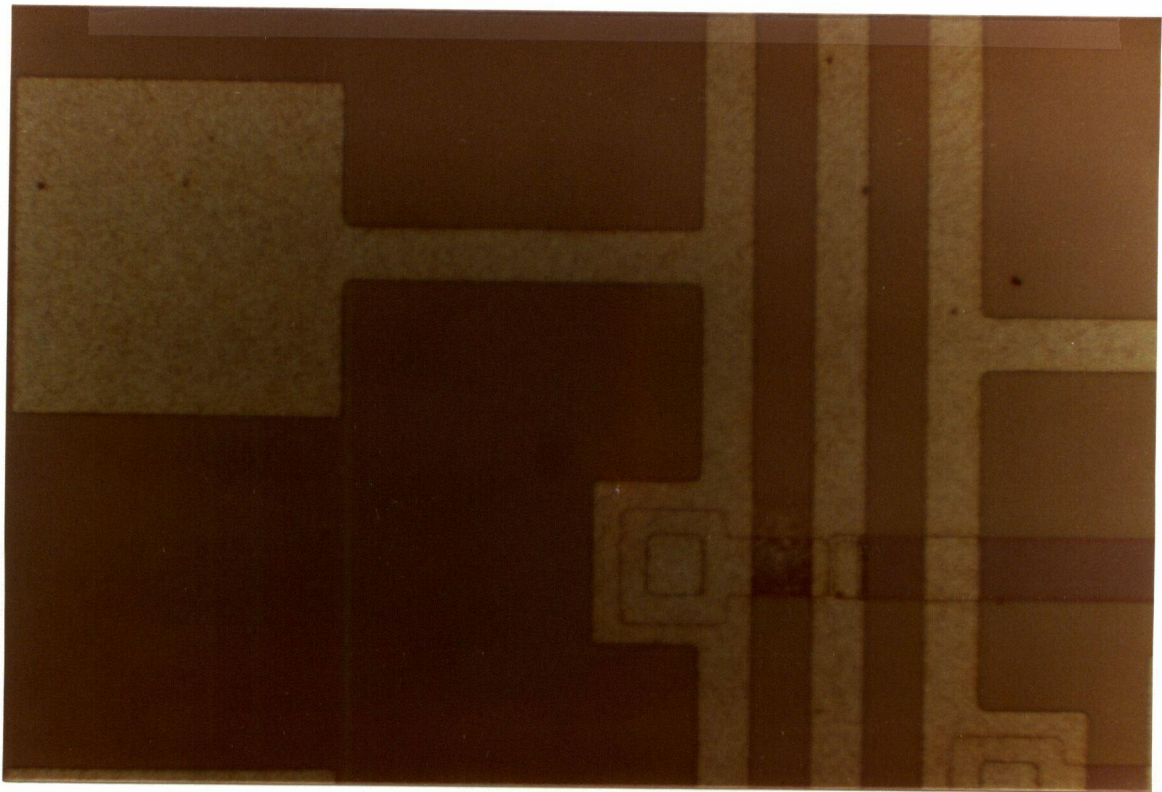
Figure 6.12 Interconnection and contact pad detail.

CHAPTER 7

RESULTS AND MEASUREMENTS ON MTAOS FIELD EFFECT TRANSISTORS

The devices fabricated as described in the preceding Chapters, were tested using conventional methods, in order to determine their overall performance. Of great interest and importance in MOS technology are the following device parameters:

1) The C-V and I-V curves of the gate insulator.

2) The Gate Threshold voltage.

3) The Drain Current-Voltage (output) curves with Gate Voltage as a parameter.

4) The Drain Current vs. Gate Voltage (transfer) curves.

5) The device transconductance and channel conductance.

6) The pulse response, rise and fall times of the Drain output voltage waveform.

{7.1} TESTING AND MEASUREMENT PROCEDURE:

The C-V and I-V curves were obtained using the method and equipment described in Chapter 5. The only difference was the use of the Wafer Probing Microscope (Micromanipulator Model 1800 AO Prober with AO Instruments Model 570 microscope). This made it possible to make a good contact to the Al metal pads in the dice, and to select the proper mask quadrant. The latter is a consequence of the

mask organization, as they are made in such a way to reduce their number, at the expense of yield. Four patterns are printed in the same mask, hence only one dice is functional and the remaining three are scrambled.

The gate threshold voltage was obtained by inspection of the Id vs. Vds curve, when the gate is connected to the drain. The projection of the curve to the Vds axis gives the V_T. This is a standard industry test on MOS devices. The drain current follows then the relation $Id=\beta Vds^2$. The V_T can also be obtained by inspecting the transfer curves as explained below.

The output curves were obtained with a Tektronix 577 Transistor Curve Tracer and they provide the quasistatic characteristics with the gate voltage varying as a staircase function. Pictures were obtained of the various devices, and they are shown in Figures 7.13 to 7.22. An attempt was made to obtain the static output curves. This was done using the circuit of Figure 7.1. The gate voltage was accurately fixed with the attenuator (for precise gate voltage control) and then the drain voltage was slowly swept manually. The result is a set of parametric curves, which are quite close to the ones obtained with the curve tracer, as shown in Figures 7.2 and 7.3.

The transfer curves were obtained by static measurements, using the test equipment arranged as shown in Figure 7.1. By keeping the drain voltage fixed as a parameter, the gate voltage was swept manually and the drain current measured. The resultant curves are shown in Figures
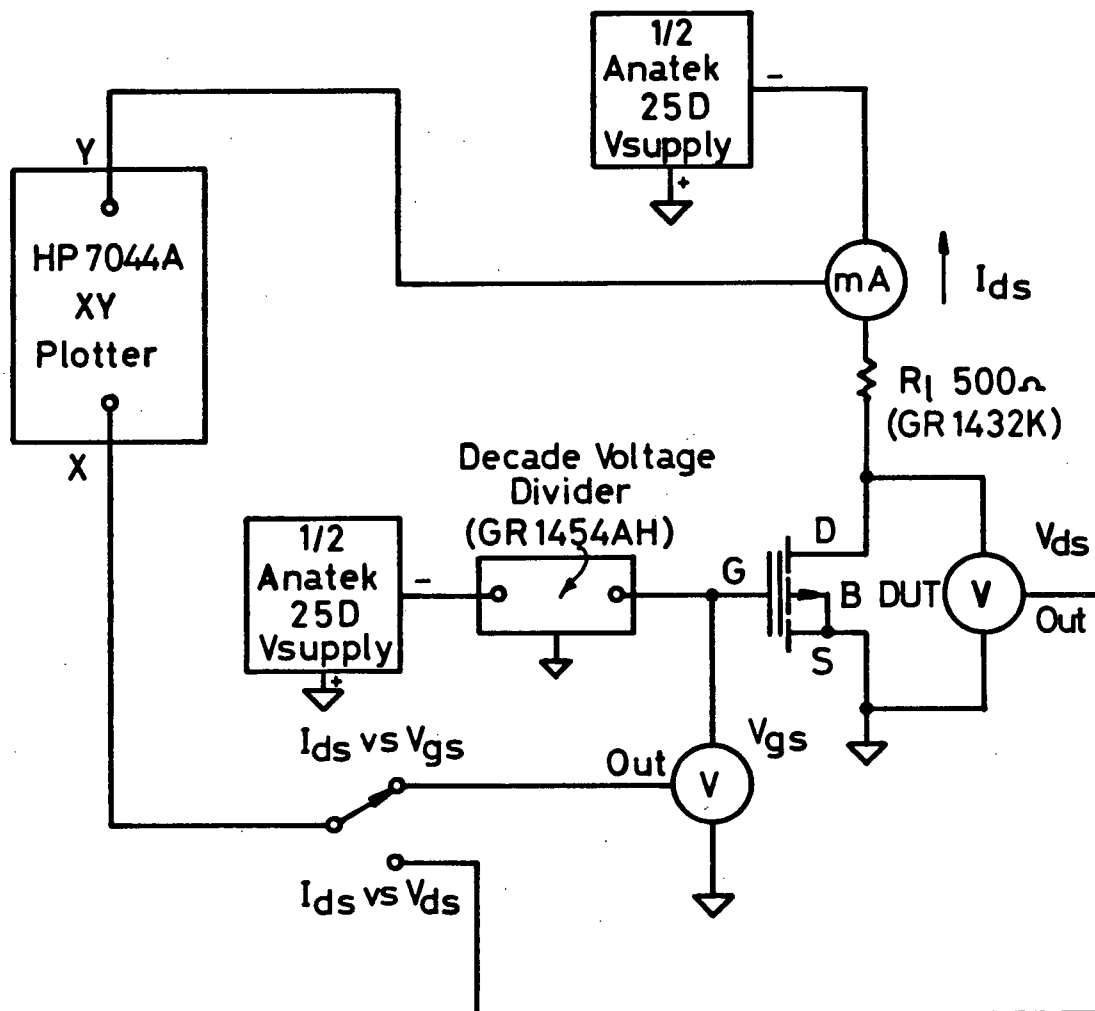
Figure 7.1 System for Plotting MOSFET Static Curves.

Figure 7.2 Static Output Curve, Sample MTAOS3 Thermal.
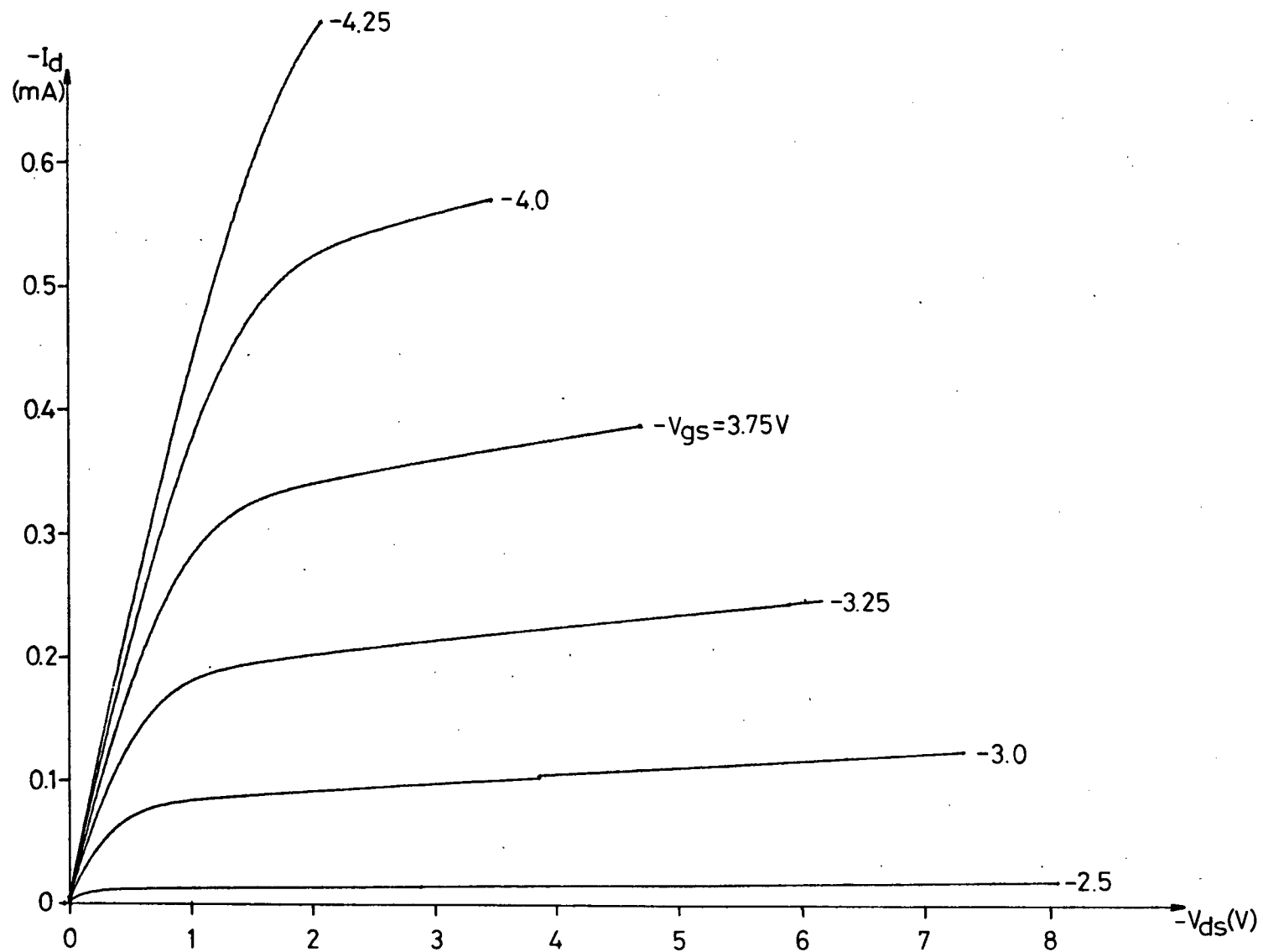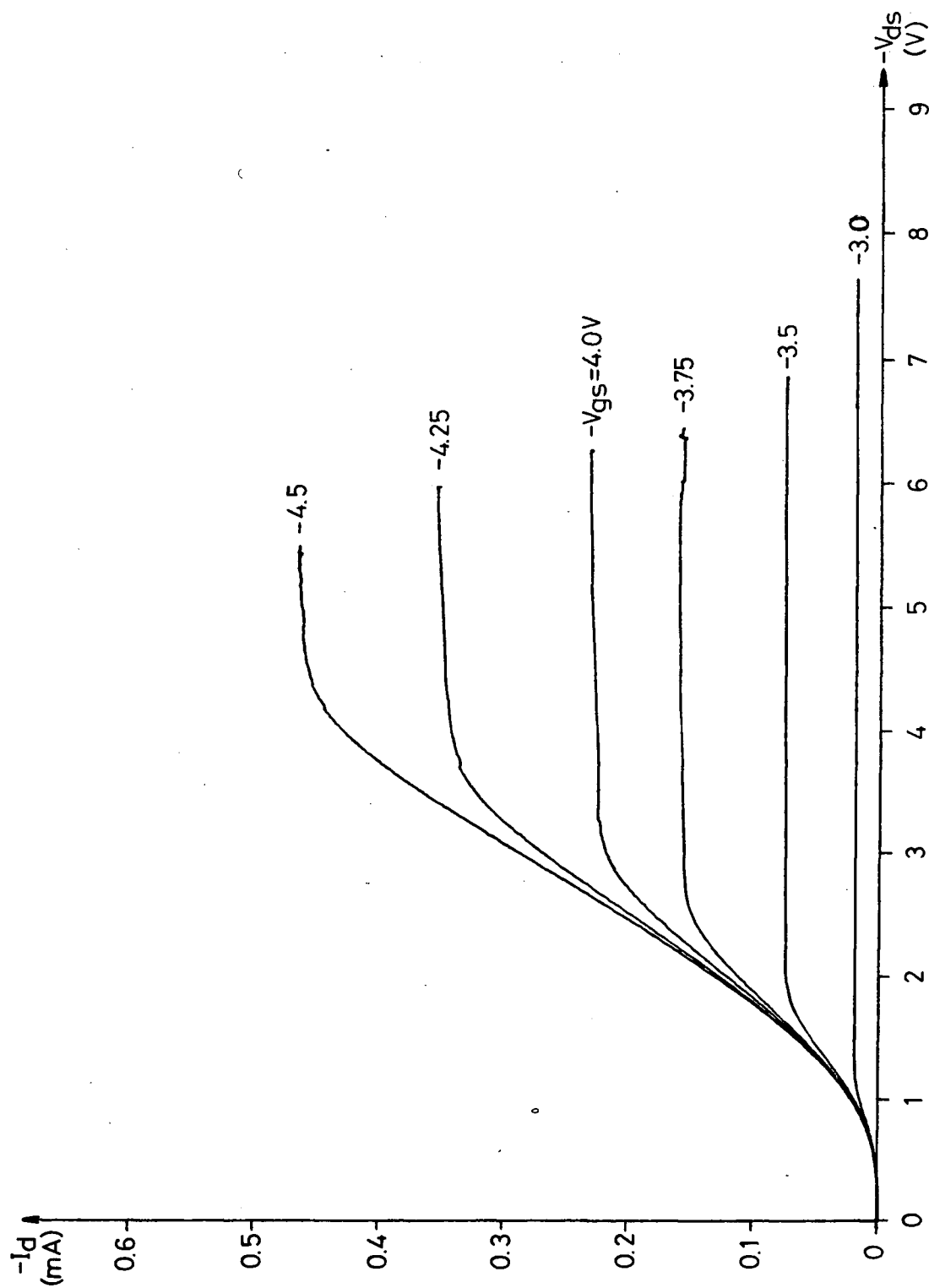
Figure 7.3 Static Output Curve, Sample MTAOS4 Anodic.
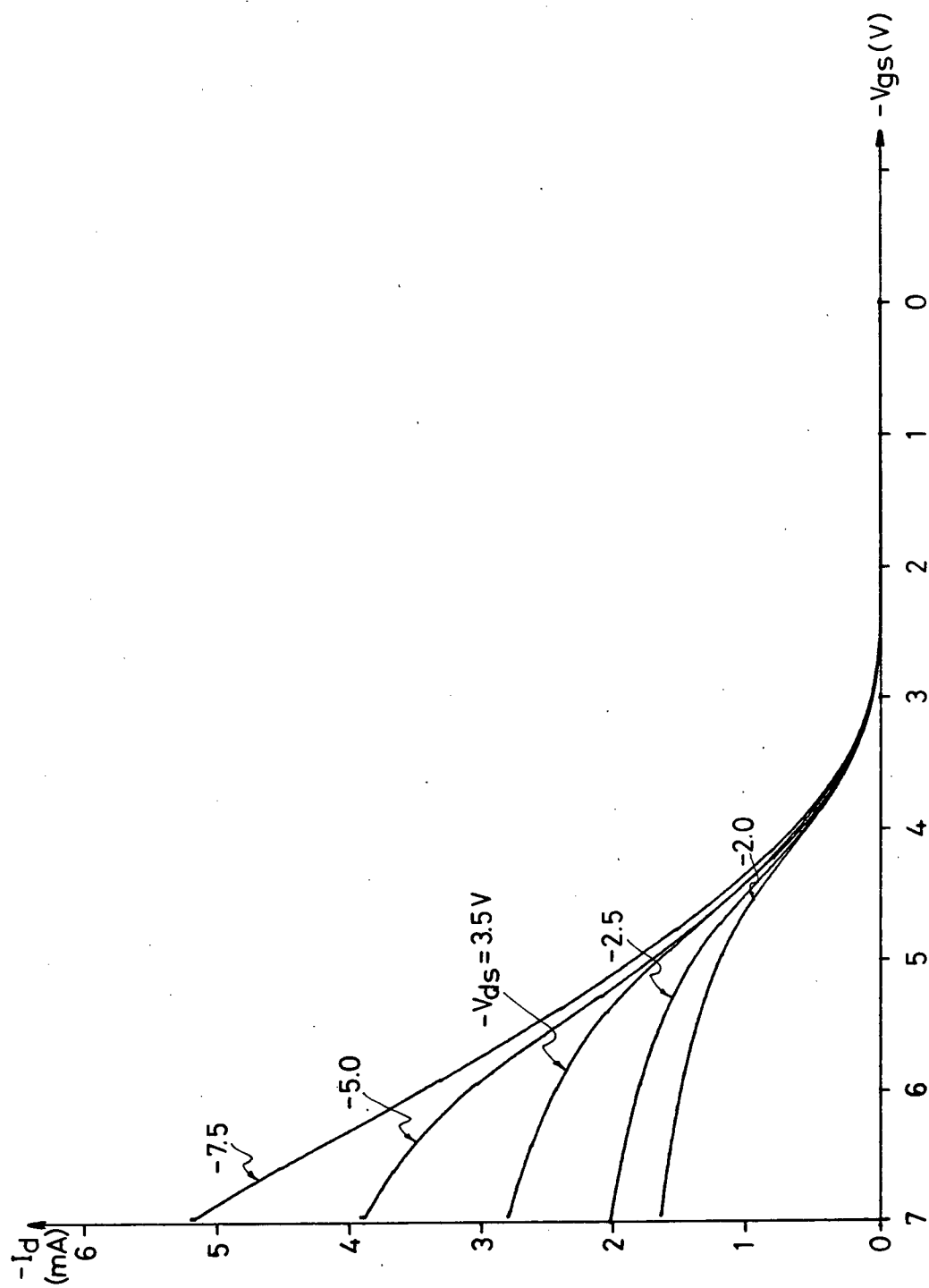
Figure 7.4 Static Transfer Curve, Sample MTAOS3 Thermal.
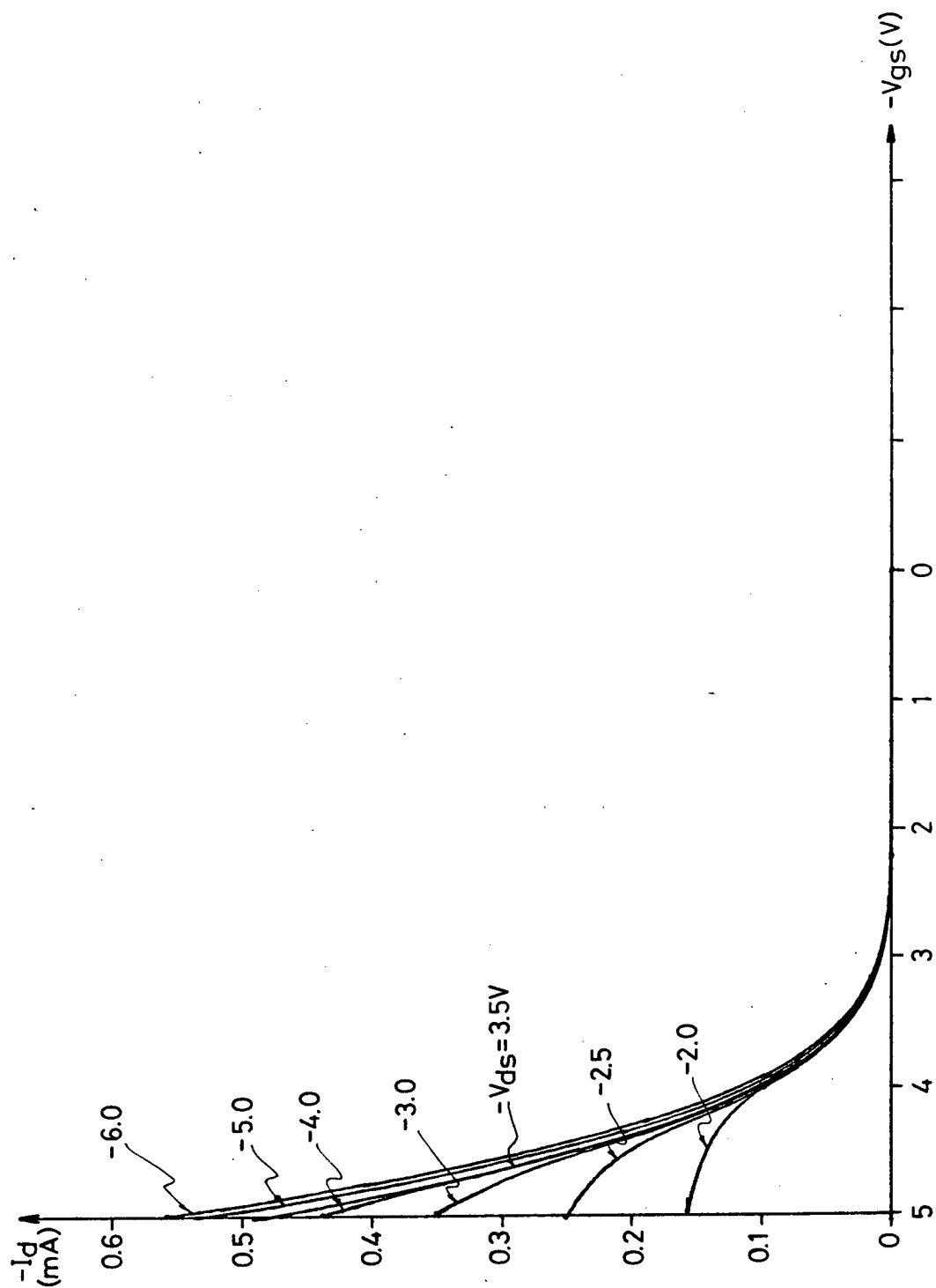
Figure 7.5 Static Transfer Curve, Sample MTAOS4 Anodic.

7.4 and 7.5. The gate threshold voltage can be obtained by inspecting these curves at the point where the drain current falls to a negligible value, i.e. the cutoff point. Above this threshold, appreciable drain current flows, and below it, the current is very small or near zero.

The transient or pulse response was obtained using the circuit shown in Figure 7.6. A Microdot Model F210B Function Generator was the pulse source and a Tektronix 5440 Oscilloscope with camera attachment (Tektronix C-5C) was used to record the output waveform. Measurements were made at 10 and 100 kHz, 50% duty cycle square wave, repetition frequencies. Care was taken to minimize the lead lengths at both gate and drain connections, as any stray inductance and/or capacitance can affact the results. Tests were performed with Vdd=-6 V, a resistive (carbon) load resistor of 1 kΩ, and a gate pulse of -5 V peak. By correctly triggering the oscilloscope, it is possible to examine the rising and falling edge of the drain output voltage pulse, as the trigger polarity can be selected. Delayed time measurements were helpful in observing with greater detail the pulse edges and shape at the output.
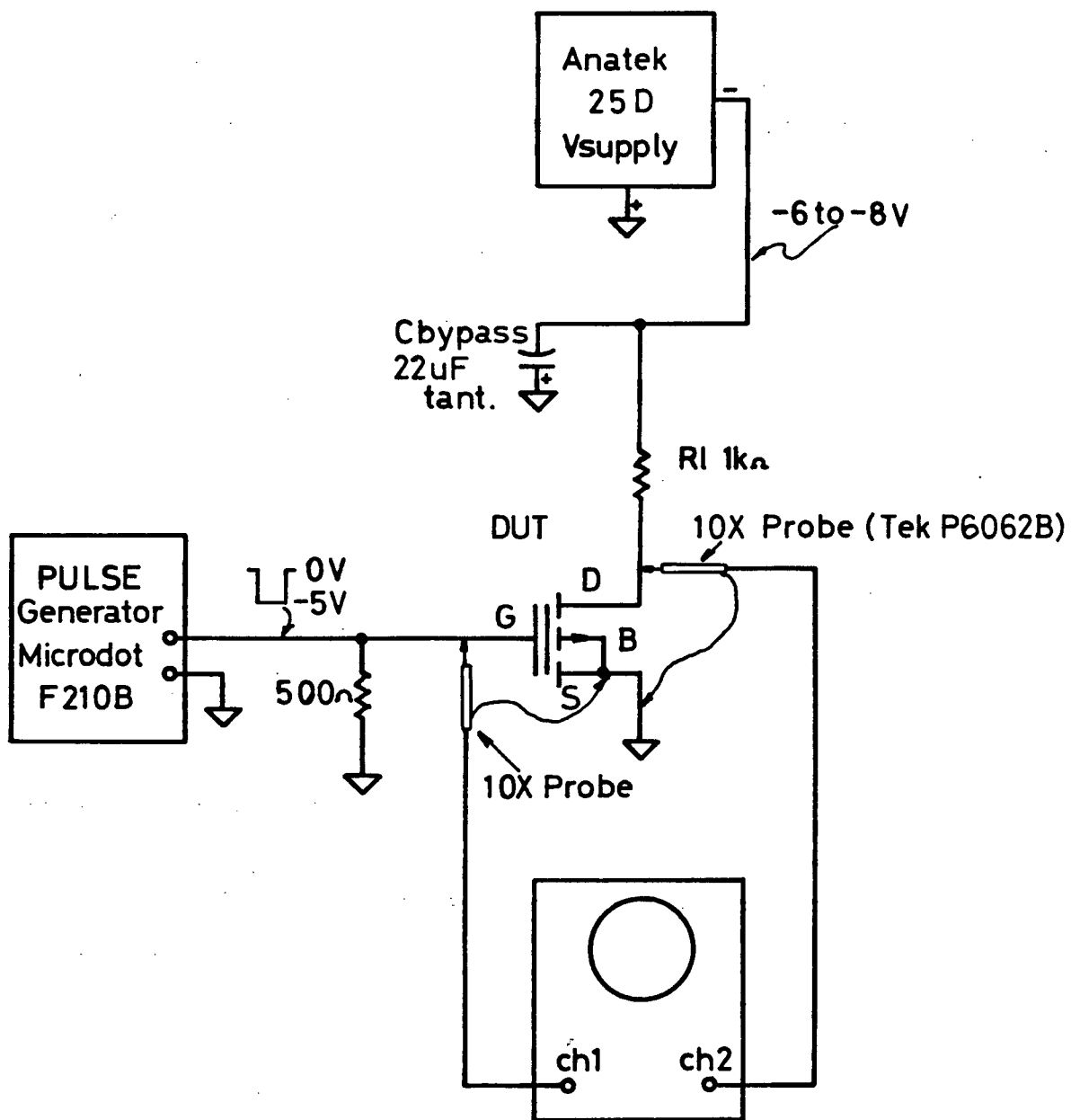
Figure 7.6 System for Measuring the MOSFET Pulse Response.

{7.2} DISCUSSION OF RESULTS

{7.2.1} C-V CURVES ON DOUBLE DIELECTRIC INSULATOR:

As mentioned in the previous chapter, additional samples were prepared and processed, so that the quality of the double dielectric insulator could be evaluated independently from the device wafers. The curves are shown in Figures 7.8 and 7.9. From them, it can be seen that a good quality double insulator is obtained, with well defined accumulation and inversion regions, little hysteresis, and generally a smooth curve that indicates that surface states have small or no influence on the insulator performance. This is essential for the proper and successful operation of the double dielectric MOSFET, and the high quality C-V curves obtained are indicative that the technology is not only feasible, but also successful. Similar results are obtained for both anodic and thermal Ta_2O_5 samples, except that significantly less accumulation capacitance is obtained for the anodic process, as compared with the thermal tantalum oxide. This is probably due to a inhomogeneous or porous film, as discussed in Chapter 5. As a consequence, the dielectric constant of the film is reduced, resulting in less oxide capacitance which is interpreted in the C-V plot to correspond to the capacitance in accumulation.

An attempt was made to obtain the C-V gate characteristic in the MOSFET devices. This would be the definitive indication of the double dielectric insulator quality. The C-V plotting equipment already described, was connected to the wafer probing microscope, with special

attention given to stray capacitances and lead lengths. The Capacitance Meter was carefully nulled and adjusted. A successful C-V plot was obtained between the gate and substrate for the thermal Ta_2O_5 devices, as shown in Figure 7.9. In the case of the anodic Ta{oxide}, a curve with large hysteresis was obtained (Figure 7.10), indicating that for a particular wafer, the quality of the double insulator approached those of a memory devices, as described in the paper by Angle and Talley (1978). It is interesting to notice that the C-V curve for the thermal Ta oxide sample is similar of that of a low frequency MOS capacitor C-V plot [Grove, 1967; Penney and Lau, 1979]. This is due to the fact that in the inversion region, minority carriers have to be generated thermally, usually from electron-hole pairs. However these recombine at a certain rate. The C-V plot is obtained by a small AC signal superimposed on a linear sweep, which is used to measure the change of capacitance with voltage. If the sweep rate is constant, we have two possibilities: the recombination rate can be such that not enough minority carriers are generated; or a sufficient number minority carriers are generated to form an inversion layer that follows the sweep voltage. In the first case, a low frequency C-V plot is obtained, and no inversion takes place for large positive gate voltage. In the second case, a high frequency curve with a defined inversion region is obtained. In the case of a MOSFET, in which the gate and channel are bounded by the source and drain regions, these provide an electrical connection for the inversion layer,
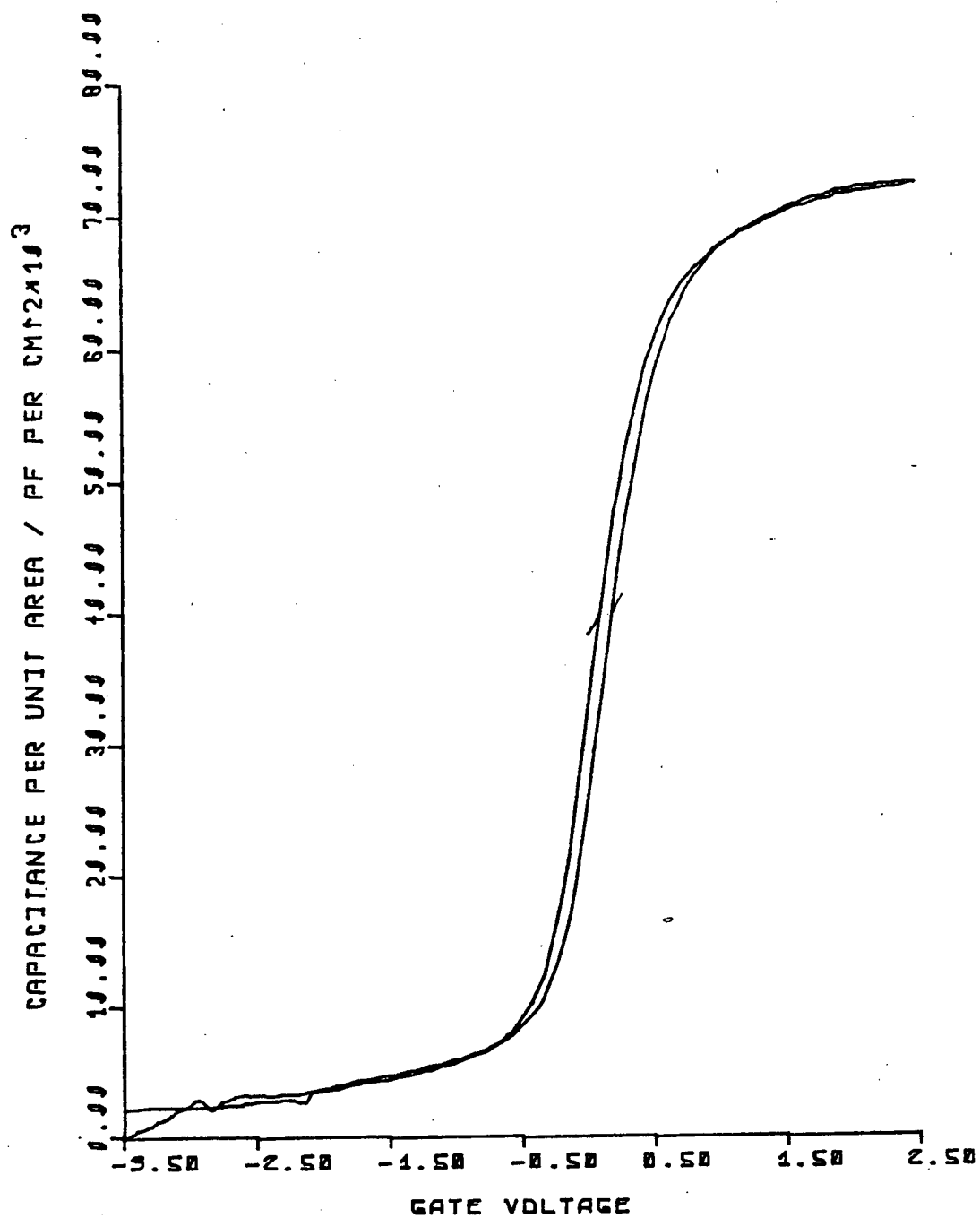
Figure 7.7 C-V Curve on Double Dielectric Test Wafer (sample MOSCTest 200A thermal).
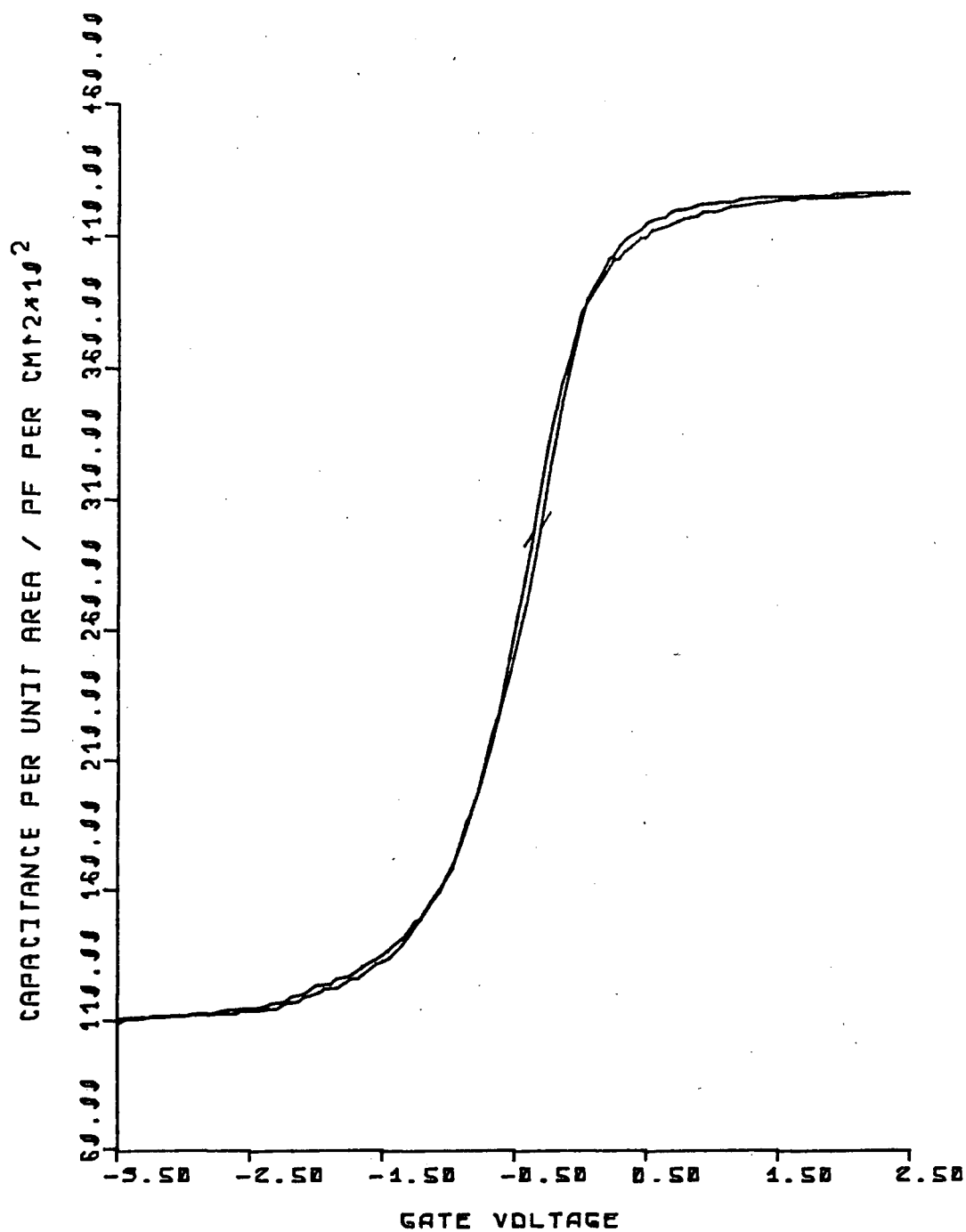
Figure 7.8 C-V Curve on Double Dielectric Test Wafer (sample MOSCTest 200A anodic).
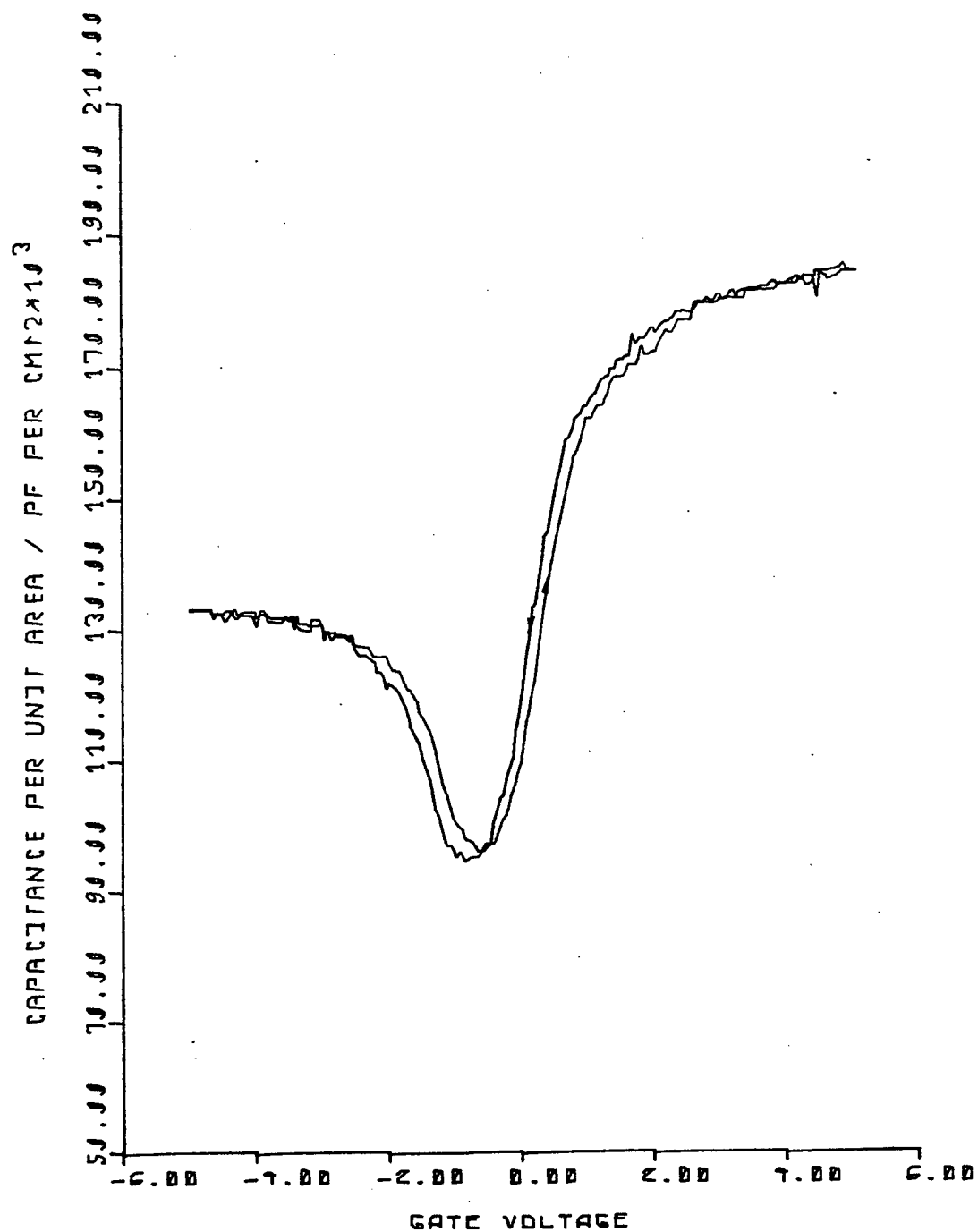
Figure 7.9 C-V Curve of MOSFET Gate, Thermal Sample MTAOS3.
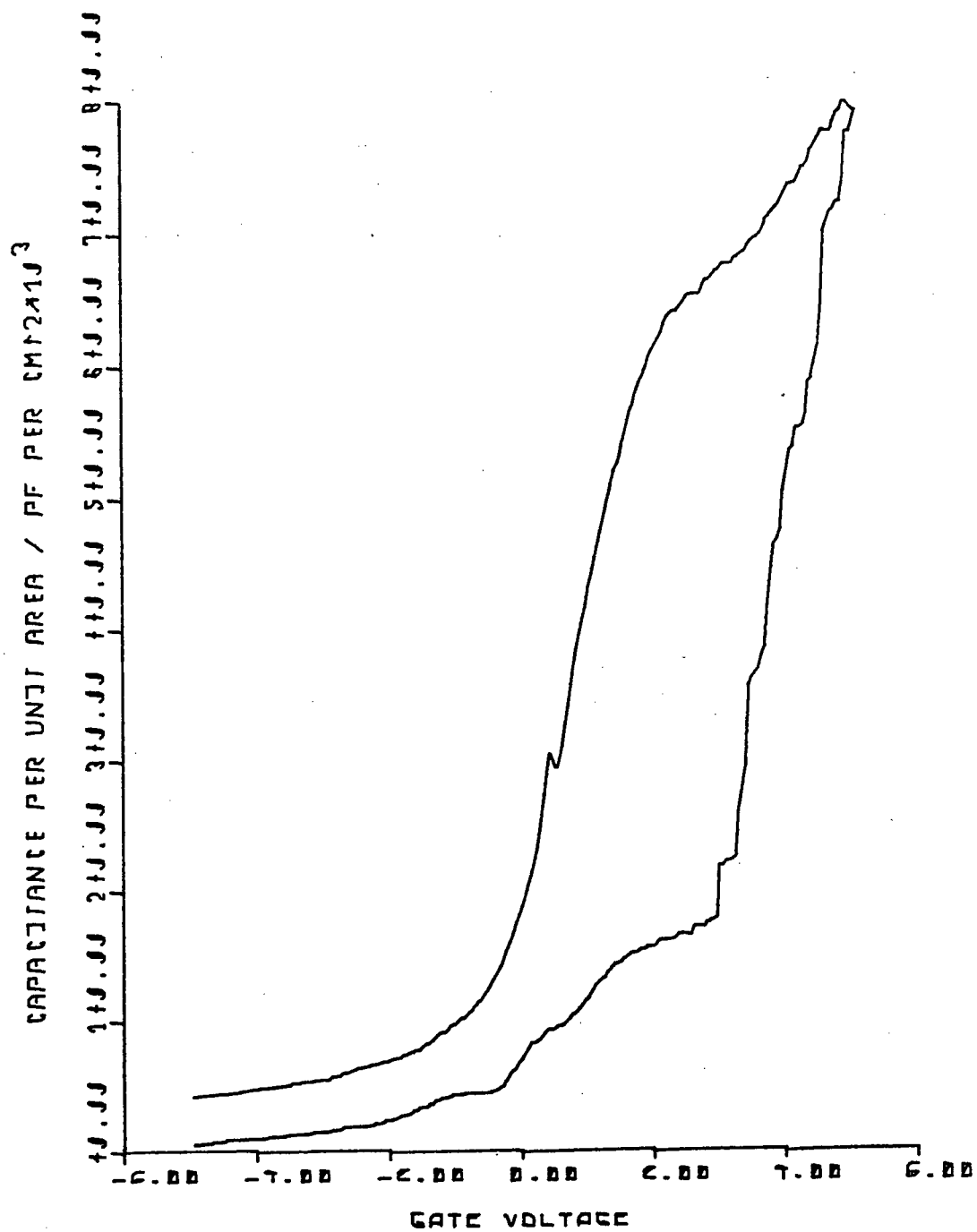
Figure 7.10 C-V Curve of MOSFET Gate, Anodic Sample MTAOS5.

acting as a sink or source of minority carriers to the external circuit. Thus, for large gate voltage, no inversion is produced and the capacitance is then that of accumulation, interpreted as the gate insulator capacitance.

{7.2.2} I-V CURVES ON THE DOUBLE DIELECTRIC GATE INSULATOR:

The I-V measurements gave an idea of the conduction (leakage) current of the gate under normal operation. The curves were obtained in a quasistatic way, in order to avoid any capacitive effects. The results are shown in Figures 7.11 for a typical thermal oxide sample and in Figure 7.12, for an anodic process wafer. Differences between the leakage currents are large, indicating that the anodic oxide has more leakage than its thermal counterpart. Also, the position of the threshold of gate conduction depends on the applied source to drain voltage, Vds. This was not the case of the thermal Ta{oxide} samples, in which a small, but consistent leakage current flows.

{7.2.3} GATE THRESHOLD VOLTAGE:

A standard procedure to determine the threshold voltage V_T, is to perform a plot of the drain current Id vs. drain to source voltage Vds, with the gate connected to the drain circuit. This ensures that the transistor is fully saturated, thus the square law characteristic of the Ids vs. Vds curve. From the curve obtained, the threshold voltage is that which above it, there is appreciable flow of drain current, and below it, there is very little. This is

obtained by inspection of the Transfer or Saturated curves, the latter are shown in Figures 7.14 and 7.18.

{7.2.4} THE OUTPUT CURVES:

The drain current vs. Drain to source voltage, with the Gate voltage as a parameter (output characteristics) was obtained both with the Transistor Curve Tracer (Tektronix 577) and in a quasistatic way. This is because the curve tracer generates a staircase pulse in the gate circuit, and some concern existed whether improper responses could be created. Both methods gave similar results, however it was found that more devices were damaged using the curve tracer, than with the manual quasistatic method. This was in spite of all precautions taken to ensure than no static discharge was damaging the gate insulator by oxide breakdown. Excellent quality curves were obtained (Figures 7.13 and 7.17) indicating that the devices behave electrically like MOSFET's and that they present gain if connected in a circuit. In some wafers, the yield was low and some transistors had excessive gate leakage, probably due to processing faults. An example is given in Figures 7.21 and 7.22. Also, the anodic Ta{oxide} wafers were very sensitive to applied voltages and it was quite easy to damage them. The order of connecting the probes in the Wafer Probing equipment is also important: the least damage was with the source probe first, gate second and then the drain. Voltage spikes (pulses of short duration) also contribute to a lower yield: for example, the Wafer Probing Microscope is equipped
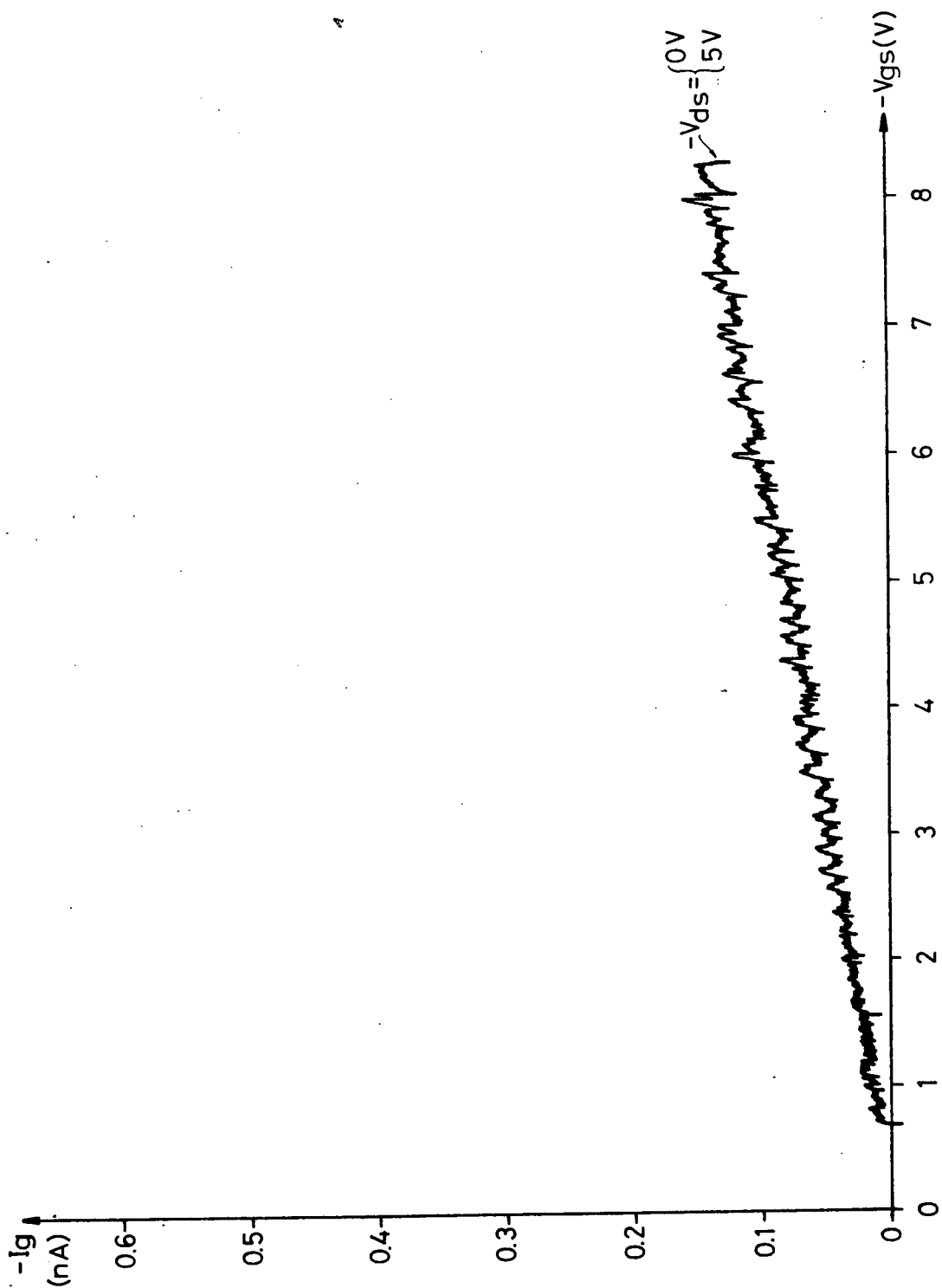
Figure 7.11 I-V Curve on MOSFET Gate,
Thermal Sample MTAOS3.
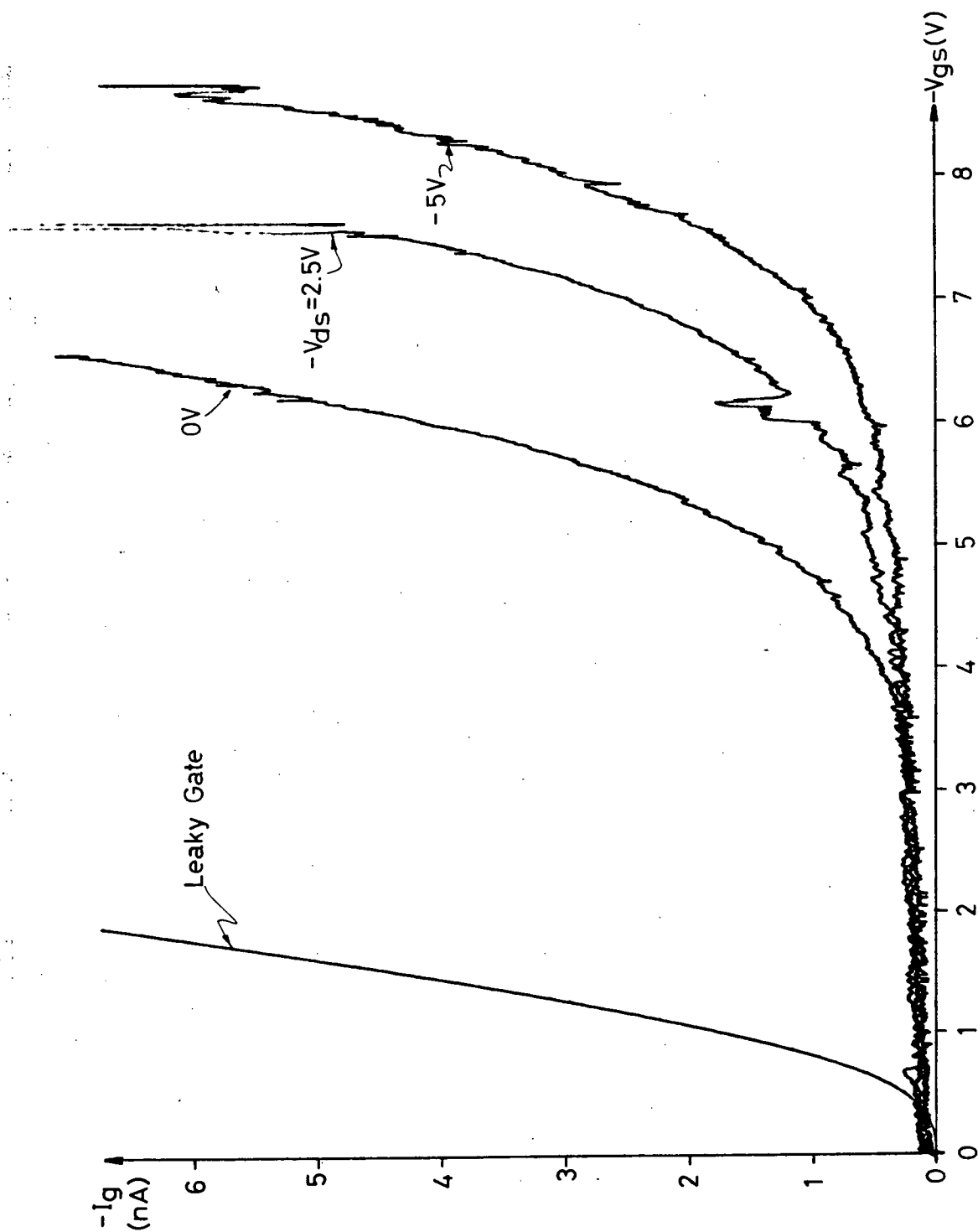
Figure 7.12 I-V Curve on MOSFET Gate,
Anodic Sample MTAOS4.

with a fluorescent lamp and ballast (!), which generates a beautiful spike when the lamp is switched on or off. After a few disasters, we simply disconnected the lamp and grounded its leads.

An examination of Figures 7.3, 7.13 and 7.17 indicates that for low values of Vds, the corresponding drain current does not have a linear variation. Moreover, the gate voltage has little effect on this phenomenon, which shows that the channel conductance does not follow the usual relationship with Vds and Ids, i.e. the slope of the curves close to the origin are quite distinct and equal to the channel conductance. The reasons behind this unusual behaviour are not known, but it is possible that the changes in channel conductance are related to electron trapping in the silicon.

{7.2.5} THE TRANSFER CURVES:

These were obtained by the quasistatic method, manually adjusting the gate voltage, and measuring the drain current, with the drain voltage as a parameter. The slope of these curves gives the transconductance of the device. These indicate that the devices exhibited moderate values of gm, as summarized in Table 7.1. Again, curves were obtained for both anodic and thermal Ta{oxide} samples. The first ones presented a smaller transconductance as compared with the latter. This is probably due to a reduced insulator capacitance, as described before. The curves are shown in Figures 7.4 and 7.5.

{7.2.6} PULSE RESPONSE OF THE DD MOSFET's:

Another important parameter is the switching time of the device, characterized as the ton and toff times, corresponding to the time to turn ON and turn OFF the transistor. A pulse generator and fast oscilloscope were used, as shown in Figure 7.6. Short leads around the device, and good grounds assured a minimum of stray capacitance and inductance. Several measurements were made, one at 10 kHz and another at 100 kHz square waves. Delayed sweep was used to expand the trace around the switching points, in order to accurately measure ton and toff. Some differences exist between the anodic and thermal Ta{oxide} samples. Generally, the anodic version is slower than the thermal oxide samples, when used in the same circuit. The pictures of the actual scope traces are shown in Figures 7.15, 7.16, 7.19 and 7.20. Table 7.1 summarizes the results obtained in the MOSFET measurements.

TABLE 7.1

SUMMARY OF DOUBLE DIELECTRIC MOSFET CHARACTERISTICS

	THERMAL Sample MTAOS3	ANODIC Sample MTAOS4
Cox	185000 pf/cm^2	84000 pf/cm^2
Gate Leakage	1 nA at Vgs=-5 V	4 μA at Vgs=-5 V
Gate Threshold	-2.0 V	-2.5 V
gm at Vgs=-3 V	300 μS	475 μS
gm at Vgs=-6 V	1750 μS	1125 μS
ton	400 ns	500 ns
toff	220 ns	250 ns

{7.2.7} SPICE SIMULATION OF MOSFET CHARACTERISTICS:

In order to verify the performance of the double dielectric devices, the simulation program SPICE was used in conjunction with the device parameters and external circuit components. This was done using the same circuit values as used in the actual pulse test; plus the circuit stray capacitances. The MOSFET geometry parameters were obtained from the microscope inspection of the devices (channel length and width, drain and source areas and perimeters). The threshold voltage and transconductance parameter were obtained from experimental values. The DC Transfer Curves indicate that the device has a threshold close to -2.5 V and the Transient Analysis shows a fast turn on in 10 ns and a turn off in 70 ns. The simulated device is then much faster than the actual one, as the internal junction and gate overlap capacitances were not taken into account during the simulation. Also, the small stray inductances of connecting wires and cables were not included in the simulated model. The combined effect of these result in slower pulse response for the measured device. Results of the SPICE simulation are given in Appendix IV.
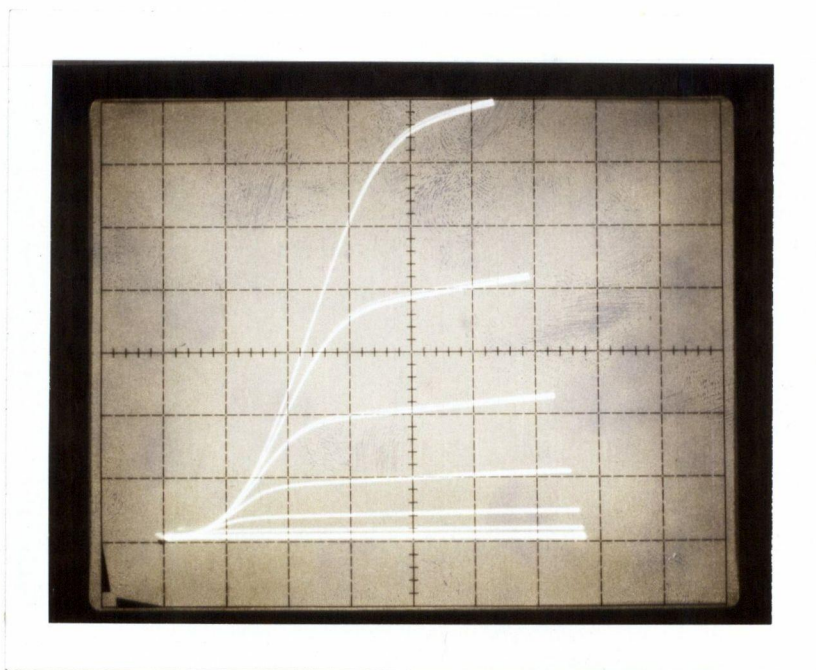
Figure 7.13 Double Dielectric MOSFET Output Curves, Sample
MTAOS 3 (Vgs step 0.5 V, Hor. 1 V/div., Vert. 0.1 mA/div.)
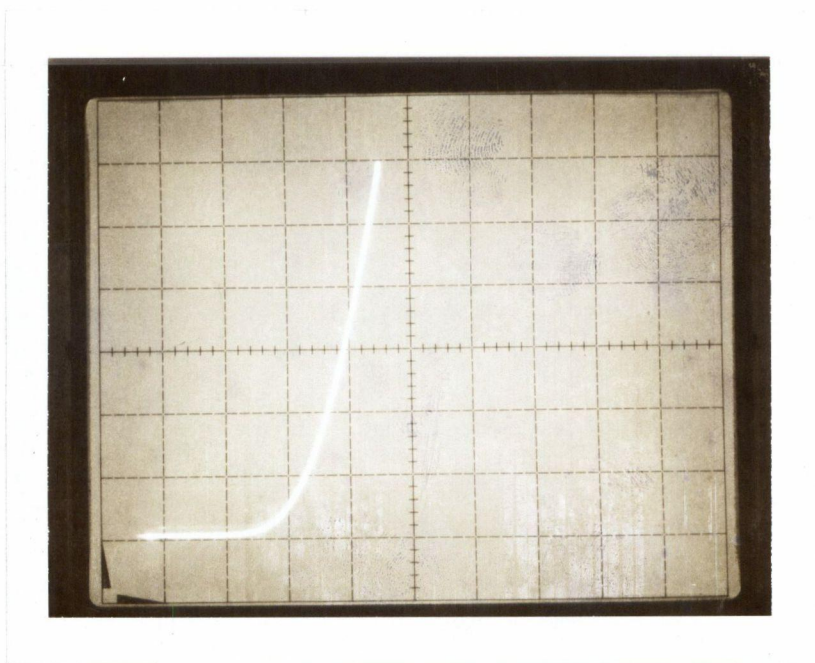
Figure 7.14 Double Dielectric MOSFET Saturated Test, Sample
MTAOS 3 (Vgs=Vds, Hor. 1 V/div., Vert. 0.2 mA/div.)
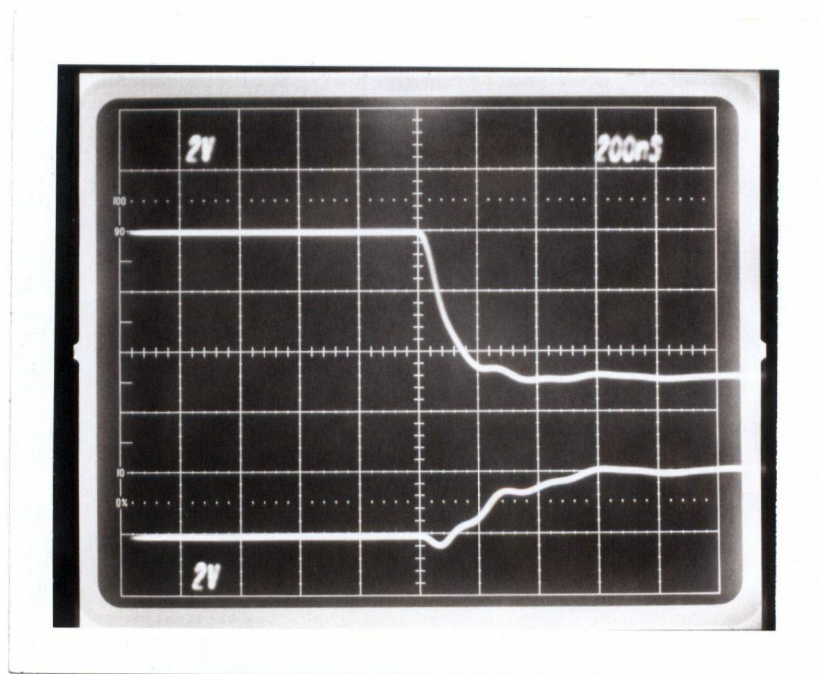
Figure 7.15 Double Dielectric MOSFET Pulse Test (Turn On),
Sample MTAOS 3 (top trace is Vgs input, lower is Vds output)
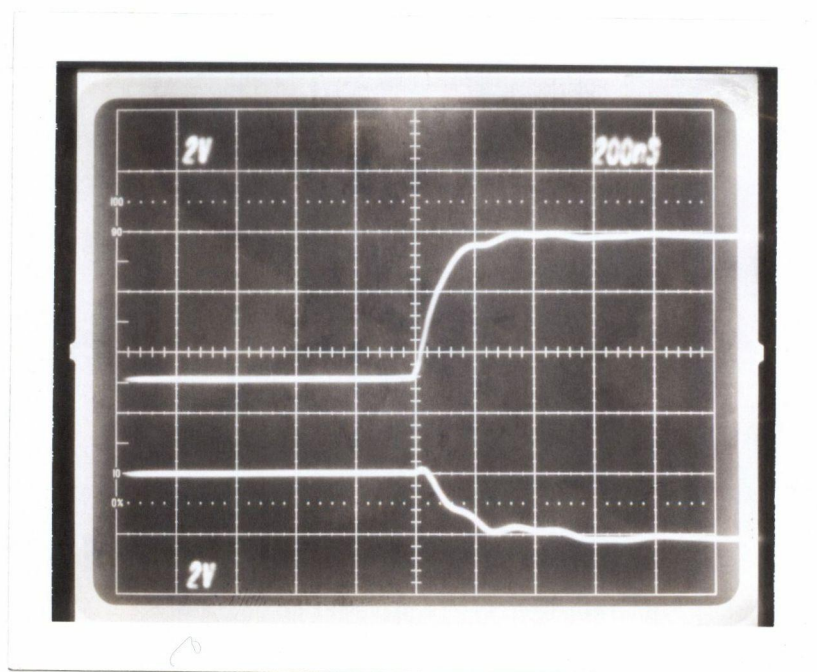
Figure 7.16 Double Dielectric MOSFET Pulse Test (Turn Off),
Sample MTAOS 3 (top trace is Vgs input, lower is Vds output)
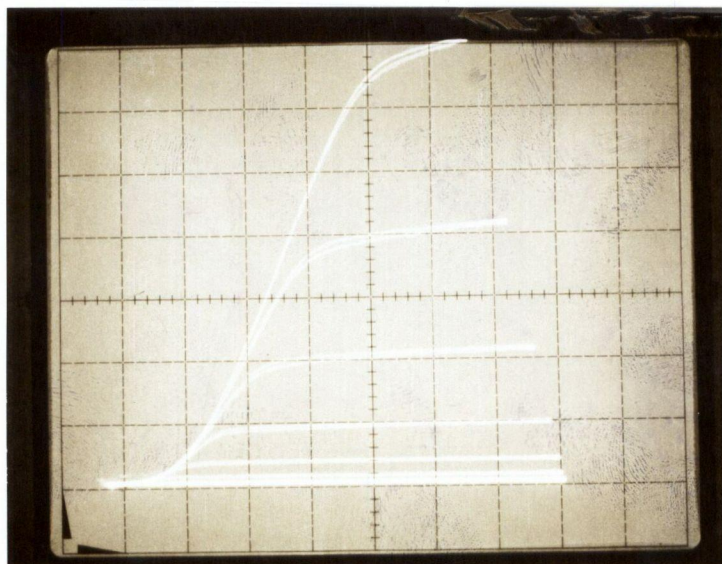
Figure 7.17 Double Dielectric MOSFET Output Curves, Sample
MTAOS4 (Vgs step 0.5 V, Hor. 1 V/div., Vert 0.1 mA/div.)
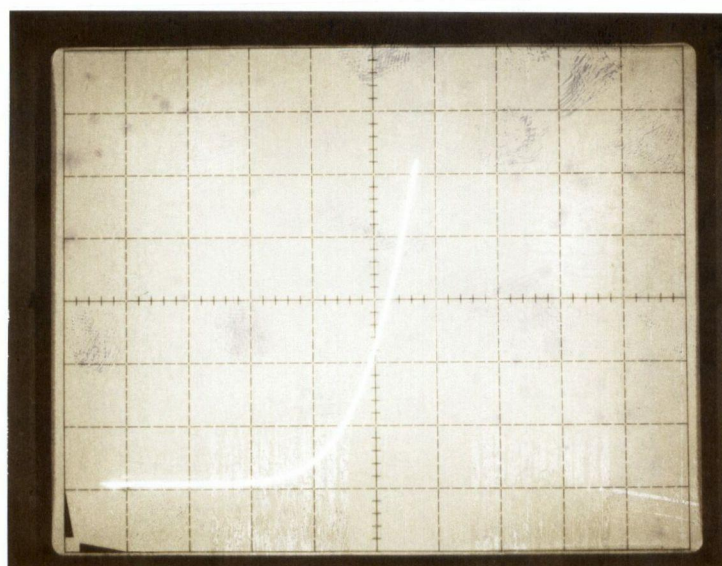
Figure 7.18 Double Dielectric MOSFET Saturated Test, Sample
MTAOS4 (Vgs=Vds, Hor. 1 V/div., Vert. 0.1 mA/div.)
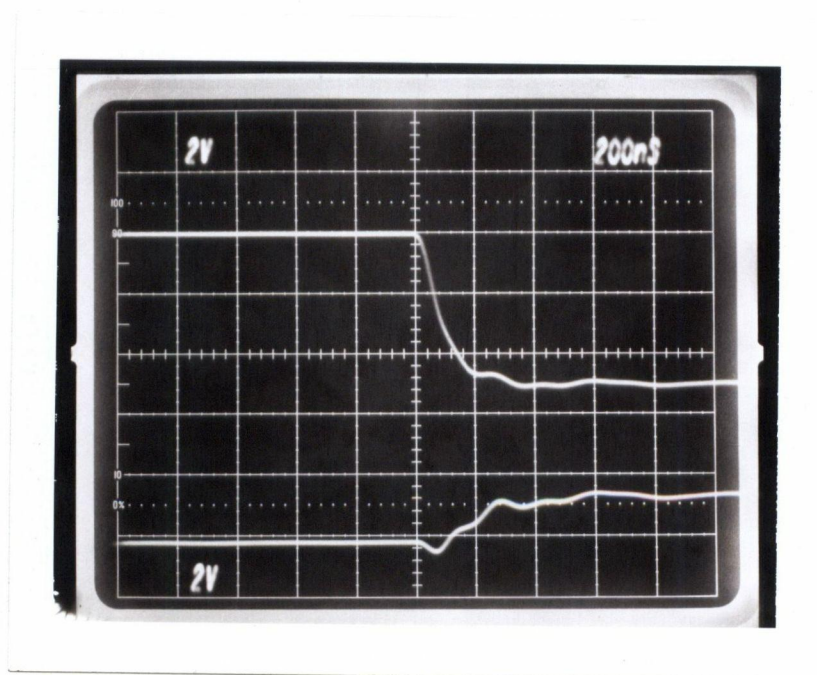
Figure 7.19 Double Dielectric MOSFET Pulse Test (Turn On),
Sample MTAOS4 (top trace is Vgs input, lower is Vds output)
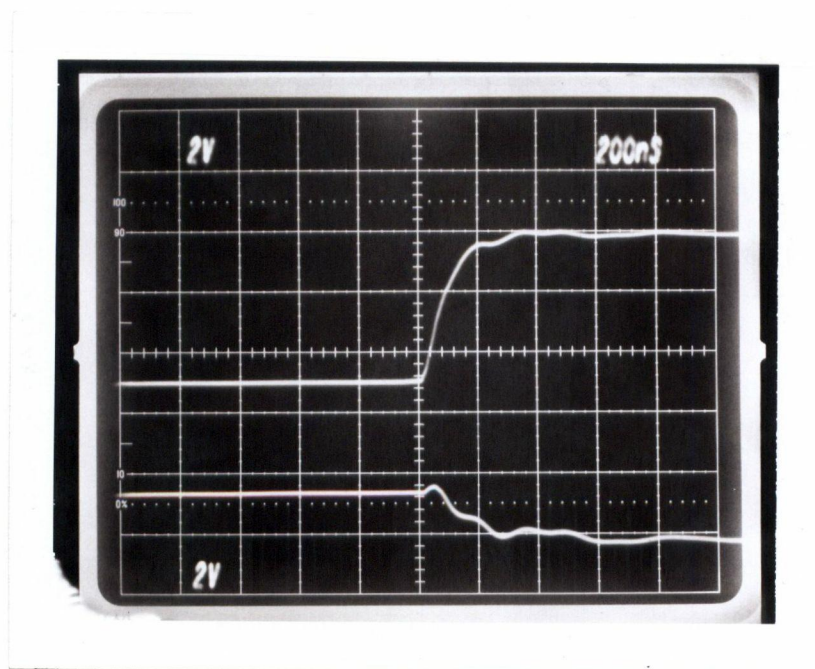
Figure 7.20 Double Dielectric MOSFET Pulse Test (Turn Off),
Sample MTAOS4 (top trace is Vgs input, lower is Vds output)
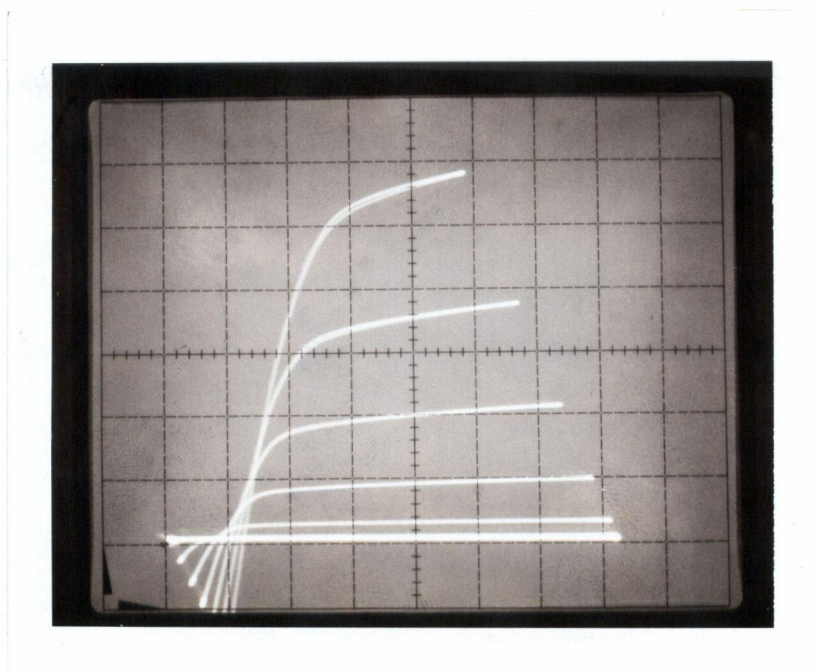
Figure 7.21 Leaky Gate in MOSFET, Anodic Ta$_2$O$_5$, Sample MTAOS4 (Vgs step 0.5 V, Hor. 1 V/div., Vert. 0.2 mA/div.)
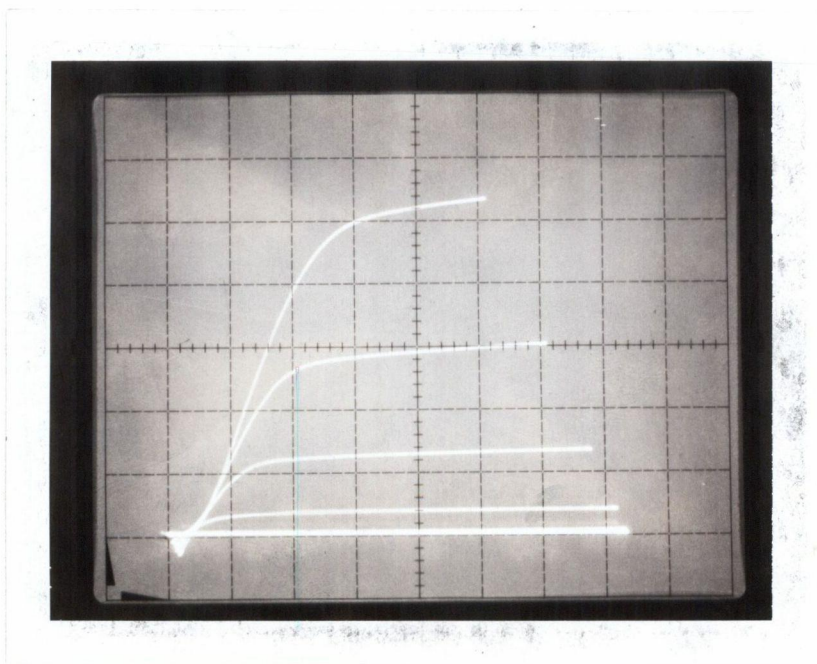
Figure 7.22 Leaky Gate in MOSFET, Thermal Ta$_2$O$_5$, Sample MTAOS3 (Vgs step 0.5 V, Hor. 1 V/div., Vert. 0.2 mA/div.)

{7.3} DOUBLE DIELECTRIC MOSFET EQUIVALENT CIRCUIT:

Based on the experimental characteristics of the MTAOS transistor, a Small Signal model can be made. The equivalent circuit is shown in Figure 7.23, and it is based on the single dielectric MOSFET model [Millman and Halkias, 1972], with the addition of a finite input conductance (Ggs) due to the increased gate leakage and an the input capacitance due to the double dielectric gate insulator with increased permittivity (Cgs). The capacitance Cgd appears as a result of the overlap between the drain and gate areas. Its effect is to modify the input and output admittances Yin and Yout due to Miller effect.

MTAOS FET
Small Signal Equivalent Circuit
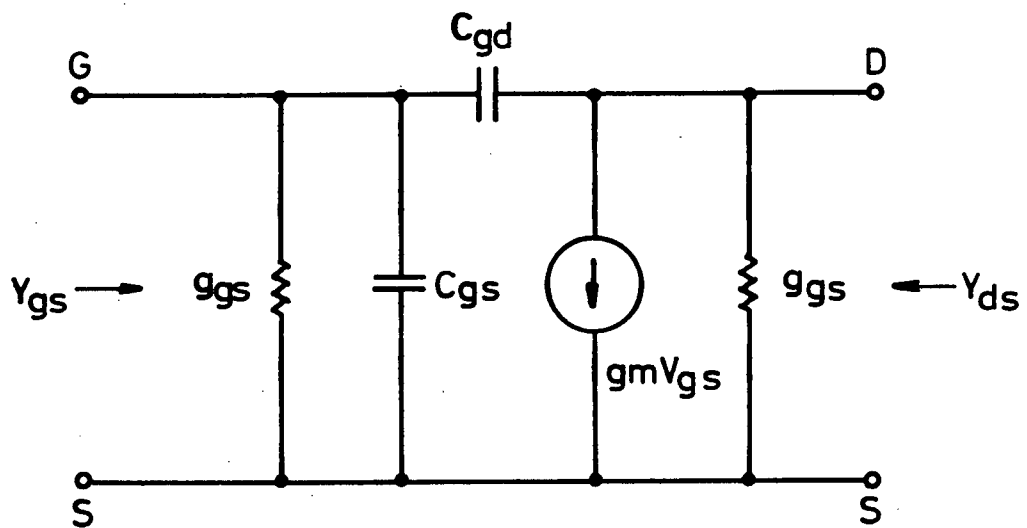
After Miller Transformation:

$$Y_{gs} = g_{gs} + j\omega\{C_{gs} + (1-A)C_{gd}\}$$

$$Y_{ds} = g_{ds} + j\omega\{(1-A)/A\}C_{gd}$$

Where A is the circuit gain

Figure 7.23 Double Dielectric MOSFET Equivalent Circuit.

CHAPTER 8

SUMMARY AND CONCLUSIONS

In this work, we have presented the theory, design and development of a MOSFET with a double dielectric gate insulator, utilizing the Ta_2O_5/SiO_2 insulator structure. The initial MOS capacitor work, paved the road for the successful development of MTAOS Field Effect Devices. We have demonstrated that this technology is feasible, reproducible, and reliable. It can be extended to Integrated Circuits of more complex nature, without excessive hardships, thus opening new avenues of research and development for an entirely new member of the MOS family. No attempts were made to reduce the size of our final devices, which for today's standards are quite large (channel length $\simeq 10\mu m$). This will be part of future work on this family of devices, aimed towards the VLSI and ULSI technologies.

The MOS capacitor performance was well within the range of reported work by previous authors, except perhaps the conduction characteristics for our devices. The double dielectric devices exhibited very small leakage (conduction) currents, thus rendering them useful in gate insulators for MOSFET's. Photoconduction phenomena was quite evident for these devices, and it is another area of possible research, still not quite explored nor understood. High capacitance densities (50000 pf/cm^2) were obtained in the single (Ta_2O_5) capacitors.

The Double Dielectric MOSFET devices presented good output and transfer characteristics, moderate transconductance and fast switching times. Gate leakage current was very low for the thermal tantalum pentoxide devices, and somewhat higher for the anodic version. The threshold voltage was 2-2.5 V. The devices were stable and the yield obtained was compatible with laboratory production levels.

From this work, the following can be concluded:

1. The tantalum pentoxide insulator is a feasible dielectric for use in MOS technology.

2. Both anodic and thermal tantalum oxides can be grown as thin films on silicon substrates. They are compatible with standard MOS processing and fabrication.

3. The properties of an insulating film can be derived from MOS capacitor C-V curves. The I-V plots provide additional information on the conduction mechanisms.

4. Single and Double dielectric MOS capacitors using the $Al-Ta_2O_5-Si$ and $Al-Ta_2O_5-SiO_2-Si$ structures are possible and practical.

5. Double Dielectric MOS Field Effect Transistors, using tantalum pentoxide over silicon dioxide are a developed, feasible and successful technology at the University of British Columbia.

6. The interfacial oxidation of silicon below tantalum pentoxide proved to be a successful technique in the processing of double dielectric MOS capacitors.

7. Both MOS capacitors and transistors can be improved by better processing and fabrication methods, in particular the patterning of tantalum and tantalum oxides.

8. That this author has verified once again that Thomas A. Edison was absolutely correct in stating that "everything takes 10% inspiration and 90% perspiration".

If future work is attempted, the following areas of development are recommended to be refined:

1. A better and more scientific study should be made on the formation of hillocks and pinholes on the deposited Ta metal on silicon substrates. In particular for RF sputtering, as this is quite a popular technique.

2. The problem of contamination of the tantalum pentoxide film should addressed. Alkali ions are known to cause havoc in silicon dioxide, the question is then: Do the alkali ions (i.e. sodium) or other ions affect the quality of the Ta_2O_5 insulator?

3. A compatible patterning of Ta metal and its oxides with silicon has to be studied and developed. A trend exists towards Reactive Ion Etching (RIE), using plasma etching equipment, which offers interesting solutions. [Seki et al., 1983].

4. Besides the standard RFS deposition method, others such

as Electron Beam and Reactive RF sputtering should be developed. In particular, one that deposits directly the tantalum pentoxide over the substrate, with minimum damage, should be close to ideal.

5. Little or no data exists on the Electron Affinity, Work Function differences and Barrier Height of tantalum pentoxide on silicon. Even worse is the situation in the double dielectric structure. Energy Band diagram data should be compiled, if a better understanding of this insulator is required.

6. Memory devices should be investigated. The double dielectric MOSFET, with very thin silicon dioxide, should exhibit enough hysteresis so that a memory cell can be built using a single transistor. Ideal for Dynamic Random Acess Memories (DRAM's), and considering the amount of interest on the 1 Mbit RAM, it should be worthwhile.

7. The interfacial oxidation of silicon below tantalum pentoxide should be further developed. This is an interesting technique that offers many solutions in the processing of the Double Dielectric structure.

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APPENDIX II

COMPUTER SOURCE PROGRAMS

{A2.1} FORTRAN IV PROGRAM FOR OBTAINING I-V CURVES:

The following is a listing of the source code written in FORTRAN IV, which is used to obtain the I-V data in the form of Current-Voltage plots, in either Linear or Schottky graphs. The main program and its assembler routines run under the OS/8 operating system in the PDP8/E. Some of the routines were provided by D. Smith, they are written in the OS/8 assembler code, octal addressing and RALF mnemonics. This source code and its callable subroutines runing under the operating system with the required hardware, produces a graph of the I-V data:

```
C         FILE LEAKY
C         MOSIV IN M STEPS (LESS THAN 150)
          REAL VOLT,CINC,TIME,SVOLT,TVOLT
          DIMENSION VOLT(160),CINC(160),TIME(160)
          DIMENSION SVOLT(160),TVOLT(160),SPANN(160),STROM(160)
          CALL PLOTS(.005,0)
          IFST=2048
          WRITE(4,1)
     1    FORMAT(1X,'THIS IS AN IV MEASUREMENT PROGRAM')
    81    WRITE(4,6)
     6    FORMAT(1H0,'NUMBER OF INCREMENTS:      ',$)
          READ(4,7)M
     7    FORMAT(F10.0)
          WRITE(4,5)
     5    FORMAT(1X,'MAXIMUM VOLTAGE [VOLTS]:     ',$)
          READ(4,9)VMAX
     9    FORMAT(F10.5)
          WRITE(4,11)
    11    FORMAT(1X,'KEITHLEY SCALE:     ',$)
          READ(4,12)SKEITH
    12    FORMAT(E7.0)
          WRITE(4,8)
     8    FORMAT(1X,'TYCO SCALE:     ',$)
          READ(4,2) TYCOSC
```

```
      2       FORMAT(F6.0)
              WRITE(4,4) TYCOSC
      4       FORMAT(1X,'TYCO SCALE:',F6.0,'V')
              WRITE(4,3)
      3       FORMAT(3X,'I',3X,'TIME',5X,'VOLT',5X,'SVOLT',8X,'TVOL
C             INITIALIZE ARRAY TO ZERO
              DO 66 I=1,M
              VOLT(I)=0
     66       CONTINUE
              OLVOLT=0
              CALL RESET
              DO 60 I=1,M
              CINC(I)=VMAX/M
              VOLT(I)=OLVOLT+CINC(I)
              OLVOLT=VOLT(I)
              CALL DAC16(VOLT(I))
              CALL TIMEX(TIME(I),SVOLT(I),IFST)
              CALL TYCO(TVOLT(I))
              TVOLT(I)=(TVOLT(I)*TYCOSC*SKEITH)/10000
              WRITE(4,10) I,TIME(I),VOLT(I),SVOLT(I),TVOLT(I)
     10       FORMAT(1X,I3,F9.4,F10.6,F10.6,E15.5)
     60       CONTINUE
C             SET DAC OUTPUT TO ZERO WHEN FINISHED
              VOLT(M+1)=0
              CALL DAC16(VOLT(M+1))
              DATA YES,NO /'Y','N'/
C             ASK IF GRAPH IS REQUIRED
     29       CONTINUE
              WRITE(4,30)
     30       FORMAT(1X,'PLOT GRAPH? Y/N:    ',$)
              READ(4,28)ANSW
     28       FORMAT(A1)
              IF(ANSW.EQ.NO) GO TO 42
C             ASK WHAT KIND OF PLOT
              WRITE(4,26)
     26       FORMAT(1X,'LINEAR PLOT? Y/N:    ',$)
              READ(4,24)SWAN
     24       FORMAT(A1)
              IF (SWAN.EQ.YES) GO TO 40
              WRITE(4,22)
     22       FORMAT(1X,'SCHOTTKY PLOT? Y/N:    ',$)
              READ(4,20)REPLY
     20       FORMAT(A1)
              IF (REPLY.EQ.YES) GO TO 34
     40       CONTINUE
C             LINEAR PLOT
     32       WRITE(4,56)
     56       FORMAT(1X,'PLOT AXES? Y/N:    ',$)
              READ(4,48) RESP
     48       FORMAT(A1)
              IF(RESP.EQ.NO) GO TO 52
              CALL PSCALE(SVOLT,6,M,1)
              CALL PSCALE(TVOLT,8,M,1)
              X0=SVOLT(M+1)
              XINC=SVOLT(M+2)
              Y0=TVOLT(M+1)
```

```
          YINC=TVOLT(M+2)
          CALL AXIS(0,0,'VOLTAGE [VOLTS]',-15,6,0,X0,XINC)
          CALL AXIS(0,0,'CURRENT [AMPS]',14,8,90,Y0,YINC)
          CALL SYMBOL(1.5,8.5,.175,'LINEAR IV PLOT',0,14)
   52     CONTINUE
          CALL LINE(SVOLT,TVOLT,M,1,0,0)
          CALL XYPLOT(0,0,3)
          GO TO 42
   34     CONTINUE
C         SCHOTTKY PLOT
C         CALCULATE SQRT VOLTAGE AND LOG CURRENT
          DO 70 I=1,M
          SPANN(I)=SQRT(ABS(SVOLT(I)))
          STROM(I)=-ALOG10(ABS(TVOLT(I)))
   70     CONTINUE
          WRITE(4,79)
   79     FORMAT(1X,'PLOT AXES? Y/N:     ',$)
          READ(4,58)REPON
   58     FORMAT(A1)
          IF(REPON.EQ.NO) GO TO 62
          CALL PSCALE(SPANN,6,M,1)
          CALL PSCALE(STROM,8,M,-1)
          XS0=SPANN(M+1)
          XSINC=SPANN(M+2)
          YS0=STROM(M+1)
          YSINC=STROM(M+2)
          CALL AXIS(0,0,'SQRT VOLTAGE [SQRT(VOLTS)]',-26,6,0,XS
          CALL AXIS(0,0,'-LOG10 CURRENT [LOG10(AMPS)]',28,8,90,
          CALL SYMBOL(1.50,8.5,.175,'SCHOTTKY IV PLOT',0,16)
   62     CONTINUE
          CALL LINE(SPANN,STROM,M,1,0,0)
          CALL XYPLOT(0,0,3)
   42     CONTINUE
          WRITE(4,71)
   71     FORMAT(1X,'CONTINUE GRAPH? Y/N:     ',$)
          READ(4,80)WORD
   80     FORMAT(A1)
          IF(WORD.EQ.NO) GO TO 81
          GO TO 29
          END
```

{A2.2} FORTRAN CALLABLE SUBROUTINES:

These are subroutines that interface to the Real Time Clock, operate the 16 bit Digital to Analog Converter, and acquire data from the Dana and Tyco Digital Voltmeters:

```
/              ******************************
/              *       SUBROUTINE SW(I,J)          *
/              *       SUBROUTINE RELAY(I)         *
/              *       SUBROUTINE DAC16(V)         *
/              ******************************
/
/
/THESE FORTRAN CALLABLE SUBROUTINES WILL READ
/THE CONSOLE SWITCH REGISTER OR OPEN A RELAY.
/CALLING SEQUENCE:
/         CALL SW(I,J)
/                   I=SWITCH REGISTER NUMBER (0-11)
/                   J=1 IF SWITCH IS SET, 0 OTHERWISE
/         CALL RELAY(I)
/                   I=RELAY NUMBER (0-3)
/         CALL DAC16(V)
/                   V=VOLTAGE WORD (0-65535)
/
/THE ARGUMENTS OF SW(I,J) AND RELAY(I) CAN BE REAL
/OR INTEGER.
/
          SECT      SW
/
          EXTERN    SW8
          EXTERN    RELAY8
          EXTERN    VV1
          EXTERN    DAC8
          EXTERN    A8
/
          BASE      0
          JSA       SETUP     /GET ARGUMENT AND RTN PTR'S
          TRAP4     SW8       /CALL 8 MODE ROUTINE
          STARTD
          SETX      #IR       /SET INDEX TO THIS ROUTINE
          FLDA%     0,2       /GET PTR TO ANSWER
          FSTA      3         /AND STORE IT
          SETX      VV1
          STARTF
          XTA       0
          FSTA%     3         /GIVE ANS TO CALLER
          FLDA      30        /RTN TO CALLER
          JAC
                             /
SETUP,    0;0                /RETURN GOES HERE
          STARTD
          SETX      #IR       /SET TO ROUTINE'S INDEX
          FLDA%     0,1       /GET PTR TO ARG
          FSTA      3         /AND STORE IT
          SETX      VV1
          STARTF
          FLDA%     3         /USER ARG TO FAC
          ATX       0         /PASS TO 8 MODE
          JA        SETUP
                             /
          ENTRY     RELAY     /OPEN A RELAY
RELAY,    JSA       SETUP     /GET ARG FROM CALLER
```

```
        TRAP4     RELAY8    /CALL 8 MODE ROUTINE
                            /ARG IS IN FPP XR3
        FLDA      30        /RTN TO CALLER
        JAC
/
/
        ENTRY     DAC16
DAC16,  JSA       SETUP     /GET ARG AND RTN PTR'S
        FLDA%     3         /GET THE VOLTAGE WORD
        FMUL      #64K      /AND SCALE TO THE DAC RANGE
        FDIV      #25       /DIVIDE BY THE GAIN OF
                            /THE DAC (ASSUMED TO BE 25)
        ALN       0         /MAKE IT AN INTEGER
        FSTA      A8        /PASS TO 8-MODE
        TRAP4     DAC8      /CALL 8-MODE ROUTINE
        FLDA      30        /GET RETURN ADDRESS
        JAC                 /RETURN TO CALLER
/
/
#IR,    0000                /THIS ROUTINE'S INDEX
        0001                /XR1
        0002                /XR2
#64K,   F 6553.5            /FULL SCALE FOR DAC
#25,    F 25.0              /GAIN OF THE DAC



        SECT8     DECOD
/
/       SUBROUTINE ENTRY NAME
        ENTRY     DEC8
        ENTRY     SW8
        ENTRY     RELAY8
/
/       LIST OF DATA ENTRY POINTS
        ENTRY     V8A
        ENTRY     RANG8
        ENTRY     SGN
        ENTRY     VV3
        ENTRY     VV2
        ENTRY     VV1
/
/
/
/       DECODE VOLTAGE WORDS TO DECIMAL
/       START WITH VOLTAGE WORD 3
DEC8,   0
        TAD       VV3       /GET VOLTAGE WORD 3
        AND       K17       /MASK BITS 8-11
        DCA       V8A       /AND STORE
        TAD       VV3       /GET THE WORD AGAIN
        RTR                 /ROTATE RIGHT 4 TIMES
        RTR
        AND       K17       /MASK BITS 8-11
        DCA       V8B       /AND STORE
```

```
            TAD       VV3       /GET THE WORD AGAIN
            RAL                 /ROTATE LEFT
            RTL                 /5 TIMES
            RTL
            AND       K17       /MASK BITS 8-11
            DCA       V8C       /AND STORE
/
/           UNPACK VOLTAGE WORD 2
            TAD       VV2       /GET VOLTAGE WORD 2
            AND       K17       /MASK BITS 8-11
            DCA       V8D       /AND STORE
            TAD       VV2       /GET THE WORD AGAIN
            RTR                 /ROTATE RIGHT 4 TIMES
            RTR
            AND       K17       /MASK BITS 8-11
            DCA       V8E       /AND STORE
/
/           UNPACK VOLATGE WORD 1
            TAD       VV1       /GET VOLTAGE WORD 1
            RTL                 /ROTATE LEFT 2 TIMES
            AND       K1        /MASK BIT 11
            DCA       V8F       /AND STORE
/
/           DETERMINE POLARITY
            TAD       VV1       /GET VOLTAGE WORD 1
            AND       K400      /MASK AC03
            SNA                 /IS IT ZERO?
            JMP       POS       /YES. SIGN IS POSITIVE
            TAD       K1        /NO. SET SIGN CODE=1
            DCA       SGN
            JMP       RANG      /GO TO RANGE TEST
POS,        CLA CLL             /SET SIGN CODE=0
            DCA       SGN
/
/           DETERMINE VOLTAGE RANGE
/           START BY TESTING FOR .1V RANGE
RANG,       TAD       VV2       /GET VOLTAGE WORD 2
            AND       K6000     /MASK AC00 AND AC01
            SZA                 /AC=0?
            JMP       R0        /NO. TRY NEXT RANGE
            DCA       RANG8     /YES. SET RANGE CODE=0
            JMP       OUT       /RETURN
/           TRY 1V RANGE
R0,         CLA CLL
            TAD       VV2       /GET VOLTAGE WORD 2
            AND       K5400     /MASK AC00,AC02, AND AC03
            SZA                 /AC=0?
            JMP       R1        /NO. TRY NEXT RANGE
            TAD       K1        /YES. SET RANGE CODE=1
            DCA       RANG8
            JMP       OUT       /RETURN
/           TRY 10V RANGE
R1,         CLA CLL
            TAD       VV2       /GET VOLTAGE WORD 2
            AND       K5000     /MASK AC00 AND AC02
            SZA                 /AC=0?
```

```
            JMP     R2          /NO. TRY NEXT RANGE
            TAD     K2          /YES. SET RANGE CODE=2
            DCA     RANG8
            JMP     OUT         /RETURN
/           TRY 100V RANGE
R2,         CLA CLL
            TAD     VV2         /GET VOLTAGE WORD 2
            AND     K4400       /MASK AC00 AND AC03
            SZA                 /AC=0?
            JMP     R3          /NO. TRY NEXT RANGE
            TAD     K3          /YES. SET RANGE CODE=3
            DCA     RANG8
            JMP     OUT         /RETURN
/           MUST BE 1000V RANGE
R3,         CLA CLL
            TAD     K4          /SET RANGE CODE=4
            DCA     RANG8
OUT,        CDF CIF 0           /RETURN TO CALLING
            JMP%    DEC8        /ROUTINE
/
/
/
/           READ THE SWITCH REGISTER AND RETURN WITH
/           XR3=1 IF BIT IS SET
SW8,        0
            LAS                 /READ THE REGISTER WORD
            DCA     RANG8       /AND STORE IT
            TAD     VV1         /GET BIT POINTER
            CMA CLL CML         /SET UP FOR MASKING
            DCA     VV1
            RAR                 /ROTATE LINK UNTIL
            ISZ     VV1         /XR3=0
            JMP     .-2
            AND     RANG8       /MASK SWITCH WORD
            SZA CLA             /IF BIT IS SET,SET XR3=1
            ISZ     VV1
            CIF CDF 0           /RTN TO CALLER
            JMP%    SW8
/
/
/
/           ENERGIZE THE SPECIFIED RELAY
RELAY8,     0
            CLA CLL
            TAD     VV1
            AND     K3          /MASK IT TO MAKE SURE
            6354                /ENERGIZE THE RELAY
            CLA CLL
            CIF CDF 0           /RTN TO CALLER
            JMP%    RELAY8
/
K1,         1
K2,         2
K3,         3
K4,         4
K17,        17
```

```
K400,    400
K4400,   4400
K5000,   5000
K5400,   5400
K6000,   6000
V8A,     0                    /LIST OF DECODED
V8B,     0                    /VOLTAGE WORDS
V8C,     0
V8D,     0
V8E,     0
V8F,     0
RANG8,   0                    /RANGE CODE WORD
SGN,     0                    /SIGN CODE WORD
VV3,     0                    /CODED VOLTAGE WORDS
VV2,     0                    /FROM CALLING ROUTINE
VV1,     0


                 SECT8    PHO8
/
/        LIST OF SUBROUTINE NAMES
         ENTRY    PHOT8
         ENTRY    GAN8
         ENTRY    CLOK8
         ENTRY    RCLK8
         ENTRY    STEP
/
/        LIST OF DATA ENTRY POINTS
         ENTRY    T8L
         ENTRY    V2
         ENTRY    V3
         ENTRY    ERR8
         ENTRY    FAST8
         ENTRY    G8L
/
/
/
/        READ PHOTODETECTOR AND STORE DATA WORD IN ERR8
PHOT8,   0
         CLA      CLL
         TAD      CHAN        /GET CHANNEL SELECT
         6323                 /OUPUT TO DEVICE 32
PA,      6321                 /CONVERSION DONE?
         JMP      PA          /NO. TRY AGAIN
         6324                 /LOAD THE DATA WORD
         CMA                  /COMPLEMENT IT
         DCA      ERR8        /AND STORE IT
         CDF CIF 0            /RETURN TO CALLING
         JMP%     PHOT8       /ROUTINE
/
/
/
/        GET THE GAIN WORD, ADD CHANNEL NUMBER AND
/        STORE IN CHAN
```

```
/             GAIN WORD IS IN THE RANGE 0-7
/             ANALOG INPUT ON CHANNEL #17
/
GAN8,     0
          CLA     CLL
          TAD     G8L       /GET THE GAIN WORD (0-7)
          RAL               /SHIFT LEFT TO BITS 6-8
          RTL
          TAD     K7        /ADD THE ANALOG CHAN #
          DCA     CHAN      /AND STORE IT
          TAD     CHAN      /SELECT THE NEW GAIN
          6323
          CDF CIF 0         /RETURN TO CALLING
          JMP%    GAN8      /ROUTINE
/
/
/
/             READ CLOCK AND DANA
CLOK8,    0
/             INITIALIZE SYSTEM DIRECT COMMAND
          CLA     CLL
          TAD     FAST8     /GET SUPERFAST CODE
          TAD     K2000     /ADD AC01(1)
          TAD     CHAN      /ADD THE CHANNEL SELECT
          6323              /OUTPUT TO DEVICE 32
/
/             TEST FOR SYSTEM RDY--GROUND TRUE,AC06
FLG,      CLA     CLL
          6311              /LOAD FROM DEVICE 31
          AND     K40       /MASK AC06
          SZA               /IS IT ZERO?
          JMP     FLG       /NO. TEST AGAIN
/
/             GET TIME, THEN START CONVERSION--SET SYS DIR
/             TO 0, WAIT, THEN BRING HIGH AGAIN.
/             READ CLOCK WHILE WAITING
          TAD     FAST8     /GET SUPERFAST CODE
          TAD     CHAN      /ADD CHANNEL SELECT CODE
TEST,     6371              /CLOCK READY?
          JMP     TEST      /NO. TRY AGAIN
          6323              /YES. OUTPUT DATA WORD
          6361              /LOAD LOW ORDER CLOCK WORD
          DCA     T8L       /AND STORE IT
          6362              /LOAD HIGH ORDER CLOCK WORD
          DCA     T8H       /AND STORE IT
          NOP               /WAIT BEFORE BRINGING SYSTEM
          NOP               /DIRECT COMMAND HIGH AGAIN
          NOP
          NOP
          TAD     FAST8     /LOAD SUPERFAST WORD
          TAD     CHAN      /ADD CHANNEL SELECT WORD
          TAD     K2000     /ADD AC01(1)
          6323              /OUTPUT TO DEVICE 32
/
/             WHILE WAITING FOR END OF CONVERSION, STRIP OFF
/             SIGN BIT FROM THE 12-BIT TIME WORDS
```

```
            CLA       CLL
            TAD       T8L       /GET LOW ORDER TIME WORD
            RAR                 /ROTATE 1 BIT TO THE RIGHT
            DCA       T8L       /AND STORE AC
            RAL                 /GET BIT 11
            DCA       ST8L      /AND STORE IT
            TAD       T8H       /REPEAT WITH HIGH ORDER WORD
            RAR
            DCA       T8H
            RAL
            DCA       ST8H
/
/           CHECK FOR END OF CONVERSION
/           DATA READY--GROUND TRUE,AC04
DFLG,       CLA       CLL
            6311                /LOAD FROM DEVICE 31
            AND       K200      /MASK AC04
            SZA                 /IS IT ZERO?
            JMP       DFLG      /NO. TRY AGAIN
/
/           READ IN BCD VOLTAGE WORD AND STORE IN
/           V1,V2,V3
            6314                /LOAD VOLTAGE WORD 3
            DCA       V3        /AND STORE IT
            6312                /LOAD VOLTAGE WORD 2
            DCA       V2        /AND STORE IT
            6311                /LOAD VOLTAGE WORD 1
            DCA       V1        /AND STORE IT
            CDF CIF 0           /RETURN TO CALLING
            JMP%      CLOK8     /ROUTINE
/
/
/
/           RESET THE 100 MICROSECOND CLOCK
RCLK8,      0
            6374                /RESET PULSE
            CDF CIF 0
            JMP%      RCLK8
/
/
/
/           STEP THE SPECIFIED STEPPING MOTOR
/           AND WAIT FOR THE SPECIFIED TIME
/           BEFORE RETURNING
STEP,       0
            CLA       CLL
            TAD       M2        /GET MOTOR SELECT CODE
            6332                /SELECT THE MOTOR
            6334                /STEP THE MOTOR
            CLA       CLL
            TAD       SLO       /GET THE WAIT TIME WORD
            CIA                 /GET ITS NEGATIVE
BACK,       IAC                 /INCREMENT ACCUMULATOR
            SZA                 /AC IS ZERO?
            JMP       BACK      /NO. JUMP TO BACK
            CDF CIF 0           /YES. RETURN TO CALLING
```

```
            JMP%       STEP       /ROUTINE
/
/
/
/          TABLE OF CONSTANTS AND DATA WORDS
K40,       40
K200,      200
K2000,     2000
CHAN,      7                      /CHANNEL SELECT CODE
K7,        7
ERR8,      0                      /PHOTODETECTOR ERROR
T8L,       0                      /LOW ORDER CLOCK WORD
ST8L,      0
T8H,       0                      /HIGH ORDER CLOCK WORD
ST8H,      0
V1,        0                      /DANA VOLTAGE WORDS
V2,        0
V3,        0
FAST8,     0                      /SUPERFAST CODE WORD
G8L,       0                      /GAIN SELECT WORD
SLO,       0                      /DELAY WORD FOR STEP
M2,        0                      /MOTOR SELECT WORD




            SECT8      REA8
/
/          SUBROUTINE ENTRY NAME
            ENTRY      READ8
            ENTRY      DAC8
/
/          LIST OF DATA ENTRY POINTS
            ENTRY      A8
            ENTRY      D8
/
/
/          SUBROUTINE TO READ AND DECODE SHAFT
/          ENCODERS
READ8,     0
            CLA CLL
            TAD        ISC8       /GET ENCODER SELECT WORD
            6332                  /AND OUTPUT IT
            NOP                   /WAIT FOR MUX TO
            NOP                   /SETTLE
            NOP
            NOP
            NOP
            NOP
            NOP
            CLA CLL
            6302                  /GET HIGH ORDER ANGLE
            DCA        ANGH       /AND STORE IT
            6304                  /GET LOW ORDER ANGLE
            DCA        ANGL       /AND STORE IT
            TAD        ANGL       /GET LOW ORDER WORD
```

```
        AND       K17        /MASK BITS 8-11
        DCA       E8         /AND STORE DECODED BCD
        TAD       ANGL       /GET LOW ORDER WORD AGAIN
        RTR
        RTR                  /ROTATE RIGHT 2 TIMES
        AND       K17        /MASK BITS 8-11
        DCA       D8         /AND STORE DECODED BCD
        TAD       ANGL       /GET LOW ORDER AGAIN
        RTL
        RTL                  /ROTATE LEFT 5 TIMES
        RAL
        AND       K17        /MASK BITS 8-11
        DCA       C8         /AND STORE DECODED BCD
        TAD       ANGH       /GET HIGH ORDER WORD
        AND       K17        /MASK BITS 8-11
        DCA       B8         /AND STORE DECODED BCD
        TAD       ANGH       /GET HIGH ORDER AGAIN
        RTR
        RTR                  /ROTATE RIGHT 2 TIMES
        AND       K17        /MASK BITS 8-11
        DCA       A8         /AND STORE DECODE BCD
        CDF CIF   0          /RETURN TO CALLING
        JMP%      READ8      /ROUTINE
/
/
/
/         SUBROUTINE TO OUTPUT A VOLTAGE WORD TO THE
/         16-BIT D/A CONVERTER
DAC8,     0
        CLA       CLL
        TAD       B8         /GET MOST SIG WORD
        AND       K17        /MASK LOW 4 BITS
        RAR
        RTR
        RTR                  /ROTATE INTO HIGH 4 BITS
        DCA       ANGH       /AND SAVE IT
        TAD       C8         /GET LEAST SIG WORD
        RTR
        RTR                  /ROTATE RIGHT 4 BITS
        AND       K377                /MASK 8 LOW ORDER BITS
        TAD       ANGH       /GET HIGH BITS
        CMA                  /COMPLEMENT
        6173                 /AND OUTPUT TO THE DAC
        TAD       C8         /GET LEAST SIG WORD AGAIN
        AND       K17        /MASK LOW ORDER 4 BITS
        RAR
        RTR
        RTR                  /ROTATE INTO HIGH 4 BITS
        CMA                  /COMPLEMENT
        6423                 /AND OUTPUT TO THE DAC
        CLA       CLL
        CDF CIF   0          /RETURN TO CALLING
        JMP%      DAC8       /ROUTINE
/
/
/
/
```

```
K17,      17
K377,     377
ANGH,     0                    /HIGH ORDER ANGLE WORD
ANGL,     0                    /LOW ORDER ANGLE WORD
A8,       0                    /LIST OF DECODED ANGLE
B8,       0                    /WORDS IN BCD
C8,       0
D8,       0
E8,       0
ISC8,     0                    /ENCODER SELECT CODE



/         FILE:    TYCO
/
/         *******************************************
/         *                                         *
/         *         SUBROUTINE   TYCO ( VOLT )       *
/         *                                         *
/         *     READ THE VOLTAGE FROM THE TYCO       *
/         *     VOLTMETER AND RETURN THE VOLTAGE     *
/         *     TO THE CALLING ROUTINE.              *
/         *                                         *
/         *     NOTE: THE VOLTAGE IS NOT SCALED      *
/         *           TO THE VOLTAGE RANGE OF        *
/         *           THE VOLTMETER. SCALING         *
/         *           MUST BE DONE BY THE CALLING    *
/         *           ROUTINE. ALSO, THE VOLTAGE     *
/         *           WORD IS ALWAYS A POSITIVE      *
/         *           QUANTITY.                      *
/         *                                         *
/         *******************************************
/
/
/         CALLING SEQUENCE:
/
/             CALL TYCO(VOLT)
/
/         WHERE:    VOLT = VOLTAGE READ FROM THE
/                          TYCO VOLTMETER.
/
/
/
/         SECT8    DVM88
          ENTRY    TYCO
/
/
/
/         READ THE VOLTAGE FROM THE TYCO DVM,
/         DECODE THE VOLTAGE, AND RETURN TO THE
/         RALF CALLING ROUTINE.
/
DVM8,     0                    /PDP8 MODE ROUTINE ENTRY
FLAG,     CLA      CLL
          6324                 /GET THE FLAG WORD
```

```
        AND     K2000   /MASK THE FLAG BIT
        SZA             /IF DVM READY, CONTINUE
        JMP     FLAG    /ELSE, CHECK FLAG AGAIN
        6301            /GET THE LOW ORDER VOLTAGE
                        /WORD
        DCA     DVML    /AND SAVE IT
        6311            /GET THE HIGH ORDER VOLTAGE
                        /WORD
        AND     K37     /MASK THE LOW ORDER BITS
        DCA     DVMH    /AND SAVE THE WORD
        TAD     DVMH    /GET THE WORD
        AND     K17     /MASK THE PROPER BITS
        DCA     VH2     /AND SAVE THEM
        TAD     DVMH    /GET THE WORD AGAIN
        RTR
        RTR             /ROTATE RIGHT 4 TIMES
        AND     K17     /MASK THE FIRST BIT
        DCA     VH1     /AND SAVE IT
/
        TAD     DVML    /GET THE LOW ORDER WORD AGAIN
        AND     K17     /MASK THE FIRST BCD DIGIT
        DCA     VL3     /AND SAVE IT
/
        TAD     DVML    /GET THE FULL WORD AGAIN
        RTR
        RTR             /ROTATE 4 TIMES TO THE RIGHT
        AND     K17     /MASK NEXT BCD DIGIT
        DCA     VL2     /AND SAVE IT
/
        TAD     DVML    /GET THE FULL WORD AGAIN
        RAL
        RTL
        RTL             /ROTATE 5 TIMES TO THE LEFT
        AND     K17     /MASK FINAL BCD DIGIT
        DCA     VL1     /AND SAVE IT
/
        CDF CIF 0       /RETURN TO RALF
        JMP%    DVM8    /ROUTINE
/
/
/
K17,    17
K37,    37
K2000,  2000
/
/
DVML,   0000            /LOW ORDER VOLTAGE WORD
DVMH,   0000            /HIGH ORDER VOLTAGE WORD
VH1,    0000            /DECODED VOLTAGE WORDS
VH2,    0000
VL1,    0000
VL2,    0000
VL3,    0000
/
/
/
```

```
/
#BASE,    F 0.0                /BASE PAGE REG
#XR,      F 0.0                /INDEX REG'S 0-2
#VOLT,    F 0.0                /POINTER TO ARG
#TEMP,    F 0.0                /TEMPORARY STORAGE
#TEN1,    F 10.0
/
          BASE    0            /USE CALLERS BASE PAGE FOR NOW
TYCO,     STARTD               /START OF RALF ROUTINE
          FLDA    30           /GET RETURN ADDRESS
          FSTA    #GOBAK       /AND SAVE IT
          FLDA    0            /GET POINTER TO ARG
          SETX    #XR          /SET INDEX REG TO THIS PAGE
          SETB    #BASE        /SAME FOR BASE REG
          BASE    #BASE
          LDX     1,1          /PUT 1 INTO INDEX REG 1
          FSTA    #BASE        /SAVE POINTER
          FLDA%   #BASE,1
          FSTA    #VOLT        /AND SAVE IT
/
/
          STARTF               /START FLOATING POINT
          TRAP4   DVM8         /CALL THE PDP8 MODE ROUTINE
          SETX    VH1          /SET INDEX REG TO PDP8 MODE AREA
          XTA     0            /GET MOST SIG DIGIT
          FMUL    #TEN1        /MULTIPLY BY 10
          FSTA    #TEMP        /AND SAVE THE RESULT
          XTA     1            /GET NEXT DIGIT
          FADD    #TEMP        /ADD TO TEMP
          FMUL    #TEN1        /MULTIPLY BY 10
          FSTA    #TEMP        /AND SAVE THE RESULT
          XTA     2            /GET NEXT DIGIT
          FADD    #TEMP        /ADD TO TEMP
          FMUL    #TEN1        /MULTIPLY BY 10
          FSTA    #TEMP        /AND SAVE THE RESULT
          XTA     3            /GET NEXT DIGIT
          FADD    #TEMP        /ADD TO TEMP
          FMUL    #TEN1        /MULTIPLY BY 10
          FSTA    #TEMP        /AND SAVE THE RESULT
          XTA     4            /GET LEAST SIG DIGIT
          FADD    #TEMP        /ADD TO TEMP
          FSTA%   #VOLT        /PASS TO THE CALLING ROUTINE
#GOBAK,   JA      .            /RETURN TO THE CALLING
                               /ROUTINE
```

{A2.3} FORTRAN IV PROGRAM FOR OBTAINING EQUIVALENT
PERMITTIVITY CURVES:

This source code calculates the equivalent permittivity
of a double insulator stucture. Given the relative
dielectric constant of the inner and outer dielectrics and

their ratio of thicknesses, it produces a plot of the
equivalent permittivity as a function of the insulator
thickness ratio. The number of increments has to be
supplied.

```
C          FILE PERMIQ
C          THIS PROGRAM CALCULATES AND PLOTS THE EQUIVALENT PERM
C          OF A DOUBLE INSULATOR STRUCTURE, WITH T/S AS A PARAME
           REAL A,B,X,Y
           DIMENSION X(200),Y(200),TINC(200)
           CALL PLOTS(0.005,0)
           WRITE(4,1)
     1     FORMAT(1X,'NUMBER OF INCREMENTS:     ',$)
           READ(4,2)M
     2     FORMAT(F10.0)
           WRITE(4,3)
     3     FORMAT(1X,'MAX. THICKNESS RATIO OF INSULATOR II TO I:
           READ(4,4)R
     4     FORMAT(F10.0)
    14     CONTINUE
           WRITE(4,5)
     5     FORMAT(1X,'PERMITTIVITY OF INSULATOR I:     ',$)
           READ(4,6)B
     6     FORMAT(F10.0)
           WRITE(4,7)
     7     FORMAT(1X,'PERMITTIVITY OF INSULATOR II:     ',$)
           READ(4,8)A
     8     FORMAT(F10.0)
C          INITIALIZE ARRAY TO ZERO
           DO 9 I=1,M
           X(I)=0
           Y(I)=0
           TINC(I)=0
     9     CONTINUE
           OLDT=0
           DO 10 I=1,M
           TINC(I)=R/M
           X(I)=OLDT+TINC(I)
           OLDT=X(I)
           Y(I)=B*((1+X(I))/(1+X(I)*(B/A)))
    10     CONTINUE
C          ASK IF GRAPH IS REQUIRED
           DATA YES,NO /'Y','N'/
           WRITE(4,11)
    11     FORMAT(1X,'PLOT AXES? Y/N:     ',$)
           READ(4,12)RESP
    12     FORMAT(A1)
```

```
        IF (RESP.EQ.NO) GO TO 13
        CALL PSCALE(X,6,M,1)
        CALL PSCALE(Y,8,M,1)
        X0=X(M+1)
        XINC=X(M+2)
        Y0=Y(M+1)
        YINC=Y(M+2)
        CALL AXIS(0,0,'RATIO OF INSULATOR THICKNESSES',-30,6,
        CALL AXIS(0,0,'EQUIVALENT PERMITTIVITY', 23,8,90,Y0,Y
13      CONTINUE
        CALL LINE(X,Y,M,1,0,0)
        CALL XYPLOT(0,0,3)
        GO TO 14
        END
```

APPENDIX III

LABORATORY PROCESSING DETAILS

Some further details of the solid state laboratory processes are now given in greater detail. These have been followed through in the fabrication of MOS capacitors and devices. In some cases, they are modified to suit compatible requirements of the films and substrates. The reagent concentrations of the various chemicals are as follows: H_2O_2, 30%; NH_4OH, 28-30%; HF, 48%; HCl, 37-38%; H_2SO_4, 95-96%.

{A3.1} THE RCA SSEE100 CLEANING PROCEDURE FOR SILICON SUBSTRATES:

This is a standard cleaning process followed in the Solid State Laboratory, Departement of Electrical Engineering at UBC [Kern and Puotinen, 1970]. The peroxide-acid cleaning process is as follows:

1. Prepare a solution in a 5:1:1 ratio of hot (60 C) de-ionized water : hydrogen peroxide (H_2O_2) : ammonium hydroxide (NH_4OH). Typical amounts are 300 ml:60 ml:60 ml, that fits very well in a 500 ml beaker.

2. Immerse the wafers/slices in above solution for 10 min.

3. Rinse the wafers/slices in de-ionized water for 2 min. in first water cascade, then for 8 min. in the second water cascade.

4.   Prepare a 10% HF solution in Nalgene beaker. Typical amounts are 450 ml H_2O and 50 ml HF.

5.   Immerse the wafers/slices in solution 4) for 30 secs.

6.   Rinse the wafers/slices in d.i. water per 3) above.

7.   Prepare a solution in a 5:1:1 ratio of hot (60 C) d.i. water : hydrochloric acid (HCl) : hydrogen peroxide (H_2O_2). Typical amounts are 300 ml:60 ml:60 ml.

8.   Immerse the wafers/slices in solution 7) for 10 min.

9.   Rinse the wafers/slices in d.i. water per 3) above.

10. Immerse wafers/slices (stirring) in beaker with 400 ml hot (60 C) isopropyl alcohol.

{A3.2} PHOTOLITHOGRAPHY:

Negative (Waycoat HR200) and positive (Waycoat HPR204) photoresists are used in different processing steps. Exposure to UV light is normally part of the mask alignment process. Development is usually done automatically for negative photoresist and manually for the positive ones.

{A3.2.1} Negative Photoresist:

a) Place wafer/slices in drying oven for 30 min. at 200 C. Let samples cool in clean tray before applying photoresist.

b) Spin wafers/slices in spinner, once, at 5000 rpm for 15 secs. without photoresist.

c) Carefully apply photoresist with eyedropper, repeat 1b) above.

d) Prebake all wafers in oven for 15 min., at 60 C.

e) Place wafer/slices one at a time in mask aligner, expose for 8 secs.

f) Develop in automatic developer.

g) Postbake in oven for 15 min. at 135 C. Let samples cool.

{A3.2.2} Positive Photoresist:

a) Place wafers in drying oven for 2 hrs. at 300 C. Let samples cool in clean tray before applying photoresist.

b) Spin wafers/slices in spinner, once, at 5000 rpm for 20 sec. without photoresist.

c) Carefully apply photoresist with eyedropper, repeat 2b) above.

d) Prebake all wafers in oven for 30 min. at 105 C.

e) Place wafer/slices one at a time in mask aligner, expose for 12 secs.

f) Develop in 1:3 solution of Waycoat Positive LSI Developer and de-ionized water for 60 secs.

g) Postbake in oven for 30 min. at 125 C. Let samples cool.

{A3.2.3} Etching:

{A3.2.3.1} Silicon Dioxide:

a) Dip all wafer/slices in d. i. water before HF etching, this will assure that no gas bubbles are formed.

b) Pour 450 ml of buffered HF solution in Nalgene beaker.

c) Slowly immerse all wafer/samples in solution. Etching rate is approximately 850 A/min.

d) Rinse all samples for 2+8 min. in de-ionized water.

e) Inspect under microscope, etched areas should be dull gray and also in water, they are hydrophobic.

f) Etch again if required. Rinse thoroughly.

g) Place all samples in boiling isopropyl alcohol. Dry over beaker in alcohol vapours. If required use N_2 jet.

{A3.2.3.2} Aluminium:

a) Prepare a solution of 1:1 of phosphoric acid (H_3PO_4) in de-ionized water, carefully stirr. Heat to 60 C and maintain temperature, an immersion thermometer is recommended.

b) Carefully place a test wafer/slice in solution. Slow movements are required as solution is quite viscous. Etching rate varies and some experimetation is advised. Thermally evaporated Al etches very slowly (500 nm in 10-15 min.), E-Beam deposited Al is fast (500 nm 2-3 min., or less). Gas bubbles form on the surface when etching takes place. If test sample is succesful, remaining ones can be treated.

c) Rinse all samples for 2+8 min. in de-ionized water.

d) Inspect under microscope, check for under/overetching, resolution, weak spots etc.

e) Etch again if required. Do not overetch.

f) Place all samples in boiling isopropyl alcohol. Dry over beaker in alcohol vapours. If required use N_2 jet.

{A3.2.4} Stripping the Photoresist:

{A3.2.4.1} Negative:

Two possibilities exist, one that is compatible with Al metal and that is incompatible, i.e. it will remove it by etching.

These are:

{A3.2.4.1.1} Microstrip process: Al compatible.

a) Place wafer/samples in hot (60-70C) Microstrip for 5 min.

b) Immerse wafer/samples in hot xylene I (60-70C) for 5 min.

c) Place samples in hot xylene II (60-70C) for 5 min.

d) Immerse wafers in hot isopropyl alcohol (60-70C) for 5 min.

e) Dry blow in nitrogen jet.

{A3.2.4.1.2} Chromic Acid process: incompatible with Al.

a) Pour carefully 400 ml of sulfuric acid (H_2SO_4) in beaker, add 3 spoonfulls of chromic trioxide (CrO_3) and heat up to 60C, stirr thoroughly. This mixture is deadly and it should be handled with great care and respect.

b) Prepare beaker with fresh de-ionized water.

c) Slowly immerse the wafer/samples in the solution for 2 min. Alternate a total of three times between the solution and d. i. water.

d) Give a final rinse in de-ionized water for 2+8 min.

e) Place all samples in boiling isopropyl alcohol. Dry over beaker in alcohol vapours. If required use N_2 jet.

{A3.2.4.2} Positive:

a) Place wafer/samples in acetone for 60 min.

b) Rinse all samples in fresh acetone.

c) Dry in Nitrogen jet.

{A3.3} SILICON OXIDATION-FIELD OXIDE:

The thick field oxide (typically 600 nm) is grown from the substrate by "wet" oxidation in a furnace at 1100 ± 5C. The gas flows are adjusted as follows:

1. Oxygen: 1.0 l/min.

2. Hydrogen: 1.6 l/min.

3. Nitrogen: 1.0 l/min.

4. Hydrogen Chloride (HCl): 50 cc/min.

Cycle: 5-5-120-5-30 min.:

1. 5 min. O_2

2. 5 min. O_2+HCl

3. 120 min. H_2+O_2+HCl

4. 5 min. O_2

5. 30 min. N_2

{A3.4} SILICON OXIDATION-GATE OXIDE:

The thin gate oxide (typically 20 nm) is grown from the substrate by "dry" oxidation in a furnace at 1000 ± 5C. This process was a result of simulation using SUPREM and experimental verification:

1. Oxygen: 1.0 l/min.

2. Nitrogen: 1.6 l/min.

3. Hydrogen Chloride (HCl): 50 cc/min.

Cycle: 5-3-8-20 min.:

    1. 5 min. O_2

    2. 3 min. O_2

    3. 8 min. O_2+HCl

    4. 20 min. N_2

{A3.5} TANTALUM THERMAL OXIDATION:

The tantalum metal is oxidized by "dry" oxidation in a furnace at 500±1C. The gas flow is adjusted as follows:

    1. Oxygen: 1.0 l/min.

Cycle: 45 to 90 min. until fully done, for 50-100 nm Ta metal.

    1. Thermally oxidize for 45-90 min. in O_2

{A3.6} SOURCE-DRAIN DIFFUSIONS:

The diffusion process is divided into predeposition and drive-in.

{A3.6.1} Predeposition:

    a) Prepare two half wafers, n-type material, cleaned per RCA process.

    b) Set the gas flows as follows:

    1. Nitrogen, coarse: 2000 cc/min.

    2. Oxygen, fine: 15 cc/min.

3. Nitrogen, fine (source): 60 cc/min.

c) Precondition furnace and predope boat, without wafer/samples.

d) Cycle: 3-18-2 min.:

1. 3 min. N_2 coarse + O_2 fine.

2. 18 min. N_2 coarse + O_2 fine + N_2 fine (BBr$_3$ source).

3. 2 min. N_2 + O_2 fine.

{A3.6.2} Drive-in:

a) Set the gas flows as follows:

1. Oxygen: 1.5 l/min.

2. Hydrogen: 2.4 l/min.

3. Hydrogen Chloride (HCl): 60 cc/min.

b) Cycle: 5-80-30-5 min.:

1. 5 min. O_2 only.

2. 80 min. O_2 + HCl.

3. 30 min. H_2 + O_2 + HCl.

4. 5 min. O_2 only.

{A3.6.3} BORON GLASS ETCHING:

The glassy surface formed during the predeposition stage has to be removed by etching:

a) Prepare 400 ml of buffered HF solution.

b) Dip all wafer/samples in de-ionized water.

c) Immerse samples in etching solution slowly. Leave for 90 secs.

d) Rinse in de-ionized water for 2+8 min.

e) Boil in isopropyl alcohol to remove all traces of

water. Dry in N_2 jet if required.

{A3.7} POST ANODIC OXIDATION CLEANING:

After the anodic oxidation takes place, the wafer/samples are cleaned with the following process:

1. Rinse wafer/sample in anodic cell holder for 10 min in de-ionized water.

2. Carefully remove sample and place in single wafer holder.

3. Place sample in boiling trichloroethylene.

4. Immerse sample in boiling isopropyl alcohol. Dry in vapours on top of beaker.

5. Dry in nitrogen jet if required.

{A3.8} THE BNR CLEANING PROCESS:

As some of the samples had Tantalum deposited using the MES technique at Bell Northern Research in Ottawa, the following steps were used in cleaning the wafers [Miner, 1981]:

1. Ultrasonic agitation in trichloroethylene for 5 min.

2. Ultrasonic agitation in acetone for 5 min.

3. Immersion in Alconox and de-ionized water solution with ultrasonic agitation.

4. Long rinse in flowing de-ionized water for 3 hours.

5. Dip in HF.

6. Spray rinse in isopropyl alcohol and blow dry with filtered nitrogen.

{A3.9} INTERFACIAL OXIDATION OF SILICON:

The process followed a dry oxidation of tantalum at 500C, deposited by RFS, and then a wet oxidation of Silicon at 800C. This creates a double oxide structure, with Ta_2O_5 on top of SiO_2.

The gas flows were set as follows:

1. Oxygen: 1.5 l/min.

2. Hydrogen: 2.5 l/min.

The cycle used was 3-X-3 min., with X varying between 24 and 114 minutes:

a) 3 min.: O_2

b) X min: $O_2 + H_2$

c) 3 min: O_2

The furnace used is the Pacesetter II, resistance heated, 2" quartz tube.

APPENDIX IV

SPICE AND SUPREM SIMULATION RESULTS

The simulation of the double dielectric MOSFET DC and transient characteristics was accomplished using SPICE. The oxidation was simulated using SUPREM.

1*******06-19-84 ******** SPICE 2G.1 (15OCT80) ********20:08:31*****

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION

O****   INPUT LISTING   TEMPERATURE =   27.000 DEG C

O***


```
*This is the Transient Response of a MTAOSFET, designed
*and fabricated by A. Eguizabal (1983).
*
VIN 4 O PULSE(O -11 5ONS 2NS 2NS 2OONS 1OOONS)
RS 4 3 600
RIN 3 O 500
CIN 3 O 1OPF
VDD 1 O DC -6
CBYP 1 O 22UF
RL 1 2 1K
COUT 2 O 15PF
ROUT 2 O 1OMEG
M1 O 3 2 O MOD1 L=1OU W=68OU AS=7OOOOP AD=7OOOOP PD=16OOU PS=16OOU
.MODEL MOD1 PMOS  VTO=-2.5 KP=6.82E-3
.DC VIN  O -11 -O.5
.PLOT DC V(2)
.PLOT TRAN V(2)
.TRAN 1ONS 5OONS ONS
.END
```
1****************06-19-84 ********************** SPICE 2G.1 (15OCT80) ************************20:08:31****************

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION
O****   MOSFET MODEL PARAMETERS   TEMPERATURE =   27.000 DEG C   .

O***.**********

```
                MOD1
OTYPE           PMOS
OLEVEL          1.000
OVTO           -2.500
OKP          6.82E-03
```

1***************06-19-84 *********************** SPICE 2G.1 (15OCT80) ***********************20:08:31***************

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION
O****   DC TRANSFER CURVES   TEMPERATURE =   27.000 DEG C

O***

X
   VIN   V(2)

```
X                            -6.000E+00          -4.000E+00          -2.000E+00            0.0
                             - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    0.0         -5.999E+00   *                   .                   .                   .
   -5.000E-01   -5.999E+00   *                   .                   .                   .
   -1.000E+00   -5.999E+00   *                   .                   .                   .
   -1.500E+00   -5.999E+00   *                   .                   .                   .
   -2.000E+00   -5.999E+00   *                   .                   .                   .
   -2.500E+00   -5.999E+00   *                   .                   .                   .
   -3.000E+00   -5.999E+00   *                   .                   .                   .
   -3.500E+00   -5.999E+00   *                   .                   .                   .
   -4.000E+00   -5.999E+00   *                   .                   .                   .
   -4.500E+00   -5.999E+00   *                   .                   .                   .
   -5.000E+00   -5.999E+00   *                   .                   .                   .
   -5.500E+00   -5.999E+00   *                   .                   .                   .
   -6.000E+00   -6.583E-02   .                   .                   .                 *.
   -6.500E+00   -2.927E-02   .                   .                   .                 *
   -7.000E+00   -1.918E-02   .                   .                   .                 *
   -7.500E+00   -1.431E-02   .                   .                   .                 *
   -8.000E+00   -1.142E-02   .                   .                   .                 *
   -8.500E+00   -9.505E-03   .                   .                   .                 *
   -9.000E+00   -8.142E-03   .                   .                   .                 *
   -9.500E+00   -7.121E-03   .                   .                   .                 *
   -1.000E+01.  -6.328E-03   .                   .                   .                 *
   -1.050E+01   -5.694E-03   .                   .                   .                 *
   -1.100E+01   -5.176E-03   .                   .                   .                 *
                             - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Y
1***************06-19-84 *********************** SPICE 2G.1 (15OCT80) ***********************20:08:31***************

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION
O****   INITIAL TRANSIENT SOLUTION   TEMPERATURE =   27.000 DEG C

O***

   NODE   VOLTAGE   NODE   VOLTAGE   NODE   VOLTAGE   NODE   VOLTAGE

(1)   -6.0000   (2)   -5.9994   (3)   0.0   (4)   0.0

    VOLTAGE SOURCE CURRENTS

    NAME   CURRENT

    VIN   0.0

    VDD   5.999E-07

    TOTAL POWER DISSIPATION   3.60E-06   WATTS
1****************06-19-84 ********************** SPICE 2G.1 (15OCT80) ************************20:08:31***************

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION
O****   OPERATING POINT INFORMATION   TEMPERATURE =   27.000 DEG C

O**

O
O**** MOSFETS

O   M1
OMODEL   MOD1
 ID   0.0
 VGS   5.999
 VDS   5.999
 VBS   5.999
1****************06-19-84 ********************** SPICE 2G.1 (15OCT80) ************************20:08:31***************

ODOUBLE DIELECTRIC MOSFET SPICE SIMULATION
O****   TRANSIENT ANALYSIS   TEMPERATURE =   27.000 DEG C

O**

X
    TIME   V(2)

X   -6.000E+00   -4.000E+00   -2.000E+00   0.0
                         -
    0.0   -5.999E+00   *   .   .   .
    1.000E-08 -5.999E+00   *   .   .   .
    2.000E-08 -5.999E+00   *   .   .   .
    3.000E-08 -5.999E+00   *   .   .   .
    4.000E-08 -5.999E+00   *   .   .   .
    5.000E-08 -5.999E+00   *   .   .   .
    6.000E-08 -8.229E-03   .   .   .   *
    7.000E-08 -1.188E-02   .   .   .   *

```
8.000E-08    -9.499E-03    .                         .                         .                         *
9.000E-08    -1.404E-03    .                         .                         .                         *
1.000E-07    -9.442E-03    .                         .                         .                         *
1.100E-07    -1.439E-03    .                         .                         .                         *
1.200E-07    -9.394E-03    .                         .                         .                         *
1.300E-07    -1.475E-03    .                         .                         .                         *
1.400E-07    -9.348E-03    .                         .                         .                         *
1.500E-07    -1.511E-03    .                         .                         .                         *
1.600E-07    -9.303E-03    .                         .                         .                         *
1.700E-07    -1.546E-03    .                         .                         .                         *
1.800E-07    -9.258E-03    .                         .                         .                         *
1.900E-07    -1.581E-03    .                         .                         .                         *
2.000E-07    -9.213E-03    .                         .                         .                         *
2.100E-07    -1.616E-03    .                         .                         .                         *
2.200E-07    -9.169E-03    .                         .                         .                         *
2.300E-07    -1.650E-03    .                         .                         .                         *
2.400E-07    -9.126E-03    .                         .                         .                         *
2.500E-07     1.015E-02    .                         .                         .                         *
2.600E-07    -1.788E+00    .                         .                   *                               .
2.700E-07    -3.835E+00    .                   *                               .                         .
2.800E-07    -4.890E+00    .             *                                     .                         .
2.900E-07    -5.425E+00    .        *                                          .                         .
3.000E-07    -5.710E+00    .    *                                              .                         .
3.100E-07    -5.855E+00    .  *                                                .                         .
3.200E-07    -5.927E+00    .*                                                  .                         .
3.300E-07    -5.963E+00    *                                                   .                         .
3.400E-07    -5.981E+00    *                                                   .                         .
3.500E-07    -5.990E+00    *                                                   .                         .
3.600E-07    -5.995E+00    *                                                   .                         .
3.700E-07    -5.997E+00    *                                                   .                         .
3.800E-07    -5.998E+00    *                                                   .                         .
3.900E-07    -5.999E+00    *                                                   .                         .
4.000E-07    -5.999E+00    *                                                   .                         .
4.100E-07    -5.999E+00    *                                                   .                         .
4.200E-07    -5.999E+00    *                                                   .                         .
4.300E-07    -5.999E+00    *                                                   .                         .
4.400E-07    -5.999E+00    *                                                   .                         .
4.500E-07    -5.999E+00    *                                                   .                         .
4.600E-07    -5.999E+00    *                                                   .                         .
4.700E-07    -5.999E+00    *                                                   .                         .
4.800E-07    -5.999E+00    *                                                   .                         .
4.900E-07    -5.999E+00    *                                                   .                         .
5.000E-07    -5.999E+00    *                                                   .                         .
```

Y
O

JOB CONCLUDED
O   TOTAL JOB TIME   0.0

1

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION 0-05 ***


```
1....TITLE GATE OXIDE
2....GRID DYSI=0.001, DPTH=0.2 , YMAX=1.0
3....SUBST ORNT=100, ELEM=P, CONC=4.0E14
4....PLOT TOTL=Y
5....PRINT HEAD=Y
6....STEP TYPE=OXID, TIME=3, TEMP=1090, MODL=DRYO
7....END
```
†

GATE OXIDE

STEP # 1

OXIDATION IN DRY OXYGEN
TOTAL STEP TIME   =   3.0 MINUTES
INITIAL TEMPERATURE =   1090.00   DEGREES C.
OXIDE THICKNESS   =   2.2444E-02 MICRONS

LINEAR   OXIDE GROWTH RATE =   2.492192E-03 MICRONS/MINUTE
PARABOLIC OXIDE GROWTH RATE =   3.647341E-04 MICRONS!2/MINUTE
OXIDE GROWTH PRESSURE   =   1.00000   ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT	I
PHOSPHORUS I	5.23156E-06 I	1.22179E-03 I	10.000	I 3.95133E-02	I

SURFACE CONCENTRATION = -4.375506E+14 ATOMS/CM!3

JUNCTION DEPTH	I	SHEET RESISTANCE
	I	125136. OHMS/SQUARE

NET ACTIVE CONCENTRATION

```
OXIDE   CHARGE =  1.011304E+08    IS    0.253    % OF TOTAL
SILICON CHARGE =  3.987205E+10    IS    99.7     % OF TOTAL
TOTAL   CHARGE =  3.997318E+10    IS    99.9     % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```


CHEMICAL CONCENTRATION OF PHOSPHORUS

```
OXIDE   CHARGE =  1.011304E+08    IS    0.253    % OF TOTAL
SILICON CHARGE =  3.987205E+10    IS    99.7     % OF TOTAL
TOTAL   CHARGE =  3.997318E+10    IS    99.9     % OF INITIAL
```

```
INITIAL CHARGE =  3.999999E+10
1        GATE OXIDE

         I STEP =  1     TIME =    3.0 MINUTES.
         I
DEPTH I                    CONCENTRATION (LOG ATOMS/CC)
(UM)  I
         14         15         16         17         18         19         20         21
 -0.02  *------------------------------------------------------------------------
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         * .        I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *·         I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
  0.0   *------*----------------------------------------------------------------
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *·   I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
  1.00  ------------------------------------------------------------------------
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
  2.00  ------------------------------------------------------------------------
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
  3.00  ------------------------------------------------------------------------
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
         I          I          I          I          I          I          I          I
```

```
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
  4.OO ---------------------------------------------------------------------------------
1
 SUPREM END.d
1



       *** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

                        *** VERSION O-O5 ***



  1....TITLE GATE OXIDE
  2....GRID DYSI=O.OO1, DPTH=O.2, YMAX=1.O
  3....SUBST ORNT=1OO, ELEM=P, CONC=4.OE14
  4....PLOT TOTL=Y
  5....PRINT HEAD=Y
  6....STEP TYPE=OXID, TIME=8O.O, TEMP=1O9O, MODL=DRYO
  7....END
1
 GATE OXIDE

 STEP #   1


 OXIDATION IN DRY OXYGEN
 TOTAL STEP TIME      =  8O.O MINUTES
 INITIAL TEMPERATURE =   1O9O.OO      DEGREES C.
 OXIDE THICKNESS      =    O.1198     MICRONS

 LINEAR    OXIDE GROWTH RATE =  2.492192E-O3 MICRONS/MINUTE
 PARABOLIC OXIDE GROWTH RATE =  3.647341E-O4 MICRONS!2/MINUTE
 OXIDE GROWTH PRESSURE       =   1.OOOOO      ATMOSPHERES

            I  OXIDE        I  SILICON      I               I  SURFACE      I
            I  DIFFUSION    I  DIFFUSION    I  SEGREGATION   I  TRANSPORT
            I  COEFFICIENT  I  COEFFICIENT  I  COEFFICIENT   I  COEFFICIENT  I
 --------------------------------------------------------------------------------
 PHOSPHORUS I   5.23156E-O6 I   1.22179E-O3 I    1O.OOO      I   3.95133E-O2 I

  SURFACE CONCENTRATION = -4.474924E+14 ATOMS/CM!3

    JUNCTION DEPTH       I     SHEET RESISTANCE
 ----------------------I--------------------------
                       I   126788.    OHMS/SQUARE


 NET ACTIVE CONCENTRATION

 OXIDE   CHARGE =  4.517386E+O8      IS    1.13     % OF TOTAL
 SILICON CHARGE =  3.935OO2E+1O      IS    98.9     % OF TOTAL
 TOTAL   CHARGE =  3.98O176E+1O      IS    99.5     % OF INITIAL
 INITIAL CHARGE =  3.999999E+1O
```

CHEMICAL CONCENTRATION OF PHOSPHORUS

```
OXIDE    CHARGE =  4.517386E+08    IS    1.13    % OF TOTAL
SILICON CHARGE =  3.935002E+10    IS    98.9    % OF TOTAL
TOTAL    CHARGE =  3.980176E+10    IS    99.5    % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```

1   GATE OXIDE

```
         I STEP =  1      TIME =    80.0 MINUTES.
         I
DEPTH  I                    CONCENTRATION (LOG ATOMS/CC)
(UM)   I
         14         15         16         17         18         19         20         21
-0.12  *-------------------------------------------------------------------------
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
         *          I          I          I          I          I          I          I
 0.0   *-------*-----------------------------------------------------------------
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I'         I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I          I          I
         I      *    I          I          I          I          I         .I          I
         I           I          I          I          I          I          I          I
 1.00  -----------------------------------------------------------------------------
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
 2.00  -----------------------------------------------------------------------------
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I.         I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
         I           I          I          I          I          I          I          I
 3.00  -----------------------------------------------------------------------------
```

```
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           .I          I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
    I           I           I           I           I           I           I           I
 4.00 --------------------------------------------------------------------------------
```

1

SUPREM END.ð

1

```
        *** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

                        *** VERSION 0-05 ***
```

```
    1....TITLE GATE OXIDE
    2....GRID DYSI=0.001, DPTH=0.2 , YMAX=1.0
    3....SUBST ORNT=100, ELEM=P, CONC=4.0E14
    4....PLOT TOTL=Y
    5....PRINT HEAD=Y
    6....STEP TYPE=OXID, TIME=3, TEMP=1000, MODL=DRYO
    7....END
```
1

GATE OXIDE

STEP #   1

OXIDATION IN DRY OXYGEN
TOTAL STEP TIME   =   3.0 MINUTES
INITIAL TEMPERATURE =   1000.00   DEGREES C.
OXIDE THICKNESS   =   1.4006E-02 MICRONS

LINEAR   OXIDE GROWTH RATE = 7.479377E-03 MICRONS/MINUTE
PARABOLIC OXIDE GROWTH RATE = 1.739819E-04 MICRONS!2/MINUTE
OXIDE GROWTH PRESSURE   =   1.00000   ATMOSPHERES

	OXIDE DIFFUSION COEFFICIENT	SILICON DIFFUSION COEFFICIENT	SEGREGATION COEFFICIENT	SURFACE TRANSPORT COEFFICIENT
PHOSPHORUS	6.3661OE-07	1.35026E-04	10.000	1.19299E-02

  SURFACE CONCENTRATION = -4.947440E+14 ATOMS/CM!3

   JUNCTION DEPTH   I   SHEET RESISTANCE
  ----------------------I----------------------
                        I   124966.   OHMS/SQUARE

NET ACTIVE CONCENTRATION

```
OXIDE    CHARGE =  6.576280E+07      IS   0.164      % OF TOTAL
SILICON CHARGE =  3.992655E+10      IS   99.8       % OF TOTAL
TOTAL    CHARGE =  3.999231E+10      IS   100.       % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```

CHEMICAL CONCENTRATION OF PHOSPHORUS

```
OXIDE    CHARGE =  6.576280E+07      IS   0.164      % OF TOTAL
SILICON CHARGE =  3.992655E+10      IS   99.8       % OF TOTAL
TOTAL    CHARGE =  3.999231E+10      IS   100.       % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```
1   GATE OXIDE

```
         I STEP =  1      TIME =     3.0 MINUTES.
         I
DEPTH I                    CONCENTRATION (LOG ATOMS/CC)
(UM)  I
     14          15          16          17          18          19          20          21
-0.01 *-----------------------------------------------------------------------------------
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *         · I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
      *           I           I           I           I           I           I           I
 0.0  *-------*---------------------------------------------------------------------------
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I       *   I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
 1.00 -----------------------------------------------------------------------------------
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I ·         I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
 2.00 -----------------------------------------------------------------------------------
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
      I           I           I           I           I           I           I           I
```

```
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
3.00 ----------------------------------------------------------------------
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
    I         I         I         I         I         I         I         I
4.00 ----------------------------------------------------------------------
1
 SUPREM END.ə
1
```

*** STANFORD UNIVERSITY PROCESS ENGINEERING MODELS PROGRAM ***

*** VERSION O-O5 ***

```
  1....TITLE GATE OXIDE
  2....GRID DYSI=O.OO1, DPTH=O.2, YMAX=1.O
  3....SUBST ORNT=1OO, ELEM=P, CONC=4.OE14
  4....PLOT TOTL=Y
  5....PRINT HEAD=Y
  6....STEP TYPE=OXID, TIME=5, TEMP=1OOO, MODL=DRYO
  7....END
1
 GATE OXIDE

 STEP #  1


 OXIDATION IN DRY OXYGEN
 TOTAL STEP TIME     =   5.O MINUTES
 INITIAL TEMPERATURE =   1OOO.OO    DEGREES C.
 OXIDE THICKNESS     =   2.OO74E-O2 MICRONS

 LINEAR   OXIDE GROWTH RATE =  7.479377E-O3 MICRONS/MINUTE
 PARABOLIC OXIDE GROWTH RATE =  1.739819E-O4 MICRONS!2/MINUTE
 OXIDE GROWTH PRESSURE       =   1.OOOOO    ATMOSPHERES
```

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT	I
PHOSPHORUS	I 6.3661OE-O7	I 1.35O26E-O4	I 10.000	I 1.19299E-O2	I

SURFACE CONCENTRATION = -5.045019E+14 ATOMS/CM!3

```
  JUNCTION DEPTH       I      SHEET RESISTANCE
----------------------I---------------------------
                      I   125066.    OHMS/SQUARE
```

NET ACTIVE CONCENTRATION

```
OXIDE    CHARGE =  9.653334E+07    IS   0.241    % OF TOTAL
SILICON CHARGE =  3.989433E+10    IS   99.8     % OF TOTAL
TOTAL    CHARGE =  3.999086E+10    IS   100.     % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```

CHEMICAL CONCENTRATION OF PHOSPHORUS

```
OXIDE    CHARGE =  9.653334E+07    IS   0.241    % OF TOTAL
SILICON CHARGE =  3.989433E+10    IS   99.8     % OF TOTAL
TOTAL    CHARGE =  3.999086E+10    IS   100.     % OF INITIAL
INITIAL CHARGE =  3.999999E+10
```
1   GATE OXIDE

```
        I STEP =  1     TIME =     5.0 MINUTES.
        I
DEPTH I                     CONCENTRATION (LOG ATOMS/CC)
(UM)  I
        14          15          16          17          18          19          20          21
 -0.02 *-------------------------------------------------------------------------------------
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
        *           I           I           I           I           I           I           I
  0.0  *-------*-----------------------------------------------------------------------------
        I      *    I           I          ·I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I      *    I·          I           I           I           I           I           I
        I      *    I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
 1.00  --------------------------------------------------------------------------------------
        I           I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
        I           I           I           I           I           I           I           I
```

2.00

3.00

4.00

SUPREM END.δ

1

APPENDIX I

C-V AND I-V CURVES OF MOS CAPACITORS

ADDENDUM TO THE M.A.Sc. THESIS

TANTALUM PENTOXIDE, A NON CONVENTIONAL

GATE INSULATOR FOR MOS DEVICES

by

ANTONIO L. EGUIZABAL RIVAS

THE UNIVERSITY OF BRITISH COLUMBIA

January 1984

SAMPLE N2, SINGLE DIELECTRIC

n Type, Thermal 500 C.

Sample N2
n Type Silicon
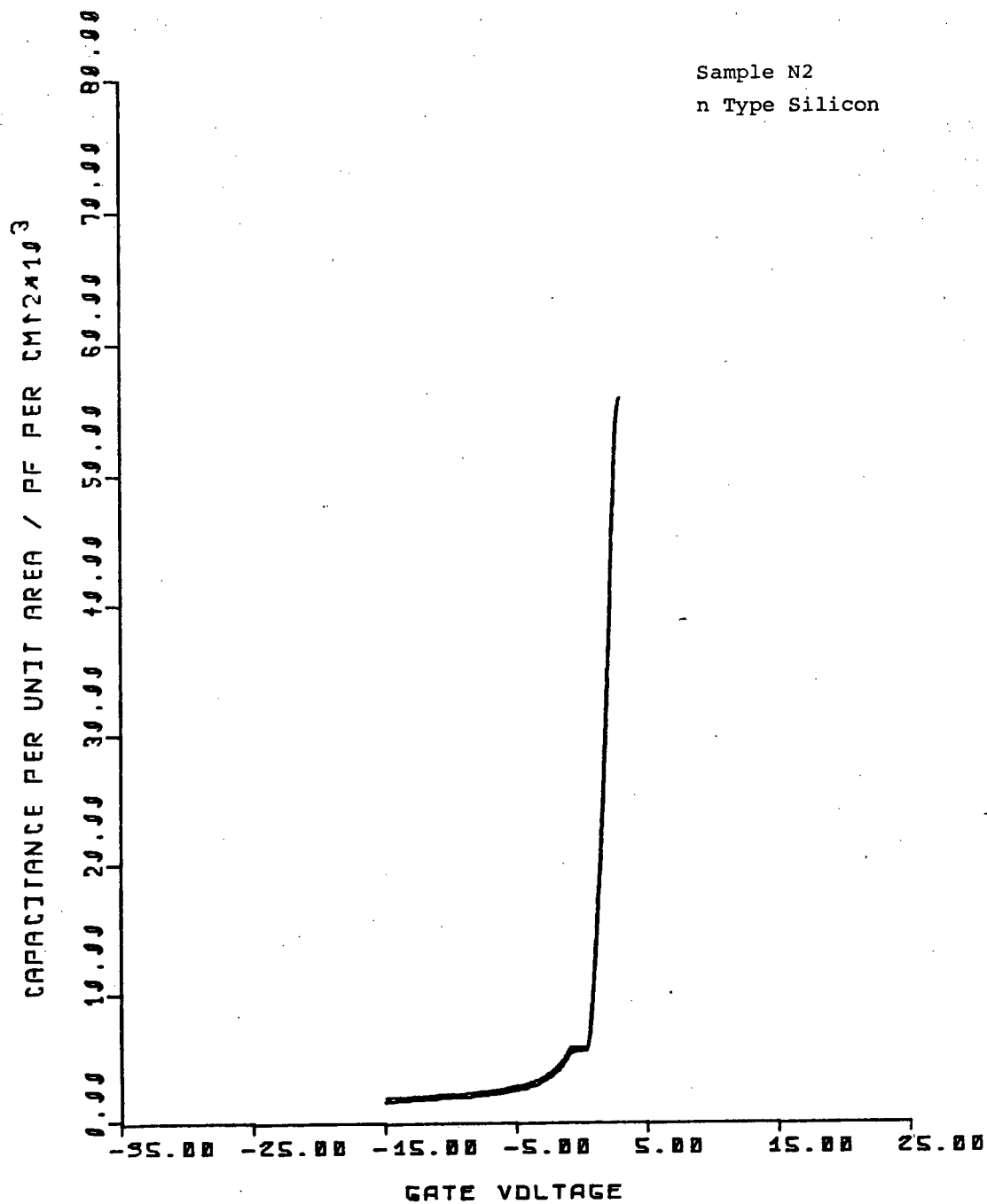
SCHOTTKY IV PLOT

Sample N2
n Type Silicon
Gate negative
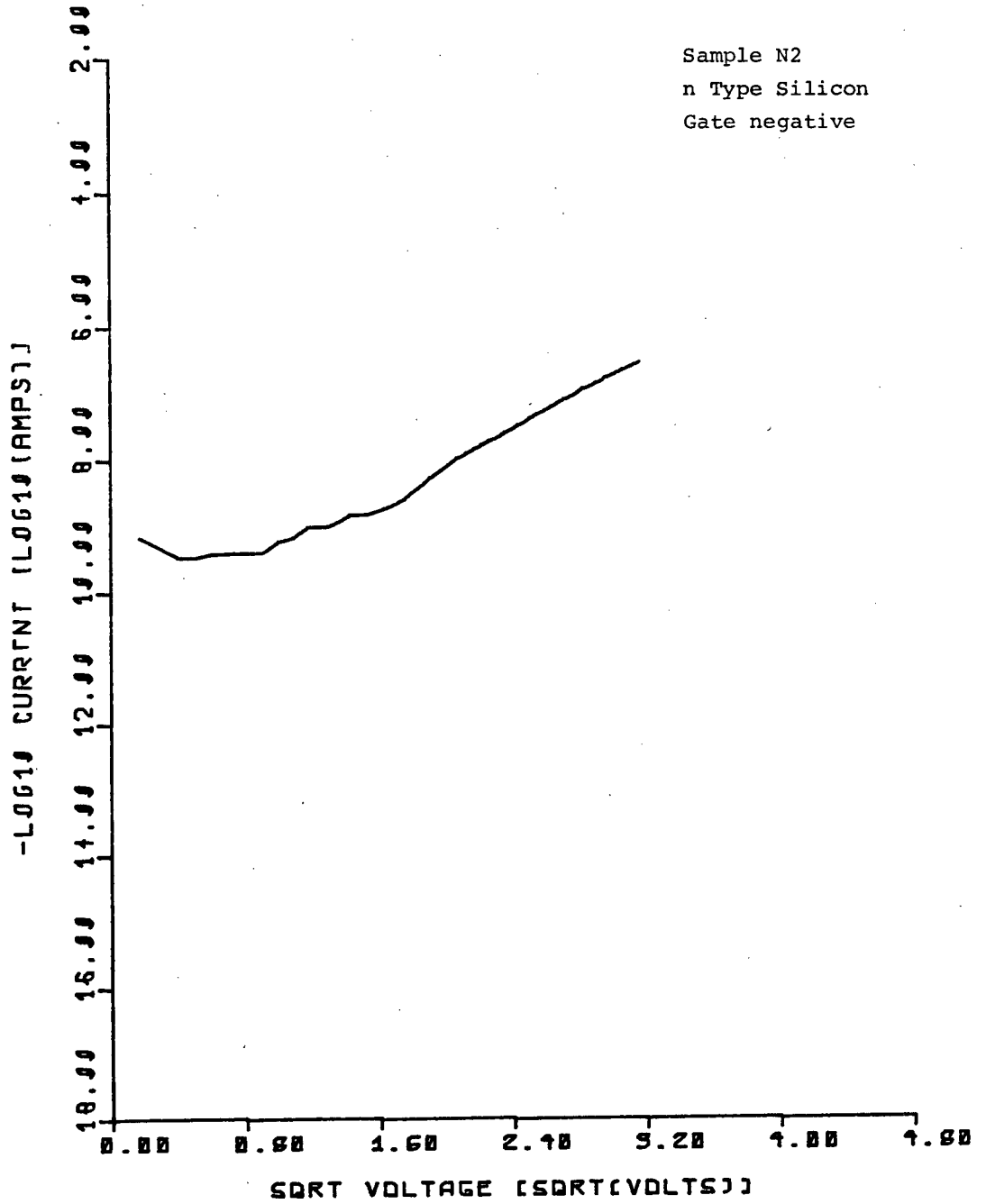
SAMPLE N3, SINGLE DIELECTRIC

n Type, Thermal 500 C.

CAPACITANCE PER UNIT AREA / PF PER CMʃ2×10²

GATE VOLTAGE

Sample N3
n Type Silicon

SCHOTTKY IV PLOT

Sample N3
n Type Silicon
Gate Negative

−LOG10 CURRENT (LOG10(AMPS))

SQRT VOLTAGE (SQRT(VOLTS))
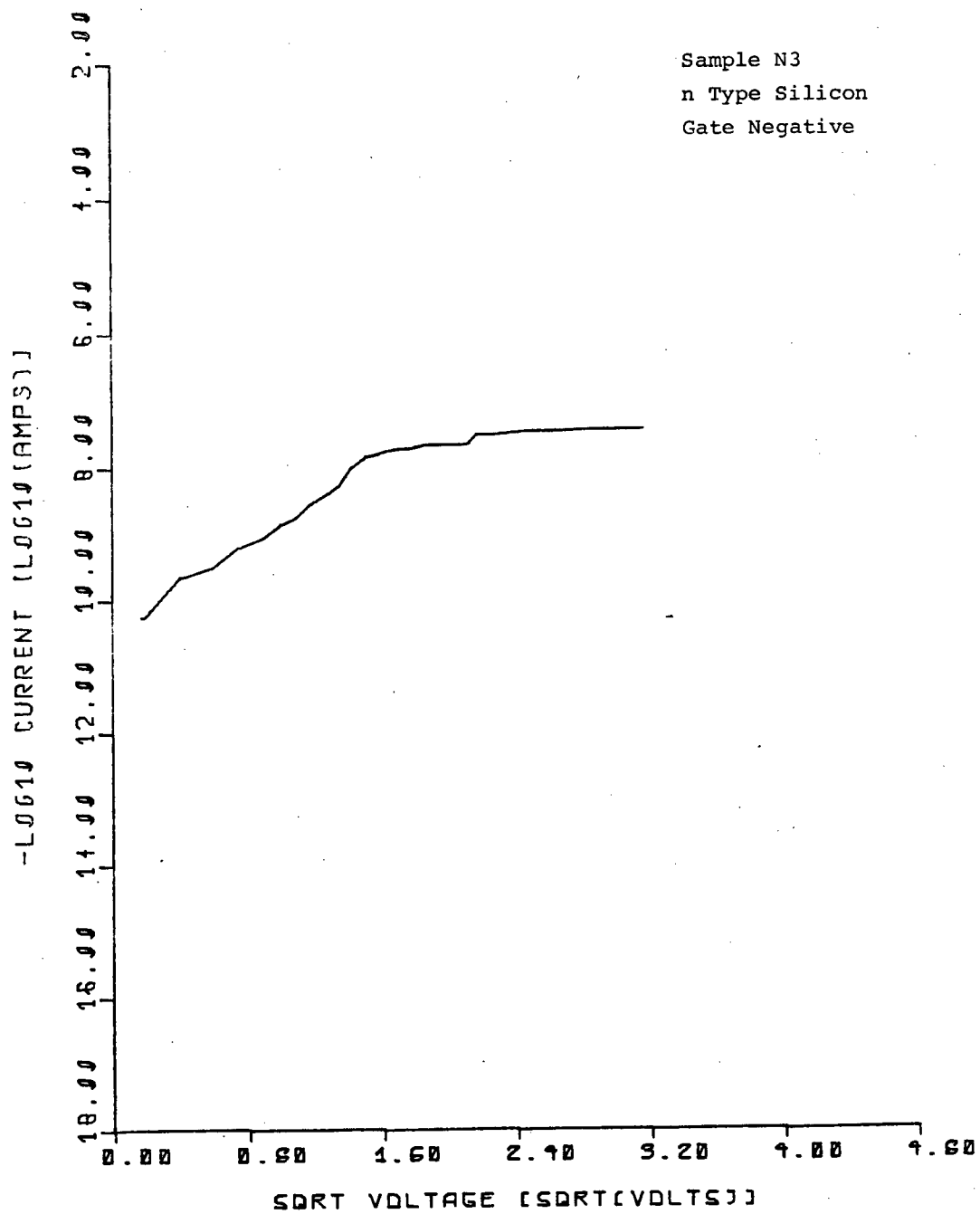
SAMPLE 1T6, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 1T6
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE
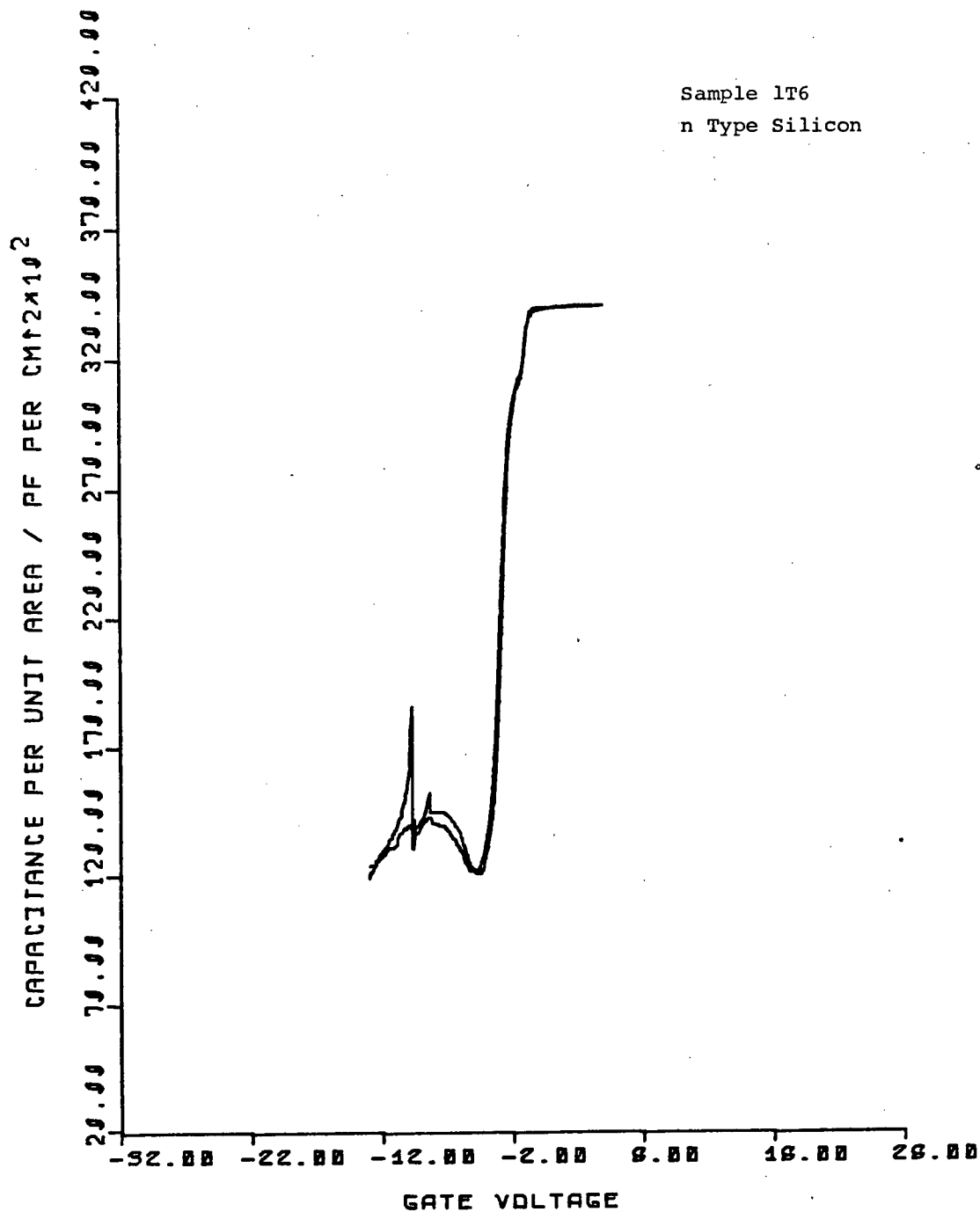
SCHOTTKY IV PLOT

Sample 1T6
n Type Silicon
Gate negative

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]
X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
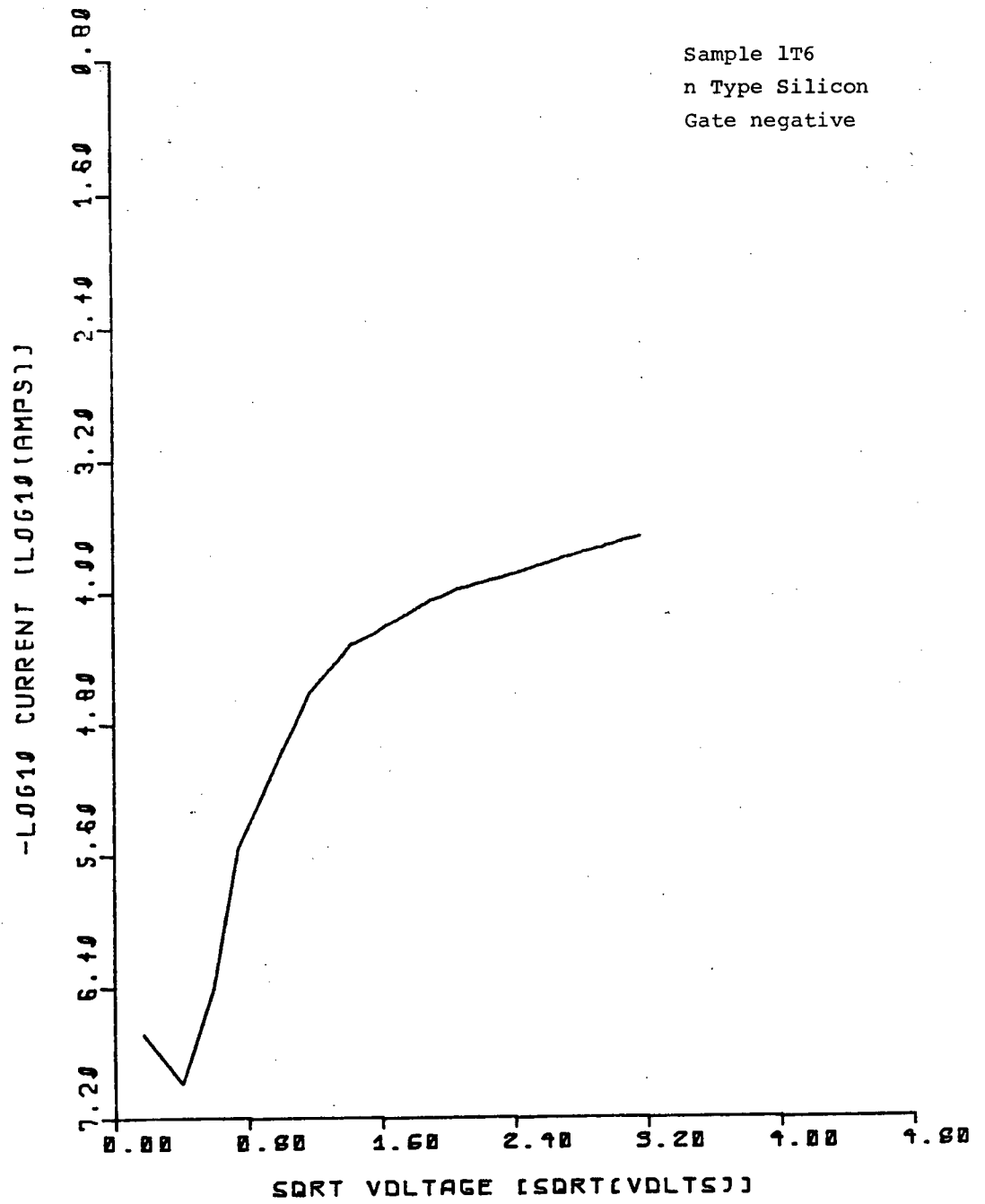
SAMPLE 2T6, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 2T6
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

(y-axis) 0.00 50.00 100.00 150.00 200.00 250.00 300.00 350.00 400.00

(x-axis) −20.00 −15.00 −10.00 −5.00 0.00 5.00 10.00
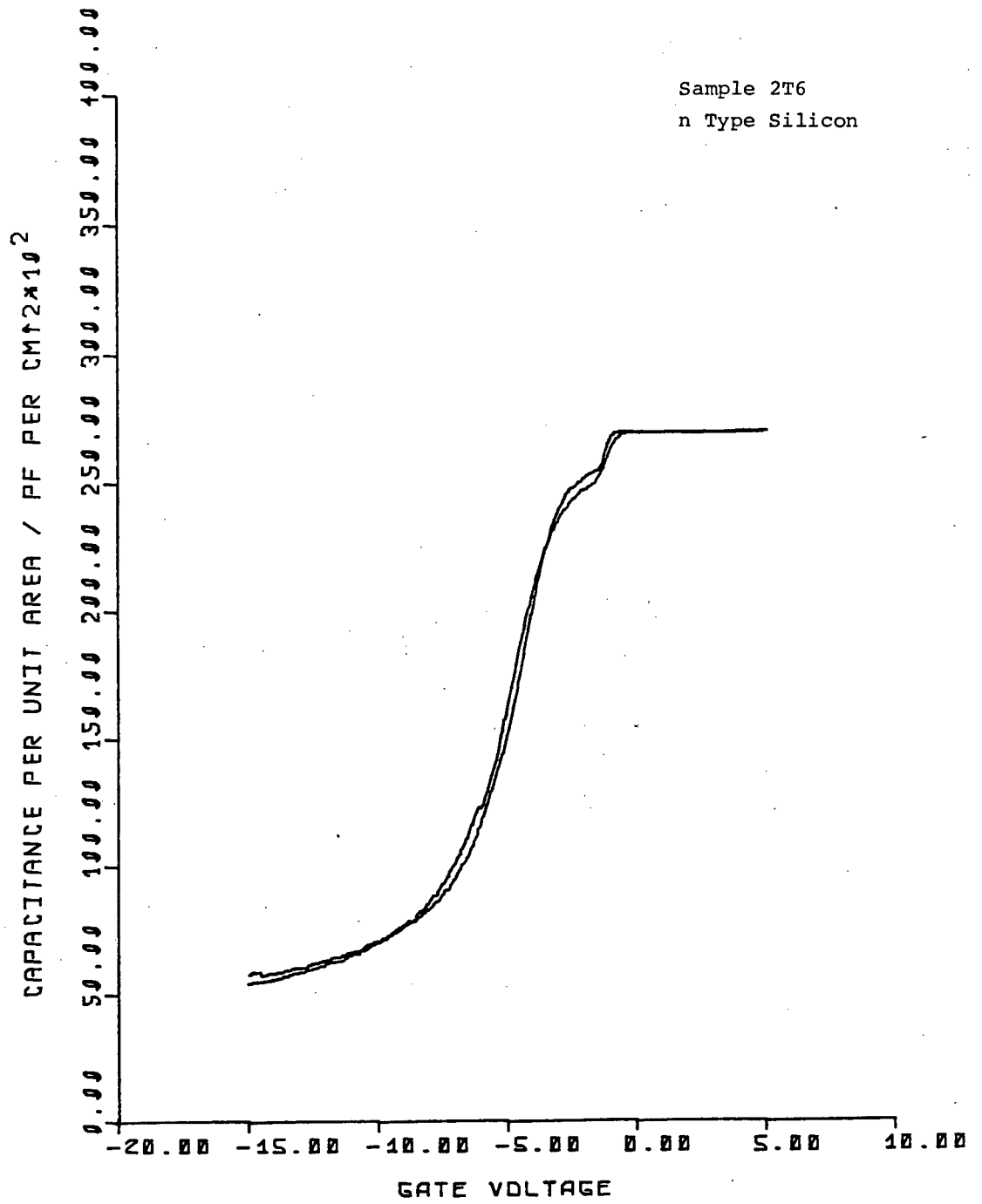
SCHOTTKY IV PLOT

Sample 2T6
n Type Silicon
Gate negative

−LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT[VOLTS]]
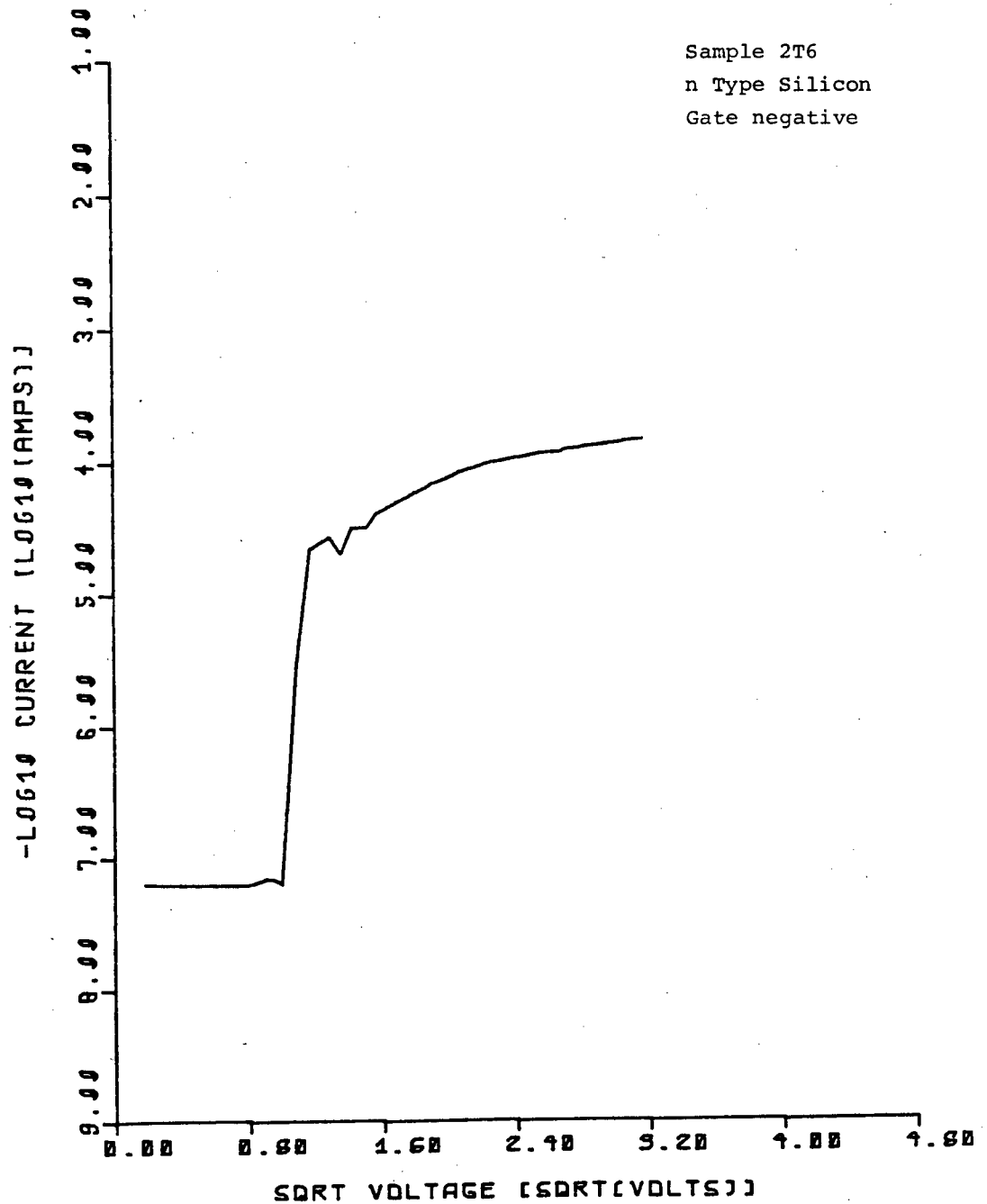
SAMPLE 3T6, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 3T6
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample 3T6
n Type Silicon
Gate negative

-LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT(VOLTS)]
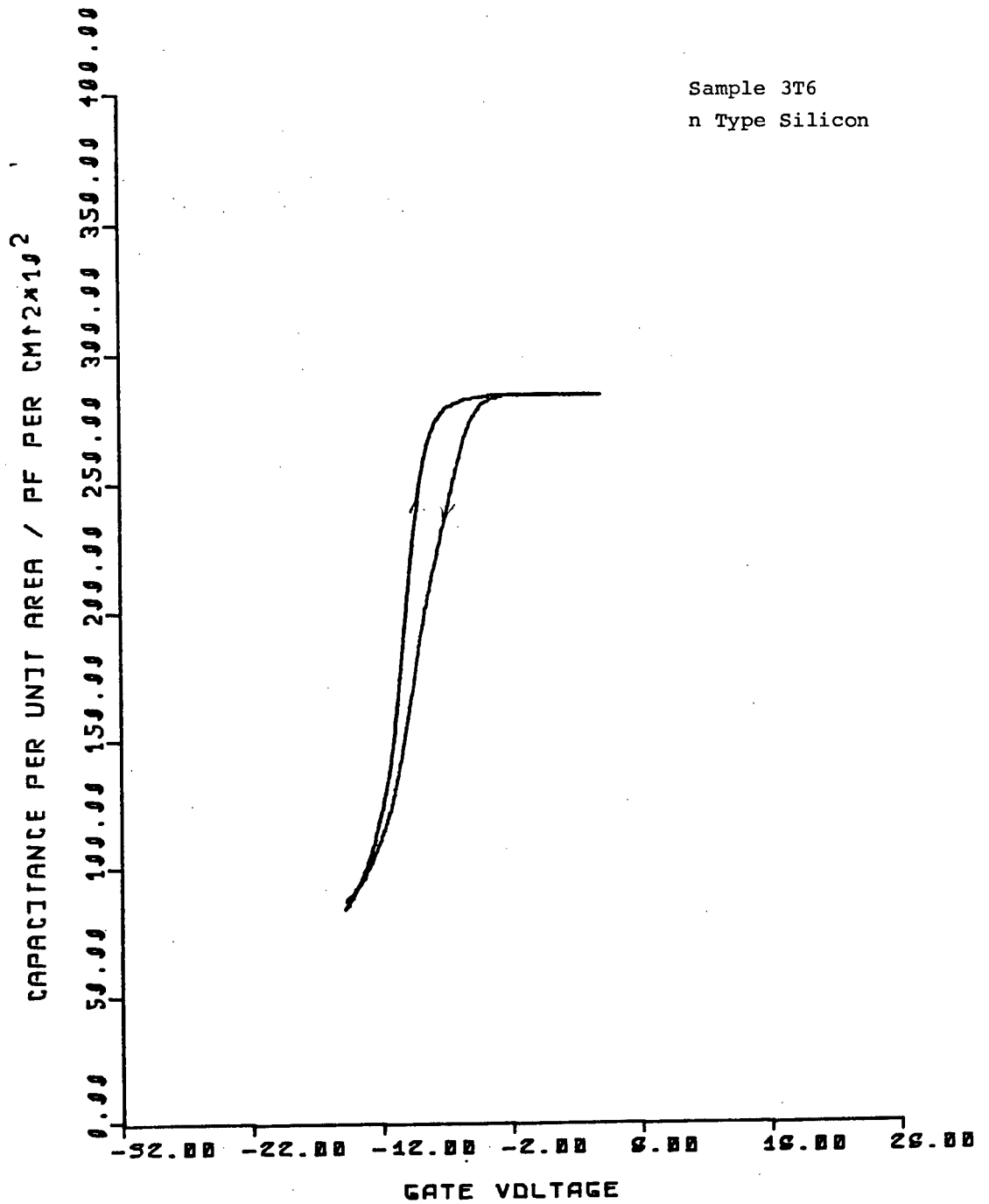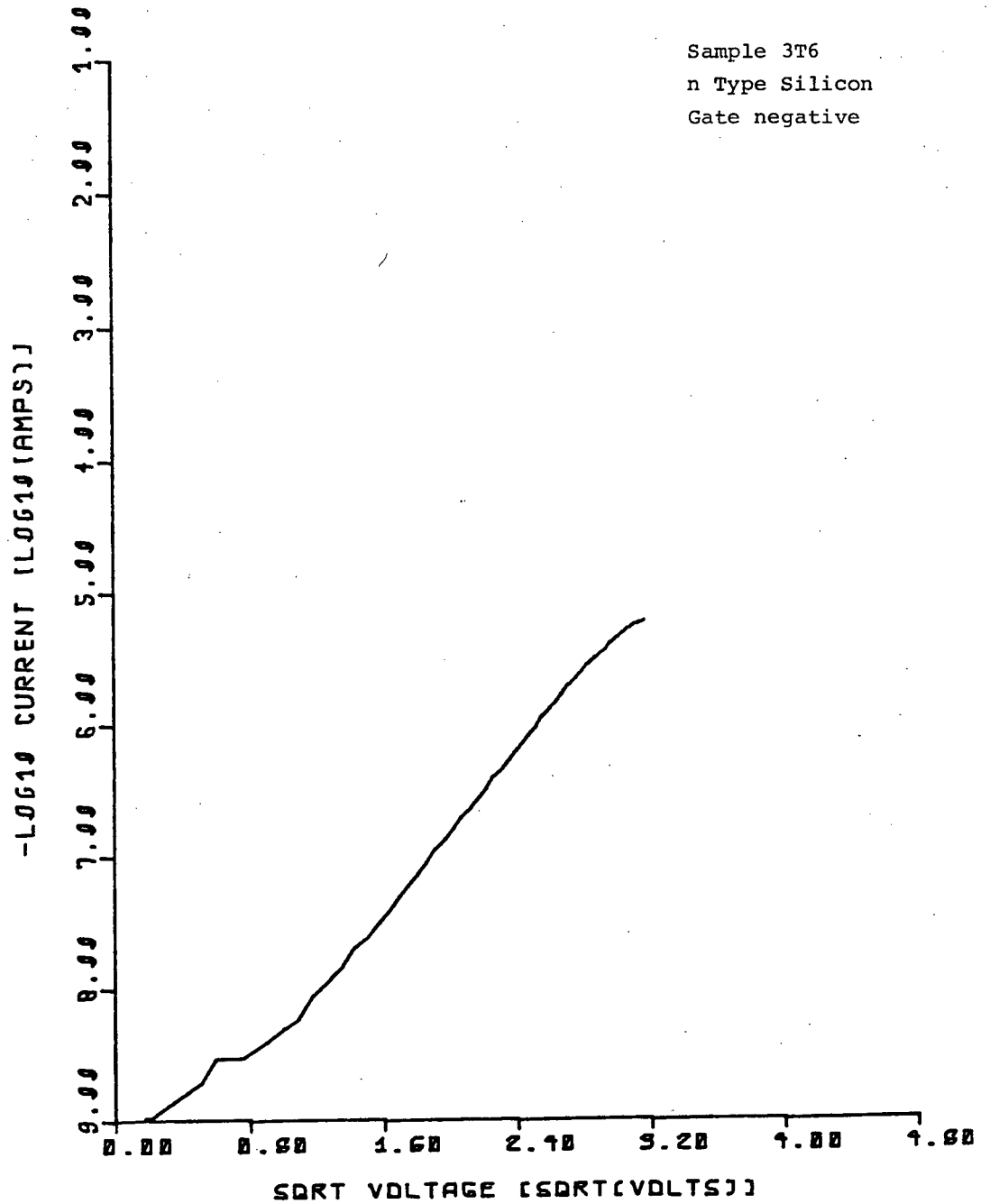
SAMPLE 4T6, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 4T6
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

400.00 350.00 300.00 250.00 200.00 150.00 100.00 50.00 0.00

GATE VOLTAGE

-32.00 -22.00 -12.00 -2.00 8.00 18.00 28.00

SCHOTTKY IV PLOT

Sample 4T6
n Type Silicon
Gate negative

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
Y-axis: -LOG10 CURRENT [LOG10(AMPS)]
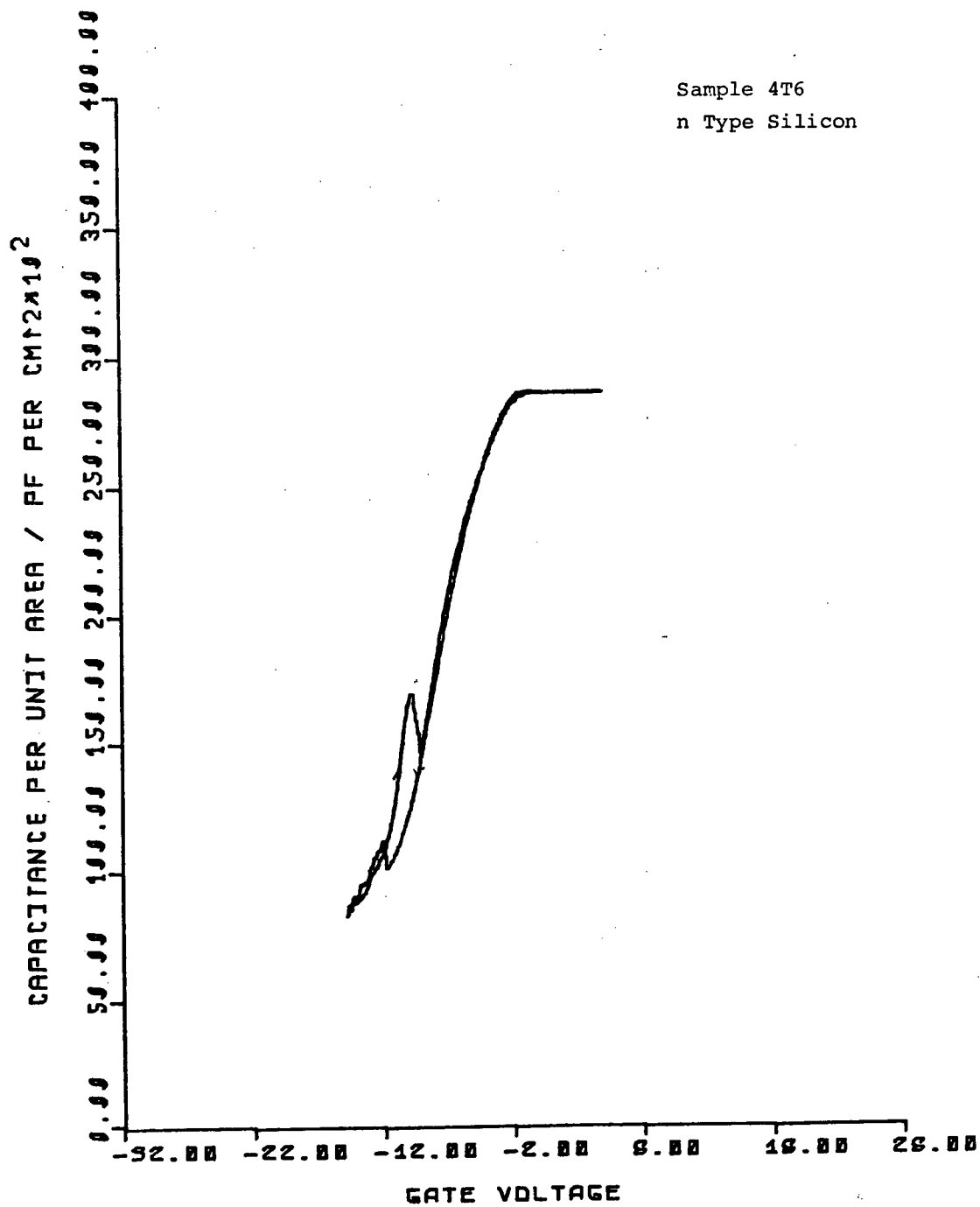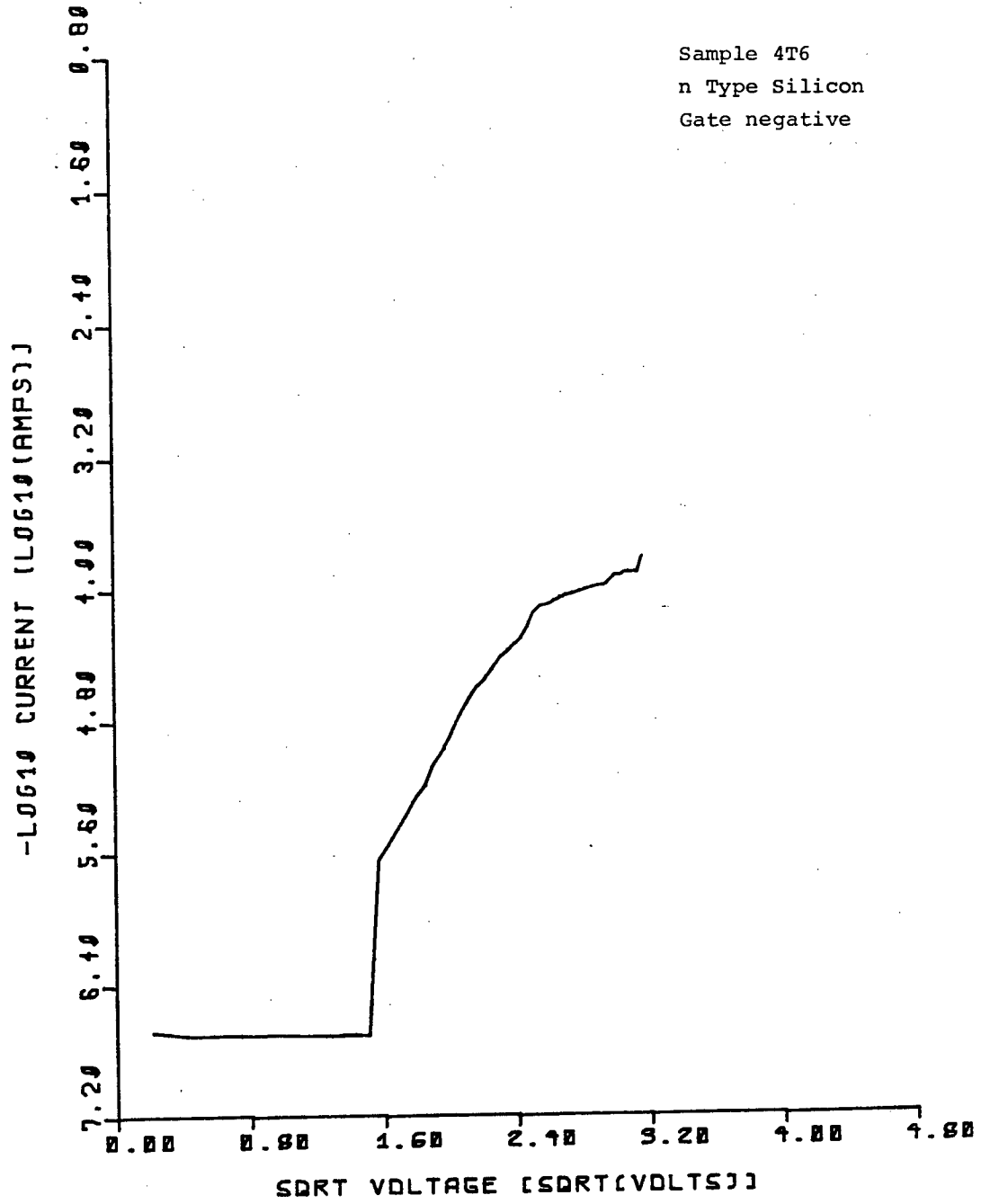
SAMPLE 1T7, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 1T7
n Type Silicon

SCHOTTKY IV PLOT

Sample 1T7
n Type Silicon
Gate negative

−LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT[VOLTS]]
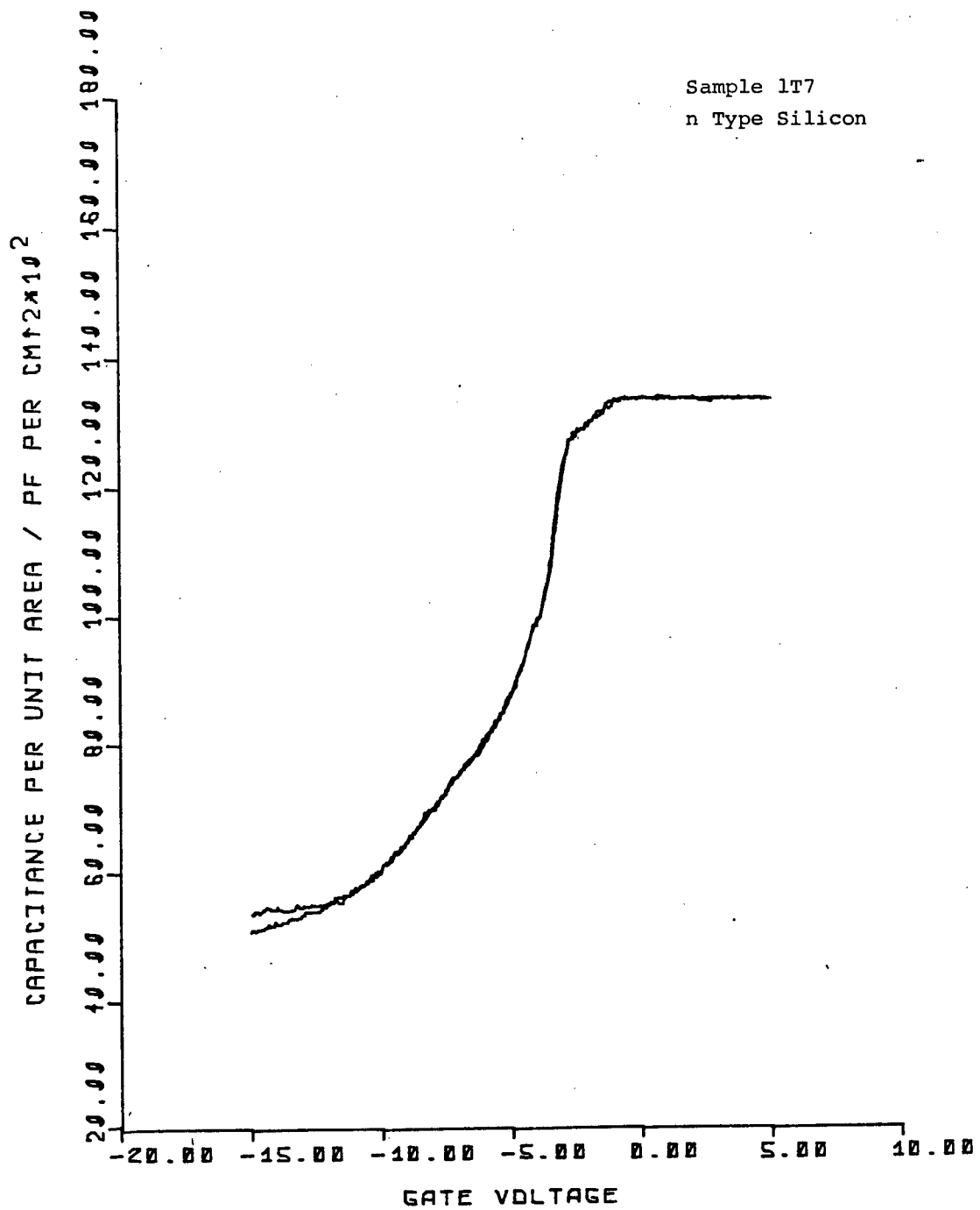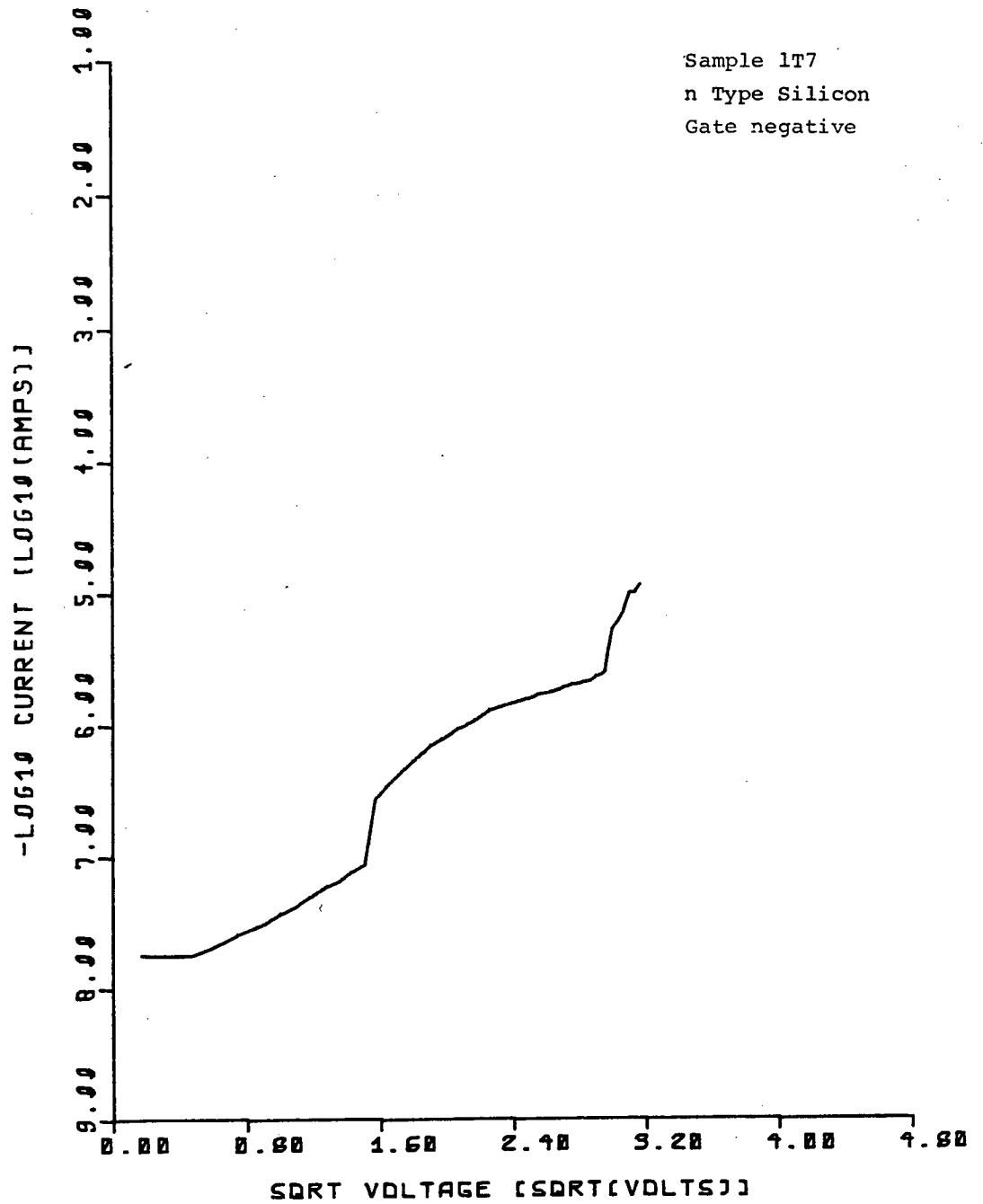
SAMPLE 2T7, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 2T7
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample 2T7
n Type Silicon
Gate negative
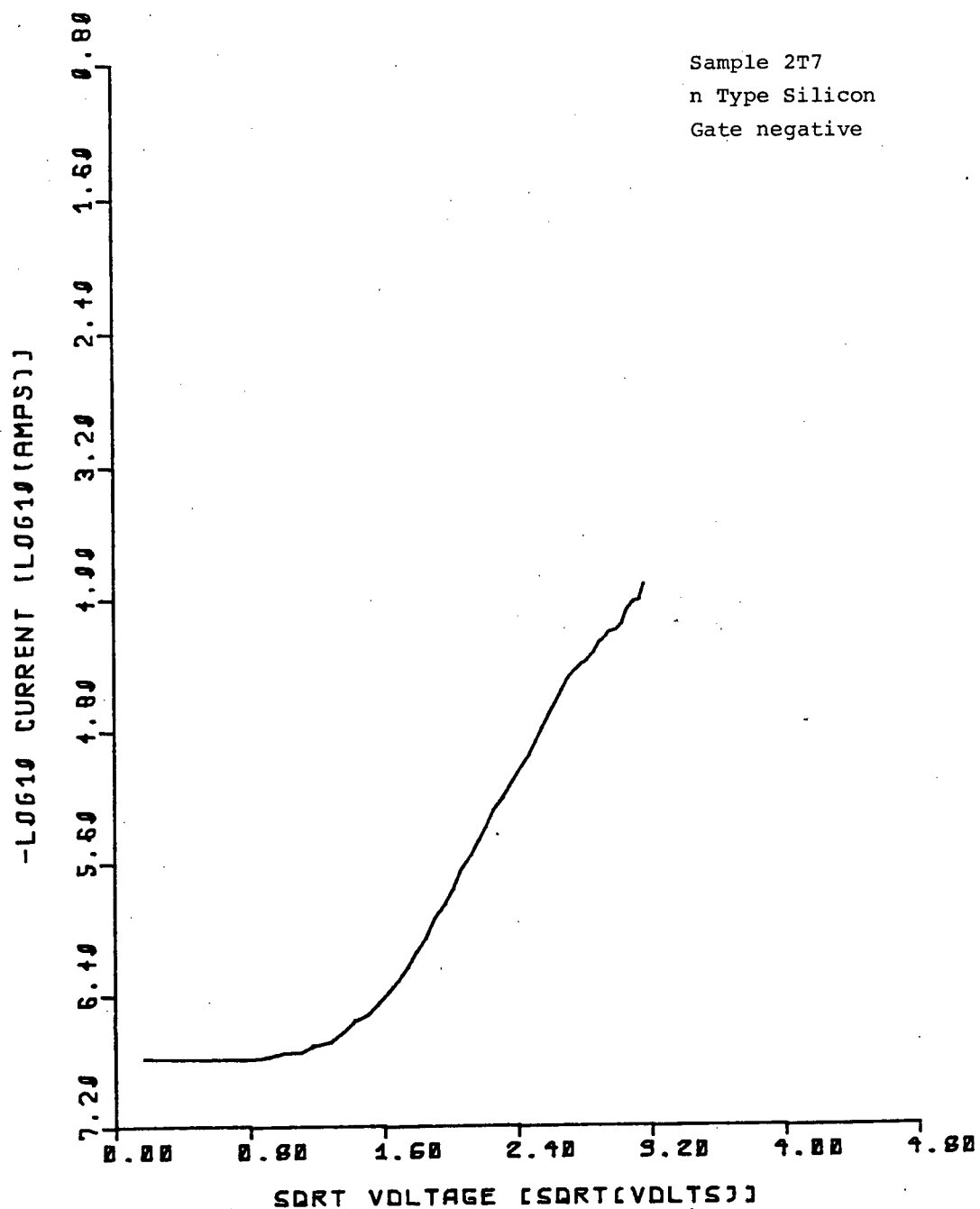
SAMPLE 3T7, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 3T7
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE
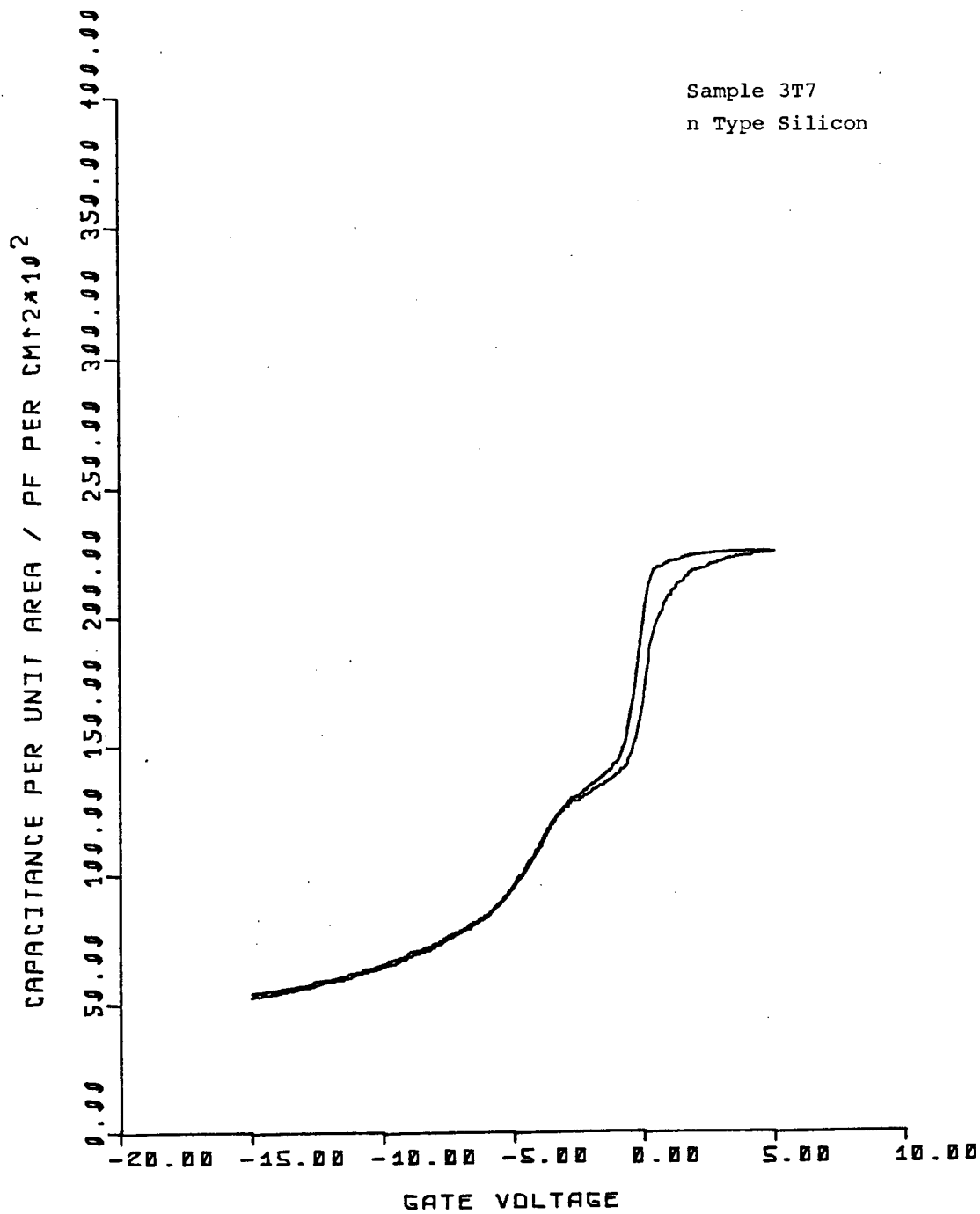
SCHOTTKY IV PLOT

Sample 3T7
n Type Silicon
Gate negative

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
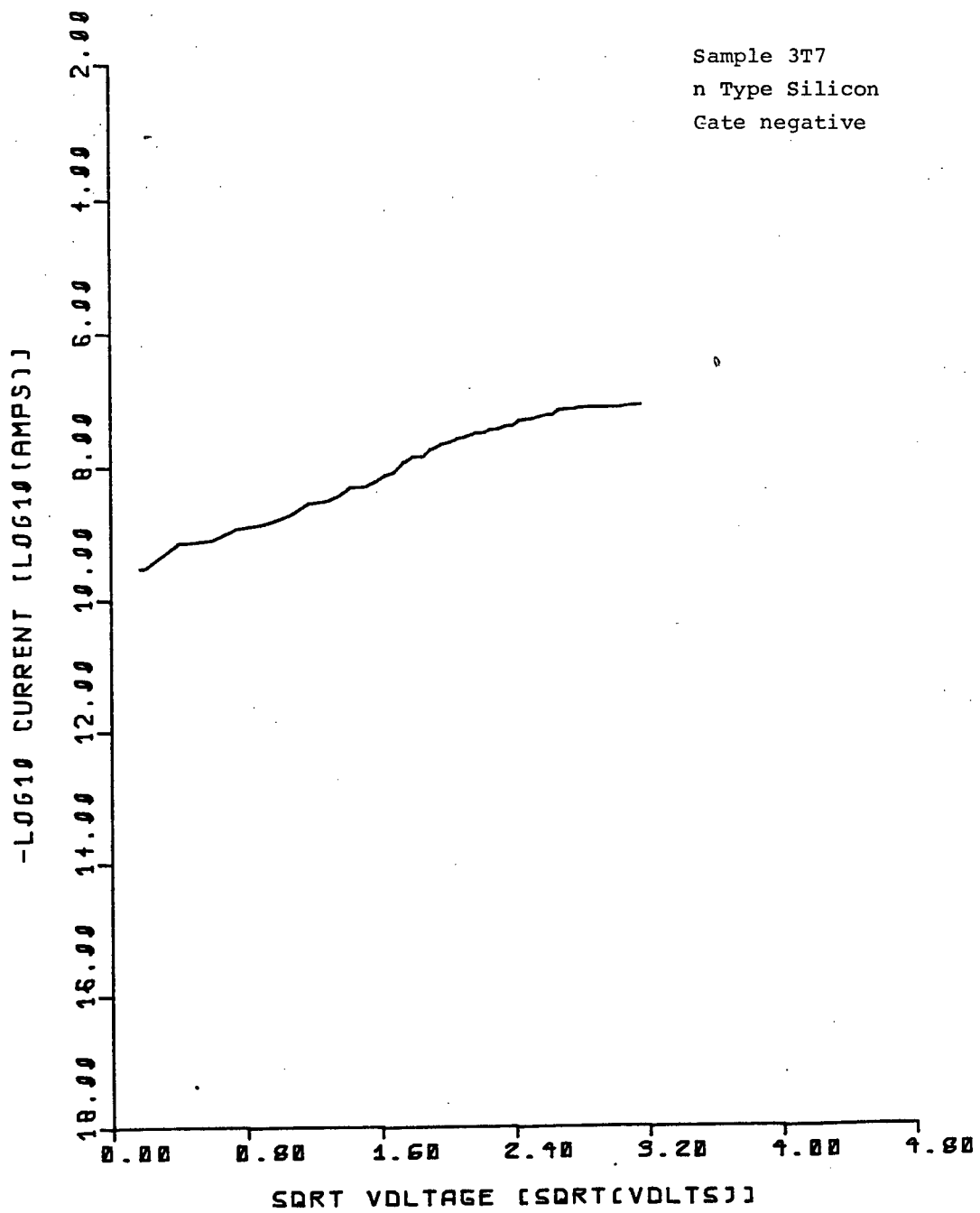
SAMPLE 4T7, DOUBLE DIELECTRIC

n Type, Thermal 500 C.

Sample 4T7
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample 4T7
n Type Silicon
Gate negative

-[LOG] CURRENT [LOG][AMPS]]

SQRT VOLTAGE [SQRT[VOLTS]]
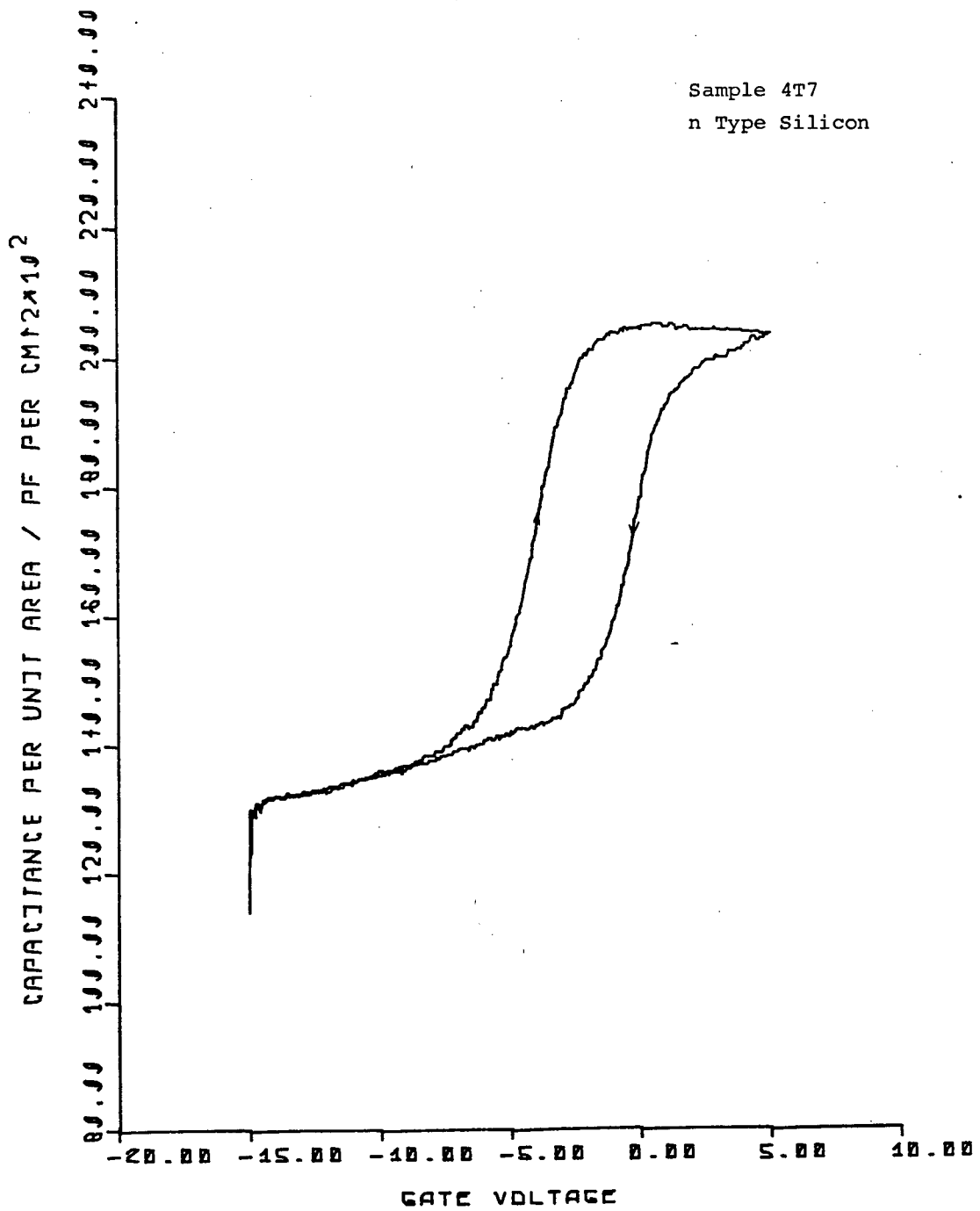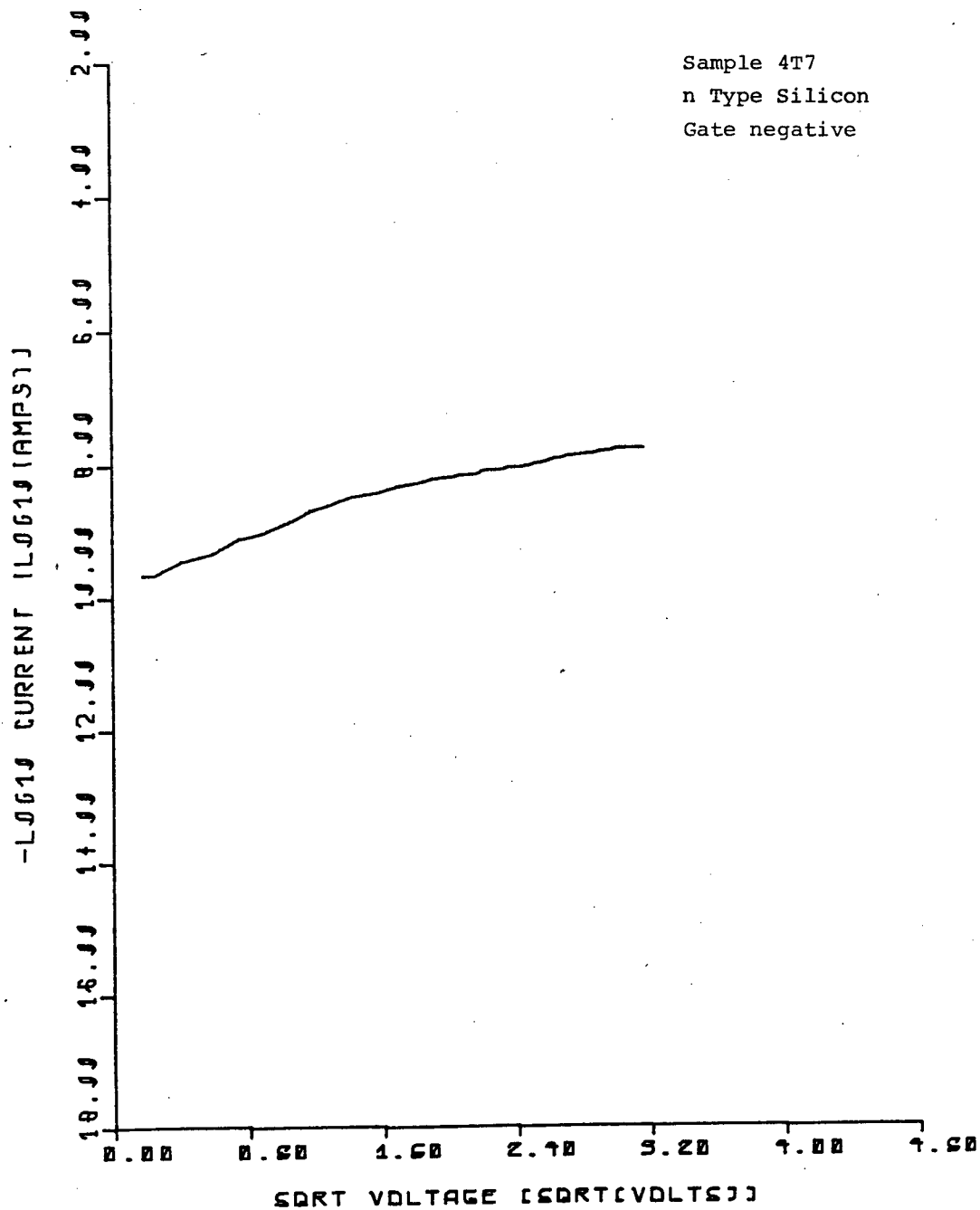
SAMPLE N1, SINGLE DIELECTRIC

n Type, Thermal 500 C.
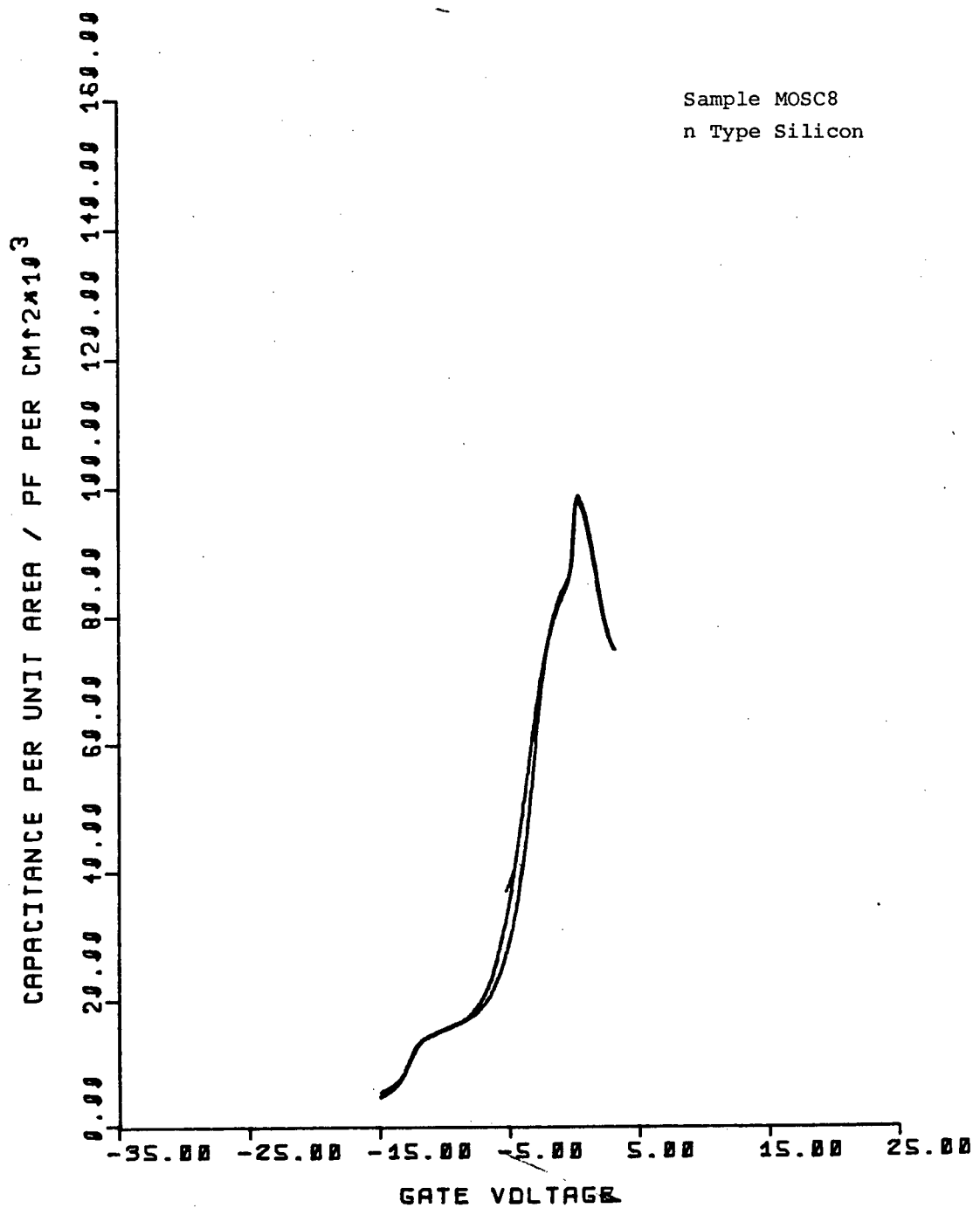
SCHOTTKY IV PLOT

Sample N1
n Type Silicon
Gate negative
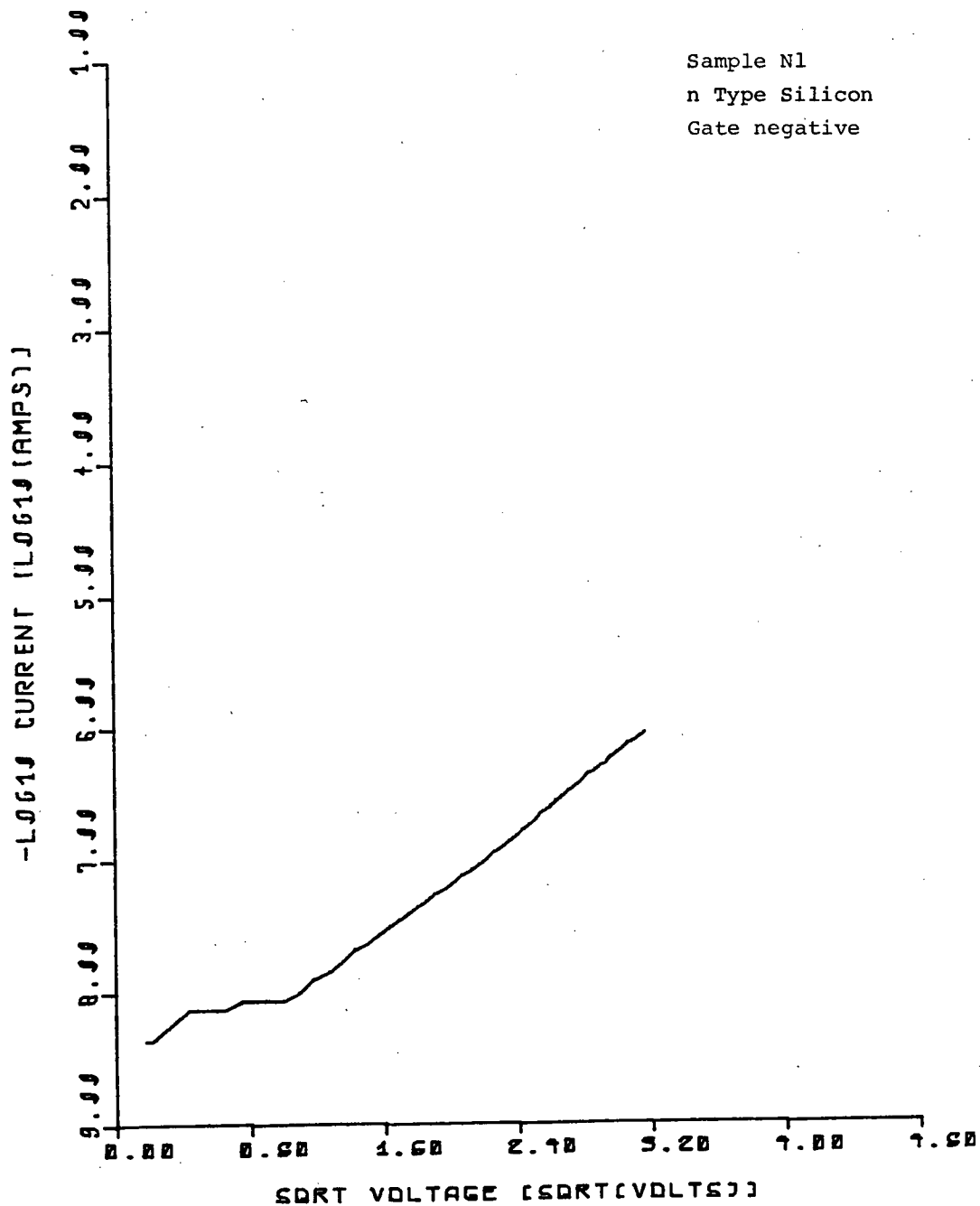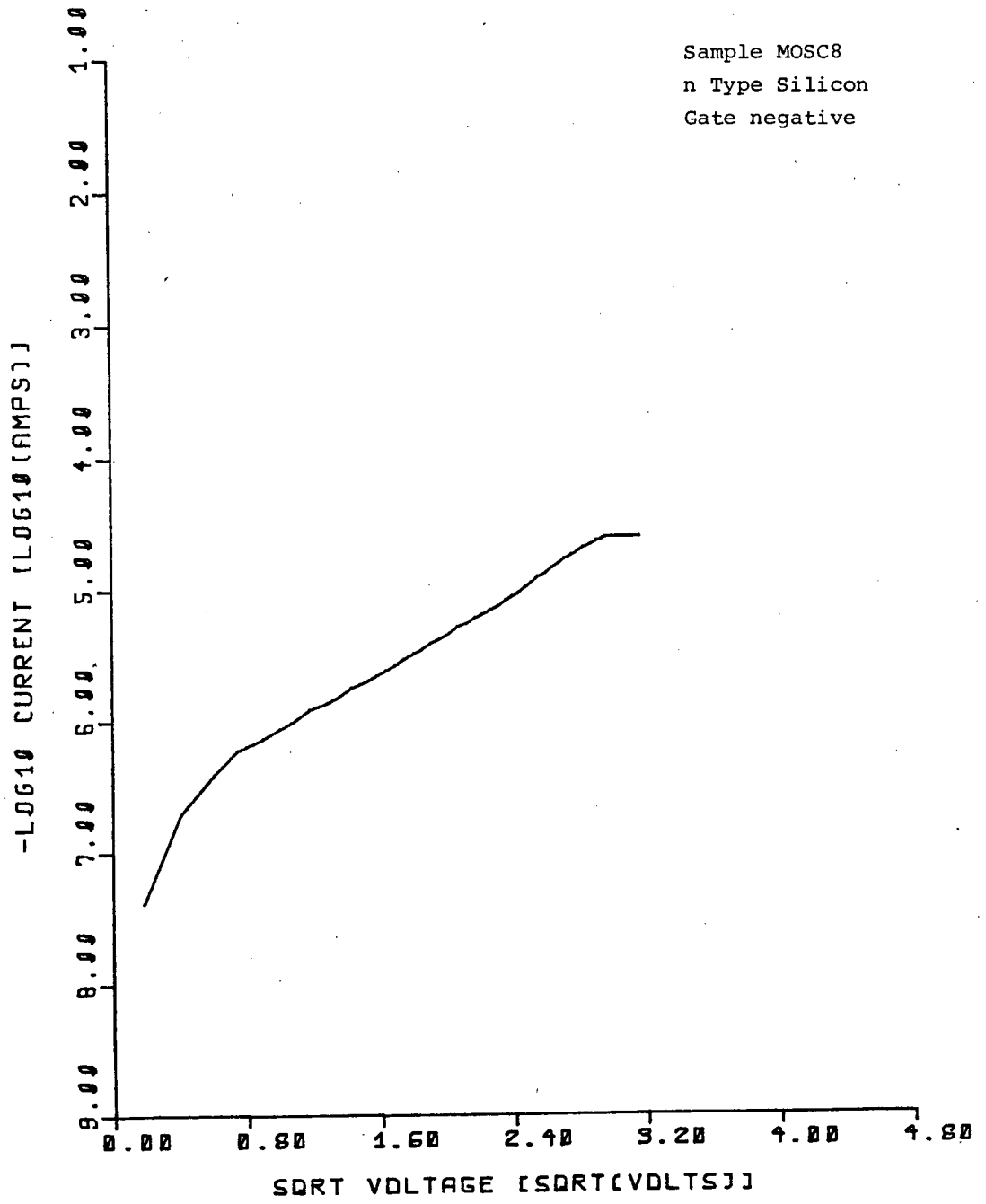
SAMPLE S7, SINGLE DIELECTRIC

n Type, Thermal 500 C.

SCHOTTKY IV PLOT

Sample S7
n Type Silicon
Gate negative

Figure: Plot of -LOG10 CURRENT [LOG10(AMPS)] versus SQRT VOLTAGE [SQRT(VOLTS)]
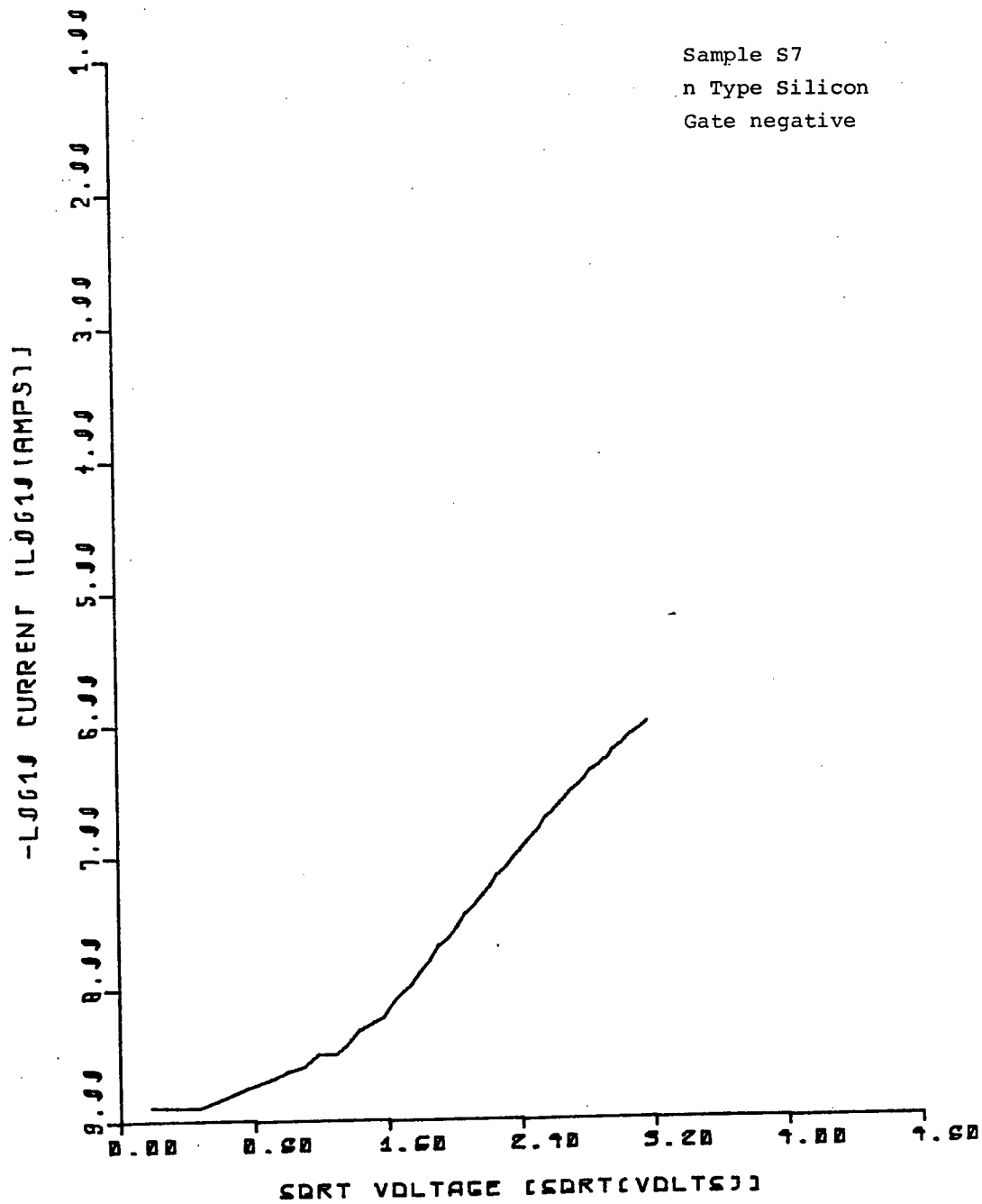
SAMPLE BNR500, SINGLE DIELECTRIC

p Type, Thermal 500 C.

Sample BNR500
p Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
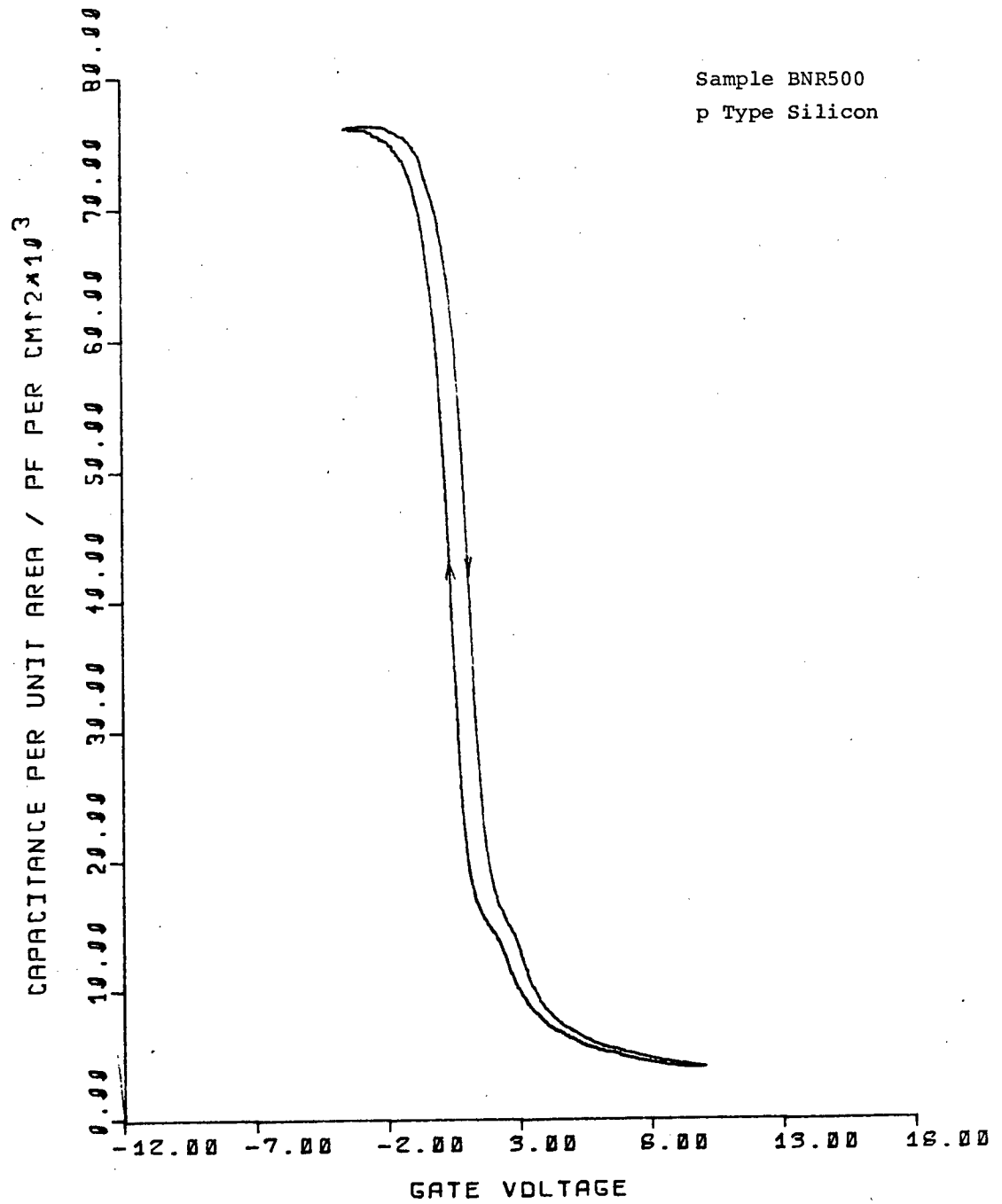
SCHOTTKY IV PLOT

Sample BNR500
p Type Silicon
Gate positive

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]
0.80, 1.60, 2.40, 3.20, 4.00, 4.80, 5.60, 6.40, 7.20

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
0.00, 0.80, 1.60, 2.40, 3.20, 4.00, 4.80
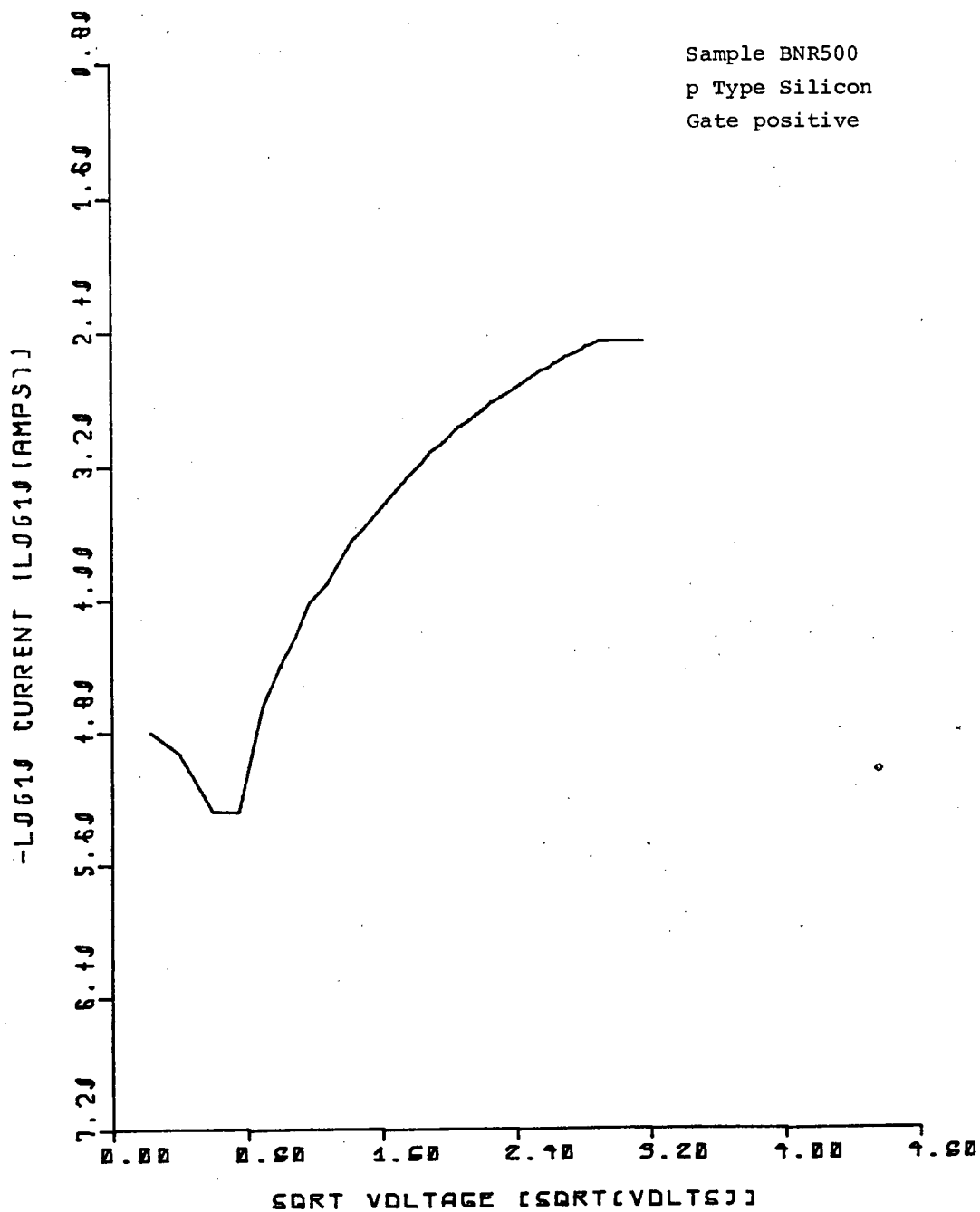
SAMPLE BNR1000, SINGLE DIELECTRIC

p Type, Thermal 500 C.

CAPACITANCE PER UNIT AREA / PF PER CM↑2*10³

GATE VOLTAGE

Sample BNR1000
p Type Silicon

SCHOTTKY IV PLOT

Sample BNR1000
p Type Silicon
Gate positive

SCHOTTKY IV PLOT — Sample BNR1000, p Type Silicon, Gate positive. Y-axis: -LOG10 CURRENT [LOG10(AMPS)]. X-axis: SQRT VOLTAGE [SQRT(VOLTS)]
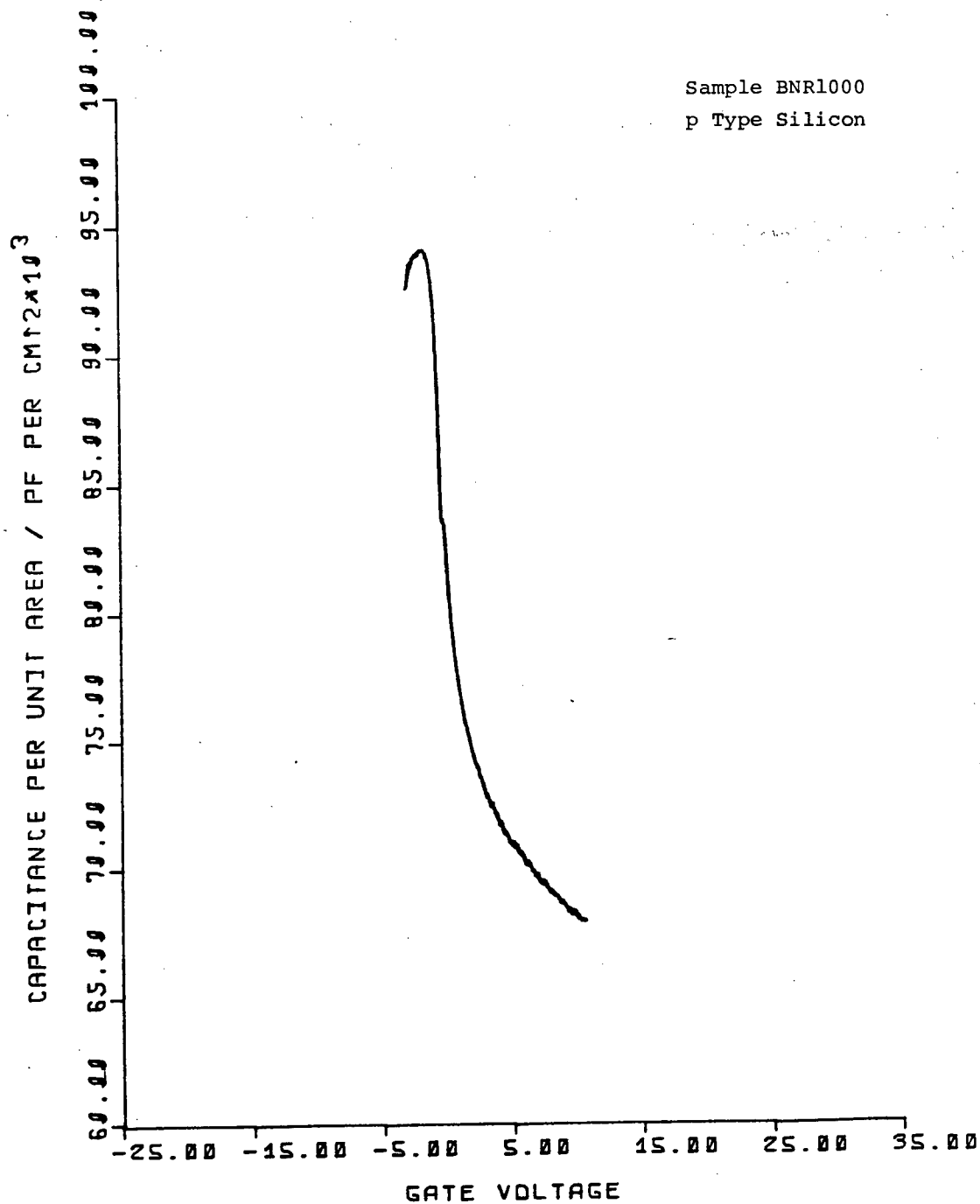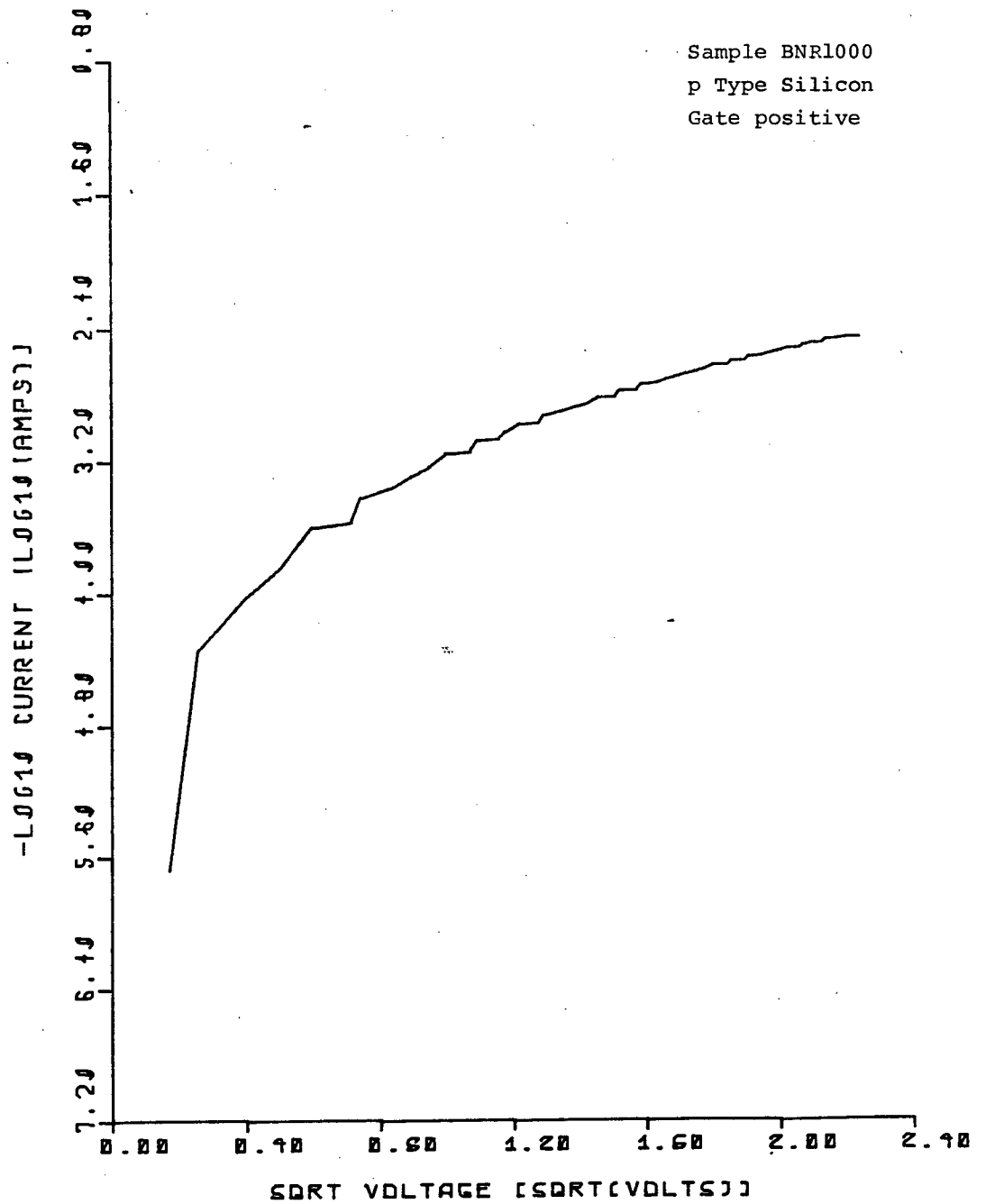
SAMPLE SampleA, SINGLE DIELECTRIC

p Type, Thermal 500 C.

Sample SAMPLEA
p Type Silicon

SCHOTTKY IV PLOT

Sample SAMPLEA
p Type Silicon
Gate positive
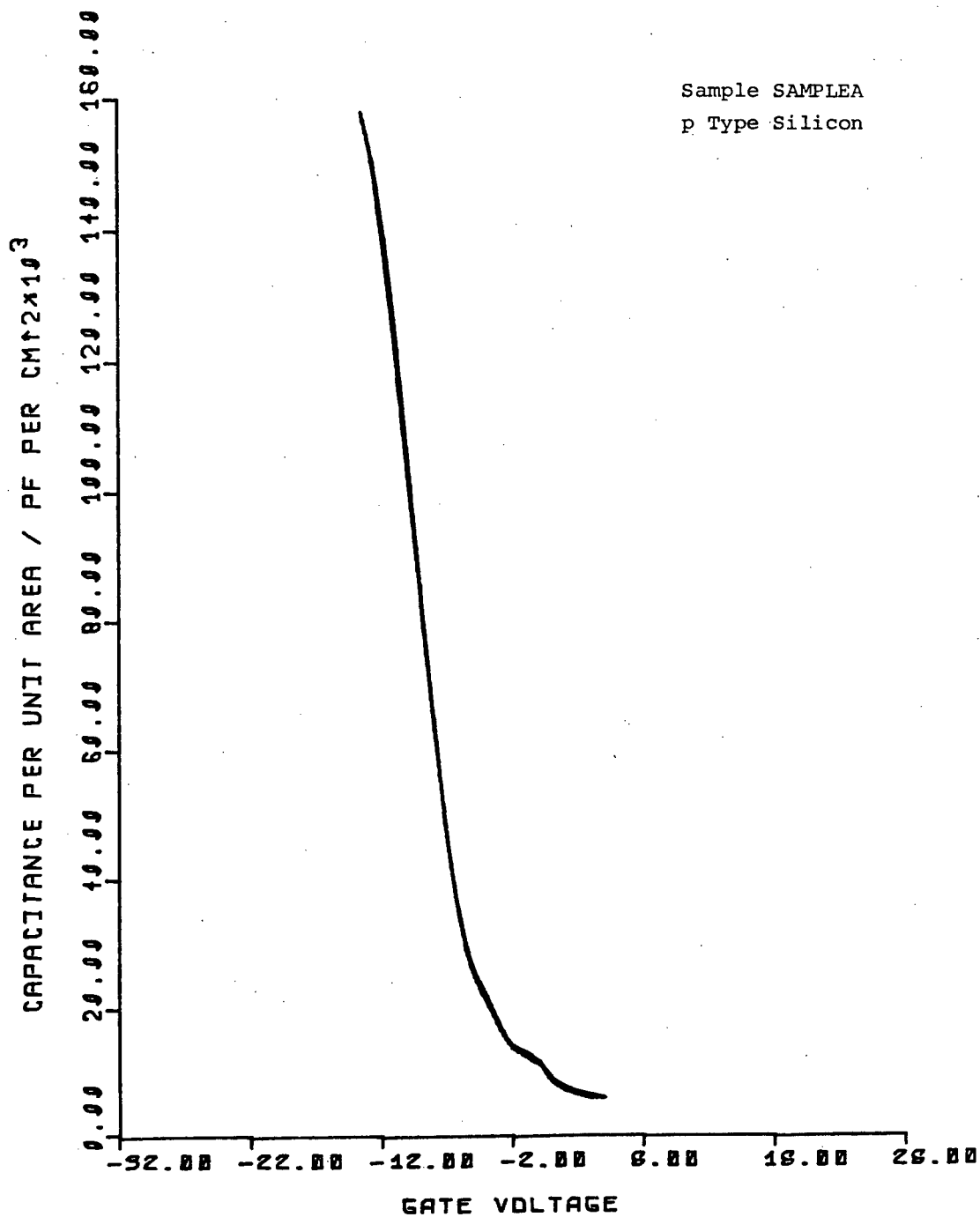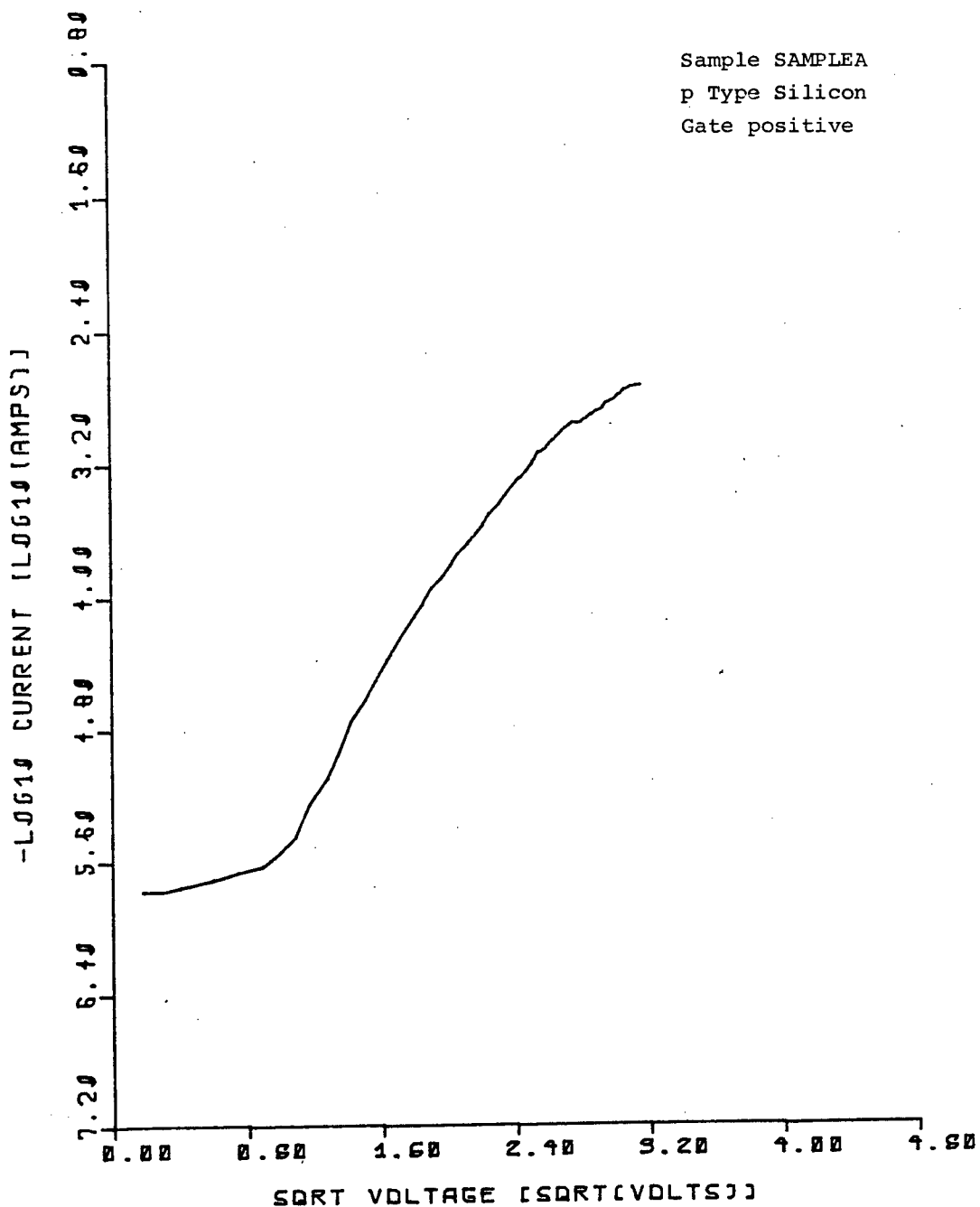
SAMPLE SampleB, SINGLE DIELECTRIC

p Type, Thermal 500 C.

Sample SAMPLEB
p Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2*10²

GATE VOLTAGE
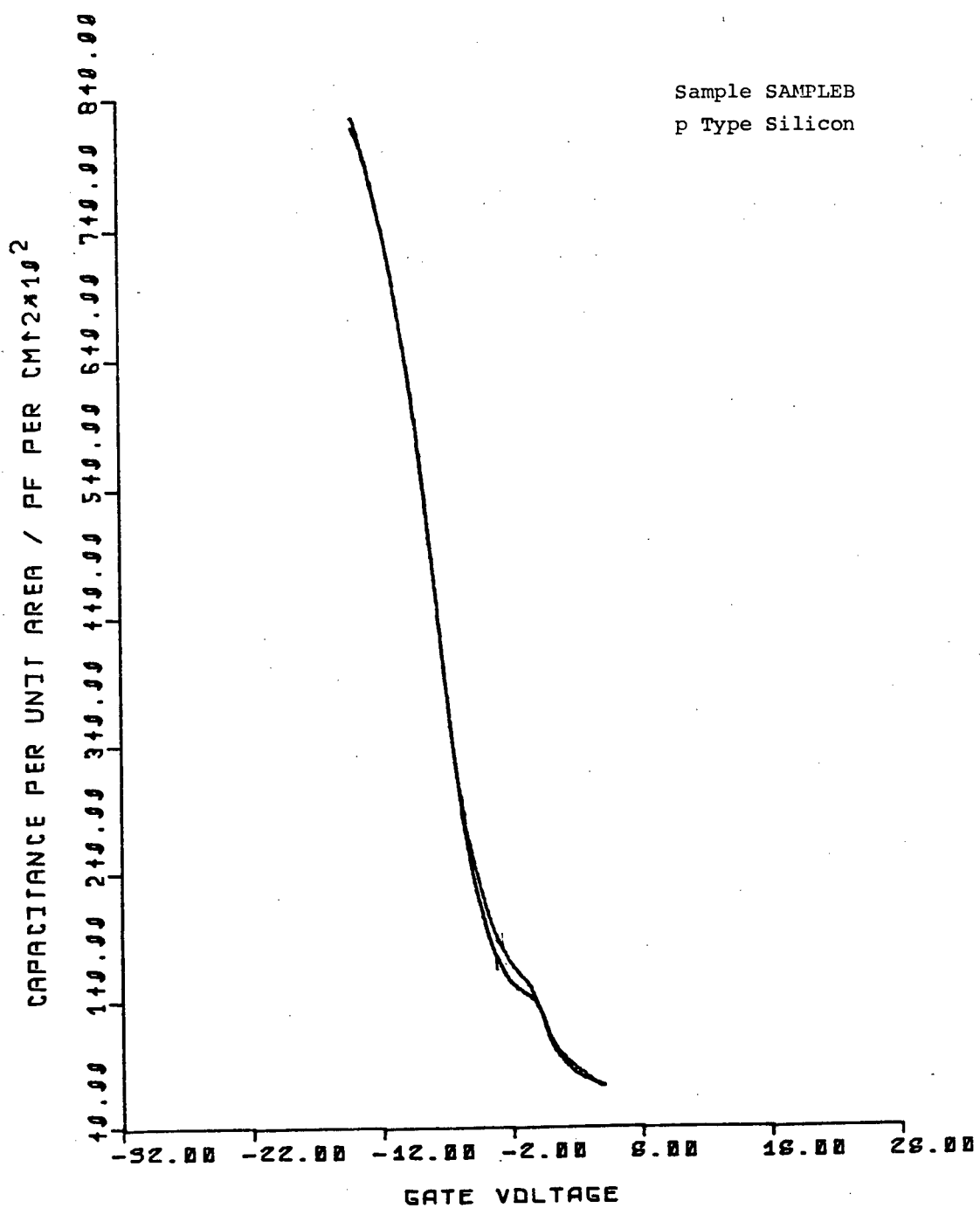
SCHOTTKY IV PLOT

Sample SAMPLEB
p Type Silicon
Gate positive

-LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT[VOLTS]]
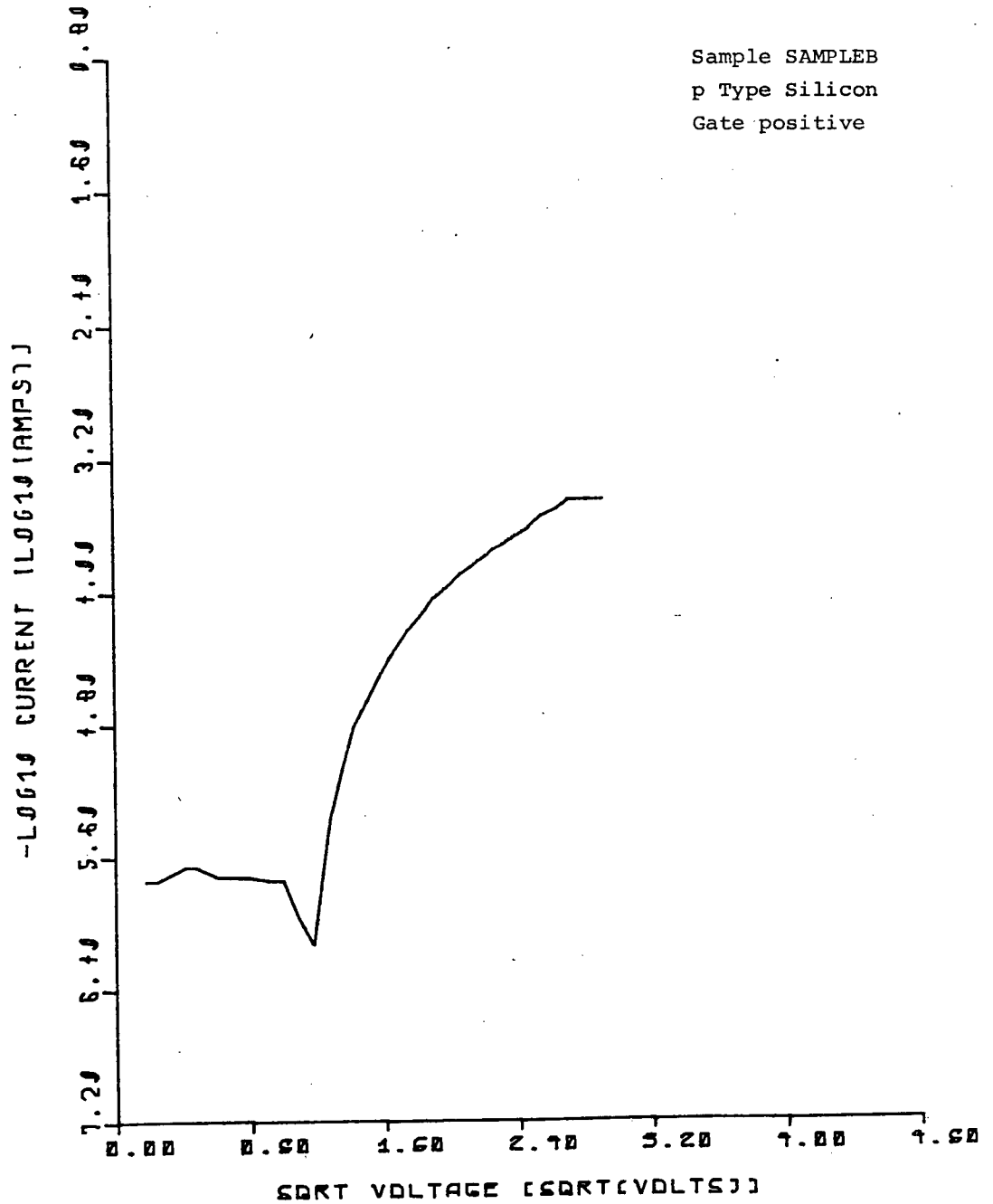
SAMPLE 1000AMOS, SINGLE DIELECTRIC

n Type, Thermal 500 C.

Sample 1000AMOS
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
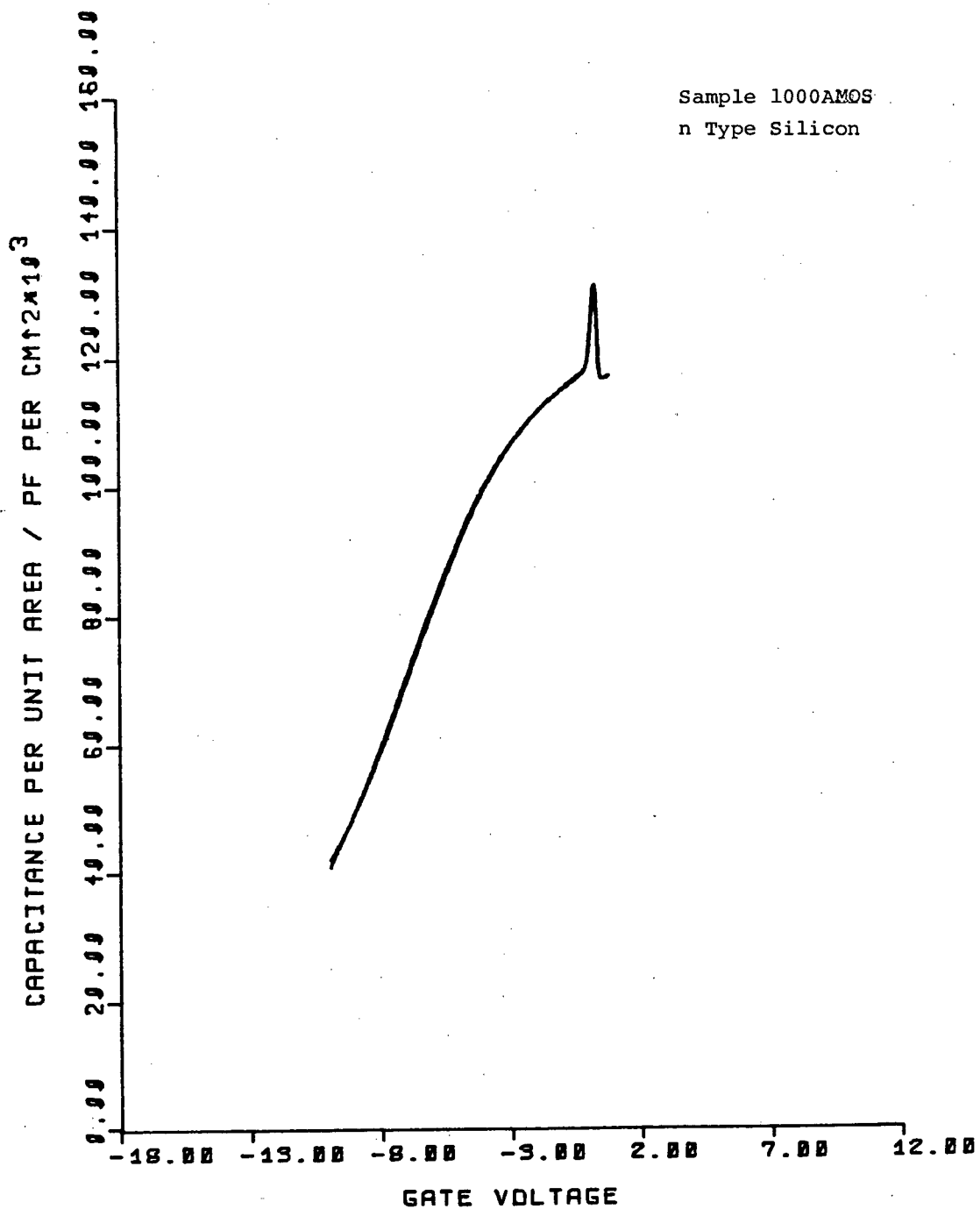
SCHOTTKY IV PLOT

Sample 1000 AMOS
n Type Silicon
Gate negative
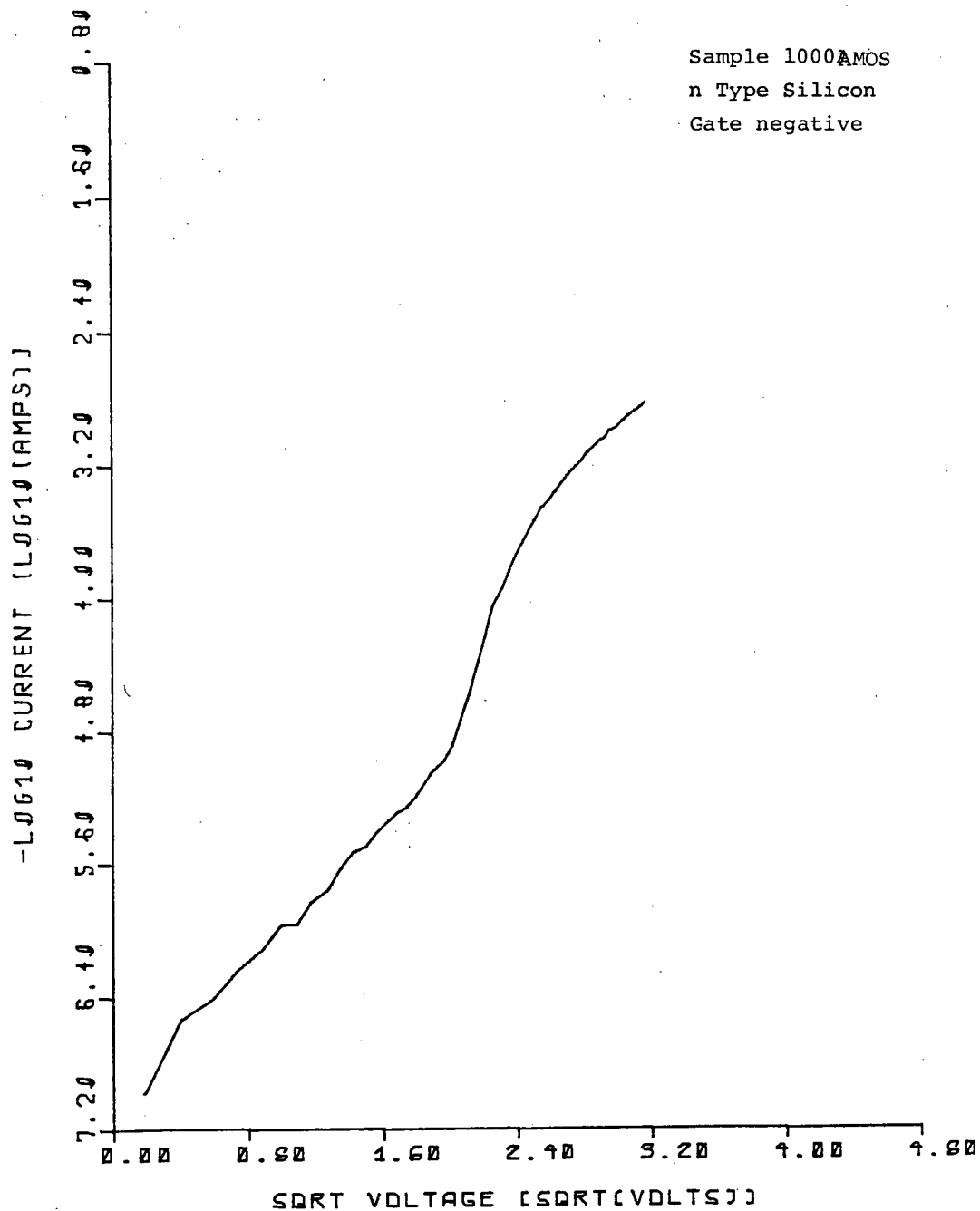
SAMPLE 500ALift, SINGLE DIELECTRIC

p Type, Thermal 500 C.

Sample 500ALift
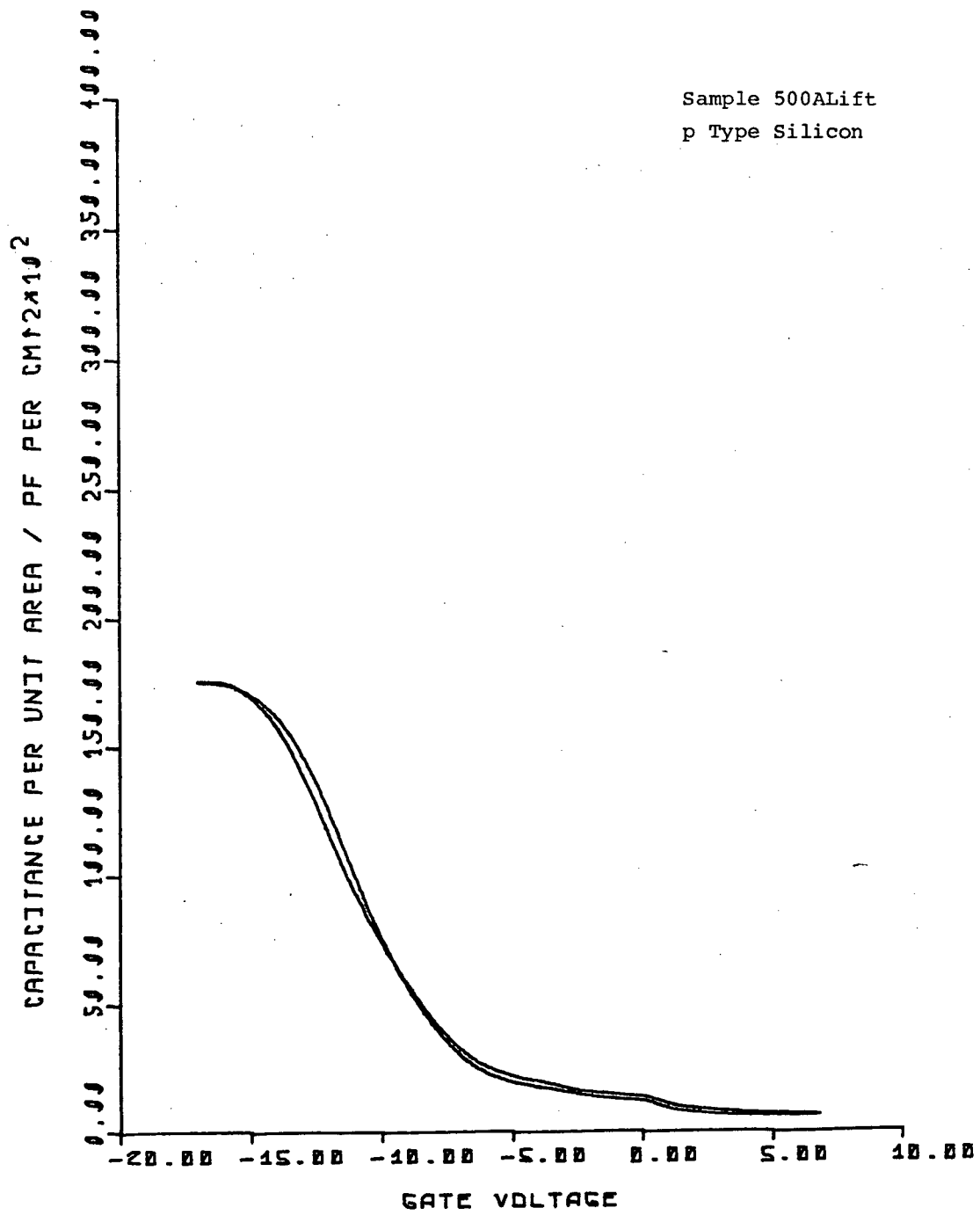
p Type Silicon

SCHOTTKY IV PLOT

Sample 500ALift
p Type Silicon
Gate positive

Axes of plot:
- Vertical axis: -LOG10 CURRENT [LOG10(AMPS)]
- Horizontal axis: SQRT VOLTAGE [SQRT(VOLTS)]
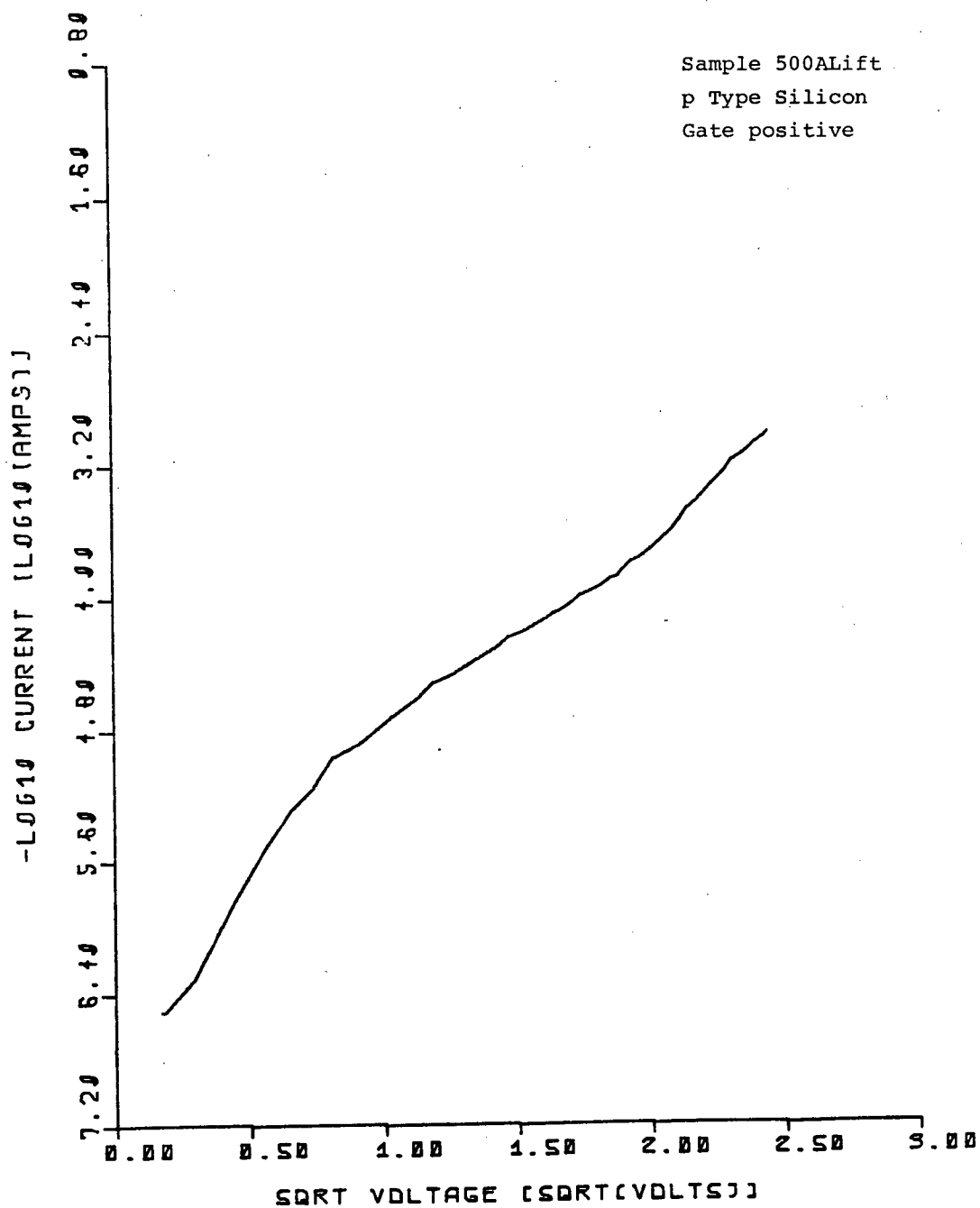
SAMPLE 1000ALift, SINGLE DIELECTRIC

p Type, Thermal 500 C.

SCHOTTKY IV PLOT

Sample 100ALift
n Type Silicon
Gate negative
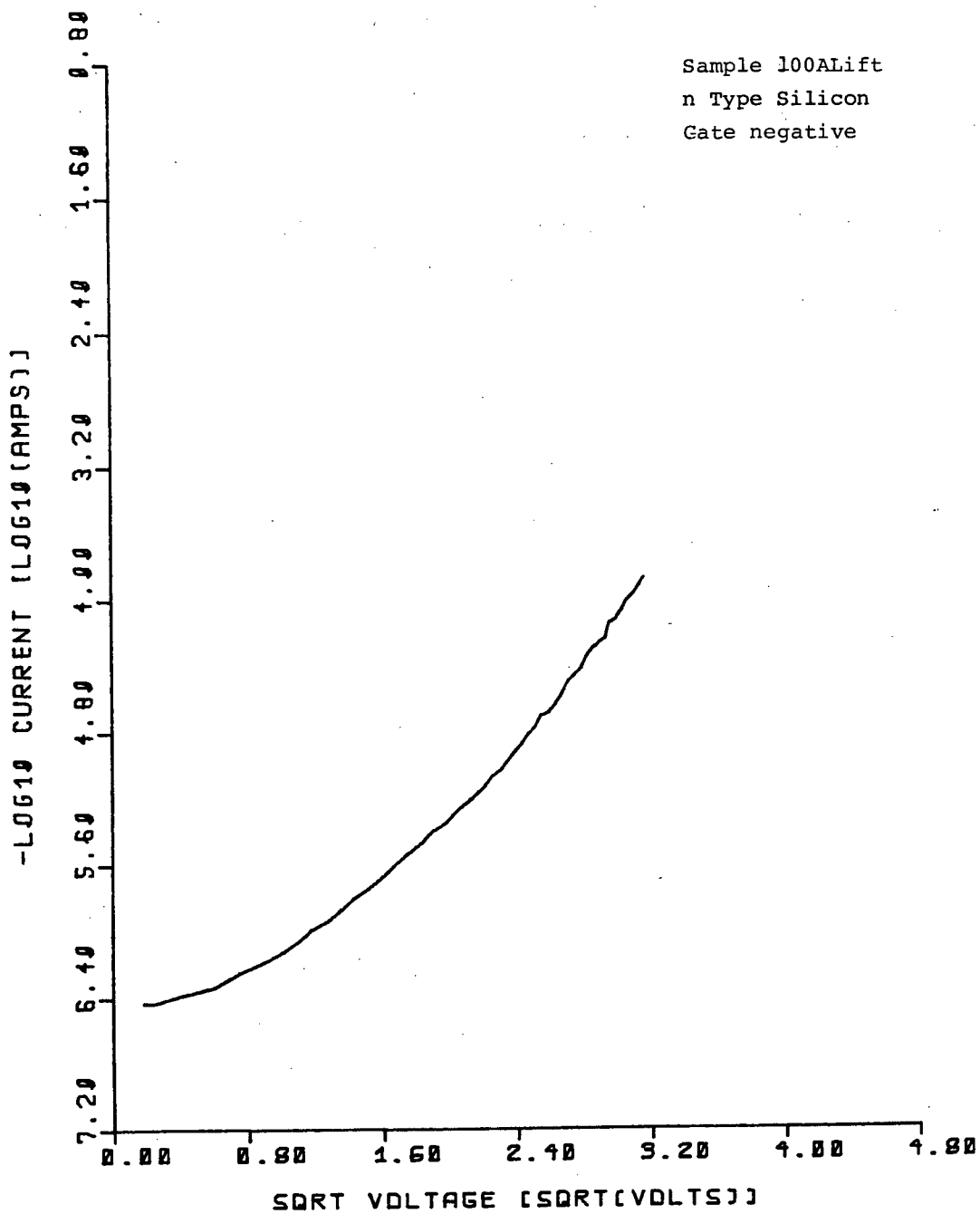
SAMPLE MOSC 6, SINGLE DIELECTRIC

n Type, Thermal 600 C.

Sample MOSC6
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

160.00 · 140.00 · 120.00 · 100.00 · 80.00 · 60.00 · 40.00 · 20.00 · 0.00

-32.00   -22.00   -12.00   -2.00   8.00   18.00   28.00

GATE VOLTAGE

SCHOTTKY IV PLOT
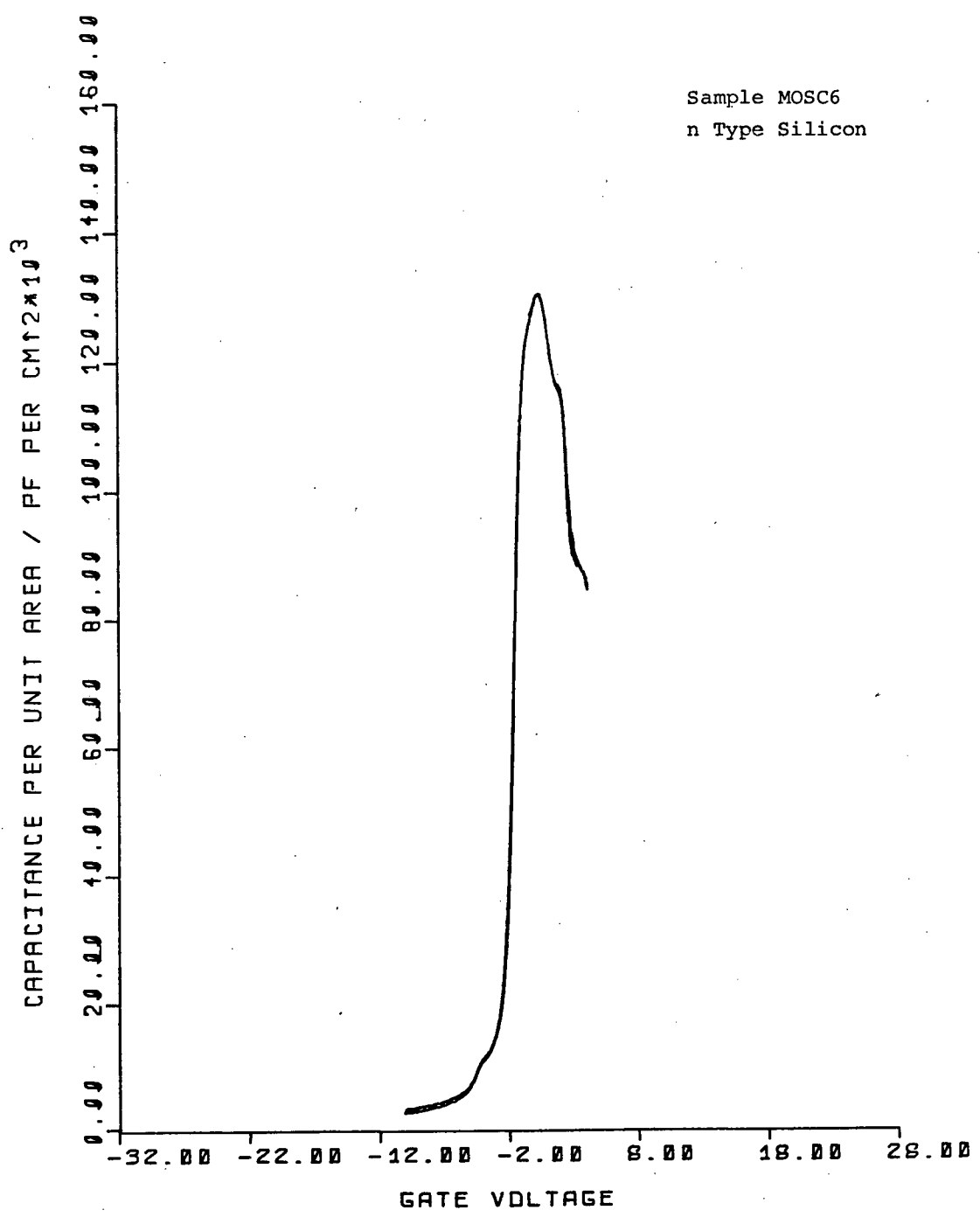
Sample MOSC6
n Type Silicon
Gate negative
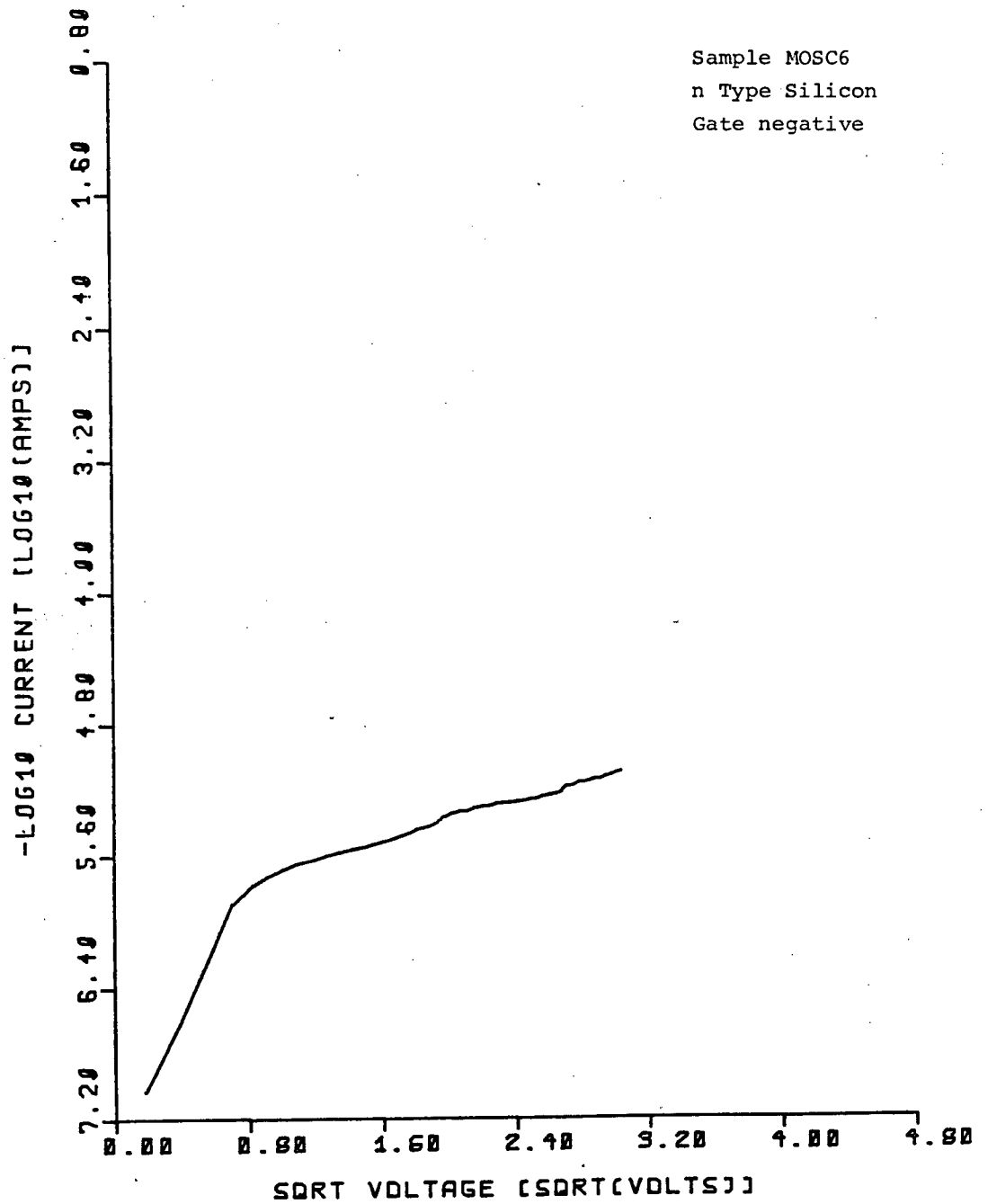
SAMPLE MOSC7, SINGLE DIELECTRIC

n Type, Thermal 400 C.

Sample MOSC7
n Type Silicon
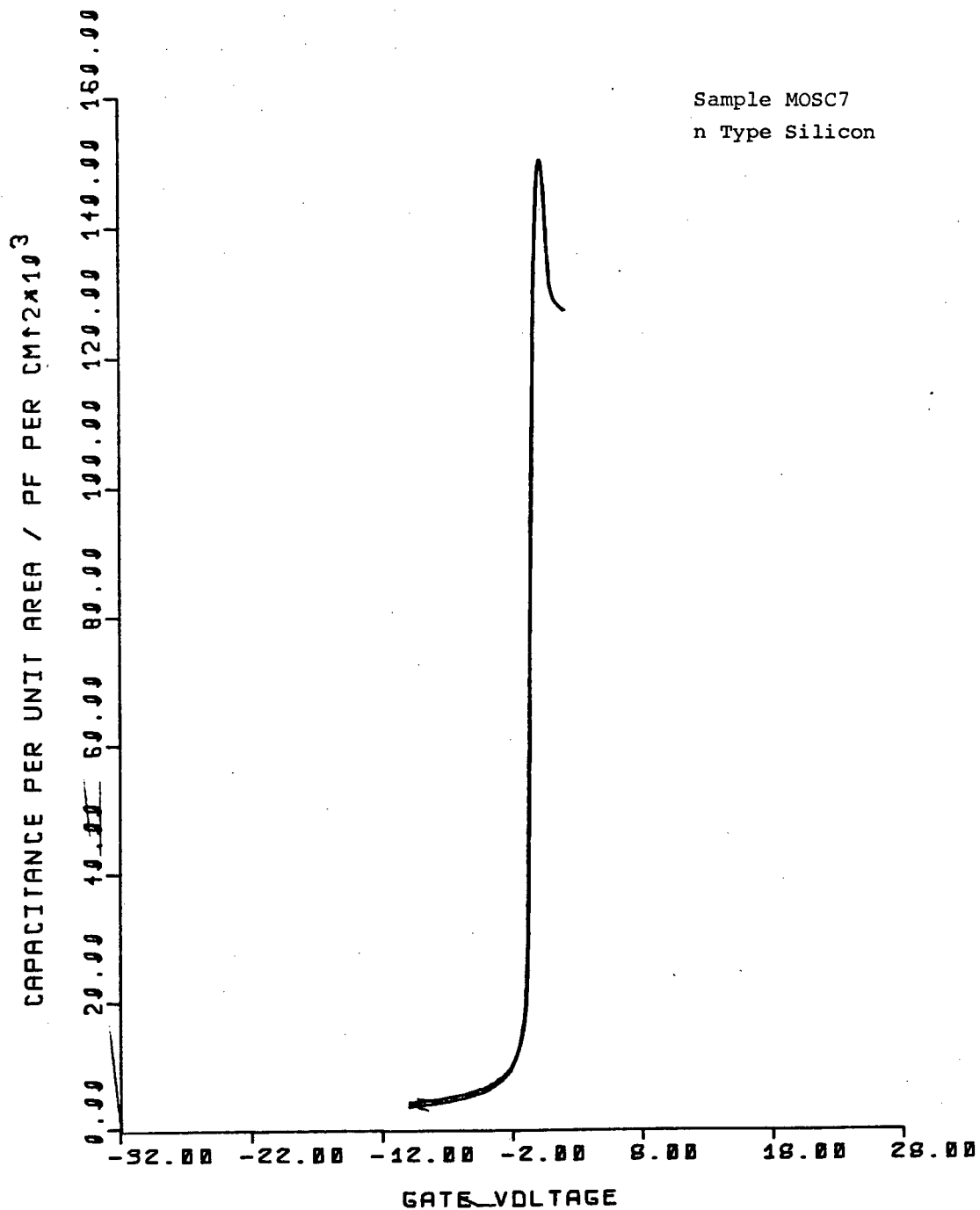
SCHOTTKY IV PLOT

Sample MOSC7
n Type Silicon
Gate negative
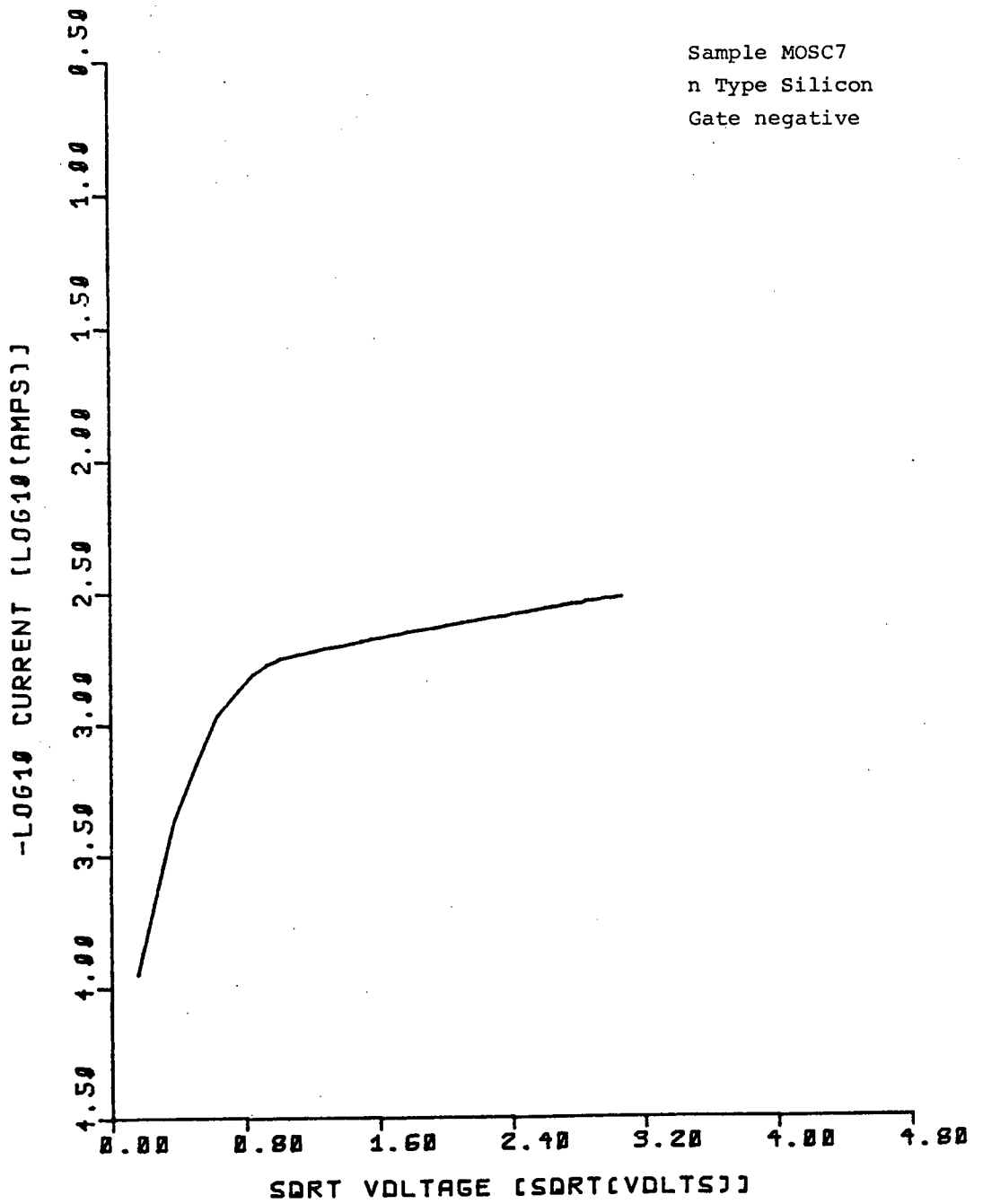
SAMPLE MOSC8, SINGLE DIELECTRIC

n Type, Thermal 600 C.

Sample MOSC8
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample MOSC8
n Type Silicon
Gate negative

-LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT(VOLTS)]

SAMPLE MOSC9, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC9
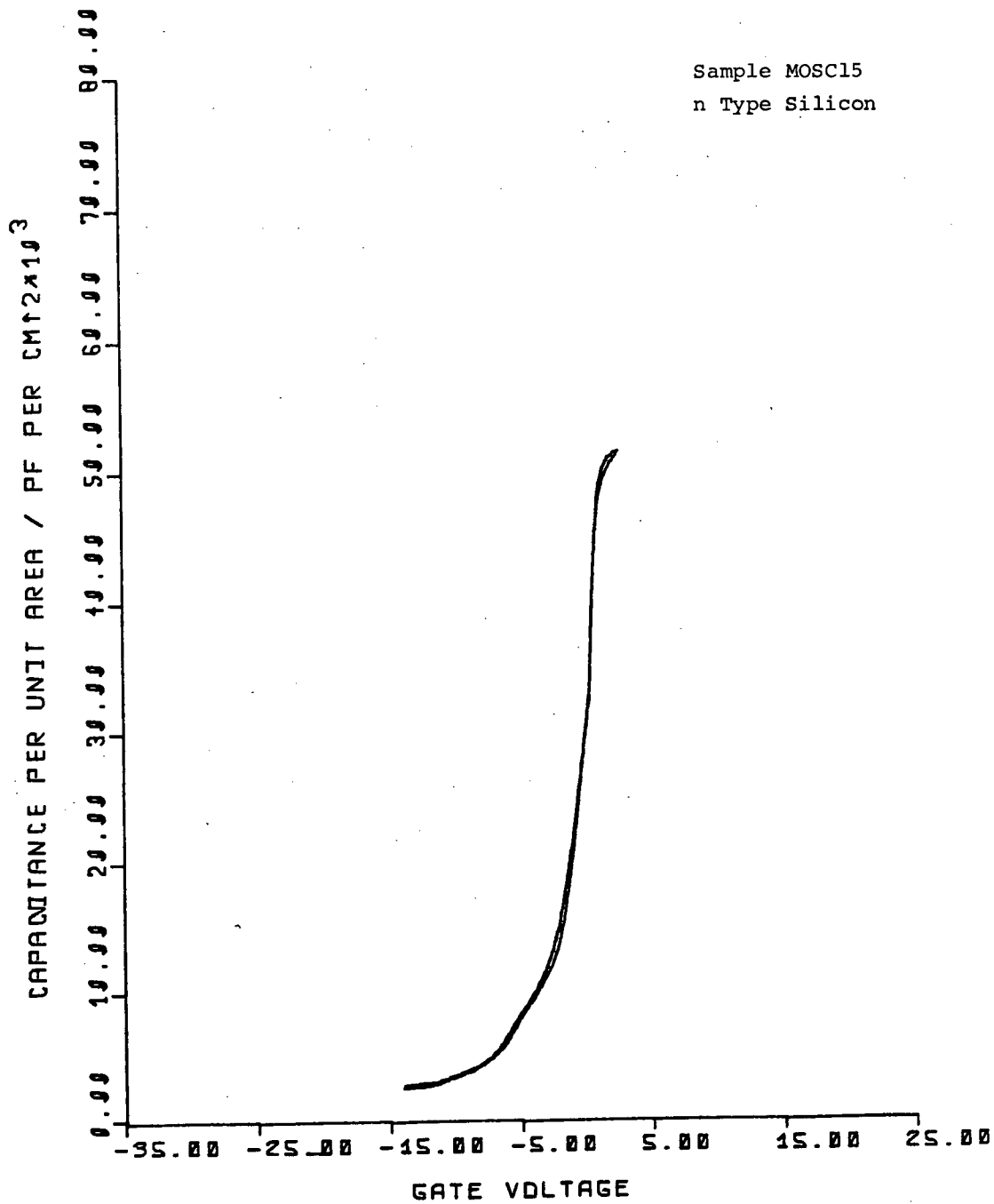n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE
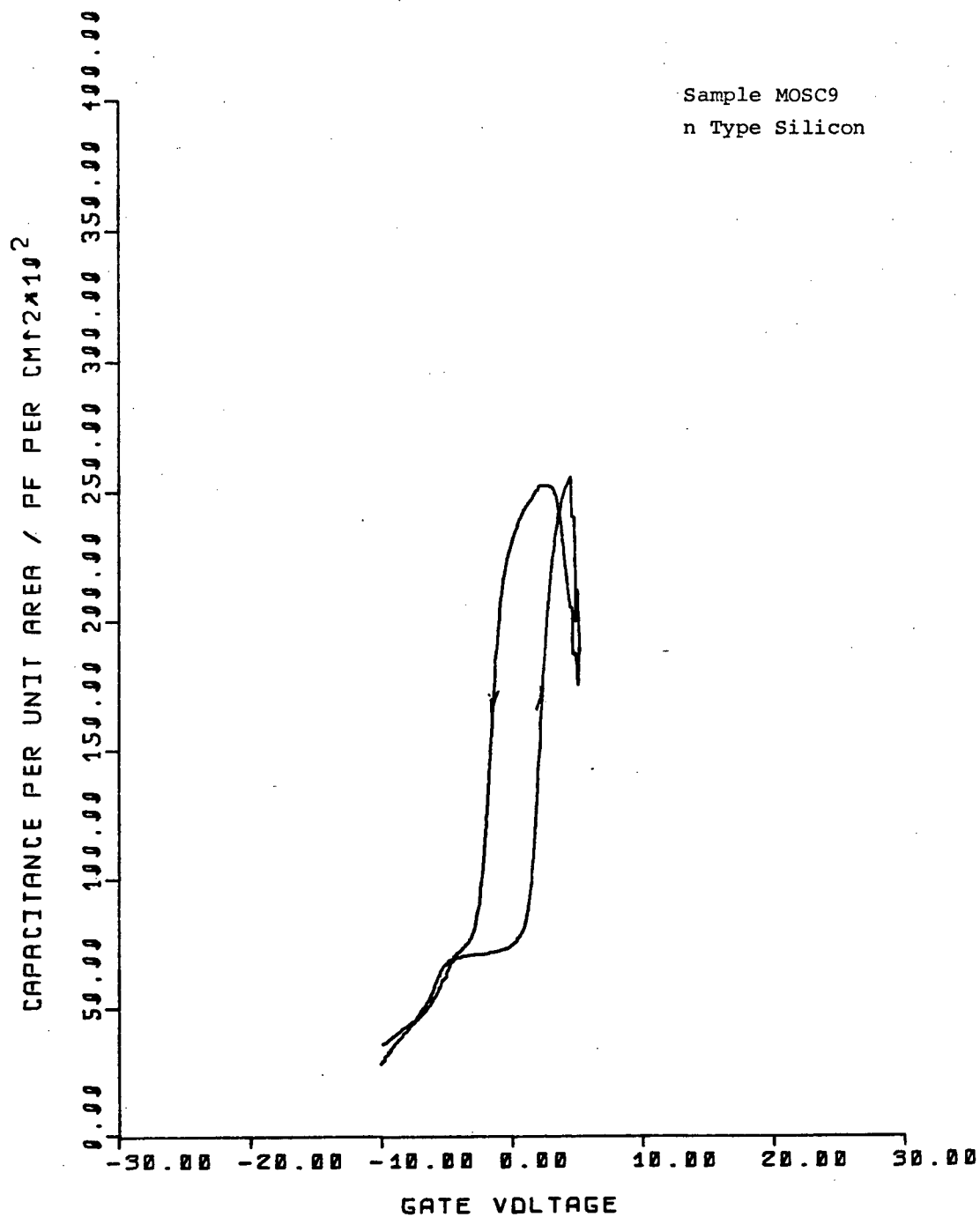
SCHOTTKY IV PLOT

Sample MOSC9
n Type Silicon
Gate negative
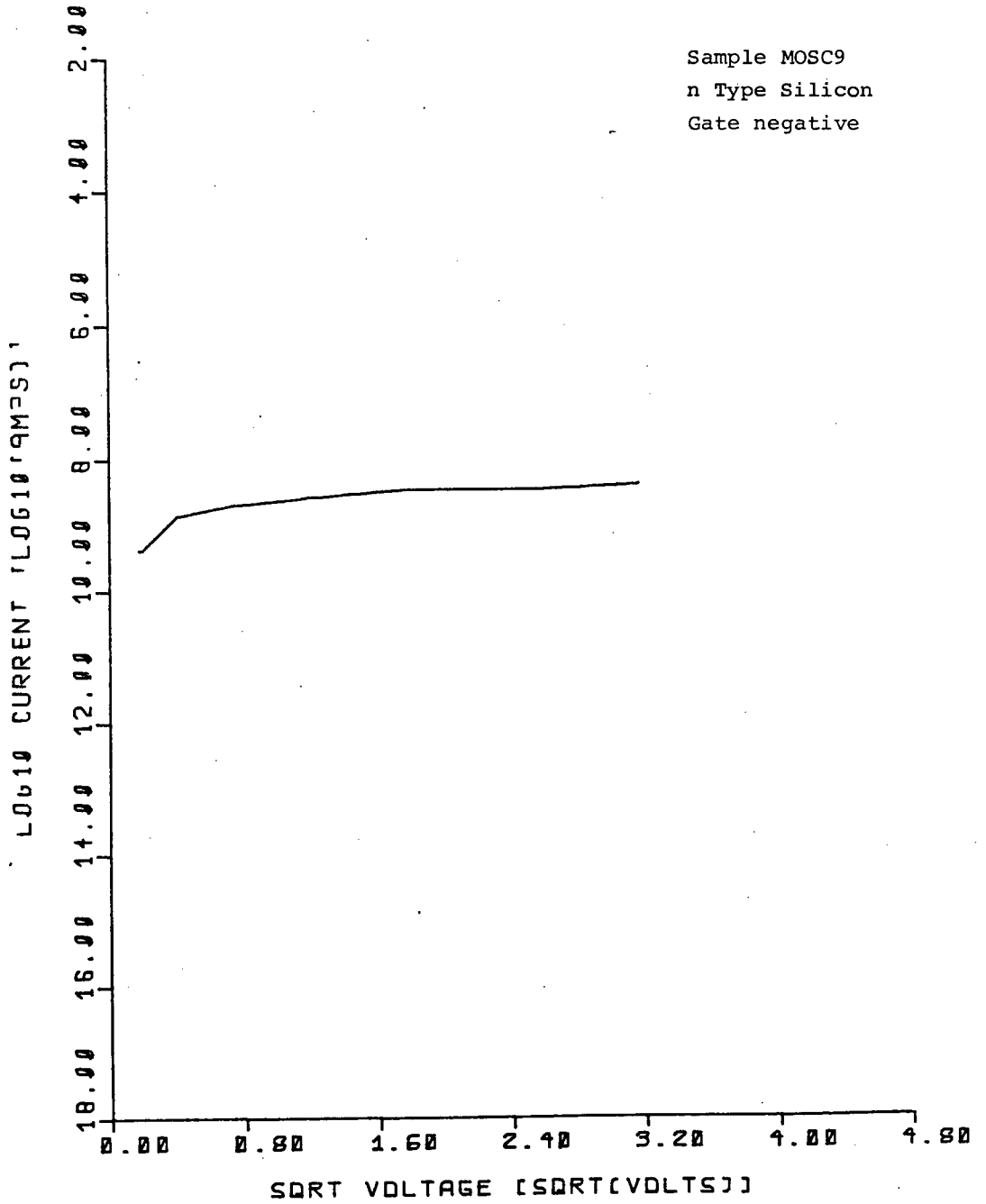
SAMPLE MOSC10, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC10
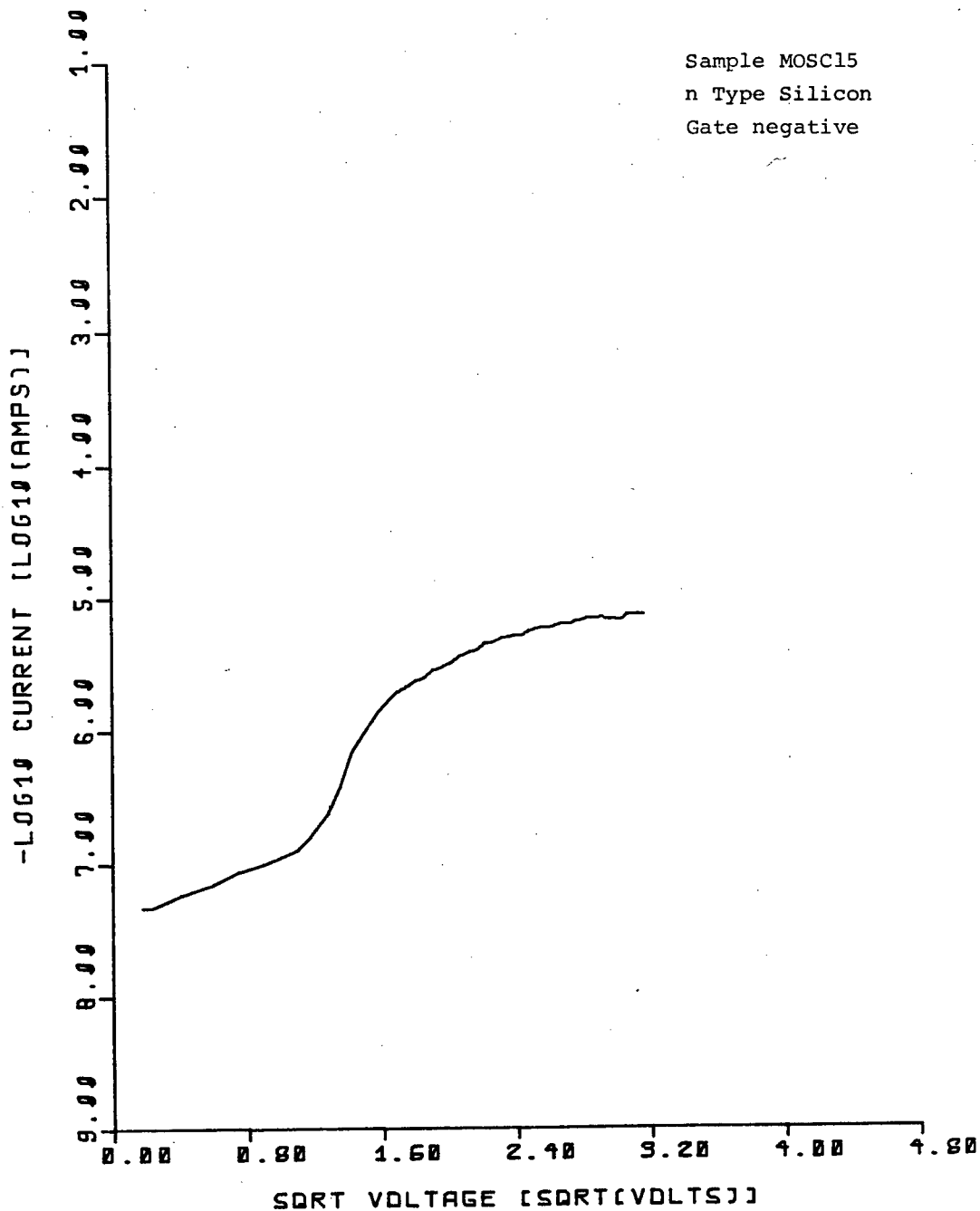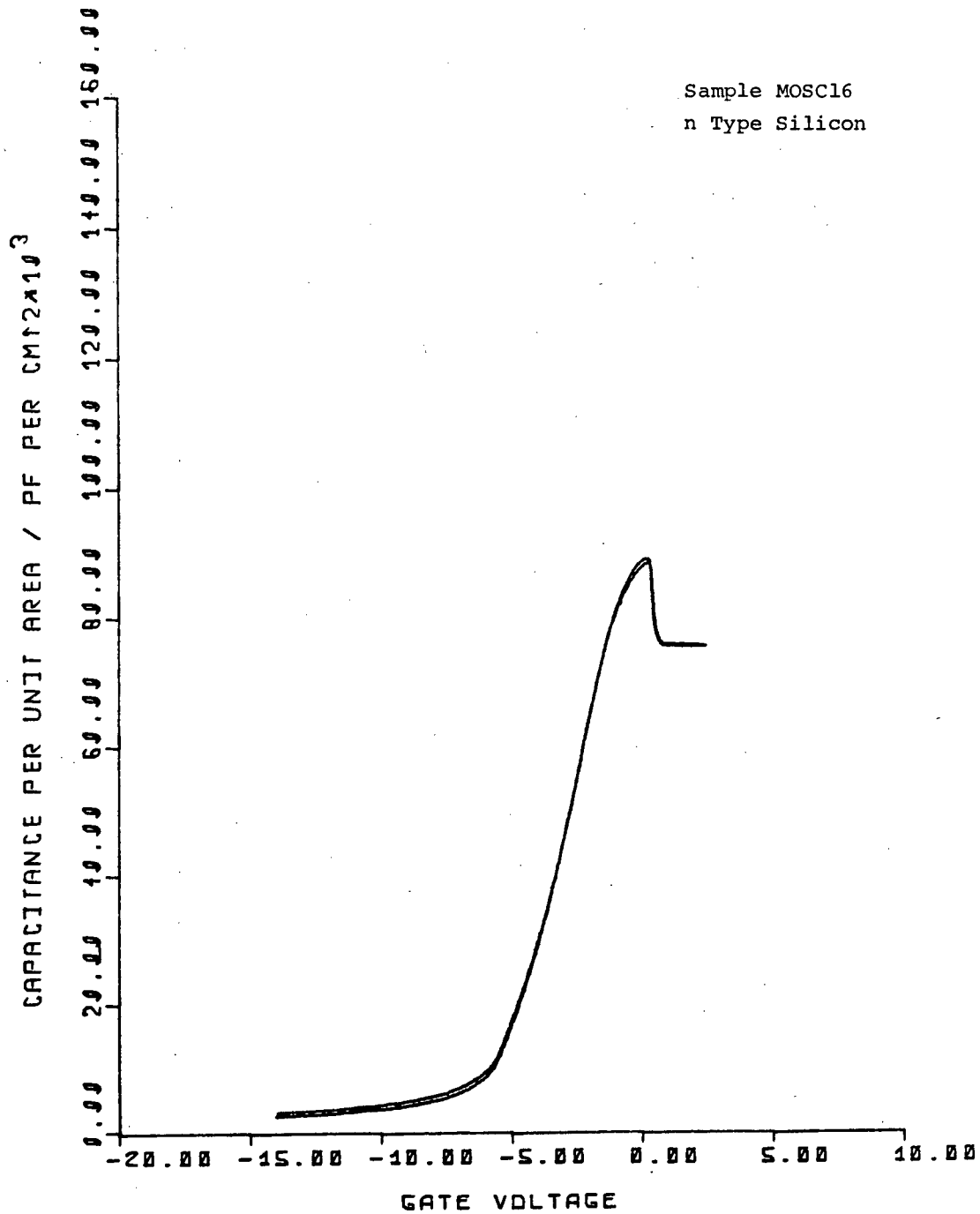n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample MOSC10
n Type Silicon
Gate negative

Y-axis: −LOG10 CURRENT [LOG10(AMPS)]

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
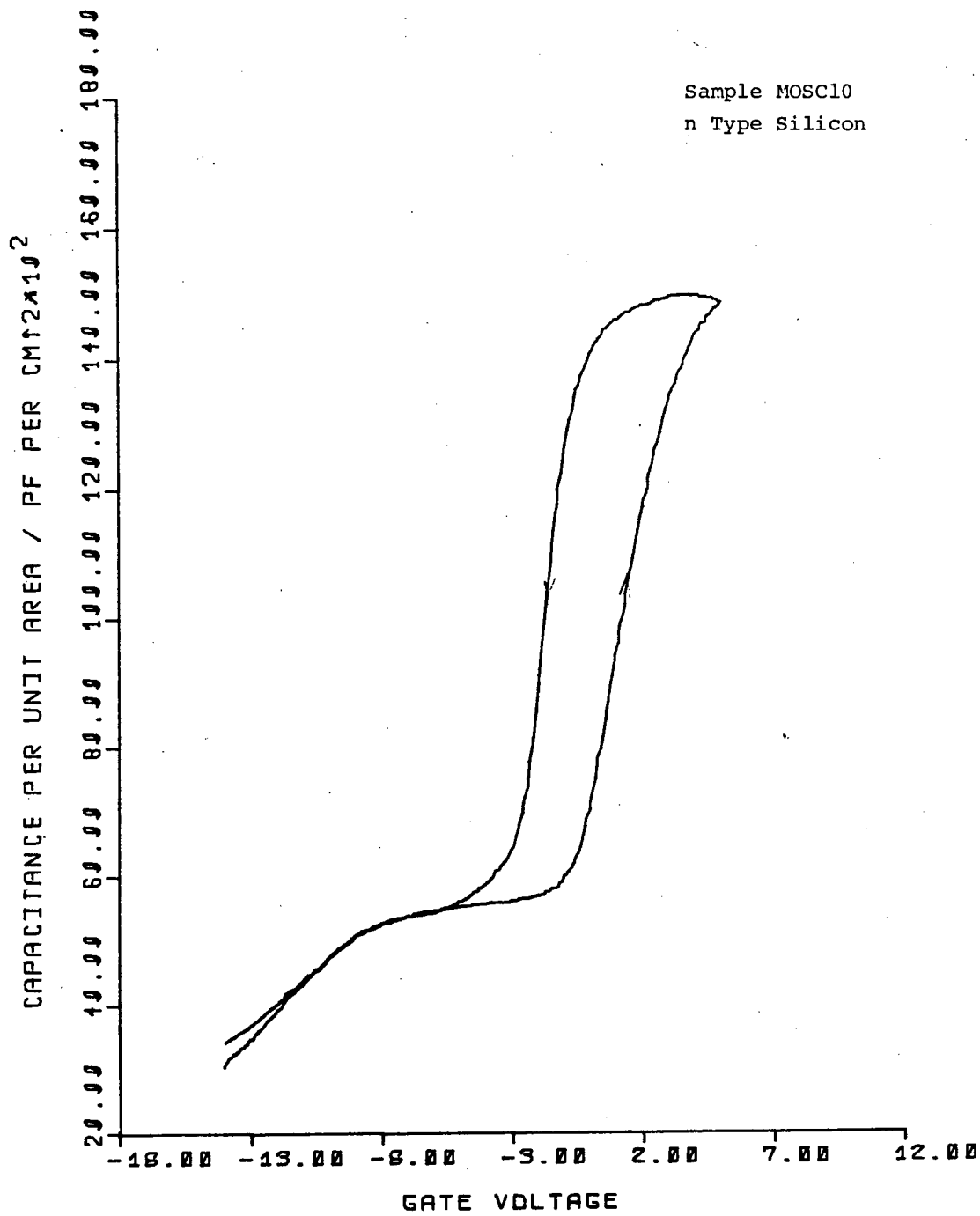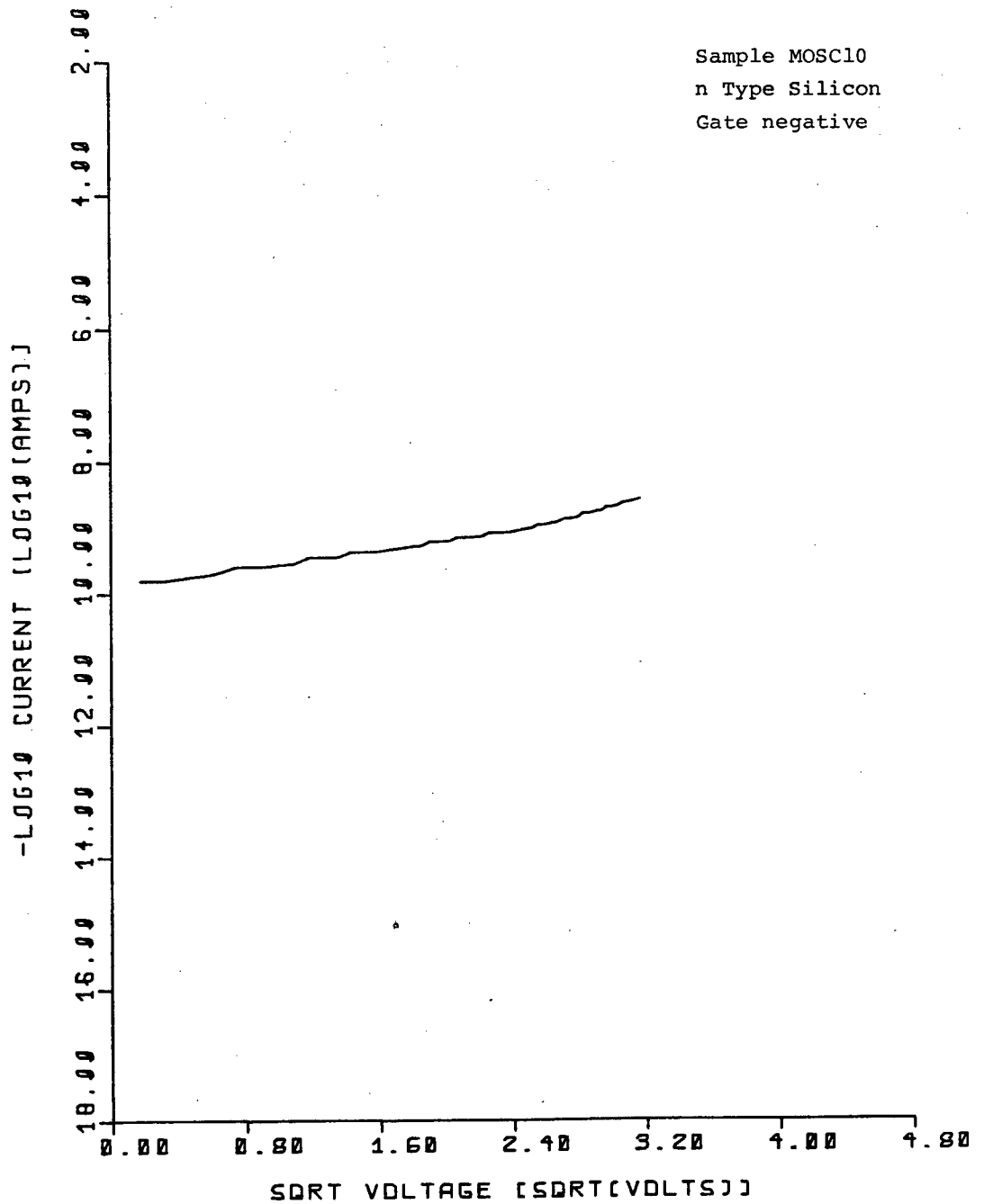
SAMPLE MOSC11, SINGLE DIELECTRIC

n Type, Anodic, Phosphoric Acid.

Sample MOSC11
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
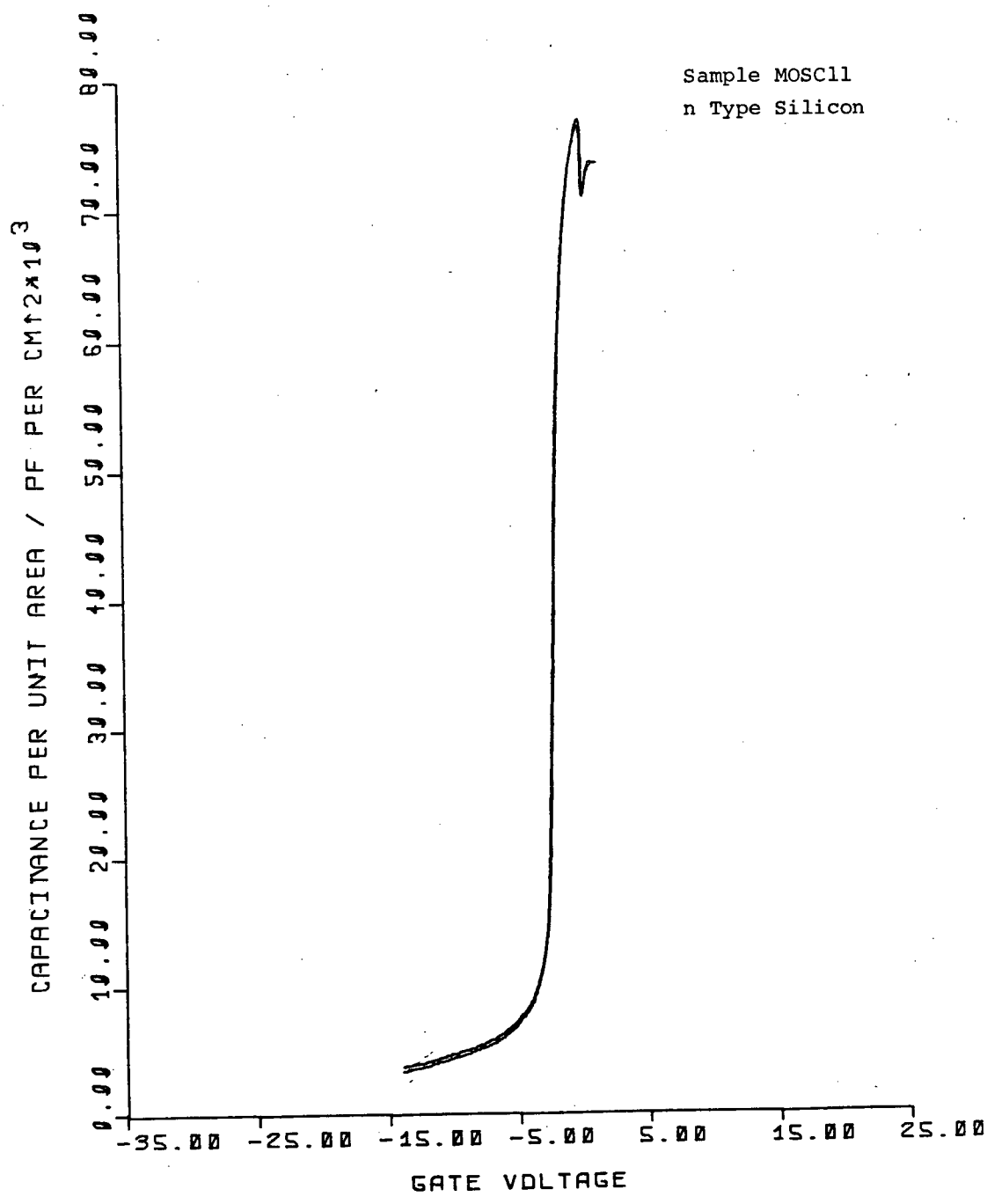
SAMPLE MOSC12, SINGLE DIELECTRIC

n Type, Anodic, Phosphoric Acid.

Sample MOSC12
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
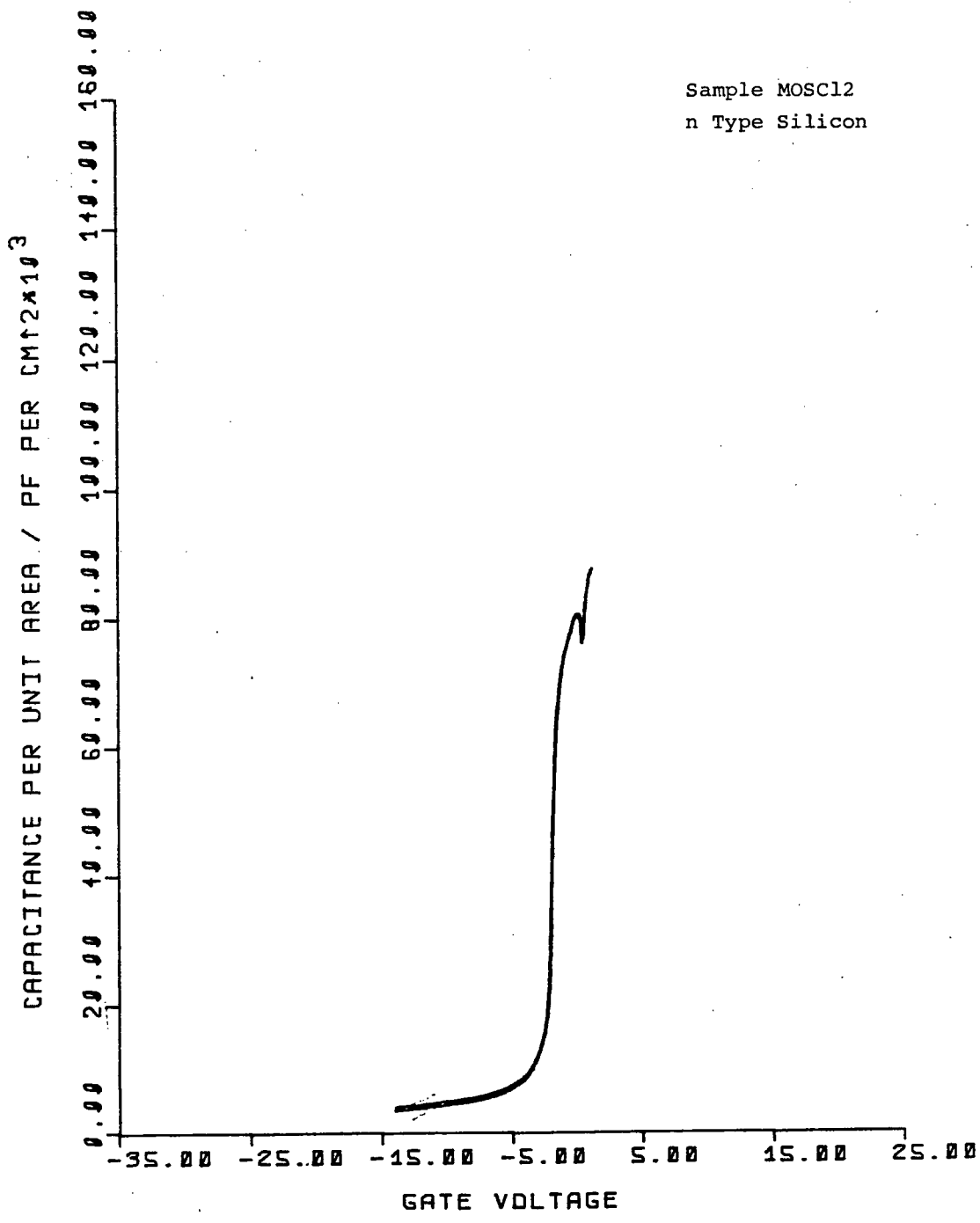
SAMPLE MOSC13, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC13
n Type Silicon
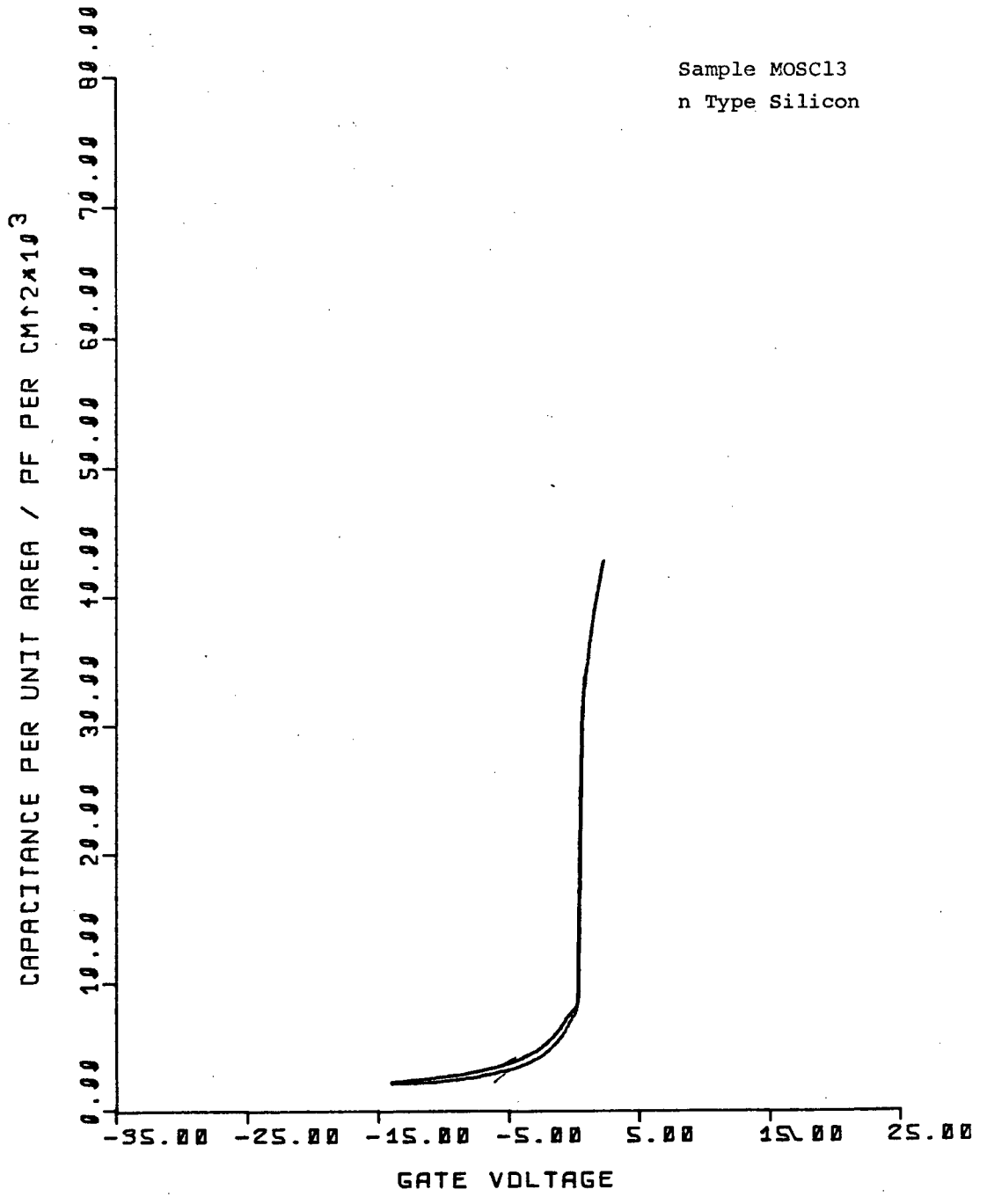
SCHOTTKY IV PLOT

Sample MOSC13
n Type Silicon
Gate negative

Axis labels:
-LOG10 CURRENT [LOG10[AMPS]]
SQRT VOLTAGE [SQRT[VOLTS]]
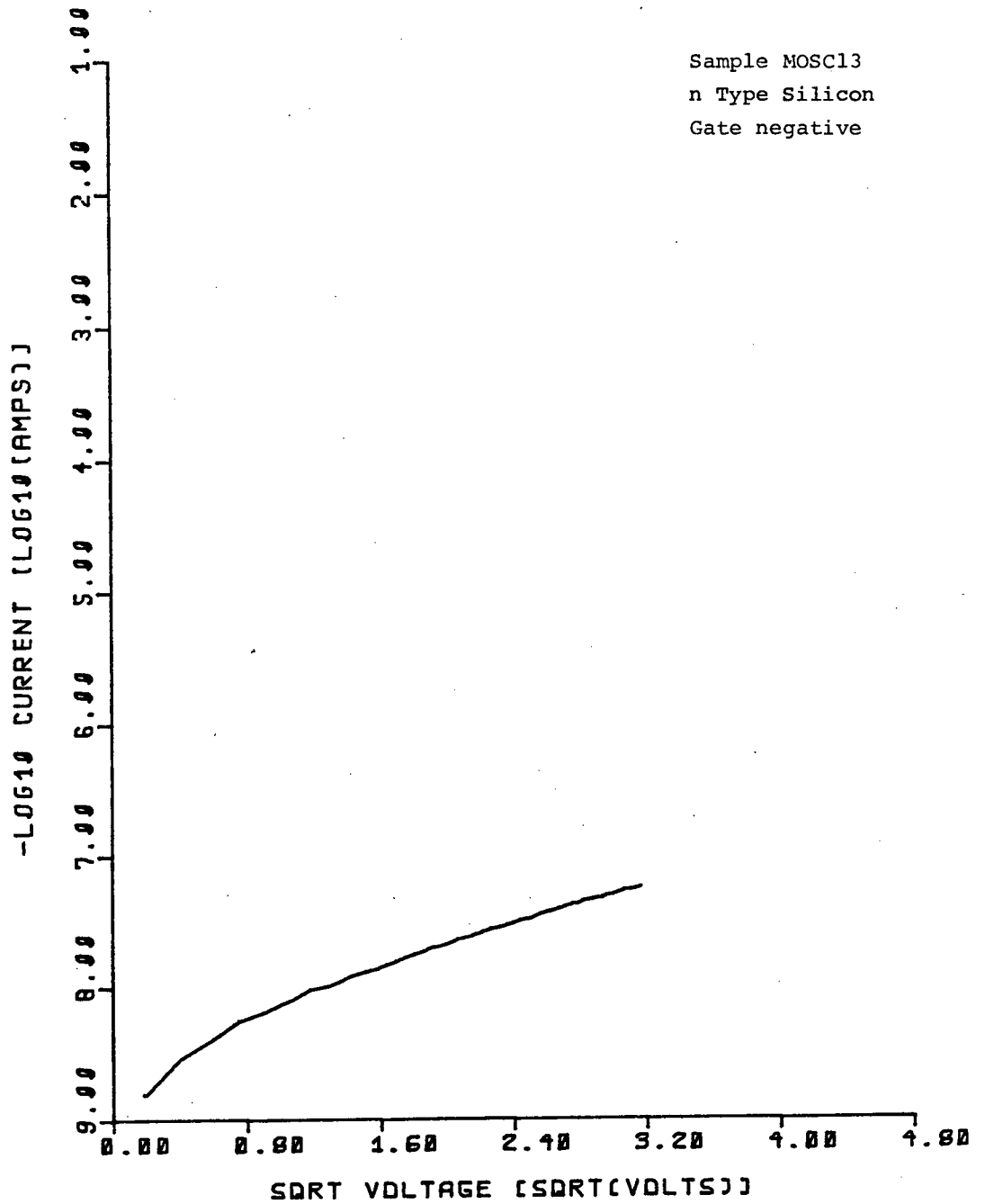
SAMPLE MOSC14, SINGLE DIELECTRIC

n Type, Anodic, Phosphoric Acid.

Sample MOSC14
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
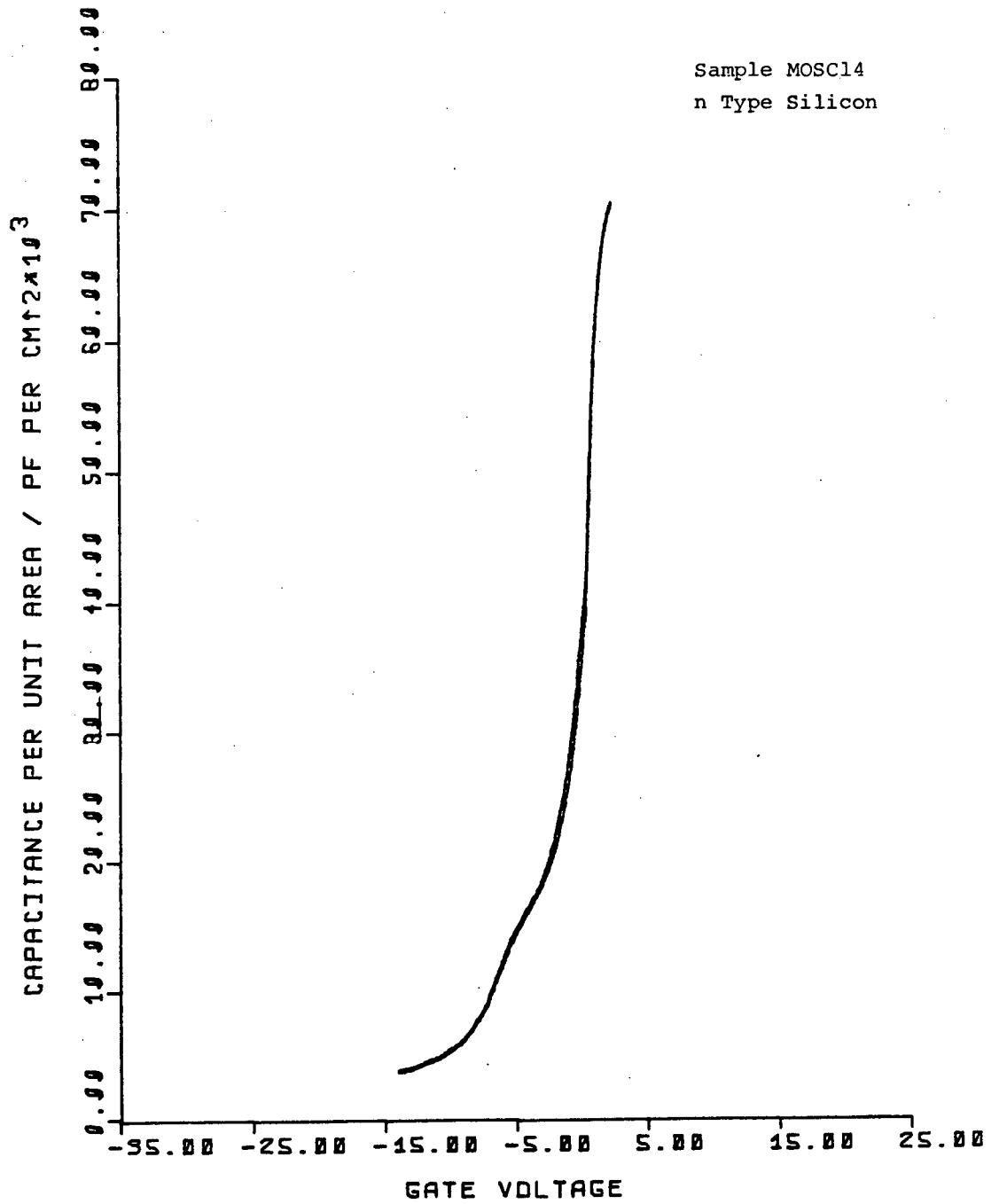
SCHOTTKY IV PLOT

Sample MOSC14
n Type Silicon
Gate negative

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
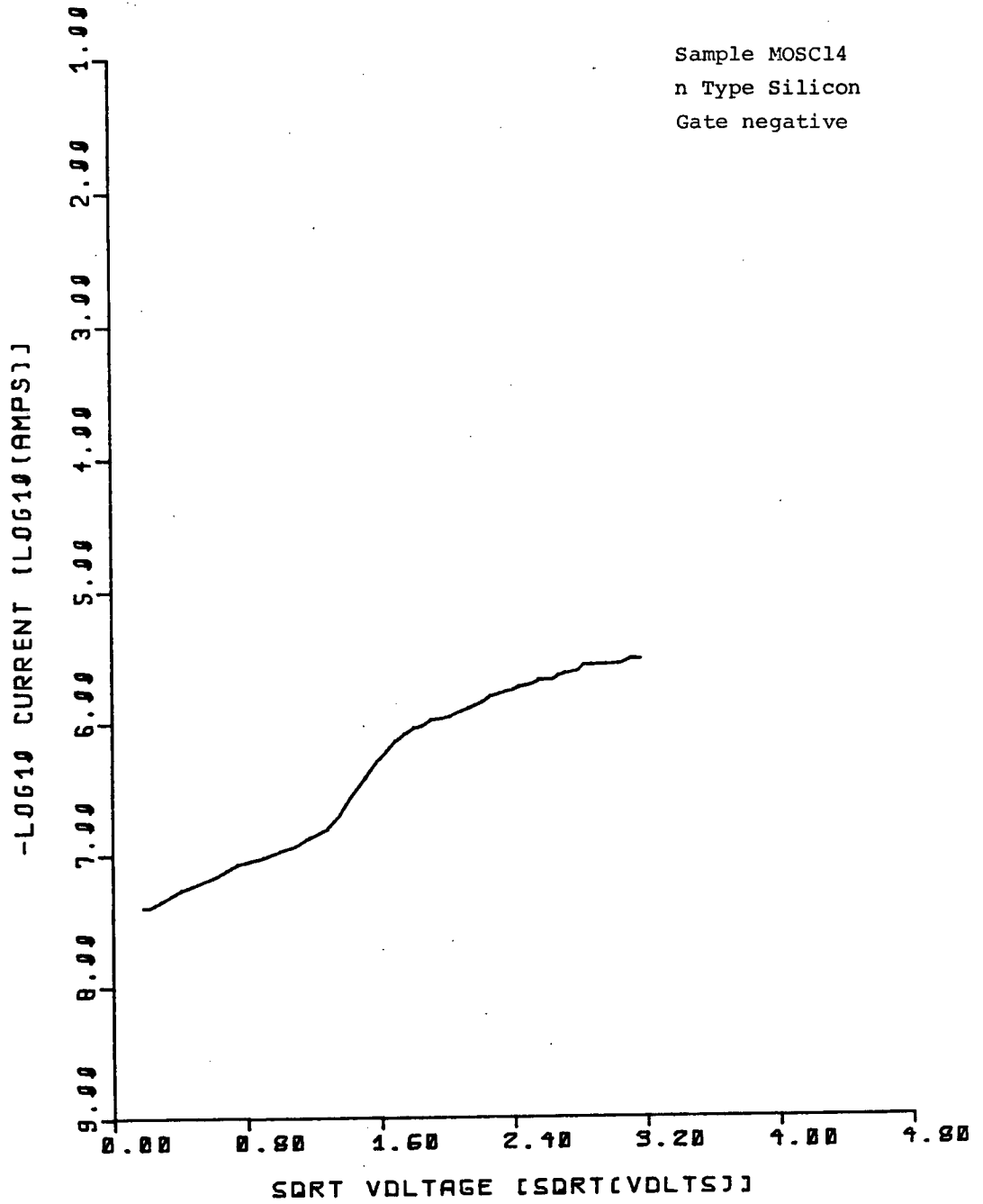
SAMPLE MOSC15, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC15
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE

80.00 70.00 60.00 50.00 40.00 30.00 20.00 10.00 0.00

-35.00 -25.00 -15.00 -5.00 5.00 15.00 25.00

SCHOTTKY IV PLOT

Sample MOSC15
n Type Silicon
Gate negative

−LOG10 CURRENT [LOG10(AMPS)] (vertical axis: 1.00, 2.00, 3.00, 4.00, 5.00, 6.00, 7.00, 8.00, 9.00)

SQRT VOLTAGE [SQRT[VOLTS]] (horizontal axis: 0.00, 0.80, 1.60, 2.40, 3.20, 4.00, 4.80)

SAMPLE MOSC16, SINGLE DIELECTRIC

n Type, Anodic, Phosphoric Acid.

Sample MOSC16
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2x10³

160.00   140.00   120.00   100.00   80.00   60.00   40.00   20.00   0.00

-20.00   -15.00   -10.00   -5.00   0.00   5.00   10.00

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample MOSC16
n Type Silicon
Gate negative

−LOG10 CURRENT (LOG10(AMPS))

SQRT VOLTAGE (SQRT(VOLTS))
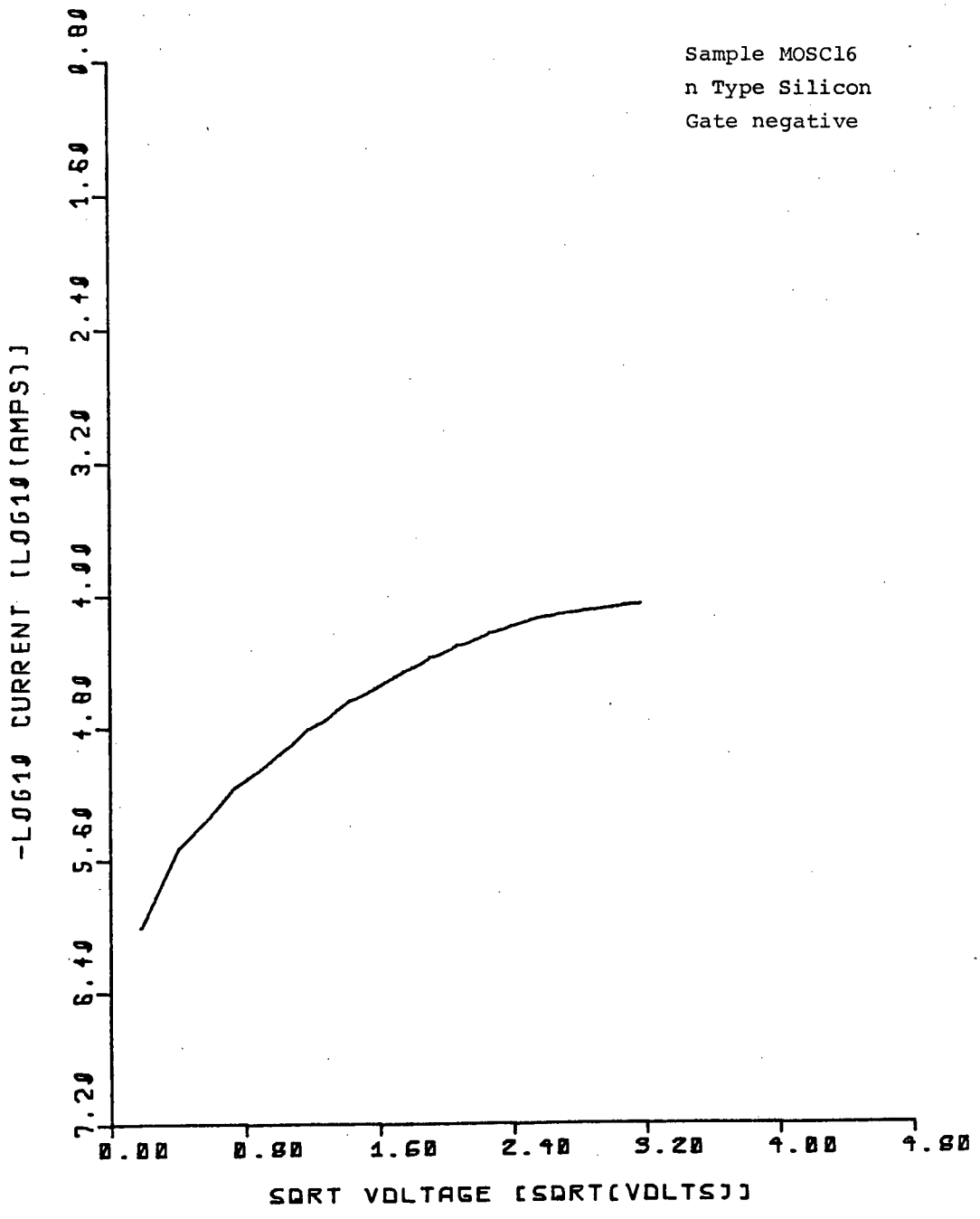
SAMPLE MOSC17, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC17
n Type Silicon
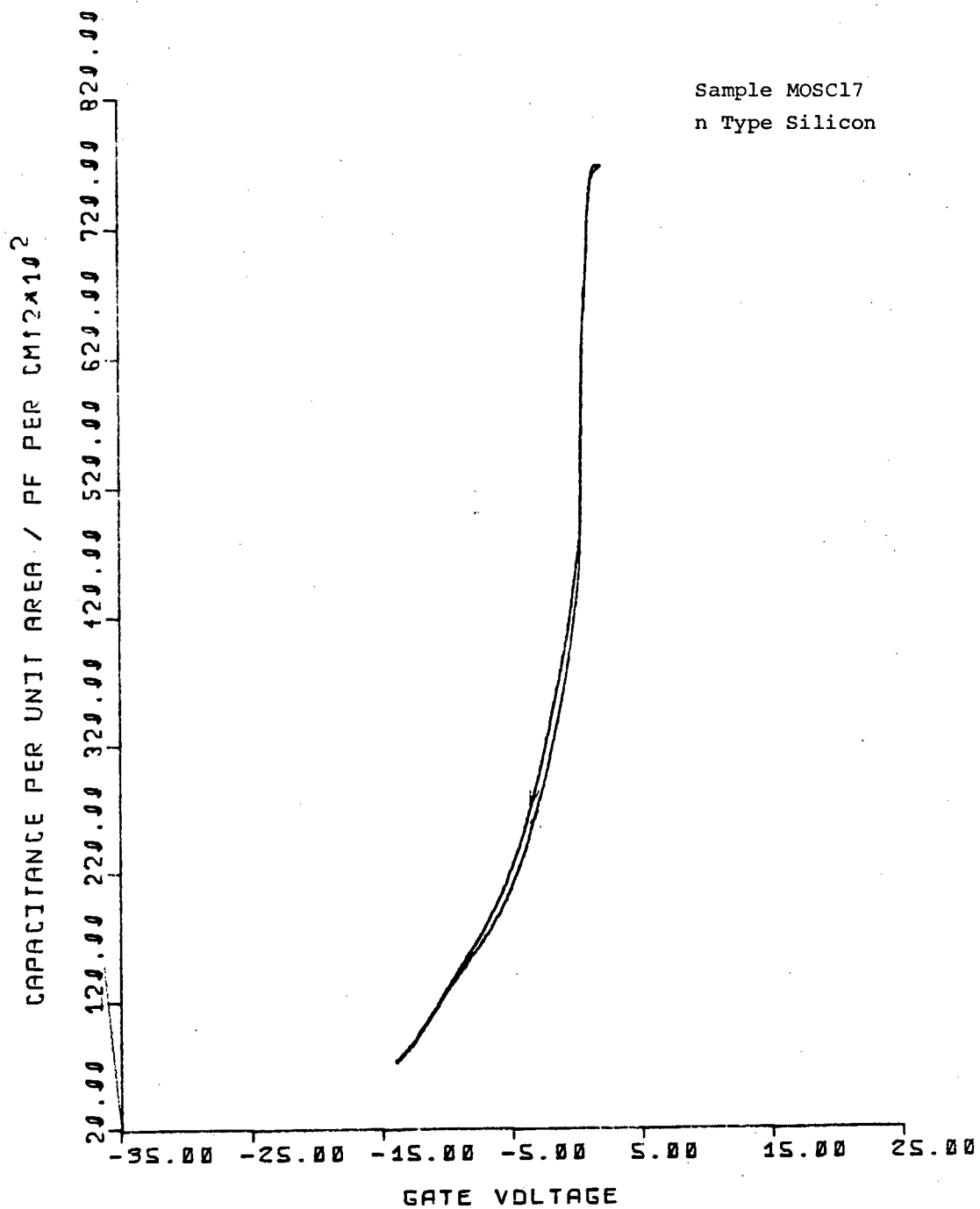
SCHOTTKY IV PLOT

Sample MOSC17
n Type Silicon
Gate negative
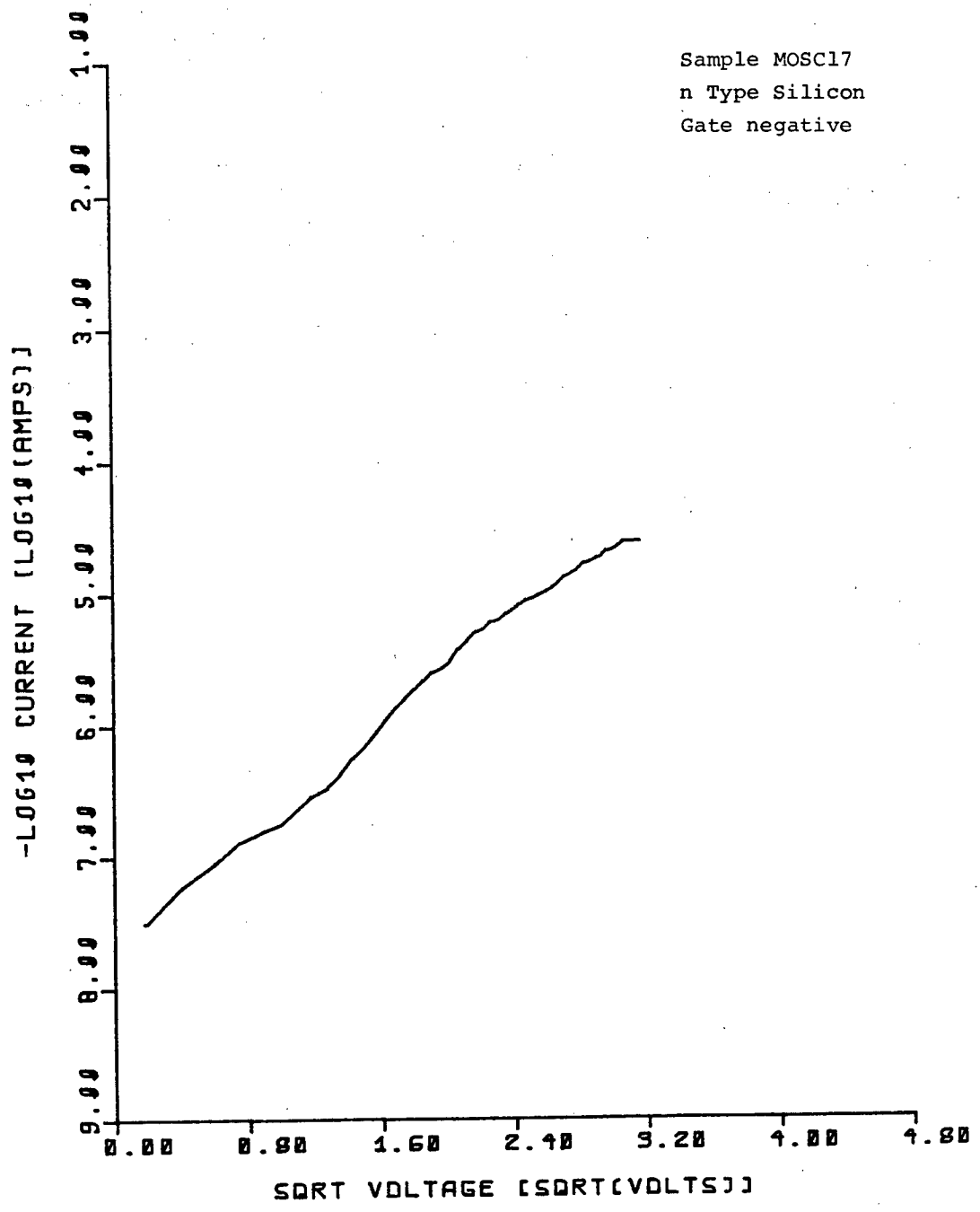
SAMPLE MOSC18, SINGLE DIELECTRIC

n Type, Anodic, Citric Acid.

Sample MOSC18
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10²

GATE VOLTAGE

SCHOTTKY IV PLOT

Sample MOSC18
n Type Silicon
Gate negative

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]

X-axis: SQRT VOLTAGE [SQRT(VOLTS)]
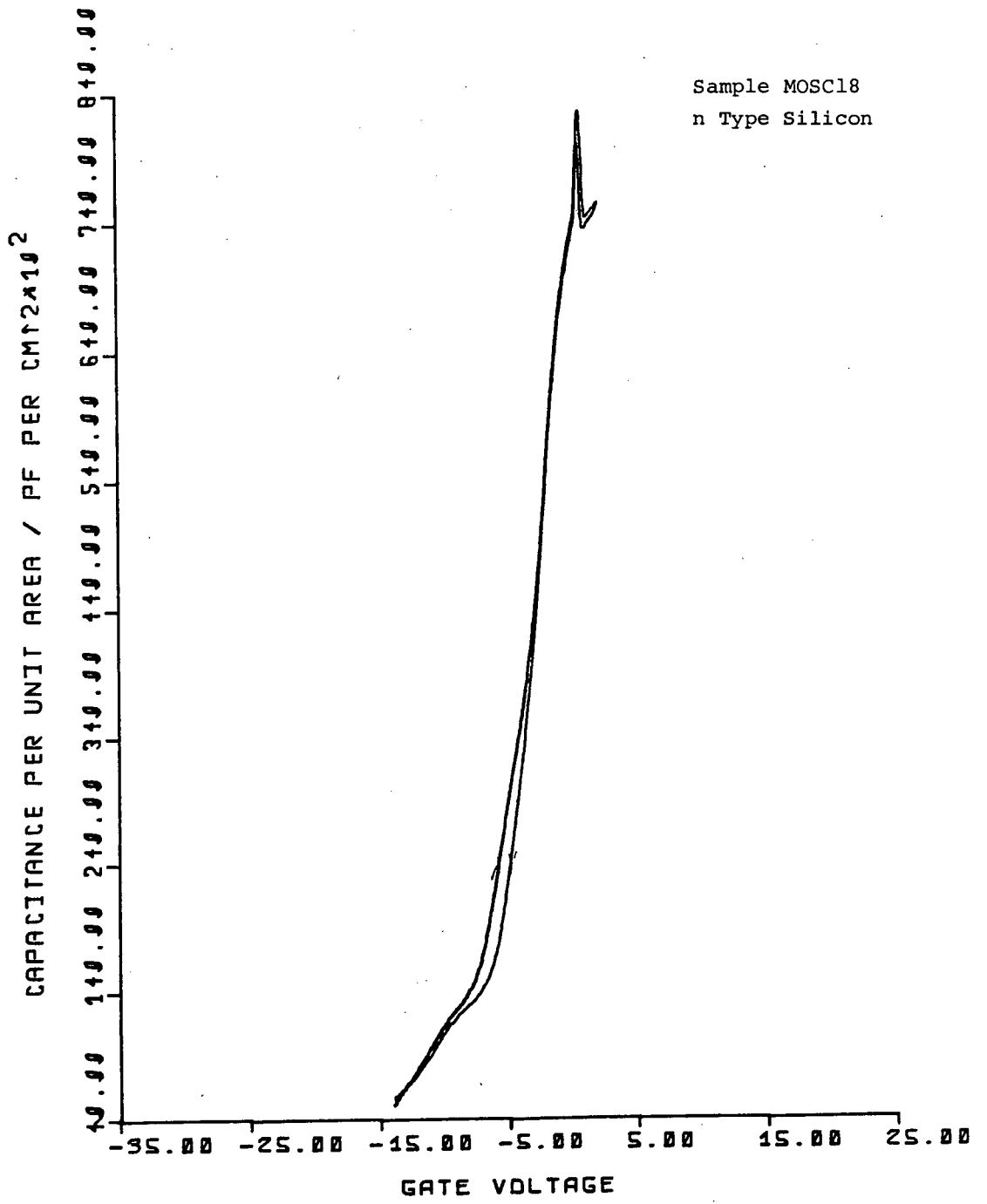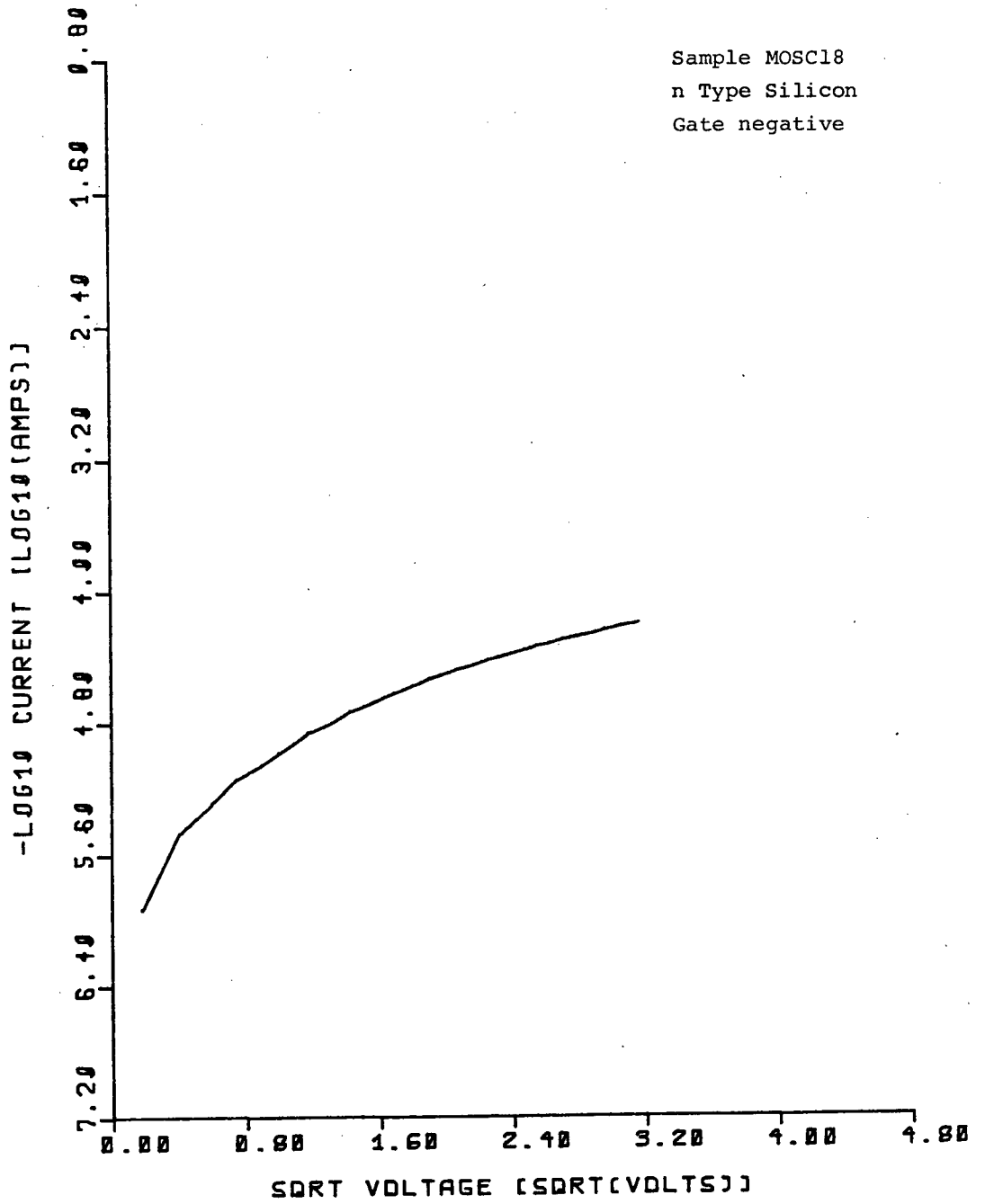
SAMPLE MTJ1, DOUBLE DIELECTRIC

n Type, Interfacial Oxidation.

CAPACITANCE PER UNIT AREA / PF PER CM↑2∗10³

GATE VOLTAGE

Sample MTJ1
n Type Silicon

SCHOTTKY IV PLOT
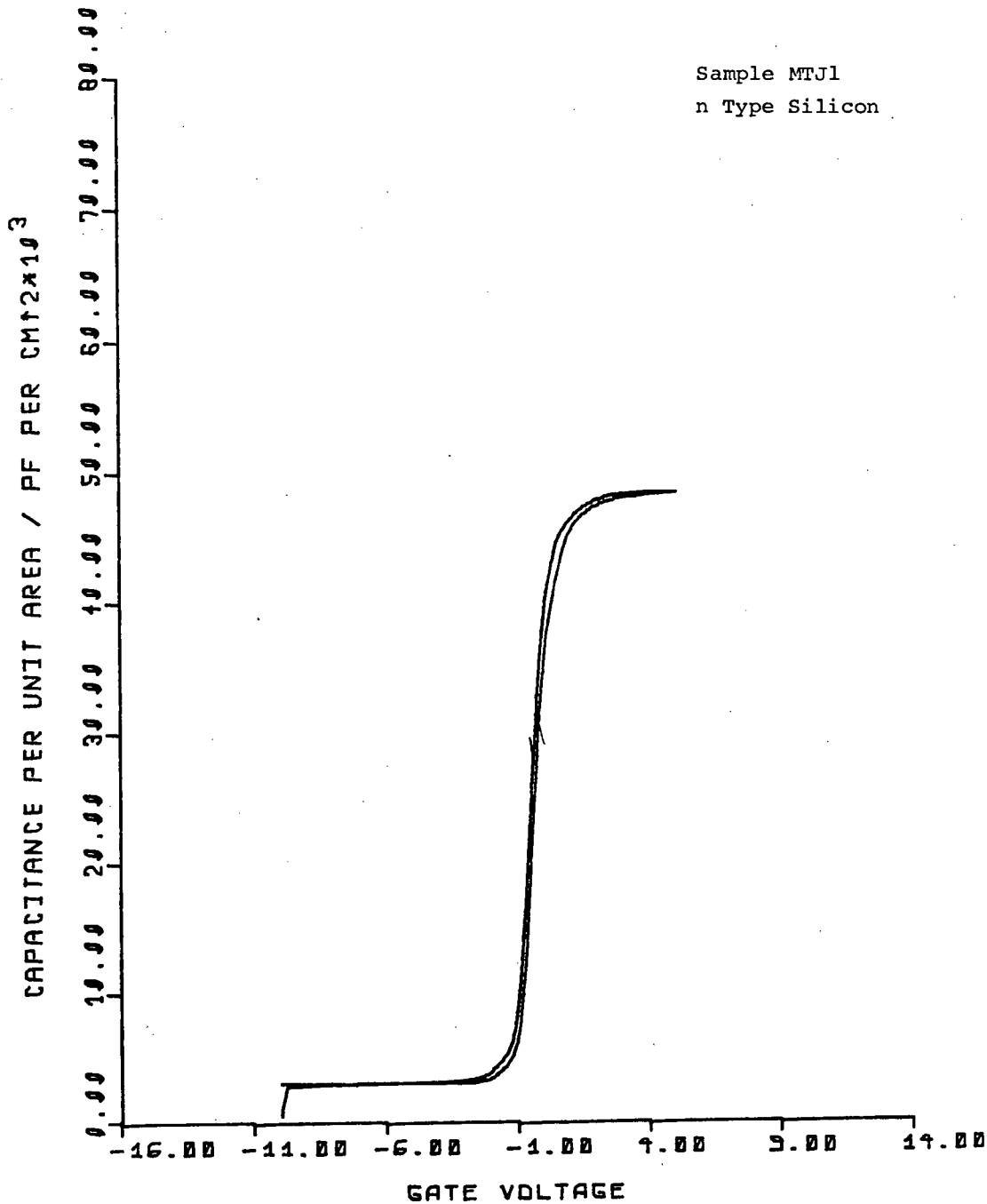
Sample MTJ1
n Type Silicon
Gate negative
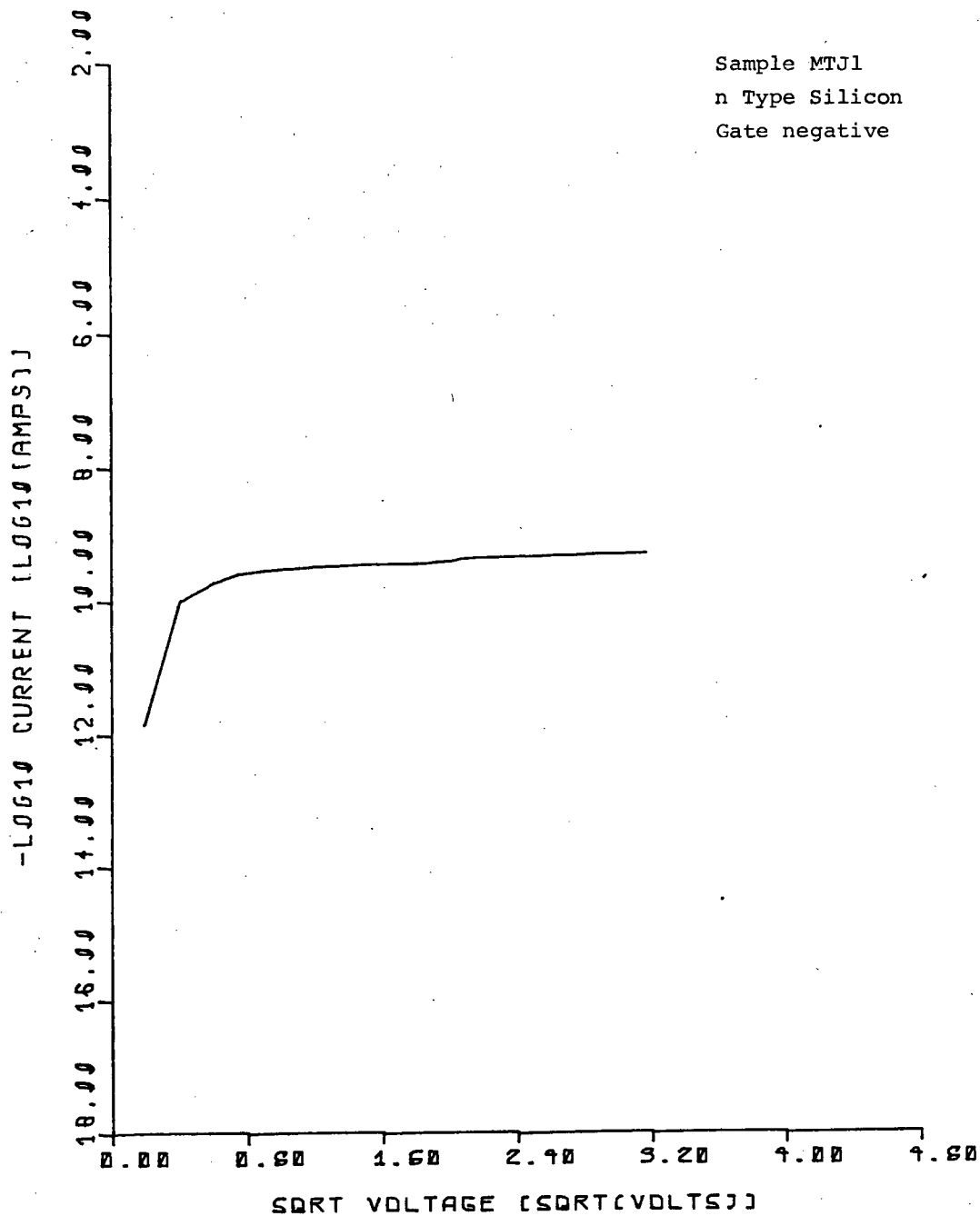
SAMPLE MTJ2, DOUBLE DIELECTRIC

n Type, Interfacial Oxidation.

Sample MTJ2
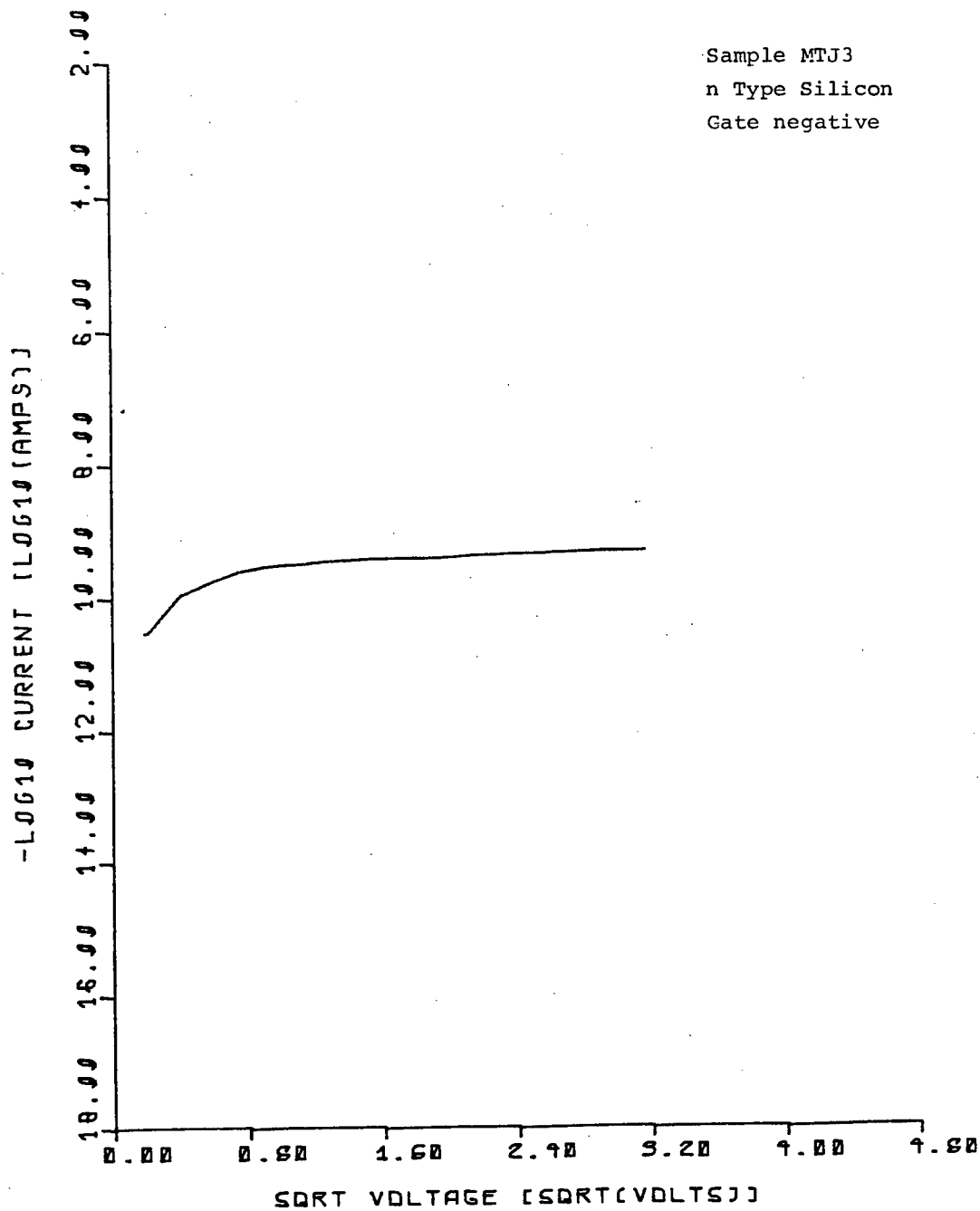n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
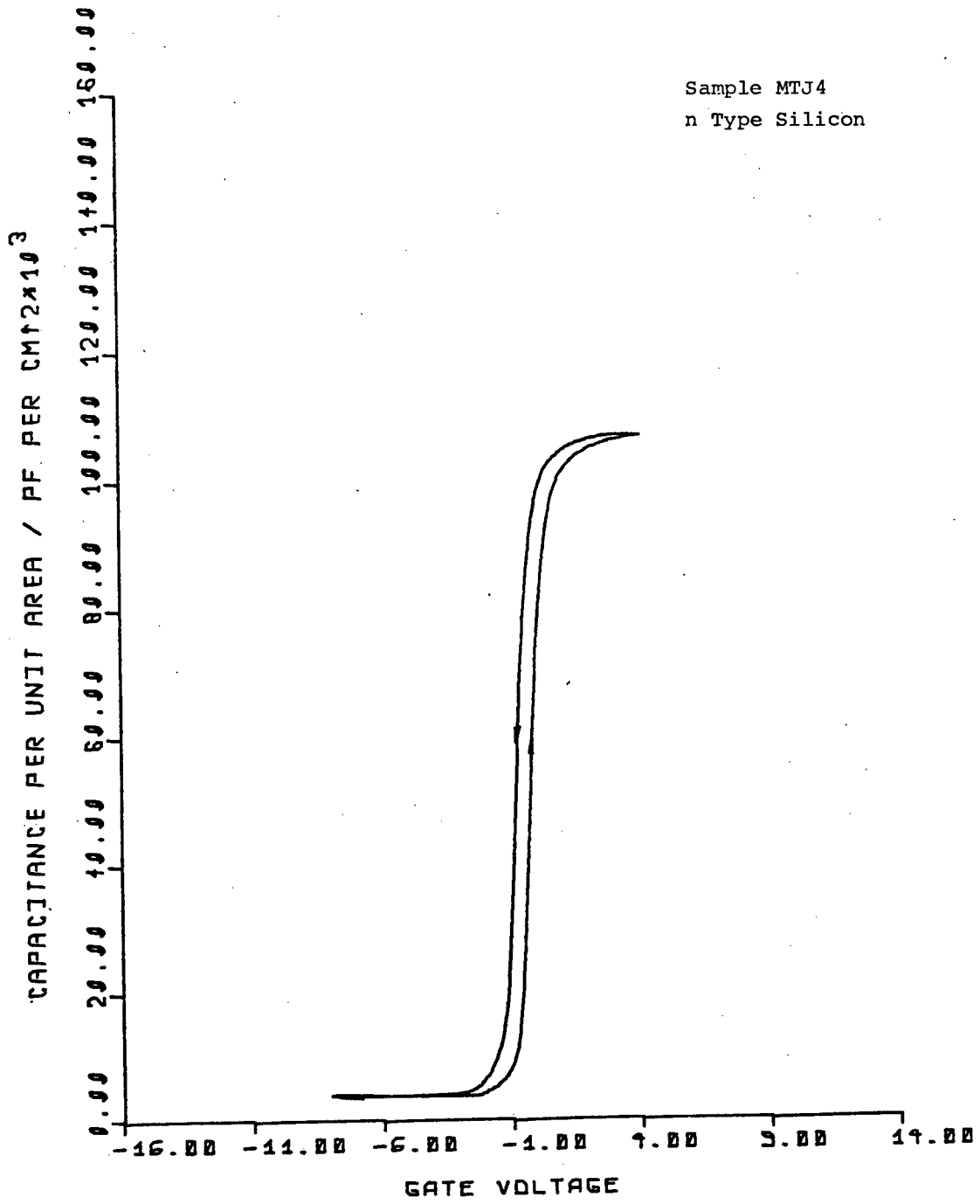
SCHOTTKY IV PLOT

Sample MTJ2
n Type Silicon
Gate negative
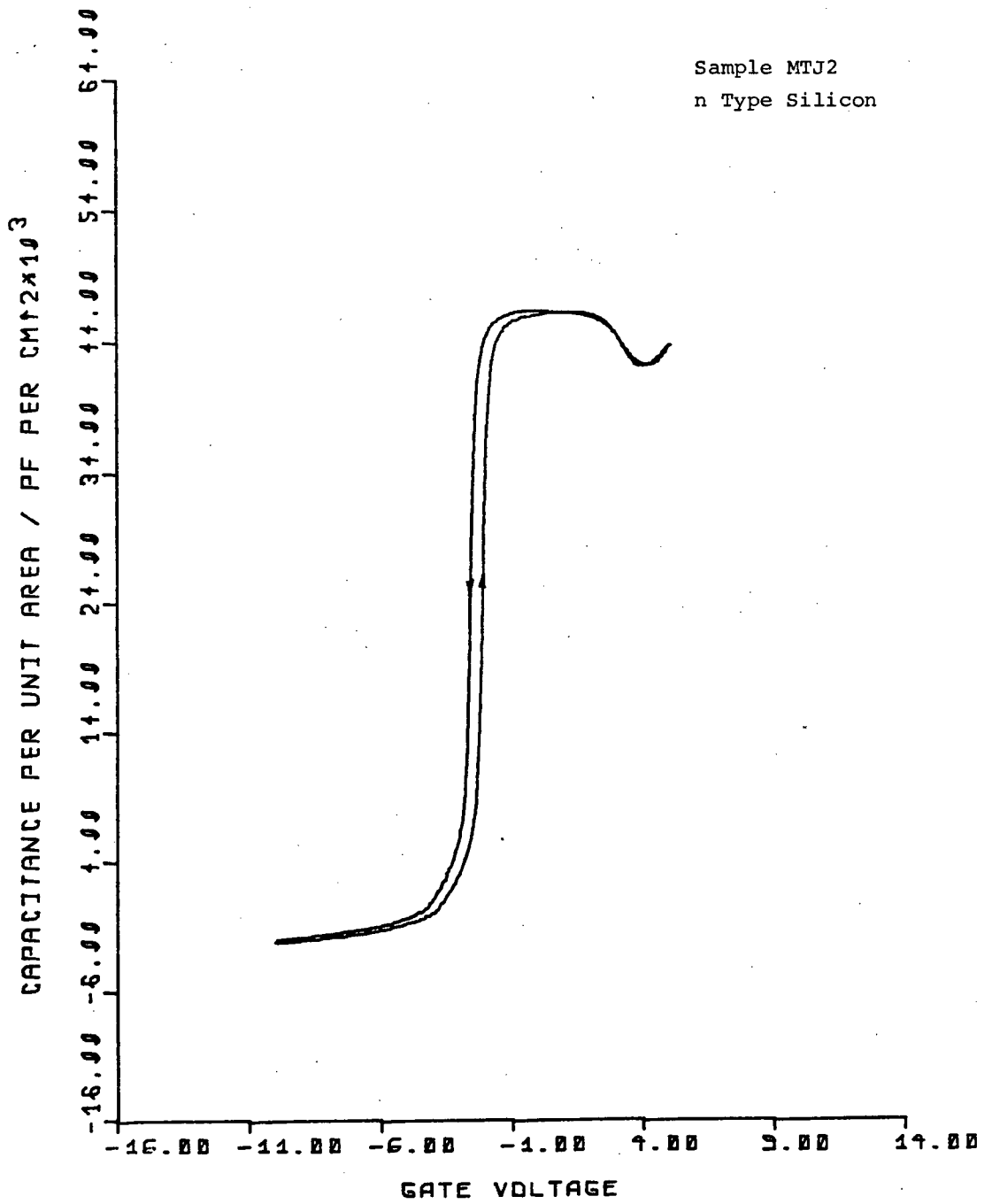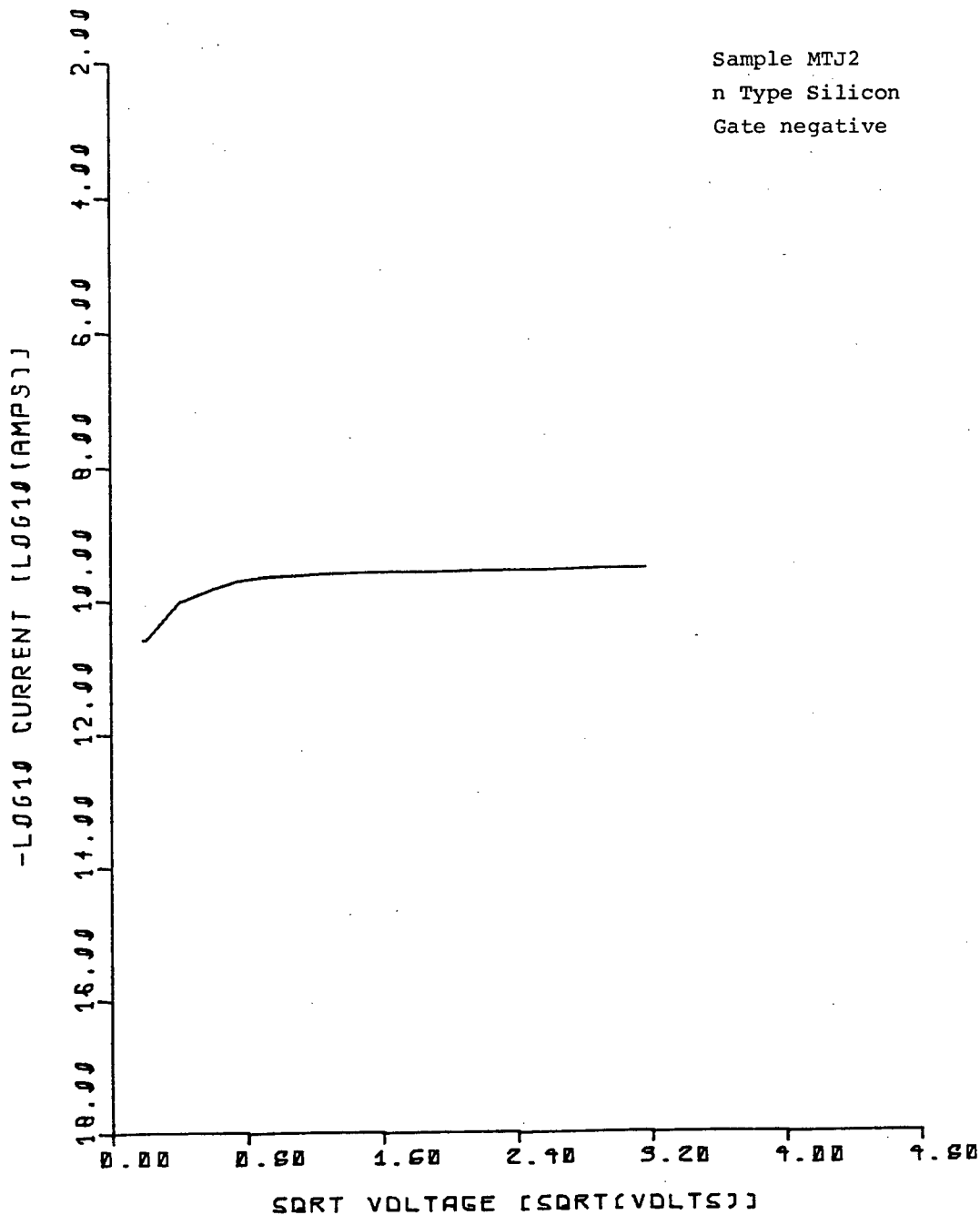
SAMPLE MTJ3, DOUBLE DIELECTRIC

n Type, Interfacial Oxidation.

Sample MTJ3
n Type Silicon

CAPACITANCE PER UNIT AREA / PF PER CM↑2×10³

GATE VOLTAGE
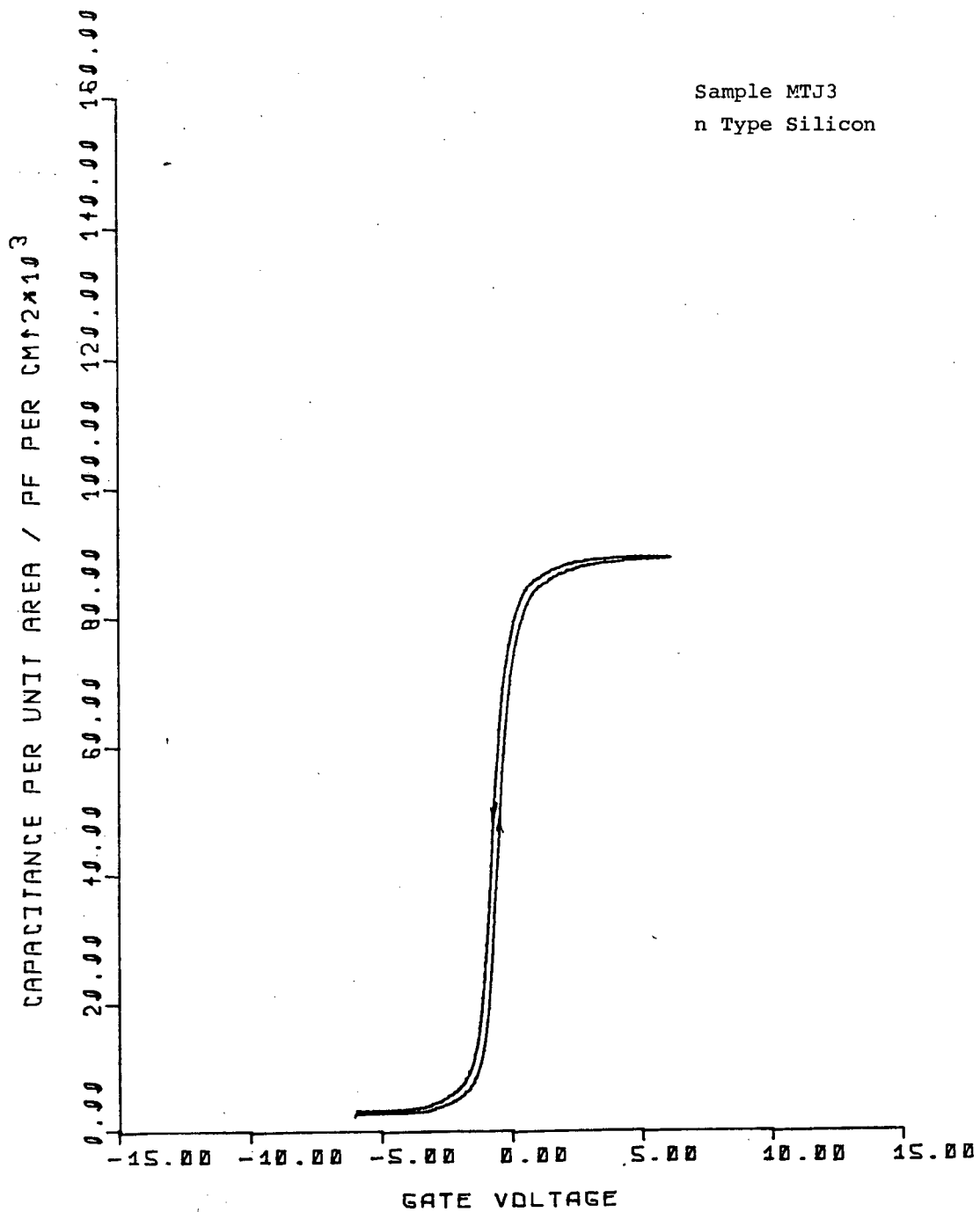
SCHOTTKY IV PLOT

Sample MTJ3
n Type Silicon
Gate negative

-LOG10 CURRENT [LOG10(AMPS)]

SQRT VOLTAGE [SQRT(VOLTS)]

Sample MTJ4, DOUBLE DIELECTRIC

n Type, Interfacial Oxidation.

Sample MTJ4
n Type Silicon

SCHOTTKY IV PLOT

Sample MTJ4
n Type Silicon
Gate negative

Y-axis: -LOG10 CURRENT [LOG10(AMPS)]

X-axis: SQRT VOLTAGE [SQRT[VOLTS]]
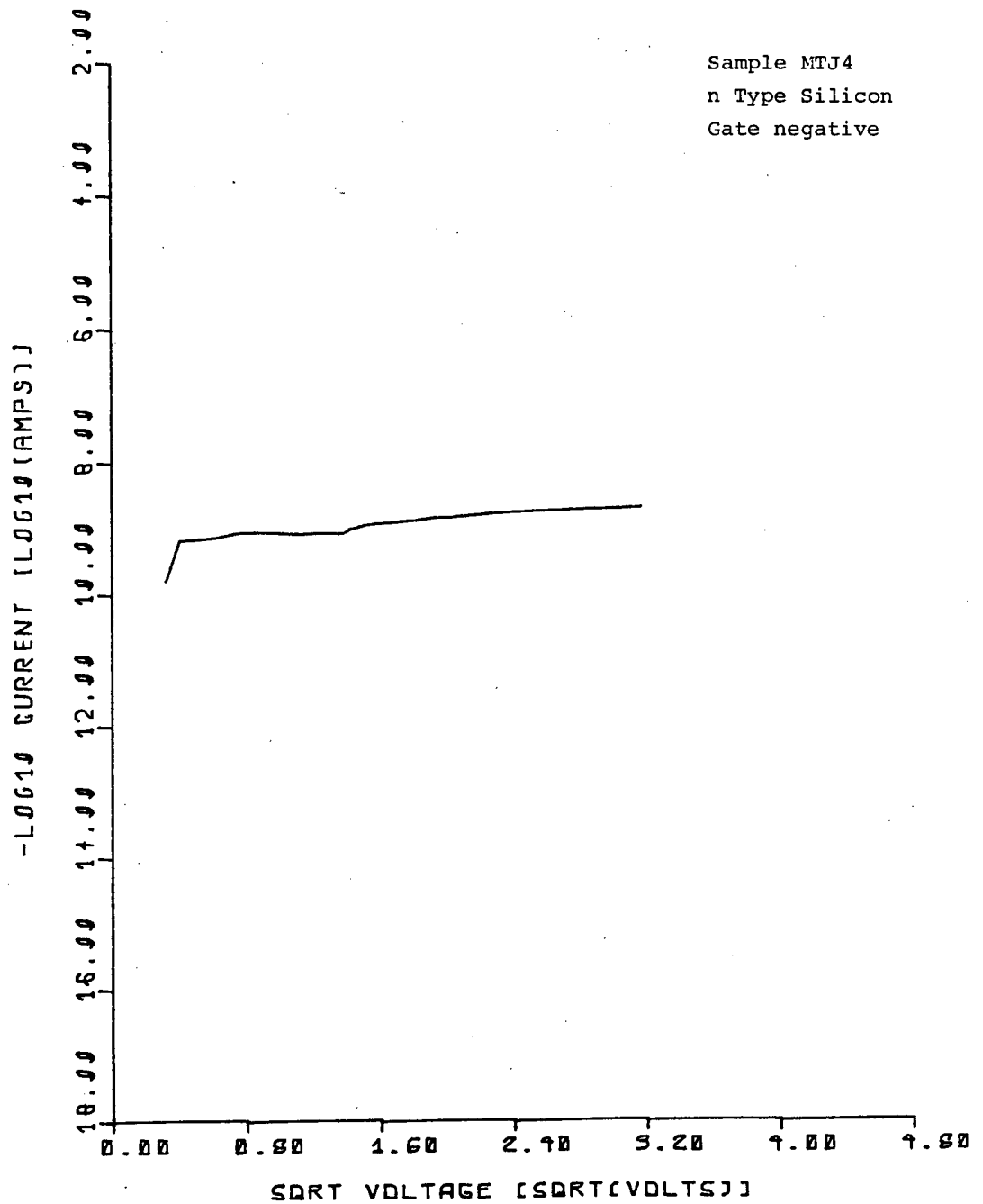
Sample MTJ5, DOUBLE DIELECTRIC

n Type, Interfacial Oxidation.
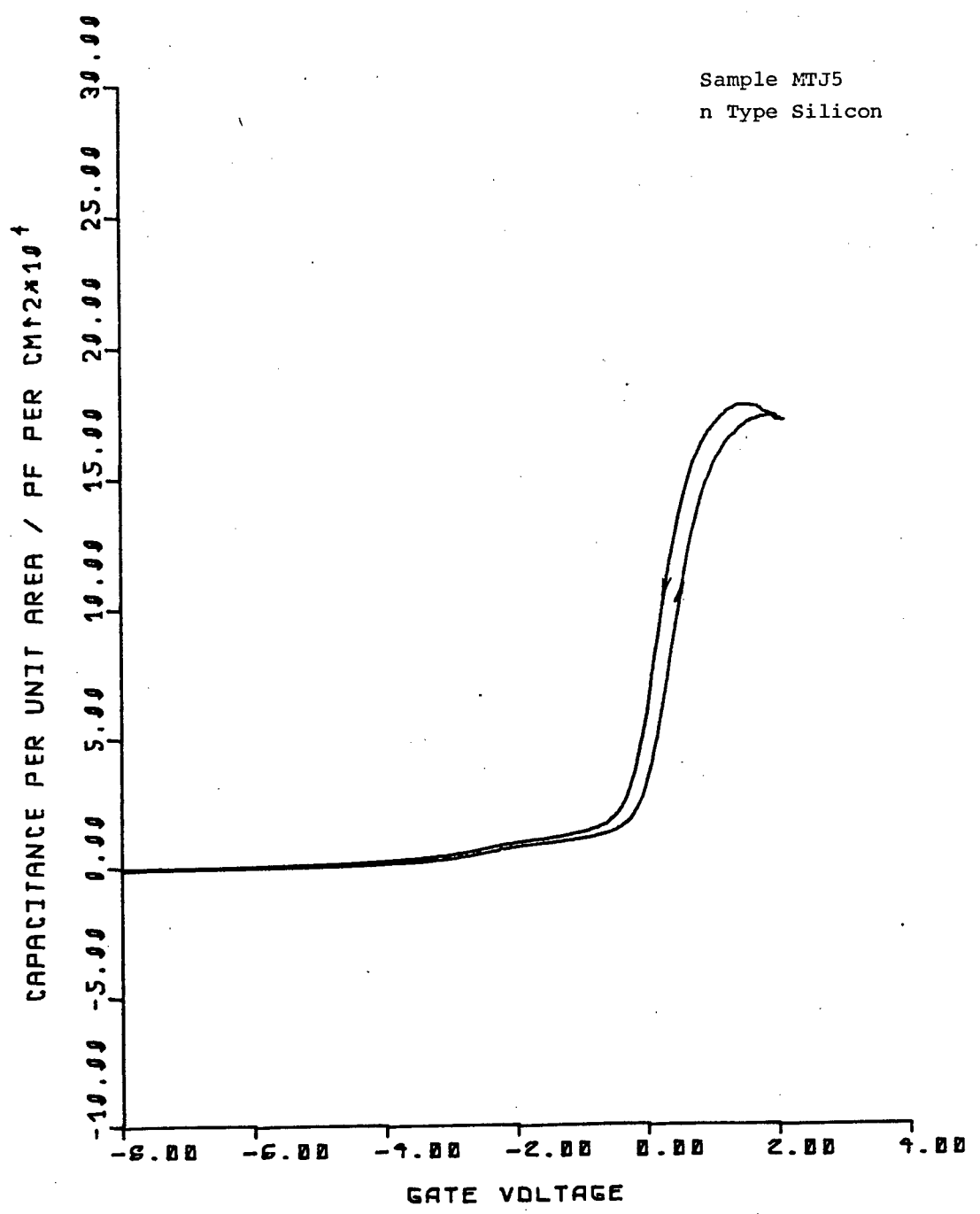
Sample MTJ5
n Type Silicon

SCHOTTKY IV PLOT

Sample MTJ5
n Type Silicon
Gate negative

-LOG10 CURRENT (LOG10(AMPS))

1.00 2.00 3.00 4.00 5.00 6.00 7.00 8.00 9.00

SQRT VOLTAGE (SQRT(VOLTS))

0.00   0.80   1.60   2.40   3.20   4.00   4.80