AN HVDC EQUIDISTANT CONVERTER CONTROL MODEL

by

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ABSTRACT

This thesis presents the design and construction details of a physical model of a six-pulse HVDC converter suitable for steady-state studies. The converter rack has been built to facilitate simple testing and breadboarding. A digital equidistant firing angle controller has been constructed for the converter-rectifier current control. An electronic phase-locked loop has been used to generate an accurate control frequency. Modifications have been suggested to make the rectifier fully operational. The control system has been constructed for future inverter control circuits and possible computer control.
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NOMENCLATURE

SYMBOLS

- C, C₁, C₂, Cₓ₁, Cₓ₂: various capacitors
- Cᵢ: voltage-zero crossing instant across valve i
- E: AC system line-line voltage, rms
- e₀: current error in analog form (e₀ = K(I_d-I_do))
- f: AC System Frequency (60 Hz nominal)
- f_c: control frequency
- f_i: valve firing instant *
- f_o: PLL output frequency
- f_r: PLL reference frequency
- f_rl: 2*f (Output of PLL input conditioning Bd37) Hz
- f_r2: 120 Hz (Output of Astable Frequency Generator)
- f_v: PLL feedback frequency
- i_d: direct current, instantaneous value
- I_d: direct current, mean value
- I_di: inverter current order
- I_dm: current margin
- I_do: desired reference direct current setting in amperes
- I_dr: rated direct current of converter
- K, K₁, K₂: constant
- L: transformer commutating inductance
- P_d: direct current power
- R, R₁, R₂, Rₓ₁, Rₓ₂: various resistors
- R_L: transmission line resistance, ohms
- V_d: direct voltage, mean value
- V_di: inverter direct voltage, mean value
rectifier direct voltage, mean value

valve i

transformer commutating reactance in per unit

firing angle delay (° after C_i) *

minimum allowable firing angle for a valve *

inverter firing angle *

extinction angle *

minimum Y per cycle *

overlap or commutation angle *

angular frequency (radians/cycle)

control parameter (I_d or γ) *

end of valve conduction instant for valve i

firing instant for valve i

time constant

firing angle error in 2's complement binary *

firing angle error for valve i *

* All angles in electrical degrees. Only reference values assume a 60 Hz frequency unless otherwise noted.

**ABBREVIATIONS**

ADC

Analog to Digital Converter

 Comparator

C0, C1, C2, C3

Data Channels

CC

Current Control

CEA

Constant Extinction Angle

CML

Control Mode Logic

CVCD

Commutating Voltage Crossover Detectors
D
DCS
FPG
HVDC
IOC
ISC
LED
LTC
MEA
OWCC
PAC
PACC
PCB
PIC
PLL
PRR
PRRC
SCR
VCM
VCO

Down Counter
Direct Current Sensor
Firing Pulse Generator
High Voltage Direct Current
Inverter Optimum Control
Inverter Safety Control
Light Emitting Diode
Load Tap Changer
Minimum Extinction Angle Control
One Way Current Control
Phase Advance Register
Phase Advance Counter Computer Enable
Printed Circuit Board
Phase-Locked Loop Input Conditioning Board
Phase-Locked Loop
Phase Reduction Register
Phase Reduction Register Computer Enable
Silicon Controlled Rectifier
Voltage Controlled Multivibrator
Voltage Controlled Oscillator

SUBSCRIPTS
A, B, C
AC phases
d
direct current or voltage
i
subscript denoting a particular valve
j
subscript denoting a particular cycle
1, 2, 3, 4, 5, 6
valve number
x
NOMENCLATURE

Logic Symbols (definition for logic "1")

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<thead>
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</tr>
<tr>
<td>ADC</td>
<td>ADC conversion is complete (1.5 μs pulse)</td>
</tr>
<tr>
<td>C</td>
<td>comparator C output (D ≥ CPRR)</td>
</tr>
<tr>
<td>CC</td>
<td>rectifier current control is on</td>
</tr>
<tr>
<td>CCI</td>
<td>ADC error is negative</td>
</tr>
<tr>
<td>CP</td>
<td>computer control is on</td>
</tr>
<tr>
<td>CPAC</td>
<td>contents of the PAC = (a binary number)</td>
</tr>
<tr>
<td>CPRR</td>
<td>contents of the PRR = (a binary number)</td>
</tr>
<tr>
<td>D</td>
<td>number in down counter D = (a binary number)</td>
</tr>
<tr>
<td>G1, G2</td>
<td>AND gates</td>
</tr>
<tr>
<td>IOC</td>
<td>transfer 0 from IOC register to PAC (pulse)</td>
</tr>
<tr>
<td>ISC</td>
<td>transfer 0 from ISC register to PRR (pulse)</td>
</tr>
<tr>
<td>OWCC</td>
<td>inverter one-way current control is on</td>
</tr>
<tr>
<td>PAC</td>
<td>error goes to PAC counter</td>
</tr>
<tr>
<td>PACC</td>
<td>computer control error goes to PAC (pulse)</td>
</tr>
<tr>
<td>PRR</td>
<td>error goes to PRR register</td>
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<tr>
<td>PRRC</td>
<td>computer control error goes to PRR (pulse)</td>
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<tr>
<td>R$_i$</td>
<td>firing pulse output from decoder</td>
</tr>
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<td>R$_i$</td>
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1. INTRODUCTION

High Voltage Direct Current (HVDC) transmission has become commercially useful since 1954 when a 20 MW submarine cable system was commissioned for Gotland Island in Sweden [1], [2]. Since then HVDC has found applications in long distance bulk power transmission, underground cable power transmission, submarine cable transmission, frequency changing, asynchronous interconnection, parallel AC/DC transmission and transmission of power without increasing the fault level at the receiving end.

AC systems are still used for generation, distribution and subtransmission because of economics and flexibility but in the area of transmission HVDC does offer an alternative.

In order for an HVDC system to be an economical alternative to an AC system, the additional expense of the converter terminal equipment must be offset by lower transmission line or cable costs. The break-even distances are about 25 - 50 km for submarine cable and 500 - 1500 km for overhead line [1]. Frequently technical requirements favour HVDC or even eliminate AC.

To date all HVDC systems have been essentially two terminal schemes. However, with advanced control systems, or development of an HVDC breaker, multi-terminal DC systems will become a reality. HVDC systems may also be used for stabilization of AC systems or parallel AC/DC ties. The rapid control of the HVDC power flow has seldom been used to its full potential but with increasing confidence in existing control systems, its use will be extended.

The basic HVDC system is shown in Fig. 1.1.
On-load tap-changing transformers regulate the AC voltage to the converters and allow different phase connections to minimize AC harmonic currents. The converters are 3-phase static switches that allow conversion of AC to DC, and vice-versa. The line reactors smooth the converter DC voltage. The line impedance depends on the length and type of transmission line or cable. AC harmonic filter banks prevent AC harmonic currents from entering the AC systems. Synchronous condensers or capacitor banks are normally required to provide lagging reactive power to both converters to enable the commutation of current from one valve to another in the converter. The HVDC system may be an asynchronous link between two AC systems or may operate in parallel with an AC tie.

A model of an HVDC system allows experimentation and development of equipment, operating techniques, and control systems. Many tests cannot be done on an actual system because of operating demands or fixed parameters. There is also the risk of damaging expensive equipment due to unknown or destructive tendencies of certain tests. A mathematical model can predict behaviour and performance and allows refinement of the model. A physical model duplicating time constants, per unit quantities and...
behaviour of a real system provides valuable practical experience and can verify a mathematical model.

This thesis describes the design and construction of a physical model of an HVDC converter and its control system. The model was scaled to be compatible with the existing micro-machine model of an AC system.

The basic converter connection for HVDC applications has been the 6-pulse 3-phase Graetz bridge shown in Fig. 1.2, however, the 12 pulse connection is becoming prevalent in thyristor installations. For mercury-arc valve converters a seventh valve - the bypass valve - is required for starting, stopping and commutation failure recovery from arc-backs. The thyristor valve converter does not suffer arc-backs so a bypass valve is unnecessary. A mercury-arc valve consists of a common mercury pool cathode and multiple anodes separated by a control grid. The valve is a single unit. A thyristor valve usually consists of several series connected modules each containing a number of Silicon Controlled Rectifiers (SCRs) connected in series or series-parallel. The modules can be individually removed from a permanent valve structure for maintenance. Thyristor valves have become popular because of the absence of arc-backs and the bypass valve, easier maintenance, and higher reliability. A third type of valve called the Liquid Metal Plasma Valve has been built and is being tested at the time of this writing [3]. This valve has an anode and cathode in a vacuum chamber. Conduction starts by shooting a small amount of mercury plasma from the cathode to the anode. This valve has potential benefits in smaller size, lower losses, increased reliability and easier maintenance. All types of converters allow the currents to flow in only one direction, consequently the power flow is changed by reversing the polarity of the voltage across the converters. A 6-pulse SCR converter has been built for this thesis.
FIGURE 1.2 RECTIFICATION - WAVEFORMS

(a) RECTIFIER BRIDGE

(b) DIRECT VOLTAGE REFERRED TO AC SYSTEM NEUTRAL

(c) TRANSFORMER PHASE "A" CURRENT

FIGURE 1.3 INVERSION - WAVEFORMS

(a) INVERTER BRIDGE

(b) DIRECT VOLTAGE REFERRED TO AC SYSTEM NEUTRAL

(c) TRANSFORMER PHASE "A" CURRENT
The operation of the converters can simply be explained with reference to Fig. 1.2 and 1.3. Detailed explanations can be found in [1], [4], [5]. The equation for the rectifier direct voltage is:

\[ V_{\text{dr}} = \frac{3\sqrt{2}}{\pi} E \left( \cos \alpha - \frac{3}{\pi} \frac{I_d}{I_{\text{dr}}} \right) \]

\[ = 1.35E \left( \cos \alpha - 0.5 \frac{I_d}{I_{\text{dr}}} X_c \right) \] (1.1)

The transformer leakage reactance, \( X_c \) and the rated direct current, \( I_{\text{dr}} \) are fixed for a particular HVDC system. \( E \) is determined by the transformer on-load tap-changer (LTC). Consequently, the rectifier direct voltage is controlled by the firing angle \( \alpha \).

The equation for the inverter direct voltage is:

\[ V_{\text{di}} = \frac{3\sqrt{2}}{\pi} E \left( \cos \gamma - \frac{3}{\pi} \frac{I_d}{I_{\text{dr}}} \right) \]

\[ = 1.35E \left( \cos \gamma - 0.5 \frac{I_d}{I_{\text{dr}}} X_c \right) \] (1.2)

Like the rectifier, the inverter direct voltage is controlled by varying the extinction angle \( \gamma \). The angles are related by

\[ \alpha + \beta = \alpha + (\mu + \gamma) = 180^\circ \] (1.3)

where \( \mu \) is the overlap or commutation angle.

The power transmitted by an HVDC system is given by:

\[ P_d = V_{\text{dr}} \cdot I_d \]

\[ = \frac{V_{\text{dr}} \cdot (V_{\text{dr}} - V_{\text{di}})}{R_L} \] (1.4)

Note that the power is proportional to the difference between rectifier and inverter voltages which means that large changes in power can occur.
for relatively small changes in voltage. It is necessary then to simultane­
eously control both the rectifier and inverter voltages. For transmission
schemes a communication system between converters is necessary. Usually
the inverter maintains the system voltage and the rectifier the direct
current.
Fig. 1.4 gives the V-I characteristic for an HVDC converter in both rectifying and inverting modes. Part 1 of the characteristic shows the natural-voltage characteristic of the rectifier; that is, the output voltage for fixed delay angle,
\[ V_d = 1.35 E(1 - 0.5 \frac{I_d}{I_{dr}} X_c) \]  

(1.5)

Part 2 shows the voltage characteristic given by equation (1.1) for different values of \( \alpha \) and \( E \). Part 3 is the constant current characteristic which extends to the inverter region. Part 4 is the constant extinction angle (CEA) characteristic given by equation (1.2). For both mercury arc and thyristor valves, some minimum time, \( \gamma_0 \), is required to deionize the valve; consequently there is no equivalent to the rectifier natural-voltage characteristic at \( \alpha = 0 \).

**FIGURE 1.5 HVDC SYSTEM CONTROL CHARACTERISTICS**
The operation of the rectifier and inverter together in a transmission system can be explained with reference to Fig. 1.5. The rectifier maintains the direct current while the inverter maintains the system voltage. The operating point is at A. The vertical distance "w" is an indication of the power transmitted across the link. Consider an AC system disturbance resulting in a lower rectifier voltage E'. The rectifier tries to maintain $I_{do}$ but $E'$ is too small and the current decreases. The inverter has a backup control made to regulate the current at a setting lower than the rectifier current order by the current margin, $I_{dm}$, which is 10%-20% of rated current. The inverter now controls the current in the link along line $I_{di} = I_{do} - I_{dm}$ and the rectifier controls the voltage. The operating point is now at B. The tap-changers in the rectifier transformers are meanwhile operating to increase the AC voltage applied to the rectifier. The point B slowly moves up the $I_{di}$ line until there is sufficient AC voltage for the rectifier to regain current control. This is a simple explanation of a typical control action. A more detailed explanation will be given later for a particular controller.

There have been two basic methods used to control the firing angle in HVDC converters [6], [7], [8]. The first is the equal angle control where the firing angles for all valves are the same as measured from the instant the voltage becomes positive for each particular valve. The firing instant is determined after each zero-crossing and is sensitive to distortions and asymmetry in the AC voltages. For this reason the older HVDC systems required strong AC systems or large reactive power supplies.

The second method is the equidistant angle control where the firing instant follows the previous firing instant by $60^\circ$ unless there is an error. Apart from protective limits, the firings are not referenced to
(a) VOLTAGE CONTROLLED OSCILLATOR EQUIDISTANT CONTROLLER

(b) PHASE-LOCKED LOOP EQUIDISTANT CONTROLLER

FIGURE 1.6 EQUIDISTANT CONTROLLERS - BLOCK DIAGRAM
the AC voltage waveform but are synchronized to the AC system frequency. Equidistant firing generates less abnormal harmonics than the equal angle firing. Consequently it can be used on weak AC systems and requires less VAR supply.

The equidistant firing can be implemented in two ways. The first is essentially an analog method and uses a voltage controlled oscillator (VCO). The input voltage corresponds to a reference voltage dependent on the AC system frequency plus the control error. The VCO output is decoded in a ring counter and applied to the valves. The VCO frequency increases for earlier firing and decreases for later firing. The second method is more digital in nature and uses a phase-locked loop (PLL) whose output frequency tracks the AC system frequency. The analog error voltage is digitized and loaded in a counter which is counted at a rate determined by the PLL. The counter output is then decoded in a ring counter before being applied to the valves. The instant of firing is varied by changing the number loaded into the counter. The second method has been implemented in this thesis because it can be interfaced with a computer more easily than the former.

The existing UBC HVDC model converters employ a commercial "equal angle" firing circuit consisting of magnetic amplifiers. This circuit has proven to be unsatisfactory in many respects [9]. It is sensitive to supply voltages, is affected by the commutation voltage distortion and becomes unbalanced for asymmetrical AC voltages. The circuit itself is epoxy sealed in a metal box making repair or modification difficult if not impossible. To allow future HVDC research to be carried out more easily, it was decided to construct a new controller which reflected the latest developments in HVDC technology. An equidistant control scheme adaptable to computer control was consequently designed and is described in the following chapters.
2. BASIS FOR DESIGN OF AN HVDC CONVERTER CONTROL

This chapter describes a closed-loop control system [10], [11] for High Voltage Direct Current (HVDC) converters with independent feedback loops of digital information to produce equidistant firing of the HVDC valves. This equidistant control forms the basis for the direct digital control implemented in the following chapters.

2.1 BASIC PRINCIPLE

The firing instant $p_i$ of a valve $V_i$ is related to the firing instant $p_{i-1}$ of the previous valve $V_{i-1}$ as follows:

$$p_i = p_{i-1} + 60^\circ + \theta_i$$

(2.1)

where $\theta_i$ is the firing angle error for valve $i$ expressed in electrical degrees, and where $i$ changes in a cyclic manner from 1 to 6. Under steady-state conditions, the firing angle error $\theta_i$ is zero. Consequently, the firing instant $p_i$ of any valve defines completely the firing instants of all the other valves by means of a train of pulses $60^\circ$ apart.

We now define the control parameter $\phi$ for each firing instant $p_i$ as the relative position of the train of firing pulses with respect to the zero-crossing of the commutating voltage. The absolute value of $\phi$ is of little importance since the quantity needed as the basis for control is the variation of the control parameter $\Delta \phi$, at each firing instant,

i.e., $\Delta \phi = \theta_i$

(2.2)

Under steady-state conditions $\phi$ is constant.

The proposed control scheme is a negative feedback control with the firing angle error made proportional to the deviation from nominal of
the control parameter such as current, power, extinction angle, frequency, etc. All types of converter control attempt to optimise the firing of the valves with respect to the parameter under control, subject to requirements of reliability of operation and of economy. The proposed control scheme gives rise to two control modes which are considered in the sections to follow:

1. Rectifier Constant Current Control (CC) and Inverter One Way Current Control (OWCC) with the DC line current $I_d$ as the control parameter.

2. Inverter Safety Control (ISC) and Inverter Optimum Control (IOC) which together constitute the Minimum Extinction Angle (MEA) control with the extinction angle $\gamma$ as the control parameter.

It should be noted that the converter control is either Current Control for the rectifier or MEA control for the inverter regardless of the control parameter for the HVDC system.

2.2 RECTIFIER CONSTANT CURRENT CONTROL - THEORY

As explained in Chapter 1, the disadvantages of the conventional constant current control lie in the use of the firing angle alpha, $\alpha$, as the controlled quantity. This can be overcome by using a control parameter which is not directly dependent on the waveshapes of the commutating voltages. Using equation (2.1) as the basis for the constant current control, the firing angle error is given by:

$$\theta_i = K \Delta I_d = K(I_d - I_{do})$$  \hspace{1cm} (2.3)

Under balanced or unbalanced steady state conditions, with sinusoidal or
distorted waveforms, the control parameter and the firing angle are constant (i.e., \( \Delta \phi = \theta_i = 0 \)) and the converter valves are fired at regular intervals of 60°. In general, firing according to (2.1) will result in six different firing angles, \( \alpha \), per cycle. During disturbances, variation of the control parameter \( \Delta \phi \) will result in equal changes of the firing angles.

i.e., \( \Delta \phi = \Delta \alpha = K \Delta I_d \)  \hspace{1cm} (2.4)

The difference between the conventional control method and the proposed method is shown in this equation. With the conventional method a common firing angle, \( \alpha \), is generated proportional to the direct current and is the same for all the valves. With the new method, a common variation of firing angles is generated proportional to the variation of direct current.

In the CC control system defined by (2.1) and (2.3) the firing angle can take any value. However, there must be a minimum AC voltage across a valve before firing is permitted. This requirement can be expressed as follows:

\[ \phi > \phi_{\text{min}} \]  \hspace{1cm} (2.5)

where \( \phi_{\text{min}} \) is \( \alpha_{\text{min}} \), the minimum allowable firing angle for a valve. Thus the rectifier operates on CC control when \( \alpha > \alpha_{\text{min}} \) and on minimum firing angle \( \alpha_{\text{min}} \) otherwise. For balanced conditions, the latter is also referred to as the natural voltage characteristic of the converter. The complete equations for rectifier operation can now be expressed as follows:

\[ f_i = \rho_i = \rho_{i-1} + 60^\circ \pm \theta_i \quad \text{if} \quad \rho_i \geq C_i + \alpha_{\text{min}} \]

\[ = C_i + \alpha_{\text{min}} \quad \text{if} \quad \rho_i < C_i + \alpha_{\text{min}} \]  \hspace{1cm} (2.6)
When $\rho_1 < C_1 + \alpha_{\text{min}}$, the CC control is overridden by the minimum firing angle limit, $\alpha_{\text{min}}$.

In addition to the converter control which is the subject of this thesis, there is a converter transformer tap control which although much slower than converter control keeps the firing angle within a range of alpha about the optimum.

2.3 INVERTER CONTROL - THEORY

The inverter has two basic control modes, the minimum extinction angle (MEA) control which is the normal control mode and the one way current control (OWCC) which is used to maintain power transmission when the rectifier is not capable of maintaining the current.

Minimum Extinction Angle Control (MEA)

Unlike conventional control methods for extinction angle, the MEA is not a predictive method. With reference to Fig. 1.3, the firing instant $\rho_i$ of valve $V_i$ is determined at the previous zero-crossing $C_{i+2}$ and is based on information about the system available at that instant. If system conditions remain unchanged during the time interval $C_{i+2}$ to $\rho_i$, then the extinction angle $\gamma_i$ will be equal to the expected value $\gamma_o$. If, however, the system conditions change, the control remains unchanged during the disturbance but readjusts the firing at the next zero-crossing. The MEA can thus be described as a discrete negative feedback control system.

With this type of control, the firing angle correction is proportional to the deviation of the extinction angle from the optimum value, i.e.,

$$\theta_i = \Delta \phi = K(\gamma_o - \gamma_{i-1})$$

(2.7)
Using equation (2.1) as the main control equation, steady state conditions will result in symmetrical valve firings. As a result of the symmetrical firing, any unbalance or distortion of waveshape may produce six different $\gamma$ per cycle.

The MEA control has two requirements:

1. $\gamma_i \geq \gamma_o \tag{2.8}$

2. $\gamma_{\text{min}} = \gamma_o \tag{2.9}$

The Inverter Safety Control (ISC) ensures that condition (2.8) is met.

The firing angle error here is given by:

$$\theta_i = K_1 (\gamma_{i-1} - \gamma_o) \tag{2.10}$$

where $\gamma_o$ is the preset extinction angle for the converter.

The ISC is a one way control process which results only in an increase in extinction angle.

The ISC is used to prevent commutation failures and consequently is effective on the firing following the disturbance.

The Inverter Optimum Control (IOC) implements (2.9) by minimizing the extinction angle during the steady-state operation of the inverter. The IOC affects the firing of all 6 valves in a cycle only after it has been established that $\gamma_{\text{min}} > \gamma_o$ during the previous cycle. This can be expressed in the following equation:

$$\theta_{j+1} = K_2 [(\gamma_{\text{min}})_j - \gamma_o] \tag{2.11}$$

Like the ISC, the IOC is a one way control process, however, it results only in a decrease in extinction angle. The complete equations for inverter MEA control are:

$$\theta_i = K_1 (\gamma_{i-1} - \gamma_o) \text{ for } \gamma_i < \gamma_o \tag{2.10}$$

$$\theta_{j+1} = K_2 [(\gamma_{\text{min}})_j - \gamma_o] \text{ for } \gamma_{\text{min}} > \gamma_o \tag{2.11}$$
Disturbances will normally cause the operation of the ISC first which is then followed by operation of the IOC. A long disturbance would normally cause the inverter transformer LTC to operate as well. A more detailed discussion of the ISC and the IOC can be found in reference [10]. It can be seen that the two independent control modes of the MEA produce opposite effects. Consequently, the overall operation of the MEA control is stable since the operation of the IOC never triggers the operation of the ISC.

One Way Current Control (OWCC)

The normal inverter control is the MEA control discussed above. The inverter also has a protective type of current control called the One Way Current Control (OWCC) which is used to keep $I_d$ from decreasing below $I_{di}$. This allows the rectifier to regain current control without shutting down the system. The OWCC can be explained by considering the transition from MEA to OWCC and vice-versa. First of all, the inverter is given a current setting $I_{di}$ which is less than the rectifier current setting $I_{do}$ by the current margin $I_{dm}$. The value of $I_{dm}$ normally is 10-20% of the system current rating.

The OWCC process is defined by (2.1) where the firing angle error is given by:

$$
\theta_i = k(I_d - I_{di}) \quad \text{if} \quad I_d < I_{di}
$$

$$
= 0 \quad \text{if} \quad I_d \geq I_{do}
$$

(2.12)

As shown in Fig. 2.1 control transfers from MEA to OWCC when $I_d \leq I_{di}$ and transfers from OWCC back to MEA when $I_d \geq I_{do}$. The OWCC process only prevents $I_d$ from decreasing below $I_{di}$, it does not prevent the current from increasing above $I_{di}$ because it can only increase the extinction angle.
FIGURE 2.1 OWCC – MEA Transfer Characteristic
3. CONSTRUCTION OF THE HVDC CONVERTER CONTROL MODEL

This chapter outlines the hardware implementation of the control method proposed in Chapter 2. The converter bridge construction is first described and then the converter rectifier control block diagram and associated equations are outlined. The detailed description of circuitry and experimental results will be discussed in Chapters 4 - 6.

3.1 CONVERTER RACK

Fig 3.1 shows the main features of the Graetz bridge used to model an HVDC converter. A device to represent the mercury-arc bypass valve or the solid state bypass switch has not been included because the model is not intended for transient modelling of start-up/shut-down procedures or protective actions. The model converter has been scaled to be compatible with the existing UBC micro-machine AC system model. The control requires two inputs from the bridge: the AC voltages and the direct current. Matched resistors have been used to construct the 3 phase voltage divider which has a single phase ratio of 100:1. The maximum phase-phase error is 0.17%. Although the resistance divider gave no problems, an improvement would be to use 3 potential transformers to provide complete ground isolation between the power and control circuits.

The 0.5 ohm resistance on the DC side gives the required voltage drop to the Direct Current Sensor which is described in 5.1.

The voltage and current panel meters shown in Fig. 3.1 are mounted at the top of the rack just above the converter bridge. Important nodes in the power circuit are brought out to a coloured mimic panel for easy monitoring with scope or meter probes. A variety of control functions
FIGURE 3.1 CONVERTER SCHEMATIC
are also mounted on the mimic panel. A breadboard shelf with five breadboards is located just below the wire-wrap pins of the printed circuit board (PCB) connectors. This is quite useful for constructing new circuits and for modifying circuits already on the PCBs. The main power supplies, a convenience receptable and the power terminals of the bridge are mounted near the bottom of the rack.

3.2 CONVERTER CONTROL MODEL

Chapter 2 briefly described the theory behind a new digital control system for HVDC converters. This section outlines a hardware implementation based on that control. The main differences with the control system described in [10] and [11] and the equidistant firing control implemented here are the use of an electronic phase-locked-loop rather than an electromechanical optical encoder to generate the control frequency and provision for possible computer control. This section gives a functional description of the control while the detailed descriptions will be given in the following chapters.

The block diagram for the rectifier control system is shown in Fig 3.2. The control can be broken down into three main parts: generation of the control frequency $f_c$, monitoring of analog quantities, and generation of the SCR firing pulses. The control frequency, $f_c$, is a multiple of the AC line frequency and remains in synchronism with it. It is the master clock for the digital portion of the control. Various analog quantities - AC voltages, direct current order and direct current response - are monitored, conditioned and processed to provide timing pulses and the digitized current error to the control. Generation of the firing pulses is done in
FOR HYDRO CONVERTER MODEL

FIGURE 3.2 BLOCK DIAGRAM - EQUIPOTENTIAL FIRING CONTROL
the digital portion from information provided by the analog front end or an external input. An outline of the function of the various blocks in the control is given below.

Generation of the Control Frequency, $f_c$

Figure 3.2 shows the main blocks affecting generation of the control frequency. Details of the individual circuits can be found in Chapter 4. One AC voltage — arbitrarily chosen as phase A — is applied to the Phase-Locked Loop Input Conditioning (PIC) board which generates a pulse train at a frequency, $f_{rl}$, double that of the AC system frequency $f$, i.e., $f_{rl} = 2f$ (3.1)

The board contains a 3-pole low-pass filter, a zero-crossing comparator and two monostables.

A digital Phase-Locked Loop (PLL) is the heart of the circuit that generates the control frequency, $f_c$. To simplify construction of the PLL, the PLL input reference frequency, $f_r$, is double the line frequency.

Since for AC power systems, the rate of frequency change is slow, the PLL time constant can be long. This results in a rather long lock-up time which is the time required for the PLL to lock on to the reference from its free running frequency. This is overcome by supplying a reference frequency, $f_r$, that is close to the nominal frequency. This is the function of the Reference Frequency Selector. If the AC voltage is below a threshold, the PLL Input Conditioning board will not produce a reliable pulse train and the Reference Frequency Selector then selects the output of the 120 Hz Astable Generator to be applied to the PLL.
i.e., \( f_r = f_{r1} \cdot (AC \ ON) + f_{r2} \cdot (AC \ ON) \) \( (3.2) \)

Consequently, the PLL either generates the desired control frequency or can generate it quickly as soon as conditions permit.

The PLL is essentially a fixed frequency multiplier generating a square wave output that tracks the input pulse train \( f_{r1} \) or square wave \( f_{r2} \).

i.e., \( f_o = 240*f_r \) \( (3.3) \)

Before the PLL output is applied to the control, it goes through the start/stop inhibit block. The equation for the control frequency generator is:

\[ f_c = 240*f_r = 480*f \] \( (3.4) \)

**Monitoring of Analog Quantities**

As shown in Fig. 3.2, there are three analog quantities being monitored for the rectifier equidistant firing control - the direct current response \( I_d \), the direct current order \( I_{do} \), and the commutating voltages. These quantities provide the control error signal \( e_1 \) of equation (2.1) and the timing pulses \( C_1 \) of equation (2.6). Circuit details can be found in Chapter 5.

The Direct Current Sensor measures the direct current using opto-isolators to achieve ground isolation between the DC power circuit and the control system. Its output, \( I_d \), and the direct current setting \( I_{do} \) from a potentiometer on the mimic panel are applied to the Error Amplifier to produce:

\[ e_o = K (I_d - I_{do}) \] \( (3.5) \)

which is applied to the Analog-to-Digital Converter (ADC).
The zero-voltage crossover points of the commutating voltages (voltages across the valves) are determined by the Commutating Voltage Crossover Detectors (CVCD). Two outputs are required. The first output is a pulse train of frequency $6f$ to the ADC to initiate the digitizing process at each zero-crossing, $C_i$. The second output is a set of $6$ pulse trains, each at frequency $f$, to the Firing Pulse Generator (FPG) for implementing the minimum firing angle logic decision of equation (2.6).

The ADC output, $\theta$, is the 2's complement binary form of $e_0$ and is applied to the Control Mode Logic described in the next section. Since conversion takes about $25$ µs, the updated value of $\theta$ is available approximately $350$ µs before it must be available (for $\alpha_{\text{min}} = 8^\circ = 368$ µs). Conversion occurs at a point in the direct current waveform where normally there are no discontinuities.

**Generation of the Valve Firing Pulse**

As shown in Fig. 3.2, this section of the control receives the control error from one of several sources, processes it and generates a firing pulse which is applied to the SCR gate. The details of the blocks outlined here are found in Chapter 6. In the ultimate configuration of the control system, the control error can come from the ADC, the inverter control circuits or from a computer control. It is the function of the Control Mode Logic to determine which source is applicable and to route the digitized error to one of two registers in the Firing Pulse Generator. The FPG has two sections. The first section implements equation (2.1).

\[ \rho_i = \rho_{i-1} + 60^\circ \pm \theta_i \]
It can be seen here that if $\theta_i = 0$, this section will produce firings that are $60^\circ$ apart. Hence this section is the heart of the equidistant firing control system.

The second section - the minimum firing angle logic - implements equation (2.6).

i.e., \[ f_i = \rho_{i-1} + 60^\circ \pm \theta_i \quad \text{if} \quad \rho_i > C_i + \alpha_{\text{min}} \]

\[ f_i = C_i + \alpha_{\text{min}} \quad \text{if} \quad \rho_i < C_i + \alpha_{\text{min}} \] (2.6)

The output of the FPC then is applied to the SCR Gate Drives which produce gate signals of about $100^\circ$ duration for each valve. Optical-isolators are also used in the Gate Drives to ensure ground isolation between the SCR bridge and the control system.
4. DESIGN AND EXPERIMENTAL RESULTS OF THE
PHASE-LOCKED LOOP AND CONTROL FREQUENCY GENERATION

This chapter describes in detail the method to generate the control frequency, $f_c$, outlined in Section 3.2. The control frequency tracks the line frequency and is the master clock for the digital portion of the control. The circuit details are given for each block together with the experimental results. The design procedure for the Phase-Locked Loop is also included.

4.1 PHASE-LOCKED LOOP INPUT CONDITIONING BOARD (PIC)

As stated in Section 3.2, the PIC provides a pulse train at $f_{rl} = 2f$ Hz for the PLL input reference frequency. Fig. 4.1 is the schematic diagram for this circuit. The input filter is a 3-pole 0.1 db ripple low-pass Chebyshev filter with a cutoff frequency of 90 Hz and is based on a design [12] using a unity gain operational amplifier to achieve the complex conjugate poles. The Chebyshev filter has high cutoff rate.

The Zero-voltage comparator is a simple op-amp driven open loop with the "Zero Adjust" ensuring that the rising and falling edges of the square wave output are exactly 180° apart. Various limit circuits using diodes and zener diodes were tried in the feedback loop but the open loop configuration was the best. The comparator output is applied to the dual monostables (one triggered on the rising edge, the other on the falling edge) to get a pulse train with pulses at every zero-crossing of the input voltage. Phase A must be at least 65 VAC measured at the primary of the voltage divider to allow the PIC to produce a reliable output.

A 3-phase version of the above circuit was constructed but was abandoned because it was quite difficult to achieve and maintain the leading edges of all 6 pulses exactly 60° apart. The PLL used in this imple-
FIGURE 4.1 PHASE-LOCKED LOOP INPUT CONDITIONING SCHEMATIC
mentation is fairly sensitive to variation in the periodicity of the input and will jitter for an input which is not periodic.

4.2 ASTABLE FREQUENCY GENERATOR AND REFERENCE FREQUENCY SELECTOR

As noted in Section 3.2, the Phase-Locked Loop (PLL) has a rather long lock-up time. With no reference frequency applied to the phase detector of the PLL, the Voltage Controlled Multivibrator (VCM) in the PLL will run at its free running frequency which is considerably higher than the center frequency of 28.8 KHz. Upon applying the reference frequency, the phase detector produces an error voltage which tends to change the VCM output to the frequency and phase of the reference. Since the PLL has a long time constant, this normally takes 10 - 15 seconds. However, it is possible for the PLL to lock in on the 3rd harmonic of the input or to latch in on the free running frequency due to amplifier saturation.

To overcome these problems, a reference frequency close to the nominal frequency input is always applied to the phase detector of the PLL. The lockup time is then reduced to about 0.1 sec.

A reference frequency, \( f_{r2} \), is generated in an Astable Frequency Generator which consists of a Voltage Controlled Multivibrator (VCM) fed by a fixed voltage. See Fig. 4.2. Fig. 4.3 shows the calibration curve of the VCM for the chosen capacitance. The operating point is chosen around the knee of the curve. For \( f_{r2} = 2f_{\text{nominal}} = 120 \) Hz Square Wave,

\[
C_{x2} = 0.0047 \mu F, \quad f_0 = 28600 \text{ Hz}
\]

Divider \( N = \frac{f_0}{f_{r2}} = \frac{28600}{120} = 238.2 = 238 \)

\[
= N_0 + 16 \times N_1
\]

\[
= 14 + 16 \times 14
\]
FIGURE 4.2 ASTABLE FREQUENCY GENERATOR SCHEMATIC

- **FIGURE 4.3 CALIBRATION CURVE FOR ASTABLE FREQUENCY GENERATOR**

CONTROL RANGE

\[ C_{x2} = 0.0047 \mu F \]

28600 Hz

\[ 28k \quad 29k \quad 30k \quad 31k \quad kHz \]

\[ N (f_{r2} = 120 \text{ Hz}) \]
3 PHASE INPUT FROM VOLTAGE DIVIDER (BD 38) → DIODE BRIDGE

DIODE BRIDGE → DIFFERENTIAL AMPLIFIER

DIFFERENTIAL AMPLIFIER → THRESHOLD DETECTOR

THRESHOLD DETECTOR → TO REFERENCE FREQUENCY SELECTOR

BLOCK DIAGRAM

SCHEMATIC

FIGURE 4.4 "AC ON" DETECTOR SCHEMATIC
Normally \[ f_{r2} = \frac{f_o}{N} = \frac{28600}{238} = 120.2 \text{ Hz} \]

Figure 4.4 shows the "AC ON" Detector circuit. The differential amplifier provides buffering between the power circuit voltage divider and the control circuit. Also the threshold detector is set for a voltage where the PIC will produce a reliable \( f_{r1} \).

![Diagram of AC ON Detector Circuit]

**FIGURE 4.5 REFERENCE FREQUENCY SELECTOR**

Figure 4.5 shows the schematic for the actual Reference Frequency Selector which implements (3.2),

\[ i.e., \quad f_r = f_{r1} \cdot (AC \text{ ON}) + f_{r2} \cdot (AC \text{ ON}) \]

Thus the Reference Frequency Selector ensures that the PLL has either the desired input, \( f_{r1} \), or an input, \( f_{r2} \), which allows quick and reliable transfer to \( f_{r1} \) when conditions permit.

4.3 PHASE-LOCKED LOOP (PLL)

The circuit produces a square wave output, \( f_o \), which is an integer multiple of the line frequency and which tracks the line frequency in phase and frequency. The output is the master clock source for the digital portion of the control to be described in Chapter 6. An accurate and reliable clock source is essential to get the proper firing instant.

In the following sections, the theory and design procedure is
first described, then the circuit details explained and finally some results tabulated.

Theory and Design Procedure

A brief description of the theory and design procedure is given here. For a more detailed explanation see [13]. The description that follows is based on a design using Motorola TTL circuits. A block diagram for the PLL is given in Fig. 4.6.

The difference in phase between the reference frequency, \( f_r \), from the Reference Frequency Selector and the feedback frequency of the PLL, \( f_v \), is determined in the digital phase detector. If the inputs are in phase then the phase detector output is about 1.5 V. If there is a phase difference, the detector produces pulses of variable width between 0.75 V and 2.25 V. The pulsed output is filtered in a low-pass or a lead-lag filter before being applied to the Voltage Controlled Multivibrator which produces an output frequency dependent on the input voltage. The calibration curve for this VCM is given in Fig. 4.7. Note that the VCM is linear only over a narrow range. The output, \( f_o \), is divided down by the integer multiple of the PLL and then fed back to the phase detector.

In most applications involving phase-locked loops, such as frequency synthesis, the reference frequency is fixed and the divider is programmable. However, this application requires that the divider be fixed and output frequency track the input frequency. The design procedure noted here follows the procedure outlined in pages 19 - 37 of [13].

1. Reference pulse repetition frequency range

nominal \( f_r = 2f = 120 \) pps

maximum \( f_r = 2 \times 65 = 130 \) pps
FIGURE 4.6 BLOCK DIAGRAM OF PHASE-LOCKED LOOP

FIGURE 4.7 CALIBRATION CURVE FOR PLL VCM
minimum \( f_r = 2 \times 56 = 112 \) pps

2. Feedback divider (fixed)

\[
N = 240 = N_o + 16 \times N_1 = 16 + 16 \times 14
\]

Accuracy \( \frac{f \times 360}{f_r \times N} = \frac{f \times 360}{2 \times f \times 240} = 0.75^\circ \text{/ pulse.} \)

3. VCM range

nominal: \( f_o = N \times f_r \text{ nom} = 240 \times 120 = 28800 \text{ Hz} \)

maximum: \( f_o = (1+20\%) N \times f_r \text{ max} = 1.2 \times 240 \times 130 = 37440 \text{ Hz} \)

minimum: \( f_o = (1-20\%) N \times f_r \text{ min} = 0.8 \times 240 \times 112 = 21504 \text{ Hz} \)

The 20\% is a safety factor.

\[
\text{Ratio} \quad \frac{f_o \text{ max}}{f_o \text{ min}} = \frac{37440}{21504} = 1.74 < 3.5
\]

This range can be implemented on the MC 4024 VCM.

From Table 1, page 55 of [13]

\( K_l = 280 \)

Therefore Tuning capacitor \( C_x = \left[ \frac{K_l}{f_o \text{ max (MHz)} - 5} \right] \text{ pf} \)

\[
= \frac{280}{0.0374} - 5
\]

\[
= 0.0075 \text{ \mu F}
\]

Figure 4.7 shows the calibration curve of the VCM for two values of capacitance. A choice was made on the basis of wide bandwidth and high input voltage.

\[
i.e., \quad C_x = 0.01 \text{ \mu F}, \quad K_v = 22 \text{ KHz/volt}
\]
Phase detector gain $K_\phi = \frac{2.25 - 0.75}{2 \pi - (-2\pi)} = 0.12$ Volts/radian

Therefore loop gain, $K_{\text{loop}} = \frac{K_\phi K_v}{N} = \frac{2 \pi \times 0.12 \times 22 \times 10^3}{240} = 69.12 \text{ sec}^{-1}$

4. For a maximum overshoot $\leq 10\%$, choose $\zeta = 1.13$

5. Loop Filter.

Since the line frequency $f$ will not change very fast even for serious fault conditions, choose a 1 sec time constant for the low-pass section of the filter $\tau_1 = 1 \text{ sec} \simeq R_1 C = 0.94, R_1 = 20 \text{ K} \Omega, C_1 = 47 \mu F$

Loop bandwidth $\omega_n = \frac{K_{\text{loop}}}{\tau_1} = \frac{69.12}{0.94} = 8.58 \text{ rad/sec}$

i.e., $f_n = 1.36 \text{ Hz}$

Integrator lag section

$$\tau_2 = R_2 C = \frac{2 \zeta}{\omega_n} = \frac{2 \times 1.13}{8.58} = 0.263 \text{ sec}$$

Therefore $R_2 = \frac{0.263}{47 \times 10^{-6}} = 5.6 \text{ K} \Omega$

Therefore filter transfer function $K_F = \frac{1 + R_2 Cs}{R_1 Cs} = \frac{1 + 0.263}{0.94} s$

PLL Circuit Details

This section outlines the details of implementing the design procedure noted above and notes some of the peculiarities of this make of PLL. The schematic is shown in Fig. 4.8.

It is essential that the digital and analog sections of the PLL have their own regulated power supplies. It is hard to overdesign the power supplies to the PLL. The major source of noise on the power supplies
FIGURE 4.8 PHASE-LOCKED LOOP SCHEMATIC
FIGURE 4.8 PHASE-LOCKED LOOP SCHEMATIC
is the VCM output buffer. The first supply is for the digital phase detector and the VCM output buffer. The second supplies power for the filter input biasing and the VCM. Even with the capacitors and regulators mounted right beside the appropriate pins, it still is impossible to remove all the noise from the VCM input. Even with a separate regulator for the VCM buffer, the best solution may be a well designed PCB.

The digital phase detector determines the phase difference between the negative transitions of the two input waveforms, \( f_r \) and \( f_v \). A charge pump produces positive and negative pulses superimposed on the 1.5 VDC level corresponding to the phase difference. The duty cycle of \( f_r \) and \( f_v \) can be different but should be close. The reference signal \( f_r \) must be periodic or else instability and even out-of-lock condition of the PLL can result.

The loop filter smooths out the phase detector pulse prior to the VCM input. Use of the op-amp active filter and the op-amp bias decreases the loading on the charge pump. Since it is possible during transients to get saturation of the op-amp and consequently poor settling time, the input resistor of the integrator lag filter is split to make a low pass front end.

Loop bandwidth \( \omega_n = 8.58 \text{ r/s} \)

Low pass cutoff \( \omega_c = (5-10)\omega_n \)

Choose \( \omega_c = 100 \)

Therefore \( C_c = \frac{2}{\omega_c \left(\frac{R1}{2}\right)} = \frac{2}{100 \times \frac{20 \times 10^3}{2}} = 2.0 \text{ \mu f} \)
Since the line frequency changes slowly and over a narrow range, a long filter time constant ($\tau_l = 0.94$ sec) is used to help override noise on the ac system even though a comparatively narrow bandwidth ($f_n = 1.36$ Hz) results. This unfortunately also results in a long lockup time (10-15 sec). A characteristic of the Motorola PLL is that it can and did lock in on the third harmonic. To overcome these problems, the Astable Frequency Generator and the Reference Frequency Selector described in Section 4.2 were built.

The VCM produces an output square wave, $f_o$, dependent on the input control voltage from the loop filter and the tuning capacitance $C_x$. A tuning capacitance of 0.01 µf was chosen (see Fig. 4.7) to get a linear response over the desired frequency range, and a high control voltage even though the gain constant was high. The VCM output is fed through a divider, which in this application is fixed at $N = 240$, to produce the feedback frequency $f_v$ to the phase detector. A square wave output is taken from the divider rather than the normal pulse output [pulse width = $\frac{1}{240} \times$ (square wave width)] to try to prevent locking on other than the fundamental.

Test Results

---

![PLL Input Waveforms](image)

**FIGURE 4.9 PLL INPUT WAVEFORMS**
PLL frequency range 35 Hz - 66 Hz (slowly varying)

Lockup time: without Astable Frequency Gen. 10 - 12 sec.
with Astable Frequency Gen. 0.1 sec.

Allowable step frequency changes 55↔60 Hz
(without losing lock) 60↔64 Hz

See Fig. 4.10 for test circuit.

<table>
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<th>Initial Freq. (Hz)</th>
<th>Final Freq. (Hz)</th>
<th>Time (approx.) (sec)</th>
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<td>62</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>60</td>
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<td></td>
<td>55</td>
<td>60</td>
<td>3</td>
</tr>
</tbody>
</table>
FIGURE 4.10 CIRCUIT FOR PLL STEP FREQUENCY TESTS
4.4 START/STOP CIRCUIT

The Start/Stop Circuit inhibits the PLL output \( f_0 \) unless certain conditions have been met and initializes the control at start-up. A block diagram is shown in Fig. 4.11 and the schematic in Fig. 4.12.

![Block Diagram of Start/Stop Circuit](image)

**FIGURE 4.11 START/STOP CIRCUIT - BLOCK DIAGRAM**

The inhibit on \( f_0 \) is removed during the normal start-up sequence. Upon energizing the AC system, the commutating voltage crossover points, \( C_1 \), are detected and one of these - \( C_6 \) has been arbitrarily chosen - is applied to the start toggle. Depressing the START toggle allows the output of comparator AB to be applied to the Alpha Timer. The output pulse width of the Alpha Timer corresponds to the desired starting firing angle. The Alpha Timer resets the control and signals the Start Monostable. The Start Monostable and other signals set the Start FF to enable the PLL output. For the ALPHA TIMER:

Range of \( \alpha \) start = 5° → 160°
FIGURE 4.12 START/STOP CIRCUIT - SCHEMATIC
\[ \alpha_{\text{start}} = 230 \, \mu s \rightarrow 7.4 \, \text{ms} \]

For \( C = 0.01 \, \mu F, \; R = 500 \, \Omega \) Pot

Therefore \( \tau = 2RC = 0 \rightarrow 10 \, \text{ms} \)

\[ = 0^\circ \rightarrow 216^\circ \text{ at } 60 \, \text{Hz} \]

Although the Alpha Timer determines the instant of the first firing pulse, with the present circuit, the second firing pulse will differ depending on the error from the Error Amplifier. For a smooth start it may be desirable to override the error amplifier output for several cycles with a decaying start order or to run the converter on forced equidistant firing for several cycles. The use of a variable starting firing angle and a smooth start is required for accurate simulation of an HVDC control but for most purposes it is not necessary. It may be possible to incorporate the simultaneous start up of both the rectifier and inverter in a system controller.

The inclusion of the PLL Input Monostable ensures that \( f_0 \) is enabled at a predictable point on the waveform. The monostable pulsewidths were determined for \( f_c = 86.4 \, \text{KHz} \) when the PIC was a 3 phase unit. With \( f_c \) decreased to 28.8 KHz the START/STOP has not behaved predictably probably because the monostable pulsewidths should be lengthened by a factor of 3. The STOP toggle and other signals like the Overcurrent Protection output reset the Start FF to inhibit \( f_c \) and must be reset prior to starting up the converter.

This chapter has described the circuits to generate the master control frequency \( f_c \). Schematics and test results have been given as well as comments on design procedures and possible changes.
5. DESIGN AND EXPERIMENTAL RESULTS OF CIRCUITS TO MONITOR ANALOG QUANTITIES

This chapter details the design outlined in Section 3.2 for circuits monitoring the direct current and the commutating voltages for the error amplifier and the analog to digital converter (ADC). The outputs of the ADC and the Commutating Voltage Crossover Detectors (CVCD) are processed by the Firing Pulse Generator (FPG) to be described in Chapter 6.

With reference to Fig. 5.1, the error amplifier compares the direct current response, \( I_d \), measured by the Direct Current Sensor and the current setting \( I_{do} \) to provide an error signal, \( e_0 \), to the ADC for digitizing so the FPG can determine the next firing instant. The CVCD provides pulses to the ADC to initiate the conversion process and to the FPG for the minimum firing angle logic. The circuit details and test results for each block of Fig. 5.1 are given in the following sections.

5.1 DIRECT CURRENT SENSOR (DCS) AND ERROR AMPLIFIER

The Direct Current Sensor (DCS) gives an isolated linear output to the control corresponding to the direct current in the DC Line. The design is based on references [14] and [15].

Theory and Circuit Details

The DCS is based on using a matched pair of photo-isolators to achieve an isolated and linear output. With reference to Fig. 5.2, the ratio \( I_o/I_1 \) is constant independent of input amplitude or component temperature,

\[
\frac{I_o}{I_1} = \frac{\text{CTR}_1 (I, T_A, t)}{\text{CTR}_2 (I, T_A, t)} = \text{constant}
\]  

(5.1)
FIGURE 5.1 MONITORING ANALOG QUANTITIES - BLOCK DIAGRAM
where $CTR_1$ and $CTR_2$ are the Current Transfer Ratios of opto-isolators 1 and 2 respectively. The non-linearities are eliminated by matching the photodiode currents.

**FIGURE 5.2 DIRECT CURRENT SENSOR - BLOCK DIAGRAM**

In this application a 0.5 ohm resistance is located in the DC line to generate a voltage which is applied to a differential amplifier that provides impedance isolation between the power circuit and the DCS. The signal is then filtered in a 3-pole low-pass 0.1 db Chebyshev filter with $f_c = 10$ Hz. (See Section 4.1). Since the current response signal $I_d$ is used for slow speed control rather than for transient control or for protection, a low cutoff frequency is permissible. The voltage signal is converted to a current signal to drive the first opto-isolator. This opto-isolator provides the ground isolation between the power circuit and the control circuit. The signal is then linearized by using a second opto-isolator and finally converted back to a scaled voltage signal.
FIGURE 5.3 DIRECT CURRENT SENSOR & ERROR AMPLIFIER - SCHEMATIC
**FIGURE 5.4** DIRECT CURRENT SENSOR - TRANSFER CHARACTERISTIC

**FIGURE 5.5** DIRECT CURRENT SENSOR FREQUENCY RESPONSE
Results

The circuit was constructed on vectorboard and is mounted on the rear of the converter rack behind the mimic panel. Figure 5.3 shows the schematic diagram of the DCS and also the error amplifier to be discussed later. Figure 5.4 shows that the DCS is linear within 0.5% over the normal operating range. Figure 5.5 shows the frequency response of the DCS.

The error amplifier shown in Fig. 5.3 provides the continuous current error to the ADC from the DCS output $I_d$ and the desired current $I_{do}$. It is a unity gain summing amplifier. All appropriate points in the circuit are brought out to pins for possible breadboarding of special characteristics into the amplifier.

The amplifier equation is

$$e_o = K (I_d - I_{do})$$

$$= I_d - I_{do}$$

5.2 COMMUTATING VOLTAGE CROSSOVER DETECTOR (CVCD)

As previously stated the Commutating Voltage Crossover Detector (CVCD) has two functions: to generate "CONVERT COMMAND" pulses for the ADC and to generate timing pulses for the minimum firing angle logic in the Firing Pulse Generator.

A simple block diagram is shown in Fig. 5.6 and the corresponding schematic in Fig. 5.7. The circuitry is located on PCB 38. The operation of this circuit can best be explained with reference to Fig. 5.8 which shows the relevant waveforms and Fig. 5.6. Voltages from the precision voltage divider are compared to determine voltage crossover points $C_1$, ..., $C_6$. For example, the output of comparator AC becomes a logic "1" or high at $C_1$ when $V_A > V_C$ and logic "0" or low at $C_4$ when $V_A < V_C$. Pulses of
FIGURE 5.6 COMMUTATING VOLTAGE CROSSOVER DETECTOR BLOCK DIAGRAM

FIGURE 5.7 COMMUTATING VOLTAGE CROSSOVER DETECTOR TYPICAL SCHEMATIC
predetermined width are generated by two monostables on the rising and falling edges of the comparator output. Cross-coupling of the monostables eliminates false triggering due to noise or ringing on the comparator output. The pulsewidth represents the minimum angle $\alpha_{\text{min}}$ at which the SCR valve can be fired. The monostables have a range of 150 $\mu$s - 1.5 ms (3° - 30°). This limit represents the minimum voltage on an HVDC valve to ensure firing of all the SCR's in the valve. These pulsewidths are sent to the minimum firing angle logic section of the Firing Pulse Generator.

Outputs from all six monostables, $C_1 + \alpha_{\text{min}}$ to $C_6 + \alpha_{\text{min}}$ are also OR'd to produce a pulse train of frequency $6f$ which is then fed to a trailing edge monostable with a pulsewidth about 1.1 $\mu$s. The resultant pulse train at $6f$ Hz with 1.1 $\mu$sec pulses is the "CONVERT COMMAND" to the ADC.

5.3 ANALOG - TO - DIGITAL CONVERTER (ADC)

The Analog - to - Digital Converter (ADC) digitizes the current error so it can be used in the Firing Pulse Generator to be discussed in Chapter 6. Figure 5.1 shows how the ADC fits into the analog circuitry. As indicated in Fig. 5.9, the sampling instant of the current error is about 0.5° after the commutating voltage zero crossing and is normally far from points on the current waveform where irregularities occur. Commutation of the DC to the next valve usually occurs at $\alpha = 15° - 20°$ for rectification and $\alpha = 150° - 165°$ for inversion. A pulse train, $C_1$, from the CVCD (discussed previously) initiates the conversion process.

The ADC is an Analog Devices Model ADC-12Q with the output 0 in the 2's complement form of $e_0$. The MSB indicates error polarity and bits 2-9 the digital error.
This chapter has described the circuits used to measure the DC line current, to determine the current error, to determine the commutating voltage crossover timing pulses and to digitize the current error. Block diagrams, circuit schematics and results have also been presented.
6. DESIGN AND EXPERIMENTAL RESULTS FOR
THE EQUIDISTANT FIRING CIRCUIT

This chapter describes in detail the equidistant firing circuit as outlined in Section 3.2. Signals from the circuits described in Chapters 4 and 5 are used in this equidistant firing controller to vary the firing instant subject to certain constraints. Figure 6.1 provides a simple block diagram of the circuitry. The firing angle error can come from three separate sources. The Control Mode Logic selects the proper source and routes the error to the relevant register in the main circuit of the Firing Pulse Generator. The main circuit which in essence is the equidistant controller determines the new firing instant. The decoder routes the firing instant pulse to the correct valve and the minimum firing angle logic ensures there is sufficient voltage across the valve prior to firing. The SCR Gate Drives convert the firing instant pulse in the control to a gate pulse on the power SCR. The following sections provide more detail for the individual circuits. The theory underlying these circuits can be found in Chapter 2.

6.1 CONTROL MODE LOGIC (CML)

As mentioned above the Control Mode Logic (CML) routes the control error to one of two registers in the Firing Pulse Generator (FPG) main circuit. A negative error ($\Theta < 0$) requires the firing instant to be sooner, that is, the firing angle $\alpha$ is to be decreased. Consequently the error is routed to the Phase Reduction Register (PRR). A positive error ($\Theta > 0$), similarly, is routed to the Phase Advance Counter (PAC) to increase $\alpha$. For zero error ($\Theta = 0$) a zero error signal is applied to both the PRR and PAC. A non-zero error can only be in one register at any time.
FIGURE 6.1 GENERATION OF VALVE FIRING PULSES - BLOCK DIAGRAM
As presently constructed, Θ can come from three sources: the ADC, the inverter control circuits or the computer control circuits. Table 6.1 indicates the routing of Θ for different control modes and polarities. At this time the inverter control circuits and the computer circuits have not been connected into the control. Consequently the status signals from these circuits have been connected to switches to allow testing of the CML and the error inputs have been connected to ground or supply as appropriate.

Using Boolean algebra the equations for enabling the two registers can be written from Table 6.1 as follows:

(Enable the PRR) = (PRR = 1)
= ADC \cdot \overline{CP} \cdot CC1 \cdot CC + ADC \cdot \overline{CP} \cdot CC1 \cdot OWCC
+ ISC \cdot \overline{CP} + PRRC \quad (6.1)

(Enable the PAC) = (PAC = 1)
= ADC \cdot \overline{CP} \cdot CC1 \cdot CC + IOC \cdot \overline{CP} + PACC \quad (6.2)

The above two equations determine which register is to contain the non-zero Θ and now we must choose the appropriate source. Table 6.2 indicates the binary code on the control lines A and B to select the appropriate error source. The PRR requires an input corresponding to Θ = 0. Putting all 8 error bits to "1" on channel C3 meets this requirement. The equations for the channel selectors can be written from Table 6.2 and equations (6.1) and (6.2).

Phase Reduction Register

\begin{align*}
C0 &= ADC \cdot \overline{CP} \cdot CC1 \cdot CC + ADC \cdot \overline{CP} \cdot CC1 \cdot OWCC \\
C1 &= ISC \cdot \overline{CP} \\
C2 &= PRRC
\end{align*}
C₃ = \overline{PRR} = \text{All inputs "1" (2's complement negative zero)}

\text{**. A₁ = ISC} \cdot \overline{CP} + \overline{PRR} = ISC \cdot CP \cdot PRR \quad (6.3)

\text{**. B₁ = PRRC} + \overline{PRR} = PRRC \cdot PRR \quad (6.4)

\text{Phase Advance Counter}

C₀ = \text{ADC} \cdot \overline{CP} \cdot \overline{CC¹} \cdot CC

C₁ = \text{IOC} \cdot \overline{CP}

C₂ = \text{PACC}

C₃ = \overline{PAC} = \text{All inputs "0" (2's complement positive zero)}

\text{**. A₂ = IOC} \cdot \overline{CP} + \overline{PAC} = IOC \cdot CP \cdot PAC \quad (6.5)

\text{**. B₂ = PACC} + \overline{PAC} = PACC \cdot PAC \quad (6.6)

Implementing (6.1) and (6.2) gives:

PRR = \text{ADC} \cdot \overline{CP} \cdot \overline{CC¹} \cdot CC \cdot \text{ADC} \cdot CP \cdot \overline{CC¹} \cdot OWCC \cdot ISC \cdot CP \cdot PRCC \quad (6.7)

PAC = \text{ADC} \cdot \overline{CP} \cdot \overline{CC¹} \cdot CC \cdot IOC \cdot \overline{CP} \cdot \overline{PACC} \quad (6.8)

Figure 6.2 is the schematic showing the implementation of the above equations and Fig. 6.3 is a block diagram showing the control error routing. The CML routes the error into the appropriate register in the main circuit of the FPG which is discussed next.

6.2 \text{FIRING PULSE GENERATOR (FPG)}

As mentioned at the beginning of this chapter, the Firing Pulse Generator (FPG) generates the firing pulses to fire the valves. The main circuit implements equation (2.1), the decoder determines the next valve to fire and the minimum firing angle logic implements equation (2.6). The following sections describe the three sections.
### TABLE 6.1

**ROUTING OF CONTROL ERROR**

<table>
<thead>
<tr>
<th>ERROR SOURCE &amp; CONTROL MODE</th>
<th>STATUS SIGNALS</th>
<th>REGISTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Rectifier Current Control (CC = 1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CC1 = 1</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>CC1 = 0</td>
<td></td>
</tr>
<tr>
<td>Inverter One Way Current Control</td>
<td>OWCC = 1</td>
<td>X</td>
</tr>
<tr>
<td>Inverter MEA Control</td>
<td>ISC = 1</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>IOC = 1</td>
<td></td>
</tr>
<tr>
<td>Computer Control (CP = 1)</td>
<td>PRCC = 1</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>PACC = 1</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:**

ADC = 1 is a 1.5 µs pulse after ADC conversion is complete.
## TABLE 6.2
DATA CHANNEL SELECTOR CODING FOR ROUTING OF CONTROL ERROR

<table>
<thead>
<tr>
<th>CHANNEL SELECTOR (MC8309)</th>
<th>ERROR</th>
<th>SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHANNEL</td>
<td>CHANNEL SELECTOR INPUTS</td>
<td>PRR</td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>C0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>C3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 6.2 CONTROL MODE LOGIC - SCHEMATIC
FIGURE 6.3 CONTROL ERROR ROUTING - BLOCK DIAGRAM
FIGURE 6.4 FIRING PULSE GENERATOR BLOCK DIAGRAM
Main Circuit

The main circuit implements the equidistant firing according to:

$$\rho_i = f_{i-1} + 60^\circ \pm \theta_i$$  \hspace{1cm} (2.1)

For $\theta_i = 0$, i.e. no control error, this circuit will ensure that all subsequent firings are $60^\circ$ apart. The operation of the circuit can be explained by referring to Fig. 6.4.

Assume that $\theta_0 = 0$ and that both PRR and PAC contain zero errors, i.e., CPRR = 1111 1111 and CPAC = 0000 0000 respectively. Thus the decoded output of PAC which is a down counter is high to G2 allowing the C output to go directly to the decoder. At instant $f_{i-1}$ a number corresponding to $60^\circ$ is loaded into D an up-counter and is then counted to $0^\circ$ by $f_c$ the control frequency from the PLL (see section 4.4). The comparator C output goes high when the number in D is greater than or equal to the control error contained in PRR,

$$i.e., \quad C = 1 = (D \geq CPRR)$$  \hspace{1cm} (6.9)

C inhibits further counting of D. Since $\theta_i = 0$, C goes high $60^\circ$ after $f_{i-1}$ and a "1" is sent to the decoder. The process is repeated when D is reloaded after $f_i$ occurs.

The binary number for $60^\circ$ is generated as follows.

Since $$f_c = 480 \times f,$$

it takes $\frac{480 \times f}{360 \times f} \times 60 = 80$ pulses of $f_c$ to count $60^\circ$. Since the D output must equal CPRR = 1111 1111 after 80 pulses for $\theta = 0$, the number 1010 1111 is loaded into D at each $f_i$,

$$i.e., \quad \begin{array}{c}
1010 \ 1111 \text{ loaded number} \\
+ \ 0101 \ 0000 \quad 80 = 60^\circ \\
1111 \ 1111 \text{ CPRR negative zero}
\end{array}$$
If the feedback divider of the PLL is changed, then the number loaded into D must be reprogrammed accordingly. D is loaded on the initial start by a pulse from the Start Monostable since $f_1$ pulses are not available.

Assume now that $\theta_1 < 0$ meaning that the firing should be sooner (smaller $\alpha$). The PRR contains the control error $\theta_1$. The PAC contains zero and G2 is enabled to allow the C output to go directly to the decoder as above. At $f_1$ D starts to count up. However, PRR contains a binary number smaller than before so the C output goes high sooner by the amount of time the firing is to be sooner. As before, the output goes directly to the decoder and stops D counting.

Assume now that $\theta_1 > 0$ meaning that the firing should be delayed (higher $\alpha$). The PRR contains zero and the PAC contains $\theta_1$. G2 is not enabled since CPAC ≠ 0. As for the case of $\theta_1 = 0$, D is up-counted until its output is the same as the contents of PRR (CPRR = 1111 1111). This takes a period of 60°. C now goes high stopping the counting of D, enabling G2 so the PAC output can go to the decoder and enabling G1 to start the down-counting of PAC. When the PAC output is zero, the decoder receives a high output from G2.

The main circuit of the FPG generates a set of serial pulses corresponding to the desired firing instants $\rho_1$ which are then decoded to determine which of the six valves is to be fired.

Normally a rectifier is run at $\alpha = 15^\circ - 20^\circ$ and an inverter at $\alpha = 150^\circ - 165^\circ$ which means that D is partially up-counted when the new error is entered into PRR and PAC. Since $\theta_1$ is entered about $C_1 + 0.5^\circ$ and for normal rectification firing is not permitted until $C_1 + \alpha_{\text{min}}$ which is $5^\circ - 10^\circ$ later there is no problem. If firing is at say $\alpha = 60^\circ - 70^\circ$ or $120^\circ - 130^\circ$, the current may see the commutation discontinuities but
these would be filtered out in the low-pass filter of the DCS described in Section 5.1.

Decoder

From the set of serial pulses from the main circuit, the decoder section determines which valve is to be fired. Referring to Fig. 6.4, the decoder section consists of a counter and a decoder. The module - 6 ring counter [16] consists of three J-K Flip-Flops and their outputs are decoded to give $q_i$ pulses which in turn are NANDed with G2 output to produce negative going pulses $\overline{q_i}$ for the minimum firing angle logic. The falling edge of the pulse is determined by the decoded output of the ring counter (i.e., $p_i$). The rising edge of the pulse is determined by the minimum firing angle logic.

Minimum Firing Angle Logic

The minimum firing angle logic ensures that there is sufficient positive voltage across the valve prior to firing. Normal AC voltages are assumed. Although the logic is useful during rectification it does not interfere with inverter control so is not inhibited for that mode of operation. This circuit implements the following equation

$$f_i = \rho_i = f_{i-1} + 60° \pm \theta_i \quad \text{if} \quad \rho_i > C_i + \alpha_{\text{min}}$$

$$= C_i + \alpha_{\text{min}} \quad \rho_i < C_i + \alpha_{\text{min}}$$

Consider first the normal operation of this circuit indicated by the first line of equation (2.6). Referring to Fig. 6.4, the $C_i + \alpha_{\text{min}}$ signal from the CVCD discussed in Section 5.2 is applied to a monostable which sets the Flip-Flop and drives one input of the NOR low. The NOR $R_i$ output remains low. The monostable is used to get a short duration pulse.
Normally the firing instant is after $a_{\text{min}}$ and when $q_i$ (firing instant from the decoder for the correct valve) arrives, it drives $R_i$ high. This also causes $f_{i-1}$ to go high and reload the up-counter D to start calculation of the next firing instant. The C output goes low, G2 goes low and the $q_i$ returns to the high state which returns $R_i$ to the low state. Consequently a short pulse $R_i$ (pulse width equals the sum of the propagation delays in the FPG) is applied to the firing pulse monostable to give two outputs. The first output is the firing pulse to the Gate Drive Circuit and the second output resets the FF. The pulse width has been fixed at about 100° to obtain a hard-drive gate pulse.

Consider the second line of equation (2.6) where the calculated firing instant is sooner than it should be. On an HVDC system this can occur while the converter transformer is undergoing a tap change or during a system disturbance. Signal $q_i$ becomes low at the calculated firing instant but the NOR output $R_i$ remains low until it receives a low output from the FF at $C_i + a_{\text{min}}$. The rest of the sequence is identical to that above.

Thus the Firing Pulse Generator uses the digital error given by the CML to produce equidistant firing signals for the SCR Gate Drives. The FPG basically works but testing with a running converter can not be done as explained in the next section.

6.3 SCR VALVE GATE DRIVES

As mentioned in Section 3.2, the Gate Drives convert the firing signals from the minimum firing angle logic in the FPG into firing pulses for the gates of the SCR's in the converter bridge. Ground isolation is achieved in these circuits. The Gate Drive circuit is based on references [17] and [18].
Referring to Fig. 6.5, the firing pulse from the FPG drives the LED of an opto-SCR which discharges the energy stored in the capacitor into the gate of the power SCR. The opto-SCR provides 1500 volts ground isolation between the control and power circuits. The resistor divider protects the 200 Volt opto-SCR from the normal 3Ø 208 VAC and also determines the capacitor charging rate. The 47 ohm resistor and the zener diode protect the power SCR gate from overcurrent and overvoltage respectively.

The circuit was breadboarded in a single SCR circuit and worked well for varying firing angles and AC voltages. A three phase bridge was constructed for the converter and inserted into the closed loop system. However, the system did not work in closed-loop configuration. The problem appears to be in the Gate Drives since the six firing pulses have
little or no resemblance to each other nor to the expected waveshape. There were no obvious construction or design errors.

Although the FPG was not completely debugged and trimmed in, it did produce firing pulses that should have started the rectifier. A number of items could be investigated on the Gate Drives. The use of a short but high current firing pulse, say 10 - 25 μsec with 100 - 500 mA, could replace the present 4.6 msec, 30 mA LED pulse. The opto-SCR could be moved closer to the gate to minimize the distance the gate pulse must travel. The use of a pulse transformer could be tried. For the use of an opto-SCR, it may be necessary to match gate drive characteristics for each power SCR.

This chapter has described the circuits associated with the Control Mode Logic (CML) which routes the error signal into the Firing Pulse Generator (FPG) so that a firing pulse can be sent to the Gate Drives. Block and schematic diagrams for the CML, the FPG and the Gate Drives have been presented. The Gate Drive circuit was described and several ideas for modification were presented to make the circuit work properly.
7. CONCLUSIONS AND RECOMMENDATIONS

This thesis has described a physical HVDC converter model. The design and construction of a 6-pulse HVDC converter rack compatible with the existing micro-machine AC system model has been outlined. The theory and design of a digital equidistant control system for the converter has been presented. The construction and test results of a rectifier control system has also been described. Some of the features of this system follow.

The phase-locked loop used in this control generates a reliable and accurate control frequency. Since the phase-locked loop tracks the AC system frequency over a wide range and for large step changes rather than depending on the AC voltage waveform, the control is insensitive to normal AC asymmetry and distortion. This allows the converter to be connected to weak AC systems. A high phase-locked loop frequency ensures accurate firing down to ±0.75°.

A circuit to provide a linear ground isolated signal has been constructed to measure DC line current. The simple error amplifier can easily accommodate modifications for experimental work. The analog front end of the control presently allows rectifier current control but other control parameters can easily be implemented. The converter rack itself has breadboarding facilities and a mimic panel to allow simple test connections.

The firing circuit has been constructed to allow a maximum expansion flexibility. The control logic can accept signals from future inverter control or computer control circuits. The SCR gate drives should be modified. Possible modifications include using a short duration high current pulse to turn on the opto-SCR, using another make of opto-SCR,
matching individual gate characteristics for each power SCR and using pulse transformers.

The converter rack can then be used as part of a model HVDC link. Inverter control circuits have to be added in order to obtain a true bidirectional converter. Depending on requirements, all or part of the converter could be duplicated to make an equidistant HVDC control system. The converter could then be connected to a higher level system controller which has been designated as computer control. The higher level controller could replace some of the existing control or could supplement it. The model could then be used to study HVDC system control, voltage control and AC/DC interactions.
BIBLIOGRAPHY


Function Diagrams for Integrated Circuits

Fairchild Semiconductor

f 7805

Although no output capacitor is needed for stability, it does improve transient response.

Required IF regulator is located an appreciable distance from power supply filter.

Basic Fixed Output Regulator

9N00/5400, 7400

9308

9324

9366/54193, 74193
## MOTOROLA SEMICONDUCTOR PRODUCTS

(Numbers in parenthesis indicates loading with other devices in same MC family)

<table>
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<th>MC3002/MC3102</th>
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<tr>
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<td><strong>Quad 2-Input AND Gate</strong></td>
<td><strong>Quad 2-Input NOR Gate</strong></td>
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<td>( P_{D} = 0.8 \text{ mW typ/pkg} )</td>
<td>( P_{D} = 1.2 \text{ mW typ/pkg} )</td>
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<th>MC3005/MC3125</th>
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<tr>
<td><strong>Quad 2-Input OR Gate</strong></td>
<td><strong>Quad 2-Input NAND Gate</strong> (Open Collector)</td>
<td><strong>Triple 3-Input NAND Gate</strong></td>
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<th>MC3010/MC3110</th>
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<tbody>
<tr>
<td><strong>Triple 3-Input AND Gate</strong></td>
<td><strong>Triple 3-Input NAND Gate</strong> (Open Collector)</td>
<td><strong>Dual 4-Input NAND Gate</strong></td>
</tr>
<tr>
<td><img src="image7.png" alt="Diagram" /></td>
<td><img src="image8.png" alt="Diagram" /></td>
<td><img src="image9.png" alt="Diagram" /></td>
</tr>
<tr>
<td>( t_{pd} = 9.0 \text{ ns typ} )</td>
<td>( t_{pd} = 8.0 \text{ ns typ} )</td>
<td>( t_{pd} = 6.0 \text{ ns typ} )</td>
</tr>
<tr>
<td>( P_{D} = 0.6 \text{ mW typ/pkg} )</td>
<td>( P_{D} = 0.6 \text{ mW typ/pkg} )</td>
<td>( P_{D} = 0.4 \text{ mW typ/pkg} )</td>
</tr>
</tbody>
</table>
MOTOROLA (cont'd)

### MC4015

**Quad Type D Flip-Flop**

- **Q3**: 06, 07 (10)
- **Q1**: 01 (10)
- **Q2**: 09, 10 (10)
- **Q0**: 00, 11 (10)

**Pinout**
- **Gnd**: Pin 7
- **VCC**: Pin 14

**Pd** = 190 mW typ/pkg

\[ \text{pd} = 16 \text{ ns typ} \]

**Note:**
- Gnd = ground pin
- Vcc = power pin
- **pD** = Propagation Delay

### MC4023

**4-Bit Universal Counter**

- **Q3**: 09 (10)
- **Q2**: 08 (10)
- **Q1**: 07 (10)
- **Q0**: 06 (10)

**Pinout**
- **Vcc**: Pin 14
- **Gnd**: Pin 7

\[ \text{pd} = 30 \text{ MHz typ} \]

**Pd** = 200 mW typ/pkg

### MC4024/MC4324

**Dual Voltage-Controlled Multivibrator**

- **VCC**: 5 V
- **VCM**: 1.13 V
- **Output Buffer**: 14

**Pinout**
- **Vcc**: Pin 14
- **Gnd**: Pin 7

\[ \text{pd} = 150 \text{ mW typ/pkg} \]

**f** = 30 MHz typ

### MC4044/MC4344

**Phase-Frequency Detector**

- **U1**: Phase-Freq. Detector 1
- **U2**: Phase-Freq. Detector 2

**Pinout**
- **Vcc**: Pin 14
- **Gnd**: Pin 7

\[ \text{pd} = 9.0 \text{ ns typ} \]
<table>
<thead>
<tr>
<th>Device Code</th>
<th>Description</th>
<th>Input/Output</th>
<th>Timing</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC5400/MC7400</td>
<td>Quad 2-Input NAND Gate</td>
<td>11-12</td>
<td>tpd = 10 ns typ</td>
<td>PD = 40 mW typ/pkg</td>
</tr>
<tr>
<td>MC5401/MC7401</td>
<td>Quad 2-Input NAND Gate</td>
<td>11-12</td>
<td>tpd = 35 ns typ</td>
<td>PD = 40 mW typ/pkg</td>
</tr>
<tr>
<td>MC5402/MC7402</td>
<td>Quad 2-Input NOR Gate</td>
<td>11-12</td>
<td>tpd = 10 ns typ</td>
<td>PD = 40 mW typ/pkg</td>
</tr>
<tr>
<td>MC5403/MC7403</td>
<td>Quad 2-Input NAND Gate</td>
<td>11-12</td>
<td>tpd = 35 ns typ</td>
<td>PD = 40 mW typ/pkg</td>
</tr>
<tr>
<td>MC5410/MC7410</td>
<td>Triple 3-Input NAND Gate</td>
<td>11-12</td>
<td>tpd = 10 ns typ</td>
<td>PD = 30 mW typ/pkg</td>
</tr>
<tr>
<td>MC5420/MC7420</td>
<td>Dual 4-Input NAND Gate</td>
<td>11-12</td>
<td>tpd = 10 ns typ</td>
<td>PD = 20 mW typ/pkg</td>
</tr>
</tbody>
</table>

**Hex Inverters**

<table>
<thead>
<tr>
<th>Device Code</th>
<th>Description</th>
<th>Timing</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC5404/MC7404</td>
<td>Hex Inverter</td>
<td>tpd = 13 ns typ</td>
<td>PD = 60 mW typ/pkg</td>
</tr>
<tr>
<td>MC5405/MC7405</td>
<td>Hex Inverter</td>
<td>tpd = 35 ns typ</td>
<td>PD = 60 mW typ/pkg</td>
</tr>
</tbody>
</table>

**MC7476 Dual J K Flip-Flop**

- tpd = 15 ns typ
- PD = 80 mW typ/pkg

**Truth Table**

- J: 4
- K: 6
- Set: 2
- Reset: 8
- Clock: 1

**Timing Specifications**

- tpd = 15 ns typ
- PD = 80 mW typ/pkg

**Power Supply**

- VCC = Pin 5, GND = Pin 13
MC5493/MC7493
4-Bit Binary Counter

\[ V_{CC} = \text{Pin 5} \]
\[ \text{Gnd} = \text{Pin 10} \]

<table>
<thead>
<tr>
<th>COUNT</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ t_{pd} = 20 \text{ ns typ/bit} \]
\[ P_D = 160 \text{ mW typ/pkg} \]

MC6309/MC9309
Dual 4-Channel Data Selector

\[ Z = \overline{A} \overline{B} X_0 + A B X_1 + \overline{A} B X_2 + AB X_3 \]
\[ W = \overline{A} B Y_0 + A B Y_1 + AB Y_2 + AB Y_3 \]

\[ t_{pd} = 9.0 \text{ to } 24 \text{ ns typ} \]
\[ P_D = 150 \text{ mW typ/pkg} \]

MC8601/MC9601
Retriggerable Monostable Multivibrator

\[ t_{pd} = 25 \text{ ns typ} \]
\[ P_D = 75 \text{ mW typ/pkg} \]

MC9601, MC8601
DM7000/DM8000 (SN5400/SN7400)
Quad 2-Input Gate

DM7010/DM8010 (SN5410/SN7410)
Triple 3-Input Gate

DM7500/DM8500
(SN5476/SN7476)
Dual J-K Flip Flop with Preset and Clear Inputs

TEXAS INSTRUMENTS

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

<table>
<thead>
<tr>
<th>CLEAR</th>
<th>A</th>
<th>B</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>↑</td>
</tr>
<tr>
<td>H</td>
<td>↓</td>
<td>H</td>
<td>L</td>
<td>↑</td>
</tr>
<tr>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>↑</td>
</tr>
</tbody>
</table>

See page 138
OPERATIONAL AMPLIFIERS

MOTOROLA

MC1741

EQUIVALENT CIRCUIT SCHEMATIC

NATIONAL SEMICONDUCTOR

LM 311

NOTE: Pin 5 connected to bottom of package.
TOP VIEW
APPENDIX B

AC SYSTEM LINE TO NEUTRAL VOLTAGES

"CONVERT COMMAND"  +1.1 μsec

ERROR INTO PAC/PRR

f_i

C_i + α_min

C_i+1 + α_min

C_i+2 + α_min

q_i

R_i

f_i

f_i+1

f_i+2

\( t \) (s)

ERROR = q_i = 0; \( α_{\text{min}} = 0° \); \( α = 15° \); SYMMETRICAL AC SYSTEM

CONVERTER CONTROL TIMING DIAGRAM