A Study of Substrate Noise in Mixed-Signal Integrated Circuits

by

Mohammad Hekmat

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Abstract

Integrating analog and radio-frequency (RF) circuits with digital blocks on a CMOS system-on-a-chip (SoC) has drawn a lot of attention, recently. One major obstacle at this high level of integration is the substrate noise, which results in undesired interaction between these circuits through the common substrate. Analog circuits are the main victims of such interactions; consequently, understanding the behaviour of substrate noise and performance degradations it causes, is indispensable for analog designers.

This work addresses three aspects of substrate noise. First, substrate noise is characterized in the time and frequency domains to identify major parameters that control substrate noise generation, propagation, and reception. Effects of many parameters on the amount of noise generation and coupling are also studied.

Second, this thesis investigates the noise impact on analog circuits from a circuit-level point of view by introducing a new small-signal model of the MOS device, which accounts for the substrate noise effects. While most works have focused on system-level or signal-level analysis, study of the noise from a circuit-level point of view is more beneficial for analog designers because it gives them more insight on how to improve the substrate noise rejection capability of their designs.

Finally, noise reduction techniques are revisited in this work. The use of passive guard-rings is reviewed in detail and the effects of many design parameters on the amount of noise attenuation provided by these structures are studied. The behaviour of guard-rings in different substrates are also discussed.
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List of Abbreviations

ADC  Analog-to-Digital Converter
BEM  Boundary Element Method
CBL  Current Balanced Logic
CCBL Complementary Current Balanced Logic
DAC  Digital-to-Analog Converter
DNC  Device Noise Coefficient
DNF  Device Noise Factor
FDM  Finite Difference Method
FSCL Folded Source Coupled Logic
GPS  Global Positioning System
LNA  Low-Noise Amplifier
PLL  Phase-Locked Loop
SAS  Switching Activity Spreading
SCL  Source Coupled Logic
SNC  Substrate Noise Coefficient
SNF  Substrate Noise Factor
SNR  Signal-to-Noise Ratio
SoC  System-on-a-Chip
SOI  Silicon-on-Insulator
SSN  Simultaneous Switching Noise
VCO  Voltage-Controlled Oscillator
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Chapter 1

Motivation

1.1 Challenges of Analog CMOS Circuits in SoCs

Continuous scaling in CMOS technology has provided improved device performance and lower cost in digital circuits over the past three decades. The proliferation of CMOS digital circuits has augmented the demand for CMOS analog and RF circuits, which were previously implemented in Bipolar or BiCMOS technologies. However, since CMOS processes have traditionally been optimized for digital applications, they are not ideal candidates for analog purposes owing to several shortcomings such as the inherent low drive capability of active devices, the relatively poor quality of on-chip passive elements, and the low power supply requirement imposed by digital applications. Despite these difficulties, analog designers have managed to develop successful CMOS analog and RF blocks with novel architectures and design techniques [1].

The feasibility of using CMOS in analog circuits has motivated people toward higher levels of integration and, ultimately, a system-on-a-chip (SoC) that will be a combination of digital, analog, and RF circuits. Figure 1.1 shows a simplified block diagram of an SoC with multi-standard RF front-end, analog-to-digital converter (ADC), digital-to-analog converter (DAC), and baseband signal processing blocks as well as other logic and digital
motivation.

units. Such SoCs will result in considerable reduction in cost, in power consumption, and in form factor, each of which are of crucial importance in handheld devices.

Recently, mixed-signal SoCs have drawn a lot of attention, as shown in Table 1.1 [2-13], especially for wireless applications; however, designing an SoC is not as trivial as putting a few blocks on the same chip. An immediate problem in abutting analog and digital blocks is the signal integrity issue and, more specifically, substrate noise effect, which is defined as the problem of performance degradation (mostly in analog blocks) due to the activity of neighbouring digital circuits.

The substrate noise issue is even more noticeable, when one realizes that many of the works in Table 1.1 have denoted substrate noise as their major challenge for single-chip integration. Those results are in addition to the published results on performance degradations of individual analog blocks such as ADCs, phase-locked loops (PLLs), and low-noise amplifiers (LNAs). Furthermore, one can anticipate that the problem will be further aggravated in future SoCs because of the increasing complexity of digital functions.

![The block diagram of a multi-standard SoC.](image)
and faster clock switchings. All these issues, coupled with the overall challenges in analog CMOS design, present a picture of the problem where understanding substrate noise would obviously be indispensable.

### 1.2 Research Goals

This research is intended to provide an intuition into the issue of substrate noise and how it can affect the performance of critical blocks in a mixed-signal SoC, especially in RF and analog parts. It targets three research areas: the first is the study of substrate noise in both the time and frequency domains and the analysis of the effect of several parameters such as clocking frequency and package parasitics on the behaviour of the noise. Additionally, some technological aspects, such as the effect of the substrate type on noise propagation and generation, will be explored; therefore, characterization is one of the primary concerns of this part of the work.

In the second part, the impact of substrate noise on the performance of LNAs, as a
representative sensitive analog block, will be studied. This is achieved through a new approach using a proposed MOS device model that accounts for substrate noise effects. Previous work on the same topic has merely considered the problem from a signal analysis aspect; however, our goal is to approach it from a circuit design point of view, which allows for an intuitive perspective on how design parameters can be changed to reduce the effect of substrate noise.

Efficient techniques to mitigate the performance degradation caused by substrate noise will be required more and more in future SoCs; thus in the last part of the work, we evaluate the efficiency of existing noise reduction methods and trade-offs in using them. After all, the goal of this research is to show that substrate noise has added new complexity to analog circuit design in mixed-signal SoCs; therefore, to achieve successful designs, it is necessary to take substrate noise into account during the design stage.

1.3 Thesis Organization

This thesis is organized as follows: first, Chapter 2 gives an overview of the substrate noise problem and briefly, discusses the previous research on this topic. Next, Chapter 3 discusses the characterization of substrate noise both theoretically and through simulations. Supply noise as a main contributor to external substrate noise sources will be studied in detail. This chapter also analyzes the impact of the substrate type on noise propagation behaviour, as well as the effect of various parameters on the amount of noise both in the time and frequency domains.

Modelling the effect of substrate noise on the performance of analog CMOS circuits
is of crucial importance; therefore, a separate chapter focuses on this topic. As such, Chapter 4 will review a general model for noise analysis in MOS circuits, which will be modified for substrate noise analysis purposes. Based on the new model, the effect of substrate noise on a typical LNA in an RF system will be studied.

Chapter 5 explores substrate noise reduction techniques. The relationship between the efficiency of these methods and several parameters such as frequency, digital activity, and physical separation will be investigated. Finally, Chapter 6 presents concluding remarks and suggestions for future work.
Chapter 2

Background

Most modern communication systems use complicated digital signal processing blocks, the activity of which affects the performance of sensitive analog circuits through interactions via the on-chip parasitics and the common substrate. Such interactions are mostly classified as noise because, by definition, any unwanted fluctuation in analog or digital signals will be considered as noise. In this thesis, substrate noise is meant to be the undesired effects of neighbouring blocks on each other in an SoC, which is propagated through the common substrate. It should be noted that, in contrast to white noise, this type of noise is not totally random but depends on the activity in different parts (mainly digital of the chip); therefore, one can consider it as pseudo-random noise.

In general, the maximum tolerable amount of noise is determined by the application and the standard. In some applications such as GPS a very stringent noise requirement is imposed, whereas others, such as Bluetooth, have a more relaxed noise margin. This has been the main obstacle in achieving single-chip solutions in certain applications. For example, as was shown in Table 1.1, the single-chip GPS was introduced much later than other wireless standards despite its relative simplicity.

The problem of performance degradation due to the activity of digital circuits was first observed in the 1980s [14], even before the introduction of mixed-signal SoCs. Most
early researchers studied this phenomenon under the name of *switching noise*. However, this type of noise applies mostly to digital circuits and refers to the variations of supply and ground voltage due to the switchings in digital circuits. Analog circuits are affected by switching in digital parts not only by supply and ground variations but also by other mechanisms such as body effect that are not addressed in switching noise analysis; therefore, analog circuits do not fit exactly into the context of switching noise, but as will be seen, substrate noise is closely related to switching noise; therefore, understanding the behaviour of switching noise is helpful in substrate noise analysis.

Early researchers in the field of switching noise mostly focused on the calculation of the maximum amount of noise without taking into account its time or frequency domain behaviour [15, 16]. It was not until the early 1990s that the first report on the substrate noise problem was published in [17]. Later, a seminal work in the study of substrate noise was reported in [18], where substrate noise was studied in the time-domain, and mostly the capacitive coupling of the noise was taken into account; therefore, packaging issues and the relationship between supply noise and substrate noise were neglected. Furthermore, a simple digital circuit had been used in their analysis; therefore, in later studies more complicated digital blocks were used as noise generators to explore the effect of various switching patterns on the behaviour of noise [19, 20].

In addition to the behaviour of noise in time domain, the frequency content of the noise is important in RF applications because mainly the in-band portion of the noise or those components that may create in-band intermodulation terms are of significance; therefore, subsequent researchers included the analysis of noise in the frequency-domain in their studies [19–21].
In general, the research on substrate noise falls into one of four major categories:

- Those focusing on substrate noise characterization either in the time or frequency domain [18–20, 22].
- Those studying the effect of substrate noise on the performance of certain analog blocks [21, 23–25].
- Those concerned about the modelling of the noise and CAD tool development [26–29].
- Those concentrating on noise reduction techniques [30–32].

In the following sections, we will explain the basic aspects of substrate noise problem and comment on issues in its characterization and modelling. We will also review the prior work on this topic and discuss their merits and shortcomings.

### 2.1 Substrate Noise Characterization

The substrate noise coupling mechanism can be modelled in three steps, as conceptually illustrated in Figure 2.1 [21]. First, the noise is generated and injected by digital circuitry into the substrate. Next, it travels through the substrate and finally couples back to sensitive analog nodes. As shown in this figure, there exists another way for the noise to transfer to analog nodes, which is by means of supply lines. It should be noted that the substrate is well connected to the supply lines through substrate contacts; therefore, any voltage variation on the supply lines will couple to the substrate and reach analog bulk nodes. We will address this issue later, because even though in this case the noise does
not directly go through the substrate, it couples back to the analog nodes using substrate contacts. As a result, this noise manifests itself through substrate contacts and changes the substrate voltage, hence it can be considered as substrate noise.

### 2.1.1 Noise Injection into the Substrate

All currents injected into the substrate will cause variations of substrate voltage that can couple back to the analog nodes. These currents can originate from various sources, such as the charging and discharging of load or parasitic capacitances, device leakage currents, etc.

In digital CMOS circuits, substrate noise is generated by two major mechanisms, namely the capacitive coupling from the switching nodes (mainly transistor terminals) and the noise from supply or ground lines due to the parasitic impedances of these lines [33]. While the former comes from the direct coupling of digital switchings through parasitic capacitances to the substrate, the latter mainly results from the voltage drop across parasitics of bondwires and package pins. It should be noted that the capacitive coupling
is inevitable because the parasitic capacitances of diffusion areas are due to the physical layout of the circuit and cannot be eliminated; however, the noise due to supply can be reduced using better packaging (with lower parasitic inductance) or on-chip decoupling capacitances.

### 2.1.2 Noise Propagation through the Substrate

Once the noise is generated in the digital blocks, it will propagate all over the chip through the common substrate. Up to several GHz, the silicon substrate can be considered a resistive medium [26]; therefore, any perturbation at any node of such a network will potentially cause voltage fluctuations at all other points. While the amount of noise injection and reception depends on the impedance of the injection and reception points and supply contacts, the key parameter in noise propagation is the impedance of the substrate path.

Since the electrical properties of the substrate are the main factors in the noise propagation behaviour, various studies have focused on investigating the effect of substrate type on the noise [18, 21, 22, 33–35]. Typically, the higher the resistance of the substrate the better the noise rejection performance; therefore, more advanced processes, such as SOI, are anticipated to be better in terms of substrate noise rejection. Interestingly, it has been found that even though these processes are more favourable from a noise propagation perspective at low frequencies, their advantage is compromised with increasing frequency mostly because of the capacitive nature of the substrate impedance [34]. Additionally, it has been shown that the effectiveness of many isolation schemes depends on the properties of the substrate; consequently, understanding the propagation behaviour of the noise in
2.1.3 Noise Reception Mechanisms

Substrate noise can impact analog circuits through two different mechanisms: directly, by affecting the signal at the output or input nodes and, indirectly, by changing the design parameters of the circuit.

One of the direct mechanisms is capacitive reception in which the voltage fluctuations of the substrate directly couple to the drain and source terminals of a MOSFET through the parasitic capacitances of these diffusion areas [36]. Another direct method is the noise coupling to the channel through depletion capacitances; however, this method can be seen as an extra contribution to the noise injected into the source and drain [36]. In many cases, this noise can be treated as common-mode noise, which can ideally be suppressed using differential structures; however, in practice, owing to nonlinearities and asymmetries, it cannot be removed completely. In addition to the terminals of active devices, passive on-chip devices such as capacitors, spiral inductors, and resistors can also act as receptors for substrate noise [37].

One of the major indirect noise reception mechanisms is body effect. This phenomenon changes the large and small-signal behaviour of the MOS device, which influences analog performance. It should be noted that, while capacitive coupling can happen in any active device (MOSFET, BJT, or diode), body effect is specific to MOS devices.

Other indirect mechanisms, such as the variation of the capacitance of varactors or changes in the biasing conditions of the circuit, are also important in certain applications, e.g., in VCOs and PLLs [23, 38]. However, for the purpose of this work, i.e., the effect of various types of substrate is important in both noise characterization and reduction.
substrate noise on LNAs, we will focus only on body effect.

2.2 Substrate Noise in Frequency Domain

Most analog circuits work in a specific frequency band. As such, studying the frequency content of the substrate noise is of interest, since out-of-band noise can be easily removed by filtering. Most previously reported work has focused on substrate noise in time domain, and only a few have investigated high-frequency content of the noise and its relationship to other parameters, such as the clocking scheme of digital blocks [19–21, 39].

An extension of the time-domain work in [18] for GPS applications was demonstrated in [21], which covered substrate noise in frequency domain. A theoretical treatment of the noise was also given; however, it is difficult to get a clear view of the noise frequency content from the formulation. The experimental results were based on a more complicated (yet with a well-defined switching pattern) digital circuit; therefore, the noise peaks in frequency were observed at multiples of clock frequency. Also predicted by this work was that the spectrum of the noise depends not only on the clock frequency but also on the switching patterns of the digital circuits, and as the switching in the digital blocks becomes more random, the noise will eventually be distributed equally over the frequency.

Another work presented in [19] used direct measurements to find the frequency content of substrate noise. One shortcoming of their technique was the limited bandwidth of the measurement system used, which limited their results to a few 100MHz. The same result as [21] was obtained, i.e., noise peaks occurred at multiples of the clock frequency. Additionally, their results supported the dependence on the switching pattern of the digital
circuit; as an example in [19] the digital circuit had a divide-by-2 nature; consequently, in addition to the main harmonics of the clock frequency, noise peaks were observed at half of the clock frequency, as well.

One of few measurement results based on an actual SoC was reported in [20], where it was shown that different cores on an SoC can generate peaks at different frequencies, which is a more realistic approach compared to the totally random activity of digital circuits in [21].

2.3 Effects of Substrate Noise

Substrate noise can affect both digital and analog circuits in an SoC; however, its effect on analog circuits is more pronounced for two reasons: first, analog circuits in general have a more limited noise budget due to the small amplitude of their input signal. Second, the mechanisms through which the noise affects their performance are more diverse in these circuits because, as discussed before, other than direct coupling of the supply noise to the input and output nodes of the circuit, and capacitive couplings through junction and device capacitances, a significant noise reception mechanism is body effect, which is not important in digital applications. The study of noise in analog circuits is also more complicated, owing to the importance of the analysis of the noise in frequency domain.

In digital circuits, substrate noise can result in false switching, erroneous storage into flip-flops [40], double clocking, and missing clocked pulses [41]. Another observed phenomenon is the change in the delay of the datapath due to substrate noise that can potentially exceed the predefined clock period.
Chapter 2. Background

The effect of substrate noise on analog systems can be analyzed from a signal degradation point of view. Three mechanisms can be distinguished through which substrate noise degrades analog signals [36]:

1. Direct coupling
2. Intermodulation
3. Sampling

Substrate noise contains high frequency components that can fall into signal band through the direct coupling of the substrate to the output nodes of the analog circuit. This process can degrade the signal-to-noise ratio (SNR) directly. In addition to direct coupling, in-band noise can be generated through the intermodulation of the noise signals due to nonlinearities in analog circuits [21]. Another consequence of modulation is variations in the bias conditions in bandgap references. An example of such effects is introduced in [38], where substrate noise in the bandgap reference circuit has resulted in a DC shift of the output voltage. The last mechanism is sampling, which is a common process in ADCs. The noise coupled to the analog circuit preceding the ADC, at an out-of-band frequency, can fold back into signal band through this process [36].

LNAs, PLLs, voltage-controlled oscillators (VCOs), operational amplifiers (op amps), and ADCs are common analog and RF blocks in mixed-signal SoCs; therefore, extensive research has been done on the study of the effects of substrate noise on the operation of these blocks.

The impact of noise on operational amplifiers was considered in [42]. In [21] the effect of noise on the performance of a GPS LNA was reviewed from a signal point of view. A
study of the effect of noise on oscillators was given in [23]. In oscillators, substrate noise can change the value of the varactors, which in turn causes the output frequency to vary, thus generating extra jitter or phase noise. In [43], the effect of substrate noise on timing jitter of a PLL was explored using a stochastic approach to substrate noise.

Comparators are another type of analog circuit widely used in ADCs. A common architecture of comparators is composed of an amplification stage followed by a latch. The speed of such comparators is a function of the transconductance of transistors in the latch. Since the transconductance is affected by the substrate noise through body effect, the speed of the comparator would also change due to the substrate noise. This effect can be considered as the output signal jitter that will decrease the SNR of the ADC [44]. It was shown in [25] that the output of an ADC can be highly distorted due to substrate noise. Furthermore, substrate noise can significantly limit the minimum detectable level of the signal that can degrade ADC's resolution and decrease its effective number of bits.

Although in most cases substrate noise only degrades the performance of the circuit, examples of malfunctioning are also reported in the literature. An example of failure was reported in [45] where an 8-bit, semi-flash pipelined video ADC continued to fail several specifications after three design fabrication iterations.

2.4 Substrate Noise Simulation

The accurate modelling of substrate noise requires the precise modelling of the whole layout and substrate, meaning that information about the geometry of all wells, well contacts, diffusion areas, trenches, etc. are needed as well as a three-dimensional (3D)
Chapter 2. Background

model of the substrate. Even in a small circuit, this comprehensive modelling entails a huge network of elements whose governing equations will not be tractable. Furthermore, since the modelling depends on the final layout of the chip, it would be difficult for designers to get an insight into the effects of substrate noise at the early stages of the design.

Accurate modelling techniques use various methods, such as the finite difference method (FDM) or the boundary element method (BEM), and Green’s function\(^1\) to accurately solve physical equations of the substrate and model it with a large and accurate RC network [27, 28, 45, 46].

Conventional tools available for substrate noise analysis, such as SPACE [47] and SNA [48], use 3D modelling of the substrate and create macromodels of the digital noise and substrate and solve the resulting network using several simplification algorithms.\(^2\) Some works have suggested small models consisting of a few lumped elements to be added to each transistor [18, 19, 34]. One major drawback of these models is that they are applicable only to epitaxial substrates owing to some special properties of these substrates\(^3\) that renders them impractical for lightly-doped ones; nonetheless, since they can be applied to simulations at the schematic level, they can be used even before the final layout is drawn.

In addition to substrate modelling, calculation of the switching digital noise is another part of substrate noise simulation that should be addressed in CAD tools. Due to the large number of elements on current chips, the accurate simulation of switchings results in a prohibitively large computation cost; therefore, various methods are proposed in the

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\(^1\)The Green’s function is the potential at any point in a medium with suitable boundary conditions due to a unit current injected at a point within the medium.

\(^2\)In this thesis, we use SeismIC noise analysis tool for the study of substrate noise, which is a part of Substrate Noise Analyst (SNA) by Cadence\(^9\).

\(^3\)We will discuss the difference between epitaxial and lightly-doped substrates in detail in Chapter 3.
literature for macromodelling digital noise [49–51]. A simple approach is to use a properly-sized chain of inverters instead of a large digital block to reduce the calculation cost.

### 2.5 Substrate Noise Reduction Techniques

Several existing substrate noise reduction techniques can be found in the literature. The use of passive guard-rings was studied in [34]. A simple substrate contact was used as a noise sensor, which is resistively connected to the substrate, whereas in a more realistic approach analog nodes are connected to the substrate both resistively and capacitively. Active noise suppression is another method, which was explored in [30, 31]. The basic idea is to measure the amount of noise and inject an inverted version of the noise into the substrate to cancel out the original noise. This approach suffers from two shortcomings: first, this technique will cancel the noise locally and cannot be applied to a large area unless multiple measuring points and circuitry are used. Additionally, in contrast to passive methods that do not impose power overhead, this method involves power consumption for noise reduction circuits, which is not desirable in low-power or handheld applications.

In addition to passive and active guard-rings, digital activity can be modified to generate less noise. This reduction is usually achieved either by reducing the amount of activity or distributing it over time.\(^4\) Many low-noise digital families are proposed, including current steering logic (CSL), current balanced logic (CBL), complementary current balanced logic (C-CBL), source-coupled logic (SCL) and folded source-coupled logic (FSCL) [52–54].

Output drivers are typically one of the major contributors to substrate noise due to the

---

\(^4\)Note that most of these techniques are similar to those used in low-power digital design because both try to reduce instantaneous current or simultaneous switching.
large instantaneous current they draw from the supplies. The design of low-noise output drivers was also addressed in [41, 55]. An example of activity distributing techniques is *switching activity spreading*, which was presented in [21, 56]. Although this technique reduces the rms value of the noise, this reduction does not necessarily mean that the noise content in the frequency band of interest is also decreased; therefore, these approaches should be used with caution in RF applications [21].
Chapter 3

Substrate Noise Characterization

Voltage variations in the substrate are caused by various sources. These sources can be classified into two major types: *internal* and *external* noises. These terms refer to the way that the generated noise couples to the substrate of analog circuits and not the propagation properties of the noise through the substrate. Figure 3.1 illustrates this concept.

![Figure 3.1: Illustration of internal and external noise sources.](image)

Internal noise refers to the case where the switching of on-chip digital gates is internally coupled to the substrate through the parasitic capacitances of active devices, wells and interconnects; therefore, it directly couples to the substrate and transmits to sensitive nodes, i.e., everything happens internally, within the silicon substrate. On the other hand, external noise applies to the situation in which a part of the noise path from digital to analog nodes falls outside of the chip substrate (e.g., on supply lines). An example of
such noise is when switching digital gates induce noise on supply/ground lines\(^1\) and then the resulting noise is coupled back to the substrate through substrate and supply contacts in the vicinity of analog circuits. Note that both the internal and external sources are consequences of switching in digital parts, but they use different paths to reach analog nodes.

In addition to the noises due to switching activity, other noises exist that are independent of switching in digital gates and are mostly due to leakage currents. Examples of such sources are *impact ionization current* and *photon induced current*. However, it has been shown that these types of noise have less of an impact on the overall substrate noise [19, 33], and thus they are ignored in our study.

In the following sections, a review of supply/ground noise as a major contributor to external noises is given first. Next, the effects of several parameters on the internal and external sources are analyzed. This section is followed by a discussion on the relative importance of internal and external sources to identify the dominant noise mechanism. Finally, the effect of substrate type on noise propagation behaviour is studied using simulation results from SeismIC substrate noise analysis tool. It should be noted that SeismIC is one of the few substrate noise analysis tools commercially available, the accuracy of which is verified by experimental results [57, 58].

\(^1\)This noise is sometimes referred to as *ground/supply bounce*, *switching*, or \(\frac{dI}{dt}\) noise.
3.1 Supply/Ground Noise due to Switching

The inductance of package pins and bondwires, along with the transient currents, are the main causes of supply or ground noise in digital circuits. The transient current during digital transition in a CMOS logic circuit comes from two sources: the main source of this current is the charging or discharging of the load capacitance of each gate through the positive supply \((V_{DD})\) or negative supply \((V_{SS})\), respectively, and the second source is the short circuit current between \(V_{DD}\) and \(V_{SS}\) during the switchings. To explore the behaviour of this current, in the following section, we develop a simplified MOSFET model, which allows for the analytical study of the switching behaviour.

3.1.1 MOS Device Modelling

Early work in the field of switching noise assumed square-law operation for the MOS device [15, 59]; however, the model now widely in use for short-channel devices is the \(\alpha\)-power law model that accounts for velocity saturation effects [60]. Based on this model, the drain current of a MOS device in the saturation region can be approximated using the following equation:

\[
I_D = K(V_{GS} - V_{th})^\alpha
\]  

(3.1)

where \(V_{th}\) is the MOSFET threshold voltage and \(\alpha\) is a technology-dependent parameter, derived to be equal to 2 for long-channel transistors and closer to 1 for deep submicron devices. Using Equation 3.1 in supply/ground noise analysis leads to a system of nonlinear differential equations that is difficult, if not impossible, to solve analytically. Different approximation techniques have been proposed to simplify and/or linearize the resulting
Figure 3.2 shows the I-V characteristic of an NMOS device along with its linear approximation. In this section, a linear approximation of the MOS device characteristic is used, which results in a set of linear differential equations [61].

Figure 3.2 shows the I-V characteristic of an NMOS device in 0.18μm technology and its linear approximation. In this figure, SPICE simulations for 0.18μm CMOS technology were used to obtain the NMOS I-V characteristic.

As Figure 3.2 shows, the linear approximation is in close agreement with the actual I-V characteristic, especially in the active region. This property is favourable, since the switching NMOS transistor will most likely remain in the active region during switching from high to low; therefore, it is expected that the linear approximation will give accurate results in switching analysis. This is particularly true for output drivers where, due to the large capacitive load, the output voltage remains almost constant during the switching of the transistor. Using data obtained from Figure 3.2, we can write the linear approximation
of the MOS device as:

\[ I_D = K_1(V_{GS} - V_{GS0}) \quad \text{for } V_{GS} \geq V_{GS0} \]  

(3.2)

where \( K_1 \) is a constant and \( V_{GS0} \) is the intersection point of the approximation line and the \( V_{GS} \) axis, which is not necessarily equal to \( V_{th} \) of the MOS device. Simulation results show that changes of \( V_{DS} \), within supply limits, have a negligible effect on the I-V characteristic and is thus ignored in the calculations of this section. It should be further emphasized that the more linear behaviour of the device, the better this approximation, meaning that this model is expected to be more accurate for more deep submicron devices.

### 3.1.2 Supply/Ground Noise in a Single Gate

Figure 3.3 shows a typical CMOS inverter, along with package and bondwire parasitics. In this figure, the parasitics of the power supply and ground lines are represented using a lumped RLC model. The capacitive load of the inverter is shown by \( C_L \), and the input signal is modelled with a ramp signal, changing from ground to supply with a finite rise-time:

\[ V_{in} = \frac{t}{t_r} V_{DD} \quad \text{for } 0 \leq t \leq t_r \]  

(3.3)

To derive an analytical formula for ground variations\(^2\) due to switching, we assume the noise on the ground line to be initially zero. The NMOS transistor is also initially in the cut-off region and starts conducting after the input signal reaches \( V_{GS0} \). The following

\(^2\)Due to the similarity of switching noise calculations on supply and ground lines, only the corresponding derivations for ground lines are presented here. The results can be readily modified to obtain equations for power-supply noise.
Figure 3.3: A typical CMOS inverter along with the package model.

The equations capture the behaviour of the circuit:

\[
I_N = K_1(V_{in} - V_n - V_{GS0}) \quad (3.4)
\]
\[
I_L = I_N - C \frac{dV_n}{dt} \quad (3.5)
\]
\[
V_n = RI_L + L \frac{dI_L}{dt} \quad (3.6)
\]

where \(I_N\) is the current of the NMOS source terminal, \(I_L\) is the current through the parasitic inductance and \(V_n\) is the noise voltage at the substrate node. Combining Equations 3.4–3.6, we have:

\[
LC \frac{d^2V_n}{dt^2} + (LK_1 + RC) \frac{dV_n}{dt} + (1 + RK_1)V = LK_1 \frac{dV_{in}}{dt} + RK_1V_{in} - RK_1V_{GS0} \quad (3.7)
\]

which is a second-order linear differential equation that can be solved analytically. It should be noted that this linear equation is a result of the linear approximation of the I-V
characteristic of the MOS device.

The analytical solution of the differential equation has the following form:

\[ V_n = V_h + V_p \quad (3.8) \]

where, \( V_p \) is the particular solution and \( V_h \) is the general solution of the homogeneous equation, and is given by:

\[ V_h = d_1e^{\lambda_1} + d_2e^{\lambda_2} \quad (3.9) \]

\( \lambda_1 \) and \( \lambda_2 \) are the roots of the characteristic equation that can be complex and \( d_1 \) and \( d_2 \) are constants that are calculated based on the initial conditions of the circuit. Assuming a linear ramp approximation, as in Equation 3.3, \( V_p \) has the following form:

\[ V_p = at + b \quad (3.10) \]

where:

\[ a = \frac{RK_1V_{DD}}{(1 + RK_1)t_r} \quad (3.11) \]

\[ b = \frac{K_1(\frac{LV_{DD}}{t_r} - RV_{GS0}) - (LK_1 + RC)a}{1 + RK_1} \quad (3.12) \]
3.1.3 Simultaneous Switching of Multiple Gates

It is a common practice in large circuits to replace individual logic blocks with a large inverter or a chain of inverters that generate the same amount of switching current. This approach decreases the computational complexity of simulations and is used in many noise macromodelling applications [49]. The derivations of the previous section can be extended to the case of \( N \) simultaneously switching gates or, equivalently, a large inverter with \( N \) times the width of a single inverter. The equations can be derived in the same manner; the final equation is as follows:

\[
\begin{align*}
LC\frac{d^2V_n}{dt^2} + (NLK_1 + RC)\frac{dV_n}{dt} + (1 + NRK_1)V &= \\
NLK_1\frac{dV_{in}}{dt} + NRK_1V_{in} - NRK_1V_{GS0}
\end{align*}
\]

(3.13)

The solution of this differential equation can be used to find the maximum peak-to-peak value of the switching noise. First, we look at the characteristic equation of this differential equation:

\[
LC\lambda^2 + (NLK_1 + RC)\lambda + (1 + RNK_1) = 0
\]

(3.14)

\[
\Delta = (NLK_1 - RC)^2 - 4LC
\]

(3.15)

Depending on the value of the parameters and \( N \), the discriminator of the quadratic equation, \( \Delta \), can be either positive, negative, or zero. We define \( N_{\text{crit}} \) as the value of \( N \) for which \( \Delta \) is zero:

\[
N_{\text{crit}} = \frac{2\sqrt{LC + RC}}{LK_1}
\]

(3.16)
For $N > N_{\text{crit}}$ the equation has two real roots, which is most likely to happen for large values of $N$. Note that, as $K_1$ increases (for example when using larger transistors), $N_{\text{crit}}$ decreases, which is the case for large output drivers. In cases where $N < N_{\text{crit}}$, the behaviour of the noise is different, and ringing due to the on-chip parasitic capacitance and inductance is observed. Since output drivers, due to their large transient currents, are the major contributors to switching noise, here the equation is solved assuming $N > N_{\text{crit}}$. In this case, both $\lambda_1$ and $\lambda_2$ are negative real numbers, resulting in a decaying exponential term in the noise expression. Moreover, it can be shown that under the circumstances mentioned above the maximum switching noise will always occur at the end of the input transition time, and its value can be calculated from the following formula:

$$V_{n_{\text{max}}} = (-a_n t_0 - b_n + \frac{a_n}{\lambda_1})e^{\lambda_2(t_r-t_0)} + a_n t_r + b_n \quad (3.17)$$

where $\lambda_1$ and $\lambda_2$ are real roots of the characteristic equation and $|\lambda_1| > |\lambda_2|$, $t_0$ is the time at which the transistor starts conducting and can be approximated by the following formula:

$$t_0 = \frac{V_{GS0}}{V_{DD}} t_r \quad (3.18)$$

In Equation 3.17, $a_n$ and $b_n$ are modified versions of $a$ and $b$ calculated for the case of $N$ simultaneously switching gates and are given by:

$$a_n = \frac{R NK_1 V_{DD}}{(1 + NRK_1)t_r} \quad (3.19)$$

$$b_n = \frac{NK_1 \left( \frac{V_{DD}}{t_r} - RV_{GS0} \right) - (NLK_1 + RC)a_n}{1 + NRK_1} \quad (3.20)$$
3.1.4 Supply/Ground Noise Simulation Results

SPICE simulations were performed in a CMOS 0.18\(\mu m\) technology to evaluate the accuracy of the proposed model. Figure 3.4 presents the transient behaviour of the noise using the linear approximation of Section 3.1.1. This figure verifies that the proposed approach closely follows SPICE simulation results, especially when the transistor is fully conducting.

![Graph showing transient behaviour of noise](image)

Figure 3.4: Switching noise voltage on ground line with \(L = 1\mu H\), \(R = 2\Omega\), \(t_r = 200\text{ps}\), and \(N = 100\).

The maximum value of the simultaneous switching noise (SSN)\(^3\) as a function of the number of switching gates is plotted in Figures 3.5 and 3.6. For the purpose of comparison, the results of two other works are also included in these figures. To make a fair comparison, the values of package resistance and capacitance are set to zero in Figure 3.5. The effect

\(^3\)This term is frequently used in the literature to represent the noise appearing on supply and ground lines due to the simultaneous switching of digital gates.
Chapter 3. Substrate Noise Characterization

Figure 3.5: Maximum noise on ground as a function of the number of switching gates ($R = 0, t_r = 200ps, L = 1nH, C = 0$).

of these parasitics are included in Figure 3.6, where a resistance of $2\Omega$ and a capacitance of $100fF$ are added in the supply parasitic network. As can be seen in Figure 3.5, there is a large discrepancy between SPICE results and those predicted by the approach presented in [15], which is primarily due to neglecting the effect of velocity saturation in that work. In the other work, the effects of package capacitance and resistance were ignored, resulting in underestimating noise values. The results of the proposed model are within 2% of SPICE simulations in Figure 3.5. The accuracy decreases as the number of gates increases due to the increase in the approximation error used in determining the initial conditions of the differential equation and neglecting subthreshold current.

Equation 3.17 can be used to analyze the effect of several parameters, such as the power supply voltage, the parasitic inductance of the package and bondwires, and the number of simultaneously switching gates, on the maximum amount of noise in the circuit.
Figure 3.6: Maximum noise on ground as a function of the number of switching gates $$(R = 2\Omega, t_r = 200ps, L = 1nH, C = 100fF)$$.

While parasitic resistance has been neglected in simultaneous switching noise calculations in [15, 16, 62], simulation results show that as CMOS technology scales down and the integration level and transient currents increase the voltage drop across this resistance can potentially be important; more specifically, Equation 3.17 suggests that this resistance creates a term that increases linearly with time; hence it is more significant in slower parts of the circuit, such as output drivers, that have larger switching time and contribute more to noise.

Equation 3.17 verifies the previous result observed in [15] and [16] that the SSN maximum value is a sublinear function of the inductance as shown in Figure 3.7. This can be considered a consequence of the built-in negative feedback of the MOS device, which does not allow the noise to increase unboundedly. Due to this built-in negative feedback, the drain current decreases as the voltage of the source of the MOS transistor increases, hence
3.2 Internal versus External Noise Sources

In the previous sections, supply/ground noise was discussed as one of the major contributors to external noise sources; nonetheless, the contribution of each of the two introduced...
sources (external and internal noises) to the total substrate noise is an interesting parameter to observe. Since external noise sources are typically much larger than internal sources they can potentially dominate the overall noise. Especially if the analog and digital circuits share the same supply lines, any noise on digital lines will directly couple to the substrate area in the proximity of analog devices through substrate contacts of that area, which will drastically increase the amount of noise; whereas in the case of separate supplies, the only way for the noise on digital supply lines to disturb analog nodes is to couple to the substrate through substrate contacts of the digital circuits.

Figure 3.8 represents SeismIC simulation results of the substrate noise at the bulk node of an analog NMOS located 100μm away from a chain of inverters. The total substrate noise is plotted as a function of the length of the bondwire, which can be translated into...
the amount of inductance.\textsuperscript{5} Two cases are plotted in this figure; in the first one the analog and digital supplies are separated, which means that the total noise is due only to internal sources, whereas in the second one supply lines are shared; therefore, both internal and external noise sources contribute to the overall noise.

Figure 3.8 reveals an important point: the amount of noise increases significantly if the supply lines of the analog and digital circuits are the same. An immediate implication of this observation is that using separate supplies for analog and digital sections significantly reduces the interaction between these two parts. In cases where use of separate supplies is not possible, the total noise can be reduced using a low-inductance package such as flip-chip. In fact based on Figure 3.8 for the circuit used in these simulations, the noise coupling from supply lines will be dominant if the amount of the inductance is larger than 200pH, which means that above this value, most of the noise would be due to supply noise rather than the direct effect of switching in digital cores.\textsuperscript{6} In other words, external noise sources dominate very quickly as the inductance in the package increases.

Hereafter, unless otherwise specified, it is assumed that digital and analog supply lines are separated, implying that only internal noise sources are causing noise at the substrate of analog nodes. In most parts of this work, a simple inverter in CMOS 0.18\textmu m is used as a testbench to study the effect of various parameters on substrate noise. The layout of the test circuit is shown in Figure 3.9.\textsuperscript{7} The noise is measured at the substrate of digital NMOS and a dummy NMOS, which is used to represent a sensitive analog device.

\textsuperscript{5}As a rule of thumb the inductance is linearly proportional to the length of the bondwire with the slope of 1nH/mm.
\textsuperscript{6}Note that 200pH is very small compared to the inductance of most available packages.
\textsuperscript{7}For more information on the layout of other testbenches please refer to [63]
Figure 3.9: Layout of substrate noise analysis testbench.

To quantify the noise behaviour, the noise attenuation factor is used in this study, which is defined as the ratio of the peak-to-peak value of the noise at the bulk node of the NMOS in the inverter to the peak-to-peak value of the noise at the bulk node of the dummy NMOS:

\[
\text{Attenuation} = \frac{V_{pp, Digital}}{V_{pp, Analog}} 
\]  

(3.21)

The attenuation factor depends on a variety of parameters, such as substrate type and digital activity. The following sections deal with the characterization of substrate noise using the attenuation factor.
3.3 Substrate Noise in Frequency Domain

The dependence of noise attenuation on the frequency of operation is an important parameter in noise analysis in high-frequency applications. Figure 3.10 presents Seismic simulation results of the dependence of the attenuation factor on frequency for various distances between noisy and sensitive parts. As can be seen, the noise attenuation improves as the frequency increases in Figure 3.10(a). This observation is interesting because one might think that at higher frequencies there is more coupling between noisy parts and the substrate. However, although the amount of noise coupling increases at higher frequencies due to the capacitive behaviour of the impedance coupling the switching nodes to the substrate, the amount of substrate coupling to quiet lines increases at the same time due to a similar effect. This can be shown by connecting a noisy ground to the circuit and measuring the amount of attenuation, as depicted in Figure 3.10(b). In this figure there has been a 1nH inductance on supply lines that resulted in a noisy ground and supply. As a result, the amount of noise attenuation decreased significantly at higher frequencies due to the increased coupling of the circuit to noisy lines. Furthermore, the local maximum observed in Figure 3.10(b) is an evidence of the existence of the two competing mechanisms mentioned above.

3.4 Noise versus Switching Time

Another important parameter is the amount of noise as the switching time of the circuit changes. Figure 3.11 depicts waveforms of substrate noise in time-domain for various input clock rise-times. The waveforms represented in Figure 3.11(a) show the case in which there
(a) Dependence of coupling on the frequency (no noise on supplies).

(b) Dependence of coupling on the frequency (noisy power supply).

Figure 3.10: Attenuation factor as a function of frequency.
Figure 3.11: Substrate noise waveforms for various clock rise-times.

is no inductance in supply lines, i.e., there is no supply noise, and Figure 3.11(b) is the same experiment but with an inductance of 1nH in the supply path, which has introduced ringing. As can be seen, there is no significant change in the maximum value of the noise, or even the waveform, which can be explained using the fact that the major contributors to the noise are those parts of the circuit that draw the largest amount of current from the supplies, e.g., the output stage, and since changing the input clock rise-time does not affect
the rise-time of the output stage, the noise has not changed significantly. On the other

hand, if the switching time of the output stage changes, e.g., by changing its capacitive
load, then the peak-to-peak value of noise will vary, as shown in Figure 3.12. The flat part
of the plot shows the situation in which the noise of the output stage is not dominant;
therefore, a further increase in its rise-time does not decrease the noise. Based on these
observations, it can be concluded that increasing the switching time of the output drivers
is an effective way of reducing noise (however, at the expense of a slower system) but it
does not help if the noise due to those parts is not dominant.

Figure 3.12: Peak-to-peak value of substrate noise as a function of the rise-time of the last
stage.
3.5 Effect of Substrate Type on Noise

As discussed in Chapter 2, substrate type plays an important role in noise behaviour, especially in noise propagation properties. Due to its resistive nature, the silicon substrate itself exhibits attenuation to some extent; however, the amount of attenuation depends on several parameters, such as substrate resistivity and structure.

To characterize noise coupling in different substrates used in CMOS technology, first, two major types of silicon wafers will be reviewed, and the dependence of noise propagation on a number of process and layout parameters will be studied in the following sections.

3.5.1 Different Substrate Types

Figure 3.13 shows the two most commonly used substrate types in CMOS integrated circuits. The lightly-doped substrate (shown in Figure 3.13(a)) is the simplest silicon substrate in terms of manufacturability; however, owing to its high susceptibility to latch-up, this type of wafer was replaced by epitaxial substrates (shown in Figure 3.13(b)) in older CMOS technologies. In an epitaxial wafer, a thin layer of silicon is deposited on top of a heavily doped bulk several hundred micrometers thick. Active devices are built into this thin high-resistivity layer. This type of substrate circumvents the problem of latch-up and allows for better device performance due to the better controllability of the doping profile of the epitaxial silicon [64].

Currently, the most widely used wafer in digital CMOS applications is the epitaxial substrate. The heavily-doped portion has a resistivity of several milliohm-cm $(m\Omega\cdot cm)$. The resistance of the epitaxial layer is typically 2–3 orders of magnitude higher than the
Chapter 3. Substrate Noise Characterization

(a) A typical lightly-doped substrate.

(b) A typical epitaxial substrate (not to scale).

Figure 3.13: Two most commonly used silicon substrates.

bulk substrate, i.e., its resistivity is in the same order as the resistivity of a lightly-doped substrate. Although epitaxial substrate has a better latch-up performance, there is a compromise between substrate noise attenuation and latch-up immunity depending on the thickness of the epitaxial layer; i.e., as the thickness of the epitaxial layer increases, the noise suppression of the substrate improves, while the latch-up characteristic deteriorates [65]. It should be noted that the scaling of CMOS technology and the use of lower supply voltages in new CMOS generations has decreased the probability of latch-up. Additionally, lightly-doped substrates exhibit better RF performance, e.g., better on-chip spiral inductors, compared to their epitaxial counterparts [66]; therefore, recently, there has been an increasing interest in using lightly-doped substrates due to their lower manufacturing cost [35].
As discussed before, the substrate is a resistive network; therefore, a simple resistive model can be used to analyze noise propagation behaviour. Figure 3.14 illustrates one simple representation of such a model. As shown in this figure, the heavily-doped bulk in epitaxial substrates can be considered a single node due to the low resistivity of the bulk silicon [18]. This is particularly important in the noise propagation behaviour because this equipotential layer (heavily-doped bulk) can act as the major noise path from digital to analog nodes instead of the surface path through the epitaxial layer.

The presence of the bulk node is the main reason for the different behaviour of the noise dependence on the layout parameters in the two types of substrate. It is also the
basis for the development of lumped-element models for the substrate [18, 19] because the bulk defines a single node that is connected to all devices through the resistances of the epitaxial layer; whereas, in lightly-doped substrates, the distributed nature of the substrate does not allow for small lumped-element models. From the model presented in Figure 3.14, one can expect that in lightly-doped substrates, increasing the distance between digital and analog nodes decreases the amount of coupling because of the increase in the impedance of the noise path, whereas in epitaxial wafers, increasing the separation is not an effective way, since the noise propagates mostly through the heavily-doped bulk that has negligible resistance.

3.5.2 Noise Behaviour in Different Substrates

Figure 3.15 shows the dependence of noise attenuation factor on the distance between digital and analog circuits in both types of substrate. As can be seen, the attenuation monotonically increases in lightly-doped substrates as the distance increases, while in the epitaxial substrates, increasing the distance above a certain limit does not increase the attenuation of the noise.

The increase in noise attenuation at short distances in the epitaxial substrate can be attributed to the fact that at short distances a significant portion of noise propagates through the high-resistivity epitaxial layer; therefore, there is no difference between the propagation behaviour of lightly-doped and epitaxial substrates; however, with the increase in separation, the noise penetrates more through the bulk, hence reducing the effect of surface attenuation. As a rule of thumb, increasing the distance between the digital and analog nodes beyond 4 times the thickness of the epitaxial layer has a negli-
Figure 3.15: Attenuation factor as a function of the distance between analog and digital nodes in two types of substrate (Note that the scales are different.)

This can also be explained using the simple resistive models of Figure 3.14. Based on the epitaxial substrate model, increasing the physical separation does not increase the resistance of the noise path; thus no further noise attenuation is provided.

Another parameter of interest is the dependence of noise on the resistivity of the bulk in lightly-doped substrates. Figure 3.16 depicts the simulation results of the inverter circuit for different values of substrate resistivity. The attenuation factor at large physical separations has a $d^{\alpha}$ behaviour, with $\alpha$ depending on the resistivity of the bulk. To justify this effect, an understanding of the dependence of the substrate resistance on the distance between two points is required. Although the calculation of the actual resistance in a real chip is quite complex due to the effects of various parameters including neighbouring
contacts and devices, in a simple case of only two contacts (shown in Figure 3.17) on a lightly-doped substrate, the following equation can be used [67]:

$$ R_{ij} = \frac{k d_{gm}^n}{\sqrt{area_i} + \sqrt{area_j}} $$  \hspace{1cm} (3.22)

where $\alpha$ and $k$ are process-dependent fitting parameters, $area_i$ and $area_j$ are the areas of the contacts, and $d_{gm}$ is the geometric mean distance between the two contacts, defined as:

$$ d_{gm} = \frac{\int_{L_2} f_{w_2} \int_{L_1} f_{w_1} r.\,dx_1.\,dy_1.\,dx_2.\,dy_2}{W_1.\,L_1.\,W_2.\,L_2} $$  \hspace{1cm} (3.23)

Equation 3.22 implies a linear increase in the resistance at large distances and faster than linear at short distances [67]; thus the observed behaviour in Figure 3.16 is in compli-
ance with the equation of the resistance, verifying that the total attenuation is proportional to the resistance of the substrate path.

In epitaxial substrates, the study of the relationship between the amount of the attenuation and the thickness of the epitaxial layer is instructive. One can expect increased attenuation in thicker epitaxial layers due to the increased resistance of the noise path to sensitive devices. This result can also be concluded from Figure 3.18, which shows the simulation results for three different epitaxial layer thicknesses.

Typically, the higher the resistivity of the substrate the better the isolation performance; therefore, lightly-doped substrates may seem to be advantageous in terms of noise suppression. However, there are controversial views on this argument; the conflict arises from the compromise between two basic mechanisms that control noise attenuation. In general, the amount of noise at sensitive nodes can be reduced either by directing the noise to a quiet line (such as supply or ground line) or the noise should be attenuated on its way to analog nodes (e.g, by the resistance of the substrate). The high resistivity substrate
seems to be better in the sense that its higher impedance results in more attenuation of noise on its path from the digital source to the analog circuit. On the other hand, a heavily doped substrate provides a low impedance path that can transfer noise to the ground, hence decreasing the effect of the noise on analog blocks [68].

### 3.6 PMOS versus NMOS

Since PMOS devices are capacitively isolated from the substrate by the underlying n-well, one may think that they are less susceptible to substrate noise. To verify this argument, a PMOS was used as a sensitive device, and the results were compared to that of an NMOS. The additional attenuation provided by PMOS as a function of frequency is plotted in
Figure 3.19. Based on this figure, PMOS has significantly better noise isolation; however, the advantage is compromised as the frequency increases due to the capacitive behaviour of the isolation. The considerable amount of noise attenuation in PMOS even at high frequencies suggests that it is beneficial to use PMOS for sensitive nodes of the circuit such as the input stage transistors of an LNA from the substrate noise point of view. However, one should be aware of the inferior performance of PMOS as compared to NMOS, due to the lower mobility of carriers, which leads to lower transconductance values and, consequently, a lower gain and a larger overall noise figure.

3.7 Summary

In this chapter, various aspects of substrate noise were studied. The dependence of supply/ground noise on switching activity and package parasitics were analyzed. Further-
more, it was shown that using the same supply line for analog and digital circuits will substantially increase the amount of substrate noise, mainly because supply lines will add an additional source of the noise to analog circuits. It was also shown that the effect of external noise sources can be mitigated using lower-inductance packages, even though, this will not be helpful if internal noise sources are dominant; a situation that requires other techniques (e.g., lowering the switching time of the output drivers) to decrease the amplitude of the noise.

It was shown that the substrate type has a crucial influence on the behaviour of the noise; therefore, the effect of various parameters such as substrate resistivity and thickness (for epitaxial wafers) on noise propagation properties was also studied.

Finally, it was shown that PMOS devices have better substrate noise performance as compared to NMOS transistors, due to the extra isolation provided by their underlying n-well. However, two considerations should be taken into account: first, PMOS is typically inferior to NMOS in terms of device performance, due to its lower carrier mobility and, second, the advantage decreases as the frequency of operation increases.
Chapter 4

Modelling the Effect of Substrate Noise

Substrate noise affects analog circuits in a multitude of mechanisms. Body effect is one of them, which is defined as the modulation of the threshold voltage of a MOS device due to variations in the source-bulk potential. It is shown that with body effect, the threshold voltage of a MOS transistor can be written as:

\[
V_{th} = V_{th0} + \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}(\sqrt{2\Phi_f + V_{sb}} - \sqrt{2\Phi_f})
\]

where \(V_{th0}\) is the threshold voltage when source-bulk potential is zero, \(\varepsilon_{si}\) is the substrate dielectric permittivity, \(N_A\) is the substrate doping, \(C_{ox}\) is the gate oxide capacitance per unit area, \(\Phi_f\) is the surface inversion potential, and \(V_{sb}\) is the source-bulk potential. Variations of \(V_{th}\) will impact both the large and small-signal behaviour of the device; i.e., it changes the drain current as well as the transconductance of the MOS transistor. The influence of body effect is typically accommodated in the small-signal model with an additional voltage-controlled current source connected between the drain and source terminals of the device.
In addition to body effect, substrate noise can directly couple to the analog nodes through supply lines and the neighbouring supply or substrate contacts and junction capacitances; however, here we assume that the supply lines of the analog and digital parts are separated; therefore, the common substrate is the main means of communication between noisy digital and sensitive analog nodes.

This chapter begins with a review of the MOS device noise model. Next, a modified version of the existing model is introduced that incorporates substrate noise effects. Finally, the impact of substrate noise on a typical LNA is studied based on the proposed model.

### 4.1 Noise Modelling in MOS Devices

A simplified MOSFET small-signal model, including device intrinsic noise sources, is shown in Figure 4.1, where all internal noise sources are combined and represented by a single noise source at the output [69].

![Figure 4.1: MOSFET small-signal model, including device internal noise sources (no substrate noise modelling or body effect).](image)

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1The reader is invited to refer to Appendix A for the full development of this model.
Two major device noise sources have been incorporated in this figure: channel thermal noise and gate-induced noise. The current source, $i_{ndg}$, represents the effect of both of these noises and is given by:

$$i_{ndg} = g_m Z_{gs} i_{ng} + \eta i_{nd}$$ (4.2)

where $g_m$ is the transconductance of the device, $i_{nd}$ and $i_{ng}$ represent channel thermal and gate-induced noises, respectively, and $Z_{gs}$ and $\eta$ are given by:

$$Z_{gs} = \frac{1}{g_m Z_{deg} + Z_g}$$ (4.3)

$$\eta = 1 - \left( \frac{g_m Z_{deg}}{Z_{deg} + Z_g} \right) Z_{gs}$$ (4.4)

Based on Equation 4.2, the mean-square value (i.e., power) of the noise, which is a more meaningful quantity in noise analysis, can be found as:

$$\overline{i_{ndg}^2} = \overline{i_{ndg}^* i_{ndg}} = \overline{i_{nd}^2} \left( |\eta|^2 + 2Re \left\{ c \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} g_m \eta^* Z_{gs} \right\} + \overline{\frac{i_{ng}^2}{i_{nd}^2}} g_m^2 |Z_{gs}|^2 \right)$$ (4.5)

where $c$ is the correlation coefficient between channel thermal noise and gate-induced noise:

$$c = \frac{\overline{i_{nd}^* i_{ng}}}{\sqrt{\overline{i_{nd}^2} \overline{i_{ng}^2}}}$$ (4.6)

We define device noise coefficient (DNC) as a measure of how intrinsic device noise sources are scaled when they are transferred to the output; therefore:

$$DNC = \frac{\overline{i_{ndg}^2}}{\overline{i_{nd}^2}} = |\eta|^2 + 2Re \left\{ c \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} g_m \eta^* Z_{gs} \right\} + \overline{\frac{i_{ng}^2}{i_{nd}^2}} g_m^2 |Z_{gs}|^2$$ (4.7)

The model shown in Figure 4.1 can be used in the noise figure calculation of a given circuit; however, it does not account for the effect of substrate noise, simply because it
neglects both the substrate noise source and body effect. In the following section, we include the effect of substrate noise in the current model, to derive a general model for substrate noise analysis purposes.

### 4.2 MOSFET Small-Signal Model Including Substrate Noise Effects

The impact of substrate noise can be added by modelling it with a voltage source connected to the substrate of the MOS device, as shown in Figure 4.2. A new terminal is added to the previous model representing the bulk node and is connected to $v_{ns}$ as the substrate noise source. $C_{sb}$ is also added to Figure 4.2 because it is the largest capacitor among all substrate parasitic capacitances that connect the bulk node to transistor’s terminals. It should be noted that here we have tacitly assumed that including body effect has a negligible impact on Equation 4.5; therefore, $i_{ndg}$ in this figure is the same as Figure 4.1.
Similar to the previous section, the effect of the additional noise source, $v_{ns}$, can be combined with the internal noise sources, $\tilde{i}_{ndg}$, in order to have a single source representing all existing noises in the device. To find the output noise current due to substrate noise, we simplify Figure 4.2 to obtain Figure 4.3, where $Z_s$ is the total impedance seen at the source terminal:

$$Z_s = (Z_g + \frac{1}{sC_{gs}}) \parallel Z_{deg} \quad (4.8)$$

and $K$ is given by:

$$K = \frac{-g_m}{sC_{gs}(R_s + sL_g) + 1} \quad (4.9)$$

Based on this figure, we can calculate the output noise current due to the substrate noise. The following equations can be written:

$$i_{out} = KV_s + g_{mb}V_{bs} \quad (4.10)$$

$$i_{out} + i_s = \frac{V_s}{Z_s} \quad (4.11)$$

$$\bar{v}_{ns} = \frac{i_s}{sC_{sb}} + V_s \quad (4.12)$$

\(^2\)Note that since we are interested in the transfer function from $\bar{v}_{ns}$ to the output, all other independent sources including $\tilde{i}_{ndg}$ should be disabled.
where \( i_{out} \) is the output current of the device (drain current), \( i_s \) is the current through \( C_{sb} \), and \( V_s \) is the source potential. By manipulating Equations 4.10–4.12, we have:

\[
\frac{i_{out}}{v_{ns}} = \frac{g_{mb}(sC_{sb} + 1/Z_s) + sC_{sb}(K - g_{mb})}{sC_{sb} + 1/Z_s - K + g_{mb}}
\]  

(4.13)

Similar to DNC, we define substrate noise coefficient (SNC) as:

\[
SNC = \frac{\overline{v^2_{out}}}{v^2_{ns}} = \frac{\left| g_{mb}(sC_{sb} + 1/Z_s) + sC_{sb}(K - g_{mb}) \right|^2}{sC_{sb} + 1/Z_s - K + g_{mb}}
\]

(4.14)

Consequently, a modified version of the total noise current, including the effect of substrate noise, would be:

\[
\overline{i^2_{ndgs}} = DNC \times \overline{i^2_{nd}} + SNC \times \overline{v^2_{ns}}
\]

(4.15)

where the first and the second terms on the right-hand side represent the effect of device and substrate noise, respectively. The final model is the same as Figure 4.1, except that the noise current source, \( i_{ndg} \), will be modified to \( \overline{i}_{ndgs} \), given by Equation 4.15. The reader may wonder why the final model does not include body effect and \( C_{sb} \). These components were omitted because it is assumed that they have negligible effect on the transfer function from the input to the output; nonetheless, their effect in the transfer function from the substrate to the output is already taken into account by \( \overline{i^2_{ndgs}} \).

---

\(^3\)It should be noted that here we have assumed that the internal noise sources and the substrate noise are uncorrelated.
4.3 Noise Figure Calculation

The model developed in the previous section can be used to study the effect of substrate noise on an inductively-degenerated LNA as a sample analog circuit. The purpose of using such LNA as a benchmark for our analysis is twofold: first, LNAs are among the most sensitive analog circuits to noise because of the extremely low amplitude of the signal at their input.\textsuperscript{4} Second, this type of LNA is the most commonly used topology in practice; therefore, it can well represent one of the critical blocks in mixed-signal SoCs. Figure 4.4 shows a generic schematic of such an amplifier.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig4_4.png}
\caption{A typical inductively-degenerated LNA.}
\end{figure}

In this circuit, $L_{\text{deg}}$ is used to create a real component in the input impedance of the circuit that can be tuned for input impedance matching and $L_g$ is included to control the resonance frequency.

In general, the noise factor, $F$, of an amplifier is defined as:

$$ F = \frac{\text{Total output noise power}}{\text{Output noise due to input source}} = \frac{\overline{v_{\text{nout(tot)}}^2}}{\overline{v_{\text{nout(in)}}^2}} $$

(4.16)

To calculate $\overline{v_{\text{nout(tot)}}}$ and $\overline{v_{\text{nout(in)}}}$, we refer to the MOS small-signal model introduced in the

\textsuperscript{4}As an example, the power of GPS signal can be as low as -130dBm [70].
previous section, based on which, we construct the small-signal model of the inductively-degenerated LNA as shown in Figure 4.5. Assuming that the amplifier is matched to the output resistance of the input source, $R_s$, we have:

$$V_{gs} = \frac{e_{ns}}{R_s + Z_{in}} \left( \frac{1}{j\omega_0 C_{gs}} \right)$$

$$= \frac{e_{ns}}{2R_s \frac{1}{j\omega_0 C_{gs}}} = \frac{1}{\omega_0 C_{gs} 2R_s j} = \left( \frac{Q}{j} \right) e_{ns}$$

$$\Rightarrow i_{nout(in)} = g_m (\frac{Q}{j}) e_{ns}$$

$$\Rightarrow \bar{v}_{nout(in)}^2 = (g_m Q)^2 e_{ns}^2$$

where $e_{ns}$ is the input noise of the LNA (due to $R_s$), $\omega_0$ is the center frequency, and $Q$ is the quality factor of the input network of the amplifier. Therefore, the noise factor will be:

$$F = \frac{(g_m Q)^2 e_{ns}^2 + \bar{v}_{ndgs}^2}{(g_m Q)^2 e_{ns}^2} = 1 + \frac{\bar{v}_{ndgs}^2}{(g_m Q)^2 e_{ns}^2}$$

(4.18)

Recalling $\bar{v}_{ndgs}$ from Equation 4.15, we have:

$$F = 1 + \frac{DNC \times \bar{v}_{nd}^2 + SNC \times \bar{v}_{ns}^2}{(g_m Q)^2 e_{ns}^2}$$

(4.19)
which can be written in the following form:

\[ F = 1 + DNF(Q) + SNF(Q) \]  \hspace{1cm} (4.20)

where \( DNF(Q) \) and \( SNF(Q) \) are the device and substrate noise factors, respectively. \( DNF(Q) \) accounts for the effect of internal noise sources of the device,\(^5\) whereas \( SNF(Q) \) shows the contribution of substrate noise; more specifically, \( SNF(Q) \) is given by the following equation:

\[ SNF(Q) = \left( \frac{SNC}{g_m Q} \right)^2 \frac{\overline{v_{ns}^2}}{4kT R_s} \]  \hspace{1cm} (4.21)

where \( k \) is Boltzmann's constant and \( T \) is the temperature. This equation shows the effect of substrate noise on the noise figure of the LNA. Furthermore, as will be discussed shortly, it reveals the trade-off between substrate noise and intrinsic device noise minimization.

Figure 4.6 depicts \( DNF \) as a function of \( Q \) in a typical LNA in 0.18\( \mu m \) technology for different values of \( c \). As defined in Equation 4.17, \( Q \) is the quality factor of the input network of the LNA. Since \( Q \) is inversely proportional to \( C_{gs} \), a lower \( Q \) corresponds to a wider transistor. As can be seen, for a given \( c \), an optimum \( Q \) exists that yields the minimum \( DNF(Q) \); thus, the overall noise figure would also be minimum (assuming that there is no substrate noise). However, in many cases, using this optimum \( Q \) leads to a large power consumption in the device; therefore, designers may consider using a higher \( Q \) to decrease power consumption, which as implied by Figure 4.6, entails increased noise figure from device noise perspective.

To further study the effect of substrate noise, various LNAs with different \( Q \) values

\(^5\)For the complete equation of \( DNF(Q) \) please refer to [69].
were designed in 0.18\mu m technology. The topology of the circuit was the same as the one shown in Figure 4.4. An additional MOS transistor was used as cascode device to increase the isolation between the input and the output and also reduce Miller effect. To analyze the effect of substrate noise, it is instructive to study the dependence of SNF on Q in Equation 4.21. The required data for this study such as the value of parasitic elements and transconductance of the input device were extracted from simulation results of the designed LNAs. By substituting values in Equation 4.14 and using the results in Equation 4.21, we obtain SNF as shown in Figure 4.7. As depicted in this figure, SNF appears to be a decreasing function of Q. Indeed, considering the fact that $C_{gs}$, $g_m$, and $g_{mb}$ are inversely proportional to Q, one can show that SNF is a decreasing function of Q.

The behaviour of SNF with respect to Q reveals an important compromise between
substrate noise and device noise minimization. As shown in Figure 4.7, SNF\(_Q\) exhibits an opposite trend as compared to DNF\(_Q\), i.e., substrate noise effect is more significant at low values of \(Q\), whereas at high values of \(Q\) the dominant noise mechanism would be the intrinsic noise of the device.

![Normalized substrate noise factor as a function of Q.](image)

Figure 4.7: Normalized substrate noise factor as a function of \(Q\).

To verify the preceding argument, the LNAs were simulated using Agilent Advanced Design System (ADS) simulator. To include substrate noise effect a noise source was connected to the bulk node of the input transistor and the resulting noise figure was measured. Figure 4.8 depicts the noise figure for various levels of substrate noise and \(Qs\). As can be seen, at low values of \(Q\), substrate noise is dominant; however, as \(Q\) increases the portion of the noise figure due to substrate noise decreases substantially. On the other hand, at high values of \(Q\), device noise starts dominating.
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The noise figure as a function of frequency is plotted in Figure 4.9 for two different Qs. This figure conveys important information about the behaviour of the noise figure. First, as expected, the effect of substrate noise is less in Figure 4.9(b) (which corresponds to a circuit with a higher Q). Another important result is that a frequency ($f_{opt}$) exists at which the noise figure in the presence of substrate noise is almost the same as that without any substrate noise.

To elaborate more on this point, it should be noted that all LNAs were designed for 1.5GHz, however, $f_{opt}$ is observed at 1.4GHz, which means that power matching and noise suppression have not occurred at the same frequency. A more careful study of these figures shows that in the absence of substrate noise the minimum noise figure is achieved at 1.6GHz which is still different from the center frequency. This discrepancy was expectable.
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(a) Noise figure as a function of frequency (Q=1.8).

(b) Noise figure as a function of frequency (Q=10).

Figure 4.9: Comparison of noise figure for different Qs. (The spectral density of substrate noise is given in $V^2/Hz$.)
because our design method is based on the power matching at center frequency and not on the noise matching. In fact, this type of behaviour is commonly encountered in LNA design. Various LNA design methodologies are either based on noise or input matching or they try to balance these two parameters [69, 70]. However, as suggested by the results of this section, the effect of substrate noise can be minimized by compromising the amount of device noise or power matching.

### 4.4 Summary

In this chapter, MOSFET small-signal model was revisited. A new small-signal model was proposed that accommodates the effects of substrate noise. Based on this model, the noise performance of an inductively-degenerated LNA was studied.

It was shown that increasing the quality factor of the input network alleviates substrate noise problem to some extent, but at the same time increases the effect of device noise sources. Based on the results in this chapter, to achieve the best noise performance substrate noise effect should be taken into account since it changes the overall noise figure characteristic of the amplifier, i.e, merely considering the effect of device noise will result in solutions that may exhibit poor substrate noise performance.

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6 In some cases, power consumption requirement is also added to the matching criteria.
Chapter 5

Evaluation of Reduction Methods

Substrate noise cannot be eliminated completely, but its deleterious effects can be controlled or minimized. Many noise reduction methods have been used by analog designers to mitigate the influence of the noise; however, the effectiveness of these techniques depends on a multitude of parameters, such as the properties of the substrate, the circuit's clocking scheme, etc., that need to be studied in order to implement them properly.

In general, substrate noise reduction methods can be categorized into three different classes: the first class consists of methods aimed at reducing the noise generated by digital blocks; the second class focuses on reducing the noise propagated through the substrate, and the last class tries to design noise-tolerant analog circuits. In this thesis, these classes will be referred to as noise injection reduction, noise propagation reduction, and noise reception reduction.

This chapter provides a review of noise reduction techniques. Since each of these methods can be a topic for a separate research, only a brief introduction to some of them is given, except for more detailed studies of two popular techniques, namely switching activity spreading and the use of passive guard-rings (GRs), from the first and the second classes, respectively.
5.1 Noise Injection Reduction

In general, techniques used in low-power design can be used to reduce switching noise, especially if they attempt to reduce circuit activity. However, care should be taken since in some cases using low-power techniques can even aggravate the noise [40].

As an example of a low-power technique, lower power supplies can be used for digital parts (not analog parts). A lower swing for digital nodes decreases the instantaneous current drawn from the supply; also use of a larger supply for analog circuits increases their relative noise margin [56]. One disadvantage of using this technique is that it may cause increased delay in logic gates, which reduces the speed of the circuit; however, it should be noted that in a logic block not all the gates need to switch quickly; therefore, less critical gates can be operated with lower supply voltages. Another disadvantage of this method is the extra routing and package pins required for different supply lines on the chip, which are not favourable in integrated circuits.

Switching activity spreading is another technique that changes the supply current waveform by introducing delays into the clock distribution network. This will spread the switching activity of logic gates in time, thus reducing the number of simultaneously switching gates. Since this technique introduces design complexity in large digital circuits, the idea can be applied only to those parts of the circuit that contribute the most to the noise, such as blocks that drive large capacitive loads. Furthermore, although this technique has been proven useful in the time-domain, its efficiency for RF applications, i.e., in frequency-domain, needs to be verified.
5.1.1 Switching Activity Spreading

Figure 5.1 illustrates the idea of switching activity spreading\(^1\) (SAS). In staggered digital circuits, part of the switching gates will be triggered with a properly delayed clock with respect to the rest of the circuit; therefore, the number of simultaneously switching gates will be reduced.

![Diagram of Switching Activity Spreading](image)

Figure 5.1: Switching activity spreading.

To investigate the effectiveness of this technique, the following experiment was performed. First, two chain of inverters were simultaneously switched, and the noise waveform was observed at the bulk node of a single transistor used as the noise sensor. Next, the same experiment was repeated by applying SAS, i.e., the clock signal of one of the chains was delayed by \(\frac{1}{4}\) of the clock period with respect to the other one. The results of both experiments are shown in Figure 5.2. As can be seen in Figure 5.2(a), the peak value of the noise has decreased by almost a factor of 2.

In addition to time-domain waveforms, the frequency content of the noise in both cases is shown in Figure 5.2(b). This graph reveals an important point; i.e., even though the noise frequency content has considerably decreased at some frequencies, this result is not a general rule. For example in Figure 5.2(b), the noise content at 650MHz has remained

\(^{1}\) Also known as activity staggering.
almost unchanged after applying SAS. Therefore, care should be taken in RF applications to make sure that SAS decreases the in-band noise.

5.2 Noise Propagation Reduction

Another noise reduction method is to prevent the noise from propagating through the substrate. Two strategies can be used: one is to increase the attenuation of the noise path, and the other one is to block the noise propagation. The simplest reduction scheme to increase the attenuation of the noise path is to increase the physical distance between the digital and analog circuitry. The efficiency of this technique was discussed in Chapter 3, where it was shown that the effectiveness of physical isolation is limited to lightly-doped substrates; moreover, this technique involves wasting of precious silicon area; therefore, several alternative methods have been exploited. Many of these techniques, such as the use of GRs, trenches, buried n-wells are studied in the literature [32, 65, 71]. It should
be noted that all of these techniques, except for passive guard-rings, require additional process features that might not be available or economically viable in all technologies. So far, passive GRs have been the most commonly used technique due to their effectiveness and relative simplicity; therefore, we will review their properties in more detail.

5.2.1 Passive Guard-Rings

Passive guard-rings are protective structures located around either the noise generating or sensitive blocks and are connected to dedicated supplies. There are two types of GRs: p⁺ and n-well GRs, which operate based on totally different principles, although their purpose is the same.

p⁺ GR provides a low-impedance path to the ground so that the noise travelling through the substrate is directed mainly to the ground before reaching sensitive devices. On the other hand, n-well GR tends to increase the impedance of the noise path, which will effectively push the noise into deep parts of the substrate and provide a higher impedance path or equivalently, more attenuation. In both cases, the GR is more effective if most of the noise travels through the surface of the chip. Some of the following questions may arise during the course of GR design:

- How do the properties of the GR change with frequency?
- What are the optimum dimensions of the GR?
- Where should it be placed?
- Should the GR fully enclose the noisy or sensitive part?
• How does the substrate type affect the efficiency of the GR?

SeismIC simulation results presented in the following sections reveal that in all cases the use of GRs significantly helps decreasing the amount of noise; therefore, passive GRs are an effective way to reduce substrate noise. To study GR properties, a simple lumped model representation of p$^+$ and n-well GRs will be used, as shown in Figure 5.3. In this figure, $R_{Sub}$ represents the substrate resistance, $R_{GR}$ is the resistance of the GR, $R_A$ and $C_A$ are the resistance and capacitance connecting the bulk of the sensitive device to the substrate, and $R_L$ is the lateral resistance between GR and the noise sensing node. In the n-well GR model (shown in Figure 5.3(b)) $C_{GR}$ is added to reflect the capacitance of the n-well to the substrate.

![Diagram of GRs in lightly-doped substrates](image)

(a) p$^+$ GR enclosing sensitive devices.

(b) n-well GR enclosing sensitive devices.

Figure 5.3: Lumped model of GRs in lightly-doped substrates.

It can be shown that in p$^+$ GRs, the lower the impedance of the GR ($R_{GR}$) the better
the noise suppression performance. In fact, the important parameters, which determine the efficiency of the GR, are the ratios of the GR impedance to the impedance of the substrate and the impedance coupling the sensitive node to the substrate. On the other hand, in n-well GRs, a higher GR impedance is more favourable, because the increased impedance will push the noise to deep portions of the substrate, hence increasing the overall impedance of the noise path and consequently, increase the attenuation.

**Frequency Dependence of GR Properties**

The GR model introduced in the previous section suggests that in p\(^+\) GRs, the effectiveness of the GR decreases as the frequency increases because the ratio of the impedance of the GR to the impedance of the sensitive node increases; therefore, less noise is directed to the ground through the GR. On the other hand, in the case of n-well GR, this might not be true because two competing mechanisms exist that control the impedance ratio. While the coupling of sensitive nodes to the substrate increases at higher frequencies, at the same time the impedance of the GR decreases, which can effectively decrease the impedance ratio. These arguments were investigated using SeismIC simulation results for a chain of inverters. Figure 5.4 shows simulation results of the amount of noise attenuation for various GR arrangements. To compare the effectiveness of GRs, the amount of additional isolation provided by each GR configuration as a function of frequency is shown in Figure 5.5, where the curve marked as 'No isolation' in Figure 5.4 is used as the reference.\(^2\)

As shown in Figure 5.5, while the performance of n-well GRs has improved with in-
Figure 5.4: Attenuation as a function of frequency for different GR arrangements.

Increasing frequency, for the other GR the results are the opposite. Another interesting point in the model for n-well GRs is that since at high frequencies the impedance due to $C_{GR}$ decreases, n-well GR can act as a sink path to AC ground. As a result, one can think of n-well GRs as p\(^+\) GRs at very high frequencies. This argument is in agreement with Figure 5.5 where at high frequencies the two plots of p\(^+\) and n-well GR tend to converge.

In all cases, it is important to connect the GR to a dedicated supply; otherwise the GR itself can provide an extra path for noise injection into the substrate.

The results shown in Figure 5.5 contrast with the previously reported results in [34] that the efficiency of p\(^+\) GRs is independent of frequency. The conflict comes from the fact that in the experiment in [34] a simple substrate contact was used as the noise sensor and no capacitive component was taken into account; thus the isolation did not change
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Figure 5.5: Additional attenuation provided by GRs as a function of frequency.

Effect of GR Width

Figure 5.6 presents the isolation provided by $p^+$ GR as a function of its width. As can be seen, the isolation increases monotonically as the width of the GR increases, suggesting that the wider the GR the lower the noise. These results could be predicted from the GR model because, as the width of the GR increases, the impedance of the noise return path to ground decreases, and so does the propagated noise.

Effect of GR Placement

Another important property to observe is the effect of the distance of the GR from the noise generation point. Figure 5.7(a) depicts the simulation results of the testbench introduced
Chapter 5. Evaluation of Reduction Methods

Figure 5.6: GR attenuation as a function of width.

Figure 5.7: Effect of GR placement.

(a) Results for single inverter.  
(b) Results for a more complicated digital circuit.
in Chapter 3, using a fixed-width GR at different distances from the noise generator. The physical separation between analog and digital circuits in this figure is 100\(\mu m\). As can be seen, more attenuation is achieved when the GR is located closer to the sensitive device. The worst isolation is achieved when the GR is placed halfway between the analog and digital blocks. Figure 5.7(b) illustrates the results of the same experiment using a more complicated digital circuit. The same behaviour is observed, but the location of the local minimum has changed, which is due to the change in the amount of the total capacitance in the digital circuit.

**Effect of GR shape**

Since the only operation of the p\(^+\) GR is to provide a path to a stable supply, one may wonder if it is necessary to implement a full ring GR, while open guards may have the desired performance. To show the effect of GR shape, three different GRs (shown in Figure 5.8) were examined using a chain of inverters circuit as a benchmark. Table 5.1 lists the results.

![Figure 5.8: Different GR shapes.](image)
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Protection Scheme | Attenuation(dB)
---|---
Without protection | 27.0
Protection with barrier | 39.8
GR with one side removed | 45.2
Full-ring GR | 46.6

Table 5.1: Noise attenuation using GRs with different shapes.

As shown in Table 5.1, the amount of isolation provided by a full GR is more than a single barrier; however, even using a barrier has a significant effect on the amount of noise propagation; therefore, one may consider using a barrier instead of a full-ring GR to save area in certain applications.

Effect of substrate type

Section 3.2 discussed that noise propagation properties through the substrate depend on the type of the substrate and its characteristics. Since the performance of GRs also depends on the impedance of the paths in the substrate and the GR, it is expected that the substrate type plays an important role in the efficiency of GRs.

Although Figure 5.7(a) shows that the placement of the GR is important in its isolation properties, this does not hold for epitaxial substrates. It should be noted that GRs are more effective in cases in which most of the noise travels through the surface of the chip; however, in epitaxial substrates, due to the low-resistivity of the bulk, the main path for noise propagation is through the deep portion of the substrate. In effect, increasing
the distance between the points does not increase the attenuation, as was observed before. The independence of the attenuation from the distance in epitaxial substrates is also inferred from the GR model in epitaxial substrates, as shown in Figure 5.9. As can be seen, only vertical impedances are important; therefore, increasing the distance does not change the GR’s noise attenuation.

![Diagram of lumped model of GRs in epitaxial substrates](image)

(a) p+ GR enclosing sensitive devices.

(b) n-well GR enclosing sensitive devices.

Figure 5.9: Lumped model of GRs in epitaxial substrates.

Simulation results also verify the previous discussion on the dependence of attenuation on the distance in various substrates. The results are shown in Figure 5.10. As can be seen, while the attenuation in lightly-doped substrates decreases monotonically as the distance increases, in epitaxial ones increasing the distance does not affect the attenuation.

---

3It should be noted that all the models used in this chapter apply only to moderate and large separations between analog and digital blocks. At very short distances the effect of lateral surface resistances should also be taken into account.
5.3 Noise Reception Reduction

This class of reduction techniques is typically used by analog designers to increase the immunity of their circuits to substrate noise. The most popular technique is the use of differential structures. Since substrate noise is mostly considered as common-mode noise, ideally it can be suppressed by differential signalling; however, due to the mismatches and the delay of noise propagation between the two inputs of the differential stage, they are not able to fully remove substrate noise. To increase the noise rejection capability, the layout must have the same parasitics coupling to each of the two differential branches, which requires a symmetric layout that can be achieved either by mirror or common-centroid symmetry.

On-chip decoupling capacitor is another technique that can be used to reduce both
noise generation and reception [72]. This technique is used both in digital and analog circuits to decouple power supply and ground lines. The additional capacitor placed between supply and ground, can act as an extra source of charge for transient currents in switching parts; therefore, a smaller transient current will be drawn from supplies; hence, less noise is induced on power lines.

As discussed in Chapter 3, use of PMOS transistors for signal handling parts, such as differential pair input transistors, and current mirrors will decrease the amount of noise reception because these devices are further isolated from the substrate by the underlying n-well. Finally, using a different supply line for analog circuits will decouple them from the noise on the supply lines of digital blocks.

5.4 Summary

In this chapter, various noise reduction techniques were introduced and discussed. Switching activity spreading was studied in time and frequency domains. It was shown that even though this technique is useful in time-domain, for RF applications it might not be helpful, since the frequency content of the noise at specific frequencies may remain unchanged after applying this technique.

In addition to SAS, passive GRs were also reviewed in detail, and the impact of several parameters on their effectiveness was investigated. Lumped models for GRs in different substrates were introduced and used to justify the simulation results. It was shown that, while the isolation property of $p^+$ GRs deteriorates as the frequency increases, n-well GRs might show an opposite trend; i.e., depending on the layout and structure of the circuit.
the effectiveness of this type of GR may improve. Furthermore, it was shown that at high frequencies, n-well GRs can act as p$^+$ GR. Finally, some general strategies for designing noise-tolerant analog circuits were given.
Chapter 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, substrate noise, as one of the main obstacles in highly-integrated circuits, was studied from three different aspects. First, the behaviour of the noise was explored in the time and frequency domains. Internal and external noise sources were considered and it was shown that external noise sources quickly dominate the overall noise as the inductance in power supply lines increases. The dependence of noise on a variety of parameters such as switching time and frequency of operation were also analyzed. The dependence of the noise behaviour on the substrate type was extensively studied and the differences between noise propagation properties in two most commonly used substrates, lightly-doped and epitaxial, were analyzed. The difference between PMOS and NMOS devices was also investigated and it was shown that, PMOS devices exhibit superior substrate noise performance as compared to NMOS transistors owing to the additional isolation provided by their underlying n-well.

Second, the effect of substrate noise on a typical LNA was investigated from a circuit-level point of view rather than the signal-level approach exploited by previous works. A new MOSFET model that includes substrate noise effects was introduced. It was shown
that, while with lowering the quality factor of the input network the noise figure of the LNA improves from the intrinsic device noise perspective, it deteriorates due to the effect of the substrate noise; therefore, there is a compromise between substrate noise and intrinsic device noise minimization inductively-degenerated LNAs.

Third, the properties of passive GRs, as the most popular noise reduction technique, were studied. It was shown that in contrast to previous results, the isolation efficiency of n-well GRs can improve by increasing frequency. In fact, an n-well GR at high frequencies can act as a p⁺ GR. Furthermore, the dependence of the additional isolation provided by GRs on several parameters such as the width, placement, and shape of the GR were investigated.

### 6.2 Future Work

Experimental verification of the approach proposed in Chapter 4 is a further step that should be taken as future work. Another possible extension to this work can be the study of the performance degradation of more analog circuits using the proposed MOSFET small-signal model. Furthermore, in addition to inductively-degenerated LNA, many other LNA configurations exist that require further research to identify the least sensitive LNA architecture to substrate noise.

In the software and CAD tool area, there are many opportunities that await exploration. The only commercially available substrate noise analysis tool is Substrate Noise Analyst by Cadence™, performance of which is mostly limited to digital circuits, i.e., the spectral analysis of substrate noise, which is crucial to noise analysis, is not addressed in
this tool; therefore, there is a need for a tool with RF capabilities. The current tool does not allow for simultaneous simulations of noise figure and substrate noise analysis; as a result, development of a tool with the capability of cosimulation of RF and substrate noise will be extremely valuable to analog designers.

This work has not addressed all possible noise reduction techniques; however, in addition to passive GRs, many other techniques exist that may be in some cases more efficient than passive guard-rings; the study of such techniques will also be a promising research direction.
Bibliography


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Appendix A

MOSFET Small-Signal Model

This appendix\(^1\) reviews the small-signal model of the MOS transistor used in noise analysis. Figure A.1 illustrates the comprehensive small-signal model of the MOS device including parasitic capacitances and various device noise sources.

![Detailed small-signal model of the MOS device](image)

Figure A.1: Detailed small-signal model of the MOS device, including device internal noise sources, parasitic capacitances, and body effect.

In this figure, \(R_{gpar}\) and \(\bar{e}_{ngpar}\) represent the parasitic resistance of the gate and the noise associated with it, \(g_g\) accounts for the effect of the distributed nature of the channel, \(\bar{i}_{nd}\) represents channel thermal and flicker noise, and \(\bar{i}_{ng}\) represents gate-induced noise. Parasitic capacitances between terminals of the device are also shown. Note that the substrate is assumed to be connected to the small-signal ground.

To simplify this model, we make some assumptions: we ignore \(R_{gpar}\) and \(\bar{e}_{ngpar}\), for

\(^1\)The material presented in this appendix are from [69].
they can be minimized by proper layout techniques; \( g_g \) is also neglected because its value is significant only at very high frequencies, i.e., frequencies close to the cut-off frequency of the device, and finally, we ignore body effect and parasitic capacitances (except \( C_{gs} \)); therefore, the simplified version of the model is as illustrated in Figure A.2.

![Simplified MOSFET small-signal model](image)

Figure A.2: Simplified MOSFET small-signal model (parasitic capacitances, gate distributed resistance, and body effect are ignored).

In this figure, two major device noise sources are included (i.e., \( \tilde{i}_{nd} \) and \( \tilde{i}_{ng} \)), the power spectrum of which are given by:

\[
\overline{i^2_{nd}} = 4kT\gamma g_{d0}\Delta f + \frac{K_f}{f_n} \Delta f \tag{A.1}
\]

\[
\overline{i^2_{ng}} = 4kT\delta g_g \Delta f \tag{A.2}
\]

where \( g_{d0} \) is the drain-source conductance at zero \( V_{DS} \), \( \gamma \) and \( \delta \) are channel noise and gate noise coefficients, respectively, \( K_f \) is an empirical coefficient and parameter \( g_g \) is:

\[
g_g = \frac{\omega^2C_g^2}{5g_{d0}} \tag{A.3}
\]

Now, we apply superposition to this model to find the total output current due to these noise sources and replace them with a single noise source, \( \tilde{i}_{ndg} \), as shown in Figure A.3.
This single noise source can be written as:

\[ \tilde{i}_{\text{ndg}} = \tilde{i}_{\text{n},ng} + \tilde{i}_{\text{n},nd} \quad \text{(A.4)} \]

where \( \tilde{i}_{\text{n},ng} \) and \( \tilde{i}_{\text{n},nd} \) represent the portion of the total noise due to gate-induced and channel thermal noises, respectively.

First, we find the noise output current due to gate-induced noise (\( \tilde{i}_{\text{n},ng} \)). Since the total output noise depends on the impedances connected to the gate and the source, these components are also included in Figure A.4 and denoted by \( Z_g \) and \( Z_{\text{deg}} \). As can be seen in this figure, the output current due to \( \tilde{i}_{\text{ng}} \) can be found using the following equation:
Figure A.5: Equivalent circuit to find $Z_{gs}$.

$$
\tilde{i}_{n,ng} = g_m Z_{gs} \tilde{i}_{ng}
$$

where $Z_{gs}$ is the impedance seen between the gate and the source. To find the value of this impedance, we use Figure A.5, based on which, by writing KCL equations at the source and the gate of the transistor we have:

\begin{align}
-i_{test} + \frac{v_{test}}{1/(sC_{gs})} + g_m v_{test} &= \frac{v_1}{Z_{deg}} \quad (A.6) \\
v_{test} + v_1 = i_{test} + \frac{v_{test}}{1/sC_{gs}} \\ Z_{gs} \frac{v_{test}}{i_{test}} &= \frac{1}{sC_{gs}} \parallel \frac{Z_{deg} + Z_g}{1 + g_m Z_{deg}} \quad (A.8)
\end{align}

Therefore, $Z_{gs}$ can be found as:

To calculate the effect of $\tilde{i}_{nd}$, we use Figure A.6, based on which, the following equations
Figure A.6: MOSFET model for the calculation of the effect of channel thermal noise.

can be written:

\[ I_{\text{n,d}} = I_{\text{nd}} + g_m V_{gs} \quad (A.9) \]

\[ V_{gs} = -V_1 \frac{1/(sC_{gs})}{1/(sC_{gs}) + Z_g} \quad (A.10) \]

\[ V_1 = I_{\text{n,nd}}(Z_{\text{deg}} || \left( \frac{1}{sC_{gs}} + Z_g \right)) \quad (A.11) \]

therefore:

\[ I_{\text{n,nd}} = \left( 1 - \left( \frac{g_m Z_{\text{deg}}}{Z_{\text{deg}} + Z_g} \right) \right) I_{\text{nd}} = \eta I_{\text{nd}} \quad (A.12) \]

Now, using superposition principle we find \( \tilde{I}_{\text{n,dg}} \) in Figure A.3 as:

\[ \tilde{I}_{\text{n,dg}} = \eta \tilde{I}_{\text{n,d}} + g_m Z_{gs} \tilde{I}_{\text{n,g}} \quad (A.13) \]

As discussed in Chapter 4, the mean-square value of the noise (i.e., its power) is the main
parameter used in the noise figure calculations, which can be found as follows:

\[
\overline{r_{ndg}^2} = \overline{i_{ndg}^*i_{ndg}} = (\eta^*i_{nd} + g_mZ_{gs}^*i_{ng})(\eta^*i_{nd} + g_mZ_{gs}i_{ng})
\]

\[
= |\eta|^2i_{nd}^*i_{nd} + i_{nd}^*i_{ng}g_m\eta^*Z_{gs} + i_{nd}^*i_{ng}(g_m\eta^*Z_{gs})^* + \overline{i_{ng}^*i_{ng}}g_mZ_{gs}|^2
\]

\[
= |\eta|^2\overline{r_{nd}} + 2\Re\{i_{nd}^*i_{ng}g_m\eta^*Z_{gs}\} + \overline{\overline{i_{ng}^*i_{ng}}g_mZ_{gs}}|^2
\]

\[
= |\eta|^2\overline{r_{nd}} + 2\Re\{\frac{i_{nd}^*i_{ng}g_m\eta^*Z_{gs}}{\sqrt{\overline{\overline{r_{nd}^2}}}} + \frac{\overline{\overline{i_{ng}^*i_{ng}}g_mZ_{gs}}^2}{\overline{\overline{i_{ng}^*i_{ng}}}}\} 
\]

(A.14)

Recalling that \(c\) was defined as the correlation factor between channel thermal noise and gate-induced noise, we can rearrange this equation in the following form:

\[
\overline{r_{ndg}^2} = \overline{r_{nd}^2}|\eta|^2 + 2\Re\{c\frac{i_{ng}^*g_m\eta^*Z_{gs}}{\overline{\overline{i_{nd}^*i_{ng}}}} + \frac{\overline{\overline{i_{ng}^*i_{ng}}g_mZ_{gs}}^2}{\overline{\overline{i_{ng}^*i_{ng}}}}\} 
\]

(A.15)

which is the equation used in Chapter 4 to derive the noise figure of the amplifier; therefore, the final MOSFET small-signal model is as shown in Figure A.3 with \(\overline{r_{ndg}^2}\) given by Equation A.15.
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