CONTROL OF SINGLE PHASE PARALLEL INVERTER SYSTEMS

by

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ABSTRACT

We have proposed two new control methods which allow two or more single phase PWM inverter modules to operate in parallel. Our main goals are to achieve balanced load sharing among all inverter modules and to eliminate any circulating currents in the system. The first proposed control technique is the current imbalance method in which each inverter module is provided with a current imbalance signal. The current imbalance signal is calculated for each module as the difference between the expected module current an the actual module current. Inverter modules use the current imbalance signal to deliver the expected current to the load; thus, the system can achieve balanced load sharing. Computer simulations of this control method provides satisfactory results for typical load values. However, at low loads, inverters do not share the load current and the system suffers from circulating currents. The prototype testing of the current imbalance method indicates more problems with this technique. Due to low noise immunity and sensitivity of the system, the load current is not fully shared among modules even for typical loads. The second proposed control technique is the single voltage control method which is similar to a conventional current mode control, with the exception of having two or more current loops (inverter modules). This technique uses a single voltage control block which provides a reference current for all the inverter modules. The effect of adding or removing inverter modules on the stability of the system has been studied. The system can be designed to tolerate a few faulty modules. Both the computer simulation and prototype testing of this technique give satisfactory results: good load sharing, no circulating currents, and stable operation over a large range of loads. Therefore, we recommend using the single voltage control method in most applications.

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1. Introduction

Pulse Width Modulation (PWM) inverters are widely used in Uninterrupted Power Supplies (UPS) to power critical loads such as communication systems, computer systems, and hospital equipment in case of an interruption in the main power. One of the challenges in designing commercial PWM inverter systems is to design a PWM inverter which is capable of delivering high power, with high reliability, and at a low cost. High power inverters need to dissipate a large amount of heat and handle large currents; these two factors, in general, result in low reliability and high cost. One solution to this problem is to design lower power inverter modules and use them in parallel to achieve high power and reliability. Figure 1 shows an inverter system which consists of N inverter modules connected in parallel. Each inverter module provides $1/N^{th}$ of the load current.

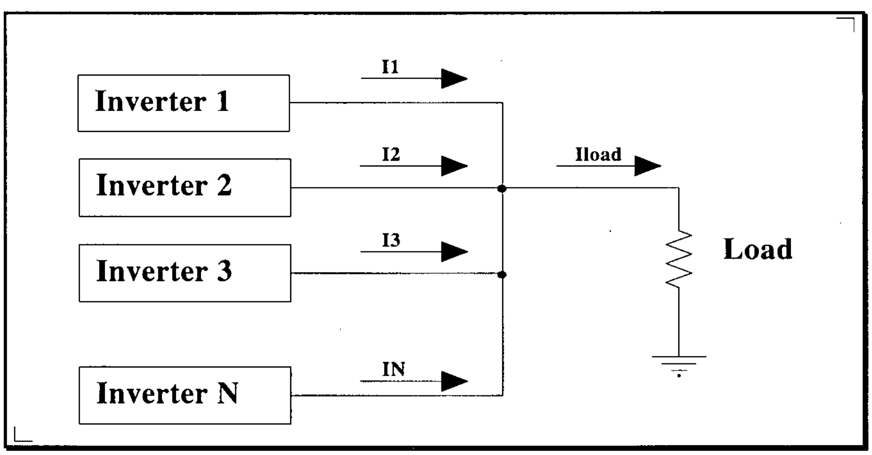

Figure 1. A System of Paralleled Inverter Modules

The outputs of all inverter modules are connected together and form the system output. Since the outputs of the inverter modules are directly connected together and since each inverter module is capable of delivering considerable amount of power, we need to pay special attention to the inverter design. In such a system, ideally, all modules should provide the same amount of current to the load. In other words, the load current should be shared equally among all the inverter modules. Furthermore, a faulty unit should be isolated from the rest of the system without disturbing the power delivered to the load. This enables us to have a system with no single point of failure.

Parallel inverter systems, made of identical modules, have several advantages over a single module system:

- **Improved heat dissipation:** Each module generates a fraction of the total heat which can be dissipated more easily.

- **Improved current handling:** Each module switches a portion of the total current. Power transistors are easier to find and circuit design is much simpler.

- **Higher reliability (redundancy):** A parallel inverter system is more reliable than a single inverter for two reasons. First, each module handles a lower current and dissipates less heat which improves module reliability. Secondly, a fault detection circuit in each module would isolate the module when the module fails. Therefore, when one or more of the parallel modules fail, output power is not interrupted nor seriously disturbed, i.e. there is no single point of failure.

- **Simplified manufacturing:** Utilizing the same inverter module to build systems with different power capabilities greatly simplifies the manufacturing process. Fewer number of components need to be stocked and fewer number of boards need to be designed. Also, assembly and testing are improved due to fewer variations.

- **Lower cost:** Component and manufacturing costs drop due to increased volume.

- **Easier shipping and installation:** Shipping and installation become easier and more cost effective as module sizes decrease.

- **Field expandable:** A modular system can be easily expanded to increase output power or degree of redundancy by adding more modules. Customers can easily expand the system in the field as their requirements change.

1.1. Design Objectives

Design of a parallel inverter system is not a trivial task. One cannot simply connect two or more PWM inverters in parallel and expect proper operation. Inverters are very sensitive and even a small difference in their operating parameters can cause several modules to fail. This is mainly due to the fact that inverters are capable of delivering considerable amounts of power and are designed to respond quickly to load changes. A small phase or voltage difference among the inverter modules may cause the output current to exceed module limitations and damage the output transistors. Also, if modules operate in the current limiting mode, then the overall system does not operate efficiently.

A parallel inverter system, therefore, should be designed to achieve the following design objectives: balanced load sharing, module synchronization, fault protection, maximized redundancy, and minimized module interdependent. These design objectives are discussed in the following sections.

1.1.1. Balanced Load Sharing

Assuming that all inverter modules are designed to have the same maximum power rating, then all inverter modules should contribute equally to the load current. Unequal output currents cause excessive stress on some modules which leads to reduced reliability and increased module failure. Or even more seriously, some modules may operate in the current limiting mode, which results in a distorted output waveform and perhaps uncontrolled interaction among the modules. This may result in a commutative failure of the modules which would eventually result in partial or total system failure.

Assuming N identical inverter modules, we can express the balanced load sharing or simply load sharing criteria with the following equation:

$$I_{inv1} = I_{inv2} = \ldots = I_{invN} = \frac{1}{N} \times I_{Load} \tag{1-1}$$

If the inverter modules are designed to have different power rating, the balanced load sharing criteria will change accordingly. In this thesis, we assume that all inverter modules are designed to have the same power rating.

1.1.2. Module Synchronization

All inverter modules, which are connected in parallel, should have the same output voltage, frequency, and phase. If the instantaneous voltages of two paralleled modules are not equal, a current, known as crosscurrent or circulating current, will flow from the module with the higher voltage to the module with the lower voltage. Due to the low output impedance of the inverter modules, even a small voltage difference can contribute to a large circulating current. Circulating currents reduce the power efficiency of the system, cause an output overload, and can result in module failures. We can categorize circulating currents into two types - low frequency circulating currents and high frequency circulating currents. These two types of circulating currents are discussed next. One of our design objectives is to eliminate or minimize both types of circulating currents.

1.1.2.1 Low Frequency Circulating Current

Low frequency crosscurrent or circulating current is generated when the paralleled inverter modules are slightly out of phase or have different voltage amplitudes. This type of circulating current has the same frequency as the output.

Figure 2 shows the simulation results when connecting two PWM inverters in parallel without having any additional control circuit for parallel operation. The output voltages of the two inverter modules were slightly out of phase (by about 2 degrees). As we can see from the simulation results, the two inverter currents, I_{out1} and I_{out2}, are not equal. Also, there are time instances at which one inverter is sourcing current and the other inverter is sinking some of that current (see the inverter currents at 10 ms time instant). As we can see, part of the current is circulating from one inverter to the other inverter; the total current is not delivered to the load. Although the resulting output voltage V_{out} and the load current I_{out} are acceptable, the system is not operating efficiently.

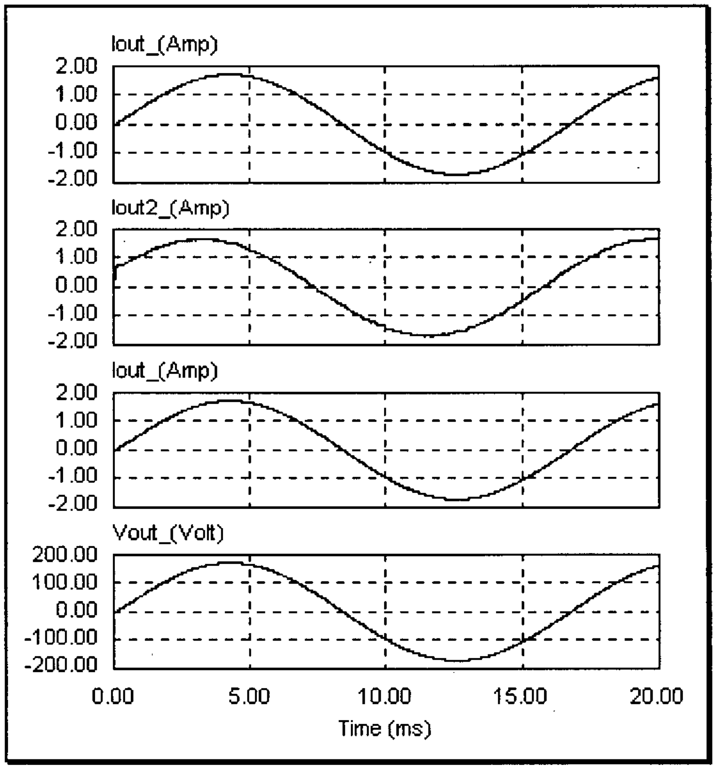

Figure 2. Low Frequency Circulating Currents

Low frequency circulating currents cause inverter modules to operate inefficiently and can results in module/system failure. Therefore, when designing a parallel inverter system, we should pay considerable attention to module synchronization and reduction of low frequency circulating currents.

1.1.2.2 High Frequency Circulating Current

A high frequency circulating current, which is generally referred to as high harmonic crosscurrent, is generated when two or more PWM inverters with insufficient output filters are connected in parallel. In this case, each inverter generates a different PWM waveform which causes a slightly different instantaneous voltage at the output of each inverter module. These slightly different instantaneous voltages, which are generally at the frequency of the PWM switching oscillator, cause a high frequency circulating current from one inverter module to the other.

Figure 3 shows the simulation results obtained from connecting two PWM inverters in parallel with insufficient output filters at the output of each inverter module. As we can see, the resulting output voltage V_{out} and load current I_{out} are acceptable and the system seems to operate properly. However, the two inverter currents, I_{out1} and I_{out2}, suffer from high frequency circulating currents.

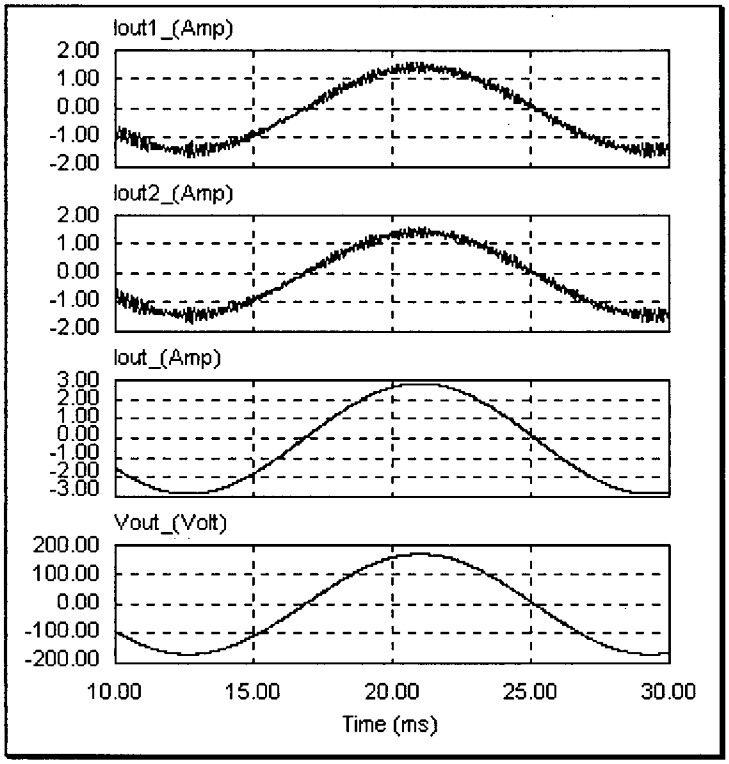

Figure 3. High Frequency Circulating Currents

Eliminating or reducing high frequency circulating currents improves the power efficiency of the system, prevents the system from intermittently operating in the current limiting mode, and reduces the emitted EMI noise.

1.1.3. Fault Protection

One of the challenges in designing parallel inverter systems is to protect the system against module failures. For example, a module may fail in a way that its output is shorted to the ground. This type of failure disturbs the output voltage and may also damage other modules. A faulty module should be detected and insulated from the rest of the system before any disturbance is noticed by the load. Adding fault protection circuitry to a parallel inverter system increases system reliability at the cost of increasing the complexity and price of the system. Detailed design of fault protection circuits are beyond the scope of this thesis paper. In this thesis, we only provide block diagrams to demonstrate how fault protection can be added to the proposed parallel inverter systems.

1.1.4. Maximize Redundancy

Failure of an inverter module should not cause any disturbance in the power delivered to the load. When an inverter module fails, the remaining inverter modules would contribute a higher current to compensate for the failed module or modules (as long as the individual module current is less than the maximum rated current of that module). In other words, there should be no single point of failure in the system. However, it is very difficult to design a fully redundant system. In most systems, there are a few common blocks which are theoretically a single point of failure. However, in practice, it is acceptable to have single points of failure as long as they have low probability of failure. Therefore, we should give special consideration to the design of the common blocks of the system. The common blocks or the single points of failure in the system must be designed to have a low probability of failure. They should operate correctly even if some of the modules fail.

1.1.5. Minimize Module Interdependence

Generally speaking, we would like the inverter modules to be independent from one another. In an independent system, a faulty module will not disturb the operation of the other modules. Module independence is very important in high-reliability inverter systems. To achieve absolute independence, it is essential that each module uses the feedback of only those variables which can be measured locally within the module. Module output voltage, output current, and inductor current are some of the local variables that are usually monitored and controlled by most inverter modules. Absolute module independence is difficult, if not impossible, to achieve in most cases. Modules need to monitor some external variables to operate properly. These external variables are points of module interdependence.

For example, in most systems, an external current feedback is provided to each module which specifies the current that the module should deliver to the load. This signal is usually calculated by a power distribution block which measures the load current and determines the share of each module. Obviously, modules are no longer independent when they all receive an external current reference signal. To increase reliability in this case, we need to design a robust power distribution block and make sure that a fault in any module does not cause any problems in the power distribution block. A system designed in this way has interdependence; however, this interdependence does not necessarily mean that a module failure causes a total system failure. In practice, it is acceptable to have module interdependence to signals which have a low probability of failure.

1.2. Survey of Previously Proposed Parallel Systems

In this section, we will review some of the previously published work on the design and implementation of parallel inverter systems. First, we look at different methods used to connect inverter modules in parallel. Then, we study various control methods employed in the parallel inverter systems.

1.2.1. Parallel Connection Methods

The output of the inverter modules can be connected together and eventually connected to the load in a number of ways. The main objective is to use a connection method that can tolerate slight variations in the modules output voltage and phase.

Four different methods of connecting inverter modules have been documented in publications. The *series inductor method* is often used in high-frequency PWM inverters where efficiency, size, and cost are considered to be important. The other three connection methods, *coupled inductor, series transformer*, and *parallel transformer*, are used in earlier low-frequency systems where size and weight are not a determining factor. In the following subsections, we briefly discuss how each connection method works and discuss the advantages and disadvantages of each method.

1.2.1.1 Series Inductor

Figure 4 shows three closely synchronized inverters connected together in parallel using the series inductor method. Each inverter is connected to the critical bus by a series inductor and a static switch. The static switch can be opened quickly for fault protection. The series inductor introduces an impedance between each inverter and the load and improves load sharing [1, 2]. The high frequency circulating currents are also reduced significantly. The series inductors simply filter out the high frequency circulating currents which are caused by the difference in the PWM waveforms of the inverters.

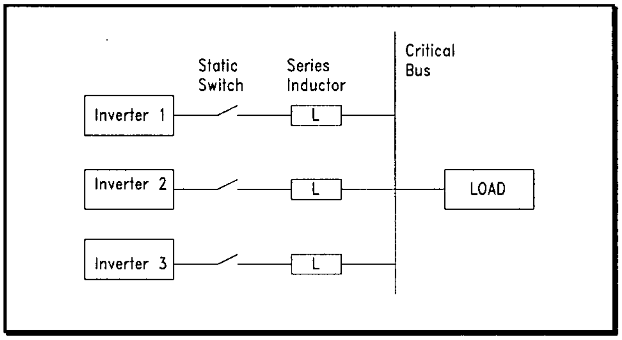

Figure 4. Series Inductors Method

The series inductor can reduce both low and high frequency crosscurrents. If the series inductor is intended to reduce low frequency as well as high frequency crosscurrents, the resulting inductor becomes bulky and expensive. However, if the series inductor is only used to reduce the high frequency crosscurrent, we can use a smaller and more cost effective inductor.

The series inductor connection method also simplifies the design of the fault protection circuit by limiting the rate of change of the current drawn from each module. For example, without a series inductor, a shorted module sinks a large amount of current. However, with a series inductor, the current increases at a slower rate. Therefore, the series inductor provides a longer delay before the maximum current limit of the system is reached. This added delay gives more time to the fault protection circuit to detect the fault and isolate the shorted module.

To summarize, the series inductor method is easy and cost effective to implement, improves the current sharing, reduces the high frequency crosscurrent, and simplifies the fault protection design. However, the inverter design must still provide both synchronization and current sharing features. The series inductor by itself is not a complete solution.

1.2.1.2 Coupled Inductors

Closely synchronized inverters can be paralleled using coupled inductors [3, 4]. Figure 5 shows two inverter modules connected to a load using the coupled inductor method. The inductance introduced by the coupled inductor improves the load sharing and reduces the crosscurrent better than the series inductor. When the output voltages of the two inverters are equal and in phase, the total magnetic flux in the coupled inductor becomes small. A small magnetic flux causes the voltage drop across the coupled inductor to approach zero. However, as the difference between modules' instantaneous voltages or their phase increases, so does the magnetic flux in the coupled inductor which results in a larger inductance. This higher inductance helps to balance the inverter currents and reduces the crosscurrent.

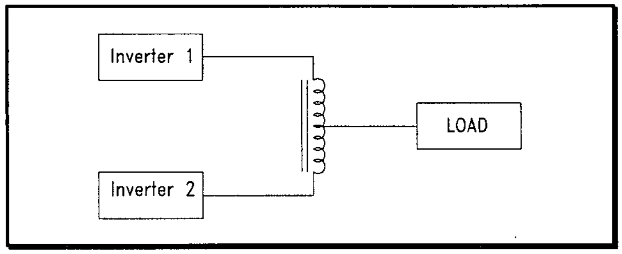

Figure 5. Coupled Inductors Method

There are some limiting problems in using coupled inductors. Manufacturing a coupled inductor for paralleling two modules is simple; however, manufacturing coupled inductors for three or more modules is not a trivial task. Moreover, the modules have to be magnetically linked which reduces the modularity of the system. Furthermore, if the coupled inductor is intended to suppress the low frequency crosscurrent, it becomes bulky and expensive.

1.2.1.3 Series Transformer

Inverter modules can be connected together using a series transformer as shown in Figure 6 [1]. When an inverter module fails, the output voltage drops by an amount which is inversely proportional to the number of paralleled modules. If the number of paralleled modules is large, the resulting voltage drop is small and insignificant.

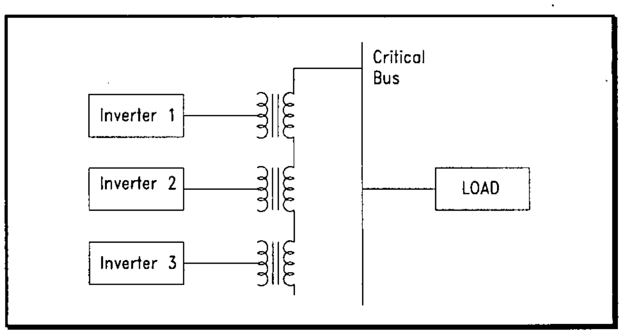

Figure 6. Series Transformer Method

The main advantages of this design are simplicity and fault tolerance. Inverter modules need to be roughly synchronized and there is no need for complicated control loops for synchronization. Fault protection is achieved automatically since a faulty module causes a small drop in the output voltage rather than a total system failure. Faulty modules can be replaced without any interruption to the load. However, the series transformer works at line frequency and is bulky and expensive. Moreover, the system is not fully modular and it can not be easily expanded in the field. These disadvantages make series transformers unfavorable in newer high-frequency systems where the designers are trying to achieve increased efficiency and expandability with reduced cost and size.

1.2.1.4 Parallel Transformer

Inverter modules can be connected using a parallel transformer as shown in Figure 7 [2]. The parallel transformer provides isolation and coupling for paralleled inverter modules. Series inductors reduce the crosscurrent and improve the load sharing.

Each inverter module must have a current control loop to share the load current. Inverters must also be phase synchronized to reduce circulating currents.

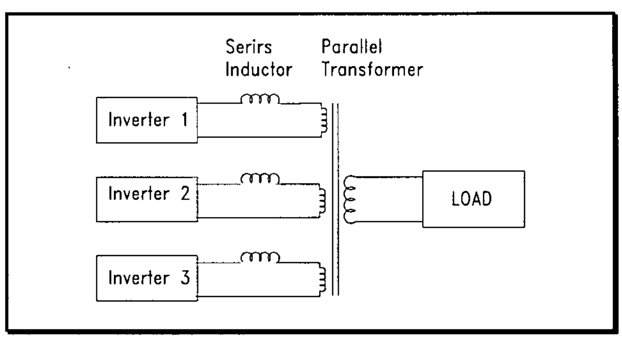

Figure 7. Parallel Transformer Method

Although this topology uses a transformer which is considered to be a single point of failure, the system is modular and can be partially expanded in the field (at an initial cost). For field expandability, we only need to provide extra, unused primary coils on the transformer. These coils may be used to connect additional modules in future as the power requirement increases.

Again, the transformer operates at low frequency and is considerably large and expensive. Furthermore, the current and voltage control loops that each module requires makes the design complicated and expensive. Thus, there are few advantages in using the parallel transformer method.

1.2.2. Parallel Control Methods

A number of different control methods have been used for parallel operation. The main objectives of the control method is to establish the desired output voltage and load current, achieve module synchronization, improve load sharing, and reduce circulating currents. In this section, we discuss three previously published control methods which all have excellent characteristics. These control methods have been simulated and tested and satisfactory operation has been reported.

1.2.2.1 Power Deviation Control

One way to achieve synchronization and current sharing in a parallel system is to control the power that each module delivers to the load. Each module can calculate the power that it is delivering to the critical bus. If the module knows how much power it is supposed to deliver to the load, it can calculate the power deviation. The power deviation method controls the power delivered by each module and makes all modules to contribute the same power to the load (i.e. minimizing the power deviation). Assuming that all inverter modules are identical, the system can calculate the total power delivered to the load and divide that by the number of active modules to calculate the power that each module is supposed to deliver.

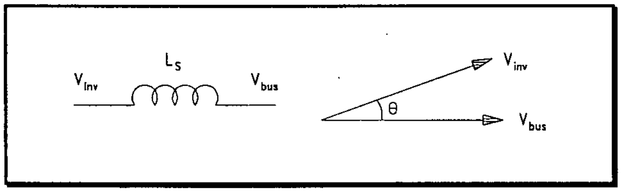

Figure 8. Measuring Real and Reactive Power Using a Series Inductor

It is known that, for stable operation, a power system requires control of both the real power P and the reactive power Q [10]. If the system only controls the real power circulating currents are not controlled and the system may not operate in the optimum range. However, if we control both real and reactive powers, the output current is shared among modules and circulating currents are minimized. Assuming that each inverter module is connected to the critical bus with a series inductor (see Figure 8), we can calculate the real power P and the reactive power Q by the following equations [9]:

$$P = \frac{V_{inv} . V_{bus}}{\omega . L_S} . \sin(\theta) \tag{1-2}$$

$$Q = \frac{V_{inv}^2}{\omega . L_S} - \frac{V_{inv} . V_{bus}}{\omega . L_S} . \cos(\theta) \tag{1-3}$$

Where:

V_{inv}: Inverter output voltage

V_{bus}: Critical bus voltage

θ: Power angle (between V_{inv} and V_{bus})

ω: Line frequency

L_S: Inductance of the series inductor

From these equations, we see that P depends predominantly on the power angle θ, and Q depends predominantly on the magnitude of the inverter voltage V_{inv}. Thus, to control both real power and reactive power we need to control the power angle and the inverter voltage. The power angle is controlled by the inverter frequency; therefore, by slightly changing the inverter frequency, we can control the real power P. The reactive power Q can be controlled by slightly varying the inverter output voltage.

The control block diagram shown in Figure 9 illustrates an implementation of the power deviation method [1]. The system calculates ΔI which is the difference between (I_L / n) (where I_L is the total load current and n is the number of active modules) and the module's current I_{inv}. Using this current deviation ΔI, the module calculates the deviated real power ΔP and the deviated reactive power ΔQ. The inverter voltage and frequency are controlled to minimize the calculated power deviations ΔP and ΔQ, respectively.

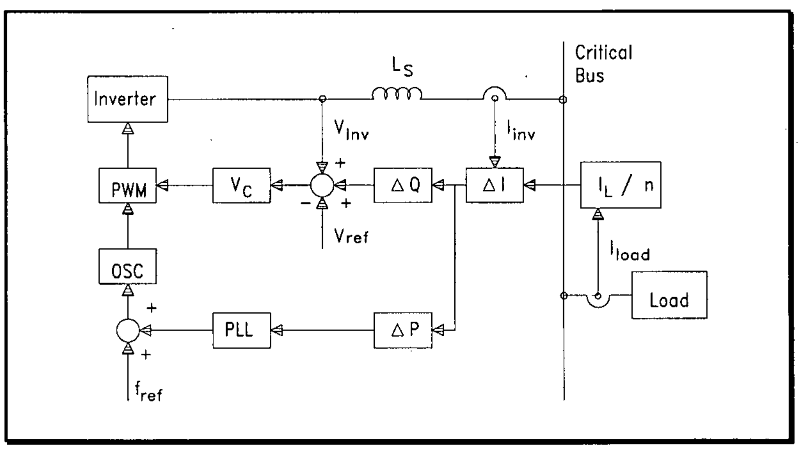

Figure 9. Power Deviation Control

This method has many advantages. Except the quantity "I_L / n", all variables are local. The system has a modular design and achieves good load sharing and small circulating currents. The main disadvantage of this design is the problem of calculating the real and reactive powers. These calculations require multiplication which requires either complicated analog circuits, or a microcontroller. Two other implementations of the power deviation control method for paralleling inverter modules have also been reported [5, 9].

1.2.2.2 Current-Controlled Voltage Source Inverters

One of the major concerns in the design of a parallel inverter system is to control the output current of the modules to improve load sharing and to reduce crosscurrents. We can use current-controlled voltage source inverters to achieve both of these goals.

Figure 10 shows a traditional current-controlled voltage source inverter [8]. The inverter has an inner (or minor) current loop and an outer voltage loop. The current loop sets the inductor current to the value given by the reference current I_{ref}. The reference current has three components. Feedforward reference current I_{ref1} which reduces the delay in the current loop and improves the inverter response to rectified capacitive loads. The voltage controller reference current I_{ref2} adjusts and stabilizes the output voltage. The filter capacitor reference current I_{ref3} establishes the no load output voltage. These three loops set the reference current I_{ref} such that it generates the desired output voltage given by the sinusoidal reference voltage V_{ref}.

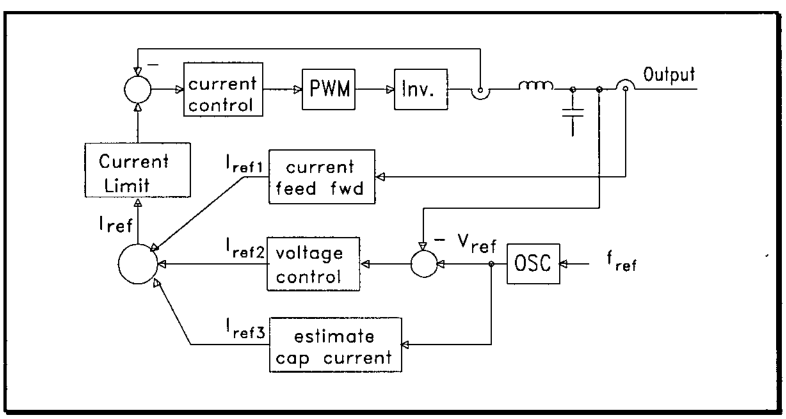

Figure 10. A traditional Current Controlled Voltage Source Inverter

This design can be modified for use in parallel systems. The inverter shown in Figure 11 adds two additional feedback loops to the traditional current controlled voltage source inverter of Figure 10 [1]. The first added feedback loop changes the frequency of the voltage reference V_{ref}, which also changes the inverter output frequency, based on the real power deviation. This ensures that all modules are contributing the same real power to the load which reduces the circulating currents. The second added feedback loop ensures that the current deviation of the module ΔI is zero. This ensures balanced load sharing.

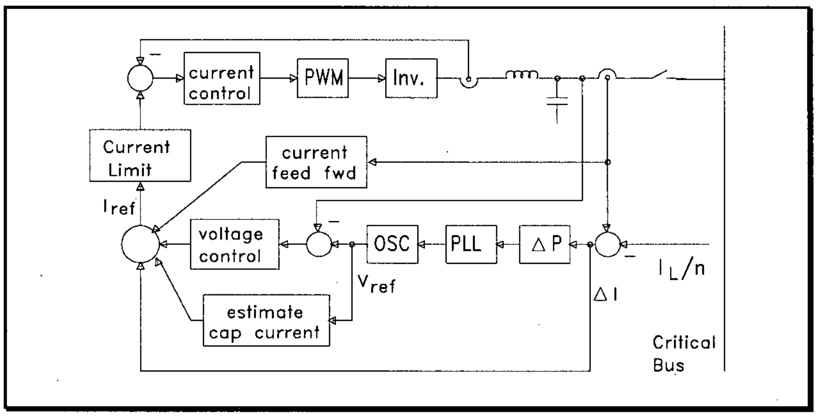

Figure 11. Current Controlled Voltage Source Inverter Method

This system has many good characteristics. The step load response of the system is excellent due to the fast response of the feedforward current loop. The output voltage is stable even when no load is connected to the system because of the capacitor current estimator loop. The inverter operates appropriately in a parallel system because of the power deviation and current deviation loops. Further investigation and development are required to fully understand the advantages and disadvantages of this design.

1.2.2.3 Combination of Voltage Source and Current Source Inverters

Another control method for parallel operation of inverter systems uses both Voltage-Controlled voltage source PWM Inverters (VCPI) and Current-Controlled current source PWM Inverters (CCPI). Figure 12 shows one implementation of such a system [6]. The VCPI module is used to establish the output voltage which also establishes the output current. A number of CCPI modules are added to supply the remaining load current.

These current source inverters follow the load current that is established by the VCPI module.

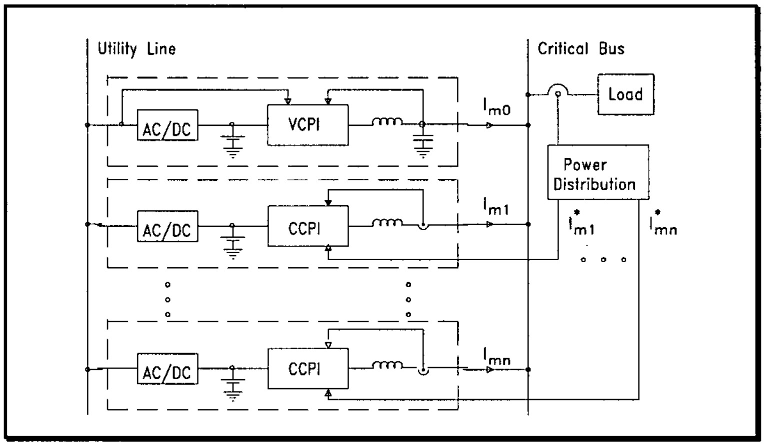

Figure 12. Combined Voltage and Current Source Inverters Method

Figure 13 shows the equivalent circuit diagram of the system. As we can see, the main module VCPI is modeled by a voltage source V_{m0} and the parallel CCPIs modules are modeled by current sources I_{m1} to I_{mn}. Inductor L_{m0} and capacitor C_{m0} are the output filter of the VCPI module; Inductors L_1 to L_n are the series inductors of the CCPI modules which reduce the circulating currents.

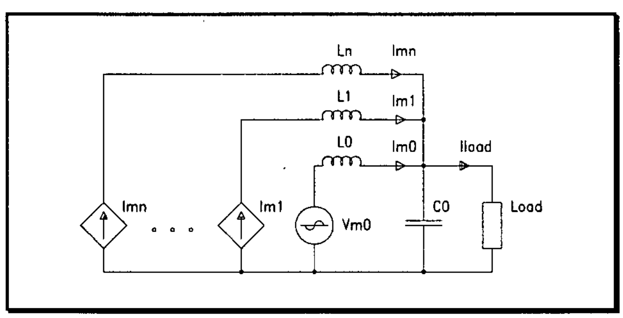

Figure 13. Equivalent Circuit of the Combined Inverter

This method of paralleling inverters has a number of advantages. First of all, it is easy to design and implement the system. All modules used in this design follow the well known design topologies and standards. In other words, AC/DC, VCPI, and CCPI modules are commonly used blocks. All control parameters, except the reference currents, I^*_{m1} to I^*_{mn}, are generated locally within the module. This simplifies module interconnection and improves fault protection. The only external signal to the module is the reference current I^*_{m1} to I^*_{mn}. The reference currents are generated by the power distribution block which monitors the load current and determines how much current is supposed to be provided by each module. To improve system reliability and to create a practically redundant system, we require a robust power distribution block. The power distribution block should also be aware of the faulty modules and it should automatically redistribute the current among all working modules.

The main disadvantage of this design is that the system has only one VCPI module; if this module fails, the system will not operate. This gives the system another single point of failure, in addition to the power distribution block, weakening the redundancy and reducing system reliability. However, a very robust VCPI can be designed to achieve a pseudo-redundant system.

1.2.2.4 Droop Control

One of the goals in designing parallel inverter systems is to reduce the number of module interconnections. Having no interconnection among the inverter modules not only increases the reliability of the system, but also increases the flexibility of the system by not restricting the modules to be physically close to one another. One control technique, which does not require any interconnecting wires among the inverter modules, is the droop control method. In conventional droop control method, load sharing is achieved by changing (drooping) the voltage and frequency of the inverter [11]. Voltage and frequency droop control systems work well for linear loads. However, when connected to nonlinear loads, the system does not share the load harmonics. Recently, a new variation of the droop control systems has been reported which works well with both linear and nonlinear loads [12, 13]. Figure 14 shows a droop control inverter module capable of driving nonlinear loads.

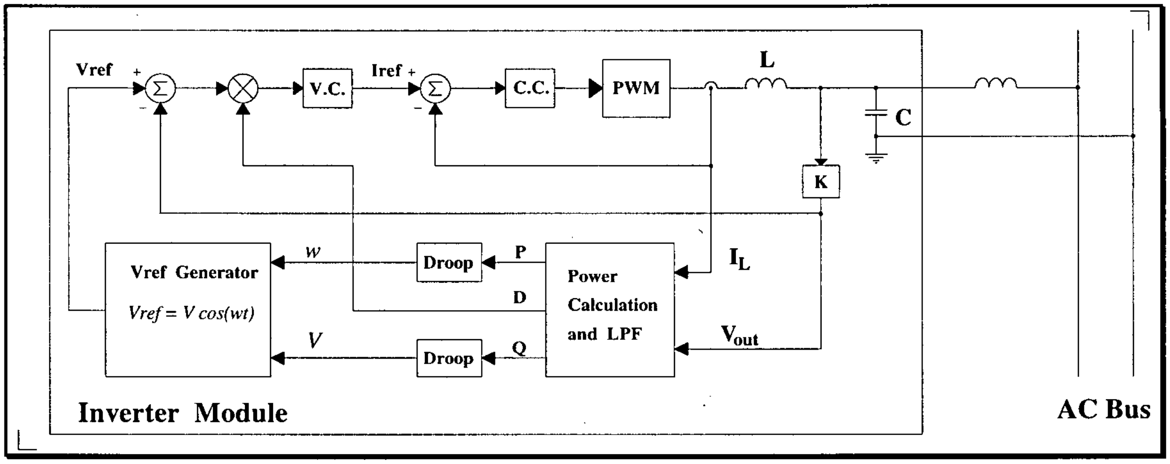

Figure 14. Droop Controlled Inverter Module

As we can see from Figure 14, each droop controlled inverter module has an inner current loop and an outer voltage loop, similar to a conventional current mode controller. The inductor current, I_L, and the output voltage, V_{out}, are the two feedback signals of the inner and outer loops, respectively. However, unlike the conventional current mode control, each inverter module calculates the real power, P, the reactive power, Q, and the distortion power, D. The calculated P and Q are used to control the frequency, w, and the amplitude, V, of the voltage reference, respectively. Therefore, the frequency and the amplitude of the system output voltage is controlled such that all modules share the real and reactive power delivered to the load [12]. Also, to provide sharing of the current harmonics, which are generated by nonlinear loads, each inverter module calculates a distortion power, D, which is the power delivered by all the current harmonics (except the fundamental harmonic) [12]. The calculated D is used to control the gain of the voltage loop. Changing the gain (and the bandwidth) of the voltage loop causes the load harmonics to droop in a manner in which the load current harmonics are shared by the inverter modules. Thus, the system slightly distorts the output voltage to achieve sharing of the load harmonic currents.

The droop control method has many advantages. No interconnecting wires are required which makes the modules independent and increases the reliability of the system. Also, inverter modules can be placed far away from one another. The main disadvantage of this control method is that the output voltage suffers from voltage and frequency droop as. Also, a microprocessor or a DSP is required to calculate the power terms, which increases the cost and complexity of the system.

1.3. Thesis Objective and Outline

The main objective of this thesis is to present two new control methods for connecting single phase PWM inverter modules in parallel. Our objective is to design a parallel system in which the inverter modules share the load current with no circulating currents. The specific objective is to develop control methods that are simple to implement, low-cost, and yet achieve a certain degree of redundancy and module interdependence.

The proposed control methods are tested using computer simulations and prototype circuits. Our objective is to verify the control methods, highlight the potential sources of problems, compare the two methods, and make recommendations.

In this thesis, we propose two control methods for connecting PWM inverter modules in parallel. Chapter 2 introduces the proposed methods and discusses the operation of each method. Chapter 2 also explains how we can add fault protection circuitry to each system and increase the reliability of the system. In chapter 3, we discuss the design of a single inverter module. Various switching and control topologies are discussed before selecting the appropriate topology for our parallel inverter system. We then calculate and design various components of the inverter module including the current loop and voltage loop controllers. Chapter 4 reviews the test results of the two proposed methods. Both computer simulation and experimental test results are presented and discussed. The conclusion is presented in chapter 5. The advantages and disadvantages of the proposed control methods are discussed and a few areas for future work are high lighted.

2. Our Proposed Approach

In this chapter, we propose two control methods for connecting PWM inverter modules in parallel – the current imbalance method and the single voltage control method. Both methods are designed to achieve balanced load sharing and to reduce circulating currents.

2.1. First Proposal: Current Imbalance Method

This section describes the first proposed method for connecting PWM inverters in parallel.

2.1.1. Concept

Our main objective is to achieve load sharing among the PWM inverter modules which are connected in parallel. One method for achieving current sharing is to use a feedback signal and force each module to deliver a predetermined percentage of the load current. In this method, we use a feedback signal which is proportional to the difference between the current that the module is supposed to deliver to the load and the current that the module is actually delivering to the load. In other words, the feedback signal is proportional to the module's "Imbalance Current". This concept is illustrated in Figure 15.

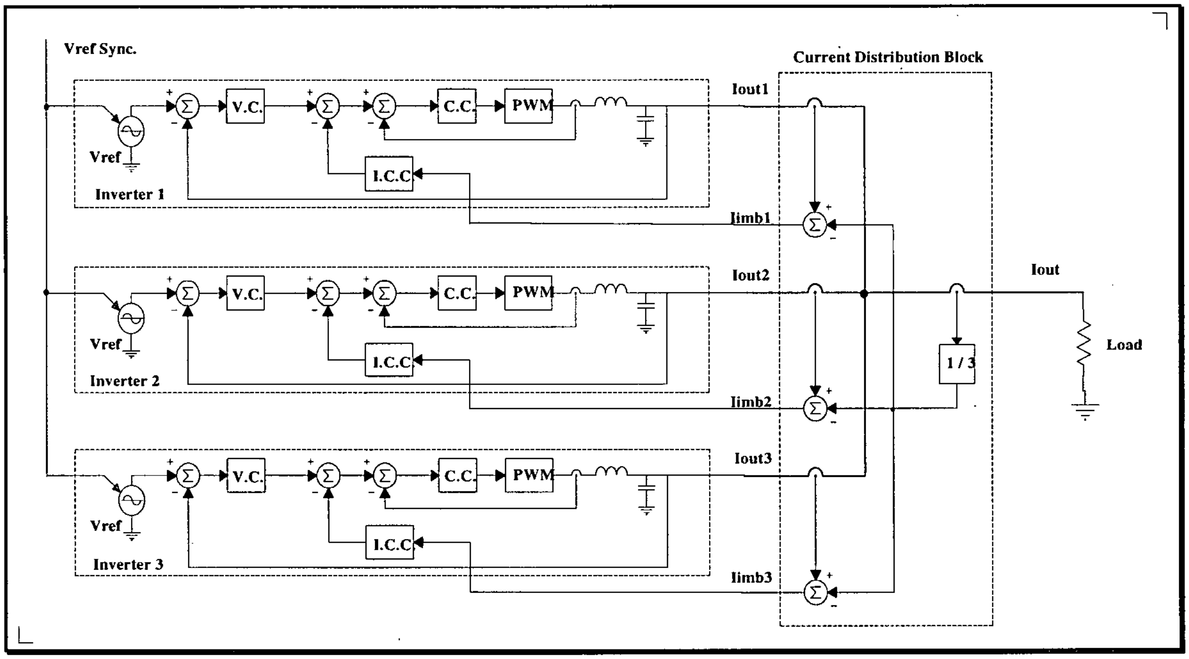

Figure 15. Paralleling PWM Inverters Using the Current Imbalance Method

Figure 15 shows three PWM inverters which are connected in parallel. Each inverter module is a "Current-Controlled Voltage-Source" PWM inverter consisting of an inner current loop and an outer voltage loop. Each inverter module has two inputs – the reference voltage synchronization signal, $V_{ref\text{-}sync}$, and the current imbalance signal, I_{imbX}. The reference voltage synchronization signal ensures that all the module's reference voltages, V_{ref1} to V_{ref3}, are synchronized together. $V_{ref\text{-}sync}$ is required to reduce the low frequency circulation currents (see section 1.1.2.1). The current imbalance signal, I_{imbX}, ensures that the output current provided by each module is exactly what the module is supposed to deliver to the load. Current imbalance signals, I_{imb1}, I_{imb2}, and I_{imb3}, are generated by the power distribution block. Each current imbalance signal is the difference between the current that the module is providing and the current which the module is supposed to deliver to the load. Assuming that we have N identical inverter modules, which are connected in parallel, then we would want each module to deliver "$1/N$" of the total load current. Therefore, I_{imb1} can be calculated as:

$$I_{imb1} = I_{out1} - \frac{1}{N} I_{load} \tag{2-1}$$

$$I_{imb1} = I_{out1} - \frac{1}{N}(I_{out1} + I_{out2} + \ldots + I_{outN}) \tag{2-2}$$

2.1.2. Discussions

In the following subsections, we will discuss some of the issues that concern the design and implementation of the current imbalance method for paralleling PWM inverters.

2.1.2.1 Load Sharing

To understand how the current imbalance method achieves load sharing, let us analyze the operation of the current control loop for one of the modules. Figure 16 shows the current loop for the first inverter module. The current loop has three inputs - I_{ref1}, I_{imb1}, and I_{L1}. The module reference current, I_{ref1}, is generated by the module's voltage control loop. I_{ref1} is proportional to the current which the module should supply in order to establish the desired output voltage. The current imbalance signal, I_{imb1}, is generated by the power distribution block. As we will see soon, I_{imb1} will adjust the module's output current, I_{out1}, and forcing it be the exact current for balanced load sharing. The module's inductor current, I_{L1}, is needed for the current loop control. The other important internal signal is the effective reference current, I_{ref1*}. The effective reference current is the reference current, I_{ref1}, after it has been adjusted by the current imbalance signal I_{imb1}. The effective reference current is calculated using the following equation:

$$I_{ref1*} = I_{ref1} - I_{imb1} \tag{2-3}$$

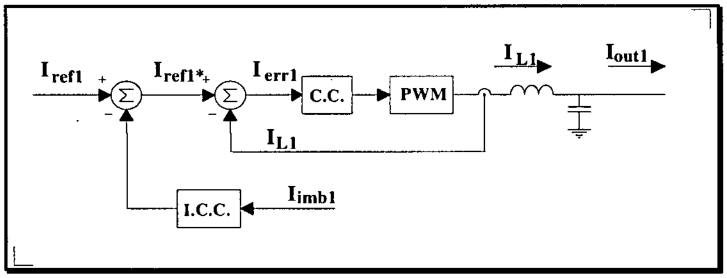

Figure 16. Imbalance Current Control Loop

To start, let us assume that the system is in perfect balance and that all modules are contributing the same amount of current to the load. In this case:

$$I_{out1} = I_{out2} = \ldots = I_{outN} = \frac{1}{N} I_{load} \qquad \textbf{(2-4)}$$

Putting the above value for I_{out1} in equation 2-1, the current imbalance signal, I_{imb1}, becomes zero and I_{ref1*} becomes equal to I_{ref1}. Therefore, the imbalance current control loop becomes identical to a conventional current control loop [14]. Thus, under balanced conditions, the current imbalance feedback does not affect the operation of the current control loop. The *N* paralleled inverter modules operate as *N* independent modules and provide equal currents to the load.

Now, we consider the case in which the system is not balanced. Let us assume that due to component tolerances in the voltage loop, module 1 reference current, I_{ref1}, is bigger than what it is supposed to be. A bigger I_{ref1} causes I_{out1} to be bigger then I_{out2} which causes I_{imb1} to become positive. This positive imbalance signal reduces the I_{ref1*} which causes the output current I_{out1} to reduce. As we can expect, the negative feedback caused by the current imbalance signal, I_{imb1}, reduces I_{out1} until a balance condition is established in which all inverter modules provide the same amount of current to the load.

Similarly, if I_{ref1} happens to be less than what it is supposed to be, then I_{out1} drops and I_{imb1} becomes negative. A negative I_{imb1} causes I_{ref1*} and I_{out1} to increase until a balanced condition is established in which all modules contribute the same amount of current to the load.

Therefore, the negative feedback provided by the current imbalance signal, I_{imbX}, causes all modules to have the same effective reference current, I_{refX*}, regardless of the variation in the module's reference current, I_{refX}.

2.1.2.2 Average Current Mode Control

The performance of the inner current loop is critical to the sharing of the load current in a parallel inverter system Two different control methods can be used in the current control – the peak current mode control and the average current mode control [14]. In this section, we will illustrate that an average current mode controller should be used in a current imbalance inverter system.

Figure 17 shows the relationship between the inductor current and the current reference signal for both peak and average current mode control methods. As we can see in a peak current mode control (Figure 17.A), as soon as the instantaneous inductor current exceeds the value indicated by the current reference signal, the PWM transistors are switched, which causes the inductor current to drop. Thus, the peak of the inductor current is proportional to the current reference and therefore the average inductor current is less than the value indicated by current reference signal. However, in the average current mode control (Figure 17.B), the average inductor current is proportional to the current reference signal and therefore the peak of the inductor current is greater than the value indicated by the current reference signal.

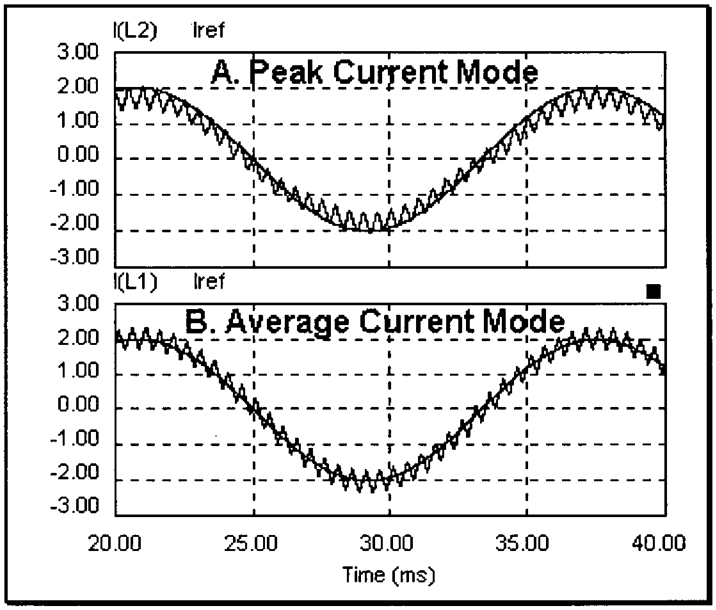

Figure 17. Inductor Current in Peak and Average Current Mode Controls

As we discussed before, the current imbalance feedback is proportional to the difference between the actual and expected module output currents (refer to Figure 15). Therefore, the current imbalance signal, I_{imb1}, is related to the module output current, I_{out1}, which is an average value. The current imbalance signal, I_{imb1}, controls the inductor current. Therefore, it is better to use an average current control mode controller. If we use a peak current controller, the difference between the peak and average current values introduces additional error in the calculated imbalance current. This error degrades the current sharing performance of the system.

2.1.2.3 Limited Load Range

One of the challenges in the design of PWM inverters is the stability of the system over a wide range of loads. As we will see in later sections, a parallel inverter system using the current imbalance method becomes unstable at low loads (i.e. as the load resistance increases). The control loops are designed to perform well at typical load values. However, as the load changes, the performance and the stability of the system degrades. Our tests show that the current imbalance system performs poorly at low loads. The load current is not shared equally by the inverter modules and the system suffers from circulating currents. Also, system may even become unstable at no load.

Beside the control loop design factors, there is another factor which adds to the instability of the system at low loads. The ICC controllers are typically realized with Op-Amps (Operational Amplifiers). Practical Op-Amps have imperfections including input offset errors. At low load currents, the Op-Amp input offset errors become significant and effect the stability of the system.

2.1.2.4 Fault Protection

The parallel inverter system using the current imbalance method (Figure 15) is prone to a complete system failure if one of the inverter modules fails by shorting the module's output to the ground. In this case, the system output is shorted to the ground which causes the load voltage to collapse. Furthermore, if inverter modules are not protected by an output current limiting circuit, the remaining inverter modules of the system will also fail due to excessive output current. Thus, a single module failure can result in a complete system failure. A fault protection circuitry needs to be added to overcome this problem.

In the following discussion, we assume that inverter modules have output current limiters which protect modules against any output short circuit. As we discuss in section 3.2, output current limiters can be easily implemented in the current mode PWM inverters by limiting the reference current, I_{refX}.

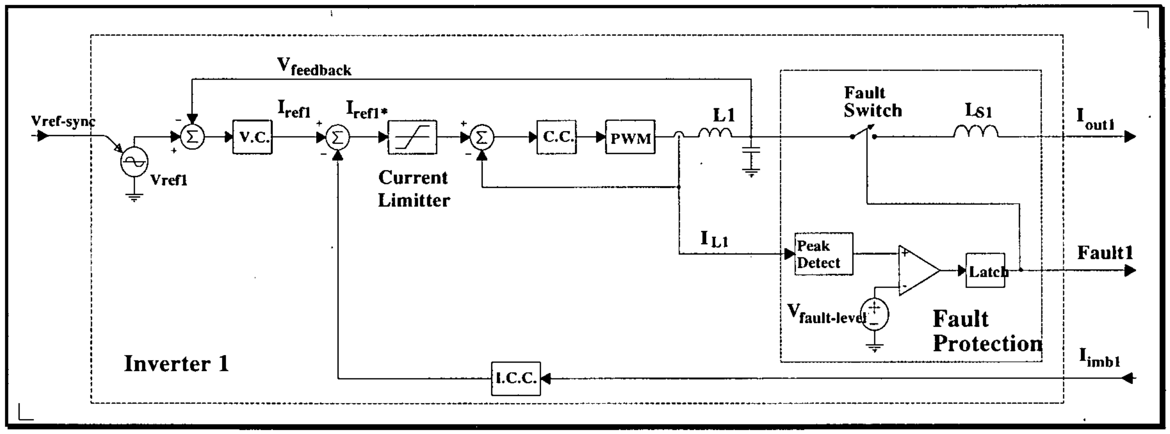

Figure 18. Fault Protection Circuitry

Now, we will discuss how a fault protection circuitry can be added to the inverter modules to prevent a total system failure in case of a module output short-circuit failure. Figure 18 shows one implementation of a short-circuit protection circuitry which disconnects the output of the module from the rest of the system in case of an excessive output current (output short-circuit). If the peak of the inductor current, I_{L1}, exceeds a predetermined fault level, $V_{fault\text{-}level}$, then a fault condition is latched. This fault indication signal, *Fault1*, causes the fault switch to open, which disconnects the output of the faulty module from the rest of the system. The fault indication signal, *Fault1*, is also used by the current distribution block.

Special care is required to ensure that in case of a module short-circuit, only the faulty module detects a fault and not any of the other modules. This can be achieved by correctly selecting the $V_{fault\text{-}level}$ and also adding a series inductor, L_{S1}, to the output of each module. This added inductance ensures that the current in the faulty module rises faster than the other modules; therefore, the faulty module detects the fault first and isolates itself from the system. The series inductor also acts as the module series inductor, which reduces the high frequency circulation currents.

The next issue to consider is what happens in the current distribution block when a module detects a fault. As we discussed before, the current distribution block calculates the current imbalance feedbacks, I_{imbX}, by subtracting the output current of each module, I_{outX}, from the desired load sharing current, I_{out} / N (where N is the number of active inverters). When a module fails, the current distribution block needs to be informed so it can compensate for the current which was provided by the faulty module. Figure 19 shows how module fault indication signals, *Fault1, Fault2*, and *Fault3*, can be used to compensate for module failures. When all modules are operating correctly, all the switches are open and the voltage divider (made by the three resistors) divides the load current, I_{out}, by 3. If one of the modules fails, the logic block closes the *S1* switch which changes the voltage divide ratio to "*1 / 2*". The output current is now divided by 2 which is the number of working modules. If two of the modules fails simultaneously, the logic block closes both *S1* and *S2* switches, changing the voltage divide ratio to "*1 / 1*". The output current is now divided by 1 which is the number of working modules. As we can see, the current distribution block proposed in Figure 19 can automatically compensate for faulty modules.

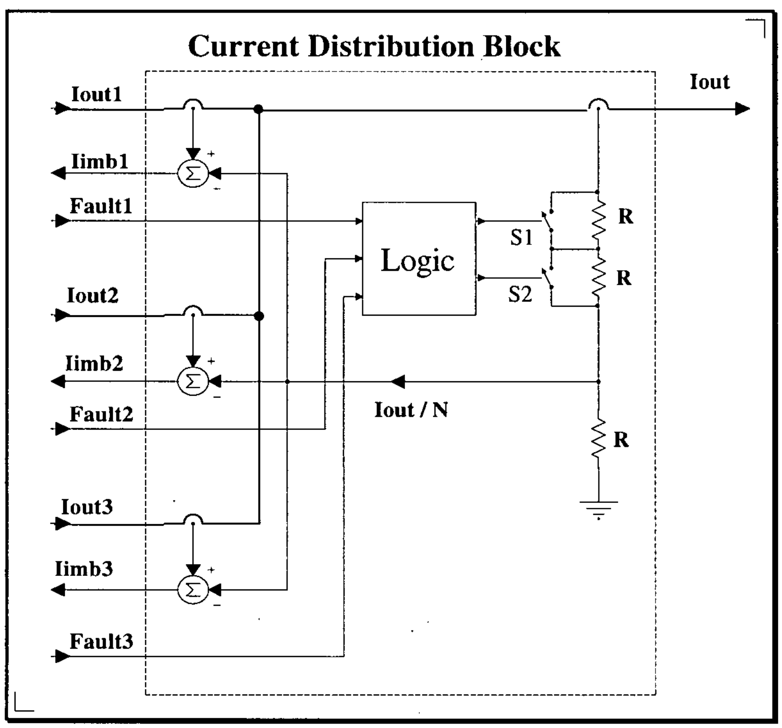

Figure 19. Power Distribution Block with Fault Detection Control

2.1.2.5 System Redundancy and Single Point of Failure

Our secondary design objective in parallel inverter systems is to maximize the system redundancy by reducing the number of "single points of failure" in the system. As we can see from Figure 15, the most obvious single point of failure in the system is the current distribution block. We will show that the current distribution block has a relatively low probability of failure (compared to the PWM inverters). Therefore, this single point of failure does not significantly reduce the redundancy of the system.

The current distribution block connects the three module's output currents, I_{out1}, I_{out2}, and I_{out3}, together to generate the load current, I_{out}. The path connecting these four quantities together carries a large current and; therefore, it is prone to failure. By using high gauge wires and good connectors, we can easily reduce the probability of failures in this high current path. All the other sections of the current distribution block operate at low currents which have a much smaller probability of failure. The module' output currents, I_{out1}, I_{out2}, and I_{out3}, and the load current, I_{out}, are usually measured by Current Transformers, CTs, which are basically a loop of wire acting as the secondary of a transformer. Due to their passive construction and small voltages induced in the CTs, the failure rate for the CTs is very low. A voltage divider is used to generate "I_{out} / N" which represents the current that each module should contribute to the load for balanced load sharing. The probability of failure of the voltage divider is relatively low because it uses resistors and analog switches which operate at low voltages. The last section of the current distribution block is summing junctions which generate the current imbalance signals I_{out1}, I_{out2}, and I_{out3}. These summing junctions are generally implemented by Op-Amps working at signal currents. Thus, they also have a low failure rate. Therefore, we can conclude that the overall probability of the failure of the current distribution block is relatively low. Thus, having this single point of failure does not significantly reduce the overall system redundancy.

2.2. *Second Proposal: Single Voltage Control Method*

This section describes the second proposed method for connecting PWM inverters in parallel.

2.2.1. Concept

Another method to achieve current sharing among parallel PWM inverters is to use a single voltage controller. The voltage controller block provides a reference current for all the PWM inverter modules. Since the reference current to all of the inverters is the same, all inverters provide the same amount of current to the load which results in balanced load sharing. This concept is illustrated in the following figure:

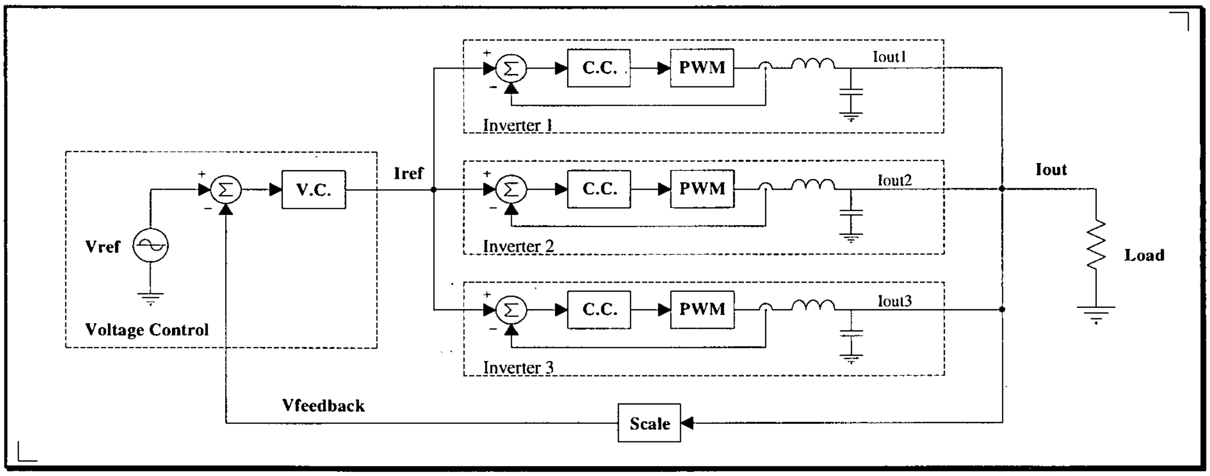

Figure 20. Paralleling Inverters Using the Single Voltage Control Method

Figure 20 shows three PWM inverters which are connected in parallel. Each inverter module is basically a current control loop which forces its inductor current, I_{L1}, I_{L2}, or I_{L3}, to be the same as the reference current I_{ref}. The inductor currents are filtered by the module's output capacitors to generate the module output currents I_{out1}, I_{out2}, and I_{out3}. These three equal output currents are added together to form the load current I_{out}. The voltage control block compares the reference voltage V_{ref} and the feedback from the output voltage $V_{feedback}$ and sets the reference current I_{ref} such that the output voltage is always proportional to the reference voltage.

This implementation is similar to a single Current-Controlled Voltage-Source PWM Inverter [15] with the exception of having N current loops connected in parallel. Each of these N current control blocks provide *"1 / N"* of the load current. The effect of paralleling N current loop on the stability of the system is discussed in section 2.2.2.2.

2.2.2. Discussions

In the following subsections, we discuss some of the design and implementation issues which need to be considered for proper operation of a parallel PWM inverter system using the single voltage control method.

2.2.2.1 Load Sharing

Load sharing is an intrinsic property of the single voltage control method for paralleling PWM inverters. All inverter modules are connected to the same current reference, I_{ref}. The inductor current of each module is proportional to the reference current, I_{ref}. As it can be seen from Figure 21, the ratio of the inductor current to the reference current, "I_{Li} / I_{ref}", is established by the amount of the feedback signal. This ratio depends on the gain of the current transformer, K_{CT}, and the gain of the voltage divider made by R_1 and R_2:

$$\frac{I_{Li}}{I_{ref}} = K_{CT} \cdot \frac{R_2}{R_1 + R_2} \tag{2-5}$$

The gain of the current transformer, K_{CT}, depends on the number of turns of the CT and the resistor R. Since the tolerances in the resistor values and in the number of turns of the CT are relatively small (about 1%), we can easily achieve the same "I_{Li} / I_{ref}" for all the inverter modules. Therefore, the inductor currents of all the inverter modules are practically equal.

$$I_{L1} = I_{L2} = ... = I_{LN} = I_{ref}.K_{CT}.\frac{R_2}{R_1 + R_2} \tag{2-6}$$

Assuming that the module capacitor currents, I_{C1}, I_{C2}, ...,I_{CN}, are small compared to the module inductor currents, I_{L1}, I_{L2}, ...,I_{LN}, module output currents, I_{out1}, I_{out2}, ...,I_{outN}, are equal. In other words, all modules share the load current equally.

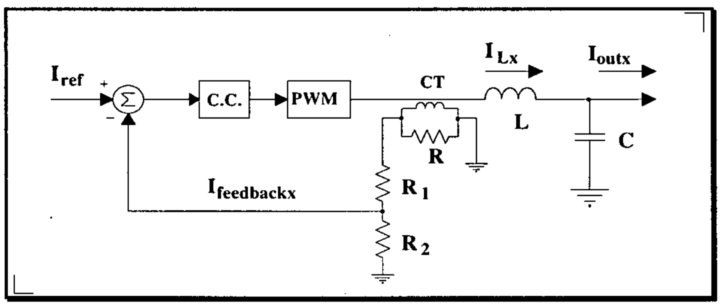

Figure 21. Current Control Loop

The assumption that the module capacitor currents are much smaller than the module inductor current is only true when we have a relatively large load. This assumption is not true if the system has no load. However, when the system has no load, in all practical situations, it is not important if the modules do not share the load current equally. The currents are too small to cause problems for any of the inverter modules. Also, in practice, we can not generally assume that the capacitor currents are equal because commercial capacitors have 10-20% tolerance.

2.2.2.2 Stability of the System and the Number of Parallel Modules

In this section, we study the effect of adding or removing inverter modules on the stability of the system. As we will see, the relative stability of the voltage loop (and the system) is affected when an inverter module is added or removed. Therefore, when designing the voltage loop, we need to ensure that the system remains stable with the specified minimum and maximum number of units.

The stability of the parallel inverter system depends on the stability of the current loops in the system and the stability of the voltage loop. The system has N current loops (each inverter module is basically a current loop). We design the current loop in each module to meet the required stability criteria. Since the inverter modules work independent from one another, the stability of the current loops in the system is not affected by the number of the inverter modules.

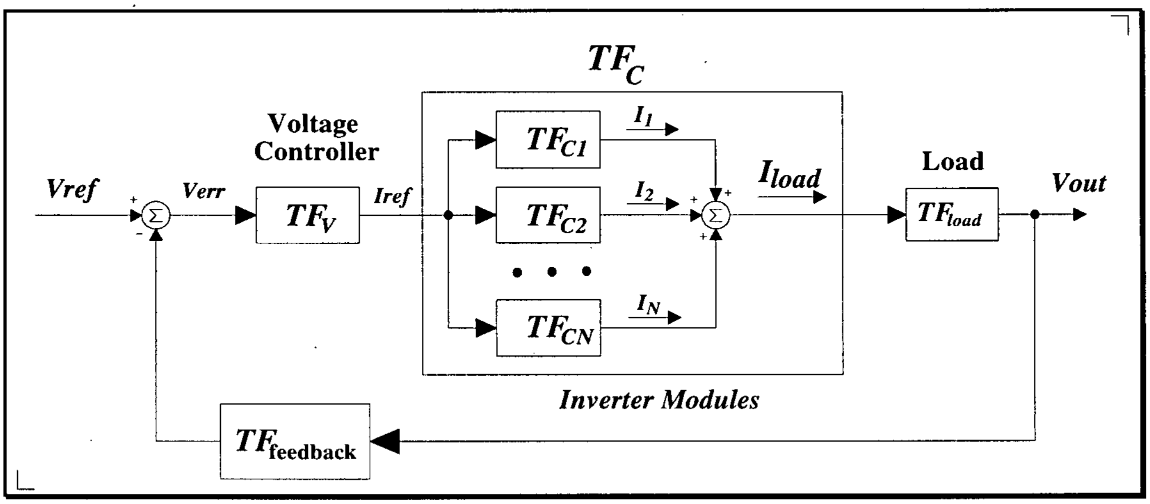

Figure 22. Voltage Loop of a Parallel Inverter System

Now, let us look at the stability of the voltage loop. The stability of the voltage loop is determined by the gain and the phase margins which are calculated from the open loop transfer function of the voltage loop [16]. From Figure 22, we can see that the open loop transfer function of the voltage loop is given by:

$$TF_{Voltage-Loop} = TF_V \cdot TF_C \cdot TF_{load} \cdot TF_{feedback} \qquad \textbf{(2-7)}$$

Where:

$TF_{Voltage\_Loop}$: Open loop transfer function of the voltage loop

TF_V : Transfer function of the voltage controller

TF_C : Transfer function of the system current loop (I_{load} / I_{ref})

TF_{Ci} : Closed loop transfer function of the ith inverter (I_i / I_{ref})

TF_{load} : Transfer function of the load (V_{out} / I_{load})

$TF_{feedback}$: Transfer function of the voltage feedback path

Now, let us determine the relationship between the transfer function of the system's current loop and the close loop transfer function of the inverter modules:

$$I_{load} = I_1 + I_2 + ... + I_N \tag{2-8}$$

$$\frac{I_{load}}{I_{ref}} = \frac{I_1}{I_{ref}} + \frac{I_2}{I_{ref}} + ... + \frac{I_N}{I_{ref}} \tag{2-9}$$

$$TF_C = TF_{C1} + TF_{C2} + ... + TF_{CN} \tag{2-10}$$

From equations 2-7 and 2-10, we can conclude that:

$$TF_{Voltage-Loop} = TF_V \cdot (TF_{C1} + TF_{C2} + ... + TF_{CN}) \cdot TF_{load} \cdot TF_{feedback} \tag{2-11}$$

The open loop transfer function of the voltage loop, $TF_{Voltage\text{-}Loop}$, depends on the closed loop transfer function of each inverter module, TF_{Ci}. However, the closed loop transfer function of each inverter is almost equal to the unity for the frequency range in which the voltage loop operates. Figure 23 shows the closed loop frequency response (bode plot) of the inverter module designed in chapter 3.

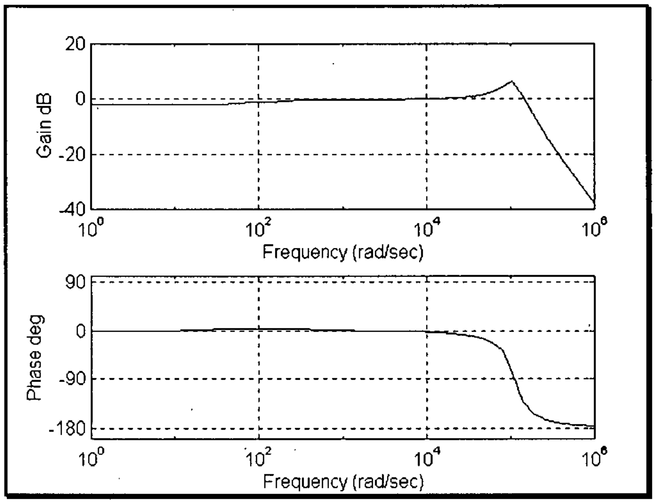

Figure 23. Frequency Response of a Typical Inverter Module

As we can see, inverter modules have unity gain (0 dB) and zero phase difference for frequencies below 10^4 radians/second. Since the crossover frequency of the voltage loop in our design is about 6×10^3 radians/second (see chapter 3), as far as the voltage loop is concerned, each inverter module has 0 dB gain and 0 degrees phase. In other words, the closed loop transfer function of each inverter module, TF_{Ci}, is almost one. Therefore, open loop the transfer function of the voltage loop can be written as:

$$TF_{Voltage-Loop} = TF_V \cdot (1+1+...+1) \cdot TF_{load} \cdot TF_{feedback} \tag{2-12}$$

$$TF_{Voltage-Loop} = N \cdot TF_V \cdot TF_{load} \cdot TF_{feedback} \tag{2-13}$$

From equation 2-13, it is obvious that adding or removing inverter modules changes the open loop gain of the voltage loop and effects the stability of the system. Therefore, we need to design the voltage loop with adequate gain and phase margins to ensure that the system remains stable with the minimum and the maximum number of specified modules.

For example, Assume we are designing a system with 4 inverter modules and we are required to tolerate up to 2 faulty inverter modules. Also, assume that the specified minimum gain margin for relative stability is 10 dB. To ensure stability at worst case, we need to design the voltage loop with at least 20 dB gain margin (assuming 4 modules). Even if 2 of these 4 modules fail, we will still have 10 dB gain margin and the system remains stable.

In the case of the inverter designed in chapter 3, the open loop phase of the voltage loop never reaches 180 degrees. The gain margin is infinity and, therefore, the system remains stable with any number of inverter modules. Off course, there are other physical and theoretical limitations on the maximum number of units.

Also, there are problems associated with having a high gain in the voltage loop. The higher the gain of the voltage loop, the higher is the crossover frequency of the voltage loop. For proper operation of the current mode controller, we require the voltage loop to have a lower crossover frequency than the current loop. This requirement puts an upper limit on the maximum gain of the voltage loop. moreover, a high gain in the voltage loop causes distortion in the output voltage. Therefore, if the stability if the voltage loop depends on the it's gain, there is a trade off between the percentage of the units which can fail in the system and the distortion in the output voltage.

2.2.2.3 Fault Protection

A parallel inverter system using the single voltage control method is prone to a complete system failure if one of the modules fails by having an output short circuit. As we discussed in section 2.1.2.4, we need to protect each module by adding both output current limiting circuits and fault protection circuits. The fault protection circuit of a faulty module detects a short circuit and isolates the output of that module from the rest of the system. The current limiting circuit is required to protect modules from failing due to the initial high current while the fault protection circuit is detecting a short circuit. The fault protection circuitry for the single voltage control method is similar to the one presented for the current imbalance method (refer to Figure 18).

2.2.2.4 System Redundancy and Single Point of Failure

As mentioned before, our secondary design objective in parallel inverter systems is to maximize the system redundancy by reducing the number of "single points of failure" in the system. As we can see from the block diagram of the parallel inverter system using the single voltage control method (Figure 20), the only single point of failure in this system is the voltage control block. The voltage control block operates at low voltages and currents; therefore, it has a relatively low probability of failure.

The only situation that we need to be concerned about is an inverter module failure which affects the current reference I_{ref}. For example, it is possible that one of the inverter modules fails in a way that I_{ref} is shorted to the ground. In this case, the reference current for all the modules becomes zero and the system output voltage drops to zero. Thus, a single module failure can cause a total system failure. We need to design the system to prevent this kind of failure. We can easily overcome this problem by isolating the I_{ref} that is fed to each module. As shown in Figure 24, we can use voltage buffers (made with Op-Amps) to isolate the reference current, I_{ref}, that goes to each inverter module. Even if one of the modules, say module one, shorts its reference current, I_{ref1}, to the ground, the other two reference currents, I_{ref2} and I_{ref3}, are not disturbed. Therefore, we have prevented a total system failure when one of the modules shorts the system reference current to the ground.

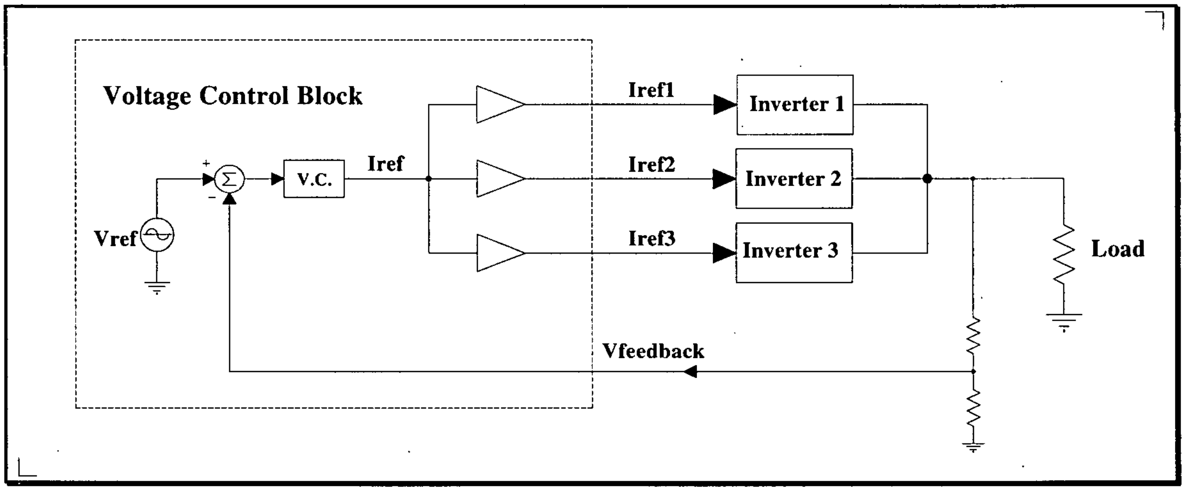

Figure 24. Fault Tolerant Voltage Control Block

Therefore, we can design a voltage control block which has a relatively low probability of failure. Hence, having a voltage control block as a single point of failure does not seriously reduce the degree of redundancy in the system.

2.3. Summary

In this chapter we presented two different methods for connecting PWM inverters in parallel – the current imbalance method and the single voltage control method.

In the current imbalance method, we have a current distribution block which generates current imbalance signals which are fed to all the inverter modules. The current imbalance for each module is calculated as the difference between the current which the module is generating and the current which the module should deliver to the load to achieve balanced load sharing. Inverter modules use these current imbalance feedback signals to set the exact current that each inverter module is supposed to deliver. Thus, all modules share the load current equally. Also, the system can be designed to tolerate module failures by adding fault protection circuitry to all inverter modules. The power distribution block is a single point of failure for the system; however, it can be designed to have a very low failure rate. Therefore, practically speaking, the degree of redundancy of the system is not greatly reduced by having the power distribution block as a single point of failure.

In the single voltage control method, the system has only one voltage control loop. The voltage control loop generates a current reference signal which is proportional to the current that the system should supply to the load in order to establish the desired output voltage. All inverter modules use this common current reference signal and generate module output currents which are equal. Therefore, all modules share the load current equally. We also determined that the relative stability of the system may change as each inverter module fails (i.e. as the number of active modules reduces). Therefore, the system may be stable as long as the number of active (operating) modules does not exceed the minimum and the maximum number of units calculated by the stability criteria. Also, to prevent a total system failure in case of a module failure, modules should incorporate fault protection circuitry such as output current limiting and fault switches. The voltage control loop is a single point of failure for this system. However, since the failure rate of the voltage loop is relatively low, the overall redundancy of the system is not greatly affected by having this single point of failure.

3. Design of a PWM Inverter

In this chapter, we discuss the design of a Voltage-Source Inverter (VSI) module and a Current-Source Inverter (CSI) module. We connect a number of VSI modules designed in this chapter in parallel and verify the operation of the proposed current imbalance method for paralleling inverter modules.

3.1. Design Objectives

Our objective in this section is to design a single-phase PWM inverter module with the following specifications:

- Nominal output voltage: 120 Vrms
- Maximum peak output current: 5 Amp
- Maximum output inductor ripple current: +/- 1.25 Amp (+/- 25%)
- Maximum output ripple voltage: +/- 0.5 V

In our design, we use the following criteria for relative stability of a feedback loop [16]:

- Minimum gain margin: 10 dB
- Minimum Phase margin: 50 degrees

3.2. Voltage Versus Current Mode Control

Two different control topologies are used for designing voltage source PWM inverters – voltage mode control and the current mode control [17]. In the voltage mode control, the inverter has a single control loop which controls the output voltage using a voltage feedback. In current mode control, the inverter has two control loops – an inner current loop which controls the output current and an outer voltage loop which controls the output voltage. Therefore, a current mode control voltage source inverter module requires a current feedback and a voltage feedback. Figure 25 shows a typical current mode control voltage source PWM inverter module.

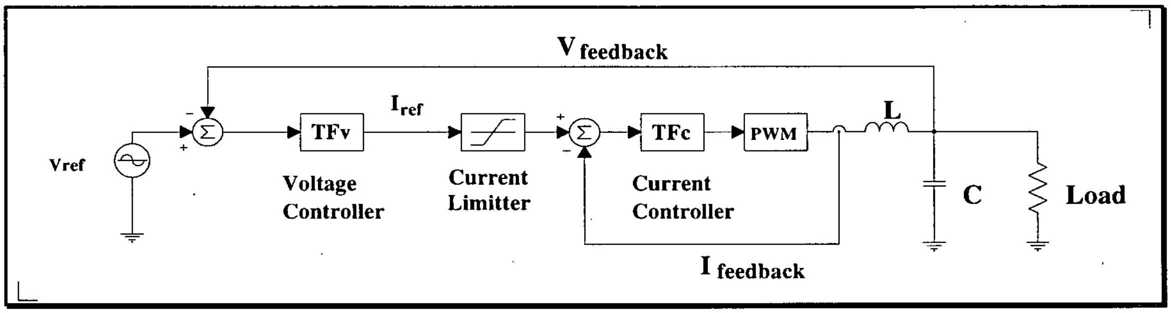

Figure 25. Current Mode Control Voltage Source Inverter

For our design, we decided to use the current mode control. This decision was based on the following reasons:

- We can easily and cost effectively add output current limiting capability to inverter modules which employ the current mode control. This can be achieved by limiting the reference current signal, I_{ref}, which drives the inner current loop (see Figure 25). As we saw in section 2.1.2.4, having output current limiting capability is a requirement for implementing fault protection circuitry.

- From the control design point of view, current mode control offers a number of advantages over the voltage mode control. First of all, the control loop design is easier for current mode control than the voltage mode control. Both the voltage controller and the current controller, TF_v and TF_c, can be first order circuits. However, voltage mode control requires a second order controller which is more difficult to design than a first order controller. Secondly, current mode control provides a better transient response than the voltage mode [17]. Generally speaking, this is due to the fact that the current loop is designed to have a high gain which responds to the output current changes quickly. However, to achieve stable operations, voltage loops are designed to have low gains which result in slower response to the changes in the output current.

While current mode control offers many advantages over the voltage mode control, it has the disadvantage that of being less immune to noise than the voltage mode control [17]. Also, for the stable operation of the peak current mode controller, the PWM duty cycle should be limited to less than 50% unless slope compensation is used [18]. The noise which is induced in the inductor current CT and in the current feedback path, due to the current spikes, can disturb the operation of the unit. However, the advantages of the current mode control far exceeds its disadvantages. Thus, we use current mode control to design PWM inverter modules. We can overcome the drawbacks of the peak current mode control method (limited duty cycle range and poor noise immunity) by using the average current mode control method. The average current mode control is discussed in section 3.5.

3.3. Switching Topology

Two different switching topologies can be used for designing PWM inverters – half-bridge and full-bridge [15]. The half-bridge PWM inverter requires a dual DC input voltage and two switching devices to convert the DC voltage to AC. The full-bridge PWM inverter requires only one DC input voltage but four switching devices to do the same conversion. We decided to use the half-bridge topology. It is easier to generate the two PWM signals to drive the half-bridge than to generate the four PWM signals for the full-bridge. Also, the half-bridge requires fewer switching devices and snubber circuits. Providing a dual DC voltage for the half-bridge circuit is not difficult in practice. Usually, we require a boost DC to DC converter to generate the input DC voltage for the inverter. We can use a center tapped isolation transformer in the DC to DC converter to generate the dual DC voltage for the half-bridge inverter. An implementation of this idea is illustrated in the following figure.

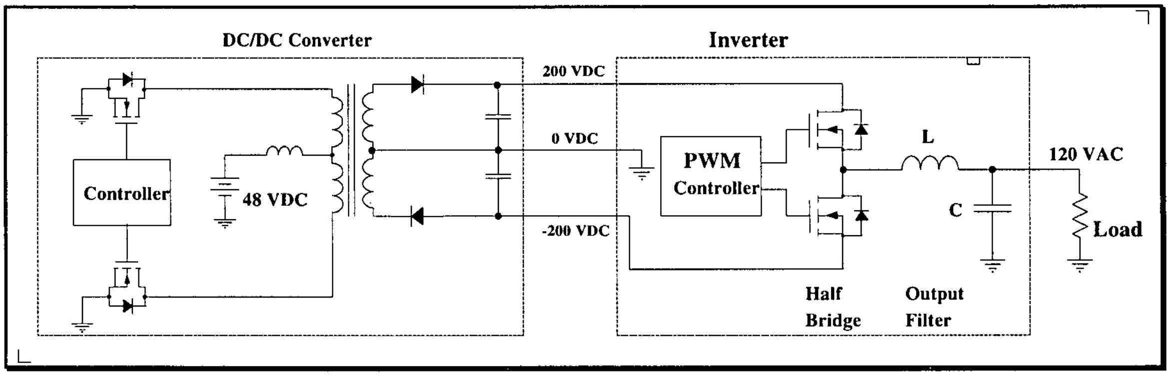

Figure 26. Power Flow Block Diagram

Figure 26 shows the power flow in a typical inverter module. The DC to DC converter operates from a 48 VDC voltage. This can be either provided by a battery bank (in Uninterrupted Power Supply) or from an off-line switcher. The DC to DC converter generates +/- 200 VDC from the 48 VDC. The transformer and the diode capacitor filter at the output of the converter operate at the switching frequency of the DC to DC converter. Since most converters operate at high frequencies (10-100 KHz), the transformer and the capacitors can be small and cost effective.

The reason for choosing +/- 200 VDC for the input voltage of the inverter is simple. We are designing an inverter module with 120 V RMS output voltage. The peak value of this voltage is about 170 V. The inverter input voltage should be slightly higher than this peak value. We choose +/- 200 VDC which is about 15% more than this peak value. This ensures no clipping even at maximum rated output current. Another factor which affects the choice of the input voltage is the PWM duty factor, *D*. As discussed in Appendix A, the PWM duty factor is the duty cycle of the PWM signal or the ratio of the "on" and "off" times for the switching transistors. For our design, the duty factor is given by:

$$D = \frac{V_{in} + V_{out}}{2 \times V_{in}} \tag{3-1}$$

Where:

$D =$ Duty Factor

$V_{in} =$ Input Voltage (200 V)

$V_{out} =$ Instantaneous Output Voltage (-170 V to +170 V)

As we can see, the PWM duty factor varies with the instantaneous value of the inverter output voltage. Thus, the minimum and maximum duty factors are calculated as:

$$D_{\min} = \frac{200-170}{2\times 200} = 0.075 \tag{3-2}$$

$$D_{\max} = \frac{200+170}{2\times 200} = 0.925 \tag{3-3}$$

When designing the control circuits of the inverter, we need to ensure that the system remains stable for the full range of duty cycle values.

3.4. Output Filter

Now, let us calculate the inductance, L, and the capacitance, C, of the output filter (refer to Figure 26). The value of the inductor, L, depends on the maximum allowable ripple current in the output inductor. The inductor ripple current is due to the PWM switching. We can use the following estimation to calculate the inductor value:

$$L = \frac{v\times dt}{di} \cong \frac{\Delta V\times \Delta T}{\Delta I} = \frac{2\times V_{DC}\times D\times T}{\Delta I} = \frac{2\times V_{DC}\times D_{\max}}{\Delta I_{\max}\times f_s} \tag{3-4}$$

Where:

L: Output inductor

V_{DC}: Inverter input voltage

f_s : Switching frequency

D_{max}: Maximum PWM duty cycle

ΔI_{max} : Maximum allowable inductor ripple current

Therefore, assuming a maximum of +/- 25% ripple current at the inverters rated current (5 Amp), we can calculate the output inductance.

$$L = \frac{2 \times 200V \times 0.925}{2.5Amp \times 20KHz} = 7.4mH \tag{3-3}$$

Based on this estimation, we decided to use an 8 mH inductor.

The choice of the output capacitor, C, determines the amount of ripple in the output voltage. Basically, the output capacitor absorbs most of the ripple in the inductor current. The output voltage ripple can be estimated as follows:

$$\Delta V_{out} = \Delta V_C \cong \frac{\Delta I_C}{C \times f_S} + r_{ESR} \times \Delta I_C \cong \frac{\Delta I_L}{C \times f_S} + r_{ESR} \times \Delta I_L \tag{3-4}$$

Where:

ΔV_{out}: Output voltage ripple

ΔI_L: Inductor current ripple

r_{ESR}: Equivalent Series Resistance (ESR) of the output capacitor

Therefore, assuming a 26 μF capacitor with 0.1 Ohm ESR, the ripple in the output voltage is about 0.73 volts which is less than the specified maximum output voltage ripple of 1.0 volts.

$$\Delta V_{out} \cong \frac{2.5Amp}{26\mu F \times 20KHz} + 0.1\Omega \times 2.5Amp = .73V \tag{3-5}$$

Therefore, we will use the following values for the inverter output filter:

L: *0.8 mH*

C: *26 μF*

3.5. Current Loop Design

In this section, we design the current loop for a PWM inverter module. As we mentioned previously, two different control methods are cab be used for current control – peak current mode control and average current mode control. Figure 27 shows a typical current control loop which can be either a peak current controller or an average current controller depending on the current controller transfer function, TF_C. If TF_C is a simple gain constant, we have a peak current controller. However, if TF_C has an some filtering capability, then the average inductor current is proportional to the reference current, i.e. an average current controller [14]. The peak to average current error is particularly important in our design.

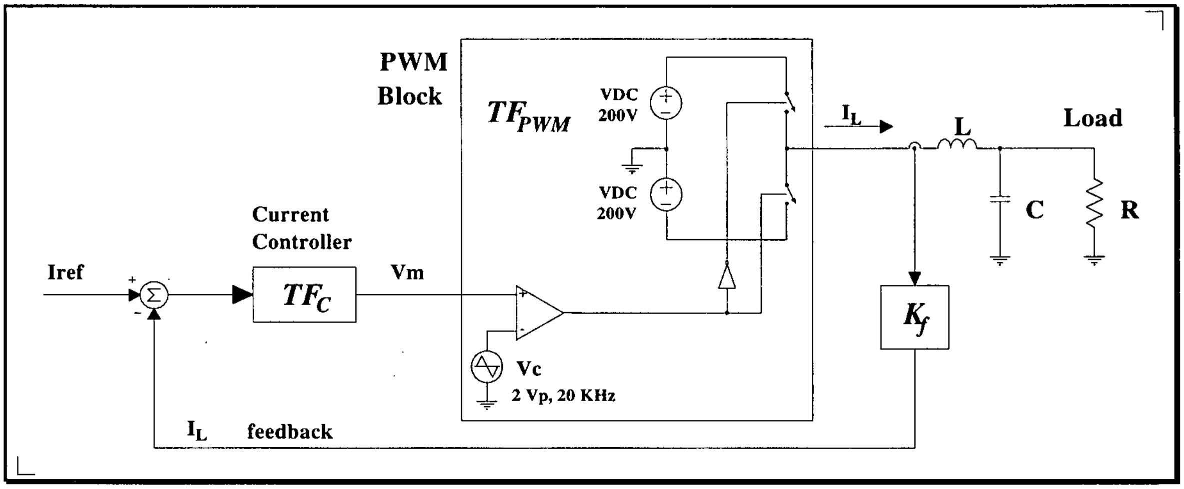

Figure 27. Peak or Average Current Mode Controller

The current averaging introduced by controller TF_c has a number of advantages. The noise immunity improves due to the averaging characteristic of the integrator. Also, no slope compensation is required which simplifies the design [14]. Furthermore, as discussed in section 2.2.2.2, the proposed current imbalance method works best with inverter modules which employ the average current mode control. Another advantage of the average current mode control over the peak. The transfer function of the controller TF_c can be tailored for optimum performance. The high frequency gain of the TF_c can be determined using the slope constraint to ensure stable operation. The low frequency gain of the TF_c can be increased to improve the step load response time [14].

For the current loop shown in Figure 27, we have so far calculated the following values:

L:	0.8 mH
C:	26 μF
V_{DC}:	+/- 200 V

We assume the following values for the PWM oscillator, the inductor current sensing circuitry:

V_c: 2 V_p (-2 V to +2 V), 20 KHz, 50% duty cycle

K_f: 1 Volt / Amp

We also need to design the inverter module to be stable with various loads. To simplify the design, we assume the load to be resistive with minimum and maximum values. Later on, we verify that the inverter module is also stable with other types of loads (rectified capacitive and inductive loads). The minimum value of the load resistance is calculated using the maximum output current rating of the inverter module. Since the maximum peak inverter current is rated at 5 A_{peak}, the minimum load resistance is 35 Ω. The maximum value of the load resistance is assumed to be the same value as the typical no load output impedance of an inverter module (about 5 KΩ). Therefore, we design the inverter module to be stable with the following load values:

R: 35 Ω to 5 KΩ

Given the above discussions, we are now ready to design the average current mode controller. In the following two subsections, we use the slope constraint and relative stability criteria based on the phase and gain margins to design a stable current loop.

3.5.1. Slope Constraint

As we can see from Figure 27, the PWM duty cycle is generated by comparing the PWM modulation voltage, V_m, with the switching oscillator triangular voltage, V_C. Typical waveforms of V_m, V_C, and the resulting PWM duty cycle are shown in Figure 28. Obviously, to generate a PWM signal, V_m and V_C waveforms must intersect with one another. One constraint to ensure that V_m and V_C intersect is to ensure that the rising slope of the V_m is less than the rising slope of the V_C. This geometric limitation of the modulation voltage, V_m, is referred to as the slope constraint. Every stable PWM loop satisfies the slope constraint.

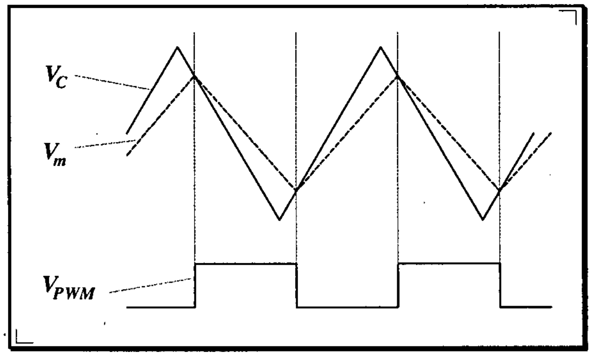

Figure 28. Slope Constraint and Generation the PWM duty cycle

Applying the slope constraint to circuit of Figure 8 gives us the following:

$$Slope\ of\ V_m < Slope\ of\ V_C \tag{3-6}$$

$$K_f.K_C.\frac{\Delta i_L}{\Delta t} = K_f.K_C.\frac{\Delta v_L}{L} = K_f.K_C.\frac{2\times V_{DC}}{L} < \frac{V_C}{T/4} \tag{3-7}$$

$$K_C < \frac{1}{K_f}.\frac{2\times L\times V_C}{T\times V_{DC}} \tag{3-8}$$

Where:

K_C: Gain of the TF_c at switching frequency

K_f: Gain of the inductor current CT (Volt / Amp)

T: Period of the switching frequency

V_C: Peak amplitude of the PWM triangular oscillator

Calculating this for our design:

$$K_C < \frac{1}{1Volt / Amp} \cdot \frac{2 \times 0.8mH \times 2Volt}{50us \times 200Volt} = 0.32 = -9dB \qquad \textbf{(3-9)}$$

Therefore, the gain of the current controller transfer function, TF_c, at the 20 KHz switching frequency must be less than –9 dB .

3.5.2. Gain and Phase Margins

Our next task is to determine the transfer function, TF_c, for the current controller in Figure 27. TF_c must satisfy the required gain and phase margins (relative stability criteria) [16]. Also, based on the pervious discussions, TF_c should be chosen such that the average (not peak) inductor current is proportional to the reference current. The gain of the TF_c at 20 KHz must be less than –9 dB to satisfy the slope constraint. Also, the gain of the TF_c at low frequencies (10 Hz to 1KHz) must be higher than its high frequency gain so the system would have a good step load response.

All the above requirements, makes determining the TF_c transfer function more a trial and error task than a step by step procedure. The following transfer function, which was found using trial and error technique, satisfies our requirements:

$$TF_C = 2 \times \frac{2 \times 10^{-4}.S + 1}{2.6 \times 10^{-8}.S^2 + 1.6 \times 10^{-3}.S + 1} \qquad \textbf{(3-10)}$$

This transfer function can be expressed in the following format:

$$TF_C = K_C \times \frac{(1 + T_2.S)}{(1 + T_1.S).(1 + T_3.S)} \qquad \textbf{(3-11)}$$

Where:

$K_c = 2$ (gain constant)

$T_1 = 1.6\times10^{-3}$ seconds (pole at 100 Hz)

$T_2 = 1.6\times10^{-4}$ seconds (zero at 1 KHz)

$T_3 = 1.6\times10^{-5}$ seconds (pole at 10 KHz)

The current loop controller has one zero and two poles. The Bode plot of this transfer function is shown in Figure 29. As we can see, the gain of the current controller at 20 KHz is –20 dB which satisfies the slope constraint.

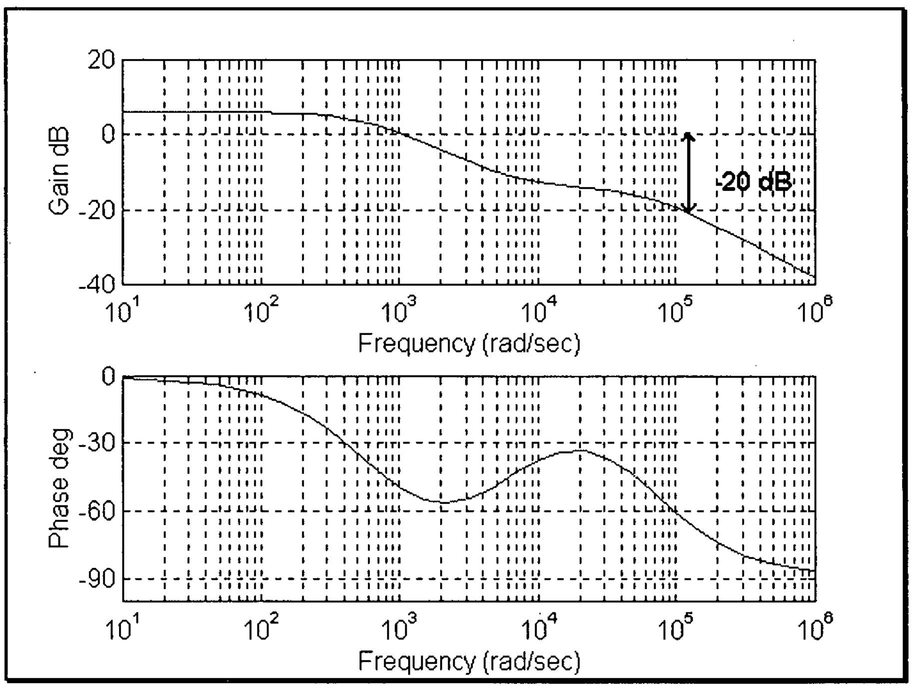

Figure 29. Bode Plot of the Current Controller

From the feedback control theory, we know that a close-loop system is relatively stable if the open-loop transfer function meets the gain and phase margin criteria [16]. In our design, we are assuming relative stability at 10 dB gain margin and 50 degree phase margin. From Figure 27, the loop transfer function of the current loop is calculated as follows:

$$TF_{C-open-loop} = TF_C.TF_{PWM}.K_f \qquad \textbf{(3-12)}$$

The transfer function of the PWM block, TF_{PWM}, is calculated in Appendix A using the small signal model:

$$TF_{PWM} = \frac{i_L}{V_m} = \frac{2 \times V_{DC}}{V_C} \cdot \frac{RCS+1}{RCS^2+LS+R} \qquad \textbf{(3-13)}$$

Now, we can calculate the open-loop transfer function of the current loop:

$$TF_{C-open-loop} = \frac{2 \times V_{DC} \times K_C \times K_f}{V_C} \cdot \frac{(RCS+1).(1+T_2.S)}{(RCS^2+LS+R).(1+T_1.S).(1+T_3.S)} \qquad \textbf{(3-14)}$$

The bode plots of the open-loop transfer function for R equal 35 Ω and 5 KΩ is plotted in Figure 30. Gain margin, G_m, and the phase margin, P_M, can be easily read from these bode plots. As we can see, these values meet our stability criteria. At worst, we have a 47 degree phase margin when system has no load (5 KΩ). Although, this slightly falls outside of the specified relative stability region; the system is fairly stable even at no loads.

$G_m = 48\ dB \quad P_m = 52\ degrees$ at R = 35 Ω

$G_m = 52\ dB \quad P_m = 47\ degrees$ at R = 5 KΩ

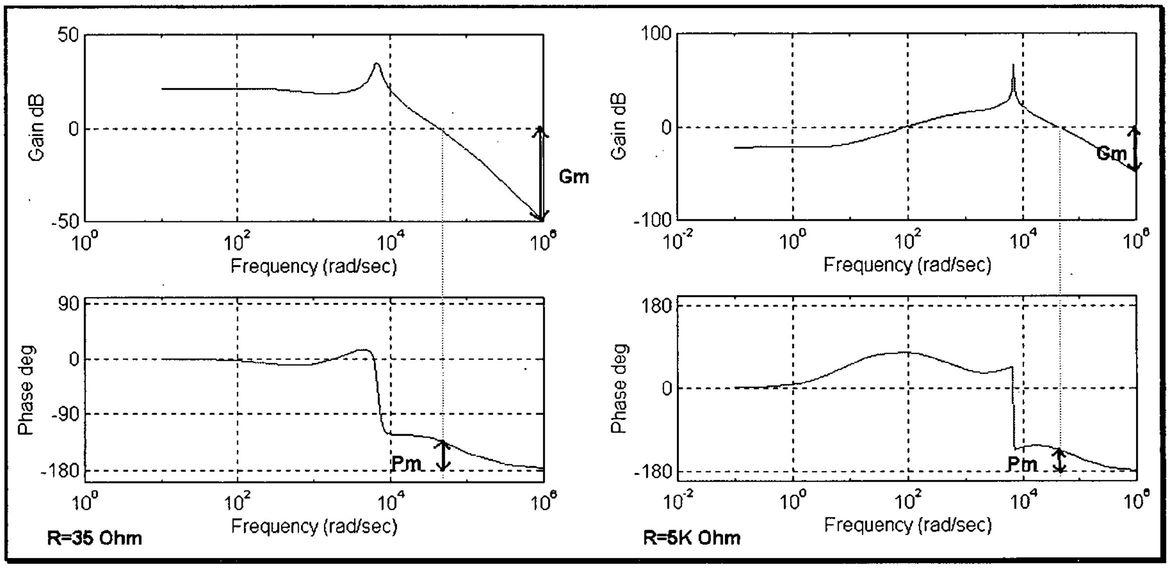

Figure 30. Bode Plots, Open-loop Transfer Function of the Current Loop

3.6. Voltage Loop Design

In this section, we design the voltage loop for a PWM inverter module. As far as the voltage loop is concerned, the closed-loop current-loop can be approximated by a unity transfer function (zero dB gain and zero degree phase shift). Therefore, we can model the voltage loop as shown in Figure 31. Again, to analyze the stability of this loop, we need to consider the gain and phase margins of the open-loop transfer function. The open-loop transfer function of the voltage loop is given next:

$$TF_{V-open-loop} \doteq K_V.TF_V.TF_{CL}.TF_{RC} \tag{3-15}$$

Where:

$TF_{V\text{-}open\text{-}loop}$	Open-loop transfer function of the voltage loop
K_V	Gain constant of the voltage feedback (0.01 is this design)
TF_V	Transfer function of the voltage controller

TF_{CL} Closed-loop transfer function of the current loop (unity)

TF_{RC} Transfer function of the output RC

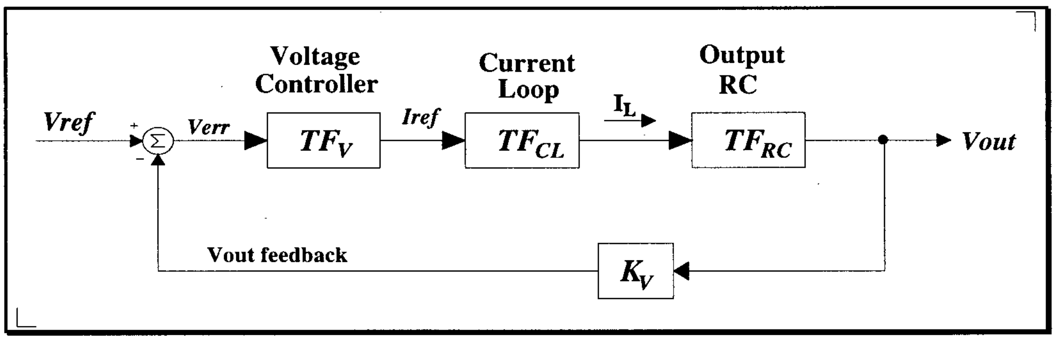

Figure 31. Model of the Voltage Loop

Substituting the values for TF_{CL} and TF_{RC}, we can derive the following open-loop transfer function:

$$TF_{RC} = \frac{V_{out}}{i_L} = \frac{R}{R.C.S+1} \tag{3-16}$$

$$TF_{V-open-loop} = TF_V \times \frac{K_V.R}{R.C.S+1} \tag{3-17}$$

The following PI controller stabilizes the loop and gives a good response:

$$TF_V = 20 \times \frac{2\times10^{-3}.S+1}{2\times10^{-3}.S} \tag{3-18}$$

The open-loop bode plots of the compensated voltage loop is shown in Figure 32. As we can see, the voltage loop is stable for both 35 Ω and 5 KΩ load values. When the gain reaches zero dB, the phase angle is about –90 degrees. Thus, we have about 90 degrees of phase margin. Also, the phase never reaches the –180 degree; therefore, the gain margin of the loop is very high (infinity). Therefore, the voltage loop meets our relative stability criteria.

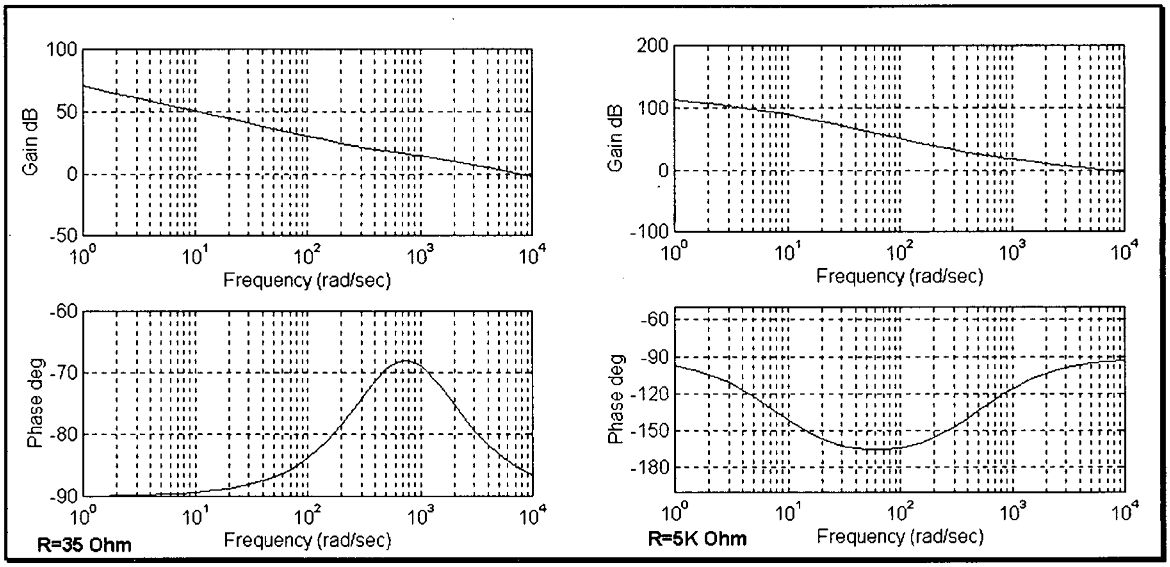

Figure 32. Bode Plots, Open-loop Transfer Function of the Voltage Loop

3.7. Design Verification

The design was verified using computer simulations. The simulation results are summarized in Figure 33. The circuit was tested under three different loads. A 5 KΩ resistive load which represents the no load condition. As we can see, the circuit is stable at no load. The next simulation was with a 35 Ω resistive load. This simulation verified that the design is capable of providing the maximum rated current (5 Amp peak). The last simulation was with a rectified capacitive load. Most modern electronic equipment can be modeled with a rectified capacitive load. As we can see, the inverter output voltage suffers from some distortion when the load suddenly starts to draw a high current. This distortion is acceptable in most commercial and industrial applications. The most important part is that the circuit remains stable. We can also see the step load response of the circuit from the rectified capacitive simulation. The circuit is capable of quickly reacting to the load change.

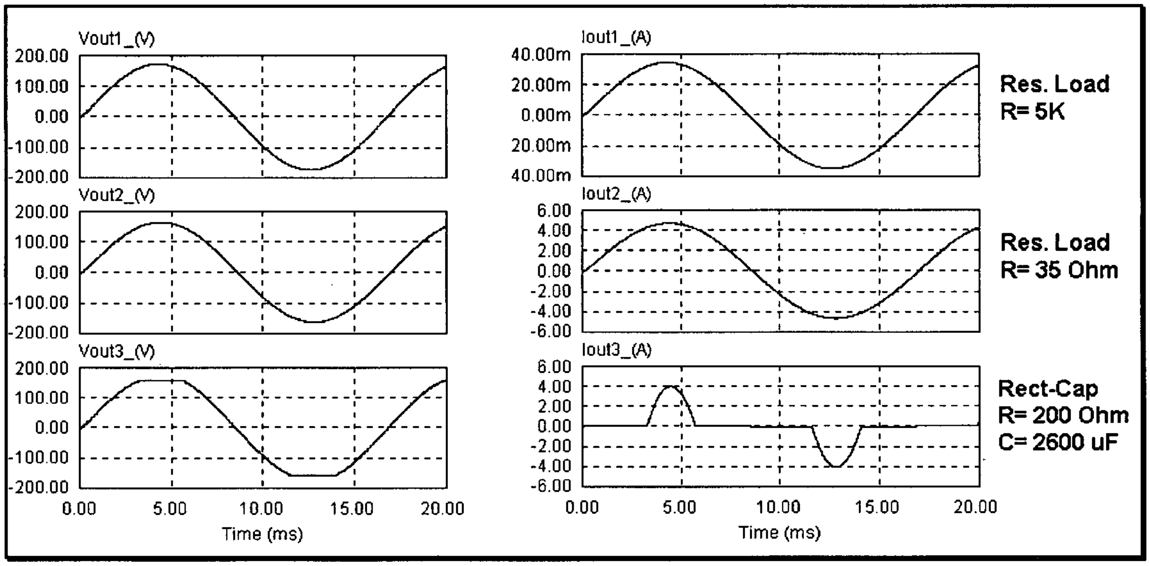

Figure 33. Simulation Results for a Single Inverter Module

3.8. Summary

In this chapter we designed a single PWM inverter module. We employed an average current mode topology for the inverter module. We designed both current and voltage loops of the system to meet our relative stability criteria. At the end the design was verified using computer simulations. In the following chapter, we use the prototype inverter modules, built based on the design in this chapter, to verify the operation of parallel inverter systems using our proposed control methods.

4. Test Results

In this chapter, we will present the simulation and experimental test results for the two proposed methods which we discussed in chapter 2. First, we discuss how to modify the simulation circuits to take into account the imperfections in a practical system.

4.1. Using Simulations to Verify Parallel Operation

We use computer simulations extensively to design and test our proposed methods for paralleling inverter modules. We would like the simulation results to be as close to the experimental results as possible. One of the major factors which causes the experimental results to be different from the simulation results is the component tolerances. The value of the components used in real circuits vary from one inverter module to the other. This causes the inverter modules to have different gains, time constants, poles, and zeros. Thus, each inverter module operates differently when compared to the other inverter modules in the system. These module variations are the main source of the imbalance in the system.

Block diagrams of the proposed current imbalance system and the single voltage control system are shown in Figures 15 and 20 respectively. We simulate these two circuits to verify the operation of our proposed methods. In order to create module variations, we can change the gains, time constants, zero locations, pole locations, inductor values, and capacitor values in all the inverter modules. However, our simulation studies show that changing most inverter parameters do not cause an imbalance condition in the system. The only two parameters which cause a significant imbalance in the system are the amplitude and phase of the voltage reference and the gain of the voltage loop controller.

To see the effects of component tolerances, we simulated the system shown in Figure 15 without the imbalance controllers (we shorted the input of the current imbalance controllers to the ground). Then, setting the amplitude and the phase of the first voltage reference, V_{ref1}, different from the other voltage references caused a major current imbalance and also resulted in circulating current. In practice, all the voltage references have the same phase because they are connected to the same synchronization signal; however, they can have different amplitudes. Also, setting the gain of the first voltage loop controller, TF_{V1}, different from the gain of the other voltage loop controllers caused a similar disturbance in the system. Therefore, to introduce some imbalance in the current imbalance system of Figure 15, we can either set the amplitudes of the reference voltages differently or set the gain of the voltage loop controllers differently. In our simulations, we set the amplitudes of the voltage references differently to create an imbalance condition in the system.

For the single voltage control system, shown in Figure 20, we can not create an imbalance condition by changing any of the system parameters. Changing the parameter values of the voltage loop can not cause an imbalance condition because all modules use the same voltage loop. Also, changing the parameter values of the current loop and the PWM converter does not cause any imbalance in the system. Therefore, the single voltage control method is simulated without any intentional module variations.

4.2. First Proposal: Current Imbalance Method

This section presents both the simulation and experimental test results for the current imbalance method. First, we present the simulation results obtained from the PSIM software. In these simulations, we investigate the operation of the current imbalance method under various load and system configurations. Next, we present the experimental test results obtained from a prototype system of two PWM inverters connected in parallel using the current imbalance method. These test results verify the operation of the prototype system under different load conditions.

4.2.1. Simulation Results

We used the PSIM software to verify the operation of the current imbalance method for connecting PWM inverters in parallel.

Figure 34 shows one of the several PSIM simulation circuits which we use to obtain the results given in this section. This circuit simulates two PWM inverters connected in parallel using the current imbalance method. The detailed design of each inverter module is discussed in chapter 3. Each inverter module has its own voltage reference, V_{ref1} and V_{ref2}. The two voltage references are synchronized (have the same phase); however, they have different RMS values. We intentionally set the RMS values different to create some imbalance in the system. In real systems, the component tolerances cause imbalance in the system (see section 4.1). The current imbalance method should compensate for this difference by preventing any low frequency circulating current. Also, the inverter modules should contribute almost equal currents to the load.

The output of the two inverter modules in Figure 34 are connected together using two series inductors L_4 and L_5. The series inductors eliminate the high frequency circulation currents (refer to section 1.2.1.1). The power distribution block consists of the voltage divider Div_1 and two summing junctions S_1 and S_2. The voltage divider divides the system output current I_{out} by 2 to generate the expected module current. The two summing junctions calculate the difference between the expected module current and the actual module currents I_{out1} and I_{out2} to generate the imbalance current feedbacks I_{imb1} and I_{imb2}. The imbalance current feedbacks are passed through two PI controllers before being fed to the inverter modules.

The parallel inverter system, shown in Figure 34, is connected to a rectified capacitive load which models the current drawn by typical switching power supplies used in modern computer equipment. We will show the simulation results for the rectified capacitive load as well as resistive (linear) loads.

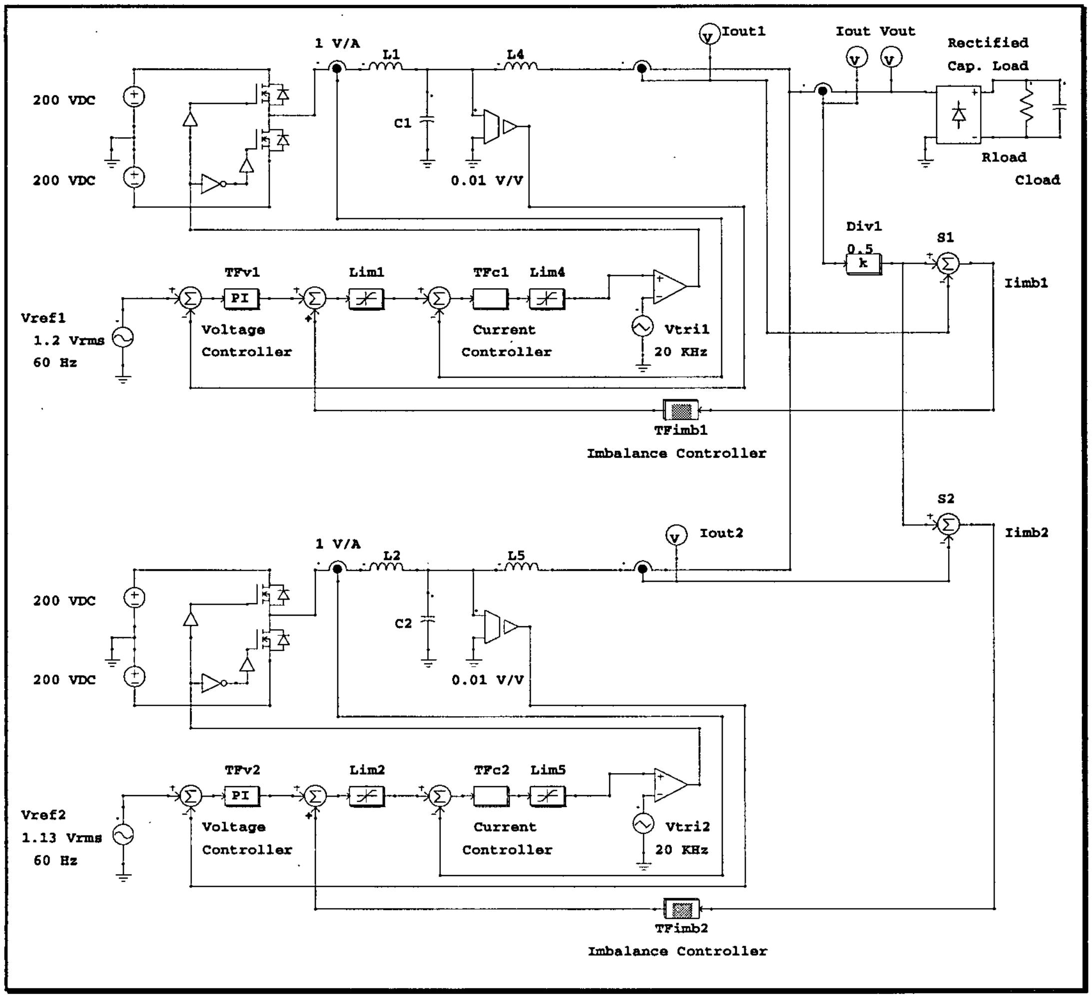

Figure 34. PSIM Simulation Circuit for the Current Imbalance Method

The component values for the current imbalance method simulation circuit are given below (except the ones which are specified in the diagram):

Switching inductors, L_1 and L_2	= 0.8 mH
Output capacitors, C_1 and C_2	= 26 uF
Series inductors, L_4 and L_5	= 2.5 mH
PWM oscillators, V_{tri1} and V_{tri2}	= -2V to +2V triangular @ 20 KHz
PWM limiters, Lim_4 and Lim_5	= -2V to +2V
Output current limiters, Lim_1 and Lim_2	= -5V to +5V (limits module current to 5 A)

Voltage controllers, TF_{v1} and TF_{v2} $= 20\times\dfrac{2\times10^{-3}\cdot S+1}{2\times10^{-3}\cdot S}$ (PI controller)

Current controllers, TF_{c1} and TF_{c2} $= 2\times\dfrac{1.6\times10^{-4}\cdot S+1}{2.6\times10^{-8}\cdot S^2+1.6\times10^{-3}\times S+1}$

Imbalance controllers, TF_{imb1} and TF_{imb2}= $1.5\times\dfrac{8\times10^{-5}\cdot S+1}{8\times10^{-5}\cdot S}$ (PI controller)

Figure 35 shows the simulation waveforms for a resistive load (50 Ω). The two module currents, I_{out1} and I_{out2}, are equal which shows the current imbalance method is working correctly (it has compensated for the imbalance condition which we introduced by different V_{ref1} and V_{ref2} RMS values). Therefore, inverter modules are not sinking and sourcing currents into one another (no circulating currents).

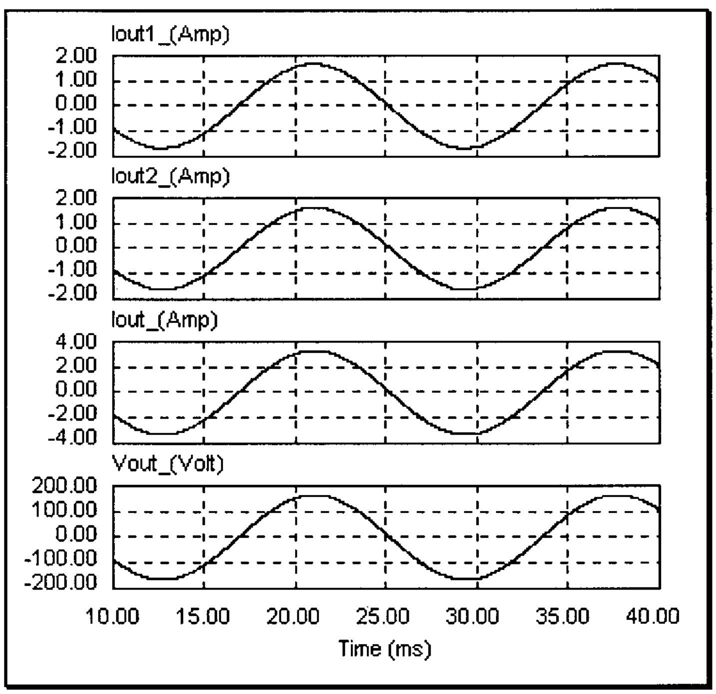

Figure 35. Current Imbalance Simulation Results with Resistive Load

To further prove the operation of the current imbalance method, Figure 36 shows the simulation results obtained from the same parallel inverter system without using the current imbalance method. To obtain this result, we set the two imbalance signals, I_{imb1} and I_{imb2}, of the system in Figure 34 to zero by shorting the inputs of the two imbalance controllers, TF_{imb1} and TF_{imb2}, to the ground. As we can see, the output currents of the modules, I_{out1} and I_{out2}, are no longer equal. The 3 currents are not in-phase. In fact, module 1 is sourcing current to module 2 and we have a low frequency circulating current. Therefore, our proposed current imbalance system has correctly operated and eliminated the imbalance in the system.

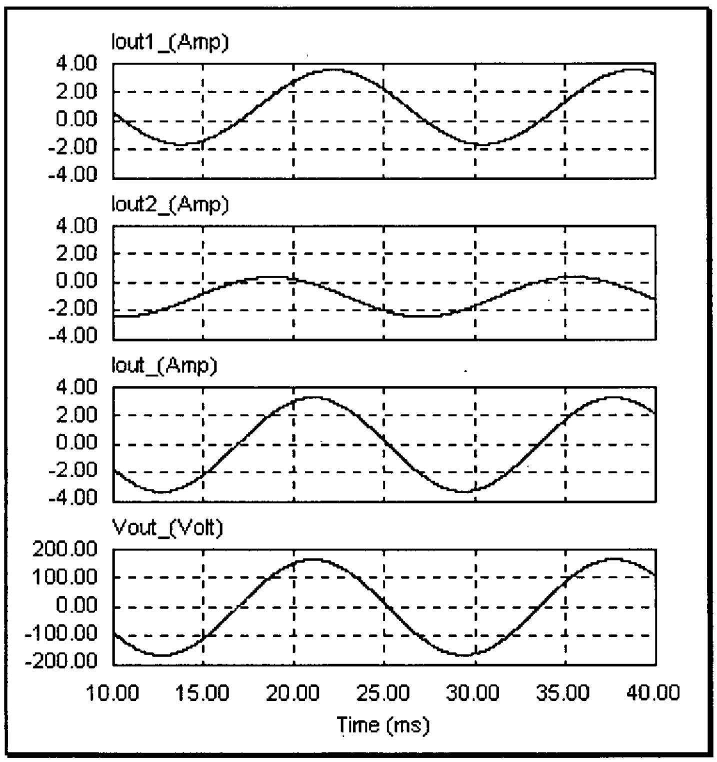

Figure 36. Simulation Results for a System without Imbalance Controller

The next figure, Figure 37, shows the simulation results obtained from circuit of Figure 34 with rectified capacitive load ($R_{load} = 200\ \Omega$ and $C_{load} = 1200\ uF$) . Again, the two modules are sharing the load current equally. This simulation verifies the stability of the system with nonlinear loads. It also shows the response of the system to a step load. As we can see, the output currents of the modules, I_{out1} and I_{out2}, are almost zero during most of the cycle. However, near the positive and negative peaks of the output voltage, the rectified capacitive load starts to draw a significant amount of current. Thus, we can see the response of the system to a step load near the positive and negative peaks of the output voltage. The output voltage, V_{out}, for a rectified capacitive load is sinusoidal with some clipping near the peaks. This output voltage is acceptable for driving most practical loads.

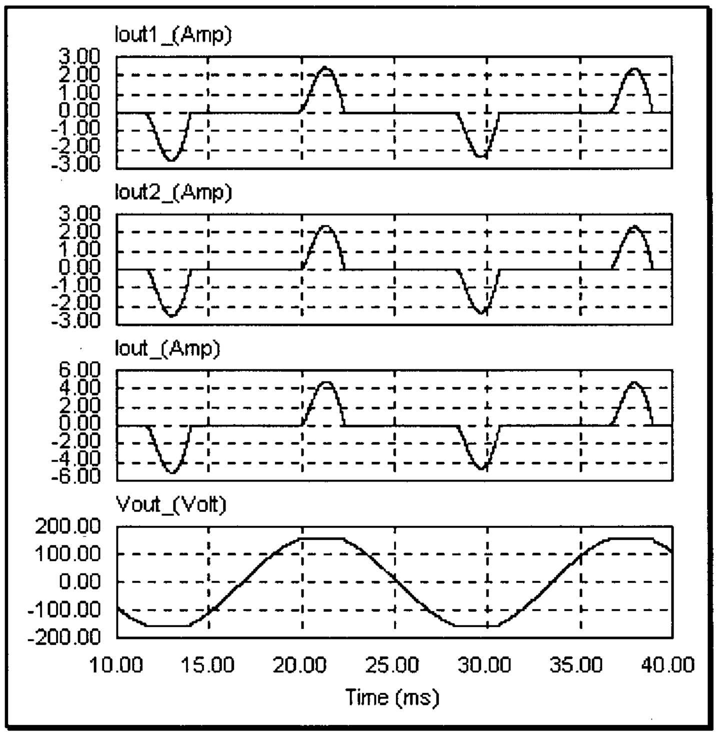

Figure 37. Current Imbalance Simulation Results, Rectified Capacitive Load

The next figure, Figure 38, shows the simulation results obtained from a system of three parallel inverter modules using the current imbalance method. As we can see, the current imbalance method works for three or more parallel modules.

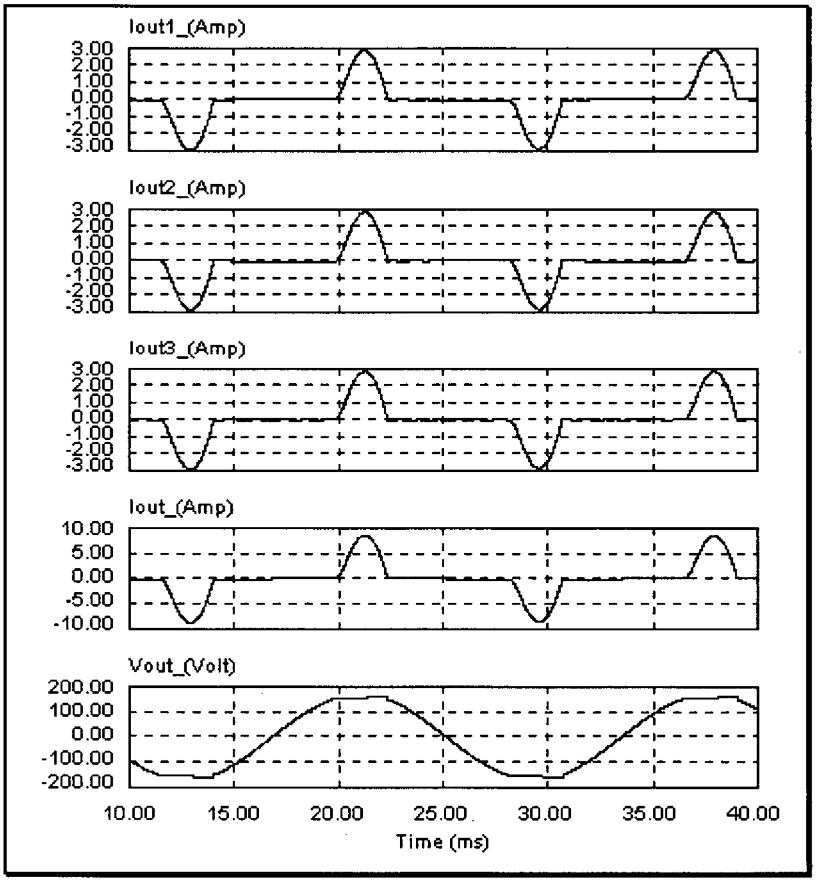

Figure 38. Current Imbalance Simulation Results with 3 Parallel Inverters

The next figure, Figure 39, shows the simulation results obtained from the circuit of Figure 34 while driving a small resistive load (*1000 Ω*). The simulation results show that the module output currents, I_{out1} and I_{out2}, are no longer equal (they have different amplitudes, different phases, and different DC values). Also, since I_{out1} and I_{out2} have different DC values, the system is suffering from circulating currents. Thus, the current imbalance method can be used as long as the load does become smaller than a given value. The system becomes unstable at no loads. We discussed the limitations of the current imbalance method in section 4.2.3.1.

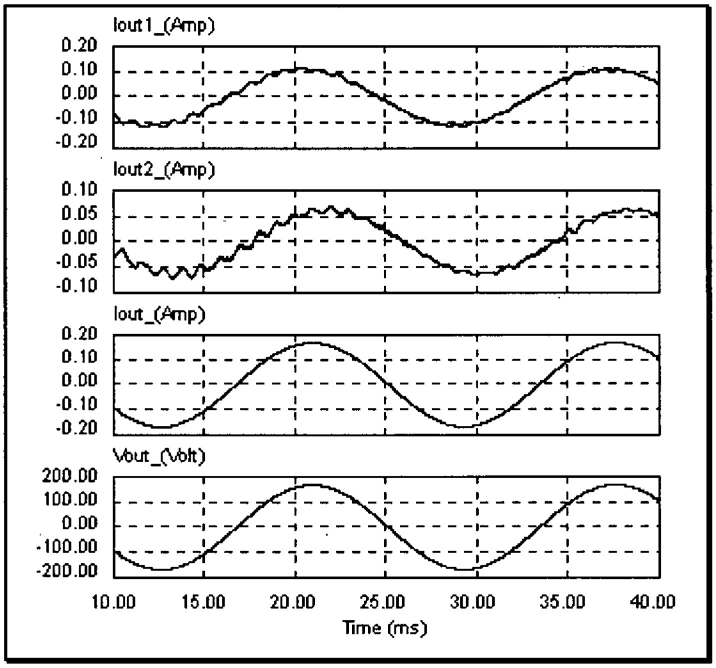

Figure 39. Current Imbalance Simulation Results with Small Load

4.2.2. Experimental Results

In this section, we present the experimental results obtained from a system of two PWM inverter modules connected in parallel using the current imbalance method. The complete schematic of the test circuit is given in Appendix II. Figure 40 shows a photograph of the prototype system used to obtain the results shown in this section.

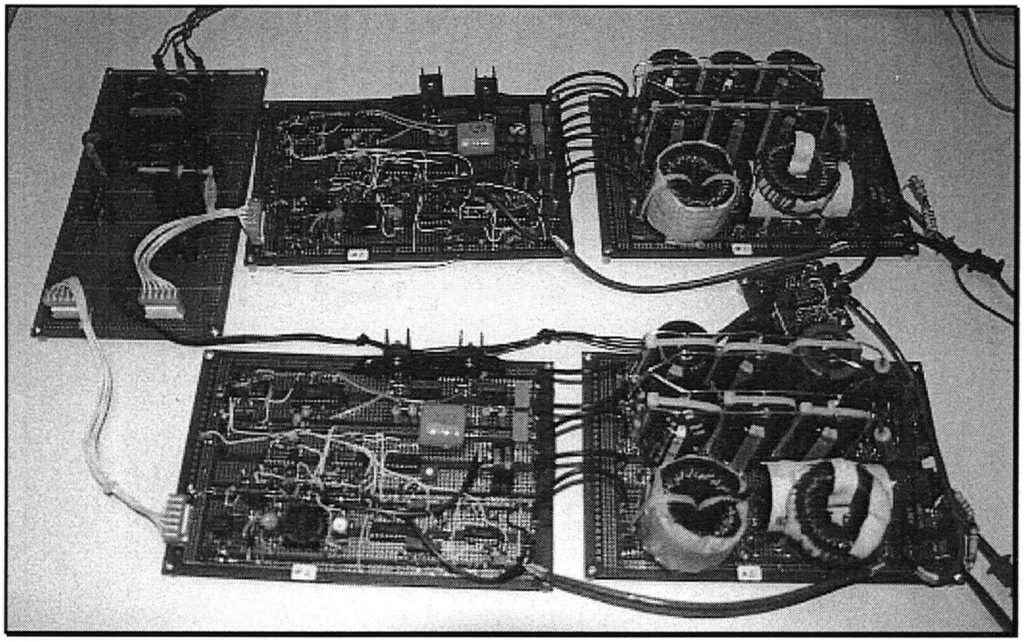

Figure 40. The Prototype for Testing the Current Imbalance Method

The system was tested under different load conditions. Figure 41 shows the measurements obtained from connecting the system to a 180 Ω resistive load. As we can see, the output voltage is sinusoidal and the load is being driven correctly. However, the currents delivered to the load by the two modules, I_{out1} and I_{out2}, are not exactly equal. Thus, the current imbalance method is not completely eliminating the imbalance in the system. Similarly, Figure 42 shows the measurements for the same circuit connected to a rectified capacitive load. We see that the two units share the load, but not exactly equally.

As we can see, the experimental results do not match the simulation results. Our simulations indicated that all modules contribute equal currents to the load. However, prototype experimentation shows a difference in the currents contributed to the load by the inverter modules. In section 4.2.3.2, we discuss this discrepancy between the simulation and experimental results and explain why the current imbalance method has poor load sharing capability.

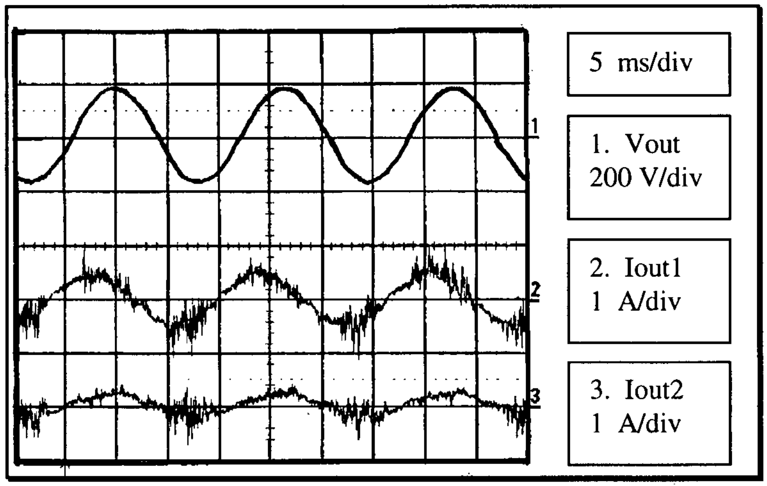

Figure 41. Experimental Results for Resistive Load

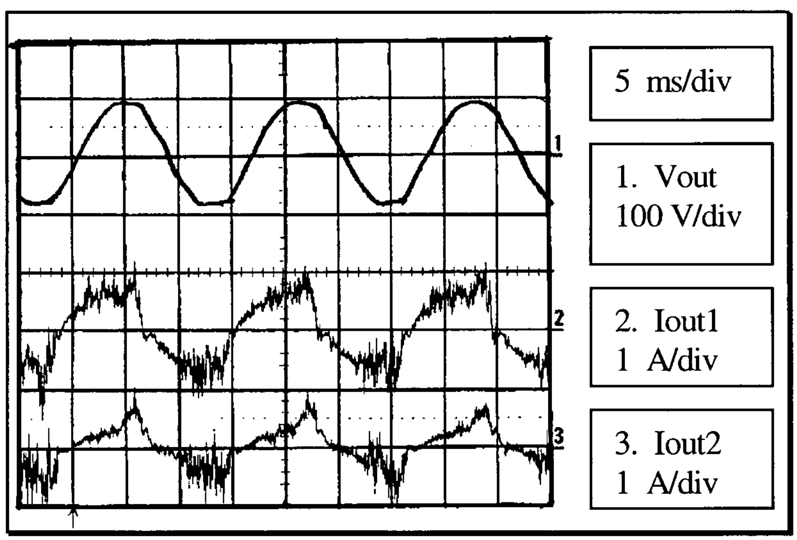

Figure 42. Experimental Results for Rectified Capacitive Load

The next figure, Figure 43, shows the measurement obtained from the current imbalance prototype driving a small resistive load (1500 Ω). As we can see, the two module currents are not equal and there is also some circulating currents. The circulating currents can be seen by noticing that during the positive sections of one output current, say I_{out1}, the second output current, I_{out2}, is negative. This means that one module is sinking a portion of the current generated by the other module. Having circulation current at low load condition, is a limitation of the current imbalance method. We also saw this limitation in the simulation results.

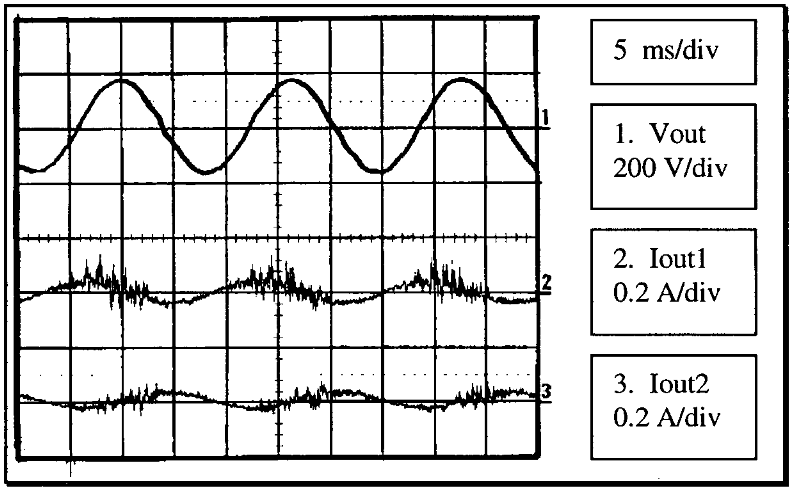

Figure 43. Experimental Results for a Small Load

4.2.3. Problems with the Current Imbalance Method

Our simulations and prototype testing of the current imbalance method show that there are two problems with the current imbalance method. First, a current imbalance control method does not perform well at low loads and the system becomes unstable at no load. Secondly, the experimental results indicate that the system does not share the load current equally among all the inverter modules. These two problems are discussed next.

4.2.3.1 Poor Performance at Low Loads

As we can see from both simulation and prototype testing, the current imbalance method does not perform well at low loads and the system becomes unstable at no load. This problem is caused by the current imbalance controllers (TF_{imb1} and TF_{imb2} in Figure 34). The current imbalance controller is a PI controller with a proportional and an integral term. We design the PI controller to operate correctly for typical load values – i.e. the ratio of the proportional term to the integral term has been optimized for nominal load current. For a low load, however, the loop becomes less stable.

4.2.3.2 Poor Load Sharing Among Inverter Modules

Our simulations indicated that all modules should contribute equal currents to the load current at typical load values. However, prototype experimentation shows a big difference in the currents delivered to the load by the different inverter modules. There are two possible explanations for this discrepancy. The first explanation is that this difference is caused by the noise in the system. The current imbalance signal is the difference between the expected module current and the actual module current. Since the expected and actual module currents are close to one another, the current imbalance signals have a relatively low amplitudes. Also, the current imbalance signals are generated by the power distribution block and are carried over a relatively long distance to the inverter modules. Therefore, the current imbalance signals are affected more than the other locally generated signals by the noise. The second reason is related to the way the current imbalance signals are calculated. The current imbalance signals change the reference current of the system current loops. Therefore, a small error in calculating the imbalance currents causes the modules output currents to be different. We use Op-Amps to calculate the imbalance currents. The non-ideal characteristics of the Op-Amps, specially the voltage offset error, results in error in the calculated imbalance currents which disturbs the balanced load sharing in the system.

4.3. Second Proposal: Single Voltage Control Method

This section presents both the simulation and experimental test results for the proposed single voltage control method. First, we present the simulation results obtained from the PSIM software. These simulations verify the operation of the single voltage control method under various load and system configurations. Next, we present the experimental test results obtained from a prototype system of two PWM inverter modules connected in parallel using the single voltage control method. These test results verify the operation of the prototype system under various load conditions.

4.3.1. Simulation Results

We used the PSIM software to verify the operation of the single voltage control method for paralleling PWM inverters.

Figure 44 shows one of the several PSIM simulation circuits which we used to obtain the results given in this section. This circuit simulates two parallel PWM inverters controlled by a single voltage control block. The detailed design of each inverter module is discussed in chapter 3. The output of the inverter modules are connected together using two series inductors, L_4 and L_5. The series inductors eliminate the high frequency circulation currents (refer to section 1.2.1.1).

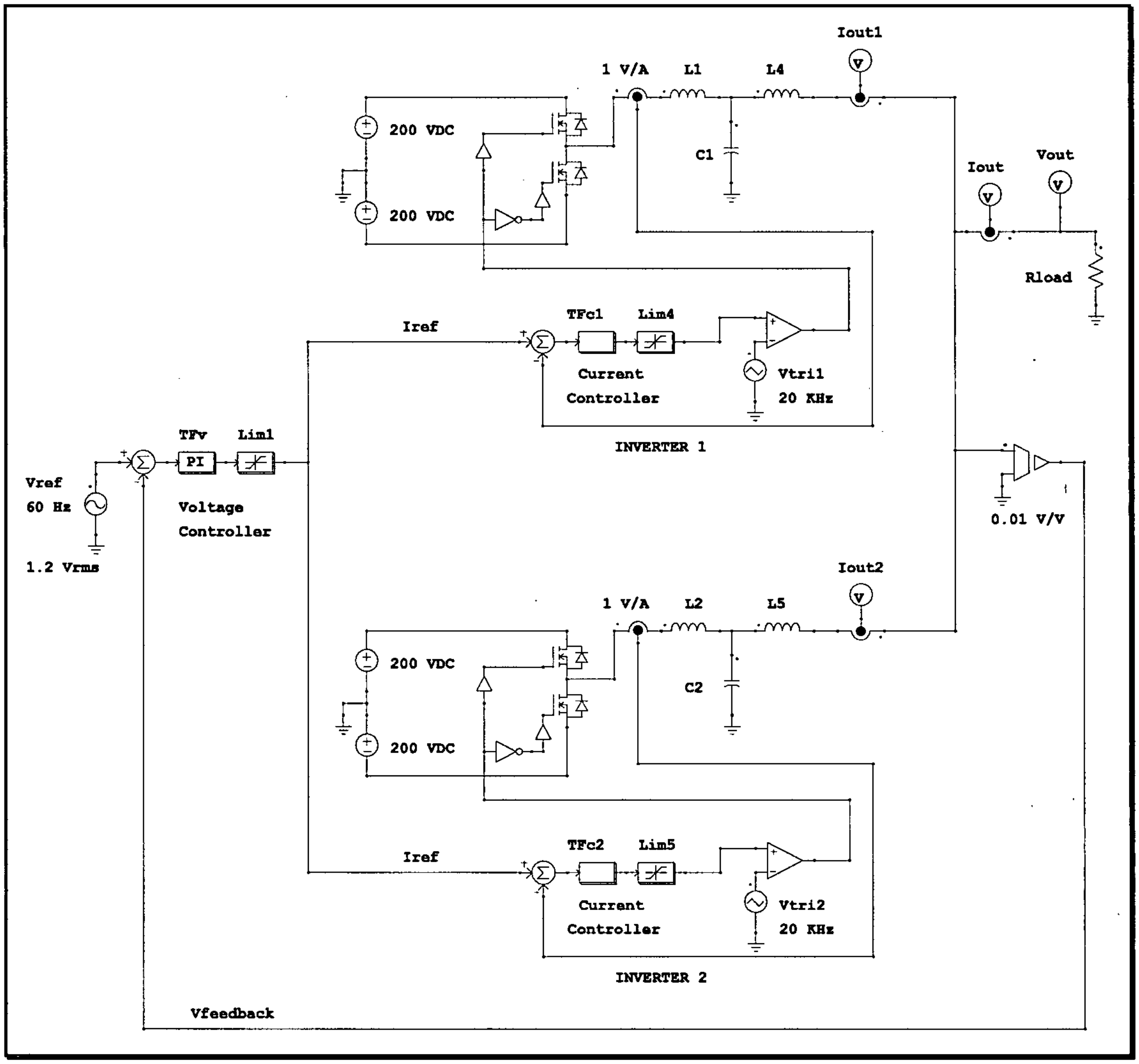

Figure 44. PSIM Simulation Circuit for the Single Voltage Control Method

The component values for the simulation of the single voltage control method are given below (except the ones specified in the diagram):

Switching inductors, L_1 and L_2	= 0.8 mH
Output capacitors, C_1 and C_2	= 26 uF
Series inductors, L_4 and L_5	= 2.5 mH
PWM oscillators, V_{tri1} and V_{tri2}	= -2V to +2V triangular @ 20 KHz
PWM limiters, Lim_4 and Lim_5	= -2V to +2V

Output current limiter, Lim_I	= -5V to +5V (limits module current to 5 A)
Voltage controller, TF_v	$= 20 \cdot \dfrac{2\times10^{-3} \cdot S + 1}{2\times10^{-3} \cdot S}$ (PI controller)
Current controllers, TF_{c1} and TF_{c2}	$= 2 \cdot \dfrac{1.6\times10^{-4} \cdot S + 1}{2.6\times10^{-8} \cdot S^2 + 1.6\times10^{-3} \times S + 1}$

Figure 45 shows the simulation waveforms for a 50 Ω resistive load. The two module currents I_{out1} and I_{out2} are equal. Therefore, the current imbalance method is working correctly. The output currents of all the inverter modules are being delivered to the load (because "$I_{out\text{-}peak} = I_{out1\text{-}peak} + I_{out2\text{-}peak}$"). In other words, the inverter modules are not sinking nor sourcing currents into one another (no circulating currents).

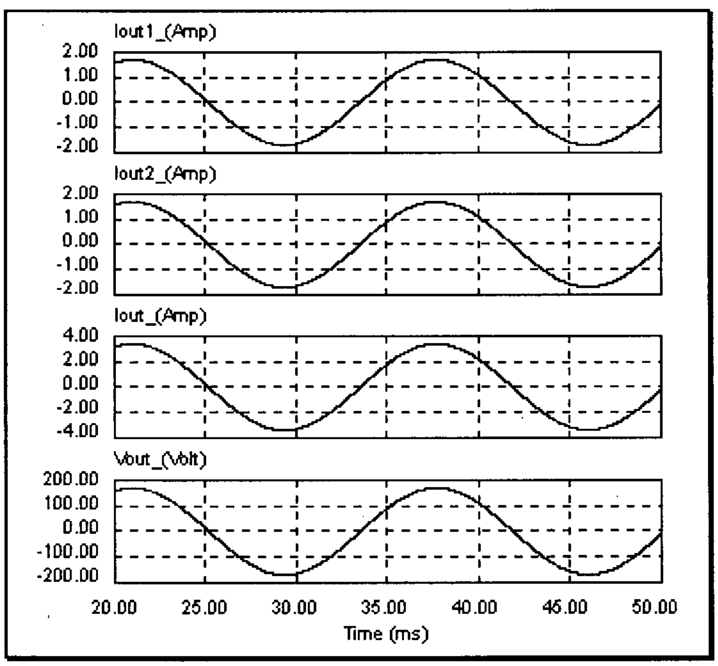

Figure 45. PSIM Simulation Result for Resistive Load

The next figure, Figure 46, shows the simulation results obtained from circuit of Figure 44 with rectified capacitive load (R_{load} = *200 Ω* and C_{load} = *1200 uF*). Again, the two modules are sharing the load current equally. This simulation verifies the stability of the system with nonlinear loads. It also shows the response of the system to a step load. As we can see, the output current of the modules, I_{out1} and I_{out2}, are almost zero during most of the cycle. However, near the positive and negative peaks of the output voltage, the rectified capacitive load starts to draw a significant amount of current. Thus, we can see the response of the system to a step load near the positive and negative peaks of the output voltage, V_{out}. As we can see, the output voltage for a rectified capacitive load is sinusoidal with some clipping near the peaks. This output voltage is acceptable for driving most practical loads.

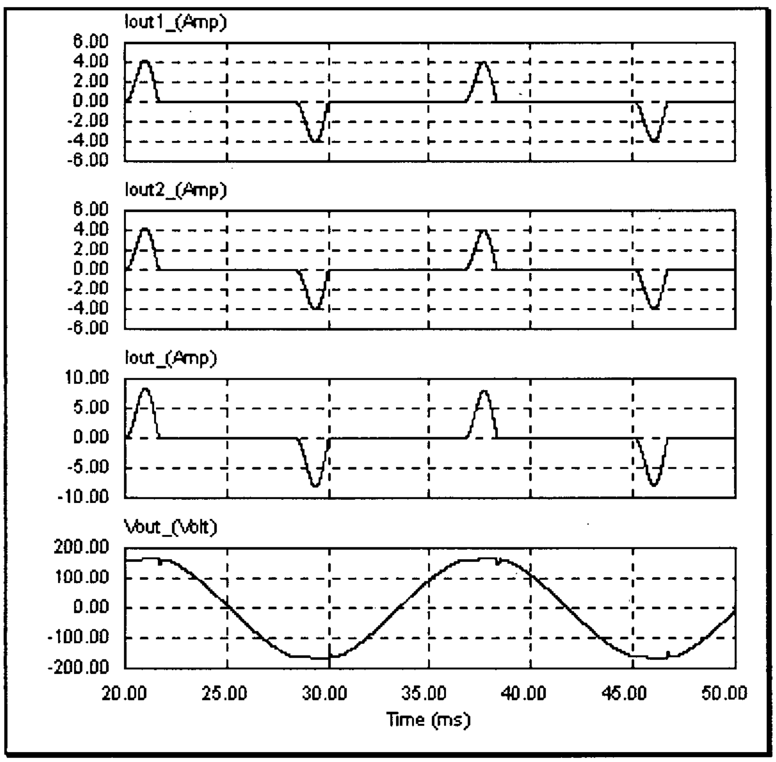

Figure 46. PSIM Simulation Result for Rectified Capacitive Load

Figure 47 shows the simulation results obtained from a system of four parallel inverter modules using the single voltage control method. As we can see, the single voltage control method works for four or more parallel modules.

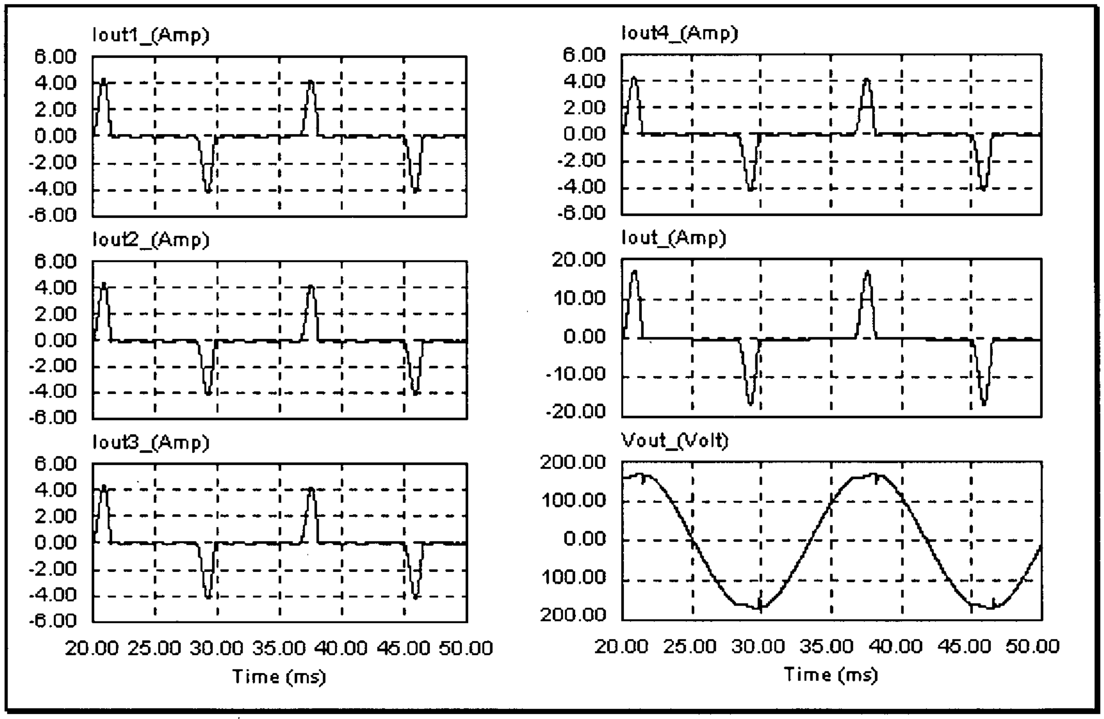

Figure 47. PSIM Simulation Result for 4 Parallel Inverters

Figure 48 shows the simulation results with an inductive load ($R_{load} = 40\ \Omega$ and $L_{load} = 100\ mH$). The system is operating correctly and it shows no indication of instability. Inductive loads are commonly encountered in industrial applications where inductive motors are commonly used.

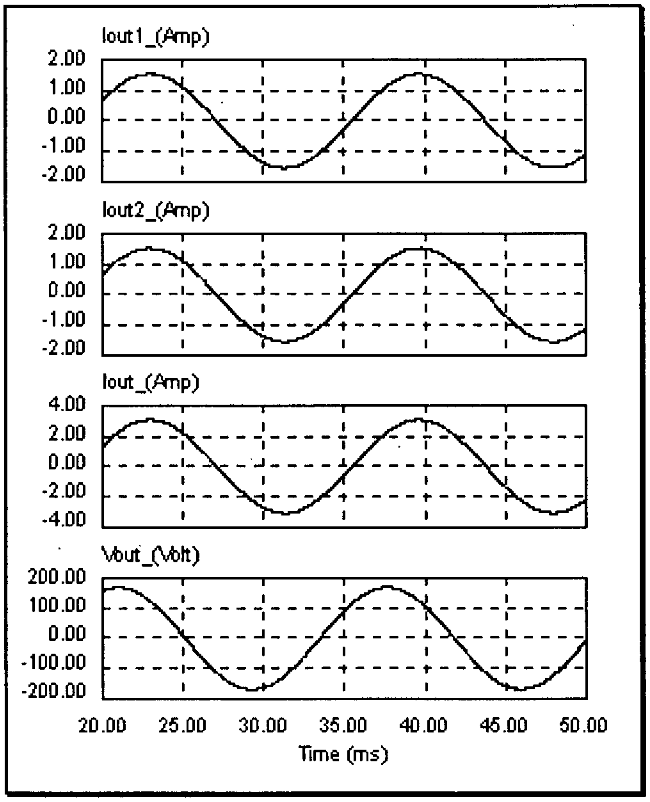

Figure 48. PSIM Simulation Result for Inductive Load

The next figure, Figure 49, presents the simulation results obtained from the circuit of Figure 44 while driving a small resistive load (*1000 Ω*). As we can see, the output current of the inverter modules, I_{out1} and I_{out2}, are almost equal and also there is no circulation current. The distortion in the modules output current waveforms are not really a sign of instability in the system; they are caused due to the relatively slower response of the current loops at low loads. In fact, simulation shows that the system remains stable even at no load.

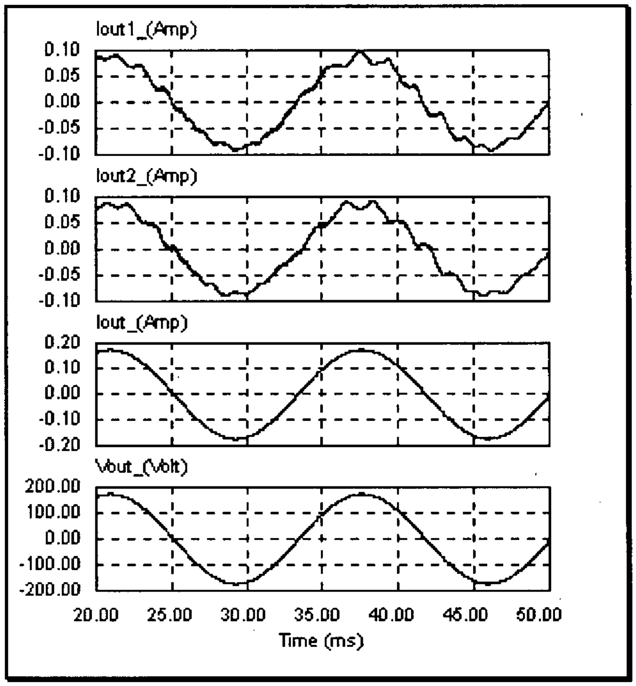

Figure 49. PSIM Simulation Result for a Small Load (No Load)

4.3.2. Experimental Results

In this section, we present the experimental results obtained from a system of two PWM inverter modules connected in parallel using the single voltage control method. The complete schematic of the test circuit is given in Appendix C. The system was tested under different load conditions. Figure 50 shows the measurements obtained from connecting the system to a 120 Ω resistive load. As we can see, the output voltage is sinusoidal and the load is being driven correctly. Also, the two module currents I_{out1} and I_{out2} are almost equal (both phase and amplitude). Thus, the single voltage control method is working correctly and it has eliminated any difference caused by component tolerances. Similarly, Figure 51 shows the measurements for the same circuit connected to a rectified capacitive load. Again we can see that the output currents of all the modules are almost equal and that the step load response of the system is acceptable.

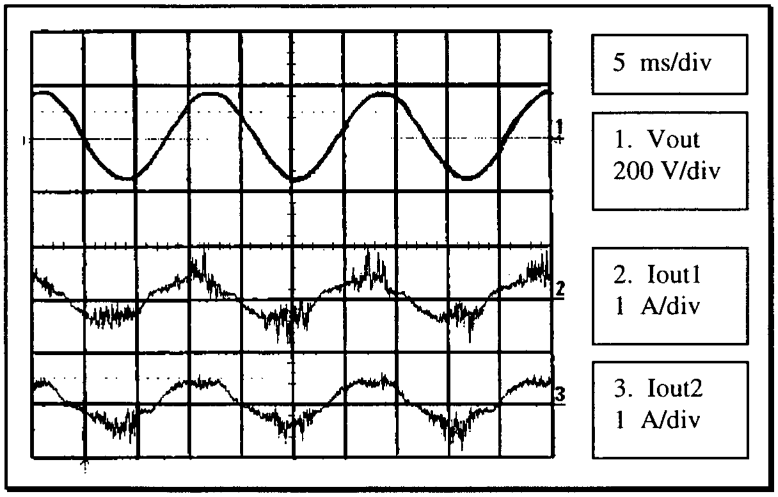

Figure 50. Experimental Results for Resistive Load

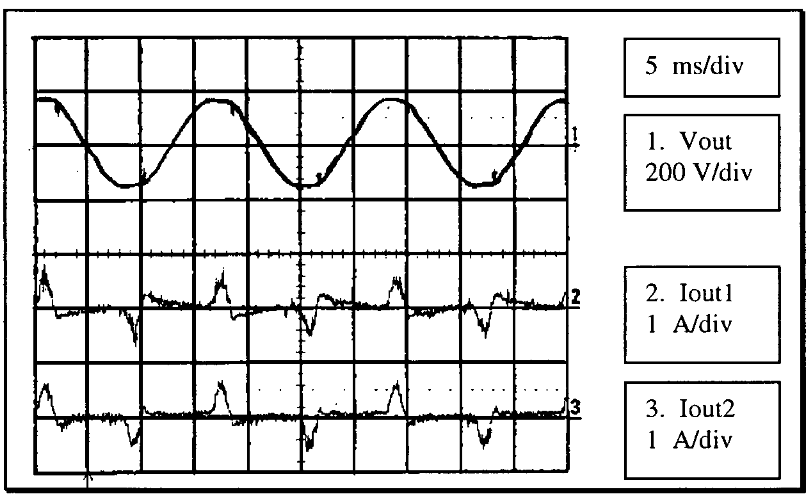

Figure 51. Experimental Results for Rectified Capacitive Load

The next figure, Figure 52, shows the measurement obtained from the current imbalance method prototype driving a small resistive load (1500 Ω). As we can see, the two module currents are more or less equal and there is no circulating currents. Therefore, the single voltage control method remains stable under small, or even, no load conditions.

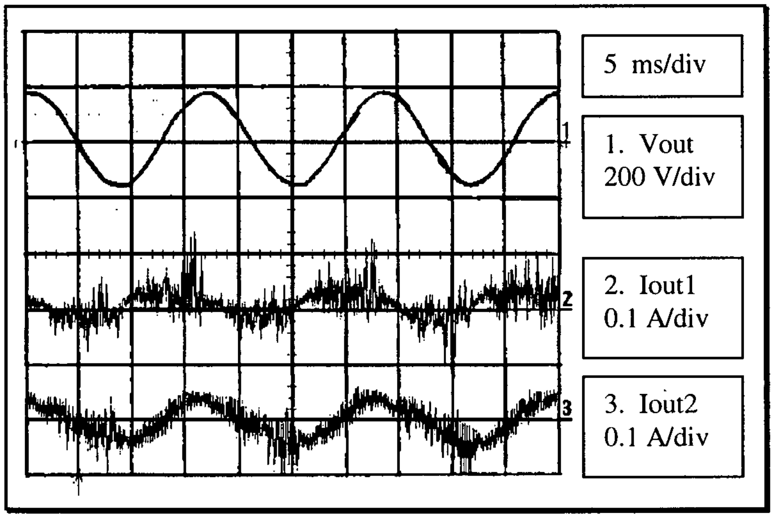

Figure 52. Experimental Results for a Small Load

4.4. Summary

In this chapter, we presented both the simulation results and the experimental results for the two proposed control methods. The results are summarized in here.

We found two problems with the current imbalance method. First, the current imbalance method requires a minimum load for proper operation. At low loads the system does not share the load current equally among all the inverter modules and circulating currents exist in the system. And even more worse, the system becomes unstable at no load. The second problem with the current imbalance method is its poor load sharing capability. As our experiments show, the load current is not shared equally among all the inverter modules. This problem is caused by the poor noise immunity of the system and also by the sensitivity of the system to the non ideal characteristics of the components. The current imbalance signals are small in amplitude and susceptible to noise. They are generated in the power distribution block and are carried over a long noisy path to the inverter modules. Thus, the current imbalance signals are significantly polluted by the noise. Also, any error in calculating the imbalance currents, caused by the non ideal characteristics of components, affects the operation of the system.

No major problems were found with the single voltage control methods. Both simulation and prototype testing, indicate that a parallel inverter system employing the single voltage control method operates correctly under different load conditions. The modules share the load current equally; there are no circulating currents; and the system remains stable even when it is not driving a load.

5. Conclusions

PWM inverters are widely used to provide uninterrupted power to critical loads. Most applications, in which the PWM inverters are used, demand a reliable power source with a low probability of failure. Inverter power systems are required to be fault tolerant and to be redundant to some degree. Also, the industry demands higher power, lower cost, and the capability to expand the system in future. All these requirements can be achieved by connecting a number of PWM inverter modules in parallel, which have a relatively lower power rating. Parallel inverter systems require special control techniques to ensure that the load current is shared by all inverter modules and no circulating current exists in the system. In this thesis, we proposed two new control methods for parallel inverter systems.

The first proposed control method for parallel operation of PWM inverter modules is the current imbalance method. This control method works based on the idea of providing an "imbalance current feedback" to each inverter module and designing the inverters to minimize the imbalance current. The current imbalance method was tested using both computer simulations and a prototype system. Our tests showed that the control method is capable of achieving load sharing and can eliminate circulating currents as long as the load does not become too small. Both simulations and experiments showed that a current imbalance system does not share small load currents and become unstable at no load. Also, our prototype testing indicated that the load sharing capability of the current imbalance method is not very good. This problem is associated with the relatively lower immunity of the system to the noise and also to the calculation errors introduced in the imbalance signals due to the non ideal characteristics of the components.

The second proposed control method for parallel operation of PWM inverter modules is the single voltage control method. A single voltage control inverter system is similar to a conventional current mode inverter with the exception of having N current loops and PWM output stages in parallel (the system has only one voltage control loop). We discussed the stability of the system as it is related to the number of active (operating) inverter modules. The relative stability of the system may change as each inverter module is removed (dropped) from the system; therefore, the system should be designed to tolerate up to a specified number of faulty modules. The single voltage control method was tested using both computer simulations and a prototype system. Our tests showed that the control method is capable of achieving load sharing and can eliminate circulating currents for a wide range of loads. It is also capable of providing a stable output under the no load condition. Thus, the test results for the single voltage control loop is quite satisfactory.

Both proposed control methods are capable of achieving balanced load sharing and reducing the circulating currents with some limitations. However, the single voltage control method has two major advantages compared to the current imbalance method:

- **Better performance over a wider range of loads:** The current imbalance method operates correctly only with a limited range of load values. The current imbalance system does not completely share small load currents among all inverter modules. Furthermore, at small load values, the current imbalance system suffers from circulating currents. And even more importantly, the system becomes unstable at no loads. However a system using the single voltage control method operates correctly at low loads. The load current is shared equally among all inverter modules and there are no circulating currents. Also, the system remains stable even at no load. Therefore, unlike the current imbalance system, the single voltage control method operates correctly over a wider range of loads.

- **Lower cost and less circuitry:** The single voltage control method has only one voltage control loop; however, the current imbalance method requires one voltage control loop per inverter module. Thus, even for a system of two parallel inverter modules, the single voltage control method has fewer voltage control loops than the current imbalance method. Also, the current imbalance method requires additional circuitry for the current imbalance controllers and a power distribution block. The single voltage control method does not require any of these blocks. Therefore, a single voltage control system requires fewer components and costs less than the a comparable current imbalance system.

As we can see, the single voltage control method has two major advantages over the current imbalance method – it has a better performance over a wider range of loads and it costs less. Therefore, we recommend using the single voltage control method over the current imbalance method.

The work presented in this thesis can be followed up in a number of different areas. Firstly, we can investigate why the prototype test results for the current imbalance method do not match the simulation results. The simulations show that the load current is shared in a parallel inverter system, which employs the current imbalance method. However, our prototype testing indicated that the modules do not fully share the load current. This problem deserves more investigation. Secondly, we can determine why the current imbalance system becomes unstable at no loads. It is worthy to try other controllers other than PI controller for the current imbalance loop. We can also try to apply the relative stability criteria to the design of the current imbalance loop. Thirdly, we can further study the stability of a single voltage control system as inverter modules are added or removed from the system. In this paper, we only tested the parallel operation of two units. A higher number of parallel modules needs to be tested and the stability of the system should be verified as inverter modules are added or removed. Also, in chapter 2, we discussed a number of ways to add fault protection circuitry to the proposed parallel inverter systems. These ideas deserve further investigation and testing.

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Appendix I. Small Signal Model of the Inverter

In this appendix we will develop a small signal model for the output stage of the single phase PWM inverter discussed in chapter 3. Our objective is the drive a transfer function for the half-bridge PWM transistor block plus the output filter *LC* shown in Figure 26.

To study the half-bridge switching, we consider two cases. In the first case, the upper transistor, which is connected to $+V_{DC}$, is on and the lower transistor, which is connected to $-V_{DC}$, is off. In the second case, the upper transistor is off and the lower transistor is on. Also, we assume that the first case lasts for duration "*d*" and the second case lasts for the duration "*1 – d*". The total duration of cases 1 and 2 is equal to "1" which is need to obtain the average of cases 1 and 2..

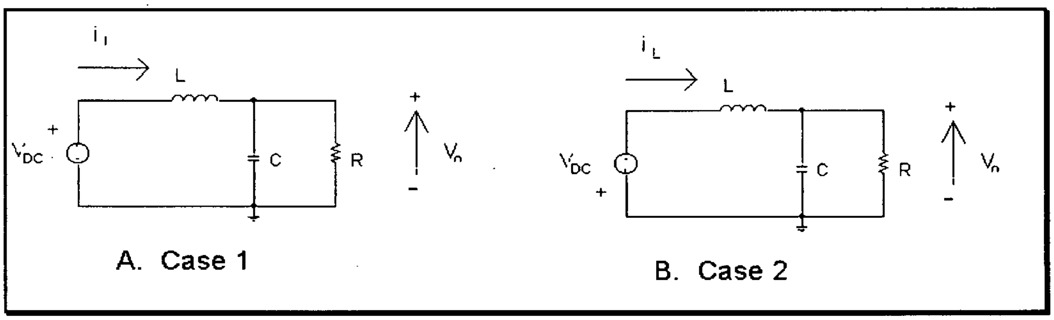


Figure 53. Simplified Models for Cases 1 and 2

Case 1: Upper transistor on, lower transistor off, duration is "*d*". A simplified model of the circuit is shown in Figure 53-A. The nodal and loop equations can be written as follows:

$$V_{DC} - V_o = L \cdot \frac{di_L}{dt} \qquad \textbf{(A1- 1)}$$

$$i_L = C \cdot \frac{dv_o}{dt} + \frac{v_o}{R} \qquad \textbf{(A1- 2)}$$

Where:

v_o	:	Output voltage
i_L	:	Inductor current
R	:	Load resistance
C	:	Output filter capacitor
L	:	Output filter inductor

Case 2: Upper transistor off, lower transistor on, duration is *"1 - d"*. A simplified model of the circuit is shown in Figure 53-B. The nodal and loop equations can be written as follows:

$$-V_{DC} - V_o = L \cdot \frac{di_L}{dt} \tag{A1- 3}$$

$$i_L = C \cdot \frac{dv_o}{dt} + \frac{v_o}{R} \tag{A1- 4}$$

Let us apply the averaging rule to the above equations. Multiplying equations A1-1 by duration *"d"* and A1-3 by duration *"1 – d"* and adding them together gives equation A1-5. Similarly, multiplying equations A1-2 by duration *"d"* and A1-4 by duration *"1 – d"* and adding them together gives equation A1-6. These equations are call the average equations.

$$V_o = (2d - 1) \cdot V_{DC} - L \cdot \frac{di_L}{dt} \tag{A1- 5}$$

$$i_L = C \cdot \frac{dv_o}{dt} + \frac{v_o}{R} \tag{A1- 6}$$

Also, let us assume that each instantaneous quantity is composed of a large signal term (denoted by upper case characters) and a small signal term (denoted by a lower case character and a bar on top):

$$v_o = V_o + \bar{v}_o \qquad \textbf{(A1- 7)}$$

$$i_L = I_L + \bar{i}_L \qquad \textbf{(A1- 8)}$$

$$d = D + \bar{d} \qquad \textbf{(A1- 9)}$$

Substituting equations A1-7 to A1-9 into equation A1-5 gives us:

$$V_o + v_o = 2.D.V_{DC} + 2.\bar{d}.V_{DC} - V_{DC} - L.\frac{d\,\bar{i}_L}{dt} \qquad \textbf{(A1- 10)}$$

Separating the large signal and small signal terms results in the following equations:

$$D = \frac{V_{DC} + V_o}{2 \times V_{DC}} \qquad \textbf{(A1- 11)}$$

$$\bar{v}_o = 2.V_{DC}.\bar{d} - L\frac{d\,\bar{i}_L}{dt} \qquad \textbf{(A1- 12)}$$

Equation A1-11 expresses the duty cycle of the PWM signal in terms of the output voltage and the two DC bus voltages.

Also, substituting equation A1-7 to A1-9 into equation A1-6 and separating the small signal term gives us:

$$\bar{i}_L = C \cdot \frac{d\bar{v}_o}{dt} + \frac{\bar{v}_o}{R} \qquad \textbf{(A1- 13)}$$

Substituting $\bar{v}_o$ from equation A1-12 into A1-13 and replacing the derivative terms with S gives us the following transfer function for the inverter output stage:

$$\frac{\bar{i}_L}{d} = \frac{2.V_{DC}.(RCS+1)}{RLCS^2 + LS + R} \qquad \textbf{(A1- 14)}$$

Since the PWM duty cycle d can be written in terms as:

$$d = \frac{V_m}{V_C} \qquad \textbf{(A1- 15)}$$

Where:

V_m : Modulation voltage generated by the current controller

V_C : The peak amplitude of the PWM triangular oscillator

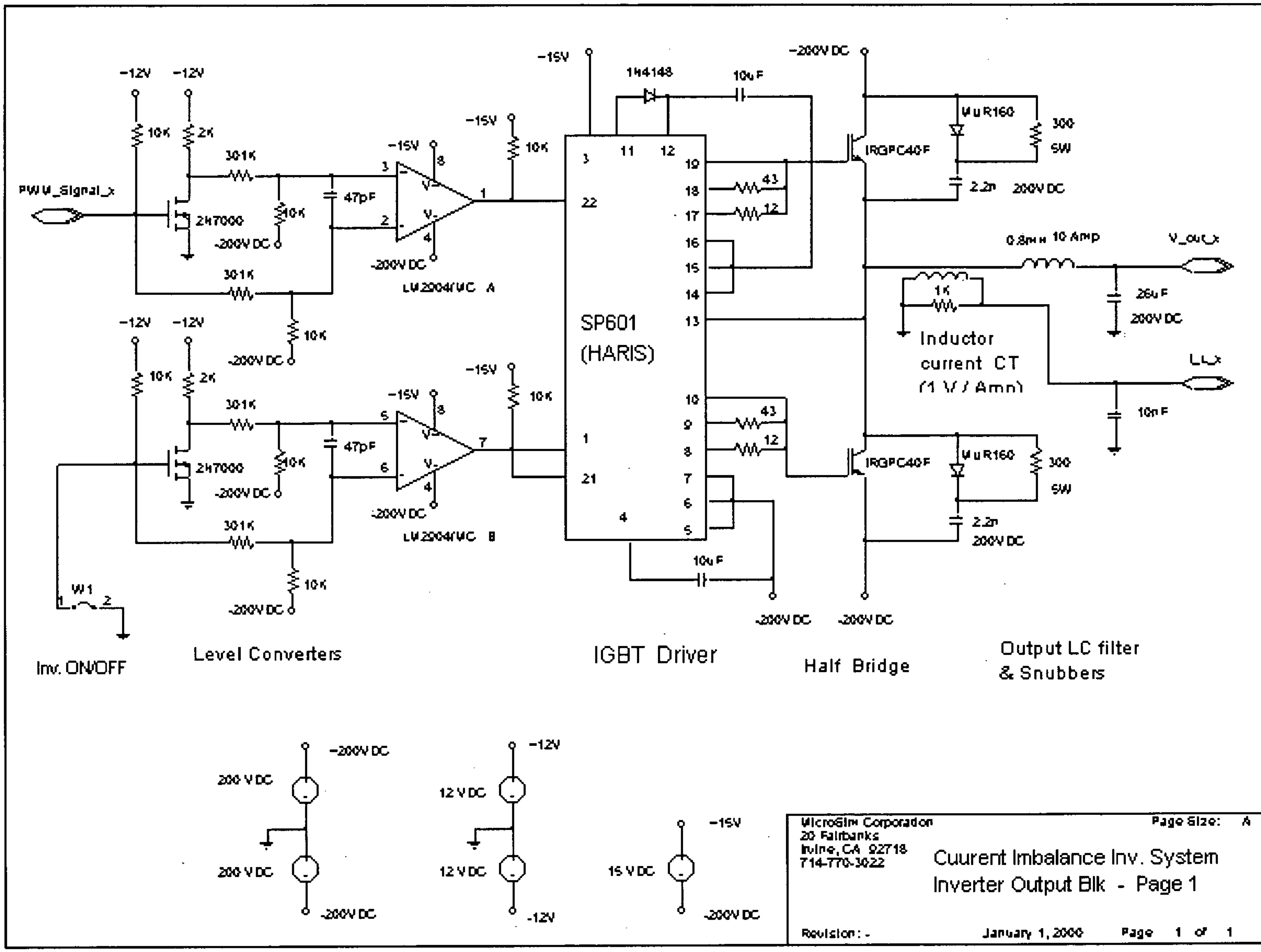
Then, from the above two equations, the PWM transfer function can be written as:

$$\frac{i_L}{v_m} = \frac{2.V_{DC}}{V_C} \times \frac{RCS+1}{RLCS^2 + LS + R} \qquad \textbf{(A1- 16)}$$

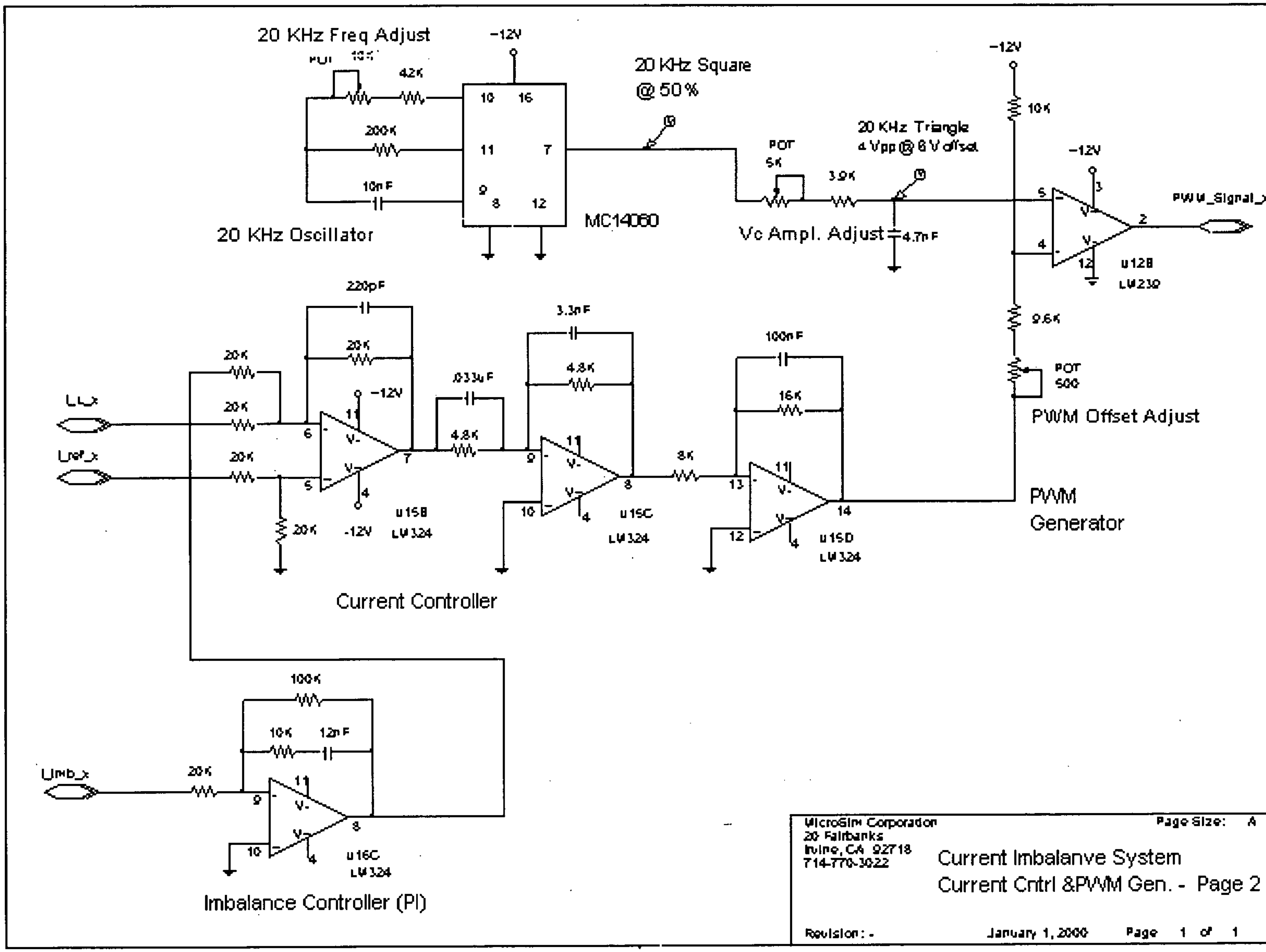
This transfer function is used in chapter 3 to design the current loop.

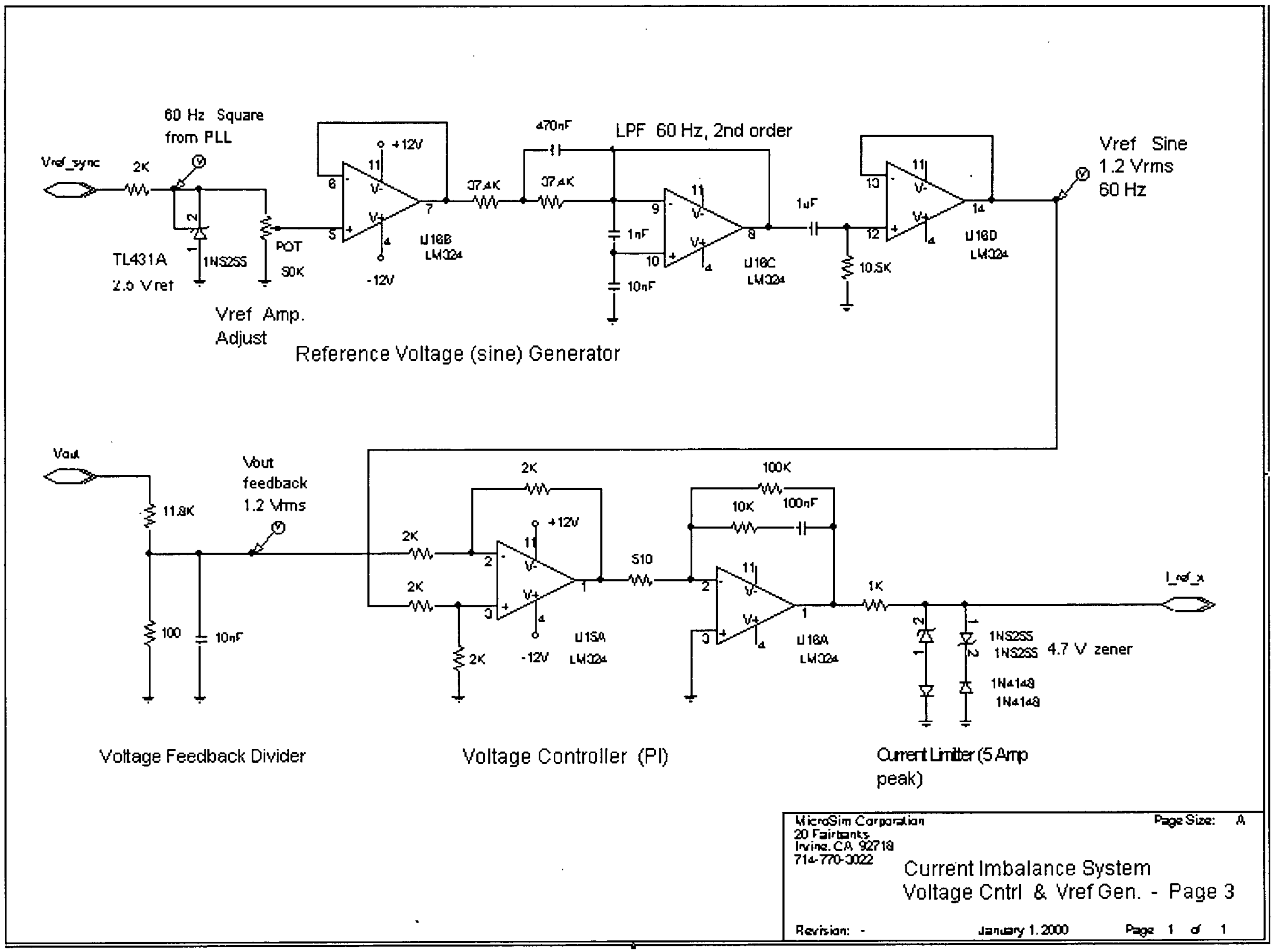
Appendix II. Schematic of the Current Imbalance Control System

In this appendix shows the schematic of our prototype current imbalance system which test results are given in chapter 4. This schematic shows only one of the inverter modules. The other inverter module is identical to the first one.

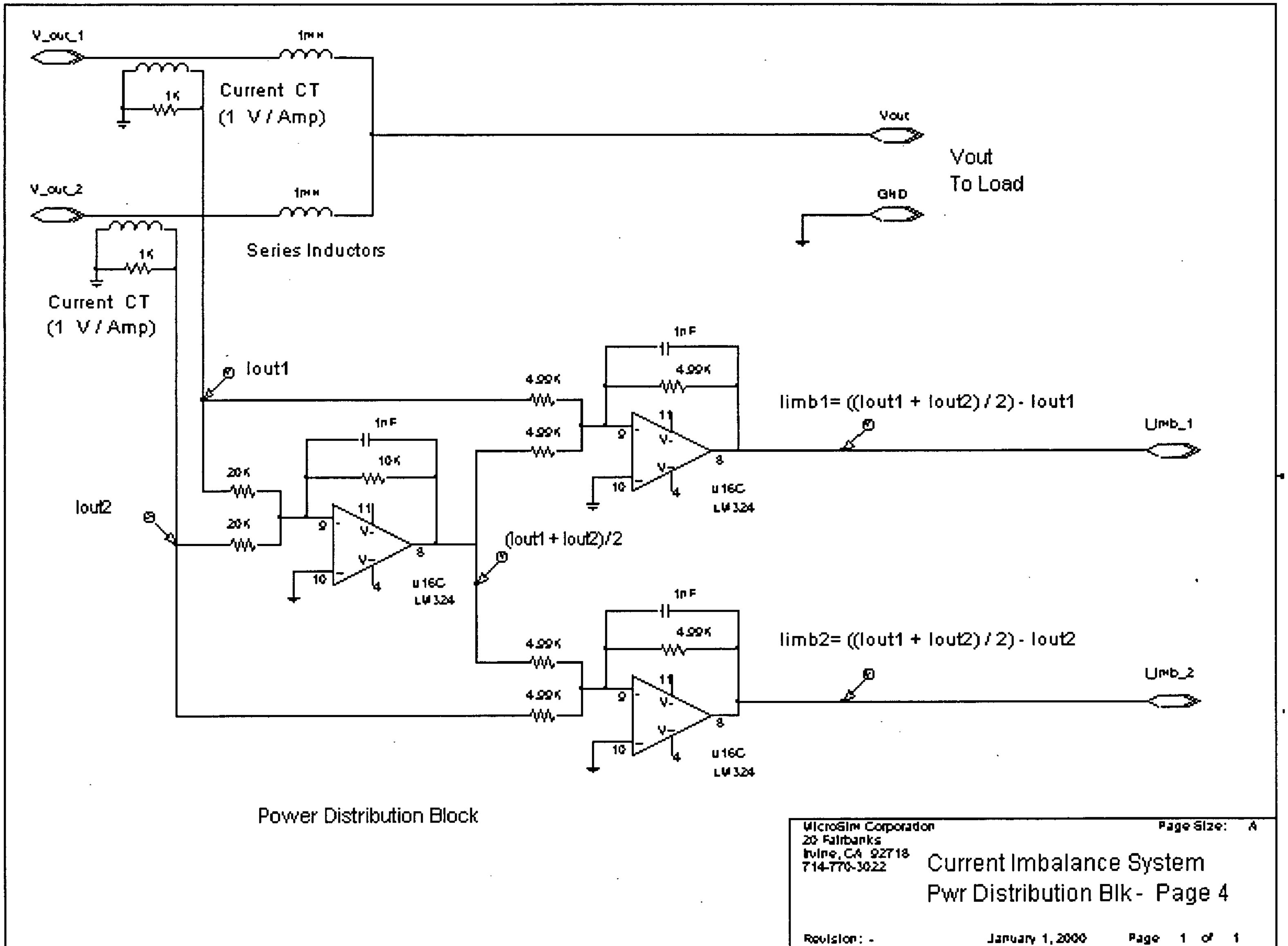


PWM_Signal_x
-12V
10K
2K
301K
2N7000
-200V DC
47pF
-15V
LM2904/UC A
LM2904/UC B
Inv. ON/OFF
W1
Level Converters
SP601
(HARIS)
1N4148
10uF
IGBT Driver
43
12
IRGPC40F
MUR160
300
5W
2.2n
200V DC
Half Bridge
0.8mH 10 Amp
V_out_x
26uF
1K
Inductor
current CT
10nF
Output LC filter
& Snubbers
200 V DC
12 V DC
15 V DC
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Cuurent Imbalance Inv. System
Inverter Output Blk - Page 1
Revision: -
January 1, 2000
Page 1 of 1


20 KHz Freq Adjust
POT 10K
42K
200K
10nF
-12V
10 16
11 7
9 8 12
20 KHz Oscillator
MC14060
20 KHz Square
@ 50%
POT
5K
3.9K
20 KHz Triangle
4 Vpp @ 6 V offset
Vc Ampl. Adjust
4.7nF
-12V
10K
-12V
PWM_Signal_x
u12B
LM230
9.6K
POT
500
PWM Offset Adjust
PWM
Generator
220pF
20K
20K
20K
20K
20K
-12V
-12V
IL_x
Iref_x
u15B
LM324
.033uF
4.8K
3.3nF
4.8K
u15C
LM324
8K
100nF
16K
u15D
LM324
Current Controller
100K
10K
12nF
20K
Imb_x
u16C
LM324
Imbalance Controller (PI)
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Current Imbalanve System
Current Cntrl &PWM Gen. - Page 2
Revision: -
January 1, 2000
Page 1 of 1



60 Hz Square
from PLL
Vref_sync
2K
TL431A
2.5 Vref
1NS255
POT
50K
Vref Amp.
Adjust
+12V
-12V
U18B
LM324
37.4K
37.4K
470nF
LPF 60 Hz, 2nd order
1nF
10nF
U18C
LM324
1uF
10.5K
U18D
LM324
Vref Sine
1.2 Vrms
60 Hz
Reference Voltage (sine) Generator
Vout
11.8K
100
10nF
Vout
feedback
1.2 Vrms
2K
2K
2K
2K
U15A
LM324
510
100K
10K
100nF
U18A
LM324
1K
I_ref_x
1NS255
1NS255
4.7 V zener
1N4148
1N4148
Voltage Feedback Divider
Voltage Controller (PI)
Current Limiter (5 Amp
peak)
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Current Imbalance System
Voltage Cntrl & Vref Gen. - Page 3
Revision: -
January 1, 2000
Page 1 of 1


V_out_1
1mH
1K
Current CT
(1 V / Amp)
Vout
Vout
To Load
V_out_2
1mH
GND
1K
Series Inductors
Current CT
(1 V / Amp)
Iout1
1nF
4.99K
4.99K
limb1= ((Iout1 + Iout2) / 2) - Iout1
4.99K
Limb_1
1nF
10K
20K
u16C
LM324
Iout2
20K
(Iout1 + Iout2)/2
u16C
LM324
1nF
4.99K
4.99K
limb2= ((Iout1 + Iout2) / 2) - Iout2
4.99K
Limb_2
u16C
LM324
Power Distribution Block
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Current Imbalance System
Pwr Distribution Blk - Page 4
Revision: -
January 1, 2000
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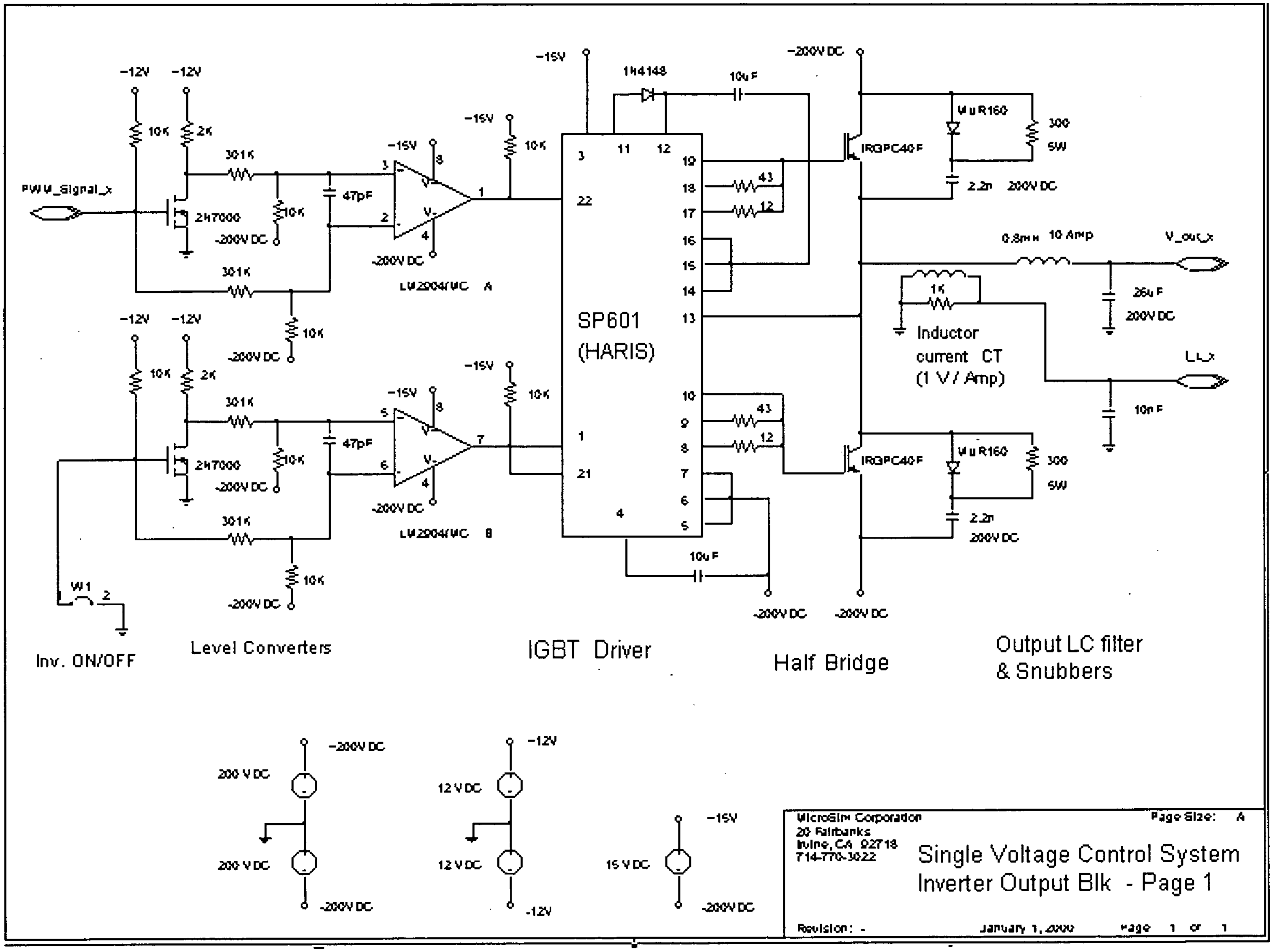
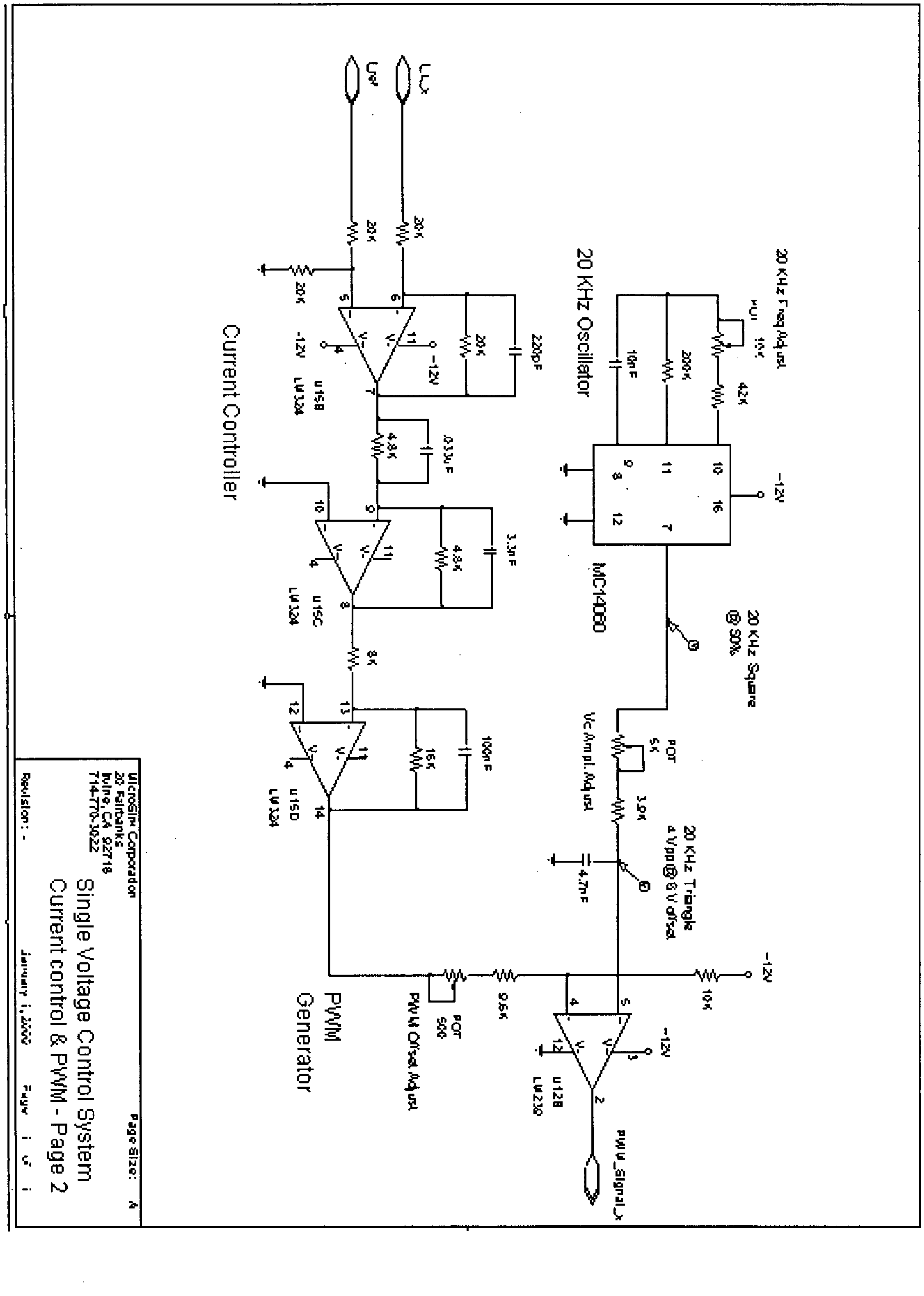
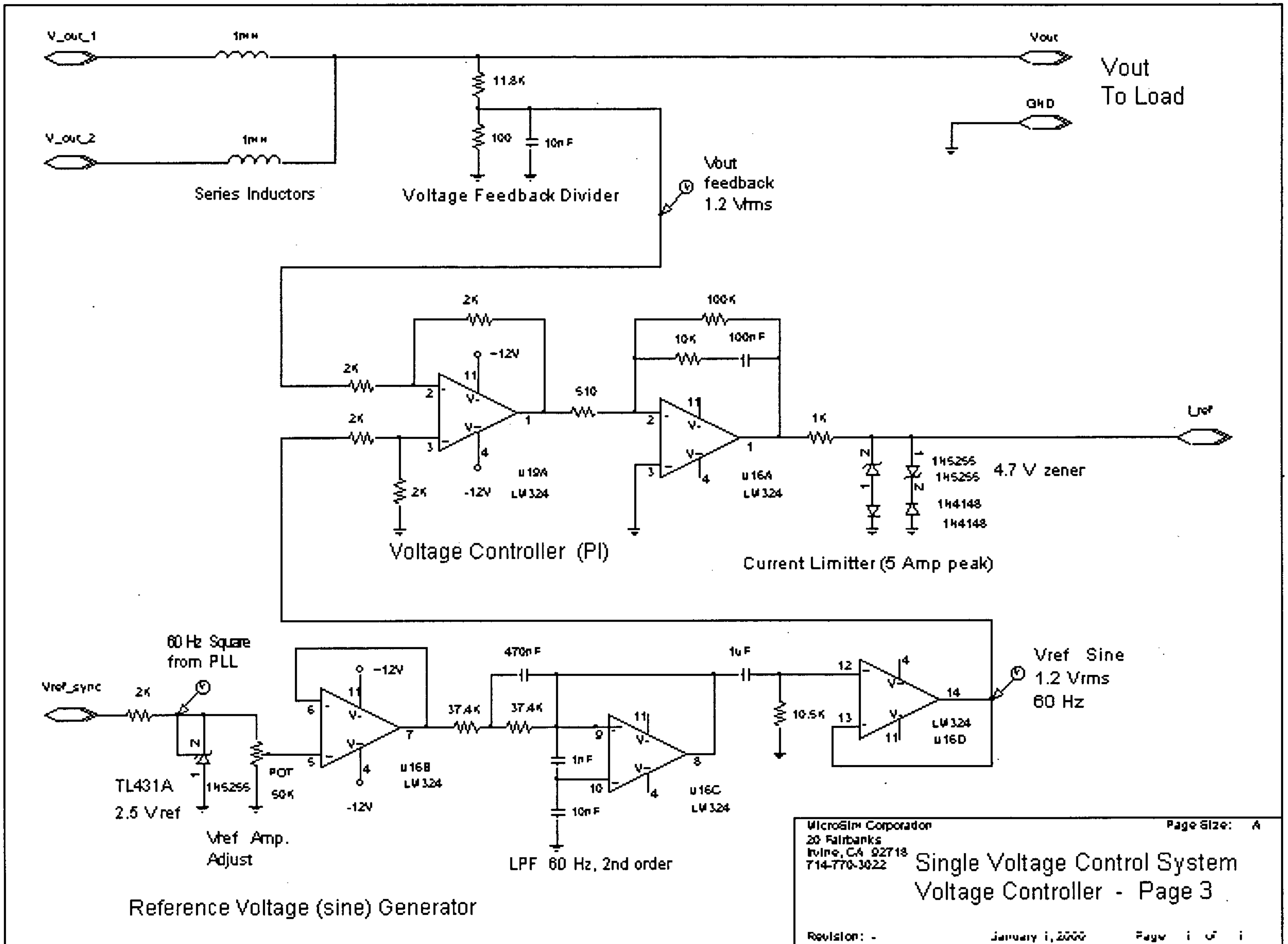
Appendix III. Schematic of the Single Voltage Control System

In this appendix shows the schematic of our prototype single voltage control system which test results are given in chapter 4. This schematic shows only one of the inverter modules. The other inverter module is identical to the first one.


PWM_Signal_x
-12V
10K
2K
2N7000
-200V DC
301K
47pF
-15V
LM2904/MC A
LM2904/MC B
W1
Inv. ON/OFF
Level Converters
SP601
(HARIS)
IGBT Driver
1N4148
10uF
43
12
IRGPC40F
MUR160
300
5W
2.2n
200V DC
Half Bridge
0.8mH 10 Amp
V_out_x
26uF
1K
Inductor
current CT
(1 V / Amp)
10nF
Output LC filter
& Snubbers
200 V DC
12 V DC
15 V DC
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Single Voltage Control System
Inverter Output Blk - Page 1
Revision: -
January 1, 2000
Page 1 of 1


20 KHz Oscillator
MC14060
Current Controller
PWM Generator
PWM_Signal_x
Single Voltage Control System
Current control & PWM - Page 2



V_out_1
1mH
V_out_2
1mH
Series Inductors
11.8K
100
10nF
Voltage Feedback Divider
Vout
GND
Vout
To Load
Vout
feedback
1.2 Vrms
2K
2K
2K
2K
-12V
-12V
U19A
LM324
Voltage Controller (PI)
510
100K
10K
100nF
U16A
LM324
1K
Uref
1N5256
1N5256
4.7 V zener
1N4148
1N4148
Current Limitter (5 Amp peak)
Vref_sync
2K
60 Hz Square
from PLL
TL431A
2.5 Vref
1N5256
POT
50K
Vref Amp.
Adjust
-12V
-12V
U16B
LM324
470nF
37.4K
37.4K
1nF
10nF
U16C
LM324
LPF 60 Hz, 2nd order
1uF
10.5K
LM324
U16D
Vref Sine
1.2 Vrms
60 Hz
Reference Voltage (sine) Generator
MicroSim Corporation
20 Fairbanks
Irvine, CA 92718
714-770-3022
Page Size: A
Single Voltage Control System
Voltage Controller - Page 3
Revision: -