PARASITIC SUBSTRATE EFFECTS IN GALLIUM ARSENIDE MONOLITHIC MESFETS

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Abstract

The present large scale GaAs integrated circuit industry is based on the fabrication of metal-semiconductor field-effect-transistors (MESFETs) on semi-insulating GaAs substrates which provide the device isolation. High-resistivity in semi-insulating GaAs is achieved by the delicate balance between shallow donors and acceptors, and deep levels. The semi-insulating substrates, however, do not provide perfect isolation and do allow crosstalk between neighboring MESFETs. One source of the crosstalk is sidegating, usually defined as the change in drain current of one MESFET as a result of applying a negative potential to a nearby contact of another MESFET. In addition, the interaction of each MESFET with the semi-insulating substrate is strong enough to affect the electrical properties of the device, the most important being the change of the output conductance with frequency. This work is concerned with the above two parasitic effects with the main focus on sidegating, which is the major obstacle for developing large scale GaAs integrated circuits.

Electron injection into the vicinity of a MESFET from a nearby contact via a semi-insulating substrate is known to produce the sidegating effect. This process is known as *single* injection, because the injection is due to a single carrier type. In this work we present a novel study of sidegating in the frequency domain (AC sidegating) and a new mechanism of DC sidegating in which holes are injected into a semi-insulating substrate from the gate of a MESFET and electrons are injected into a semi-insulating substrate from a nearby contact. This process is known as *double* injection.

We distinguish between high- and low-level double injection where the low-level injection is referred to a condition in which the excess carrier concentration is much smaller than the majority carrier concentration in semi-insulating GaAs, while the low-level injection is referred to a condition in which the concentration of injected excess carriers exceeds the majority carrier concentration in semi-insulating GaAs.

High-level double injection results in a drastic variation of a MESFET drain current at voltages lower that those predicted by the single-carrier injection model. It also results in hysteresis in current-

voltage characteristics as observed in experiments.

It is shown that sidegating may occur under conditions of low-level double injection, because of the resultant excess trapped charge distribution which produces non-linear potential profiles across the semi-insulating substrate. The contribution of hole injection and recombination processes to the non-linear potential profile is discussed.

We found that AC sidegating at least up to and including the kHz range is related to DC sidegating, in a way that upon increasing a negative sidegate voltage the AC drain current is decreasing. Upon applying small negative or positive sidegate voltages, thus preserving the conditions of low-level injection, this work predicts a strong sidegating effect in the kHz-MHz range due to the decrease by a few orders of magnitude of the resistance of semi-insulating substrates. This is because semi-insulating GaAs transforms in this frequency range from what is called a "lifetime semiconductor", in which quasi-neutrality of free carriers is preserved, to a "relaxation semiconductor", in which separation of electrons and holes in space exists through zero local recombination. The present treatment predicts that this form of AC sidegating will be only weakly sensitive to hole injection, and will increase and start at lower frequencies on decreasing the distance between the MESFETs.

The peculiar electrical properties of the semi-insulating GaAs in the frequency-domain are used to explain the frequency dependence of the output conductance of GaAs MESFETs on semi-insulating substrates. One result of the model developed in this thesis for the output admittance of GaAs MESFETs is that while the magnitude of the admittance can change by a factor of two or three, the variation of its phase is negligible.

The results of this work indicate that device performance is strongly influenced by the properties of the semi-insulating substrate. One result is that device characteristics are not determined solely by the most dominant trap in the undoped SI substrate EL2, but also by recombination centers (which are not EL2) and shallower traps.

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Glossary

MESFET — metal-semiconductor field-effect-transistor

SI — semi-insulating

VLSI — very-large-scale integration

LSI — large-scale integration

IC — integrated circuit

TFL — trap-filled-limit

SCL — space-charge-limited

MMIC — monolithic microwave integrated circuit

J — electric current density

I-V — current-voltage

DC — direct current

AC — alternate current

η — minority carrier injection ratio

τ — carrier lifetime

q — magnitude of the electronic charge

μ_n — electron mobility

μ_p — hole mobility

n_e — equilibrium electron concentration

δn — excess electron density

p_e — equilibrium hole concentration

δp — excess hole density

Acknowledgements

I would like to thank my supervisor Professor Lawrence Young for his help and support during the course of this work.

Kerry Lowe from BNR (Ottawa) is thanked for providing the test devices used in this research.

This work is dedicated to my parents.

Chapter 1

Introduction

In present GaAs technology, MESFETs are the only devices which have approached the VLSI level of integration. This is due to the simplicity of their fabrication: all we need is two ohmic contacts (source and drain) and a Schottky contact (gate) on a conductive layer (channel). However, with all its simplicity a MESFET exhibits numerous parasitic effects. This work is concerned with parasitic effects in GaAs MESFET integrated circuits, which hinder high-level integration.

The VLSI level of integration requires the fabrication of MESFETs on semi-insulating (SI) substrates, which makes the GaAs technology especially attractive because they reduce the interconnect capacitances and make device isolation simple. The MBE-grown buffer layers are currently too costly for use in the VLSI technology [1]. But the SI GaAs does not act as a mere mechanical support with high resistivity, and does allow leakage currents through the SI substrate between neighboring devices, as well as the leakage current between source and drain of each device. These currents originate effects which affect device performance. Rather than review these effects here, the reader is referred to the recently published text book on GaAs integrated circuits by Long and Butner [2]. In addition, there are review articles on the parasitic effects in GaAs integrated circuits by Rocchi [3] and more recently by Koyama *et al.* [4] and Salmon [5]. Many effects in GaAs MESFETs were investigated using the techniques that had already been developed for Si devices. But it is important to stress that there is a significant difference in the treatment of substrate effects in GaAs and Si devices. Probably the most fundamental difference is associated with the relaxation time in Si and SI GaAs substrates. While the relaxation time of a typical Si substrate is in the range of picoseconds, the relaxation time of a SI GaAs substrate is typically in the range of milliseconds-microseconds. This means that the charge injected into the bulk SI GaAs will not disappear as fast as in Si substrates. Consequently, the parasitic substrate effects will occur beyond the conventional silicon transistor bandwidth, but inside the bandwidth of GaAs MESFETs.

Additional parasitic effects are associated with a Schottky MESFET gate. It is interesting to note that Schottky junctions have never been used in the VLSI Si technology, and their most popular

usage found place in the earlier digital LSI technology (TTL). In comparison to p-n junctions many properties of Schottky junctions are much less understood. A Schottky gate is, however, an essential part of the GaAs MESFET technology, and, therefore, its contribution to the parasitic effects in GaAs MESFETs should be considered.

The major parasitic effect in GaAs integrated circuits is sidegating, the change in drain current as a result of applying a negative potential to a nearby contact (sidegate). The earlier attempts to explain this effect suggested electron injection into the device channel-substrate interface as the main source of sidegating [6]. This explanation was based on the one-dimensional Lampert's model of high-level carrier injection into the insulator with traps, according to which the current increases sharply at a certain threshold voltage [7]. Considering high trap densities in SI GaAs and typical distances between a MESFET and a sidegate, this model has difficulty in explaining the low voltages at which sidegating is often observed. To overcome this difficulty conduction through surface states was suggested [8, 9]. While some of the reported experimental results regarding sidegating could be explained in terms of surface conduction, there are many reports of sidegating in large-geometry devices and in layout arrangements in which the sidegating should have been greatly reduced if the surface had played a major role, but instead a strong effect was observed. According to the the recent review paper by Salmon, circuit manufacturers have developed processes, which control the surface properties, so that, "the surface component of backgating is negligible compared with the bulk backgating" [5].

Sidegating is a complicated phenomenon, in which several mechanisms of transferring charge into the vicinity of the MESFET channel may occur. In certain structures, and, depending on substrate properties, one of the mechanisms can prevail, but on the other hand some mechanisms can occur simultaneously. Fig. 1.1 visualizes some of the sources of parasitic effects in GaAs MESFETs on a SI substrate, that are discussed in this work.

Although the present work has focused on GaAs MESFETs, many of the results are applicable for other devices that incorporate SI material. MESFETs are used here as a probe of parasitic phenomena occurring in SI substrates. Being simpler than other GaAs-based transistors, they provide a tool for

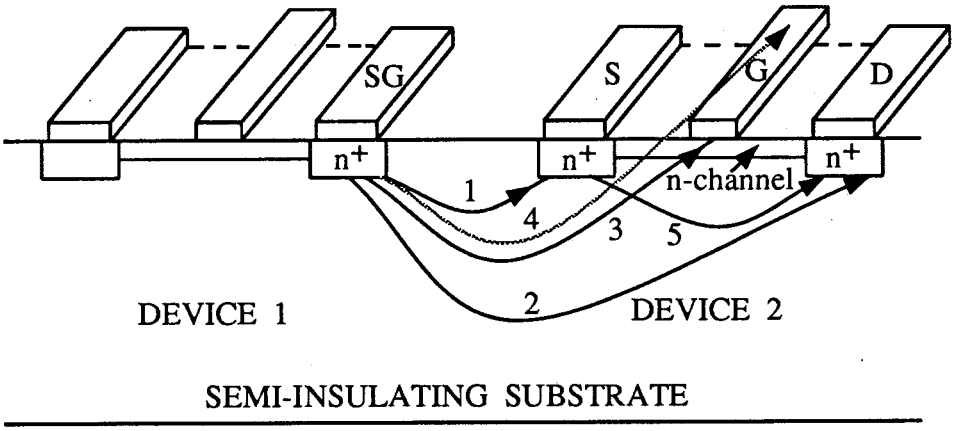


Figure 1.1: Sources of parasitic effects in GaAs MESFETs on a SI substrate. Lines 1–4 visualize interaction mechanisms between two MESFETs on a SI substrate, which can be sources of sidegating: 1–2 interaction between the source/drain to the sidegate, 3 interaction between the sidegate to the gate on a doped channel, 4 interaction between the sidegate to the portion of the gate on a SI substrate (the dashed line shows the edge of the active channel area). Line 5 shows drain-to-source leakage current, which contributes to the increase of an output conductance of a MESFET.

understanding of the interaction with the SI GaAs of more complicated devices such as HEMTs [10] and HBTs [11].

Although measurements by the author are reported throughout this work, the emphasis is not on the measurement techniques, but on the analysis and modeling of the experimental results. The reason for this is that many of the results in this work are similar to those reported by other research laboratories during the last decade. Since the general behavior of the device is known, the major task for researchers is the understanding and interpretation of this behavior. The emphasis was put on an analytical treatment, since it usually provides more insight into device physics than do numerical methods. The present state of the GaAs MESFET technology still requires understanding of the basic phenomena occurring in the integrated circuits, and, therefore, in my opinion, such analysis should precede, or at least be in parallel to, numerical analyses. For example, in order to simplify computation many numerical analyses of sidegating do not consider the continuity equation for holes, and thus eliminate from the discussion many effects predicted by the analytical analysis, which takes the participation of holes into account. An additional reason for analytical modeling is to make results useful for circuit designers by providing closed-form expressions through which a clear relationship is established between design goals and physical device parameters.

In Chapter 2 the experimental investigation and R-C network modeling of AC sidegating are reported. In Chapter 3 the sidegating under conditions of low-level injection into the SI substrate and the role of double injection in the sidegating effect are discussed. In Chapter 4 the extension of the low-level analysis to the frequency domain is presented. This frequency-domain analysis confirms and provides a new interpretation for the experimental results shown in Chapter 2. Chapter 5 shows how the frequency-domain analysis is applied to modeling of the frequency-dependent output conductance of GaAs MESFETs. Finally, conclusions are presented in Chapter 6.

Chapter 2

AC Sidegating

2.1 Introduction

Crosstalk between GaAs MESFETs on SI GaAs substrates can severely affect device isolation and is a major obstacle to the miniaturization of GaAs integrated circuits. An important source of crosstalk is sidegating. Most reports of sidegating have been for DC conditions [12–14]. The results have been subject to different interpretations [12, 15, 8] . AC measurements and their analysis may provide a tool to decide which of various postulated mechanisms is currently occurring. Recently Chen et al. [16] addressed AC sidegating (at 40MHz and 2GHz). They concluded that it must be considered in designing GaAs monolithic microwave integrated circuits. Thus modeling of sidegating, which will predict at least the trends in device behavior, is needed in designing GaAs integrated circuits. The need to extend the investigation of sidegating to the frequency domain is further shown by the following.

As with silicon CMOS technology, in which the development of digital circuits was followed by the development of analog circuits, to provide an interface between the digital circuitry and the external world, the implementation of complex digital-analog systems on a GaAs single chip may soon be at issue. An understanding of the interaction between the analog and digital portions of the system will then be required. The investigation of this interaction is expected to be particularly troublesome at low frequencies, at which anomalies in GaAs monolithic MESFETs are observed. At high frequencies understanding crosstalk is important because of the tendency to combine microwave or RF circuits with their digital control circuits, e.g. RF switches with a driver circuit. Sidegating in GaAs digital integrated circuits has been investigated by applying a pulse train to the sidegate, but only the DC component of the pulse waveform has been considered [16, 17]. The effect, for example, of the pulse train repetition rate on sidegating has not been examined.

2.2 AC Sidegating in GaAs n-i-n structures

MESFET interaction has usually been simulated by applying a negative potential to a sidegate contact on the semi-insulating GaAs substrate and examining its effect on a nearby device located on the same substrate, rather than having two MESFETs. According to the TFL model [12] sidegating is caused by electron injection into the channel-substrate interface of a MESFET and this process occurs due to the space-charge-limited conduction between the sidegate and the drain. Therefore, the sidegate-SI-drain interaction dominates sidegating, and, consequently, in the present section a simpler structure (n-SI-n) has been investigated, which avoids the complex electrical field distribution under the MESFET that otherwise complicates the analysis and the interpretation of the experimental results.

2.2.1 Experimental Procedure

The measurements were performed on planar structures of ohmic contacts on semi-insulating GaAs substrates. Both the input contact, which represent the sidegate, and the output contact, which represent the drain, were n^+ Si implanted directly into SI substrate. The two electrodes were separated by distances of 3 μm to 450 μm of semi-insulating material.

For measurement between 100Hz and 100kHz, the input of the sample was connected to a signal generator, while the output was connected to a Princeton Applied Research(PAR) 5204 lock-in analyzer via a PAR 113 low-noise amplifier, which was used in order to bring the signal to the level detectable by the lock-in analyzer.

A different experimental arrangement was used for measuring the sidegating between 500kHz and 500MHz: the sidegate was connected through a high frequency probe to the HP 8656 signal generator, while the output was connected through another high frequency probe to a HP 8558 spectrum analyzer.

Note that amplification of the signal in these two experimental set-ups is different. In the low-frequency set-up the voltage gain of the low-noise amplifier is set to 2×10^3 and its input is shunted by a 150 Ω resistor. The output resistance of the amplifier is 600 Ω and it is connected to the PAR lock-in analyzer with an input impedance equivalent to a 1 MΩ resistor in parallel with a 30 pF capacitor. In the high-frequency set-up the output is connected to a 50 Ω input of the spectrum analyzer.

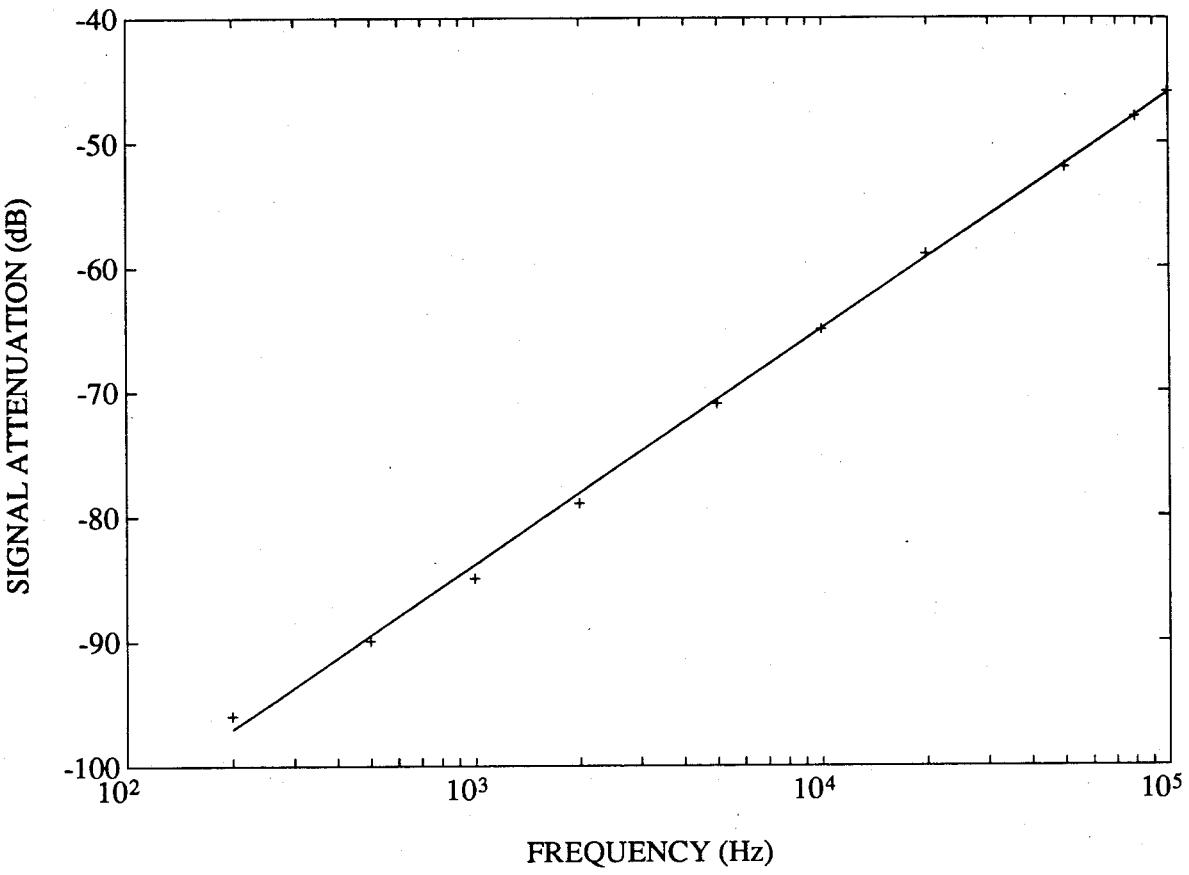


Figure 2.2: Signal attenuation at low frequencies for the 20μm long structure (for sidegate voltage $V_{SG} = -6V$) measured using the low-frequency measurement setup.

2.2.2 Results

The measured signal attenuation through the semi-insulating substrate is plotted as a function of frequency for the range 100Hz - 100kHz in Fig. 2.2. The linear fit exhibits 20dB per decade change of the output signal level with frequency. The signal attenuation at low frequencies for structures with distances of 3μm and 14μm between the n^+ contacts is plotted as function of a sidegate voltage in Figs. 2.3 and 2.4. The 3 μm long structure shows stronger sidegate voltage dependence than the 10 μm long structure at the same range of applied voltages. This effect becomes more pronounced for lower frequencies.

The measured RF signal attenuation is plotted vs. frequency for the range of 500kHz - 500MHz in Fig. 2.5. The output signal level increased 20dB per decade with frequency. Another set

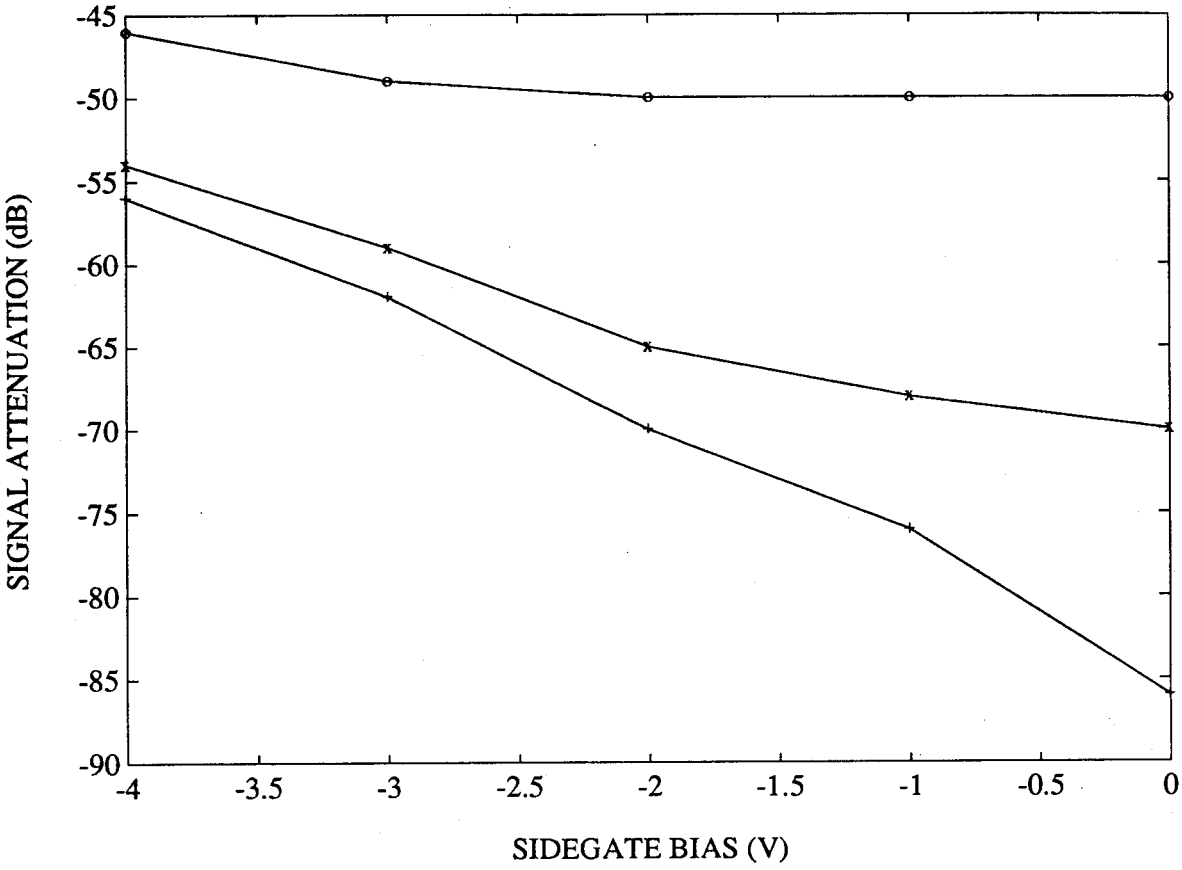


Figure 2.3: Signal attenuation vs. negative sidegate voltage at 1kHz(pluses), 10kHz(x-marks), and 100kHz(circles) measured using the low-frequency measurement setup for 3μm long structure.

of measurements (Fig. 2.6) at radio frequencies was performed on the structure with two contacts separated by 450 μm.

2.2.3 Discussion

Several mechanisms contribute to the crosstalk phenomena. For a given arrangement of conductors if the spacing is small, the electric and magnetic fields of the conductors will overlap sufficiently, so that a wave propagating in one of them will induce a wave in the others. Thus part of the AC sidegating is caused by the coupling between two metal pads through an air and a dielectric material [18, 19]. Capacitive coupling is of course directly proportional to the frequency and will increase 20dB per decade with it (see Figs 2.2 and 2.5).

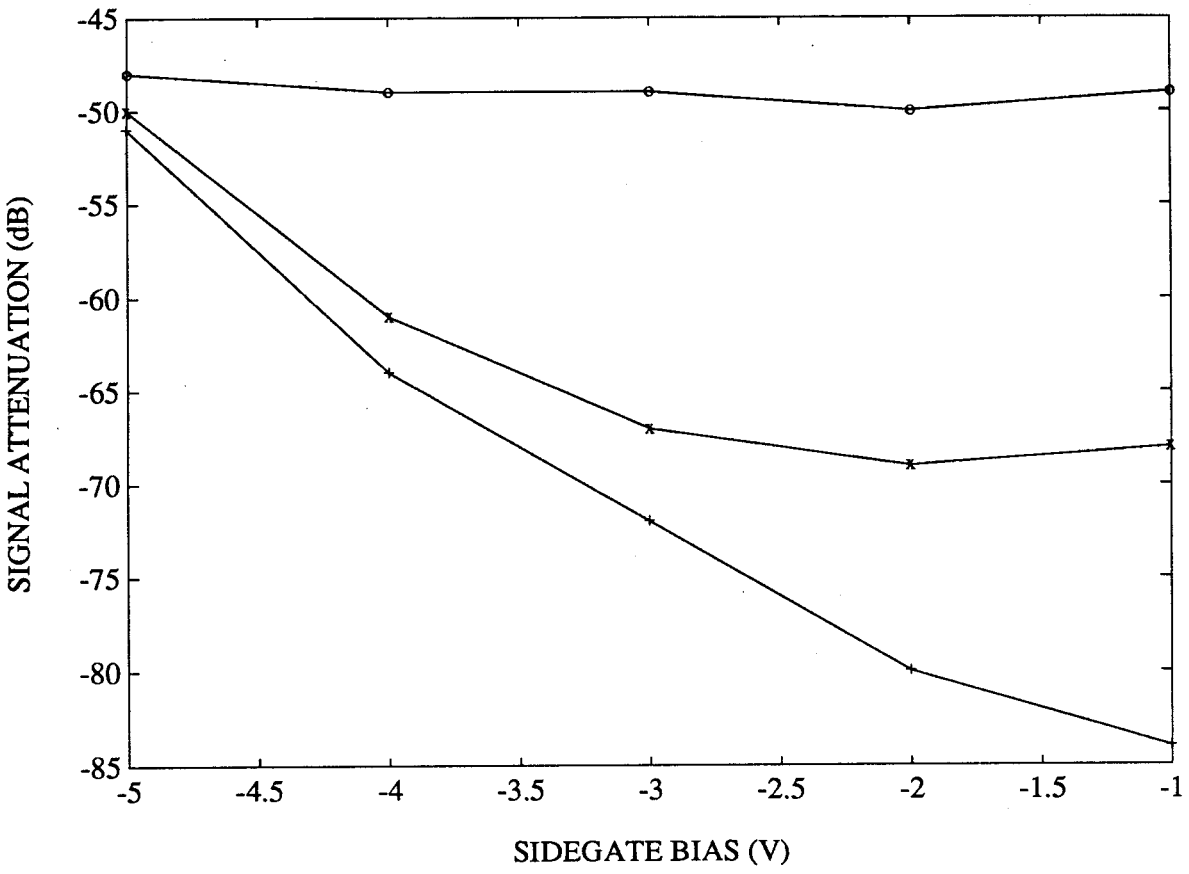


Figure 2.4: Signal attenuation vs. negative sidegate voltage at 1kHz(pluses), 10kHz(x-marks), and 100kHz(circles) measured using the low-frequency measurement setup for 14μm long structure.

Another mechanism contributing to the sidegating involves the conduction current through the insulating substrate with traps. At low voltages an ohmic current will be observed. With increasing applied voltage the injected carriers fill up the traps in the substrate and as the voltage reaches a certain threshold (trap-filled-limit voltage), at which all the traps are full, a steep rise in the current will occur [20]. According to Lee *et al.* [12] a trap-filled space-charge-limited current is observed in semi-insulating GaAs samples. The more detailed models of this phenomenon proposed by Lehovec *et al.* [21] and Horio *et al.* [22] suggest that the space-charge-limited current through the semi-insulating GaAs increases abruptly when the sidegate voltage exceeds a certain threshold and causes the substrate resistance to be reduced over a certain range of voltages. Avalanche breakdown [8] can also produce a threshold effect.

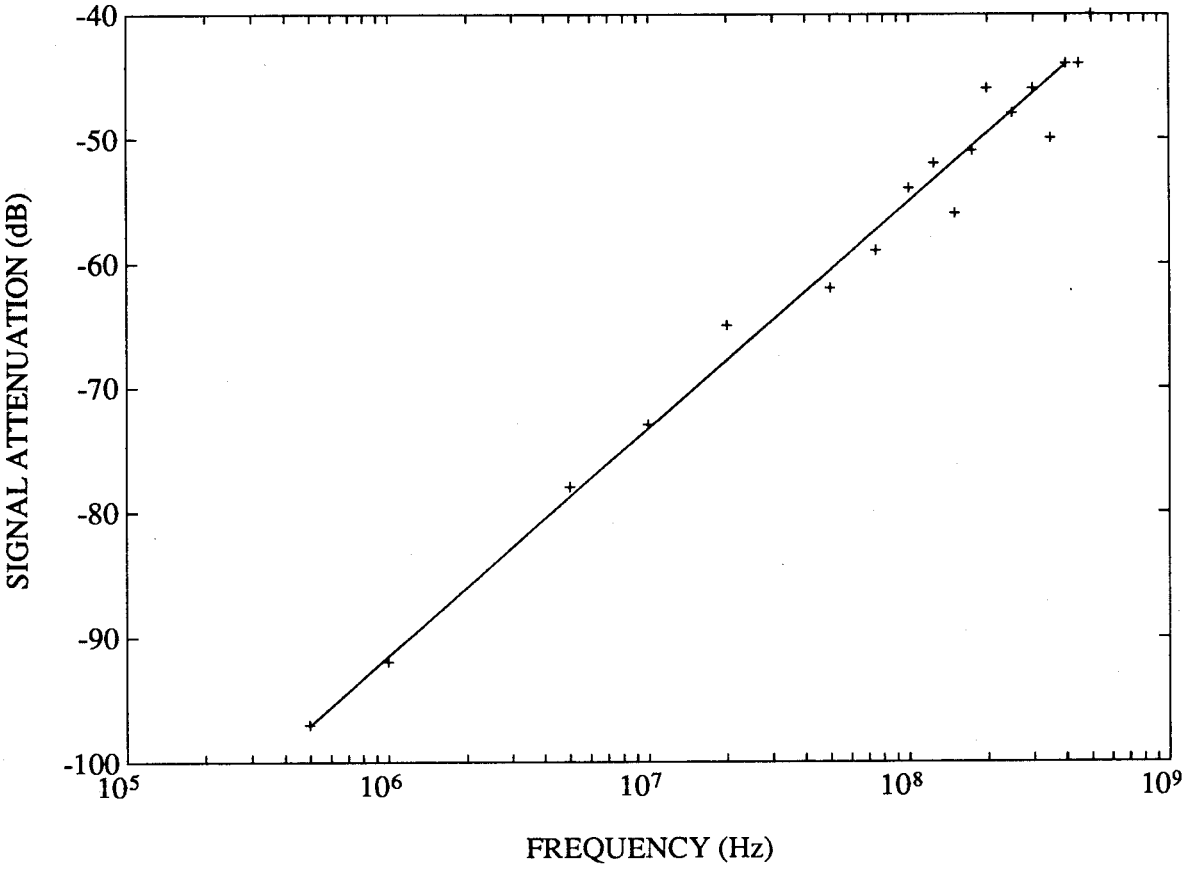


Figure 2.5: Signal attenuation at radio frequencies for the 20μm long structure (for sidegate voltage $V_{SG} = -6V$) measured using the high-frequency measurement setup.

However, the models proposed to explain the sidegating in semi-insulating GaAs concentrate on the investigation of DC current-voltage characteristics only. Semi-insulating GaAs is known to contain both electron and hole traps [23]. The dependence of the space-charge-limited conduction upon frequency is expected to be influenced by the effects of trapping [24, 25]. The frequency dependence arises from the finite time constant associated with the charging and discharging of the traps in semi-insulating GaAs. We will consider only one electron trap, commonly referred to as EL2, which is the most important trap in determining the properties of semi-insulating GaAs [26]. The trap filling can be analyzed using the Shockley-Read-Hall model for recombination through a single level, which, of course, neglects hot electron and field enhanced detrapping effects, which conceivably may be important in the present situation. The rate equation of the full traps on a single

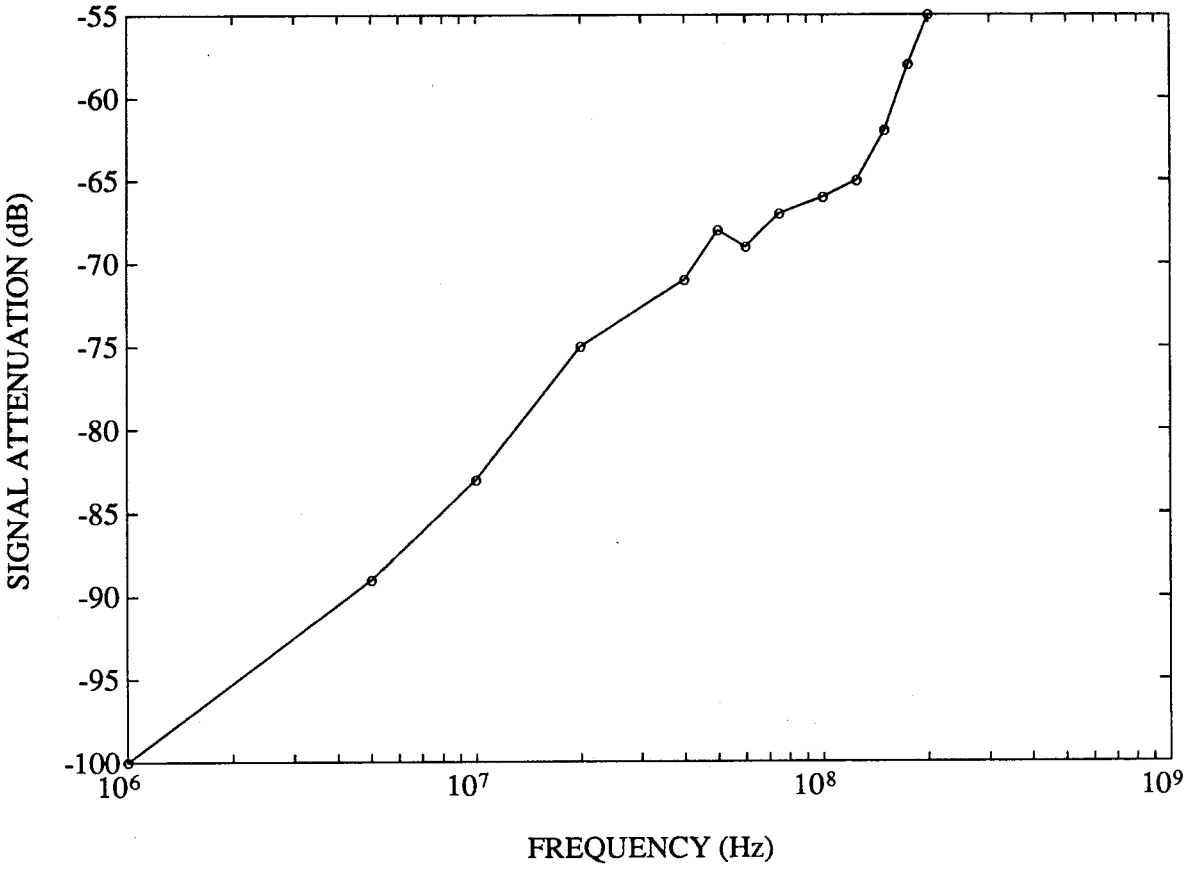


Figure 2.6: Signal attenuation at radio frequencies for the 450μm long structure (for sidegate voltage $V_{SG} = -6V$) measured using the high-frequency measurement setup.

level is given by [27]:

$$N_T \frac{\mathrm{d}f}{\mathrm{d}t} = N_T[(c_n n + e_p)(1 - f) - (c_p p + e_n)f]; \tag{2.1}$$

where N_T = density of traps, f = fraction of traps occupied by electrons, n, p = electron and hole densities, e_n, e_p = emission rates for electrons and holes, c_n, c_p = capture probabilities for electron and holes

This equation can be simplified when the concentration of one carrier largely exceeds the concentration of the other. This is true for the single carrier high injection into the substrate. Furthermore, for EL2 the emission rates for electrons are much greater than that of the holes [28]. Next, we express the electron concentration around its steady state value: $n(t) = n_0 + \Delta n(t)$. Under

these conditions the trap filling equation reduces to:

$$\begin{aligned} \frac{\mathrm{d}n_T}{\mathrm{d}t} &= -(n+n_1)c_n n_T + nc_n N_T \\ &= -[n_0 + \Delta n(t) + n_1]c_n n_T + [n_0 + \Delta n(t)]c_n N_T; \end{aligned} \tag{2.2}$$

where $n_T = N_T f$, n_1 = electron density if the Fermi level were at the trap energy level.

For small variations in electron concentration around its steady state value $[n_0 \gg \Delta n(t)]$ the time constant associated with the traps is given by [29]:

$$\tau_s = 1/c_n(n_0 + n_1)\,. \tag{2.3}$$

Since the steady state electron concentration can be much greater than its equilibrium value the time constant associated with the small variations in electron density also can be much larger than the emission time constant in equilibrium. Under these conditions the time constant does not vary with time. However, it is important to stress that the electron density and consequently the time constant vary across the region between two electrodes. If the electron concentration is 1×10^{13}, using the equilibrium EL2 emission time constant given by [28], the time constant can be estimated to be about 20 μs.

For large transient variations in electron concentration the exact solution of 2.2 is complicated. However, assuming $n_0 \gg n_1$, so that we can write $n_0 \approx n_0 + n_1$, which is true for high applied voltages or for traps lying below the Fermi level, the solution of equation 2.2 for $\Delta n(t) = \Delta n_{max} \cos(wt)$ is given by:

$$n_T(t) = N_T + [n_T(0) - N_T]exp\{-c_n[(n_0 + n_1)t + \Delta n_{max} sin(wt)/w]\}; \tag{2.4}$$

where $n_T(0)$ = initial density of the full traps. The physical system corresponding to the eq. 2.4 is shown in Fig. 2.7.

Equation 2.4 allows an examination of the trap filling time and shows that it is frequency-dependent. At high frequencies the transient response of the traps is not affected by the variations in free electron density because $\Delta n_{max}/w$ is small, but at low frequencies the variations in the free

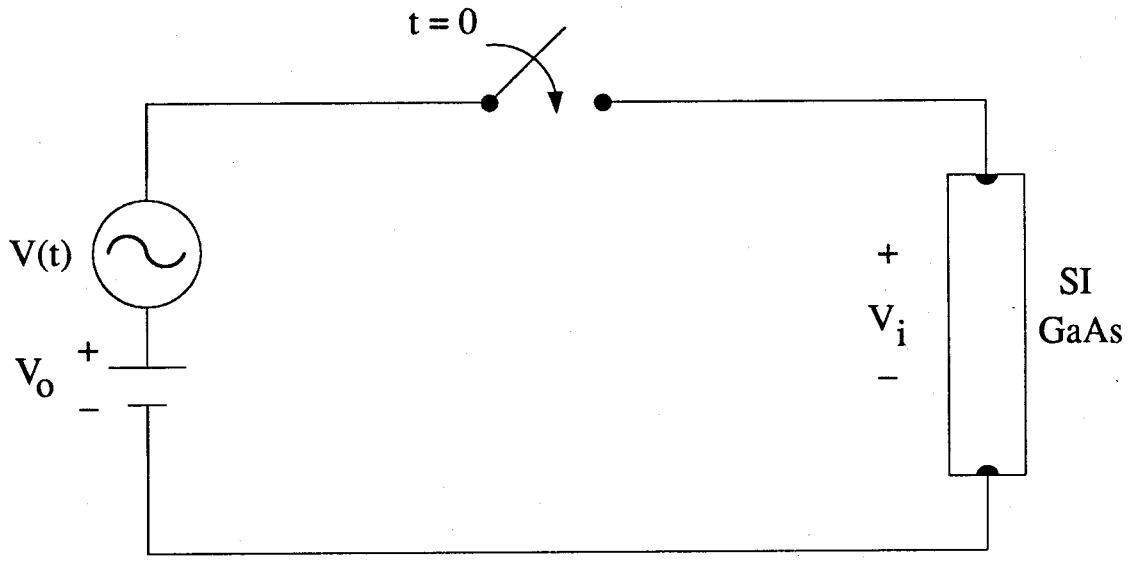


Figure 2.7: Physical system corresponding to the differential equation 2.4 which is used for investigating frequency-dependent transients in SI GaAs. At t=0 the switch is closed and the DC biasing voltage V_0 and the sinusoidal input V(t) are applied to a bar of SI GaAs, which is initially biased at V_i.

electron density are important in determining the transient response. For a very short period of time $sin(wt) \approx wt$ and the time constant is given by:

$$\tau_0 = 1/c_n(n_0 + n_1 + \Delta n_{max}). \tag{2.5}$$

For large t the exponential decay will be determined by $exp[-c_n(n_0 + n_1)t]$. Thus the trap filling time constant will vary with time under transient conditions. This time constant can be in the nanosecond range at the initial stage of transient response and will be equal to τ_s as approaching the steady state. The charge on the deep level adjusts with a time constant τ which varies from τ_0 to τ_s. In the frequency domain this means that for frequencies $f \gg 1/(2\pi\tau)$ the deep level cannot follow the variations in the electron concentration, which respond very fast to the changes in the applied voltage. However, the time constant τ is both time and spatially distributed and therefore there will be a transitional frequency region in which the traps will partly respond. The charge injected into the semi-insulating substrate is equal to the free and trapped charge. At low frequencies $[f \ll 1/(2\pi\tau)]$ the quasi-thermal equilibrium between the free and trapped electrons is maintained. Therefore, the applied voltage modulates both the free and trapped charge. However, only free electrons contribute to the conduction. Thus the low-frequency current-voltage characteristics will be

similar to the static ones, including a steep rise in the current at the trap-filled-limit voltage. At high frequencies $[f \gg 1/(2\pi\tau)]$ the traps cannot follow the changes in the applied voltage. Therefore, only the free charge is modulated and the substrate behaves as a trap-free material. Thus the high-frequency current-voltage characteristics will exhibit a trap-free square law without a steep rise in the current at any voltage. Therefore the set of dynamic current-voltage characteristics will be confined in the triangle formed by the trap-filled-limit, trap-free square, and Ohm's laws as shown in Fig. 2.8. This can be interpreted in terms of the frequency-dependent trap-filled-limit voltage, which will be confined by the DC trap-filled-limit voltage in its upper low-frequency limit, and by the voltage in which the transition from the Ohm's law to the trap-free square law occurs in its lower high-frequency limit. Thus the substrate small-signal resistance will exhibit a frequency dependence at moderate frequencies, but will act as a simple resistance at low and high frequencies (neglecting the electron transit-time effects). This frequency dependence is expected to occur in the megahertz range, which is above the frequency limit (100kHz) of our low-frequency experimental arrangement that was used to investigate the AC sidegating as a function of sidegate voltage.

The above analysis shows that the semi-insulating GaAs can be represented as a bias and frequency dependent conductance and capacitance in parallel. The impact of the resistive component will be more pronounced for low frequencies and for lower resistance. The resistance can be reduced for example by:

1. decrease in the sidegate - output pad separation
2. increase of the magnitude of the applied negative bias voltage

Thus, one might observe this effect at low frequencies for the structures with a short separation. The experimental results between 1kHz - 100kHz for these structures are shown in Figs. 2.3 and 2.4. At these frequencies the conduction in the substrate is not expected to be frequency dependent. The measured DC voltage at which the decrease of a small-signal resistance occurs is $\approx 1.6V$ and $\approx 0.3V$ for the 14μm and 3μm long structures respectively. At 1kHz and 10kHz the coupling variation with the sidegate potential is clearly shown. This dependence is stronger for the shorter structure. At 100kHz the sidegating is dominated by the capacitive coupling and therefore exhibits a weaker bias dependence.

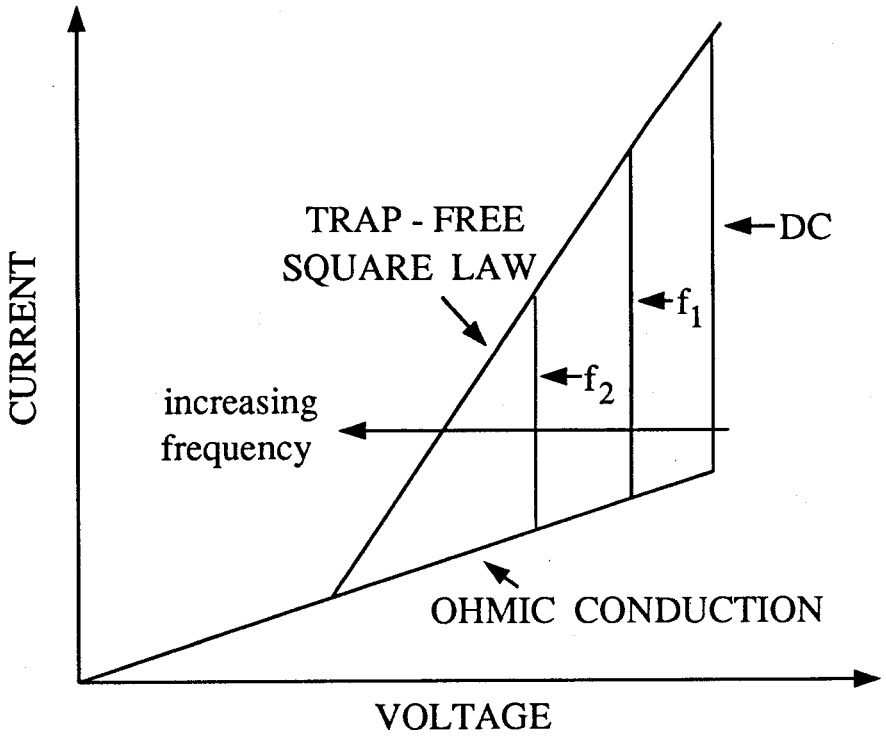


Figure 2.8: Schematic AC current-voltage characteristics for space-charge-limited conduction in SI GaAs at two frequencies $f_2 > f_1$. The current will be confined in the triangle bounded by the lines formed by the DC traps-filled-limit voltage, the trap-free square law and the ohmic conduction.

The capacitance between two long metal electrodes located on the dielectric substrate is determined by the ratio between the metal pad width and the separation distance [19]. A larger separation between the sidegate and the output contact weakens the coupling by decreasing the capacitance and increasing the resistance between the two electrodes. It also increases the voltage required to initiate the trap-filled space-charge-limited conduction in the semi-insulating GaAs substrate. For the applied voltages well below the trap-filled-limit voltage, ohmic current through the semi-insulating substrate is expected. One may anticipate typical parallel RC network bias-independent behaviour in the frequency domain under these conditions. However, the experimental results which are shown in Fig. 2.6 indicate different frequency dependence: output signal level increases with frequency until it saturates at approximately 40MHz and increases again at higher frequencies (above 150MHz). One possible explanation of the experimental data is by the frequency dependence of the conductivity in semi-insulating material which stems from the potential fluctuations resulting from the non-uniform distribution of donors and acceptors and the lack of screening by free carriers. Potential fluctuations

in p-n Si junctions have been discussed by Shockley [30], who pointed out that this phenomenon is important in highly-compensated material. Potential fluctuations existing in compensated and lightly doped semiconductors were discussed in more detail by Shklovskii and Efros [31]. Recently this theory was applied to the semi-insulating GaAs by Pistoulet *et al.* [32]. According to their model the AC conductivity starts from σ_{DC}, grows as w^s (s close to 1) over a wide range of frequencies and then saturates as ω continues to increase. Jonscher *et al.* [33] also indicate the frequency-dependent conductivity of semi-insulating GaAs. The experimental data presented in Fig. 2.6 for large sidegate - output separation behaves below 150MHz qualitatively similar to the data shown by Pistoulet *et al.*. The high frequency response (above about 150MHz) is determined by the increasing capacitive coupling.

In conclusion the AC conductivity in the semi-insulating substrate was investigated over a wide range of frequencies. Analysis of the mechanisms contributing to the AC sidegating shows that for short distances between the ohmic contacts on the same semi-insulating GaAs substrate, the capacitive-resistive coupling will be predominant. The resistive coupling, which probably stems from the trap-filled space-charge-limited conduction through the semi-insulating substrate, is bias dependent and will be important for large sidegate voltages and for low frequencies. The resistive coupling is also expected to be frequency-dependent at moderate frequencies, which are estimated to be in the megahertz range. At low applied voltages, where the capacitive coupling prevails, the experimental arrangement can be used for measuring the capacitance between the input and output electrodes following the procedure described in Ref. [34] applied to the two-terminal structure.

For larger distances the coupling is reduced, and the AC sidegating will be characterized in terms of the inherent AC conductivity properties of semi-insulating GaAs as described in Ref. [32]. The frequency dependence in this case stems probably from the potential fluctuations exhibited in compensated and semi-insulating materials as a result of the non-uniform distribution of donors and acceptors and the absence of screening by free carriers.

The relationship between DC and AC sidegating mechanisms has yet to be established . This relationship is not obvious: the trap-filled space-charge-limited current is not the only conduction mechanism that should be considered. Additional mechanisms are possible and some of them can be

obscured by others. For example, because of the possible surface conduction between the devices, the space-charge-limited current through the substrate can be masked. In this case one can expect a smaller resistance at DC than at some higher frequencies where the surface states will not respond. This work shows that the frequency-domain measurements and analysis are important tools in the crosstalk investigation, which allow the separation of the various effects contributing to the sidegating.

2.3 AC Sidegating in GaAs MESFETs

MESFET interaction has been simulated by applying a negative potential to a sidegate contact on the SI GaAs substrate and examining its effect on a nearby MESFET located on the same substrate, e. g. [6]. This interaction requires an understanding of both the conduction mechanism through the SI GaAs substrate and the electric field distribution under the MESFET gate which depends on the bias voltages. Improvements in GaAs technology, such as higher "quality" SI substrates, better control of fabrication steps, introduction of new processing techniques and new device structures will eventually reduce sidegating. One aim of the present analysis is to seek conditions for minimization of sidegating through an understanding of the relation of the sidegating to the electric field distribution in the MESFET channel as determined by the bias voltages.

The analytic expression for AC sidegating, derived in section 2.3.1 by using a distributed network, relates it in a simple manner to gate and sidegate voltages. The model parameters are evaluated in Section 2.3.2. The experimental data are presented in Section 2.3.3. The results of this work are discussed in Section 2.3.4.

2.3.1 Modeling

An equivalent circuit, which is distributed so as to be applicable to high frequencies, was used. To include substrate effects, in particular conduction through the SI substrate, a 4-terminal network representation of the MESFET is required, where the fourth terminal represents the nearest sidegate contact. The elements of the equivalent circuit are closely related to MESFET physical parameters corresponding to the shape of the space charge distribution in the device as shown in Fig. 2.9. The active layer is bounded by a Schottky barrier contact and a SI substrate. The space charge regions,

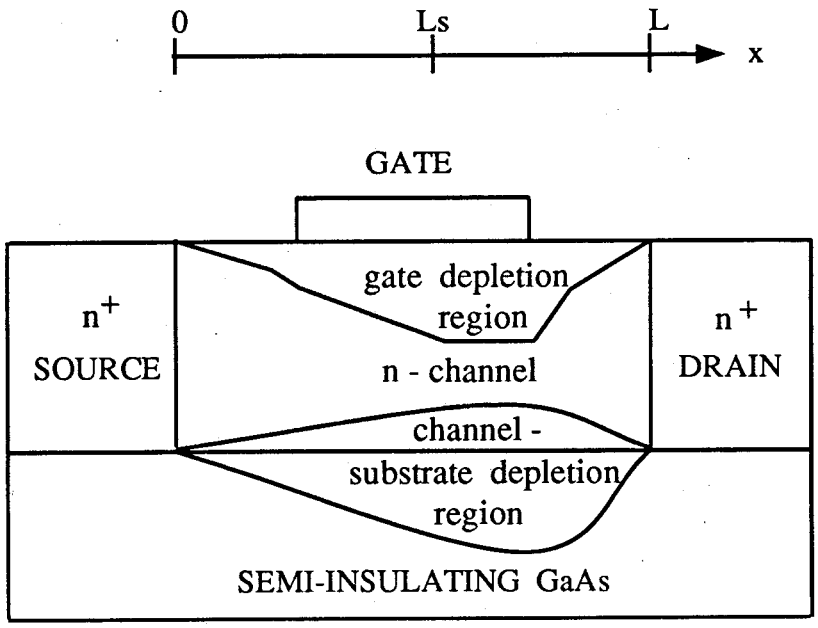


Figure 2.9: Schematic space charge distribution in a GaAs MESFET operating in the saturation region with a negative gate bias.

which are responsible for the channel current modulation, are modified as a result of applying a voltage to the gate and to the sidegate contact and are affected by the surface states on the GaAs surface. Several assumptions have been made.

1. A channel is assumed to be uniformly doped in order to relate in a simple manner the elements of the equivalent circuit to the bias voltages. Ion implantation into SI GaAs substrate is the most widely used technique for fabrication of GaAs integrated circuits and our measurements were performed on low pinch-off ion-implanted GaAs MESFETs. However, in such devices a Gaussian profile can be approximated by an effective uniform doping profile [35].
2. The parasitic capacitances and resistances associated with gate-drain and gate-source regions have been omitted in the distributed network. This is because the surface depletion layer that exists in these regions causes a series resistance and a gate capacitance to be added to the intrinsic MESFET [36] only at low frequencies (below 10kHz) where the surface states can respond [37]. At higher frequencies the gate-drain and the gate-source regions can be represented by pure resistances and the drain resistance is simply added to the external load resistance. The absence of the source resistance in the network can be justified because it is virtually grounded to the

AC grounded gate through the gate capacitance at high gate bias voltages. With decrease in the gate bias the gate capacitance decreases and thus cannot serve as an AC ground, but the channel resistance becomes larger and the source resistance can be neglected with respect to it. It is important to stress that the source resistance must be considered for the MESFET with double-gate excitation (gate and sidegate) since the gate is not AC grounded in this case.

3. The distance between the sidegate and the source is assumed to be much larger than the drain-to-source distance. This allows the region between the sidegate and the MESFET channel to be represented as a uniform R-C network.
4. The shunt leakage resistance of the gate depletion layer is neglected. This resistance may introduce a large time constant which may affect the analysis at low frequencies.

In the linear mode of MESFET operation for small drain-to-source voltages the intrinsic MESFET can be represented by an R-C transmission line [38, 39] with the channel resistance r_{ch} and the gate capacitance c_j per unit length as parameters. Shulman and Young [40] have suggested that the region of semi-insulating material between two ohmic contacts can be modeled as a R-C network. Thus a R-C network, where the resistance r_s represents the conduction through the GaAs SI substrate, the series capacitance c_b represents the space charge region formed at the substrate-channel interface, the resistance r_b represents the conduction through the substrate-channel interface, the parallel capacitance c_s describes the coupling between the sidegate electrode and the MESFET channel, was added to the circuit. In saturation the longitudinal MESFET cross-section can be roughly divided into two regions according to the electric field distribution in the channel. We assume that the electron velocity saturates when the electric field reaches E_s at distance l_s from the source, which corresponds to the boundary between two regions in the device. The resultant network is shown in Fig. 2.10. The network parameters in the first region ($0 \leq x \leq l_s$) are evaluated as follows. The gate depletion layer thickness at distance x from the source is given by:

$$d(x) = \sqrt{2\epsilon[V_B - V_G - V(x)]/qN_D}\,, \tag{2.6}$$

where ϵ is the permittivity of GaAs, N_D is effective uniform donor density, V_B is the built-in voltage, V_G is the gate potential relative to source and $V(x)$ is the channel potential at distance x from the

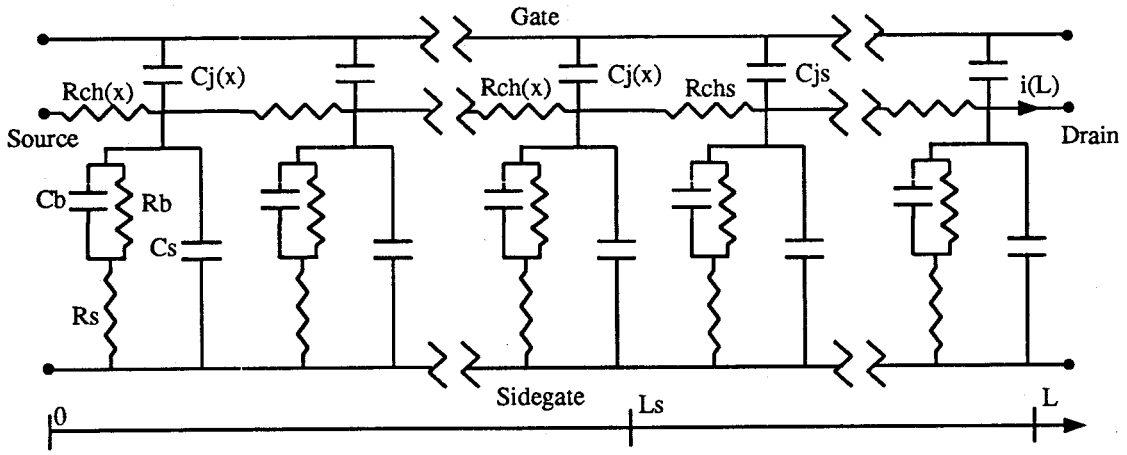


Figure 2.10: Distributed network for a GaAs MESFET in the saturation region.

source, which is $\approx E_s x$. The channel resistance and gate capacitance can be approximated as:

$$\begin{aligned} r_{ch}(x) &= \frac{1}{q\mu N_D w[a-d(x)]} \\ &\approx \frac{k}{q\mu N_D w a(k-1)}\left[1+\frac{E_s k^2}{2V_p(k-1)}x\right], \end{aligned} \tag{2.7}$$

$$c_j(x) = \frac{\epsilon w}{d(x)} \approx \frac{\epsilon w}{a}\left[1-\frac{E_s}{2(V_B-V_G)}x\right], \tag{2.8}$$

where μ is the low-field electron mobility, w is the device width, a is the channel thickness, $V_p = qN_D a^2/2\epsilon$ is the pinch-off voltage and $k = \sqrt{V_p/(V_B - V_G)}$. Eqn. (2.7) and (2.8) can be considered as first-order approximations of exponential functions, so that we can write [38] :

$$r_{ch}(x) \approx r_{cho} e^{\alpha x} \tag{2.9}$$

and

$$c_j(x) \approx c_{jo} e^{-\beta x}, \tag{2.10}$$

where

$$r_{cho} = \frac{k}{q\mu N_D w a(k-1)}, \tag{2.11}$$

$$\alpha = \frac{k^2 E_s}{2V_p(k-1)}, \tag{2.12}$$

$$c_{jo} = \epsilon w k/a \tag{2.13}$$

and

$$\beta = \frac{E_s}{2(V_B - V_G)} . \tag{2.14}$$

The differential equation for the first region for the sidegate excitation is given by:

$$\frac{\partial^2 v}{\partial x^2} - \alpha \frac{\partial v}{\partial x} - r_{ch}(x)\{jw[c_j(x) + c_s] + y_s\}v = -r_{ch}(x)(jwc_s + y_s)v_{sg} , \tag{2.15}$$

where the AC potentials of the channel and sidegate were designated correspondingly by v and v_{sg}, and $y_s = [r_s + r_b/(1 + jwc_b r_b)]^{-1}$. An analytic solution of (2.15), given in Appendix B, can be obtained by assuming that $wc_j(x) \gg wc_s$, y_s and $\alpha = \beta$. The first assumption is reasonable for a MESFET operating at intermediate and high frequencies and for relatively low substrate conduction between the sidegate terminal and the MESFET. The second requirement imposes $V_p = 4(V_B - V_G)$, which corresponds to the condition that the gate depletion layer at the source end is equal to half of the device thickness. This condition may appear to severely restrict our analysis since it becomes valid only for one particular value of the gate voltage. However, this gate biasing voltage corresponds to the normal mode of MESFET operation. Thus, the following analysis can serve as indication of the sidegating dependence on the gate bias around its typical value. Furthermore, no restrictions were made on the drain-to-source voltage. Therefore, the sidegating behavior due to the variations in drain-to-source voltage can be investigated.

In the second region ($l_s \leq x \leq l$) the channel resistance and the gate capacitance are assumed to be constant and are given by $r_{chs} = r_{cho}e^{(\alpha l_s)}$ and $c_{js} = c_{jo}e^{(-\beta l_s)}$. The differential equation for the second region is given by:

$$\frac{\partial^2 v}{\partial x^2} - [jw(c_{js} + c_s) + y_s]r_{chs}v = (jwc_s + y_s)r_{chs}v_{sg} . \tag{2.16}$$

The solution of the above equation is given in Appendix A. Combining (2.15) and (2.16) with the boundary conditions zero potential at $x = 0$ and $x = l$ and current and potential continuity at $x = l_s$ yields the following expression for sidegate transconductance $[i(l)/v_{sg}]$:

$$g_{mb} = \frac{jwc_s + y_s}{Au} \times \{A + \frac{pe^{(p+\alpha/2)l_s}[1 - \coth(pl_s)] - e^{(\alpha l_s)}[\alpha/2 - p\coth(pl_s)]}{jwc_{jo}r_{chs}/u^2} \\ - e^{[-u(l-l_s)]}[u - \alpha/2 - p\coth(pl_s)] - p\coth(pl_s) - \alpha/2\} , \tag{2.17}$$

where

$p = \sqrt{(\alpha/2)^2 + jwr_{cho}c_{jo}}$,

$u = \sqrt{r_{chs}[jw(c_{js} + c_s) + y_s]}$ and

$A = [\alpha/2 + p\coth(pl_s)]\sinh[u(l - l_s)] + u\cosh[u(l - l_s)]$.

For practical device parameters eqn. (2.17) reduces to:

$$g_{mb} = (jwc_s + y_s)/u\,. \tag{2.18}$$

2.3.2 Determination of model parameters

The method used to evaluate the MESFET equivalent circuit parameters was simple and fast at some expense of accuracy. The channel resistance was obtained from the current-voltage characteristics of the MESFET operating in the linear region using an HP 4145A semiconductor parameter analyzer (SPA). The substrate resistance was evaluated from the sidegate current-voltage measurements using the SPA. The substrate resistance measured between 0 and -3 volts was $\approx 2G\Omega$. The resistance was drastically reduced below -3V. Interpretation of the sidegate current-voltage characteristics is difficult and can lead to significant errors in the resistance evaluation [41]. Our DC measurements [42, 43] and the hysteresis observed by other researchers [15] suggest the possibility of double injection into the semi-insulating substrate. Even a small amount of hole injection from the channel into the substrate will result in most of the resistance being near the hole-injecting contact [41]. Consequently we assigned r_b to be 95% of the measured resistance.

The coupling capacitance between the sidegate and the channel was estimated to be 15fF using the graphs of the characteristic impedance of coplanar strips given in [19]. Measurements of the small-geometry MESFET gate capacitance followed a procedure similar to that in [34]. The source and drain terminals were fed from a common AC source. The AC current through the gate was fed into a Keithley 417 high speed picoammeter, whose output was connected to a Princeton Applied Research 5204 lock-in amplifier. The capacitance was evaluated from the measurements of the capacitive part of the AC current through a Schottky barrier. The measured gate capacitance of the depletion-mode

MESFET for $V_G = -0.1V$ at 1kHz was 80fF. The measurements at lower frequencies showed higher values of the gate capacitance. This is consistent with effects due to the presence of the deep levels in the device [44] and to the presence of the surface states in the gate-source and gate-drain spacings which increase the effective gate capacitance [36]. To avoid these problems the measurements at higher frequencies are preferred, which in our case were limited to 1kHz by the frequency response of the system. The capacitance of ion-implanted devices for the gate voltages lower and higher than $V_G = -0.1V$ were found by [45] :

$$c_j = c_{jo}(1 - V_G/0.75V)^{-1.33}, \tag{2.19}$$

where c_{jo} is zero-bias gate capacitance. Measurement of the capacitance associated with a channel-substrate interface is difficult due to the existence of a very high series resistance presented by the substrate [46] and therefore it was calculated using the equation for the width of the channel-substrate depletion region as a function of voltage given in [47].

2.3.3 Comparison with experimental results

Experiments were performed on recessed-gate depletion and enhancement mode ion-implanted GaAs MESFETs made at a commercial foundry. The gate length of the transistors was 1 μm and their width was 52 μm. The length of the regions between the gate and the source and between the gate and the drain was 2 μm. The sidegate was located parallel to the source at a distance 14 μm. An HP 4145A SPA was used to bias a GaAs MESFET: the drain terminal was connected to the parameter analyzer through the load resistor(150 ohm), while the gate was biased directly and the source was grounded. The sidegate was negatively biased with respect to the source and was connected to the signal generator, while the drain was connected to the lock-in amplifier. Figures 2.11-2.16 compare the sidegating experimental data as a function of frequency and various bias conditions with results calculated by (2.18). AC sidegating as a function of the gate bias for the depletion mode MESFET operating at small drain-to-source voltage is shown in Fig. 2.11. Fig. 2.12 shows the AC sidegating dependence on the gate bias for the enhancement mode transistor operating at small drain-to-source voltage. The dependence of AC sidegating on the gate bias for

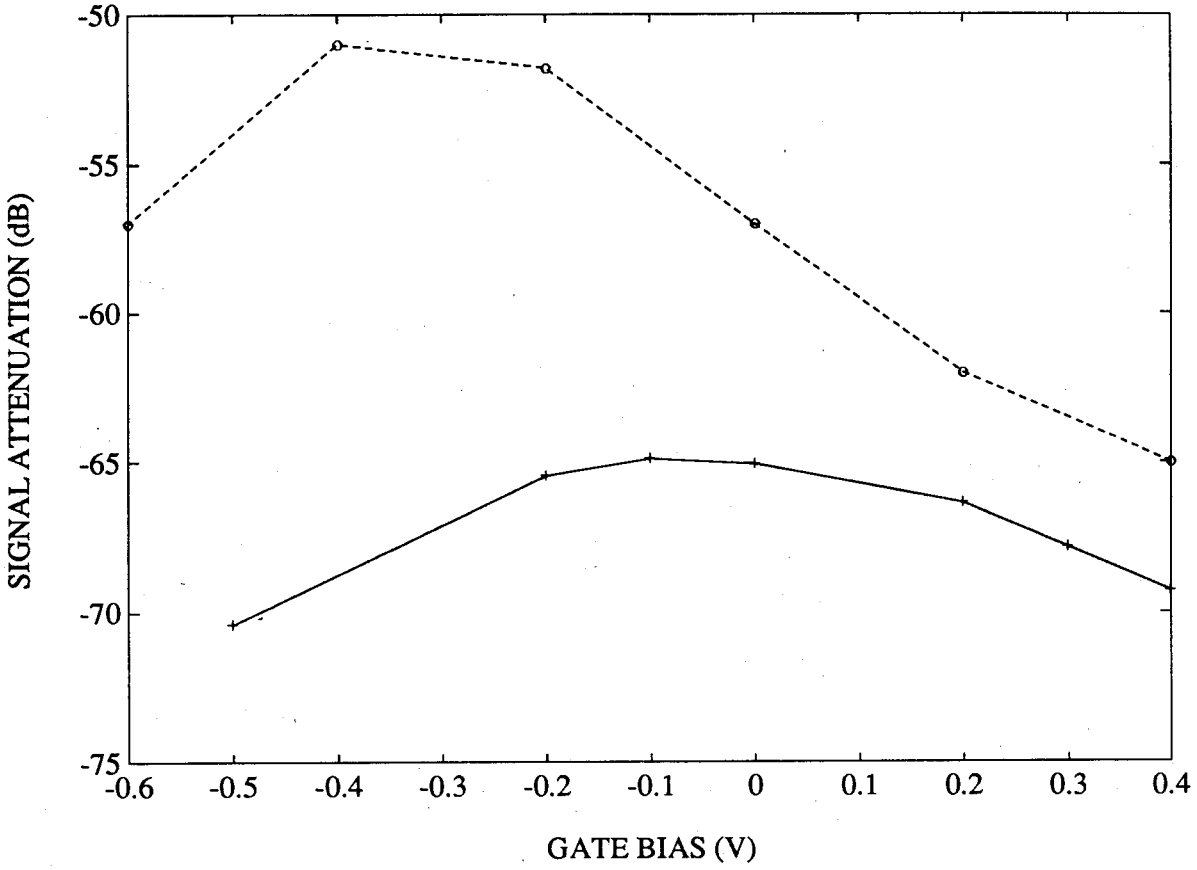


Figure 2.11: Experimental (dashed line) and calculated (solid line) dependences of AC sidegating on the gate bias for a depletion-mode GaAs MESFET operating at $V_{DD} = 0.5V$, $V_{SG} = -3V$, 100kHz. Parameters: $c_b = 15.4$fF, $r_b = 1.1$GΩ, $r_s = 0.06$GΩ, $c_s = 15$fF. Zero bias gate capacitance is 90fF.

the depletion mode transistor operating at large drain-to-source voltage is shown Fig. 2.13. The dependence of sidegating on the drain-to-source voltage is presented in Fig. 2.14. The sidegating exhibits less than 1dB variation over the range of 2-4 volts. AC sidegating as a function of the sidegate bias is shown in Fig. 2.15. The sidegating increases below -3V which corresponds to the threshold voltage in the DC sidegate current-voltage characteristics (see subsection 2.3.2). Finally the sidegating frequency dependence is shown in Fig. 2.16.

2.3.4 Discussion

The assumptions in the above analysis restrict its validity at low frequencies. Surface states associated with gate-source and gate-drain spacings may cause these regions to respond to the variations

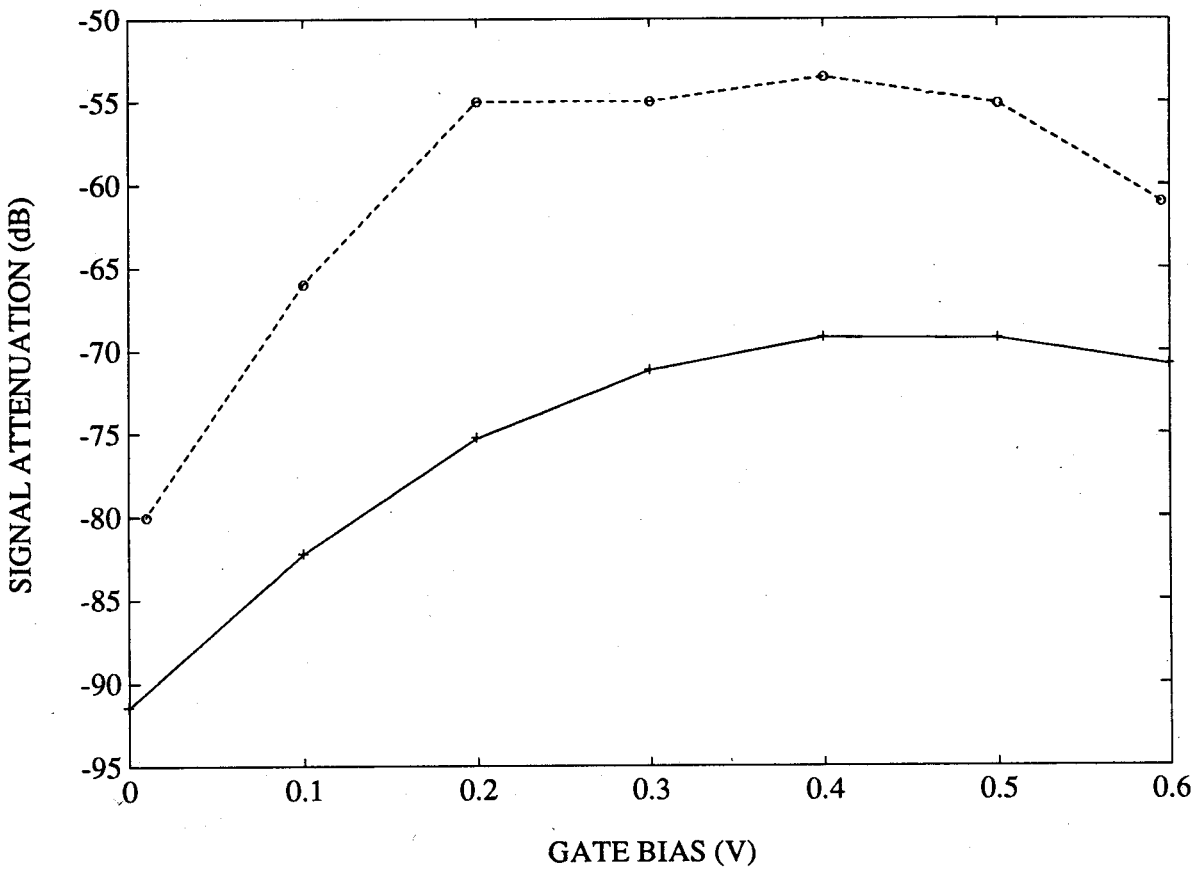


Figure 2.12: Experimental (dashed line) and calculated (solid line) dependences of AC sidegating on the gate bias for a enhancement-mode GaAs MESFET operating at $V_{DD} = 0.5V$, $V_{SG} = -1V$, 100kHz . Parameters: c_b = 17fF, r_b= 2.8GΩ, r_s= 0.15GΩ, c_s = 15fF . Zero bias gate capacitance is 10fF.

in the sidegate potential. A recent analysis of low-frequency dispersion of gate transconductance in GaAs MESFETs, which relates it to the surface states, indicates that it will be important below 1kHz [48]. The frequency response of the sidegating shown in Fig. 2.16 can be roughly divided into two regions. The frequency response below 5kHz is probably controlled by the surface states. The frequency response above 10kHz is due to the capacitive and resistive coupling between the sidegate and the MESFET channel. The present experimental data confirm the theory in that at higher frequencies, in which MESFETs normally operate, the sidegating grows as $w^{1/2}$.

The dependence of the sidegating on the gate bias given by (2.18) originates from the following relation:

$$g_{mb} \sim \sqrt{1/r_{chs}c_{js}} \propto \sqrt{d(a-d)} \tag{2.20}$$

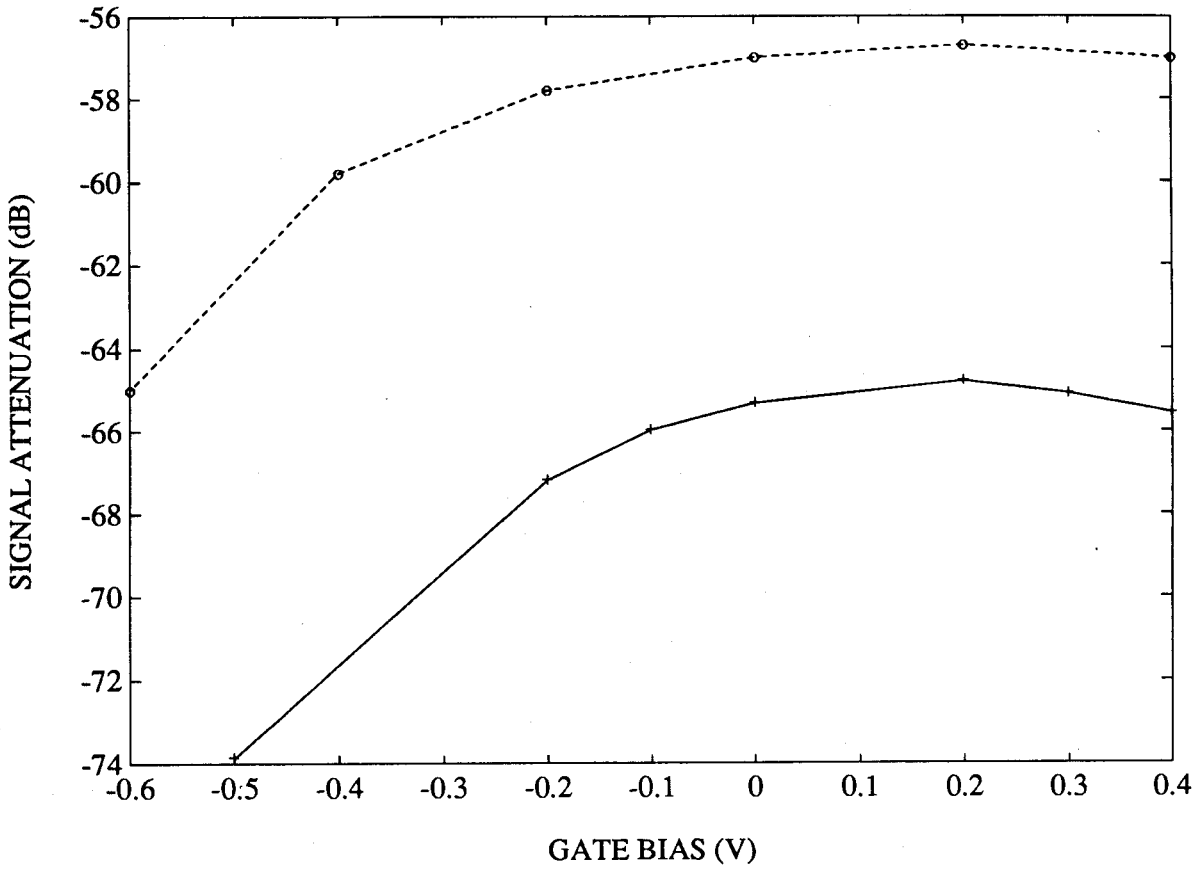


Figure 2.13: Experimental (dashed line) and calculated (solid line) dependences of AC sidegating on the gate bias for a depletion-mode GaAs MESFET at $V_{DD} = 3V$, $V_{SG} = -1V$, 100kHz. Parameters: $c_b = 17\text{fF}$, $r_b = 2.8\text{G}\Omega$, $r_s = 0.15\text{G}\Omega$, $c_s = 15\text{fF}$.

Thus, a parabolic dependence of AC sidegating on gate bias with a maximum at the bias corresponding to a half-depleted channel is expected. Generally, this behavior was indeed observed for MESFETs operating at small drain-source voltage as shown in Fig. 2.11 and 2.12. Sidegating for depletion mode GaAs MESFETs exhibits a maximum as a function of gate potential due to the fact that the conductive layer in these transistors can change drastically in thickness as it goes from a fully open channel to a very thin layer as a result of applying a gate bias and the condition of a half-depleted channel can be reached. The channel in the enhancement mode transistors is already depleted for zero gate bias. This means that the fully open channel can be achieved only at high gate voltages. As a consequence, the gate bias for which maximum sidegating is obtained shifts to higher voltages (see Fig. 2.12). For large drain-to-source voltage the sidegating increases and eventually saturates with gate bias (see Fig.

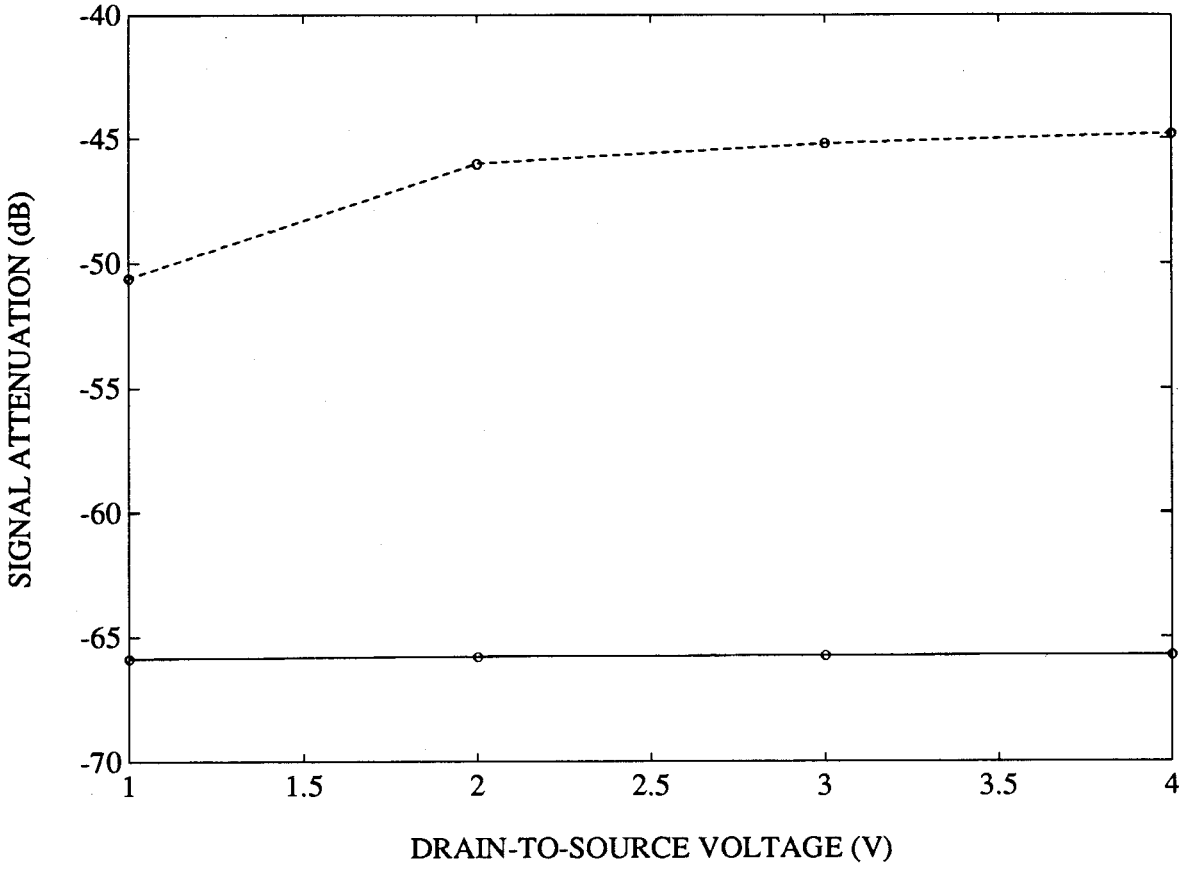


Figure 2.14: Experimental (dashed line) and calculated (solid line) dependences of AC sidegating on the drain-to-source voltage for a depletion-mode GaAs MESFET operating at $V_G = 0V$, $V_{SG} = -2V$, 100kHz. Parameters: $c_b = 16.3\text{fF}$, $r_b = 3.2\text{G}\Omega$, $r_s = 0.17\text{G}\Omega$, $c_s = 15\text{fF}$, $r_{chs} \approx 210\Omega$, $c_{js} \approx 84\text{fF}$.

2.13). The minimal thickness of the gate depletion layer in the high-field region is determined by the drain voltage. This results in a conductive layer that normally is well below half the device thickness for any gate bias. Therefore the sidegating does not exhibit a maximum as a function of gate voltage but rather increases monotonically with it. Our calculated results show good qualitative agreement with data for devices biased far away from pinch-off. This is probably due to the slowly-varying R-C product of the channel under these biasing conditions. At high gate voltages the leakage resistance must be taken into account. At lower gate voltages near pinch-off our calculations indicate lower sidegating, because eqn. (2.19) overestimates the gate capacitance in this region.

Our experimental observations indicate that, when the device is biased near pinch-off, AC sidegating diminishes drastically in magnitude and is often accompanied by oscillations which makes

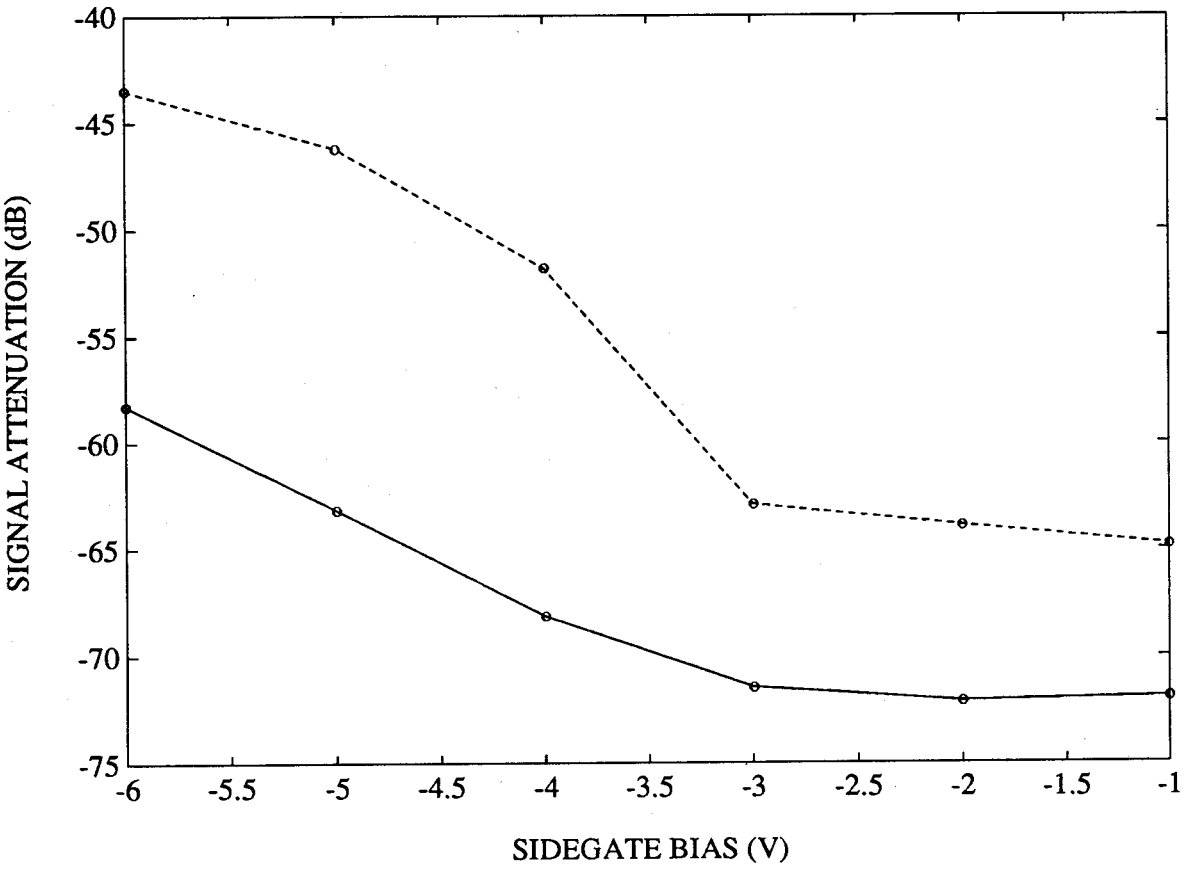


Figure 2.15: Experimental (dashed line) and calculated (solid line) dependences of AC sidegating on the sidegate bias for a depletion-mode GaAs MESFET operating at $V_G = 0V$, $V_{DD} = 0.5V$, 10kHz . Parameters: $r_{chs} = 175\Omega$, $c_{js} = 90\text{fF}$, $c_s = 15\text{fF}$.

it very difficult to perform accurate measurements. This abrupt decrease in sidegating is due to a very larger $r_{chs}c_{js}$ product. Lehovec and Zuleeg [49] evaluated the R-C product of the channel near the pinch-off region. They suggested that its large value is due to very low mobilities of electrons at the channel-substrate interface caused by extensive trapping. Therefore the channel resistance will be determined mostly by the properties of the semi-insulating substrate. The observed low-frequency oscillations are supporting evidence for this interpretation since they have been observed in semi-insulating GaAs [50].

The sidegating depends on drain-to-source voltages only by way of channel-length modulation. Therefore, the sidegating in the saturation region, will not be too sensitive to the variations in drain-to-source voltage as indeed was observed in the experimental results shown in Fig. 2.14.

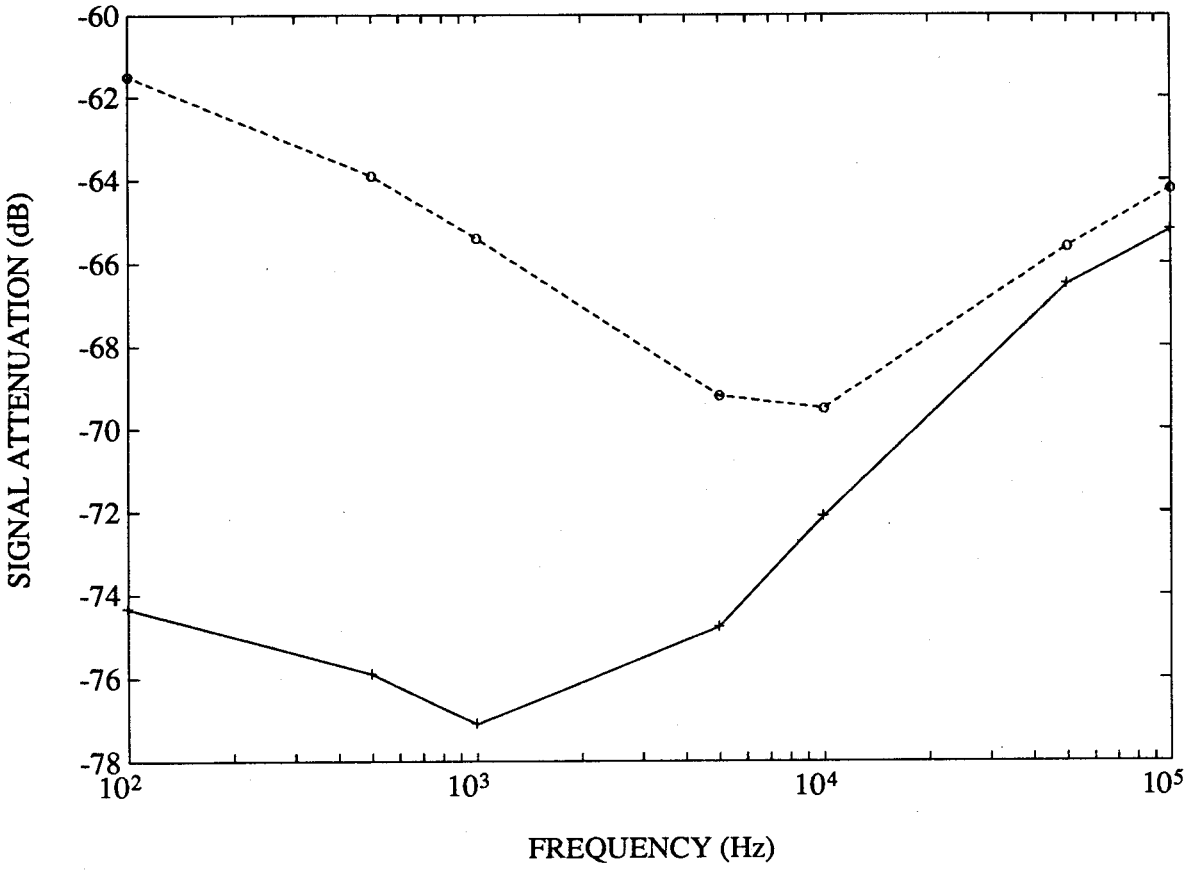


Figure 2.16: Experimental (dashed line) and calculated (solid line) frequency dependence of sidegating for depletion-mode GaAs MESFET operating at $V_G = 0V$, $V_{DD} = 0.5V$, $V_{SG} = -1V$. Parameters: $r_{chs} = 175\Omega$, $c_{js} = 90\text{fF}$, $c_b = 17\text{fF}$, $r_b = 2.8\text{G}\Omega$, $r_s = 0.15\text{G}\Omega$, $c_s = 15\text{fF}$.

Fig. 2.15 shows a strong dependence of AC sidegating on sidegate voltages between -3 and -6 volts. These experimental observations are in qualitative agreement with the modeling results which predict that as the negative sidegate bias increases in magnitude the substrate resistance diminishes, thus increasing the sidegating intensity. The abrupt change in the sidegating as a result of applying a sidegate voltage below -3V has been taken as indicating the possibility of the injection current conduction in the semi-insulating substrate. However, r_s is not the only parameter that relates the sidegating to the sidegate bias: c_b which represents the the space charge region at the channel-substrate interface may play a significant role in determining AC sidegating. When the sidegate voltage increases in magnitude more and more electrons are injected into the substrate. Due to the injection effects the channel-substrate capacitance will be probably higher than that evaluated in

this work. This could explain the large discrepancy between the calculated results and the data at high sidegate voltages. The network parameters r_s and c_b are expected to be frequency dependent. The substrate resistance is expected to be smaller at higher frequencies for short distances between MESFET and sidegate [40]. The capacitance is expected to be larger at low frequencies because of the finite time constant associated with the charging and discharging of the traps in semi-insulating material [51].

In conclusion, distributed network analysis has been applied to the interpretation of the sidegating effect in GaAs MESFETs. Analytic expressions for the sidegating were derived and using a simple model were related to the bias voltages. Results presented in Fig. 2.15 show that AC conduction through the substrate plays an important role in determining the sidegating. The accuracy of the present model could be increased by retaining the same equivalent circuit but using more sophisticated models for the network parameters. The experimental data presented in this thesis agree qualitatively with the sidegating model expressed as a function of the frequency and bias voltages. The sidegating for the MESFET operating in the saturation region will not be sensitive to the variations in the drain-to-source voltage. The main conclusion which can be drawn from this work is that the sidegating effect can be reduced by applying the lowest possible gate bias to MESFET or in other words, by operating the device at low current.

2.4 Summary

The mechanisms of crosstalk in *n-SI-n* GaAs structures were investigated over a frequency range of 100Hz-500MHz. The sidegating mechanism was found to be dependent on the frequency and on the distance between the sidegate and the output contacts. The crosstalk can be represented as a parallel RC network, where the capacitance is associated with the interaction of fringing fields around the input and output electrodes.

For shorter distances the resistive component represents a conductive path through the semi-insulating GaAs substrate normally associated with the trap-filled space-charge-limited current. In general the resistance will be bias-dependent. Furthermore, it is expected to be frequency-dependent

because of the finite time constant associated with the charging and discharging of the traps in semi-insulating GaAs.

For longer distances the capacitive coupling is reduced. Also a higher biasing voltage is required in order to initiate the space-charge-limited current for the distant input and output contacts. Thus at low voltages the resistive component is associated with the ohmic leakage current through the substrate. This resistance exhibits a frequency dependent conductivity, which is a result of potential fluctuations in the compensated semiconductor.

At low frequencies the capacitive coupling is reduced and the resistive coupling tends to prevail. At high enough frequencies capacitive coupling dominates disregarding the distance between the input and output electrodes.

The bias and frequency dependence of AC sidegating in GaAs MESFETs was modeled using a distributed R-C network. The resultant analytic expression for the sidegate transconductance was compared with experimental results over the range of 100Hz - 100kHz. They agreed in that the sidegating at small drain-to-source voltage exhibits a maximum as a function of gate bias, while at large drain-to-source voltage the sidegating increases and eventually saturates with gate voltage, and is not sensitive to drain-to-source voltage. The present experimental measurements show that AC sidegating (like DC) is greatly enhanced after a negatively biased sidegate reaches a threshold. Both experimental data and the model show that AC sidegating increases approximately as $w^{1/2}$ at high frequencies.

Chapter 3

The role of minority carriers in the sidegating effect

3.1 Introduction

A field-effect transistor has been always a synonym to a unipolar transistor in the literature [52, 53]. This is not surprising, considering the nature of contacts, that constitute a MESFET: source and drain are ohmic contacts and therefore are unable to inject holes, and Schottky contacts practically do not inject holes according to the early studies by Scharfetter [54] and Yu and Snow [55]. We, however, show in this chapter that the gate of a MESFET can inject holes and this results in parasitic effects that severely degrade the MESFET performance.

In Section 3.2 we investigate sidegating under conditions of low-level injection, for which the excess free holes and electrons are much less than equilibrium hole and electron concentrations respectively. Without further assumptions we solve analytically continuity equations for holes and electrons plus Poisson's equation. The results show that the presence of recombination centers in the SI substrate and even weak hole injection from the gate significantly enhance sidegating. In Section 3.3 we propose a mesurement technique to evaluate this hole injection, and our experimental results confirm the participation of holes in sidegating. In Section 3.4 our analysis deals mainly with high-level hole injection and we discuss hysteresis in current-voltage characteristics, geometrical effects and process-related issues in sidegating as a result of hole injection.

3.2 Sidegating effect under conditions of low-level injection

3.2.1 Introduction

Weak sidegating has been observed for small sidegate voltages and currents by many researchers, e.g. [8]. In spite of the insulating substrate the sidegate acts as if it were close to the MESFET channel, suggesting that there is a mechanism which transfers the applied voltage to the vicinity of MESFET.

Most research has concentrated on strong sidegating accompanied by high-level electron injection into the substrates and predicting the magnitude of a threshold voltage, at which a sharp decrease in the drain current occurs [22, 56]. In this chapter an analysis of weak sidegating is given, which occurs below the threshold voltage. In this range of voltage only low-level injection occurs i.e. the injected densities of free carriers are much less than the equilibrium free carrier densities. While the restrictions on the concentration of injected minority carriers are harsh in the case of an extrinsic semiconductor, they are less severe for SI GaAs in which the equilibrium carrier densities of electrons and holes are not very different from each other. The low-injection regime is valid up to the voltage at which a deviation from ohmic behavior occurs. For material with deep traps, the threshold is the traps-filled-limit voltage or the voltage, at which negative resistance appears[7]. This threshold depends on material properties such as trap densities and distribution, minority carrier lifetime, and homogeneity of the substrate. The threshold voltage could be measured and provided to circuit designers as a designation of the "disaster" area, similar to providing maximum operating drain voltages. The modeling of the low-injection region is more relevant to them, since it occurs in the operating region of transistors. The results of the analysis are provided with flexible boundary conditions, which allow the investigation of a variety of physical situations.

3.2.2 Sidegating model

Many numerical studies of isolation in GaAs integrated circuits, performed on symmetrical *n-i-n* structures, have been published recently[22, 57, 56]. Some of the studies deal with transport equations for majority carriers only, e.g. [56], while others provide more general analysis, but assume restrictive boundary conditions such as ohmic contacts at the edges of the structure [22].

These studies do not consider the interaction between gate and sidegate. Our measurements shown in Fig. 3.17 and experimental data by other researchers [58] indicate interaction between gate current and sidegate voltage. The gate current consists of the saturation current of a Schottky diode and the current to a sidegate. Since the saturation current is small, changes in the gate current upon applying sidegate voltage can be easily observed. In Fig. 3.17 the gate current is negative for sidegate

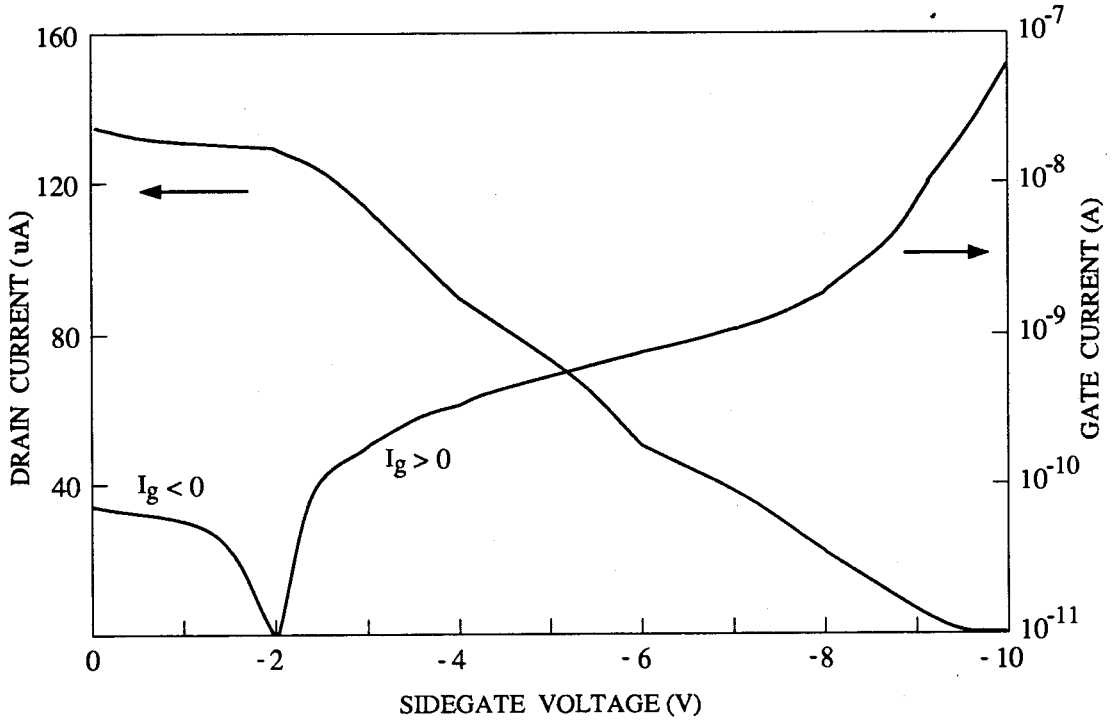


Figure 3.17: Typical drain and gate currents as a function of sidegate voltage ($V_D = 2\,V, V_G = 0\,V$). The measurements were performed in the dark on depletion-mode MESFETs fabricated by ion implantation into a SI substrate. The typical threshold voltage was $-0.6\,V$. The gate length was 1μm and width 4μm. The gate-source and gate-drain distances were 2μm. The ohmic contact of the adjacent MESFET, which served as a sidegate in our measurements, was placed parallel to the source at a distance of 8μm and was 23μm from the gate.

voltage between 0 and $-2\,V$ and it is positive for sidegate voltages more negative than $-2\,V$. Also noteworthy is a rapid increase in the gate current when the MESFET is almost pinched off.

High Schottky barriers in MESFETs are beneficial, because they increase the noise margin in GaAs digital integrated circuits. But high barriers create an inversion layer beneath the gate, which may inject holes under forward bias conditions, although there is some controversy regarding the magnitude of hole injection[59]. Thus *n-i-n* structures, in which hole injection is negligible, represent only one particular case of channel-substrate interaction. These structures may represent the conductive path from sidegate to drain and source, but not necessarily that from sidegate to channel.

The channel region of the MESFET is sandwiched between two closely spaced depletion regions, which are associated with the Schottky barrier and the channel-substrate interface. Since the Schottky depletion region is thin, the study of hole injection from the gate should be based on thermionic

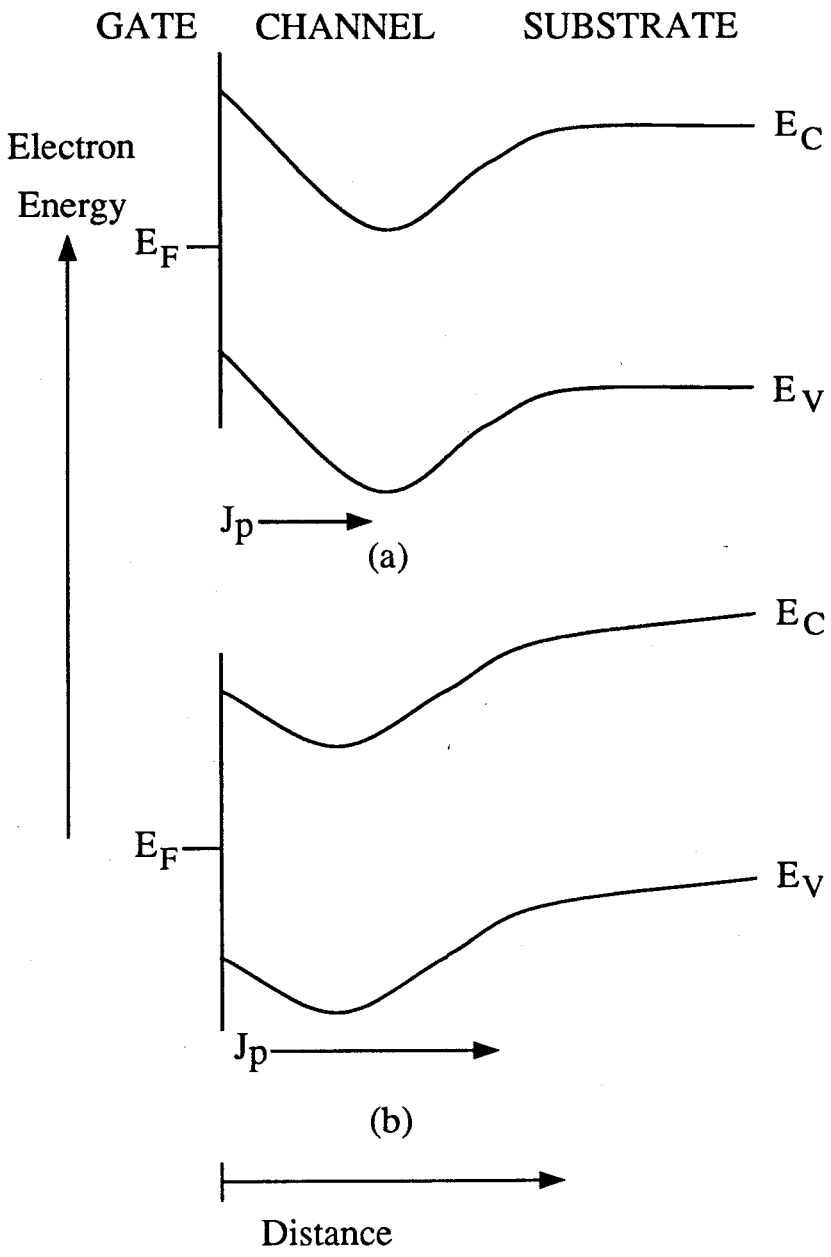


Figure 3.18: Hole injection from Schottky gate. (a) For a small sidegate voltage. (b) For a large sidegate voltage.

emission theory[60]. Figure 3.18(a) depicts the situation for a small sidegate voltage, when the channel is not depleted and a negligible hole current is expected. The drain current decreases upon applying a negative voltage to a sidegate. Larger negative voltages cause a reach-through depletion of the channel as shown in Fig. 3.18(b). A situation similar to reach-through has been analyzed by Wager and McCamant [61], who showed using thermionic emission theory that the hole current can

greatly exceed the electron current. We suggest that the sidegating is accompanied by an increase in hole current at the gate. By applying a negative voltage to the sidegate the conductive part of the channel shrinks, allowing more holes to reach the substrate. As we shall see in the next section the hole injection creates a field overshoot causing a high voltage drop in the vicinity of the channel-substrate interface. Consequently, most of the additional applied voltage will drop near this region causing an even stronger depletion of the channel. This will lower the hole injection barrier allowing for many more holes to be injected. Thus this process is self-supporting and for high enough voltages will result in a reach-through depletion of the channel and a rapid increase in the gate (hole) current.

An additional source of holes is the avalanche process due to high drain voltage. Electron-hole pairs are generated in the channel. The holes are attracted to the substrate due to an assisting field at the channel-substrate interface, while the electrons "see" an energy barrier of approximately half the band-gap.

3.2.3 Detailed analysis

An analytical study of the potential distribution in SI substrates has been made by Ohno and Goto [62]. Their analysis was based on the assumption of local space-charge neutrality, but we report an analysis free of this assumption. Manifacier and Henisch have investigated minority-carrier injection into semiconductors with and without traps by solving linearized transport equations[63, 64, 41]. Their detailed analysis was applied mainly to semi-infinite and *long* structures. We have extended the analysis of Manifacier and Henisch by incorporating both recombination centers and traps into Poisson's equation. We report a closed form for the space-charge, electric field and potential distribution in SI *short* structures.

The schematic equilibrium band diagram of the structure analyzed in this paper is shown in Fig. 3.19. The sidegate n^+ region is assumed to inject only electrons, while the other contact is assigned a variable injection ratio η. Additional boundary conditions, which simplify the solution, are zero field at $x = 0$ and $x = L$ [41]. Because of short carrier lifetimes in SI GaAs and distances between MESFETs in integrated circuits, which are typically long in comparison to diffusion length, recombination must be considered. Even though GaAs is a direct band-gap material, the presence

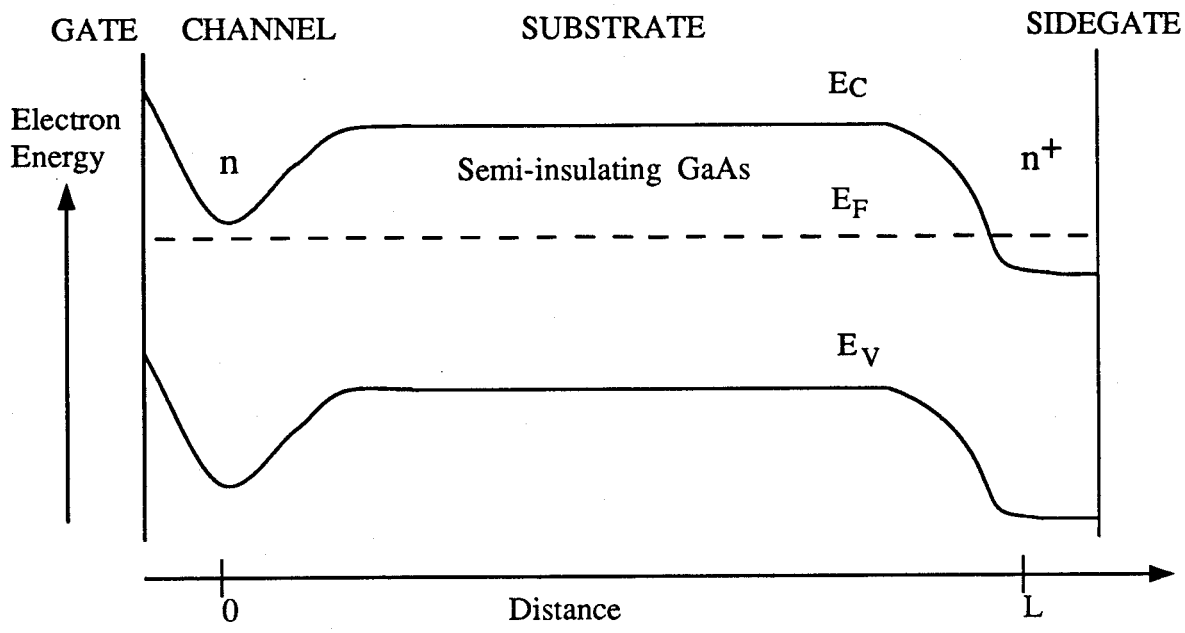


Figure 3.19: Schematic band diagram of the gate-sidegate structure in equilibrium.

of a high density of deep levels in this material dominates the recombination process[65]. The insulating properties of the GaAs substrate are based on the balance between shallow donors and acceptors, and deep levels. The mid-gap deep donor EL2 with a concentration of about $10^{16}\,cm^{-3}$ plays an dominant role in the compensation mechanism[26]. Nevertheless EL2 acts as a trap rather than a recombination center because of its small hole capture cross section. SI GaAs may contain high densities of deep acceptors in addition to EL2[66, 67]. Wong *et al.* have proposed some of them as recombination centers with an estimated concentration of at least $5 \times 10^{15}\,cm^{-3}$[68]. Any general discussion of transport in semi-insulating GaAs should include a dominant recombination center in addition to EL2. Under conditions of low-level injection the recombination rate determined by Shockley-Read-Hall model is given by [41]:

$$U = \frac{p_e \delta n + n_e \delta p}{\tau(p_e + n_e)} \tag{3.21}$$

where $\delta n, \delta p$ are excess free electrons and holes, n_e, p_e are equilibrium electron and hole concentrations, and τ is the lifetime. The linearized current density and continuity equations can be written as[63, 64]

$$J_n = \frac{b}{1 + P_e}\left(E + \frac{d\delta N}{dX}\right) \tag{3.22}$$

$$J_p = \frac{1}{1+P_e}\left(P_e E - \frac{d\delta P}{dX}\right) \tag{3.23}$$

$$\frac{d^2\delta N}{dX^2} + \frac{dE}{dX} - \frac{A_n}{1+P_e}(P_e\delta N + \delta P) = 0 \tag{3.24}$$

$$\frac{d^2\delta P}{dX^2} - P_e\frac{dE}{dX} - \frac{A_n b}{1+P_e}(P_e\delta N + \delta P) = 0 \tag{3.25}$$

with

$$A_n = \epsilon/q\mu_n\tau(n_e + p_e), \tag{3.26}$$

where q is the magnitude of the electronic charge, μ_n is electron mobility, ϵ is the dielectric constant, and b is ratio of electron to hole mobility. The parameters $\delta N, \delta P$ and P_e represent excess free carriers and equilibrium hole concentration respectively, normalized to the equilibrium electron concentration. The field is normalized to kT/qL_D, the current density to $\mu_p kT(n_e + p_e)/L_D$ and $X = x/L_D$, where

$$L_D = \sqrt{[\epsilon kT/q^2(n_e + p_e)]}\,. \tag{3.27}$$

Poisson's equation can be written for the general case of non-interacting multiple traps. The concentration of the i^{th} trap occupied by electrons under steady-state condition is given by[69]

$$q_t^i = \frac{N_t^i(c_n^i n + e_p^i)}{c_n^i n + e_n^i + c_p^i p + e_p^i} \tag{3.28}$$

where N_t^i is the i^{th} trap density, e_n^i, e_p^i are its emission rates for electrons and holes,c_n^i, c_p^i are the capture probabilities for electrons and holes, and n, p are electron and hole concentrations. In equilibrium the occupied density of the i^{th} trap is given by

$$q_{te}^i = \frac{n_e}{n_e + n_i^i} \tag{3.29}$$

where n_e is equilibrium electron concentration, and n_i^i is electron density if the Fermi level were at the energy level of the i^{th} trap. The excess trapped carrier density is

$$\sum_i \delta q_t^i = \sum_i (q_{te}^i - q_t^i). \tag{3.30}$$

It can be expressed under low-level injection as

$$\sum_i \delta q_t^i = \alpha \delta p - \beta \delta n \,, \tag{3.31}$$

with

$$\alpha = \sum_i \frac{N_t^i c_p^i n_e}{\left(n_t^i + n_e\right)\left(e_n^i + c_n^i n_e + e_p^i + c_p^i p_e\right)} \,, \tag{3.32}$$

$$\beta = \sum_i \frac{N_t^i e_n^i}{\left(n_t^i + n_e\right)\left(e_n^i + c_n^i n_e + e_p^i + c_p^i p_e\right)} \,. \tag{3.33}$$

In this work we consider only EL2 and a dominant recombination center. The Poisson equation is modified to include these two traps:

$$\frac{dE}{dX} = \frac{1}{1+P_e}\left(\delta P - \delta N + \delta Q_t^1 + \delta Q_t^2\right) \tag{3.34}$$

where $\delta Q_t^1, \delta Q_t^2$ are the concentrations correspondingly of the deep traps (EL2) and recombination centers occupied by electrons and normalized to the equilibrium electron density. Carrier concentration, field, and potential profiles are obtained from eqs. (3.22)-(3.25), and (3.34):

$$\begin{aligned} \delta N(X) = \lambda[&\frac{M\cosh\left(X\sqrt{\nu}\right) - R\cosh\left((L-X)\sqrt{\nu}\right)}{\sqrt{\nu}\sinh\left(L\sqrt{\nu}\right)} \\ &+ \frac{P_e\cosh\left(X\sqrt{\xi}\right) + K\cosh\left((L-X)\sqrt{\xi}\right)}{\xi\sinh\left(L\sqrt{\xi}\right)}] \end{aligned} \tag{3.35}$$

$$\begin{aligned} \delta P(X) = \lambda[&M\frac{P_e\cosh\left(X\sqrt{\xi}\right) + K\cosh\left((L-X)\sqrt{\xi}\right)}{\sqrt{\xi}\sinh\left(L\sqrt{\xi}\right)} \\ &- P_e\frac{M\cosh\left(X\sqrt{\nu}\right) - R\cosh\left((L-X)\sqrt{\nu}\right)}{\sqrt{\nu}sinh(L\sqrt{\nu})}] \end{aligned} \tag{3.36}$$

$$\begin{aligned} E(X) = \lambda\{&\frac{(1+\beta) - M(1+\alpha)}{A_n(P_e+b)}[\frac{P_e\sinh\left(X\sqrt{\xi}\right) - K\sinh\left((L-X)\sqrt{\xi}\right)}{\sinh\left(L\sqrt{\xi}\right)} + K] \\ &+ \frac{M\sinh\left(X\sqrt{\nu}\right) + R\sinh\left((L-X)\sqrt{\nu}\right)}{\sinh\left(L\sqrt{\nu}\right)} - R\} \end{aligned} \tag{3.37}$$

$$\begin{aligned} V(X) = \lambda\{&\frac{(1+\alpha)M - (1+\beta)}{A_n(P_e+b)} \\ \times[&\frac{P_e\left(\cosh\left(X\sqrt{\xi}\right) - 1\right) + K\left[\cosh\left((L-X)\sqrt{\xi}\right) - \cosh\left(L\sqrt{\xi}\right)\right]}{\sqrt{\xi}\sinh\left(L\sqrt{\xi}\right)} + KX] \\ -&\frac{M(\cosh\left(X\sqrt{\nu}\right) - 1) - R[\cosh\left((L-X)\sqrt{\nu}\right) - \cosh\left(L\sqrt{\nu}\right)]}{\sqrt{\nu}\sinh\left(L\sqrt{\nu}\right)} + RX\} \end{aligned} \tag{3.38}$$

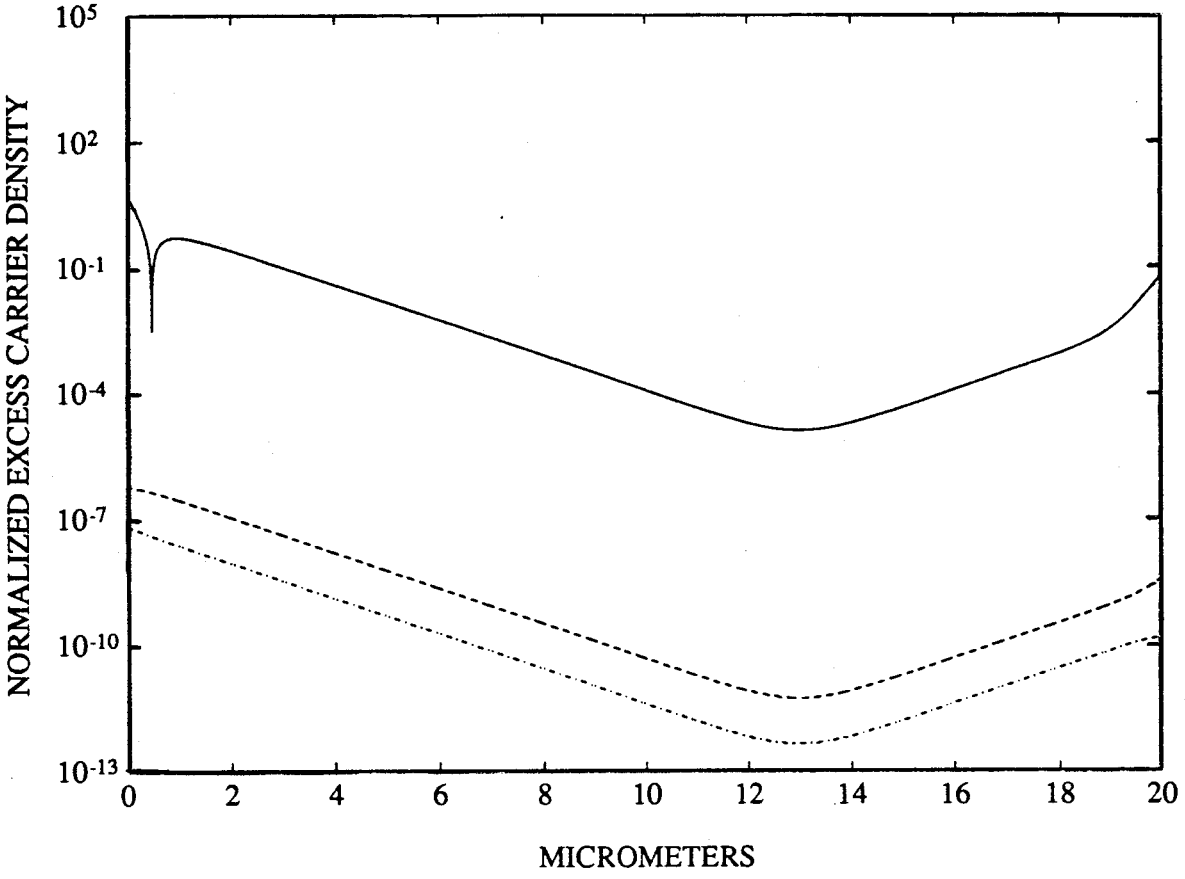


Figure 3.20: Concentration profile of trapped and free excess carriers in the 20μm long model structure. The solid line corresponds to trapped carriers, dashed line to electrons, and dashdots to holes. The carrier densities are normalized to the equilibrium electron concentration The sidegate voltage is -5V, the equilibrium electron concentration is $\approx 7 \times 10^6\, cm^{-3}$, the equilibrium hole concentration is $\approx 2 \times 10^5\, cm^{-3}$, the electron mobility is $4 \times 10^3\, cm^2/Vsec$, the hole mobility is $400\, cm^2/Vsec$, and the lifetime is $1\, nsec$. EL2 is assumed to be 0.75eV from the conduction band, its density $10^{16}\, cm^{-3}$, and the ratio of its capture cross sections for holes and electrons 10^{-3}. The recombination center is assumed to be 0.65eV from the conduction band, with density $10^{15}\, cm^{-3}$, and the ratio of its capture cross sections 100.

with $\nu = [P_e(1+\alpha)+(1+\beta)]/(1+P_e)$, $\xi = A_n(P_e+1)/(1+P_e)$, $K = \eta(b+P_e) - P_e$, $M = (1+\beta-A_n b)/(1+\alpha-A_n)$, $R = \eta(b-M)+M$, $\lambda = J(1+P_e)/b(M+P_e)$. The zero potential reference point is taken at x=0 (see Fig. 3.19). The parameter λ is determined by the applied voltage at x=L.

Fig. 3.20 shows the distribution of trapped and free carrier concentrations throughout the structure with typical trap densities in SI GaAs $\left(N_{t1} = 10^{16}\, cm^{-3}, N_{t2} = 10^{15}\, cm^{-3}\right)$ and for an applied voltage of $-5\, V$. The MESFET was assumed to inject holes only. The results shown on Fig.

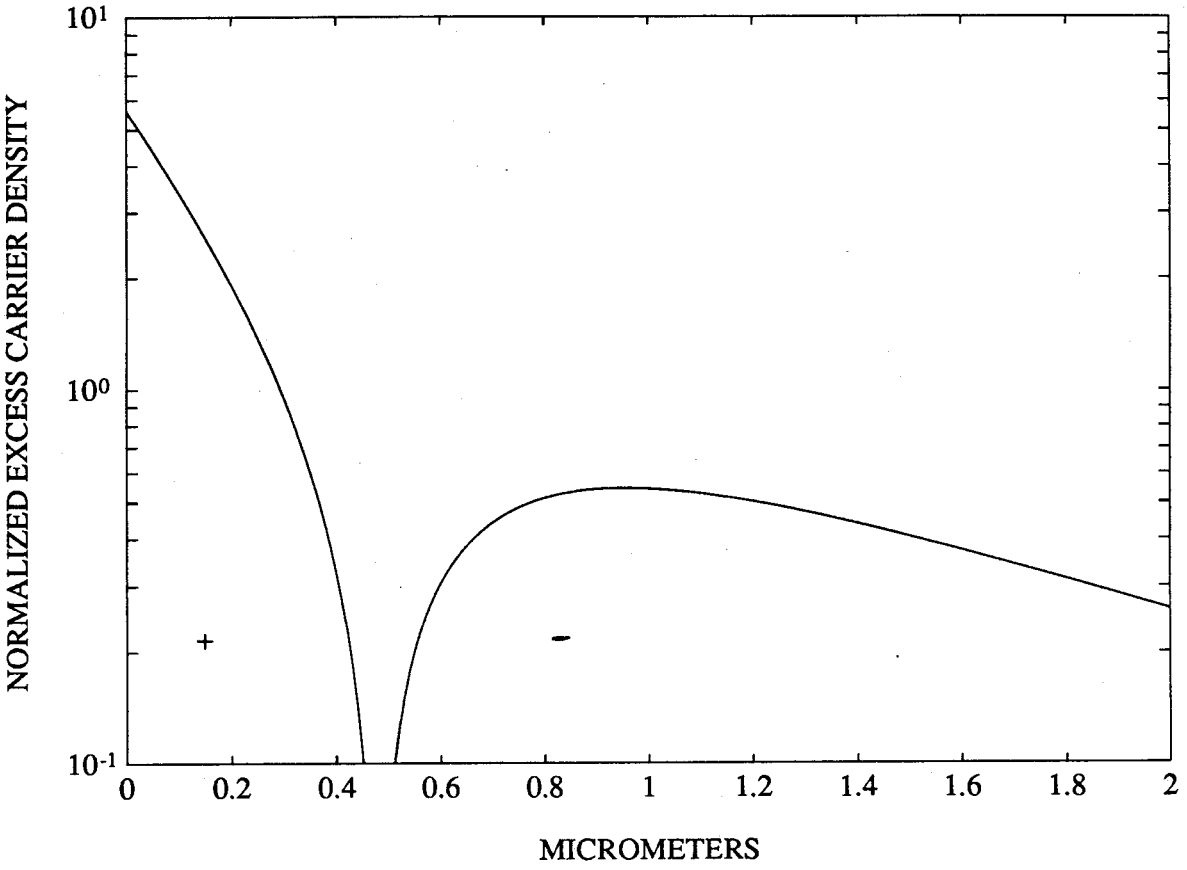


Figure 3.21: Concentration profile of trapped excess carriers as in Fig. 3.20, but only in the vicinity of hole injecting edge (x=0). The charge profile changes polarity at around 0.4μm.

3.20 indicate that the *local* space-charge neutrality is not preserved at any point along the structure. The investigated structure (see Fig. 3.18) represents only part of the two-terminal system, which is confined between two zero-field points. This means that the total excess charge in the structure is zero. Thus the *total* space-charge neutrality in the structure is preserved, even though *local* is not. Excess free carrier densities in the structure are below carrier equilibrium values in agreement with conditions of low-level injection. The densities of excess free carriers are far below the trapped carrier density, which means that only the trapped carriers need be considered in the Poisson's equation.

Fig. 3.21 presents a more detailed picture of the trapped carrier concentration in the vicinity of the hole injecting edge. The trapped charge is positive in the very narrow region adjacent to the edge, but is negative throughout rest of the structure. This is a reason for an electric field overshoot

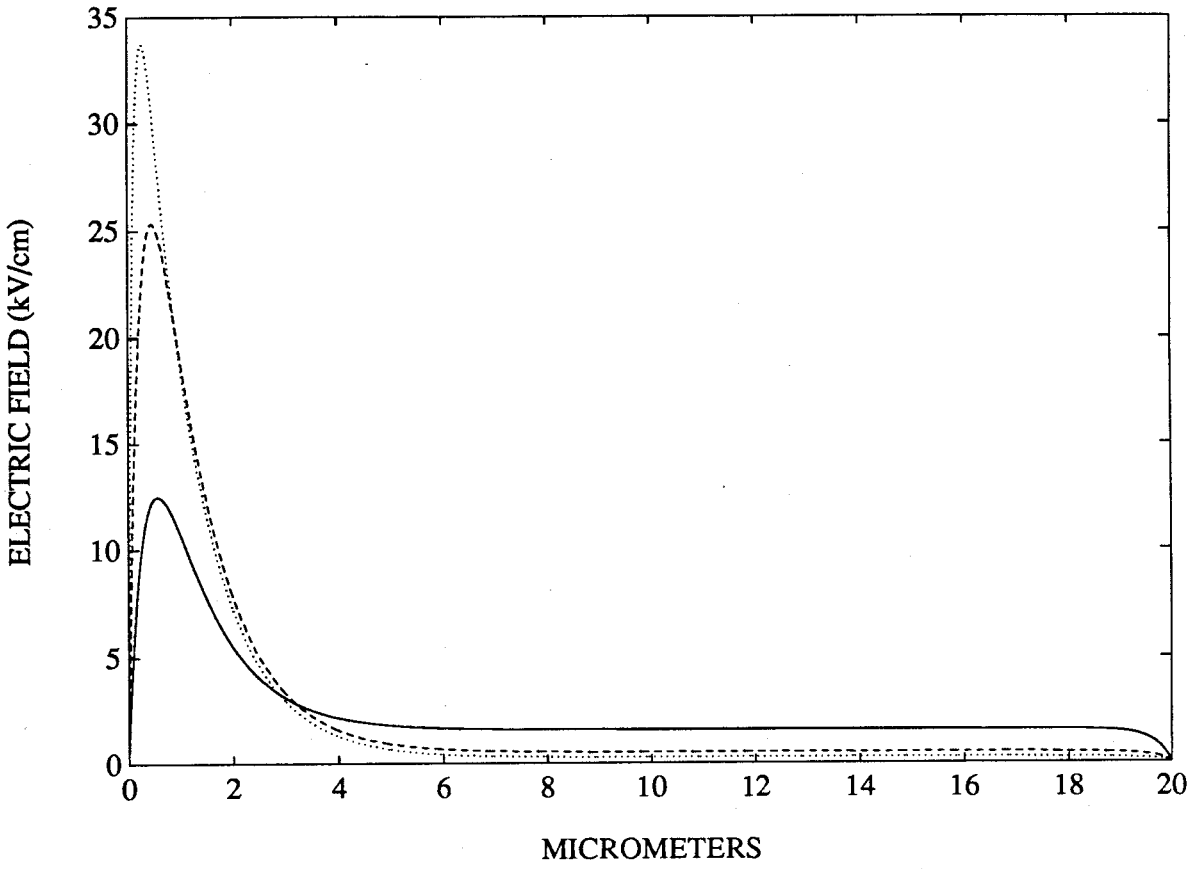


Figure 3.22: Electric field profile in the investigated structure with the same parameters as in Fig. 3.20, but for different densities of recombination centers: dots correspond to $10^{16}\,cm^{-3}$, dashed line to $10^{15}\,cm^{-3}$, and solid line to $10^{14}\,cm^{-3}$.

at about $0.4\,\mu m$ from the edge as shown in Fig. 3.22. This figure also illustrates the effect of the concentration of recombination centers on the field profile, while keeping the EL2 trap density fixed at $10^{16}\,cm^{-3}$. Reduction of the recombination center density results in a decrease of the field overshoot. In the remaining portions of the structure the electric field is far below the value anticipated for the case of ohmic conduction ($5V/20\mu m = 2.5kV/cm$). Fig. 3.22 shows that for material with a high density of traps most of the applied voltage drops across the region adjacent to the hole injecting edge, as expected from the presence of the field overshoot depicted in Fig. 3.23.

The effect of hole injection on the field and potential profiles is shown in Fig. 3.24 and 3.25 respectively. Hole injection increases the field overshoot and creates a non-uniform voltage distribution across the structure.

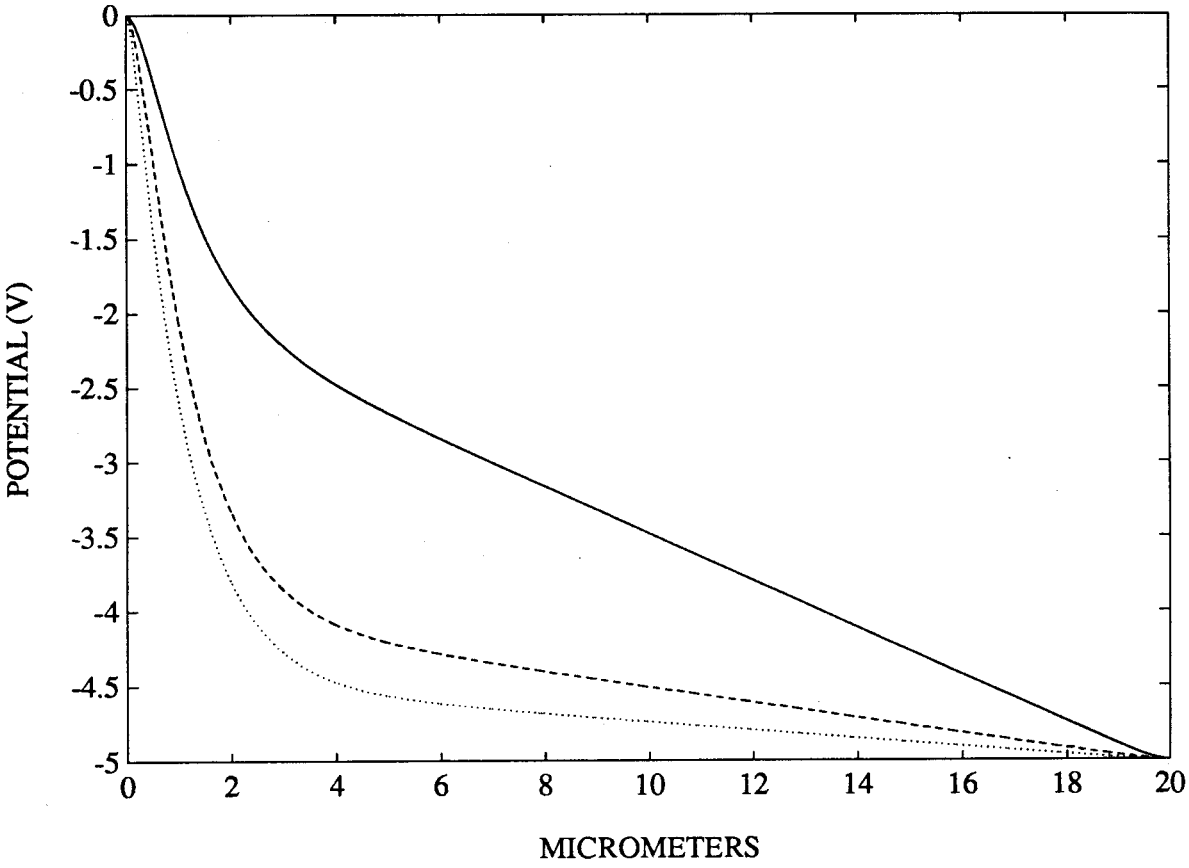


Figure 3.23: Potential profile corresponding to the conditions described in Fig. 3.22.

3.2.4 Discussion

Our analysis indicates that the availability of recombination centers and hole injection in the substrate significantly increase the voltage drop in the vicinity of the channel-substrate interface, which in turn may modulate the carrier concentration in the channel or in other words cause sidegating. While the presence of a high density of recombination centers is confirmed by experimental data [68], there are not many studies on hole injection into a SI substrate. As was mentioned, the existence of the inversion layer beneath the gate due to the high Schottky barrier makes hole injection from the gate into the channel possible. Scharfetter has shown that the minority carrier injection in Schottky diodes is negligible because of the small voltage drop across the neutral part of the Schottky diode over a wide range of currents [54]. He, however, considered epitaxial diodes which were long in comparison to the channel thickness of about $0.1 - 0.2\,\mu m$ in modern GaAs MESFETs. Furthermore,

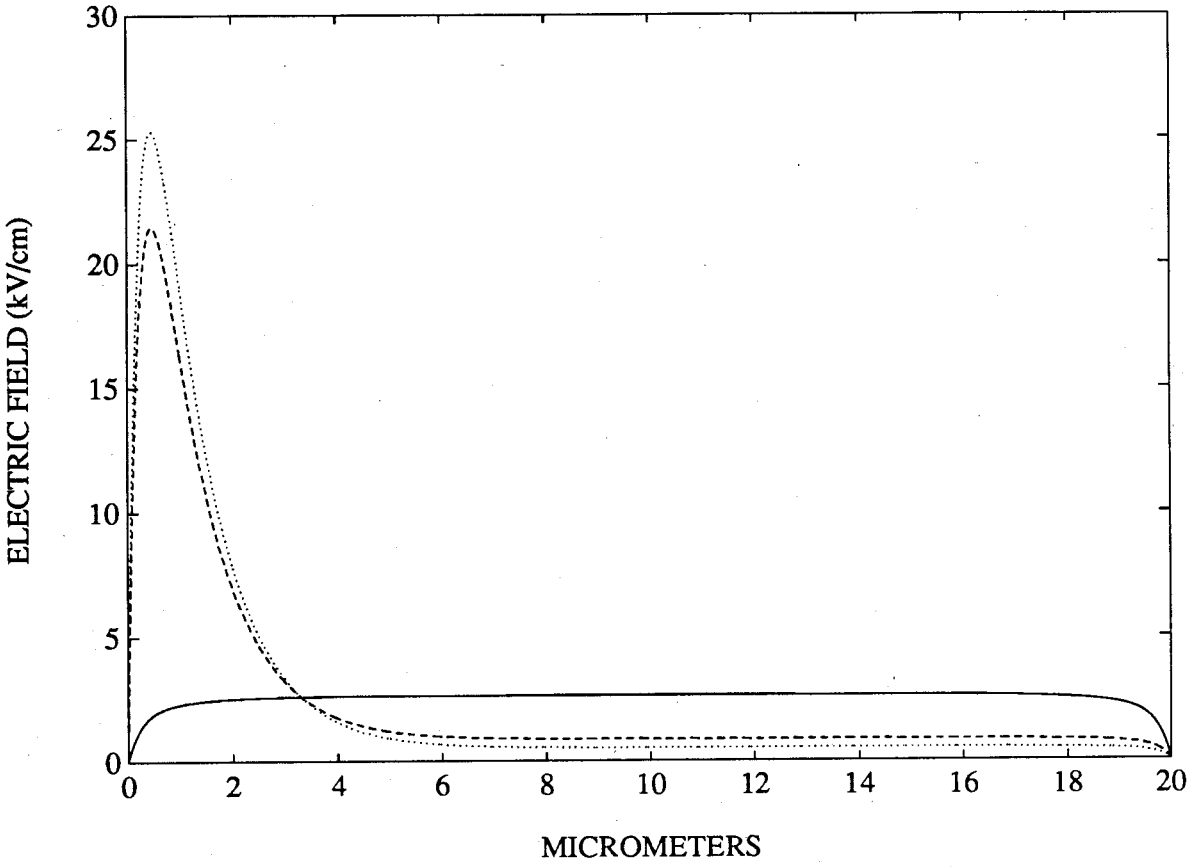


Figure 3.24: Electric field profile in the investigated structure with the same parameters as in Fig. 3.20, but for different values of the minority carrier injection (η): dots correspond to η=1, dashed line to 0.5, and solid line to 0.

most MESFETs are fabricated by ion implantation, which creates a non-uniform impurity profile and consequently a built-in field. This field will assist holes to move into the SI substrate, while impeding electrons.

Zero field is assumed at the edges of the structure, which implies no space-charge in the structure in equilibrium (zero current). But the edges are located at the junctions between doped and SI regions, which exhibit a built-in field and space-charge. Although our analytic results are thus not valid in equilibrium, with structures some tens of micrometers long, only a small error is introduced in the overall potential profiles under non-equilibrium conditions. This is because of a small voltage drop across the heavily doped regions. The depletion region into the channel is small and the zero-field point at the edge of this region will not be far away from the channel-substrate interface. With

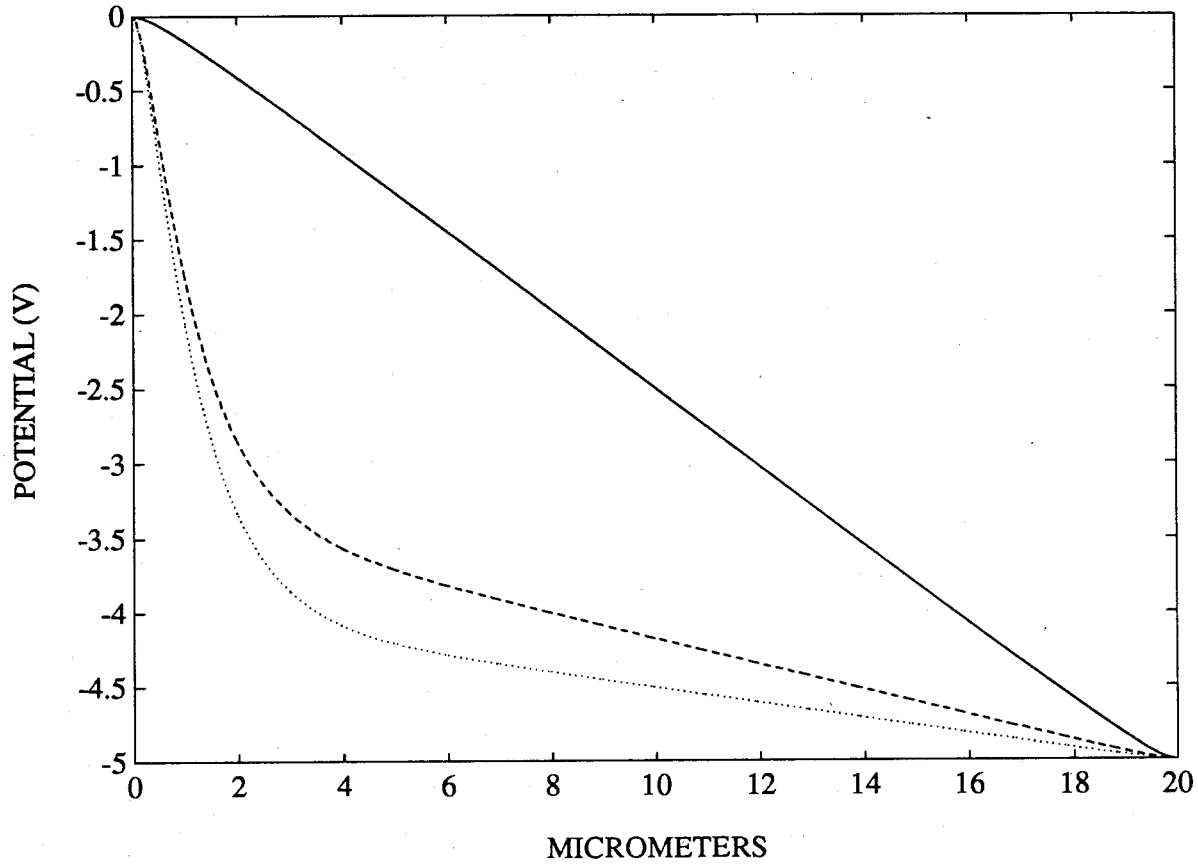


Figure 3.25: Potential profile corresponding to the conditions described in Fig. 3.24.

increase in applied voltage there will be an extension of the depletion region into the channel. But this extension will be small in comparison to the overall structure. So the boundary conditions introduce only a small error in the overall potential profile across the SI material.

The extension of the depletion layer into the channel upon increasing a negative bias on the sidegate may be small in comparison to the sidegate-gate distance, but significant with respect to the channel thickness. To obtain a quantitative picture we superimpose a potential profile of channel-substrate junction in equilibrium with a non-equilibrium potential profile across the SI substrate as shown schematically in Fig. 3.26. Over a wide range of biasing conditions the substrate space-charge density at the channel-substrate junction is a sum of density of deep(N_{da}) and shallow(N_{sa}) acceptors[70]. The space-charge may be even higher because of the possible presence of deep levels at the channel-substrate interface created by implantation damage. We assume an abrupt channel-

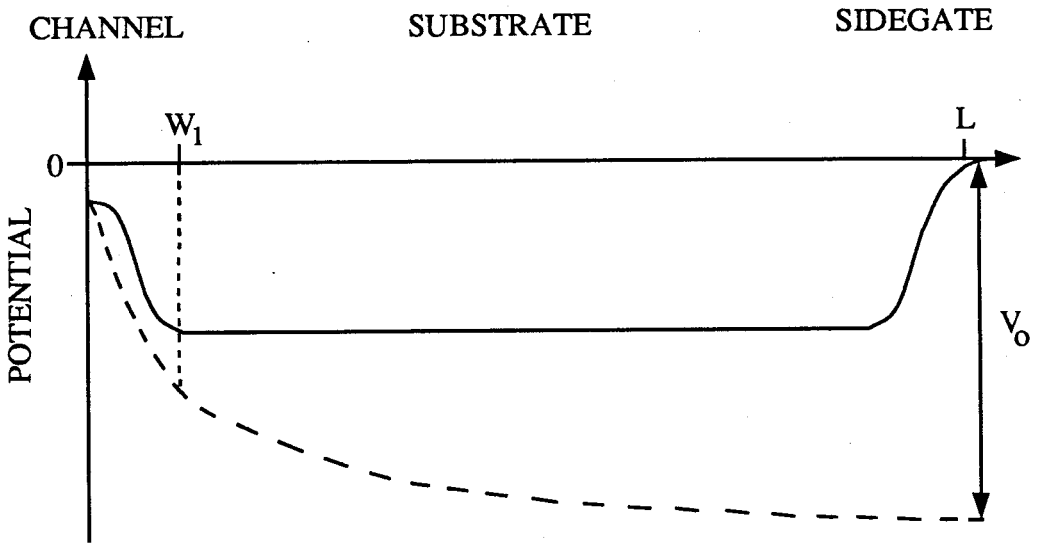


Figure 3.26: Schematic superimposition of the potential profile across the investigated structure in the presence of a sidegate voltage V_0 (dashed line), and for zero applied voltage (solid line). W_1 designates the width of the substrate-channel depletion layer.

substrate junction with the depletion layer consisting mostly of the substrate depletion region, which is consequently given in equilibrium by:

$$W_1 \approx \sqrt{2\epsilon V_{bi}/q(N_{da} + N_{sa})} \tag{3.39}$$

where V_{bi} is the built-in potential of the channel-substrate interface, which is approximately equal to but less than half the band-gap. The voltage across the channel-substrate junction is given by eqn. (3.38) at $x = W_1$. This voltage can be used in evaluating a pinchoff voltage of ion-implanted MESFETs following the procedures in [35]. The width of the channel depletion region is [71]

$$W_2 = \sqrt{\frac{2\epsilon(V_{bi} - V(W_1))(N_{da} + N_{sa})}{qN_{ch}(N_{ch} + N_{da} + N_{sa})}} \tag{3.40}$$

where N_{ch} is the channel donor density.

We have presented a one-dimensional analysis of sidegating, which ignores the drain-source field. The next question that we should ask is how the gate can communicate with the sidegate in the presence of a large drain voltage. For a MESFET biased in saturation, a high-field region is established in the gate-drain region, while the field of about $2 - 3\,kV/cm$ is sustained in the

gate-source region. Since the gate-sidegate field can be comparable to that in the latter region, some of the holes that are injected from the gate towards the source can reach the substrate. To obtain quantitative results a two-dimensional analysis is needed.

The phenomenon of sidegating recovery under conditions of large drain voltage has been discussed by several authors, who attributed it to hole injection from the channel due to an avalanche effect[72, 73]. In our experiments this phenomenon occurred only upon applying a very high drain voltage and was not correlated with the appearance of an excess gate current. We suggest that it was due to inhibition of the gate-sidegate communication: for large enough drain voltages, the field in the gate-source region increases and prevents from most of the holes reaching the substrate.

Our analysis does not take into account the non-linear velocity-field relationship. The results presented in this paper show that in the presence of hole injection the electric field can only be high only over a very narrow region and in the remaining portions of the structure it is below its ohmic value. Consequently the electron velocity can reach saturation only in the vicinity of the hole-injecting electrode, where it would probably result in an even higher voltage drop in this region. An increase in the voltage drop indicates that a larger portion of the sidegate voltage will be in the vicinity of the channel thus enhancing sidegating.

Gunn effect (instabilities due to intervalley electron transfer) has been invoked to explain sidegating and oscillations in GaAs MESFETs[74]. The present work indicates that because of the very low field throughout almost the entire structure in the presence of hole injection, intervalley electron transfer is unlikely to occur. The experiments on semiconductors with traps showed a greatly reduced region of negative mobility in I-V characteristics [75, 76] and, therefore, even at higher fields it is difficult to explain sidegating in terms of the Gunn effect.

As has been already pointed out Lee *et al.* [12] suggested a mechanism of a charge transport in SI GaAs in sidegating effect. Their traps-filled-limit model was based on the high-level injection theory of Lampert and Mark[7]. This model qualitatively explains sidegating, but has some difficulties in explaining it quantitatively [8]. Lampert theory is based on carrier transport by drift only. In contrast, under conditions of low-level injection both the diffusion and drift components of the current are important. Low-level and high-level analyses are just two extremes of the injection phenomenon into

semiconductor with traps; namely its small and large-signal analyses. Another important difference between the above two analyses is that they treat different geometries: while the Lampert theory is applicable for long structures, our analysis has been applied to configuration of two relatively closely-spaced contacts, which is a typical case for integrated circuits. Still, both of the theories are important as mentioned before: the results of the small-signal analysis should be useful for circuit designers, while large-signal analysis is useful for predicting abrupt variations in I-V characteristics.

In conclusion, sidegating in GaAs MESFETs was investigated using analytical techniques. One-dimensional expressions for carrier concentration, field, and potential profiles in a SI substrate were obtained without some of the assumptions, which are usually made in analytic approaches, such as local space-charge neutrality, neglect of recombination, and diffusion or drift component of the current. A variable boundary condition on the channel side of the structure allowed investigation of injection into a SI substrate. Although only one-dimensional the present analysis provides new insight into device physics. In the presence of hole injection it was shown that:

1. The local space-charge neutrality is not preserved.
2. Both diffusion and drift component currents are important in transport in short SI GaAs structures.
3. The Gunn effect is unlikely to occur in short structures.

The analysis was performed on a configuration of two closely-spaced contacts, but the results, such as an appearance of the field overshoot in the presence of hole injection, are similar to those obtained for longer structures [41]. Therefore, the low-injection analysis may explain the long-range sidegating.

In our physical model of sidegating hole injection from the gate plays a major role and this is consistent with our experimental observations (see Fig. 3.17), which showed that the gate current is a better indicator of sidegating than the sidegate current.

3.3 Evaluation of hole injection

When sidegating occurs the negative sidegate voltage progressively depletes the channel and reduces its electron concentration. Consequently, the potential barrier for holes is reduced and more

holes are injected into the channel. Since the channel of low pinch-off ion-implanted MESFETs is very thin, few holes are lost due to recombination in neutral channel, and most of them reach the substrate. Furthermore, due to the impurity profile of ion-implanted devices there is a built-in electric field, which assists holes to move into a substrate. The hole current through the gate may exceed the electron current in the gate-channel-SI-sidegate structure. To show this consider the energy band diagram in Fig. 3.18. Upon applying a negative bias to a sidegate the depletion edge of the channel-substrate junction is pushed into the channel. When two depletion regions merge the electron barrier is reduced allowing more electrons to be injected into the gate. The number of available electrons, however, is limited by their supply from the sidegate determined by the resistance of a SI region. Thus the maximum electron current can be estimated from the electron ohmic current density through a SI substrate:

$$J_e = qn_e\mu_n V_a/L \tag{3.41}$$

where V_a is the applied gate-sidegate voltage, and L is the distance between gate and sidegate. On the other hand we can find the hole current from the thermionic emission theory [60], which is applicable here due to a very thin Schottky depletion region. Thus the maximum hole current density is given by:

$$J_{pm} = A_p^* T^2 e^{-q\varphi_p/kT} \tag{3.42}$$

where φ_p is the hole barrier height [77] and A_p^* is the effective Richardson constant for holes. For $\varphi_p = 0.6eV$, $n_e = 10^7 cm^{-3}$, $\mu_n = 4000\, cm^2/Vsec$, $L = 20\mu m$ and $V_a = 3V$ the hole and electron currents are $5.69 \times 10^{-4} A/cm^2$, and $9.6 \times 10^{-6} A/cm^2$ respectively. Clearly the maximum hole current will strongly depend on the Fermi level at the surface of the channel. For instance, for $\varphi_p = 0.55eV$ we obtain $J_{pm} = 3.9 \times 10^{-3} A/cm^2$.

In low pinch-off MESFETs the distance between the edges of a Schottky gate depletion region and a channel-substrate junction is normally in the range of Debye length. So even for a small decrease in the thickness of the undepleted channel the channel electron concentration deviates drastically from its equilibrium value [27]. The maximum electron concentration in the channel can be expressed

as [78]:

$$n_0 = n_i exp(U_0) \tag{3.43}$$

with

$$U_0 = sinh^{-1}(N_D/2n_i)\{1 - 0.5exp[-(d - w_G - w_I)/L_D]\} \tag{3.44}$$

where L_D is defined in (3.27), n_i is intrinsic carrier concentration, d is the channel thickness, w_G is the thickness of a Schottky gate depletion region, and w_I is the extension of the channel-substrate junction into the channel. The thermionic emission hole current density can be expressed in terms of the maximum electron concentration in the channel:

$$J_{ps} = A_p^* T^2 e^{-q(\varphi_p + V_D - V_{as})/kT} = A_p^* T^2 N_c e^{-qE_g/kT}/n_0 \tag{3.45}$$

where N_c is the effective conduction band density of states in the conduction band, E_g is the energy band-gap, V_D is the built-in potential of the Schottky contact [77], and V_{as} is the applied voltage on a Schottky contact. Using eqn. (3.43)-(3.45) it is possible to calculate the hole current from the gate into the substrate as a function of a sidegate voltage by determining w_I from the sidegating experiment. Our calculations of the hole current as a function of w_I reveal that the hole current density does increase significantly when w_I is approaching $d - w_G$, but it is still much smaller than the electron ohmic current density. Upon increasing the negative sidegate voltage the condition of channel punch-through is achieved. With further increase in voltage the hole current increases rapidly until reaching its maximum value, given by (3.42). Our analysis is confirmed by the measurements of the gate current in MESFETs that exhibited a gradual decrease in the drain current upon applying a negative sidegate voltage. The measurements, which are shown in Fig. 3.27, indicate that as the drain current is reduced with a sidegate voltage, the gate and sidegate current increase and above around – 8V they coincide. This indicates that as the channel is progressively depleted, more holes are injected from the gate, increasing the gate current, and more of these holes reach the substrate, where they recombine with the electrons coming from the sidegate. As shown in Fig. 3.28. the gate current and the corresponding sidegate current depend only weakly on the gate bias. This may seem surprising because the gate bias alters the thickness of the undepleted channel and therefore should

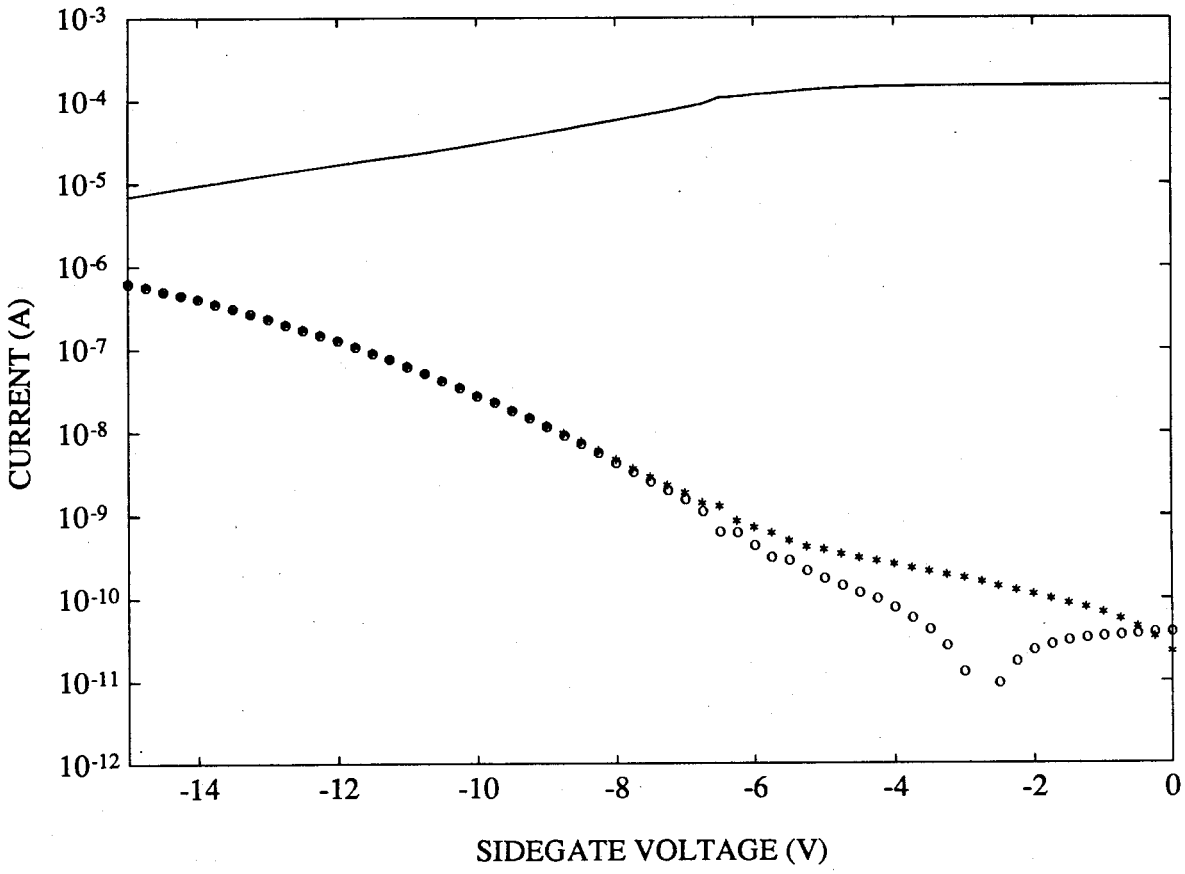
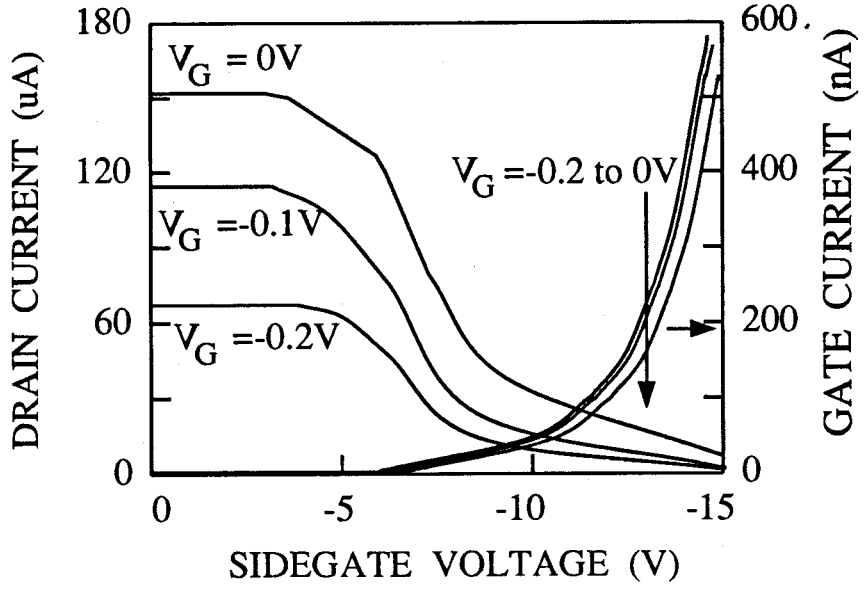


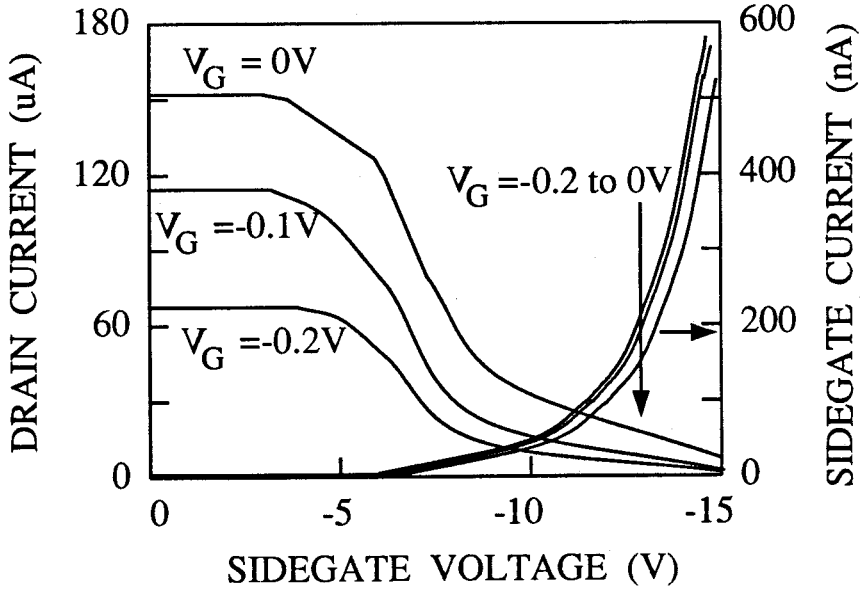
Figure 3.27: Drain (solid line), gate (circles), and sidegate (asterisks) currents vs. sidegate voltage ($V_D = 2V$, $V_G = 0V$). The gate current changes its polarity at about $-3V$. The gate and sidegate currents coincide at the voltages more negative than $\approx -8V$.

affect the voltage, at which punch-through condition occurs. However, it is probably due to the two-dimensional nature of hole injection through the channel, which involves both the gate-sidegate and drain-source interaction. The hole injection is strongest in the region where the drain-source electric field is weakest, namely, between gate and source. By applying more negative gate bias the hole injection from the gate is enhanced, but the electric field in the gate-source region increases as well, resulting in less holes being able to get through the channel. Thus these two effects balance each other resulting in the gate current rise occurring approximately at the same sidegate voltage.

In the above section we have proposed a sidegating model based on hole injection from the gate. The purpose of the following section is to report experimental results [42] which confirm the participation of hole injection in sidegating. So far, experimental observation of the participation of



(a)



(b)

Figure 3.28: Channel punch-through in low pinch-off GaAs MESFETs ($V_D = 2V$, V_G : $0V$ to $-0.2V$): (a) gate current increases rapidly when a MESFET is nearly pinched off as a result of applying a negative sidegate voltage. (b) the corresponding sidegate current.

holes in the sidegating effect has been reported only when large drain voltages were applied, and under such biasing conditions the holes are believed to be generated by impact ionization in the channel,

from where they can be injected into the SI substrate[72, 79, 73]. We report hole injection from the Schottky gate when no drain voltage is applied. Hole injection from the Schottky metal on a SI substrate has been reported previously [61]. In contrast, we focus on hole injection from the Schottky metal on the doped channel and show that it can be significant for a large negative sidegate voltage.

Minority carrier injection in *epitaxial* Schottky diodes increases with current under conditions of high forward bias[54]. This is related to an increase in the electric field in the quasi-neutral region of the diode. However, since the voltage drop across this region is very small in practical situations, the injection of minority carriers is negligible. The situation is very different in the Schottky gates of MESFETs fabricated by shallow ion implantation into SI GaAs substrates, illustrated by a schematic band diagram shown in Fig. 3.29(a). The structure consists of two closely spaced depletion regions which are associated with the Schottky barrier and the channel-substrate interface. Since the Fermi level is pinned at the channel surface at about $0.8\,eV$ from the conduction band [61], there is an inversion layer beneath the gate, that is, at the surface the number of holes exceeds the number of electrons. Under forward-bias conditions the holes are injected from the gate into the channel and are subject to an assisting field due to a steep impurity profile. On applying a negative voltage to the substrate, only a small portion of the applied voltage drops across the Schottky barrier; most is absorbed at the channel-substrate barrier and in the SI region. As a result, the two depletion regions start to merge, and the potential barrier for holes starts to decrease, causing more holes to be injected into the substrate, as shown in Fig. 3.29(b). Manifacier and Henisch have shown that the hole injection into a SI substrate may result in a very large electric field overshoot in the vicinity of the channel [41]. This will cause an even higher voltage drop in the channel-substrate depletion region, consequently extending it into the channel and lowering further the hole injection barrier[80]. This process is self-regenerating. At high enough applied voltages it will result in the punch-through of the channel and a rapid increase in the gate current.

To test the model, measurements were performed on a structure consisting of two low-pinch-off MESFETs shown in Fig. 3.30. The MESFETs were fabricated in a commercial foundry using direct n and n^+ Si ion implantation into undoped liquid encapsulated Czochralski GaAs substrates. The channel width, gate length, gate-source and gate-drain spacings were $4\,\mu m$, $1\mu m$, $2\,\mu m$ and $2\,\mu m$,

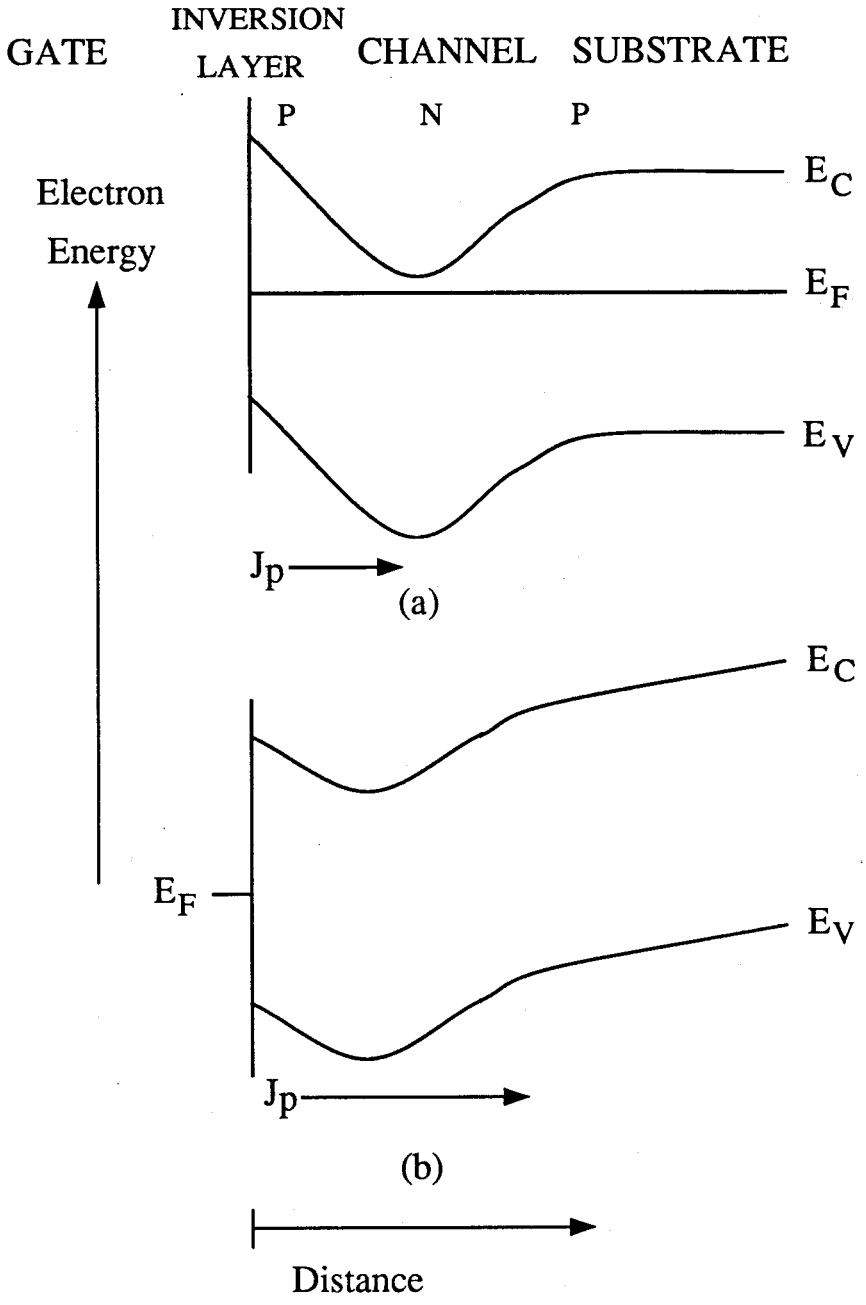


Figure 3.29: Hole injection and a corresponding energy-band diagram for a (a) quasi-neutral MESFET, (b) MESFET with a large negative sidegate voltage applied. The combination of the inversion layer, n-channel and semi-insulating substrate creates a P-N-P looks like structure.

respectively. The MESFETs had a threshold voltage of about $-0.7\,V$ and we estimated the channel thickness to be$0.15\,\mu m$ and the maximum electron concentration in the channel to be $10^{17}\,cm^{-3}$. The gate and ohmic contacts of device 2, which were slightly forward-biased, and a negatively biased

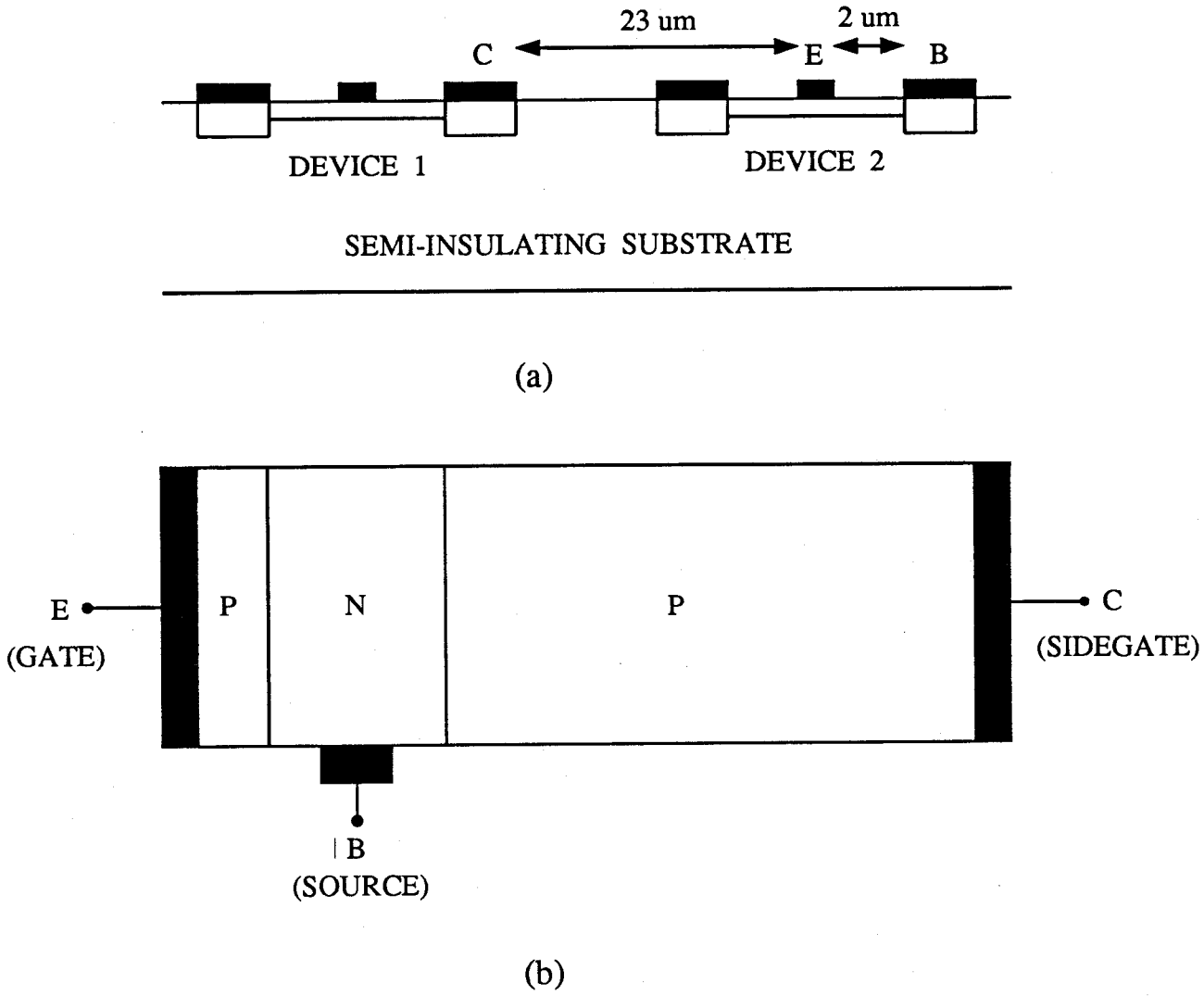


Figure 3.30: (a) Cross section of the investigated three-terminal structure consisting of two MESFETs. Using a Schottky (gate) and an ohmic contact (source/drain) of one MESFET together with an ohmic contact of the other MESFET, the structure acts as a surface-barrier transistor with a gate operating as an emitter. (b) An equivalent bipolar transistor structure with a long collector region.

ohmic contact of device 1 were used to simulate the interaction between MESFETs. Under these conditions this three-terminal structure functions as a surface-barrier transistor [81, 55] that features hole injection based on the punch-through of the channel as a result of applying a negative collector (sidegate) voltage. Since the channel width is much smaller than the emitter-base distance, most of the injected holes are collected by the substrate. Because of the large emitter-collector distance, the injected holes will recombine with the electrons coming from the collector terminal. Thus the current measured at the collector contact is roughly the hole current of the Schottky diode. A more

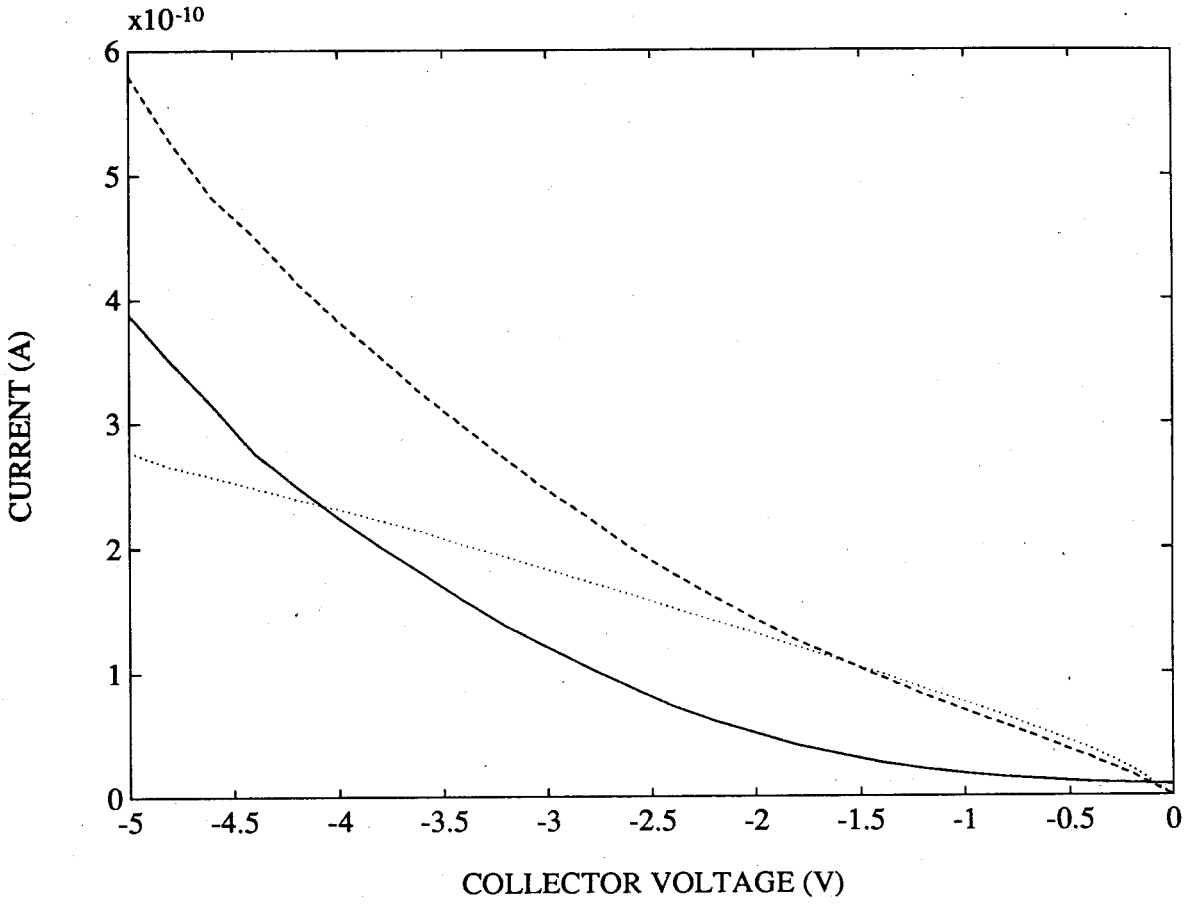


Figure 3.31: Measured currents vs. collector voltage characteristics. The solid line corresponds to the emitter (gate) current I_E and the dashed line to the collector (sidegate) current I_C. The leakage current I_L (designated by dots) is the current between base and collector when the emitter is floating.

accurate estimate of the hole current is obtained by subtracting the base-collector leakage current from the measured collector current. The measured currents are presented in Fig. 3.31. The hole injection ratio, which is the ratio of the hole-to-emitter current, is shown in Fig. 3.32 as a function of collector bias and emitter-base bias as a parameter. The hole injection is negligible for collector bias between zero and $-1.5\,V$, but increases significantly for more negative voltages, in good agreement with the model.

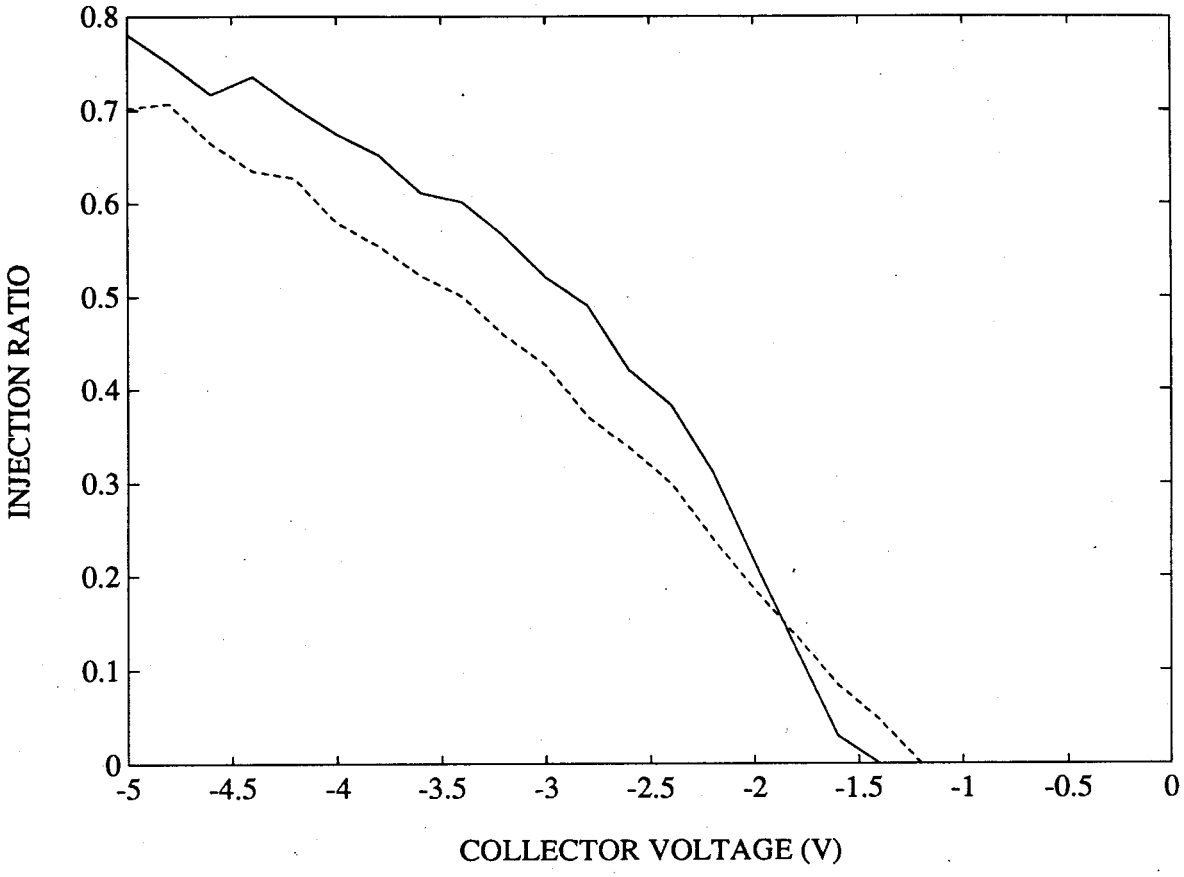


Figure 3.32: Calculated hole injection ratio, defined as $(I_C - I_L)/I_E$, for the emitter-base bias of 0.1 V (solid line) and 0.2 V (dashed line). I_E,I_C and I_L are defined in caption of Fig. 3.31.

3.4 High-level double carrier injection in the sidegating effect

3.4.1 Introduction and Model

We have already noted that Lee *et al.* [12] found a correlation between substrate current and sidegating and explained it by the traps-filled-limit model (TFL) [20]. According to Lee *et al.* [12] electron injection from the sidegate to the MESFET channel-substrate interface is initiated at a certain threshold voltage, determined by the sum of sidegate and drain voltages. However, TFL model predicts threshold voltages larger than normally observed [8, 9]. Also, some sidegating experiments have been reported, where no dependence on drain voltage was found [8]. Furthermore, the oscillations which have been observed by several researchers (e.g. [74]) and the recently reported hysteresis in the sidegate current [15] are difficult to explain in terms of single carrier space-charge-limited conduction.

In the above studies of sidegating the interaction between gate and sidegate has not been considered, and measurements of the gate current were not reported. It has been established that in Schottky barriers consisting of metal on n-type *doped* semiconductor under forward bias minority carriers can be injected from the metal into the semiconductor [82], although there is some controversy regarding the magnitude of hole injection in Schottky diodes [59]. Hole injection from positively biased metal pads into the *semi-insulating* GaAs substrates was discussed by Wager and McCamant [61]. Goto *et al.* [83] analyzed the sidegating effect, based on the numerical simulation of a structure that included Schottky metal on the SI substrate, and explained it in terms of hole injection from the gate. Their results did not show hysteresis in I-V characteristics and consequently in their analytical model they did not try to explain the instabilities often observed in sidegating effect. Recently a series of measurements by Liu *et al.* [58] showed that a small portion of the gate that overlaps the n-channel on to the SI substrate can play an important role in the sidegating effect.

Our physical model is based on experimental observations of strong dependence of the gate current on the sidegate voltage, and new results, which relate the gate current jumps to hysteresis in test devices [43]. We propose that these phenomena originate from double injection into the SI

substrate. We suggest that the gate, when biased positively with respect to the sidegate, is a major source of hole injection into the SI substrate.

At low sidegate voltages *low-level* double injection creates a non-linear potential profile across the SI substrate, resulting in a significant portion of the sidegate voltage being applied on the channel-substrate junction.

For a high enough sidegate voltage the transit time of holes from the gate to the sidegate across a SI substrate becomes less than their lifetime. The holes reach the vicinity of the electron injecting sidegate, compensate the negative space charge formed there by the trapped electrons, and consequently cause a steep rise in the sidegate and gate currents. This is a *high-level* double injection mechanism, which is known to produce a negative resistance in I-V characteristics often exhibited through hysteresis and oscillations [20, 84]. Reduction of the space charge in the vicinity of sidegate results in many more electrons being injected into the channel-substrate interface. The injected electron charge is compensated by further extension of the depletion layer into the channel, resulting in a sharp reduction of the drain current. Our experimental results confirm the importance of hole injection as proposed by Goto *et al.* [83], but our model suggests a new and more general interpretation of their results.

3.4.2 Experiments

We now report some new experiments which indicate double injection in the sidegating effect. Low pinch-off (threshold voltage $\approx -0.7V$) depletion mode ion-implanted GaAs MESFETs fabricated at a commercial foundry were used with gate length 1 μm and width 4 μm. The gate-source and and gate-drain spacings were both 2 μm. The sidegate was 8μm from the source and 23 μm from the gate. The layout of the test structure is shown in Fig. 3.33. An HP 4145A semiconductor parameter analyzer was used to obtain I-V characteristics at room temperature in the dark.

Fig. 3.34 shows MESFET drain, gate, and sidegate currents versus sidegate voltage. The drain voltage was 2V and the gate was grounded. The drain current gradually decreased starting from a sidegate voltage of -3V. Jumps in the currents occurred at a sidegate voltage of about -6V. Correlation between gate and sidegate currents was apparent not only in that jumps in each occurred at the same

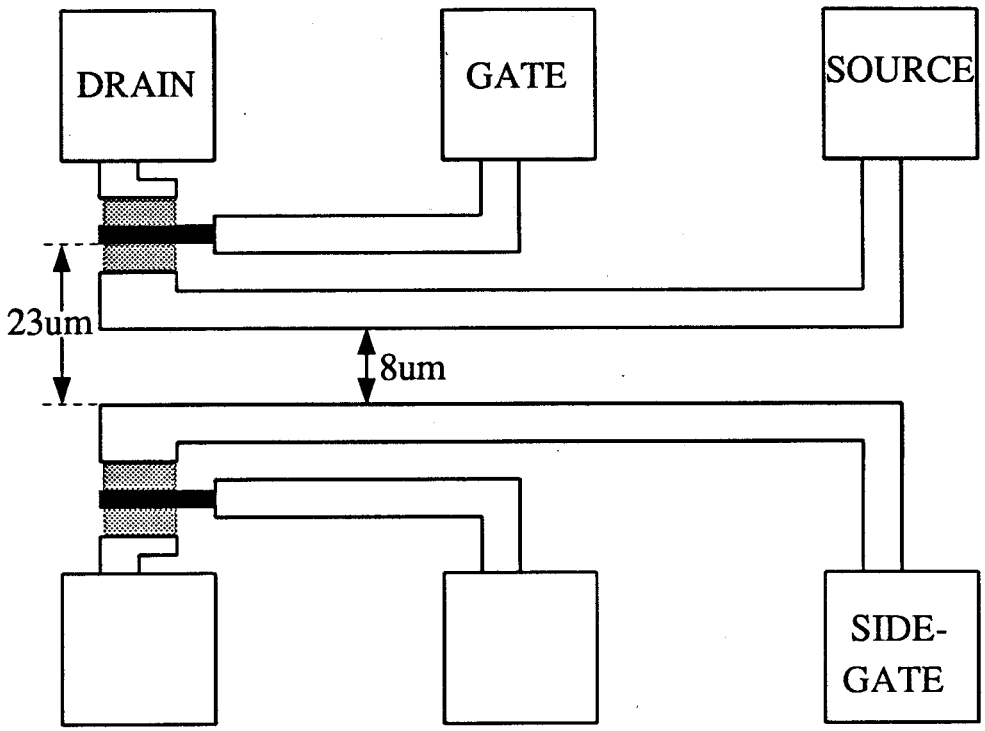


Figure 3.33: Schematic layout of the mirror-image structure of two MESFETs that were used in the sidegating measurements. The channel width, gate length, gate-source and gate-drain spacings were 4 μm, 1 μm, 2 μm and 2 μm respectively. The dotted area is the active layer area of the MESFETs. When one of the MESFETs was biased, the other's ohmic contact served as a sidegate. The sidegate was 8 μm from the source and 23 μm from the gate.

sidegate voltage, but also in that they then exhibited the same magnitude. Changes in drain voltages ($V_D : 0.5 - 4V$) had no effect on the sharp threshold voltage.

The drain current as a function of sidegate voltage for a MESFET with the gate floating and the drain voltages from 1 to 5V is presented in Fig. 3.35. At drain voltages below 3V a *soft* threshold behavior was exhibited with no evident current jumps. Also no jumps were observed in the sidegate current (not shown in Fig. 3.35). However, with increasing drain voltage a jump in the drain current appeared, which corresponded to the jump in the sidegate current.

The current between the grounded gate and the biased sidegate as a function of a negative sidegate potential, with the remaining electrodes floating, is shown in Fig. 3.36. This figure also shows MESFET current-voltage characteristics when the source and drain are biased. Both the gate and drain currents exhibited hysteresis with the same two threshold voltages at about -5V and -6V. The hysteresis behavior described here was reproducible when long integration time and small voltage

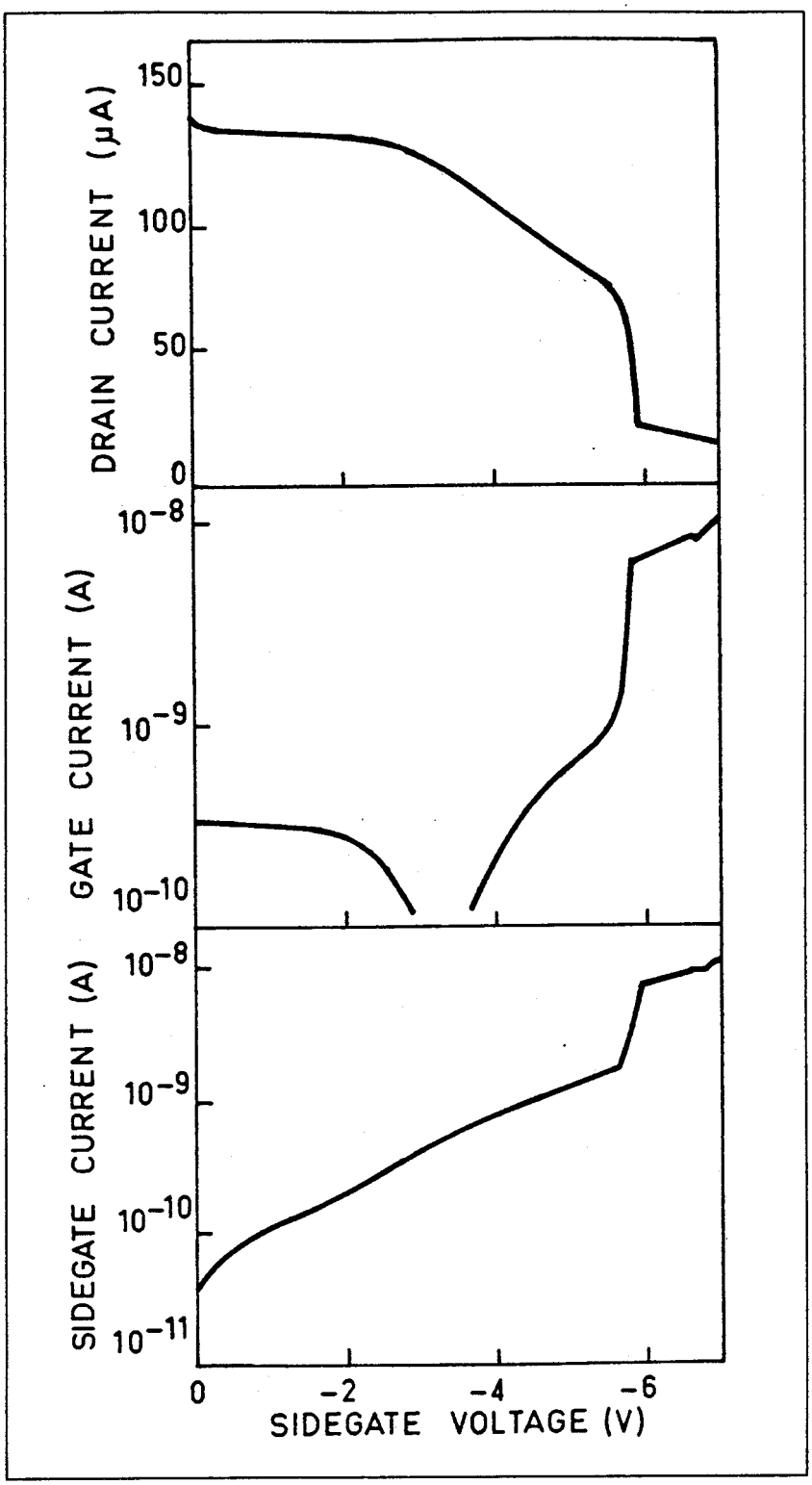


Figure 3.34: Drain, gate and sidegate currents as a function of sidegate voltage ($V_D = 2V$, $V_G = 0V$).

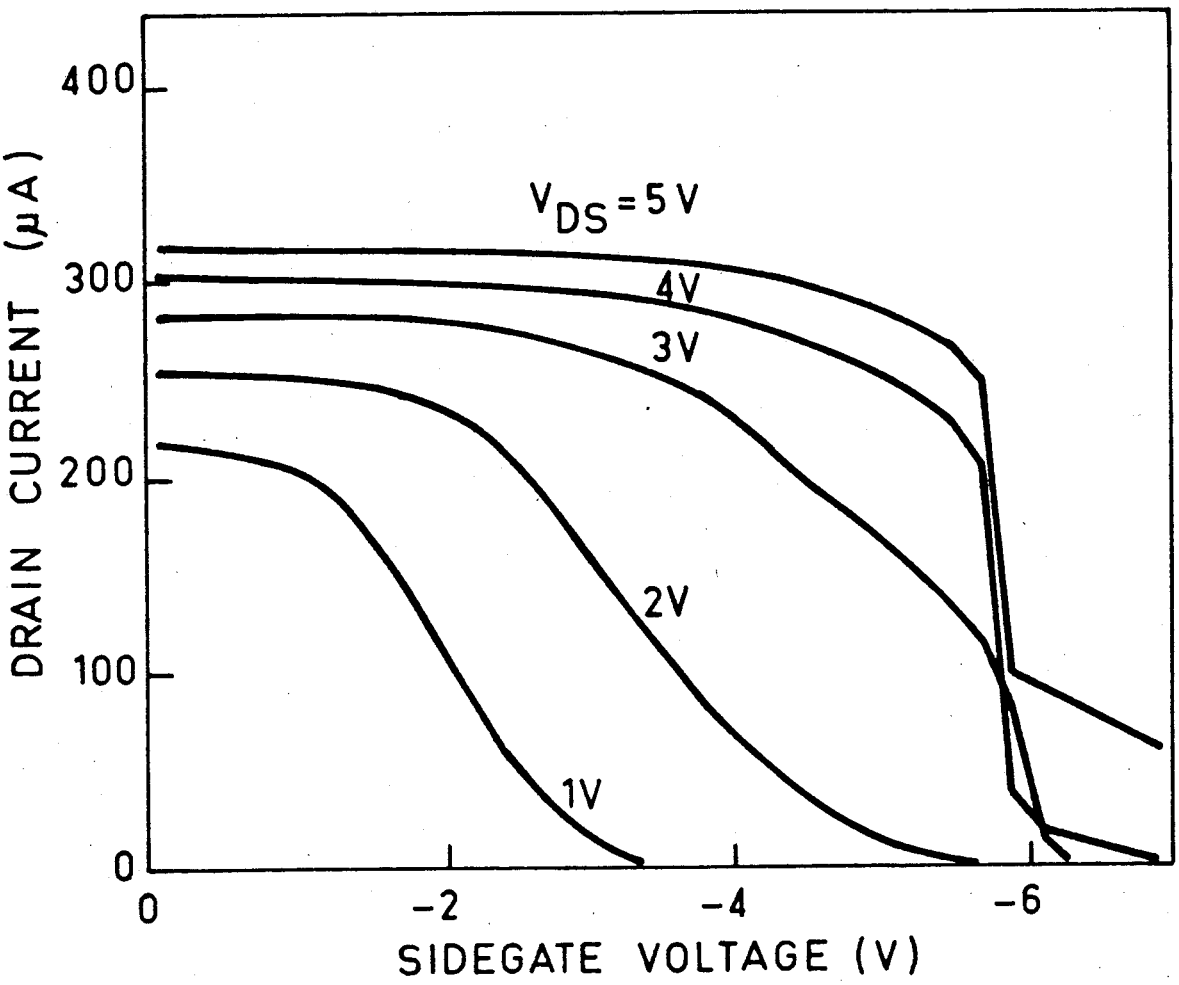


Figure 3.35: Drain current versus sidegate voltage for a MESFET with a floating gate ($V_D : 1 - 5V$).

steps were used in the measurements. For the sidegate positively biased with respect to the gate neither current jump nor hysteresis were observed. Note that Li *et al.* have shown that the hysteresis in sidegating is an artifact of the voltage-controlled measurement and in the current-controlled case the current-voltage characteristics exhibit negative resistance [15]. We, however, have performed our measurements by applying constant sidegate voltages, because these measurements imitate the real-life environment in the GaAs integrated circuits, in which the worst-case sidegating is determined by the negative voltage supply (which ideally is a supplier of unlimited current).

3.4.3 Analysis and Discussion

Double injection into a semiconductor with traps is known to produce a negative resistance regime [20, 84], which exhibits current jumps, oscillations and hysteresis as found in sidegating

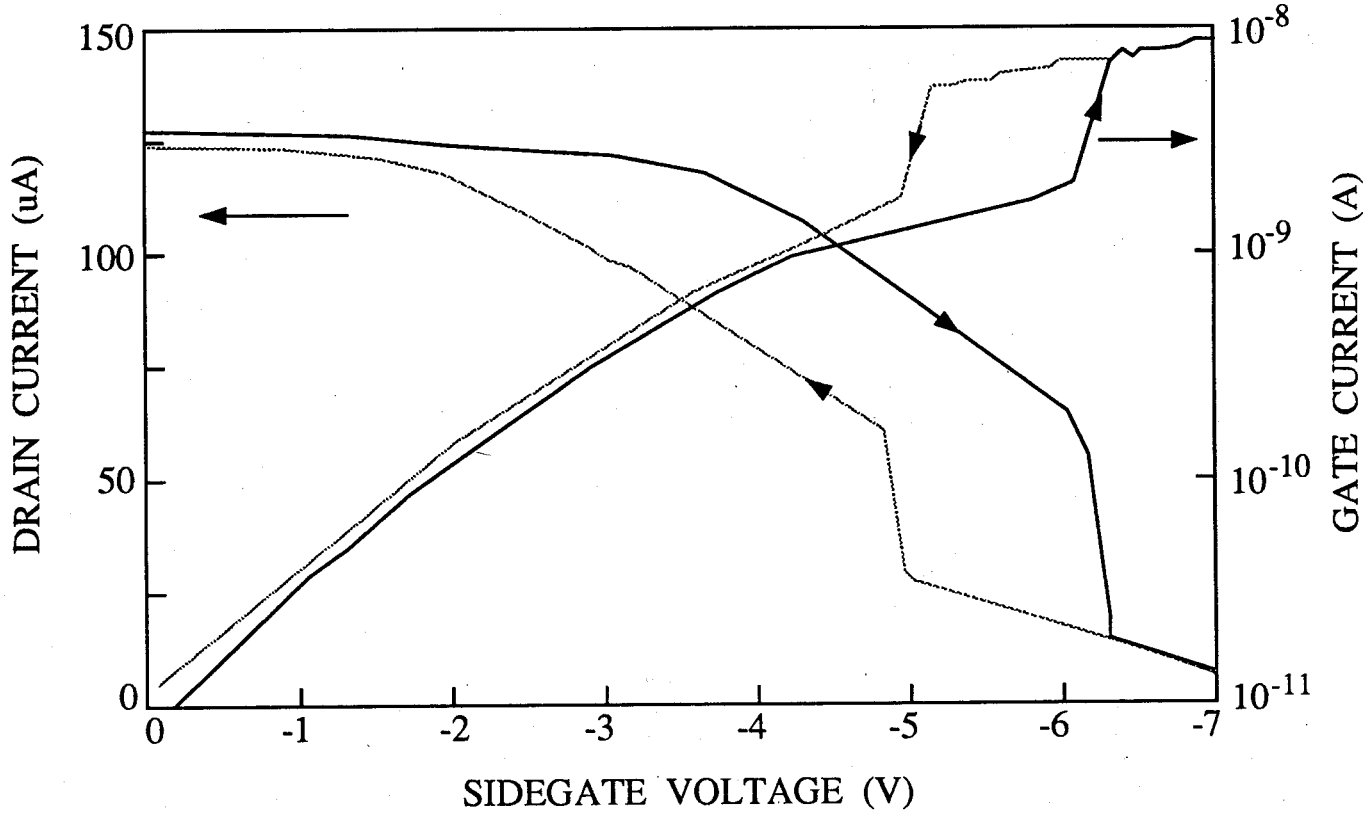


Figure 3.36: Hysteresis in the drain current ($V_D = 2V$, $V_G = 0V$), and in the gate-sidegate current (source and drain are floating). The solid line represents a decreasing (more negative) sidegate voltage, while the dotted line represents the opposite direction.

experiments. The following observations in our experiments, even if separately they do not prove the double injection mechanism, together provide strong evidence for it.

1. Sidegate and gate currents were found to be equal after a threshold sidegate voltage was reached. This indicates direct communication between gate and sidegate.
2. Hysteresis and current jumps in the gate-sidegate structure did not appear upon applying a positive sidegate voltage, but only under forward bias conditions (negative sidegate voltage), for which hole injection from the Schottky gate is possible [82].
3. Drain current-voltage characteristics exhibited hysteresis with threshold voltages corresponding to the ones observed in a gate-sidegate structure. Thus MESFET characteristics are directly related to the transport mechanism between gate and sidegate.

4. Hole injection is not expected in MESFETs with a floating gate operating at low drain voltages and, consistently, no jumps in the drain or sidegate currents were observed in our experiment under such biasing conditions as shown in Fig. 3.35.

However, for larger drain voltages Fig. 3.35 shows jumps in the drain current accompanied by jumps in the sidegate current. It is possible that the gate obtains an intermediate value between drain and source voltages, which cause it to be forward-biased. In this case there is no difference between these results and those shown in Fig. 3.34. However, the prebreakdown impact ionization effects, observed by Tsironis [85] in GaAs MESFETs and epitaxial layers for drain voltages higher than 4-5 volts, also may explain our observations. Thus, the prebreakdown impact ionization generates pairs of holes and electrons in the channel. Because of the energy barrier at the channel-substrate interface only high-energy electrons can be injected into the SI substrate. By contrast, holes have an assisting field at the interface and consequently are attracted by the negatively biased sidegate and participate in the double injection process causing the current jump.

Fig. 3.34 shows that *soft* and *sharp* gate current reduction corresponds to *soft* and *sharp* and drain current reduction with a threshold at -3V and -6V respectively. It is difficult to explain the sharp current reduction by electron injection from the sidegate for a drain-sidegate distance of 26μm, a drain voltage of 2V and a sidegate voltage of only -6V. For instance, a recent numerical analysis of n-SI-n structures indicates that electron current increases significantly at about 10V applied on a 5 μm one-dimensional structure [56]. Even higher threshold voltages were obtained for two-dimensional structures. Furthermore, as already mentioned in subsection 3.4.2, the sharp threshold voltage did not change due to variations in a drain voltage. This is not expected from the TFL model, which predicts a decrease in the sidegate threshold voltage with increasing drain voltage.

Fig. 3.36 indicates that the drain current reduction is caused by the gate-source interaction. The current jumps and hysteresis in gate-sidegate structure were observed at an applied field of $\approx 2.5\mathrm{kV/cm}$, which is too small to initiate impact ionization, that can also produce hysteresis in I-V characteristics [15]. Furthermore, Fig. 3.34 shows clearly that the gate current is a strong function of sidegate voltage. Even before the current jump, a sidegate voltage of -3V is enough to reverse the gate current polarity, which indicates abnormal MESFET operation. If we consider a MESFET

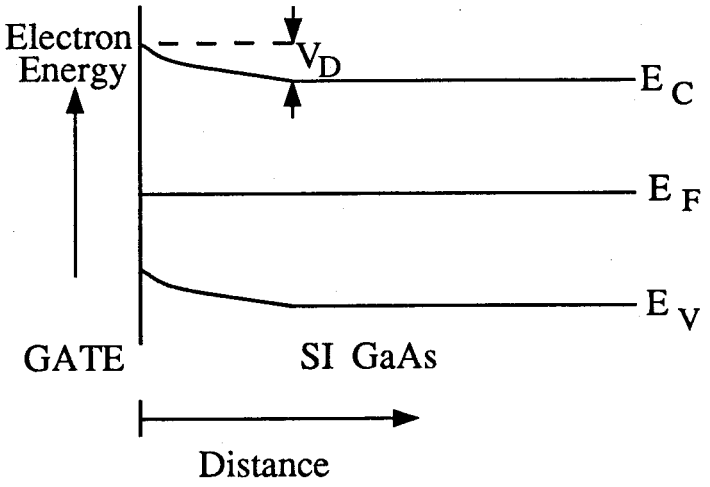


Figure 3.37: Schematic energy-band diagram of a MESFET gate on a SI substrate.

on a SI substrate as a combination of three Schottky diodes, then the experiments show that for high enough sidegate voltage the gate-sidegate diode is dominant. We, therefore, concentrate on the gate-sidegate interaction.

As shown in Fig. 3.33 there is a part of Schottky metallization that is on a SI substrate. Fig. 3.37 depicts the energy levels in equilibrium of a gate on a SI substrate. The Fermi level is pinned at about $0.8\,eV$ [60] from the conduction band and as a result an inversion layer is formed beneath the gate. The thickness of the Schottky depletion region is given by [86]:

$$w_{dep} \approx \sqrt{2\epsilon V_D / qN_{EL2}} \tag{3.46}$$

where V_D is a Schottky built-in potential. For $V_D = 0.15eV$ and $N_{EL2} = 10^{16}cm^{-3}$ we obtain $w_{dep} \approx 0.15\mu m$. If a negative bias is applied on the sidegate the gate becomes forward biased. Since the Schottky depletion region is thin we can discuss the transport across the Schottky contact in terms of thermionic emission theory [60]. Under these conditions the hole injection from the metal was shown largely to exceed the electron injection [61]. Thus, the gate-SI-sidegate structure acts as a *P-I-N* diode with a heavily compensated intrinsic region.

For low sidegate voltages we deal with low-level double injection between gate and sidegate. Under these conditions the potential distribution across a SI substrate can be calculated using eqn. (3.38). Fig. 3.25 shows the results of this calculation which indicate that a significant portion of the

voltage across a SI substrate is dropped in the vicinity of the hole-injecting boundary. This potential profile is a result of the dipole, consisting of positive and negative excess trapped carriers, which is formed in the close neighborhood to the hole-injecting interface [80]. Three major contributors to the formation of the dipole are high trap densities, high ratio of electron to hole mobility, and low lifetime in SI GaAs [41]. When only a small portion of the applied gate-sidegate voltage is dropped across a Schottky depletion region, the results in Fig. 3.25 show that in the presence of hole injection a significant portion of the applied voltage is dropped across the channel-substrate interface. A gradual increase in the applied negative voltage will result, consequently, in a gradual decrease in the drain current as shown in Fig. 3.34 for low sidegate voltages.

During the double low-level injection a negative space-charge region is formed in the vicinity of sidegate by the electrons trapped in deep EL2 levels. For higher sidegate voltages the transit time of holes across a SI substrate becomes comparable to their lifetime. They reach the vicinity of a sidegate electrode and reduce the negative space-charge. As a result many more electrons are injected into the substrate and reach the channel-substrate depletion region. The injected negative charge is compensated by the depletion of the channel, resulting in a strong decrease in the drain current. During the injection process some holes are captured by the recombination centers. As a result hole lifetime increases and consequently a smaller voltage is needed to bring holes to the sidegate electrode. This is the source of the appearance of a negative resistance in double injection process according to Lampert's theory [20]. In our experiments the devices that exhibited sharp sidegating also exhibited hysteresis. We have investigated an appearance of hysteresis in the gate-sidegate structures. The source and drain were floating, the sidegate was grounded, and the gate was positively biased. The negative resistance regime started typically between 5 to 6V and was accompanied by a strong increase in the current as shown in Fig. 3.38. The location of the second threshold varied from device to device over the range of 6 to 18V. Neither hysteresis, nor current jumps were observed in gate-sidegate structures when the gate was negatively biased with respect to the sidegate. According to Lampert's theory [20] the current increase in the negative resistance regime should be approximately given by the ratio of the recombination center density to the equilibrium free electron concentration. For a recombination center density of $10^{15} cm^{-3}$ and the electron concentration of $10^{7} cm^{-3}$ in SI

GaAs we should expect an abrupt increase of eight orders of magnitude in the current. But in our experiments we observed an increase of a maximum of five orders of magnitude in the current. Our results are in agreement with the studies of GaAs $P-I-N$ diodes reported by Weiser and Levitt [87], and Selway and Nicolle [88]. They found the appearance of a negative resistance at voltages and currents smaller than those predicted by the Lampert [20] or Ashley-Milnes [84] theories and explained it in terms of an optical feedback mechanism suggested in GaAs by Dumke [89, 84]. Additional mechanisms of double injection such as filament formation were proposed for GaAs [84]. According to Dumke's model under increasing external illumination the negative resistance should decrease and disappear. We performed this experiment on our gate-sidegate structures and the results, which confirm Dumke's theory, are shown in Fig. 3.38. Nevertheless, the threshold voltage for the end of a negative resistance regime in double injection process according to the Lampert's one-dimensional model for an insulator with length L [20]:

$$V_{th} = L^2/2\mu_p\tau; \tag{3.47}$$

are in the range normally observed, e.g., taking $L = 23\mu m$, $\mu_p = 320cm^2/Vsec$ [90], and a typical hole lifetime in high-resistivity GaAs $\tau = 1nsec$ [91] we obtain a threshold voltage of 8.3V.

Geometrical effects in sidegating become very important when holes are injected from only a small portion of the gate that is on a SI substrate. In this case the double injection process occurs only beneath part of the channel, as visualized in Fig. 3.39. Thus the sidegating effect can be analyzed using an equivalent circuit consisting of two MESFETs in parallel. One of them will be cut off under conditions of strong double injection, while the other is not influenced by it. This may explain why the MESFET in Fig. 3.34 was not completely cut off after a jump in the gate current had occurred.

Not all gate-sidegate structures on the same wafer exhibited hysteresis. We suggest that this is due to substrate inhomogeneity involving variations in the concentration of the recombination centers either present in the as prepared wafer or process-induced, for example as a result of ion-implantation. In addition, double injection is expected to be strongly dependent on the thickness of the oxide layer, which is normally present between a gate and a SI substrate. The non-uniformity of the oxide layer across the substrate can result in different sidegating behavior for devices on the same

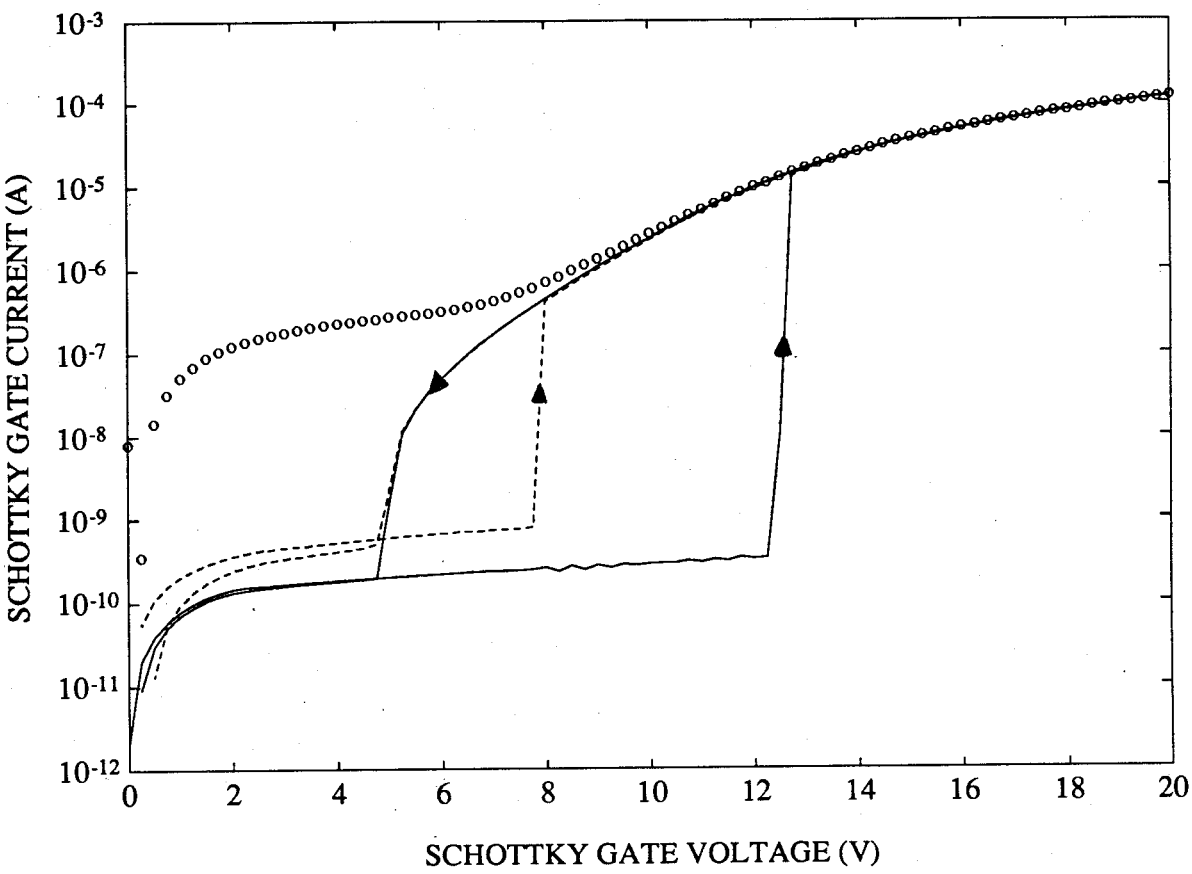


Figure 3.38: Hysteresis in the gate-sidegate structures under increasing illumination ($V_{SG} = 0V$, drain and source are floating). The solid line corresponds to the data obtained in the dark, dashed line corresponds to the data obtained with room lights, and the open circles correspond to the data obtained under microscope lamp illumination. Results obtained in the dark or with room lights show hysteresis, while those obtained under direct illumination show no hysteresis.

wafer. Therefore, the gate formation processing steps, particularly oxide removal before depositing a Schottky metal, can be important in determining sidegating. In this case, the sidegating effect can be different from one process run to another, even if identical substrates are used.

Since the negative resistance in gate-sidegate structures may appear at sidegate voltages, for which a MESFET is already cut off, it may easily be overlooked. But the hole injection from the gate on a SI substrate is still present, resulting in a *soft*, but not necessarily a weak, sidegating effect.

In conclusion, double injection should be considered in investigating sidegating associated with a *sharp* threshold behavior. We propose a physical model, which accounts for abrupt current variations

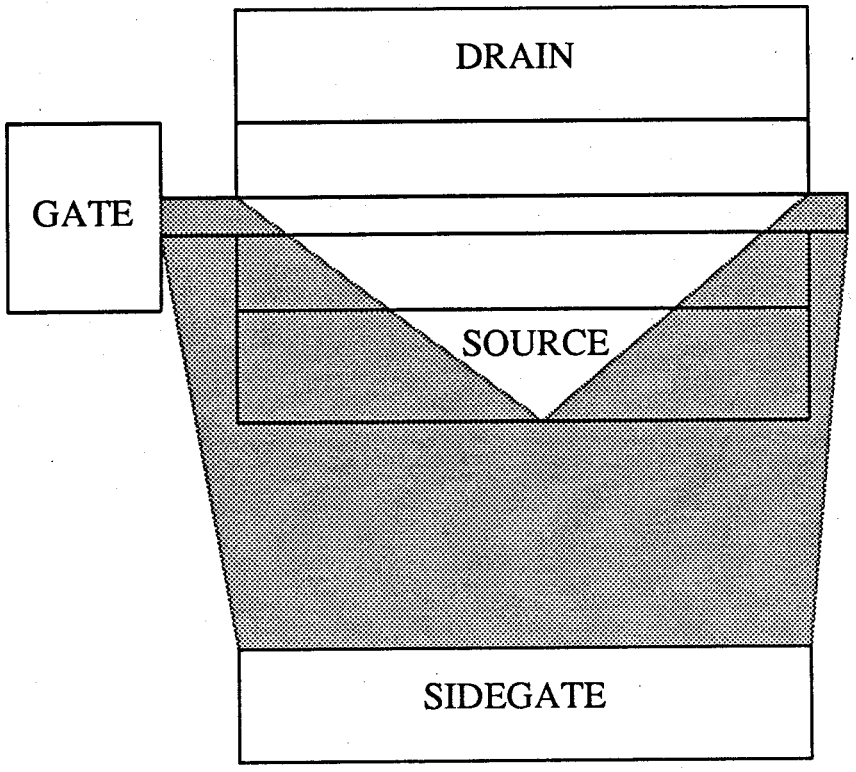


Figure 3.39: Schematic top view of the area (designated by gray pattern) that is affected by hole injection from the gate on a SI substrate.

and hysteresis in sidegating. Our measurements of hysteresis are in general agreement with Dumke's model for double injection in GaAs. The predominant mechanism of double injection, however, is probably to be determined by device geometry and material properties. The role of hole injection in enhancing *soft* sidegating effect was discussed through the analytical expression for the potential distribution across a SI substrate. Our model accounts for sidegating light sensitivity [13] because photo-generated hole-electron pairs will participate in the double injection process: the generated holes will be attracted to the negatively biased sidegate through a SI substrate, in a similar way of attracting holes generated by a prebreakdown impact ionization. It was shown that a channel punch-through may result in significant hole injection from the gate. Our analysis of hole injection does not take into account the difference in the gate and sidegate areas, which can be significant. Hole injection for small-area Schottky diodes was shown by numerical analysis to be much higher than that for the large contact devices [92]. More accurate treatment will require two-dimensional

analysis, which is beyond the present scope of this work. Our results show the need to include gate current measurements in investigating the sidegating.

3.5 Summary

Double injection into the SI GaAs substrate was investigated as a mechanism of sidegating in GaAs MESFETs. We propose a physical model for sidegating based on a series of measurements, which show change of gate current with sidegate voltage and correlation between abrupt variations in drain, gate and sidegate currents and instabilities in test devices. An analytical treatment of carrier, field, and potential distribution in a SI substrate under conditions of low-level injection shows that an electric field overshoot may develop in the vicinity of the MESFET when hole injection occurs. This results in a large portion of the applied voltage being dropped across the channel-substrate interface and, consequently, in sidegating. Sharp sidegating, exhibited through an abrupt decrease of the drain current, is explained by high-level double injection.

Measurements of currents in gate-source-sidegate structures, when the gate is slightly forward-biased and the sidegate is negatively biased with respect to the source, showed that significant hole injection from the gate occurs for large sidegate voltages. This is in agreement with a proposed model, in which the presence of an inversion layer under the Schottky gate due to the pinning of the Fermi level at the channel surface causes hole injection into the channel when the gate is positively biased with respect to the sidegate. Upon increasing negative sidegate voltage the substrate-channel depletion region is expanded, and consequently, the neural region of the channel is shrunk. This results in more holes being injected into the substrate from the gate.

Chapter 4

Low-frequency transport in semi-insulating GaAs

4.1 Introduction

In silicon the presence of deep levels was shown to introduce low-frequency dependence into the capacitance and conductance of a p-n or metal-semiconductor junction [29, 51, 69, 44]. It is also well known that many of the parameters of GaAs MESFETs on SI substrates exhibit low-frequency-dependent behavior. While the frequency dependence of some of the parameters (e.g. transconductance) has usually been attributed to the surface states [48], it has been pointed out by many researchers, e.g. [93], that the frequency dependence of the output conductance is due to the properties of the SI substrate. The analysis of transport in SI GaAs in the frequency domain is therefore vital for understanding many of the properties of GaAs MESFETs at low-frequencies. Furthermore, this analysis contributes to the understanding of crosstalk between two adjacent MESFETs on a SI substrate [40, 94].

4.2 Analysis and results

We assume that both deep donors and deep acceptors are present in the SI GaAs one-dimensional structure confined between two contacts: contact 2 is an ohmic contact which can inject only electrons, while contact 1 is a Schottky contact which may inject holes and is assigned a variable injection ratio η (η=0 corresponds to zero hole injection, and η=1 to zero electron injection). The schematic equilibrium band diagram of the structure is depicted in Fig. 4.40. In Chapter 3 we reported an analytical study of the DC charge, field and potential distribution in such structures [80]. Our analysis was based on the investigation of minority-carrier injection into semiconductors with traps by Manifacier and Henisch [64, 41]. We assume that the deep levels in the structure do not interact and thus separate rate equations can be written for each level. If we restrict the magnitude of excess charge densities to small variations around their equilibrium values then the rate equation for a single

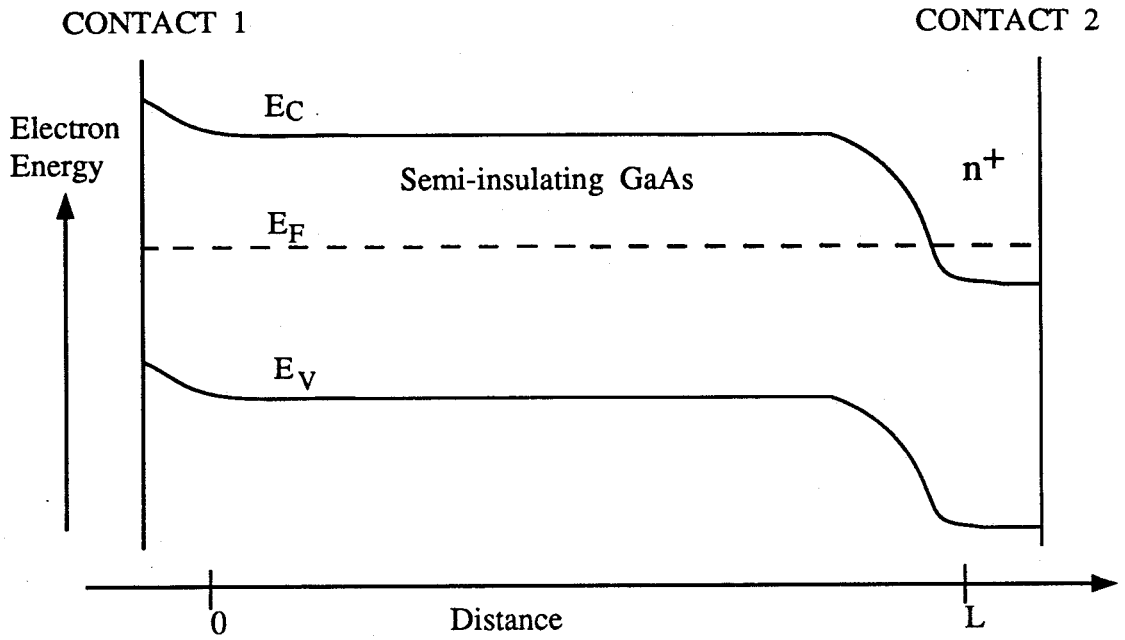


Figure 4.40: Schematic equilibrium band diagram of the semi-insulating structure of a length L between zero-field points in the vicinity of N^+ and Schottky contacts.

deep level is given by [29]:

$$\frac{d\delta N_t}{dt} = -\delta N_t(c_n n_e + e_n + c_p p_e + e_p) + \delta n N_t \frac{c_n n_1}{n_e + n_1} - \delta p N_t \frac{c_p n_e}{n_e + n_1} \tag{4.48}$$

where N_t is the density of a deep level, e_n, e_p are the emission rates of a deep level for electrons and holes,c_n, c_p are the capture probabilities of a deep level for electrons and holes, and n_e, p_e are the equilibrium electron and hole concentrations, n_1 is the electron density if the Fermi level were at the energy level of the deep level. We decompose the excess free electron, free hole and trapped electron densities respectively into AC and DC components to yield:

$$\delta n(x) = \delta n_{dc}(x) + \delta n_{ac}(x) e^{jwt}\,, \tag{4.49}$$

$$\delta p(x) = \delta p_{dc}(x) + \delta p_{ac}(x) e^{jwt}\,, \tag{4.50}$$

$$\delta N^t(x) = \delta N^t_{dc}(x) + \delta N^t_{ac}(x) e^{jwt}\,. \tag{4.51}$$

Substituting (4.49)-(4.51) into (4.48) to obtain:

$$\delta N_{ac}^{t}(x) = \beta \delta n_{ac}(x) - \alpha \delta p_{ac}(x) \tag{4.52}$$

with

$$\beta = \frac{\tau_T^D}{\tau_n^D(1+jw\tau_T^D)} + \frac{\tau_T^A}{\tau_n^A(1+jw\tau_T^A)} \tag{4.53}$$

$$\alpha = \frac{\tau_T^D}{\tau_p^D(1+jw\tau_T^D)} + \frac{\tau_T^A}{\tau_p^A(1+jw\tau_T^A)} \tag{4.54}$$

where indexes D and A designate deep donors and deep acceptors respectively,

$$1/\tau_T^{D,A} = c_n^{D,A} n_e + e_n^{D,A} + c_p^{D,A} p_e + e_p^{D,A}, \tag{4.55}$$

$$1/\tau_n^{D,A} = c_n^{D,A} N_t^{D,A} n_1^{D,A} / \left(n_e + n_1^{D,A}\right), \tag{4.56}$$

$$1/\tau_p^{D,A} = c_p^{D,A} N_t^{D,A} n_e / \left(n_e + n_1^{D,A}\right). \tag{4.57}$$

For $w = 0$ α and β yield DC solutions [80] as expected. The linearized [63] time-dependent continuity equations for electrons and holes, and Poisson's equation can be written as:

$$\frac{\partial^2 \delta N}{\partial X^2} + \frac{\partial E}{\partial X} - \frac{A_n}{1+P_e}(P_e \delta N + \delta P) = \frac{qL_D^2}{\mu_n kT}\frac{\partial \delta N}{\partial t} \tag{4.58}$$

$$\frac{\partial^2 \delta P}{\partial X^2} - P_e\frac{\partial E}{\partial X} - \frac{A_n b}{1+P_e}(P_e \delta N + \delta P) = \frac{qL_D^2}{\mu_p kT}\frac{\partial \delta P}{\partial t} \tag{4.59}$$

$$\frac{dE}{dX} = \frac{1}{1+P_e}[(1+\alpha)\delta P - (1+\beta)\delta N] \tag{4.60}$$

with $L_D = \sqrt{[\epsilon kT/q^2(n_e+p_e)]}$, $A_n = \epsilon/q\mu_n\tau(n_e+p_e)$, where α and β are defined in (4.53) and (4.43), q is the magnitude of the electronic charge, μ_n is the electron mobility, μ_p is the hole mobility, $b = \mu_n/\mu_p$, τ is the lifetime, ϵ is the dielectric constant, $\delta N, \delta P$ and P_e are the excess

free carriers and equilibrium hole concentration respectively, normalized to the equilibrium electron concentration. The field is normalized to kT/qL_D, the potential to kT/q, the current density to $\mu_p kT(n_e + p_e)/L_D$ and the distance to L_D.

Substitution of (4.60) into (4.58)-(4.59) and decomposing the excess electron and hole densities into the DC and AC components yields two coupled differential equations, which can be separated into DC and AC parts. For frequencies much below the reciprocal of carrier lifetime the AC and DC sets of equations are identical, except in the AC set α and β are given by (4.53) and (4.54). As a result excess carrier concentration and potential profiles in the frequency domain are readily obtained from the DC solution for zero field boundary conditions [80]:

$$\delta N_{ac}(X) = \lambda[\frac{M\cosh(X\sqrt{\nu}) - R\cosh((L-X)\sqrt{\nu})}{\sqrt{\nu}\sinh(L\sqrt{\nu})} + \frac{P_e\cosh(X\sqrt{\xi}) + K\cosh((L-X)\sqrt{\xi})}{\sqrt{\xi}\sinh(L\sqrt{\xi})}] \tag{4.61}$$

$$\delta P_{ac}(X) = \lambda[M\frac{P_e\cosh(X\sqrt{\xi}) + K\cosh((L-X)\sqrt{\xi})}{\sqrt{\xi}\sinh(L\sqrt{\xi})} - P_e\frac{M\cosh(X\sqrt{\nu}) - R\cosh((L-X)\sqrt{\nu})}{\sqrt{\nu}\sinh(L\sqrt{\nu})}] \tag{4.62}$$

$$V_{ac}(X) = \lambda\{\frac{(1+\alpha)M - (1+\beta)}{A_n(P_e+b)} \times[\frac{P_e(\cosh(X\sqrt{\xi}) - 1) + K[\cosh((L-X)\sqrt{\xi}) - \cosh(L\sqrt{\xi})]}{\sqrt{\xi}\sinh(L\sqrt{\xi})} + KX] - \frac{M(\cosh(X\sqrt{\nu}) - 1) - R[\cosh((L-X)\sqrt{\nu}) - \cosh(L\sqrt{\nu})]}{\sqrt{\nu}\sinh(L\sqrt{\nu})} + RX\} \tag{4.63}$$

with $\nu = [P_e(1+\alpha) + (1+\beta)]/(1+P_e)$, $\xi = A_n(P_e+b)/(1+P_e)$, $K = \eta(b+P_e) - P_e$, $M = (1+\beta-A_n b)/(1+\alpha-A_n)$, $R = \eta(b-M) + M$, $\lambda = J_{ac}(1+P_e)/b(M+P_e)$. The normalized admittance Y is obtained from (4.63):

$$Y = J_{ac}/V_{ac}(L) = G + jwC. \tag{4.64}$$

The distribution of excess trapped and free carriers calculated from eqs. (4.52), (4.61), (4.62) for the hole injection ratio η=0 is shown in Figs. 4.41–4.42 for 1Hz and 1MHz correspondingly. Figs.

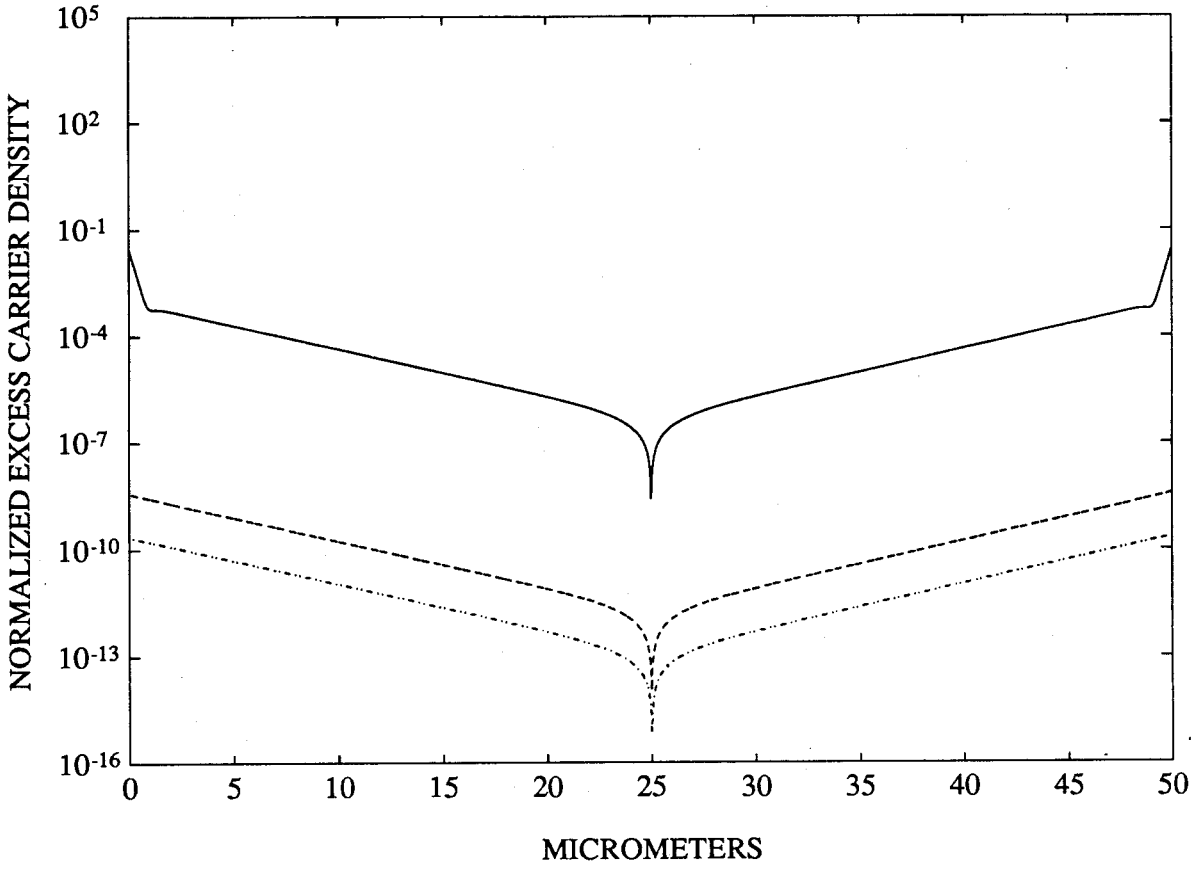


Figure 4.41: Concentration profile of excess trapped and free carriers in the 50μm long model structure at 1Hz with no hole injection (η=0). The solid line corresponds to trapped carriers, dashed line to electrons, and dots to holes. The amplitude of AC applied voltage is 50mV, the equilibrium electron concentration is $\approx 7 \times 10^6\, cm^{-3}$, the equilibrium hole concentration is $\approx 2 \times 10^5\, cm^{-3}$, the electron mobility is $4 \times 10^3\, cm^2/Vsec$, the hole mobility is $400\, cm^2/Vsec$, and the lifetime is $10\, nsec$. The deep donor is assumed to be 0.75eV from the conduction band, its density $2 \times 10^{16}\, cm^{-3}$, and with the capture cross section of $1 \times 10^{-13} cm^2$ for electrons and $1 \times 10^{-16} cm^2$ for holes . The deep acceptor is assumed to be 0.65eV from the conduction band, with density $5 \times 10^{15}\, cm^{-3}$, and with the capture cross section of $1 \times 10^{-13} cm^2$ for holes and $1 \times 10^{-16} cm^2$ for electrons.

4.43–4.44 show the distribution of excess trapped and free carriers calculated for η=1 at 1Hz and 1MHz correspondingly.

Fig. 4.45 shows conductance as a function of frequency evaluated from the real part of eq. (4.64) for η=0 and η=1. Fig. 4.46 shows the capacitance as a function of frequency evaluated from the imaginary part of eq. (4.64).

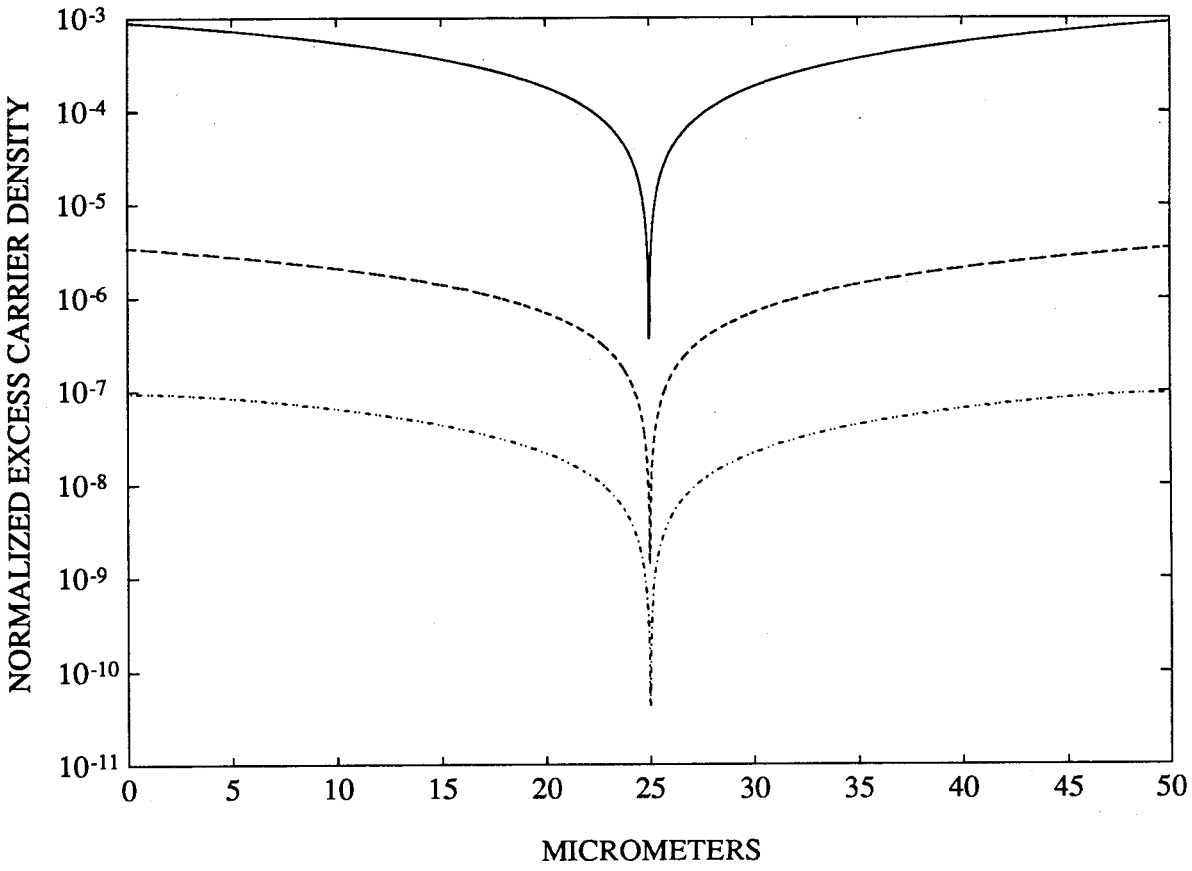


Figure 4.42: Concentration profile of trapped and free excess carriers at 1MHz with no hole injection. The rest of the parameters are given in Fig. 4.41.

4.3 Discussion

The solution of the transport equations in semiconductors was shown by van Roosbroeck and Casey [95] to be largely dependent on whether dielectric relaxation time is smaller or larger than carrier lifetime, and, consequently, they classified semiconductors into lifetime or relaxation types. In the latter no local space charge neutrality but rather charge separation through zero net local recombination is established. When the local space charge neutrality ($\delta N = \delta P$) is *not* assumed the solution of the continuity equations and Poisson's equation under conditions of low-level injection results in terms containing $exp(\pm X\sqrt{\nu})$ and $exp(\pm X\sqrt{\xi})$. The parameters $\sqrt{\nu}$ and $\sqrt{\xi}$ can be expressed in terms of a static screening length L_s and an ambipolar diffusion length L_{Da} [96] respectively:$\sqrt{\nu} = L_D/L_s$, $\sqrt{\xi} = L_D/L_{Da}$. Manifacier and Henisch modified

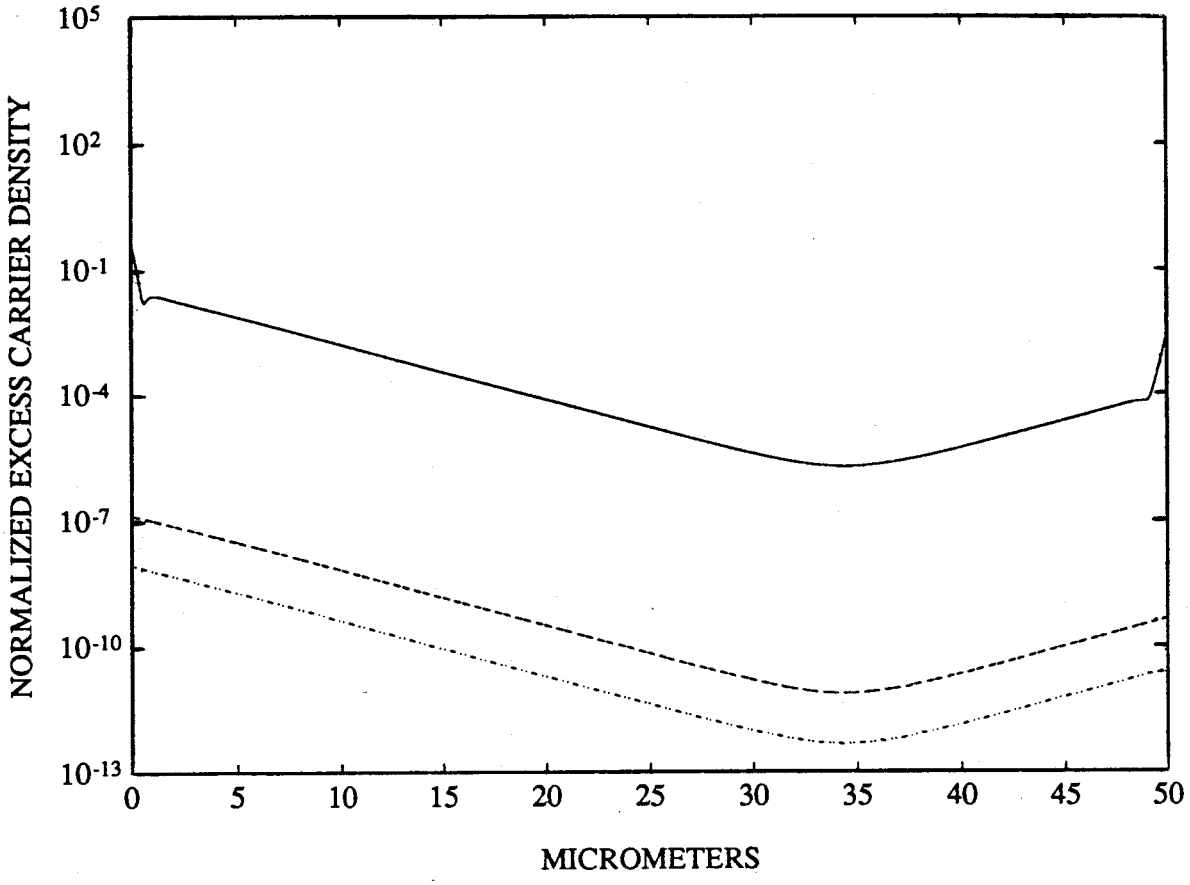


Figure 4.43: Concentration profile of trapped and free excess carriers at 1Hz in the presence of hole injection (η=1). The rest of the parameters are given in Fig. 4.41.

the criterion suggested by van Roosbroeck and Casey [95] and classified semiconductors with traps into a lifetime or relaxation case according to the ratio L_{Da}/L_s with a large ratio corresponding to lifetime semiconductors and the small to relaxation semiconductors [96]. When frequencies approach $1/\tau_T$ both excess trapped and free carriers become frequency-dependent through α and β (see eqs. (4.53)-(4.54)). Note that τ_T does not depend on the trap density and thus the frequency dependence is not necessarily initiated by the trap with largest density. Indeed, in our case τ_T^D is about 0.03sec, while τ_T^A is about 0.4sec and determines the range of frequencies in which frequency-dependent phenomena appear. Thus at 1Hz L_{Da} is about 3μm and the absolute value of L_s is about 0.08μm. At 1MHz the ambipolar diffusion length is the same but L_s changes significantly and it now stands at about 34μm. Consequently, SI GaAs exhibits lifetime-like behavior at low frequencies, but behaves

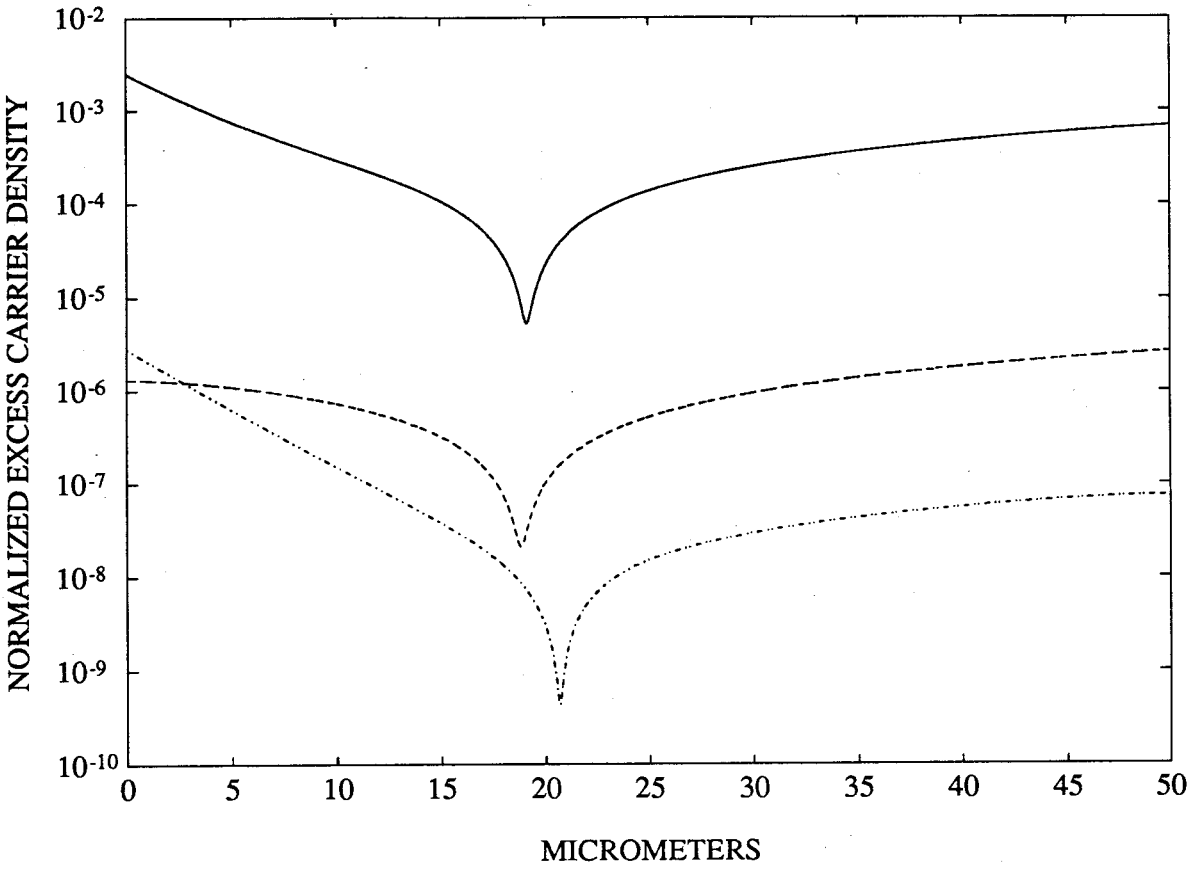


Figure 4.44: Concentration profile of trapped and free excess carriers at 1MHz in the presence of hole injection (η=1). The rest of the parameters are given in Fig. 4.41.

like a relaxation semiconductor at high frequencies. Note that the assumption of local space-charge neutrality results in the solution containing only $exp(\pm X\sqrt{\xi})$, which are frequency-independent at low frequencies (much below the reciprocal of carrier lifetime).

At 1Hz (see Figs. 4.41 and 4.43) the distribution of excess trapped and free carriers in the bulk of SI GaAs is dominated by $exp(\pm X\sqrt{\xi})$ since the diffusion length is much larger than the screening length. When hole injection occurs (see Fig. 4.43) the electrons move so as to neutralize the injected holes. The excess hole and electron densities are both positive and have similar exponential distribution throughout the structure, which is expected for a lifetime semiconductor. But in contrast to the classical lifetime behavior the local space charge neutrality is not preserved due to the high density of the traps in the SI substrate. At 1MHz the charge distribution in the SI structure is becoming

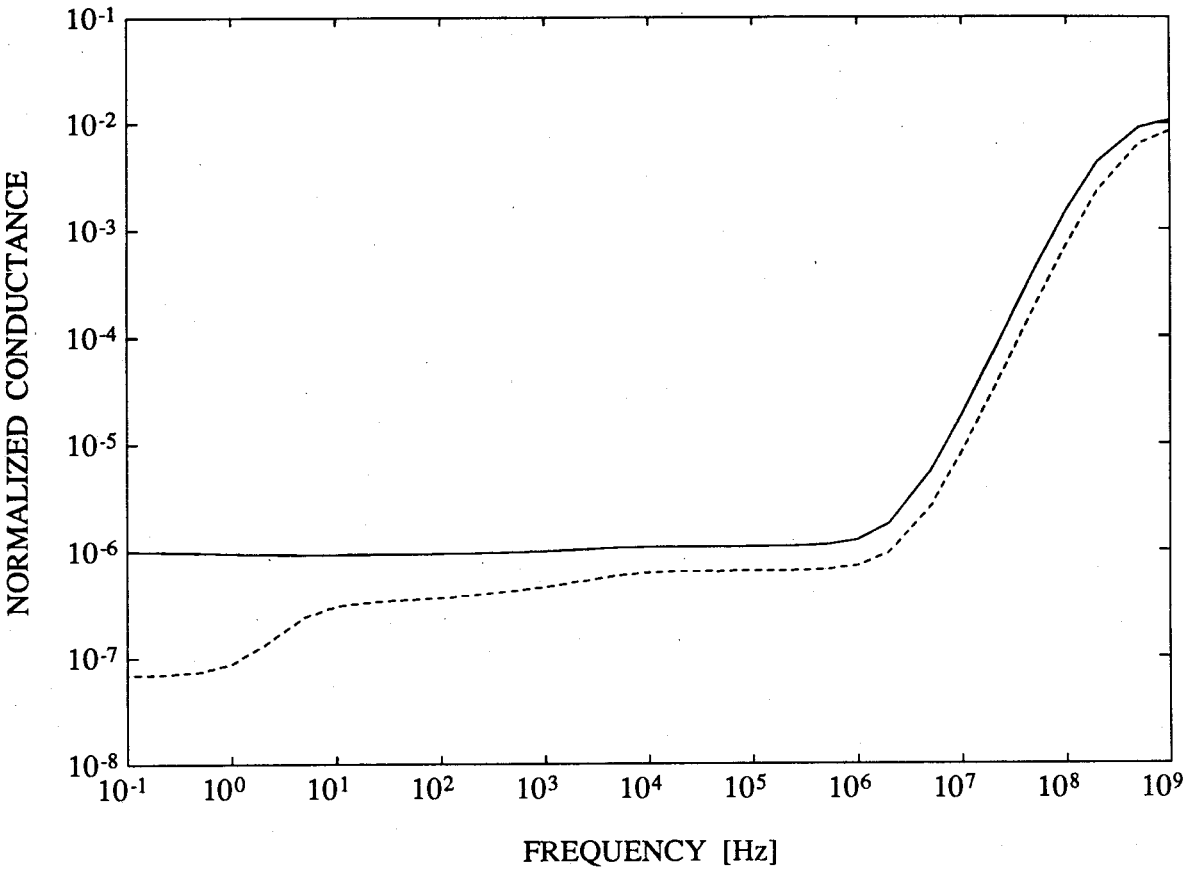


Figure 4.45: Frequency dependence of the conductance of the SI structure calculated using eq. (4.64). The dashed line corresponds to the conductance in the presence of hole injection (η=1) and the solid line to the conductance when no hole injection occurs (η=0). The rest of the parameters are given in Fig. 4.41.

less sensitive to the presence of hole injection (see Figs. 4.42 and 4.44). Since the screening length now is larger than the ambipolar diffusion length when hole injection occurs the effect of the latter on the carrier distribution appears only within the distance L_{Da} from the hole-injecting contact. After this the material is dominated by the zero net local recombination, which is typical of relaxation semiconductors, resulting in $\delta P(X) \approx -P_e \delta N(X)$ [41]. Normally in SI GaAs $P_e = p_e/n_e < 1$ and hence the excess hole and electron densities have opposite signs with the electron density being larger. This is observed in Figs. 4.42 and 4.44. Since the zero field boundary conditions dictate the total excess charge neutrality the excess carrier density changes sign around the middle of the structure.

Comparison between the carrier profiles at 1Hz and 1MHz reveals that the ratio of free to trapped carriers increases with frequency. The charge injected into the SI structure consists of a free and

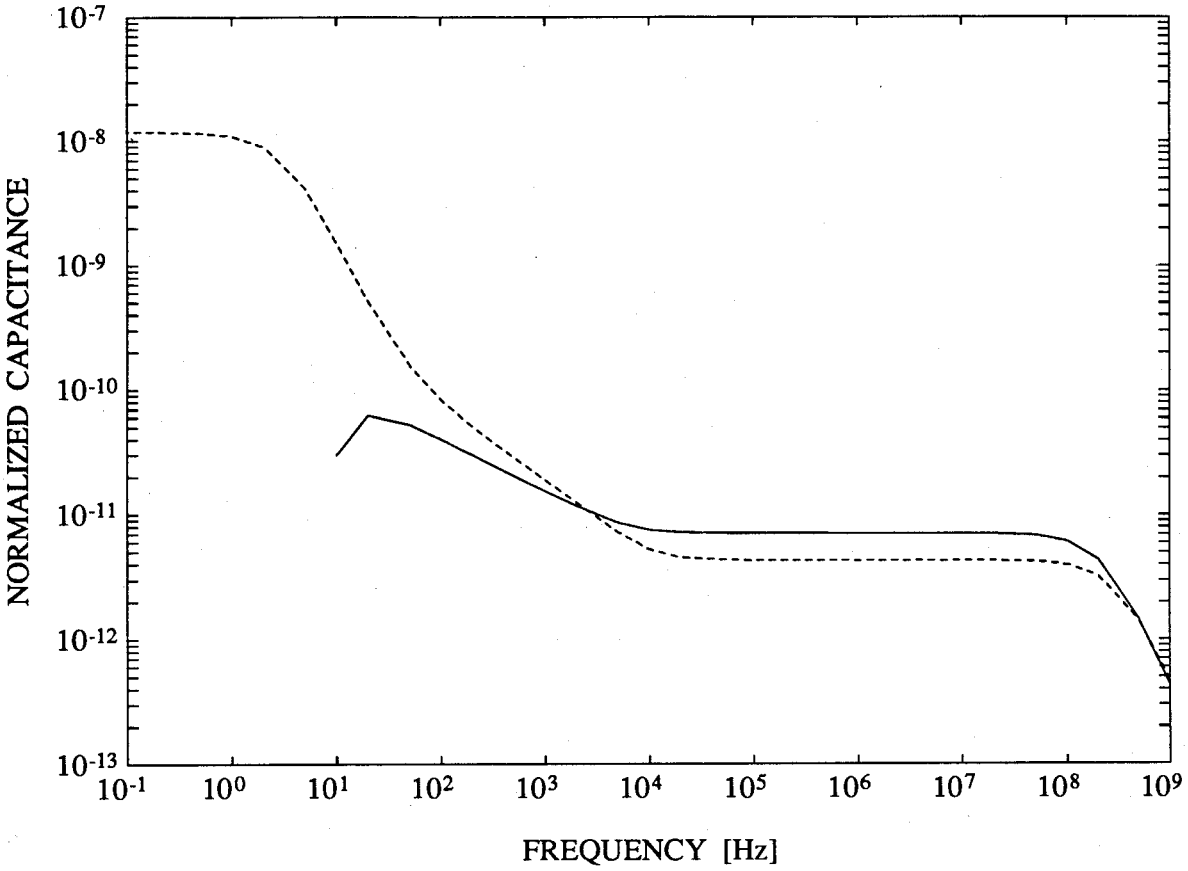


Figure 4.46: Frequency dependence of the capacitance of the SI structure calculated using eq. (4.64). The dashed line corresponds to the capacitance in the presence of hole injection (η=1) and the solid line to the capacitance when no hole injection occurs (η=0). The rest of the parameters are given in Fig. 4.41.

trapped charge. At 1Hz most of the injected carriers will be trapped which results in low conduction. At high frequencies few injected carriers are immobilized in traps and thus most contribute to the free carriers resulting in higher conduction.

Fig. 4.45 shows that at low frequencies the conductance is reduced in the presence of hole injection. This is because the injected holes attract the much more mobile electrons to the vicinity of a hole-injecting contact. At low frequencies the spatial distribution of injected free electrons resembles the distribution of free holes, as a result of the attempt to preserve local space charge neutrality. This results in a diffusion of the electrons in the same direction as the holes, thus decreasing the total current and, consequently, the admittance [41]. At higher frequencies this phenomenon is eliminated due to the fact that the free carrier distribution is determined by zero local recombination. This

results in the frequency response being insensitive to hole injection. At low frequencies in the presence of hole injection both the hole and electron traps play an important role in determining the charge distribution as shown in Chapter 3 and in Ref. [80], and, therefore, their frequency responses determine the frequency dependence of the conductance. The conductance starts to increase at about 0.4 Hz, which corresponds to the time constant associated with the hole trap τ_T^A. This is due to the fact that a reduction in the hole trap density in the presence of hole injection will increase the conductance [41]. This increase saturates at about 5 Hz, which corresponds to the time constant associated with the electron trap τ_T^D. This is because at this frequency the electron trap density starts to decrease, and thus compensates the reduction of the hole trap density. In the absence of hole injection an ohmic conduction will dominate the transport in SI GaAs at low frequencies, and therefore the frequency response of the deep levels has almost no effect on the conductance as can be seen in Fig. 4.45. There is another bump on the conductance curves, which occurs between 1 kHz and 50 kHz. This frequency range is determined by the frequencies at which $|\beta| = A_n b$ and $|\alpha| = A_n$. The first frequency can be evaluated to be $f_1 \approx \sqrt{1/(\tau_n^D A_n b)^2 - 1/(\tau_T^D)^2}/2\pi$, and the second one is $f_2 \approx \sqrt{1/(\tau_p^A A_n)^2 - 1/(\tau_T^A)^2}/2\pi$. Note that f_1, f_2 depend on the traps characteristics through $\tau_{n,p}$ and τ_T, and on the mobility and lifetime through A_n. The conductance increases a few orders of magnitude in the MHz frequency range and then saturates with frequency. The sharp increase begins at about 0.5 MHz when $|L\sqrt{\nu}| \approx 1$, and ceases at about 0.5 GHz when $|\beta| \approx 1$. Clearly, the frequency at which the conductance starts to increase depends not only on the frequency response of the deep levels, but also on the distance between two electrodes: it decreases as the distance decreases. If hole traps are not included in the simulation, or their density is greatly reduced the discrepancy in the curves due to hole injection vanishes. If several electron traps are included in the simulation, their effect on the admittance can be examined in terms of their contribution to β which dominates over α because for an electron trap $\beta \gg \alpha$ due to the difference in the trap capture cross-sections for holes and electrons. In the absence of hole injection the trap with the highest density will normally be dominant at frequencies up to the corresponding $1/\tau_T$, after that the dominance is transferred to the trap with the second largest density, which has a higher frequency response, etc. Thus in this case a low-density trap would determine the admittance behavior in a

certain frequency region, if it outlived rest of the higher-density traps. A shallow electron trap will normally have a higher frequency response than a deep electron trap, if both of them have similar cross sections for electrons. Therefore, inclusion of a shallower electron trap in addition to EL2 will result in the strong increase of the conductance starting at higher frequencies.

Fig. 4.46 depicts the frequency dependence of the capacitance. In the presence of hole injection the capacitance starts to decrease at about 5 Hz, which corresponds to τ_T^D and then saturates at about 50 kHz, which corresponds to f_2 discussed above. At low frequencies the capacitance increases with hole injection, because the latter forms a trapped charge dipole in the vicinity of the hole-injecting electrode [80]. As in the case of conductance, not including hole traps in the simulation results in the curve which is insensitive to hole injection. The resultant shape of the curve is similar to that shown in Fig. 4.46 in the presence of hole injection: namely it exhibits the transition of the capacitance from high to low values, which was observed in silicon p-n junctions with deep traps [51, 69]. As shown in Fig. 4.46 at higher frequencies the capacitance becomes insensitive to hole injection.

The results presented in Figs. 4.45 and 4.46 are in good agreement with experimental data for SI GaAs [32], namely small bumps on the conductance curves, that can be seen at low frequencies and high temperatures and a drastic increase in the conductance at higher frequencies (Fig. 3 in [32]), and a transition of the capacitance from the high to low values (Fig. 4 in [32]). Although Pistoulet *et al.* [32] explained some of the results in terms of their potential fluctuations theory, our work shows that the principal features of their data for SI GaAs can be reproduced by solving continuity and Poisson's equations in the frequency domain. The validity of our results becomes questionable at frequencies above the reciprocal of carrier lifetime, which is about 20 MHz in our calculations. However, the sharp increase in the conductance was shown to be dependent on the distance between the electrodes and on the traps characteristics, and it is possible to show that by changing these parameters the strongly transitional region of the conductance can be shifted to lower frequencies in which our analysis is definitely valid.

Physically the sharp increase in the conductance in the MHz range occurs probably due to the fact that the SI GaAs transforms in this frequency range from a lifetime semiconductor to a relaxation semiconductor. Because of zero-field boundary conditions only a diffusion component of the total

current plays a role in determining the conductance. At low frequencies there is quasi-neutrality of excess free carriers in the SI GaAs: the excess holes and electrons have similar distribution in space, and, consequently, the hole and electron diffusion currents have opposite signs, decreasing the total current. With increasing frequencies the shape of the excess free holes and electrons change from being similar to a mirror image (with unequal magnitudes). Thus at higher frequencies the diffusion currents of holes and electrons sum up, increasing the total current.

In conclusion, the free and trapped carrier profiles and the potential profile in SI GaAs were found to be frequency-dependent. At lower frequencies the material behaves like a *lifetime* semiconductor, in which electrons are trying to neutralize the injected holes. At higher frequencies charge separation occurs, typical of *relaxation* semiconductors. It was shown that the local space charge neutrality is not preserved in both low and high frequencies. It was found that up to about 100 kHz the admittance can be represented by an equivalent circuit consisting of a frequency-dependent conductance and a more strongly frequency-dependent capacitance. At low frequencies the conductance decreases, while the capacitance increases in the presence of hole injection. At higher frequencies the conductance increases by a few orders of magnitude. This increase occurs at lower frequencies for shorter distances between the contacts. The comparison between the structures with two ohmic contacts and the structures with one ohmic and one Schottky contact reveals that their admittances differ at very low frequencies but are very similar at higher frequencies.

4.4 Applications to AC sidegating

The above results indicate an increase of a few orders of magnitude in the SI GaAs conductivity in the kHz-MHz range, depending on the trap parameters and device geometry. The increase in the conductivity will be higher and will be stretched over a wider frequency range by decreasing spacings between devices. Thus, in addition to the DC sidegating effect due to hole injection or space-charge-limited currents in the SI substrate, discussed in Chap. 2, a strong AC sidegating effect may exist. This effect has been overlooked, probably because for GaAs MMIC's capacitive coupling is assumed as the only way of crosstalk, while for GaAs digital integrated circuits only DC sidegating has been investigated. However, for wide-bandwidth circuits, such as operational amplifiers this effect cannot

be ignored. Furthermore, switching waveforms in digital circuits will normally have higher frequency harmonics besides DC components, which may affect significantly the crosstalk between devices. In [94] we analyzed AC sidegating in GaAs MESFETs and the calculated results, shown there, while they agreed with trends in the experimental data, underestimated the magnitude of the crosstalk. These calculations were based on the parameters evaluated from DC measurements: specifically the substrate admittance was evaluated from DC measurements. However, considering the frequency dependence of the admittance of the GaAs SI substrate, presented in this chapter, it is clear that the admittance might have been a few orders of magnitude larger than its DC value, resulting in a better agreement of the calculations with the experimental results.

In the next Chapter we will see applications of the results derived in this section to modeling of the output conductance of GaAs MESFETs on SI substrates.

4.5 Summary

By extending to the frequency domain the analysis of transport in semi-insulating GaAs two-terminal structures, in which one terminal injects only electrons and the other may inject holes, closed form solutions were obtained for AC charge and potential distribution under conditions of low-level injection. The presence of deep traps results in frequency dependence of both the excess free and trapped carriers. At low frequencies free electrons move so as to neutralize injected holes, but at higher frequencies charge separation of free carriers through the zero local recombination, typical of relaxation semiconductors, occurs. The corresponding admittance can be represented by an equivalent circuit consisting of a frequency-dependent conductance in parallel with a frequency-dependent capacitance. At very low frequencies the conductance decreases with increasing hole injection. At higher frequencies it increases and then saturates with frequency. At low frequencies the capacitance is a strongly decreasing function of frequency. At higher frequencies the admittance depends only weakly on the hole injection ratio.

Although we focus on semi-insulating GaAs, the equations presented are in a general form, which is applicable to the frequency-dependent transport in a variety of other semiconductors under conditions of low-level injection.

Chapter 5

Modeling frequency dependence of the output conductance of GaAs MESFETs

5.1 Introduction

The output conductance of a GaAs MESFET is one of the major parameters, which determine device performance, and, consequently, its variation with frequency has attracted the attention of many researchers recently [93, 97–99]. In these papers the output admittance is modeled as a single time constant (zero-pole) function. Although this function can be tailored to fit the variation with frequency of the output admittance magnitude, the phase change calculated using this approach is greatly overestimated [93, 45], suggesting a more complicated behavior in the frequency domain. The numerical simulations of the output conductance dispersion provide more understanding of the phenomenon [6, 100], but do not produce an adequate model for circuit simulation.

5.2 Modeling

The frequency dispersion of the output conductance, expressed as a drain-lag effect in the time domain [45], has been widely ascribed to the channel-substrate interface [93, 97, 6, 101]. To illustrate the channel-substrate interaction consider the cross-section of a GaAs MESFET shown in Fig. 5.47. The conductive channel is bounded by the gate and channel-substrate depletion regions. The saturation current in GaAs MESFETs, assuming a constant electron concentration N_D, is given in the velocity saturation region by:

$$I = qN_D Z v_s (A - d - h) \tag{5.65}$$

where q is the magnitude of the electron charge, Z is the device width, d is the thickness of the gate depletion region, h is the extension of the channel-substrate depletion region into the channel, and v_s is the saturation velocity. Using the abrupt depletion region approximation, we evaluate d and h at the drain edge of the gate ($l_1 = l_{sg} + l_g$ in Fig. 5.47):

$$d = \sqrt{\frac{2\epsilon(V_{BSC} + V_{DST} - V_G)}{qN_D}} \tag{5.66}$$

$$h = \sqrt{\frac{2\epsilon(V_{BCS} + V_{DST} - V_{SB}(l_1))N_A}{qN_D(N_A + N_D)}} \tag{5.67}$$

where ϵ is the permittivity, V_{BSC} is the Schottky gate built-in voltage, V_{DST} and V_{SB} are the channel and substrate voltages respectively at l_1, V_{BCS} is the built-in voltage of the channel-substrate interface, V_G is the gate voltage, and N_A is the sum of density of shallow and deep acceptors [70]. We can write the drain conductance as:

$$G_d = -qN_D Z v_s \left(\frac{\partial d}{\partial V_{DS}} + \frac{\partial h}{\partial V_{DS}} \right) \tag{5.68}$$

The first term in the brackets is due to the displacement of the velocity saturation point and the consequent channel widening [102]. The second term represents the modulation of the width of the channel-substrate depletion layer through the SI substrate by a drain voltage, and can be interpreted as an electrostatic drain feedback effect [103]. Although the potential profile in the channel changes

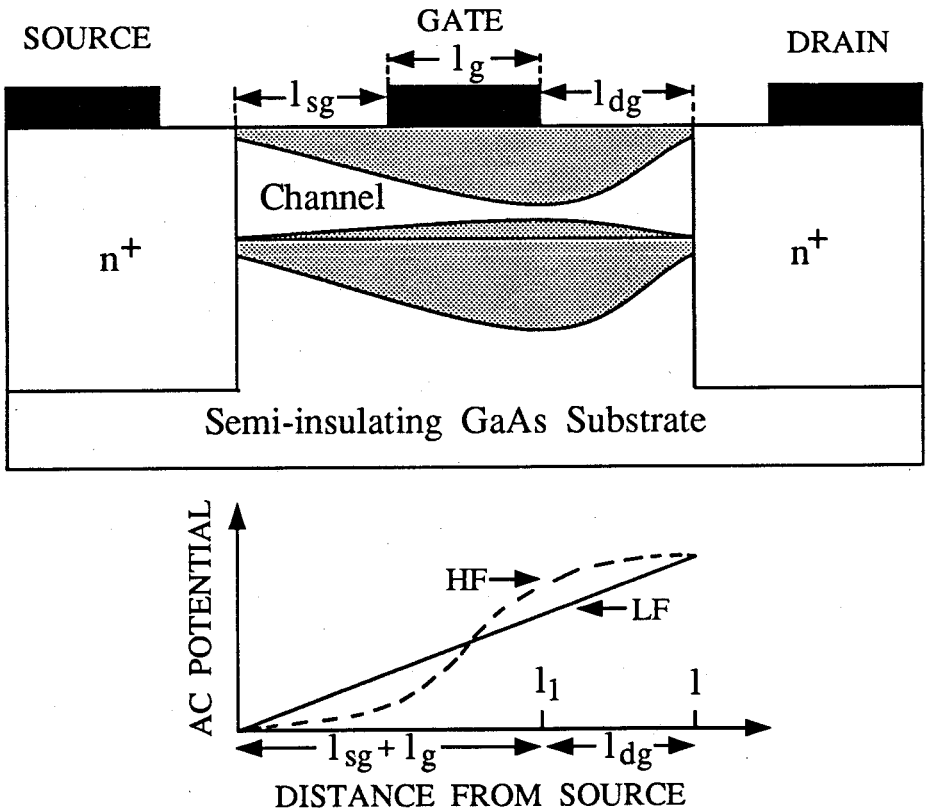


Figure 5.47: Schematic cross section of a MESFET and an AC potential profile across the drain-substrate-source region. LF corresponds to the profile at low frequencies, HF at high frequencies.

with the drain voltage, its variation is much weaker than that in the substrate, and, therefore, we assume that the modulation of h is due to the latter only. As we shall see in the following analysis, the potential distribution across the drain-substrate-source region is frequency-dependent, as shown in Fig 5.47, and, thus, the modulation of the width of the conductive channel, and, consequently, the output conductance depend on frequency.

Our analysis is restricted to drain voltages which satisfy the condition of low-level injection into the substrate. In non self-aligned transistors the typical distance between source and drain is about 3–6 μm, and for such distances two-dimensional numerical analysis of n-SI-n structures predicts high-level electron injection occurring at voltages larger than 5 V [56]. Abrupt current increase in such structures has been reported previously at lower voltages, but it has been attributed to surface effects [104]. We, however, consider the SI region under the channel, which is not normally affected by the surface states, particularly in large-geometry devices. An analytic expression for the potential distribution in one-dimensional SI GaAs structures has been obtained previously by solving the time-dependent continuity equations for holes and electrons and Poisson's equation under conditions of low-level injection, without further assumptions such as space charge neutrality and neglect of the diffusion component of the current [105]. The solution is restricted to the range of frequencies below the reciprocal of the carrier lifetime in GaAs, which is sufficient for discussing the frequency-dependent effects in GaAs MESFETs. This restriction is not necessary for obtaining analytic expressions, but greatly simplifies them. For the boundary conditions of zero field and zero hole current, the obtained DC potential profile is almost insensitive to the substrate properties, exhibiting nearly linear distribution [80]. But the AC potential profile, given by in the following expression, is frequency-dependent and is sensitive to the density and location in the energy band of the traps in the SI material [105].

$$\tilde{V_{sb}}(x,w) = A\{M\left[x - \frac{\cosh(x\sqrt{\nu}) - \cosh((l-x)\sqrt{\nu}) + \cosh(l\sqrt{\nu})}{\sqrt{\nu}\sinh(l\sqrt{\nu})}\right] + \frac{P_e[(1+\alpha)M - 1 - \beta]}{A_n(P_e+b)}\left[\frac{\cosh(x\sqrt{\xi}) - \cosh((l-x)\sqrt{\xi}) + \cosh(l\sqrt{\xi})}{\sqrt{\xi}\sinh(l\sqrt{\xi})} - x\right]\} \tag{5.69}$$

with

$$\nu = [P_e(1+\alpha) + (1+\beta)]/(1+P_e),$$

$$\xi = A_n(P_e + b)/(1 + P_e),$$

$$M = (1 + \beta - A_n b)/(1 + \alpha - A_n),$$

$$\alpha = \tau_T/[\tau_p(1 + jw\tau_T)],$$

$$\beta = \tau_T/[\tau_n(1 + jw\tau_T)],$$

where

$$1/\tau_T = c_n n_e + e_n + c_p p_e + e_p,$$

$$1/\tau_n = c_n N_T n_1/(n_e + n_1),$$

$$1/\tau_p = c_p N_T n_e/(n_e + n_1),$$

w is the angular frequency, N_T is the density of a deep level, e_n, e_p are the emission rates of a deep level for electrons and holes, c_n, c_p are the capture probabilities of a deep level for electrons and holes, n_e, p_e are the equilibrium electron and hole concentrations, $P_e = p_e/n_e$, n_1 is the electron density if the Fermi level were at the energy level of the deep level, l is the drain-source spacing. In (5.69) the distance x is normalized to $\sqrt{\epsilon kT/q^2(n_e + p_e)}$, and the parameter A can be determined by the drain voltage.

Substituting (5.69) into (5.68) and separating the obtained result into DC and AC parts yields the AC component of the drain admittance:

$$g_d = \frac{Zv_s\left[\tilde{V}_{sb}(l_1, w) - \tilde{V}_{sb}(l_1, 0)\right]}{\tilde{V}_{sb}(l)} \sqrt{\frac{q\epsilon N_A N_D}{2(N_A + N_D)(V_{BCS} + V_{DST} - V_{SB}(l_1))}} \tag{5.70}$$

The drain conductance is given by the real part of (5.70). The parameter V_{DST} will depend on the device geometry: in non self-aligned devices biased in saturation most of the drain voltage is dropped across the gate-drain region, and, therefore, V_{DST} is only slightly higher than the saturation voltage, but in self-aligned transistors this will not be the case [106]. Therefore, in this work V_{DST} is used as a fitting parameter. The DC component of the output conductance can be evaluated from DC I-V characteristics, and the total output conductance is thus obtained by summing up the AC and DC components. The resulting equivalent circuit of a MESFET is shown in Fig. 5.48. In Fig. 5.48 R_0 is the DC output conductance, g_m is the transconductance, g_d is defined in eq. (5.70), R_{sub} and C_{sub} represent the substrate admittance, which is due to the conduction between source and drain through the SI substrate [105]. Note that the above equivalent circuit includes frequency-dependent

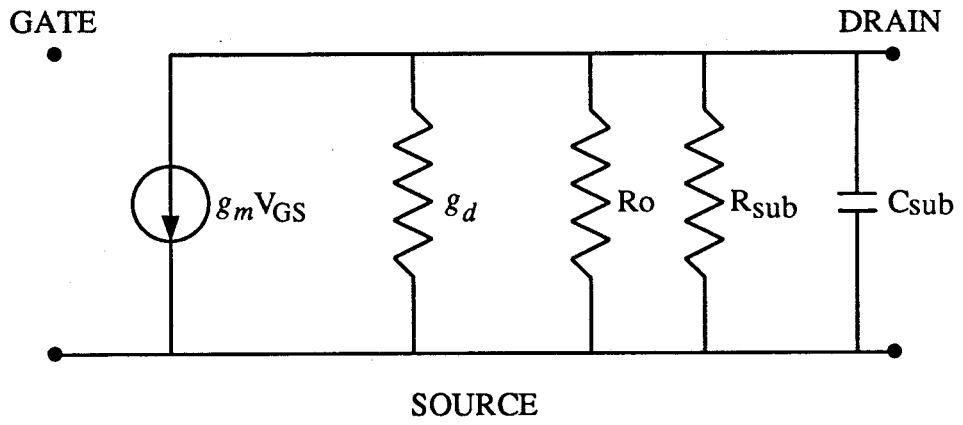


Figure 5.48: Small-signal equivalent circuit of a GaAs MESFET at low frequencies.

elements g_d, R_{sub} and C_{sub}, and in that it is different from the previously proposed circuits, for example, the ones suggested by Scheinberg *et al.* [107] and by Lee and Forbes [98]. The output admittance is given by:

$$Y_{out} = \frac{1}{R_o} + \frac{1}{R_{sub}} + jwC_{sub} + g_d \tag{5.71}$$

In comparison to other models our model has a certain degree of predictability, since its inputs are parameters of the traps that are present in the SI substrate and device geometry.

5.3 Comparison with experimental and numerical data

The analysis of the AC potential distribution across the source-substrate-drain structure under conditions of low-level injection is valid for a wide range of drain voltages, and, therefore, it can be used for investigation of drain-lag effects and AC I-V characteristics. This is confirmed by the fact that the drain current overshoot and the drain conductance dispersion were observed at drain voltages as low as 1 V [101, 99], indicating that these phenomena are not originated, but perhaps enhanced, by high-level injection into the SI substrate. To test the validity of the model, we examine first if it predicts the major trends in device behavior.

According to the model the frequency-dependent component of the drain conductance increases with the acceptor density in the substrate in agreement with numerical simulations [6]. However, controversial results have been reported regarding the effect of a buried p layer beneath the channel:

while it is established that the buried layer improves DC characteristics of GaAs MESFETs, there is no consensus whether it reduces the AC/transient-dependent effects [108, 101]. Our model predicts that a p layer slightly beneath the channel will increase the frequency dependence of the drain conductance through the increase of the shallow acceptor density, while it will not affect the frequency-dependent potential distribution in the substrate, altogether making the frequency dispersion of the output conductance even worse. But a deep implant, which provides in addition to the depletion layer a conductive layer beneath the channel, will eliminate the frequency dependence. This is in agreement with the reported experimental data: when a deep implant was used no drain current transients were observed [109, 108], but when a shallow implant was used in order to keep the p-layer completely depleted, the drain current transients increased [101].

To examine AC I-V characteristics we replace the DC voltage $V_{SB}(l_1)$ in (5.67) by its AC value evaluated from (5.69). The resultant eq. (5.65) yields a higher current, since $\tilde{V_{sb}}(l_1)$ increases with frequencies in the low-frequency range. This is in agreement with the measured data, which indicate larger saturation currents at kHz range [98, 99]. According to the AC potential profile shown in Fig. 5.47, it is possible to devise structures, for which the frequency-dependent effects are reduced. Minimum effect will occur when the drain side of the gate is about the middle of the drain-source distance, that can be expressed as: $(l_{sg} + l_g)/l_{dg} \approx 1$. Maximum effect will occur when the drain side of the gate is about $l/4$ from the drain, that can be expressed as: $(l_{sg} + l_g)/l_{dg} \approx 3$. The predictions of this simple analysis are in agreement with experimental data of drain current overshoots as a function of gate-drain and gate-source spacings [101]. The results of this analysis for MESFETs with and without p-type buried layer are visualized in Fig. 5.49.

Direct comparison between our model and measured data requires knowledge of substrate properties. The analysis is further complicated by the fact, that in the substrate region beneath the channel, in addition to the presence of the traps, originated in as-grown SI substrates, deep levels may be induced by processing [110]. Our model allows incorporation of multiple non-interacting traps in the analytic expression for the AC drain conductance as described in [80, 105]. We have compared our results with the numerical and measured data extracted from [111, 100]. The numerical analysis suggested that in addition to EL2, there is a shallower electron trap, which plays a role in

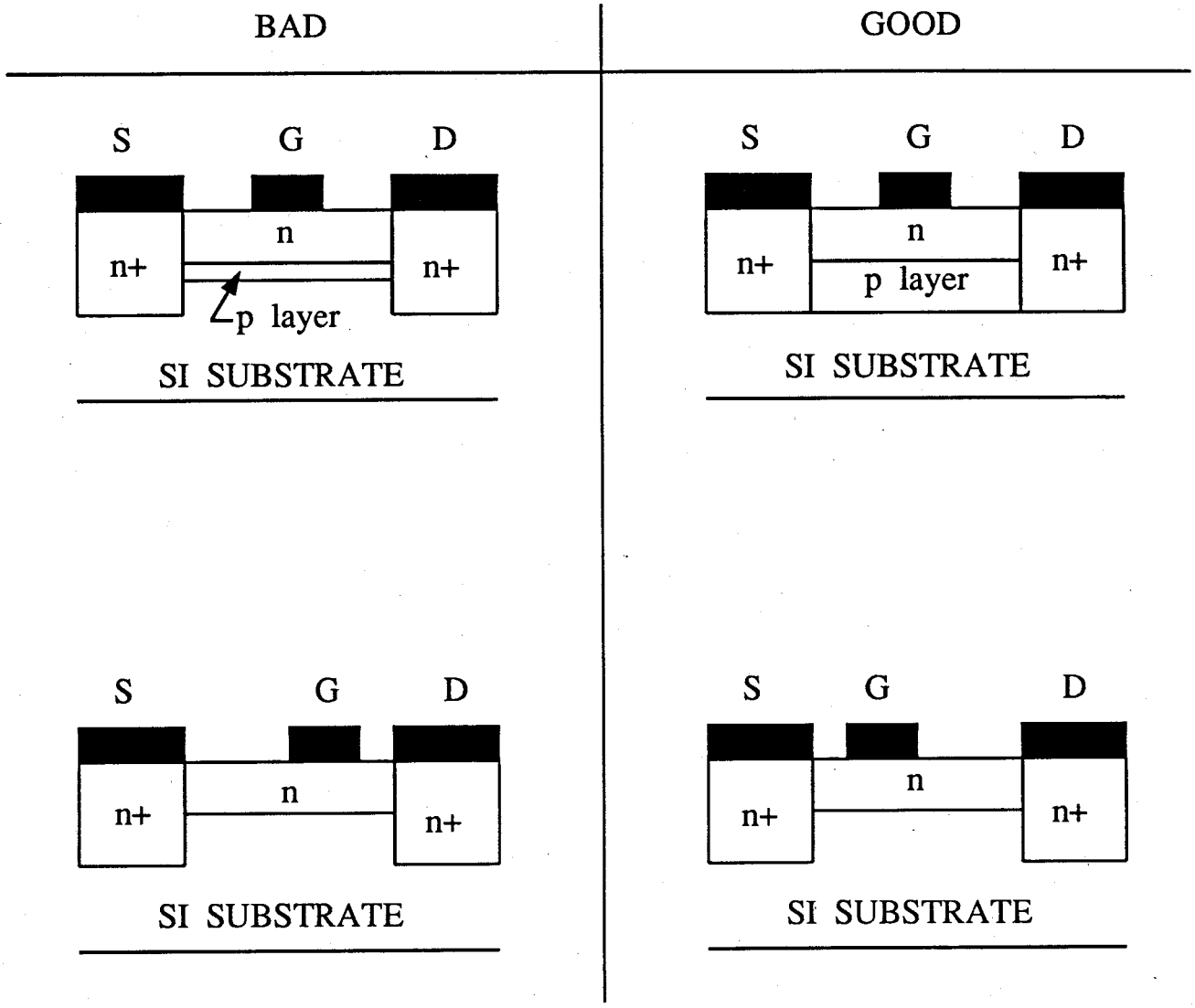


Figure 5.49: The impact of the device structure on the frequency dependence of the output admittance. The first row shows MESFETs with a p-type buried layer. A deep p layer reduces the frequency dependence, while a shallow p layer may increase it. The second row shows the effect of the gate location on the frequency-dependent output admittance: placing gate closer to the source enhances the frequency dependence, while placing it closer to the source may reduce the effect.

the frequency-dependent effects [100], and, consequently, we used similar parameters to those in the numerical simulation. Our results, calculated by (5.70), are in very good agreement with the numerical and measured data, as shown in Fig. 5.50. Not shown in Fig. 5.50, but noteworthy, is the fact that the phase variation over the frequency range $1 - 10^5$ Hz , calculated by (5.70), is less than 2^o.

We have examined the temperature effects by considering temperature-dependent emission rates for EL2 [112]: $e_n = 2.83 \times 10^7 T^2 exp(-0.814/kT)\ s^{-1}$ and $e_p = 10^{-3} e_n$, and the temperature

dependence of the carrier concentration and the EL2 energy level. Fig. 5.51 shows drain conductance versus frequency at two different temperatures, calculated by (5.70) assuming only one deep level (EL2) in the substrate, together with the measured data extracted from [99]. Our results reflect the trend in device behavior, which is the shift of the frequency-dependent region of the drain conductance to higher frequencies at higher temperatures. Experimental results indicate a smoother increase in the drain conductance, suggesting presence of additional traps in the substrate.

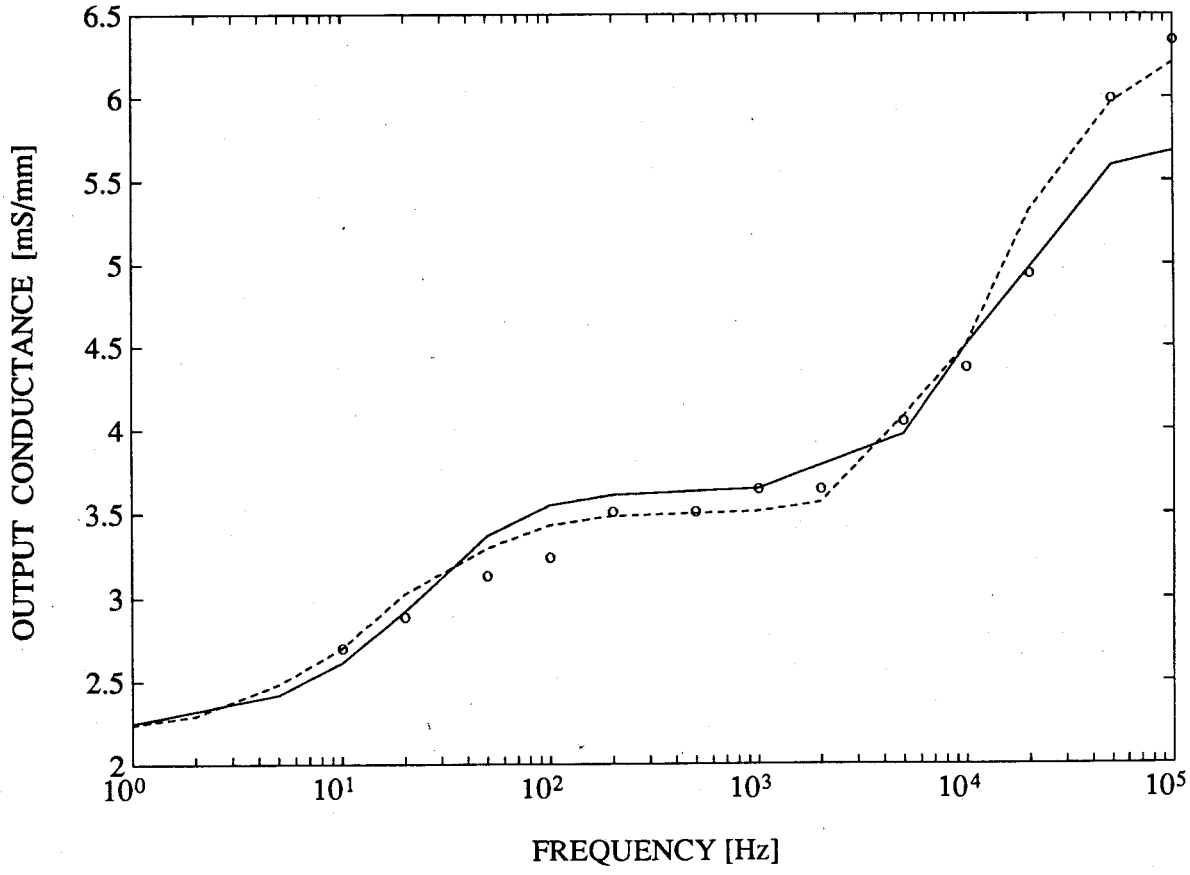


Figure 5.50: Drain conductance vs. frequency. Results of the present model (solid line) are superimposed on numerical results (dashed line) [7], and experimental data (circles) [20]. Parameters used: T = 300 K, $N_D = 10^{17}cm^{-3}$, $N_A = 6 \times 10^{15}cm^{-3}$, $V_{DS} = 2.5V$, $V_{DST} = 1.45V, l_{sg} = l_{dg} = 1\mu m, l = 1.2\mu m$, $n_e \approx 7 \times 10^7 cm^{-3}, p_e \approx 10^5 cm^{-3}$, for trap at 0.69 eV;$N_1 = 5 \times 10^{16}cm^{-3}$, $\sigma_{n1} = 2 \times 10^{-14}cm^2$, $\sigma_{p1} = 2 \times 10^{-18}cm^2$, for trap at 0.5 eV;$N_2 = 5 \times 10^{15}cm^{-3}$, $\sigma_{n2} = 5 \times 10^{-13}cm^2$,, $\sigma_{p2} = 5 \times 10^{-17}cm^2$.

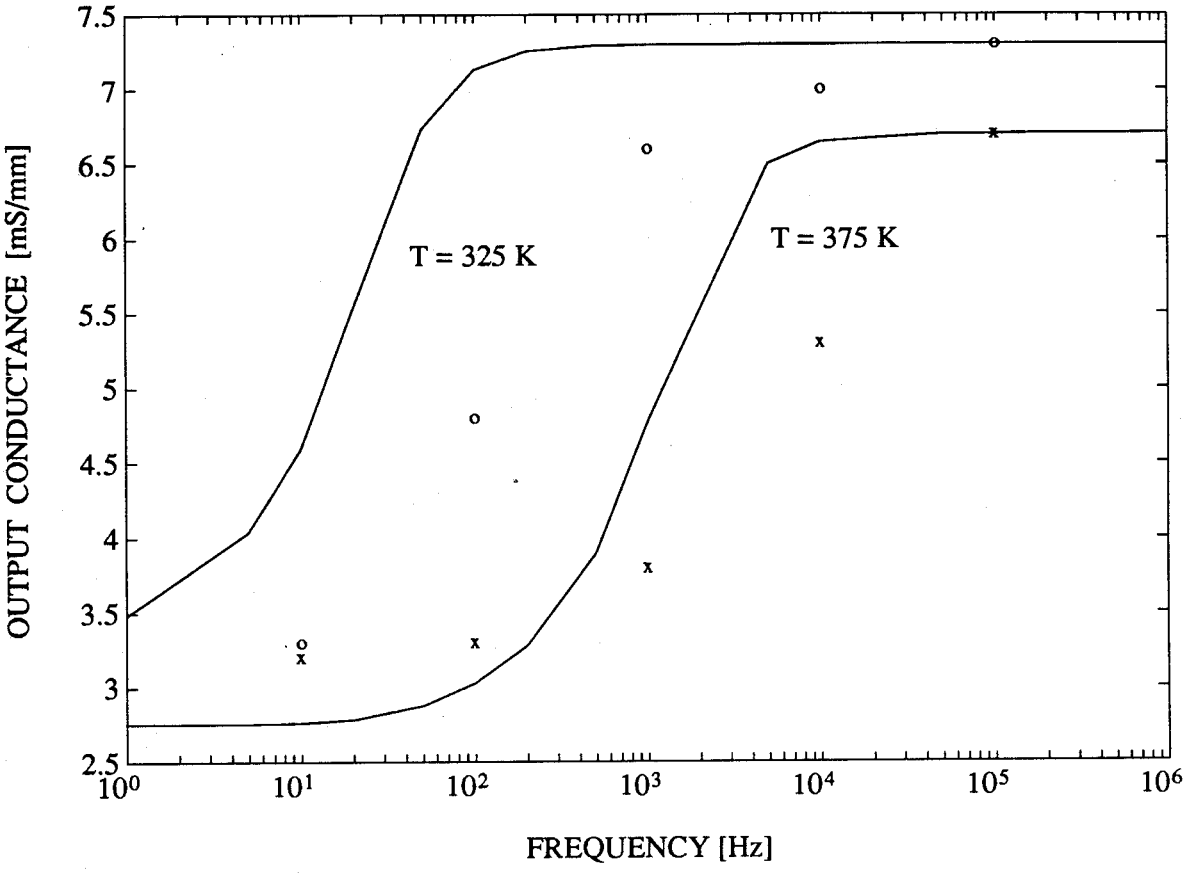


Figure 5.51: Drain conductance vs. frequency at 325 K and 375 K. Results of the present model (solid line) are superimposed on experimental data (circles and asterisks) after Canfield et. al [4]. Parameters used: $N_{EL2} = 5 \times 10^{16} cm^{-3}$, $N_A = 5 \times 10^{15} cm^{-3}$, $l_{sg} = l_{dg} = l_g = 1\mu m$, $V_{DS} = 3V$, $V_{DST} = 1.6V$.

In conclusion, physically based model of the frequency-dependent drain conductance has been developed. It allows an examination of the impact of device geometry and substrate properties, particularly the presence of multiple traps, on GaAs MESFET characteristics. The model reflects major trends in the output admittance, namely: low-frequency dependence, temperature dependence, negligible phase variation, dependence on drain voltages. Being analytical, it should be useful for circuit simulations.

5.4 Summary

The small-signal output conductance of GaAs MESFETs on SI substrates is known to exhibit

frequency dependence. So far this phenomenon has been modeled using equivalent circuits and numerical techniques. In contrast, we propose an analytical physically-based model. The model accounts for alteration of the thickness of the conductive channel through the channel-substrate junction modulation by the drain voltage. Because of the presence of deep levels the AC potential distribution across the SI material between drain and source will be frequency dependent, and, consequently, will result in a different AC voltage drop across the channel-substrate interface at different frequencies. This will result in a change of the output conductance with frequency.

A closed form for the AC potential distribution across the SI material was obtained by solving the continuity equations for holes and electrons plus Poisson's equation under conditions of low-level injection and low frequencies without some commonly used assumptions, such as local space-charge neutrality, neglect of recombination, and diffusion or drift component of the current. The solution for the AC potential distribution is affected by the density and location of deep levels in the SI substrate, and can be easily extended to the general case of non-interacting multiple traps. Thus, the model provides a tool for investigating the effect of trap parameters on the frequency characteristics. It reproduces experimentally observed and numerically simulated results for the output conductance. Being analytical, the expression for the frequency-dependent output conductance is suitable for incorporation in circuit simulators.

Chapter 6

Conclusions

The majority of text books on semiconductor devices are based on the research spanning the last four decades on silicon. Many concepts developed for and commonly used in the silicon device theory, such as space charge neutrality, neglect of recombination in short structures etc. are entirely misleading when dealing with GaAs devices on SI substrates. This is due to the fact that trap densities in SI GaAs are much higher than in Si, while carrier lifetimes are much shorter. Examining eqn. (3.34) leads to the conclusion, that under non-equilibrium conditions space charge neutrality in SI GaAs is rather an exception than a rule, and occurs only when the concentrations of excess trapped holes and electrons are equal. Van Roosbroeck , who introduced the concept of ambipolar transport to the semiconductor theory [113] , based on local quasi-neutrality of the excess free carriers, was the one (with Casey), who classified some of the materials as relaxation semiconductors, in which separation of the excess free electrons and holes is established through zero local recombination [95]. In addition, ambipolar approach omits from the analysis the Poisson's equation [114]. This omission is not justified for SI GaAs, in which the excess trapped carrier densities are much higher than the excess free carrier densities. The ambipolar approach is commonly used in analysis of silicon devices [114]. In comparison to silicon SI GaAs has much higher resistivity and much shorter lifetimes. The clues for different treatment of such materials were discussed by McKelvey [115]. But since at the time these materials were not a part of the mainstream research effort, many of the conclusions regarding them have been overlooked. One of the main conclusions of my work is that many concepts developed for Si should be reexamined when talking about the GaAs technology. The borrowing of concepts from Si technology may lead to severe errors in understanding GaAs devices on SI substrates.

In Chapter 1 the use of MESFET as a tool for investigating of the interaction with the SI substrate of more complicated devices was suggested. It is interesting to note that the gate, which was identified as one of the main players in the sidegating effect in MESFETs [43], was also found to play a major role in the sidegating effect in HEMTs [116]. Sidegating remains the major obstacle

to fabrication of high density GaAs integrated circuits [5]. This work contributes to understanding and modeling of this problem by:

1. Identification of hole injection from the gate as one of the possible sources of sidegating. The hole injection from the portion of the gate on a *SI substrate* was shown numerically by Goto *et al.* [83] and experimentally by Liu *et al.* [58] to play an important role in sidegating. Our results show the possibility of hole injection from the gate on a *doped channel* and also provide a new interpretation of the results in Refs. [83] and [58], namely, appearance of hysteresis as a result of a strong hole injection into the SI substrate and the effect of weak hole injection on sidegating.
2. Identification of the role of recombination processes and, consequently, recombination centers (that are different from EL2) in sidegating.
3. Application of the analysis of low-level injection reported first by Manifacier and Henisch [41] to sidegating problem. Low-level analysis has not been applied before to sidegating, since it is usually assumed that "nothing happens" under these conditions because the carrier transport is dominated by ohmic conduction. This work shows that even though the I-V characteristics may be nearly ohmic, many physical processes may occur under conditions of low-level injection resulting in such effects as non-linear voltage distribution across a SI substrate. The processes leading to such behavior have been discussed in this work. The resultant non-linear potential profiles were used to explain sidegating at low sidegate voltages and long range sidegating.
4. Providing close form expressions for the potential distribution across a SI GaAs substrate and the output admittance of GaAs MESFETs on SI substrates, which should be useful in circuit simulations.
5. Extension of the low-level injection analysis to the frequency-domain.
6. Application of the above analysis to modeling the frequency dependence of the output impedance.
7. Investigation of sidegating in the frequency domain (AC sidegating). It was shown that a strong sidegating effect may exist due to inherent properties of SI GaAs. While it was shown that hole injection plays an important role in the DC sidegating effect, the sidegating effect in the kHz-MHz range does not depend on hole injection and does not require specific biasing conditions [105]. This effect will have most impact on wide-band circuits used in analog and mixed analog-

digital systems. The analysis of sidegating in the frequency domain can also be used as a tool for separating various processes occurring at the same time in sidegating effect, since they are expected to have different frequency responses.

The results presented in Chapters 3–5 indicate that device characteristics depend strongly on the substrate properties which, in turn, are determined by trap parameters. Under non-equilibrium conditions even shallow traps may affect the device characteristics. Thus different combinations of multiple trap parameters will result in different device behavior [117]. Even if the properties of the as-grown substrate are completely controlled, additional traps may be induced by processing steps. Despite the difficulties in obtaining reproducible performance for devices on SI substrates, the continuation of this work is necessary because there will be always demand for GaAs technology, particularly in optoelectronic circuits [118]. The problems may not be solved, but understood, and, consequently, predicted (=modeled) and controlled. It is possible that innovative circuit techniques will contribute to this. Future work may include:

1. Measurements of and modeling the hole injection from the gate of a GaAs MESFET. This means more studies towards understanding of the nature of Schottky contacts on GaAs, particularly the effect of a Schottky contact area on hole injection.
2. Incorporation of the results of Chapter 4 in investigating crosstalk in GaAs integrated circuits.
3. In Chapter 1 sidegating was presented as a three-dimensional effect. Therefore, the extension of the existing one-dimensional analysis to two and three dimensions by numerical techniques should provide more insight into sidegating.
4. Extension of the low-level injection analysis into the time domain.
5. Extracting the trap parameters from the AC measurements of the conductivity of a SI GaAs substrate.
6. Identification and characterization of recombination centers, which is according to my work as important as an investigation of EL2.
7. Sidegating is known to be a temperature-dependent effect [119], and, therefore, the results presented here should be analyzed as a function of temperature.

8. In this work the effect of deep levels in the SI substrate on the drain conductance was investigated. Their effect on the transconductance, which is known to degrade under high frequency operation [120], should be investigated.
9. Implementation of the analytical model of the drain admittance in SPICE (circuit simulator).
10. Development of circuit techniques to avoid sidegating.

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Appendix A Potential distribution in the uniform channel

The solution of (2.16) is given by:

$$v(x) = Ce^{px} + De^{-px} + B/A\,, \tag{A.72}$$

where $p = \sqrt{r_{chs}[jw(c_{js} + c_s) + y_s]}$,$A = [jw(c_{js} + c_s) + y_s]r_{chs}$,$B = (jwc_s + y_s)r_{chs}v_{sg}$ and C, D are constants to be determined by the boundary conditions. The current in the channel is given by:$i(x) = -[1/r_{chs}(\partial v/\partial x)]$.

Appendix B Potential distribution in the exponentially tapered channel

Assuming $wc_j(x) \gg wc_s, y_s$ and $\alpha = \beta$, eqn (2.15) transforms into:

$$\frac{\partial^2 v}{\partial x^2} - \alpha \frac{\partial v}{\partial x} - jwr_{cho}c_{jo}v = -r_{cho}e^{\alpha x}(jwc_s + y_s)v_{sg} \,. \tag{B.73}$$

The solution is given by:

$$v(x) = (jwc_s + y_s)e^{\alpha x}v_{sg}/jwc_{jo} + Ee^{[(p+\alpha/2)x]} + Fe^{[(\alpha/2-p)x]} \,, \tag{B.74}$$

where E and F are constants to be determined by the boundary conditions. The current in the channel is given by: $i(x) = -(1/r_{cho}e^{\alpha x})(\partial v/\partial x)$.