ELECTRONIC SYSTEMS

A COURSE BASED ON ADULT EDUCATION PRACTICES

by

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ABSTRACT

The causes of low student attendance for continuing education courses in electronics at the Pacific Vocational Institute (PVI) are analyzed. The unsatisfactory student persistence reflected inadequacies in the approaches used to instruct and in the textbooks utilized in these courses.

This report describes how modern principles of adult education were employed to identify these inadequacies and how the application of these principles was used to develop a new curriculum and a new book (appendix F). The new curriculum and its accompanying book not only incorporate the latest developments from the electronics industry, but they also incorporate the continuing application of adult education principles and practices.

The criteria for the selection of electronic components is discussed. The resulting component selection provides the students with a moderately priced kit that is easy to transport, and whose components find repeated application throughout the various experiments in the course.

The students' attendance records provide one index of the success achieved by the new course. These records show that the successful application of adult education principles has renewed the interest and promoted the active participation of continuing education students attending electronics courses.

Another indicative index of the success of the course is the result of field tests performed by other instructors at PVI as well as at other institutions. These results confirm that the new curriculum, the new book and the application of the recommended adult education practices provide the same successful responses as those experienced during the initial tests and development of the course.

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INTRODUCTION

In this essay I am discussing the present teaching practices of electronics, in particular at post secondary education institutions. For the past three years I have taught this subject at the Pacific Vocational Institute in Burnaby, B. C., both during the day program and in the evening Continuing Education Program. This experience has brought me into close contact with both Day Program Students and Continuing Education Students. This close contact made me aware that the current practices in teaching this subject in the day program are successful as far as attracting sufficient students to justify giving the course and also that a large enough percentage of these students succeed in satisfying the course requirements. However, the same approaches did not seem to provide satisfactory results with the students of continuing education courses, who showed lack of involvement and a declining attendance after a few sessions of their course.

In this essay I describe both how I have attempted to identify and correct the basic weaknesses in the practices used to instruct the continuing education students, in accordance with the modern practices of adult education as elaborated in the literature, and the process that I followed in the preparation of a new textbook whose use requires approaches suitable for teaching adults, and which is meant to be used in a revised course.

This paper is organized into ten sections as follows: The curriculum used to teach electronics, Student performance and persistence in previous programs, Identification of inadequacies of previous approaches, Factors leading to the development of the new curriculum and the new book,

Development of the new curriculum and the new textbook, Selection Criteria for laboratory components, Recommendations for the use of the textbook, Field testing of the new book and the new course, Insights acquired from the field test, Conclusions. In the appendices the following materials are presented in addition to a copy of the new textbook: Curriculum coverage of the ten month daytime program, The new curriculum, Cost of laboratory components for the new curriculum, Attendance records of courses using the new curriculum, Field testing from Whittier Union High School District.

THE CURRICULUM USED TO TEACH ELECTRONICS

As an electronics instructor in a ten-month program of Electronics taught at the Pacific Vocational Institute, I can describe the traditional curriculum and laboratory materials used for this subject, both during the ten-month day program, and during the four year Continuing Education Program.

The ten-month daytime curriculum[1] is a typical example of the organization of content taught in most post secondary electronics training centres throughout British Columbia. While I do not consider it totally inadequate for those students who can affort the time and are willing to immerse themselves in a course designed to train them in this discipline, I find both the content and the methods used in teaching it unsuitable for average adult students. I refer to this ten-month curriculum, when applied to continuing education courses, as the OLD CURRICULUM, to differentiate it from the proposed curriculum discussed in this essay and which is referred as the PROPOSED or NEW CURRICULUM.

The old curriculum is presented to the adult students as an imposed discipline whose planning does not involve their participation. The students confronted with this approach quite often fail to recognize how this curriculum will help them to understand, in a short period of time, the operation of modern electronics devices, unless they are prepared to devote a much longer time than they had previously anticipated. This extra time needed is not available to most of these students.

The Continuing Education program using this old curriculum also

[1]Appendix A, Curriculum Coverage of the Ten Month Daytime Program.

utilizes the same laboratory facilities and techniques of the ten-month daytime program.[2] The continuing education program is offered two evenings per week during the winter sessions and students require four years to complete it.

The same basic material for the ten-month daytime courses is included in the continuing education courses, but under different names. For example, the first year continuous education courses are called Telecommunications Principles, Practical Mathematics and Engineering Science. The second year continuing education courses are called Telecommunications Principles A, Mathematics A and Computers A. The third and fourth years bear the letters B and C for each course respectively.

For the first year, Telecommunications Priniciples and Practical Mathematics are offered on Tuesdays and Thursdays respectively, from September to the first weeks in January. Engineering Science is then available, on the same days of the week, from January to the first weeks of May. The same schedule is followed for the second year, i.e. Telecommunications Principles A and Mathematics A are offered from September to the first weeks in January, and Computers A from January to the first weeks of May.

[2]Appendix A, Laboratory Materials in use for the Old Curriculum,p.36.

STUDENT PERFORMANCE AND PERSISTENCE IN EXISTING PROGRAMS

Day Program Students

The enrollment for day programs in electronics is limited to a maximum of twenty students per class. Usually there are more applicants than spaces available for these courses. The selection of successful applicants is done on the basis of pre-requisites and date of the application for admission. The basic pre-requisites call for a certificate from secondary school, indicating the successful completion of the grade 12 mathematics and physics. Notification of eligibility to enroll in these courses is on short notice, usually less than a week. A total of 18 students normally register in a starting course. As a point of general observation and previous experience, during the first week, two to three students decide to withdraw from the course, and another two students quit within the next two weeks. The remaining students, fourteen to sixteen, usually persist to the end of the course.

The students who persist are usually very highly motivated. Some are sponsored by the Canadian Employment and Immigration Commission (C.E.I.C.) or other agencies, but in general they do not hold part-time positions. Thus, these students are able to spend full-time working on their studies. They are constantly involved with electronic equipment and appliances and have the opportunity to discuss problems in this area with more advanced students as well as with possible future employers. They often attend seminars offered by the local industry and they participate in field trips. All these contacts and exposure seem to strengthen their motivation, since they appear to be willing to study all the basic concepts, even those whose

usefulness is not apparent. In general they are active participants of the electronics discipline.

Continuing Education Students

The enrollment practices for continuing education students are similar to those of the day program. Although the academic background of the continuing education student is similar to that of the day program student, his persistence rate in these courses is much lower.

As an average, eighteen students have enrolled each September to take the first year courses, but no more than ten to twelve of them finish their first year. Of those students who finish the first year, only five to seven students enroll in second year courses.

Students in these courses are usually employed, though their employment may not be related to electronics. The great majority of them are employees of B. C. Telephone Company. Upon successful completion of their first year, this company revises and upgrades their work position. Therefore, it is in the students' interest to finish at least the first year course. Salary increases for second, third and fourth years of education are not as substantial as for the first year.

Other students who do not work for B. C. Telephone Company usually work for other electronics-related companies. They claim to be interested in improving their positions in the work force and in keeping abreast of the changes taking place in this rapidly advancing area.

Finally, there are students interested in a general understanding of this subject in order to appreciate the latest products from the electronics industry. In general, these last students are not interested in studying the fudamental theorems in great detail, since electronics is usually only of

general interest to them. These students may work during the day on something that is unrelated to electronics. They lack contacts and exposure in the electronics industry and quite often do not discuss electronics matters at work. They often admit to being just observers on what is going on in electronics, rather than participants. Some of these students are not willing to spent time studying concepts unless an immediate application is found.

This last group of students does not enroll in more advanced courses because:

a) Unless the student satisfies the pre-requisites for more advanced courses, he will not be admitted to them on the basis that the electronic equipment used in advanced laboratories could be hazardous to persons without their knowledge of safe and appropriate procedures.

b) Even if they are accepted into the theory portion of more advanced courses, they would be unable to comprehend the advanced concepts because of their inadequate foundation in this area.

c) The school will not run a course if the number of students is fewer than twelve, and usually there are insufficient applicants for these advanced courses.

Accordingly, few eligible continuing education students endure the first sessions of these courses, because these courses are based on a curriculum that offers no opportunities for their active participation. Instead of involvement, this old curriculum requires the students' acceptance of a coverage which most of them find unrelated to what they want to learn.

IDENTIFICATION OF INADEQUACIES OF CURRENT APPROACHES

The Old Curriculum

The old curriculum requires the student to study the basic electrical coverage as it is defined from a disciplinary standpoint. Students often have difficulty identifying the purpose of this basic coverage because initially they do not have the knowledge to enable them to relate that basic coverage to the modern devices they want to assemble and operate. Also typically nobody explains the relationship to them. The coverage of this basic electrical material takes most of the initial time allocated in the old time schedules, a fact which discourages many students who do not have the desire to endure long periods of study in matters that do not seem related to their immediate occupational goals.

In these traditional courses the student is held responsible only for the material described by a rigid curriculum and is required to attend classes in which the instructor delivers canned audiovisual presentations without discussion. These students are not participants in the planning of their studies and they are not given the opportunity to learn how to define their goals or how to achieve them. Most of the students who endure the old curriculum do so in order to achieve an accreditation that eventually might be used to obtain a salary raise from the employers who subsidize part time studies. Regarding the expectation of a raise as a motivating factor we make reference to Malcolm S. Knowles. He considers the objective "being able to make more money" an important incentive to learning but he calls it an "interest" rather than a "need" and adds:

> Interests are relevant to the adult educator's technology but in relation to his mission we are talking about something different and more fundamental - indeed, about something about which individuals are less conscious than they are of their interests. We are talking about the more ultimate needs and goals of human fulfillment. (1)

The fact that most students motivated by the expectation of a salary raise endure only one year of the old curriculum indicates that while their interests are satisfied, their ultimate needs are not being fulfilled.

The old curriculum does not consider the student's ever-changing needs and the contents of this curriculum are presented in a standard way to the student who is expected to accept their validity without question. This situation constitutes a violation of the modern practices of adult education, because, as is pointed out by Knowles:

> There is a distinct shift in emphasis in andragogy away from the transmittal techniques so prevalent in youth education - the lecture, assigned readings, and canned audio-visual presentation - toward the more participatory experiential techniques. Indeed, "participation" and "ego-involvement" are

[1] Malcolm S. Knowles, The Modern Practice of Adult Education, (New York: Association Press, 1977), p. 23.

> boldfaced words in the lexicon of the adult educator, with the assumption often being made that the more active the learner's role in the process, the more he is probably learning. (2)

The aftermath of using a standard curriculum without any consideration of differences among the adult students is that many of them leave the classroom after the first session and do not return.

The New Curriculum

The new curriculum relates more closely than the old to the developments that have attracted students to take a course in electronics. It teaches them how modern electronic circuits operate. By outlining the possible interconnections needed to produce the complex devices these students are eager to assemble, it makes the application of the knowledge readily apparent. A common example is that of students who want to learn electronics so that they can install visual displays in their cars, such as digital clocks, speedometers, tachometers or voltmeters. The new curriculum is designed to teach students as early as possible about the most common modern circuits used to make up those complex devices; how these circuits work; how to connect them; how to look for their corresponding technical specifications; how to evaluate their advantages and limitations; the kind of power supplies needed to operate them; how to select the components needed from technical catalogs; how to evaluate their cost; and how to assemble the devices.

[2]Malcolm S. Knowles, The Modern Practice of Adult Education, p. 45

I set out to develop the new curriculum following the guidelines of superior conditions of learning from Knowles[3] which call for a high level of student involvement. Thus, I have allowed the new curriculum to offer the student the opportunity to contribute suggestions regarding the depth of coverage as well as suggestions on special applications that they want to learn. This feature gives the students the opportunity to get involved in their own learning immediately at the beginning of their course.

Such involvement at the beginning of previous courses seldom took place, because the contents of previous curricula call for the lengthy coverage of basic material before the students can begin to appreciate how this coverage will satisfy their original interests in particular applications. Students taking courses using this old approach must endure a coverage that in its initial stages appears unsatisfactory and remote to their felt needs, failing thus to promote their involvement.

The approach and coverage of the new curriculum requires that the instructors find out, during the first session, what is it that the students want to learn and the type of applications in this field that interest them most. Then, based on the students' response, the instructors must set out to determine the necessary depth of coverage and extra materials needed to satisfy those desires in the shortest possible time. This approach is possible because of a new and careful selection of material coverge utilizing present technical innovations.

When I discussed the new plan and content for the achievement of

[3]Malcolm S. Knowles, The Modern Practice of Adult Education, p. 52.

their objectives with the students, I found they did not object to the challenge of participation, and willingly set out to research and study on their own. This corroborated Knowles' statement that learning is internally motivated and:

> The important implication for adult-education practice of the fact that learning is an internal process is that those methods and techniques which involve the individual most deeply in self-directed inquiry will produce the greatest learning. (4)

Teaching Practices

Some instructors claim that the old curriculum contents are not suitable for discussion, at least during the initial stages of the course. They feel that new students will require long periods of training before they can make any worthwhile contribution. Therefore, these instructors deliver their lectures using a factual approach without any discussion. These teaching approaches violate the modern practices of adult education because they fail to involve the students.

Textbooks

Most of the texts suggested for previous courses in electronics are no more than factual presentations of the theory in this field.

[4]Malcolm S. Knowles, The Modern Practice of Adult Education, p. 51.

The following is a list of commonly recommended reference books for electronics courses at PVI:

Herbert W. Jackson, Introduction to Electric Circuits, (New Jersey: Prentice-Hall, 1981)

Bernard Grob & Milton S. Kiver, Applications of Electronics, (New York: McGraw-Hill, 1966)

Training Publications Division of the Naval Personnel Program Support Activity, Washington, D. C., Basic Electronics,(New York: Dover, 1973)

Robert L. Shrader, Electronic Communication, (New York: McGraw-Hill/ Gregg Division, 1980)

T. A. Lovelace, Engineering Principles, (Hong Kong: Thomas Nelson and Sons, 1976)

R. N. Renton, Telecommunication Principles, (Bath, Great Britain: The Pitman Press, 1973)

G. L. Danielson & R. S. Walker, Radio and Line Transmission, (London: Iliffe Books, 1969)

The design of the above books anticipates that the approach will be accepted by the students without question regarding their validity, therefore their approach is not conducive to student involvement and violates fundamental principles of adult education.

The circuit schematics presented in most textbooks are in general not meant to be assembled. These schematics are meant to illustrate isolated theoretical descriptions. Besides being incomplete, these schematics depict circuits that often will not work when connected as shown in these textbooks. This is why in most present day books the schematic diagrams are drawn quite small, since the author does not expect the student to attempt their assembly, therefore neither the author nor the publisher is concerned about their legibility in a laboratory setting.

Only persons with extensive knowledge of electronics would feel confident enough to even attempt assembling these circuits, which require a great deal of knowledge, resources and time. These persons must be willing to investigate the many sources of technical data and be able to read, interpret and understand such sources. They must also possess a working and practical knowledge of commercially available components and be familiar with the wide range of expensive laboratory equipment needed to assemble and test prototypes of these circuits. In essence, these persons must have a deep understanding of laboratory procedures, component selection, test procedures and trouble-shooting techniques and must feel quite confident in their ability to assemble projects. These persons are not average students and constitute only a small minority compared with the vast majority who are eager to attain an adequate level of expertise.

The average student who attends adult education courses becomes quite frustrated in his attempts to assemble a circuit from the skimpy information provided by ordinary textbooks because he does not have this advanced knowledge. To the average student the task of comprehending this kind of presentation is not only an immense obstacle in his learning but also inhibits his gaining the necessary confidence to proceed successfully with studies in his chosen field. This is probably one of the reasons many students become despondent in their efforts to learn electronics. Students who are determined to continue their studies using these books quite often find themselves unable to describe the operation of various circuits without making constant reference to the text. This is because these students have not been given the opportunity and guidance to become involved in the development, the practical assembly, and the testing of those circuits.

While searching for a suitable textbook to be used with the new proposed curriculum, it soon became apparent to me that none of the available books contained the desired coverage nor conformed to adult education standards. Many books were found to be out of date, some were too advanced for use in continuing education courses and still others could only be used as technical reference manuals.

The out-of-date books do not address the present needs of the students. Many of these books still show the use of obsolete devices, such as vacuum tubes, which are no longer commercially available.[5] Most of them do not consider integrated circuits in their coverage.

The advanced textbooks expect the learner to be familiar with all the basic literature, i. e. they assume that the learner has acquired most of the basic knowledge as well as most of the more advanced concepts (which take many years of intense study to acquire), in order to appreciate much of the material that the authors consider unnecessary to explain. These books are apparently intended for university students or graduates in the sciences and not for the average person who does not possess many of the pre-requisites.[6]

[5]Bernard Grob & Milton S. Kiver, Applications of Electronics,(New York: McGraw-Hill, 1966)
Training Publications Division of the Naval Personnel Program Support Activity, Washington, D. C., Basic Electronics, (New York: Dover, 1973)
Robert L. Shrader, Electronic Communication, (New York: McGraw-Hill/ Gregg Division, 1980)
T. A. Lovelace, Engineering Principles, (Hong Kong: Thomas Nelson and Sons, 1976)
R. N. Renton, Telecommunication Principles, (Bath, Great Britain: The Pitman Press, 1973)
G. L. Danielson & R. S. Walker, Radio and Line Transmission, (London: Iliffe Books, 1969)

[6]Joseph A. Edminister, Electric Circuits, (New York: McGraw-Hill, 1965)
T. P. Sifferlen & V. Vartanian, Digital Electronics with Engineering Applications, (Englewood Cliffs, N. J. : Prentice-Hall, 1970)

Another kind of book is the technical manual published for diverse electronics companies. These manuals are meant to be used only for the training of employees within the particular company that issues them. The manuals usually contain reference material about the construction and operation of the company's products and equipment. To understand their contents, and employee must receive instruction from a company's training supervisor, usually in specialized training centers where the different products and equipment are discussed. In general it is very difficult to interpret the contents of these manuals without the equipment or the guidance of a person conversant with it. Therefore, these manuals are unsatisfactory for self-directed studies. They can be classified only as reference material.[7]

Finally there are books of the "cookbook" type which contain a selection of circuit schematics collected from a wide range of designers. Many of these books advertise their projects as: "do-it-yourself electronics" and promise that all the projects are easy to build. The presentation of these circuits is not organized in an educational manner, since no educational outcomes are expected nor planned for the person who purchases the book. The purpose of the books is generally limited to serving as

[7]The following are examples of company publications using this approach:

IBM Systems Development Division, 1443 N1 Printer, (North Carolina: IBM Product Publications, 1968)
Olivetti/General Electric, GE 115/2 CR 10 Subsystem, (Italy: General Electric Information Systems Division, 1966)
Hewlett Packard, Model 2402A Integrating Digital Voltmeter, (Palo Alto, California: Hewlett Packard Company, 1969)
The Decca Navigator Company, Loran C (Long Range Aid to Navigation) Model DL91, (Surrey, England: Decca Technical Publications Department, 1975)

reference material for experienced technicians who design electronic circuitry.[8]

The type of presentation used in technical manuals is useful when company trade procedures are to be kept relatively private among the employees of those companies. Unfortunately, many authors make use of similar presentation in their books. One of the immediate results is that these books appeal only to a few selected students.

David Hume[9] pointed out to me on a conversation held last May 1981, that the above textbook presentations appeal to some instructors, unsure of themselves, who find satisfaction from the admiration and respect that they seem to command when they interpret the content of those books to their students. Mr. Hume indicated also that these instructors generally do not appreciate books with clear presentations because such books eliminate the satisfaction that these instructors derive from interpreting obscure texts.

I find that this type of presentation leads to frustration for most students, and misleads them into thinking that the subject is beyond their capabilities unless they receive adequate help.

[8]Don Lancaster, TTL Cookbook, (Indiana: Howard W. Sams, 1977)
Don Lancaster, CMOS Cookbook, (Indiana: Howard W. Sams, 1978)

[9]David Hume, Director of Extension Services, British Columbia Institute of Technology, Burnaby, B. C.

TECHNICAL FACTORS LEADING TO THE DEVELOPMENT OF THE NEW CURRICULUM AND THE NEW TEXTBOOK

Present technical innovations have made possible the development, production and marketing of micro-miniature electronic circuits. These circuits are known as Integrated Circuits (IC's) and are available to the consumer in conveniently sealed packages. Compared with previous conventional circuits they are physically small, inexpensive, require small amounts of power to operate, are very reliable and can be used in many applications. These are the main reasons why they are replacing with an unprecedented rapidity the big, bulky, and expensive circuits that formerly were custom built for each particular application or piece of equipment.

Integrated circuits contain thousands of electronic components reduced by photographic means into microscopic sizes. They are then enclosed into small packages and are ready to be used. Their production in large quantities has permitted manufacturers to reduce their price, making their use economically attractive. The electronics equipment that uses integrated circuits is smaller, lighter, requires less power to operate, and its repair and maintenance are greatly facilitated by the easy replacement procedures possible only with integrated circuits, further reducing the costs of their operation.

Integrated circuits are compatible with different electronic configurations, and can be reused repeatedly. This universal acceptability of a common set of circuits is already paving the way to an overall standardization in the electronics industry that will affect all the present industrial processes. Examples of this acceptance can be found easily, such

as in the circuits used to represent voice and television images. These television images are being transmitted from country to country, where different and incompatible television systems may be in use, by decoding and translating digital information into their own television system prior to local re-broadcasting. Another example is the use of laser beams to carry telephone conversations, where these conversations are transmitted digitally. Even more recently, digital records have made their appearance in the consumer's market.

The present state of the electronics technology offers the possibility of new material coverage in order to give the student the option for a simpler and shorter approach to his learning. The long periods of training needed using traditional approaches discouraged many students from taking the course. Thus the new curriculum calls for a change of the traditional order of presentation of topics that does not hamper the students' future progress. The development of the new curriculum required the rearrangement of previous materials, the addition of new materials, and the application of the latest innovations in electronics.

Instead of teaching the fundamental ideas on the components and design procedures that make up an electronic circuit, the new curriculum begins by teaching the operation and use of its pre-assembled equivalent, which is what many students are eager to learn. The experience gained by the student while using and operating pre-assembled circuits can be used then to facilitate his understanding of the basic theorems and mathematical principles behind them. Thus the new curriculum provides the students with the basic practical applications of electronic circuits and facilitates their future progress and advancement in this field.

Many attempts have been made to modify the old curriculum in order to accelerate the coverage of basic material. This has been done to introduce students much sooner to the applications that they want to learn. However all of these attempts have been unsuccessful, since they involve the removal of material from and old curriculum which does not lend itself to such changes, and the students still have to learn the removed material at unplanned stages of their course.

The new course and textbook are designed to involve the student, so that he can develop the confidence and abilities exhibited by highly qualified technicians in the design, assembly, and testing of electronic circuits and thus come to understand the procedures and techniques of this field.

DEVELOPMENT OF THE NEW CURRICULUM AND THE NEW BOOK

During the development of the new course and book, it seemed essential that relevant laboratory experiments were needed to follow any theoretical description mentioned in the text so that the student could verify that the theory is correct and thus proceed confidently to the next stages of his learning, because he now knows that what he is doing is right, not because it is written in a book but because the student himself has been able to verify it with actual electronic circuitry. The new course and new book call for the student to verify the theory behind each circuit at all levels of his training, from basic circuits to more advanced ones. This verification is facilitated with laboratory components whose careful selection allows the students to assemble, test, and prove to themselves that the theoretical statements in the book are indeed correct.[1]

Pre-requisites for the New Course

The pre-requisites for the new course and the understanding of the book do not include university level mathematics or physics. In fact, the knowledge acquired by students who have completed courses such as tenth grade mathematics or physics is often sufficient to enable these students to complete the course successfully. Thus the course and its textbook become suitable for a great number of students, i. e. for students with related advanced studies as well as for those students that are newcomers to the field.

[1]Appendix F, Electronic Systems Book, p. 8

I have found that most of the advanced students generally welcome a thorough review of materials already familiar to them, because a review seems to refresh and reinforce their previously acquired knowledge. They also profit by learning new applications to this knowledge. As for the students with only a basic understanding of mathematics, they find that the material is explained in simple terms with plenty of analogies to which they can relate and understand.

The new curriculum and its book follow the procedures outlined by Knowles, who asserts:

> The central dynamic of the learning process is thus perceived to be the experience of the learner, experience being defined as the interaction between an individual and his environment. The quality and amount of learning is therefore clearly influenced by the quality and amount of interactionbetween the learner and his environment and by the educative potency of the environment. The art of teaching is essentially the management of these two key variables in the learning process - environment and interaction - which together define the substance of the basic unit of learning, a "learning experience." The critical function of the teacher, therefore, is to create a rich environment from which students can extract learning and then to guide their interaction with it so as to maximize their learning from it. (2)

This learning experience is accelerated by the confirming results from relevant laboratory experiments and produces the desired level of

[2]Malcolm S. Knowles, The Modern Practice of Adult Education, p.51.

involvement of students as well as of the instructors who conduct the course. The application of these principles in the text has also permitted advanced students to use it as a self-study guide.[3]

Title of the New Book

The title "ELECTRONIC SYSTEMS" was chosen for the textbook because it considers the circuits used in the evaluation, analysis and control of measurable physical phenomena. In present day technology, physical phenomena measurements are represented by equivalent values of voltage, known as ANALOG VOLTAGES, prior to their electronic processing. Electronic processing consists in storing, analyzing and comparing analog voltages against standard values that the designer or user may consider as desirable, e. g. the setting of an air conditioning dial to a desired temperature.

Twenty years ago, electronic processing was done using mostly analog devices, however these devices were useful to control only a limited number of physical applications. Now, thanks to the great versatility of available digital systems, that employ a universal mathematical system, the only restriction placed on analog voltages of any origin is their conversion into a digital form. This analog to digital conversion (ADC) combines both analog and digital techniques.

After the above conversion has taken place, the resulting figures are processed digitally and the answers converted back into analog voltage form. These analog results are then used to activate electrical controls that correct the intended physical phenomena. The digital to analog conversion (DAC) also makes use of digital and analog techniques. This book and the

[3]Appendix E, Field Testing from Whittier Union High School District.

new curriculum are concerned with ADC and DAC procedures, as well as with the basic processes taking place in the digital processor, therefore the contents cover both digital as well as analog techniques, and justify the title "ELECTRONIC SYSTEMS".

SELECTION CRITERIA FOR LABORATORY COMPONENTS

As previously discussed, the development of integrated circuits offers countless possibilities to improve on previous approaches. Their availability has facilitated the development of this new curriculum, permitting the introduction of advanced circuits at much earlier stages of the students' training than was possible before. In the new coverage it is no longer necessary to discuss the principles that led to the design of these integrated circuits, nor the operation of each of the components used in their construction, because this is the primary concern of design engineers. Therefore the new coverage considers only their operation and applications, which is what most students want to learn.

If a student were to assemble an equivalent circuit using the regular standard components, he would find that the resulting assembly occupies several hundred times the space of the original integrated circuit. The student not only would be faced with increased space requirements, but also would have to waive the advantages that integrated circuits have on the previous technology, such as reduced power requirements, low static interference between components due to their close proximity, and above all, low costs that result from their production in assembly lines. For example, the purchase of an oscillator circuit in integrated circuit form, such as the 555 and which has been pre-tested to insure its proper operation, costs only 38 cents.[1] On the other hand, the assembly of its equivalent circuit using standard components that require an area comparable to that of a

[1]Appendix C, Cost of Laboratory Components for the New Curriculum.

standard brief case, costs in the vicinity of $70.00. Thus the new technology also offers immense possibilities to improve on the cost of the components used in previous teaching approaches.

Up to the present, hundreds of dollars have been spent on standard laboratory equipment. If a student wants to purchase these standard laboratory facilities he would have to be prepared to invest at least $1000.00 in order to purchase power supplies worth up to $300.00, volt-ohmmeters worth up to $200.00, signal generators worth up to $200.00 and a few other pieces of test equipment. This estimate does not include oscilloscopes, since their unit price is close to $1500.00. Compared with these costs, the use of integrated circuits described in the new curriculum and book amount to $47.20.[2] The power supplies consist of inexpensive six volt batteries, that are sufficient to provide the power requirements of most integrated circuits. The components listed for the new curriculum also include the necessary parts to assemble an electronics test probe that is used as a voltage indicator throughout the course,[3] and the parts needed to assemble a signal generator.[4] It should be noted that the laboratory components used in standard laboratories and those proposed in the new curriculum are equally satisfactory in carrying out the experiments of the new curriculum, but not their price as indicated above.

The size of the components needed for this course, besides being within the economic reach of the students, facilitates their transportation. This factor allows students to take them home and carry out experiments there that otherwise would never have been possible using standard facilities.

[2]Appendix C, Cost of Laboratory Components for the New Curriculum.
[3]Appendix F, Electronic Systems Book, Section 1.
[4]Appendix F, Electronic Systems Book, Section 5.

Technical criteria for the selection of these components was based on their ease of handling and operation. Some specialized components can be damaged easily at the touch of the hand due to electrostatic charges in a human body. Special procedures are required for their handling. Their use was avoided to eliminate concerns that might distract the students while performing their laboratory experiments.

Finally, another criteria for the selection of laboratory components was their repeated use in different experimental configurations throughout the course. This consideration was meant to further reduce the cost of the components needed in the course without affecting the coverage of the book. This factor also helps students to realize that the same component can be used in different configurations to perform different functions.

RECOMMENDATIONS FOR THE USE OF THE TEXTBOOK

The proposed course and textbook are meant to provide the students with basic and fundamental coverage as well as with the advanced material required to understand and utilize the most recent developments in this field. They also aim to provide the students with the procedures needed to allow them to conduct their own inquiry and plan their own learning in this field. This is because the new curriculum is based on Knowles' guideline that the greatest learning is produced by methods and techniques that involve the students in their own self-directed inquiry. This does not mean that an instructor using the new curriculum should give up his responsiblility, but that he now has the option to use a process of reasoning and demonstration to convince the students of the utility of the objectives that he suggests.

Therefore instructors using the new curriculum and book are required to conduct class discussions in order to: consider the students' needs and goals, to help the students relate the new contents with their own goals, and to allow them to undertake reasonable objectives within the length of the course. Students with a sound knowledge and experience on technical matters can be expected to achieve much more in a shorter time than students who lack that kind of background. The new curriculum and book permit students of different backgrounds the opportunity to achieve their individual goals, providing the instructor is willing to coordinate and lead them in the achievement of their expectations.

FIELD TESTING OF THE BOOK AND THE NEW COURSE

The first time the new curriculum was offered to students was during the winter session of 1979-1980 under the name of Electronic Systems Parts I and II. The students enrolled in this first course included high school teachers, engineers, electrical and electronics technicians as well as people with a general interest in this subject. Their diverse backgrounds provided the opportunity to test the efficacy of the new curriculum and its recommended teaching practices. The new curriculum proved effective in involving all the students in class without inhibiting the progress of the more advanced students. This involvement was evident by the excellent student attendance recorded from the beginning to the end of the course.[1]

During the initial winter session, I also carried out minor modifications on the curriculum under test, in order to improve the general continuity of its presentation. These changes led to the final preparation of the present curriculum in the summer of 1980,[2] and the completion and subsequent publication of the new book in September 1980.[3] This new curriculum was successfully tested once more during the winter session of 1980-1981.

The students performance has been assessed on the basis of their ability to design and assemble practical electronic devices, and not on a final exam. At the end of these courses each student has been requested to present projects that work as intended, according to the principles behind their operation. These students have shown a great degree of confidence in

[1]Appendix D, Attendance Records of Courses using the New Curriculum.
[2]Appendix B, The New Curriculum.
[3]Appendix F, Electronic Systems Book.

the selection of electronic components, in the assembly of circuits and in the use of test equipment. These factors corroborate the efficacy of the new curriculum that helps them achieve their desired goals at an earlier stage of their training than the longer periods previously expected from the old curriculum. The same findings have also been reported by other instructors at the Pacific Vocational Institute using this curriculum as well as at high school levels.[4]

[4]Appendix E, Field Testing from Whittier Union High School District

- INSIGHTS ACQUIRED FROM THE FIELD TEST

The response from other instructors and teachers from PVI as well as from other institutions indicate that most of them have found the new curriculum and the new book most useful in their task. Their results confirm that there is an increased participation and involvement of students taking this course, and that advanced students have even managed to use the text as a guide to their self-directed study.[1]

Some instructors have mentioned that a few of their less advanced students have experienced difficulty understanding some basic mathematical concepts. Since the course calls for a basic knowledge of mathematics and electricity, I set to investigate the cause of these isolated difficulties. My impression is that in the introduction of new mathematical concepts, these instructors do not provide as many analogies as needed by these students so that they can relate the new concepts with their own experience. Therefore, in a second edition of this book more analogies will be included and others suggested to the instructors to further facilitate its readability to the largest possible number of interested students.

Additional material will include problems, more exercises and examples and the insertion of technical data as originally intended but withheld pending the permission to reprint from electronics manufacturers.

[1]Appendix E, Field Testing from Whittier Union High School District.

CONCLUSION

At the Pacific Vocational Institute I observed a problem with continuing education courses in electronics. Students would enroll in beginners' courses but many of them would drop out after a few sessions. This situation seemed inconsistent with their initial interest. In my investigation of their reasons for discontinuing their course, it became apparent that they were discouraged by methods of instruction that failed to involve them and also by a curriculum whose contents did not appear related to the applications that they wanted to learn.

To solve this problem I constructed a new curriculum by combining two major developments: the modern principles of adult education as outlined by Knowles; and the most recent innovations that our present electronics technology has to offer, namely pre-assembled circuits. These two developments were put together to produce the new book "ELECTRONIC SYSTEMS"[1] which requires adult education principles for its use and places great emphasis on the students' involvement.

The field tests done on the use of the new curriculum and the new book have basically confirmed the utility of the approach. The successful application of these principles is reflected by the popularity and interest that the course is enjoying, the regular attendance from participating students, the reports of successful field testing from other instructors and their financial backing in the purchase of books and accompanying electronic components.

[1]Appendix F, Electronic Systems Book.

APPENDIX A

CURRICULUM COVERAGE OF THE TEN MONTH DAYTIME PROGRAM

During the first month of the daytime program, electronics is taught with emphasis on the physical characteristics of the elements and materials used in electricity. The presentday theories about the atomic nature of electricity are discussed, as well as the conduction of electric currents through different media, i. e. solids, liquids and gases.

The Systeme International (SI) is introduced. To its basic three units to measure length, weight and time, a fourth unit is added: the AMPERE. This last unit is used to measure electrical currents, and together with the previous three units, it defines the essential aspects of an electrical system.

The need to represent quantities numerically is self-evident, because any measurement must be taken in relation or comparison with known values. A few examples of these comparisons are: twice as fast as, half as loud as, three times as heavy as, five times as far as.

The student is also taught that electrical quantities have a wide range of values, varying from millionths of a given quantity, to millions and billions of another quantity. This wide range of values brings the need for special notations, which are presented to the student as "Scientific Notation" or also called "Engineer's Representation of Numbers". In these notations, quantities are represented by a digit, 1 to 9, with or without a decimal, times the base number 10, and this base number may use positive or negative exponents as required, e.g. 7.2×10^6.

Besides the above system, the student is introduced to the prefixes used by the electronics industry, such as MEGAhertz (one million hertz), or NANOsecond (one billionth of a second). The student is taught to relate the scientific notation to the industry's jargon.

The four basic elements that constitute an electric system are introduced: (1) Power Sources; (2) Conductors; (3) Control Elements, such as switches and fuses; (4) The Work-load, i. e. anything that requires electricity to do an intended amount of work.

During the second month, the student learns what physical characteristics of matter oppose the flow of electrical currents. The student gets inititated into the study of one of the three properties of electricity, i. e. RESISTANCE, which is the property that opposes the flow of electrical currents.

During the third, fourth and fifth month, the student learns electrostatics and magnetism, studies that lead him into the remaining two other properties of electricity, i. e. CAPACITANCE and INDUCTANCE.

During this period, the student is also introduced to circuit analysis techniques, that will enable him to predict how a given circuit will react to particular conditions of current and voltage, where the sources of energy for these studies consist of:

a) Direct Current (DC), where the currents or voltages do not vary with respect to time.

b) Alternating Current (AC), for given frequencies, where the currents or voltages alternate, being positive for one half a cycle and negative for the other half. The student is taught appropriate mathematical procedures, known as Complex

Variable, to help him determine the physical response of a circuit under this type of source.

c) Transient Conditions and response to Pulses. At this stage, the student needs to use more advanced mathematical procedures, in order to determine how a circuit will react to any particular pulse. These advanced mathematical procedures include the use of calculus.

The circuit analysis techniques are based on physical laws first defined by earlier scientists and that bear their names. These basic laws used in electricity are know as Ohm's Law, Kirchhoff's voltage law, and Kirchhoff's current law. These circuit analysis techniques include:

a) Equivalent Circuits, where a circuit gets replaced by a dummy load without any effect on the source under study, and then the total current is defined, e. g. the loudspeaker in a radio may be replaced by a resistor, and though there is no sound, all the circuits continue normal operation.

b) Black Box Concept, which considers any circuit as a source together with an electrical component called impedance. Impedance is the name of the combination of one or all the three basic properties of electricity, i. e. Resistance, Capacitance and Inductance. Through this black box concept, a very complex circuit feeding power into a load, is replaced by a simple pair of elements, and the load will not miss any of its original supply circuits. As an example we can consider

AC/DC pocket calculators, which may be plugged into the power outlets or may be used with batteries.

The theorems that define the black box concept are known as: Thevenin's Equivalent Circuit and Norton's Equivalent Circuit.

c) Loop Analysis Techniques, derived from Kirchhoff's voltage law.

d) Node Analysis Techniques, derived from Kirchhoff's current law.

In the sixth month, when the above principles and techniques have been mastered by the student, the student is introduced to devices that have the ability to amplify electrical signals. These devices are known as active components and include tubes and transistors.

The basic physical properties of matter are discussed in order to explain the operation of these devices.

During the seventh and eighthmonths, the student begins to study the basic electronic circuits. These basic circuits, common to any electronics application, fall under any of the three following groups: (1) Rectifiers; (2) Amplifiers; (3) Oscillators.

During the ninth and tenth months, the student begins to study specialized applications, such as: Radio Transmission, Radio Reception, Radar, Television, Microwave and Telephone Communications, Computers, Satellite Communications, Marine and Aircraft Electronics and Control Electronics.

Laboratory Materials in use for the Old Curriculum

The student is issued a laboratory kit. The kit contains tools and a set of discrete electrical components. Some of the tools include: soldering irons, pliers and screw drivers. The electrical components

include: resistors, capacitors, coils and chokes, transformers and connectors.

The test equipment is supplied as the experiments call for it. This equipment consists of Vacuum Tube Voltmeters, Volt-Ohmmeters and Oscilloscopes. The student also receives Power Supplies, Frequency Generators, Transistor and Tube Testers.

The student spends about four months on experiments that are strictly electrical in nature. These experiments use discret components of the passive type such as resistors, inductors and capacitors.

Another four months are spent in experiments that are electronic in nature. These experiments use active components, such as tubes and semiconductor devices. The semiconductors studied include: Rectifiers, Zener Diodes, Tunnel Diodes, Transistors and their applications to Amplifiers and Oscillators.

APPENDIX B

THE NEW CURRICULUM

The new curriculum has been covered in a new continuing education course at PVI. This new course has been taught in 32 evening sessions for a period of 16 weeks. Therefore, this appendix lists its coverage based on a weekly basis.

During the first week, the student is handed the electronic components used for the course. The student learns to identify them. This task includes the introduction to electrical color codes and the meaning of the physical size in these components. The student also learns to assemble a simple logical indicator, used to identify the presence of voltage. A basic explanation is given regarding the operation of transistors when used as ordinary switches in this indicator.[1]

The second week, the student is introduced to Boolean Algebra. This is the algebra that defines the response of binary devices, i. e. those devices that have only two possible states like a switch which is either on or off. The student identifies the integrated circuits that will produce the boolean functions defined in class, and proceeds to assemble and verify the accuracy of the mathematical statements that define their operation.[2]

The third week, the student learns the laws of binary algebra and proceeds to corroborate their accuracy when the circuits described by this algebra are assembled and their response determined. The most basic form of binary addition is then introduced.

[1]Appendix F, Electronic Systems Book, p. 4.

[2]Appendix F, Electronic Systems Book, Section 2

The fourth week the student learns the different number systems associated with computers to carry out arithmetic operations. He learns to interpret binary results and also to use electronic circuits capable of translating those answers to our decimal system using seven segment displays.

The fifth week, the student is introduced to graphical methods designed to simplify the boolean algebra expressions.[3] Complex boolean statements as well as their simplified versions are implemented with electronic components and the student verifies that both circuits yield the same response but one is simpler and more economical to build than the other. Now the student is intoduced to the importance of the time element in logical circuitry. He learns the basic forms of memory used by most computers, and relates the storage of information with the application of timing pulses called Clock Pulses (CP's).[4]

The sixth week, the student learns the operation of more sophisticated units of memory and connects the corresponding integrated circuits to test their performance. He also learns the basic operation of electronic oscillators, plus the role of capacitors in the production of oscillations, and proceeds to assemble several types of oscillators.[5]

The seventh week, the student learns to use integrated circuit oscillators. The student calculates and measures their frequencies of oscillation and applies these frequencies to electronic counting circuits.[6]

[3]Appendix F, Electronic Systems Book, Section 3.
[4]Appendix F, Electronic Systems Book, Section 4.
[5]Appendix F, Electronic Systems Book, Section 5.
[6]Appendix F, Electronic Systems Book, Section 6.

When an oscilloscope is available, the student is introduced to its use, so that he can observe the waveforms taking place in different circuits. Special laboratory exercises have been provided for students that do not have an oscilloscope, so that they can still observe the behaviour of different frequencies of oscillation.

The eighth week the student learns how to produce any given count using electronic circuits.[7] Different applications are found for counters such as: the measurement of time in digital clocks; the measurement of frequency in speedometers and tachometers; and the production of light chasing effects used in advertisements.

The ninth week the student is introduced to the Shift Register,[8] used to store strings of binary quantities. Their applications include the transmission of information between two separate electronic devices or the internal use within a digital system.

Visual Displays are covered during the tenth week, to decode the information stored in binary form and then display it in the more familiar decimal notation.[9] During this same week the student is introduced to the Operational Amplifier[10] and its applications. The student uses it to add two or more voltages and also to compare and detect the largest voltage from two different sources.

The eleventh week the student learns to use operational amplifiers to shape various waveforms. He uses them to transform triangular waves into square waves (differentiator-action), and square waves back into triangular waves (integrator-action). Waveshaping circuits find application in television circuits as well as in analogous computers. The student is also introduced

[7]Appendix F, Electronic Systems Book, Section 7
[8]Appendix F, Electronic Systems Book, Section 8
[9]Appendix F, Electronic Systems Book, Section 9
[10]Appendix F, Electronic Systems Book, Section 10

to the Digital to Analog Converter (DAC), a device that produces an output voltage proportional to the binary quantity stored in a register. The student is introduced to its various control applications such as brightness controls for illumination or speed controls for motors.

The twelfth week is spent learning the operation of more sophisticated types of Digital to Analog Conversion circuits. The student is introduced to equivalent circuits, such as those described by Thevenin's Theorem.[11]

During the thirteenth week, the student is introduced to the Analog to Digital Converter (ADC). This is the electronic circuit used to convert the analogous voltages from external devices into binary quantities used for digital displays as well as in computer processing. The student learns different methods to obtain this conversion and assembles and calibrates his own circuits.

During the fourteenth week, other ADC methods are studied and their corresponding circuits are assembled and tested. During this week the student is also introduced to the design of power sources that use transformers and integrated circuits.

The fifteenth week, the student learns to interface systems powered by low voltages to external devices that operate at higher voltages. He learns to apply different isolating techniques.

The sixteenth week is spent learning computer languages and applying them to solve electrical circuit problems. As an example, the student learns to use the Ohm's Law Matrix,[12] to predict the response of electrical circuits to different applied voltages. The procedure described in the book is

[11]Appendix F, Electronic Systems Book, p. 232
[12]Appendix F, Electronic Systems Book, p. 241.

easily programmed into a computer and yields answers in fractions of the time needed by other methods.

Laboratory Materials for the New Curriculum

The laboratory components for the new curriculum are listed in the new book.[13] They were selected on the basis of their ease of handling and operation as well as of their repeated use in different experiments throughout the course. Their cost is within the economic possibilities of interested students.[14] Once the students learn their operation and some of their uses, they usually find many other applications for them, extending thus their usefulness.

[13]Appendix F, Electronic Systems Book, p. 8.
[14]Appendix C, Cost of Laboratory Components for the New Curriculum.

APPENDIX C

COST OF LABORATORY COMPONENTS FOR THE NEW CURRICULUM

The following table lists the cost of the components needed for the new curriculum. The prices were quoted by the following local distributors on January 13, 1981.

RAE Industrial Electronics Ltd./3455 Gardner Court/Burnaby, B. C.

CAM GARD Industrial Electronics/2055 Boundary Road/ Vancouver, B. C.

VARAH Electronics/2077 Alberta Street/Vancouver, B.C.

These distributors quoted prices for individual items but these prices were based on the purchase of one hundred units. The lowest price of each item was chosen as representative of the value of each component, and is listed on the last column to the right. It is felt that this is the cost that a careful shopper would normally have to pay for these components.

ITEM	QTY/KIT	PRICE			
		RAE	CAMGARD	VARAH	LOWEST TOTAL
INTEGRATED CIRCUITS					
555	1	0.45	0.38	0.75	0.38
µA741	2	0.39	0.46	0.51	0.78
FND 507	1	2.04	1.79	1.83	1.79
4066	1	0.95	0.89	1.06	0.89
7400	2	0.35	0.36	0.46	0.70
7402	2	0.35	0.36	0.46	0.70

ITEM	QTY/KIT	PRICE			
		RAE	CAMGARD	VARAH	LOWEST TOTAL
7404	1	0.44	NIL	0.49	0.44
7410	1	0.35	0.36	0.46	0.35
7413	1	0.63	NIL	0.68	0.63
7427	1	0.62	0.42	0.49	0.42
7442	1	0.58	NIL	0.97	0.58
7447	1	1.63	0.91	1.67	0.91
7476	2	0.50	0.43	0.52	0.86
7486	1	0.68	0.45	0.51	0.45
7490	2	0.53	0.45	0.92	0.90
74107	2	0.77	NIL	1.25	1.54
74LS190	1	2.72	0.82	1.81	0.82
74LS283	1	0.90	NIL	2.23	0.90
SEMICONDUCTORS					
RED LED	5	15.50/h	17.50/h	0.46	0.78
GREEN LED	5	31.00/h	23.00/h	0.51	1.15
DIODE 1N4005	4	NIL	5.99/h	0.15	0.24
ZENER 1N761	1	0.20	0.12	2.81	0.12
2N2222	1	0.27	0.18	0.82	0.18
CAPACITORS					
10µF (16V)	1	0.85	0.13	0.20	0.13
22µF (16V)	1	1.36	0.13	0.20	0.13

ITEM	QTY/KIT	PRICE			
		RAE	CAMGARD	VARAH	LOWEST TOTAL
RESISTORS					
430 Ω ¼ W	7	2.07/h	2.03/h	1.64/h	0.14
3.3 kΩ ¼ W	2	2.07/h	2.03/h	1.64/h	0.04
4.7 kΩ ¼ W	4	2.07/h	2.03/h	1.64/h	0.08
10 kΩ ¼ W	6	2.07/h	2.03/h	1.64/h	0.12
22 kΩ ¼ W	2	2.07/h	2.03/h	1.64/h	0.04
39 kΩ ¼ W	4	2.07/h	2.03/h	1.64/h	0.08
82 kΩ ¼ W	6	2.07/h	2.03/h	1.64/h	0.12
1 MΩ ¼ W	1	8.19/h	3.59/h	1.64/h	0.03
2.2 MΩ ¼ W	2	9.27/h	3.59/h	1.64/h	0.07
1 MΩ Potentiometer with thumbwheel	2	0.49	NIL	6.89	0.99
ACCESSORIES					
BREADBOARD (SK-10)	1	21.50	NIL	NIL	21.50
TRANS-BOX	1	NIL	NIL	NIL	7.22
TOTAL COST PER KIT					$47.20

APPENDIX D

ATTENDANCE RECORDS OF COURSES USING THE NEW CURRICULUM

The following attendance records were compiled from the Continuing Education Registers at PVI. They correspond to the four times that the new curriculum has been covered in courses offered by this department. These courses were scheduled over a period of two consecutive winter-spring sessions.

1979 - 1980 SESSION (WINTER)

Course Name: Electronic Systems Part I

Scheduled dates: September 10, 1979 to November 5, 1979

Number of sessions	16
Number of enrolled students	23
Possible attendance (Students x Sessions)	368
Absences	46
Percentage of attendance	88%

Course Name: Electronic Systems Part II

Scheduled dates: November 7, 1979 to January 21, 1980

Number of sessions	16
Number of enrolled students	10
Possible attendance (Students x Sessions)	160
Absences	16
Percentage of attendance	90%

1979 - 1980 SESSION (SPRING)

Course Name: Computers A and Computers B

Scheduled dates: February 5, 1980 to May 13, 1980

Number of sessions	30
Number of enrolled students	8
Possible attendance (Students x Sessions)	240
Absences	8
Percentage of attendance	97%

1980 - 1981 SESSION (WINTER)

Course Name: Electronic Systems Part I

Scheduled dates: September 15, 1980 to November 10, 1980

Number of sessions	16
Number of enrolled students	20
Possible attendance (Students x Sessions)	320
Absences	18
Percentage of attendance	94%

Course Name: Electronic Systems Part II

Scheduled dates: November 12, 1980 to January 19, 1981

Number of sessions	16
Number of enrolled students	20
Possible attendance (Students x Sessions)	320
Absences	27
Percentage of attendance	92%

1980 - 1981 SESSION (SPRING)

Course Name: Electronic Systems Part I

Scheduled dates: January 21, 1981 to March 16, 1981

Number of sessions	16
Number of enrolled students	21
Possible attendance (Students x Sessions)	336
Absences	20
Percentage of attendance	94%

Course Name: Electronic Systems Part II

Scheduled dates: March 18, 1981 to May 13, 1981

Number of sessions	16
Number of enrolled students	15
Possible attendance (Students x Sessions)	240
Absences	37
Percentage of attendance	85%

APPENDIX E

FIELD TESTING FROM WHITTIER UNION HIGH SCHOOL DISTRICT

WHITTIER
UNION
HIGH SCHOOL
DISTRICT

• Whittier, California 90605 •

BOARD OF TRUSTEES: Joan Nay, President • Jerry Sarchet, Ph.D., Vice President • Roy Salas, Clerk • Eve Burnett, Henri Pellissier, Members
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March 27, 1981

To Whom It May Concern:

Our school district has recently had the pleasure of reviewing and field testing an electronics text Electronic System by Miro Angeles.

I personally reviewed the book regarding readability and format and found it to be very appropriate for a high school population.

We had our most experienced and respected electronics instructor field test the book in his classroom/lab. He found the book to be very well laid out with the theory clearly presented and followed by lab experiments that the students found very relevant. Some advanced students used the book in an independent study mode and found it to be excellent.

If you should have any further questions feel free to call.

Sincerely yours,

Ronald J. Rhodes
Director, Pupil Personnel Services

RJR:pb

APPENDIX F

ELECTRONIC SYSTEMS BOOK

E L E C T R O N I C

S Y S T E M S

MIRO ANGELES © 1980

DISTRIBUTED BY:
AB DIGITECH CORP.
STATION S, P. O. BOX 76711
VANCOUVER, B. C.

TELL ME AND I WILL FORGET

SHOW ME AND I MIGHT REMEMBER

INVOLVE ME AND I SHALL UNDERSTAND

To AMELIA, mother.

ABOUT THE AUTHOR

Mr. Angeles is a graduate in Electronics and Communications Engineering (1958), from the National Polytechnic Institute (Mexico City). He also holds a B. A. Sc. in Electrical Engineering from U. B. C. (1966) and a Diploma in Adult Education from U. B. C. (1972). At present he is working toward a Master of Education Degree at U. B. C.

Mr. Angeles is a registered Professional Engineer in the Province of Ontario, where he has worked in different aspects of the electronics industry. He has extensive experience in computer software (programming) and hardware (circuit design). At the Steel Company of Canada, he worked as a design engineer in computer operated mills.

Mr. Angeles holds a Professional Certificate from the B. C. Department of Education. He taught Computer Science and Electronics at Hillside Secondary School and at present is an electronics instructor in a post secondary education institute in Burnaby, B. C.

FOREWORD

This book is written for Senior Secondary and Post Secondary Students, as well as for the interested Public in general.

The book discusses the use and application of integrated circuits, treating them as building units. This way, the student does not need to learn electronics from the fundamentals, nor have more than grade 10 mathematics.

The student learns to read and interpret technical data and soon becomes aware of the latest products available to him from the electronics industry.

The student assembles the projects discussed in the text and soon becomes capable of designing and assembling projects of his own, which seldom happens when the student reads a cookbook.

The material is presented at a level that is easily understood by the average reader. Many analogies of physical phenomena and electronics procedures have been included, so that the reader can relate them to familiar experiences.

For completeness, some important circuit analysis procedures have been included in the appendix.

The author wishes to acknowledge the assistance received from Mr. F. C. Bailey, proof reading many sections of this book; Ms. Patricia Cave, collating the pages of this book; and Ms. Elaine Angeles for the Book Cover.

WHITTIER
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Director, Pupil Personnel Services

RJR:pb

IMPORTANT NOTE

Please notice that the Manufacturer's Specification Sheets have been excluded from this first edition, pending permission from those manufacturers to reprint their material.

The above material may be found in the following technical publications:

ANALOG DEVICES
Data Acquisition Products
Catalog Supplement 1979

CANADIAN GENERAL ELECTRIC CO. LTD.
Silicon Controlled Rectifier
GE-X1

ELECTRONICS TODAY INTERNATIONAL
Toronto Ontario

EXAR
Timer Data Book
May 1979

FAIRCHILD
TTL Data Book
1978

FAIRCHILD
Voltage Regulator Handbook
1978

GENERAL INSTRUMENTS
Catalog of Optoelectronic Products
1980

HAMMOND MFG. CO. LTD.
166 Series Transformers
Channel Bracket Mounting

INTERSIL
Monolithic MAXCMOS
Voltage Converter
1980

LITRONIX
BAR LED'S

MONSANTO
Solid State Optoelectronics
Product Selection Guide
Jan. 1979

MOTOROLA
Linear Integrated Circuits
1979

NATIONAL SEMICONDUCTOR
CMOS Data Book
1978

NATIONAL SEMICONDUCTOR
Linear Data Book
1976

NATIONAL SEMICONDUCTOR
Data Acquisition Handbook

POTTER & BRUMFIELD
Distributor Stock Relays
April 1980

RCA COS/MOS
Integrated Circuits
1978

SIGNETICS ANALOG
Data Manual
1979

TECCOR ELECTRONICS, INC.
Technical Data T-1078
May 1978

TEXAS INSTRUMENTS
The TTL Data Book
2nd. Edition

TEXAS INSTRUMENTS
The Optoelectronics Data Book

VARO SEMICONDUCTOR, INC.
Rectifier and Bridges
June 1977

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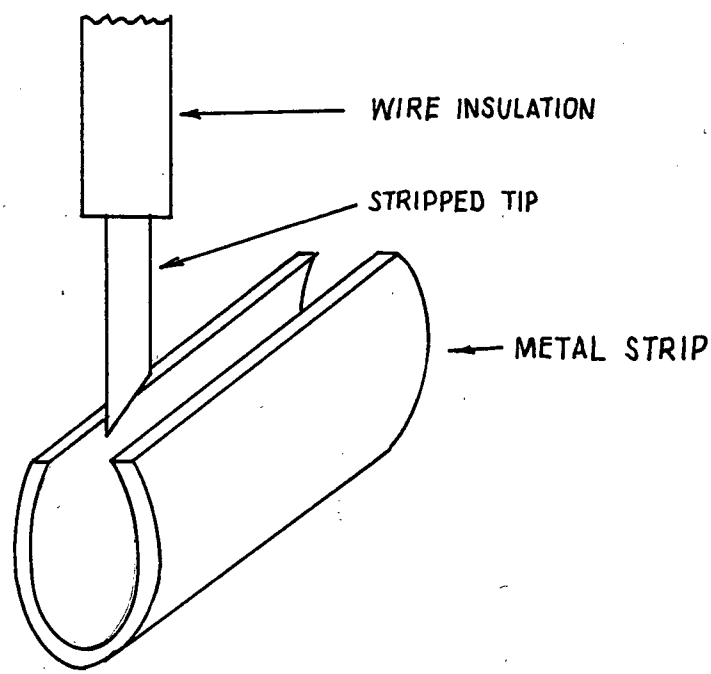
ASSEMBLY OF LOGICAL CIRCUITS

Several strip bread boards are available in the electronics market, such as: SK-10; BIMBOARDS; SUPER-STRIPS; EX300 and EX600; etc.

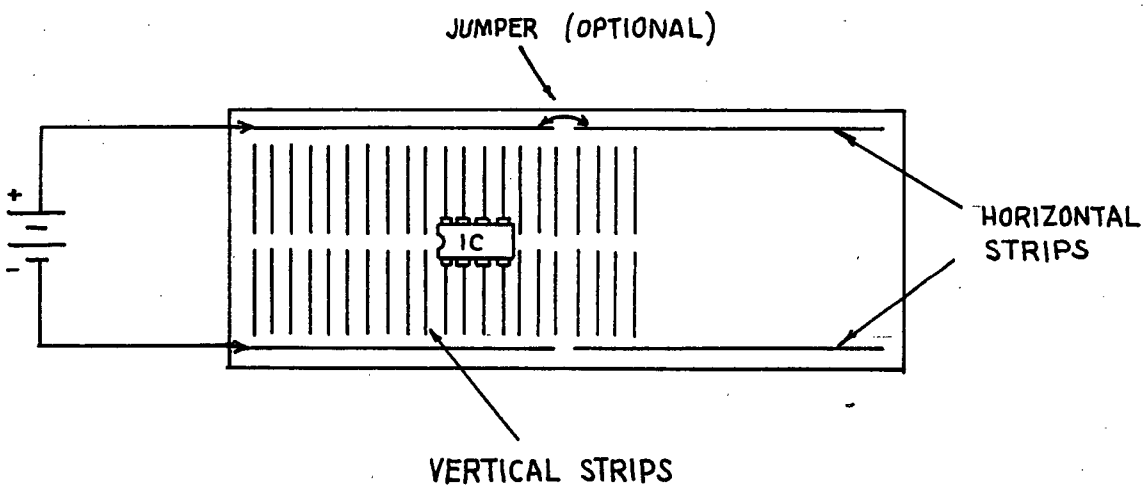
They provide a convenient and easy way to mount integrated circuits and the accompanying peripheral components.

Strip bread boards consist of distribution metal strips. These strips are covered by a perforated plastic surface. The components get inserted in the available plug-in-tie points without the need to solder such connections.

Each metal strip looks like a U-shaped miniature trough. Components and integrated circuits get inserted into them. Care must be taken to prevent excessive stress, for example large diameter wires can damage the shape of the strip. The recommended wire gauge is #22. Such wires can fit firmly without slipping out or deforming the strip.



Matrix arrangement of these strips vary with the manufacturer, but in general, horizontal strips run across the top and also at the bottom of the board, see figure below.

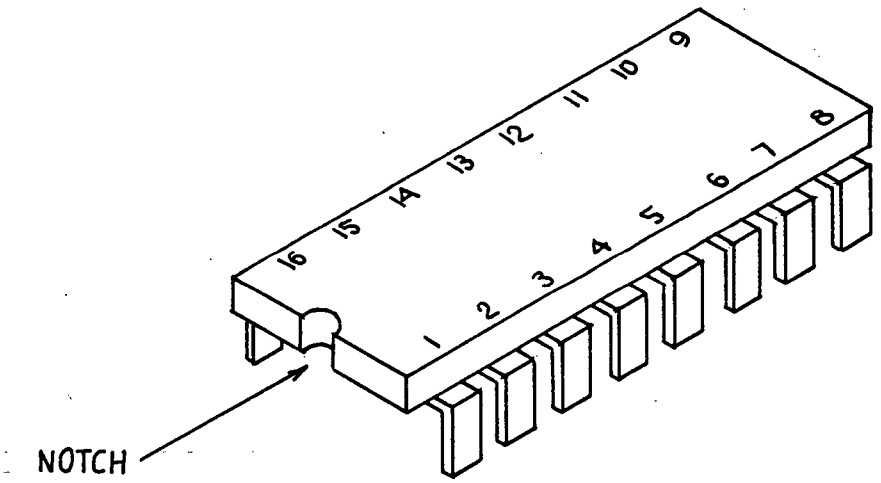


Above horizontal strips can be used to supply power to the components on the board. For example, the top strip can be connected to the positive end of a battery and the bottom strip to the negative end.

Notice that these strips do not run fully across the board, and if it is desired to use all the top for positive voltage supply, one must add jumpers, as shown in the figure above.

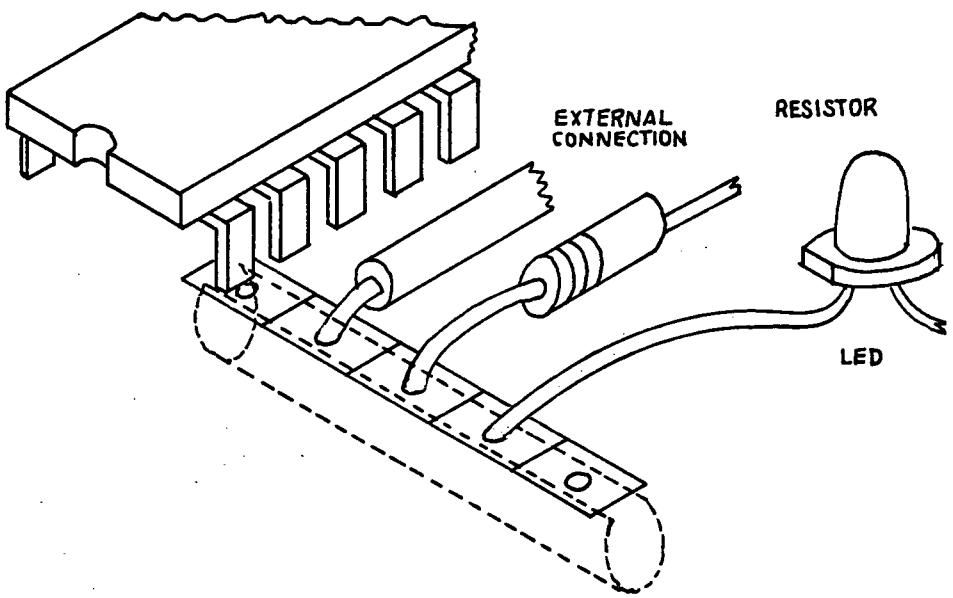
To provide power to the different components, a battery holder and four size D batteries may be used. This power supply will be sufficient for most of the experiments in this book.

Vertical strips are used to hold the pins of integrated circuits. Most integrated circuits are of the DIP type, i. e. Dual-In-Line package. In this configuration, the pins are arranged in two rows, one at the top of the IC and the other at its bottom. Each pin is numbered and the count starts counter-clockwise from a notch at the left side of the integrated circuit.



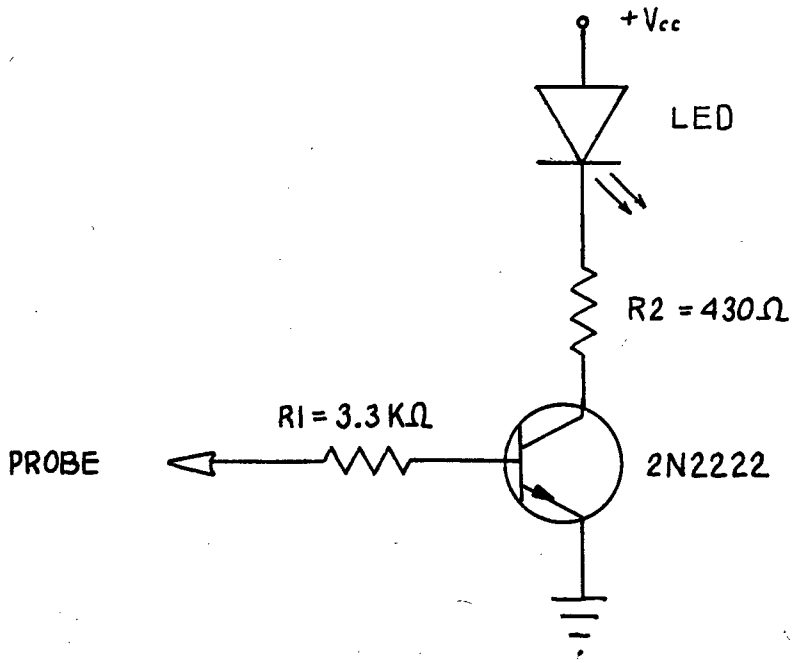
When the integrated circuit is mounted at the center of the bread board, each pin gets inserted on a separte vertical strip.

Each vertical strip provides five tie points. Since one tie point is used for each IC pin, then the four remaining tie points are available for external connections to or from the pin under consideration, as well as for the direct insertion of other electrical components. See the figure below.



PROBE TO TEST LOGIC LEVELS

To test the different logic levels and outputs of integrated circuits, the following circuit may be made into a useful probe.



As a probe, above circuit produces satisfactory results for the voltage levels used in TTL (Transistor-Transistor-Logic) circuits, which is 0 V or +5 V. This circuit uses LED's (Light Emitting Diodes) connected in series with 430 ohm resistors. These resistors limit the current through the LED's, down to the recommended manufacturer's values (about 10 mA), thus protecting the LED's.

Notice that this circuit uses a transistor (2N2222) with high input impedance (3.3 KΩ). This high impedance limits the loading effect on the integrated circuit. This is a desirable feature, since then the test probe does not draw large currents from the IC connections, yet it indicates whether the IC pin connection has a HI condition, or a LO condition.

The circuit operates as follows. A HI voltage will bias the NPN transistor in such a way that it goes into saturation, i. e., it conducts heavily and turns the LED on. The LED light therefore acts as an indicator of a HI condition at the probe's tip.

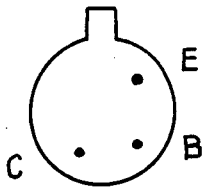
A LO condition at the probe's tip will not be sufficient to bias the transistor's base and consequently the transistor remains in the cut-off condition, i. e. it does not conduct. Consequently the LED will not glow.

This circuit may be assembled on a small piece of vector board. The parts list and the physical connections are shown below.

PARTS LIST

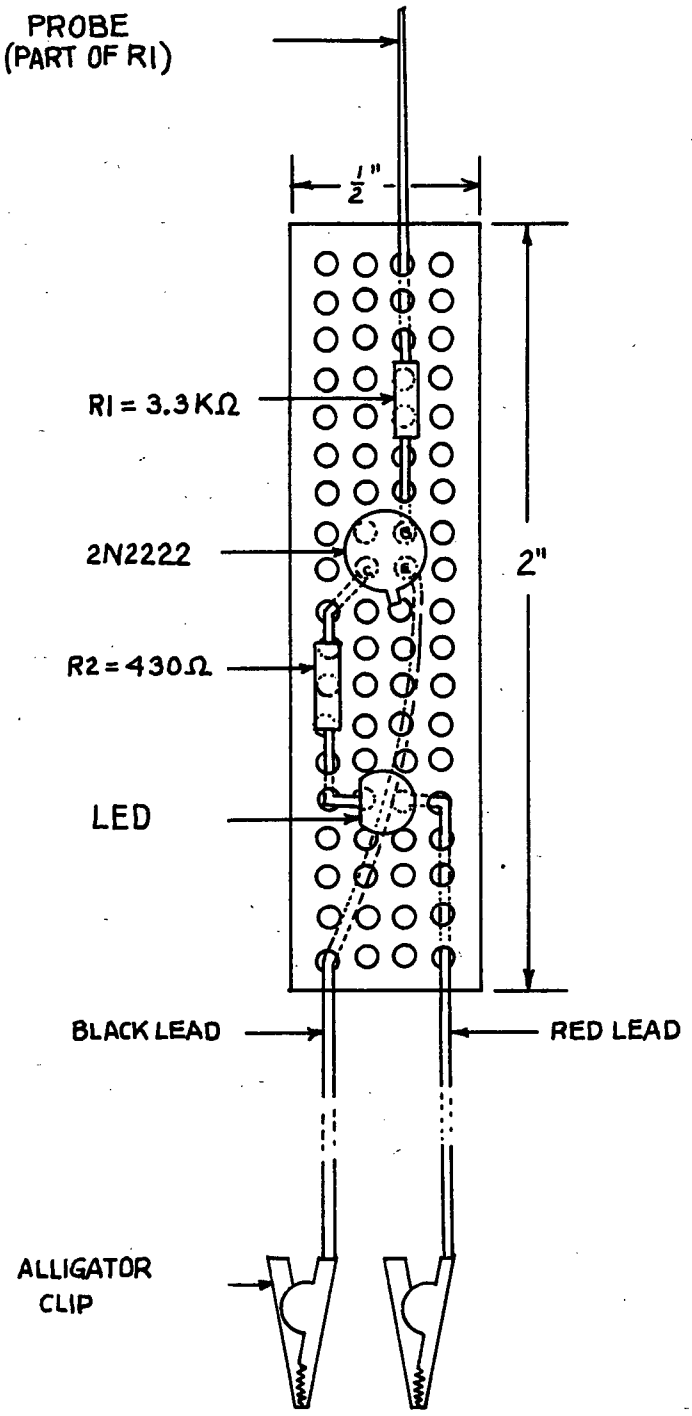
QUANTITY	DESCRIPTION
1	3.3 KΩ Resistor (R_1)
1	430Ω Resistor (R_2)
1	2N2222 Transistor (NPN)
1	LED Light Emitting Diode
2	Alligator Clips
1	18" #22 Red Wire
1	18" #22 Black Wire
1	½" x 2" Vector Board #169P84-062 (Sylmar, California)

2N2222



Bottom View

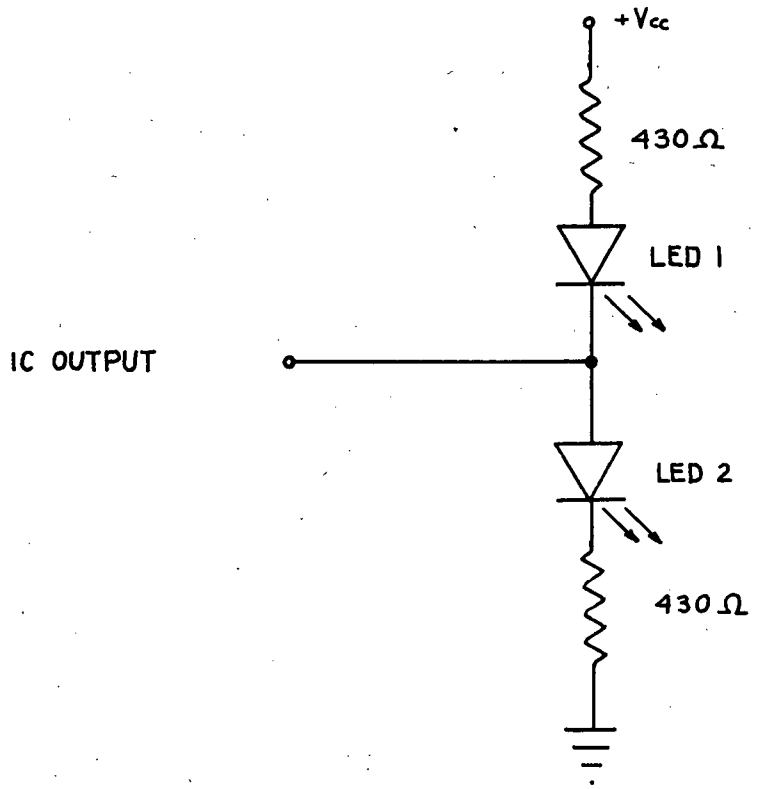
PICTORIAL DIAGRAM



LOGICAL INDICATOR ON IC CIRCUITS

The following circuit may be installed on the strip bread board, to indicate HI, LO or both conditions. It is used on IC's that are not driving other loads or IC's. When a HI condition occurs at the probe tips, LED2 will be driven into conduction by the IC, thus indicating a HI. When a LO condition is being present, the LED1 will permit current through it into the IC, i. e. the IC will sink this flow of current, lighting LED1.

For most applications, the connection of LED1 will be sufficient to indicate the conditions of an IC or of a Counter.



ELECTRONICS COMPONENTS FOR COURSE

The following is a list of the suggested electronics components required for most of the experiments in this book.

ITEM	RECOMMENDED QUANTITY
INTEGRATED CIRCUITS	
555	1
μA741	2
FND 507	1
FND 500	1(Optional)
4066	1
7400	2
7402	2
7404	1
7410	1
7413	1
7427	1
7442	1
7447	1
7448	1(Optional)
7476	2
7486	1
7490	2
74107	2
74LS190	1
74LS283	1

ITEM	RECOMMENDED QUANTITY
SEMICONDUCTORS	
LED's RED	5
LED's GREEN	5
DIODE 1N4005	4
1N761/5.4V Zener Diode	1
2N2222 (NPN)	1
CAPACITORS	
10 μF	1
22 μF	1
RESISTORS	
430Ω, $\frac{1}{4}$ W	7
3.3 kΩ, $\frac{1}{4}$ W	2
4.7 kΩ, $\frac{1}{4}$ W	4
10 kΩ, $\frac{1}{4}$ W	6
22 kΩ, $\frac{1}{4}$ W	2
39 kΩ, $\frac{1}{4}$ W	4
82 kΩ, $\frac{1}{4}$ W	6
1 MΩ, $\frac{1}{4}$ W	1
2.2 MΩ, $\frac{1}{4}$ W	2
1 MΩPotentiometer	2
STRIP BREAD BOARD	1

NOTE.- Should the reader be interested in purchasing above components in a single package, please address:

AB DIGITECH CORP.
STATION S, P. O. BOX 76711
Vancouver, B. C.

LOGICAL CIRCUITS

INTRODUCTION

The basic component in logical circuits are switches. A switch is either "on" or "off", not in between. Since switches can have either one of two values, we find that there are many components that can satisfy this condition. Those two conditions are referred by different names such as: on/off; hi/lo; true/false; 1/0; set/reset; hole/no-hole; saturated/cut-off; open/closed; etc.

In order to deal with a number system consisting of the values "0" or "1", extensive use is made of Boolean Algebra. This is a mathematical system devised by the British mathematician George Boole (1815-1864). During Boole's lifetime, this algebra did not find substancial practical application, but in 1938, the Bell Telephone Company found it very suitable to describe the telephone switching gear. Ten years later, with the advent of the first commercial computers, such as ENIAC, it was found that Boolean Algebra not only simplified the concepts involved in computer design, but became indispensable in their understanding.

BOOLEAN ALGEBRA

Boolean Algebra uses two-valued variables called binary variables. These variables are represented by a "1" or a "0". If a variable "A" represents the positions of a switch, then, when the switch is closed, A = 1 and when the switch is open, A = 0

There are three fundamental propositions: NOT, AND, and OR.

The logical circuits divide into two classes: Combinational and Sequential. Combinational circuits are analogous to lock mechanisms, where the tumblers must be pushed the right distance by a key. Sequential circuits are analogous to combination locks, where the right sequence of turns must be used to open them.

In the combinational class, time is not important, but as we get into the sequential circuits, we will have to consider time as an important element to determine the sequence of events.

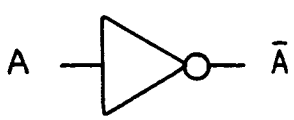
FUNDAMENTAL OPERATIONS

NOT

The NOT operation negates the condition of a switch. If switch "A" is true, i. e. A = 1, then, by the use of the NOT operation it becomes $\overline{A}$, i. e. a zero. $\overline{A}$ is read NOT A, or A NOT.

When dealing with voltage levels, many computer systems use a +5 V to indicate a true value, and a 0 V to indicate a false value. Thus, a NOT operation simply inverts the voltage level.

The logical graphic symbol for the NOT operation is:

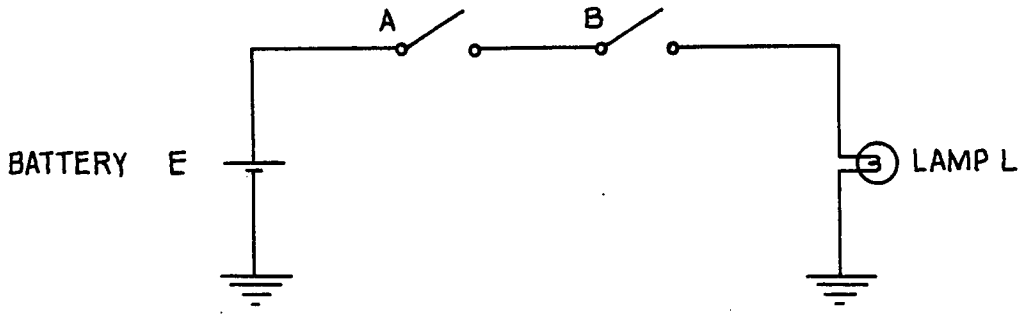


A truth table for this operation is simply the reversal of any initial condition, and is indicated below:

A	$\overline{A}$
0	1
1	0

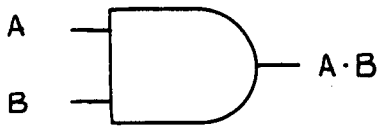
AND

This operation is a form of multiplication. It indicates that two variables must be true for an output to be true. To perform this operation, two switches will be connected as shown below:



The logical algebraic symbol used for this operation is a dot between variables, or simply no symbol between them, i. e. A·B or AB, and it is read A AND B.

The logical graphic symbol for an AND operation device or gate is:

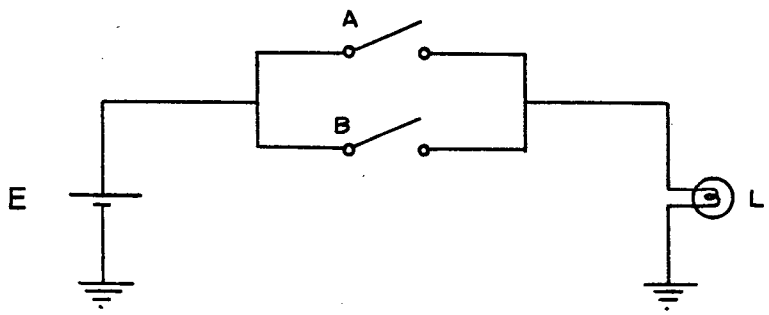


Its corresponding truth table is:

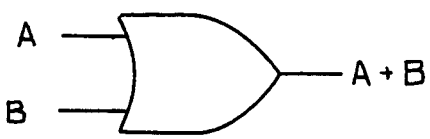
A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1

OR

This operation is a form of addition and indicates that either one of two variables, or both, must be true for an output to be true. See the switch implementation of this operation:



The logic algebraic symbol used for this operation is a plus sign between variables, e. g. A + B, and it is read A OR B. When used in logic diagrams, its graphic symbol is:

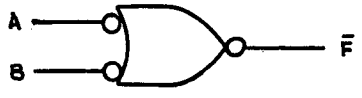


Its truth table is the following:

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

The next page depicts these basic logic symbols and their corresponding truth table. Notice that a small circle at the input of a gate means inversion of the input signal. Also, a small circle at the output of a gate means inversion of the output logical function.

LOGIC SYMBOLS AND THEIR TRUTH TABLES

AND GATES	OR GATES	A	B	F
		1	1	1
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	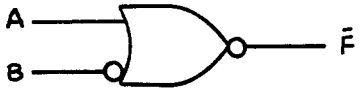	1	1	0
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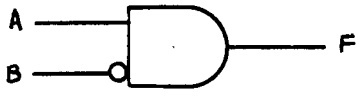
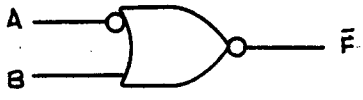
		0	1	1
		0	0	0
		1	1	0
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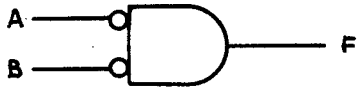	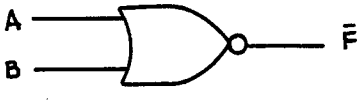	1	1	0
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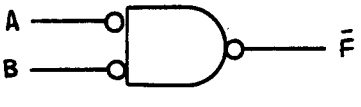	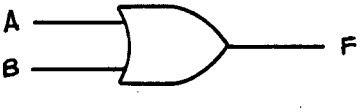	1	1	1
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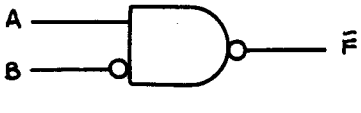	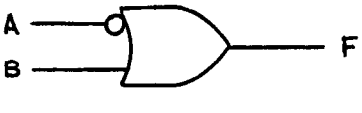	1	1	1
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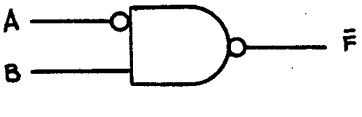	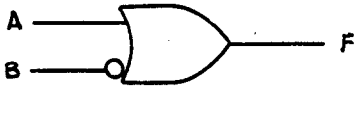	1	1	1
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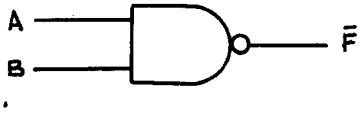
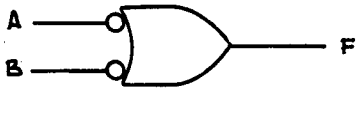
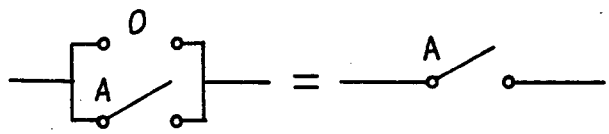
		1	1	0
		1	0	1
		0	1	1
		0	0	1

BOOLEAN ALGEBRA LAWS

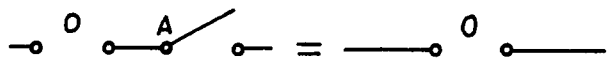
These laws are useful in the simplification of Boolean expressions. We can verify them by the use of truth tables or implementing them with switches.

1.- ONE and ZERO rules

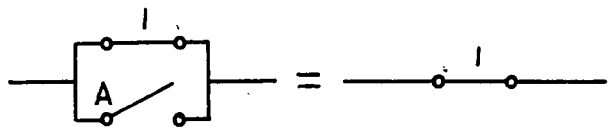
$0 + A = A$



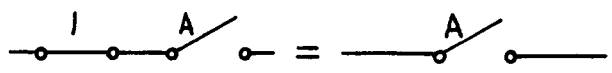
$0 \cdot A = 0$



$1 + A = 1$

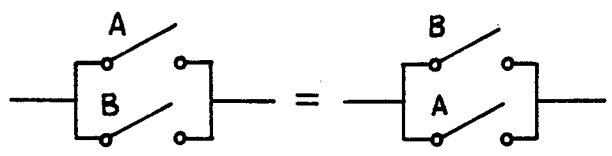


$1 \cdot A = A$

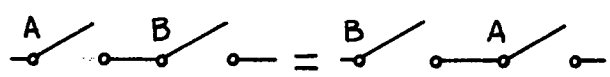


2.- Commutative laws

$A + B = B + A$



$A \cdot B = B \cdot A$



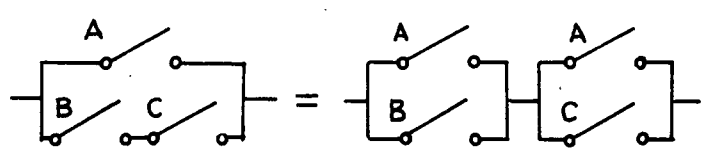
3.- Associative laws

$A + (B + C) = (A + B) + C$

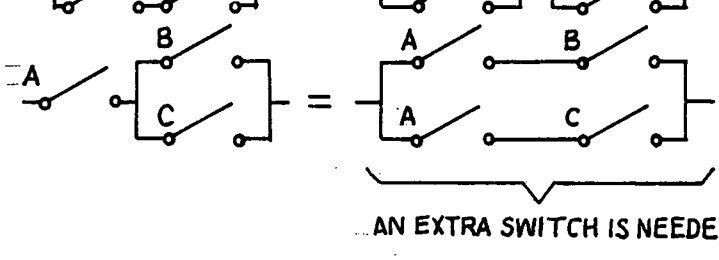
$A \cdot (B \cdot C) = (A \cdot B) \cdot C$

4.- Distributive laws

$A + B \cdot C = (A + B)(A + C)$

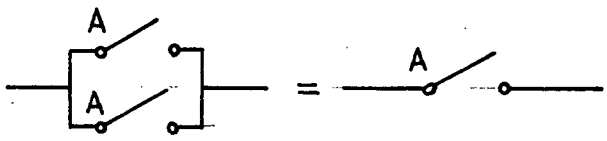


$A(B + C) = A \cdot B + A \cdot C$

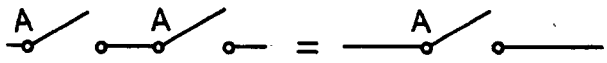


5.- Idempotence laws

$A + A = A$

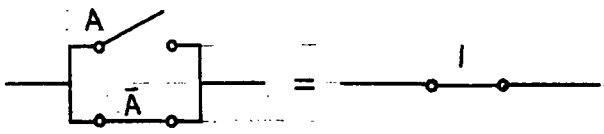


$A \cdot A = A$



6.- Complementary laws

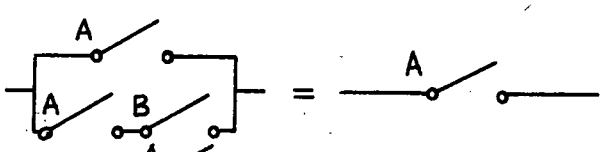
$A + \overline{A} = 1$



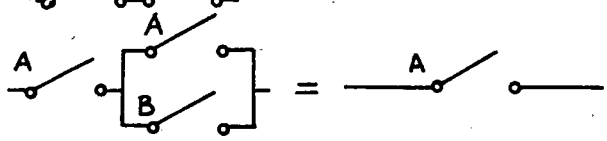
$A \cdot \overline{A} = 0$

7.- Absorption laws

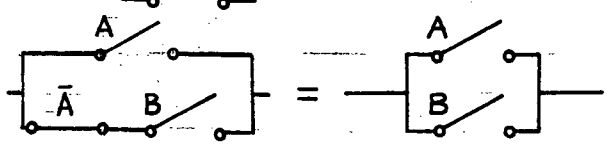
$A + A \cdot B = A$



$A \cdot (A + B) = A$



$A + \overline{A} \cdot B = A + B$



8.- Involution

$$\overline{\overline{A}} = A$$

9.- Inversion laws, also known as DeMorgan's Theorems

$$\overline{(A + B)} = \overline{A}\,\overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

DeMorgan's theorems are very important in the simplification of logical equations, which in turn results in the use of fewer gates while implementing them. Their proof is done by means of truth tables. A graphical proof is discussed under the section of Venn Diagrams.

A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A}$	$\overline{B}$	$\overline{A} + \overline{B}$	$A + B$	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$
0	0	0	1	1	1	1	0	1	1
0	1	0	1	1	0	1	1	0	0
1	0	0	1	0	1	1	1	0	0
1	1	1	0	0	0	0	1	0	0

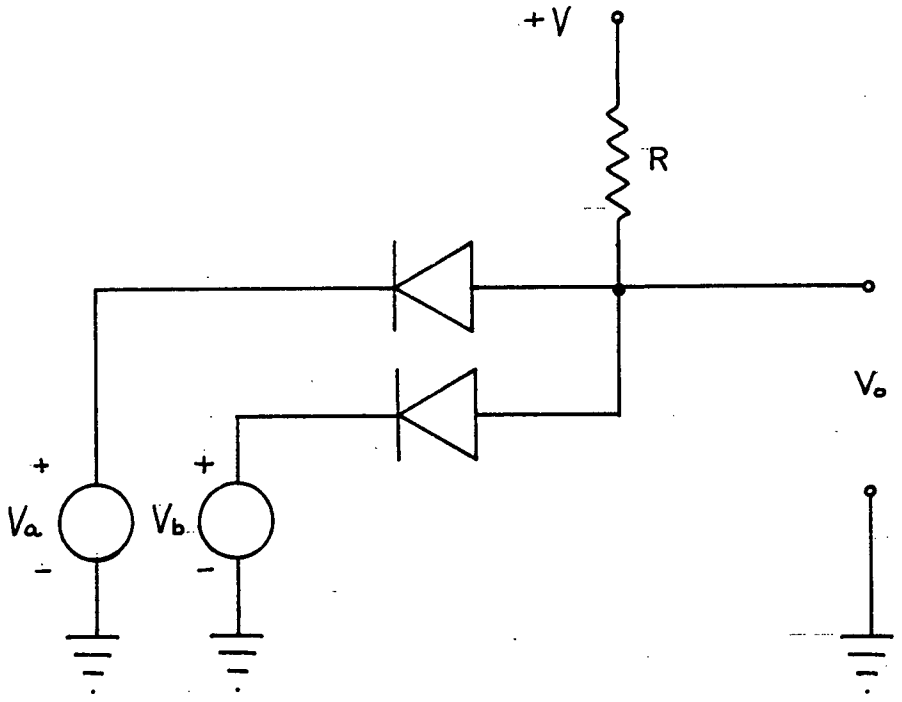
IMPLEMENTATION OF GATES

While implementing gates, we should notice that only two fundamental operations are needed, i. e. either NOT and AND, or NOT and OR. This is due to the fact that a given circuit may be an AND for a logic called positive, and an OR for a logic called negative.

In positive logic, a HI is defined as a "1" and a LO as a "0", whereas in negative logic, the opposite is true, i. e. a HI is a "0" and a LO is a "1".

GATE IMPLEMENTATION USING DIODES

The following circuit corresponds to an AND gate for positive logic and for negative logic it corresponds to an OR gate.



In order to prove above statements, let us consider the output readings obtained with a voltmeter, regardless of the chosen logic.

V_a and V_b can each take on two values, which we designate H for high level and L for low level. Assuming ideal diodes, the output V_o can be tabulated in accordance with the input conditions, as shown below.

V_a	V_b	V_o	REMARKS
L	L	L	Both diodes conducting (short circuit)
L	H	L	
H	L	L	
H	H	H	Both diodes off (open circuit)

Using positive logic, an "H" will be a "1" and an "L" will be a "0", therefore above table becomes:

A	B	V_o
0	0	0
0	1	0
1	0	0
1	1	1

From the truth table, it is easy to see that V_o = A B and that it satisfies the conditions for an AND gate.

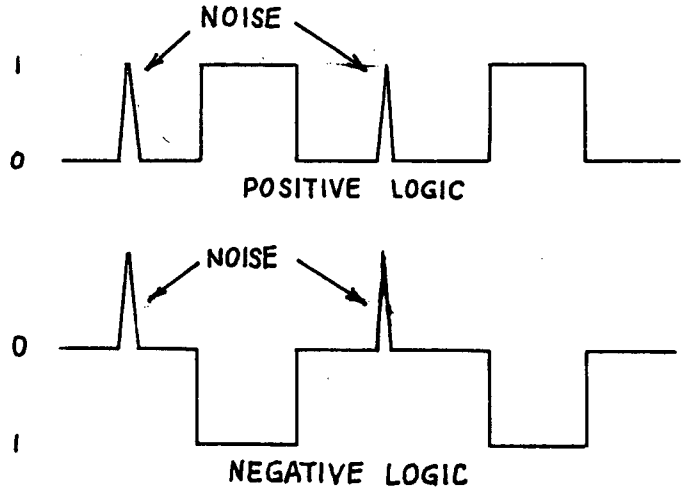
If on the other hand, we use negative logic, then we must interpret "H" as a "0" and "L" as a "1", in which case the voltage table becomes:

A	B	V_o
1	1	1
1	0	1
0	1	1
0	0	0

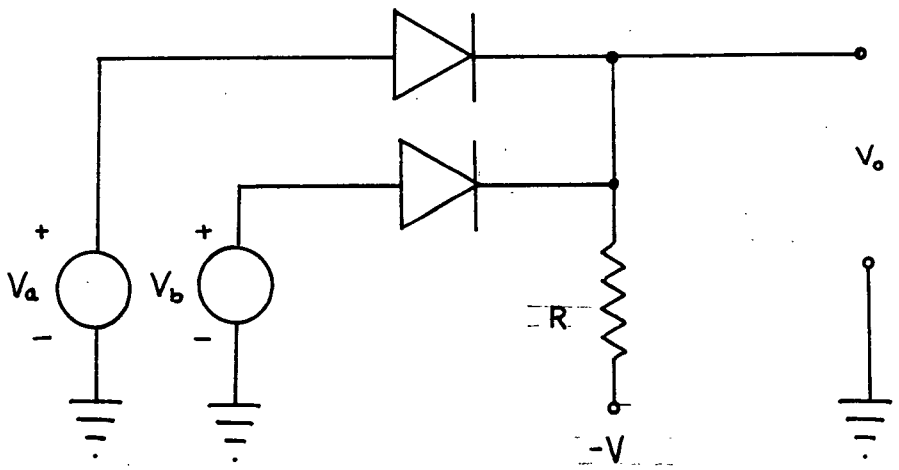
Above truth table satisfies the condition V_o = A + B and corresponds to an OR gate.

From this example, it can be seen that the same piece of hardware can be used as an AND gate or an OR gate, depending on our definitions of positive or negative logic.

Negative logic is often used in the transmission of data, where noise in the form of voltage spikes may introduce errors in the transmitted data. When positive logic is used, each spike may be interpreted as a "1", whereas in negative logic, a spike will be interpreted as a zero, and negative spikes do not occur.



Let us consider above same circuit, except that this time we reverse the bias. The bias reversal makes it into an OR gate for positive logic and an AND gate for negative logic.



Using a voltmeter, we can tabulate our physical results as shown below.

V_a	V_b	V_o	REMARKS
L	L	L	Neither diode conducts
L	H	H	Diode in series with V_b conducts causing V_R across R that makes the output positive.
H	L	H	
H	H	H	

Using positive logic, the resulting truth table is the one that corresponds to a logical OR gate:

A	B	V_o
0	0	0
0	1	1
1	0	1
1	1	1

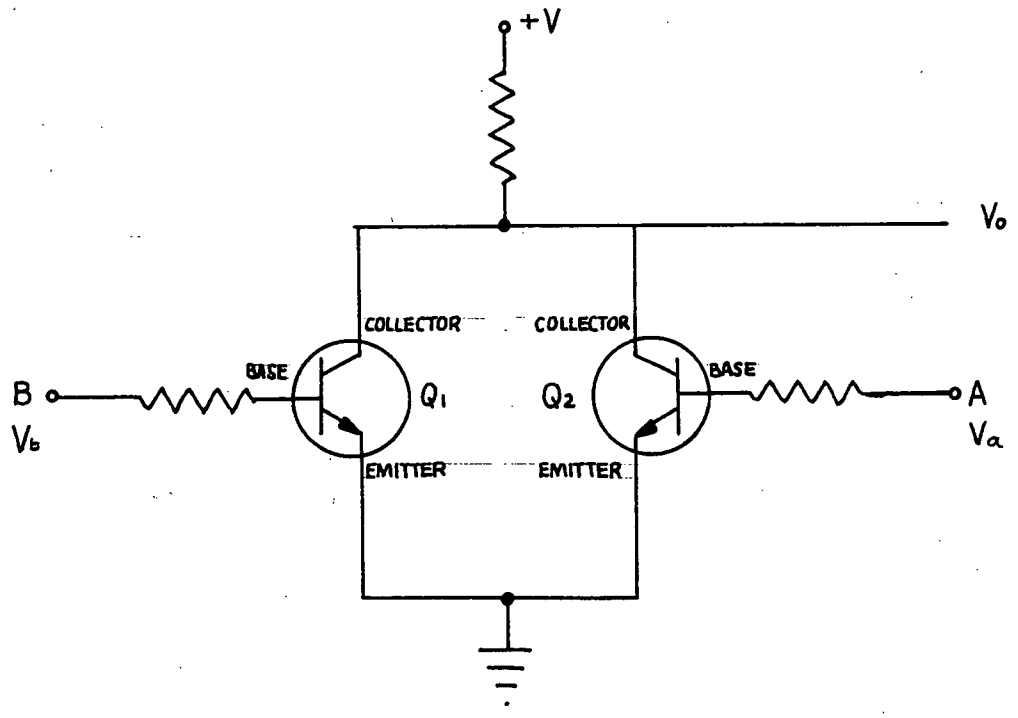
Applying negative logic, we find that the resulting truth table corresponds to a logical AND gate:

A	B	V_o
1	1	1
1	0	0
0	1	0
0	0	0

Because diodes do not have gain, their use is limited. Therefore, we will consider the use of transistors to implement logical functions.

GATE IMPLEMENTATION USING TRANSISTORS

Consider the following circuit, we shall prove that for positive logic it represents a NOR gate (NOT OR), and for negative logic it represents a NAND gate (NOT AND).



NOTE.- The transistors shown in the circuit above are NPN type, since the arrow in the emitter points out. This type of transistor, in order to conduct, requires a positive voltage at its base. For switching transistors, a positive voltage at their base causes them to conduct heavily, that is, they become saturated and appear as a virtual short circuit to ground. A negative voltage at their base causes them to cut-off, and they stop conducting, acting as an open circuit.

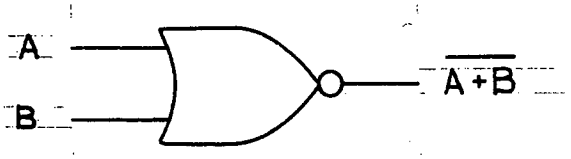
Based on the principle of operation of transistors, we can build a table with the different combinations and output results that a voltmeter would indicate.

V_a	V_b	V_o
L	L	H
L	H	L
H	L	L
H	H	L

The positive logic table where H = "1" and L = "0", shows that above circuit corresponds to the NOR operation, i. e. to $\overline{A + B}$

A	B	V_o
0	0	1
0	1	0
1	0	0
1	1	0

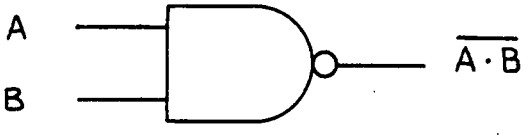
The logic graphic symbol for a NOR gate is:



The negative logic table, where H = "0" and L = "1", shows that above circuit corresponds to the NAND operation, i. e. to $\overline{A\ B}$

A	B	V_o
1	1	0
1	0	1
0	1	1
0	0	1

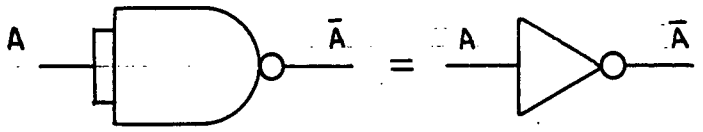
The logic graphic symbol for a NAND gate is:



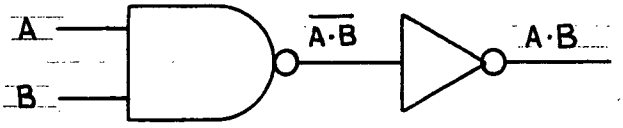
UNIVERSALITY OF NAND

It is advisable, from the economics point of view, to have a piece of hardware that does all the work. Thus, we can build all the logical functions with NAND gates or with NOR gates.

INVERTER USING NAND GATES



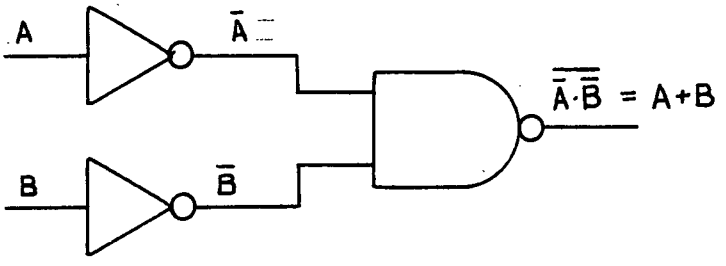
AND GATE USING NAND'S



OR GATE USING NAND'S

To implement an OR gate using NAND gates, one can make use of DeMorgan's Theorem: $\overline{\bar{A} \cdot \bar{B}} = A + B$

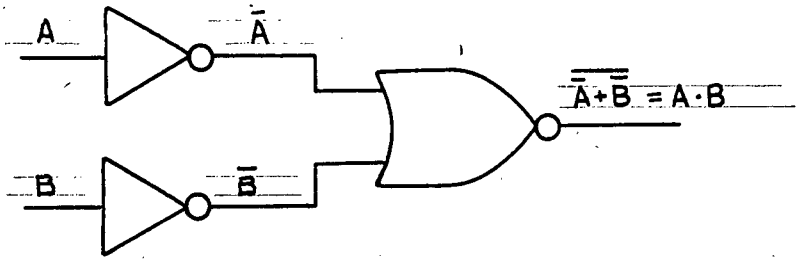
Therefore:



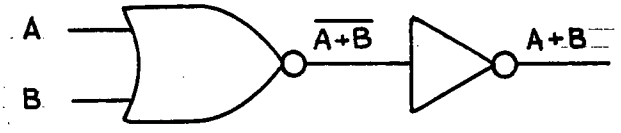
AND GATE USING NOR'S

To implement an AND gate using NOR gates, one can make use of the second DeMorgan's Theorem: $\overline{\bar{A} + \bar{B}} = A \cdot B$

Therefore:

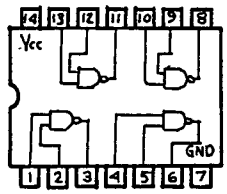


OR GATE USING NOR'S



PIN LAY OUT FOR INTEGRATED CIRCUITS

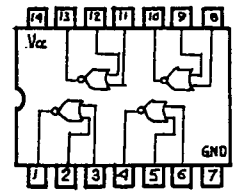
The pin connections for the integrated circuits suggested in in this text are included next. Most of these integrated circuits belong to the TTL family (Transistor Transistor Logic). They require minimum electrostatic charge care while handling.



7400

QUAD 2-INPUT NAND GATE

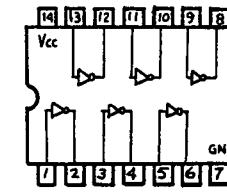
POSITIVE LOGIC : $Y = \overline{AB}$



7402

QUAD 2-INPUT NOR GATE

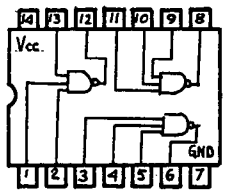
POSITIVE LOGIC $Y = \overline{A+B}$



7404

HEX INVERTER

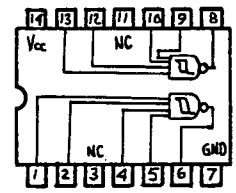
POSITIVE LOGIC $Y = \overline{A}$



7410

TRIPLE 3-INPUT NAND GATE

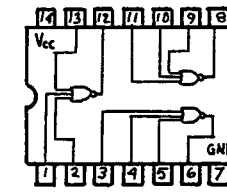
POSITIVE LOGIC: $Y = \overline{ABC}$



7413

DUAL 4 INPUT SCHMITT TRIGGER

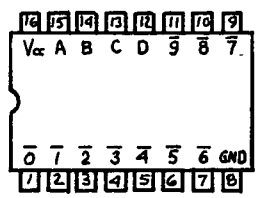
POSITIVE LOGIC : $Y = \overline{ABCD}$



7427

TRIPLE 3-INPUT NOR GATE

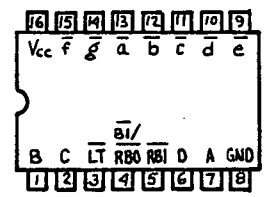
POSITIVE LOGIC : $Y = \overline{A+B+C}$



7442

FOUR LINE TO TEN LINE DECODER

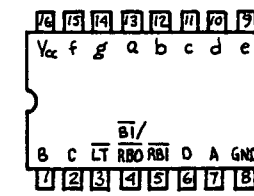
(1 - OF - 10)



7447

BCD TO 7-SEGMENT

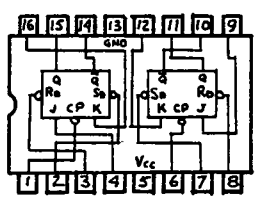
DECODER / DRIVER



7448

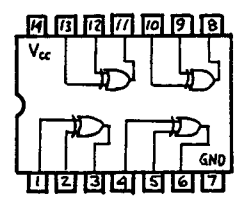
BCD TO 7-SEGMENT

DECODER



7476

DUAL JK MASTER/SLAVE FLIP FLOP WITH SEPARATE SETS (PRESETS), CLEARS (PRERESETS) & CLOCKS

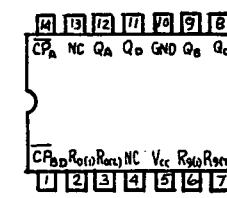


7486

QUAD 2-INPUT

EXCLUSIVE-OR GATE

POSITIVE LOGIC : $Y = A \oplus B$

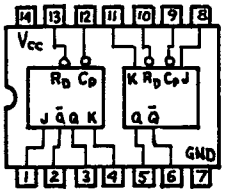


7490

DECADE COUNTER

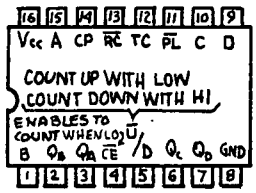
R_0 — RESET — ZERO INPUTS

R_9 — RESET — NINE INPUTS



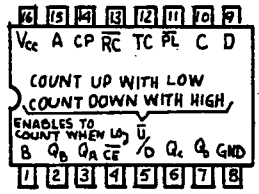
74107

DUAL JK MASTER/SLAVE FLIP-FLOP WITH SEPARATE CLEARS(PRERESETS) AND CLOCKS



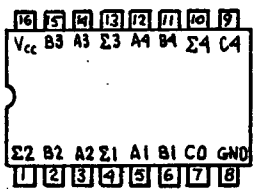
74LS190

SYNCHRONOUS UP/DOWN DECADE COUNTER WITH PRESET AND RIPPLE CLOCK



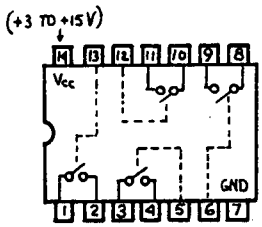
74LS191

SYNCHRONOUS UP/DOWN BINARY COUNTER WITH PRESET AND RIPPLE CLOCK



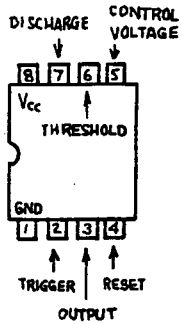
74LS283

FOUR BIT BINARY FULL ADDER WITH FAST CARRY

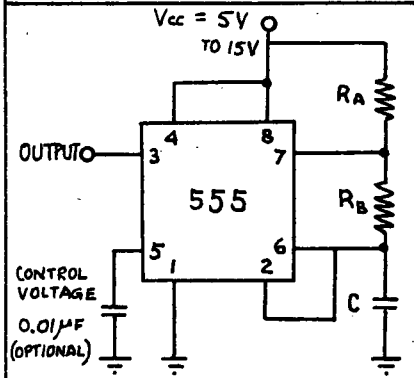


4066

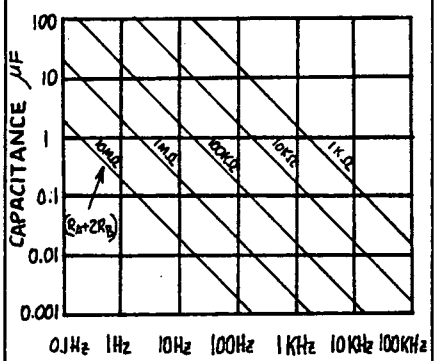
QUAD BILATERAL SWITCH SHOWN IN DIGITAL MODE



555 TIMER



555 IN ASTABLE MODE



FREE RUNNING FREQUENCY

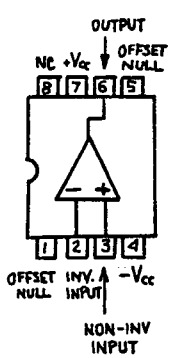
CHARGE TIME (OUTPUT HIGH) : $0.693(R_A+R_B)C$

DISCHARGE TIME (OUTPUT LOW) : $0.693\,R_B C$

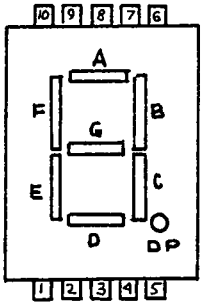
PERIOD : $0.693(R_A+2R_B)C$

$$\text{FREQUENCY} = \frac{1.44}{(R_A+2R_B)C}$$

$$\text{DUTY CYCLE} = \frac{R_B}{R_A+2R_B}$$

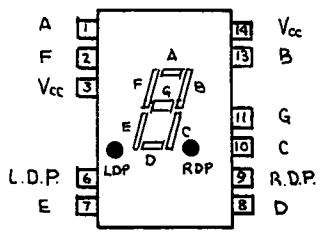


μA741N, μA741CN



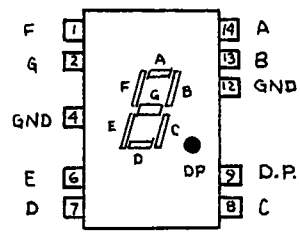
FND 507/567 COMMON ANODE
FND 500/560 COMMON CATHODE

PIN	FND 507/567	FND 500/560
1	SEGMENT E	SEGMENT E
2	SEGMENT D	SEGMENT D
3	COMM. ANODE	COMM. CATH.
4	SEGMENT C	SEGMENT C
5	DEC. POINT	DEC. POINT
6	SEGMENT B	SEGMENT B
7	SEGMENT A	SEGMENT A
8	COMM. ANODE	COMM. CATH.
9	SEGMENT F	SEGMENT F
10	SEGMENT G	SEGMENT G



TIL 312 COMMON ANODE
DP = DEC. POINT; L = LEFT ; R = RIGHT

PIN 1	CATHODE A
PIN 2	CATHODE F
PIN 3	ANODE DIGIT & DECIMAL
PIN 4	OMITTED
PIN 5	OMITTED
PIN 6	CATHODE LEFT DECIMAL
PIN 7	CATHODE E
PIN 8	CATHODE D
PIN 9	CATHODE RIGHT DECIMAL
PIN 10	CATHODE C
PIN 11	CATHODE G
PIN 12	OMITTED
PIN 13	CATHODE B
PIN 14	ANODE DIGIT & DECIMAL



MAN 3640 COMMON CATHODE
D.P. = DECIMAL POINT

PIN 1	ANODE F
PIN 2	ANODE G
PIN 3	OMITTED
PIN 4	COMMON CATHODE
PIN 5	OMITTED
PIN 6	ANODE E
PIN 7	ANODE D
PIN 8	ANODE C
PIN 9	ANODE DECIMAL POINT
PIN 10	OMITTED
PIN 11	OMITTED
PIN 12	COMMON CATHODE
PIN 13	ANODE B
PIN 14	ANODE A

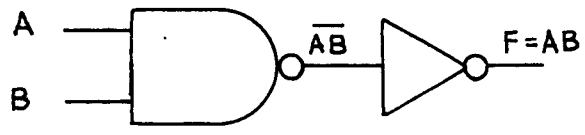
LABORATORY

Using the data provided for the above list of integrated circuits, the student can assemble the circuits so far discussed. The assembly is done on a strip bread board. A probe like the one described in the beginning of this book will enable the student to verify the operation of these circuits. This check is done by comparing the truth tables with the electrical results.

The integrated circuits needed so far, include: 7400, 7402 and 7404.

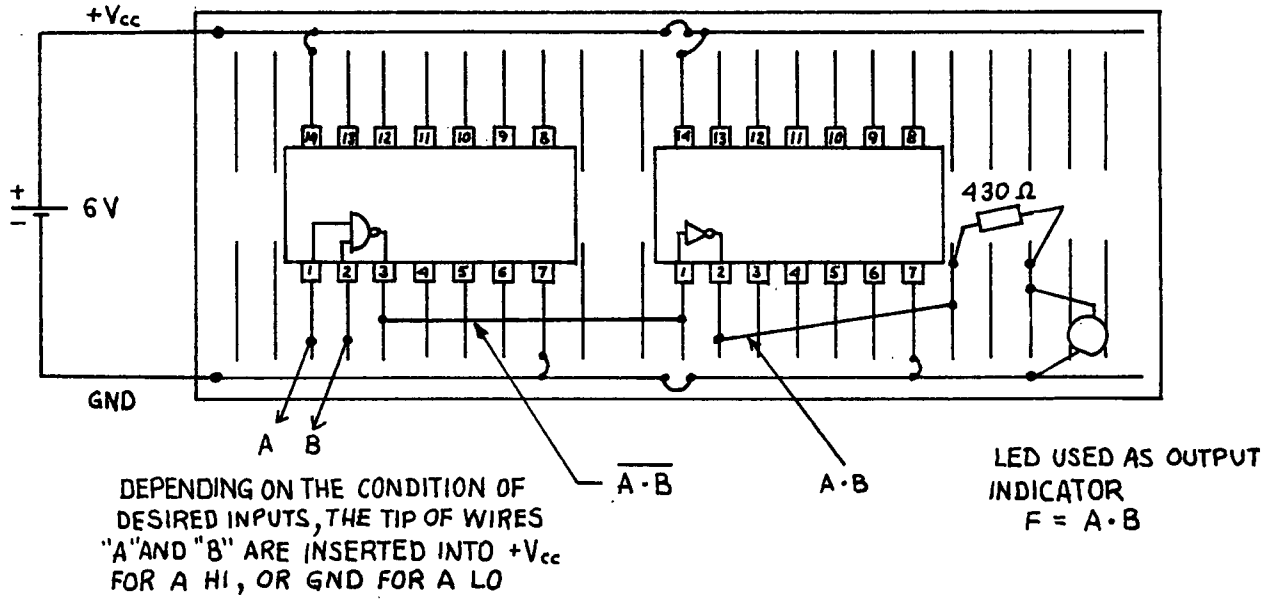
EXAMPLE.- Test the AND gate using NAND's.

The logical circuit and truth tables are given below.



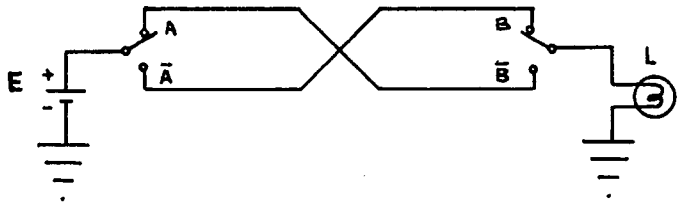
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

The physical connections are shown below.



EXCLUSIVE OR

An Exlcusive Or is also known as: Half Add, Partial Add, Selective Complement or Add Modulus-2. It is defined as the condition where the output is true if EITHER ONE OF THE INPUTS IS TRUE BUT NOT BOTH. This condition is found in the three-way switches used in stairways and house corridors. One can turn one switch on to turn a light on, but not both switches. See figure.



LAMP L IS ON WHEN
$A \cdot \bar{B}$ OR $\bar{A} \cdot B$
LAMP L IS OFF WHEN
$A \cdot B$ OR $\bar{A} \cdot \bar{B}$

The logical algebraic symbol for an "exclusive or" is $\oplus$ and its truth table is the following.

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

There are several equation forms that describe the exclusive or, some of them are listed below.

$$A \oplus B = A \cdot \overline{B} + \overline{A} \cdot B$$

$$= \overline{\overline{A}\,\overline{B}}\,(A + B) = (\overline{A} + \overline{B})(A + B)$$

$$= \overline{\overline{A\,(\overline{A}\,\overline{B})}\;\overline{B\,(\overline{A}\,\overline{B})}}$$

$$= \overline{\overline{A} + \overline{B} + A + \overline{A} + \overline{B} + B}$$

All forms above can be proven with the use of truth tables or by means of Boolean Algebra manipulation. For example, using DeMorgan's theorem $\overline{a \cdot b} = \overline{a} + \overline{b}$, we can prove the following:

$$A \oplus B = \overline{\overline{A\,(\overline{A}\,\overline{B})}\;\overline{B\,(\overline{A}\,\overline{B})}}$$

$$\overline{\overline{A\,(\overline{A\,B})}}\;\overline{\overline{B\,(\overline{A\,B})}} = \overline{\overline{A\,(\overline{A\,B})}} + \overline{\overline{B\,(\overline{A\,B})}}$$

$$= A\,(\overline{A\,B}) + B\,(\overline{A\,B})$$

$$= A\,(\overline{A} + \overline{B}) + B\,(\overline{A} + \overline{B})$$

$$= A\,\overline{A} + A\,\overline{B} + B\,\overline{A} + B\,\overline{B}$$

$$= A\,\overline{B} + \overline{A}\,B \qquad \text{(Q. E. D.)}$$

The truth table of an exclusive or is also the table for the addition of two one-bit binary numbers. Therefore, there are many important applications for this operation.

ADDITION OF BINARY NUMBERS

The four possible conditions for the addition of two one-bit binary numbers are shown below.

0	0	1	1
+ 0	+ 1	+ 0	+ 1
0	1	1	1 0
			↑ CARRY

If variables A and B are used to represent above values, then the following truth table will result.

A	B	S(SUM)	C(CARRY)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

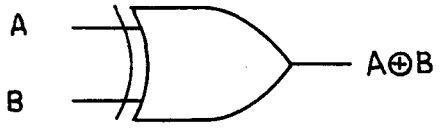
Comparing the results of the column S (SUM), in the table above, with the truth table for an "exclusive or", we find that:

$$S = A \oplus B$$

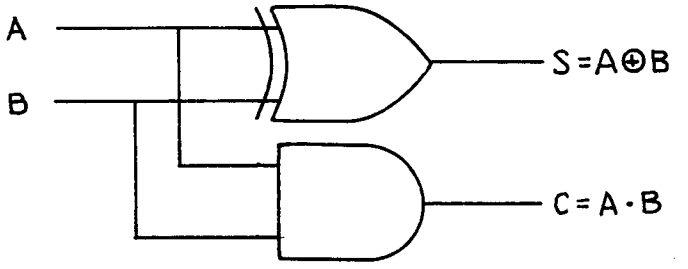
The column for the carry can also be represented by the logical function:

$$C = A \cdot B$$

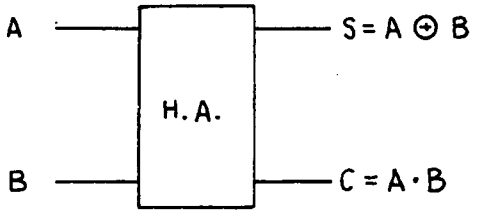
The logical symbol assigned to an exclusive or is:



Then, a "half-adder" can be represented by the following logical circuit:

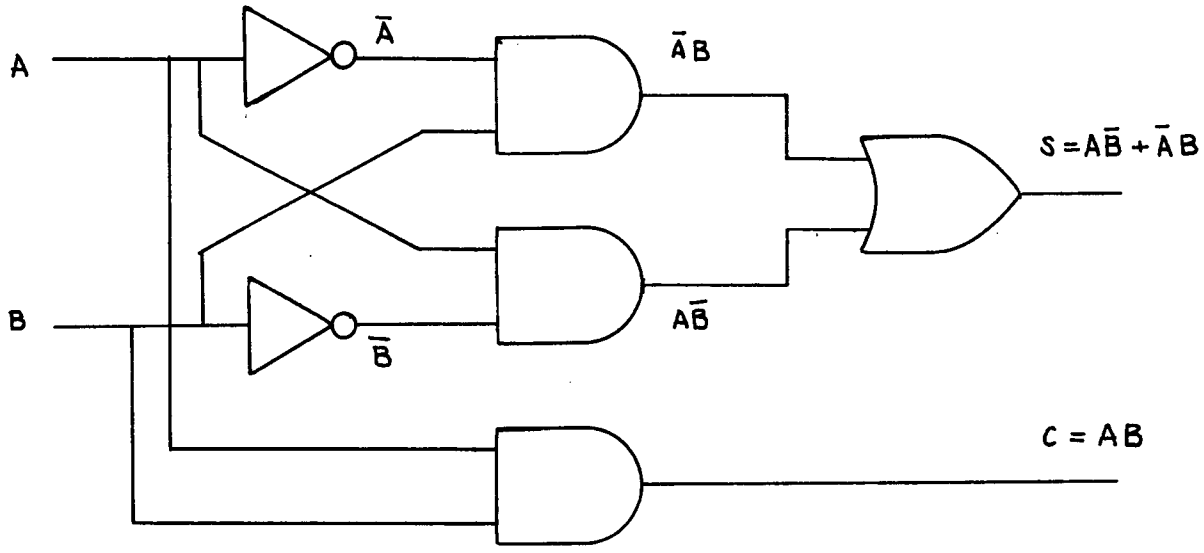


The logical symbol for a "half-adder" is:

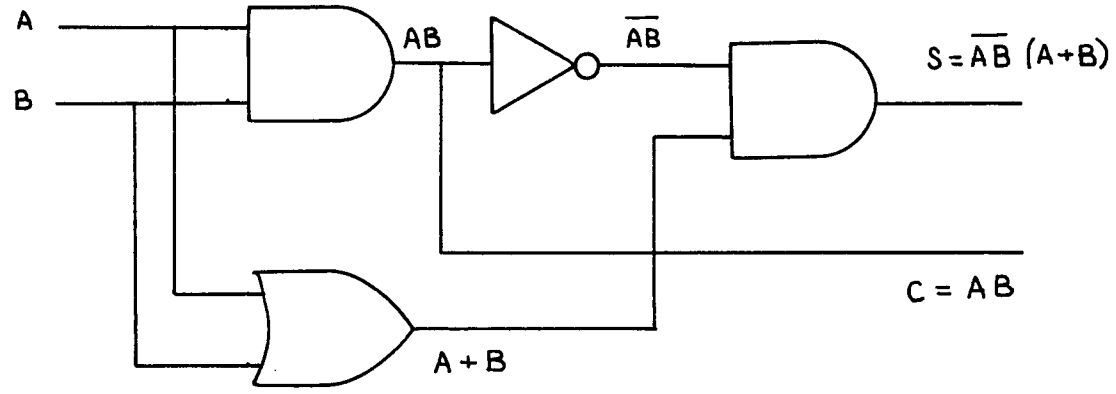


IMPLEMENTATION OF A HALF-ADDER

a) Using simple AND and OR gates:

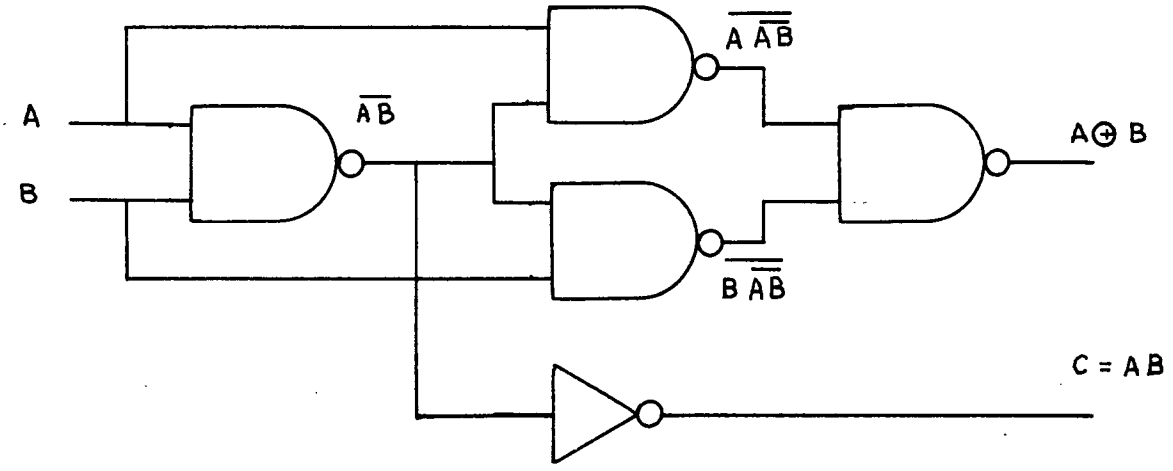


b) Using DeMorgan's Theorem, a half-adder can be simplified further. The equation used is: $A \oplus B = \overline{A \cdot B}\ (A + B)$



It should be noticed that this circuit uses two gates less than the circuit in (a). That is, the implementation of circuits is greatly facilitated by the use of simpler equivalent Boolean expressions. Other methods to reduce complex expressions are discussed under Karnaugh Maps.

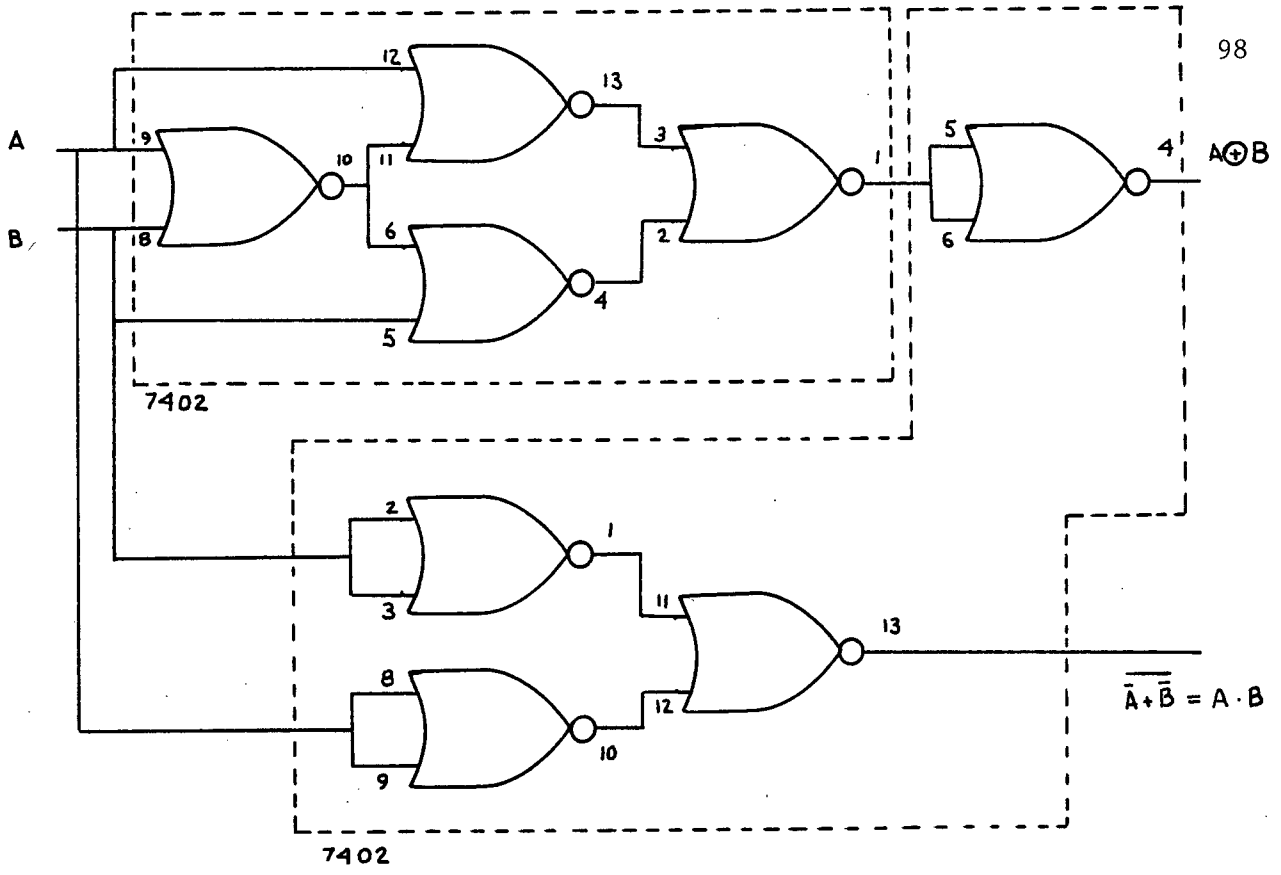
c) Using NAND gates and the identity: $A \oplus B = \overline{A \cdot \overline{A \cdot B}} \cdot \overline{B \cdot \overline{A \cdot B}}$



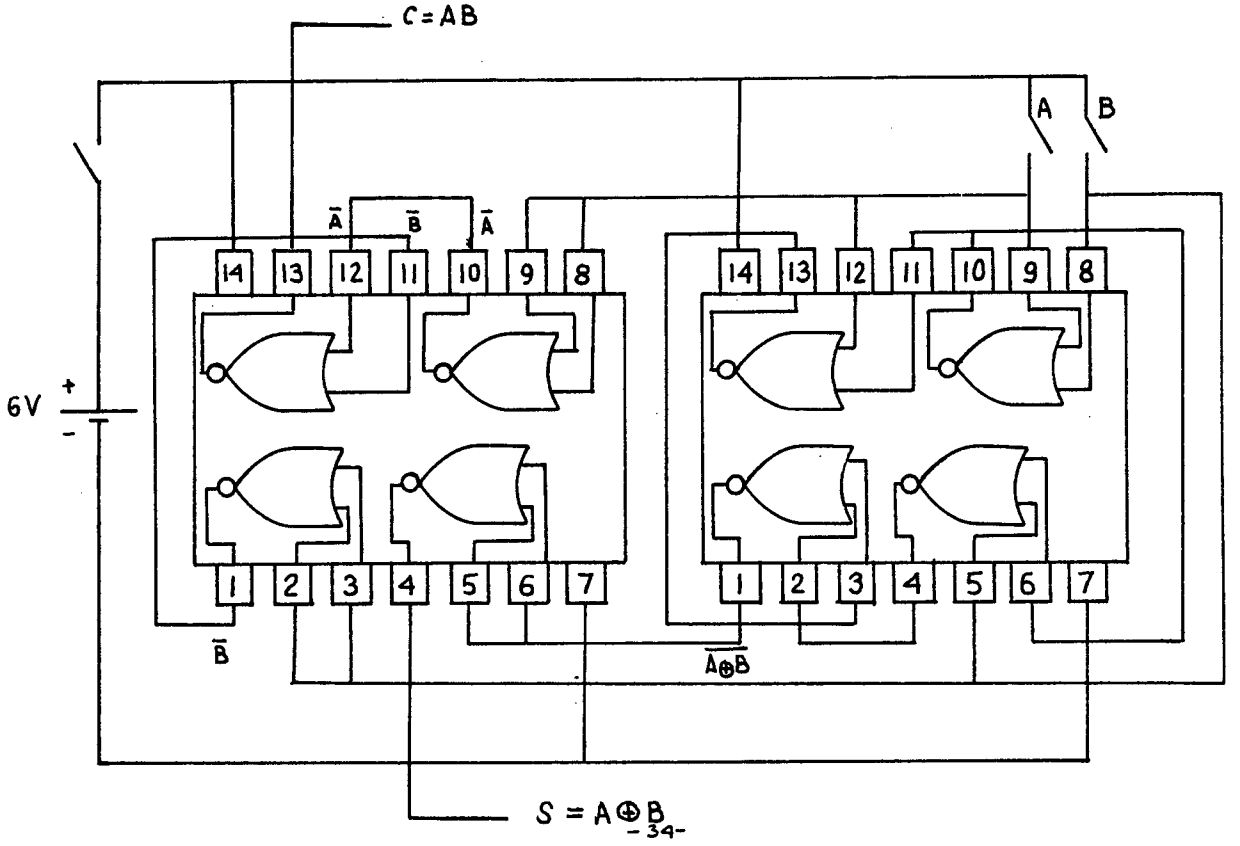
Although above circuit uses an extra gate compared with the circuit in (b), it has the advantage of permitting us to implement the circuit with only NAND gates. It will not be necessary to have IC's with different functions on the same strip bread board. At an early stage in the development of Digital Systems, this advantage also resulted in economic savings.

d) Implementation using NOR gates. The figure below shows the logic diagram. It can be assembled by using two 7402 IC's. The 7402 is a QUAD 2 I/P NOR GATE. QUAD means that there are four NOR gates. Each NOR gate has two inputs. The suggested pin connections for each gate have been indicated on this diagram. It is advisable that the student gets the habit of indicating his pin connections, for it will help him while testing and troubleshooting his circuits.

NOTE.- Anyone of above circuits can be assembled on a strip bread board. The truth tables may be corroborated using LED's or a logic levels probe. It is also recommended to test the integrated circuit 7486, that corresponds to a Quad 2-Input Exclusive Or Gate.



A pictorial diagram of connections for the same half-adder is shown below.



MECHANIZATION OF ADDITION OF BINARY NUMBERS

Consider the addition of binary variables A and B below:

	9	8	7	6	5	4	3	2	1
A =	1	0	0	1	0	1	1	0	1
+ B =	1	1	0	1	1	0	1	0	0
A + B =	0	1	1	1	0	0	0	0	1

In the process of adding above variables, we find that the sixth column from right to left yields the sum $S_n = 1$. The subscript n refers to the column number, and in this particular case $n = 6$. The sum S_6 consists of A_6 plus B_6 and also a carry C_5 that originates in the previous column. The previous column can be referred in general as C_{n-1}. Sum S_6 also produces a carry C_6 of its own, referred below as C_n.

The table below considers all the possible combinations of A_n, B_n and C_{n-1}, and the resulting S_n and C_n values.

C_{n-1}	A_n	B_n	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

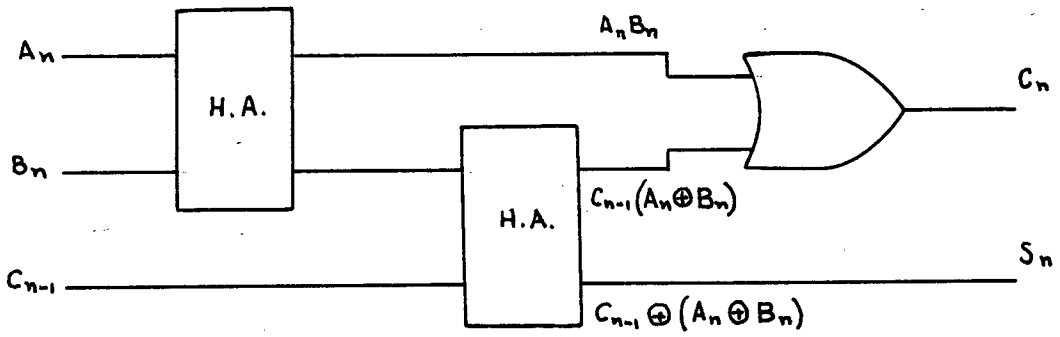
The following boolean expressions represent the values of the previous table. The verification of their equivalency can easily be accomplished by means of truth tables.

$$S_n = C_{n-1} \oplus (A_n \oplus B_n)$$

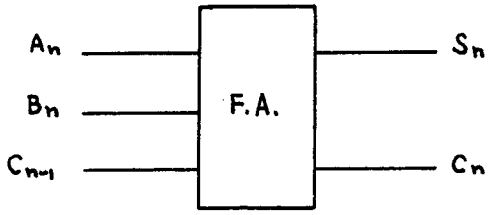
$$C_n = A_n B_n + C_{n-1} (A_n \oplus B_n)$$

As can be seen from above expressions, a full sum S_n, corresponding to any column n, consists of two half additions. To implement this operation, it is necessary to have two HALF-ADDERS, hence the name.

The full adder circuit is shown below.

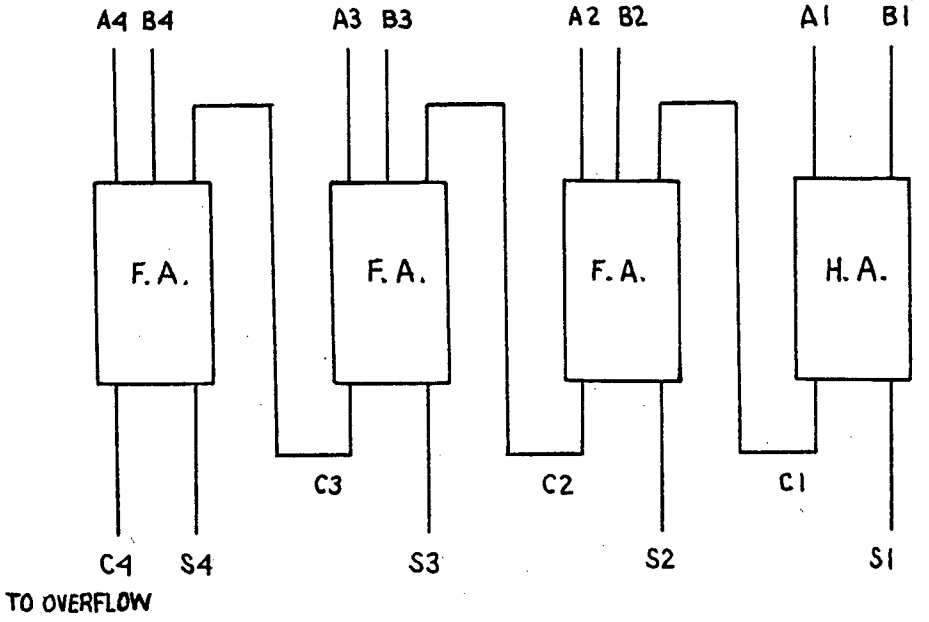


A Full Adder is represented by the following logical graphic symbol:



IMPLEMENTATION OF A FULL ADDER FOR FOUR BINARY DIGITS (BITS)

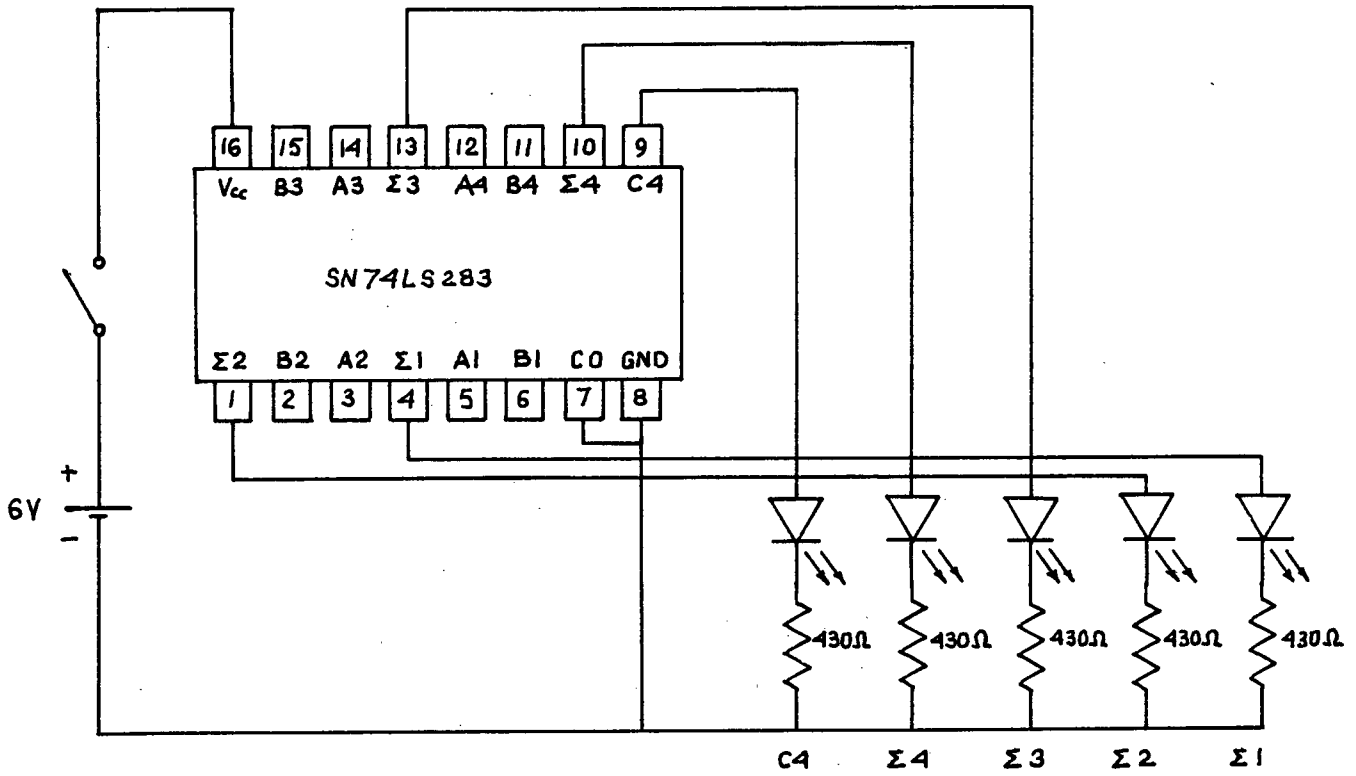
To add two vinary variables A and B with four bits each, the following logical circuit may be used. Addition made this way is known as Parallel Addition, because the quantities are all entered at the same time.



Integrated Circuits with all the required logic shown above are available. One of such IC's is the 74LS283PC. See the TTL Data Book, 2nd. Edition, published by Texas Instruments. The accompanying technical specifications were taken from this book and were used to assemble and test the circuit below.

Notice that in this circuit, C0 corresponds to a carry from another IC cascaded to this one. If it is not required, it must be connected to ground to prevent an extra digit in the displayed results. C4 may be connected to an Overflow Indicator as shown in the figure.

Notice that LED's are used to indicate the state of each output (Σ 1 to Σ4), as well as the state of the carry (C4).



In the diagram shown above, the connections for A_1, A_2, A_3, A_4, B_1, B_2, B_3 and B_4 have been left open. They represent the bits that make up the variables A and B. These connection inputs can be made to represent logic 1's or 0's, by connecting them to $+V_{cc}$ or to GND respectively.

The bit arrangement for quantities A and B is:

$$\begin{array}{cccc} A_4 & A_3 & A_2 & A_1 \\ + \; B_4 & B_3 & B_2 & B_1 \\ \hline \Sigma_4 & \Sigma_3 & \Sigma_2 & \Sigma_1 \end{array}$$

For example, to add A = 0101 and B = 0110, A_1 and A_3 go to V_{cc} and A_2 and A_4 go to GND, for B, B_2 and B_3 go to V_{cc} and B_1 and B_4 go to GND. The results have LED indicators.

3

SYNTHESIS OF BOOLEAN FUNCTIONS

Synthesis is the development of boolean expressions from a given truth table. It is the inverse process to that of analysis, since analysis was the process of testing the truth of a boolean expression by the use of truth tables.

Synthesis is carried out by inspecting the truth table and considering the statements that either make the function true or false.

EXAMPLE

Find the boolean expression that describes the following table:

	C	B	A	F
ROW 1	0	0	0	1
ROW 2	0	0	1	0
ROW 3	0	1	0	0
ROW 4	1	0	0	1

By inspection, one can see that the function F is true only in ROW 1 "OR" ROW 4, that is:

$$F = (\text{ROW } 1) + (\text{ROW } 4)$$

ROW 1 results when A = 0, B = 0 and C = 0, i. e. when $\overline{A}\,\overline{B}\,\overline{C}$

ROW 4 results when A = 0, B = 0 and C = 1, i. e. when $\overline{A}\,\overline{B}\,C$

Therefore:

$$F = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C$$

Simplifying:

$$F = \overline{A}\,\overline{B}\,(\overline{C} + C) = \overline{A}\,\overline{B}$$

Above expression describes the results of the previous table. This result is verified below:

C	B	A	$\overline{A}$	$\overline{B}$	$\overline{A}\,\overline{B} = F$
0	0	0	1	1	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	1

EXAMPLE

Given the table for the addition of binary numbers, find the boolean expression for S_n.

C_{n-1}	A_n	B_n	S_n
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

SOLUTION

$$S_n = \overline{A}_n B_n \overline{C}_{n-1} + A_n \overline{B}_n \overline{C}_{n-1} + \overline{A}_n \overline{B}_n C_{n-1} + A_n B_n C_{n-1}$$

Factoring:

$$S_n = \overline{C}_{n-1} (\overline{A}_n B_n + A_n \overline{B}_n) + C_{n-1} (\overline{A}_n \overline{B}_n + A_n B_n)$$

Using the definition of EOR: $A \oplus B = \overline{A}\, B + A\, \overline{B}$, plus the expression that corresponds to its inversion:

$$\overline{A \oplus B} = \overline{A}\ \overline{B} + A\ B$$

the above formula becomes:

$$S_n = \overline{C}_{n-1}\ (A_n \oplus B_n) + C_{n-1}\ (\overline{A_n \oplus B_n})$$

Using the definition for EOR again:

$$S_n = C_{n-1} \oplus (A_n \oplus B_n)$$

EXAMPLE

Find the boolean expression that describes the following table:

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

SOLUTION

$F = \overline{A}\ \overline{B} + \overline{A}\ B + A\ \overline{B}$

Simplifying:

$F = \overline{A}\ (B + \overline{B}) + A\ \overline{B} = \overline{A} + A\ \overline{B} = \overline{A} + \overline{B}$ ..... (a)

An alternate procedure can be worked out by considering the case when the function is not true, i. e., the function is not true only when A = 1 and B = 1 :

$\overline{F} = A\ B$

Therefore:

$F = \overline{A\ B}$ ..... (b)

Expressions (a) and (b) represent the same function, for they are one of DeMorgan's theorems.

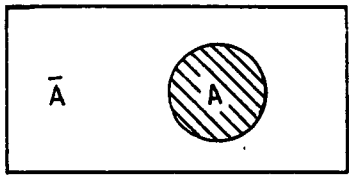
VENN DIAGRAMS

These diagrams are useful in describing the theory of sets. Their applications to boolean algebra provide us with graphical solutions. Such is the case with the graphical proof to DeMorgan's theorems.

Although their use is limited to very few binary variables, these diagrams lead directly to the use of Karnaugh Maps. These latter ones prove to be very useful in the simplification of boolean algebra expressions.

A simple Venn diagram is shown below. The rectangle represents all the possible conditions in a set, whether true or false, i. e., it represents the totality of "1".

The shaded area "A" represents all the true conditions of "A". Therefore, any point that does not belong to "A" will be outside of "A", where it is marked $\overline{A}$.

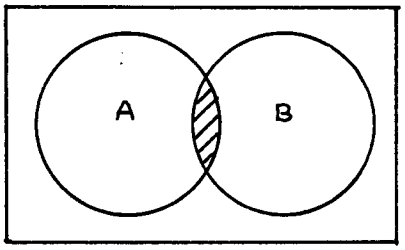


Using above diagram for boolean algebra, it represents one of the complementary laws:

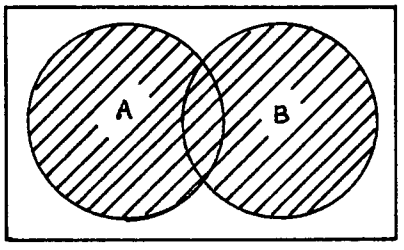
$$A + \overline{A} = 1$$

Where A is a binary variable.

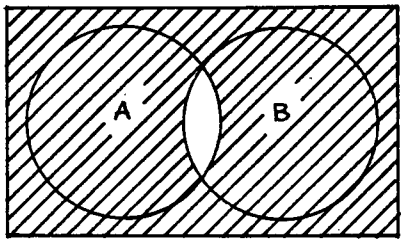
When two variables intersect each other, the intersection represents the logical operation AND. The Venn diagram for this operation, A B, is shown below.



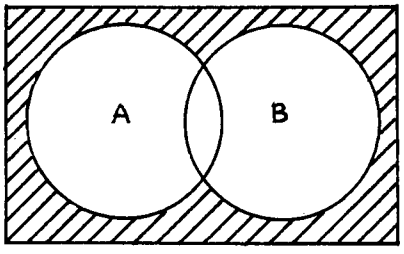
The combined area of A and B, A + B, is represented below.



Negations correspond to the area outside the intersecting or combined areas. For example $\overline{AB}$ is the area outside of the intersection AB.

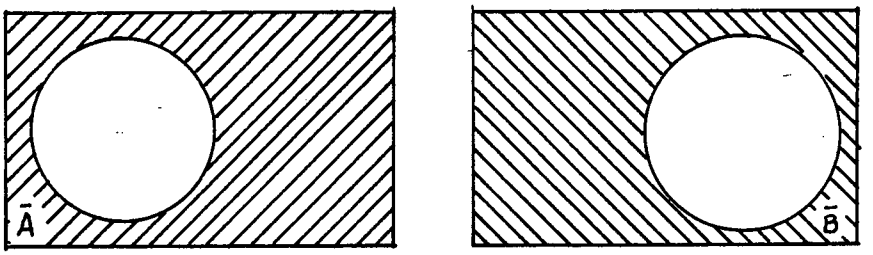


$\overline{A + B}$ is the area outside the combined area A + B.

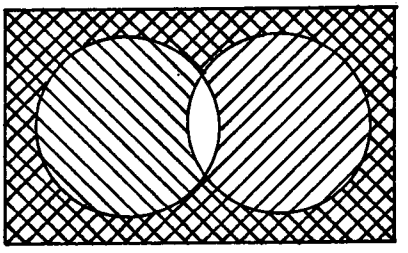


DeMORGAN'S THEOREMS:

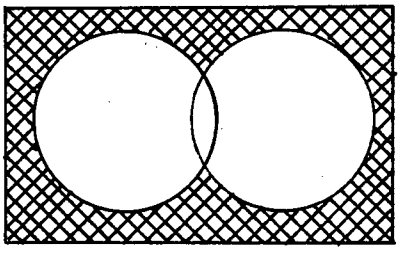
a) Consider $\overline{A}$ and $\overline{B}$ separately:



When their areas get combined, to obtain $\overline{A} + \overline{B}$, it should be noticed that the total hatched section is the same as the area corresponding to $\overline{AB}$, therefore: $\overline{AB} = \overline{A} + \overline{B}$

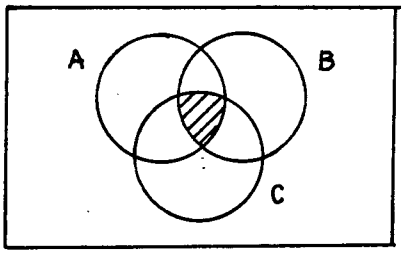


b) The intersection of $\overline{A}$ and $\overline{B}$, i. e. $\overline{A}\,\overline{B}$, is given by the cross-hatched area seen below.

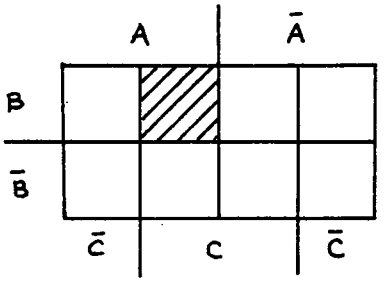


This area corresponds to $\overline{A + B}$, therefore: $\overline{A}\,\overline{B} = \overline{A + B}$

Venn diagrams get complicated as we run into more variables, e. g. the intersection of three variables A B C is represented by the shaded area:



If instead of circles we use rectangles to represent the variables A, B and C, we obtain the following figure, where the shaded area represents the intersection A B C.



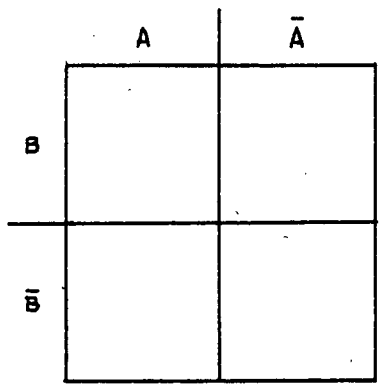
Above matrix arrangement is known as a Karnaugh Map. Karnaugh maps prove very useful in simplifying Boolean Algebra expressions.

KARNAUGH MAPS

Karnaugh Maps constitute a very useful means of simplifying Boolean Algebra expressions. Although their use is limited to a maximum of six variables, they are well suited for most practical applications.

TWO VARIABLE KARNAUGH MAP

Consider the following figure. It represents a two variable Karnaugh Map, where the variables are A and B.



In the above map, each variable or its negation defines two squares. i. e.

Variable A defines the upper left and lower left squares.

Variable $\bar{A}$ defines the upper right and lower right squares.

Variable B defines the upper left and upper right squares.

Variable $\bar{B}$ defines the lower left and lower right squares.

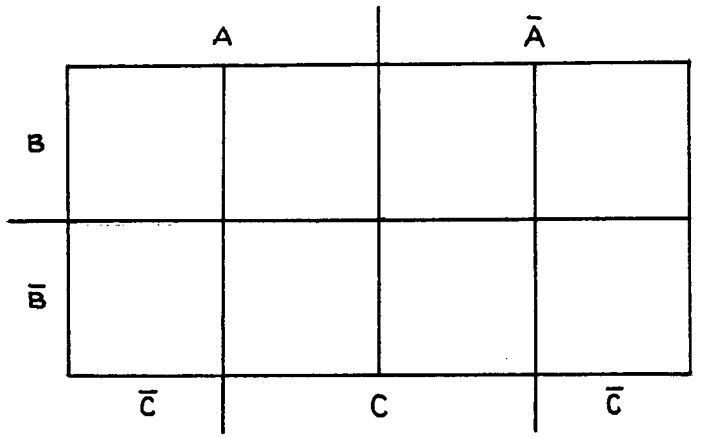
From the above area definitions, it can be seen that any combination of variables will intersect and identify a single square.

Examples:

The product A B defines the upper left square.

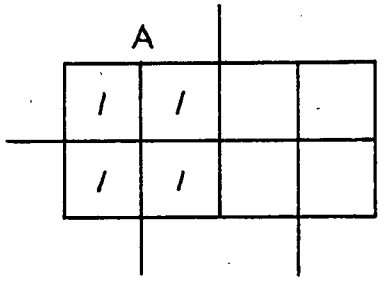
The product $\bar{A}$ B defines the upper right square.

The following Karnaugh Map may be used to describe the variables A, B and C.

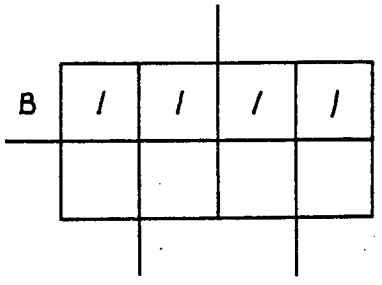


In the above map, each variable defines four squares. Consider the following examples:

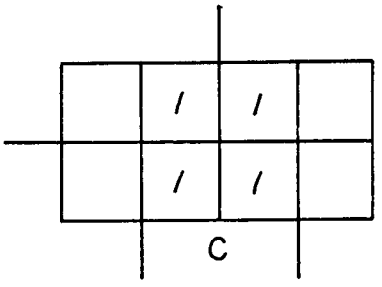
Variable A defines the four squares to the left of a vertical center line.



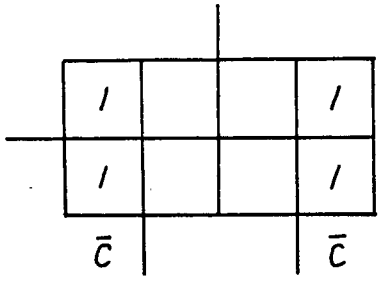
Variable B defines the four squares in the upper horizontal row.



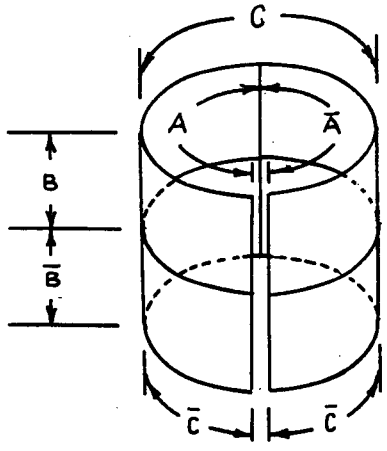
Variable C defines the two center squares of the top row and the two center squares of the bottom row.



Variable $\overline{C}$ defines the two squares in the left hand vertical column plus the two squares in the right hand vertical column.

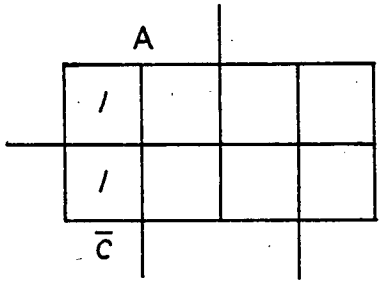


NOTE.- The region defined by the variable $\overline{C}$ may appear at first as consisting of two separate regions. However, if we consider wrapping the map around a vertical cylinder, as shown below, then the left hand vertical column comes into contact with the right hand vertical column, and the apparent two separate regions merge into a single one.

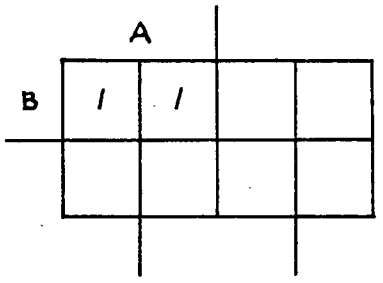


The intersection of two variables defines a region made up of two squares. Consider the following examples:

The product A $\overline{C}$ defines the two squares in the left hand vertical column.

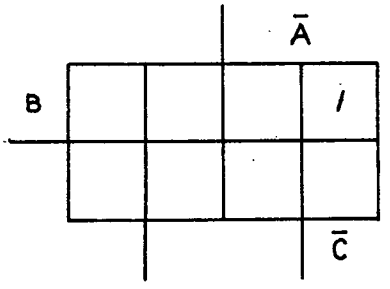


The product A B defines the left two squares in the upper horizontal row.



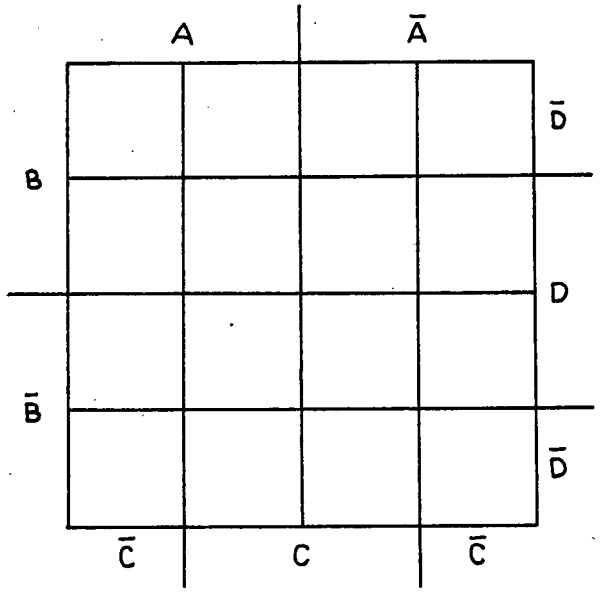
The intersection of three variables defines a region made up of a single square. Consider the following example:

The product $\overline{A}$ B $\overline{C}$ defines the upper right square.



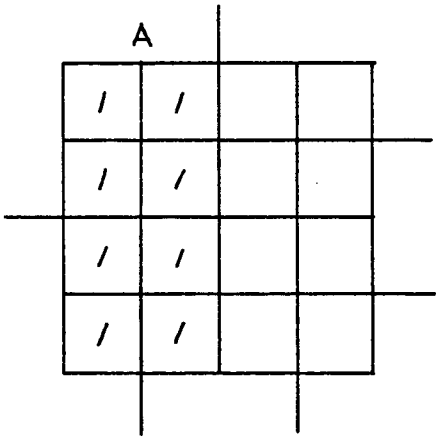
FOUR VARIABLE KARNAUGH MAP

The following Karnaugh Map may be used to describe the variables A, B, C, and D.

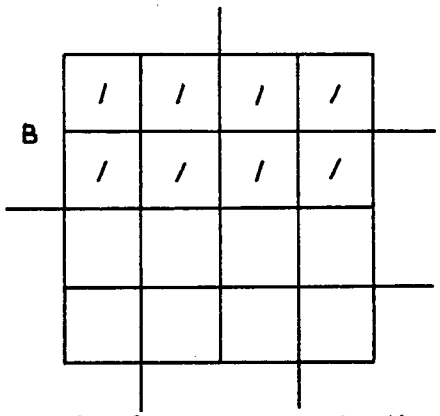


In the above map, each variable defines eight squares. Consider the following examples:

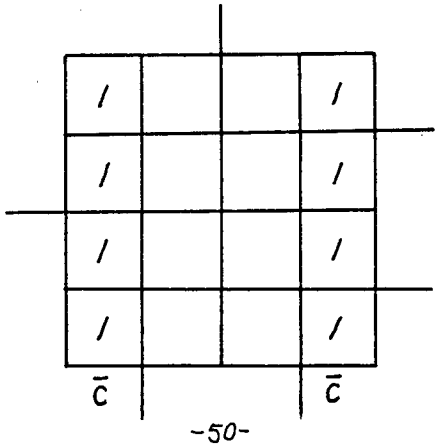
Variable A defines the eight squares to the left of a vertical center line.



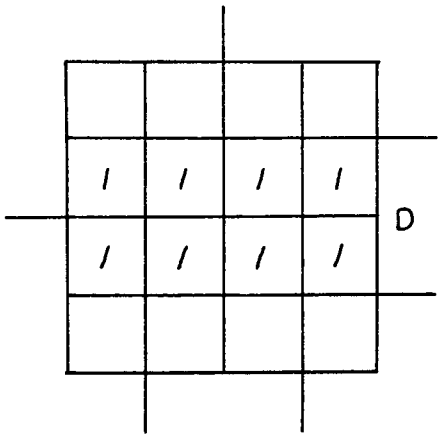
Variable B defines the four squares of the upper row plus the four squares of the second row from the top.



Variable $\overline{C}$ defines the four squares in the left hand vertical column plus the four squares in the right hand vertical column. These eight squares constitute a single continuous region, as discussed under the note for the Three Variable Karnaugh Map.

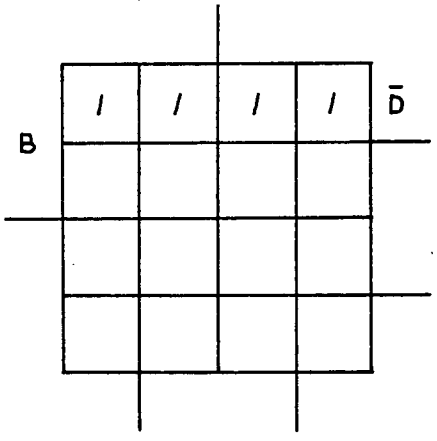


Variable D defines the eight squares in the horizontal second and third rows.

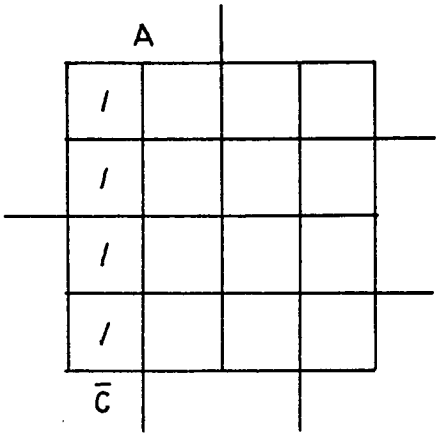


The intersection of two variables defines a region made up of four squares. Consider the following examples:

The product B $\overline{D}$ defines the four squares in the upper horizontal row.

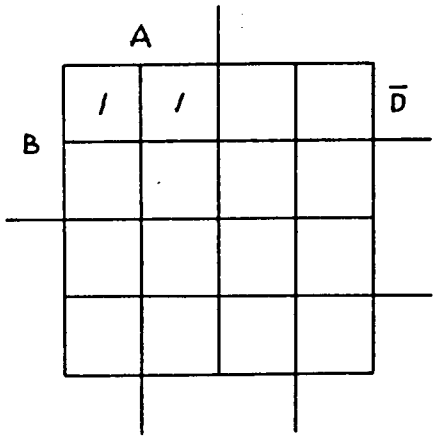


The product A $\overline{C}$ defines the four squares in the left hand vertical column.



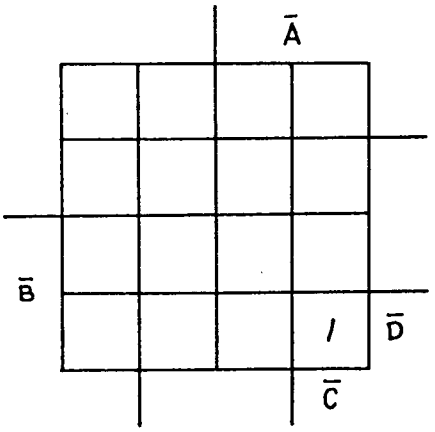
The intersection of three variables defines a region made up of two squares. Consider the following example:

The product A B $\overline{D}$ defines the left two squares in the upper horizontal row.



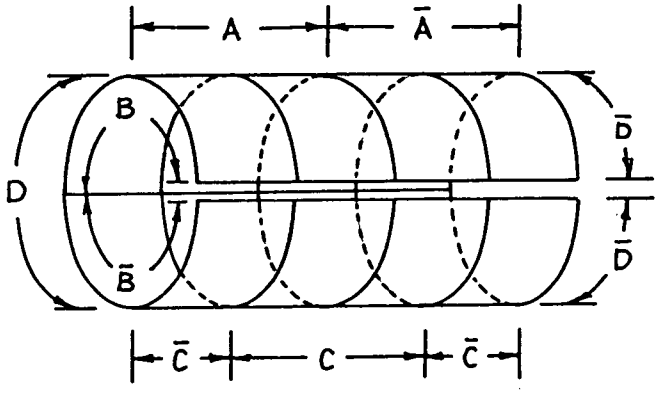
Finally, the region where the product of four variables intersect is a single square. Consider the following example.

The product $\overline{A}$ $\overline{B}$ $\overline{C}$ $\overline{D}$ defines the right square in the lower horizontal row.



NOTE.- The region defined by the variable $\overline{D}$, is similar to that defined by $\overline{C}$. Just like region $\overline{C}$, the region $\overline{D}$ also appears as consisting of two separate regions.

However, wrapping the Karnaugh Map on a horizontal cylinder, as shown below, until the top upper row comes into contact with the bottom row, causes the two apparent separate regions to merge into a single one.



SIMPLIFICATION OF BOOLEAN EXPRESSIONS USING THE KARNAUGH MAP

The basic steps required to simplify a given boolean expression are the following:

1.- The number of variables in the boolean expression determines the size of the Karnaugh Map.

2.- Draw the Karnaugh Map.

3.- Each term in the Boolean Expression defines a region in the Karnaugh Map. Mark the square or squares defined by each term of the expression with X's or 1's. Each square needs to be marked only once. When different terms in the boolean expression also call for the same square or squares, the simplification of

the original expression becomes apparent, since there is no need to define any region more than once.

4.- Once all the terms of the boolean expression have been marked on the Karnaugh Map, redefine the regions marked with X's or 1's. The largest the region, the fewer the number of variables needed to define them, this results in a boolean expression that is simpler than the original one.

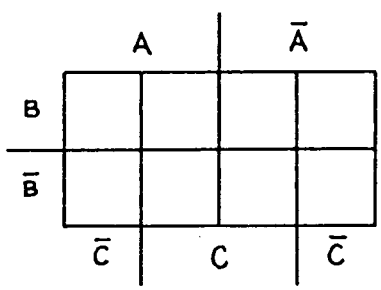
NOTE.- For the cases when this method yields two different simplified expressions, each with the same minimum number of variables, (even though the variables are not the same), then both expressions are considered correct and either can be chosen.

EXAMPLE 1.- Simplify the following expression:

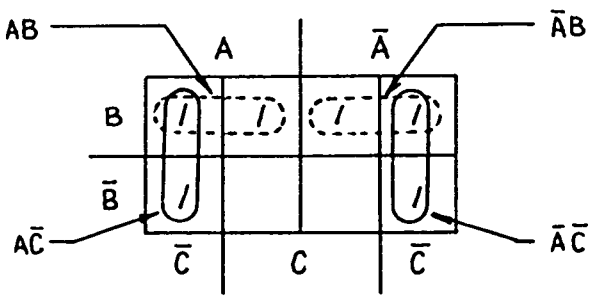
$$f = A\,\overline{C} + A\,B + \overline{A}\,B + \overline{A}\,\overline{C}$$

Solution: 1.- There are three variables:A, B and C.

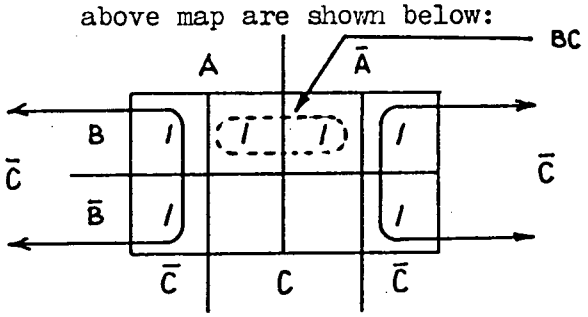
2.- The corresponding Karnaugh Map is:



3.- Each term of the above expression defines the regions shown below:



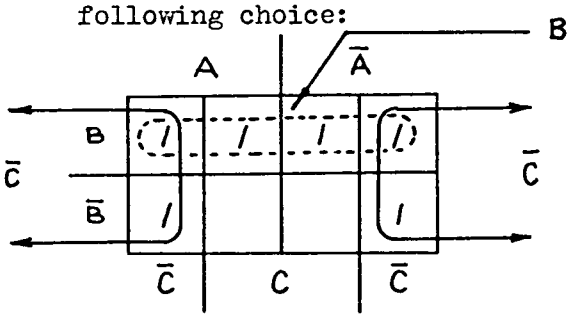
4.- The largest regions that can be redefined on the above map are shown below:



Therefore the simplified expression is:

$$f = B\,C + \bar{C}$$

However, equally as accurate, but even better, since it covers larger regions with less variables, is the following choice:



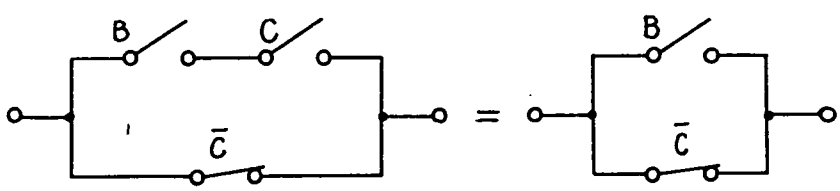
The resulting simplified expression becomes:

$$f = B + \bar{C}$$

Above two solutions prove one of the absorption laws previously described:

$$B\,C + \bar{C} = B + \bar{C}$$

How the absorption takes place can be seen clearly when the functions are implemented with switches:

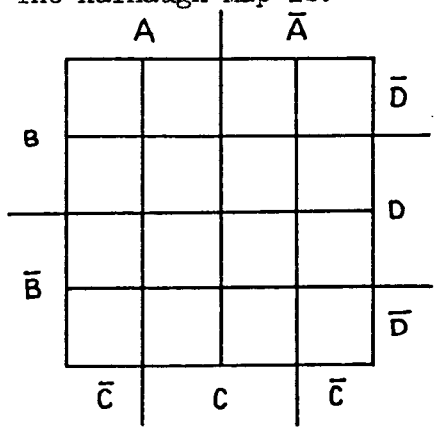


EXAMPLE 2.- Simplify the following expression:

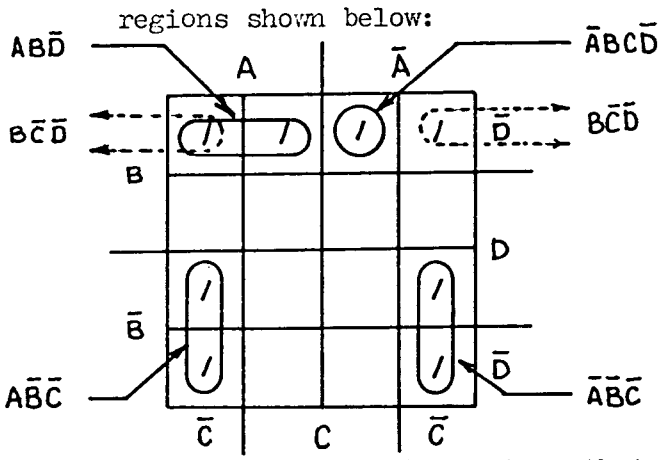
$$f = A\,B\,\bar{D} + A\,\bar{B}\,\bar{C} + B\,\bar{C}\,\bar{D} + \bar{A}\,\bar{B}\,\bar{C} + \bar{A}\,B\,C\,\bar{D}$$

Solution: 1.- There are four variables: A, B, C and D

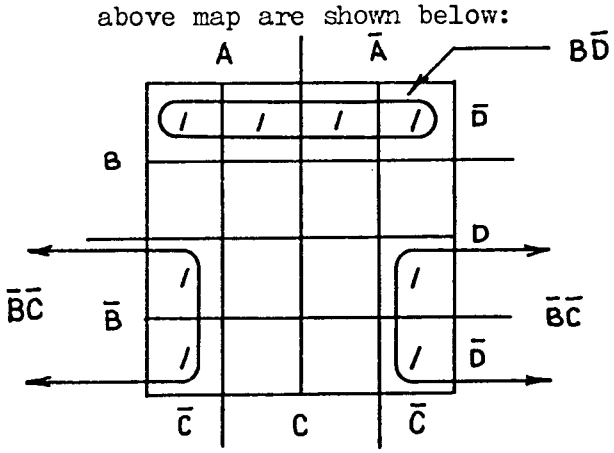
2.- The Karnaugh Map is:



3.- Each term in the above expression defines the regions shown below:



4.- The largest possible regions that can be defined from above map are shown below:



Therefore, the simplified expression becomes:

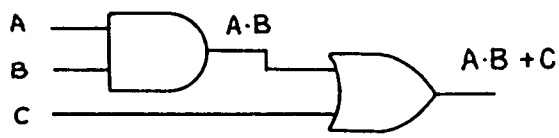
$$f = B\,\bar{D} + \bar{B}\,\bar{C}$$

SEQUENTIAL CIRCUITS

4

Up to here, all the circuits described belong to the Combinational Classification, where time is not important, and the system responds to input conditions whenever they happen.

For example, for the function $F = A \cdot B + C$, its logical configuration is the following.



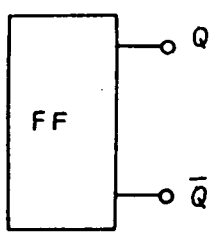
In the circuit given above, the function F occurs whenever A, B and C are present. No provision is made for their sequence of appearance.

On the other hand, sequential circuits must respond to a chain of events, consequently, these circuits must keep track or have "memory" of all the changes taking place with respect to time.

Sequential circuits require memory and master oscillators or clocks, in order to keep track of the given sequence of pulses. In above example, C may be preceded only by B and B preceded by A for function F to occur.

BASIC MEMORY UNIT

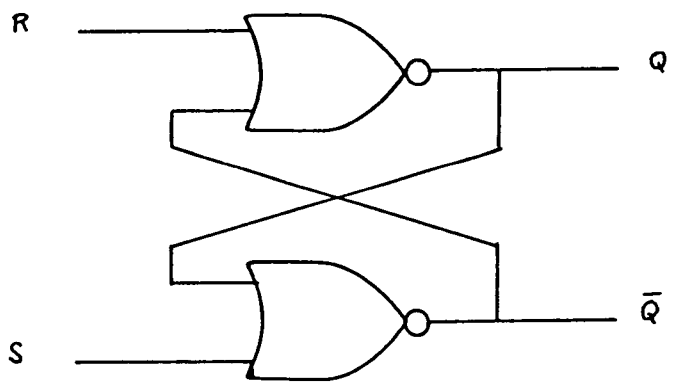
The FLIP FLOP (FF) is a sequential device that stores a binary digit or "bit". It is represented by a box, and has two outputs called Q and $\overline{Q}$.



If Q is a "1" or HI, the flip flop is said to be SET. If it is a "0" or LO, the flip flop is said to be RESET.

RS FF USING NOR GATES

This flip-flop has two inputs called S for Set and R for Reset. Feedback lines are used to implement it, see figure below:



The circuit rests in eitherof two states, thus storing one bit.

OPERATION:

a) If S = 1 and R = 0, the HI input to the lower gate makes $\overline{Q}$ = 0. $\overline{Q}$ then feeds back its LO into the input of the upper gate. The input to the upper gate has now two LO's that make Q = 1 (HI). Q then feeds its HI into the input of the lower gate, which now has two HI's. In this way, the flip-flop is locked into the SET condition, even after the initial inputs are gone.

b) If S = 0 and R = 1, the flip-flop locks in the RESET condition (i. e. Q = 0).

c) If S = 0 and R = 0, as is the case when no signal is being applied, the flip-flop remains unchanged.

d) If S = 1 and R = 1, both Q and $\overline{Q}$ become "0" (LO), giving rise to an indeterminate state. The last input to return to LO, determines the final state of the flip-flop.

Above indeterminate state is analogous to a coin being held vertically by two persons. Each individual pushes their respective side to win, but the one that wins is the one that holds his coin side the longest.

The operation of this flip-flop can be summarized in the following table:

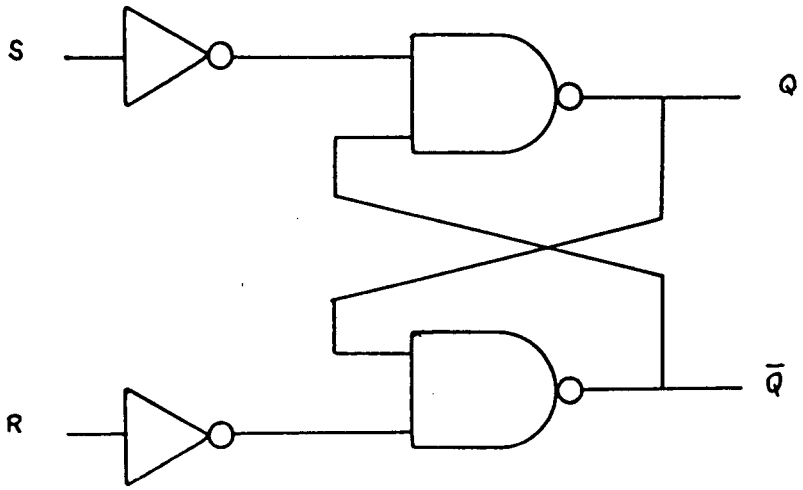
S	R	Q_n	Q_{n+1}
1	0	Q_n	1
0	1	Q_n	0
0	0	Q_n	Q_n
1	1	Q_n	INDETERMINATE ($Q = 0$; $\overline{Q} = 0$)

Q_n is the state of the flip-flop, either a "1" or a "0" before applying S and R.

Q_{n+1} is the state of the flip-flop that results from inputs S and R.

RS FF USING NAND GATES

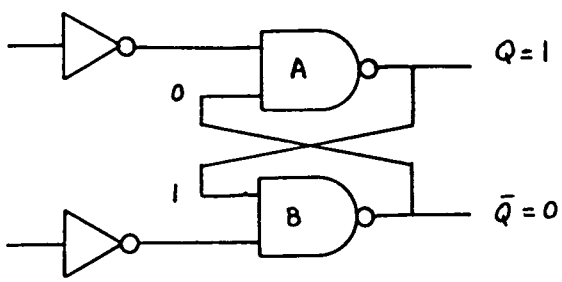
These flip-flops are implemented with two NAND GATES. Notice that in the circuit below, inverters have been added to the S and R inputs so that the operation and resulting table become similar to the ones described for the NOR GATE FF.



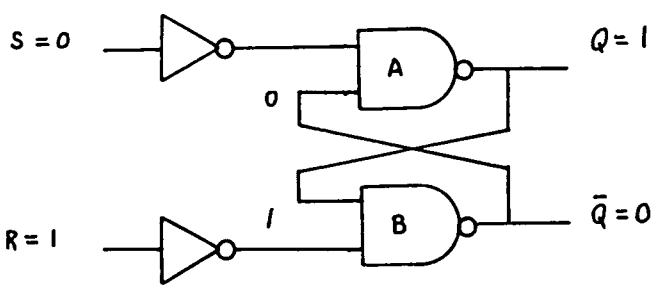
OPERATION:

a) Assume a given output as initial condition (e.g. Q = 1, $\bar{Q}$ = 0).

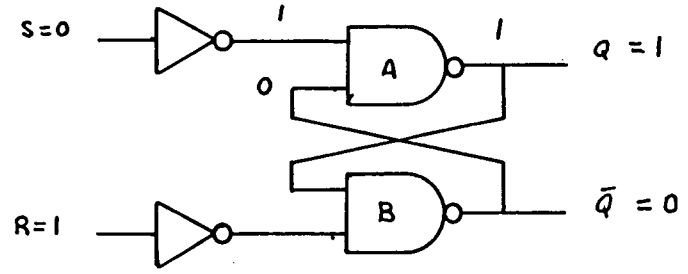
b) Mark the corresponding conditions on the feedback lines.



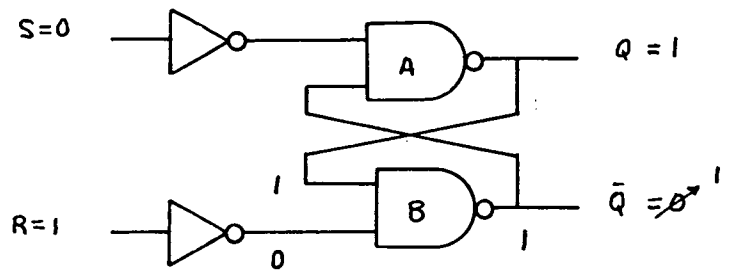
c) Add any desired combination of input signals (e. g. S = 0, R = 1).



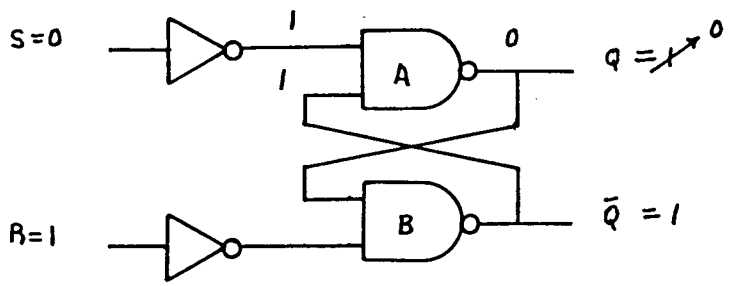
d) Analyze the response of the gates, one gate at a time. For instance, starting from gate "A", its inputs will be: a "1" from an inverted S = 0, and a "0" from the feedback of $\overline{Q}$. Its output will be "1" ($\overline{0 \cdot 1}$) and as a result, Q remains a "1".



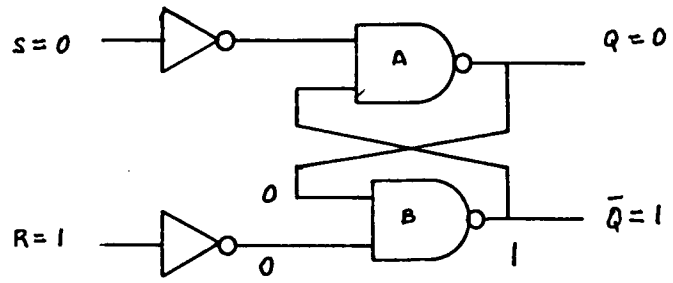
e) Now, we analyze the response of gate "B". Its inputs are a "1" from the feedback of Q (as seen in (d), it remained a "1"), and a "0" from the inverted R = 1, therefore its output will become a "1" ($\overline{1 \cdot 0}$).



f) See if above step changes the feedback conditions. In our example it does, inputs to "A" become: a "1" from the inverted S = 0 and a "1" from the new feedback from $\overline{Q}$. Then, the output from "A" will change from a "1" to a "0"



g) Through feedback lines, above new condition in the output from gate "A" will modify the input to gate "B". Gate "B" will have two zeroes for inputs, one from the inverted R and another from the feedback from Q. These inputs will keep the output of gate "B" as a "1" ($\overline{0\ \ 0}$).



f) Thus, the input condition S = 0 and R = 1 will cause the flip-flop to settle at Q = 0 and $\overline{Q}$ = 1, which conforms to the results of the previous truth table.

TIMING IN SYSTEMS

Many devices require synchronous operation, some examples are given below:

a) Television Systems, where the horizontal and vertical deflection of the television set must be synchronized to those deflections of the television camera.

b) Record players must run at 33⅓rpm to play 33⅓rpm records.

c) Digital computers, where a master oscillator or clock gates the propagation of signals from stage to stage with a sequence of timing pulses.

d) Digital instruments such as frequency counters, tachometers, digital voltmeters, etc.

A synchronous analogy may be drawn by a train of stretched freight cars. When the locomotive moves from a still position, all the cars move at the same time.

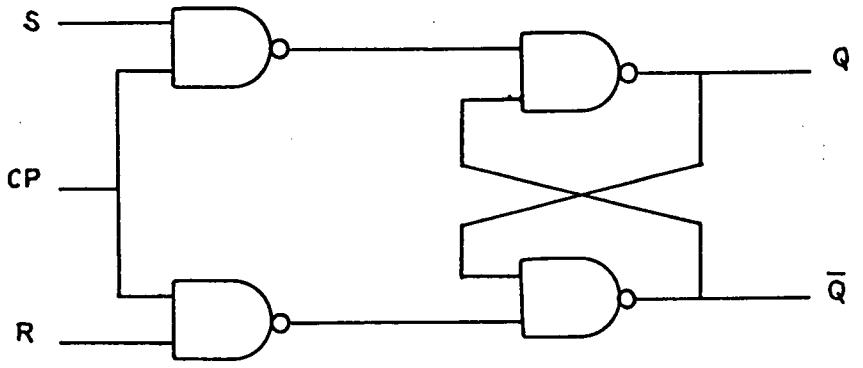
The asynchronous example is that of cars waiting at an intersection. When the light turns green, the second car does not move until the first does, and the third car does not move until the second car is in motion, etc.

Another synchronous analogy is that of a group of soldiers waiting for the order to march. When the order arrives, all the soldiers move at the same time, i. e. the first soldier as well as the last one in the formation.

The asynchronous counterpart is that of a queue of people waiting outside a theater. When the gates are opened, only the first person in the queue can move, then the second and so on. As a result, a considerable amount of time elapses from the opening of the gates before the last person in the queue can begin to move.

CLOCKED RS FF

If an RS FF is to be used in a synchronous manner, it must be able to accept a synchronizing "clock pulse". This is easily achieved as shown below:



The absence of a clock pulse (CP) INHIBITS the input gates from accepting incoming signals S and R.

When a CP is present, it ENABLES the input gates, and signals S and R can be fed through into the flip-flop.

The truth table for above flip-flop is:

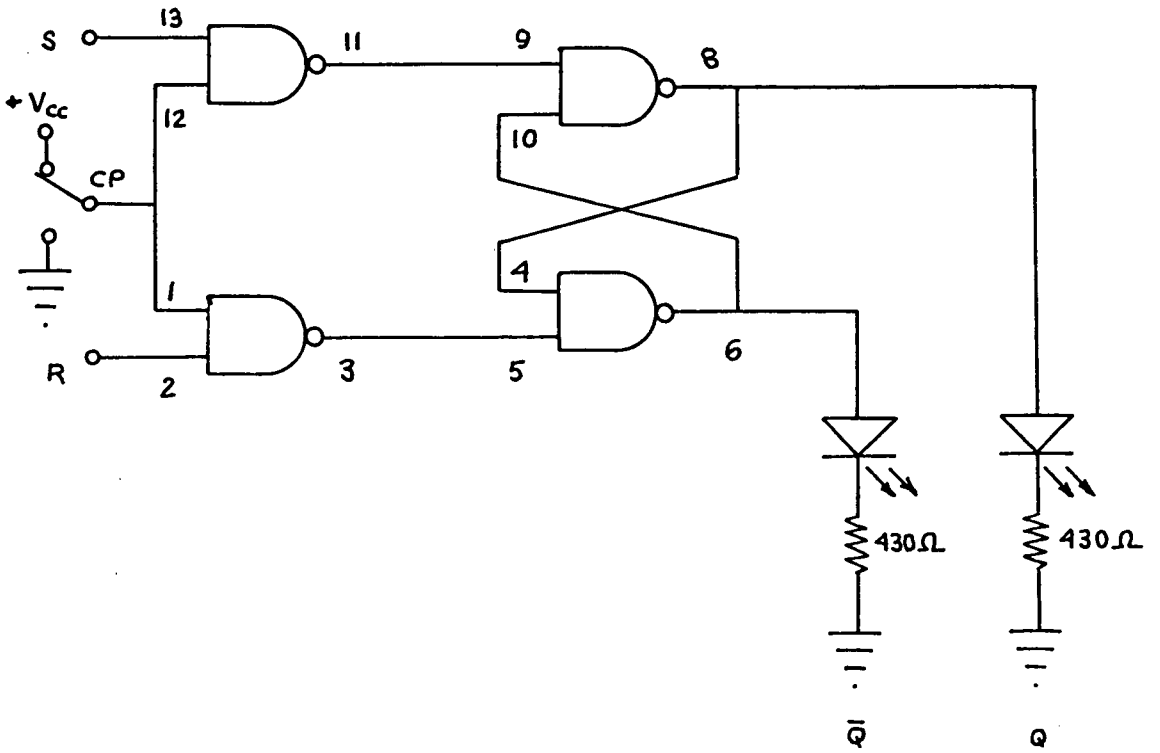
S	R	Q_n	Q_{n+1}
0	0	Q_n	Q_n
0	1	Q_n	0
1	0	Q_n	1
1	1	Q_n	*

* The state of the flip-flop is indeterminate and $Q = \overline{Q} = 1$

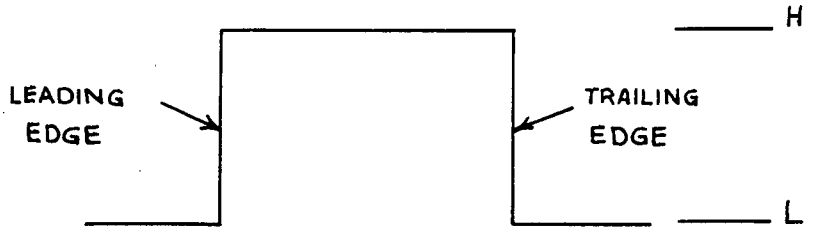
Note.- Outputs Q and $\overline{Q}$ are zero if the CP is zero.

In above table, Q_n refers to the initial condition before the clock pulse, and Q_{n+1} refers to the output result after the clock pulse.

Assemble the following circuit and test the truth tables given above. In the following circuit a 7400 integrated circuit is used. The pin connections are suggested but other pins may be used.



Above clocked RS flip flop changes state on the leading edge of the clock pulse.



CLOCK PULSE

Clock pulses may last for a relatively long period of time. During this time, the input gates of the flip flops remain enabled and may accept unwanted information from feedback paths.

The condition of unwanted feedback loops during the time the gates are enabled is known as RACE-AROUND. During race-around, the flip flops are unstable and means must be provided to eliminate this condition.

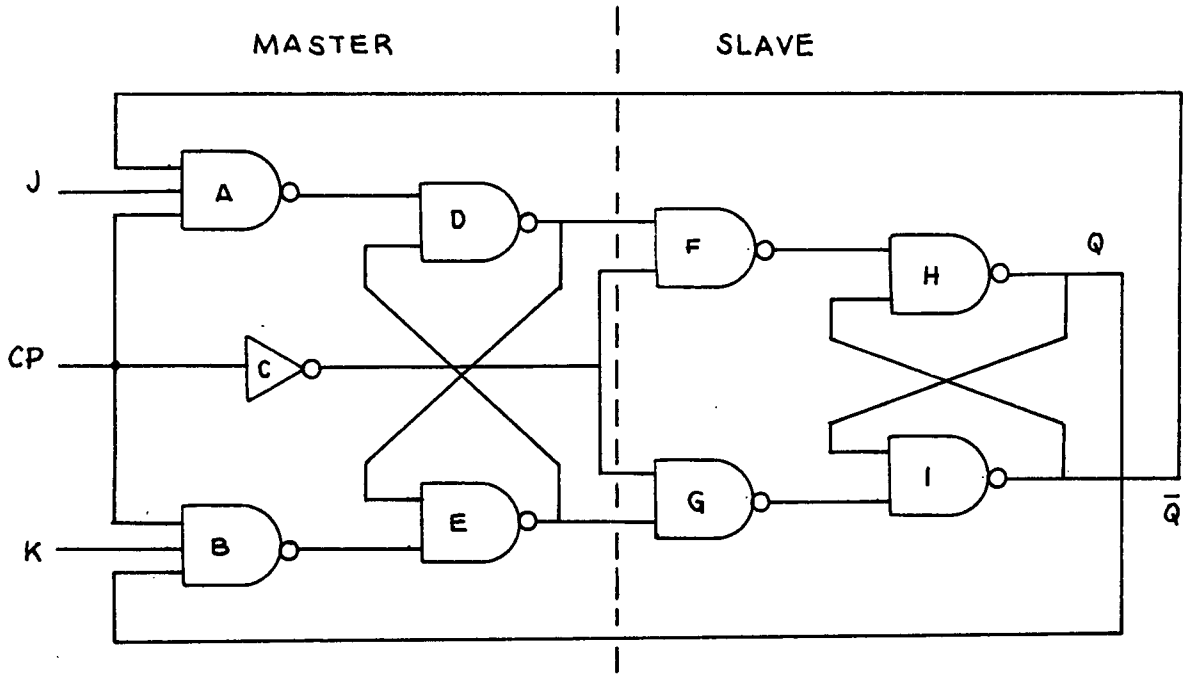
JK MASTER SLAVE FLIP FLOP

If the flip flop is designed to change state after the clock pulse has disappeared, race-around will be eliminated.

The MASTER SLAVE system is the most common solution adopted by manufacturers of integrated circuits.

In the master slave system, two flip flops are connected in tandem. The flip flop that receives the incoming signal is called the MASTER. The master has two inputs called J and K. Inputs J and K update the information stored in the master flip flop.

Updating of information takes place when gates A and B are enabled, see the figure below:



The gates A and B are enabled by:

a) the leading edge of a clock pulse plus

b) a feedback line from the slave portion, used to prevent indeterminate states when J and K are both HI, as explained further below.

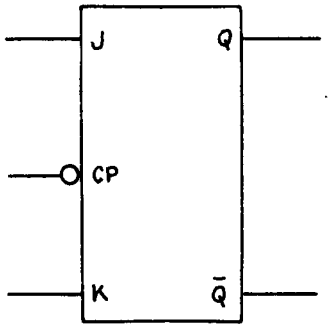
While the clock pulse is on, the inverter "C" inhibits the slave flip flop from changing state.

Once the information has been fully updated, the contents of the master get transferred into the slave flip flop. This transfer of data from master to slave takes place only during the trailing edge of the clock pulse.

During the trailing edge, the HI to LO transition of the clock pulse gets inverted by "C", thus enabling gates F and G in the slave section.

In this way, the slave flip flop now accepts the contents from the master flip flop. Notice that during this transfer, the master flip flop can not accept any other input, since its gates A and B are inhibited by a low clock pulse.

The logic symbol for a JK master slave flip flop (JK M/S FF) is:



The bubble on the clock input indicates that the flip flop changes state on the trailing end of the clock pulse, that is, during the HI to LO transition.

The truth table for this circuit is:

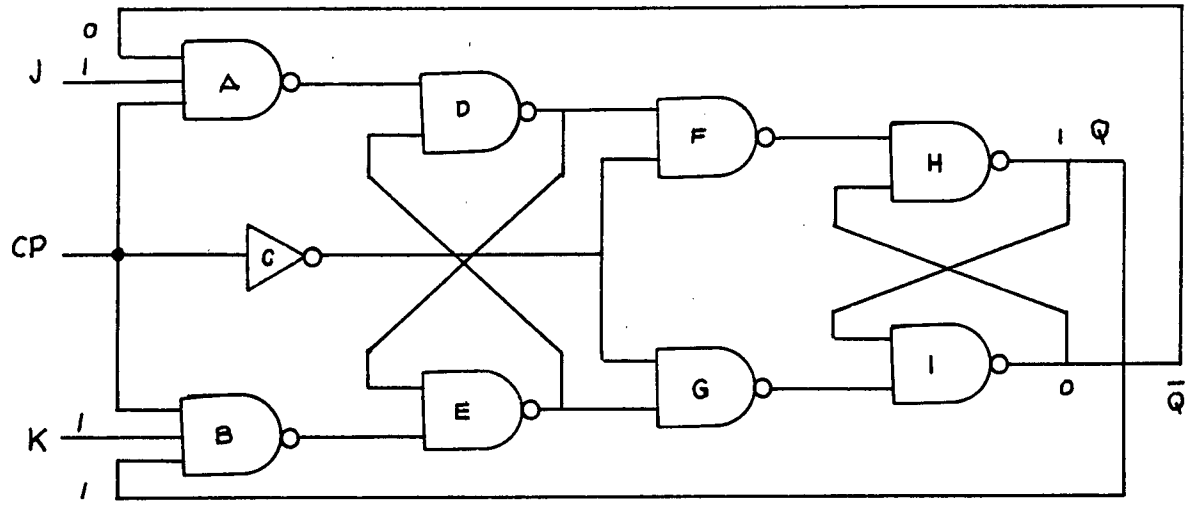
J	K	Q_n	Q_{n+1}
0	0	Q_n	Q_n
0	1	Q_n	0
1	0	Q_n	1
1	1	Q_n	$\overline{Q}_n$

When J = 1 and K = 1, the above table indicates that the state of the flip flop will be reversed, i. e. toggled after a clock pulse. This result is in contrast with that of previous flip flops, where the above condition resulted in an indeterminate state.

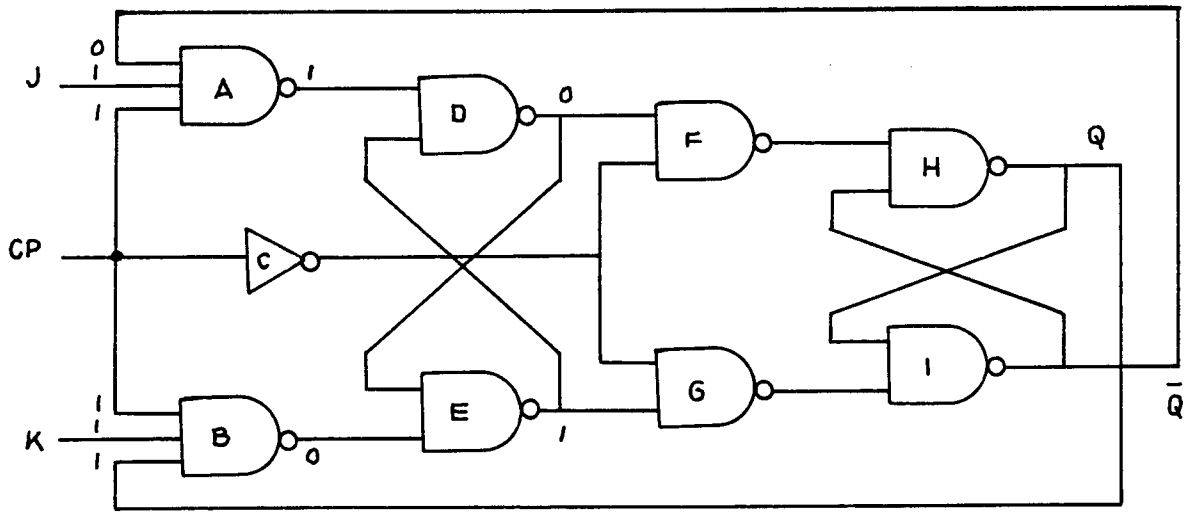
Above toggling action will be described below:

a) Assume a given output condition, e. g. $Q = 1$; $\overline{Q} = 0$

b) Draw J = K = 1 on the logic diagram:



c) Consider the first part of the clock pulse. After the leading edge of the clock pulse, ⌐ , the inputs to the master section become those shown below:



The output from gate A is a 1 $(\overline{0 \cdot 1 \cdot 1})$

The output from gate B is a 0 $(\overline{1 \cdot 1 \cdot 1})$

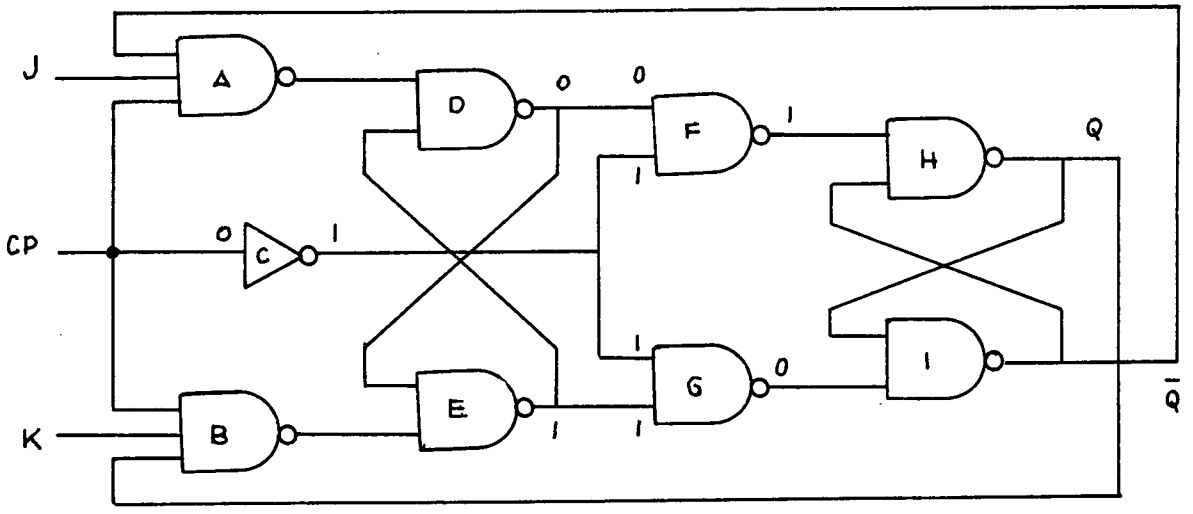
Therefore, the output state of the master flip flop becomes:

Output from gate D = 0

Output from gate E = 1

Above is not an indeterminate state, as seen in previous flip flops. This is due to the feedback lines from the slave flip flop.

d) After the HI to LO transition of the clock pulse, ⌐, the inverter C causes a LO to HI which enables the slave input gates F and G. Thus, the slave flip flop accepts the transfer of information from the master flip flop.



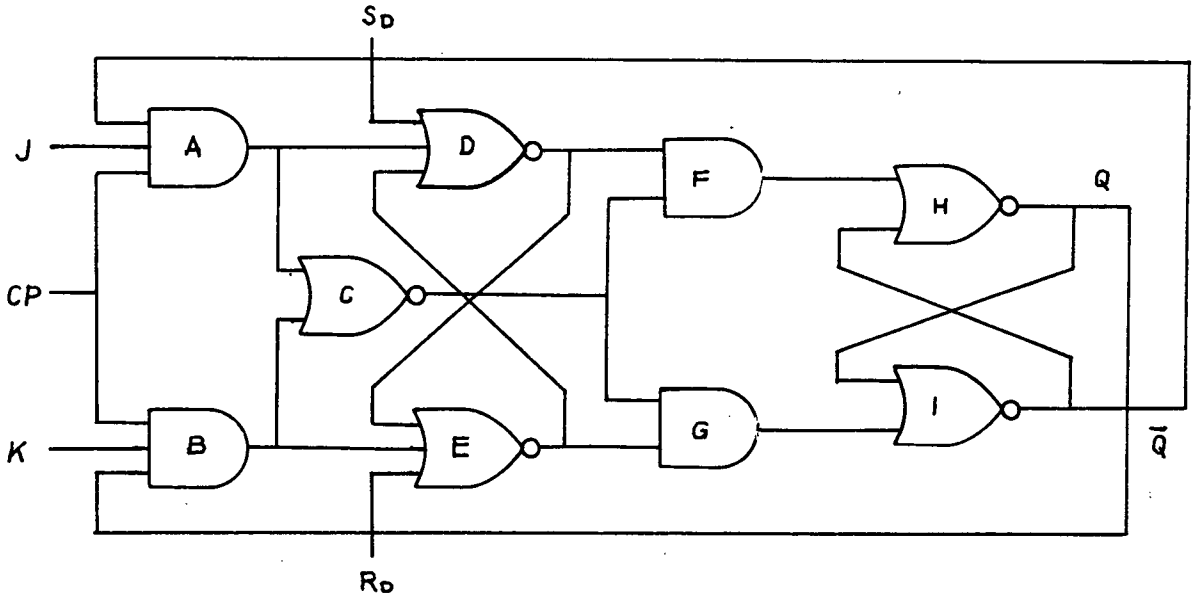
As seen above, the output from gate F becomes a "1" ($\overline{0 \cdot 1}$), and the output from gate G becomes a "0" ($\overline{1 \cdot 1}$).

Therefore Q becomes a "0" where previously it was a "1", and $\overline{Q}$ becomes a "1" where previously it was a "0".

Thus, the master slave flip flop reverses states every time a clock pulse arrives if and only if J = K = 1.

This toggle switch action is used extensively in Counter Circuits and Shift Registers.

The following JK master slave flip flop has two extra inputs called PRESET and PRERESET, labelled S_D and R_D respectively.



Inputs S_D and R_D allow one to preset or prereset the flip flop when the clock pulse is low. This is so, because a low clock pulse causes a HI out of gate C, thus enabling the input gates F and G to accept pulses S_D or R_D. By the use of the preset and prereset inputs, when the clock pulse is LO, one can cause the circuit to act as a simple RSFF.

Above mode of operation is very useful, in particular with counters or shift registers, where an initial condition is often desired prior to its operation.

Above circuit also allows one to preset and prereset the flip flop even when the clock pulse is a HI. This can be accomplished as follows:

a) When the clock pulse is HI, the only way to preset the flip flop is with $S_D = 1$ and $J = 0$

b) When the clock pulse is HI, the only way to prereset the flip flop is with $R_D = 1$ and $K = 0$.

NOTE.- Conditions (a) and (b) are applicable only to the circuit shown above. In most JK master slave flip flops, the preset and the prereset inputs are independent of the clock pulse.

Finally, by tying the J and K inputs together in above circuit, the flip flop will function as a toggle switch, changing output conditions with every clock pulse, a highly desirable characteristic.

JK master slave flip flops are available in dual packages, such as the 7476 and the 74107. Notice that the 74107 has only a prereset input R_D, whereas the 7476 comes with preset S_D as well as prereset R_D inputs. The technical specifications for these flip flops are included.

To get familiar with the JK master slave flip flop, it is recommended to test the information supplied by the manufacturers. This can be accomplished by using a manual pulser as a clock pulse on either the 7476 or the 74107. Then, the conditions listed on the respective truth tables should be verified, applying the respective voltage levels to inputs J and K and also testing inputs S_D and R_D. LED indicators may be connected at the Q and $\overline{Q}$ outputs.

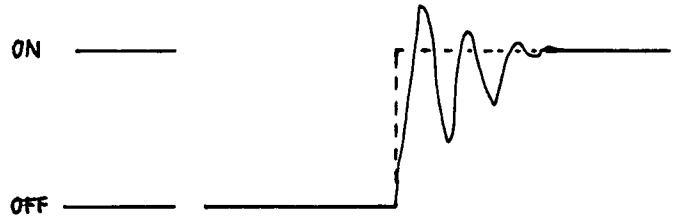
5

CLOCKS

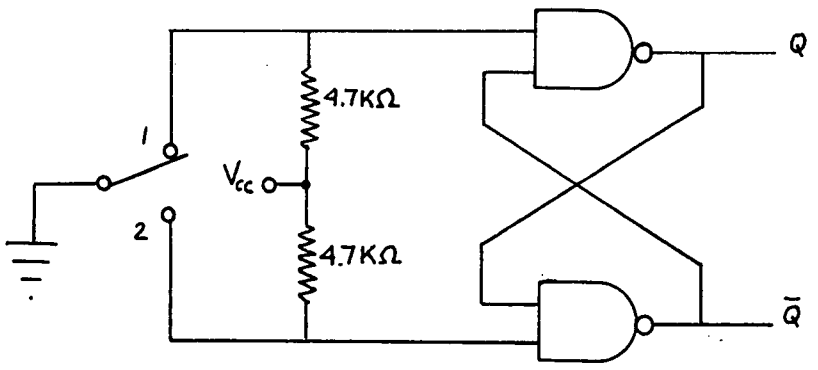
In order to generate clock pulses, any of the following circuits may be used.

a) MANUAL PULSER

A manually produced signal is very useful to test circuits and verify truth tables, especially if one wants to do it at one's own speed, rather than at the speed of a fast electronic switching device. However, the use of ordinary switches, by themselves, is not satisfactory, since ordinary switches produce spikes when closed or opened due to the mechanical bouncing of their contacts, as well as electrostatic sparks between contacts when they are in close proximity.



Above spikes cause misreadings or noise in subsequent circuits, and thus they must be removed. A simple method to remove spikes is by the use of the following manual pulser. In fact, this pulser may replace any manually operated switch in a logical system.



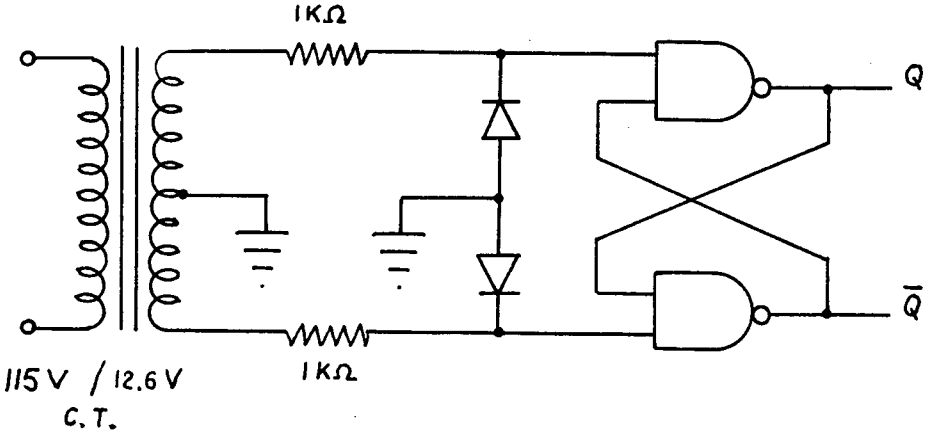
MANUAL PULSER WITH CONTACT BOUNCE ELIMINATION

OPERATION

When the switch moves into position 1, it applies a LO to the input of the upper gate and a HI to the input of the lower gate. Therefore, the Q output locks into a HI, regardless of subsequent momentary spikes.

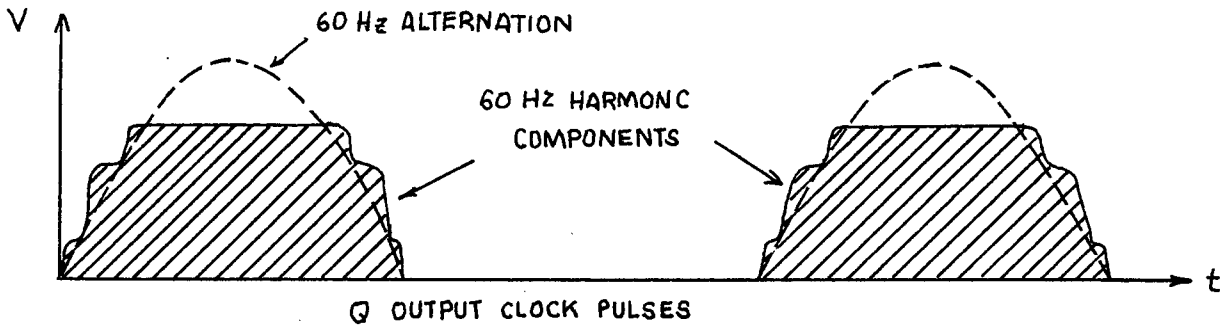
b) 60 HERTZ CLOCK

This clock makes use of the line frequency.



However, the resulting clock pulses have a 60 Hz harmonic component on their leading and trailing edges, as shown in the following figure, where the rise time and the fall time are very slow. Notice that rise time t_r is

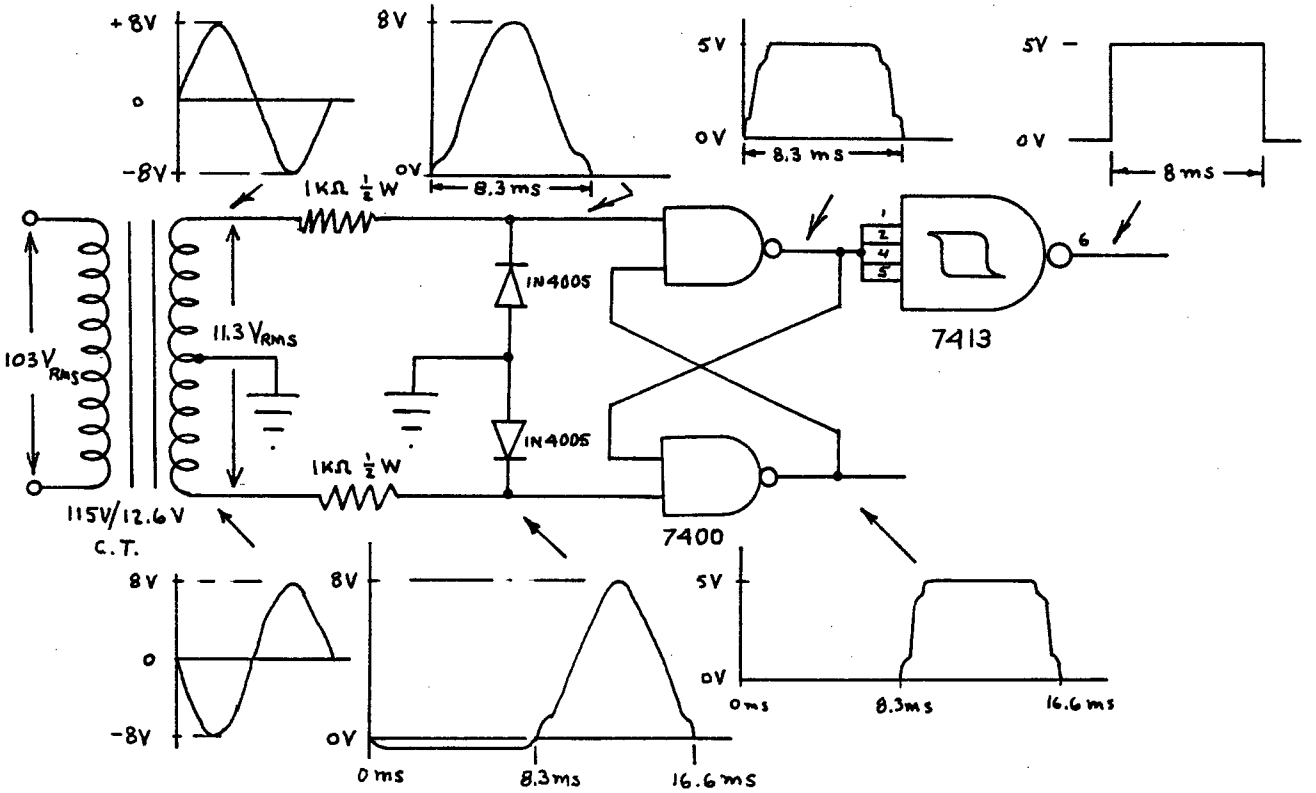
defined as the time required by the driving pulse to rise from 10% to 90% of its maximum level. Likewise, the fall time t_f is defined as the time in 139 which the signal drops from 90% to 10% of its maximum level.



In order to decrease the rise time of the leading edge and the fall time of the trailing edge, a wave shaping circuit may be used. A device commonly used in these applications is the Schmitt Trigger circuit.

The figure below shows a 60 Hz clock that uses a 7400 integrated circuit, followed by a 7413 that corresponds to a Schmitt trigger with NAND gate inputs. The symbol used for this Schmitt trigger has a hysteresis loop, to indicate its mode of operation.

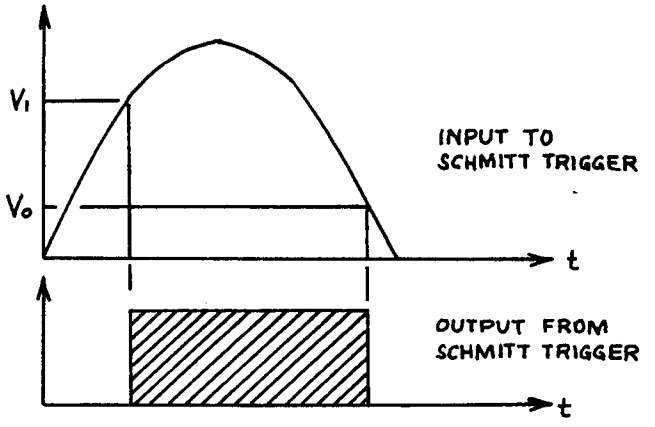
The resulting waveforms, as seen with an oscilloscope, are also shown. Where possible, this circuit should be assembled and tested.



THE SCHMITT TRIGGER CIRCUIT

The Schmitt trigger circuit is a wave shaping circuit. When used to produce a square wave from a positive sinusoidal alternation, it fires at a low voltage level V_1, producing a fast rise time.

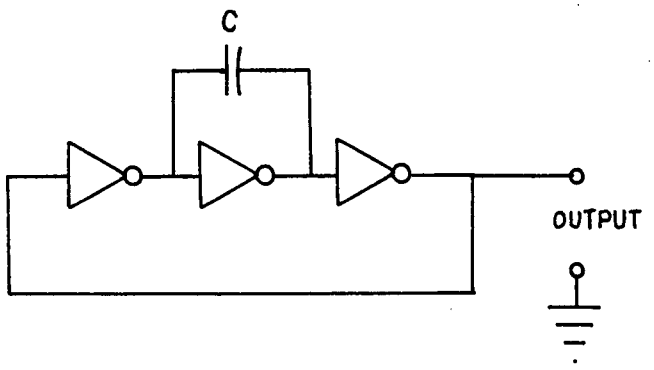
When the input voltage drops below a level V_o, see figure below, the Schmitt trigger circuit drops its output voltage with a fast fall time. In between voltage levels V_1 and V_o it maintains a constant output voltage that looks flat, and it thus shapes a positive alternation into a square looking pulse.



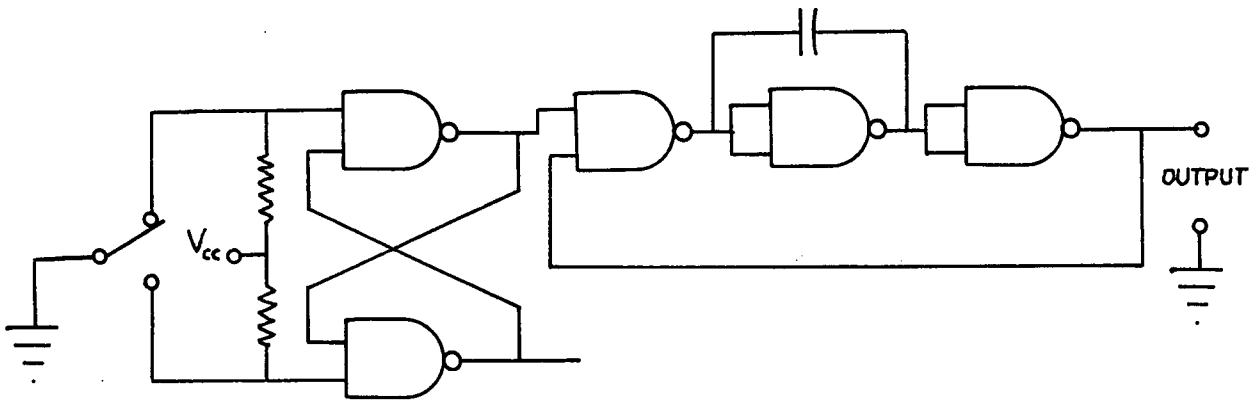
Notice that the output wave shape can be improved even further by including a Monostable Circuit to follow the Schmitt trigger. See the 555 timer used in Monostable mode.

c) RING OSCILLATOR CLOCKS

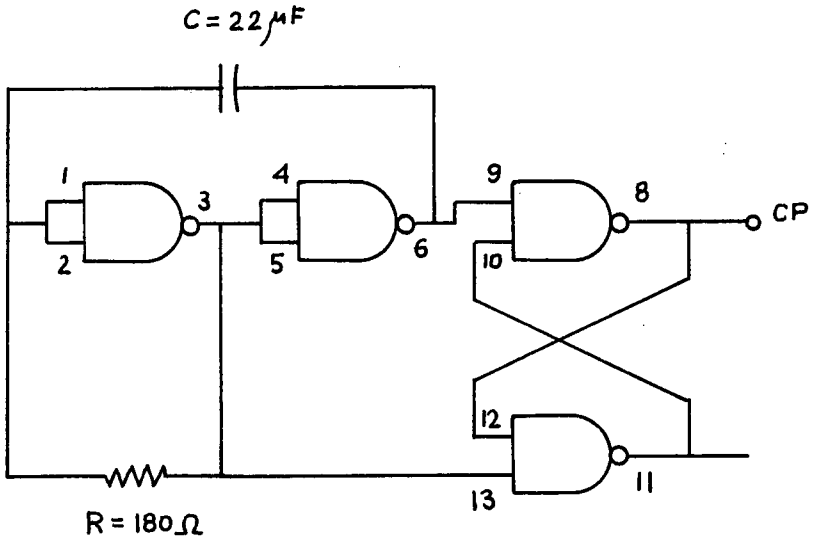
These circuits consist of strings of two or three inverters or amplifiers, where feedback loops are used to produce the oscillation condition. The simplest to assemble and test is the following.



If it is desired to gate above circuit, i. e., to get it to oscillate or to stop oscillating at a particular instant of time, nand gates and a manual pulser can be used as shown below.



Another oscillator that offers good timing pulses is shown next. Notice that the output wave shape can be improved even further by the addition of a flip flop as shown in the diagram. The numbers by the side of each input or output indicate suggested connections when an integrated circuit 7400 is used.



The frequency of oscillation can be estimated using the following expression:

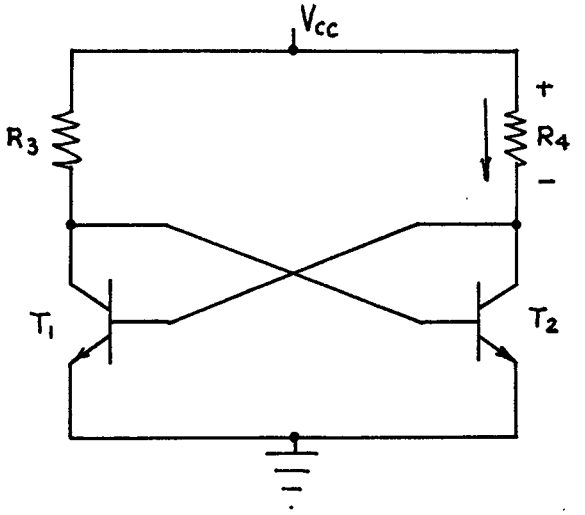
$$f = \frac{1}{3\ R\ C}$$

For the component values shown in the circuit above, this frequency becomes: $f = 84.3$ Hz

d) ASTABLE MULTIVIBRATOR

This is a basic oscillator circuit. Its theory of operation is outlined below, where two NPN transistors are used in the configuration. The advent of integrated circuits has facilitated the incorporation of more components to stabilize its operation, without complicating its use, as is seen in section (e) for the 555 Timer.

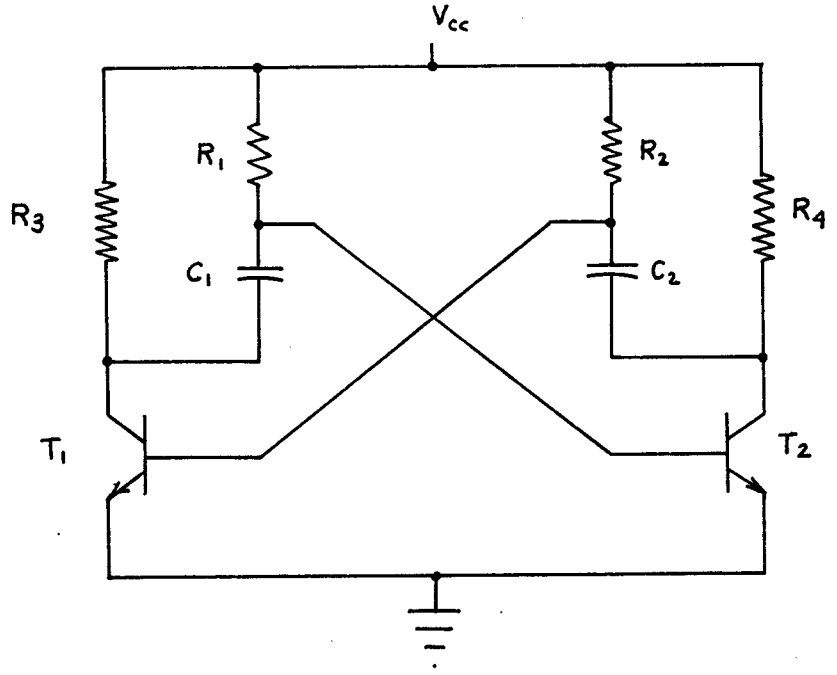
Consider the circuit below, where NPN transistors are used. Note that an NPN transistor conducts when its base receives a positive bias.



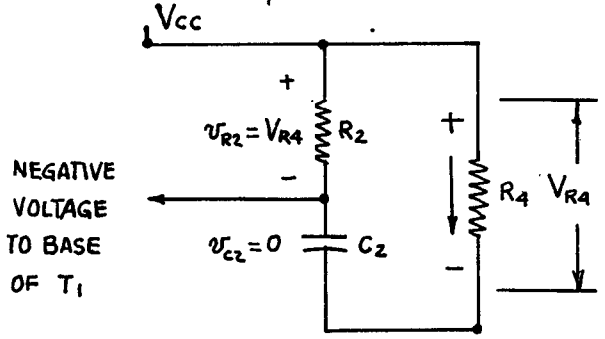
When power is applied, either transistor T_1 or T_2 will conduct, depending on which is ready to do so. If T_2 conducts more readily than T_1, then there is a voltage drop across R_4 with the polarity shown above. The negative voltage resulting from V_{R4} will be applied to the base of T_1, cutting it off.

Since T_1 is not conducting, the voltage at the collector of T_1 will be +V, and this positive voltage is applied to the base of T_2 keeping transistor T_2 turned "ON".

Above locked condition will remain as long as there is power, and can be broken by the addition of two RC circuits connected across R_3 and R_4 as shown below.

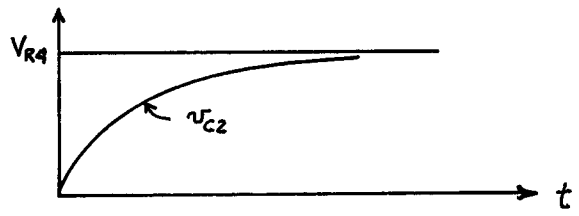


When power is applied to above circuit, if we assume that transistor T_2 is the first to switch on, we will see that the current through R_4 causes V_{R4}. At this instant of time, the voltage $v_{R2} = V_{R4}$ as seen in the sketch below, and consequently, a negative voltage gets applied to the base of transistor T_1, making sure that it remains cut off.

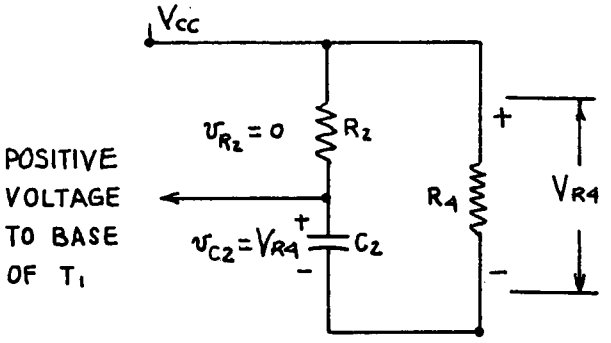


Since T_1 is cut off, the voltage at its collector is $+V_{cc}$ and when applied to the base of transistor T_2, it keeps this transistor T_2 switched on.

However, as time progresses, the capacitor C_2 charges exponentially to a maximum value of V_{R4}. Notice that $V_{R4} = v_{R2} + v_{C2}$.

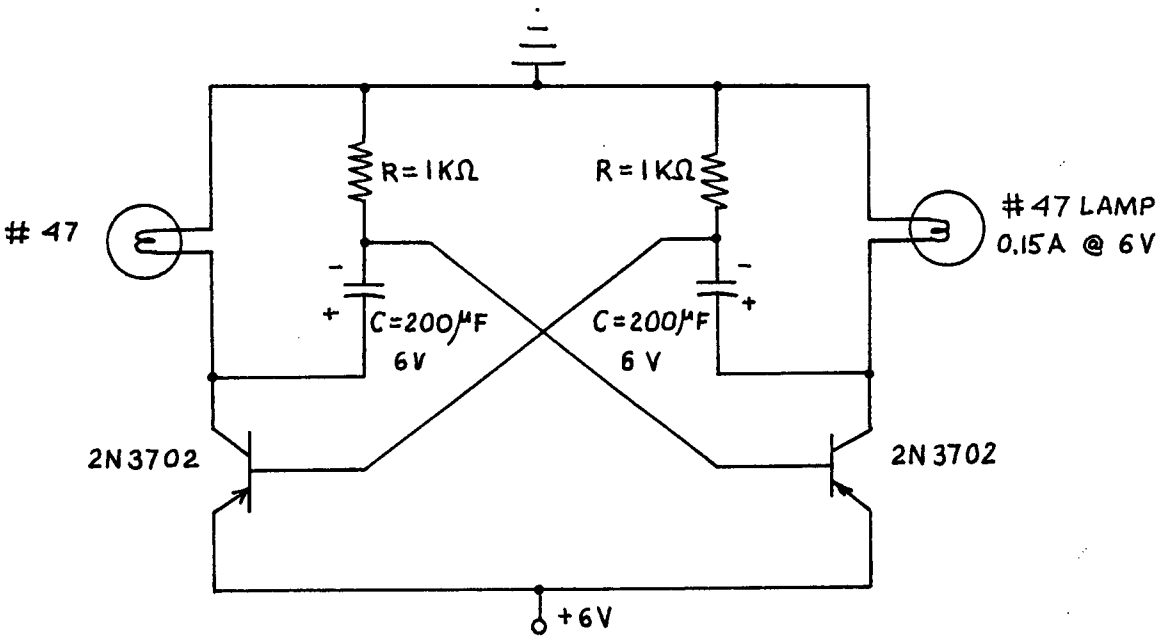


When $v_{C2} = +V_{R4}$, this positive voltage, fed to the base of transistor T_1, will trigger it to the "ON" condition.



Once the transistor T_1 begins to conduct, it acts as a short circuit to ground, and the current through it will cause voltage V_{R3}. Since $V_{R3} = v_{R1} + v_{C1}$ and $v_{C1} = 0$ at this instant of time, then the negative end of R_1 will apply a negative voltage to the base of transistor T_2, shutting it "OFF". The process is repetitive.

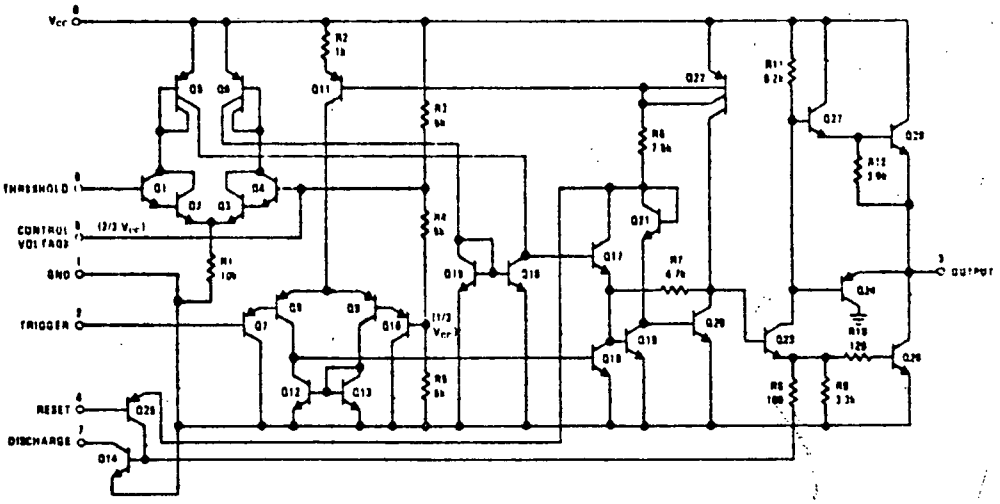
To verify above principles of operation, the following circuit may be assembled. Note that the time each lamp is on is given approximately by the expression $t_{on} = 0.7\ RC$.



Notice that the biasing in above circuit has been reversed, because the transistors used are PNP.

e) 555 TIMER

An astable multivibrator can be built using a 555 integrated circuit. This IC is called a Monolithic Timing Circuit. It is a very popular component used extensively in the electronics industry. Its electronic diagram is the following.

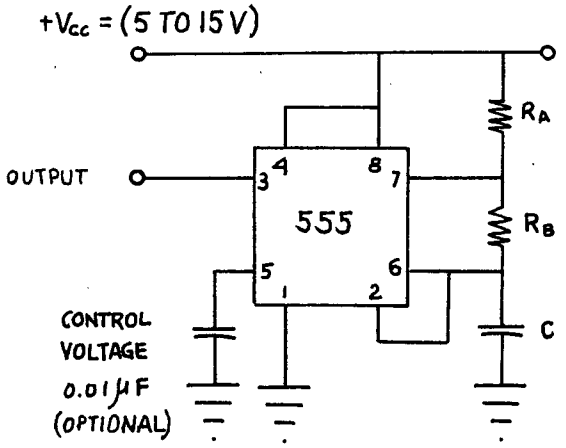


The 555 is a highly stable device for generating accurate time delays or oscillations. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits. Timing is from microseconds through hours.

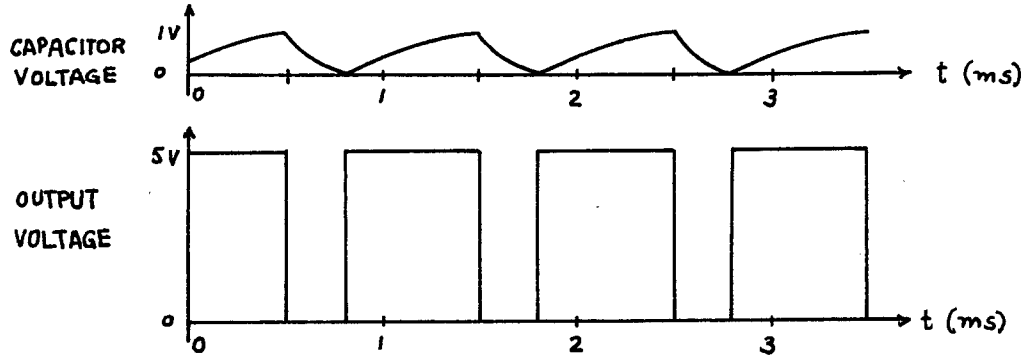
OPERATION IN THE ASTABLE MODE

In this mode of operation, the capacitor C shown in the figure below charges between 1/3 V_{cc} and 2/3 V_{cc}. The charge and discharge times,

as well as the frequency are independent of the supply voltage.



The following figure shows the actual wave forms generated in this mode of operation.



If the circuit is connected as shown above, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

The charge time (output HI) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

The discharge time (output LO) is given by:

$$t_2 = 0.693\ (R_B)\ C$$

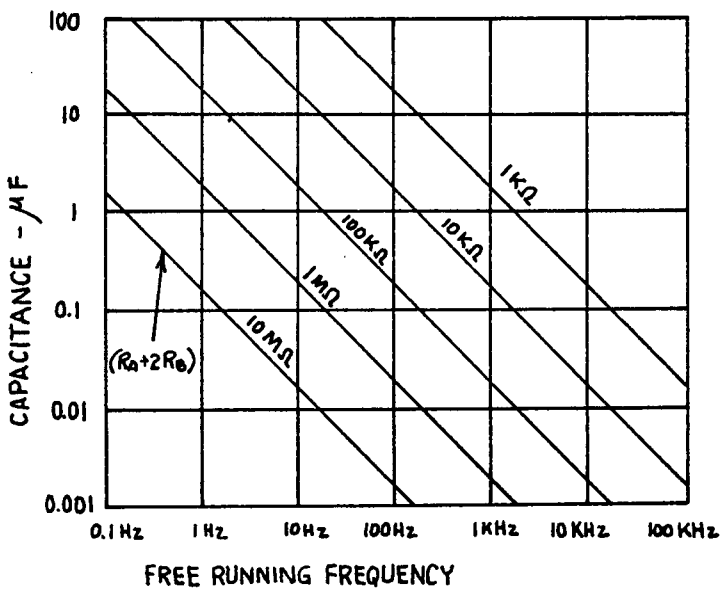
Therefore, the total period is given by:

$$T = t_1 + t_2 = 0.693\ (R_A + 2\ R_B)\ C$$

The frequency of oscillation is then:

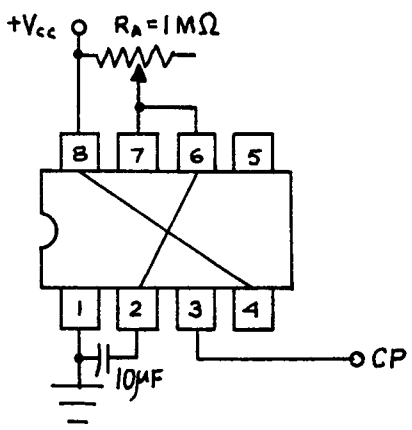
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Above frequency of oscillation may be easily found by the use of the following nomogram.



CALCULATION EXAMPLES USING ABOVE NOMOGRAM

EXAMPLE 1) The following configuration may be used to produce low frequency clock pulses. The one meghom potentiometer is intended to provide a manual control to determine desired frequency.



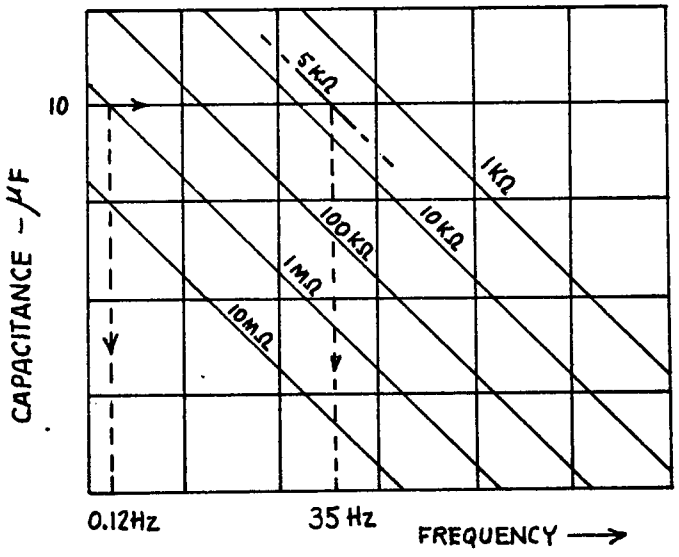
Using the above nomogram, the approximate range of frequencies can be estimated. e.g.

i) If the potentiometer is set for 1 megohm:

$$R_A + 2R_B = 1\ M\Omega + 2 \cdot 0 = 1\ M\Omega$$

$$C = 10\mu F$$

After reading the value of C on the C-axis, one moves to the right until the 1 MΩ line is intersected. Then one moves downwards until the frequency axis is intersected. It reads about 0.12 Hz.



ii) If the potentiometer is set for 5 KΩ, then:

$$R_A + 2R_B = 5\ k\Omega + 0 = 5\ k\Omega$$

We repeat the process of reading the value of C on the C-axis and move to the right until the 5 kΩ line is intersected. Since this line is not in the nomogram, it must be interpolated. This is done by observing that the scales are logarithmic, therefore, the 5 kΩ line will not be at the geometric center of the 1 kΩ and the 10 kΩ lines, but rather closer to the 10 kΩ line than the 1 kΩ line.

At the estimated intersection, we move down to the f-axis and read the frequency to be: f = 35 Hz

Therefore, for potentiometer settings between 5 kΩ and 1 MΩ, the resulting range of frequencies will be between 1.2 Hz and 80 Hz.

Above circuit can be assembled and tested at its lower frequency range using a stopwatch. For higher frequencies, a frequency counter or an oscilloscope will be necessary.

EXAMPLE 2) Determine the frequency if R_A = 100 kΩ, R_B = 20 kΩ and C = 10 μF.

Solution: $R_A + 2R_B = 100\ k\Omega + 2 \cdot 20\ k\Omega = 140\ k\Omega$

Read C = 10 μF on the C-axis and move to the right until the 140 kΩ line is intersected (it is closer to 100 kΩ than to 1 MΩ). Then, moving downwards, read the frequency on the f-axis. It is about 10 Hz.

EXAMPLE 3) Determine the value of R_A for R_B = 0 and C = 30 μF, to yield a frequency of 10 Hz.

Solution: Read f = 10 Hz on the f-axis and also read C = 30 μF on the C-axis. Now find where lines perpendicular to these readings intersect.

They intersect above the 10 kΩ line. Considering the logarithmic interpolation, we estimate them to be at 8 kΩ.

Therefore: $R_A + 2R_B = 8\ k\Omega$

Since $R_B = 0$, then $R_A = 8\ k\Omega$

NOTE.- If R_A happens to be a linear potentiometer, i. e. each mechanical angular rotation corresponds to an even change in resistance, this potentiometer will act as a tapered resistor (logarithmic response), due to the nature of the nomogram and the circuit response.

OUTPUT WAVEFORMS AND SYMMETRY

The charge time, when the output pulse is HI is determined by the resistors R_A, R_B and the capacitor C. It is given by the expression:

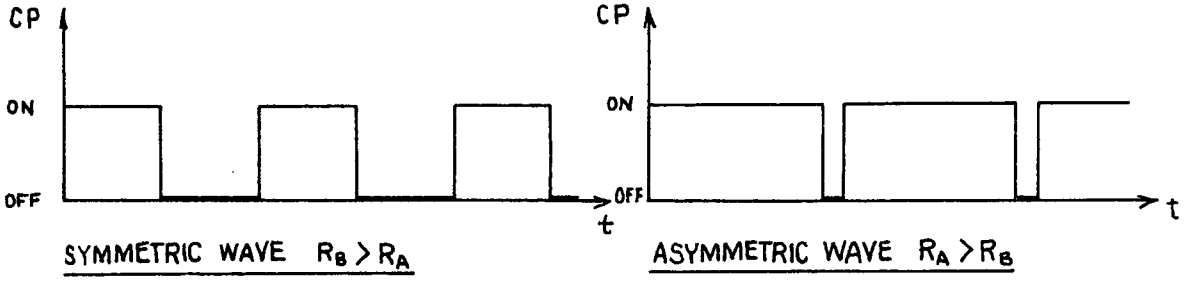
$$t_1 = 0.693\ (R_A + R_B)\ C$$

The discharge time, when the output pulse is LO, is determined only by the resistor R_B and the capacitor C. It is given by the expression:

$$t_2 = 0.693\ (R_B)\ C$$

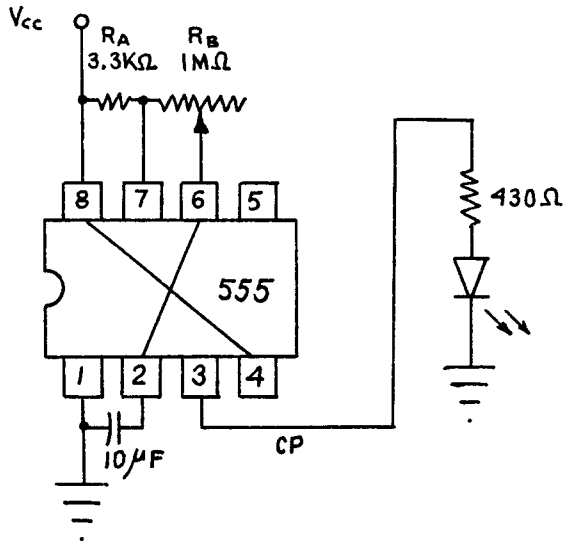
Therefore, by carefully selecting the ratio R_A to R_B, one can vary the length of time when the pulse is HI with respect to when it is LO. This variation can take place for a pulse being HI 50% of the time, i. e. the symmetric condition, to pulses being HI up to 99.9% of the time, i. e. the asymmetric condition.

Notice that the output pulse cannot be HI less than 50% of the time. Also, that the condition for symmetry is that R_B is made large with respect to R_A.

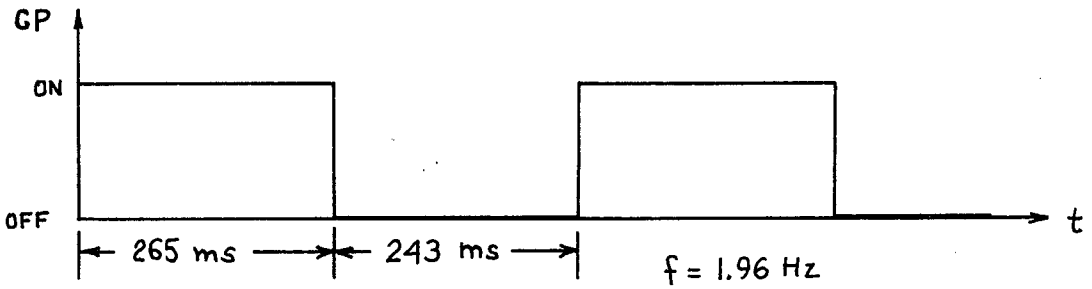


LABORATORY EXPERIMENT

The following astable multivibrator circuit may be assembled to corroborate the symmetry of the output waves. An oscilloscope may be useful but is not indispensable.

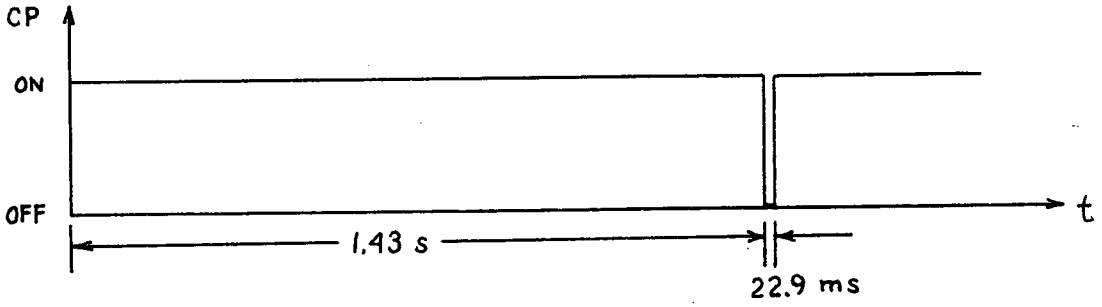


a) VISUAL SYMMETRY.- When R_A = 3.3 kΩ and R_B is close to 55 kΩ, the condition for symmetry is satisfied. This yields an output frequency close to 2 Hz. This low frequency is easy to monitor with an LED as an output indicator and a stop watch. The length of time that the LED is ON corresponds closely to the length of time when it is OFF, thus verifying symmetry.



However, if R_B is made to be about 500Ω, asymmetry occurs, because R_B is no longer greater than R_A. This last condition can no longer be verified visually, because the frequency rises to about 33 Hz.

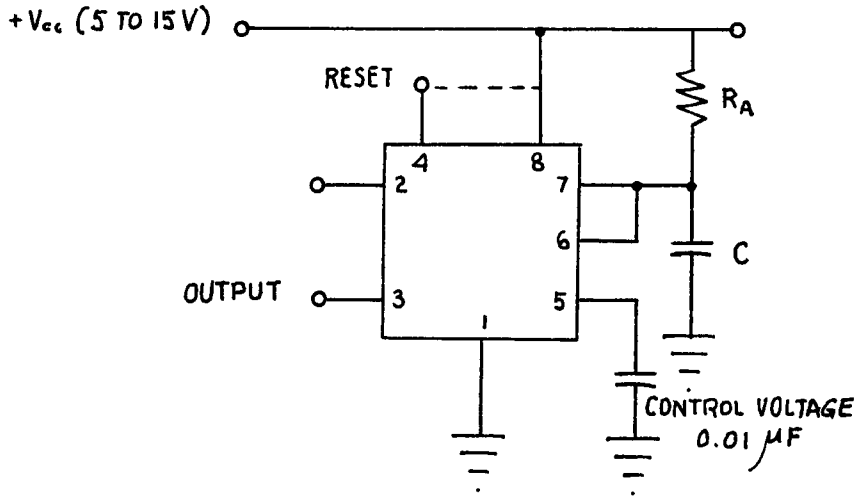
b) VISUAL ASYMMETRY.- In the absence of an oscilloscope, the same circuit, with a small modification, can be used to observe the asymmetric condition. Simply exchange the potentiometer and the fixed value resistor, so that the potentiometer is now connected between pins 7 and 8 of the 555 timer, and the 3.3 kΩ resistor is connected between pins 6 and 7 of the same timer. By setting the potentiometer (R_A in this case) to a value close to 200 kΩ , asymmetry results since $R_A > R_B$ where now R_B = 3.3 kΩ. The resulting frequency is close to 0.7 Hz and the asymmetric condition can be observed visually. The LED will be ON for about 1.43 seconds and then OFF for close to 23 ms.



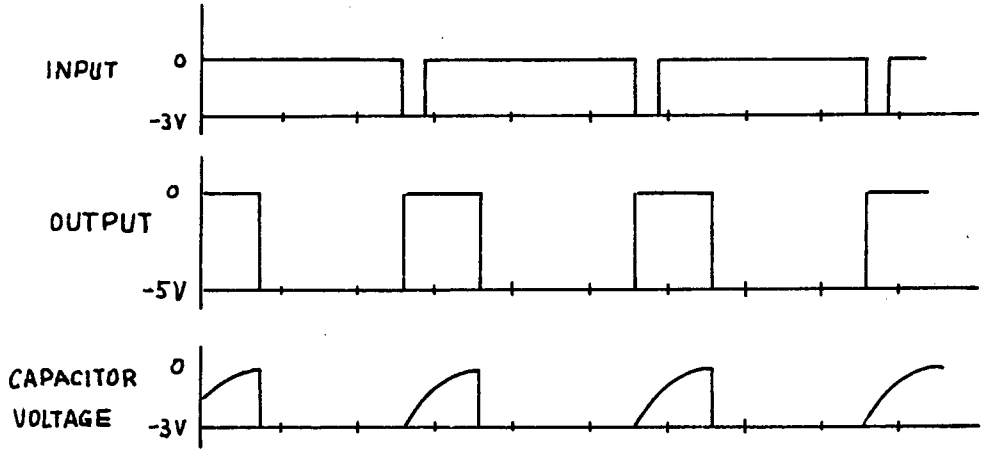
For this last configuration, if R_A is set to a low value, say 200Ω , then $R_B > R_A$ and symmetry is re-established again. However, it can not be monitored visually because the frequency rises to about 21 Hz.

OPERATION IN THE MONOSTABLE MODE

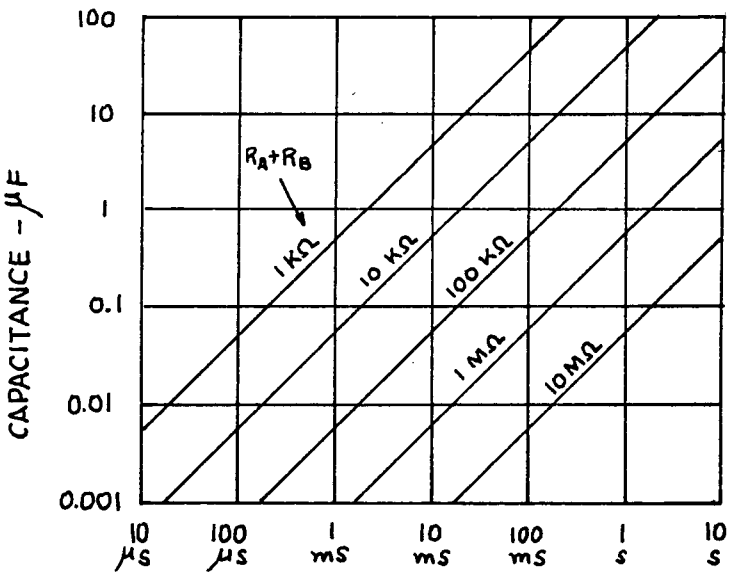
In this mode of operation, the timer functions as a one-shot. Referring to the figure below, the external capacitor is initially held discharged by a transistor inside the timer.



Upon application of a negative trigger pulse to pin 2, the flip flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now increases exponentially with the time constant $\tau = R_A C$. When the voltage across the capacitor equals 2/3 V_{cc}, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state. The actual wave forms generated in this mode are shown below.



The circuit triggers on a negative going input signal when the level reaches 1/3 V_{cc}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it gets triggered again during this interval. The time that the output is in the high state is given by $t = 1.1\ R_A\ C$ and can easily be determined by the nomogram below.



Since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of the supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{cc} to avoid any possibility of false triggering.

6

COUNTERS

Counters are arrangements using flip flops to store and update a set of initial or current conditions, according to a predefined sequence. Their use is of great importance in electronic digital systems. The state of a counter may be displayed in different ways, according to desired use.

Digital clocks display the state of a counter. Digital voltmeters indicate the binary count that takes place while comparing voltages. Distance measuring devices count the time a pulse takes to reach a given destination. The sequential change of a counter is used to give the impression of movement in advertising displays. Their use in computer operation as well as in the transmission of data makes them indispensable.

Counters can be divided into Asynchronous and Synchronous circuits.

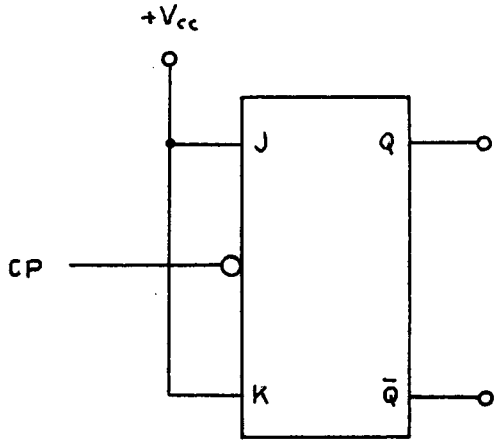
THE ASYNCHRONOUS COUNTER

This counter is also known as a Ripple Through Counter because only the first flip flop in the circuit receives a clock pulse, and it takes a finite time for all the other flip flops to get updated.

The final limit on the number of flip flops in a ripple through counter is the total propagation time, where propagation time is the time it takes a signal to go through each flip flop.

Since each flip flop delays the initial clock pulse, the total propagation time within the circuit must be less than the time defined between two consecutive clock pulses.

Ripple through counters may be assembled using JK master slave flip flops. These master slave flip flops are used in the toggle mode, which is the result of the following connections.

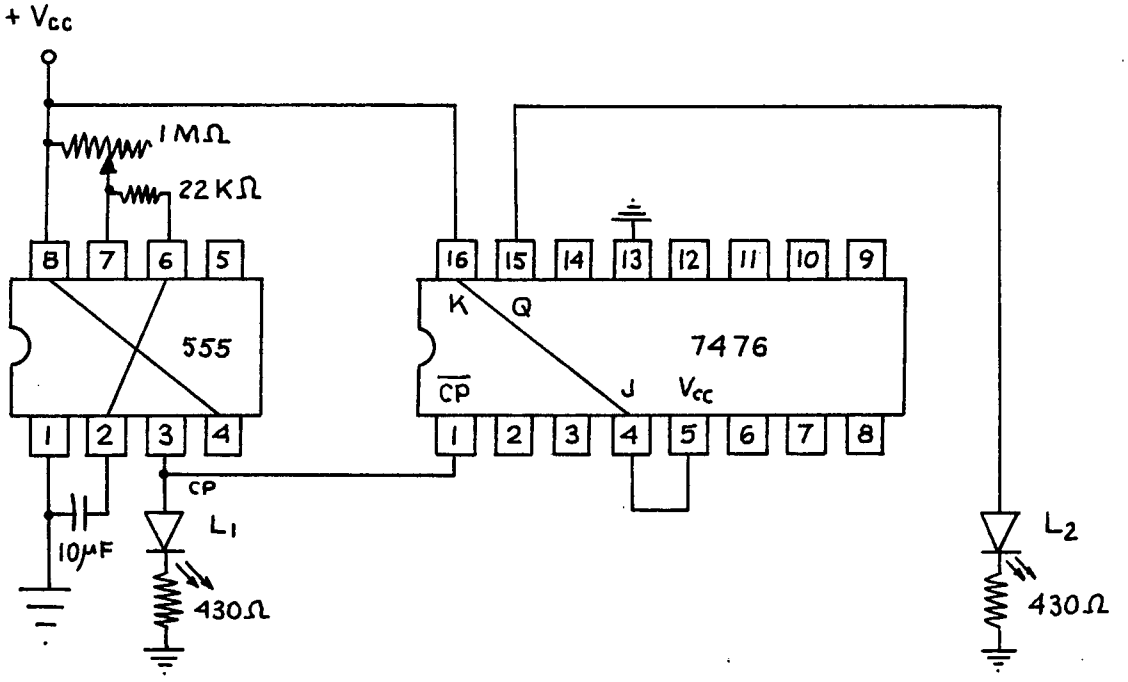


In this mode of operation, each flip flop will change state with every HI to LO transition on its CP input. From the truth table shown below, one can see that if J = K = 1, then, after a CP input pulse, the output conditions in the flip flop reverse from a condition Q (a "1" or a "0"), to a condition $\overline{Q}$ (a "0" or a "1" respectively).

J	K	Q_n	Q_{n+1}
0	0	Q_n	Q_n
0	1	Q_n	0
1	0	Q_n	1
1	1	Q_n	$\overline{Q}_n$

Toggle Condition

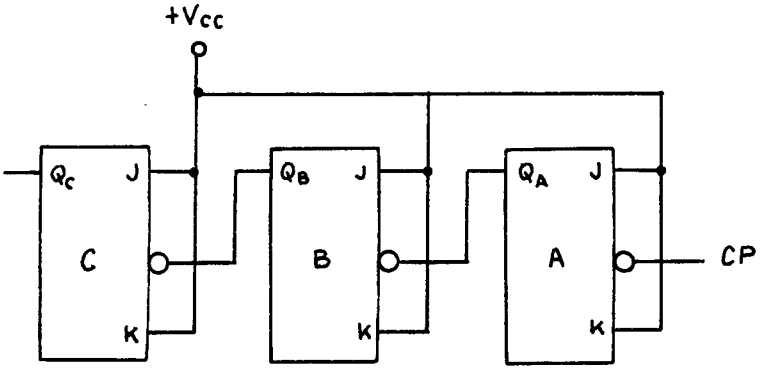
In order to corroborate the toggle action of a JK master slave flip flop, the following circuit may be assembled.



If the clock frequency is kept sufficiently low, one should be able to observe that LED 2 turns ON or OFF every time that LED 1 goes OFF, i. e., during the HI to LO transition.

0 - 7 RIPPLE THROUGH COUNTER

This circuit consists of three JK master slave flip flops used in the toggle mode. These flip flops are connected in tandem as shown below.



To analyze its operation, we can build up a truth table. Due to the toggle mode of the flip flops,

- FF A will change every time a clock pulse changes from a HI to a LO, i. e. the flip flop will change state with every clock pulse from the master clock.
- FF B will change state every time that FF A changes from a "1" to a "0".
- FF C will change state every time that FF B changes from a "1" to a "0"

Above results are used to build up the table below. An initial condition has been assumed, where the state of the flip flops A, B and C is zero.

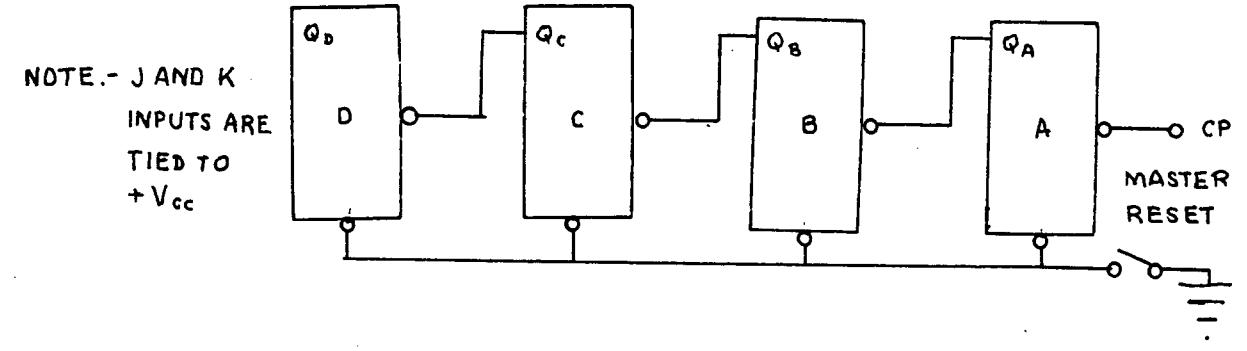
From the table, it is clear that a binary count takes place. This count is from 0 to 7 and recycles itself to zeroes after the maximum number in the count has been reached.

COUNT	C	B	A
	BINARY WEIGHTS		
	$2^2=4$	$2^1=2$	$2^0=1$
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
0	0	0	0

The state table for this counter is given below.

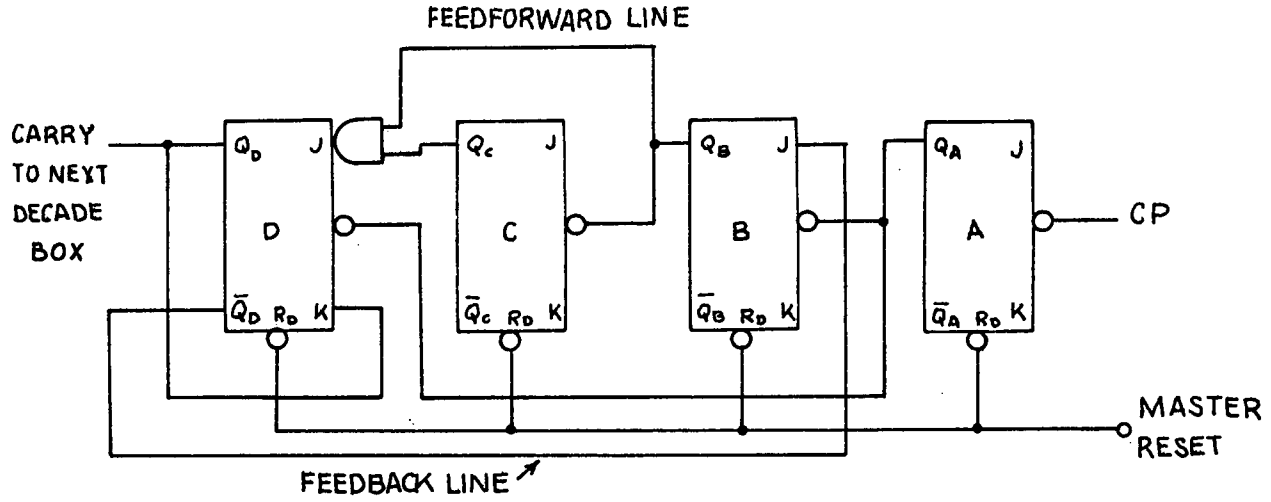
COUNT	D	C	B	A
	BINARY WEIGHTS			
	2^3	2^2	2^1	2^0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

The circuit below has provision to prereset the counter to zeroes. The circuit is an extension of the 0 - 7 ripple through counter with an added flip flop.



8421 BCD DECADE COUNTER

The 8421 Binary Coded Decimal Decade Counter is a well thought out application of feed-forward and feed-back lines. Detection is made of the presence of N-1 where N is the desired count. Thus the counter is reset whenever the Nth. pulse takes place. The counter counts from 0 to 9 in binary weighted fashion and resets to 0 to start the count all over again.



NOTE.- J AND K INPUTS SHOWN WITHOUT CONNECTION ARE TIED TO $+V_{cc}$

DESCRIPTION OF OPERATION

After a Master Reset Pulse, the counter stores 0000. Under this circumstance, FF D stores a 0, therefore the J input of FF B will be conditioned, i. e. J and K inputs to FF B are HI.

Both inputs to FF D will be inhibited: Input J by the AND gate (BC) and input K by the Q output of FF D.

The set J input to FF B is conditioned with a HI from $\overline{Q}_D$ so that it can operate normally with incoming pulses from 1 to 7.

The counter counts in binary sequency until a count of 0111 is reached.

At count 0111, the J input to FF D is conditioned by the AND gate (BC).

The eighth input pulse will reset A, B, C and FF D will be set to a "1" by its J input.

The nineth input pulse sets A = 1, therefore the count will be 1001. FF B is inhibited by a LO from $\overline{Q}_D$ into its J input, therefore it will not change state during the 9th. and 10th. pulses, otherwise it would read 1011 for a nine and 0010 for zero.

The tenth input pulse causes A to go to zero, and the HI to LO transition from FF "A" is fed forward to the clock input of FF D. Since input K of FF "D" is conditioned and input J of FF "D" is inhibited, FF D changes to "0", thus completing the cycle.

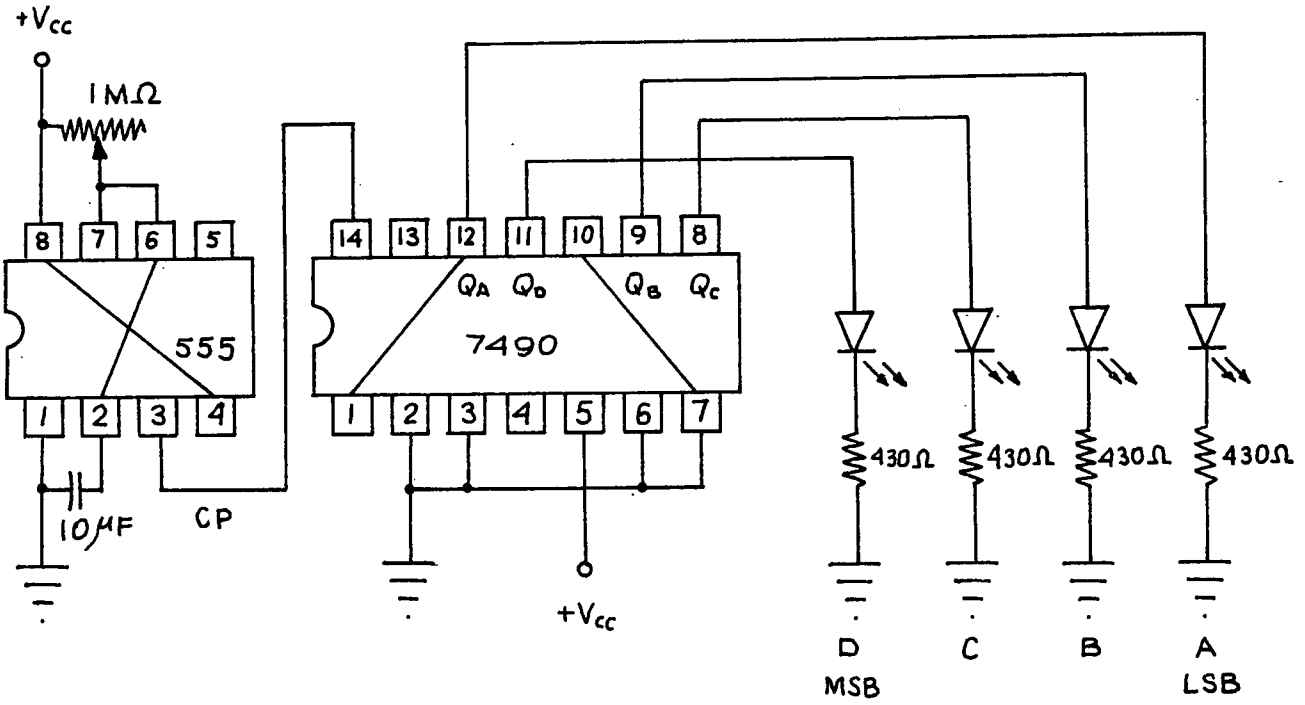
Notice that above last HI to LO transition of FF D occurs only once during the whole count, therefore it can be used to drive another stage of BCD counters to count from 0_{10} to 99_{10}, etc.

STATE TABLE

COUNT	D	C	B	A
	BINARY WEIGHTS			
	$2^3=8$	$2^2=4$	$2^1=2$	$2^0=1$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

To test the previous table,the following circuit may be assembled. Notice that it uses a 555 timer to produce the clock pulses, and a 7490 Decade Counter, to do the count. Technical specification sheets are included regarding the 7490 decade counter.

The display of the count is done by the use of light emitting diodes, where LED D corresponds to the Most Significant Bit (MSB = $2^3 = 8$) and LED A corresponds to the Least Significant Bit (LSB = $2^0 = 1$).



7

THE SYNCHRONOUS COUNTER

This counter is one of the most extensively used in digital systems, because of its ability to accept clock pulses.

Synchronous counters are used to produce binary counts as well as special counts. Among the special counts, we find circuits known as ring counters, mobius counters and many different kinds of light chasers.

Above special counts are applications of a more general circuit known as the shift register.

Shift registers are used to manipulate data in computer systems as well as in the transmission and reception of digital information.

DESIGN OF SYNCHRONOUS BINARY COUNTERS

The binary count from these counters is read from the state of binary weighted flip flops. If the count is from 0 to 1, the circuit is also known as Modulo 2, and requires only one flip flop. If the count is from 0 to 3, two flip flops are needed. If the count is from 0 to 7, three flip flops are required, etc. In general, the count and the number of flip flops are related by the expression: $\text{COUNT} = (2^n - 1)$ where n = number of flip flops

The design procedure is the following.

a) A table of the binary count is made, with the corresponding state for each flip flop.

b) A table of the triggering functions needed to step each count is added to step (a).

c) The table of triggering functions is synthesized using Boolean expressions.

d) Above Boolean expressions are simplified by means of Karnaugh maps.

e) The circuit gets implemented according to the resulting Boolean expressions.

0 - 7 BINARY SYNCHRONOUS COUNTER

To build up this synchronous binary counter:

a) Make a table with the desired count and its binary weighted equivalent. In the table below, the contents of A, B and C will be stored in three JK master slave flip flops.

COUNT	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
0	0	0	0

b) Investigate which triggering pulses will change the state of each of the three JK master slave flip flops in order to result in the next count.

Example.- For count 0 to 1, we need to change only the state of Flip flop A, therefore, the triggering pulses must be:

$$A_t = 1 \; ; \quad B_t = 0 \quad \text{and} \quad C_t = 0$$

For the count 1 to 2 we need to change the state of flip flops A and B, therefore:

$$A_t = 1 \; ; \quad B_t = 1 \quad \text{and} \quad C_t = 0$$

In the fashion shown above, the table of triggering pulses is made and is placed adjacent to the previous one:

COUNT	C	B	A	C_t	B_t	A_t
0	0	0	0	0	0	1
1	0	0	1	0	1	1
2	0	1	0	0	0	1
3	0	1	1	1	1	1
4	1	0	0	0	0	1
5	1	0	1	0	1	1
6	1	1	0	0	0	1
7	1	1	1	1	1	1
0	0	0	0			

c) Now, we can proceed to the synthesis of the triggering pulse table, i. e., A_t, B_t and C_t will be expressed as Boolean equations.

A_t occurs every time a count is to be updated, therefore, everytime that a clock pulse arrives:

$$A_t = CP$$

B_t is true in any of the following rows:

2nd. row, when A = 1, B = 0 and C = 0, i. e. when $A\ \overline{B}\ \overline{C}$

4th. row, when A = 1, B = 1 and C = 0, i. e. when $A\ B\ \overline{C}$

6th. row, when A = 1, B = 0 and C = 1, i. e. when $A\ \overline{B}\ C$

8th. row, when A = 1, B = 1 and C = 1, i. e. when $A\ B\ C$

Therefore:

$$B_t = A\ \overline{B}\ \overline{C} + A\ B\ \overline{C} + A\ \overline{B}\ C + A\ B\ C$$

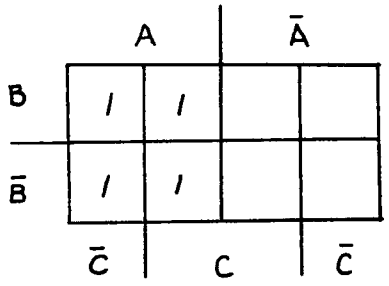
C_t is true on the fourth row, when $A\ B\ \overline{C}$, or on the 8th. row, when A B C. Therefore:

$$C_t = A\ B\ \overline{C} + A\ B\ C$$

d) Above expressions can be simplified best by the use of Karnaugh Maps:

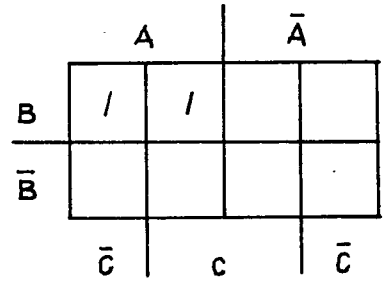
For A_t we know that $A_t = CP$, which is just a wire connected to CP.

For B_t:



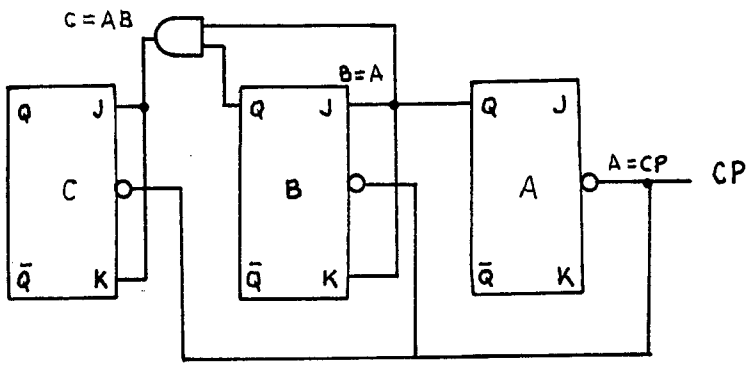
Therefore: $B_t = A$

For C_t:



Therefore: $C_t = A\ B$

e) Implementation of the circuit. Draw three JK master slave flip flops and wire them in accordance to the previous equations:



OPERATION.-Inputs J and K for flip flop A are tied to $+V_{cc}$, therefore flip flop A will change state every time a clock pulse arrives.

Flip flop B will change state only every other clock pulse, when its inputs J and K receive a HI from flip flop A.

At the end of count 3, C = 0; B = 1 and A = 1, therefore:

The J and K inputs of C have a HI from A B.

The J and K inputs of B have a HI from A.

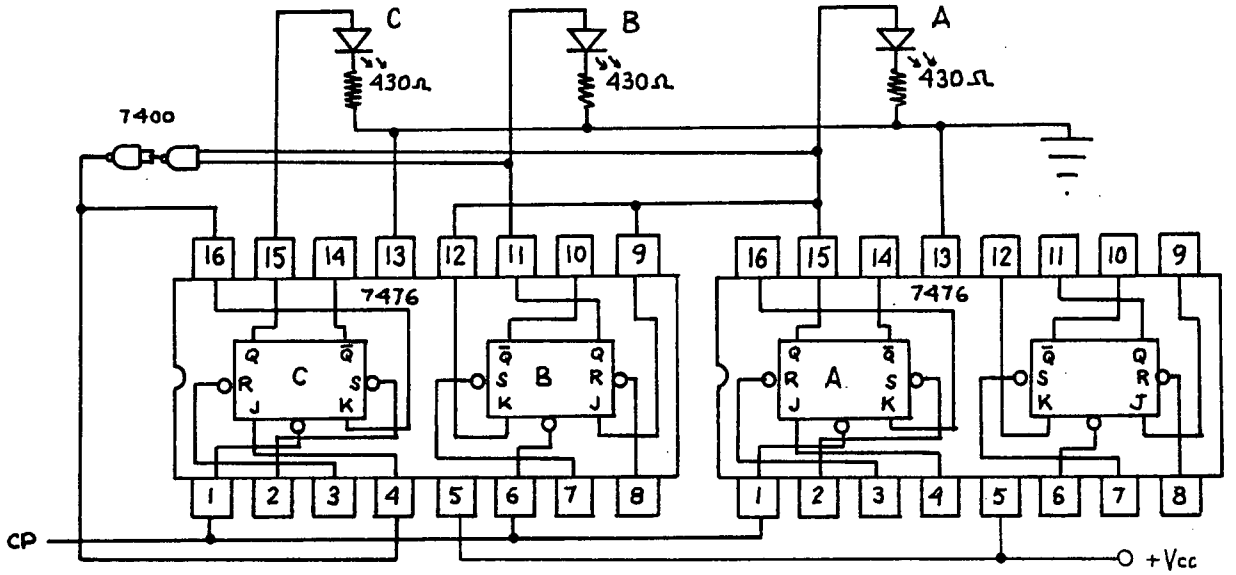
The J and K inputs of A have a HI from V_{cc}

When the next clock pulse arrives, it changes above three states to: C = 1; B = 0 and A = 0

The same J and K input conditions for A, B and C repeat at the end of count 7, when C = 1; B = 1 and A = 1.

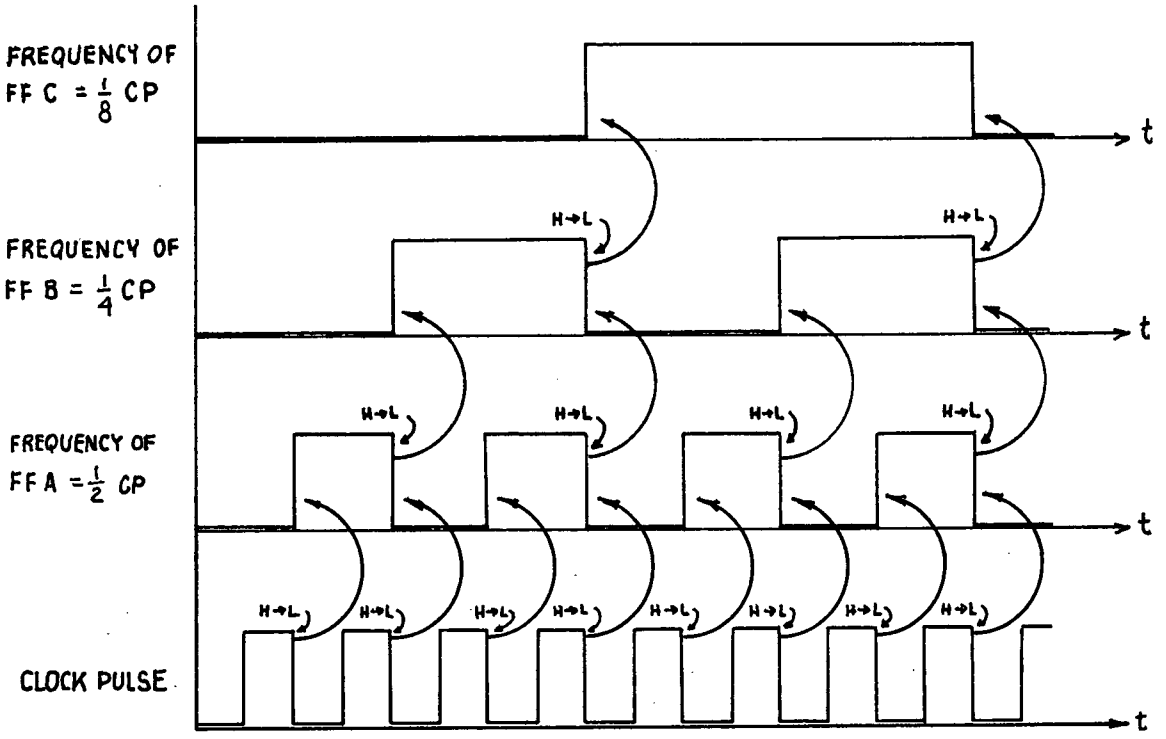
Therefore, the next clock pulse after the count of 7 will reset the three flip flops to: C = 0; B = 0 and A = 0 thus commencing the cycle all over again.

This circuit may be assembled using two dual master slave flip flops like the 7476 integrated circuit and one 7400 as shown below. Notice that LED's have been used as indicators, and that they are installed at the Q output of each flip flop. Pin connections are suggested but different arrangements may be used.



The state of each flip flop versus time is shown below. Notice that the resulting voltage levels have different frequency than that of the initial clock pulse. This result allows these circuits to be used as frequency dividers.

Digital clocks make use of this important application by subdividing the master clock frequency into subfrequencies that will trigger the seconds, the minutes and the hours.



STATE OF FLIP FLOPS									
C	0	0	0	0	1	1	1	1	0
B	0	0	1	1	0	0	1	1	0
A	0	1	0	1	0	1	0	1	0
BINARY COUNT	0	1	2	3	4	5	6	7	0

MODULO 16 BINARY SYNCHRONOUS COUNTER

This circuit should count from 0 to 15. The procedure used to develop it is the one outlined above.

a & b) State table:

COUNT	D	C	B	A	TRIGGERING FUNCTIONS			
					D_t	C_t	B_t	A_t
0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	1
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	1	1	1
4	0	1	0	0	0	0	0	1
5	0	1	0	1	0	0	1	1
6	0	1	1	0	0	0	0	1
7	0	1	1	1	1	1	1	1
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	1	1
10	1	0	1	0	0	0	0	1
11	1	0	1	1	0	1	1	1
12	1	1	0	0	0	0	0	1
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	0	1
15	1	1	1	1	1	1	1	1
0	0	0	0	0				

c) Synthesis of triggering functions. The boolean expressions for above triggering functions are:

$$A_t = CP$$

$$B_t = A\,\overline{B}\,\overline{C}\,\overline{D} + A\,B\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,\overline{D} + A\,B\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + A\,B\,\overline{C}\,D + A\,\overline{B}\,C\,D + A\,B\,C\,D$$

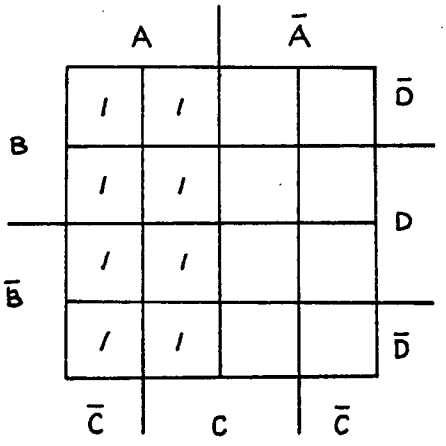
$$C_t = A\,B\,\overline{C}\,\overline{D} + A\,B\,C\,\overline{D} + A\,B\,\overline{C}\,D + A\,B\,C\,D$$

$$D_t = A\,B\,C\,\overline{D} + A\,B\,C\,D$$

d) Simplification of above expressions by means of Karnaugh maps:

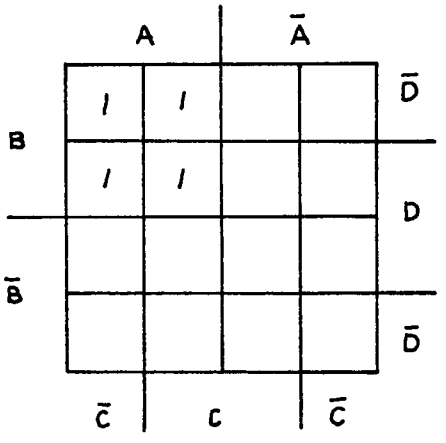
For A_t: $A_t = CP$

For B_t:



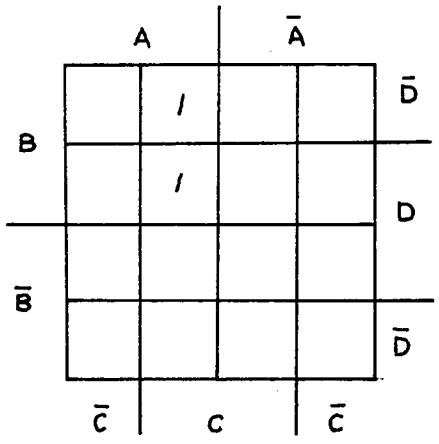
Therefore: $B_t = A$

For C_t:



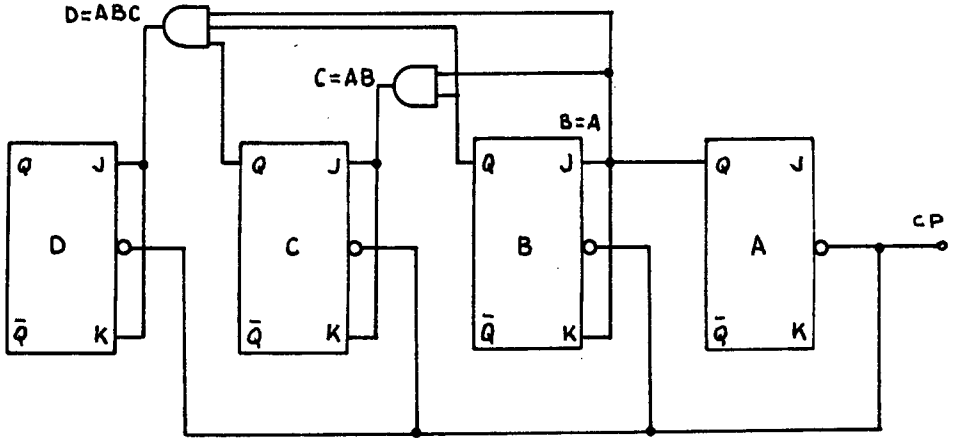
Therefore: $C_t = A\,B$

For D_t:

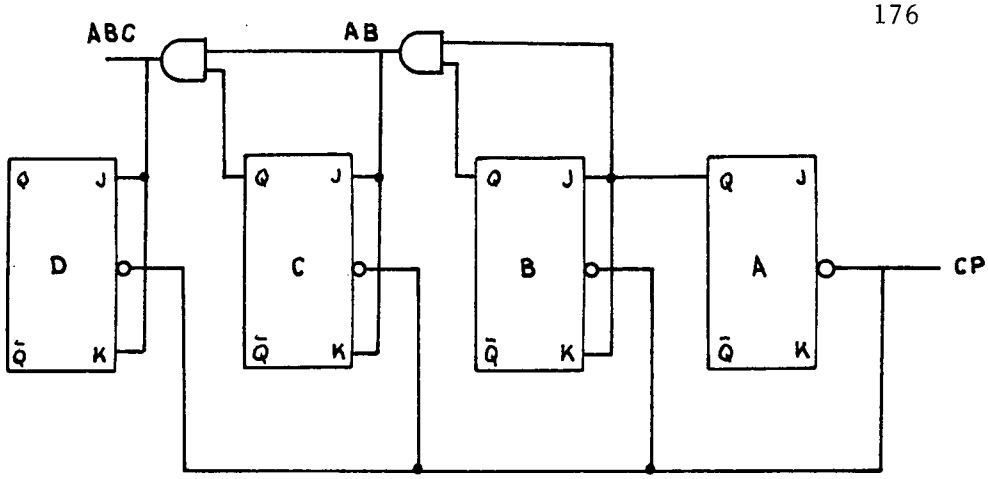


Therefore: $D_t = A\ B\ C$

e) Circuit implementation



In long counter chains, gates will require a large number of inputs or "FAN-IN", as these inputs are also referred to. A solution to limit this fan-in is the connection shown below.



The gates in above circuit have a maximum fan-in of two, i. e. only two inputs. The only restriction is that in long counter chains, all the gating must have taken place before the HI to LO transition of the clock pulse, otherwise a race condition will affect the results.

COUNT DOWN COUNTER

Above counter may be used to count down. This is achieved by taking the results from the $\overline{Q}$ outputs, this way, the read out will be that of the inverted values.

Above can be easily seen if we start with the initial zero value in the table below, and continue to count up.

Q_D	Q_C	Q_B	Q_A	COUNT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
etc.				

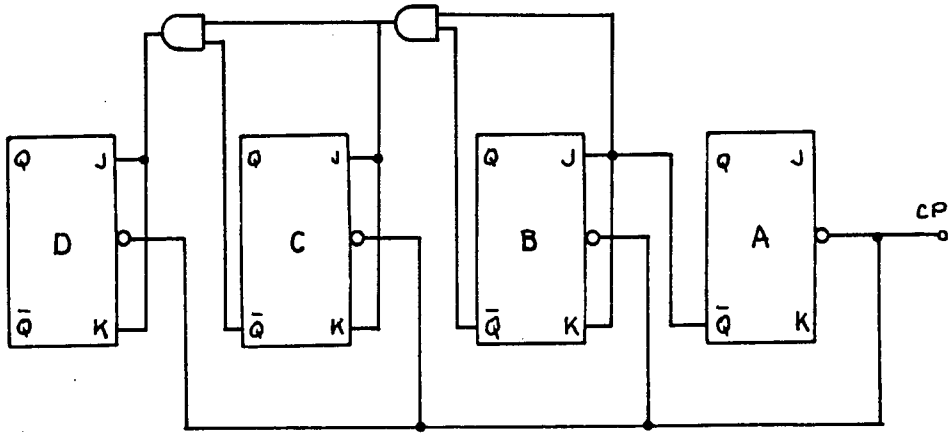
If we now obtain the outputs from the $\overline{Q}$ lines, instead of the Q lines, the first row of our count will correspond to the inversion of 0000, i. e. 1111, the second row will correspond to the inversion of 0001, i. e. 1110 and so on, so that our table will look as shown below.

$\overline{Q}_D$	$\overline{Q}_C$	$\overline{Q}_B$	$\overline{Q}_A$	COUNT
1	1	1	1	15
1	1	1	0	14
1	1	0	1	13
1	1	0	0	12
1	0	1	1	11
etc.				

Therefore, with above provision, the counter counts down.

If it is desired to obtain the outputs from the Q lines, a variation of above circuit will be to connect the $\overline{Q}$ output of a previous stage to the gated inputs of succeeding stages.

The circuit below may be assembled to test its operation, and also, it may be analyzed, by using the procedure outlined in the next section.



ANALYSIS OF SPECIAL SYNCHRONOUS COUNTERS

As mentioned before, some of these special counts are particular applications of the more general Shift Register.

Once a counter is given, we can always analyze its operation as shown below.

a) Consider the state of the flip flops after an initial condition, usually determined by a master reset pulse.

b) Consider the logic level of the J and K inputs (either HI or LO).

c) Add a clock pulse and observe the changes that it causes on the state of each flip flop.

d) Tabulate the changes that occur in each flip flop for each clocking pulse.

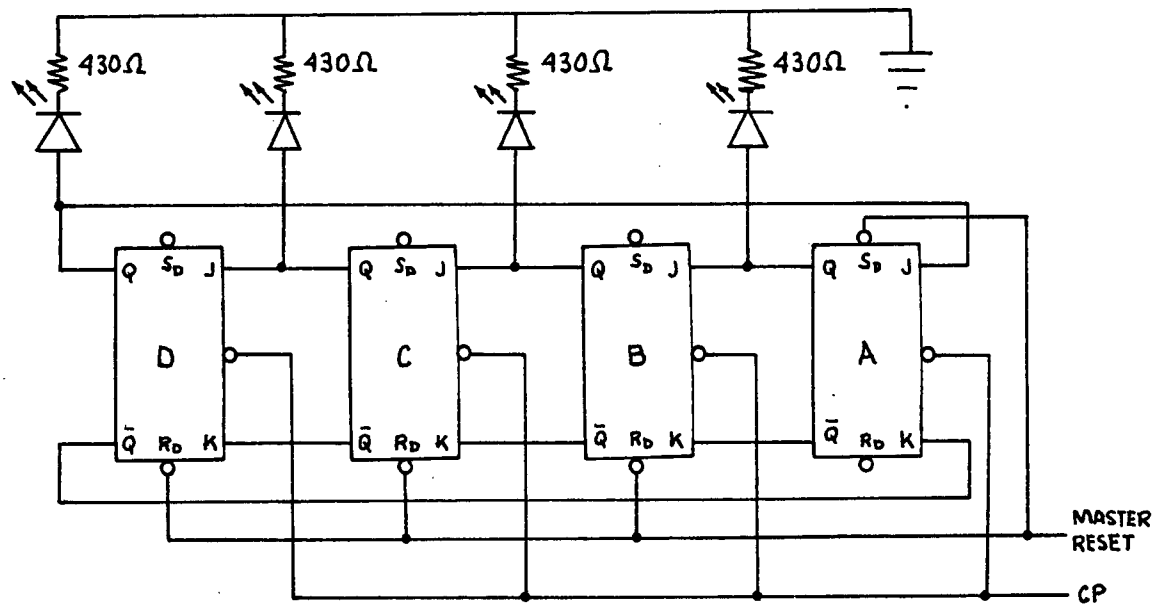
e) Repeat (a) to (d) until a pattern or return to initial conditions occurs.

RING COUNTER

This circuit is an electronic distributor, and is often used in sign advertising and also in car ignition systems.

It receives its name for the way its flip flops are connected, i. e. Q outputs to J inputs and $\overline{Q}$ outputs to K inputs, until the last flip flop gets connected in this manner to the first flip flop.

The initial value of the count is set by a master reset which reaches the preset and prereset gates of the flip flops in use.



OPERATION

a) For the circuit shown above, the master reset line is connected to the preset gate of flip flop A and to the prereset gates of flip flops B, C and D. Consequently, after initializing, the state of the counter will be the following:

PULSE	D	C	B	A
MASTER RESET	0	0	0	1

b) Consider the logic level of the J and K inputs as a result of above flip flop states:

$J_A = 0$ and $K_A = 1$ (since FF D = 0)

$J_B = 1$ and $K_B = 0$ (since FF A = 1)

$J_C = 0$ and $K_C = 1$ (since FF B = 0)

$J_D = 0$ and $K_D = 1$ (since FF C = 0)

c) Add the first clock pulse (CP1) and observe how it affects the state of the flip flops.

FF A becomes 0 ($J_A = 0$, $K_A = 1$)

FF B becomes 1 ($J_B = 1$, $K_B = 0$)

FF C remains 0 ($J_C = 0$, $K_C = 1$)

FF D remains 0 ($J_D = 0$, $K_D = 1$)

d) Record the new state of the flip flops after CP1.

PULSE	D	C	B	A
MASTER RESET	0	0	0	1
CP1	0	0	1	0

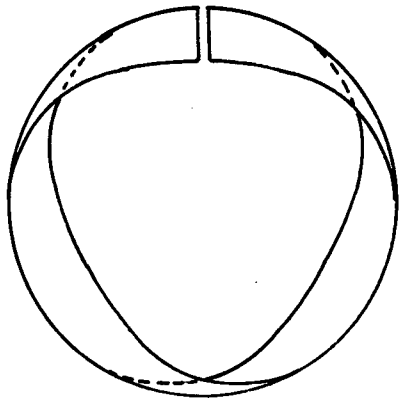
e) Repeat the procedure used in (a), (b), (c) and (d), until the initial conditions are repeated. The state table becomes:

PULSE	D	C	B	A
MASTER RESET	0	0	0	1
CP1	0	0	1	0
CP2	0	1	0	0
CP3	1	0	0	0
CP4	0	0	0	1

Above circuit may be assembled using two dual master slave flip flops like the 7476 and a variable frequency clock, so that above results may be verified at low frequencies. As the frequency increases, the light chasing effect will be created. Notice also that the light arrangements can be modified by reconnecting the master reset differently, for example, if we want three flip flops ON and one flip flop OFF, then the master reset could be connected to the preset inputs of flip flops B, C and D and to the prereset input of flip flop A, in which case the count sequence will be the following: 1110 / 1101 / 1011 / 0111

SWITCHED TAIL RING COUNTER

This counter is also known as the Mobius counter, for the similarity of the electric configuration to that of the Mobius Strip, shown below.

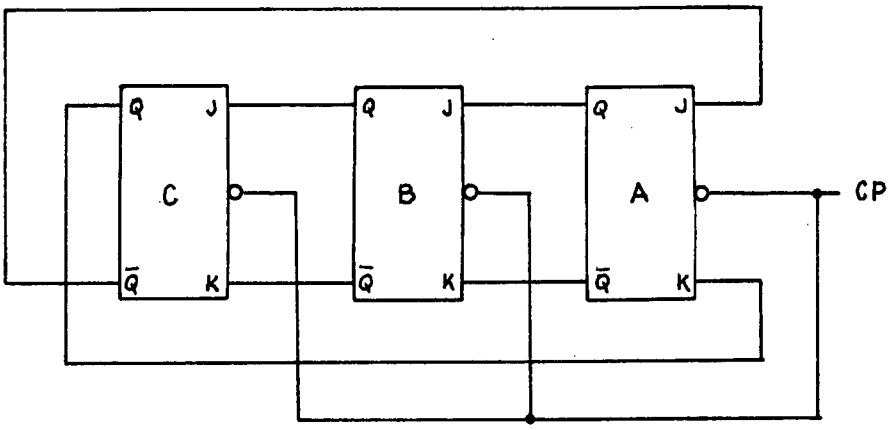


A CONTINUOUS LINE DRAWN FROM THE OUTSIDE WILL END UP IN THE INSIDE

In the Mobius counter, the Q outputs are connected to the J inputs and the $\overline{Q}$ outputs are connected to the K inputs as in the ring counter, except for the last flip flop where its Q output is connected to the K input of the first flip flop and its $\overline{Q}$ output is connected to the J input of said first flip flop.

This counter is often used to generate control and test patterns for transmission of data and is also used to drive the rear turning lights in some car models.

This circuit is shown next and may easily be assembled and tested, in order to corroborate its state table. The analysis procedure is the same outlined above.



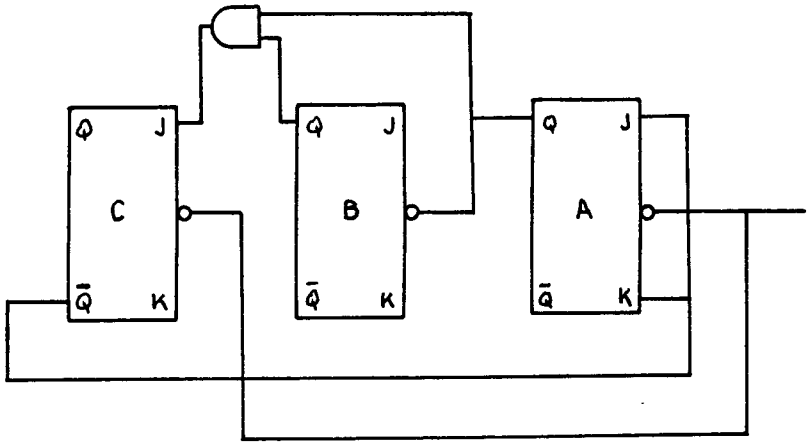
The state table for the Mobius counter is shown below.

PULSE	C	B	A
MASTER PULSE	0	0	0
CP1	0	0	1
CP2	0	1	1
CP3	1	1	1
CP4	1	1	0
CP5	1	0	0
CP6	0	0	0

FURTHER EXAMPLE OF SPECIAL COUNTS

a) For the counter shown below, determine the sequence of states that take place after a master reset pulse sets it to 000.

b) What happens if the counter is initially in state 110 or 111 for flip flops C, B and A respectively.



SOLUTION

a) Assuming that a master reset pulse will set A, B and C to zeroes, then the state table becomes the following. Notice that it is a binary counter that counts from 0 to 4.

PULSE	C	B	A
MASTER RESET	0	0	0
CP1	0	0	1
CP2	0	1	0
CP3	0	1	1
CP4	1	0	0
CP5	0	0	0

b) If the counter is initially in state 110 or 111, the state tables below show that the circuit will restore itself to its normal counting mode, i. e. the count becomes 010 or 011 respectively, after CP1.

PULSE	C	B	A
MASTER RESET	1	1	0
CP1	0	1	0

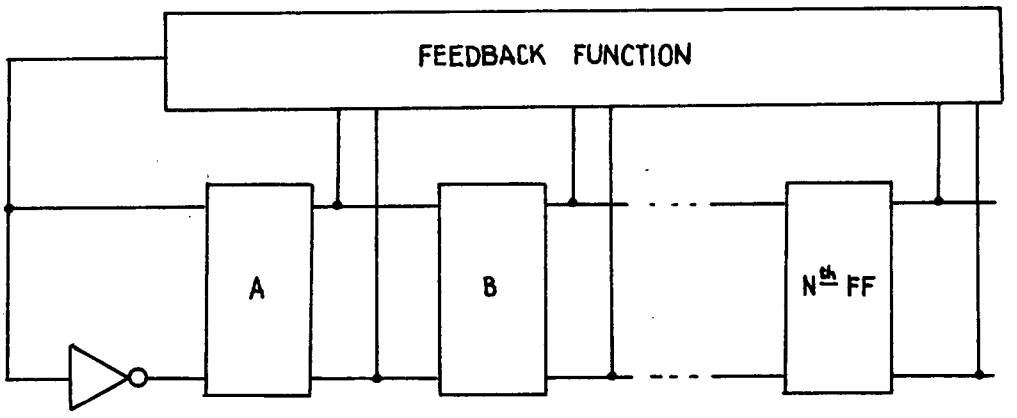
PULSE	C	B	A
MASTER RESET	1	1	1
CP1	0	1	1

8 SHIFT REGISTERS

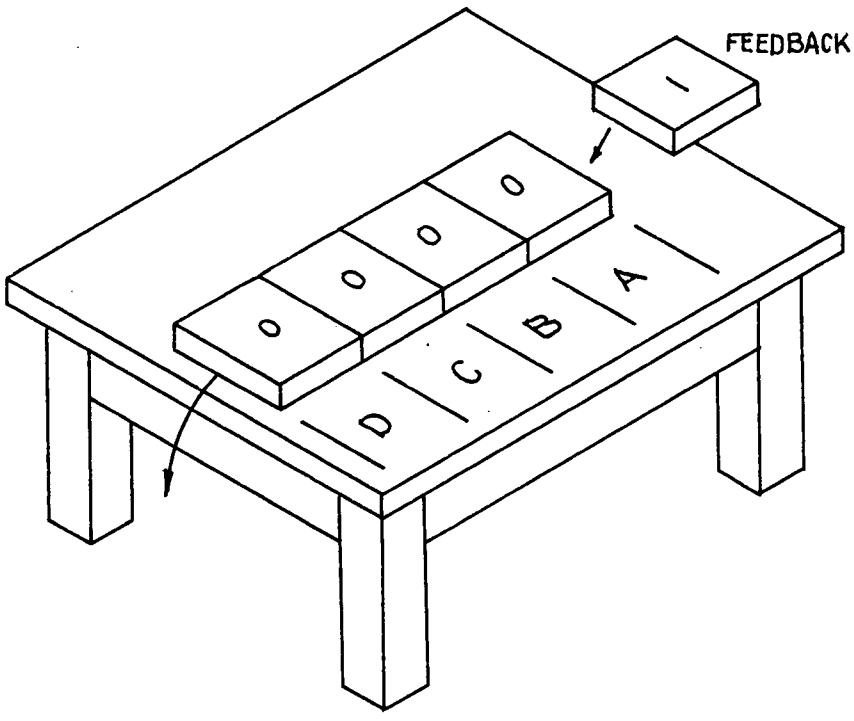
INTRODUCTION

Shift registers consist of cascaded flip flops. Clock pulses reach all these flip flops simultaneously. Each clock pulse causes the contents of a feedback function, a "0" or a "1", to be transferred into the first flip flop of the register; at the same time, the contents of the first flip flop are transferred to the second flip flop; the contents of the second flip flop are transferred to the third flip flop; and so on, until the last flip flop stores the contents of its previous flip flop.

Between clock pulses, the contents of each flip flop are combined to make up the new feedback function. See the following block diagram.



The above operation is similar to shifting domino bones on a table. Consider the following analogy for a four flip flop shift register. Each flip flop is assigned an area on the table marked A, B, C and D. See the next figure.



The state of each flip flop is determined by the single domino bone that occupies its area. The domino bones are marked either as a "0" or as a "1".

The feedback function is represented by new domino bones that can only be placed in the least significant bit position, i. e. FF A.

Since each flip flop area can store only one bone at a time, the new bones must push those already on the table, shifting them one position to the left, as shown in the above figure. This way, the bone in area A will now occupy the area B, that in area B is shifted to area C, that in area C is shifted to area D and that in area D gets removed altogether from the table.

The resulting count is displayed by the remaining bones.

POSSIBLE STATES OR COUNTS OF A REGISTER

The number of different states or counts that a register may contain at any one time is dependent on how many flip flops are there in the register. Including trivial cases, i. e. those situations where the shift register becomes locked in a loop, the number of different states is given

by the following expression:

$$1 \leq (\text{Number of different states}) \leq 2^n$$

In the above expression, n is the number of flip flops in the shift register. Examples:

a) A shift register with four flip flops has a maximum of 16 different states or counts.

b) A shift register with five flip flops has a maximum of 32 different states or counts.

STATE TABLES

State tables are used to list all the possible counts of a shift register. As an example, we will show the procedure used to tabulate the states of a four flip flop shift register.

It must be noted that the feedback functions can only be "1" or "0".

Assuming that the initial count is zero, i. e. 0000_2:

a) Adding a feedback function with zero value will not change the state of the count. Repeated use of this zero feedback will keep the shift register locked in a trivial loop.

b) Adding a feedback function with a value of ONE will change the state of the count to a 1, i. e. 0001_2, because:

FF A becomes 1 (due to the feedback function)

FF B remains 0 (i. e. the previous value of FF A)

FF C remains 0 (i. e. the previous value of FF B)

FF D remains 0 (i. e. the previous value of FF C)

When the count is ONE, i. e. 0001_2:

a) Adding a feedback function with zero value will change the state of the count to a 2, i. e. 0010_2, because:

FF A becomes 0 (due to the feedback function)

FF B becomes 1 (i. e. the previous value of FF A)

FF C remains 0 (i. e. the previous value of FF B)

FF D remains 0 (i. e. the previous value of FF C)

b) Adding a feedback function with a value of ONE, will change the state of the count to a 3, i. e. 0011_2, because:

FF A becomes 1 (due to the feedback function)

FF B becomes 1 (i. e. the previous value of FF A)

FF C remains 0 (i. e. the previous value of FF B)

FF D remains 0 (i. e. the previous value of FF C)

The remaining states are determined using this procedure. The table below lists all the 16 states with the feedback functions that produce them.

COUNT	D	C	B	A	FEEDBACK FUNCTION
0	0	0	0	0	"1"
1	0	0	0	1	"0" or "1"
2	0	0	1	0	"0" or "1"
3	0	0	1	1	
4	0	1	0	0	
6	0	1	1	0	"0" or "1"
5	0	1	0	1	
7	0	1	1	1	
8	1	0	0	0	
12	1	1	0	0	
10	1	0	1	0	
14	1	1	1	0	
9	1	0	0	1	
13	1	1	0	1	
11	1	0	1	1	
15	1	1	1	1	

STATE DIAGRAMS

For analysis and design purposes, it is useful to know the sequential order of the states or counts in a shift register.

When the state sequences are mapped on special graphs, they become known as State Diagrams. Once a State Diagram is completed, it becomes a useful reference to determine sequential counts at any time.

STATE DIAGRAM FOR ONE FLIP FLOP

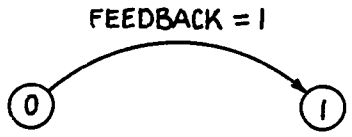
A single flip flop has two possible states or counts, i. e. a "0" or a "1". These two states are represented graphically by two nodes.

A feedback function, fed during a clock pulse, will produce the following results:

a) If the flip flop is in the "0" state, a ZERO feedback function will not alter its state. Thus, the flip flop remains in the "0" state. This is a trivial case and is represented by a closed loop around the node 0.

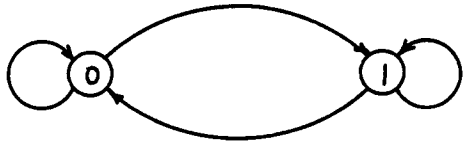
b) If the flip flop is in the "1" state, a ZERO feedback function will change it into the "0" state. This transition is represented by an arrow drawn from node 1 to node 0.

c) If the flip flop is in the "0" state, a ONE feedback function will set the flip flop into a "1". This transition is represented by an arrow drawn from node 0 to node 1.



d) If the flip flop is in the "1" state, a ONE feedback function will only keep the flip flop in the same "1" state. This is another trivial case and is represented by a closed loop around the node 1.

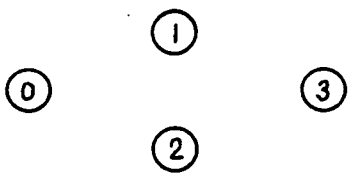
The complete State Diagram is the composite of the above four cases and is shown below.



STATE DIAGRAM FOR A TWO FLIP FLOP SHIFT REGISTER

When a shift register consists of two flip flops, A and B, it has four possible states or counts. Each of these counts is designated by a node.

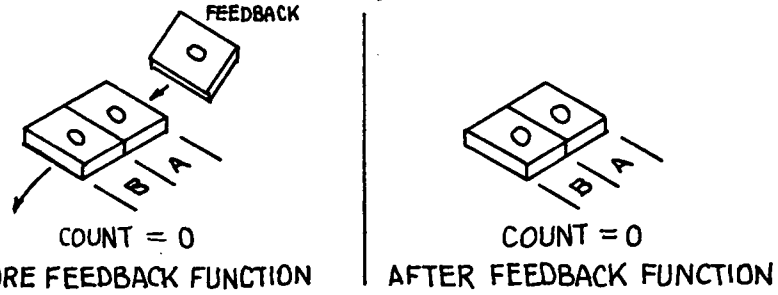
Node zero represents the count 00_2; node 1 represents the count 01_2; node 2 represents the count 10_2 and node 3 represents the count 11_2.



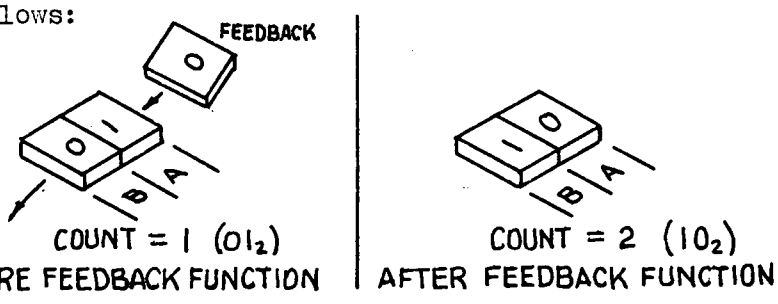
Feedback functions modify only the least significant bit of the shift register. Therefore, we will consider the effect of a feedback function when: a) the feedback is ZERO and b) when the feedback is ONE.

a) When the contents of the register are zero, a ZERO feedback

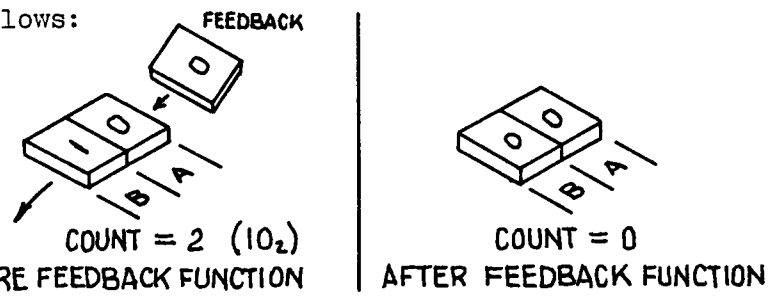
function will not alter the results. This can be seen readily when we use the domino analogy:



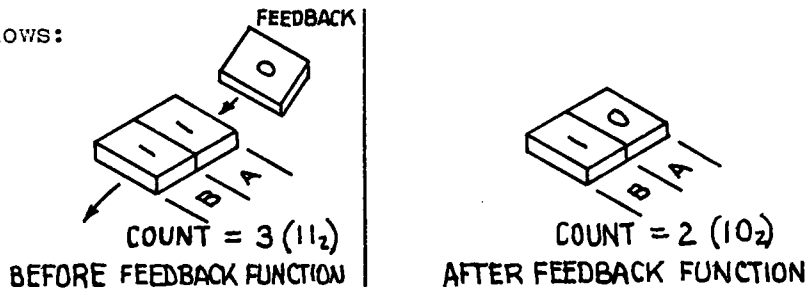
When the initial contents of the shift register have a count of "1", (01_2), then a ZERO feedback function will modify them as follows:



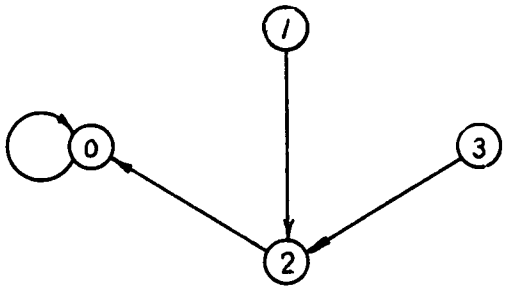
When the initial contents of the shift register have a count of "2", (10_2), then a ZERO feedback function will modify them as follows:



When the initial contents of the shift register have a count of "3", (11_2), then a ZERO feedback function will modify them as follows:

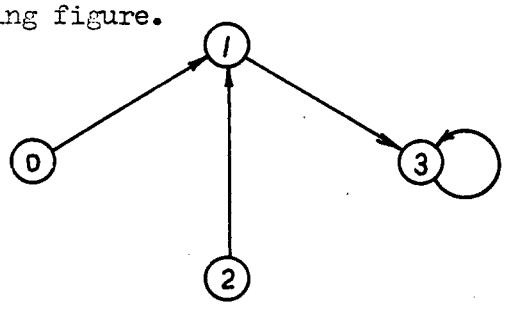


Above four conditions are summarized graphically below:

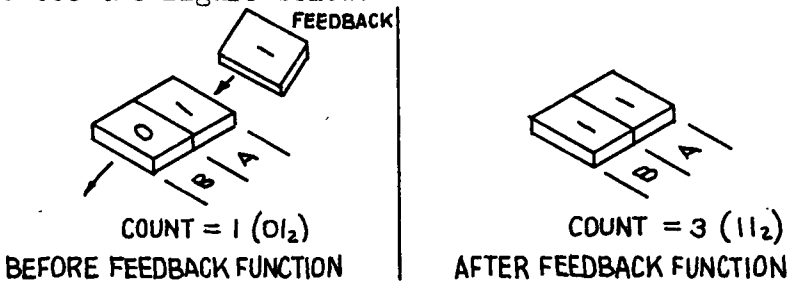


Notice that the arrows indicate the direction in which the transitions take place, when the feedback function is ZERO.

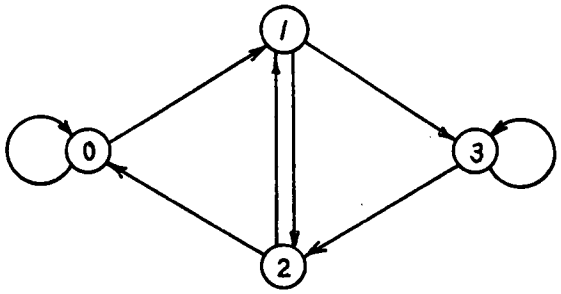
b) A feedback function equal to "1" will modify the contents of the same shift register, in the direction shown by the arrows in the following figure.



Notice that the same domino analogy may be applied to any individual case. For example, consider the case when the initial count is a "1", (01_2), and the feedback function is also a "1", then the only possible new count is a "3", that is: 11_2. See the figure below:

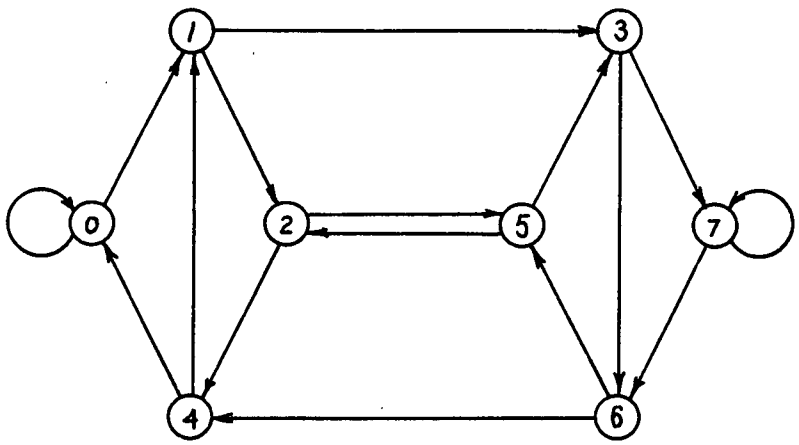


The complete state diagram is the composite of the above partial diagrams. See the next figure.



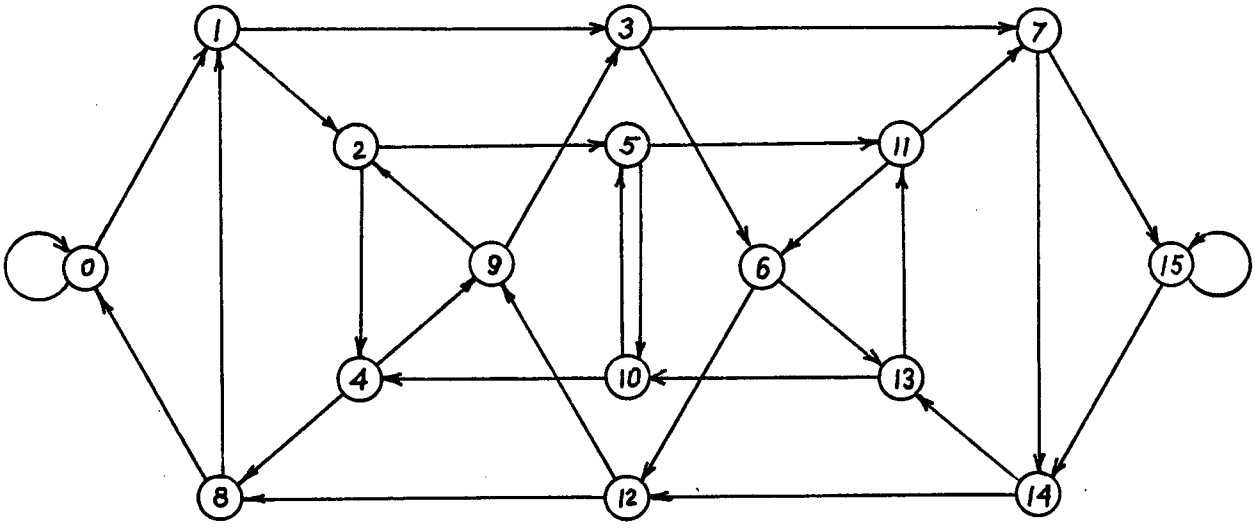
STATE DIAGRAM FOR A THREE FLIP FLOP SHIFT REGISTER

A shift register with three flip flops has eight possible states or counts. Nodes 0 to 7 are used to designate those counts. The possible transitions between counts due to a feedback function are indicated by arrows. The absence of arrows between two nodes indicates that no transition is possible between them.



STATE DIAGRAM FOR A FOUR FLIP FLOP SHIFT REGISTER

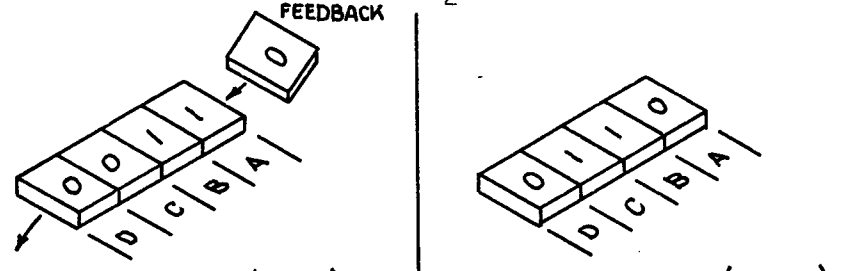
A shift register with four flip flops has sixteen possible states or counts. The possible transitions, due to feedback functions are shown in the state diagram below.



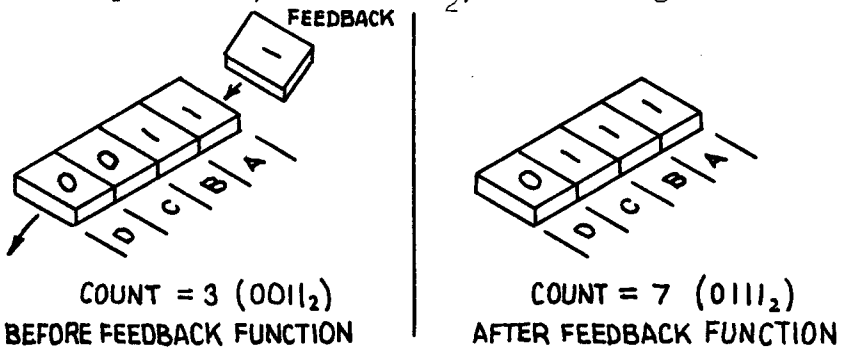
The above diagram shows nodes of all the possible counts, and it also indicates, with arrows, all the possible new counts available from each of those nodes.

The domino analogy may also be applied to any individual state shown in the above diagram. For example, consider the case when the initial count is a 3, i. e. 0011_2. The two possible new states or counts are dependent on whether the feedback function is: (a) ZERO; or (b) ONE.

a) When the feedback function is a "0", the only possible new count is equal to 6, i. e. 0110_2, see the figure below:



b) When the feedback function is a "1", the only possible new count ie equal to 7, i. e. 0111_2, see the figure below:



DESIGN OF A SHIFT REGISTER

Shift registers are used to transmit information in accordance to specified sequences. Thus, the desired sequence determines the size and configuration of the shift register as well as that of its feedback logics.

The design procedure, based on a feasible count sequence, is summarized below:

1.- Use the appropriate State Diagram or any of its portions.

2.- Construct a table with the desired count sequences. Refer to the state diagram, to make sure that the count sequences are feasible.

3.- For each of the counts listed in the table of part (2), determine the value of the feedback function that will produce the next state. List those values of feedback functions in an extra column.

4.- Synthesize the feedback function from the values listed in the feedback column.

5.- Simplify the feedback function, by the use of Karnaugh Maps.

6.- Implement the logical diagram.

EXAMPLE 1

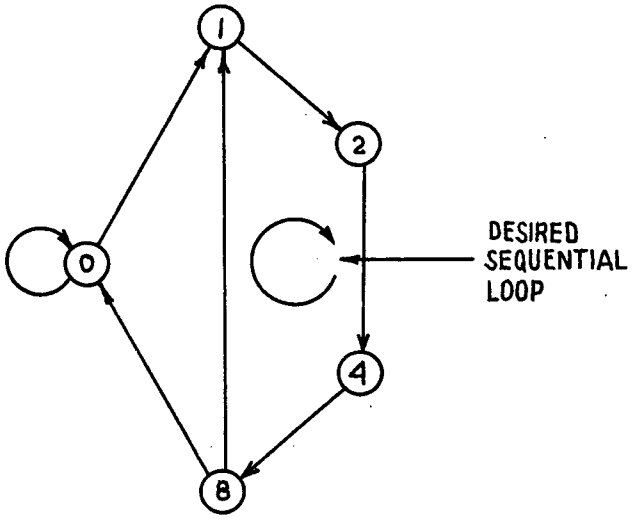
Design a shift register to produce the following sequential counts:

0, 1, 2, 4, 8, 1, etc.

Notice that the implemented circuit will have commutating characteristics, of the type used in light chasing effects.

SOLUTION

1.- The shift register must contain four flip flops, because the requested maximum count is an eight, that is, 1000_2. Notice that the above sequence is part of the state diagram for a four flip flop shift register. The partial diagram is shown below.



2.- Build up a table containing the desired sequential counts, and assign corresponding values to each of the four flip flops.

COUNT STATES	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
4	0	1	0	0
8	1	0	0	0
1	0	0	0	1

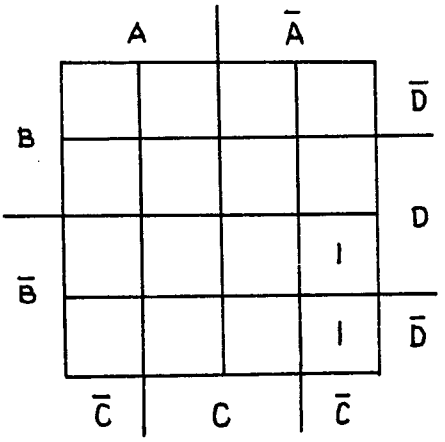
3.- List the required feedback functions on an extra column. These are the functions that will step any count into its following state.

COUNT STATES	D	C	B	A	FEEDBACK FUNCTION
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
4	0	1	0	0	0
8	1	0	0	0	1
1	0	0	0	1	

4.- Synthesize the feedback function from its corresponding column. The rows where this function is true are "added" in the following Boolean Algebra Expression.

$$f = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D$$

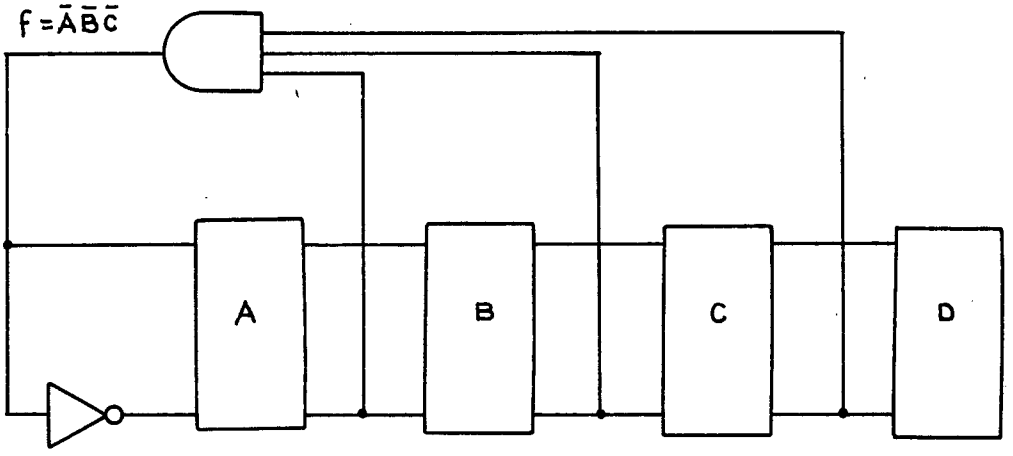
5.- Simplify the above expression, by using Karnaugh maps:



The simplified feedback function becomes:

$$f = \bar{A}\,\bar{B}\,\bar{C}$$

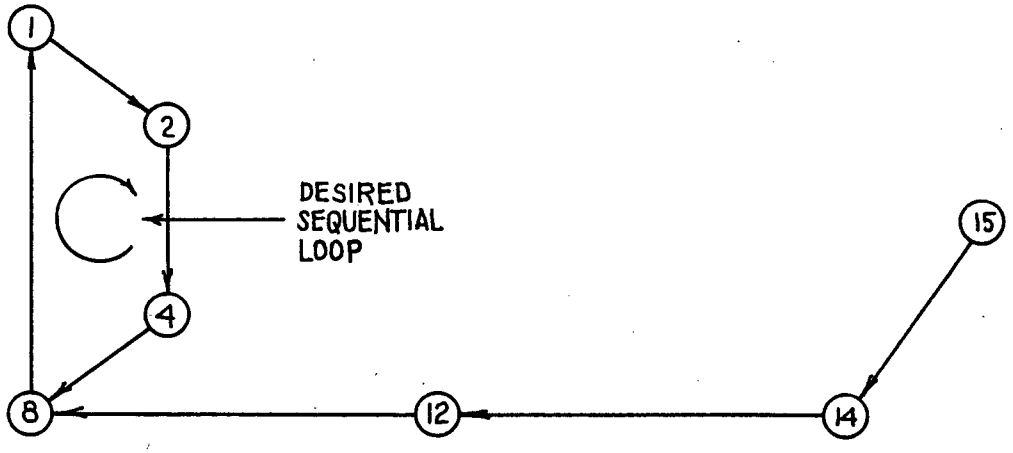
6.- The implemented logical diagram is the following:



When the above circuit is first energized, a random condition may appear on each of its flip flops. Assuming that the shift register is initially set to ONE's, it can be seen that after a few clock pulses, the sequential count is eventually restored to its intended sequential loop. This is shown in the following truth table, where a master reset pulse produces the initial count of 15. Columns $\bar{A}$, $\bar{B}$ and $\bar{C}$ are used to derive the feedback functions (f-column), which determine the state of the new count, every time a clock pulse is received.

CLOCK PULSE	COUNT	D	C	B	A	$\overline{A}$	$\overline{B}$	$\overline{C}$	$f = \overline{A}\,\overline{B}\,\overline{C}$
MASTER RESET	15	1	1	1	1	0	0	0	0
CP 1	14	1	1	1	0	1	0	0	0
CP 2	12	1	1	0	0	1	1	0	0
CP 3	8	1	0	0	0	1	1	1	1
CP 4	1	0	0	0	1	1	1	0	0
ETC.									

Notice that the above count follows a portion of the four flip flop state diagram, as shown below, and then it restores itself to the desired sequential loop.



It may also be corroborated, by following the above procedure, that this circuit always restores itself to its intended mode of operation, regardless of the value of the initial count (0 to 15). Therefore, a master reset pulse is not required.

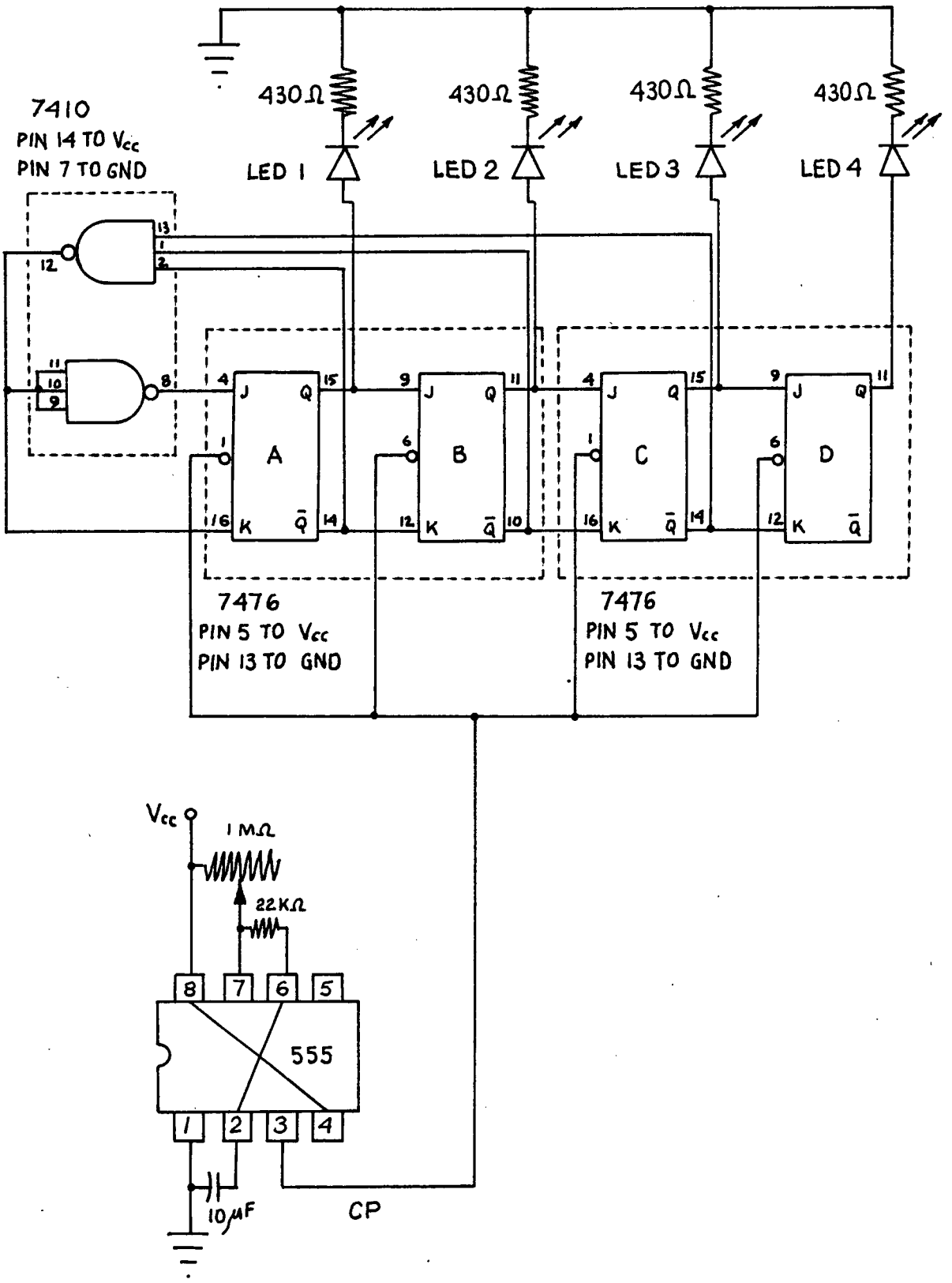
The above logical diagram may be assembled and tested by using the following components:

Two dual master slave flip flops 7476

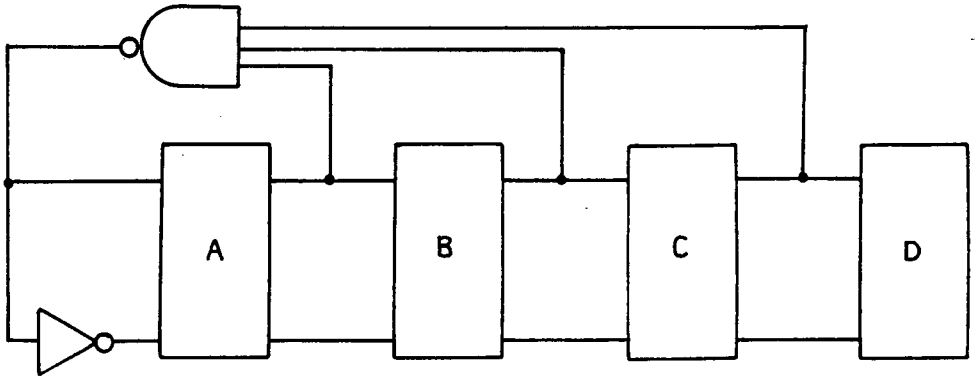
One triple 3-input NAND gate to be used as an AND gate as well as an inverter.

One 555 timer to produce the clock pulses.

See the next figure.


7410
PIN 14 TO Vcc
PIN 7 TO GND
430Ω
430Ω
430Ω
430Ω
LED 1
LED 2
LED 3
LED 4
A
B
C
D
7476
PIN 5 TO Vcc
PIN 13 TO GND
7476
PIN 5 TO Vcc
PIN 13 TO GND
Vcc
1 MΩ
22KΩ
555
10μF
CP

The previous circuit may be modified so that the Q lines feed the feedback function. The "AND" gate is changed for a"NAND"gate to prevent locking the shift register into the trivial modulo 1 state, i. e. 0000.



The table that describes the states of the count is:

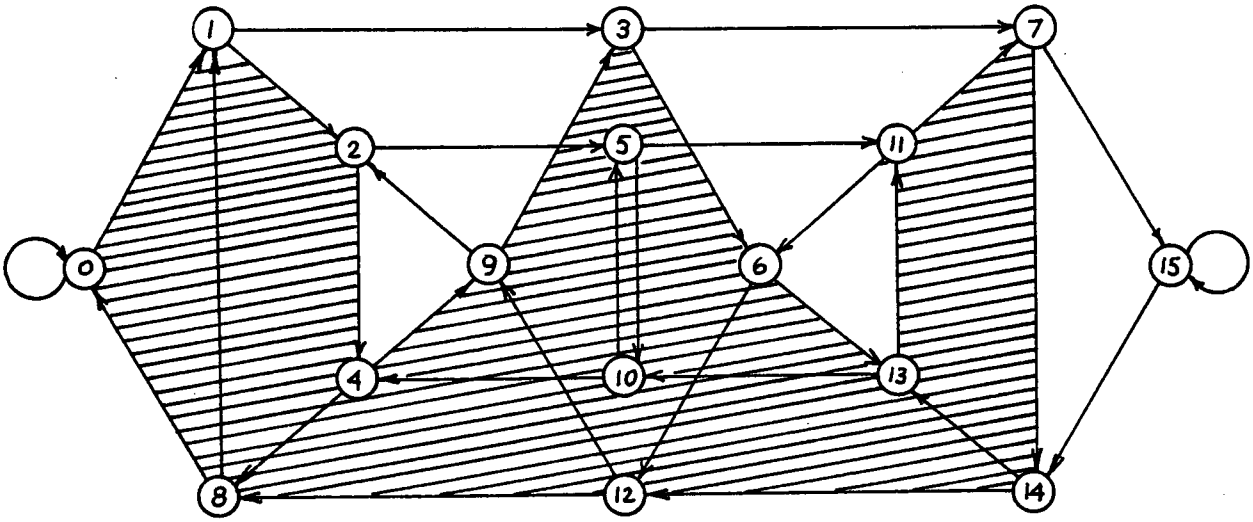
PULSE	D	C	B	A
MASTER RESET	0	0	0	0
CP1	0	0	0	1
CP2	0	0	1	1
CP3	0	1	1	1
CP4	1	1	1	0
CP5	1	1	0	1
CP6	1	0	1	1
CP7	0	1	1	1

This circuit does not require a master reset pulse. If the Q outputs get connected to LED's, it produces a pattern where a no-light seems to chase three lights.

EXAMPLE 2

Using the shaded portion of the state diagram shown below, design a shift register that will assume all those indicated states, that is:

0, 1, 2, 4, 9, 3, 6, 13, 11, 7, 14, 12, 8, 0



Above count has thirteen different states, i. e. a modulo 13. The circuit therefore must use four flip flops.

SOLUTION

1.- The State Diagram has already been provided.

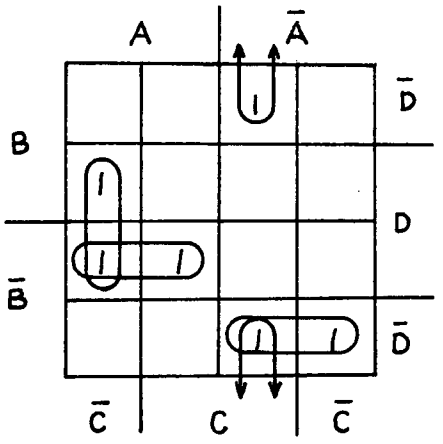
2 & 3.- The states of the count and their respective feedback functions are listed below:

COUNT STATES	D	C	B	A	FEEDBACK FUNCTION
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
4	0	1	0	0	1
9	1	0	0	1	1
3	0	0	1	1	0
6	0	1	1	0	1
13	1	1	0	1	1
11	1	0	1	1	1
7	0	1	1	1	0
14	1	1	1	0	0
12	1	1	0	0	0
8	1	0	0	0	0
0	0	0	0	0	

4.- In terms of Boolean algebra, the feedback function is synthesized as follows:

$$f = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\,\overline{D} + A\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\,C\,\overline{D} + A\,\overline{B}\,C\,D + A\,B\,\overline{C}\,D$$

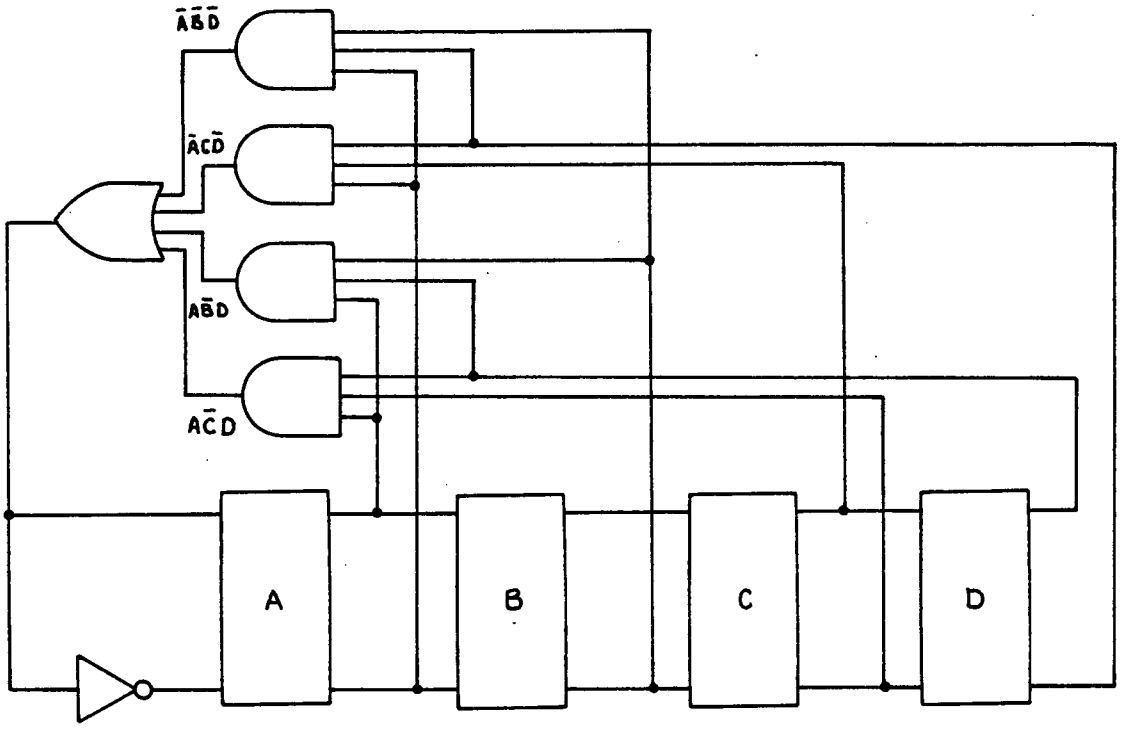
5.- Simplification by means of Karnaugh maps yields:



Therefore, the feedback function becomes:

$$f = A\,\bar{C}\,D + A\,\bar{B}\,D + \bar{A}\,C\,\bar{D} + \bar{A}\,\bar{B}\,\bar{D}$$

6.- The implemented circuit is shown below.



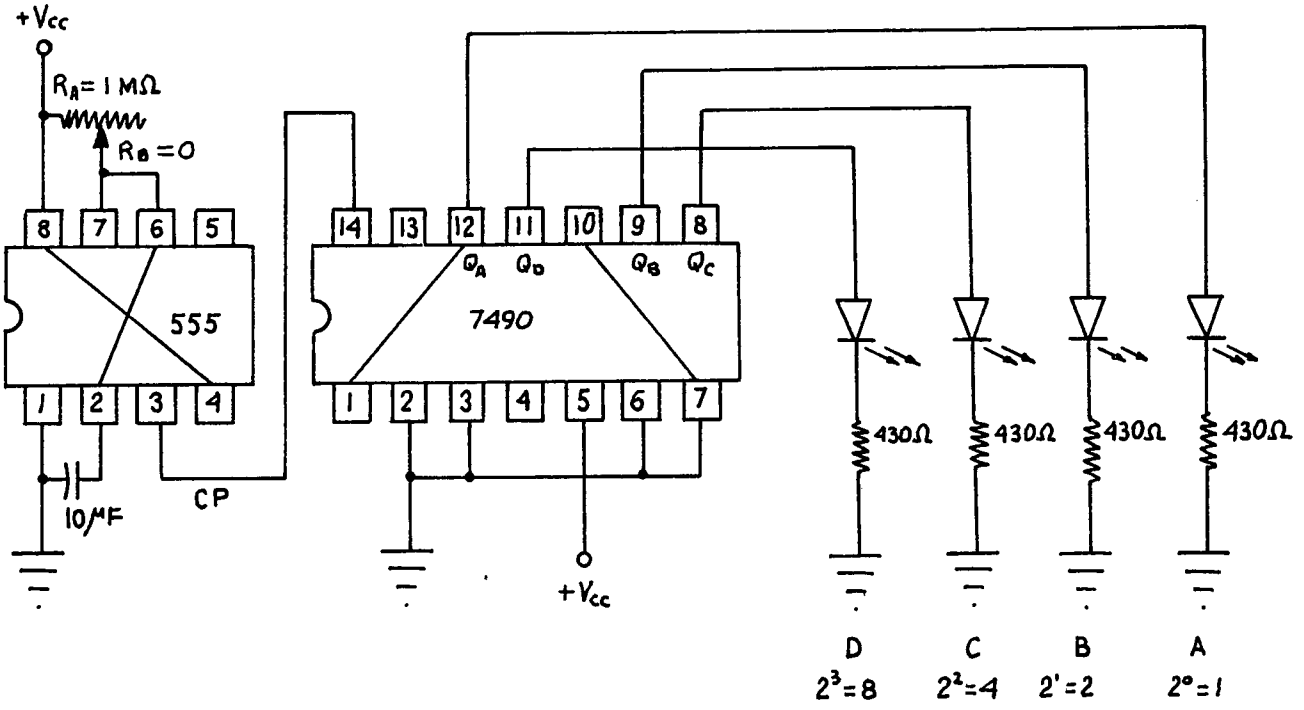
Visual displays are commonly used to retrieve information from electronic systems. Electronic digital displays are mostly made with incandescent lamps, nixie tubes, neon lamps, light emitting diodes (LED), liquid crystal displays (LCD) and cathode ray tube displays (CRT).

In this section, only light emitting diodes are considered, since their application mode is general to all the displays listed above.

BINARY WEIGHTED LED INDICATORS (8, 4, 2, 1)

As previously mentioned, the logical state of a circuit, HI or LO, can be known by using light emitting diodes as indicators.

For a BCD decade counter, the following arrangement was used to display the state of the count. These LED indicators are used in the binary coded weight mode, i. e. 8, 4, 2 and 1. In order to read the count, one must interpret the indicated weights.



DECIMAL WEIGHTED DISPLAY (9, 8, 7, 6, 5, 4, 3, 2, 1, 0)

These circuits save us the effort to interpret the binary coded weights. The output consists of 10 light emitting diodes where each is weighted in our familiar decimal number system.

The translation of results from a binary coded weight system into the decimal number system is done by using a 4-LINE-TO-10-LINE DECODER, such as the 7442 integrated circuit, see attached technical specifications.

The previous circuit can be modified if we add a 7442. The required ten light emitting diodes will be used to indicate the state of the count. Notice that the 7442 integrated circuit sinks the current from the LED indicators, therefore, the light emitting diodes must be connected in the common anode configuration to $+V_{cc}$.

The resulting circuit may be used as an electronic roulette wheel.

OPERATION AS A ROULETTE WHEEL

The frequency of oscillation in the clock of this circuit can be varied by varying the one megohm potentiometer, i. e. R_A. Notice that the clock pulse is only indicated in the next figure, but its oscillator is the same one used in the previous display.

As the resistance R_A is decreased, the frequency of oscillation increases. See how this takes place graphically, referring to the nomogram for the 555 timer in the astable multivibrator mode, or simply consider the design equation below, where $R_B = 0$ and $C = 10\mu F$.

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

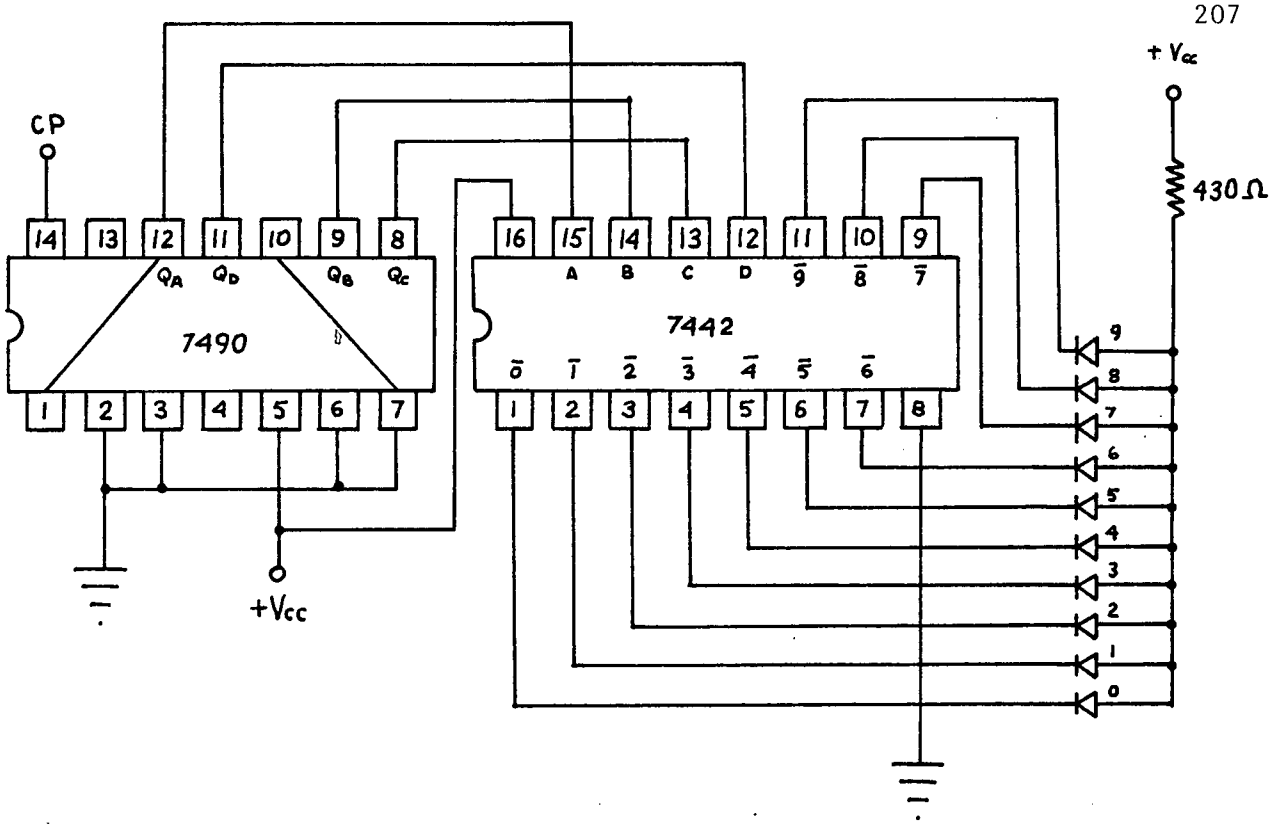
Notice that if R_A becomes less than 1 kΩ, then the circuit reaches an unstable region, as seen in the nomogram, to the right side of the 1 kΩ line. If R_A is decreased further, the circuit will stop oscillating. This condition can happen when R_A is close to 100 ohms.

When the oscillation stops, there are no more clock pulses to trigger the counter. Without triggering pulses, the counter stops, retaining the count from the last clock pulse.

The oscillation stops at any random count, because prior to it, the oscillator is operating in an unstable region and the frequency is high enough to make the LED indicators of the count appear as if they were all lit.

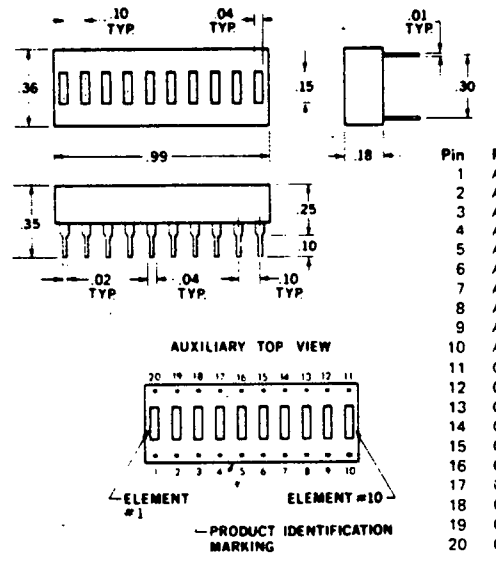
Above count may be any number from 0 to 9, and the display will show one light to be lit out of ten.

The display light emitting diodes may be arranged in a circular pattern and light emitting diodes of different colours may be used.



Instead of individual light emitting diodes, a package may be used, where all the light emitting diodes are assembled inside of a single unit. An example of these packages is found in the RBG-/OBG-/GBG-/YBG-1000. The first letter indicates the colour of the light emitting diodes i. e. red/orange/green/yellow. The pin identifications are included below.

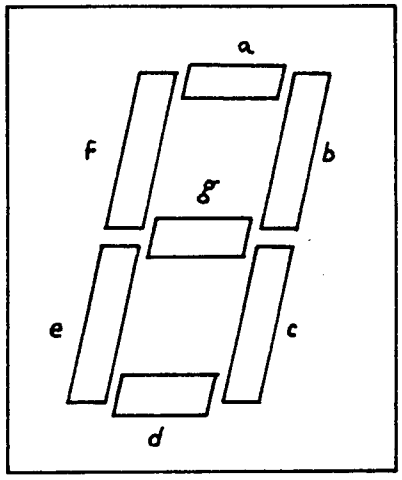
RBG-/OBG-/GBG-/YBG-1000 97



Pin	Function
1	Anode 1
2	Anode 2
3	Anode 3
4	Anode 4
5	Anode 5
6	Anode 6
7	Anode 7
8	Anode 8
9	Anode 9
10	Anode 10
11	Cathode 10
12	Cathode 9
13	Cathode 8
14	Cathode 7
15	Cathode 6
16	Cathode 5
17	Cathode 4
18	Cathode 3
19	Cathode 2
20	Cathode 1

SEVEN SEGMENT DISPLAYS

A numerical display is easier to read than any of the two previously discussed displays. The output consists of seven light emitting diodes arranged to look like a number 8, and each diode is labelled with letters "a" to "g" as shown below.

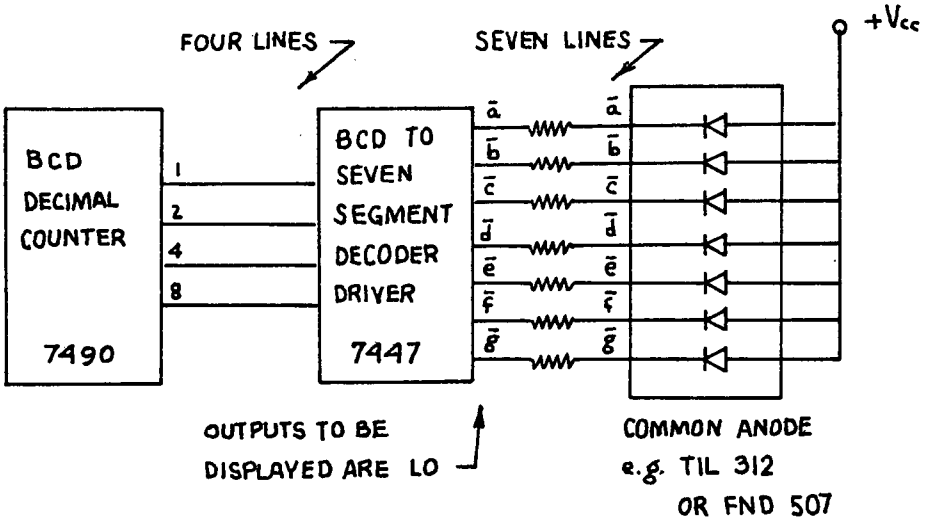


Notice that the display can still be interpreted properly if segment "d" happens to be disconnected or inoperative.

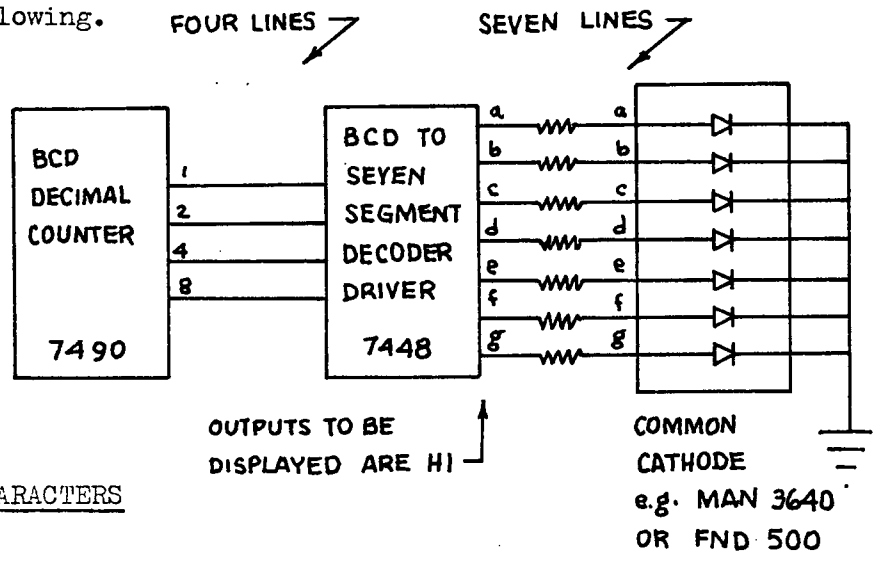
The translation of results from a binary coded weight system into a seven segment system is done by using a BCD-TO-SEVEN-SEGMENT DECODER/DRIVER, such as the 7447 integrated circuit, or the 7448 integrated circuit, see attached technical specifications.

Notice that the 7447 "sinks" the current from the elements of the seven segment display that need to be energized. This type of decoder/driver requires a COMMON ANODE SEVEN-SEGMENT DISPLAY, such as the TIL 312 from Texas Instruments, or the FND 507 from Fairchild.

For the counter discussed above, its block diagram using a 7447 and a common anode seven segment display, is the following.



A decoder/driver, such as the 7448 can also be used. It must be noticed that this 7448 integrated circuit "sources" current to the elements of the seven segment display that need energizing. Therefore, this type of decoder/driver requires a COMMON CATHODE SEVEN-SEGMENT DISPLAY, such as the MAN 3640 from Monsanto or the FND 500 from Fairchild. The corresponding block diagram for the counter in question is the following.

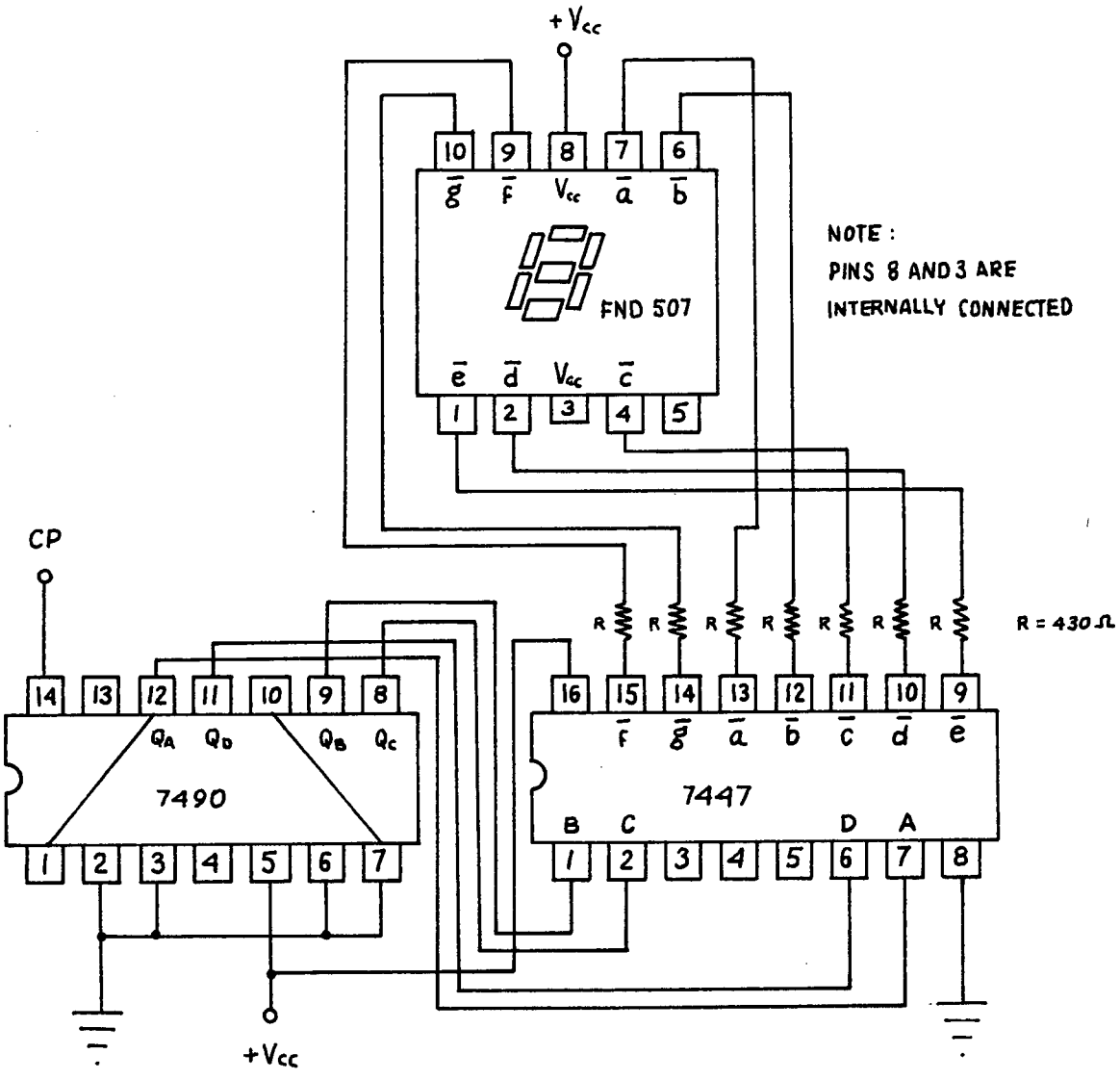


SPECIAL CHARACTERS

Special characters include plus sings, left decimal point, right decimal point, asterisks, semicolons and others needed for special type of applications.

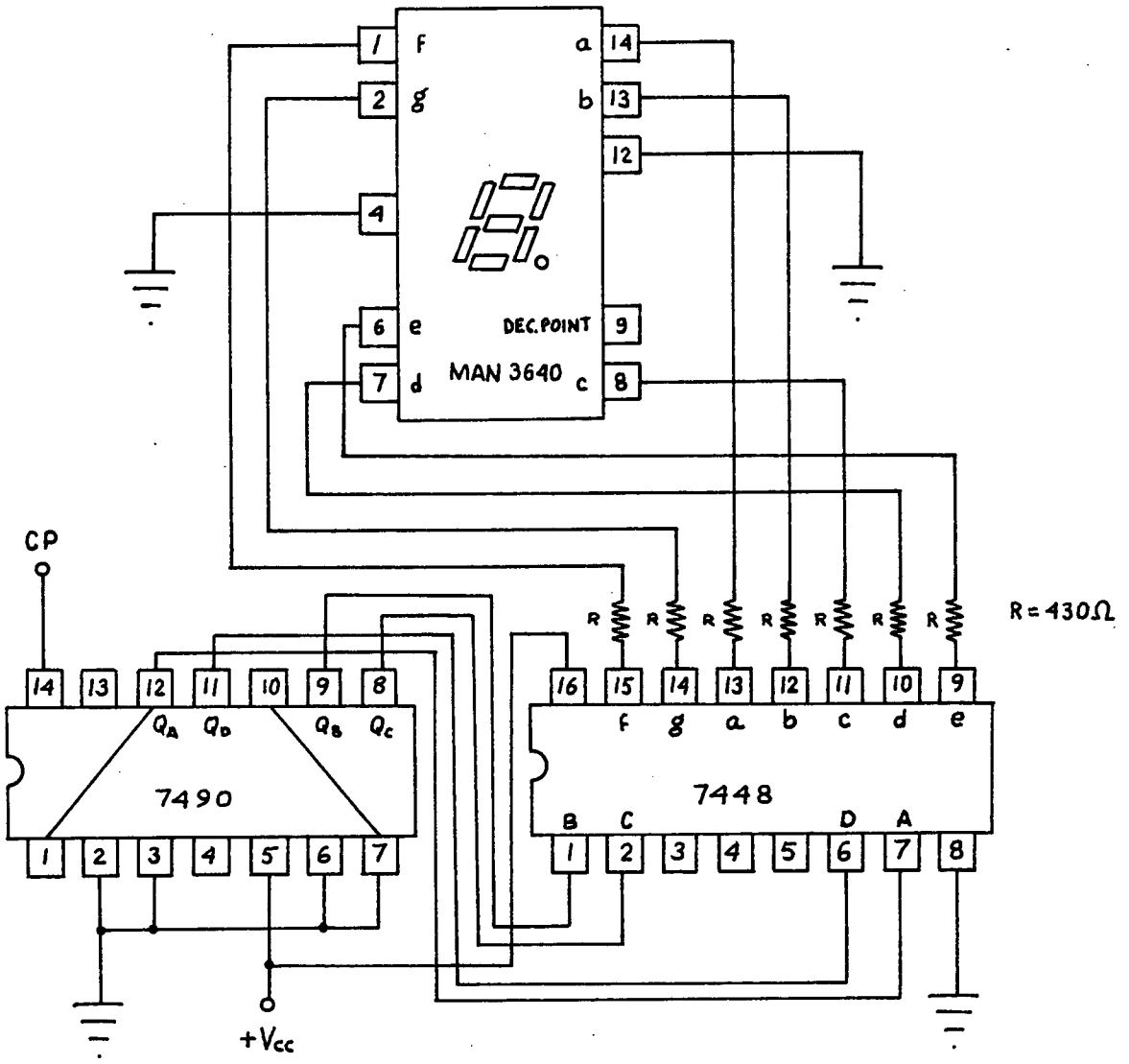
These special character displays and their corresponding connections are supplied by the different manufacturers. Their mode of operation is the same as for a numeric seven segment display.

The following circuit may be assembled to test the characteristics of a common anode display and its driver.



DIGITAL COUNTER USING COMMON CATHODE DISPLAY

The following circuit may be assembled to test the characteristics of a common cathode display and its driver.



10 THE OPERATIONAL AMPLIFIER

The operational amplifier is one of the most widely used and useful electronic components of control technology.

Some of its applications are listed below.

a) Summing amplifiers

b) Comparators

c) Active Filters

d) Waveshaping circuits

e) Audio Amplifiers and Mixers

As a summing amplifier, it permits equivalent voltage levels to be obtained from binary weighted outputs. When binary data from a computer or any other electronic system is converted into equivalent voltage levels, the resulting control applications are numerous. Some of these applications include switch activation of ovens and temperature regulating systems, speed control of motors, brightness controls in illumination, direction finders in radio, tracking mechanisms in satellites and missiles, computer simulation systems, such as aircraft training devices, etc.

As a comparator, the operational amplifier makes it possible to compare two voltages and then to determine which one is larger. With this feature, the contents of an up or down binary counter may be compared to external voltage sources, so that the state of the count can be stopped whenever a match occurs. This is the basic principle of Analog to Digital Converters (ADC), of which the digital voltmeter is an example. Its application in Real Time Computers, to make decisions while industrial processes are taking place, makes them extremely important.

Operational amplifiers are used in the design of active filters. Active filters are used to reproduce sound and video from a set of short duration pulses. This mode of transmission is known as Pulse Code Modulation (PCM) and is becoming increasingly important due to present technical innovations, such as the use of fiber optics in transmission systems.

In pulse code modulation, sound information is sent as a sequence of pulses, each with different binary coded value. At the receiver end, the active filter restores the continuous nature to those signals before reproduction takes place on a loudspeaker.

Present users of PCM are telephone companies, aircraft, and systems where a bulky number of cables can be greatly reduced.

The operational amplifier, used as a waveshaping circuit, is briefly discussed in this section, although this application mode is not digital. Waveshaping circuits are used in the transmission and reception of TV non-digital signals. These circuits were also used in the now outdated analog computer systems.

The operational amplifier is also used as an Audio Amplifier and Mixer. In this mode it sums or adds different sound tracks and produces a single channel. This operation mode is not digital but shows the great versatility of the device.

GENERAL CONSIDERATIONS

The fundamental requirements for an operational amplifier are: extremely high open loop voltage gain and also high open loop current gain.

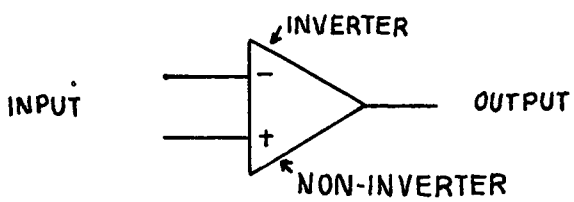
Open loop voltage gains can run from 40,000 to 250,000 volts/volt depending upon the price tag of the component, and current gains of 50,000 amps/amp are not uncommon.

The magnitude of the output voltage and output current is usually in the order of $\pm$ 20 V, and $\pm$ 25 mA respectively.

The flexibility and usefulness of the amplifier comes from the fact that by choosing the correct feedback and input components, the amplifier can be made to operate with almost any transfer function that can be conceived. It is from this fact that the amplifier derives its descriptive name of "operational".

Most of the amplifiers available in industry have two inputs, one is the inverting input, labelled "-" or "I", which means that the polarity of the input voltage is inverted at the amplifier output, and the other, the non-inverting input, labelled "+" or "NI", which means that the polarity of the input voltage is not inverted at the output.

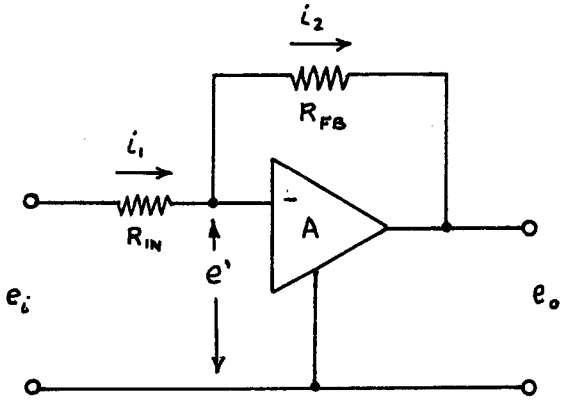
Its logic symbol is shown below. Notice that the inputs may be labelled "-" and "+", or "I" and "NI" respectively.



Voltage gain is designated by the letter A_v, or simply A, and is given in volts/volt. Current gain is designated by the letter A_i and is given in amperes/amp.

BASIC CIRCUIT CONFIGURATION

The circuit below shows input resistor R_{in} and feedback resistor R_{fb} connected to an operational amplifier.



Voltages and currents are designated as follows:

e_i = input voltage

e' = voltage at the inverting input

e_o = output voltage

i_1 = input current

i_2 = feedback current

By Ohm's law, the input current becomes:

$$i_1 = \frac{e_i - e'}{R_{in}}$$

Since this circuit inverts and amplifies the input signal by a factor A, then the output voltage is:

$$e_o = -e' A$$

By Ohm's law, the current in the feedback circuit will be given by:

$$i_2 = \frac{e' - e_o}{R_{fb}}$$

If we consider the fact that the current gain of the actual amplifier is in the order of 20,000 to 50,000 amps/amp, then the drain of current into the inverter input can be ignored, therefore:

$$i_1 = i_2$$

Substituting the previous equations for i_1 and i_2,

$$i_1 = \frac{e_i - e'}{R_{in}} = \frac{e' - e_o}{R_{fb}} = i_2$$

Since the working range of e_o can be between $\pm$ 20 V and the amplifier may have a voltage gain of 100,000 volts/volt, then e' will have the following magnitude:

$$e' = \frac{e_o}{A} = \frac{20}{100,000} = 0.2 \text{ mV}$$

From above result, it is assumed that e' is approximately zero, that is, it is a virtual ground. This assumption permits us to ignore the value of e' from the previous expression, therefore:

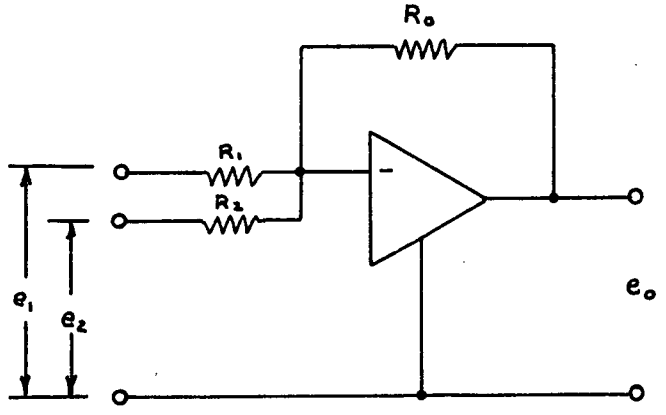
$$\frac{e_i}{R_{in}} = \frac{-e_o}{R_{fb}}$$

Above yields the final expression:

$$e_o = - e_i \frac{R_{fb}}{R_{in}}$$

SUMMING AMPLIFIER

As a summing amplifier, the operational circuit adds the value of incomming inputs. This is easily seen from the circuit below and the considerations outlined with it.



If e_{o1} denotes the output due to input e_1 only, then, using the expression derived for the operational amplifier,

$$e_{o1} = - \frac{R_o}{R_1} e_1$$

Also, if e_{o2} denotes the output due to input e_2 only,

$$e_{o2} = - \frac{R_o}{R_2} e_2$$

The output voltage e_o is the sum of above two voltages, therefore:

$$e_o = e_{o1} + e_{o2} = -\left(\frac{R_o}{R_1} e_1 + \frac{R_o}{R_2} e_2 \right) = - R_o \left(\frac{e_1}{R_1} + \frac{e_2}{R_2} \right)$$

If we now make $R_1 = R_2 = R_o = R$, then:

$$e_o = - (e_1 + e_2)$$

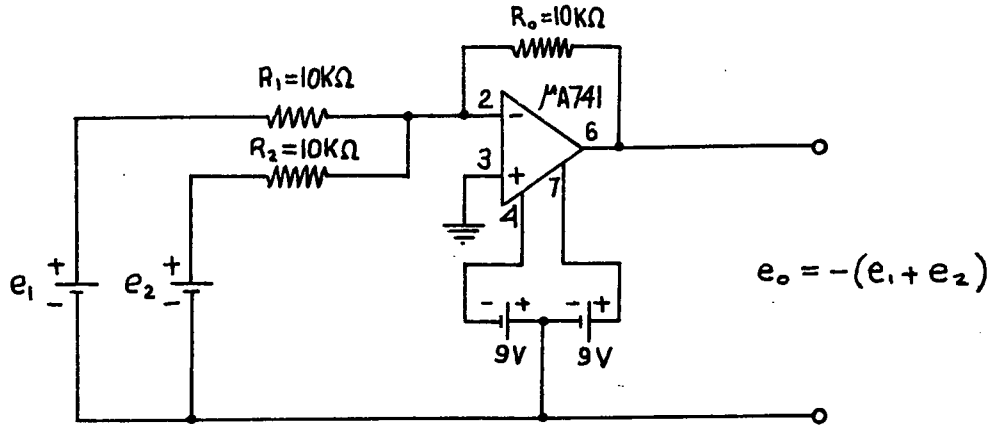
This last expression shows that the amplifier output is the sum of the input voltages, and that the amplifier acts as an adder of voltages.

Notice that if the input voltages have opposite polarities, e. g. $e_1 > 0$ and $e_2 < 0$, then, the output voltage expression becomes:

$$e_o = -(e_1 - e_2)$$

and the amplifier then acts as a subtractor.

The following summing amplifier may be assembled. Its operation may be verified for different values of e_1 and e_2. The circuit uses a μA741 operational amplifier. The technical data for this integrated circuit has been included at the end of this section.



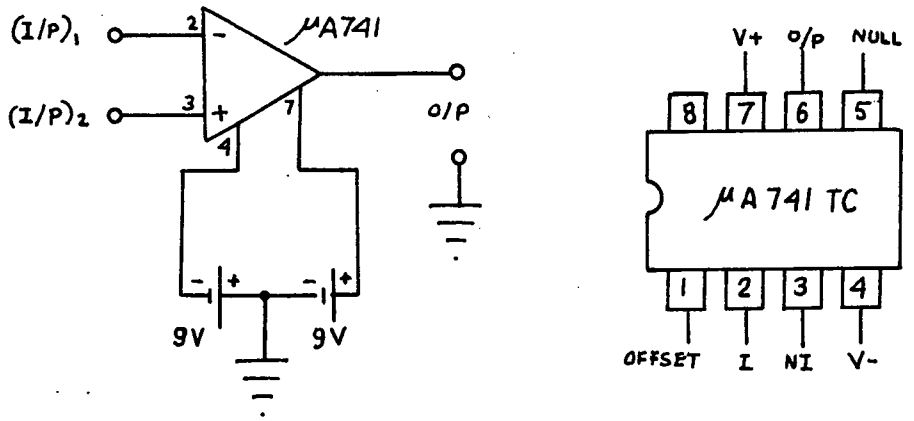
Two 9 V radio batteries provide the supply voltage for the operational amplifier. The magnitude of this supply voltage determines the maximum voltage range available for summing actions. This means that the summing amplifier equation: $e_o = -(e_1 + e_2)$, will be satisfied only if the sum of the input voltages does not exceed the value available from the supply, i.e. only if: $|e_1 + e_2| \leq 9$ V

In order to use the above circuit as a subtractor, simply invert the polarity of the input that needs to be subtracted.

NOTE.- There are no loop currents between input sources, i. e. between branch e_1, R_1 and branch e_2, R_2, because the input to the operational amplifier (pin 2) is a virtual ground.

COMPARATORS

The basic circuit configuration of a comparator is given in the next figure. It uses a μA741 integrated circuit. The supply voltage was provided with two 9 V batteries, of the type available for transistor radios. The pin connections shown are those recommended for this particular device, see drawing of pin connections on the right, as well as the attached tachnical data.



PRINCIPLE OF OPERATION

If the input voltage $(I/P)_1$ into the inverter section is greater than the input voltage $(I/P)_2$ into the non-inverter section, then the output is negative.

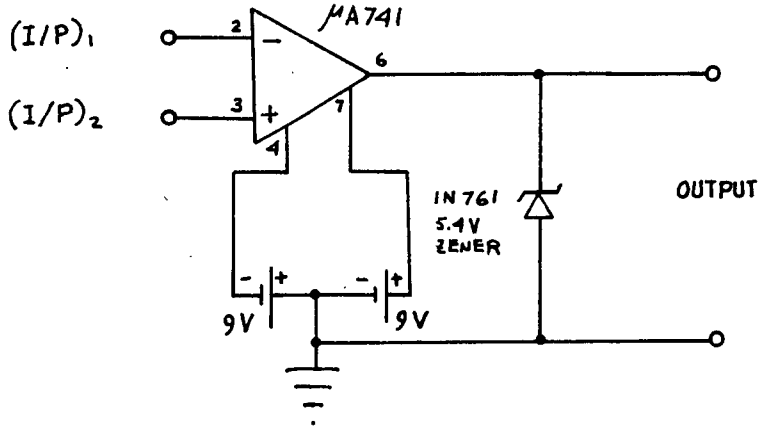
If the input voltage $(I/P)_2$ into the non-inverter section is greater than the input voltage $(I/P)_1$ into the inverter section, then the output is positive.

Above can be summarized in the following table:

INPUT CONDITION	OUTPUT
$(I/P)_1 > (I/P)_2$	- 9 V
$(I/P)_2 > (I/P)_1$	+ 9 V

Notice that the available output is proportional to the supply voltage. According to the included technical specifications for the μA741, the supply voltage may not exceed a maximum of ± 18 V.

In digital circuits, the recommended logical voltage levels are in the order of + 5 V. Therefore, above output voltages must be limited in order to conform to digital requirements. This is accomplished below, by connecting a semiconductor zener diode across the output terminals. The zener diode shown below is a 1N761, and it limits the output voltage between -0.7 V to a maximum value of + 5.4 V.



Using above circuit with its limiting device, gives a table of values that can be summarized as follows:

INPUT CONDITION	OUTPUT WITH ZENER
$(I/P)_1 > (I/P)_2$	- 0.7 V
$(I/P)_2 > (I/P)_1$	+ 5.2 V

NOTE.- A comparator is a very sensitive circuit and cannot determine a balance condition. Therefore, when connected as shown above, it will produce a HI or a LO at anyone time.

The following readings, measured with a volt-ohmmeter, conform to the previous table. Above circuit may be assembled to corroborate these results.

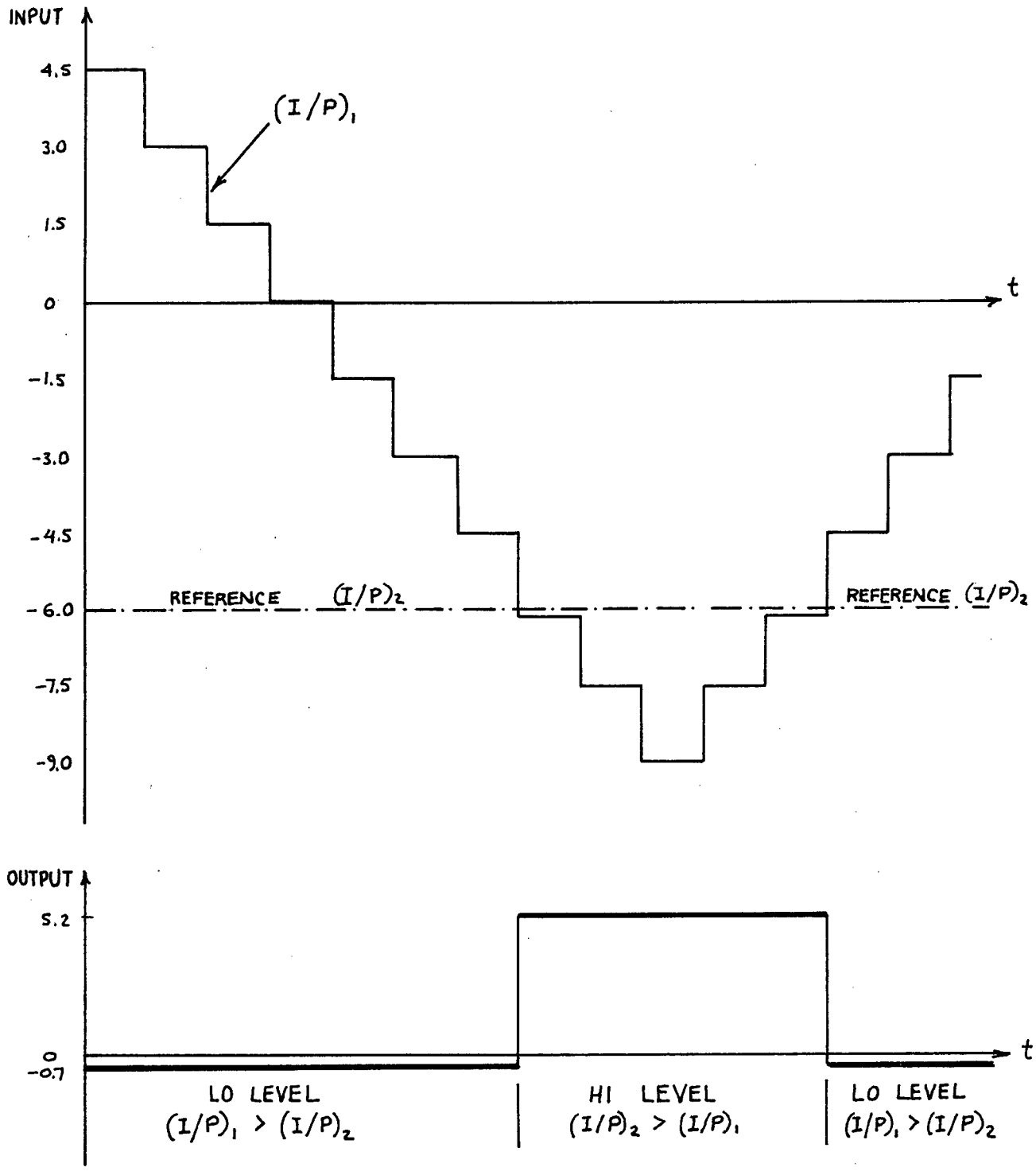
$(I/P)_1$	$(I/P)_2$	OUTPUT	REMARKS
- 4.5	- 6	- 0.7	$(I/P)_1 > (I/P)_2$
- 1.5	- 6	- 0.7	
+ 1.5	- 6	- 0.7	
+ 4.5	- 6	- 0.7	
- 6.0	0	+ 5.2	$(I/P)_2 > (I/P)_1$
- 3.0	0	+ 5.2	
+ 1.5	0	- 0.7	$(I/P)_1 > (I/P)_2$
+ 4.5	0	- 0.7	
- 4.5	+ 6	+ 5.2	$(I/P)_2 > (I/P)_1$
- 1.5	+ 6	+ 5.2	
+ 1.5	+ 6	+ 5.2	
+ 4.5	+ 6	+ 5.2	

GRAPHIC INTERPRETATION

The values used to draw the following graph were measured in a similar fashion to those from the previous table. While drawing the graph, it was assumed that those readings occurred at regular time intervals and in a staircase arrangement. This last step is done to familiarize the reader with staircase waveforms, commonly generated from binary counter circuits, as it will be shown in the section of Digital to Analog Conversion.

In this graph, $(I/P)_2$ is kept at - 6 V and is used as a reference voltage, whereas $(I/P)_1$ is varied between + 4.5 V and - 9 V.

Notice also, that a logic LO level occurs if $(I/P)_1 > (I/P)_2$, but a logic HI level occurs whenever $(I/P)_2 > (I/P)_1$.

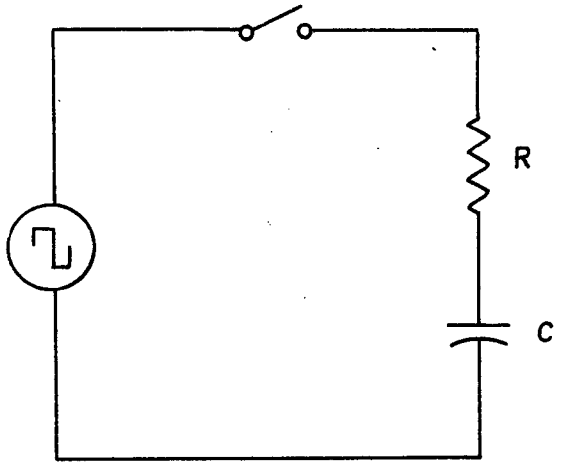


WAVESHAPING CIRCUITS

These circuits have predetermined transfer functions that transform input signals into specifically shaped outputs.

RC WAVESHAPING CIRCUIT

The circuit shown below consists of a square wave signal generator and a load. The load is made up of a resistor and a capacitor connected in series.



When a square wave signal is applied, the resulting waveforms, which appear across the resistor and across the capacitor, will not have the same shape as the input square wave.

The next figure shows the differences between the original square wave and the waves across the capacitor and the resistor.

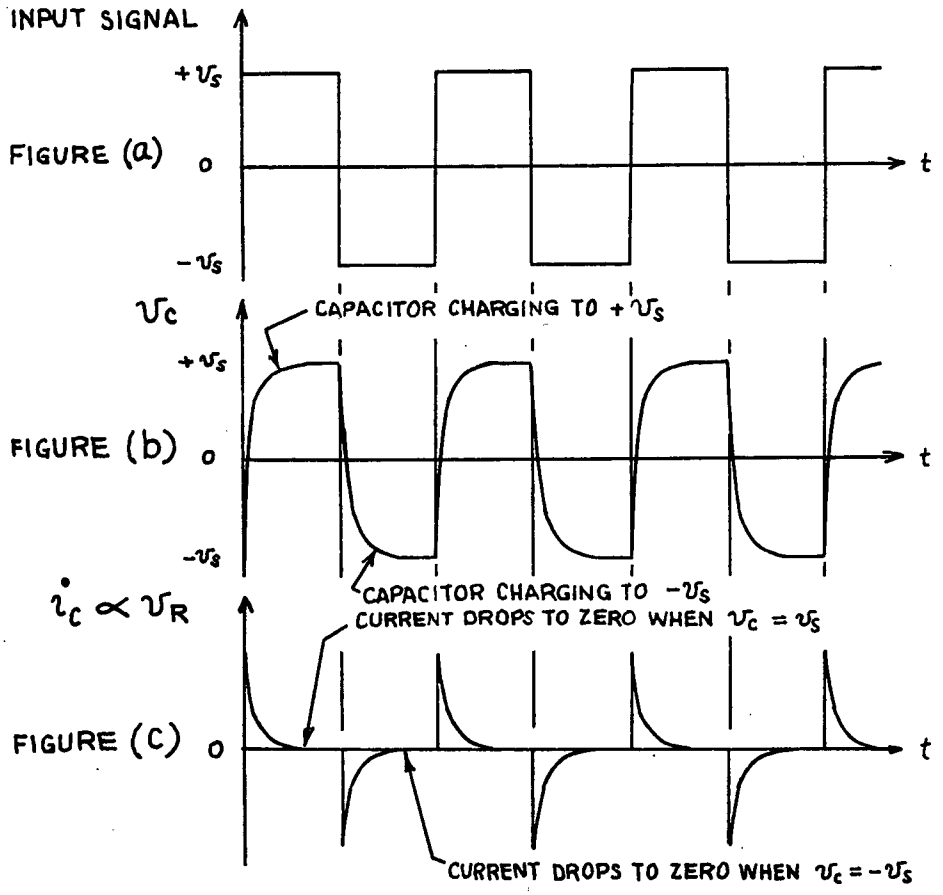


Figure (a) shows the input voltage versus time, i. e. the square wave signal from the generator.

Figure (b) shows that the voltage v_C across the capacitor does not change instantaneously with new voltage levels. New voltage levels take place exponentially in the same way that a tank with a floater controlled faucet fills up with water, i. e. fast when the tank is empty, because the floater is fully down and the faucet is fully open, and not so fast as the tank fills up with water and the water level lifts the floater, closing the faucet more and more.

Figure (c) shows the change of magnitude and direction of the capacitor current i_C. If the capacitor needs to charge from $-v_s$ to $+v_s$,

a very large current will circulate in the circuit, but this current becomes smaller, in an exponential fashion, as the voltage in the capacitor approaches the new value v_s. This is similar to what happens to the tank with the floater controlled faucet. When the tank is empty, the floater is fully down and the faucet is fully open, then a large flow of water starts to fill the tank. However, this flow of water becomes smaller as the tank fills up with water and the water level lifts the floater, closing the faucet more and more.

Similar action takes place when the capacitor needs to charge from $+v_s$ to $-v_s$, except that the current will be in the opposite direction.

The waveshapes shown above can easily be seen on an oscilloscope. Although oscilloscopes display voltage waveforms, they do not directly display current waveforms.

Therefore, to observe the current waveforms due to i_C, it must be noticed that:

a) The capacitor and the resistor are connected in series, therefore: $i_C = i_R$.

b) By Ohm's law, the current i_C will produce a voltage drop across the resistor, which is directly proportional to i_C, because the resistance is constant. Therefore $i_C \propto v_R$.

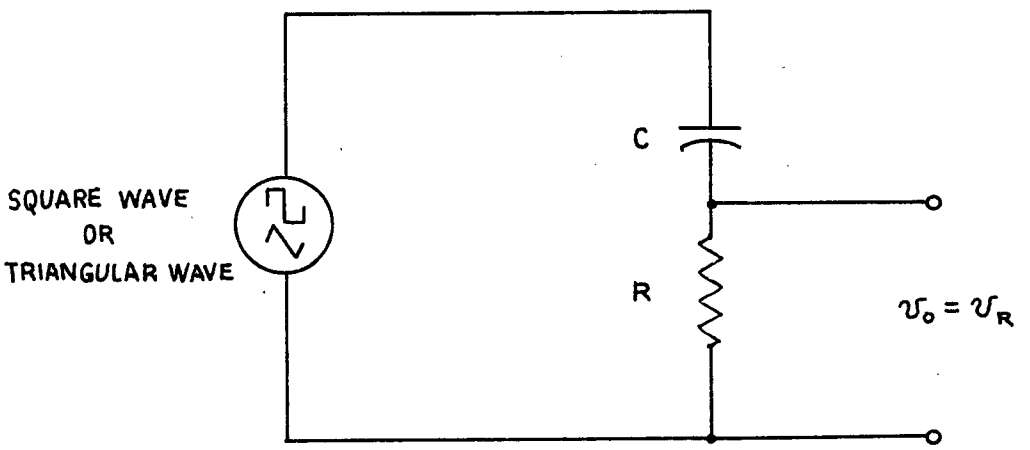
Thus, by connecting the oscilloscope across R, the resulting waveform v_R will be proportional to the current waveform for i_C.

RC DIFFERENTIATORS

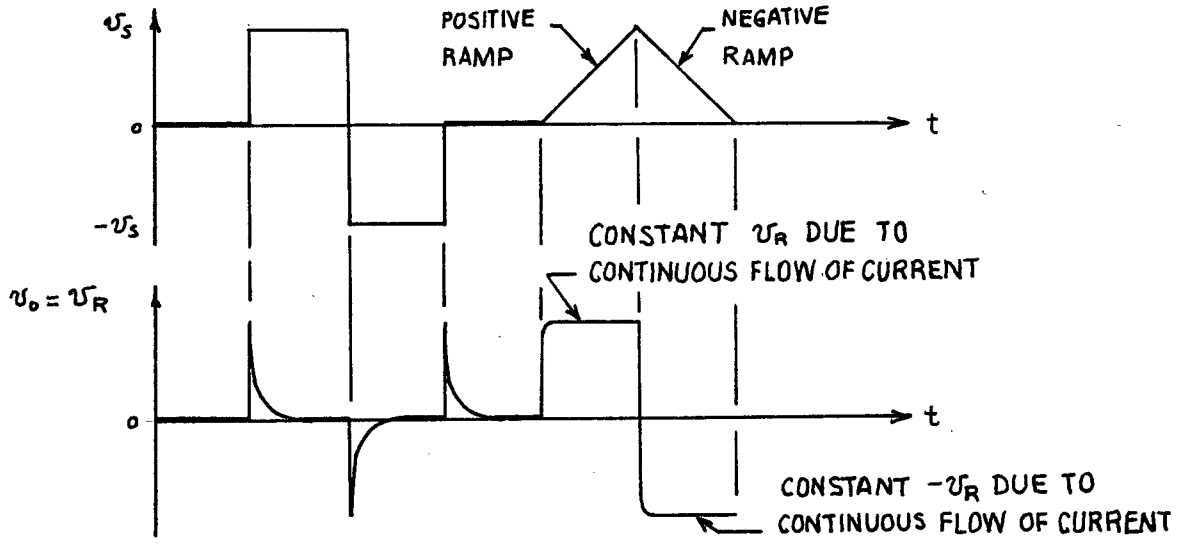
An RC waveshaping circuit yields two different output signals, depending on the output connections.

When the output connections are placed across the resistor R, as shown below, the output waveshape is roughly the differentiated input signal. The term "differentiated" refers to the mathematical operation that describes the changes in shape undergone by an input signal, when it reaches the output of this configuration.

In our case, the output shapes are the current variations that take place in a resistive capacitive circuit, since $v_R \propto i_C$.



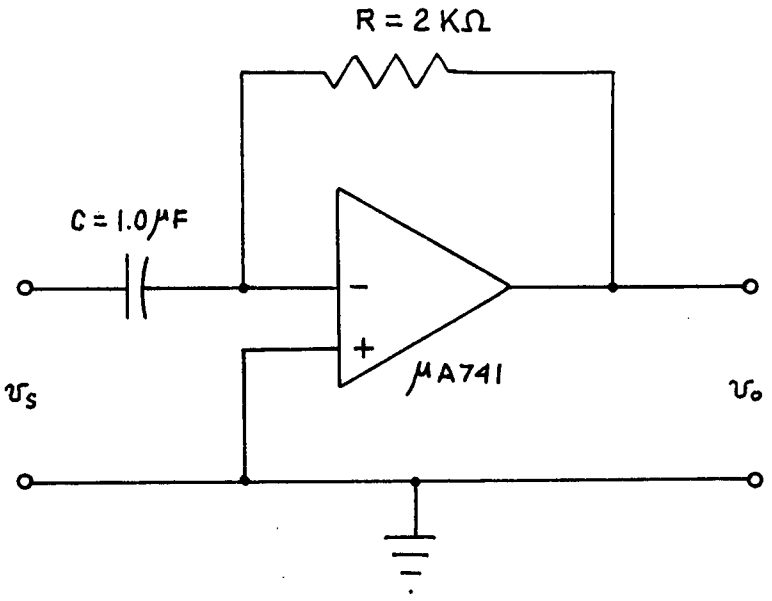
The output responses to different input waveforms are shown below:



When v_s is a ramp, the capacitor charges at a constant rate. Because the voltage across R is proportional to this charging current, then the voltage v_R is constant. This is equivalent to a tank with a floater controlled faucet. If the tank volume is increased at a constant rate, the floater would never be lifted up and the current would flow continuously.

The simple RC circuit has two major disadvantages, it loads other circuits, and also attenuates the input signal, since it is made up of passive components.

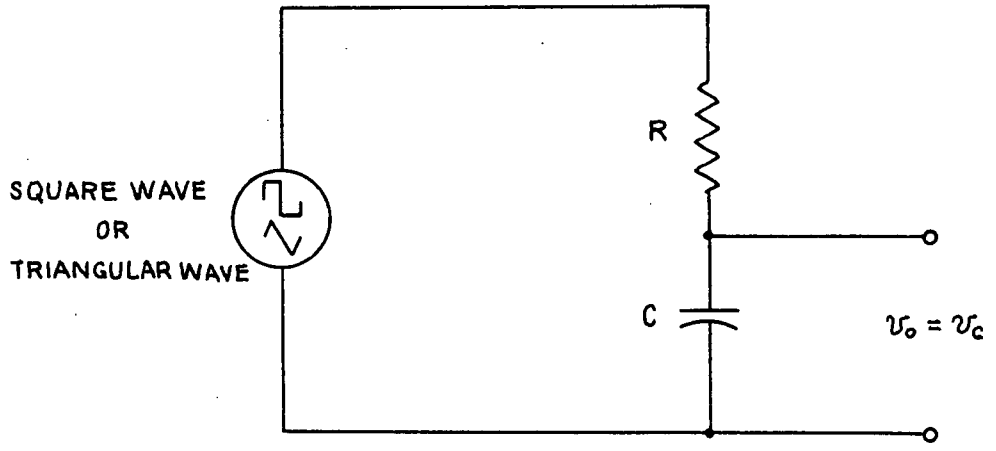
These disadvantages can be overcome, by the use of operational amplifiers. A differentiating circuit, using one of these operational amplifiers is shown below.



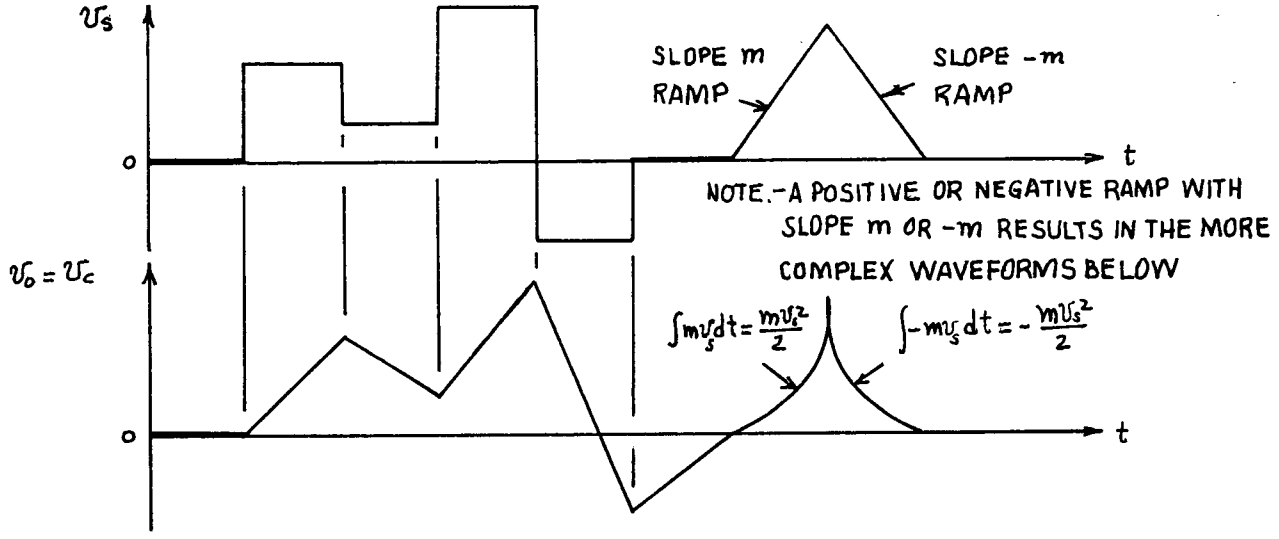
RC INTEGRATORS

When the output connections of a resistive capacitive circuit are placed across the capacitor C, as shown below, the output waveshape is roughly the "integrated" input signal. The term "integrated" refers to the mathematical operation that describes the changes in shape undergone by an input signal, when it reaches the output of this configuration.

The output shapes, for this circuit, are those corresponding to the voltage variations across the capacitor C.

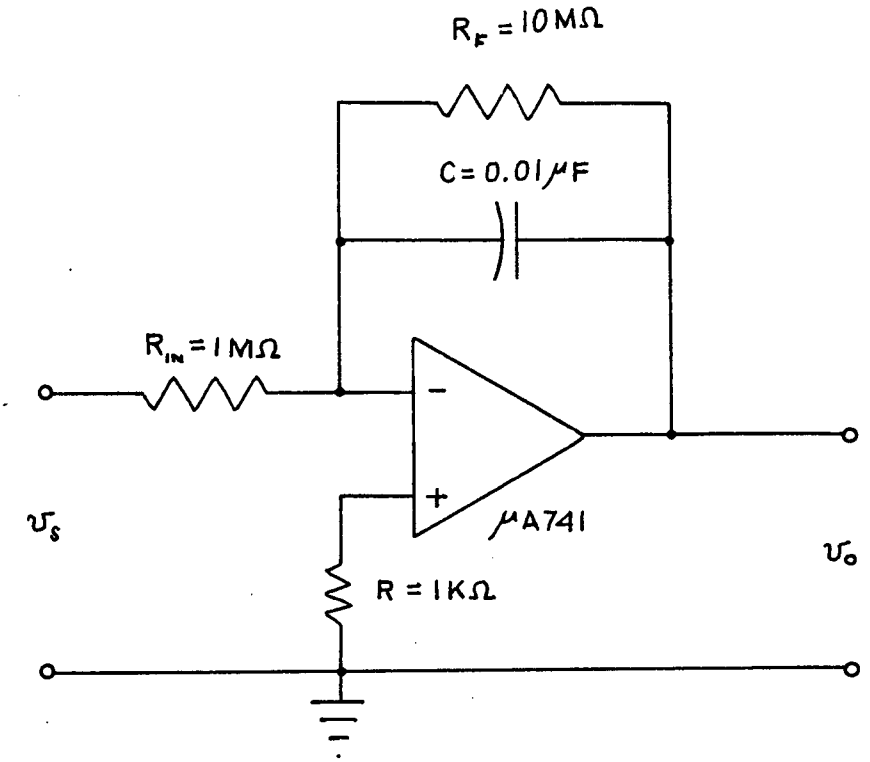


The output responses to different input waveforms are shown below:



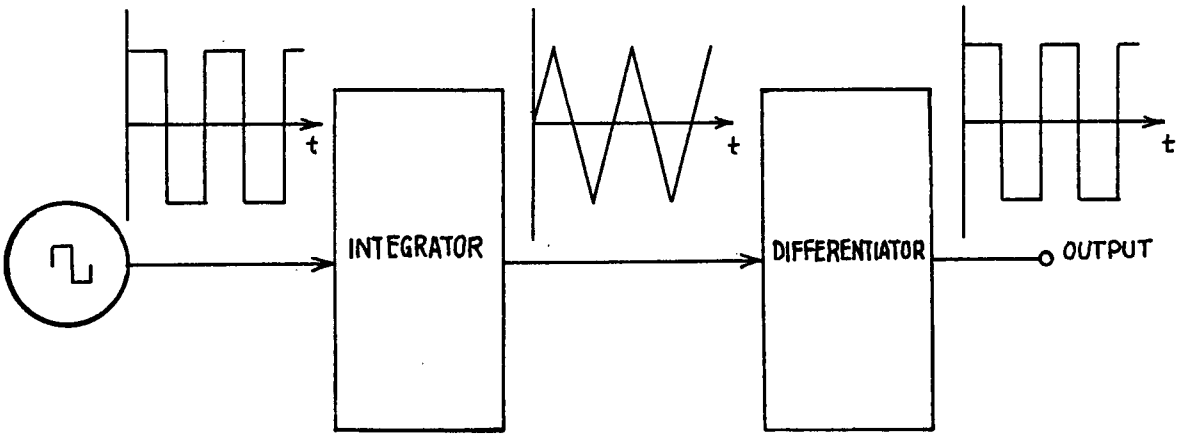
Notice that integration is the inverse process from differentiation. Therefore square voltage levels result in increasing or decreasing outuput ramps. This is so, because the capacitor tries to charge up to those new voltage levels. Although capacitors charge exponentially, if the change of voltage levels occurs faster than the capacitor takes to charge to those new levels, then the rate of charge of the capacitor will look almost like a linear ramp.

Compensated circuits, using operational amplifiers, produce fairly linear ramps out of square voltage level variations. One of these circuits is shown below.



The connection of an integrator followed by a differentiator, causes a square input signal to become a triangular waveshape at the output of the integrator, then the differentiator restores this triangular waveshape back into a square wave. This arrangement may be assembled to show that integration and differentiation are inverse functions.

Notice that a 555 timer connected in the astable multivibrator mode will produce the required square waves for this experiment. Also, this clock circuit can supply fairly good triangular waveshapes. These are the waveshapes that appear across the external capacitor during the operation of the clock. These waveshapes can be used by connecting a set of output leads between the pin number two of the 555 timer and ground.


t
INTEGRATOR
t
DIFFERENTIATOR
t
OUTPUT

The results from a binary count are in binary form. The state of a count may be used to control the brightness level of an outside lamp. We may want the results of a low count to produce a low voltage on the lamp, and the results of a higher count to produce a higher voltage on the same lamp. These output voltages may be stepped up in discrete quantities, as a function of an upwards binary count.

The process of converting binary data into specific voltage levels is known as Digital to Analog Conversion (DAC). This process is the fundamental form of communication between a computer system and the external systems under its control.

FACTORS AFFECTING DAC

For the counters so far discussed, binary coded weights have been assigned to the output lines of each flip flop. These weights are based on powers of two. For a 0 to 15 counter, their distribution by flip flop position is shown in the table below.

FF	WEIGHT	REMARKS
A	$2^0 = 1$	LSB
B	$2^1 = 2$	
C	$2^2 = 4$	
D	$2^3 = 8$	MSB

If the count is 15, i. e. if the four flip flops A to D are set, then their outputs will be $Q_A = Q_B = Q_C = Q_D = V_{cc}$. If each output line is fed individually and directly to an external lamp, the external lamp would produce the same brightness with the LSB line as with the MSB line, because the only thing that distinguishes these lines is their electrical position within the counter.

Thus, to discriminate between the different counter output lines:

a) Each HI output line must be multiplied by its respective weight.

b) All the resulting weights must be added.

SUMMING AMPLIFIER FOR SELECTED VOLTAGE SOURCES

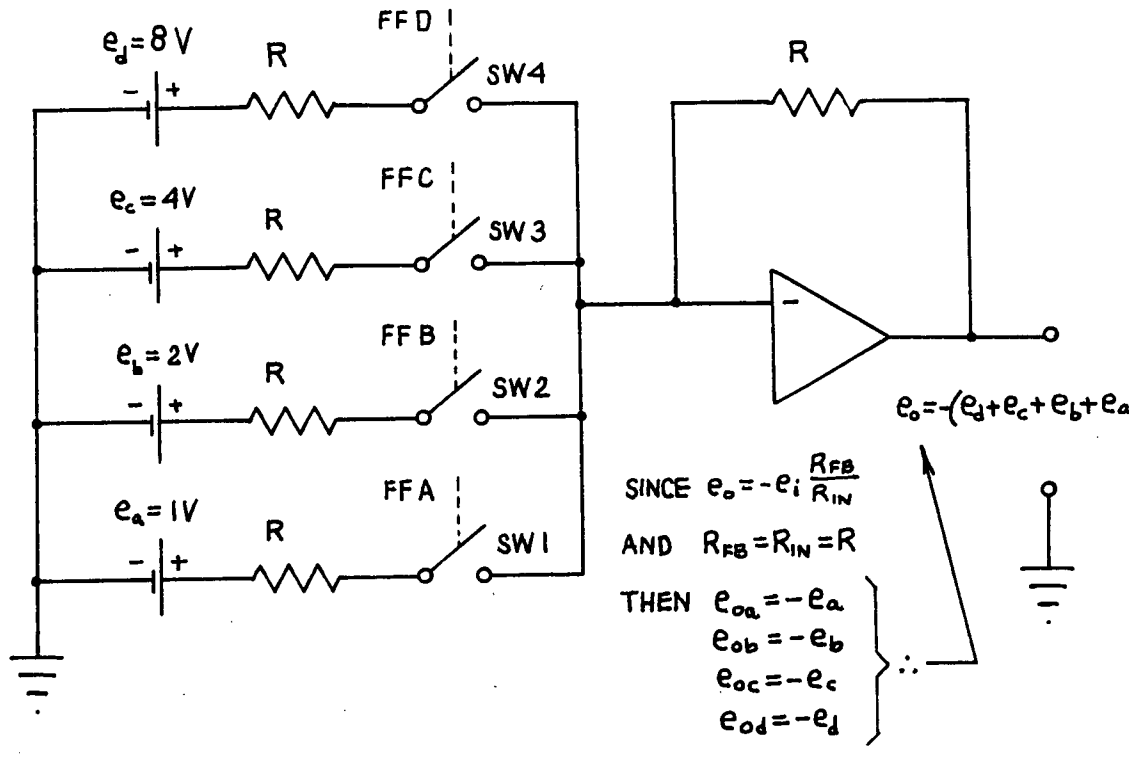
A summing amplifier adds the voltages available at its input. In the circuits used in this section, one, two or more voltage sources are selected to make up the input or inputs to the summing amplifier.

In order to connect these sources, one has to determine which source or sources are needed in the SUM, and then activate the desired choice by closing the appropriate switch or switches.

The connection of the selected sources is done by manually openning or closing wires on an SK10 board, or with ordinary switches. For fast operation, electronic switches must be used, like the ones available in a 4016 or a 4066 integrated circuits.

The potential level of the sources is set usually to voltages that are proportional to weighted binary coded variables. It is these weighted binary quantities that need to be converted into corresponding analog voltage levels.

The circuit needed to convert the digital results from a binary coded count (0 to 15), into analog output voltages, is shown below. Notice that four sources and four switches constitute the inputs to the summing amplifier. Also that the values of each source are weighted and each source is switched ON by a position weighted selector switch.



The table of selector switches versus summing outputs is given below.

SELECTOR SW	SWITCHING WEIGHT	SELECTED SOURCE	SUMMING OUTPUT
1	$2^0 = 1$	1 V	1 V
2	$2^1 = 2$	2 V	2 V
3	$2^2 = 4$	4 V	4 V
4	$2^3 = 8$	8 V	8 V

As an example, consider the contents of a binary counter to be: Q_A = 1 (LSB); Q_B = 0; Q_C = 1 and Q_D = 0 (MSB). The analog equivalent of this count is made by closing selector switches 1 and 3. This way, the voltages from the 1 V source and the 4 V source are inputs to the summing amplifier and thus added. Their 5 V sum is the desired analog equivalent.

The operation of the "Summing Amplifier for Selected Voltage Sources" may be verified by assembling the following circuit. It consists of:

1.- A 555 timer used to produce clock pulses at a variable rate.

2.- A 7490 BCD Decade Counter to produce a 0 to 9 binary count.

3.- Four voltage supplies with convenient weighted values, like those shown in the schematic diagram, i. e. 6V, 3V, 1.5V and 0.75V.

NOTE.- It must be kept in mind, when choosing these supplies, that the maximum input to a summing amplifier is limited by the value of its supply voltage, and that this supply voltage should not exceed the maximum rated value of $\pm$18V.

4.- An electronic switch 4066, used in the digital mode. See its electrical specifications, included at the end of this section.

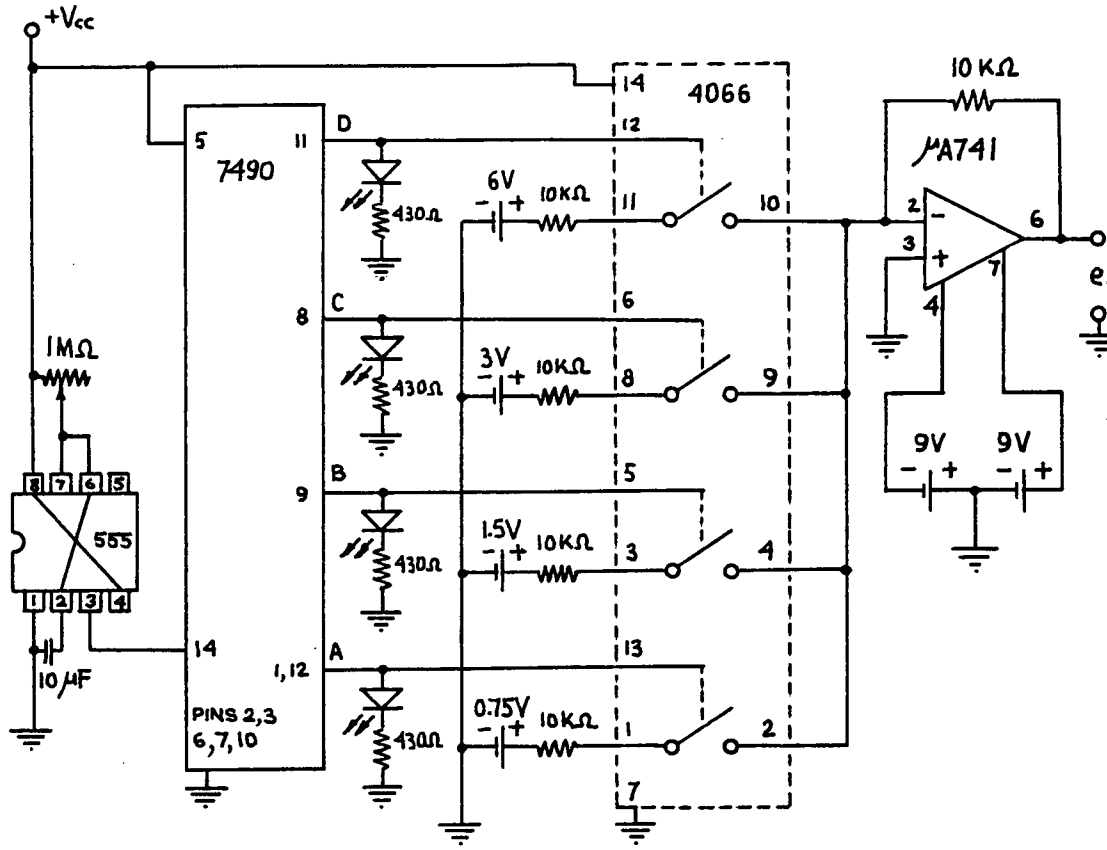
5.- A μA741 operational amplifier, used in the summing amplifier mode. Two 9 V radio batteries may be used to provide the $\pm$ 9 V supply requirements.

Notice that in this circuit, the inputs to the operational amplifier are virtual grounds, as can be verified by measuring the voltage at pin number two of the μA741. Therefore, when different voltage sources get "switched", i. e. connected to the operational amplifier, no loop currents ever result.

When the frequency is sufficiently low, the output voltage from the operational amplifier may be measured with a volt-ohmmeter. The recorded values may be used to complete the accompanying table.

When an oscilloscope is available, the frequency must be increased to observe the resulting staircase display.

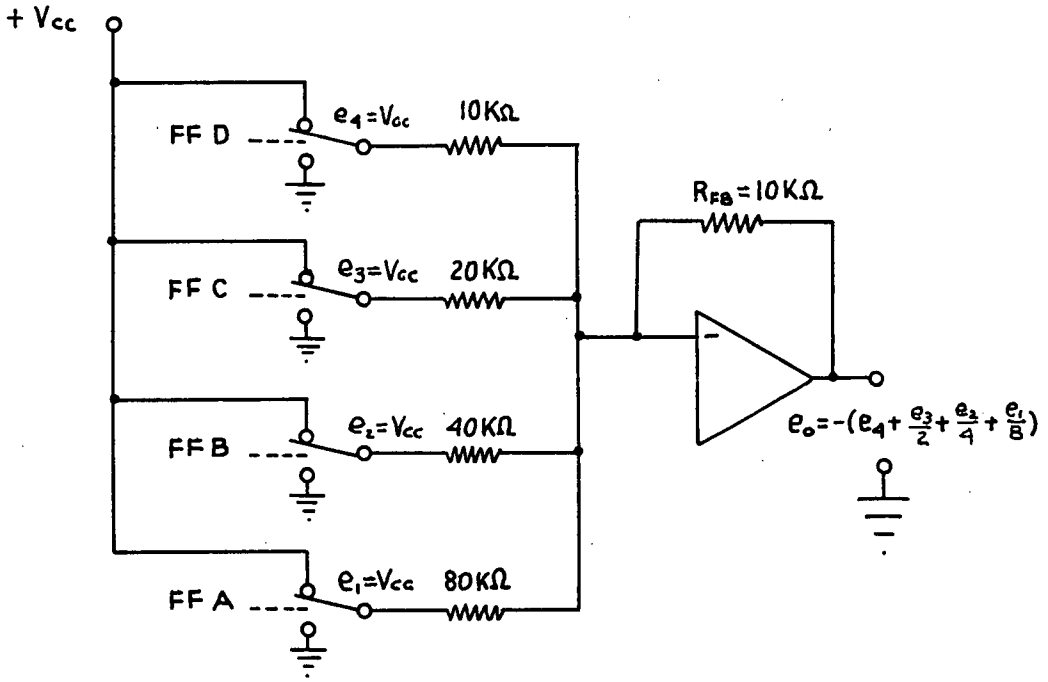
The drawback with this circuit is that it requires a large number of voltage sources with a high degree of accuracy in their rated values.



BINARY COUNT	D	C	B	A	e_o
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					

SUMMING AMPLIFIER WITH WEIGHTED INPUT VOLTAGES

This amplifier uses the supply voltage as its single reference voltage. The proper weighted voltages are achieved by selecting the correct voltage dropping resistors. This selection is done with four individual switches in the circuit shown below.



The resistor values used in the above circuit, have been selected using the summing amplifier equation, that was developed in the section of operational amplifiers:

$$e_0 = - e_i \frac{R_{FB}}{R_{IN}}$$

The flip flops from a binary counter may be used to activate each individual switch. Thus, each flip flop controlled switch will produce a weighted output voltage e_{04}, e_{03}, e_{02} and e_{01}:

$$e_{04} = - V_{cc} \frac{10\ k}{10\ k} = - V_{cc}$$

$$e_{03} = - V_{cc} \frac{10\ k}{20\ k} = - \frac{1}{2} V_{cc}$$

$$e_{02} = - V_{cc} \frac{10\ k}{40\ k} = - \frac{1}{4} V_{cc}$$

$$e_{01} = - V_{cc} \frac{10\ k}{80\ k} = - \frac{1}{8} V_{cc}$$

It can be seen, from above calculations, that the output voltages are weighted values of the supply voltage.

When all the input switches are closed, the total output voltage is given by the summing amplifier expression:

$$e_0 = - (e_4 + \frac{1}{2} e_3 + \frac{1}{4} e_2 + \frac{1}{8} e_1)$$

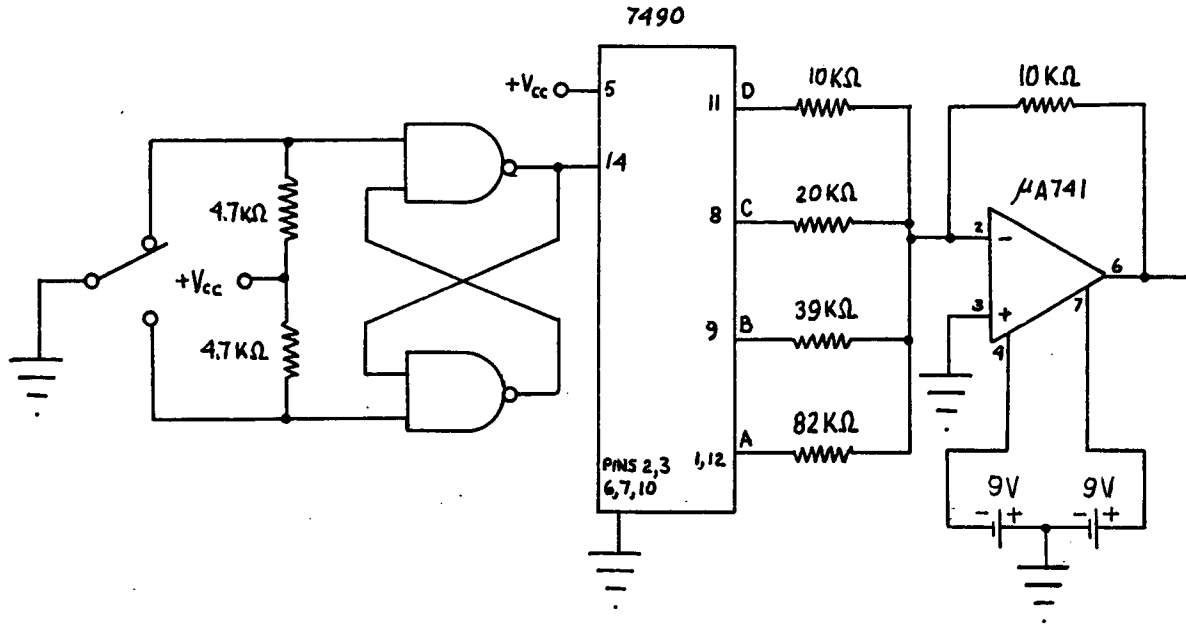
Where: $e_1 = e_2 = e_3 = e_4 = + V_{cc}$

The following circuit may be assembled and tested. It uses a manual pulser, so that a count may be stepped up manually. This procedure permits the use of a volt-ohmmeter to measure the resulting output values.

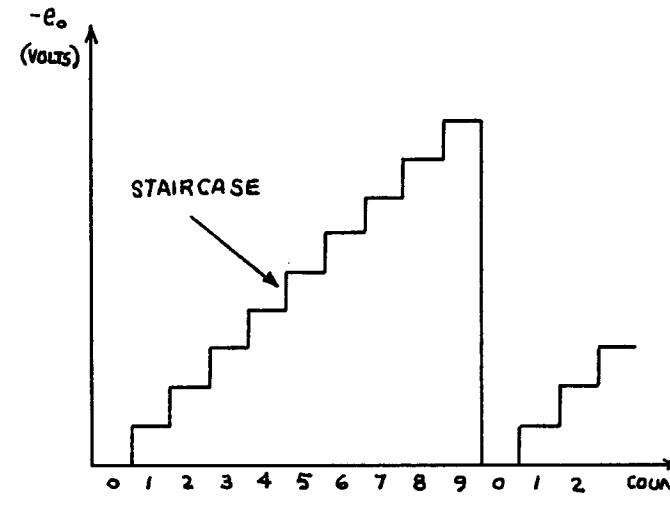
The table that accompanies the circuit may be completed with the recorded values. Notice that the power requirements are met by two 9 V radio batteries for the μA741, plus a separate supply for the + V_{cc} bias.

When an oscilloscope is available, a 555 timer may be used to trigger the counter at higher frequencies. This procedure allows to observe the resulting output voltage staircase on the oscilloscope screen.

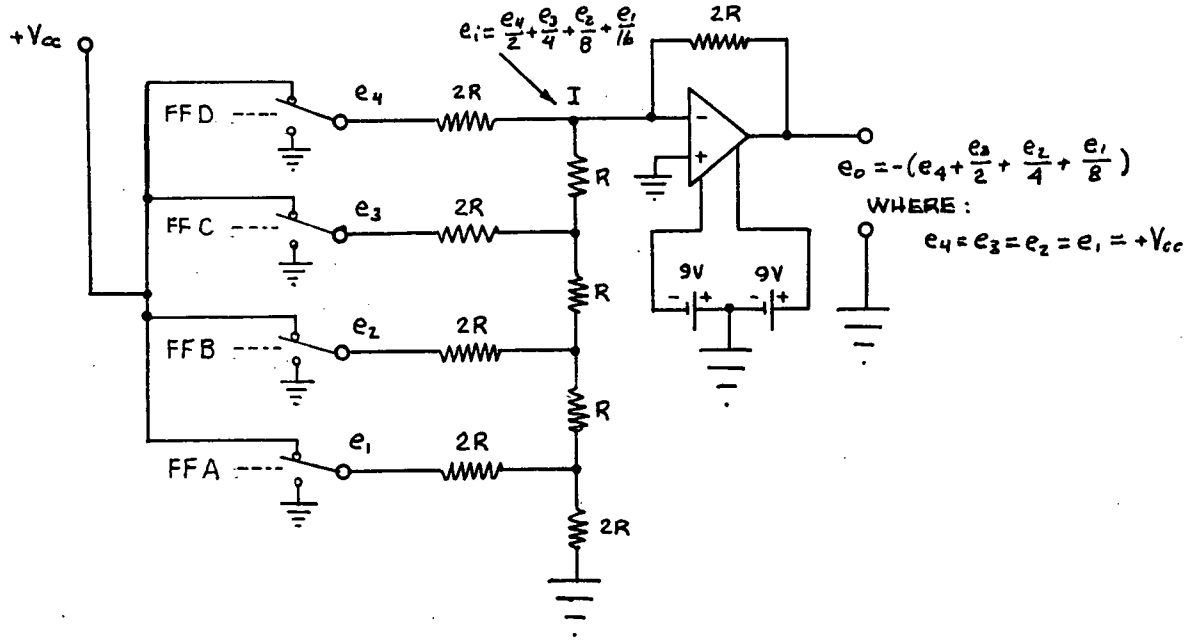
The drawback for this circuit is the large range of resistors needed. **Their value doubles every time that the binary inputs are increased.**



COUNT	D	C	B	A	e_o(V)
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					



This circuit weights the binary input voltages with a resistive ladder attenuator. The advantage of the ladder network is that it uses only two values of resistance. The circuit configuration is shown below:



EQUIVALENT VOLTAGE CONTRIBUTION AT POINT "I" DUE TO EACH SOURCE

It is shown in the appendix, with the use of circuit analysis techniques, that the input voltages e_4, e_3, e_2 and e_1, when fed into such network, will become attenuated in a weighted fashion. See appendix under Thevenin's Theorem, examples 1 and 2.

Point "I" in the above circuit is the output of the resistive ladder network. At this point, the input voltages produce the weighted values shown below.

$$e_4 \longrightarrow \frac{1}{2} e_4$$

$$e_3 \longrightarrow \frac{1}{4} e_3$$

$$e_2 \longrightarrow \frac{1}{8} e_2$$

$$e_1 \longrightarrow \frac{1}{16} e_1$$

Thus, when all those voltages are present, their contribution at point "I" will be:

$$e_i = \frac{e_4}{2} + \frac{e_3}{4} + \frac{e_2}{8} + \frac{e_1}{16}$$

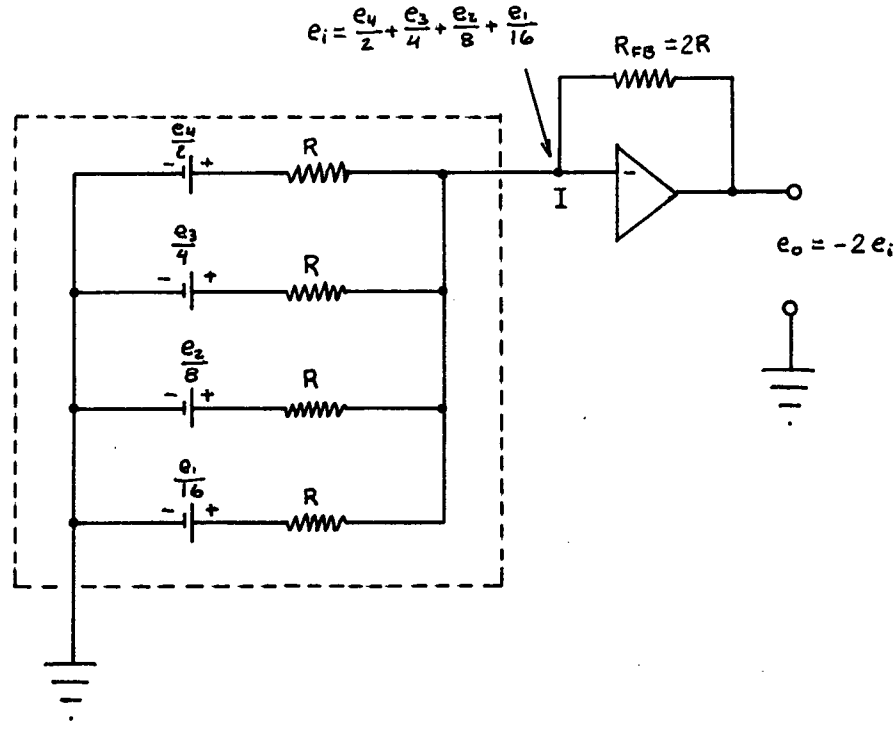
Above expression is clearly the sum. However, the summing amplifier is still needed to insure that the resistive ladder network is isolated and does not load other circuits. Besides, by selecting the proper feedback resistor in the operational amplifier, different values of amplification can be obtained.

EQUIVALENT RESISTANCE OF EACH SOURCE AS SEEN FROM POINT "I"

Again, by the use of circuit analysis techniques, discussed in the appendix, it can be shown that as far as point "I" is concerned, each input source e_4, e_3, e_2 and e_1, can be replaced by equivalent sources with weighted values: $\frac{e_4}{2}$, $\frac{e_3}{4}$, $\frac{e_2}{8}$ and $\frac{e_1}{16}$ respectively, only if each of these new sources is connected in series with an equivalent resistor R, instead of the resistive ladder network.

EQUIVALENT CIRCUIT

Thus, when the input sources and ladder network get replaced by their equivalent circuit, the following configuration results. Compare it with the Summing Amplifier for Selected Voltage Sources.



Above circuit will produce the same voltages at point "I", as those produced by the original sources, when tied to the original resistive ladder network.

The advantage of this equivalent circuit is that it is easier to analyze. For example, using the equations developed for the summing amplifier, it is clear that R_{in} is equal to R, a fact that is not obvious from the original resistive ladder network.

If in above circuit, R_{FB} is chosen so that $R_{FB} = 2R$, then the resulting voltage e_0 at the output of the operational amplifier becomes:

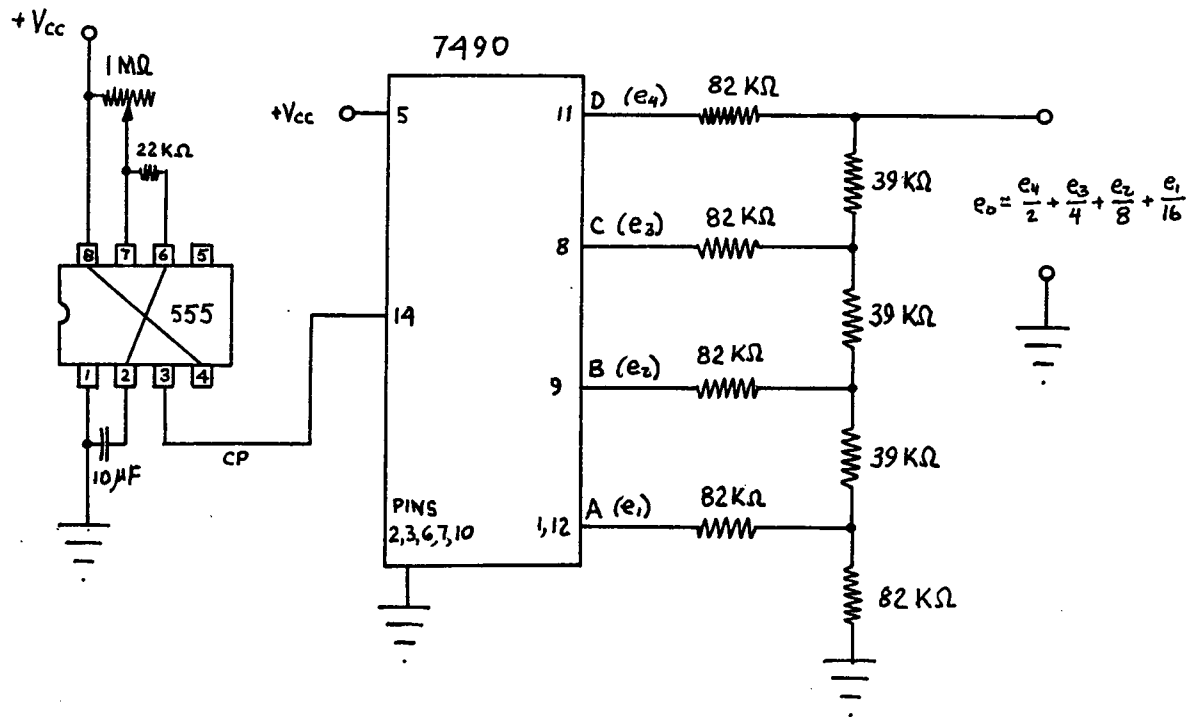
$$e_0 = - e_i \frac{R_{FB}}{R_{in}} = - e_i \frac{2R}{R} = - 2e_i$$

Thus, every voltage at point "I" in the above circuit is inverted and doubled by the operational amplifier. Notice that other values for R_{FB} could be selected, depending on the desired ratio for output voltages.

The final expression for the output voltage due to e_4, e_3, e_2 and e_1 is:

$$e_0 = -2\left(\frac{e_4}{2} + \frac{e_3}{4} + \frac{e_2}{8} + \frac{e_1}{16} \right) = -\left(e_4 + \frac{e_3}{2} + \frac{e_2}{4} + \frac{e_1}{8} \right)$$

The following circuit may be assembled. It consists of a 555 timer, a 7490 BCD decade counter and a resistive ladder network. If the clock frequency is sufficiently slow or manually applied, the output voltages may be measured with a volt-ohmmeter. If an oscilloscope is available, the clock frequency may be stepped up to observe the resulting staircase display. Recorded values may be used to complete the accompanying table.



COUNT	D	C	B	A	e_0
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					

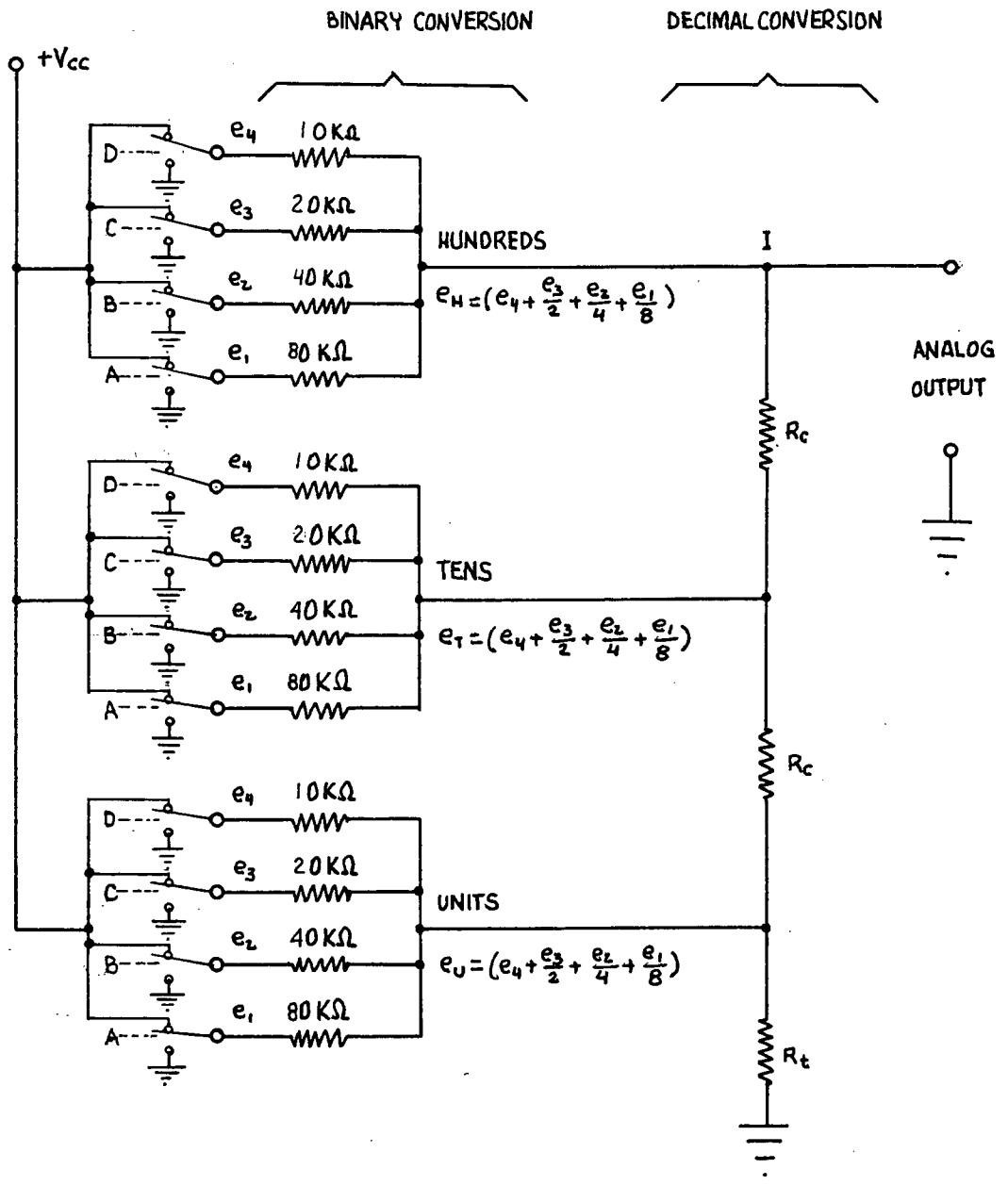
BCD LADDER NETWORK

Most counters with a total count greater than 10, use BCD boxes, so that the count is made in multiples of 10, e. g. 009, 099, 999, etc. The following approach, to convert BCD box counts into analog voltages is used:

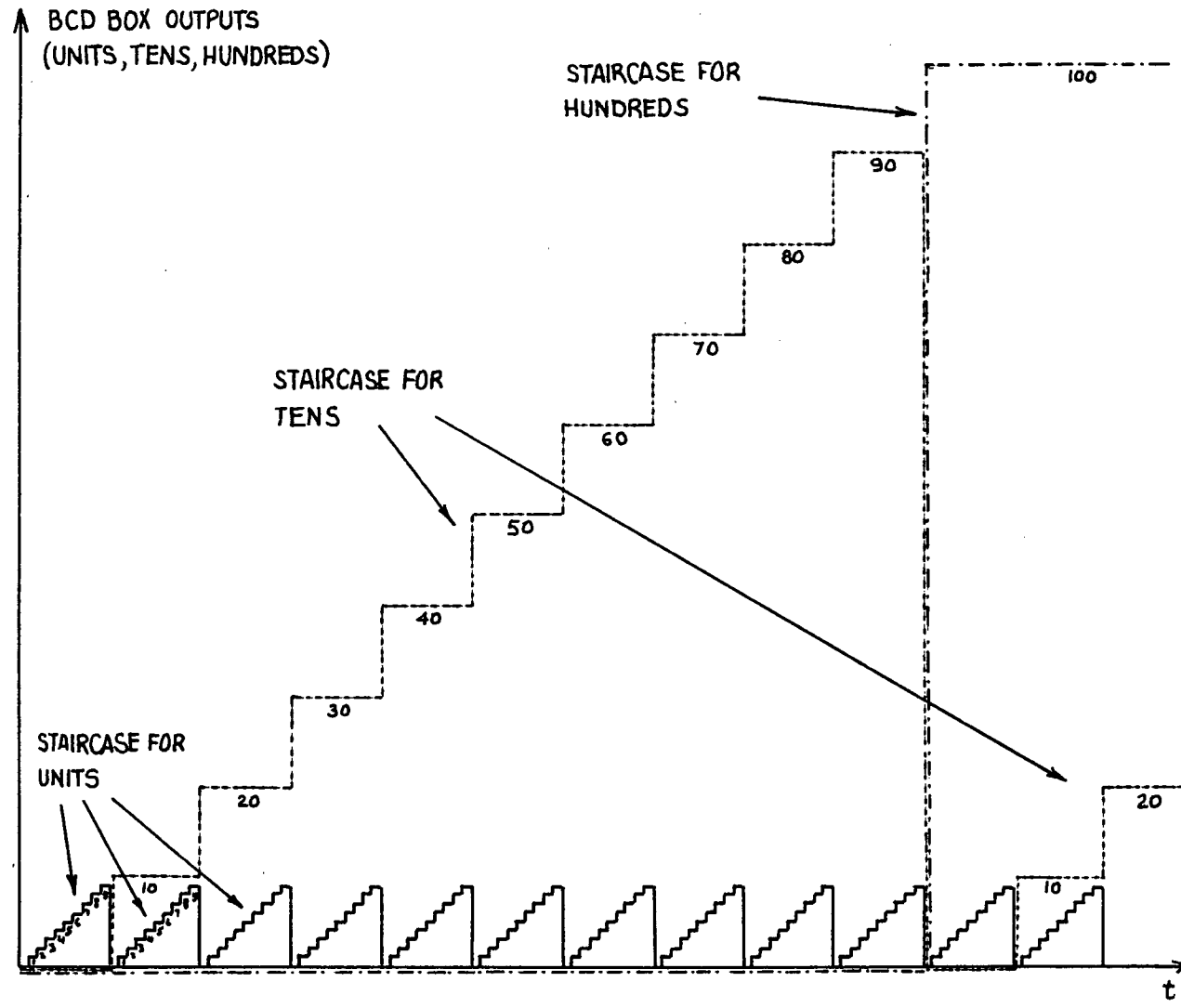
1.- Each BCD box must be weighted with binary weights, using the previously discussed summing amplifier with weighted input voltages. Notice that the voltage levels are still given in $\frac{1}{8}$ increments, since $e_0 = e_4 + \frac{e_3}{2} + \frac{e_2}{4} + \frac{e_1}{8}$, even though these voltage levels are used to represent a count from 0 to 9.

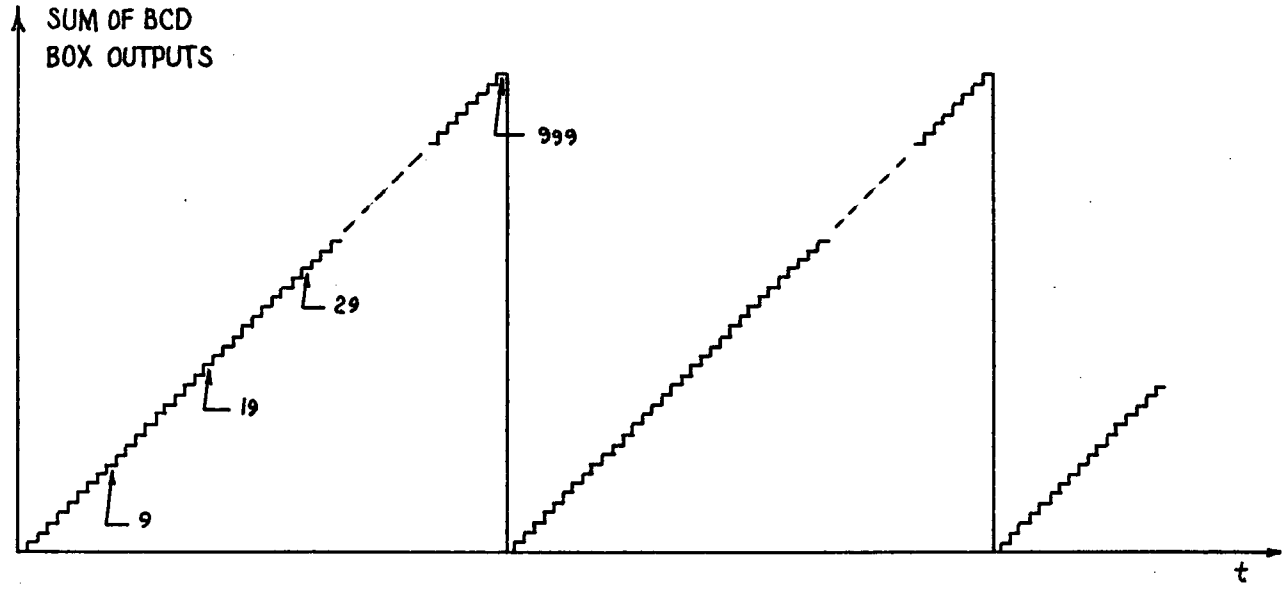
2.- The resulting analog contents of each BCD box are then weighted again, this time to account for the multiple of 10 that each one of them must contain. Thus, each BCD box should provide the correct voltage contribution in $\frac{1}{10}$ increments.

The following network is used for this conversion. It shows each BCD box replaced by a summing amplifier with weighted input voltages.



This network should produce three simultaneous staircases, one corresponding to the binary weight conversion for "units", one corresponding to the "tens" and one to the "hundreds". Since the three staircases are added at point "I", the output results in a single staircase with 999 voltage levels. See the following figures.


BCD BOX OUTPUTS
(UNITS, TENS, HUNDREDS)
STAIRCASE FOR
HUNDREDS
100
90
80
70
60
50
40
30
20
STAIRCASE FOR
TENS
STAIRCASE FOR
UNITS
10
20
10
t


SUM OF BCD
BOX OUTPUTS
999
29
19
9
t

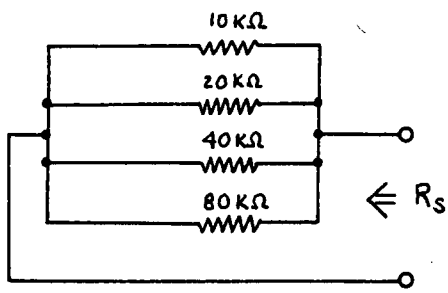
DETERMINATION OF VALUES FOR R_c AND R_t

The equivalent circuit for the network must be defined first. This is done using the circuit analysis techniques discussed in the Appendix. For this particular case, see appendix under Thevenin's Theorem, examples 3 and 4. It is shown in this section, that the BCD voltages for "hundreds" e_H, and "tens" e_T, produce the equivalent values e_H' and e_T' at the output of the BCD ladder network, i. e. at point "I":

$$e_H \longrightarrow e_H \frac{R_t}{R_t + R_s} = e_H'$$

$$e_T \longrightarrow e_T \frac{R_t}{R_t + R_s} \frac{R_s}{R_t + R_s} = e_T'$$

Where R_s represents the resistance of each BCD box when all its voltage sources are shorted, i. e.

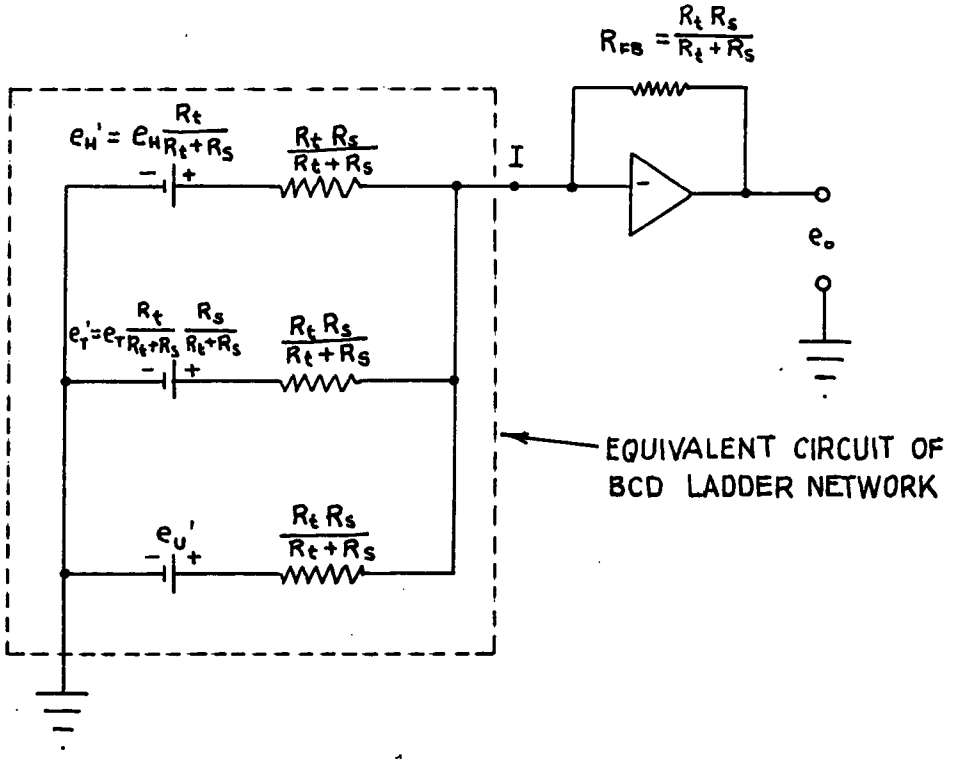


$$R_s = \frac{1}{\frac{1}{80\text{ k}} + \frac{1}{40\text{ k}} + \frac{1}{20\text{ k}} + \frac{1}{10\text{ k}}}$$

$$= 5.33\text{ k}$$

Also, as far as point "I" is concerned, each input source e_H, e_T, and e_U can be replaced by their equivalent sources e_H', e_T' and e_U', only if each of these new sources is connected in series with an equivalent resistor $\frac{R_t R_s}{R_t + R_s}$, instead of the BCD ladder network.

With above values, the equivalent circuit for the BCD ladder network becomes:



Notice that e_T' has to be $\frac{1}{10}$ of e_H', in order to satisfy the desired decimal weighting:

$$e_T' = \frac{1}{10} e_H'$$

Therefore:

$$\left(e_T \frac{R_t}{R_t + R_s} \frac{R_s}{R_t + R_s}\right) = \frac{1}{10} \left(e_H \frac{R_t}{R_t + R_s}\right)$$

Also notice that when each BCD box has the same count, disregarding their decimal weights, their individual voltage outputs are the same, due to the fact that all BCD boxes use the same voltage reference $+V_{cc}$, i. e.

$$e_H' = e_T' = e_U'$$

Therefore, our previous equation gets further simplified:

$$e_T \frac{R_s}{R_t + R_s} = \frac{1}{10} e_H$$

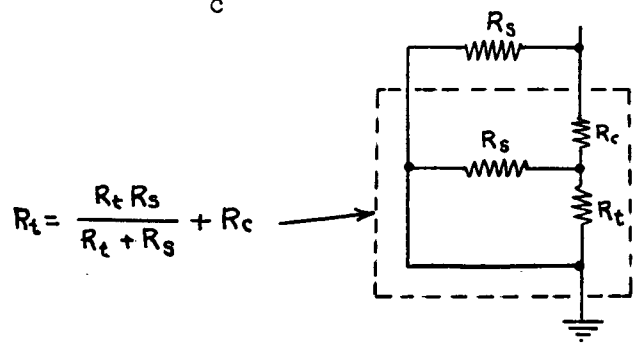
Therefore:

$$R_s = \frac{1}{9} R_t$$

Substituting the value for R_s found above, i. e. $R_s = 5.33\ k\Omega$, into our last expression, yields the value for R_t:

$$R_t = 9\ R_s = 9 \times 5.33\ k\ = 48\ k\Omega$$

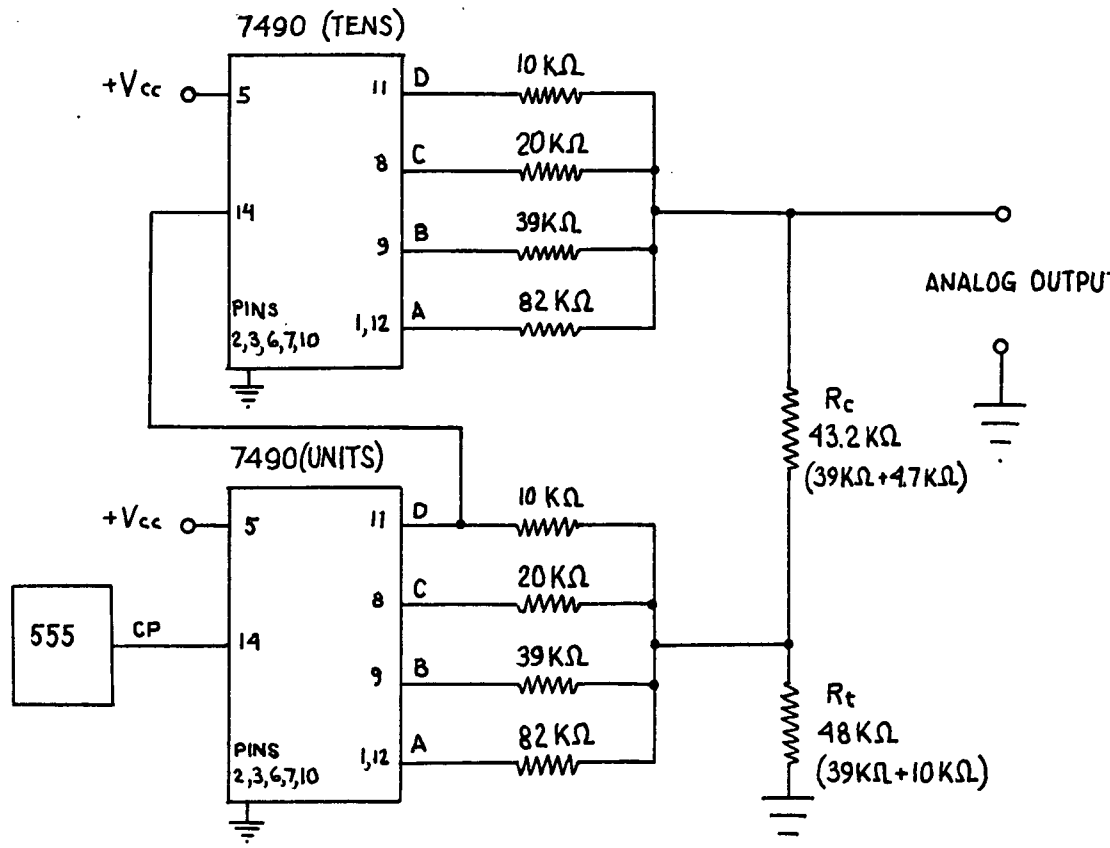
The value for R_c is derived from the basic network relationship shown below:



Therefore:

$$R_c = R_t - \frac{R_t\ R_s}{R_t + R_s} = 43.2\ k\Omega$$

Using above values, we can assemble and test the following circuit. An oscilloscope will be useful to show the discrete voltage levels, but a volt-ohmmeter can still show the gradual increase in the analog output voltage as the count proceeds upwards from 0 to 99.



12 ANALOG TO DIGITAL CONVERTERS

Analog to Digital Converters (ADC) are also referred to as Encoders. They constitute the link between the external analog world and a digital system.

Most of nature's processes are in analog form. Some examples are: temperatures, pressures, wind velocities, distances, acceleration rates, amounts of illumination, volume variations of sound (pressure), friction forces, etc.

Man has tried to relate the amount of those processes with ratios of measurable quantities, e. g. twice as much light as ..., three times as fast as ..., half as warm as ..., etc.

Electrical transducers have allowed him to convert those amounts into analog voltages. The process is the following.

a) A man has to read the analog display, e. g. the indicator needle of a volt-ohmmeter.

b) He then makes up a decision, either to record the measured quantity into a file, IN DIGITAL FORM!, or use the recorded information to determine the outcome of other activities.

Above task can be done using an Analog to Digital Converter. These ADC's allow the conversion of analog voltage read outs into binary coded weighted quantities. The read out can then be displayed using seven-segment displays, or stored directly into the memory of a computer. Then the computer program can take over to activate other instruments or equipment.

An ADC performs its function as follows.

a) It compares the analog input with internally generated counts or quantities.

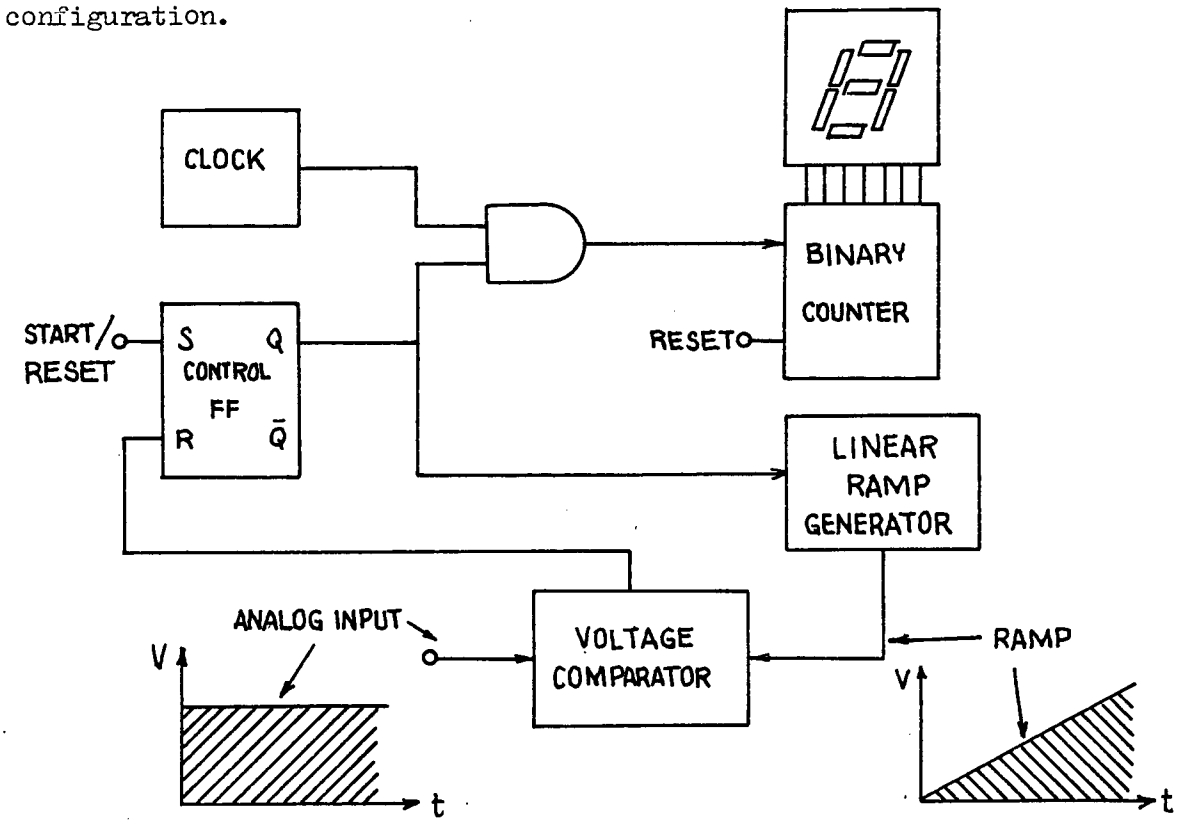
b) When the external analog read out equals the internal count, a message is sent to stop the counter.

Thus, it is the contents of a counter, in digital form, that become the digital read out.

Hence the great importance of counters and comparators in the Analog to Digital conversion of external data.

SWEEP TIMING ANALOG TO DIGITAL CONVERTER

This analog to digital converter uses the following block configuration.



DESCRIPTION

1.- A start pulse:

a) Resets a counter to zeroes.

b) Sets a control flip flop. The control FF then enables clock pulses into a counter.

c) Triggers a linear ramp generator to begin a ramp.

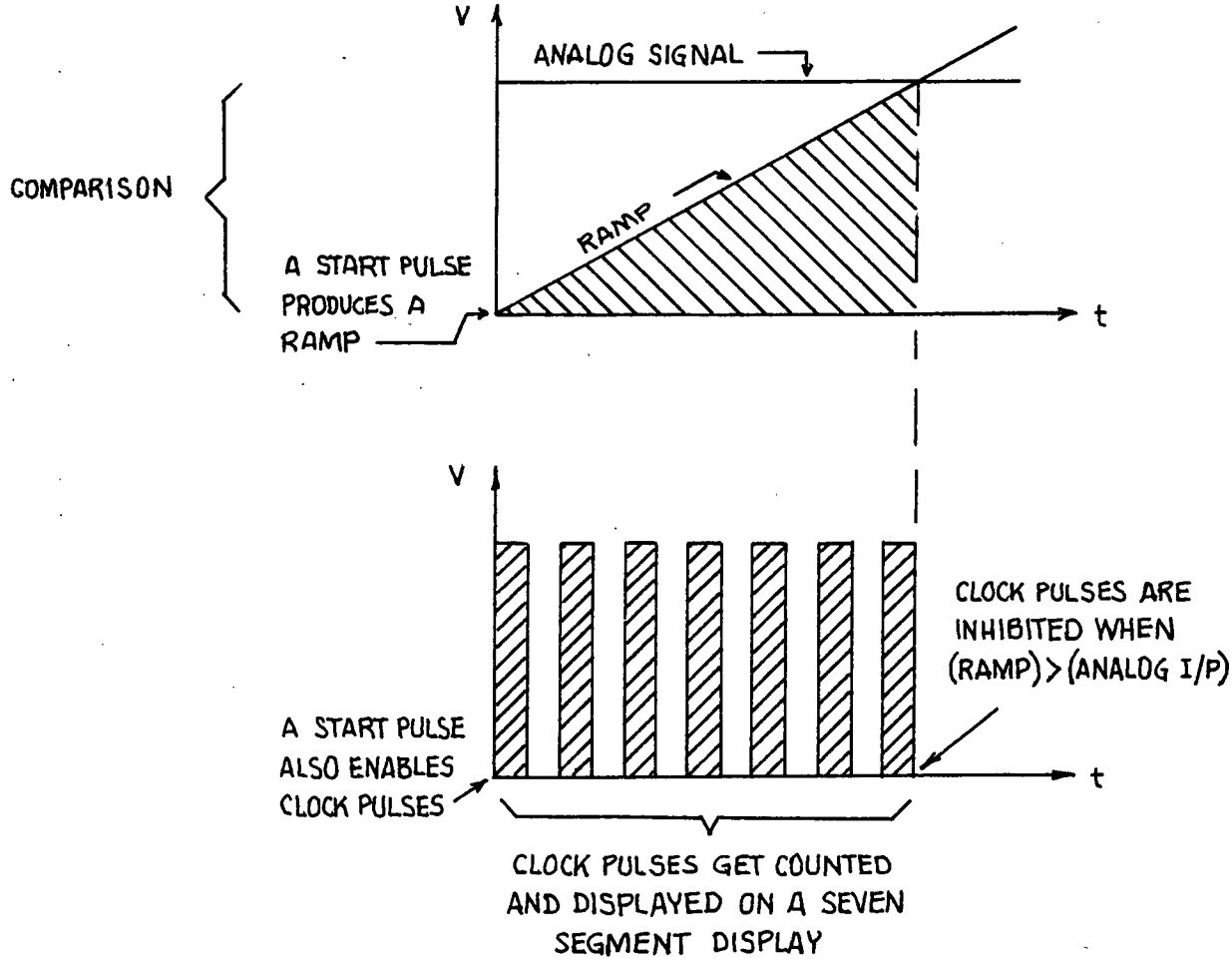
2.- An analog input is compared with the value of the linear ramp.

3.- When the "RAMP VOLTAGE" exceeds the "ANALOG INPUT", the comparator sends a HI pulse into the reset input of the control flip flop.

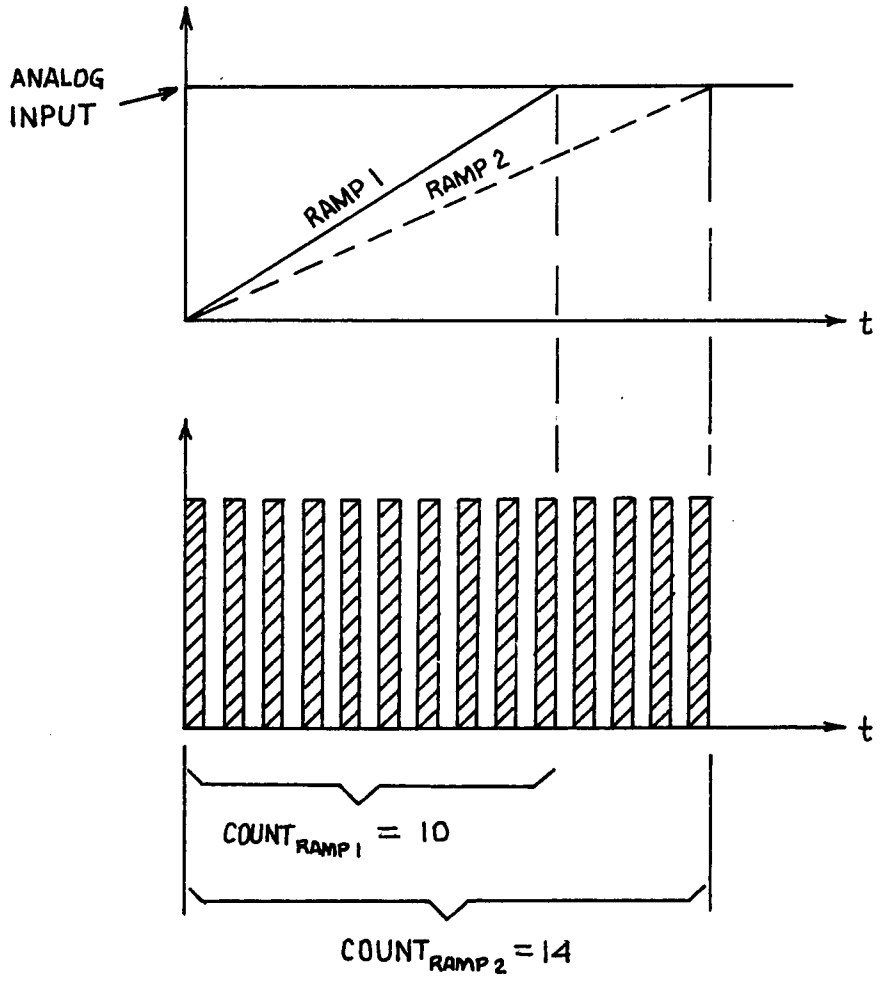
4.- Once the control FF is reset, it inhibits the clock pulses from triggering the counter.

5.- The counter displays the number of clock pulses accepted before the generated ramp exceeds the analog input.

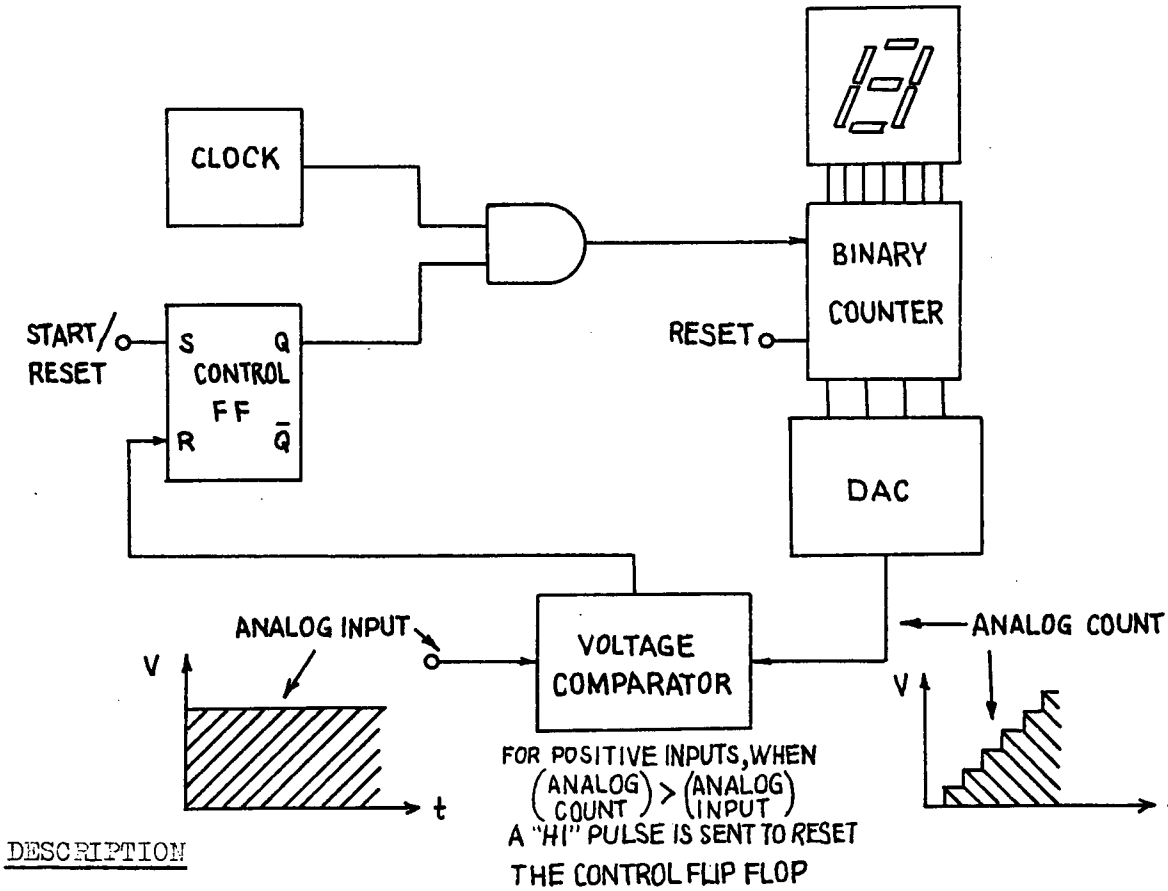
The following figures show the graphical comparison between the "ANALOG SIGNAL" and the "GENERATED RAMP". The results of the count are also indicated, in the interval where the "ANALOG SIGNAL" is greater than the "GENERATED RAMP".



The disadvantage of above configuration is that a slight variation in the slope of the ramp will produce a large variation in the number of pulses counted. See the following figure.



This converter compares the analog input versus a staircase waveform (instead of a ramp). The staircase waveform is the DAC of the state of a counter. See the following general block diagram.



DESCRIPTION

1.- A start pulse:

a) Resets the counter to zeroes.

b) Sets the control flip flop. The control flip flop then enables clock pulses to trigger the counter.

c) Once the counter begins to count, its count is shown on a seven-segment display, and is also converted into an analog voltage equivalent. This analog equivalent is a staircase waveform.

2.- An analog input is compared with above staircase waveform.

3.- When the "ANALOG COUNT" is greater than the "ANALOG INPUT",

assuming that both of these inputs are positive, then the comparator sends a HI pulse into the reset input of the control flip flop. 255

4.- When the control flip flop is reset, it inhibits the clock pulses from triggering the counter.

5.- The value stored by the counter corresponds to the value of the "ANALOG INPUT".

CIRCUIT IMPLEMENTATION

An Analog to Digital Converter Circuit, using the feedback method, is included next. This circuit may be assembled to corroborate above description. The operation of its main blocks, enclosed in dashed lines, is the following.

CLOCK.- It provides the clock pulses for the counter. It consists of a 555 timer in the astable multivibrator mode, and its frequency may be controlled manually.

"AND" GATE.- A 7400-I integrated circuit is used to logically "AND":

a) The enabling pulse from the control flip flop; and

b) The clock pulses fed into the BCD counter.

When the START/RESET SWITCH is closed, it uses a NAND gate from this same 7400-I, to produce a HI pulse out of its pin number 3.

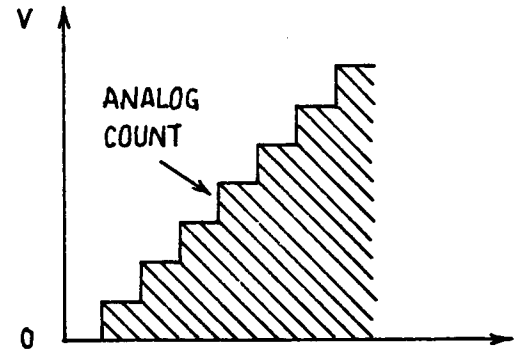
CONTROL FF.- It is an RS flip flop made up with two NAND gates from a second 7400 integrated circuit, (7400-II).

When the START/RESET SWITCH is closed, a HI from pin number 3 of the 7400-I sets the control flip flop. The Q-output of the control flip flop is then used to ENABLE clock pulses into the 7490 counter.

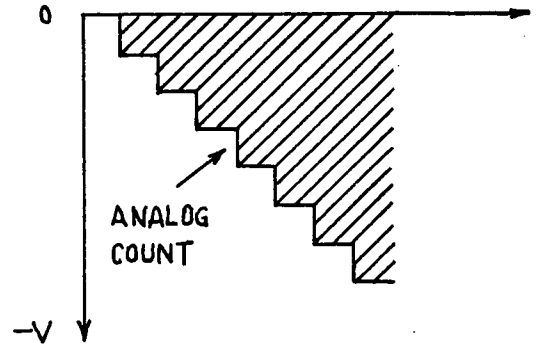
BCD COUNTER.- It consists of a 7490 Decade Counter. When a START/RESET SWITCH is closed, it produces a HI pulse into its pins 2 and 3, reseting the counter to zeroes.

DRIVER AND DISPLAY.- It consists of a 7447, BCD-TO-SEVEN-SEGMENT DECODER/ DRIVER, and an FND507, COMMON ANODE SEVEN-SEGMENT DISPLAY.

DAC.- The Digital to Analog Converter uses a resistive ladder attenuator, and a μA741 operational amplifier. The output voltage from the ladder network, i. e. the "ANALOG COUNT", is a positive increasing staircase waveform, like the one shown below.



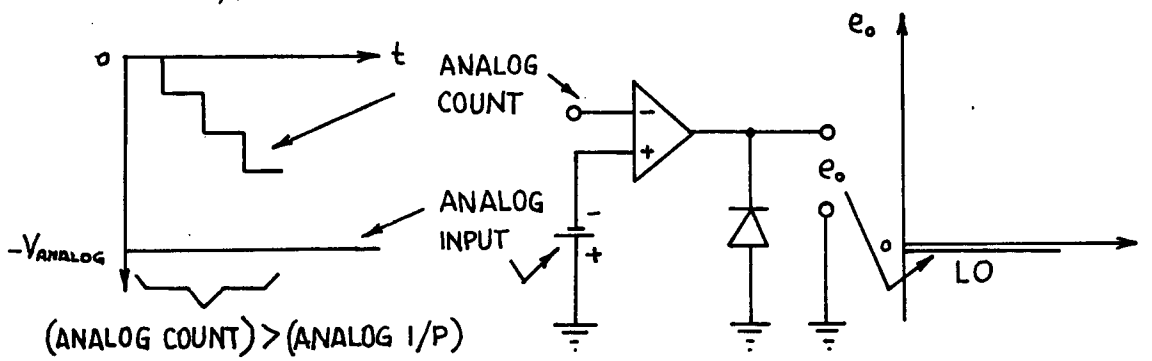
Once above waveform is fed into the inverting pin number 2 of the μA741, it results in an inverted staircase waveform at its pin number 6, see the figure below.



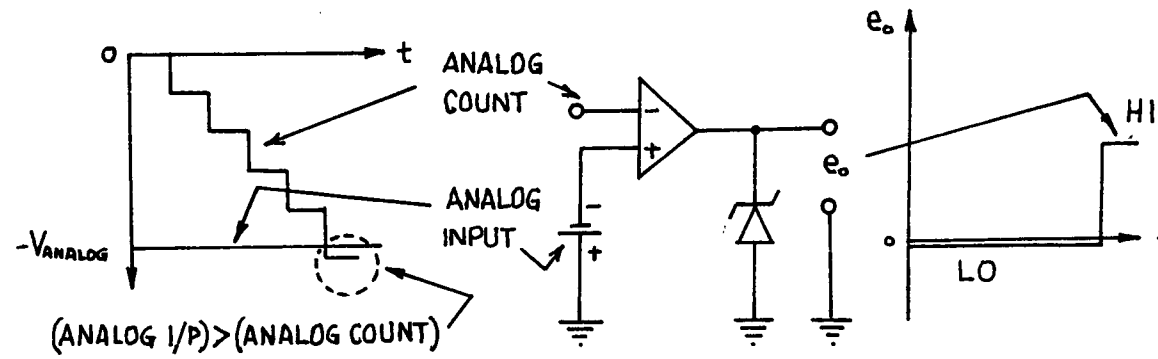
COMPARATOR.- A μA741 is used in the comparator mode. The inverted "ANALOG COUNT" is fed into its pin number 2 and a negative "ANALOG INPUT" is fed into its pin number 3.

When a comparison takes place, and the "ANALOG COUNT" is greater than the "ANALOG INPUT", then the output of the μA741 becomes - 9 V. If a diode is connected at the output, as

shown below, then the output level gets closer to "GROUND", producing a LO level output. (It actually measures about -0.7 V, i. e. the value of the forward bias voltage drop across the diode).



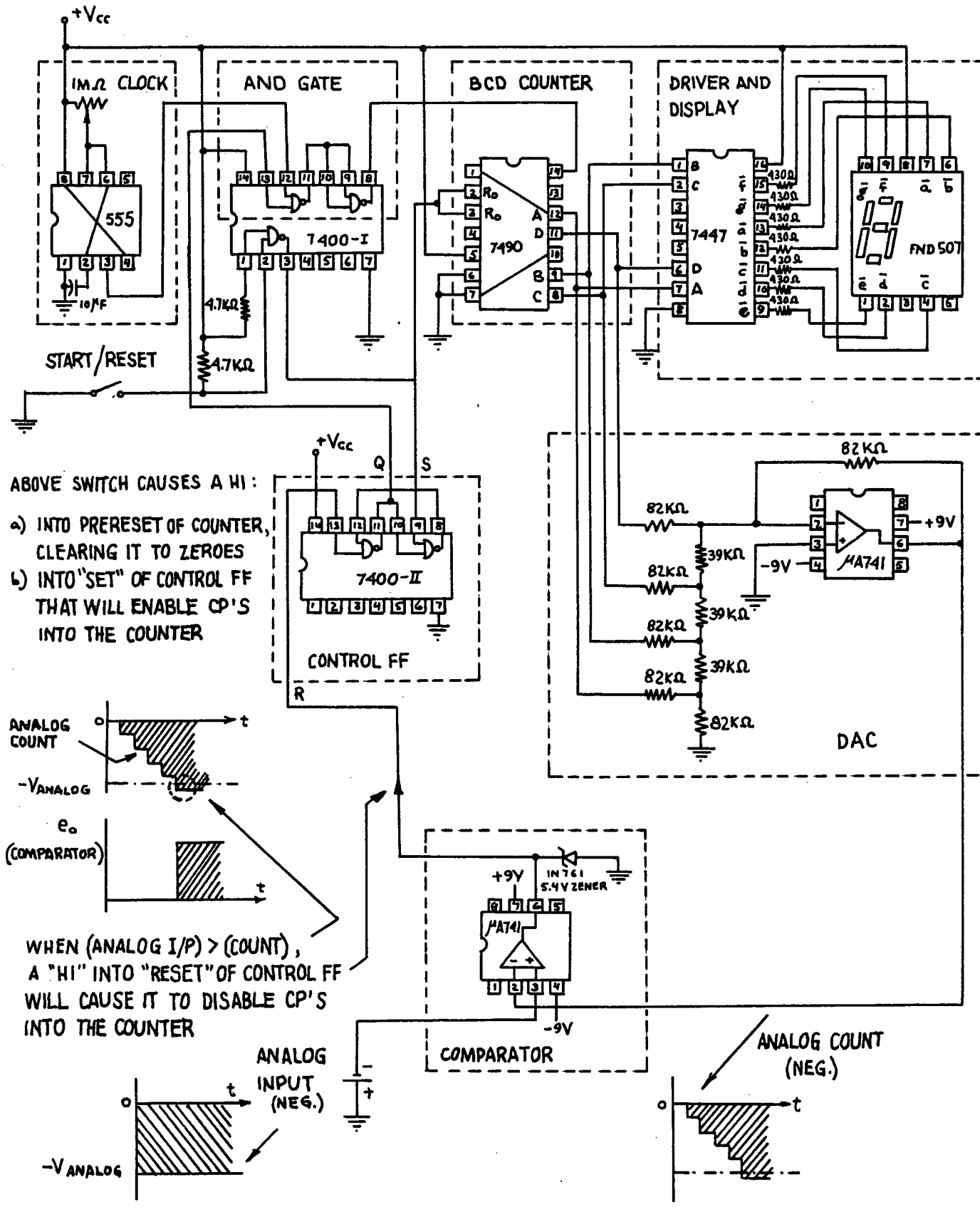
When the "ANALOG INPUT" becomes greater than the "ANALOG COUNT", the output of the μA741, normally an expected + 9 V, (no more than the supply voltage for the μA741), gets clamped down to + 5.2 V. This event takes place only if above diode is replaced by a + 5.2 V zener diode. Thus, a logical HI level is obtained.



Above HI level output is then used to "reset" the RS control flip flop, so that it DISABLES further clock pulses from reaching the counter.

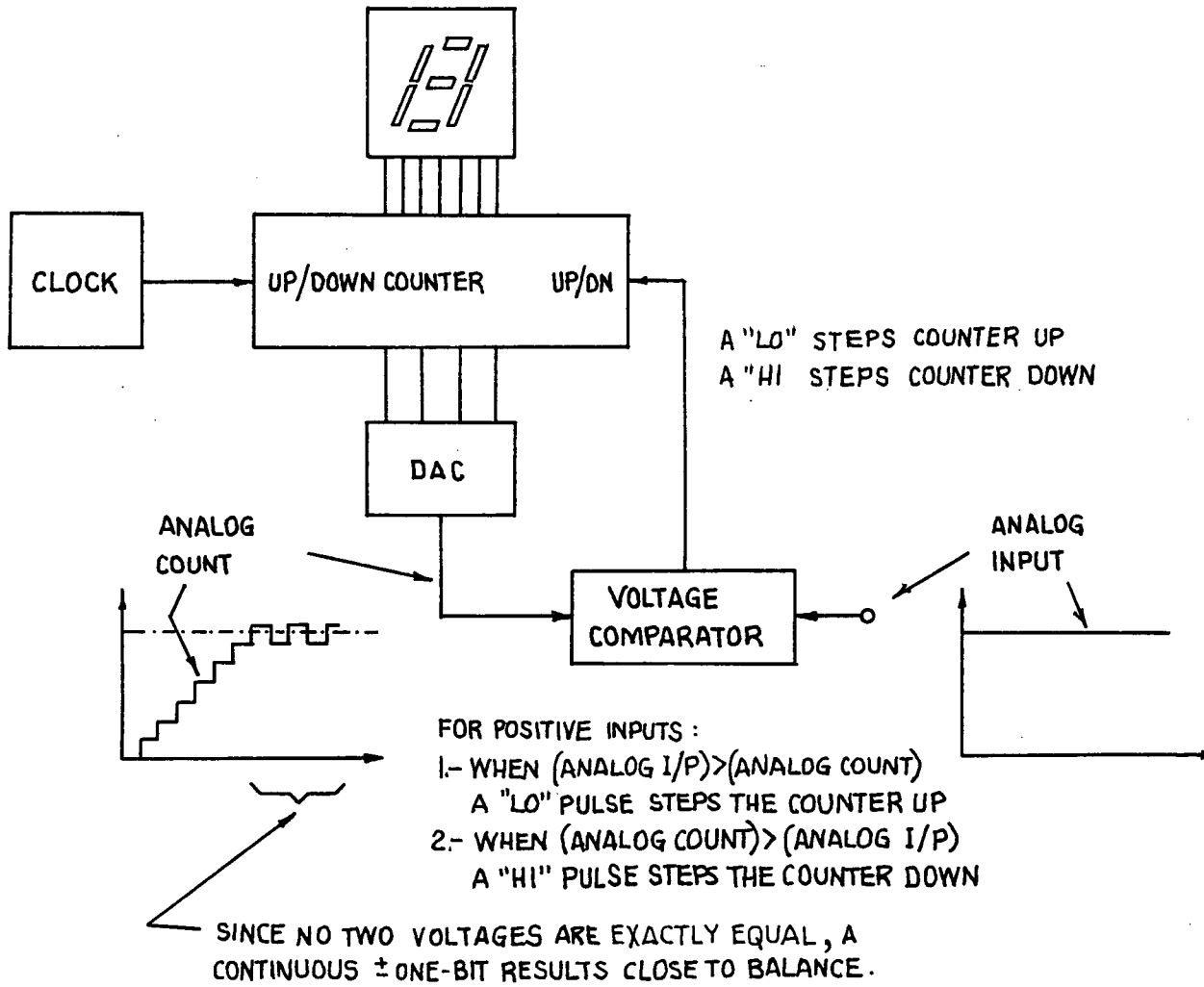
ANALOG TO DIGITAL CONVERTER

FEEDBACK METHOD



ANALOG TO DIGITAL CONVERTER - TRACKING METHOD

Tracking converters use an up/down counter to determine the equivalent digital count of analog inputs. If the analog inputs vary, their variations will be tracked down by the converter. The block diagram of this method is shown below.



DESCRIPTION

When the power is turned on:

1.- An analog input is compared with the analog contents of a binary up-down counter.

2.- The results of above comparisons are used to step up or to step down the contents of the counter.

3.- A comparator, being a very sensitive circuit, can detect even the most minute difference between two voltages. Since no two voltages are exactly alike, the balance condition can never be reached. Therefore, the digital equivalent of an analog input is found only when a continuous $\pm$ one-bit in the counter causes a like change in the Least Significant Digit of the display.

4.- Any futher changes of the analog input will be detected by the comparator, causing the counter to track down the new value or values, within the range of the counter, until a $\pm$ one-bit condition exists again.

CIRCUIT IMPLEMENTATION

The following circuit is an Analog to Digital Converter, it uses the Tracking Method. This circuit may be assembled to corroborate the description given above. The diagram is shown subdivided into functional blocks. The components and function of these blocks is given below.

CLOCK.- A 555 timer in the astable multivibrator mode, with manual control over its frequency.

UP/DOWN COUNTER.- A 74190 integrated circuit is used. This circuit is a synchronous UP/DOWN BCD Decade Counter, with Down/Up mode control.

Its technical specifications are included at the end of this section.

An ENABLE input in this circuit, located in pin number 4, must be connected to ground. This last connection permits the clock pulses to step the counter.

The circuit counts UP with a LO input into pin number 5, and it counts DOWN with a HI input into the same pin.

DRIVER AND DISPLAY.- It consists of a 7447 BCD-TO-SEVEN-SEGMENT DECODER/ DRIVER, and an FND507 COMMON ANODE SEVEN-SEGMENT display.

DAC.- The Digital to Analog Converter consists of a resistive ladder attenuator and a μA741 operational amplifier. This DAC is used to obtain the analog count. For a negative Analog Input, when the power is turned on, an up-count is initiated from zero. The resulting count is an inverted staircase.

COMPARATOR.- A μA741 is used in the comparator mode. This circuit compares the voltage levels fed into its two inputs. These voltage levels correspond to:

a) The Analog Count, which is fed into pin number 2, i. e. the inverting input of the operational amplifier. This Analog Count is a negatively biased staircase from the DAC.

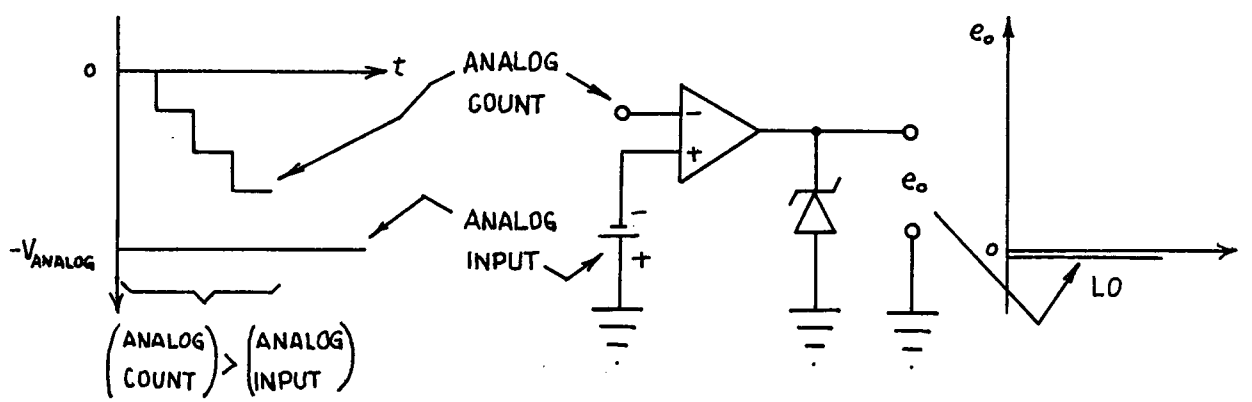
b) The Analog Input, which is fed into pin number 3, i. e. the non-inverting input of the operational amplifier. This Analog Input must be negative, so that it can be tracked down and crossed over by the negatively biased Analog Count. This last condition occurs when both voltages are close to the same value.

COMPARATOR OPERATION

When the power is first turned on, the voltage of a negative ANALOG INPUT is compared with that of an ANALOG COUNT. At this instant, the ANALOG COUNT is zero volts, which is greater than the negative ANALOG INPUT.

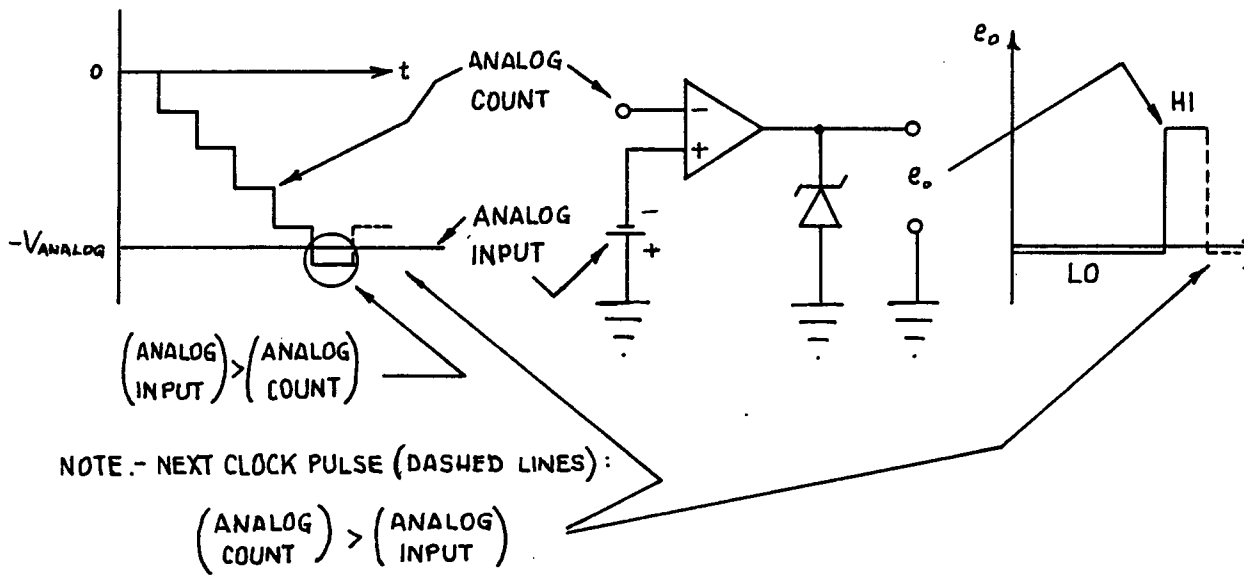
As long as the ANALOG COUNT remains greater than the ANALOG INPUT, the output of the μA741 will be a negative voltage (-9 V). In order to convert this negative voltage into a logical LO level, a zener diode is connected across the output terminals of the μA741. The zener diode conducts when its anode terminal, which is connected to ground, becomes less negative than its cathode terminal. This forward bias conduction clamps the negative output voltage of the μA741 to a nearly ground potential, thus resulting in the desired logical LO.

Above LO, when fed into the up/down counter, will step the count upwards.



When the ANALOG INPUT becomes greater than the ANALOG COUNT, the output of the μA741 will try to be equal to +9 V. Due to the zener diode, that has a reverse break down voltage of +5.2 V, the output e_o is clamped, this time to +5.2 V, resulting thus in a positive HI level.

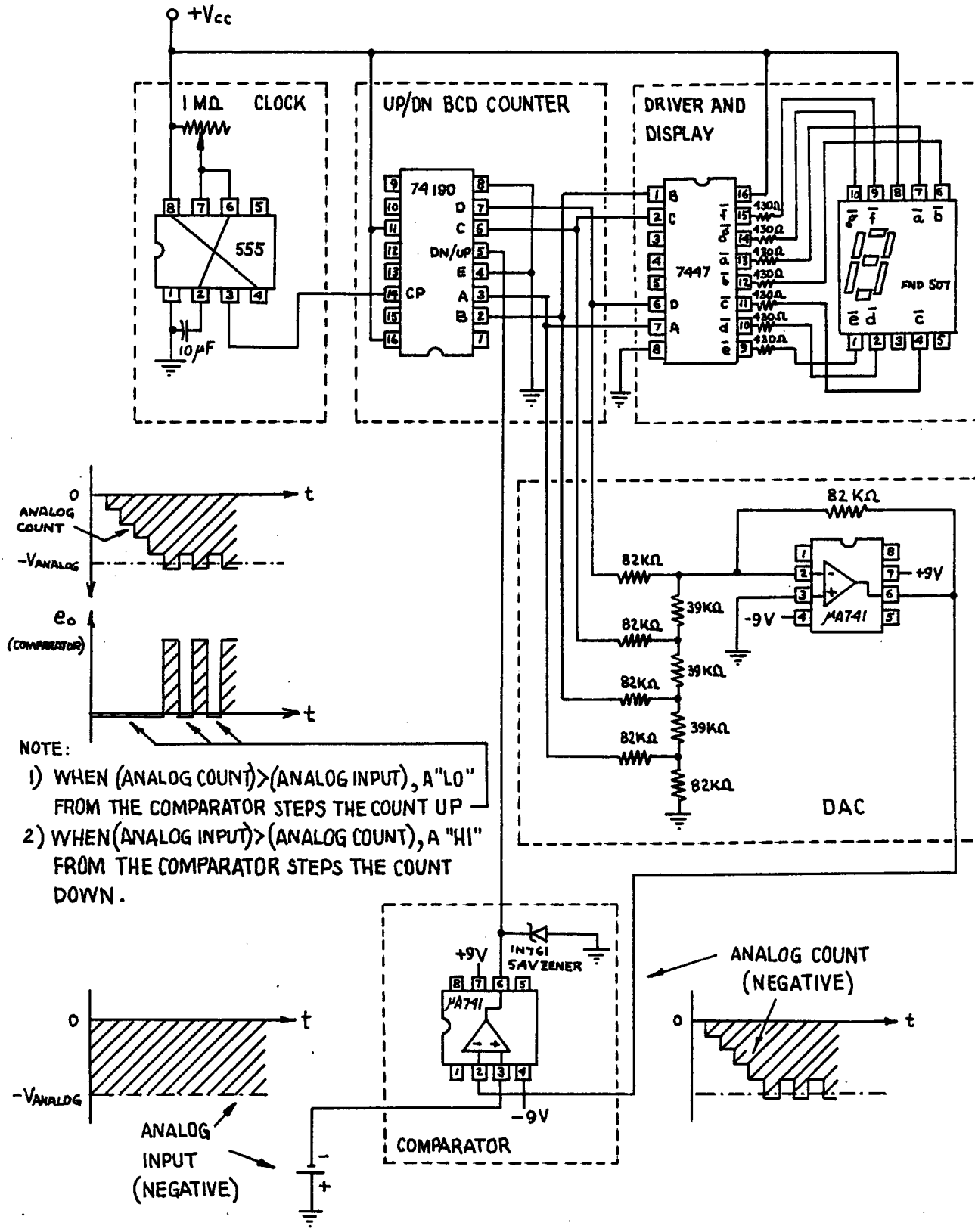
Above HI, when fed into the up/down counter, will step the count down.



Since a comparator cannot determine a balance condition, the next clock pulse will find that the ANALOG COUNT, having been stepped down, is now greater than the ANALOG INPUT. This condition results in a LO that will step the counter up again. Thus, the digital equivalent of an analog input is found when a continuous $\pm$ one-bit results in the counter.

ANALOG TO DIGITAL CONVERTER

TRACKING METHOD



SUCCESSIVE APPROXIMATION

The methods previously described for Analog to Digital Conversion are often referred to as "integration methods". A count is initiated to match the value of the Analog Signal. Each step of the count corresponds to a clock pulse. Devices employing this method are slow but accurate, and not very expensive.

When higher speeds of conversion are required, one must use Successive Approximation Methods. These methods require fewer clock pulses per conversion than the integration types, though they are more expensive.

Successive approximation may be of the "analog type" or of the "ladder type" (digital).

ADC - ANALOG TYPE

This analog type of conversion may be described by the following example.

To measure the unknown volume of liquid in an uncalibrated container, the following procedure may be used:

Four binary weighted measuring containers are used for this example. The volume of each of these containers is a submultiple of the maximum measurable volume V_{ref}. The submultiple volumes are as follows:

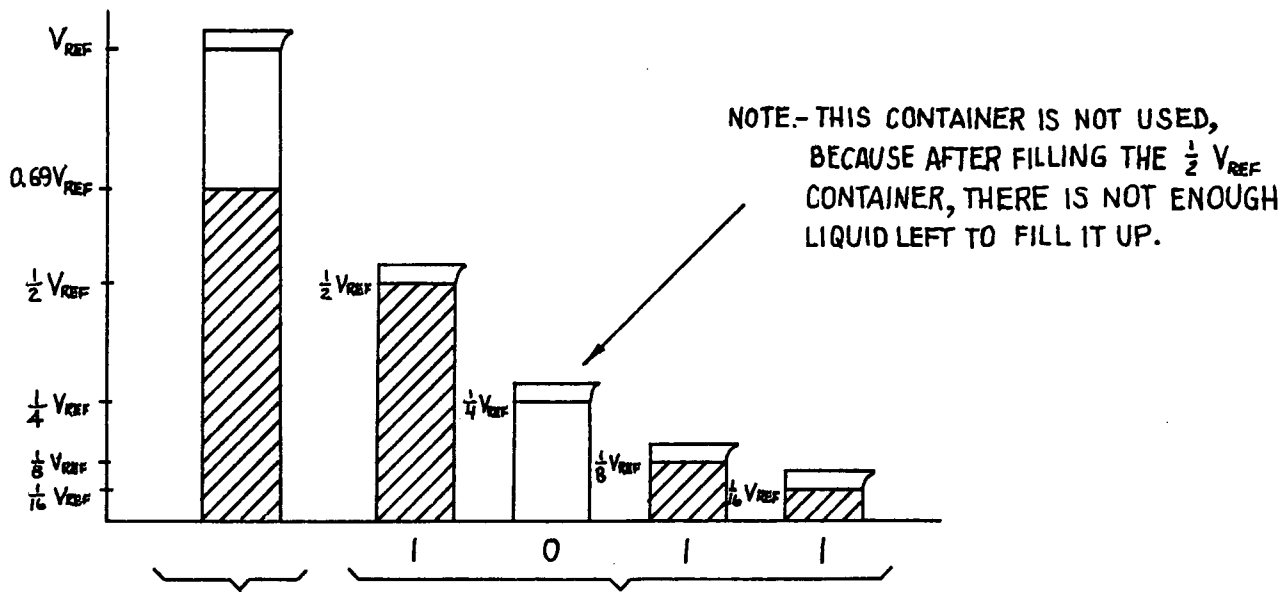
$$\frac{1}{2} V_{ref} , \quad \frac{1}{4} V_{ref} , \quad \frac{1}{8} V_{ref} , \text{ and } \frac{1}{16} V_{ref} .$$

All the measuring containers are to be tried, starting first with the largest one, and then proceeding to the smaller ones. Each container used must be filled to maximum capacity. A full container will indicate a "one" and an empty container a "zero".

Once the unknown volume has been distributed among the four

measuring containers, a four digit read-out will indicate the value of the unknown volume. The small amount left over is the measurement error. This error may be reduced further by increasing the number of binary weighted measuring containers.

EXAMPLE.- Assume that the unknown volume is 0.69 V_{ref}, then by using the above procedure, the following measured volume will result:



(UNKNOWN VOLTAGE) = (SUM OF FULL MEASURING CONTAINERS) + (ERROR)

$$2^{-1}\ 2^{-2}\ 2^{-3}\ 2^{-4}$$

$$\text{MEASURED VOLUME} = (0.\ 1\ 0\ 1\ 1)V_{REF} = (1\times2^{-1}+0\times2^{-2}+1\times2^{-3}+1\times2^{-4})\,V_{REF}$$

$$= (0.5 + 0 + 0.125 + 0.0625)\,V_{REF} = 0.6875\,V_{REF}$$

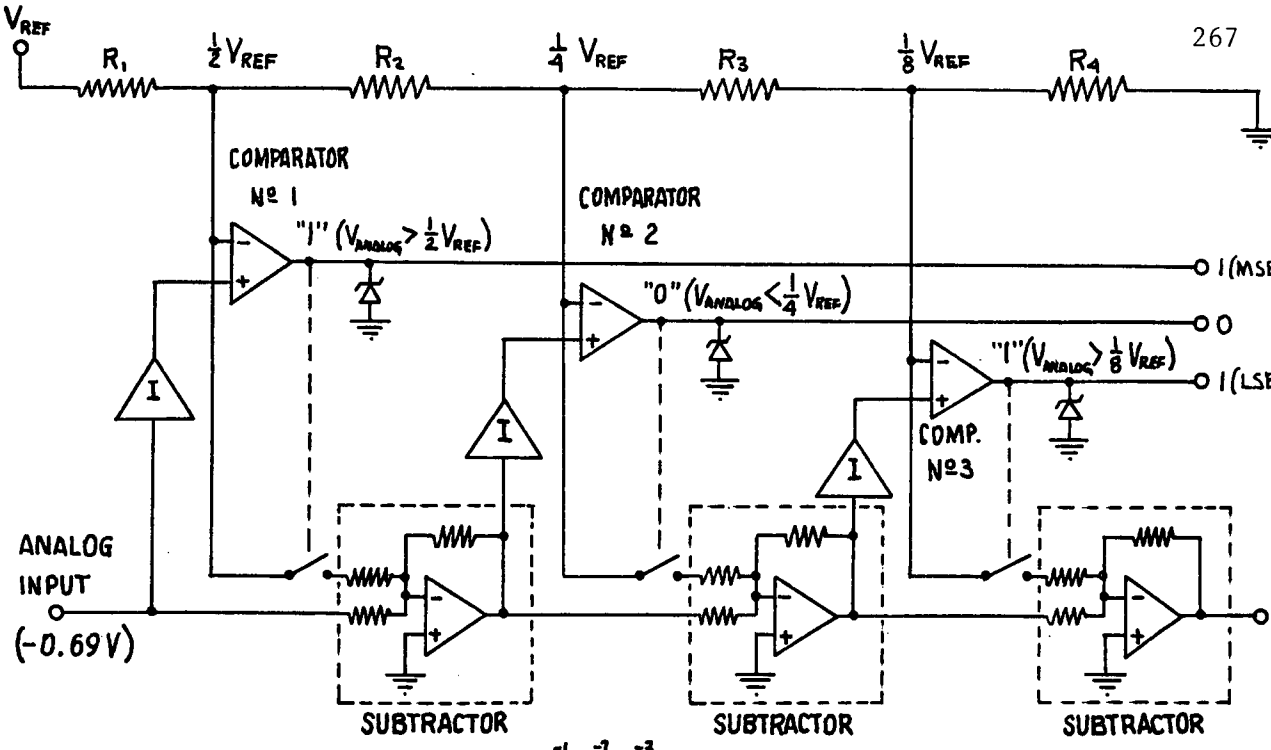
$$\text{ERROR} = 0.0025\,V_{REF}$$

The accuracy of the above results is dependent on:

1.- The accuracy of the standard volume chosen as V_{ref}.

2.- The number of available measuring containers.

One possible circuit implementation, for the above analogy, is given below, where the volumes are replaced by voltages, and the measuring containers are replaced by the results of a comparator, which decides whether a subtraction of voltages should or should not take place.



FOR A 3 BIT OUTPUT (ABOVE) } MEASURED VOLTAGE = $(0.\ 1\ 0\ 1)V_{REF}$ ($2^{-1}\ 2^{-2}\ 2^{-3}$) $= 0.625\,V_{REF}$; ERROR = $0.0625\ V_{REF}$

FOR A 4 BIT OUTPUT (NOT SHOWN) } MEASURED VOLTAGE = $(0.\ 1\ 0\ 1\ 1)V_{REF}$ ($2^{-1}\ 2^{-2}\ 2^{-3}\ 2^{-4}$) $= 0.6875\,V_{REF}$; ERROR = $0.0025\ V_{REF}$

The accuracy of the results in the above circuit is dependent on:

1.- The accuracy of the standard voltage chosen as V_{ref}.

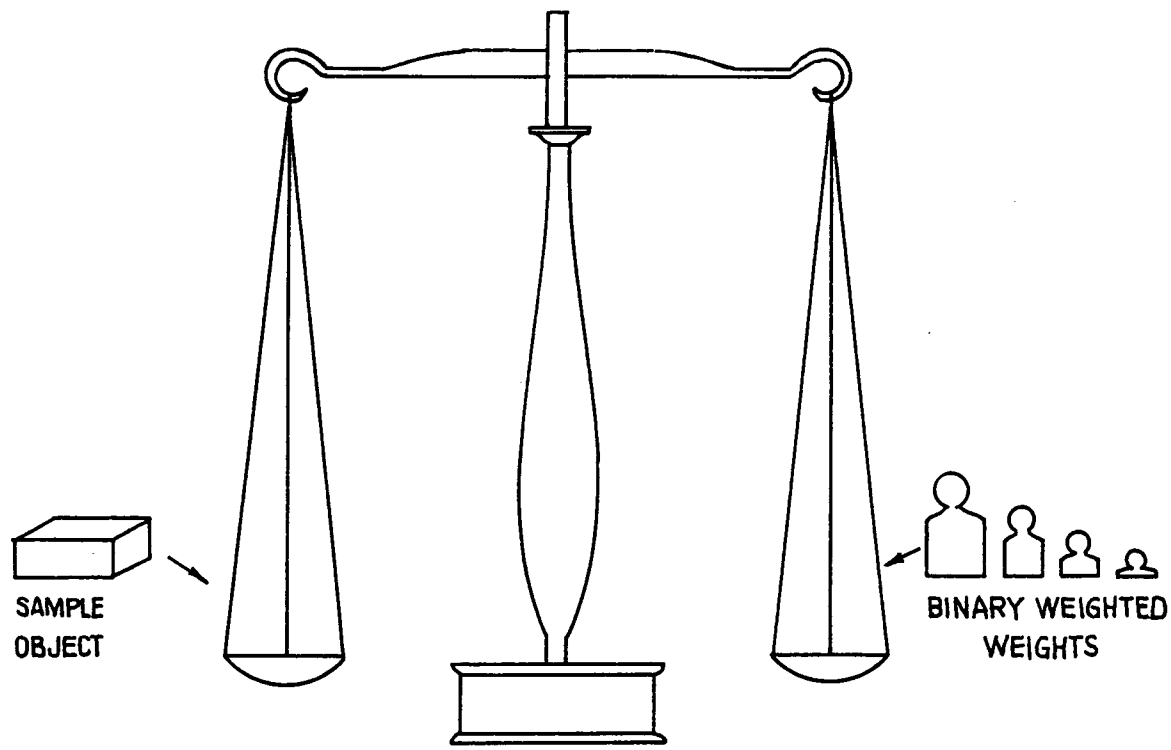
2.- The number of available comparators and subtractors.

VOLTAGE REFERENCES

From the above considerations, it can be seen that the accuracy of the reference voltage is a critical factor in determining the absolute accuracy of its DAC or ADC systems. In electronic circuits, this reference voltage is usually provided by specially designed zener diode circuits. These circuits are temperature compensated to prevent drift or fluctuation due to changes in temperature. A guide for reference voltage circuits is usually supplied by most manufacturers. One of these guides is provided next and is from the "National Semiconductor Linear Data Book".

ADC - LADDER TYPE

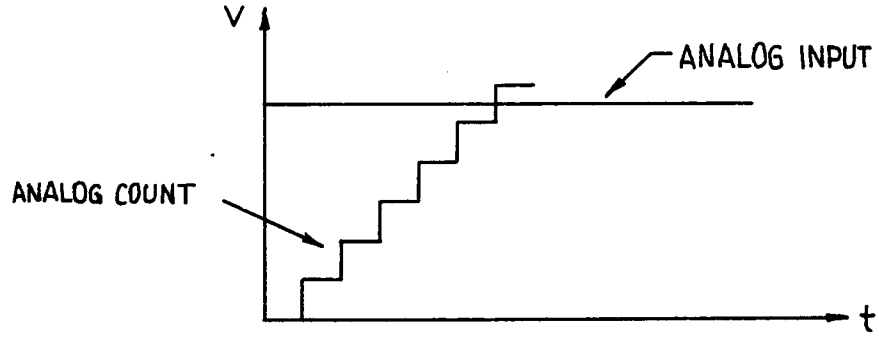
This method of measurement consists of balancing the desired Analog Input in a similar way to the process used to weigh an object on a chemical or apothecary balance.



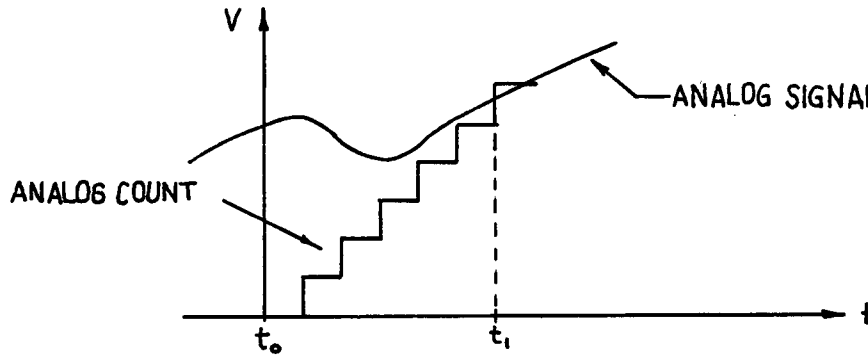
The sample object to be weighed is placed on one side. It is counterbalanced by the heaviest reference weight first. If it is heavier than the sample object, it gets replaced by the next weight or weights, and the procedure is repeated until the smallest weight has been tried and the closest match occurs.

A similar process is used in the ADC0800 Analog to Digital Converter from National Semiconductors. Its specification sheets are included here and were taken from the "National Data Acquisition Book".

When measuring constant values of analog inputs, the time taken for measurement is not important, and any ADC method will do, see the figure below, where an integrator ADC generates the Analog Count:



However, when measuring rapidly changing analog signals, the integrator ADC may give an erroneous answer, see the figure below:



The value of the analog input is known at the time t_1, when the analog count equals the analog signal, but not at the time t_o, when the read-out is desired.

A solution to this problem is to use a faster converter, such as the successive approximation type. Another general solution is the use of "Sample and Hold" circuits.

These circuits are used to measure rapidly changing voltages at specified intervals of time. A sample voltage is taken from those rapidly

varying quantities by charging a capacitor, and then obtaining the digital equivalent of the voltage across the capacitor terminals.

The advantage of these circuits is that taking the sample usually takes less time than carrying out the A-D conversion. Thus, one can know the value of the voltage very close to the time the sample was obtained.

An analogy for the above procedure occurs when one considers making the chemical analysis of river water. Chemical analyses usually include several tests and may not be done on the spot. Therefore, so long as a careful record is kept of the time at which the samples are removed, then the analysis can take as long as necessary.

For very high speed applications, even the successive approximation methods require "sample and hold" circuits. Sample and Hold circuits are available in integrated circuit form.

For ultra high speed applications, the sample and hold circuits include a tracking function, where the sampling capacitor follows the voltage variations of the analog signal at all times. This way, the voltage across the sampling capacitor terminals is readily available for measurement when required, without having to wait for it to charge from a 0 V discharged condition up to the value of the analog input.

This tracking function is analogous to taking the photograph of a fast moving object by following its motion with the camera finder. The object will appear stationary during the lens aperture time, and its picture will not be blurred.

See the attached data specifications for an Ultra High Speed Sample/Track-and-Hold Amplifier, manufactured by Analog Devices, Inc.

POWER SOURCES FOR DIGITAL CIRCUITS

Electronic circuits are powered by two kinds of voltage source. One of them, such as utility outlets, supply an alternating voltage (AC), whereas other sources, such as batteries, supply a constant voltage (DC).

For a given circuit, its different functional blocks may have different DC voltage requirements. As an example, most TTL logic circuits discussed in this book require +5 V, whereas linear systems, like those used for summing and comparing, require from ± 3 V to ± 18 V, see supply voltage requirements for the operational amplifier μA741.

When different voltage levels are needed, those voltage levels can be obtained from different sources. This is an expensive procedure, and a more practical approach is to obtain them from a single source.

The utility outlet supplies AC voltages. These voltages are easy to step up or to step down, by the use of transformers. The resulting AC voltage levels are then rectified and filtered to yield the required constant DC voltage levels.

A given DC voltage level can then be stepped down using voltage dividers, to obtain as many different levels as needed.

However, when the original main source of energy is a battery, while its voltage may be stepped down easily, the process of stepping this same voltage up is not that simple.

Transformers cannot be used to directly step up DC voltages, because transforemers only operate with dynamic voltage changes at their input in order to induce AC voltages at their output.

The special circuits used to step up DC voltages are known as voltage converters. These circuits may use transformers and/or capacitors to raise the supply DC voltage level.

Basically, voltage converters produce an AC voltage from a given DC input. Then, this AC voltage is stepped up by:

a) Using a transformer, where the resulting AC voltage levels are then rectified and filtered, or

b) Using the AC voltage to act on a set of electronic switches to charge or discharge capacitors, so that a voltage doubling effect can take place.

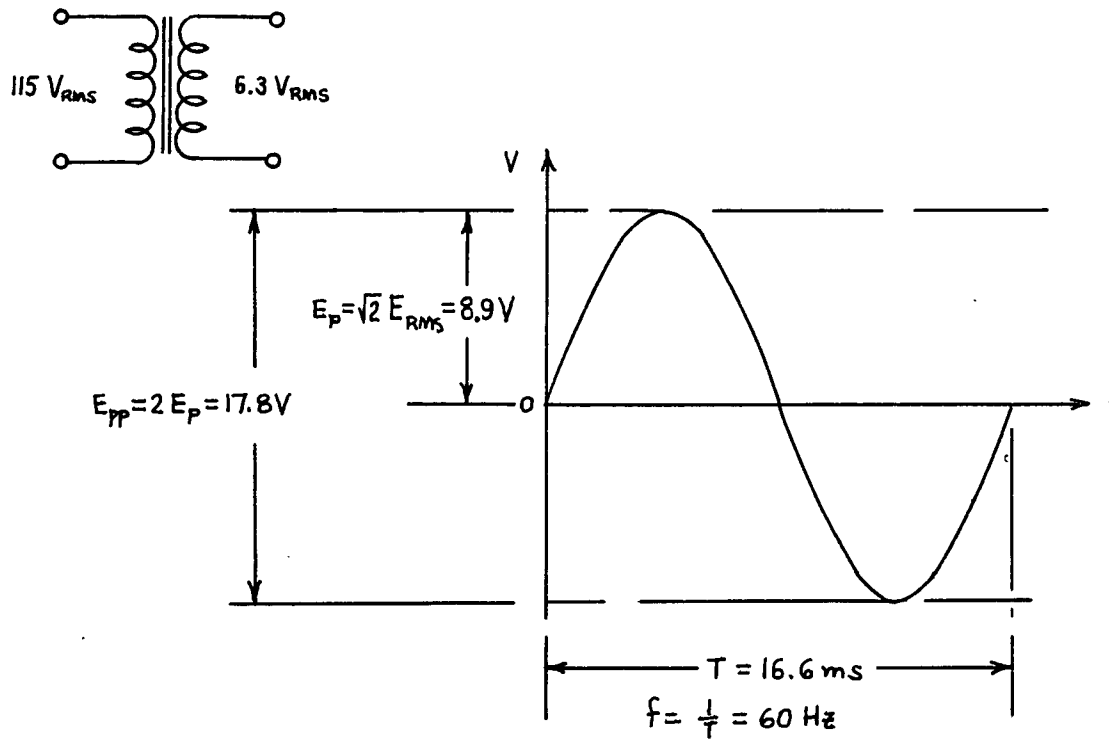
A +5 V POWER SUPPLY

A useful +5 V power supply, adequate for most of the applications suggested in this book, is described below. It operates from the utility AC voltage.

TRANSFORMER

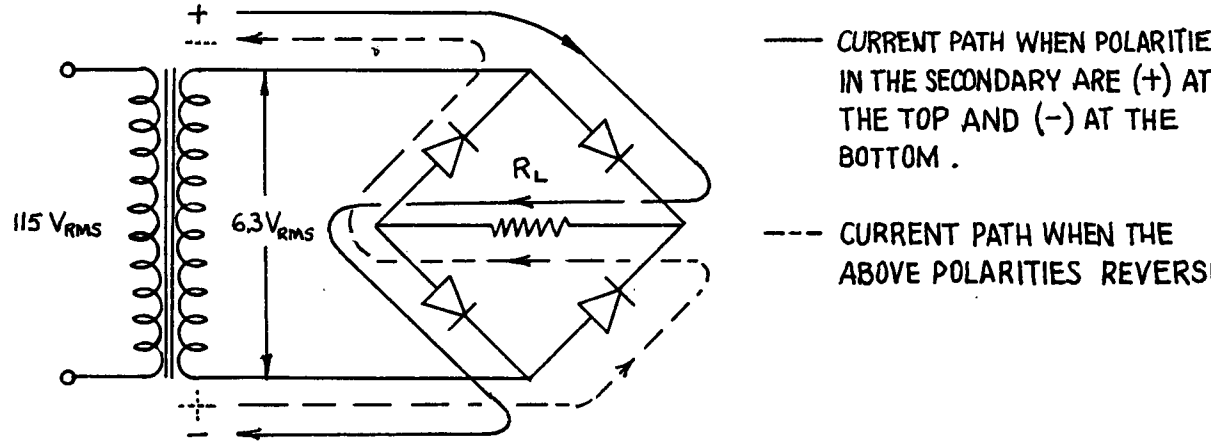
Above power supply includes a transformer made by Hammond, catalog number 166F6, with a transformation ratio of 115 V/6.3 V. It must be noted that transformers are made by many manufacturers to suit a large variety of applications. Manufacturer's catalogs permit the selection of the transformer that is most suitable for a particular application. A typical specification sheet is included at the end of this section, which also lists the above transformer.

When the primary of this transformer is connected to the AC power outlet, it steps the 115 V (RMS) down into a 6.3 V (RMS). The secondary voltage, seen on an oscilloscope, appears as follows:



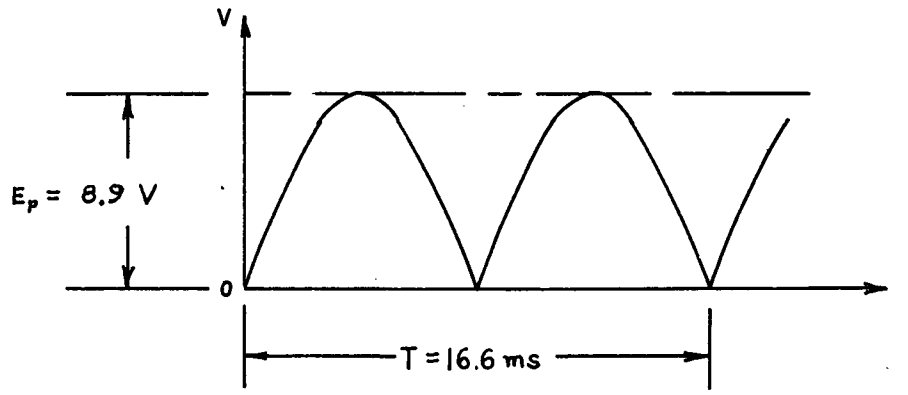
RECTIFIER

A bridge rectifier circuit will provide full wave rectification of the above input. The rectifier bridge can be made by connecting four diodes as shown below.



Notice that conventional current flow is considered in the above figure. Also notice that the graphic symbol for a diode is derived from this conventional flow. Its symbol is an arrowhead pointing in the direction of conventional flow. It also indicates that no conventional current flows against its arrowhead.

In order to observe the rectified output, a dummy load R_L = 2.2 kΩ with 2 W rating may be connected across the rectifier output. The corresponding oscilloscope display is as follows:

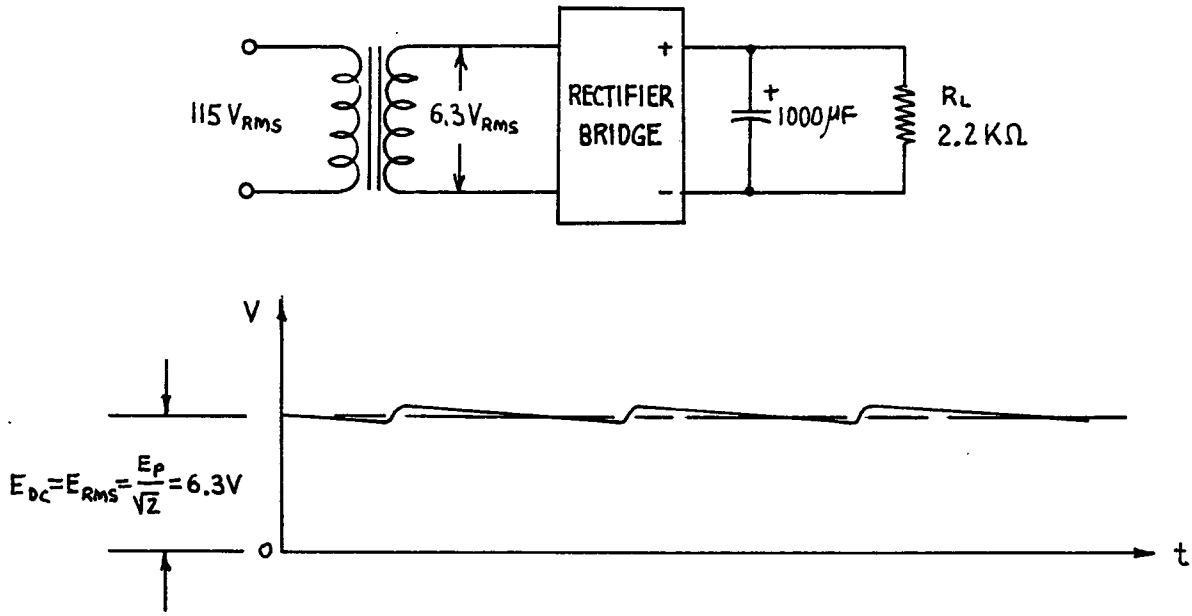


Above bridge may be replaced by one already assembled in a Dual-In-Line package, such as the one available from Varo Semiconductor, Inc., catalog number VM18. This package offers the advantage of reduced space and it is also easy to mount on a strip bread board, of the kind recommended for the assembly of experimental circuits in this book. See the technical specifications sheet for this 1 Amp Dual-In-Line bridge, at the end of this section.

FILTER

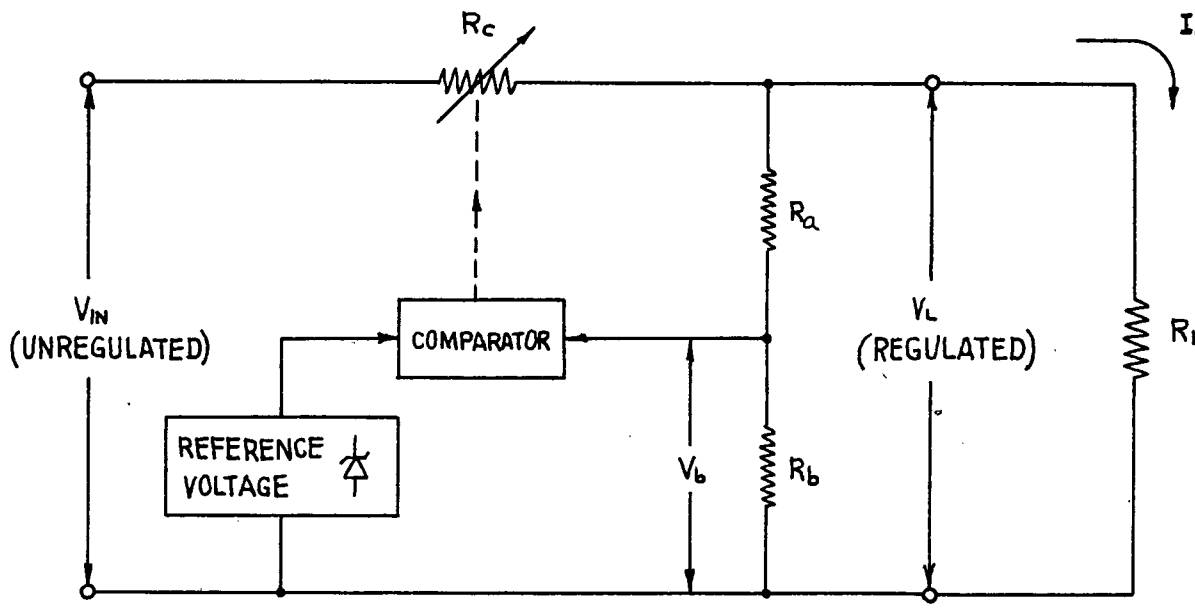
The resulting output from a rectifier is a DC pulsating wave. This wave must be filtered, in order to make the output a constant DC value. A good size capacitor, such as a 1000 μF unit, will produce a fairly smooth output, except for some small amount of voltage ripple. This resulting voltage ripple can be nearly eliminated with the use of a voltage regulator, described next.

Notice that the property associated with capacitors is called capacitance, and it is the property that opposes changes of voltage. This property is analogous to what happens in a reservoir tank, where the drain pipe does not follow the fluctuations that occur in the main pipe used to fill it.



VOLTAGE REGULATORS

Voltage regulators are circuits that control the value of their output voltage, by comparing it with an accurate internally generated reference value. Their input voltage must be greater than the controlled output voltage. Their principle of operation is described next, making reference to the following block diagram.



A sample of the output voltage is obtained from resistors R_a and R_b, which are connected across the load. By voltage divider action, the voltage V_b, across R_b, is proportional to the load voltage V_L.

Above voltage V_b is then compared with the reference value from a zener diode.

The result of this comparison is used to control the current through R_c, and in this way, the load current I_L. R_c may be a transistor circuit, and a change of its biasing results in a change in the current through it.

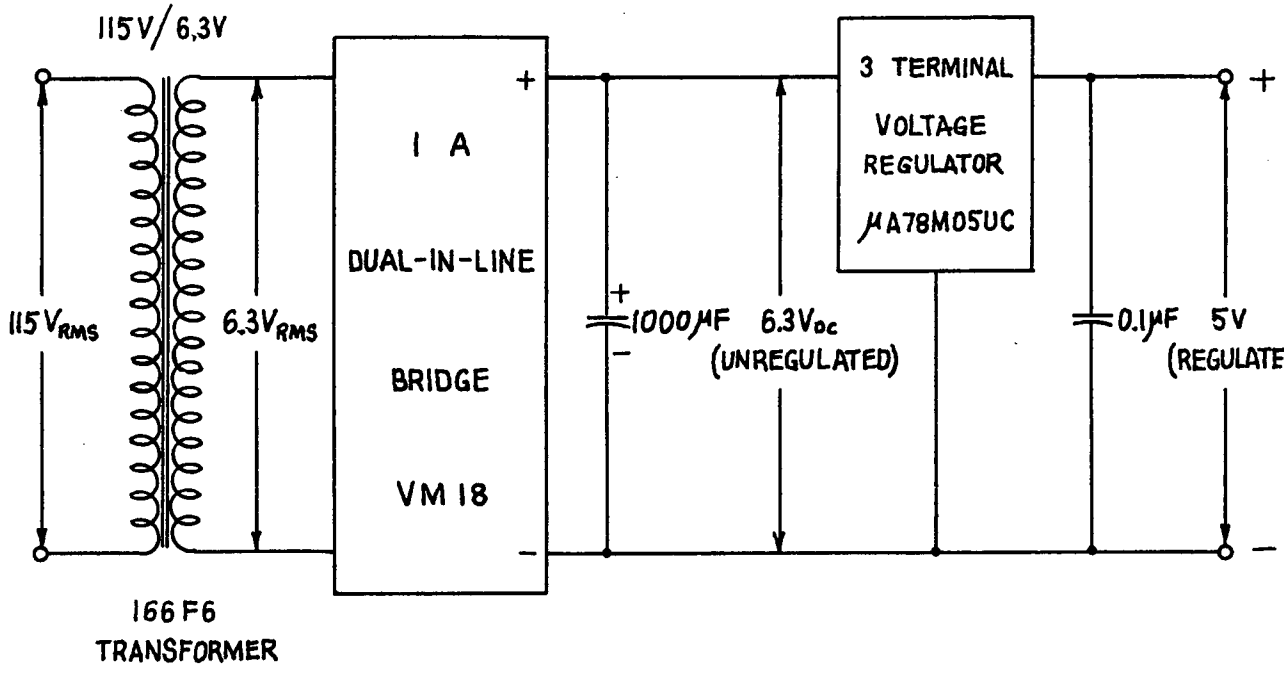
When V_L tries to drop due to either a drop in V_{in} or an increase in I_L, because of additional load requirements, then the comparator will cause R_c to decrease, restoring V_L to its regulated value.

Also, when V_L rises, due to either a rise in V_{in} or a decrease in I_L, because of a reduction in load requirements, then the comparator will cause R_c to increase, which once again restores V_L to its regulated value.

This regulating action effectively causes the regulator to act as a filter.

Voltage regulators are commercially available as integrated circuits. For most of the examples in this book, where the V_{cc} requirements are +5 V, the voltage regulator μA78M05UC was found satisfactory, since it can deliver up to 500 mA of output current, i. e. 200 mA above the output current of the transformer 166F6. When larger amounts of current are required, it is recommended to consult the manufacturer's data sheets. For your convenience, the technical specifications for the μA78M05UC have been included at the end of this section.

The complete power supply is shown below. The 0.1 μF capacitor has been added across the output to by-pass any high frequency ripple that may be present.



VOLTAGE CONVERTERS

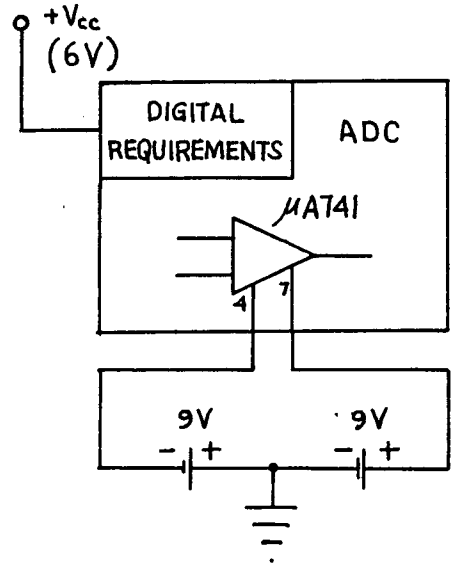
Above +5 V power supply is very useful for most digital functions. However, in systems where analog functions are used, such as DAC's and ADC's, commonly found in Data Acquisition Systems, a -5 V supply should also be made available.

Rather than using two separate supplies, the -5 V voltage may be derived from the existing +5 V source, using a voltage converter.

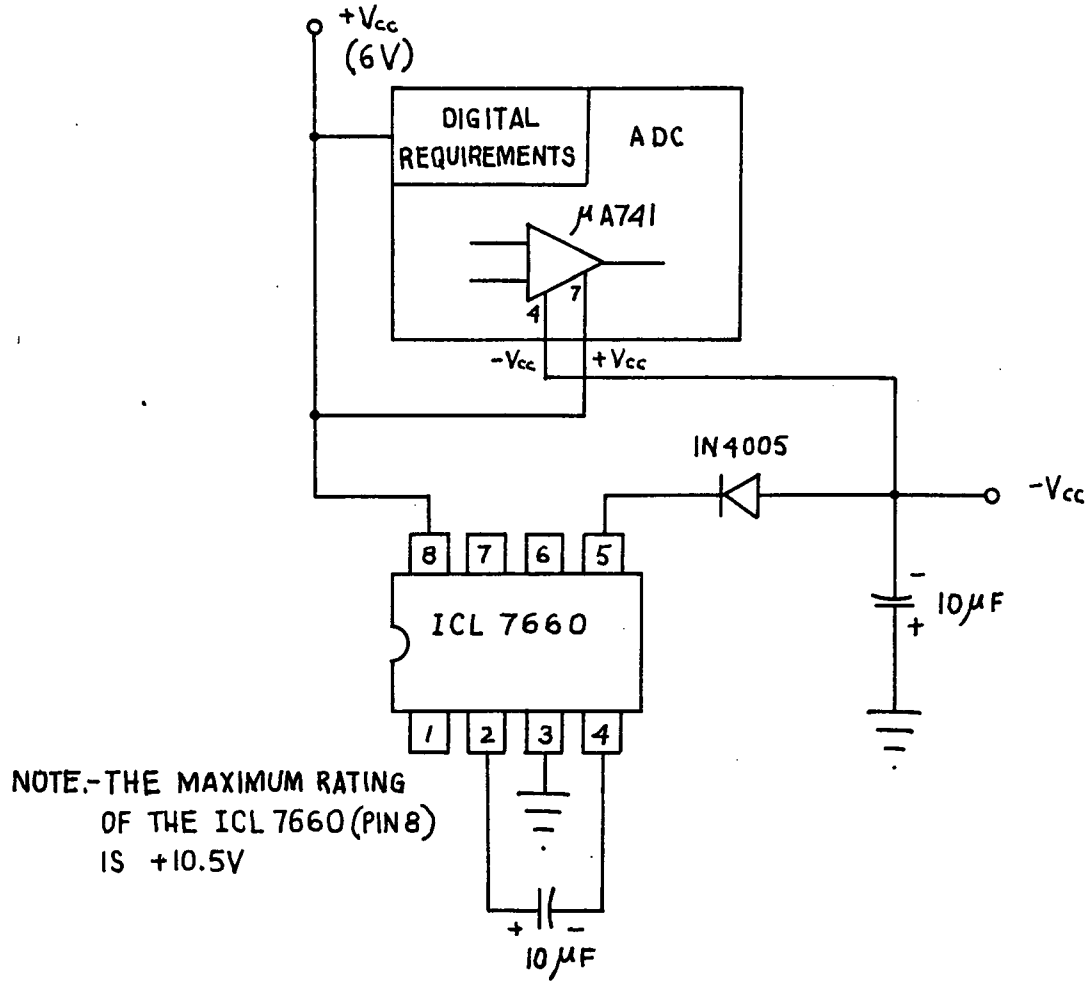
The ICL 7660 voltage converter is commercially available from Intersil, Inc.. It generates an AC voltage that acts on electronic switches. These switches charge or discharge capacitors and produce a voltage doubling effect. The technical specifications for the ICL 7660, which comes in a dual-in-line package, are included at the end of this section.

This voltage converter may be used to bias the μA741 operational amplifiers used in the Analog to Digital Converters discussed in this book.

The three bias supplies used for the above ADC's are represented in the following block diagram. These supplies are: a 6 V source for digital circuits, and two 9 V sources for the analog components (μA741).



The above three bias supplies may be replaced by a single one ($+V_{cc}$), and an ICL 7600 Voltage Converter. The peripheral components and connections for the voltage converter are shown below:



Notice that in the sections for DAC's and ADC's, the operational amplifiers were biased with ± 9 V supply voltages. The DAC's were designed to yield maximum output values, so that the staircase waveforms could be observed clearly with a Volt-Ohmmeter.

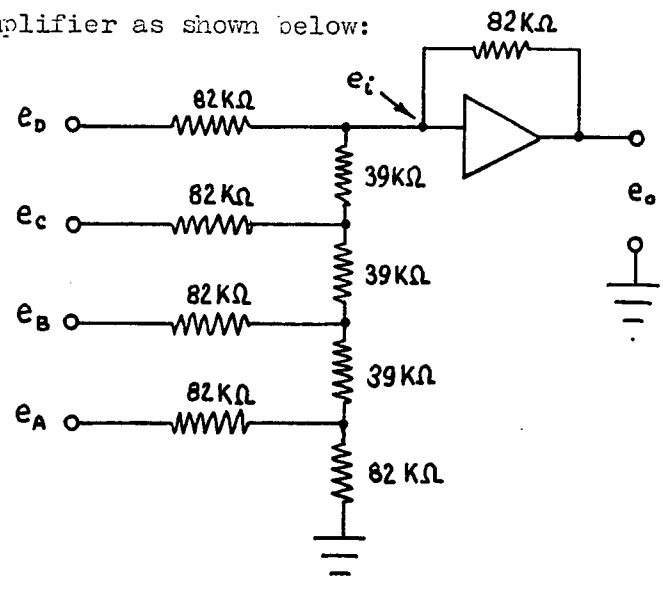
The following two basic considerations were met, applicable to operational amplifiers in the Summing Mode:

1.- Its input values should not exceed the supply voltage. The right choice of resistors in the resistive ladder attenuator was used to meet this requirement.

2.- The output voltage should not exceed the supply value. This requirement was achieved by choosing the right value of feedback resistors.

Since the bias for the operational amplifiers will be reduced to $\pm$6 V, we must make sure that above requirements are still met.

Voltages e_D, e_C, e_B and e_A when taken from the true outputs of a 7490 BCD counter, are approximately equal to 4 V. These voltages are applied to the summing amplifier as shown below:



The maximum input to the operational amplifier is:

$$e_{i\ max} = \frac{e_D}{2} + \frac{e_C}{4} + \frac{e_B}{8} + \frac{e_A}{16} = \frac{4}{2} + \frac{4}{4} + \frac{4}{8} + \frac{4}{16} = 3.75\ V$$

The above voltage is less than the new supply voltage for the μA741, (i. e. $\pm$6 V), and condition (1) is met.

Regarding condition (2), the output of the operational amplifier is given by:

$$e_o = -\frac{R_{FB}}{R_{in}}\left(\frac{e_D}{2} + \frac{e_C}{4} + \frac{e_B}{8} + \frac{e_A}{16}\right)$$

Where R_{FB} was chosen to be twice the value of R_{in} (R_{in} = 39 kΩ), so that a larger output could be measured more easily on a Volt-Ohmmeter.

When all the input voltages are present:

$$e_{o\ max} = -\frac{2R_{in}}{R_{in}}\left(\frac{e_D}{2} + \frac{e_C}{4} + \frac{e_B}{8} + \frac{e_A}{16}\right) = -2(3.75) = -7.5\ V$$

This output voltage now exceeds the new supply values of ± 6 V, and condition (2) is NOT satisfied.

If the circuit is not modified, its operation will result in the loss of the higher counts. When the output voltage attempts to exceed the supply bias, the inputs to the operational amplifier are no longer virtual grounds.

A satisfactory solution is to reduce the output voltage by reducing the value of the feedback resistor.

For $R_{in} = 39\ k\Omega$,

a) If R_{FB} is made to be 39 $k\Omega$ then: $e_{o\ max} \cong -3.75$ V

b) If R_{FB} is made to be 22 $k\Omega$ then: $e_{o\ max} \cong -1.875$ V

Above steps reduce the output voltage considerably and thus are not easily measured with a Volt-Ohmmeter, but they are readily observed on an oscilloscope.

THE INTERFACE OF ELECTRONIC SYSTEMS

The term INTERFACE refers to the interconnection between two pieces of equipment having different functions. In digital systems, interfacing is used to:

a) Collect and transmit information from equipment external to a digital system, into this latter system. This operation is referred to as DATA ACQUISITION. Data from the external equipment may be in analog form, in which case, it must be converted first into its digital equivalent. ADC's are used to perform this conversion.

b) Send messages to external devices, in order to alter the operation of other systems. This is a CONTROL FUNCTION that often requires digital data to be converted into its analog equivalent. When this conversion is required, a DAC must be used.

Digital systems that include a Data Acquisition System(DAS), as well as a Control System, are used to monitor, analyze and control real time events, such as: Continuous Processes in Manufacturing, Flight Control Systems, Navigation Systems, Security and Alarm Systems, Fire Control Systems, Machine Controls, etc.

This section considers the development of an interface system, to control illumination devices. The state of these illumination devices will be defined by the logical state of a digital circuit. The procedures outlined here may be made extensive to other similar applications.

INTERFACING A DIGITAL CIRCUIT TO AN AC, 120 V DEVICE

This interfacing consists of using the state of a JK master/slave flip flop to control the ON-OFF condition of a 120 V lamp. The lamp is powered by a 120 V, 60 Hz system, whereas the flip flop is powered by a 5 V DC supply. The interface circuit will interconnect these two electrical systems.

The output from a flip flop has very low current drive, therefore a simple approach is to use the logical "0" or logical "1" from the flip flop to drive a 2N2222 transistor. This transistor will provide the necessary current to drive other electronic switching devices, such as Silicon Controlled Rectifier Diodes (SCR), or Triacs, as well as Electromechanical relays.

As an example of driving requirements, consider the following typical devices:

a) An SCR GE-X1 requires a triggering current of 15 to 25 mA at 1.2 to 2.5 V.

b) A Triac Q2004L4 requires a triggering current of 25 mA at 2.5 V.

c) A small electromechanical relay, such as the R10-E1-Y2/V52, requires an energizing current of 0.115 A at 6 V. This current is calculated, from the appropriate technical specifications, as follows:

$$I = \sqrt{\frac{P}{R}} = \sqrt{\frac{0.69}{52}} = 115 \text{ mA}$$

The technical specification sheets for the SCR GE-X1, for the Triac Q2004L4 and for the relay R10-E1-Y2/V52, are included at the end of this section.

ELECTRONIC SWITCHING DEVICES

A triggered SCR will act as a regular diode, conducting in only one direction. When the SCR is connected in series with a 60 Hz system, it will conduct only on every other alternation. Therefore, a lamp in series with the SCR will glow on every other alternation and will produce only half the amount of light compared with a direct connection to the power main.

A Triac is a back to back connection of two SCR's. When connected in series with a lamp, this feature enables the lamp to be operated at full brightness.

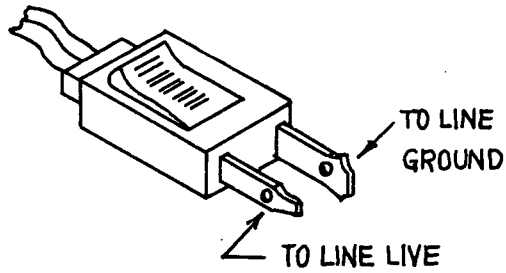
Each one of these two devices has its advantage as well as its shortcoming. The SCR will prolong the life-time of the lamp, by allowing the lamp to operate only at half brightness, whereas the Triac permits full brightness but a shorter life-time.

The power requirements to trigger an SCR are similar to those of a Triac. Both require low current and low voltage to be triggered.

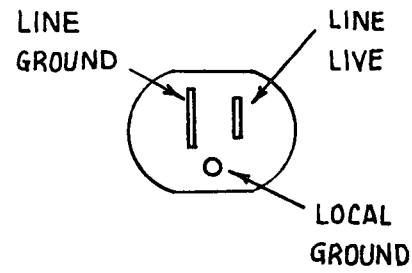
The following circuits control the ON-OFF condition of external devices according to the state of a digital flip flop. They use either one of the above electronic switching devices. The following precautions must be observed when assembling these circuits.

CAUTION.- Because the digital system and the power main share a common connection, the following precautions must be taken:

1.- A polarized plug must be used to ensure that the ground of the line is always connected to the common of the circuit.



POLARIZED PLUG



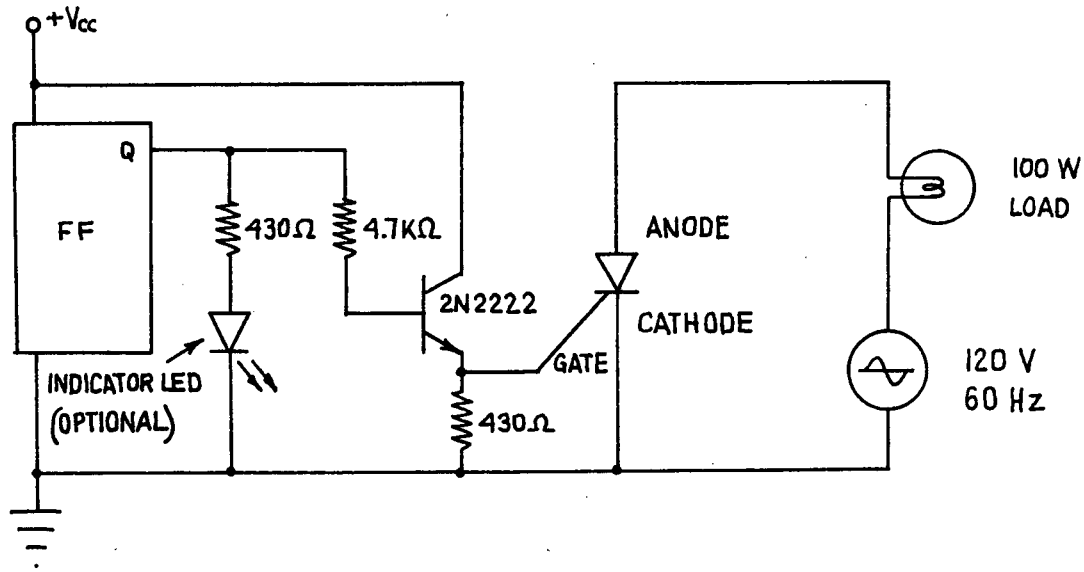
UTILITY OUTLET

2.- The casing for the circuit must be made of non-conducting materials, such as plastic or wood, and the circuitry must not be allowed to touch the casing.

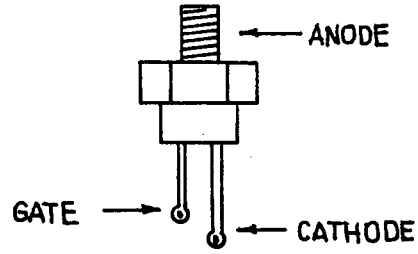
3.- An isolation transformer should be used if tests are to be made on the circuit, such as oscilloscope measurements.

COMMON COLLECTOR DRIVER

This circuit uses a transistor 2N2222 to drive the gate of an SCR. The transistor is connected in the Common Collector mode, therefore, the signals into its base are not inverted when taken out from its emitter. Consequently, when the Q output from the flip flop is a logical HI, the lamp is switched ON, and the same lamp is switched OFF when the Q output becomes a LO.



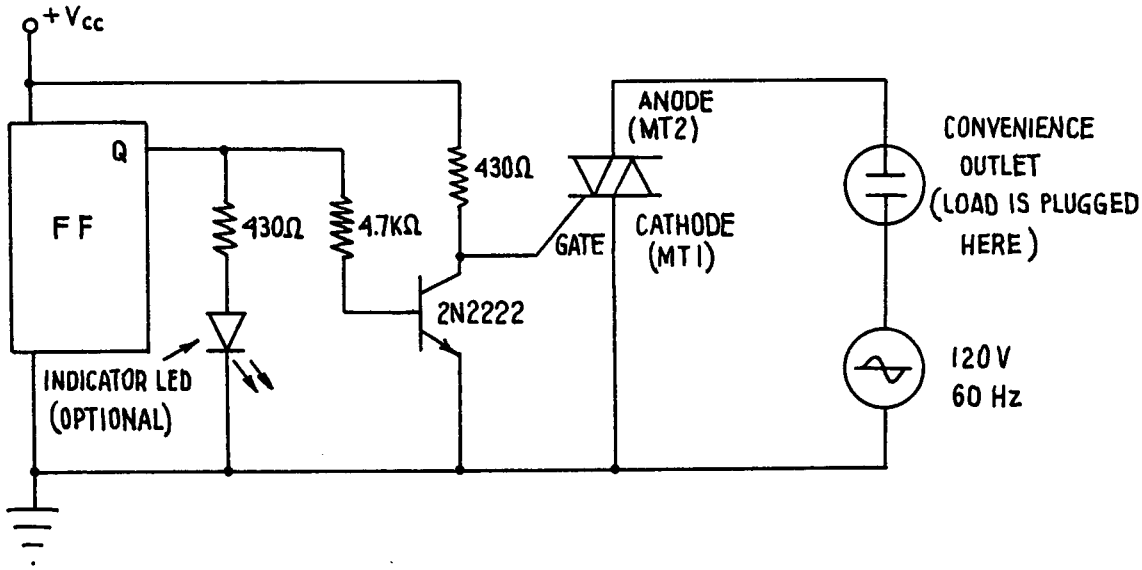
The physical configuration of the GE-X1 is the following:



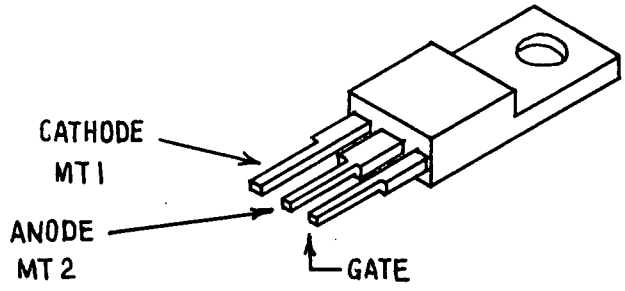
Note.- The above SCR must be mounted on a Heat Sink in order to dissipate the generated heat of the device.

COMMON EMITTER DRIVER

When inversion of the digital signal is desired, the 2N2222 transistor may be connected in the Common Emitter Configuration, as shown below. The signals into the base of the transistor will now be inverted when taken out from its collector. Thus, the load will be switched ON whenever the Q output from the flip flop is a logical LO, and the same load will be switched OFF when the Q output becomes a logical HI. In this circuit, a Triac performs the electronic switching function.



The physical configuration of the Triac is the following:



Note.- The above Triac must also be mounted on a Heat Sink to dissipate the generated heat.

Caution.- The leads of the Triac must be insulated to prevent possible shorts.

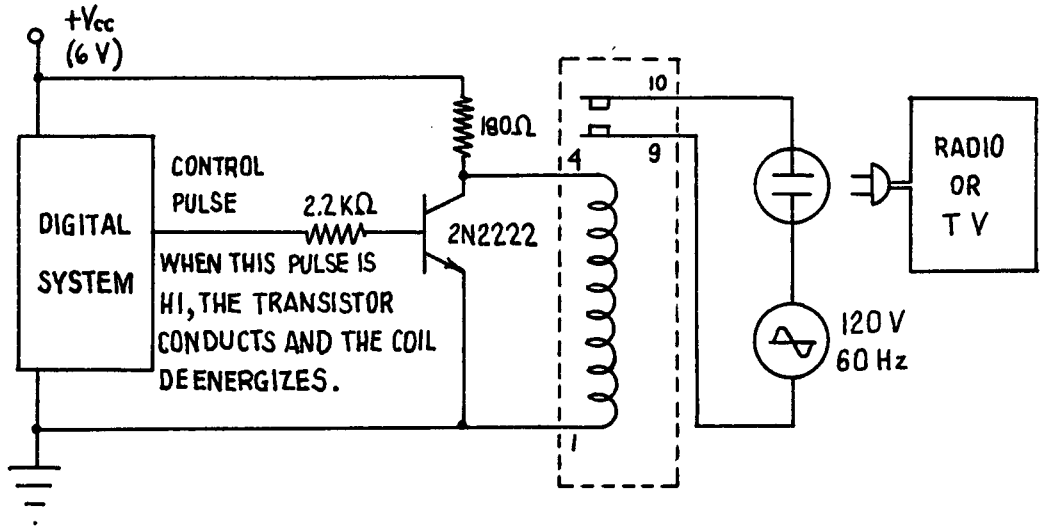
OPTOISOLATORS

Optoisolators may be used to isolate the digital system from the power line. The control pulses from the digital system are then transferred through a beam of light into the controlled system. See the technical specification sheet, at the end of this section, for a GENERAL INSTRUMENT Optoisolator, catalog number 6N138, 6N139.

Optoisolators protect the digital system from possible power overloads in the 120 V line. However, two separate power supplies are required, and one of them still has to share a common connection with the power main.

ELECTROMECHANICAL RELAYS

Relay contacts close by electromagnetic induction, and their coils may be completely isolated from the power main. See the following circuit diagram:



Some of the shortcomings for electromechanical relays are:

a) They require more power to become energized than the power used by electronic switching devices.

b) Because of their moving components, they lack the fast switching capabilities needed in high frequency applications.

c) They are more expensive than electronic switches.

They have the following advantages when rapid switching is not essential:

a) When activated, their contacts conduct AC signals during a full cycle, without the loss of alternations.

b) Because their contacts are not connected electrically to their coil, they do not require too many isolation precautions.

An example of a practical application of relays is in Digital Alarm Clocks. The coil is connected to the Digital System, and the contacts may be connected in series with the power line, to activate a radio or a

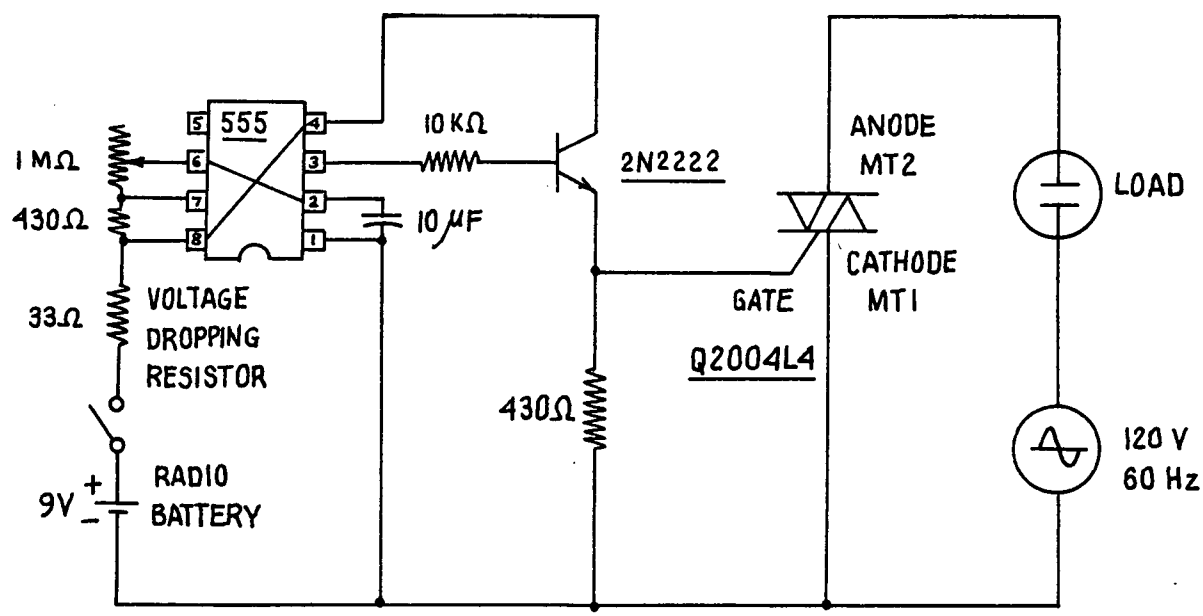
television set. Thus, the control pulses generated in the clock may be used to:

a) Automatically activate a radio or TV set at a predefined time, or

b) Automatically disconnect the above appliances, after a predefined period of operation.

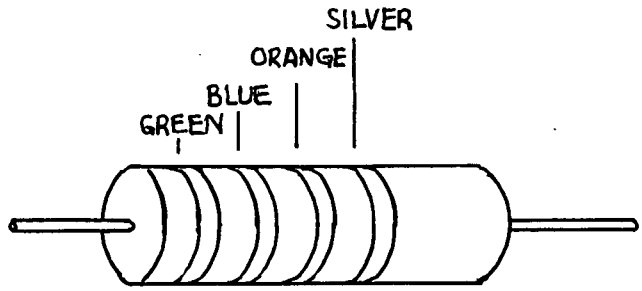
VARIABLE SPEED FLASHER

The following circuit may be used to turn on or to turn off a lamp or a string of lamps, such as those used to decorate Christmas trees. It consists of a 555 timer with a rheostat to manually control its frequency of oscillation. The interfacing circuit is one of those discussed in this section. The same precautions previously mentioned for circuits that share a common connection with the power main are applicable, and must be observed.



COLOUR CODE FOR RESISTORS

CONSIDER A RESISTOR WITH COLOUR BANDS AS SHOWN BELOW :



EACH BAND INDICATES { FIRST SIGNIFICANT FIGURE | SECOND SIGNIFICANT FIGURE | NUMBER OF ZEROES | TOLERANCE

THE EQUIVALENT DIGIT FOR EACH COLOUR IS : (SEE TABLE BELOW) { 5 | 6 | 0 0 0 | ± 10 %

THEREFORE, THE RESISTOR SHOWN ABOVE HAS AN OHMIC RESISTANCE OF : 56 000 Ω ± 10 % .

COLOUR CODE TABLE	
COLOUR	DIGIT
BLACK	0
BROWN	1
RED	2
ORANGE	3
YELLOW	4
GREEN	5
BLUE	6
PURPLE	7
GRAY	8
WHITE	9

TOLERANCE TABLE	
COLOUR	PERCENT
NONE	± 20 %
SILVER	± 10 %
GOLD	± 5 %
RED	± 2 %

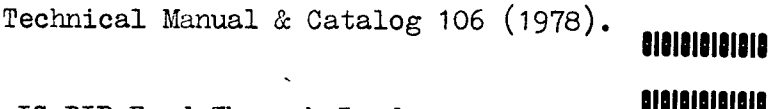
A2

MAKING A PC BOARD

1.- LAY OUT

Do the lay out on Mylar. Use the matted side to apply Slit Tape, Donut pads, IC DIP Feed Through Leads, Lettraset Letters, etc. See Technical Manual & Catalog 106 (1978).

e.g.



IC DIP Feed Through Leads ---------- 6781 (pg.32)

Slit Tape: 0.015" x 20 yds ---------- 201-015-11 (pg.57)

0.040" x 20 yds ---------- 201-040-11 (pg.57)

0.050" x 20 yds ---------- 201-050-11 (pg.57)

Donut Pad (0.093") ---------- D137 (pg.60)

Donut Pad (0.100") ---------- D101 (pg.60)

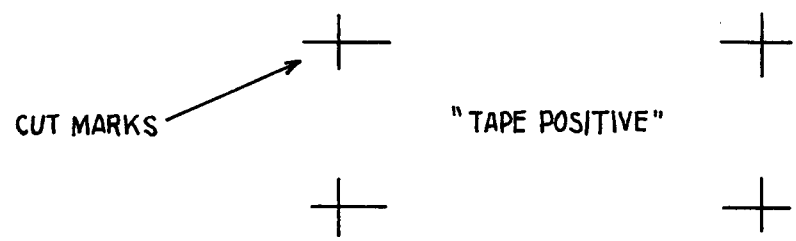
2.- MULTIPLE LAYOUTS

Multiple Layouts can be ordered from places like:

Blair Behnsen/ 835 Cambie / ph. 684-6581

GDL Graphics / c/o Larry Wells / ph. 685-2358

Make CUT MARKS on your original tape positive, so that the multiple layouts just overlap on those cut marks.



Multiple layouts are made on sheets with the following standard dimensions:

10" x 12" ; 8" x 10" ; 14" x 17"

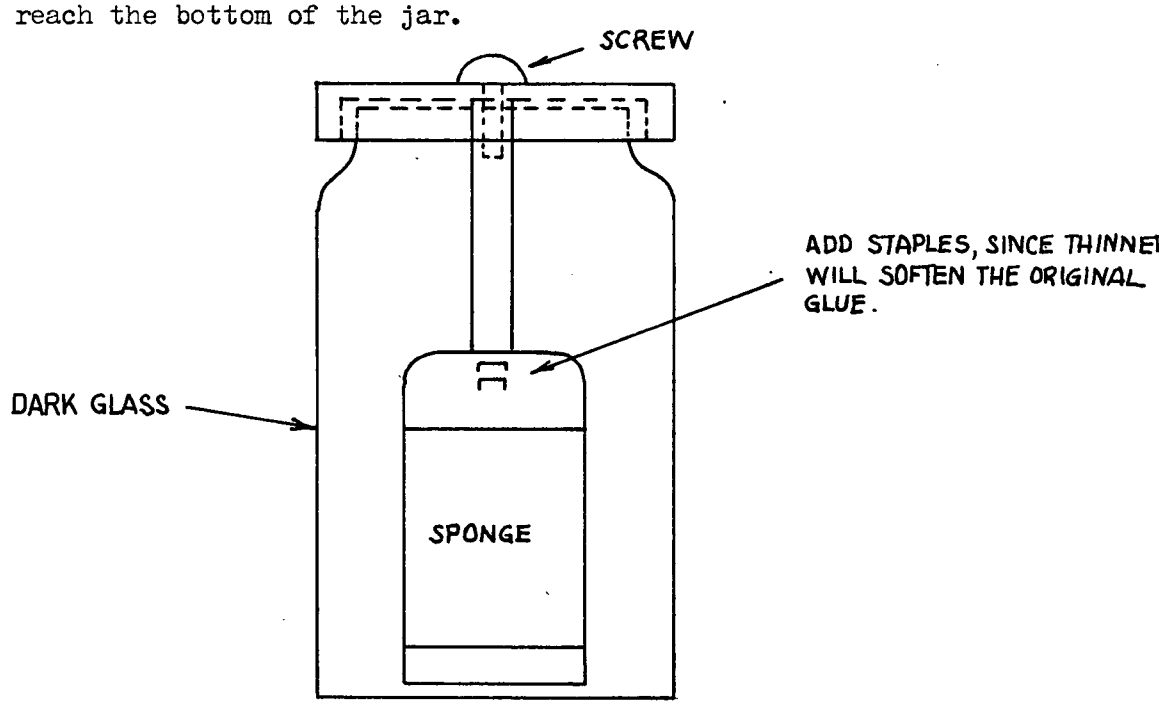
Reproduction shops will provide both, a Positive and a Negative of the reproduced tape positive.

Note.- For etching purposes, it is advisable to use only the Positive Slide, since it calls for chemicals that are not flamable and which do not have a bad smell.

3.- Sensitizing the Copper Covered Board

a) Cleaning the Board.- The board must be clean. Cleaning is done using "SCRUB CLEAN POWDER". This powder is applied with a sponge and water in the same way one uses any other cleaning powder. The scrubbing on the board is done in one direction only, until all oxidizing marks are removed. A clean board loses some of its copper glow but looks very uniform in colour. Make sure the board is properly dry before proceeding to the next step.

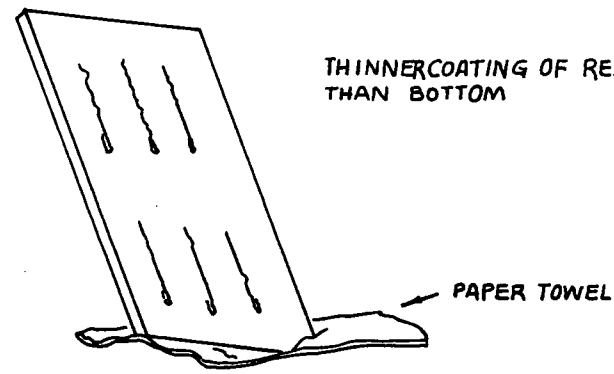
b) Applying Photo Resist (Shipley for Positive Slides).- Buy a DeCoupage Brush and attach to the cover of a dark glass jar. The brush should reach the bottom of the jar.



Combine $\frac{3}{4}$ parts of Resist to $\frac{1}{4}$ part of Thinner.
Using the brush, apply resist on clean board horizontally ($\rightleftarrows$) and then vertically ($\downdownarrows$). Let the resist to completely dry by resting the board on a paper towel for 15 min to $\frac{1}{2}$ hour. The use of a heat gun is recommended, for it dries as it cures. An oven may be used, when set at 150° for $\frac{1}{2}$ hour, however, the oven will be left smelling pretty bad.

A hot drier may also be used. There is no need to have a dark room during this step.

Note.- Due to the action of gravity, the resist will drip down, leaving the upper portion with a thinner cover of resist than the lower portion.

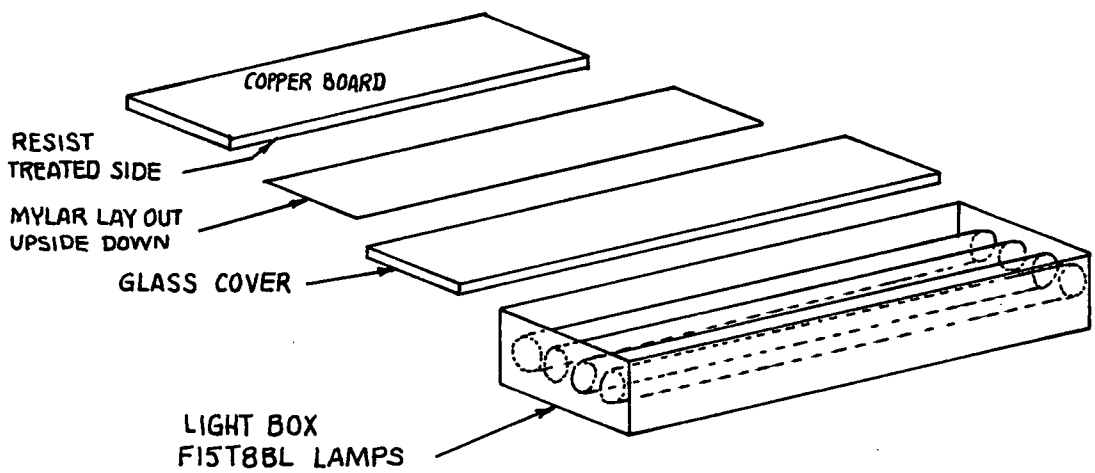


This will cause the upper part to expose more rapidly and to develop quicker than the bottom portion.

To prevent above discrepancy in thicknesses, a turntable may be used to dry the board.

4.- EXPOSURE

a) Use four equally spaced lamps (F15T8BL) inside a glass covered box.



CAUTION.- These lamps produce short-wave ultraviolet light. At these frequencies, damage to unprotected eyes is permanent. Avoid looking at these lamps when they are lit.

b) Place the mylar layout upside down

c) Place the copper board on top with the resist treated side facing the light box.

d) Expose to light. Different times may be tried. About 1½ minutes is an expected average. Optimum time can be found by trial.

5.- DEVELOPMENT

Use Shipley Developer. Mix one part of this developer to eight parts of water. Wash and Dry.

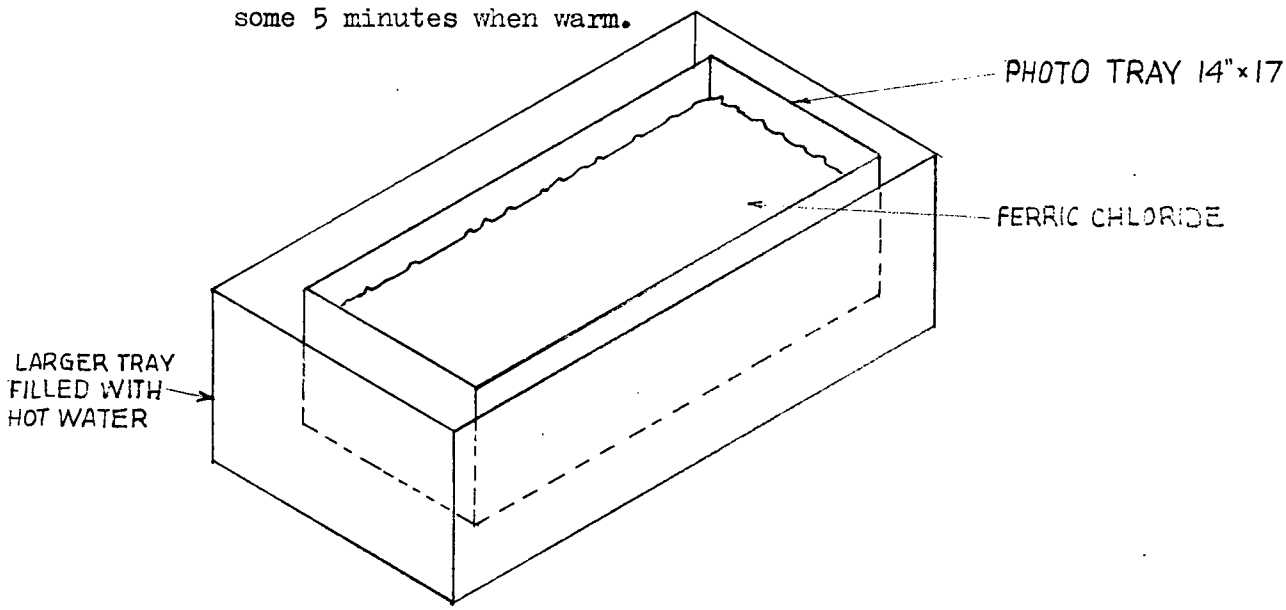
Development comes as a negative. The exposed portions turn out purple and the unexposed parts (circuit lines) come out red.

Note.- If the board was not exposed long enough, the lines will wash out.

6.- ETCHING

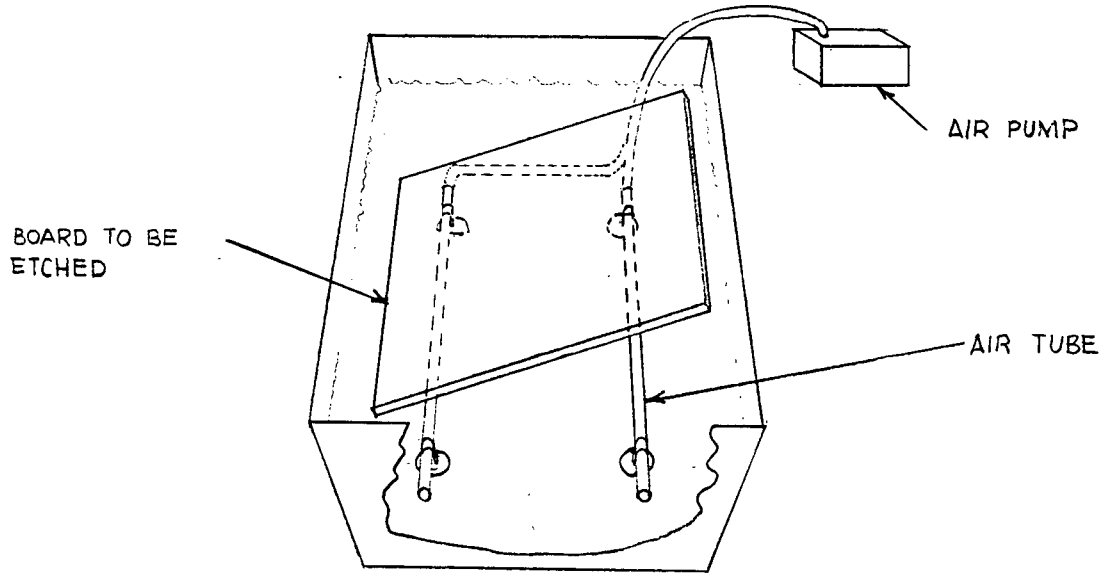
Use warm ferric chloride, heated to 130°F. A double tray may be used to warm the ferric chloride.

Note.- Cold FeCl takes longer to etch a board, up to ½ hour, instead of some 5 minutes when warm.



Caution.- Use rubber gloves and a laboratory coat. Ferric Chloride stains do not wash out.

Clean etching can be obtained by using the air bubbles from two air tubes and an air pump. The tubes and pump may be acquired at a retailer shop of acquarium supplies.



Make sure the board is at an inclined plane, so that the bubbles can wash the etched copper particles as they move upwards. Wipe excess copper on a sink to prevent the FeCl from getting too dirty.

7.- FINISHING THE PRINTED CIRCUIT BOARD

a) Wash the Printed Circuit Board on a sink.

b) Dry it.

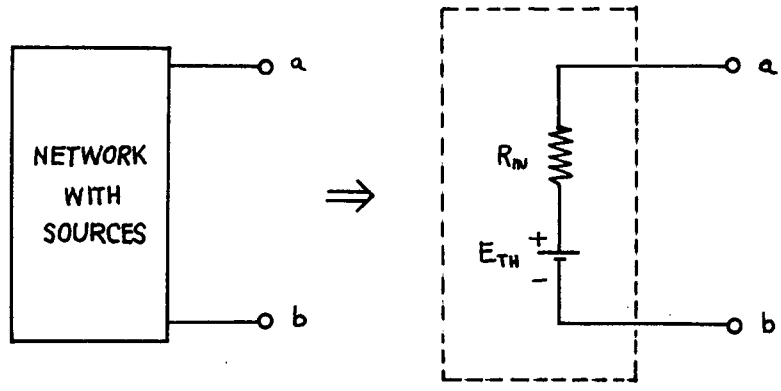
c) Drill holes into it.

Use a: Dremel Mototool 381
Dremel Stand 210
Drills #55 to #60 (for most holes)

When the hole is positioned, the dremel stand pushes the board up against the rotating drill.

THEVENIN'S THEOREM

This theorem states that a network with sources may be replaced by an equivalent source E_{TH} in series with an equivalent resistor R_{in}.



The equivalent circuit will perform just as the original one. Therefore, a load placed between points "a" and "b" will have the same voltages and currents regardless of the circuit that drives it, i. e. whether driven by the original circuit or by its equivalent.

The equivalent source E_{TH} and the equivalent resistor R_{in} are defined as follows:

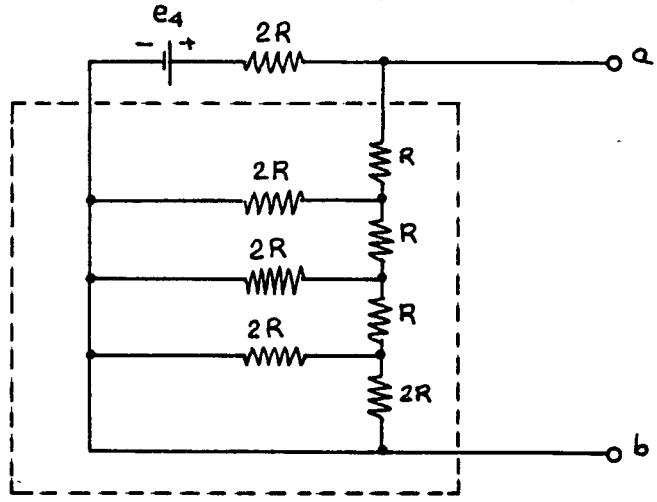
E_{TH} = Open Circuit Voltage between points "a" and "b". It can be measured or calculated.

R_{in} = Resistance between points "a" and "b", provided all the active sources of the original network are removed. This means that all the voltage sources must be short circuited, and all the current sources must be open circuited. R_{in} can be measured or calculated.

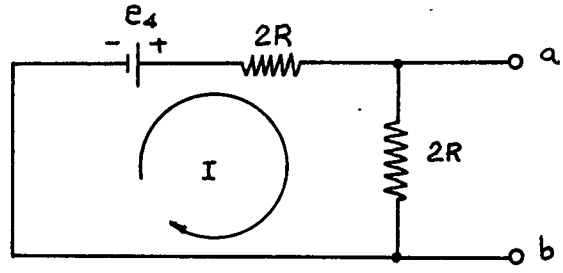
The advantages of the equivalent circuit are that it facilitates the calculation of voltages and currents on any given load, by replacing complex looking configurations with a single voltage source in series with a single resistor.

EXAMPLE 1.- Determine the equivalent circuit for the following network:

(See section on Digital to Analog Conversion).



SOLUTION.- The dashed section can be reduced by combining resistors in parallel and series:

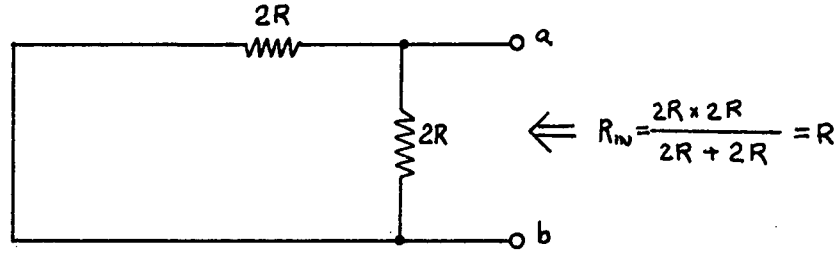


Now we apply Thevenin's Theorem.

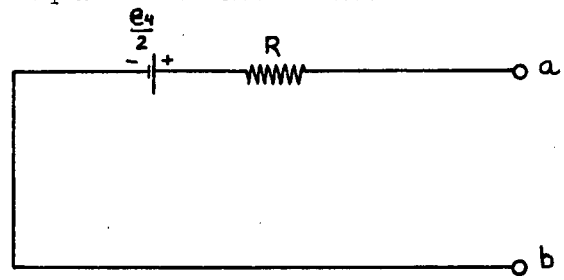
a) The open circuit voltage, across points "a" and "b":

$$E_{TH} = I\,(2R) = \frac{e_4}{2R + 2R}\,(2R) = \frac{e_4}{4R}\,2R = \frac{e_4}{2}$$

b) The resistance R_{in} between points "a" and "b", when the voltage source is shorted:

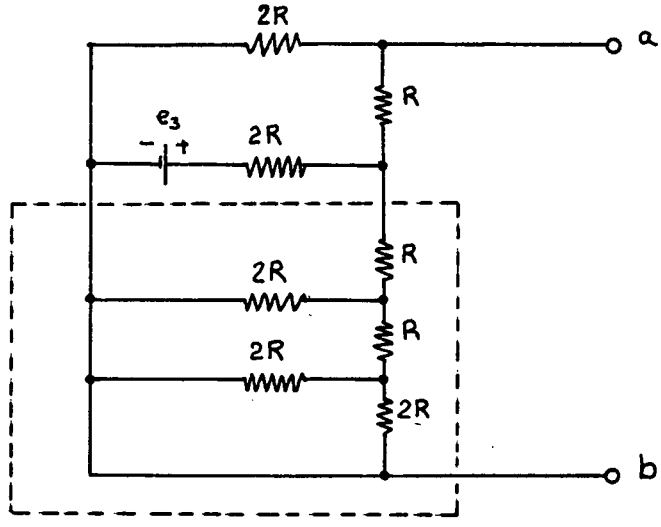


Therefore, the equivalent circuit is:

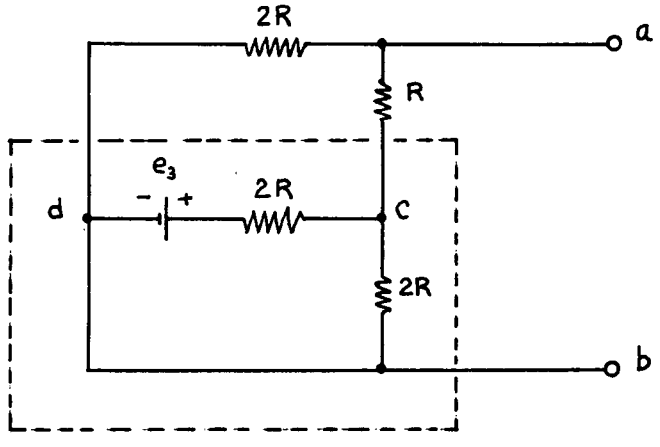


EXAMPLE 2.- Determine the equivalent circuit of the following network.

(See section on Digital to Analog Conversion)



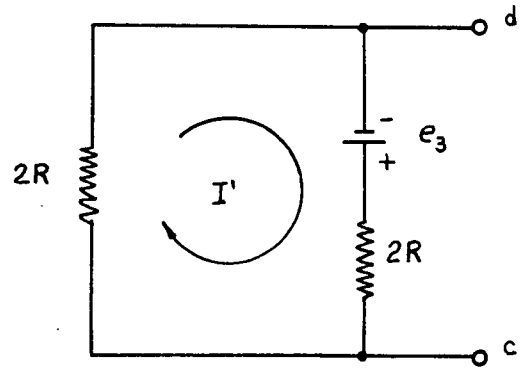
SOLUTION.- The dashed section can be reduced by combining resistors in parallel and series:



The equivalent circuit between points "a" and "b" is easier to calculate, if we know the equivalent circuit between points "c" and "d". This means we can apply Thevenin's Theorem to obtain intermediate results, before the determination of the system's

overall equivalent.

The circuit between points "c" and "d", shown above in dashed lines is:

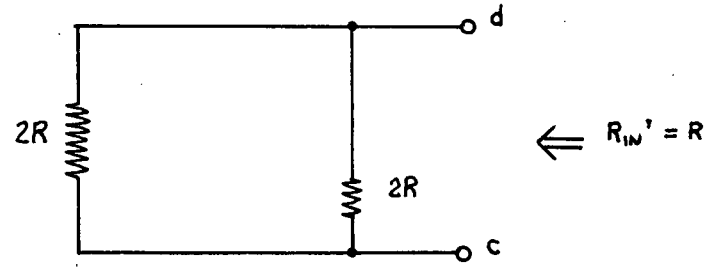


Applying Thevenin's Theorem to above circuit:

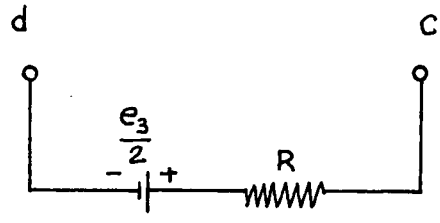
a) The open circuit voltage across points "c" and "d" is:

$$E_{TH}' = I' (2R) = \frac{e_3}{2R + 2R} (2R) = \frac{e_3}{4R} (2R) = \frac{e_3}{2}$$

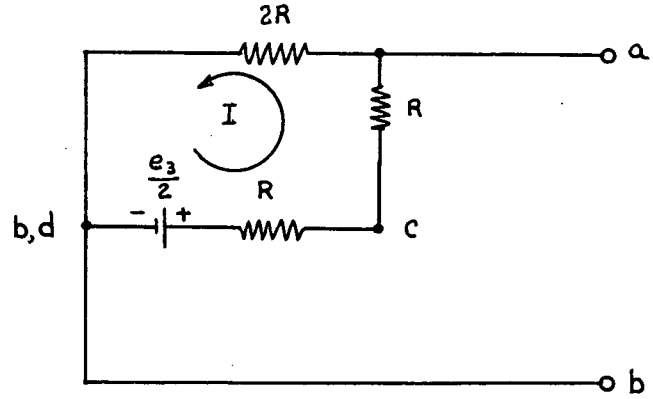
b) The resistance R_{in}' between points "c" and "d" when e_3 is shorted:



The circuit between points "c" and "d" becomes:



Therefore, incorporating above partial equivalent circuit into our overall circuit:

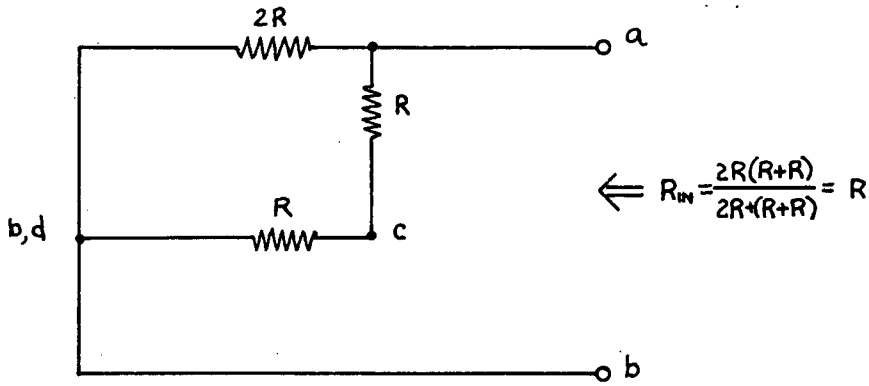


Applying Thevenin's Theorem once more:

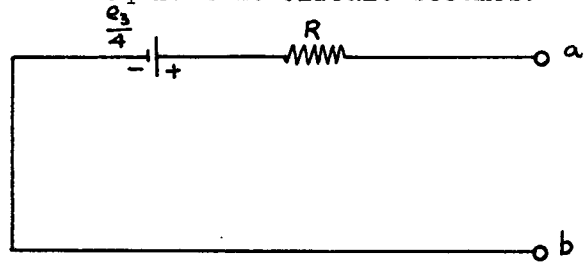
c) The open circuit voltage across points "a" and "b" is:

$$E_{TH} = I\ (2R) = \frac{\frac{e_3}{2}}{R + R + 2R}\ (2R) = \frac{e_3}{4}$$

d) The resistance R_{in} between points "a" and "b" when $\frac{e_3}{4}$ is shorted:



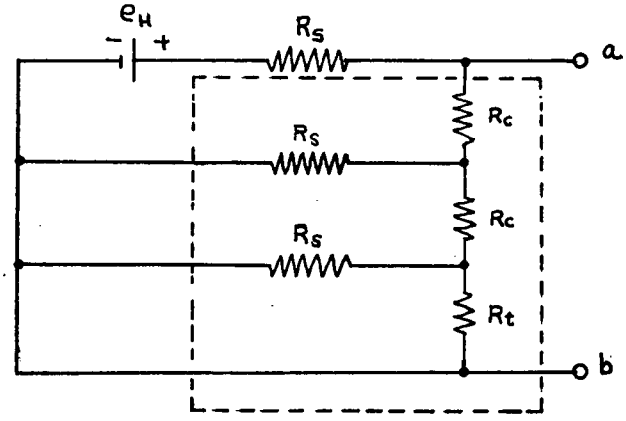
Therefore, the total equivalent circuit becomes:



NOTE.- The voltage across points "a" and "b" can be calculated directly by OHM'S LAW MATRIX, see the corresponding appendix.

EXAMPLE 3.- Determine the equivalent circuit for the following network.

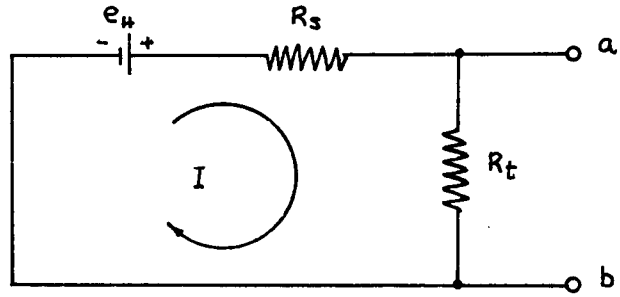
(See the section on the BCD Ladder Attenuator).



SOLUTION.- The dashed section can be reduced using the basic ladder network relationship:

$$R_t = \frac{R_t R_s}{R_t + R_s} + R_c$$

Then, above circuit becomes:

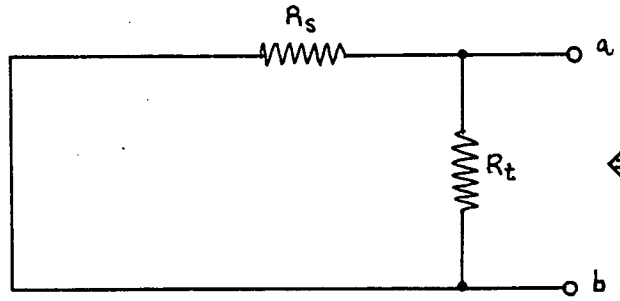


Now we apply Thevenin's Theorem.

a) The open circuit voltage, across points "a" and "b":

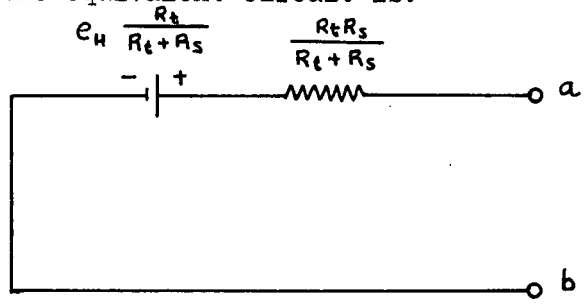
$$E_{TH} = I\ (R_t) = e_H \frac{R_t}{R_t + R_s}$$

b) The resistance R_{in} between points "a" and "b", when the voltage source is shorted:



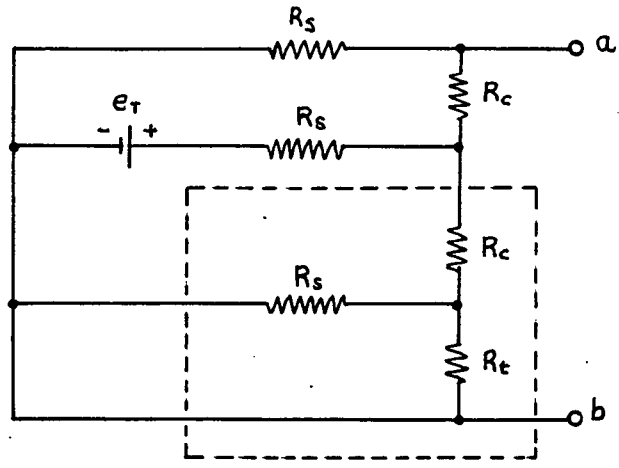
$$\Leftarrow R_{IN} = \frac{R_t R_s}{R_t + R_s}$$

Therefore, the equivalent circuit is:

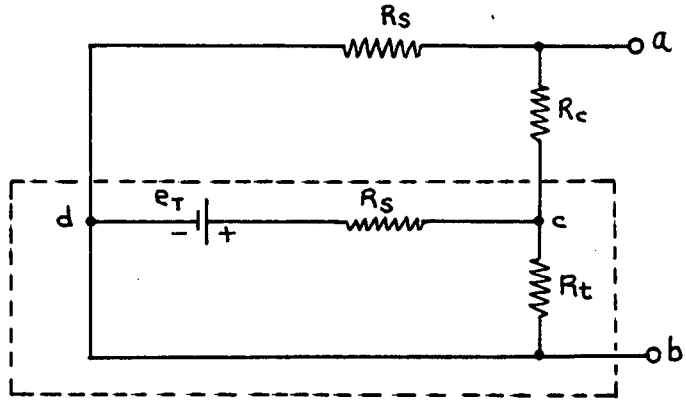


EXAMPLE 4.- Determine the equivalent circuit for the following network:

(See the section on the BCD Ladder Attenuator).

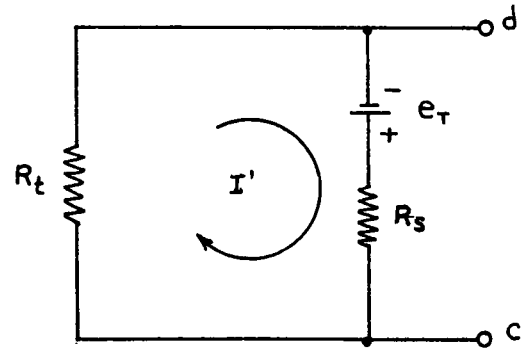


SOLUTION.- Using the basic ladder network relationship (see previous example), the dashed portion reduces to R_t, and above circuit simplifies into the following one:



Before calculating the equivalent circuit, between points "a" and "b", we can reduce above dashed section by an intermediate application of Thevenin's Theorem.

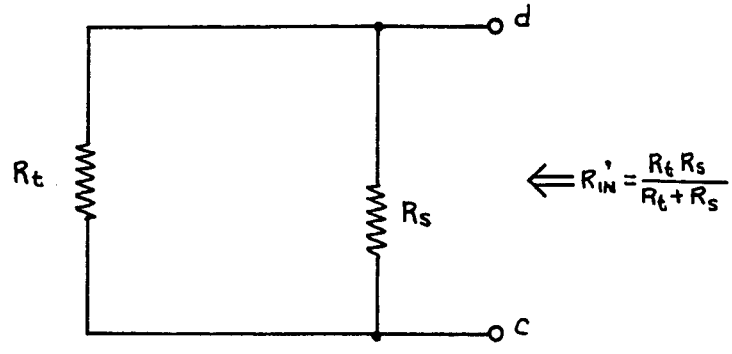
Therefore, considering only the dashed section, between points "c" and "d":



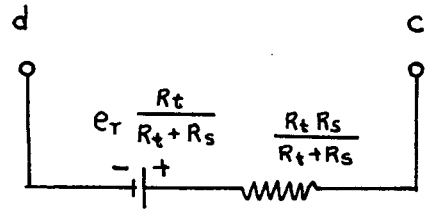
a) The open circuit voltage across points "c" and "d" is:

$$E_{TH}' = I' (R_t) = \frac{e_T}{R_t + R_s} (R_t)$$

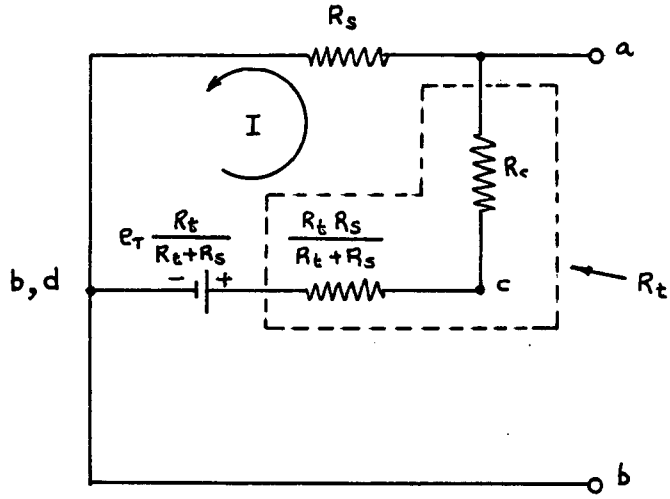
b) The resistance R_{in}' between points "c" and "d", when e_T is shorted:



Therefore, the circuit between points "c" and "d" becomes:



Incorporating above circuit into our overall configuration:

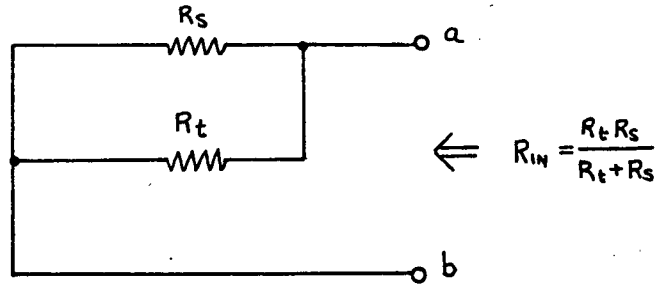


Using Thevenin's Theorem once more on above circuit:

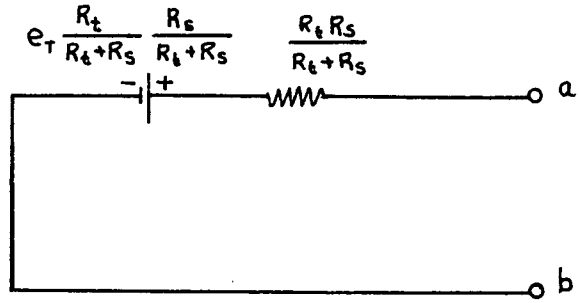
c) The open circuit voltage across points "a" and "b" is:

$$E_{TH} = I\,(R_s) = \frac{e_T \dfrac{R_t}{R_t+R_s}}{R_t + R_s} R_s = e_T \frac{R_t}{R_t + R_s} \frac{R_s}{R_t + R_s}$$

d) The resistance R_{in} between points "a" and "b" when the source $e_T \dfrac{R_t}{R_t + R_s}$ is shorted is:



Therefore, the total equivalent circuit becomes:



SOLUTION OF CIRCUITS USING THE OHM'S LAW MATRIX

A4

This method permits one to order the data of any electrical circuit into mathematically meaningful arrays.

The resulting data arrays make up a matrix equation. I refer to this equation as the Ohm's Law Matrix. It is another way of writing the simultaneous equations that describe a given electrical circuit.

The Ohm's Law Matrix may be solved directly or it may be rewritten first as a set of simultaneous equations. Any method to solve simultaneous equations may be used to solve for the unknowns. In the examples that follow, the method of determinants is employed.

Due to the mechanical nature involved in the solution by determinants, any microprocessor or programmable pocket calculator may be advantageously used.

The Ohm's Law Matrix is made up of three arrays of data, its format looks like the regular Ohm's Law:

$$(R)\ (I) = (E)$$

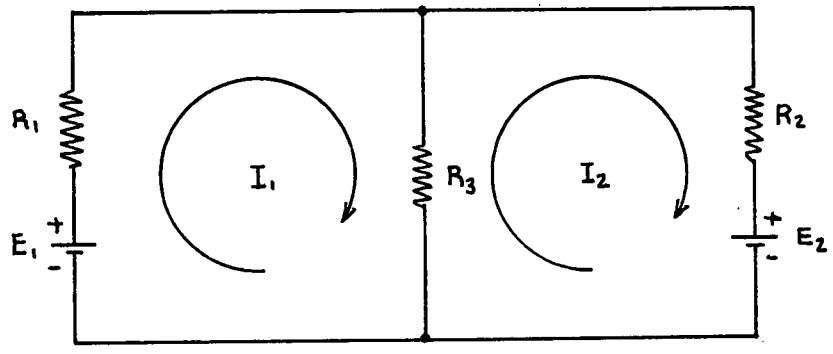
Where: (R) is the array of the resistive data of a given circuit.

(I) is the array of the loop currents in that circuit.

(E) is the array of the voltage sources in the circuit.

The Ohm's Law Matrix combines loop analysis techniques, Kirchhoff's Voltage and Current Laws, plus Ohm's Law. Later on, in this section, it will be shown how to derive the Ohm's Law Matrix. However, first we will show how to transpose electrical data into arrays and then solve for the unknowns.

Any electrical circuit, with one, two or more loops, can be solved using the Ohm's Law Matrix. Consider the two loop system shown below:



SOLUTION

1.- Define the two loop currents as I_1 and I_2, always in the clockwise direction.

NOTE.- If any current or all currents happen to be assigned the wrong direction, their resulting numerical value will be negative. This negative answer indicates that their direction needs to be reversed.

2.- The Ohm's Law Matrix for two loops is stated as follows:

$$\begin{pmatrix} R_{11} & -R_{12} \\ -R_{21} & R_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} E_1 \\ E_2 \end{pmatrix}$$

Where: a) R_{11} is the total resistance in loop 1. For above example:

$$R_{11} = R_1 + R_3$$

R_{22} is the total resistance in loop 2. For above example:

$$R_{22} = R_2 + R_3$$

$(-R_{12})$ or $(-R_{21})$ is the resistance common to both loops. For above example:

$$(-R_{12}) = (-R_{21}) = (-R_3)$$

NOTE.- In the matrix equation, the resistance common to both loops is always written as negative. This is done to account for the direction of the loop currents through this element. For one loop, the voltage due to one loop current will be always positive, whereas for the other loop, it will be always negative, because the second loop current will oppose the first one, (loop currents were defined to be CW).

b) The sign for sources E_1 and E_2 is defined as follows:
It is considered as positive, if the corresponding loop current sees it as a voltage rise, i. e. if the current moves from the negative terminal to the positive terminal. Otherwise, it is considered as negative, because the loop current will see it as an effective voltage drop.

3.- Above Ohm's Law Matrix can easily be converted into simultanous equations by manipulating the array terms as follows:

$$R_{11}\ I_1 - R_{12}\ I_2 = E_1$$
$$-R_{21}\ I_1 + R_{22}\ I_2 = E_2$$

4.- The solutions for the unknowns, in above case I_1 and I_2, can be obtained by several methods. The method of determinants is used below. This method can be programmed into a microprocessor or a programmable pocket calculator.

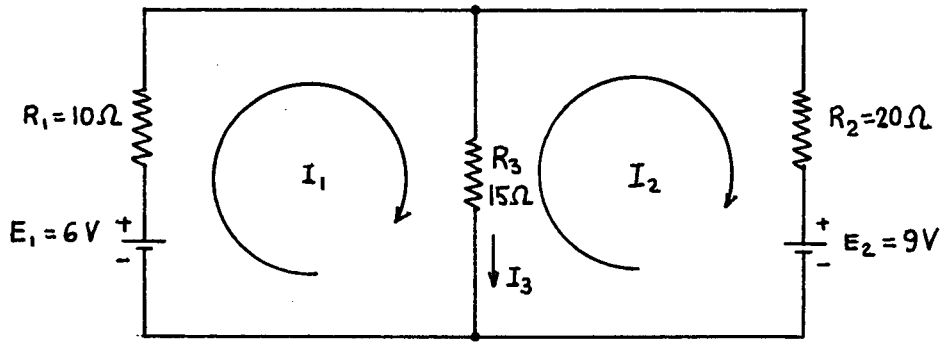
$$I_1 = \frac{\begin{vmatrix} E_1 & -R_{12} \\ E_2 & R_{22} \end{vmatrix}}{\begin{vmatrix} R_{11} & -R_{12} \\ -R_{21} & R_{22} \end{vmatrix}} = \frac{(E_1)(R_{22}) - (E_2)(-R_{12})}{(R_{11})(R_{22})-(-R_{21})(-R_{12})}$$

$$I_2 = \frac{\begin{vmatrix} R_{11} & E_1 \\ -R_{21} & E_2 \end{vmatrix}}{\begin{vmatrix} R_{11} & -R_{12} \\ -R_{21} & R_{22} \end{vmatrix}} = \frac{(R_{11})(E_2) - (-R_{21})(E_1)}{(R_{11})(R_{22}) - (-R_{21})(-R_{12})}$$

5.- Once the loop currents are known, then the currents through the common elements may be calculated. They will be the difference of the loop currents that flow through the same common element. For above example, if I_3 is considered moving downwards, it will be:

$$I_3 = I_1 - I_2$$

EXAMPLE 1.- Determine the currents through each of the resistors R_1, R_2 and R_3 in the following circuit.



SOLUTION

1.- Define the loop currents I_1 and I_2 in the clockwise direction, and mark them on the circuit as shown above.

2.- For above circuit, its Ohm's Law Matrix is:

$$\begin{bmatrix} 10 + 15 & -15 \\ -15 & 15 + 20 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} +6 \\ -9 \end{bmatrix}$$

3.- The corresponding simultaneous equations are:

$$25\ I_1 - 15\ I_2 = +\ 6$$

$$-15\ I_1 + 35\ I_2 = -\ 9$$

4.- The solution by determinants is:

$$I_1 = \frac{\begin{vmatrix} 6 & -15 \\ -9 & 35 \end{vmatrix}}{\begin{vmatrix} 25 & -15 \\ -15 & 35 \end{vmatrix}} = \frac{(6)(35) - (-9)(-15)}{(25)(35) - (-15)(-15)} = \frac{75}{650} = + 0.115 \text{ A}$$

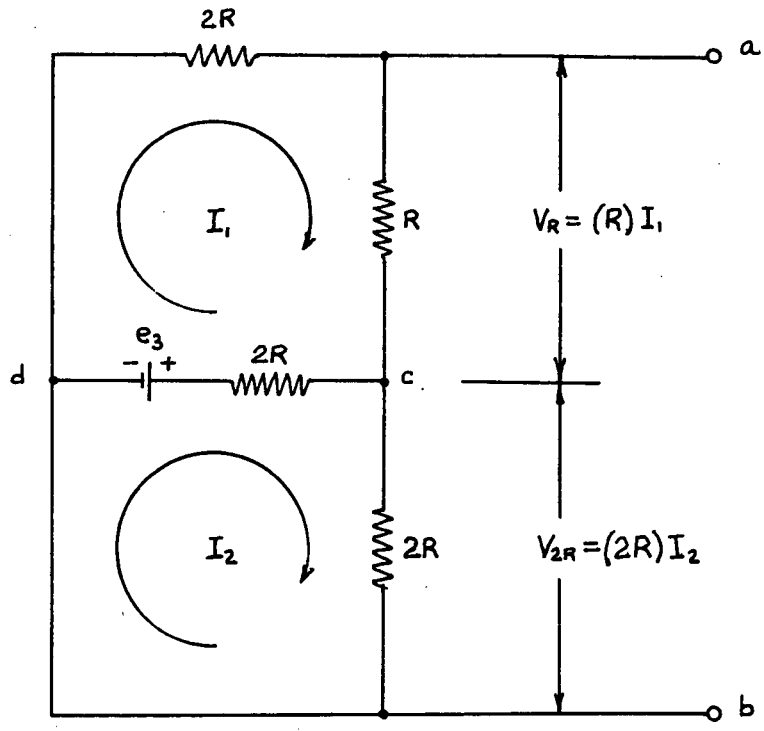
$$I_2 = \frac{\begin{vmatrix} 25 & 6 \\ -15 & -9 \end{vmatrix}}{650} = \frac{(25)(-9) - (-15)(6)}{650} = \frac{-135}{650} = - 0.208 \text{ A}$$

5.- From above results:

$$I_3 = I_1 - I_2 = + 0.115 - (-0.208) = 0.323 \text{ A}$$

Notice that I_2 is negative. This means that the direction of I_2 is opposite to the one shown on above circuit.

EXAMPLE 2.- Determine the voltage across points "a" and "b" in the next circuit. Notice that this voltage was calculated by Thevenin's Theorem in the corresponding appendix.



SOLUTION

1.- Define the loop currents I_1 and I_2 in the clockwise direction, and mark them on the circuit as already done above.

2.- The Ohm's Law Matrix is:

$$\begin{bmatrix} 5R & -2R \\ -2R & 4R \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} -e_3 \\ e_3 \end{bmatrix}$$

3.- Above matrix may be rewritten as a set of simultaneous equations:

$$(5R)\ I_1 - (2R)\ I_2 = -e_3$$
$$(-2R)\ I_1 + (4R)\ I_2 = e_3$$

4.- While solving for the unknowns by determinants, we can calculate the denominator determinant first:

$$\Delta = \begin{vmatrix} 5R & -2R \\ -2R & 4R \end{vmatrix} = 20\ R^2 - 4\ R^2 = 16\ R^2$$

The loop currents I_1 and I_2 are calculated next:

$$I_1 = \frac{\begin{vmatrix} -e_3 & -2R \\ e_3 & 4R \end{vmatrix}}{16R^2} = \frac{-4Re_3 + 2Re_3}{16R^2} = \frac{-2Re_3}{16R^2} = -\frac{e_3}{8R}$$

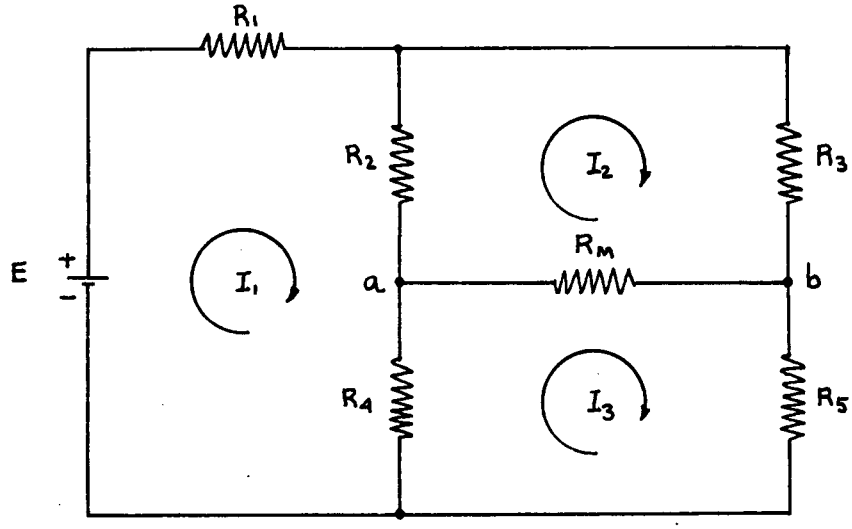
$$I_2 = \frac{\begin{vmatrix} 5R & -e_3 \\ -2R & e_3 \end{vmatrix}}{16R^2} = \frac{5Re_3 - 2Re_3}{16R^2} = \frac{3Re_3}{16R^2} = \frac{3e_3}{16R}$$

5.- Therefore:

$$e_{ab} = V_R + V_{2R} = (R)\ I_1 + (2R)\ I_2 = (R)\left(-\frac{e_3}{8R}\right) + (2R)\ \frac{3e_3}{16R}$$
$$= -\frac{e_3}{8} + \frac{3e_3}{8} = \frac{2e_3}{8}$$
$$= \frac{e_3}{4}$$

OHM'S LAW MATRIX FOR A THREE LOOP SYSTEM

Consider the three loop circuit shown below. Assume that we want to know the expression for the voltage between the points "a" and "b".



SOLUTION

1.- Define the loop currents I_1, I_2 and I_3 in the clockwise direction as shown above.

2.- Above system is described by the general Ohm's Law Matrix:

$$\begin{bmatrix} R_{11} & -R_{12} & -R_{13} \\ -R_{21} & R_{22} & -R_{23} \\ -R_{31} & -R_{32} & R_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

Where: R_{11} represents the total resistance in loop 1

R_{22} represents the total resistance in loop 2

R_{33} represents the total resistance in loop 3

$(-R_{12})$ or $(-R_{21})$ represents the resistance common to loops 1 and 2

$(-R_{13})$ or $(-R_{31})$ represents the resistance common to loops 1 and 3

$(-R_{23})$ or $(-R_{32})$ represents the resistance common to loops 2 and 3

E_1 represents the algebraic sum of the voltage sources in loop 1.

E_2 represents the algebraic sum of the voltage sources in loop 2.

E_3 represents the algebraic sum of the voltage sources in loop 3.

Transposing the electrical data from above circuit into the Ohm's Law Matrix yields:

$$\begin{bmatrix} R_1 + R_2 + R_4 & - R_2 & - R_4 \\ - R_2 & R_2 + R_3 + R_M & - R_M \\ - R_4 & - R_M & R_4 + R_M + R_5 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} + E \\ 0 \\ 0 \end{bmatrix}$$

3.- If desired, we can write the corresponding simultaneous equations:

$$\begin{aligned} (R_1 + R_2 + R_4)\, I_1 \quad & -R_2\, I_2 \quad & -R_4\, I_3 &= + E \\ -R_2\, I_1 + (R_2 + R_3 + R_M)\, I_2 \quad & - & R_M\, I_3 &= 0 \\ -R_4\, I_1 \quad & -R_M\, I_2 + (R_4 + R_M + R_5)\, I_3 &= 0 \end{aligned}$$

4.- Above literal values may be substituted into the general solution by determinants, given below:

$$\Delta = \begin{vmatrix} R_{11} & -R_{12} & -R_{13} \\ -R_{21} & R_{22} & -R_{23} \\ -R_{31} & -R_{32} & R_{33} \end{vmatrix} =$$

$$= ((R_{11})(R_{22})(R_{33}) + (-R_{12})(-R_{23})(-R_{31}) + (-R_{13})(-R_{21})(-R_{32})) -$$
$$-((-R_{31})(R_{22})(-R_{13}) + (-R_{32})(-R_{23})(R_{11}) + (R_{33})(-R_{21})(-R_{12}))$$

$$I_1 = \frac{\begin{vmatrix} E_1 & -R_{12} & -R_{13} \\ E_2 & R_{22} & -R_{23} \\ E_3 & -R_{32} & R_{33} \end{vmatrix}}{\Delta} =$$

$$= \frac{\begin{array}{l} ((E_1)(R_{22})(R_{33}) + (-R_{12})(-R_{23})(E_3) + (-R_{13})(E_2)(-R_{32})) - \\ -((E_3)(R_{22})(-R_{13}) + (-R_{32})(-R_{23})(E_1) + (R_{33})(E_2)(-R_{12})) \end{array}}{\Delta}$$

$$I_2 = \frac{\begin{vmatrix} R_{11} & E_1 & -R_{13} \\ -R_{21} & E_2 & -R_{23} \\ -R_{31} & E_3 & R_{33} \end{vmatrix}}{\Delta}$$

$$= \frac{\begin{array}{l}((R_{11})(E_2)(R_{33}) + (E_1)(-R_{23})(-R_{31}) + (-R_{13})(-R_{21})(E_3)) - \\ -((-R_{31})(E_2)(-R_{13}) + (E_3)(-R_{23})(R_{11}) + (R_{33})(-R_{21})(E_1))\end{array}}{\Delta}$$

$$I_3 = \frac{\begin{vmatrix} R_{11} & -R_{12} & E_1 \\ -R_{21} & R_{22} & E_2 \\ -R_{31} & -R_{32} & E_3 \end{vmatrix}}{\Delta}$$

$$= \frac{\begin{array}{l}((R_{11})(R_{22})(E_3) + (-R_{12})(E_2)(-R_{31}) + (E_1)(-R_{21})(-R_{32})) - \\ -((-R_{31})(R_{22})(E_1) + (-R_{32})(E_2)(R_{11}) + (E_3)(-R_{21})(-R_{12}))\end{array}}{\Delta}$$

5.- From Kirchhoff's Current Law: $I_M = I_2 - I_3$

Therefore: $V_{ab} = I_M R_M$

NOTE.- The Ohm's Law Matrix holds true for any number of loops. In actual practice, the largest number of loops found in most electrical circuits is three. However, when a four loop system is found, the solution by determinants calls for the use of cofactors.

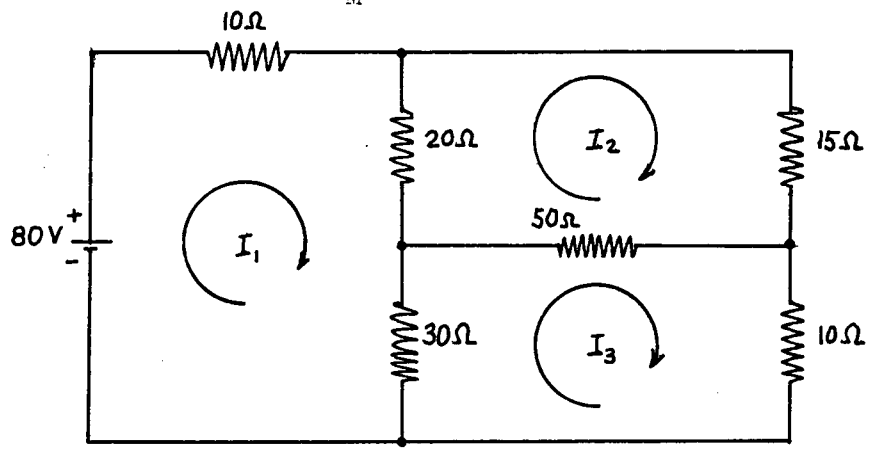
Another way to solve four simultaneous equations is the use of Gauss's Elimination Method, also known as the Addition and Subtraction Method, and is suitable for computer programming.

An alternate procedure to solve a four loop system, is to reduce it into a three loop system by a careful application of Thevenin's Theorem.

Whichever is the chosen procedure to solve simultaneous equations, the Ohm's Law Matrix is always a valid representation of the electrical system or systems.

The following examples have been solved using the Ohm's Law Matrix and a computer. The computer program was based on the previous determinant equations.

EXAMPLE 3.- Determine the current I_M in the following circuit.



SOLUTION

1.- Define the loop currents I_1, I_2, and I_3 in the clockwise direction as shown above.

2.- The corresponding Ohm's Law Matrix is:

$$\begin{pmatrix} 60 & -20 & -30 \\ -20 & 85 & -50 \\ -30 & -50 & 90 \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} = \begin{pmatrix} 80 \\ 0 \\ 0 \end{pmatrix}$$

4.- The computer solutions to above matrix are:

$$I_1 = 3.0183 \text{ A}$$

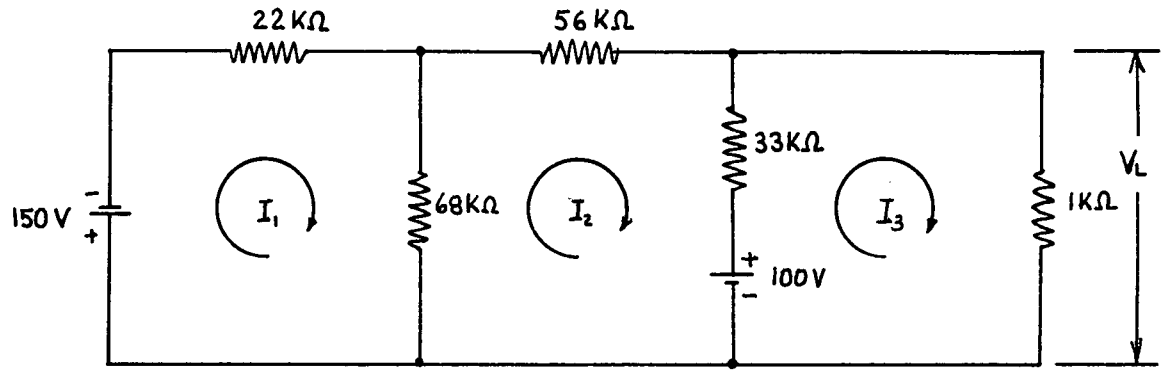
$$I_2 = 1.934 \text{ A}$$

$$I_3 = 2.0805 \text{ A}$$

5.- By Kirchhoff's Current Law:

$$I_M = I_3 - I_2 = 0.1465 \text{ A}$$

EXAMPLE 4.- Determine the load voltage V_L in the following circuit:



SOLUTION

1.- Define the loop currents I_1, I_2 and I_3 in the clockwise direction as shown above.

2.- The Ohm's Law Matrix is:

$$\begin{pmatrix} 90k\Omega & -68k\Omega & 0 \\ -68k\Omega & 157k\Omega & -33k\Omega \\ 0 & -33k\Omega & 34k\Omega \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} = \begin{pmatrix} -150 \\ -100 \\ 100 \end{pmatrix}$$

4.- The computer solutions for the currents are:

$$I_1 = -2.86 \times 10^{-3} \text{ A}$$

$$I_2 = -1.579 \times 10^{-3} \text{ A}$$

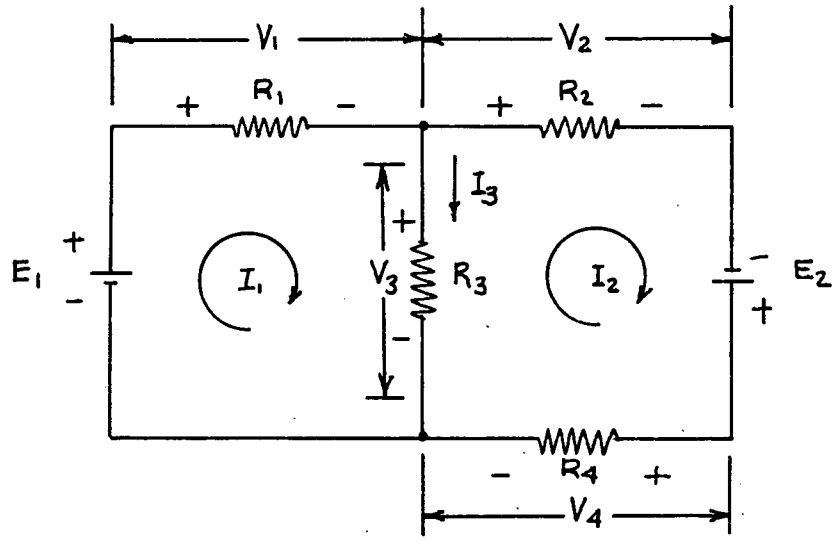
$$I_3 = 1.407 \times 10^{-3} \text{ A}$$

5.- Therefore, by Ohm's Law:

$$V_L = I_3 \times 1 \text{ k}\Omega = 1.407 \text{ V}$$

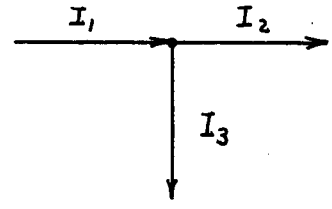
DERIVATION OF THE OHM'S LAW MATRIX

This equation is derived using loop analysis techniques. As a sample circuit, consider the two loop array shown below.



For the above circuit:

1.- Assume loop currents I_1 and I_2, and draw them clockwise (CW). Assume the resulting center branch current I_3 to be moving downwards. Its value is determined by Kirchhoff's Current Law, which states that all the currents entering a connection must be equal to all the currents leaving that connection:

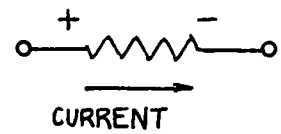


By Kirchhoff's Current Law: $I_1 = I_2 + I_3$

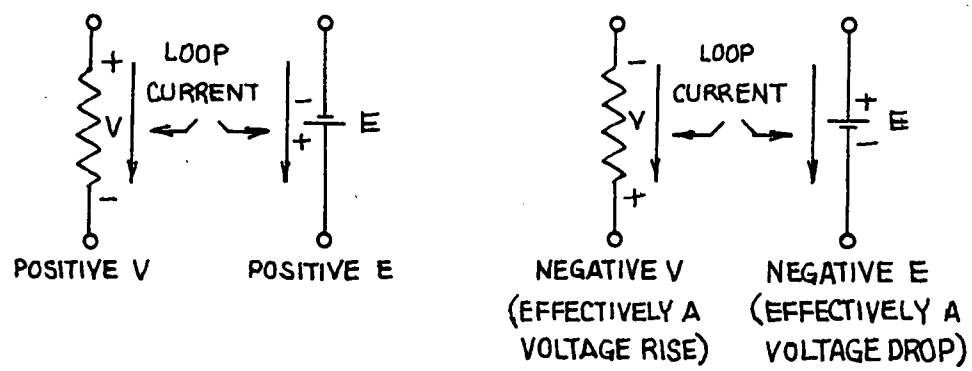
Therefore: $I_3 = I_1 - I_2$

NOTE.- If any or all the current directions were to be assumed in the wrong direction, then, the resulting current(s) will be negative, reminding one to correct its/their direction.

2.- Above currents will produce voltage drops on the resistors in their path. Therefore, assign polarity marks to each resistor, based on the direction assumed for each current, i. e.



3.- Use Kirchhoff's Voltage Law for each of the loops of the circuit configuration. Kirchhoff's Voltage Law states that in a closed loop all the voltage drops must equal all the voltage rises. Voltage signs are assigned, depending on what polarities the loop current encounters in each element, as shown below:



The first loop yields:

$$V_1 + V_3 = E_1 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

The second loop yields:

$$V_2 - V_3 + V_4 = E_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

4.- Apply Ohm's Law to each voltage drop in the above equations:

$$R_1 I_1 + R_3 \overbrace{(I_1 - I_2)}^{I_3} = E_1 \quad \ldots\ldots\ldots\ldots \quad (1')$$

$$R_2 I_2 - R_3 \overbrace{(I_1 - I_2)}^{I_3} + R_4 I_2 = E_2 \quad \ldots\ldots\ldots \quad (2')$$

5.- Factor all the loop currents:

$$(R_1 + R_3)\, I_1 - R_3\, I_2 = E_1 \quad \ldots\ (1")$$

$$-R_3\, I_1 + (R_2 + R_3 + R_4)\, I_2 = E_2 \quad \ldots\ (2")$$

6.- Order the terms of above simultaneous equations into arrays, to yield the following matrix equation:

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 + R_4 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E_1 \\ E_2 \end{bmatrix}$$

7.- We can write above equation in its general form:

$$\begin{bmatrix} R_{11} & -R_{12} \\ -R_{21} & R_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E_1 \\ E_2 \end{bmatrix}$$

Where: R_{11} corresponds to $(R_1 + R_3)$. That is, it is the sum of all the resistance in loop 1.

R_{22} corresponds to $(R_2 + R_3 + R_4)$. That is, it is the sum of all the resistance in loop 2.

$(-R_{12})$ or $(-R_{21})$ corresponds to $(-R_3)$. That is, it is the resistance common to either loop with a negative sign. This sign accounts for the fact that the two loop currents, having all of them been drawn clockwise, produce positive or negative voltages on the same common element. For example, when R_{12} is multiplied by loop current I_1 in loop one, the resulting voltage has a positive value, but, when in loop two, the same R_{12}, when multiplied by the same loop current I_1, results in a negative voltage.

8.- Above matrix equation can be rewritten symbolically as:

$$(R)\ (I) = (E)$$

In either form, I call this expression the OHM'S LAW MATRIX. When this matrix is written as shown above, it is very easy to remember and to use.

Matrices as well as determinants, are arrays of numbers meant to be used as mnemonic aids, that is, aids to the memory. Their purpose is to simplify some equations and their mathematical procedures of solution.